R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

01

+3V/+5V S5 PG.35
+1.05V PG.36
CPU Core PG.40~41
DDR3 PG.37
Charge PG.34
Dis-Charge PG.39
+VGACORE PG.42
+VCCSA PG.38
+1.0V/+1.8/ +3 VGA PG.43

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A
SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL IVY
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8 — AMD Mars / SUN XT 29mm X 29mm TDP 35W / 25W PG.14~20
DDR3 900MHz — VRAM 128Mx16x8,128bit PG.21~22
EDP

FDI DMI

HDD PG.32 — SATA0
ODD PG.32 — SATA1

INTEL PCH
Panther Point
Power : 3.5 Watt
Package : FCBG989
Size : 25 x 25 (mm)
PG.6~11

LVDS — PG.24 — LVDS
DP Port B — PG.25 — HDMI
CRT — PG.23 — CRT

PCI-E x 1 — LANE2 / LANE1
LAN RTL8166 10/100 PG.29
WLAN BT COMBO PG.33 — USB 2.0 PORT10

USB 3.0 — USB3.0 Ports X2 PG.28 — Webcam PG.24
USB 2.0 — PORT1,2 / PORT4 / PORT0,1
USB2.0 Ports PG.28

PCI-E x 1 — LANE3
Accelerometer PG.33 — SMBUS
Card Reader RTS5239 PG.26

KBC EnE KB3940QF A1 PG.30 — PC
KB PG.31 | TP PG.31 | ROM PG.30 | FAN PG.31

AUDIO CODEC ALC 3227 PG.27
Speaker PG.27
HP/MIC PG.28
Analog MIC PG.28

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

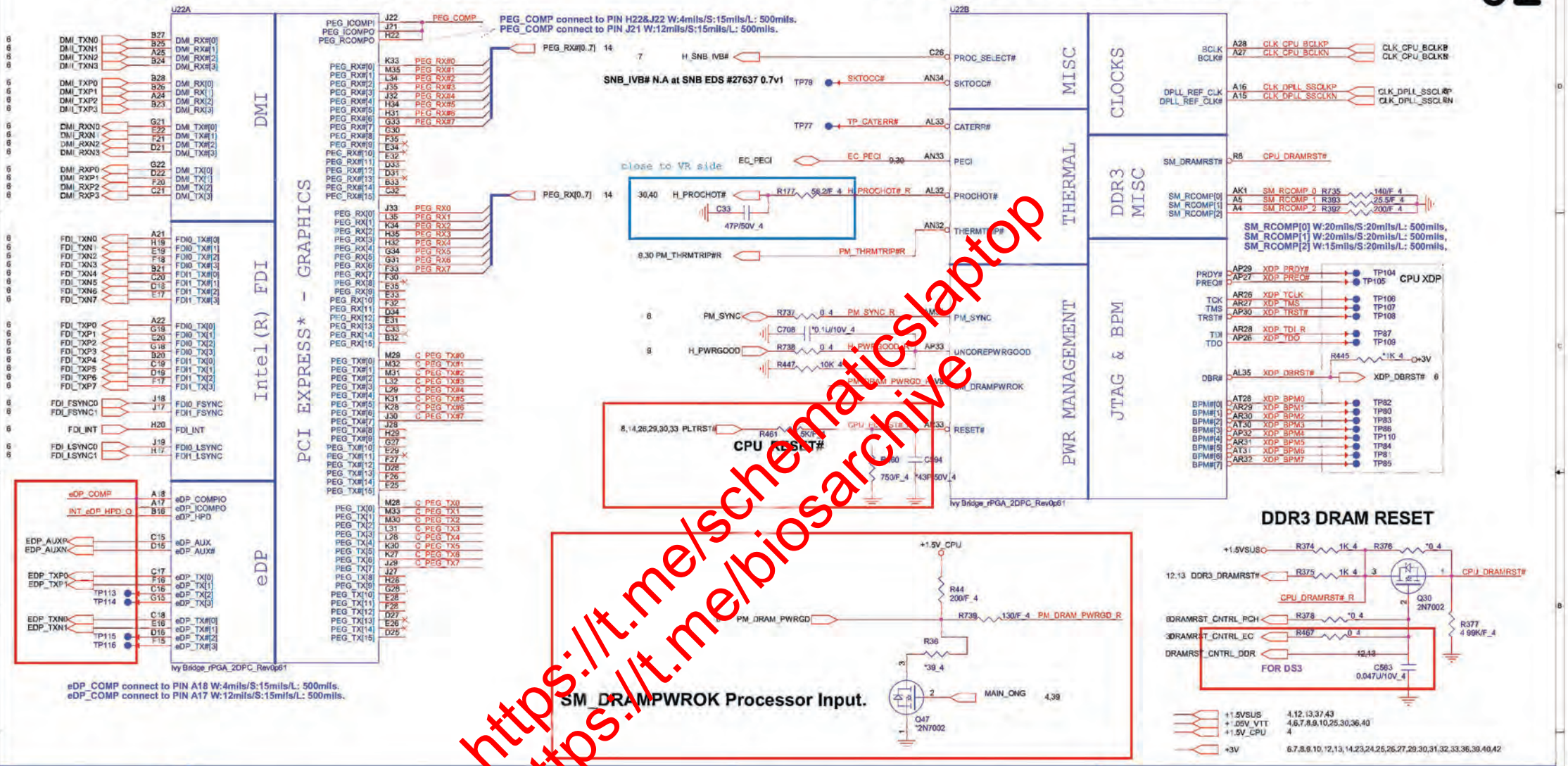
PROJECT : R62
Quanta Computer Inc.

Size: Custom | Document Number: BLOCK DIAGRAM | Rev: 1A
Date: Monday, October 22, 2012 | Sheet 1 of 43

Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

02



PEG x8 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

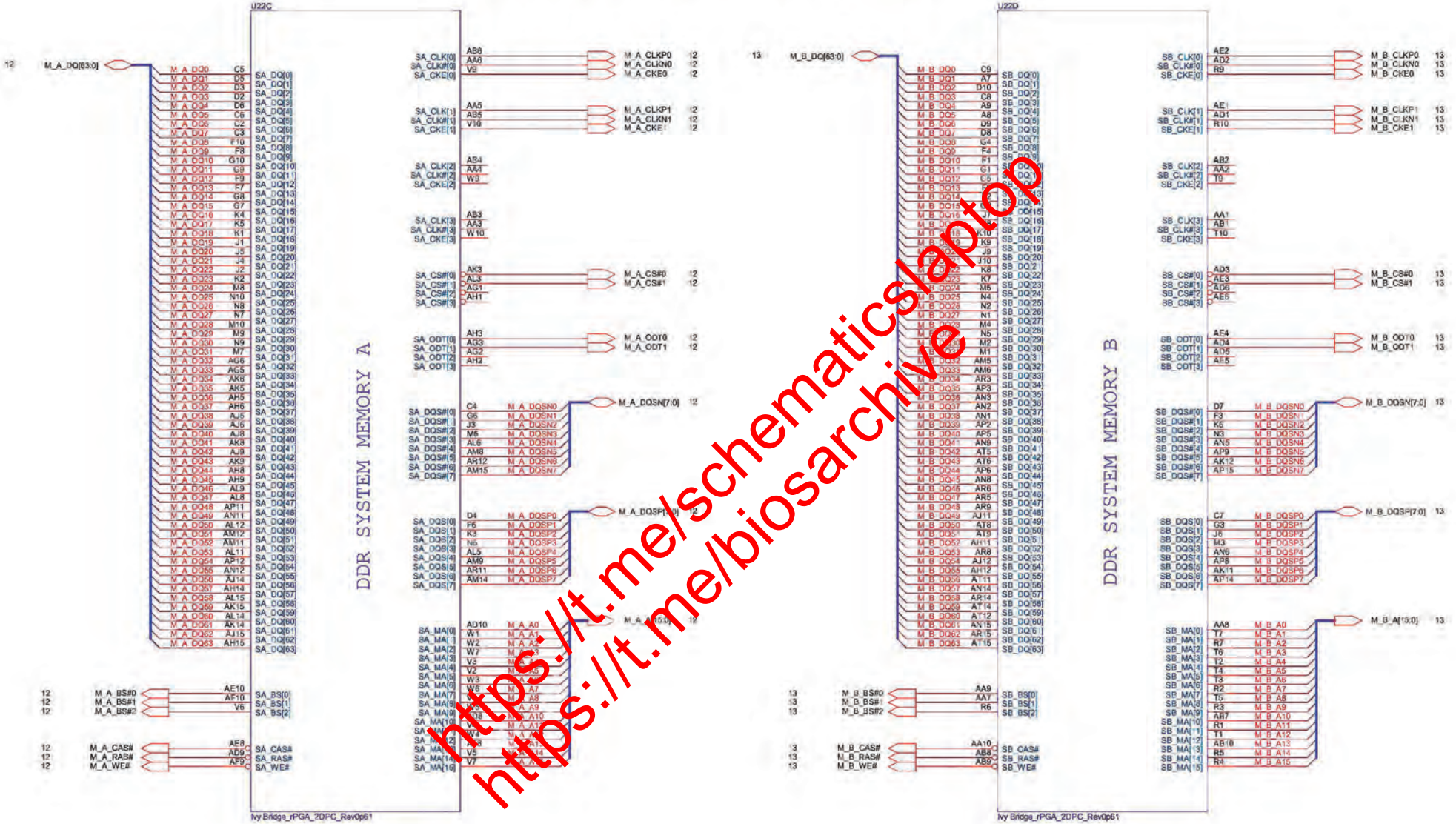
PROJECT : R62
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Monday, October 22, 2012 Sheet 2 of 43

Ivy Bridge Processor (DDR3)



NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: SNB 2/4 (DDR3 I/F)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 3 of 43	

Ivy Bridge Processor (POWER)

POWER

U22F

SNB: 55A
IVY: 55A
+VCC_CORE

CORE SUPPLY

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

PEG AND DDR

SNB: 8.5A
IVY: 8.5A
+1.05V_VTT

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

SVID

VIDALERT#
VIDSCLK
VIDSOUT

SENSE LINES

VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSS_SENSE_VCCIO

Trace Route to Power IC area.

+1.05V_VTT

Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5V	10,12,27,33
+1.8V	7,10,37,43
+VCCSA	38
+1.5VSUS	2,12,13,37,43
+1.5V_CPU	2
+VCC_GFX	41
+1.05V_VTT	2,6,7,8,9,10,25,30,36,40
+VCC_CORE	41

POWER

U22G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX
SNB: 21.5A

GRAPHICS

SNB: 1.5A
+1.8V

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

1.8V RAIL

Ivy Bridge_rPGA_2DPC_Rev0p61

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

VREF

SM_VREF
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ

DDR3 -1.5V RAILS

SNB: 5A
+1.5V_CPU

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

SNB: 6A
+VCCSA

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE
VCCSA_VID[0]
VCCSA_VID[1]
VCCIO_SEL

+1.5V_CPU
R752 *0_8/S
+1.5V
40mile routing

R747 100/F_4 +VCC_GFX
VCC_AXG_SENSE 40
VSS_AXG_SENSE 40
R748 100/F_4

+1.5V_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
+VDDR_REF_CPU
R454 1K/F_4
Q48 2N7002
DDR_VTTREF 12,13,37
R455 3.3K/F_4
MAIND 39
C634 470P/50V_4
SMDDR_VREF_DQ2M3
SMDDR_VREF_DQ1M3
R391 *1K_4
R366 *1K_4

VCCSA_SENSE_R R750 0_4 VCCUSA_SENSE 38
VCCSA_SEL0 38
VCCSA_SEL 38
R71 10K_4
R751 10K_4
R389 0_4 H_VTTVID1 36

SVID CLK

H_CPU_SVIDCLK → VR_SVID_CLK 40

SVID DATA

Place PU resistor close to CPU
R754 130/F_4
H_CPU_SVIDDAT → VR_SVID_DATA 40

SVID ALERT

Place PU resistor close to CPU
C352 0.1U/10V_4
+1.05V_VTT R756 75/F_4
H_CPU_SVIDALRT# R757 43_4 → VR_SVID_ALERT# 40

Layout note: need routing together and ALERT need between CLK and DATA.

CPU VDDQ

+1.5VSUS
+1.5V_CPU
Q10 QM3002N3
R753 220_8
MAIND
C54 *470P/50V_4
Q22 2N7002
MAIN_ONG 2,39
C582 0.1U/10V_4
C580 0.1U/10V_4
C574 0.1U/10V_4
C577 0.1U/10V_4
Placement close to CPU.

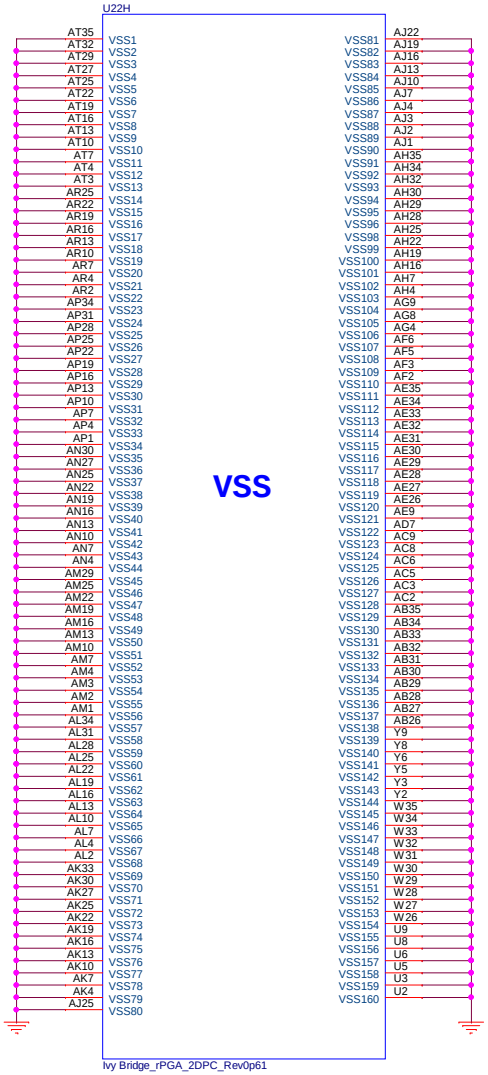
NB5

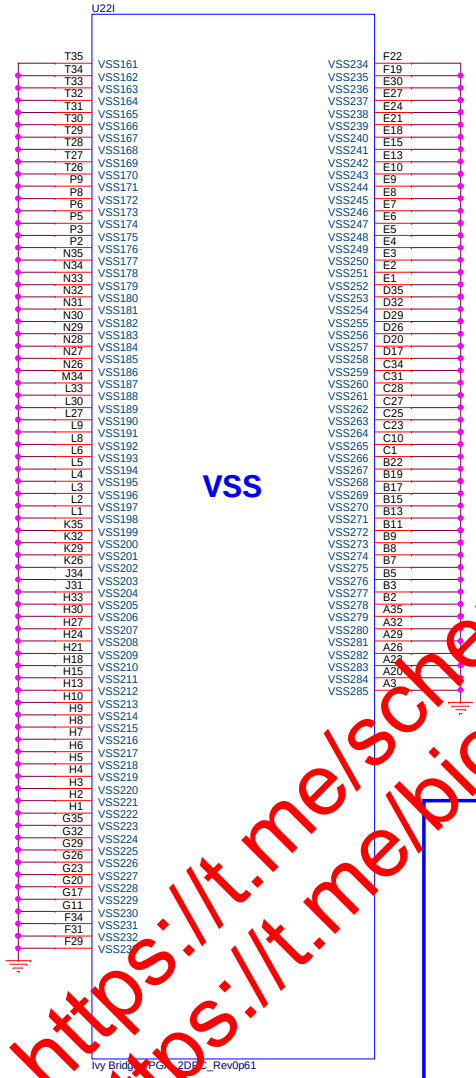
PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Monday, October 22, 2012 Sheet 4 of 43

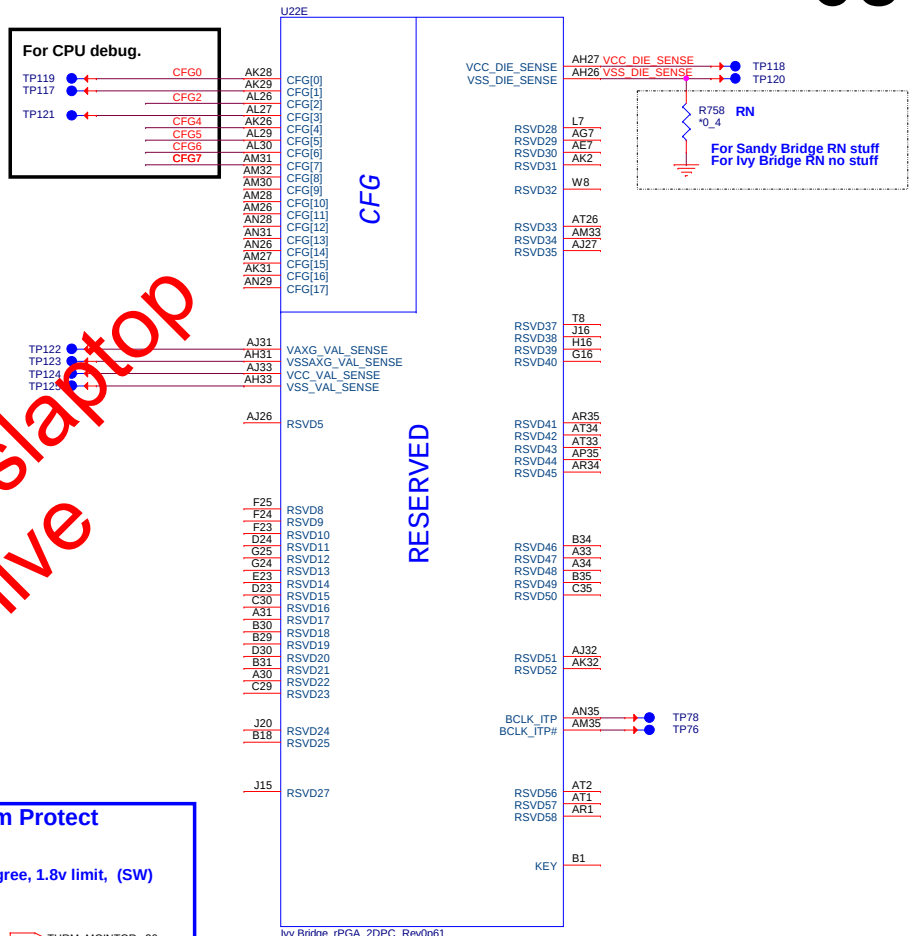
Ivy Bridge Processor (GND)

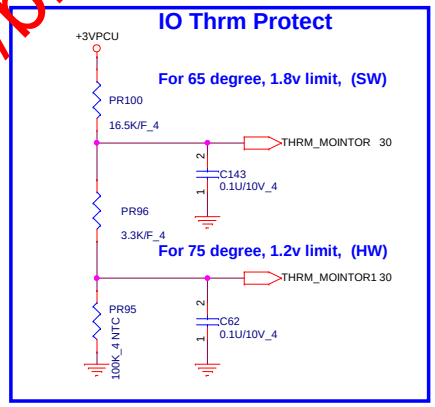




Ivy Bridge Processor (RESERVED, CFG)

05

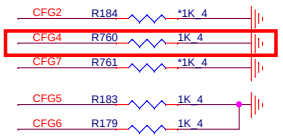




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

Date: Monday, October 22, 2012 Sheet 5 of 43

Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06

U32C

U32D

DMI

FDI

System Power Management

LVDS

Digital Display Interface

CRT

INT. HDMI

for DS3

(+3V)

(+3VS5)

(DSW)

PCH to Res routeing 37.5 ohm impedance.
Res to connect filter routeing 50ohm Impedance. PD Res place close to PCH

Reserve for power on sequence

Reserve from EMI request

PCH Pull-high/low(CLG)

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)

On Die DSW VR Enable

High = Enable (Default)
Low = Disable

CPT_PPT_Rev_0p5

+3V_DEEP_SUS	7,8,9,10,39
+3V_RTC	7,10,25
+1.05V	2,4,7,8,9,10,25,30,36,40
+3VPCU	5,7,25,30,31,33,34,35
+3VS5	7,9,10,33,35,36,39,43
+3V	2,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
+5V	7,10,23,25,27,31,32,33,39

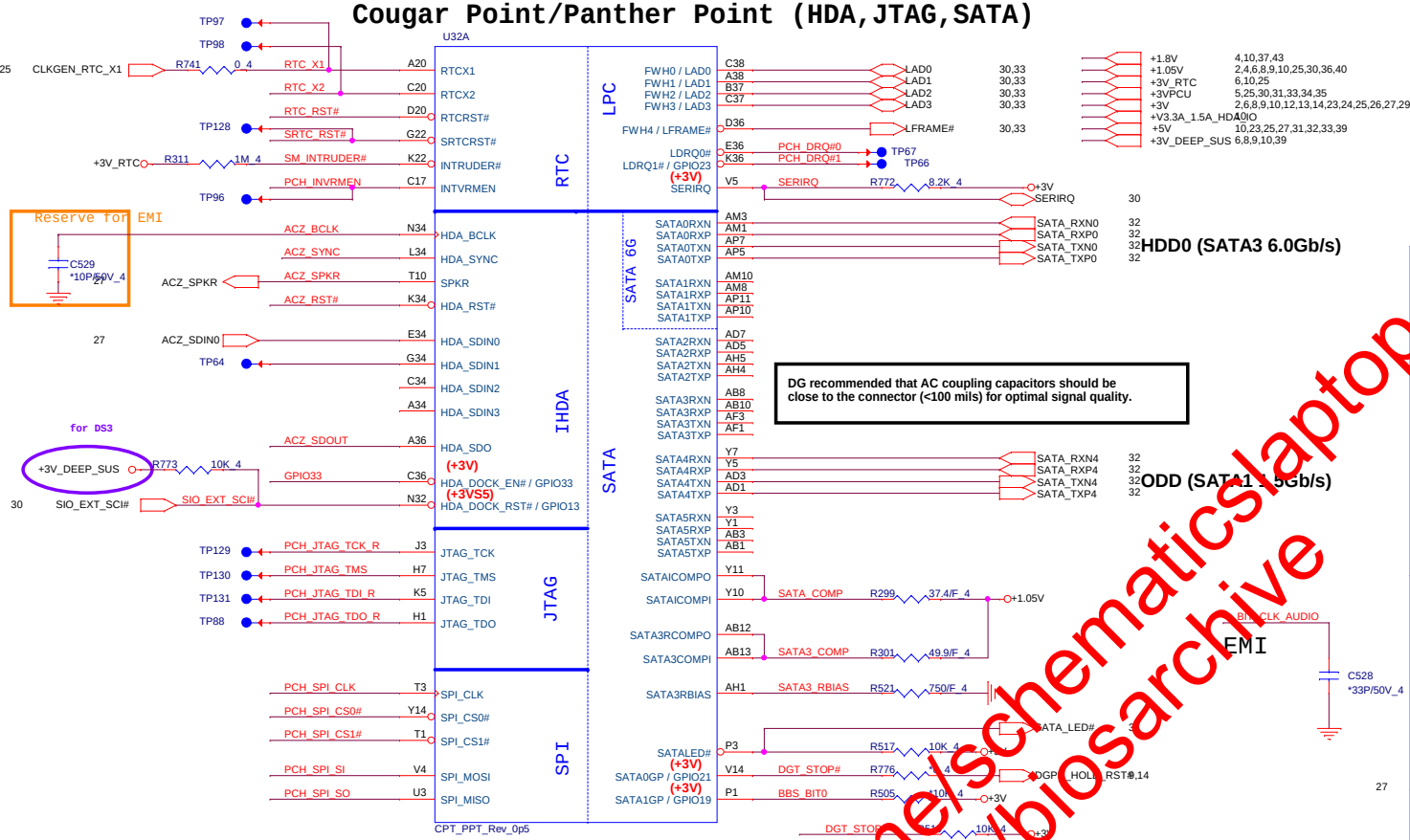
NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Monday, October 22, 2012 Sheet 6 of 43

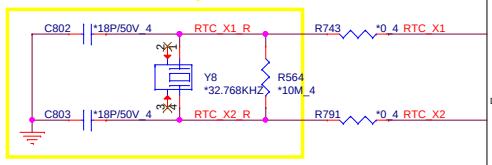
Cougar Point/Panther Point (HDA,JTAG,SATA)



07

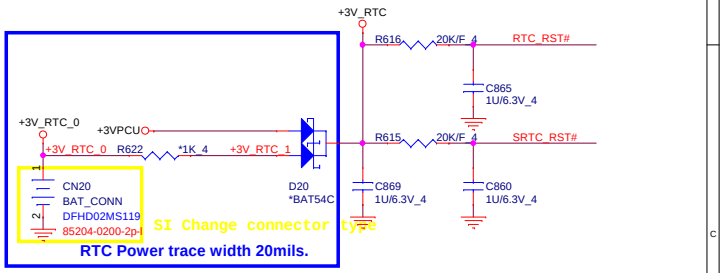
RTC Clock 32.768KHz

SI DEL reserve parts

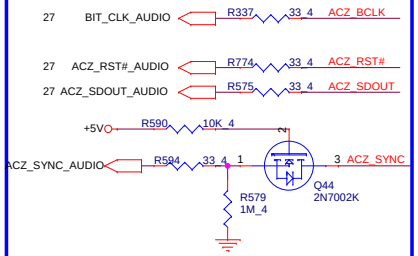


RTC Circuitry(RTC)

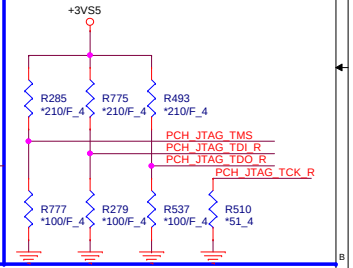
30mils



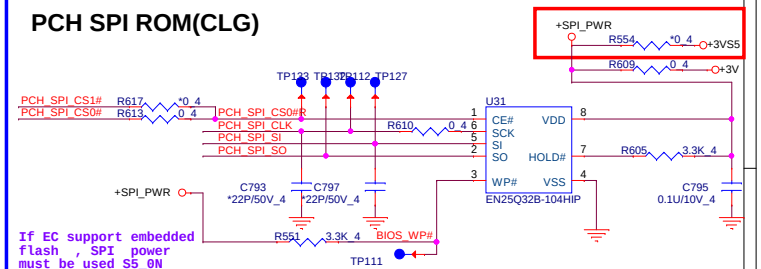
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
PMC	4MB	AKE39ZN0500 (PM25LQ032C-BCE)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R595 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0_4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 0 / 0 / SPI 0 / 1 / PCI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R782 *1K_4 BBS_BIT0 R585 *1K_4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R783 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R526 2.2K_4 R546 1K_4 NV_CLE 9 H_SNB_IVB# 2 Sandy/Ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO R784 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overridden	GPIO33_E ACZ_SDOUT R673 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

Date: Monday, October 22, 2012 Sheet 7 of 43

Cougar Point/Panther Point (PCI,USB,NVRAM)

Cougar Point/Panther Point(PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

SMBus/Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

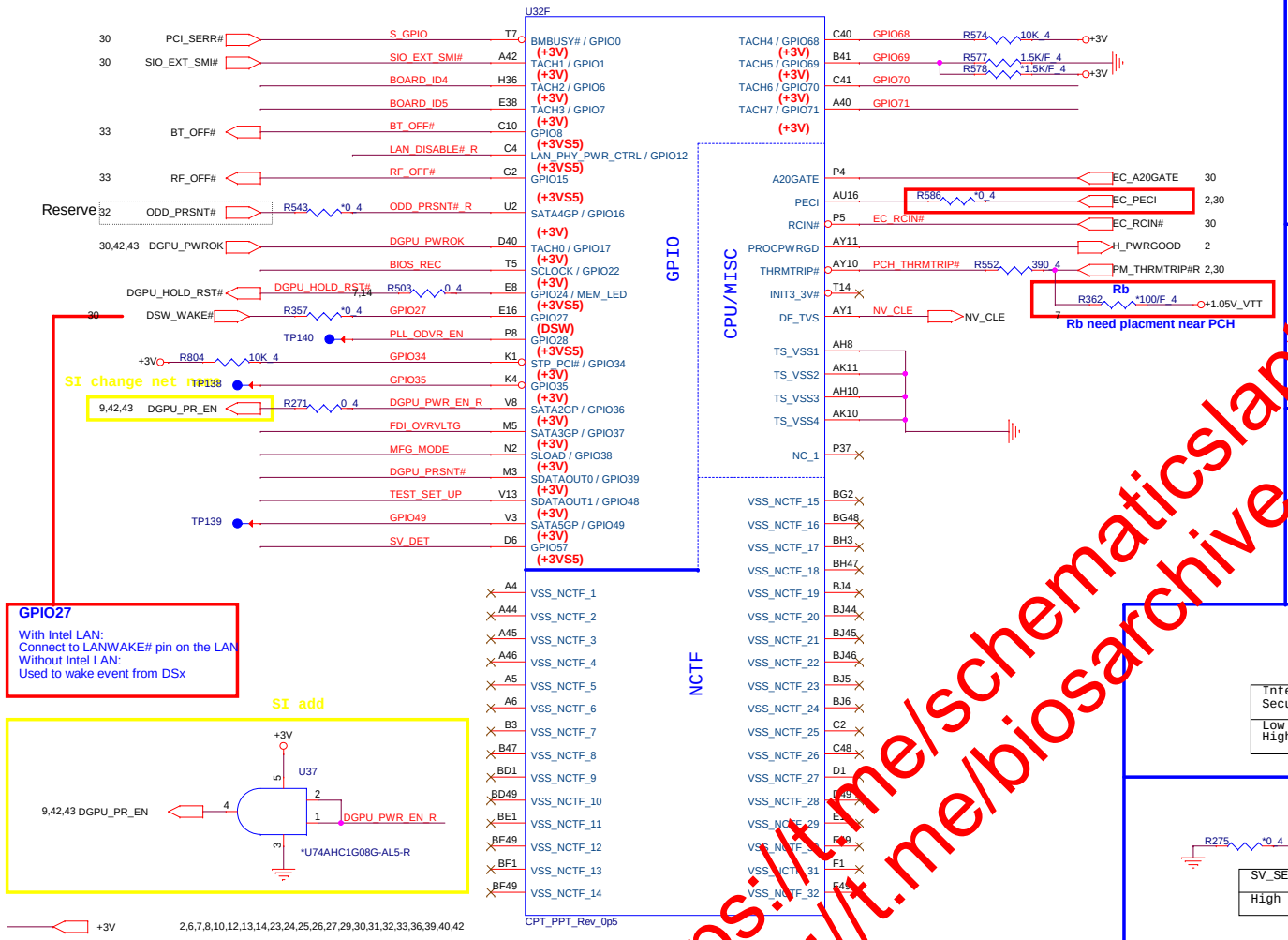
PROJECT : R62
Quanta Computer Inc.

NB5

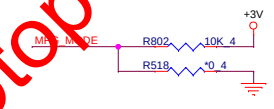
Size: Custom | Document Number: PCH 3/6 (PCIE/USB/CLK) | Rev: 1A

Date: Monday, October 22, 2012 | Sheet 8 of 43

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

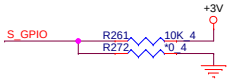


MFG-TEST

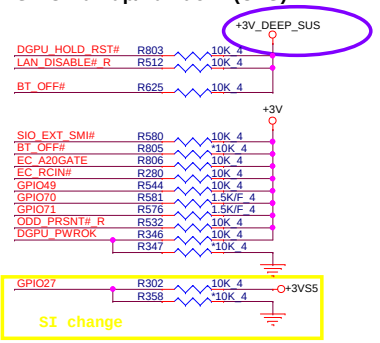


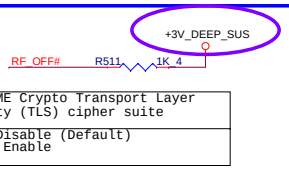
Swap GPIO

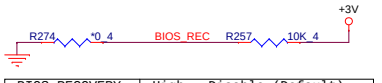
0 = SGPIO
1 = Default

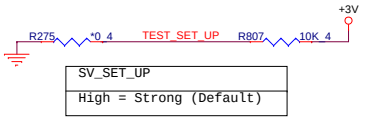


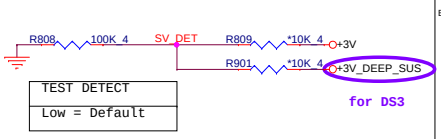
GPIO Pull-up/Pull-down(CLG) for DS3



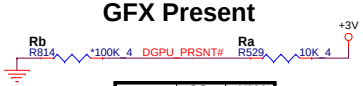








GFX Present

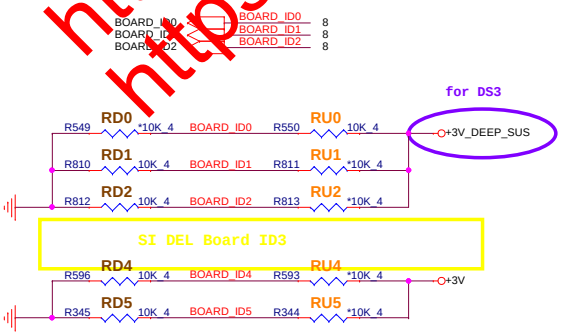


	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING

BOARD_ID1
For Stage Use

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
				0	1	1
				1	1	1
				0	0	0



NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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Cougar Point/Panther Point(POWER)

COUGAR POINT/Panther Point (POWER)

PCH DS3 PWR

PCH DS3 PWR

If have power noise issue then stuff it.

If EC support embedded flash , SPI power must be used S5_0N power rail for EC load code.

SI add C1107 for 3D mark Screen garbage issue.

+3V_DEEP_SUS	6,7,8,9,39
+1.05V	2,4,6,7,8,9,25,30,36,40
+3V_RTC	6,7,25
+1.5V	4,12,27,33
+3VS5	6,7,9,33,35,36,39,43
+3V	2,6,7,8,9,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
+5VS5	28,29,33,35,36,37,38,39,40,41,42,43
+5V	7,23,25,27,31,32,33,39
+1.8V	4,7,37,43

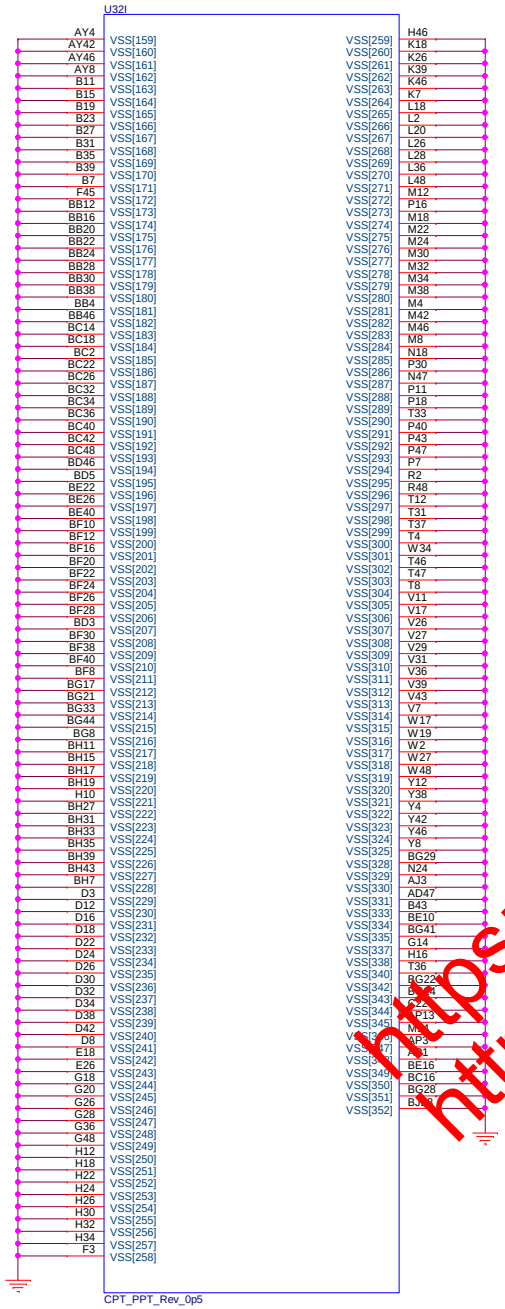
NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

Date: Monday, October 22, 2012 | Sheet 10 of 43

Cougar Point/Panther Point (GND)



NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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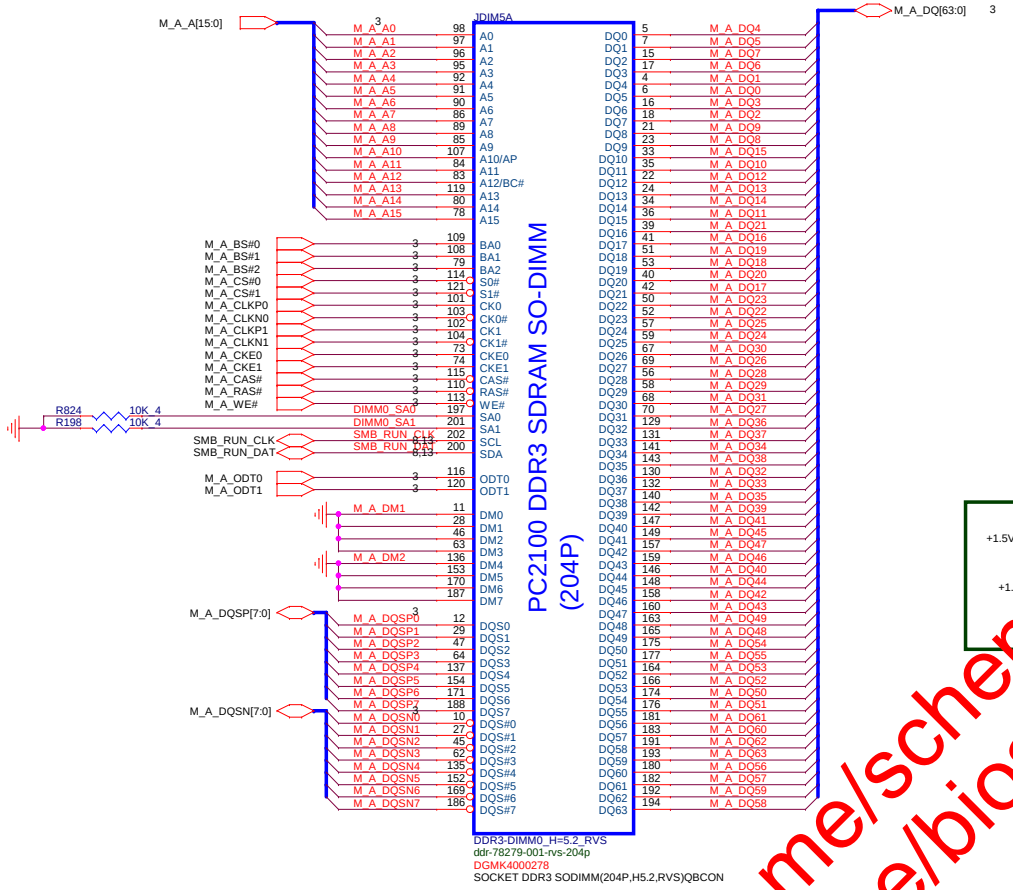
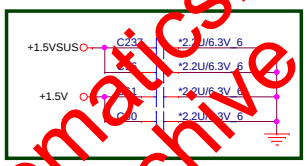
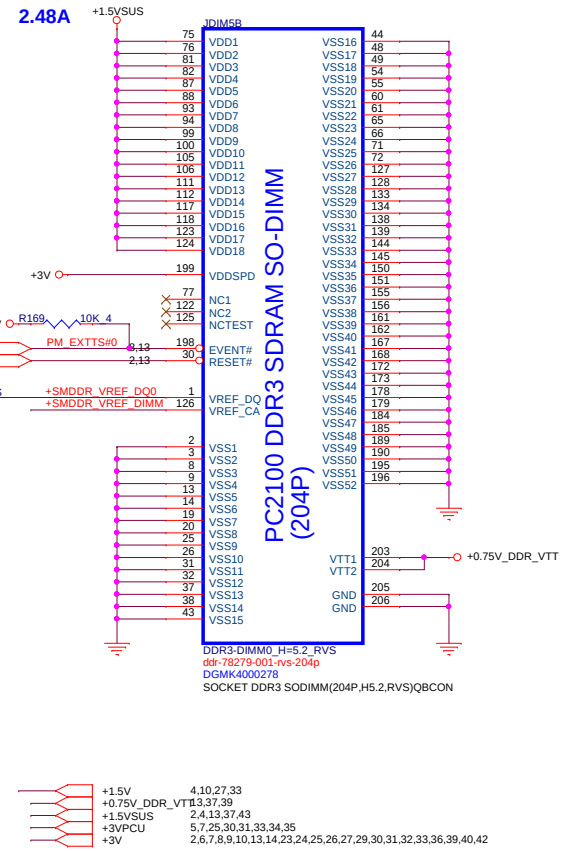
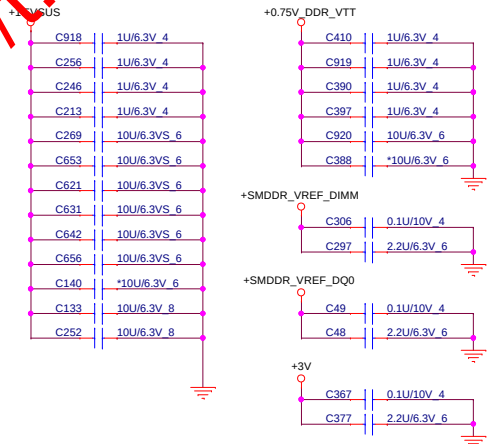


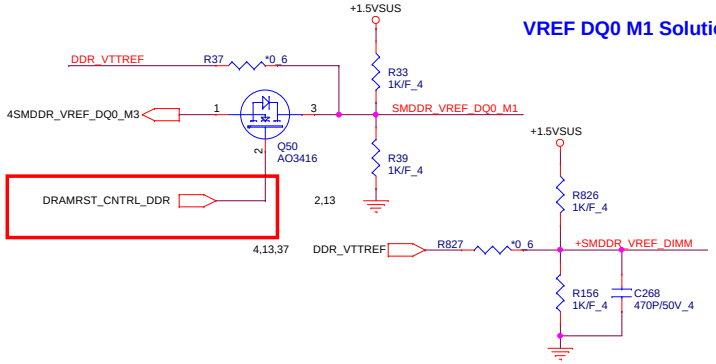




Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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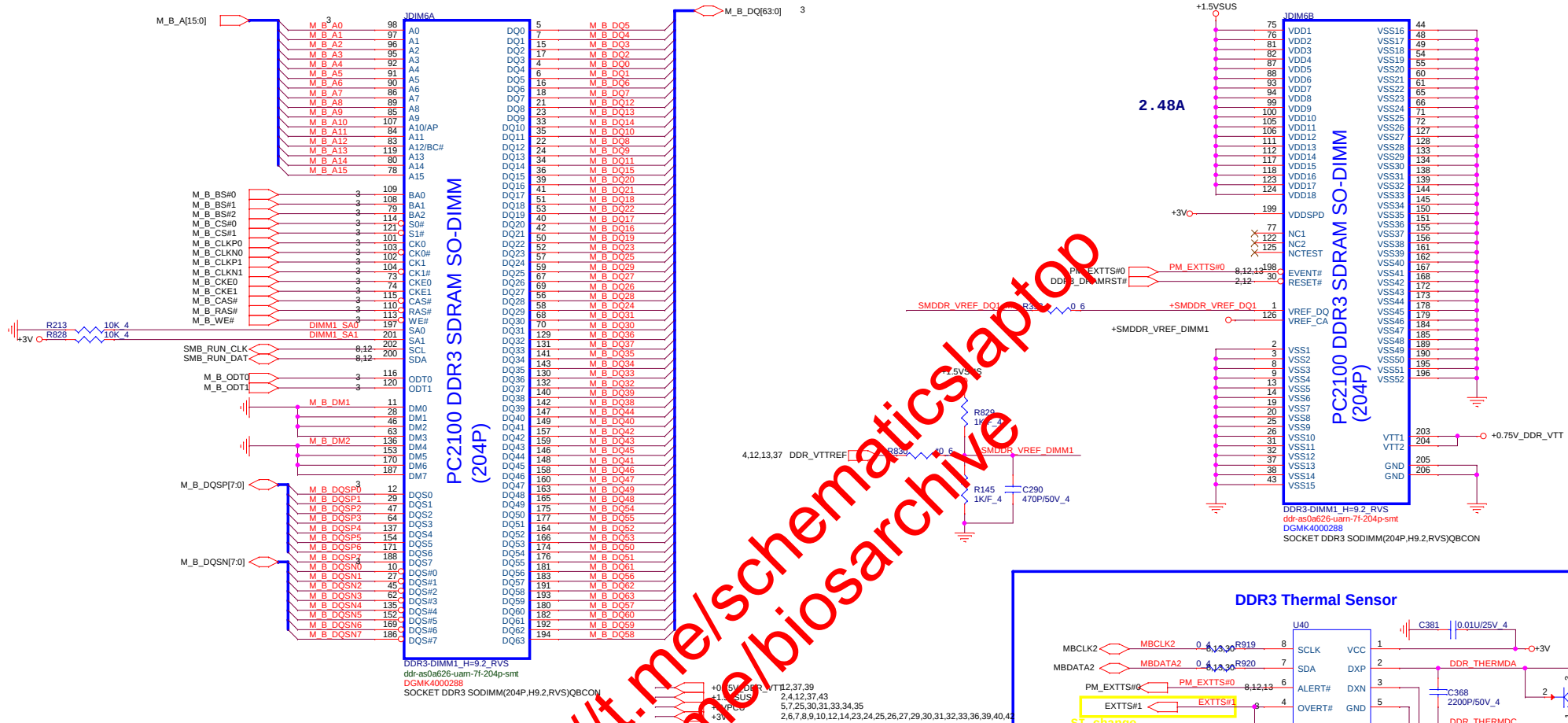
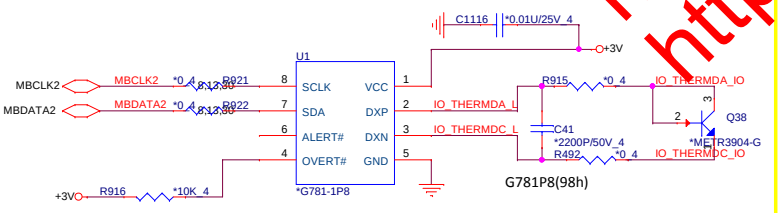


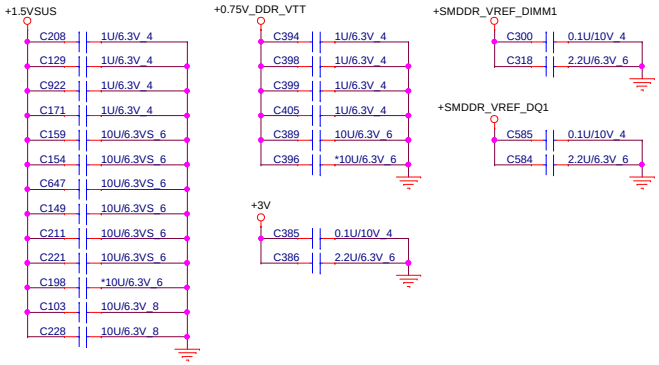
DDR3 Thermal Sensor

SI Add

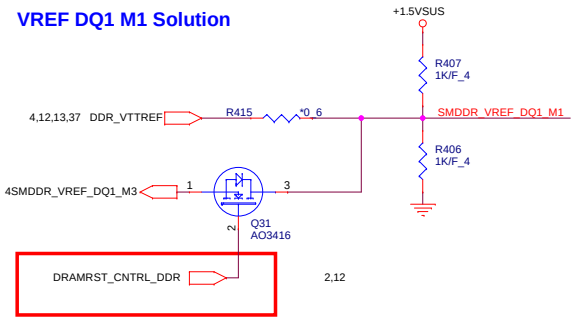
Local Thermal Sensor



Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
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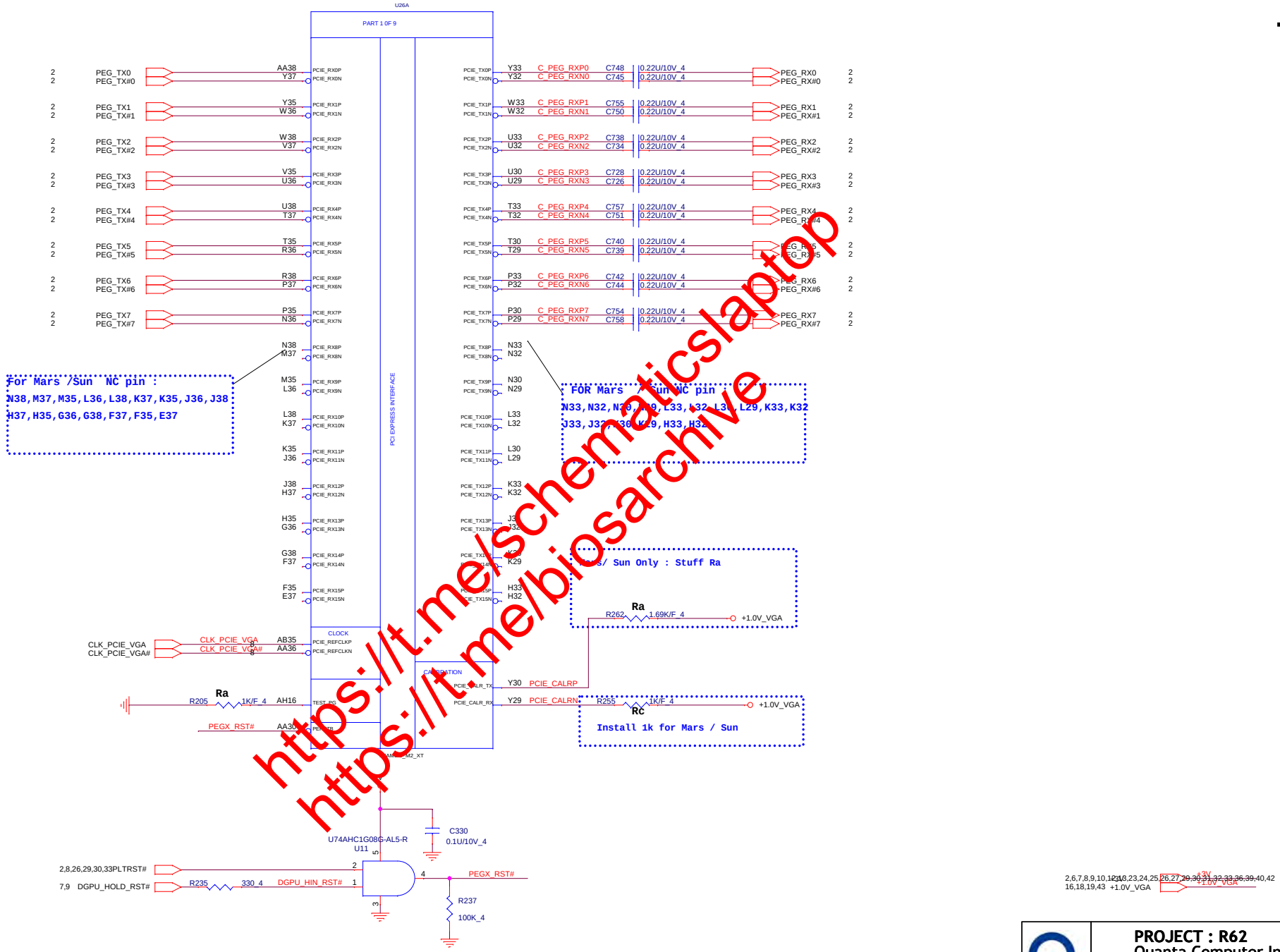

NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: THAMES_PCIE_Interface	Rev: 1A
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For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD20 /AC20 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

SI add

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

A 3-K external pull up (3.3 V) is required if an external BIOS ROM chip is used.

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20
AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff
For Sun Nc: R167, R141, C923

SI change to SUN setting

FOR MARS: AD37/ AE38 / AD35 / AC35 to GND
FOR SUN : AD37/ AE38 / AD35 / AC35 to PU

SI DEL revrse R749,R778,R781

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36
AD37/ AC36 / AC38 / AB34 /

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

Thermal Solution(Close to GPU)

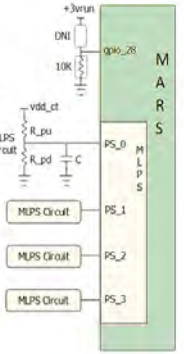
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Reserve for Power Play

For Mars: Stuff Ra, Rc=> VDDC 1.1V

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance



Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

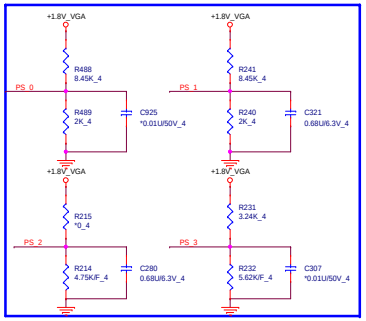
R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K



PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pces	AKD5PGWTW08 IC SDRAM(96P)H5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M16HA-093G:E	256Mx16 *4 pces	AKD5PZSTL01 IC SDRAM(96P)MT41J256M16HA-093G:E	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pces	AKD5PZDT501 IC SDRAM(96P)K4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FFR-11C	128Mx16 *4 pces	AKD5MZDTW03 IC SDRAM(96P)H5TC2G63FFR-11C	1G
100	4	Micron	MT41J128M16JT-093G:E	128Mx16 *4 pces		1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pces	AKD5MGGT535 IC SDRAM(96P)K4W2G1646E-BC1A	1G

14,16,18,19,42 +1.0V_VGA
16,18,19,25,42 +1.8V_VGA
17,18 +3V_DELAY

NB5

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Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

La

+1.8V_VGA — L23 0_6 — +1.8V_DPLL_PVDD

Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

C259 10U/6.3V_8 | C264 1U/6.3V_4 | C265 0.1U/10V_4

Lb

+1.0V_VGA — L21 0_6 — +1.0V_DPLL_VDDC

DPLL_VDDC : 0.935V @ 140mA

1.0V(125mA DPLL_VDDC)

C928 10U/6.3V_8 | C929 1U/6.3V_4 | C267 0.1U/10V_4

DPLL_PVSS

+1.8V_MPLL_PVDD

MPLL_PVDD : 1.8V @ 150mA

+1.8V_VGA — HCB1608KF-471T10 L35 — +1.8V_MPLL_PVDD

C441 10U/6.3V_8 | C437 1U/6.3V_4 | C438 0.1U/10V_4

+1.8V_SPLL_PVDD

SPLL_PVDD : 1.8V @ 75mA

+1.8V_VGA — L16 TB160808U121N005 — +1.8V_SPLL_PVDD

C167 10U/6.3V_8 | C176 1U/6.3V_4 | C191 0.1U/10V_4

+1.0V_SPLL_VDDC

SPLL_VDDC : 0.935V @ 150mA

+1.0V_VGA — L19 HCB1608KF-471T10 — +1.0V_SPLL_VDDC

1.0V(125mA DPLL_VDDC)

C181 10U/6.3V_8 | C932 1U/6.3V_4 | C216 0.1U/10V_4

SPLL_PVSS

DPEF_VDD18

SI change to DP_VDDR

R212 Ra *0_4

R249 Rb *0_4

reserve Ra, Rb for future ASIC

U26I

PART 9 0F 9

AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 MPLL_PVDD
H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS

PLLS/XTAL

THAMES_M2_XT

SI 27MHz change to XTALIN

R742 0_4 — VGA_XTAL27_IN 25

XTALIN AV33 — R818 *0_4 — EVGA-XTALI — *22P/50V_4 C244

R207 *10M_6 | Y2 *7A27000010

XTALOUT AU34 — R819 *0_4 — EVGA-XTALO — *22P/50V_4 C245

SI DEL reserve p

XO_IN AW34 — TP148

XO_IN2 AW35 — R487 *0_4

CLKTESTA AK10 CLK_TSTA
CLKTESTB AL10 CLKTESTB

Debug only,
for clock observation,
if not needed, DNI

C930 *0.1U/10V_4 | C931 *0.1U/10V_4

R171 *51.1/F_4 | R181 *51.1/F_4

route 50ohms
single-ended/
100ohms diff and keep short

U26F

PART 6 0F 9

AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U34 V34 W31 W34 Y34 Y39 — PCIE_VSS

F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L2 L22 L24 L6 M17 M22 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27 — GND

A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13 — GND

AG22 is nc pin

VSS_MECH A39 AW1 AW39

THAMES_M2_XT

14,18,19,43 +1.0V_VGA — +1.0V_VGA

15,18,19,25,42 +1.8V_VGA — +1.8V_VGA

NB5

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Custom	THAMES_XTAL	1A

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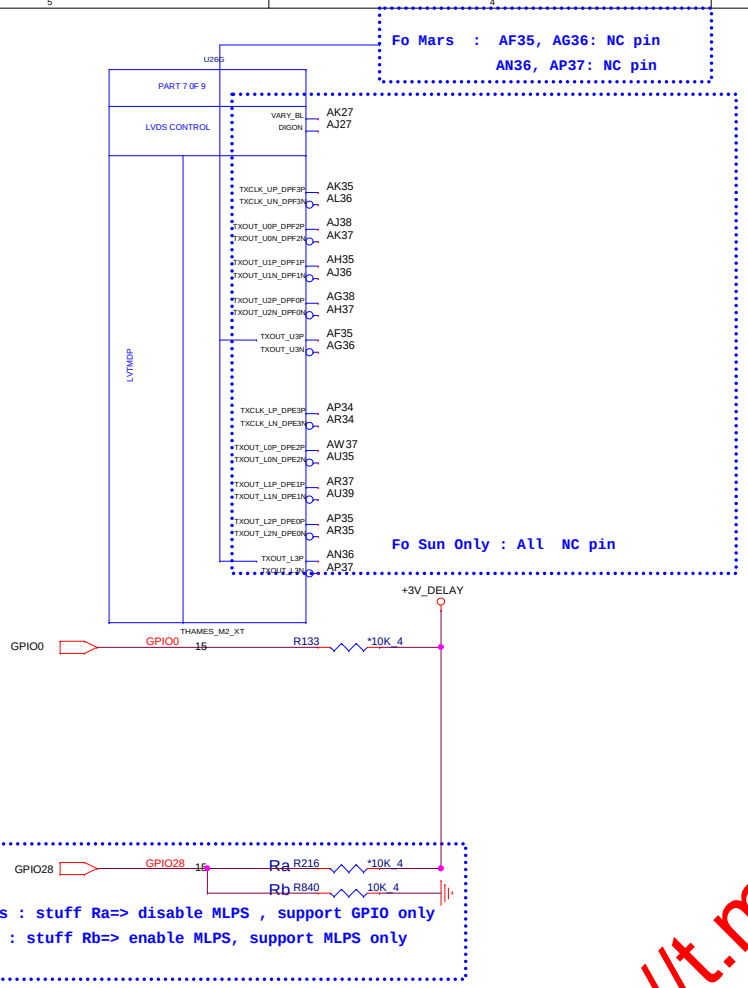


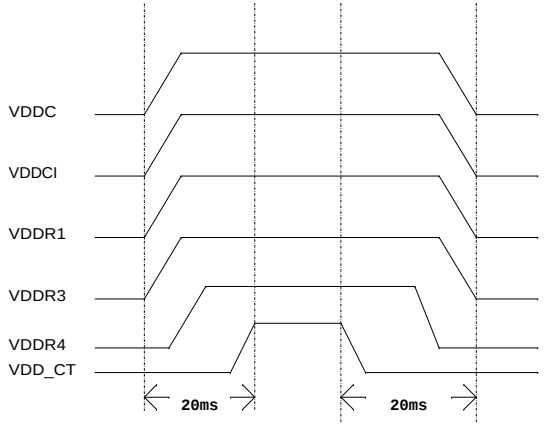
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capability enabled 1: VGA controller capability disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 000 - 512Kbit M25P05A (ST) 100 - 2Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 000 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 = No audio function 01 = Audio for DP only 10 = Audio for DP and HDMI if dongle is detected 11 = Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11	
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	
0	512M	1	0	0	+3.3V_Delay
0	1G	1	0	1	
0	2G	1	1	0	+1.8V_VGA
0	4G	1	1	1	+1.8V_VGA

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



NB5

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+1.5V_VGA

VDDR1 , 1.5V @ 2A, GDDR5 900MHz

I/O power for the memory interface.

C933 1U/6.3V_4 C934 1U/6.3V_4 C719 1U/6.3V_4 C468 1U/6.3V_4 C935 1U/6.3V_4 C764 1U/6.3V_4 C335 1U/6.3V_4 C936 1U/6.3V_4 C725 1U/6.3V_4 C470 1U/6.3V_4

C401 10U/6.3VS_6 C479 10U/6.3VS_6 C942 10U/6.3VS_6 C943 10U/6.3VS_6 C689 10U/6.3VS_6 C944 10U/6.3VS_6

Reserve for Drop

C826 *22U/6.3VS_8 C254 *22U/6.3VS_8 C453 *22U/6.3VS_8 C178 22U/6.3VS_8 C449 *22U/6.3VS_8

C457 *22U/6.3VS_8 C205 22U/6.3VS_8 C785 *22U/6.3VS_8 C609 *330u_2.5V_3528 C710 *330u_2.5V_3528

VDDC_CT: 1.8V @250mA

+1.8V_VGA L49 0_6 +1.8V_VDD_CT

C672 *10U/6.3VS_6 C660 1U/6.3V_4 C661 1U/6.3V_4 C655 1U/6.3V_4 C654 0.1U/10V_4

+3V_VGA L17 0_6 +3V_DELAY

VDDR3 : 3.3V @ 60mA

C676 *10U/6.3VS_6 C673 1U/6.3V_4 C240 1U/6.3V_4 C674 1U/6.3V_4

For Mars: stuff

L18 *0_6

For Sun: NC L18, C214, C223,C241, C232, C311, C955

+VDDR4

VDDR4 : 1.8V @ 300mA

C214 *10U/6.3VS_6 C223 *10U/6.3VS_6 C241 *1U/6.3V_4 C232 *1U/6.3V_4 C311 *0.1U/10V_4 C955 *0.1U/10V_4

SI DEL parts for SUN setting

Route as differential pair and connect to the VSEN and RTN pins of the VR through a decoupling and termination circuit.

VGPU_CORE_SENSE — AF28 — FB_VDDC

TP33 — AG28 — FB_VDDCI

VSS_GPU_SENSE — AH29 — FB_GND

U26E

PART 5 OF 9

MEM I/O — LEVEL TRANSLATION — I/O — DVP — VOLTAGE SENSE

PCIE — BACO — CORE — ISOLATED CORE I/O

THAMES_M2_XT

+1.8V_VGA

C961 0.1U/10V_4 C376 1U/6.3V_4 C362 10U/6.3VS_6

PCIe Digital Power Supply

PCIE_VDDC : 0.935V @ 1.88A (GEN2.0)

PCIE_VDDC : 0.935V @ 2.5A (GEN3.0)

+1.0V_VGA

C939 0.1U/10V_4 C373 0.1U/10V_4 C940 0.1U/10V_4 C366 1U/6.3V_4 C393 1U/6.3V_4 C379 1U/6.3V_4 C941 1U/6.3V_4 C374 1U/6.3V_4 C363 1U/6.3V_4

C378 1U/6.3V_4 C945 1U/6.3V_4 C364 1U/6.3V_4 C380 1U/6.3V_4 C361 10U/6.3VS_6 C360 10U/6.3VS_6

BIF_VDDC

R267 Ra 0_8

R290 Rb *0_8

+VGA_CORE

	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

C946 1U/6.3V_4 C372 1U/6.3V_4 C356 1U/6.3V_4 C371 1U/6.3V_4 C354 1U/6.3V_4 C210 1U/6.3V_4 C353 1U/6.3V_4 C219 1U/6.3V_4 C384 1U/6.3V_4 C370 1U/6.3V_4

C313 1U/6.3V_4 C947 1U/6.3V_4 C948 1U/6.3V_4 C355 1U/6.3V_4 C369 1U/6.3V_4 C949 1U/6.3V_4 C314 1U/6.3V_4 C315 1U/6.3V_4 C180 1U/6.3V_4 C950 1U/6.3V_4

C951 1U/6.3V_4 C317 1U/6.3V_4 C350 1U/6.3V_4 C952 1U/6.3V_4 C316 1U/6.3V_4 C953 1U/6.3V_4 C340 1U/6.3V_4 C239 1U/6.3V_4 C342 1U/6.3V_4 C954 1U/6.3V_4

C217 10U/6.3VS_6 C956 10U/6.3VS_6 C224 10U/6.3VS_6 C203 10U/6.3VS_6 C957 10U/6.3VS_6

C242 10U/6.3VS_6 C309 10U/6.3VS_6 C234 10U/6.3VS_6 C338 10U/6.3VS_6 C351 330u_2.5V_3528

BIF_VDDC

C403 22U/6.3VS_8 C959 1U/6.3V_4 C404 1U/6.3V_4 C391 10U/6.3VS_6

20,21,22,43 +1.5V_VGA
14,16,19,43 +1.0V_VGA
15,16,19,25,44 +1.8V_VGA
43 +3V_VGA
33,42,43 +VGA_CORE

+1.5V_VGA
+1.0V_VGA
+1.8V_VGA
+3V_VGA
+VGA_CORE

+VDDCI

VDDCI 0.8-1.15V @ 6A

+VGA_CORE

C312 1U/6.3V_4 C375 1U/6.3V_4 C343 1U/6.3V_4 C331 1U/6.3V_4 C339 1U/6.3V_4 C382 1U/6.3V_4 C958 1U/6.3V_4 C387 1U/6.3V_4

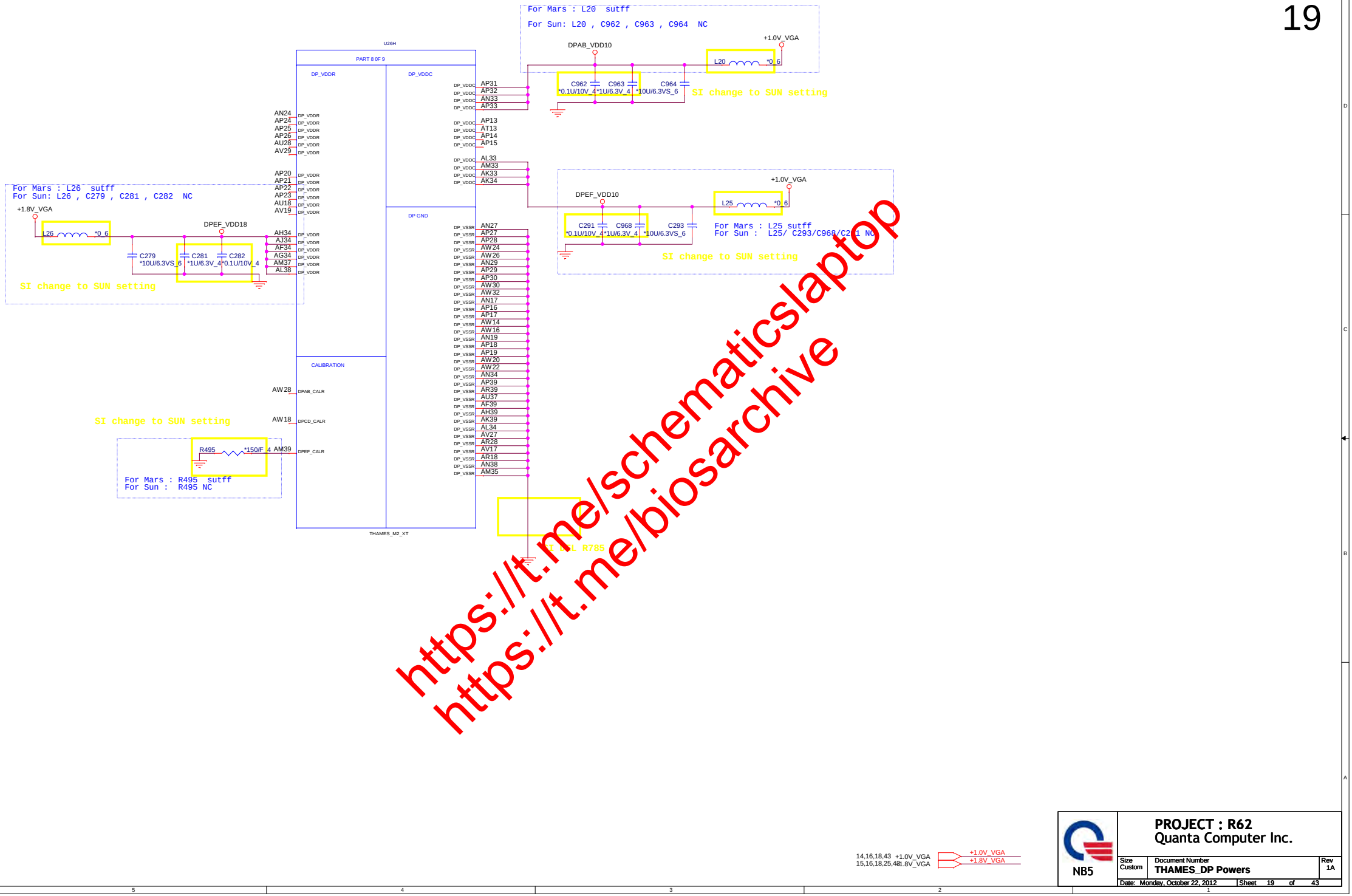
C383 10U/6.3VS_6 C960 10U/6.3VS_6 C395 10U/6.3VS_6 C365 1U/6.3V_4 C348 1U/6.3V_4

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_Power & BACO	1A

Date: Monday, October 22, 2012 Sheet 18 of 43



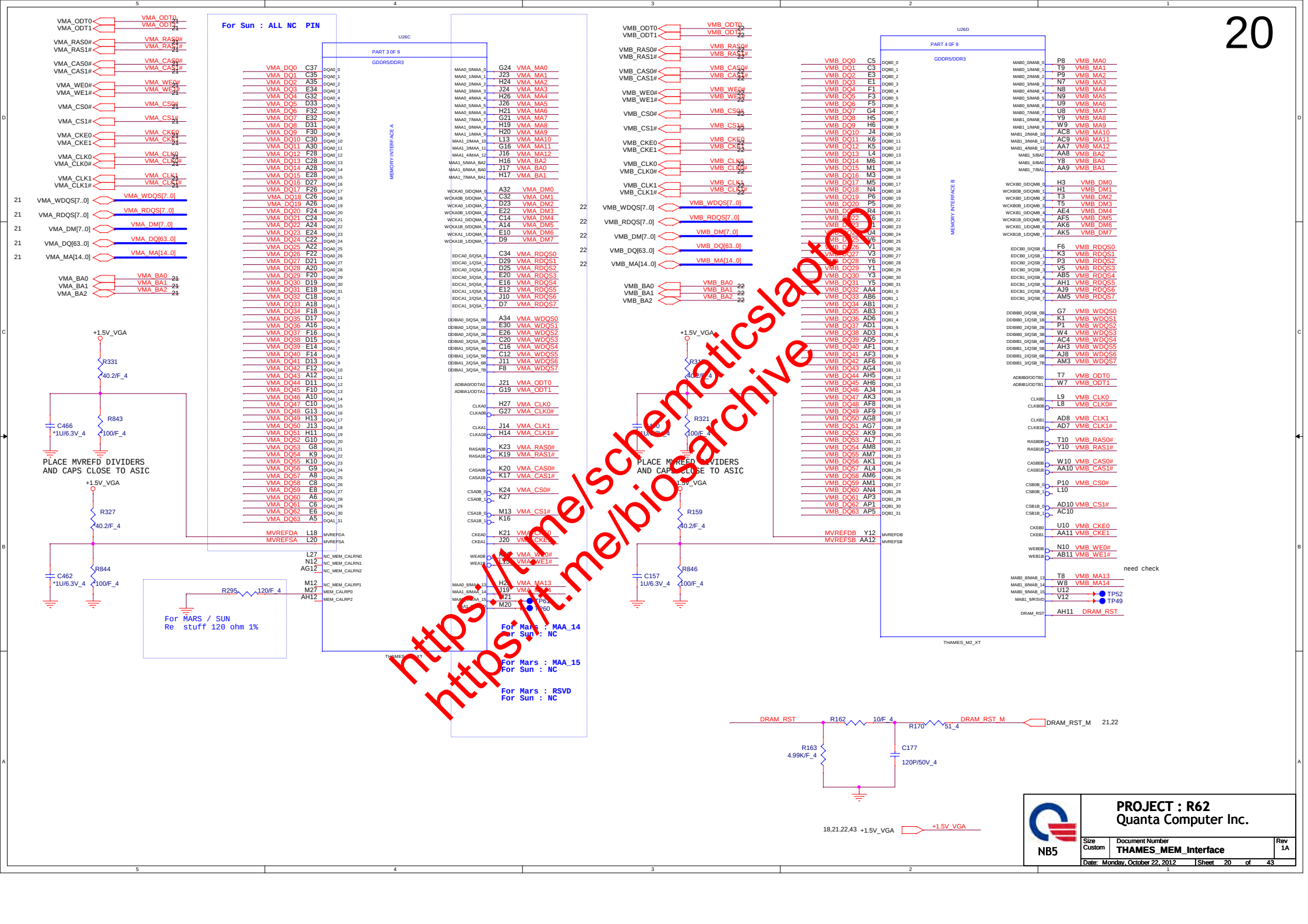
14,16,18,43 +1.0V_VGA
15,16,18,25,48 +1.8V_VGA
+1.0V_VGA
+1.8V_VGA

NB5

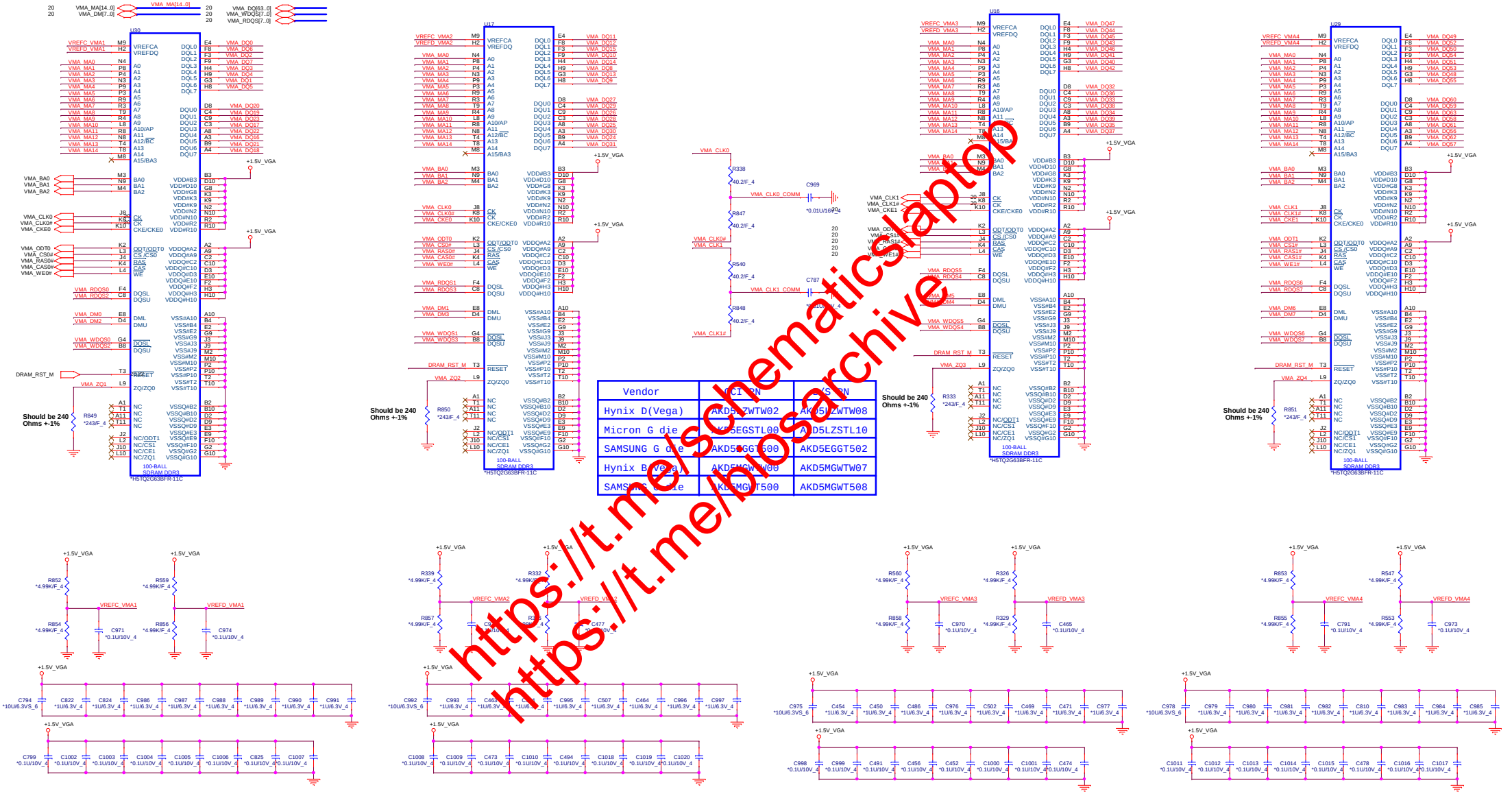
PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_DP Powers	1A

Date: Monday, October 22, 2012 Sheet 19 of 43



CHANNEL A: 256MB/512MB DDR3

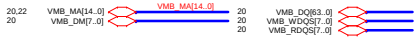


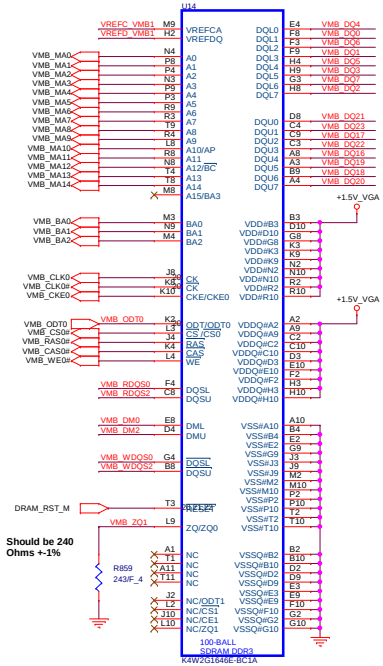
Vendor	DCI P/N	non-DCI P/N
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	KD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG B die	AKD5MGWT500	AKD5MGWT508

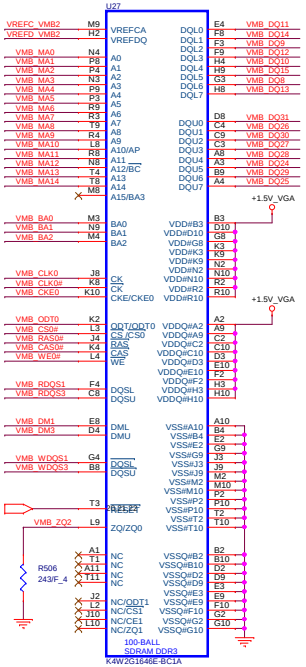
18,20,22,43 +1.5V_VGA +1.5V_VGA

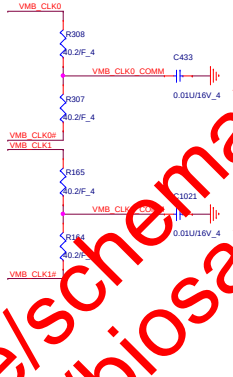
NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: Custom	Document Number: VRAM-A (DDR3 BGA96)	Rev: 3A
	Date: Monday, October 22, 2012	Sheet 21 of 43	

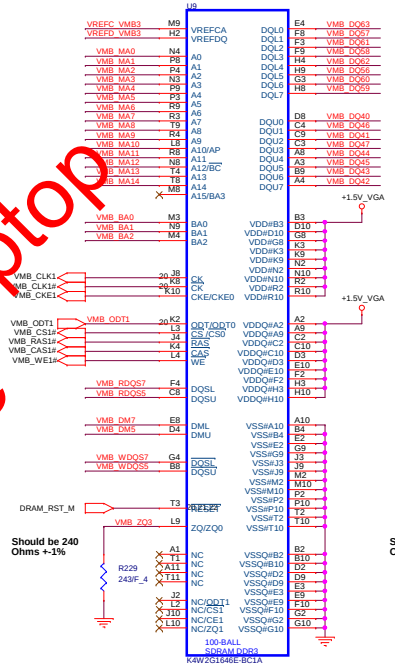
CHANNEL B: 256MB/512MB DDR3

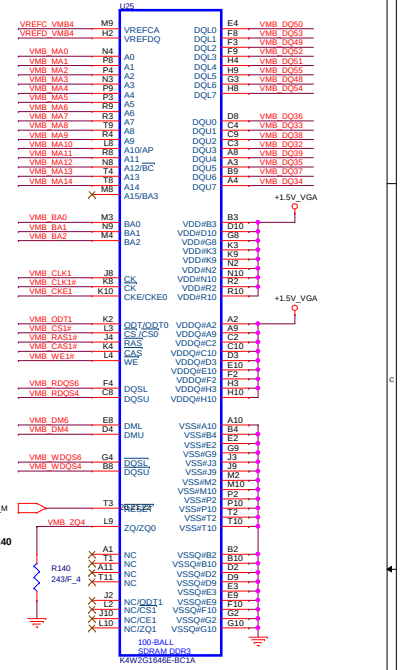


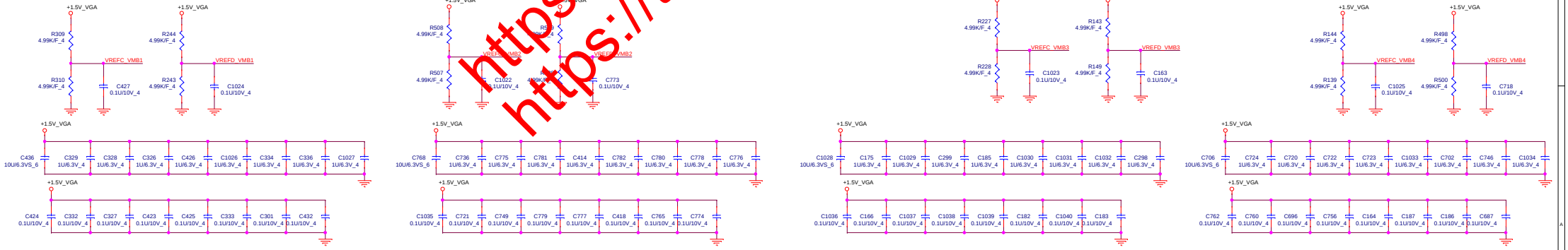








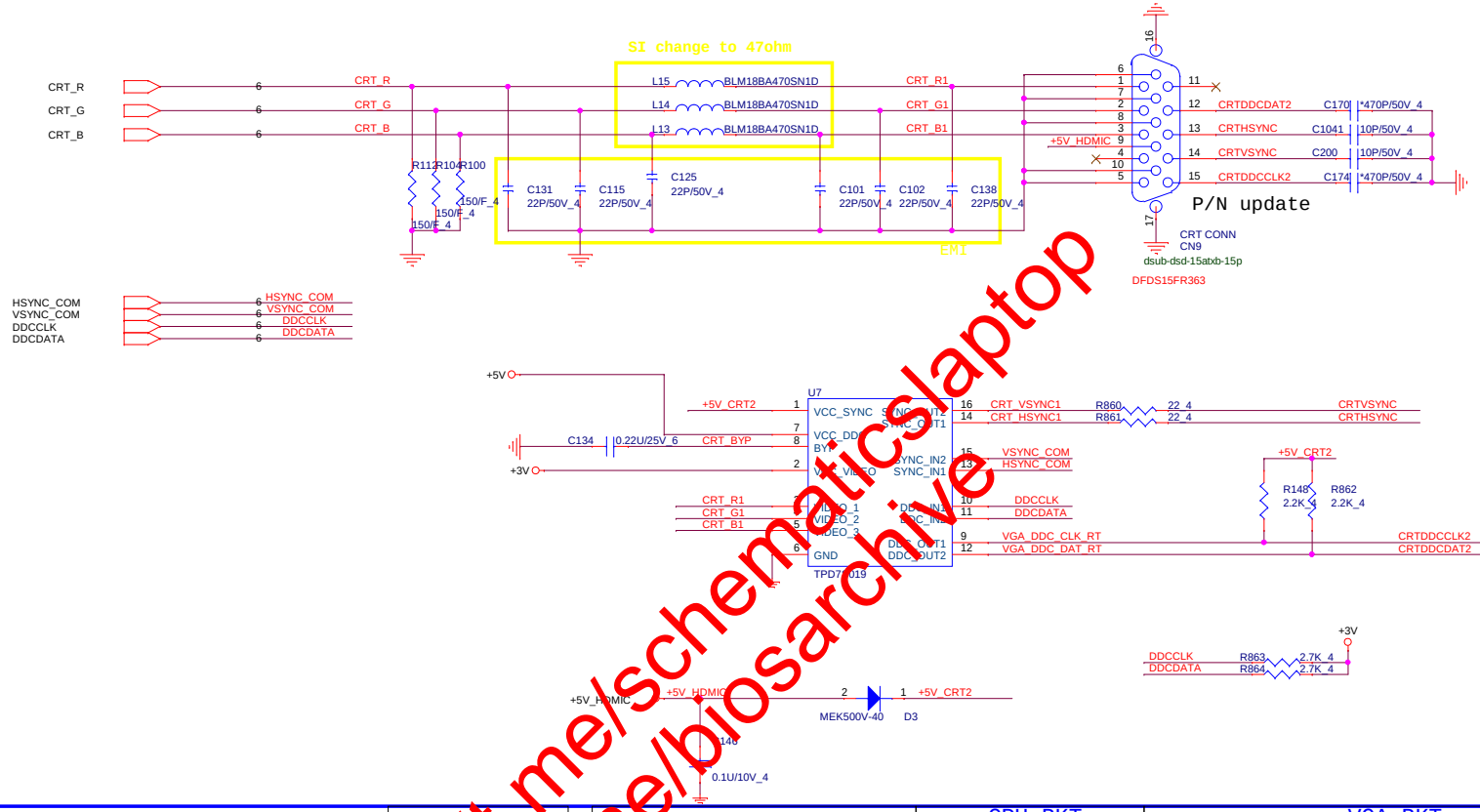




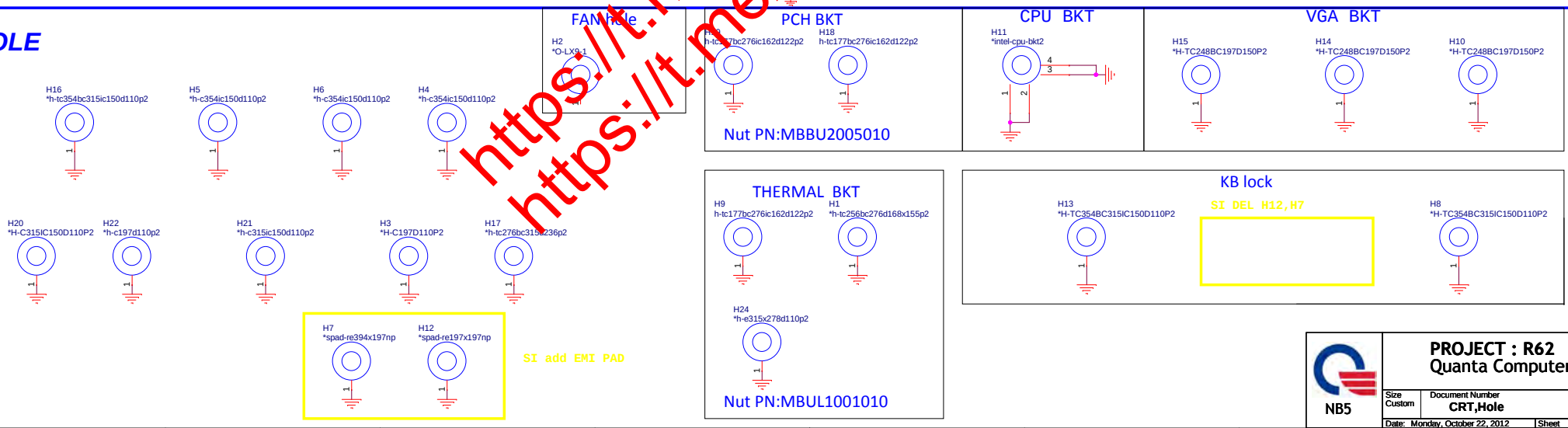
18,20,21,22,42 +1.5V_VGA
18,20,21,22,42 +1.5V_VGA

NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: Custom	Document Number: VRAM-B (DDR3 BGA96)	Rev: 1A
	Date: Monday, October 22, 2012	Sheet 22 of 43	

CRT PORT

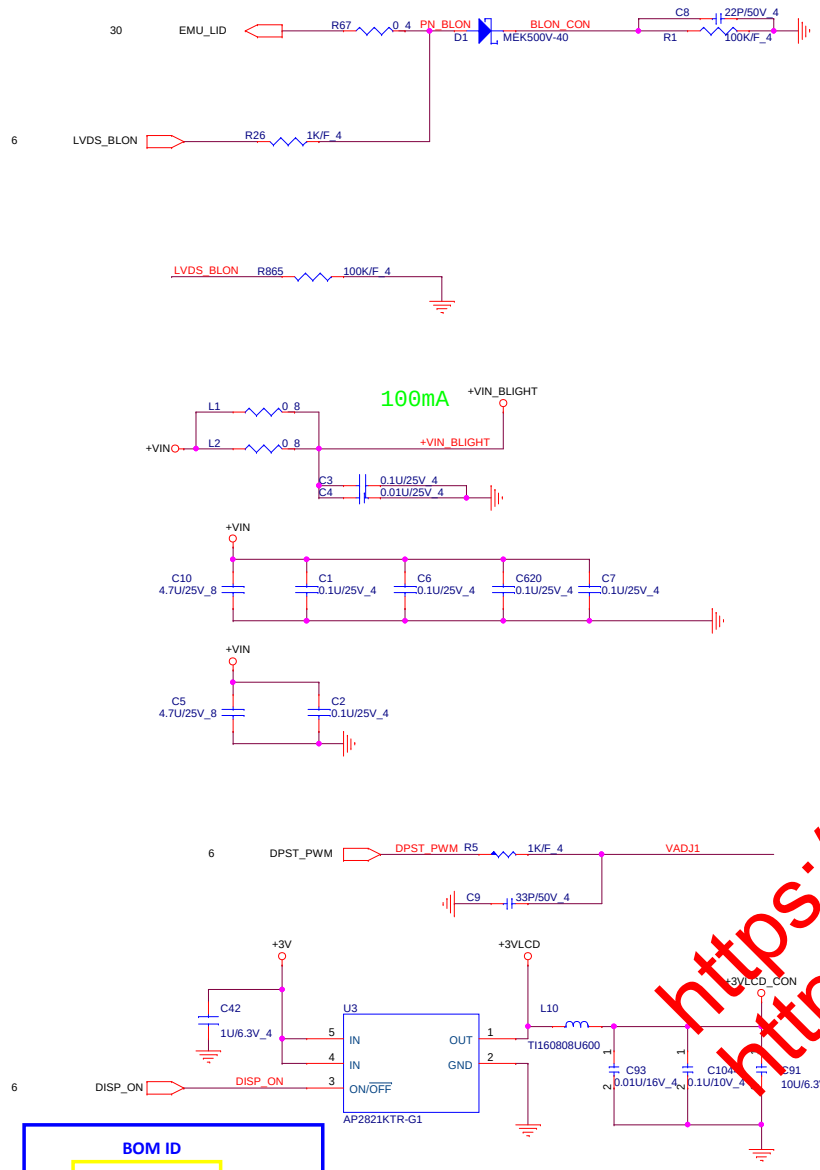


HOLE



NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: CRT,Hole	Rev: 1A
Date: Monday, October 22, 2012	Sheet 23 of 43	

LID Switch



BOM ID

R910 *0_4

R911 *0_4

SI Add BOM ID

6 TXUCLKOUT- TXUCLKOUT-
6 TXUCLKOUT+ TXUCLKOUT+
6 TXUOUT0+ TXUOUT0+
6 TXUOUT0- TXUOUT0-
6 TXUOUT1+ TXUOUT1+
6 TXUOUT1- TXUOUT1-
6 TXUOUT2+ TXUOUT2+
6 TXUOUT2- TXUOUT2-
6 TXLCLKOUT+ TXLCLKOUT+
6 TXLCLKOUT- TXLCLKOUT-
6 TXLOUT2+ TXLOUT2+
6 TXLOUT2- TXLOUT2-

For LVDS Only:

+3V
R19 4.7K_4 EDIDCLK
R15 4.7K_4 EDIDDATA
RF
C22 *10P/50V_4
C19 *10P/50V_4

+3VLCD_CON

+VIN_BLIGHT R20 Ra *0_6
+3V R21 Rb 0_6
C23 1000P/50V_4
C34 0.047U/10V_4
C39 0.047U/10V_4

For LVDS Only: Stuff Rb

For EDP Only: Stuff Ra

For LVDS Only: Stuff Rc

For EDP Only: Stuff Rd

2 EDP_HPD R9 Rd *0_4 EDP_HPD_R
Rc R8 0_4

EDIDCLK
EDIDDATA
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

CN1
GS12401-1011-9H
DFHS40FS075
GS12407-11141-9H-40P-R

DIGITAL_D1 27 L5 TB160808U301N000 DIGITAL_D1_L
DIGITAL_CLK 27 L4 DIGITAL_CLK_L
TB160808U301N000
8 USBP4- USBP4- R
8 USBP4+ USBP4+ R
L3
MCM2012B900GBE
+3V_CAM
VADJ1
BLON_CON
+VIN_BLIGHT

DIGITAL_D1_L
DIGITAL_CLK_L
C14 100P/50V_4
C13 100P/50V_4

6 EDP_TXP0 TXLOUT0+_2136 TXLOUT0-_2136 2 EDP_TXN0
R12 0_4 R13 0_4
C17 *0.1U/10V_4
C18 *0.1U/10V_4
TXLOUT0+
TXLOUT0-

2 EDP_TXP1 6 TXLOUT1+_2136 6 TXLOUT1-_2136 2 EDP_TXN1
R10 0_4 R11 0_4
C15 *0.1U/10V_4
C16 *0.1U/10V_4
TXLOUT1+
TXLOUT1-

2 EDP_AUXN 6 EDIDDATA_2136 6 EDIDCLK_2136 2 EDP_AUXP
R16 0_4 R17 0_4
C20 *0.1U/10V_4
C21 *0.1U/10V_4
EDIDDATA
EDIDCLK

For EDP Only: stuff Cap

For LVDS only stuff Resistor

+3V R7 *0_4/S +3V_CAM
C11 *0.01U/16V_4
C12 *4.7U/6.3V_6

For EDP Only: stuff

+3V
R14 *100K_4 EDIDDATA
R18 *100K_4 EDIDCLK
+3V
R6 *1K_4 DPST_PWM
R48 *1K_4 LVDS_BLON

+3V 2,6,7,8,9,10,12,13,14,23,25,26,27,29,30,31,32,33,36,3
+3VPCU 5,7,25,30,31,33,34,35
+VIN 33,34,35,36,37,39,41,42,43

NB5

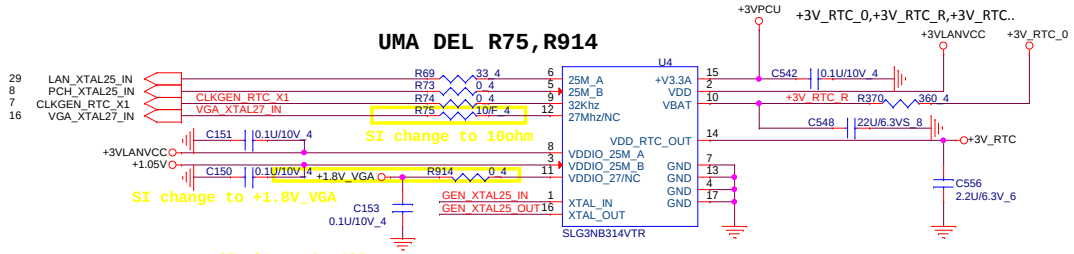
PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Monday, October 22, 2012	Sheet 24 of 43	

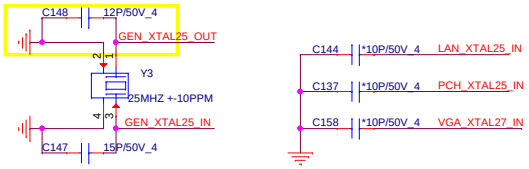
Green CLK Circuitry

20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..

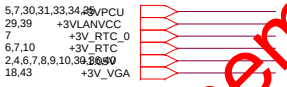
UMA DEL R75,R914



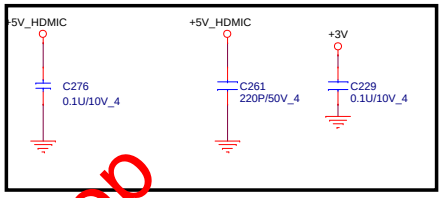
SI change to 12P

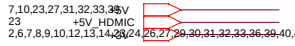


	U4 P/N
UMA	AL3NB244000
DIS	AL000314000

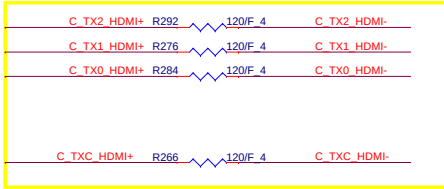


EMI request

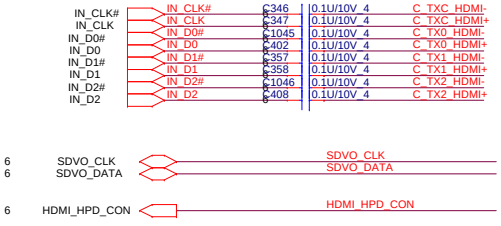




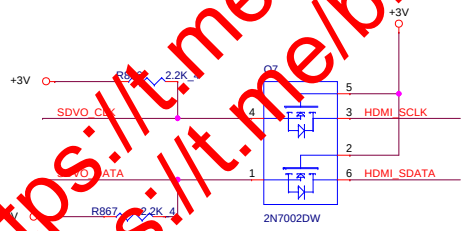
EMI request

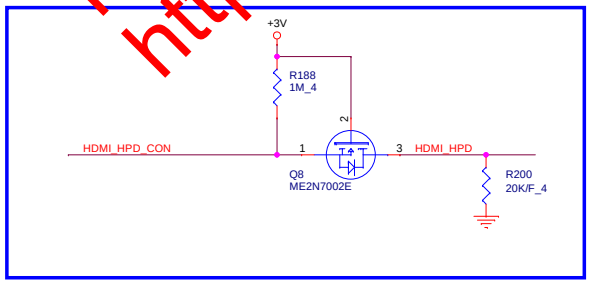


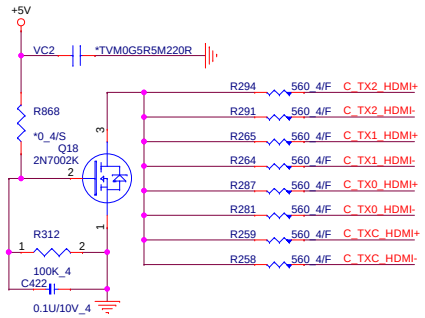
close to HDMI conn

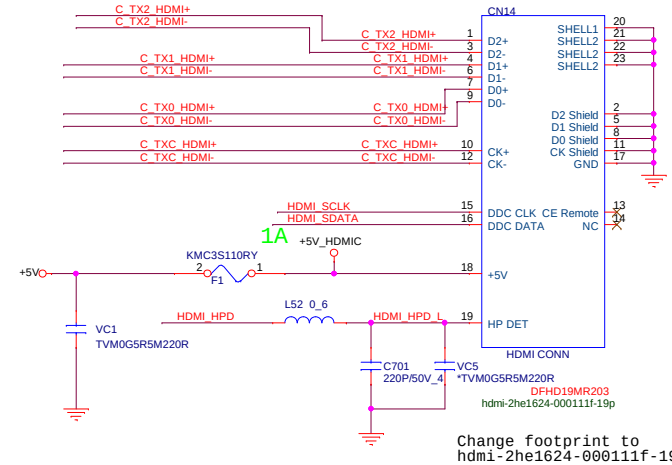


Close to HDMI Connector

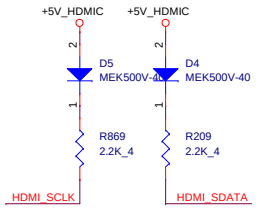








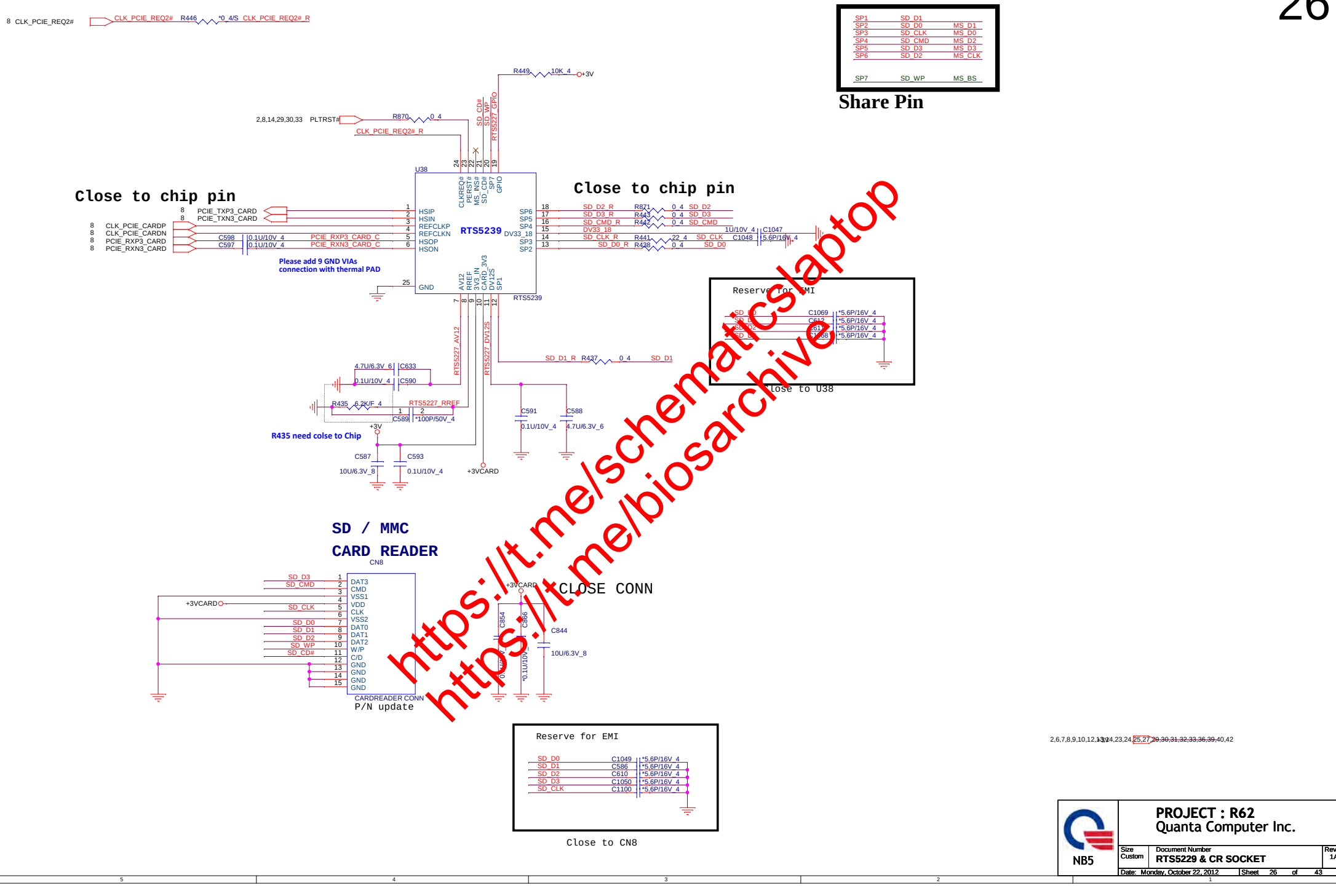
Change footprint to
hdmi-2he1624-000111f-19p

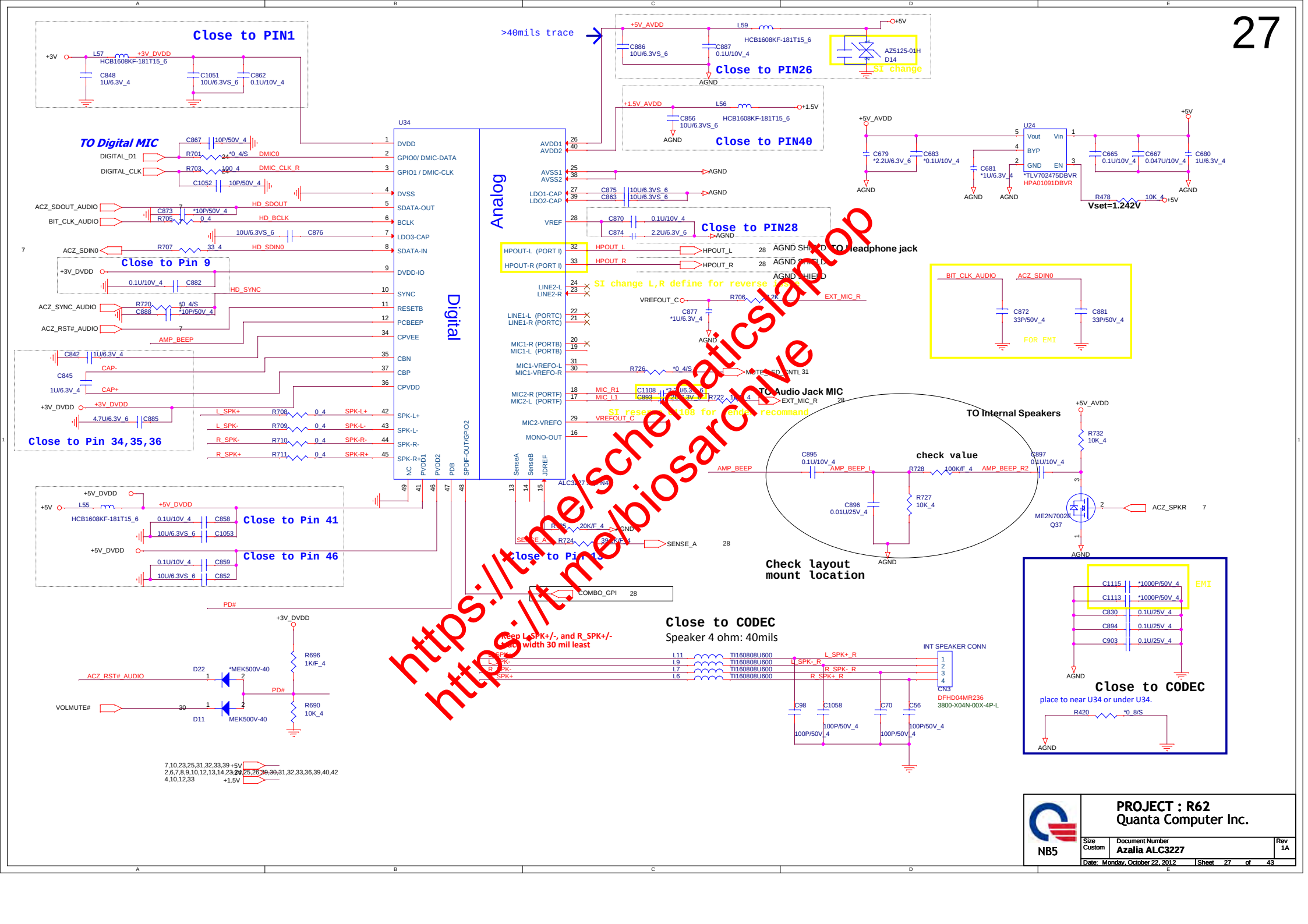


NB5

PROJECT : R62
Quanta Computer Inc.

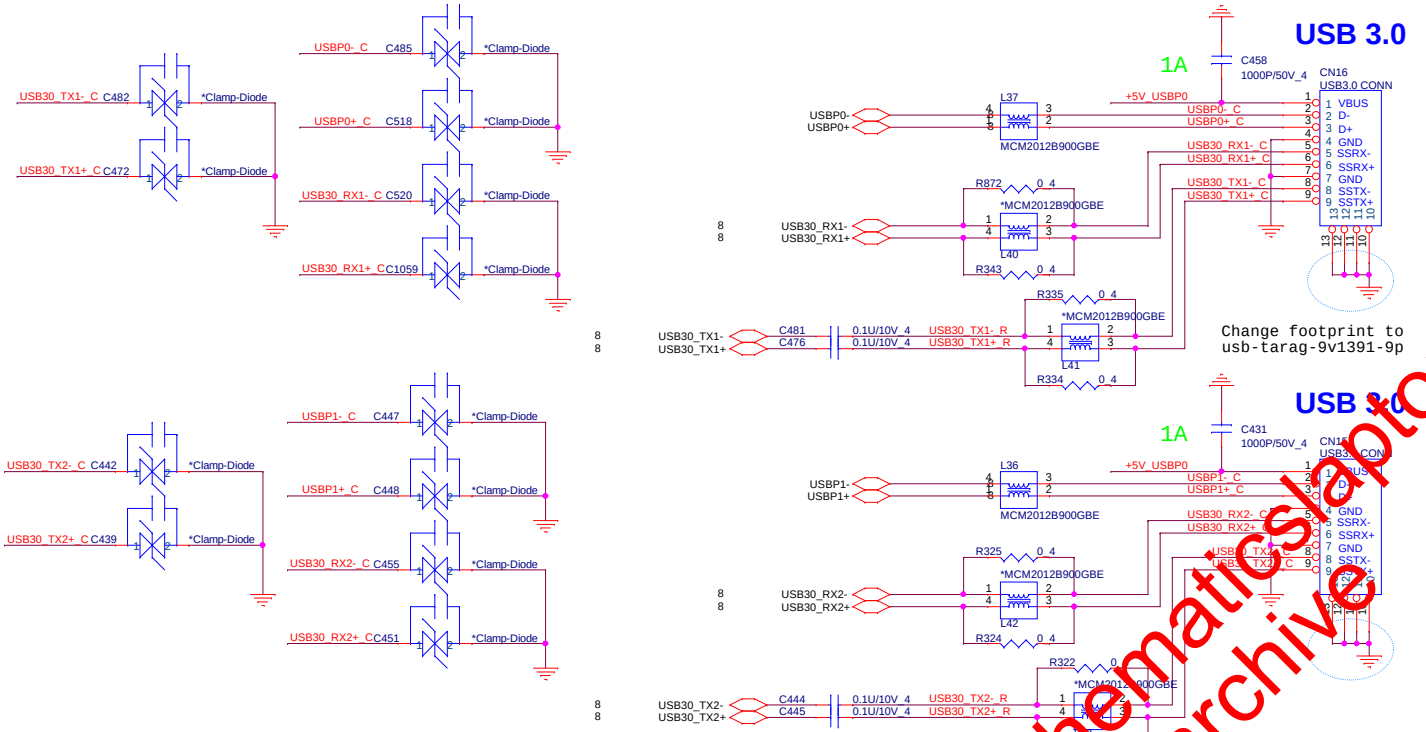
Size	Document Number	Rev
Custom	HDMI CONN	1A
Date: Monday, October 22, 2012	Sheet 25 of 43	


Share Pin
SP1 SD_D1
SP2 SD_D0 MS_D1
SP3 SD_CLK MS_D0
SP4 SD_CMD MS_D2
SP5 SD_D3 MS_D3
SP6 SD_D2 MS_CLK
SP7 SD_WP MS_BS
Close to chip pin
Close to chip pin
RTS5239
U38
Please add 9 GND VIAs connection with thermal PAD
R435 need colse to Chip
Reserve for EMI
Close to U38
SD / MMC
CARD READER
CN8
CLOSE CONN
CARDREADER CONN
P/N update
Reserve for EMI
Close to CN8
https://t.me/schematicslaptop
https://t.me/biosarchive

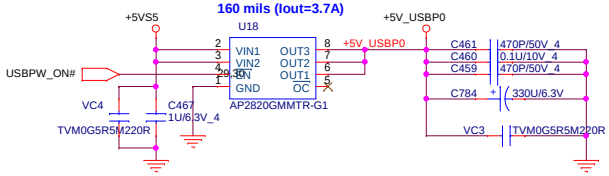


PROJECT :	R62
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Azalia ALC3227
Rev:	1A
Date: Monday, October 22, 2012	Sheet 27 of 43

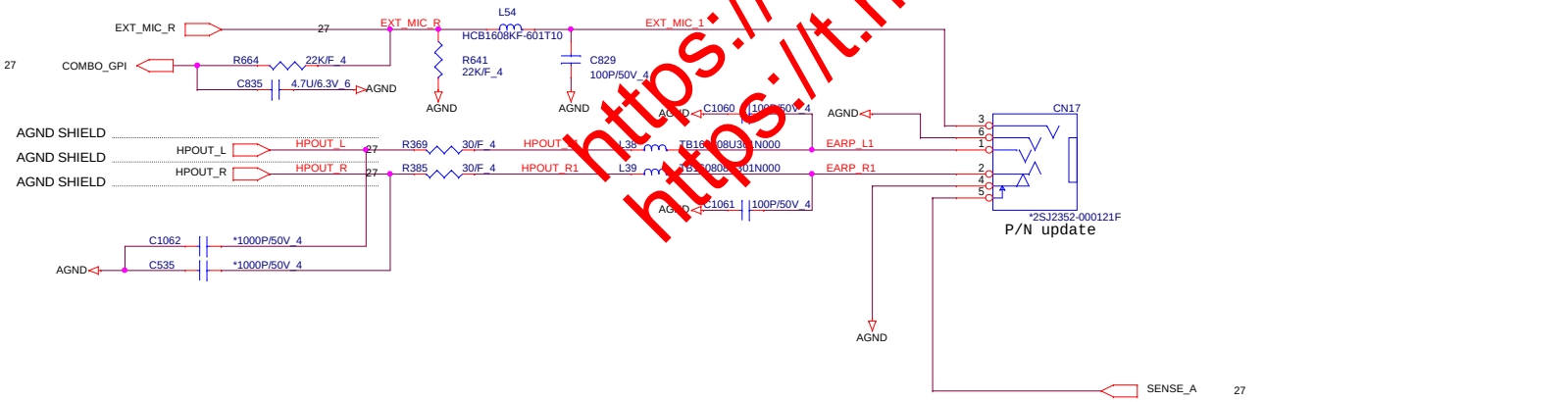
USB 3.0



USB3.0 X 2/USB2.0 COMBO



COMBO JACK



NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: USB/BT/Audio JacK	Rev: 1A
Date: Monday, October 22, 2012	Sheet 28 of 43	

SI DEL reserve parts

LAN_XTAL1 R92 *10_4 XTAL1_R R54 *0_4 XTAL1

Y1 1 2 *25MHz

XTAL2_R R55 *0_4 XTAL2

R53 0_4 LAN_XTAL25_IN 25

C92 *27P/50V_4 C1063 *27P/50V_4

Green Clk

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf close to each VDD10 pin-- 8, 30 only,

Power trace Layout 寬度> 60mil

>60mil >60mil

+1.05V_LAN_REGOUT R371 0_8 L46 *4.7UH,+-20%,650MA_1210 +1.05V_LAN

La

C1101 0.1U/10V_4

Ca Cb

C1065 *0.1U/10V_4 C624 *4.7U/6.3V_6

Trace<30 mil
Width > 60 mil

Cc Cd Ce Cf Cg Cf

C1066 *0.1U/10V_4 C117 *0.1U/10V_4 C63 0.1U/10V_4 C74 0.1U/10V_4 C1067 *1U/6.3V_4 C130 *1U/6.3V_4

reserve for colay

For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb

For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

+3V_LAN +3VLANVCC C66 *0.1U/10V_4 Ca C127 0.1U/10V_4 Cb C77 0.1U/10V_4 Ce

reserve for colay

* Place Cc and Cd close to each VDD33 pin-- 23

DVDDL C108 *4.7U/6.3V_6 Cc C69 *0.1U/10V_4 Cd

Remove For Not Using SWR mode

For GIGA
Stuff Cc ,Cd

For 10/100
NA: Cc, Cd

2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42
25,39 +3VLANVCC

+1.05V_LAN TP3 R70 2.49K/F_4 LANRSET

LAN_YLED# R907 *0_4 LAN_GLED#

LED1:
FOR 8166:Stuff R908,NA R907
FOR 8161:Stuff R907,NA R908

R908 0_4 LAN_GLED#

SI ADD R907,R908 FOR LED issue

+3V R98 1K_4 ISOLATEB R99 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U5

RSET VDD10 XTAL2 XTAL1 LED0 LED1

AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 LED0/GPO LED2(LED1)

33 GND

Please add 9 GND VIAs connection with thermal PAD

MDI0+ MDI0- VDD10 MDI1+ MDI1- MDI2+ MDI2- VDD10

MDIP0 MDIN0 AVDD10(NC) MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10

RTL8166EH-CG

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

24 +1.05V_LAN_REGOUT
23 DVDDL
22 VDD10
21 PCIE_WAKE#
20 ISOLATEB
19 P
18 PCIE_RXN2_LAN_L C106 0.1U/10V_4
17 PCIE_RXP2_LAN_L C1064 0.1U/10V_4

R S T #

MDP3(NC) MDN3(NC) AVDD33(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N

LAN_CLKRQ

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN2_LAN PCIE_TXP2_LAN

8 PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R90 0_4

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# 6,30,33 PLTRST# 2,8,14,26,30,33 PCIE_RXN2_LAN 8 PCIE_RXP2_LAN 8 CLK_PCIE_LANN 8 CLK_PCIE_LANP 8 PCIE_TXN2_LAN 8 PCIE_TXP2_LAN 8

FOR GIGA: 8161GSH: AL008161004
FOR 10/100 : 8166EH: AL008166001

Right SIDE USBX1 and LAN CONN

For 10/100 only

R873 0_4 *MCM2012B900GBE L8 MDI0+_R MDI0-_R R874 0_4

R875 0_4 *MCM2012B900GBE L12 MDI1+_R MDI1-_R R899 0_4

R902 *0_4 *MCM2012B900GBE L28 MDI2+_R MDI2-_R R904 *0_4

R905 *0_4 *MCM2012B900GBE L29 MDI3+_R MDI3-_R R906 *0_4

28,30

L47 MCM2012B900GBE

USBP9+ USBP9- +5VS5 USBPW_ON#

CN2 LAN USB CONN

USBP9+_R USBP9-_R USBPW_ON# LAN_GLED# +3VLANVCC LAN_YLED# MDI0+_R MDI0-_R MDI1+_R MDI1-_R MDI2+_R MDI2-_R MDI3+_R MDI3-_R

C107 220P/50V_4 USBPW_ON#

C43 1000P/50V_4 LAN_YLED#
C39 1000P/50V_4 LAN_GLED#
C45 0.1U/10V_4 +3V

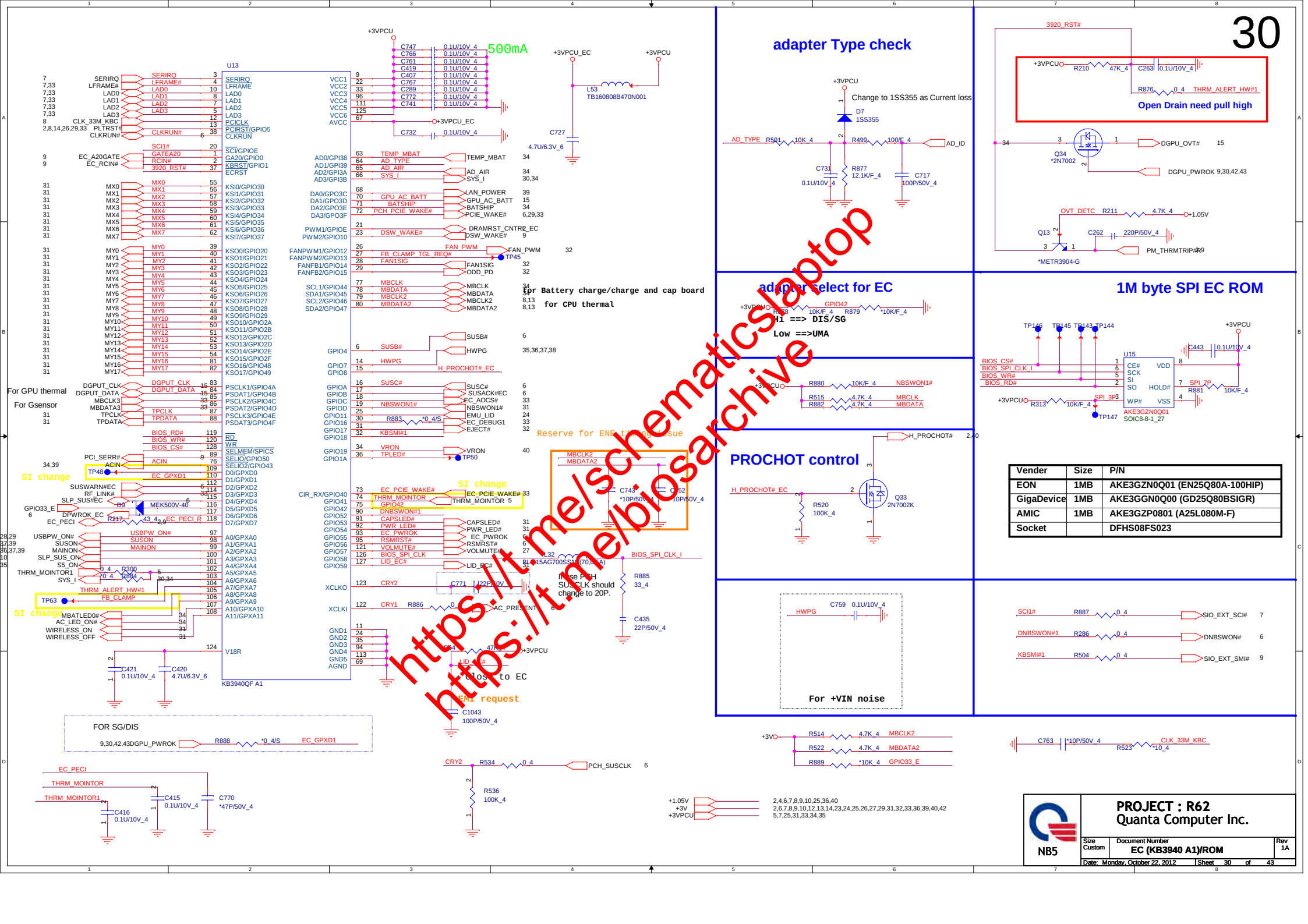
+5VS5 C57 0.1U/10V_4

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

Date: Monday, October 22, 2012 Sheet 29 of 43



Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3940 A1)/ROM	1A

Date: Monday, October 22, 2012 Sheet 30 of 43

KEYBOARD Con.

30 MY[0..17] MY[0..17]
30 MX[0..7] MX[0..7]

KB CONN 50698-03201-001-32p-l
DFFC32FR035

P/N update

MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17

SATA_LED

C902 *AVLC 5S
SATA_LED# SATA_LED#
ACC_LED# SATA_R_LED1
R734 39_6 +3V
R733 200/F_6
LED2 LED 3P WHITE/AMBER (Amber)
C899 *AVLC 5S

KEYBOARD PULL-UP

RP2: MY6 MY3 MY12 MY13 MY15 MY10 MY11 MY14
+3VPCU *10P8R-8.2K
RP1: MY9 MY0 MY5 MY1 MY8 MY7 MY4 MY2
+3VPCU *10P8R-8.2K
R173 R176 *8.2K_4 MY16 MY17

MY5 C109 MY6 C142 MY3 C145 MY7 C1070 MY8 C141 MY9 C76 MY10 C173 MY11 C169 *220P/50V_4

MY1 C128 MY2 C136 MY4 C139 MY0 C1071 MX4 C82 MX6 C73 MX3 C104 MX2 C97 *220P/50V_4

MX7 C1072 MX0 C1073 MX5 C90 MX1 C1074 MY12 C1075 MY13 C152 MY14 C1076 MY15 C190 MY16 C201 MY17 C206 *220P/50V_4

CAPSLED# R185 R191 200/F_6
MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R
CN6

MUTE_LED_CNTL Q6 2N7002K R147 10K/F_4

SI, add Mute LED feature

EC KB3920 has included K/B pull-up resistor and function

R195 *200/F_6 WIRELESS_ON_R Q52 DRC5144E0L WIRELESS_ON
R208 *200/F_6 WIRELESS_OFF_R Q9 DRC5144E0L WIRELESS_OFF
R199 1K/F_4

PWR_LED

+3VPCU R440 360_4 LED1 3P WHITE LED
C601 *AVLC 5S DEEP_PWRLED#
SATA_LED# C1077 1000P/50V_4
DEEP_PWRLED# C604 1000P/50V_4

POWER BOTTON CONNECT

100mA
C116 *4.7U/6.3V_6
C114 1U/10V_4
C113 0.1U/10V_4
+3VPCU
30 LID_EC#
30 NBSWON1#
PWR_LED# R116 *0_4 30,31
DEEP_PWRLED# R117 0_4
PWR_LED1#
CN4
PWR BTN CONN
DFFC06MR001
88513-0601-6P-L-SMT

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

C110 PWR_LED# *0.1U/10V_4
C112 LID_EC# 0.1U/10V_4
C111 NBSWON1# 0.1U/10V_4

+3VPCU R120 10K/F_4
Q5 DRC5144E0L
PWR_LED# 30,31
C135 0.1U/10V_4
DEEP_PWRLED#
for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.

+3VSUS R890 4.7K_4 TP_SMB_CLK
R323 4.7K_4 TP_SMB_DATA

change to +3VSUS
close conn

+3VSUS R891 4.7K_4 TPCLK
R892 4.7K_4 TPDATA

C429 10P/50V_4
TPCLK L34 TB160808B470N001
TPDATA L33 TB160808B470N001
C428 10P/50V_4
CN7
TPCLK-1
TPDATA-1
TP_SMB_DATA
TP_SMB_CLK
TOUCH PAD CONN
DFFC06MR001
88513-0601-6P-L-SMT

25 mils

C880 *10P/50V_4
C878 *10P/50V_4
+3VSUS C430 0.1U/10V_4

Change footprint to 88513-0601-6P-L-SMT

+3VSUS
Q19 *2N7002DW
TP_SMB_CLK SMB_PCH_CLK 8
TP_SMB_DATA SMB_PCH_DAT 8

PV , HP request Image sensor
SMBUS reserve to PCH

+3VPCU +5V +3VSUS +3V
5,7,25,30,33,34,
7,10,23,25,27,32
39
2,6,7,8,9,10,12,1
27,29,30,32,33,36,39,40,42

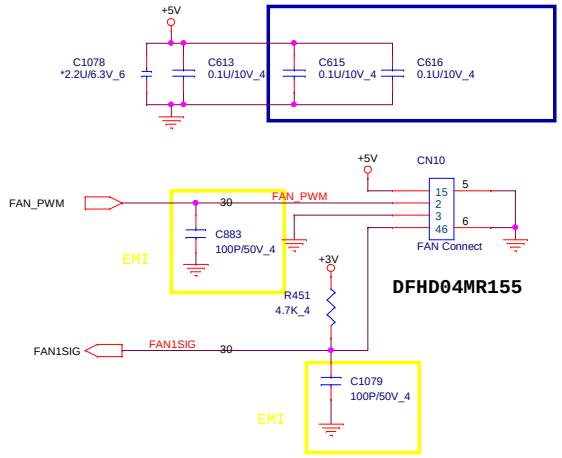
NB5

PROJECT : R62
Quanta Computer Inc.

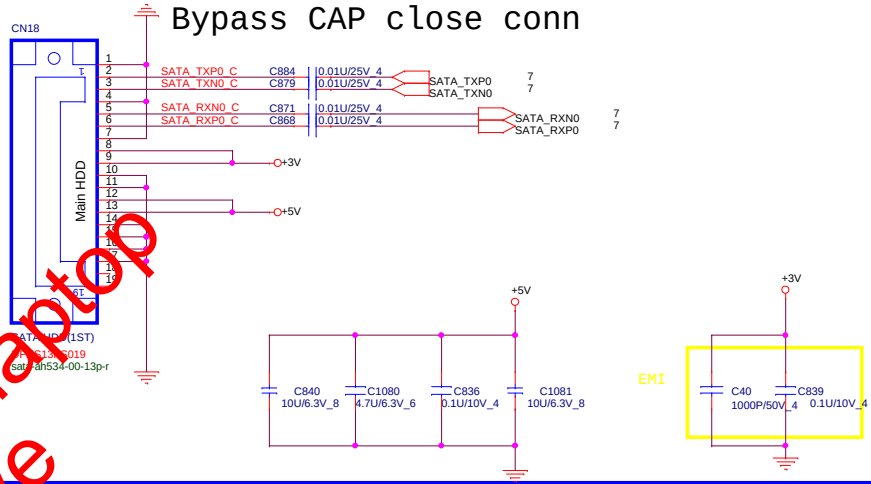
Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

Date: Monday, October 22, 2012 Sheet 31 of 43

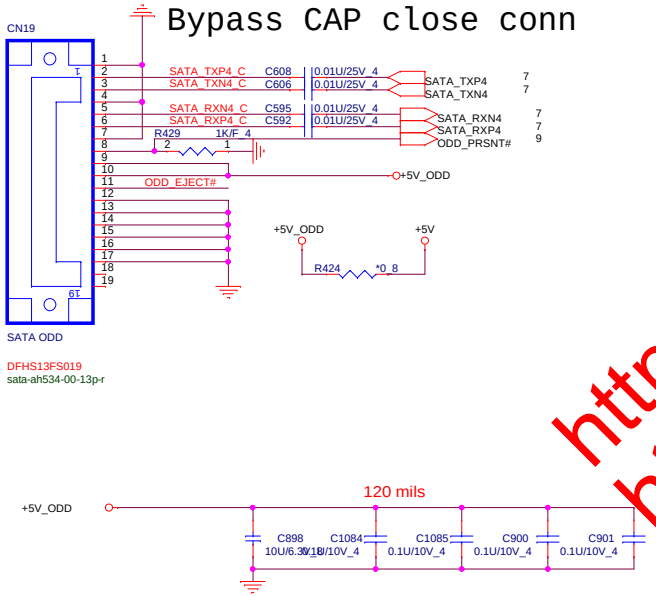
CPU FAN



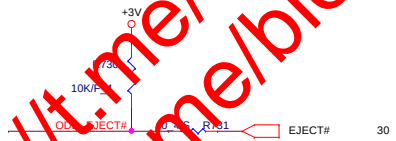
SATA HDD CONNECTOR



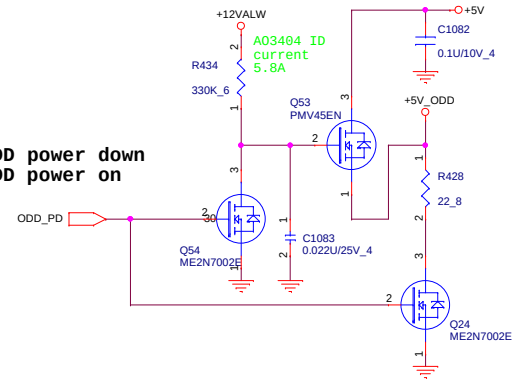
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on



+3V	2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
+3VPCU	5,7,25,30,31,33,34,35
+5V	7,10,23,25,27,31,33,39
+12VALW	34,39,43

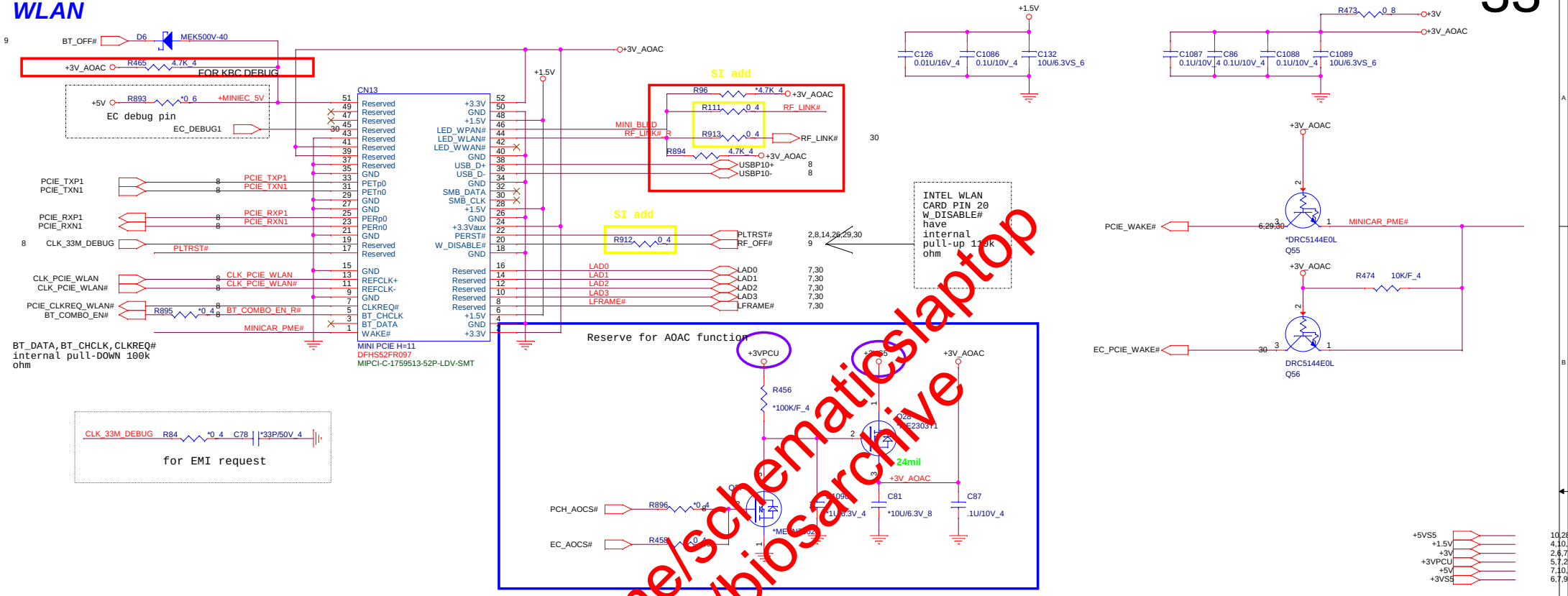
NB5

PROJECT : R62
Quanta Computer Inc.

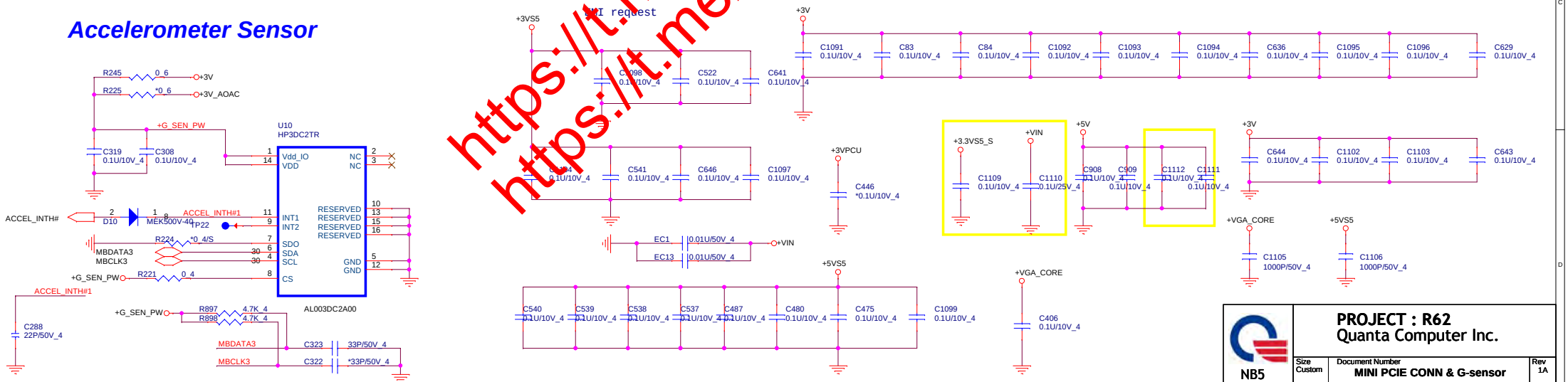
Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

Date: Monday, October 22, 2012 Sheet 32 of 43

Mini PCI-E Card 1
WLAN



Accelerometer Sensor



NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN & G-sensor	1A
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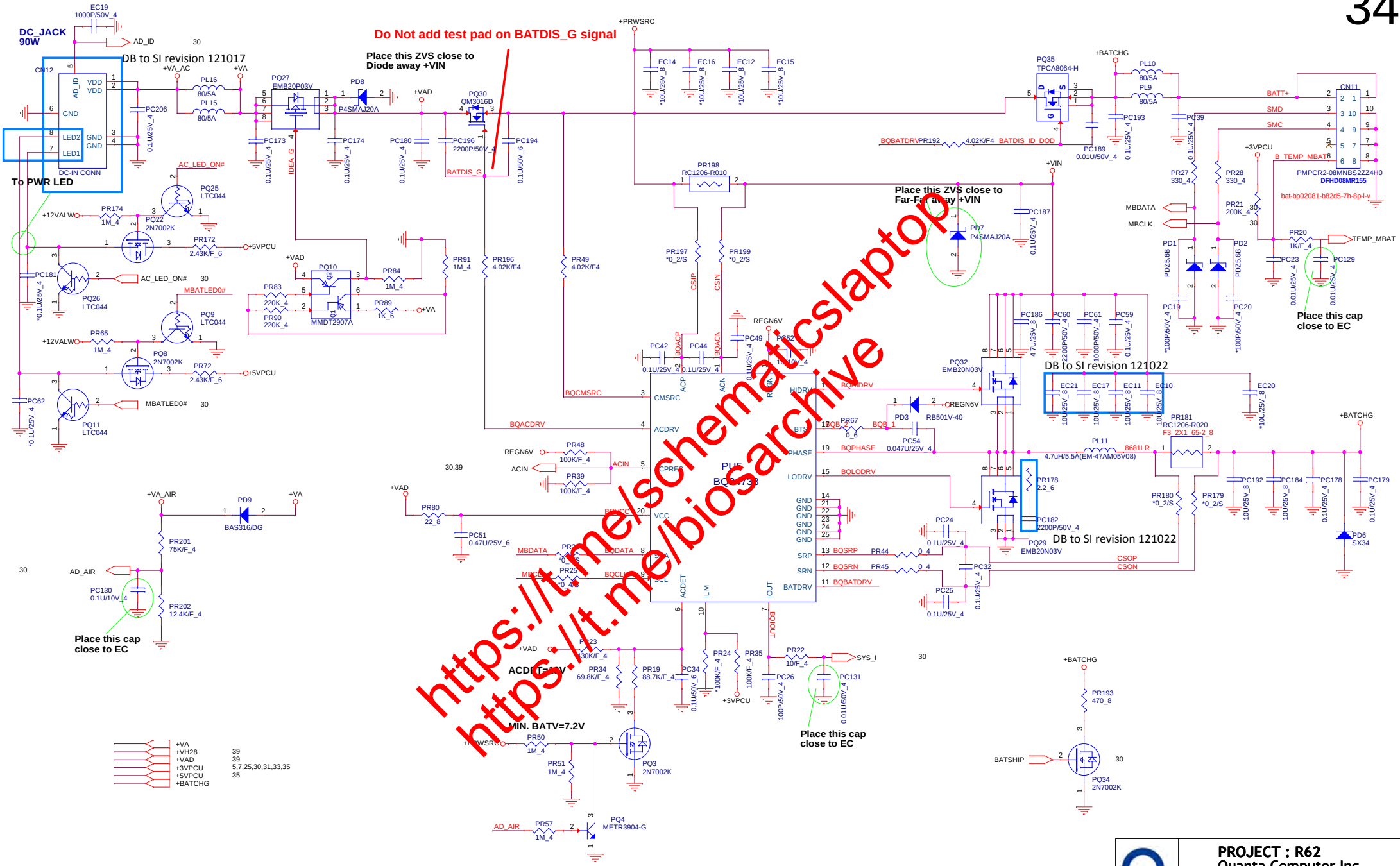
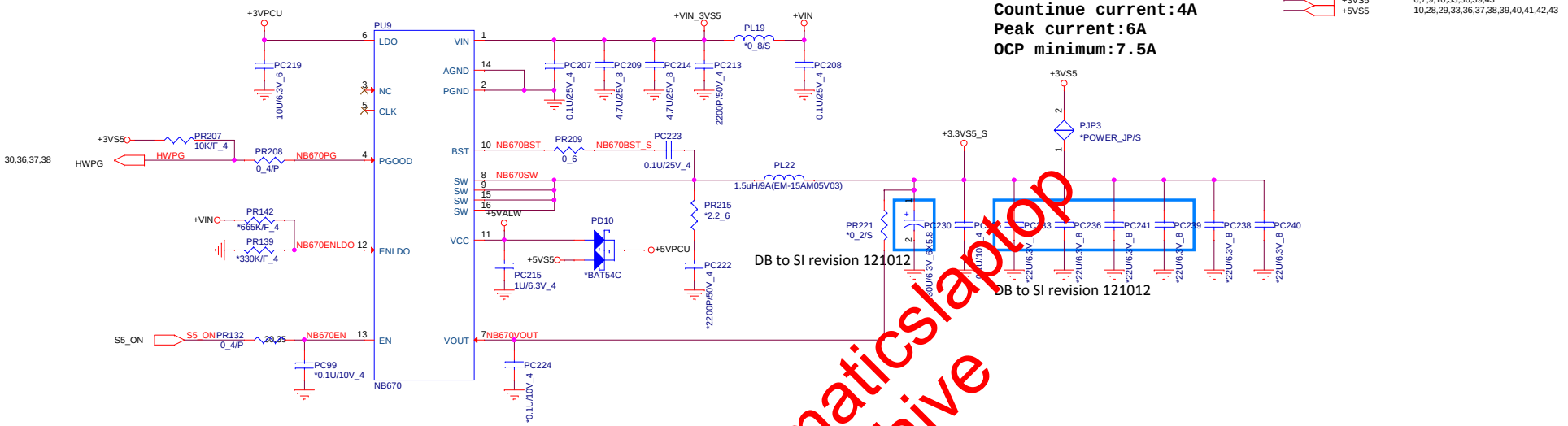
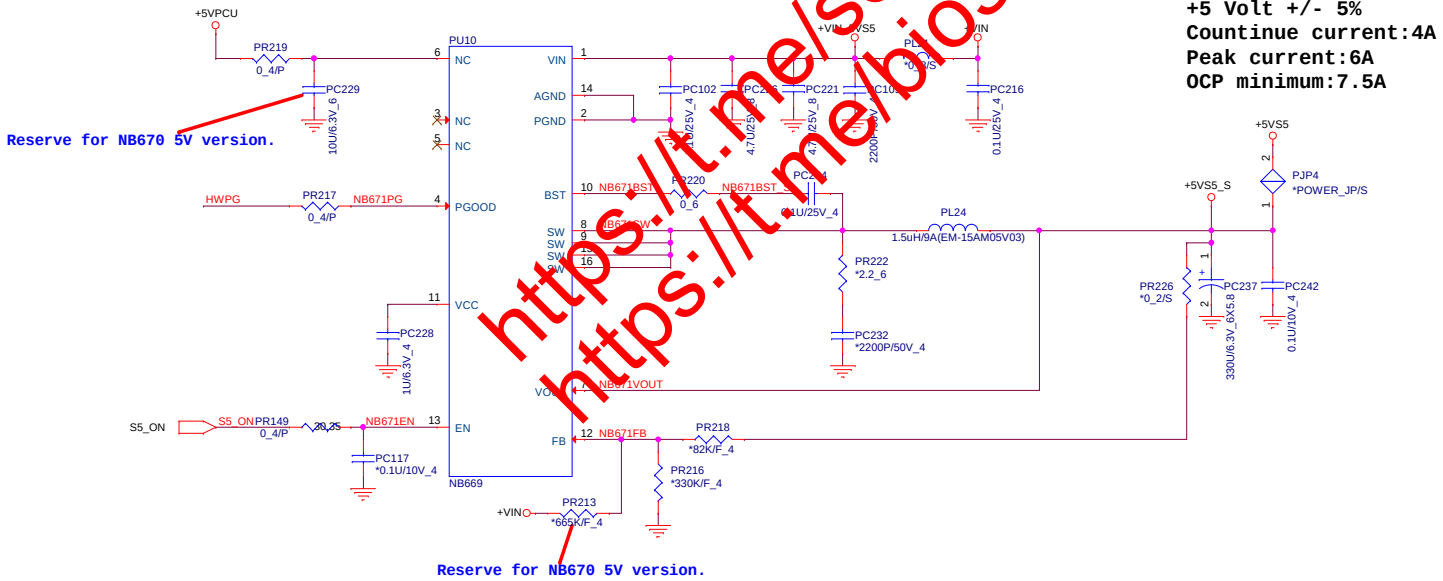
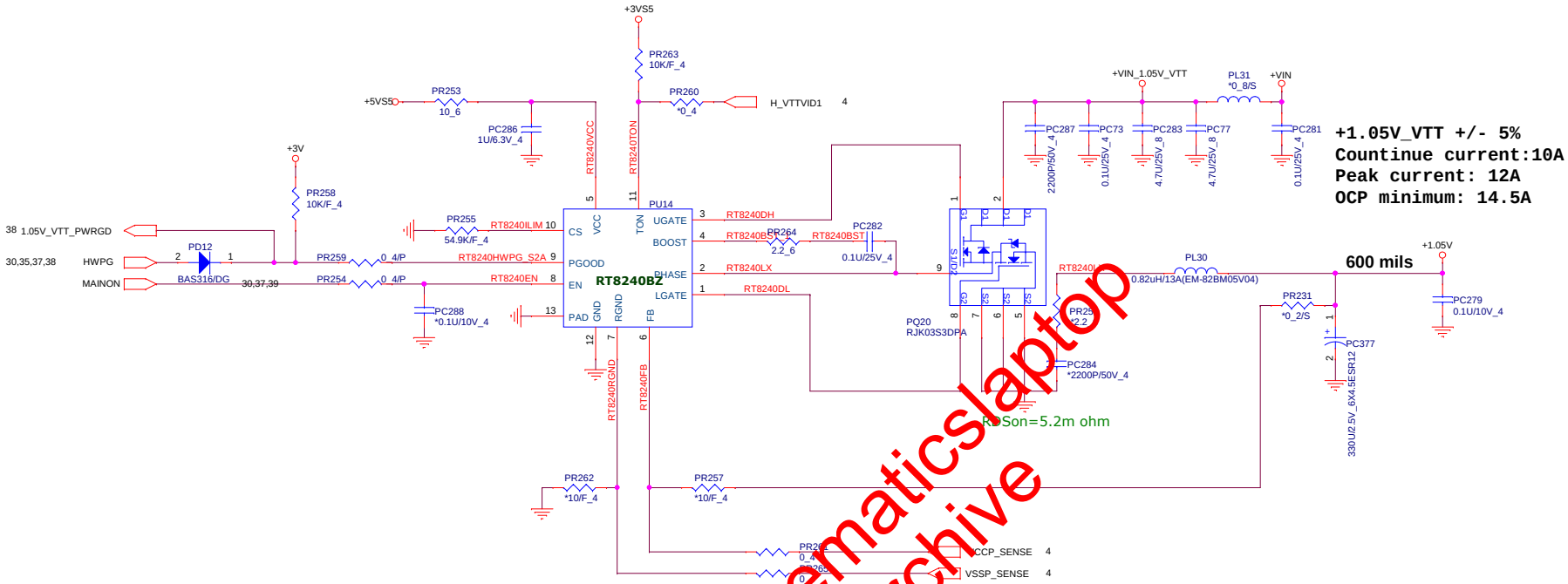


NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 34 of 43	





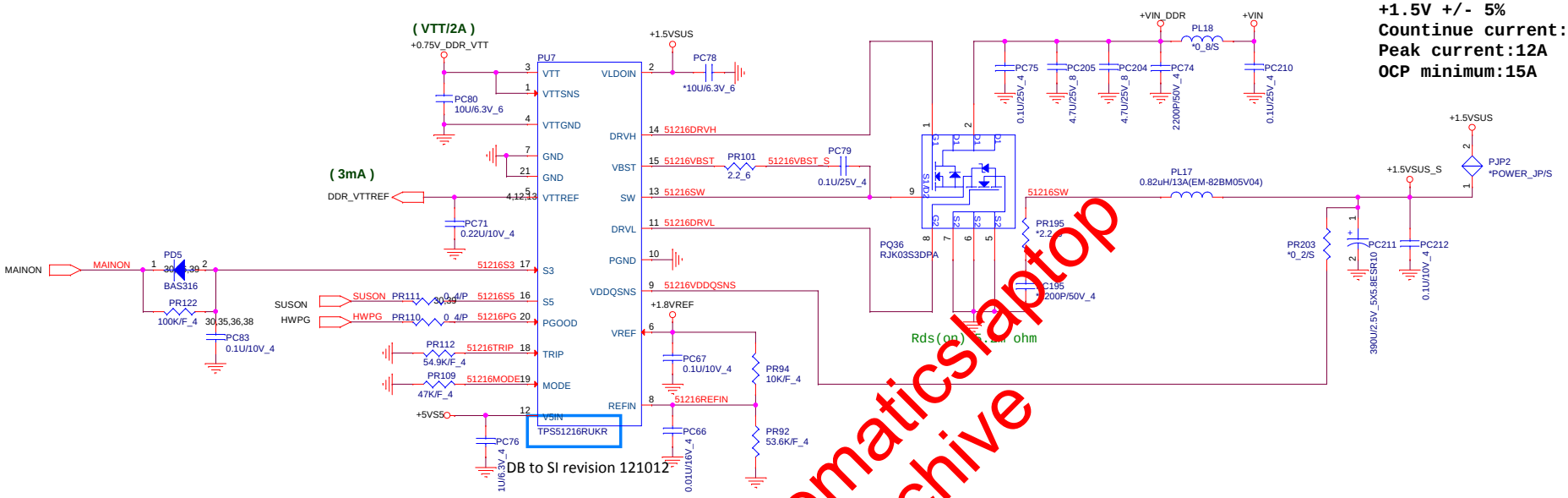
NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VPCU(RT8243A)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 35 of 43	



NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: 1.05V(RT8228BZ)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 36 of 43	

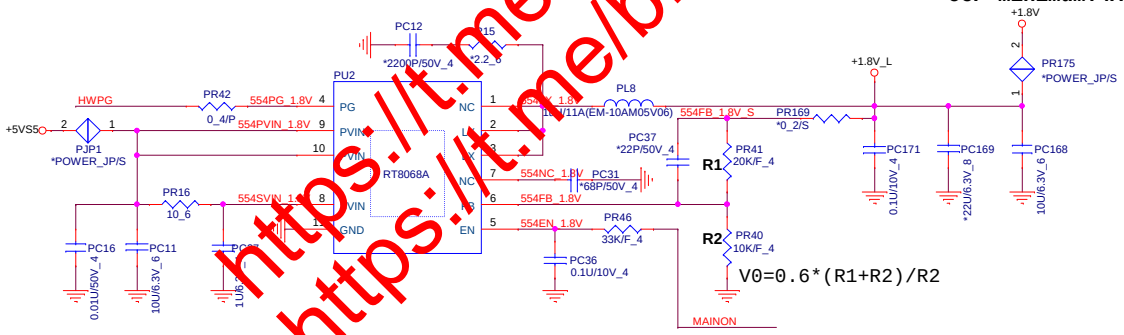
+1.5VSUS 2,4,12,13,43

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum:15A



DB to SI revision 121012

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

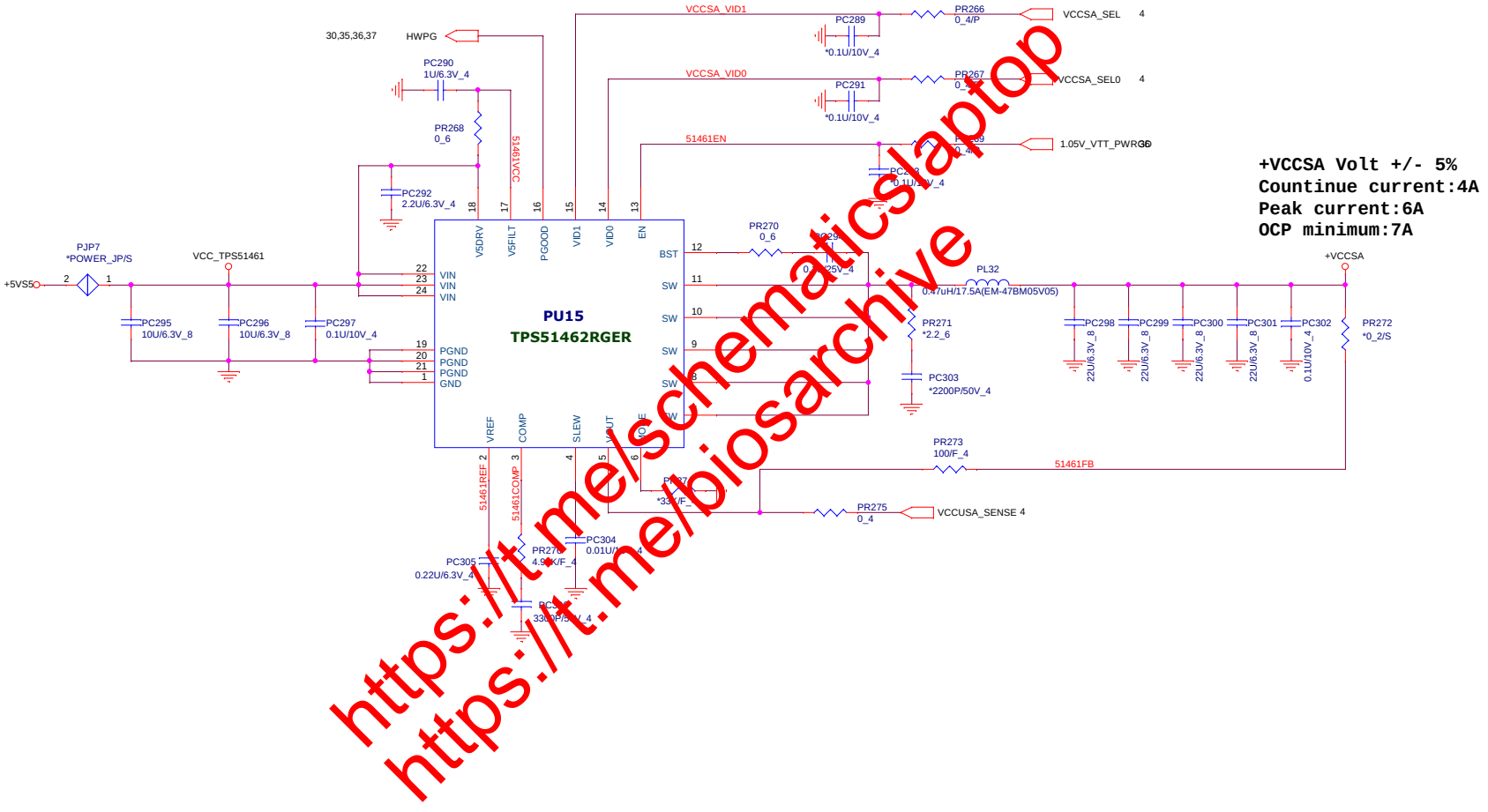


NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3L(APW8819)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 37 of 43	

TPS51462RGER/AL051462000

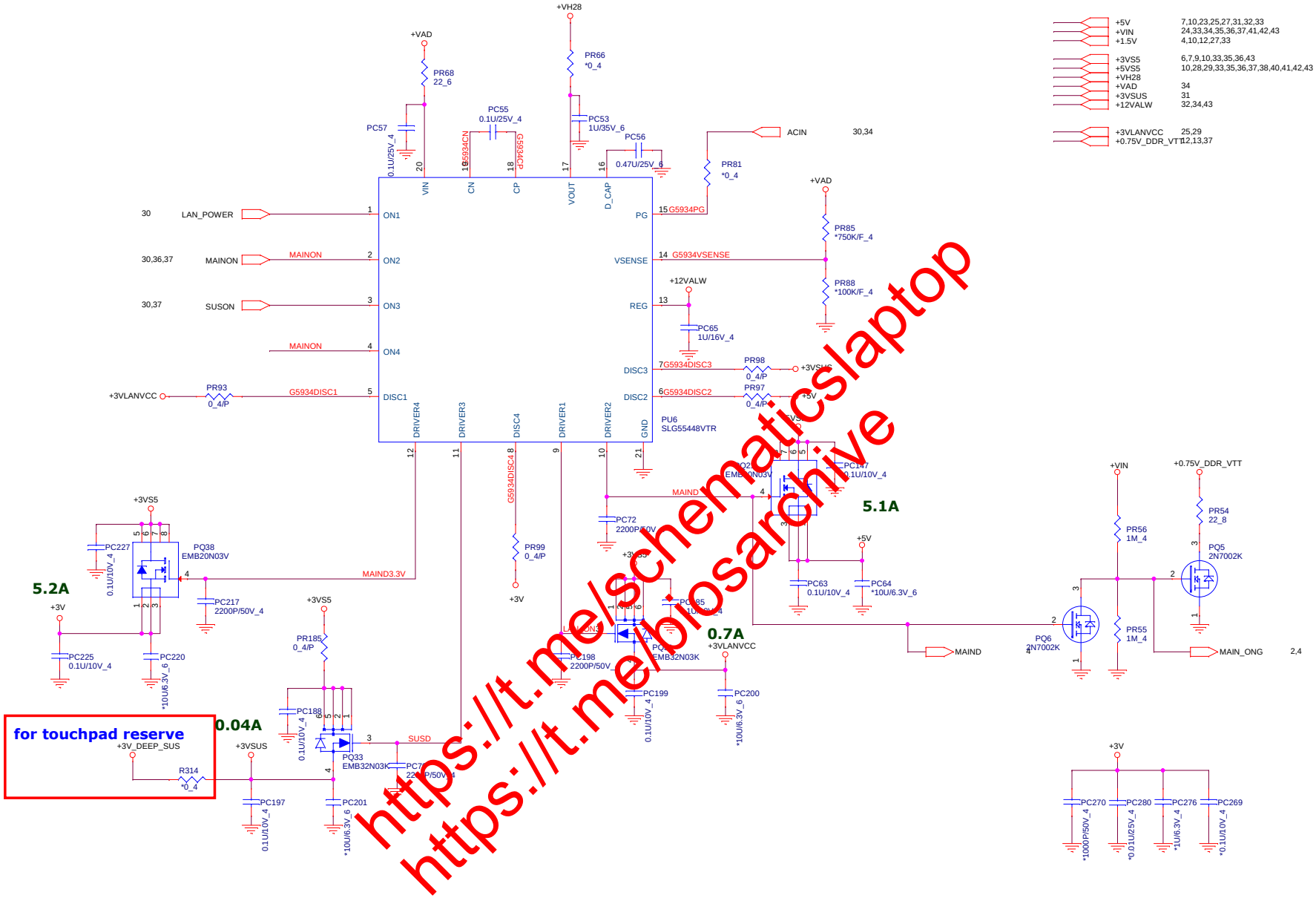
For CPU SV system agent voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

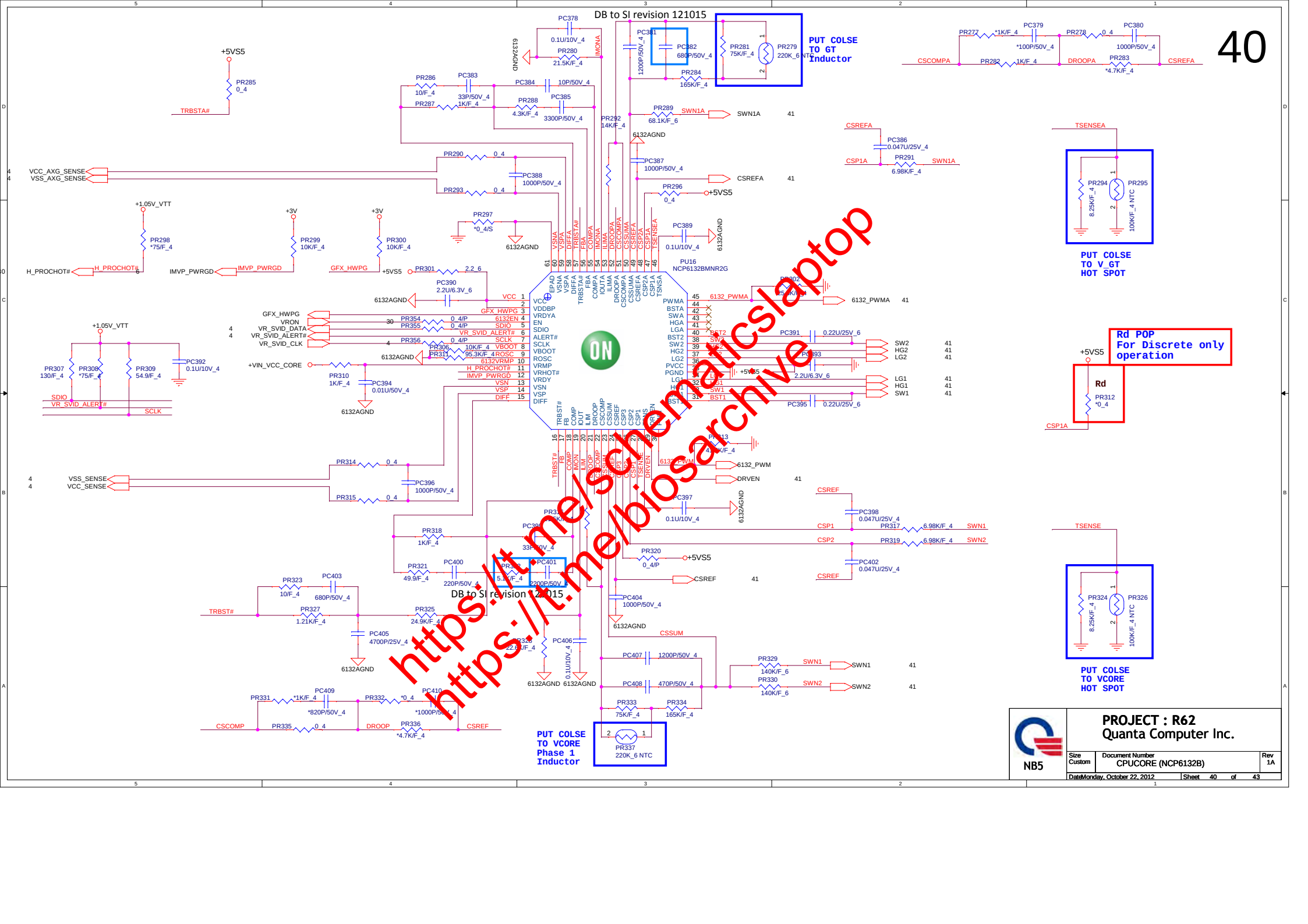


+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3L(APW8819)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 38 of 43	



NB5	PROJECT : R62 Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (G5934)	Rev: 1A
Date: Monday, October 22, 2012	Sheet 39 of 43	


DB to SI revision 121015
PUT COLSE TO GT Inductor
PUT COLSE TO V_GT HOT SPOT
Rd POP For Discrete only operation
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Phase 1 Inductor
PU16 NCP6132BMNR2G
DB to SI revision 121015
https://t.me/schematicslaptop
https://t.me/biosarchive
PROJECT : R62
Quanta Computer Inc.
NB5
Size Custom
Document Number CPUCORE (NCP6132B)
Rev 1A
Date Monday, October 22, 2012
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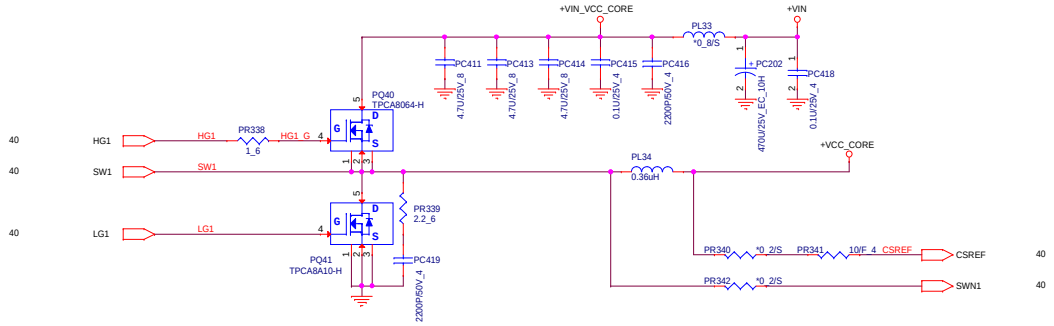
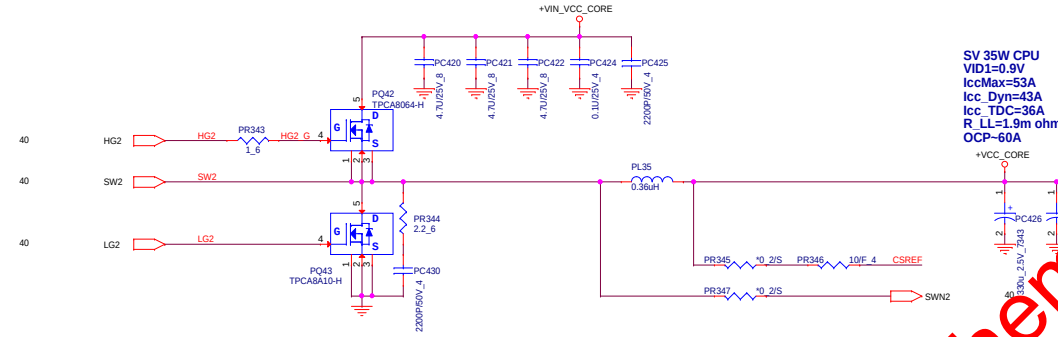
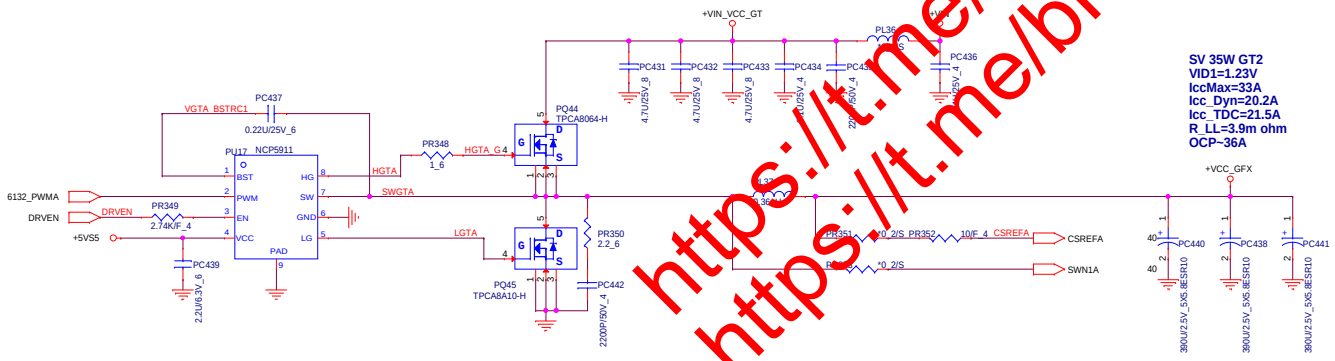




SV 35W CPU
VID1=0.9V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~60A



SV 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~36A

NB5	PROJECT : R62 Quanta Computer Inc.		
	Size: C	Document Number: NCP5911	Rev: 1A
	Date: Monday, October 22, 2012	Sheet 41 of 43	

VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

+VGA_CORE 18,33,43

42

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

PU8 NCP3218G

DCR_1.4m ohm

DB to SI revision 121018

DB to SI revision 121015

DB to SI revision 121022

DB to SI modify on 1008

DB to SI revision 121012

This NTC Close to Phase 1 MOSFET

Close to Phase 1 Inductor

Shortest the net trace

PROJECT : R62
Quanta Computer Inc.

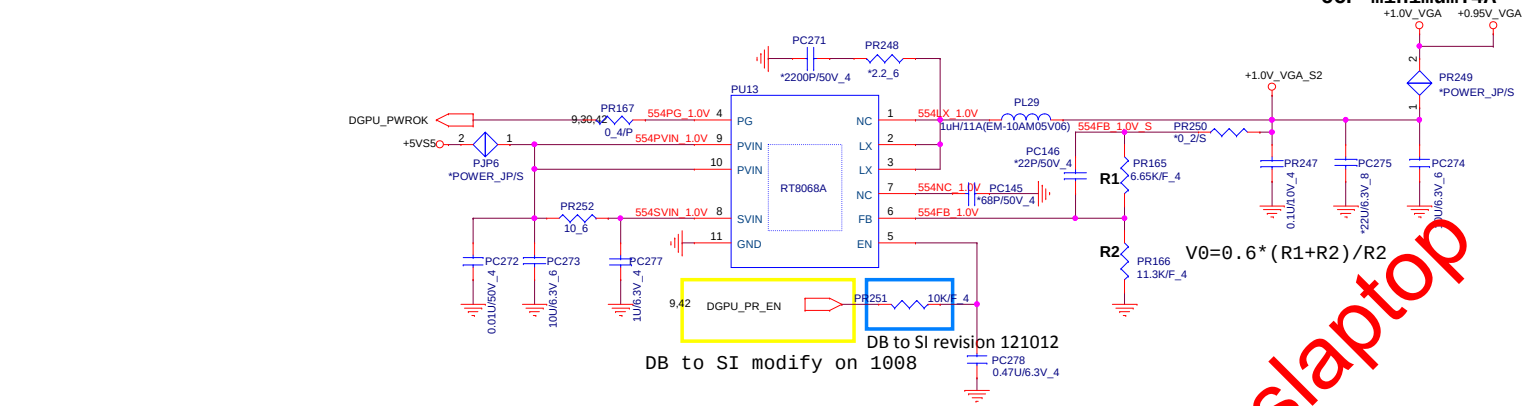
NB5

Size Custom | Document Number +VGACORE NCP3218G) | Rev 1A

Date: Monday, October 22, 2012 | Sheet 42 of 43

R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

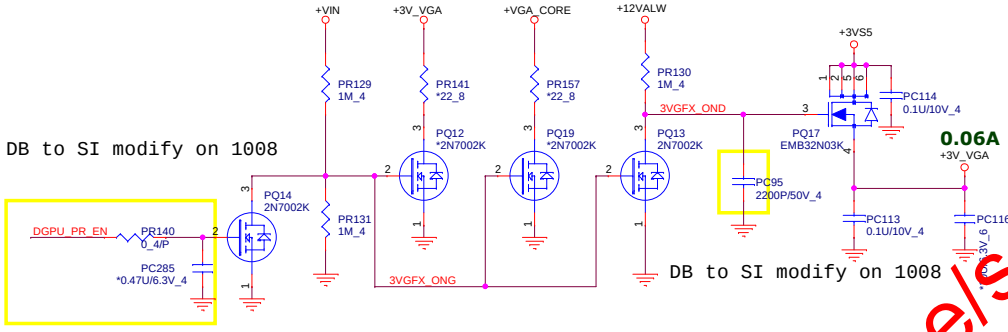
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



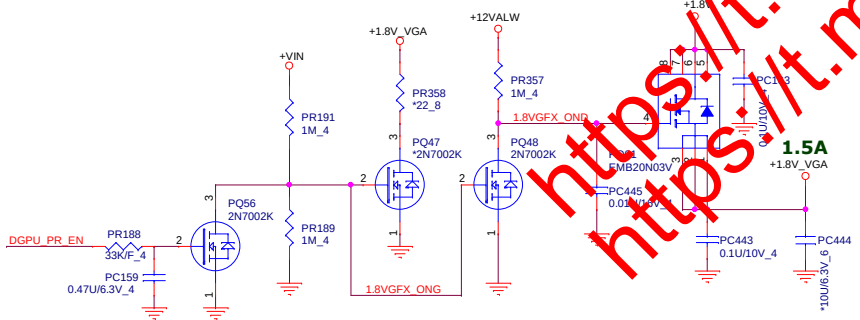
DB to SI modify on 1008

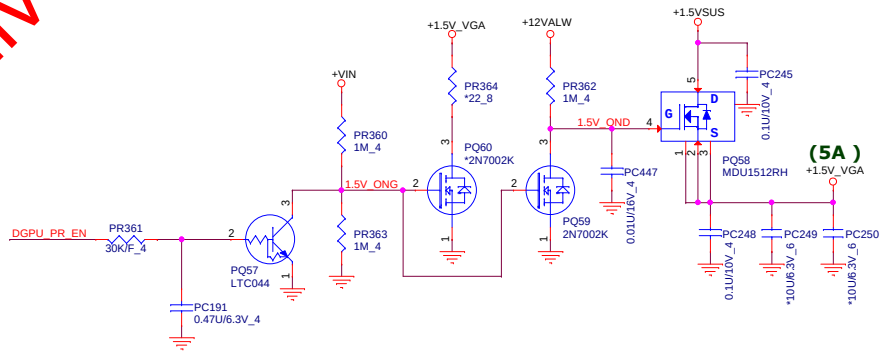
DB to SI revision 121012

DB to SI modify on 1008



DB to SI modify on 1008





+1.8V_VGA 15,16,18,19,25
+1.0V_VGA 14,16,18,19
+3V_VGA 18

NB5

PROJECT : R62
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A
Date: Monday, October 22, 2012	Sheet 43 of 43	