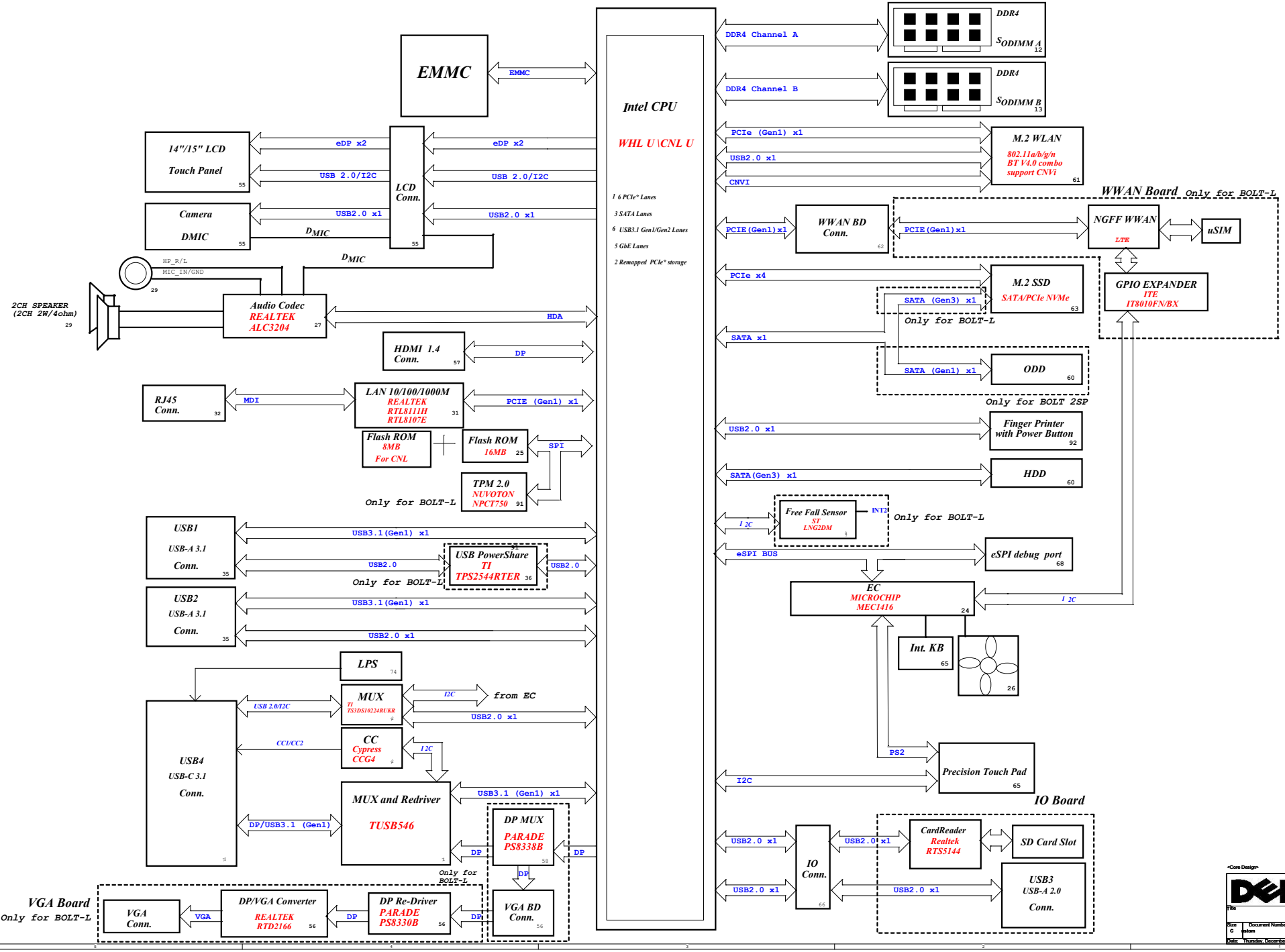
Project Code : QRQY00000009
PCB P/N : 17938
Revision : 1

Bolt WHL Block Diagram



CHARGER ISL95522/ISL95538 44

INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	

SYSTEM DC/DC TPS51225RUKR-GP 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR
	3D3V_S5
	5V_PWR
	5V_S5

CPU Core Power NCP81208MNTXG 46~50
NCP81382MNTXG x 2
NCP81382MNTXG (23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS RT8231AGQW-GP APL5930KAI-TRG 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3
3D3V_S5	0D6V_S0
	2D5V_S3

CPU VCCPRIM_CORE 1V 11

INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A AOZ2262QI-10-GP-U 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V APL5930KAI-TRG 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 TPS22966DPUR-GP 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e) TPS22961DNYT 40

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA AO3419L 86

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE ISL62771HRTZ-GP-U 85

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V VGA_S0 Y8288RAC-GP 86

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

<Core Design>

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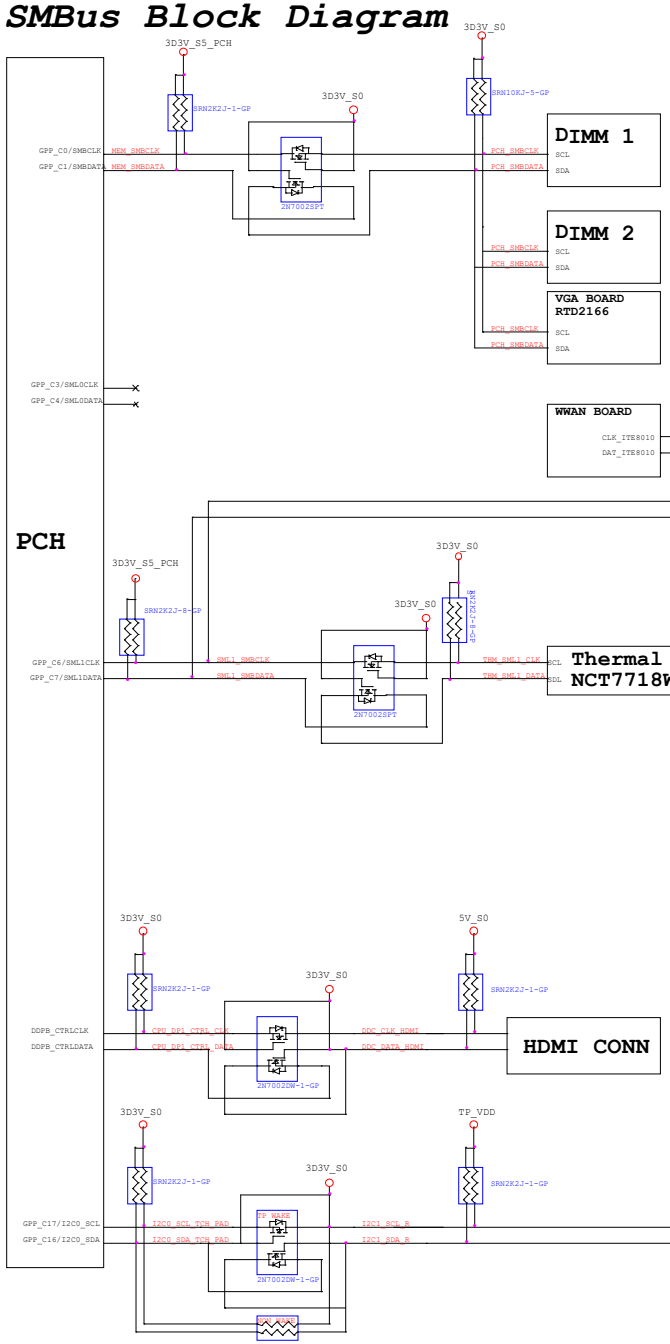
Title: Block Diagram

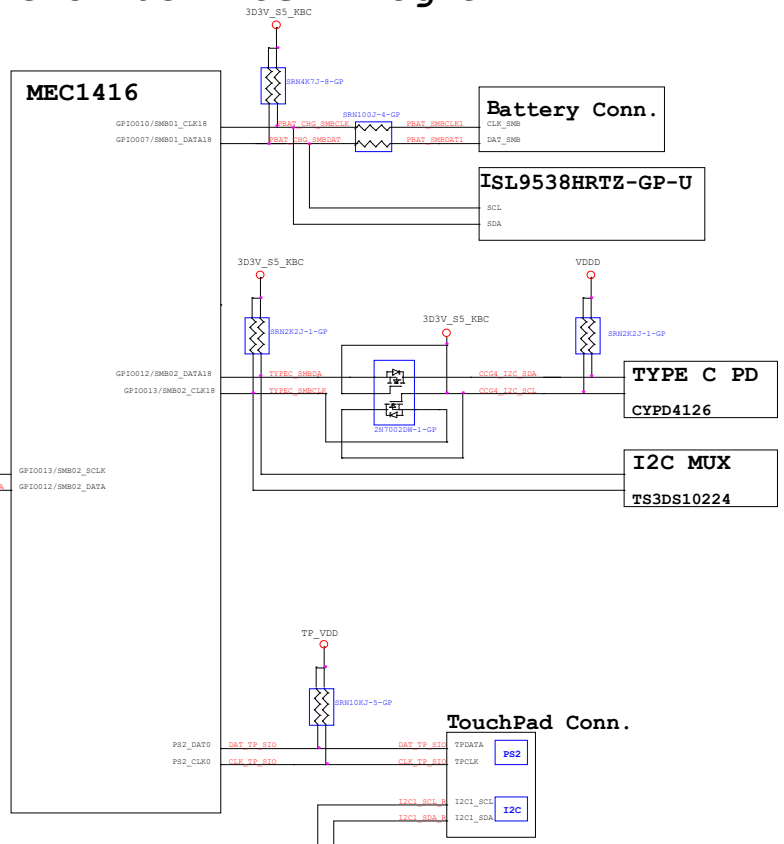
Size	Document Number	Rev
C	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 2 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



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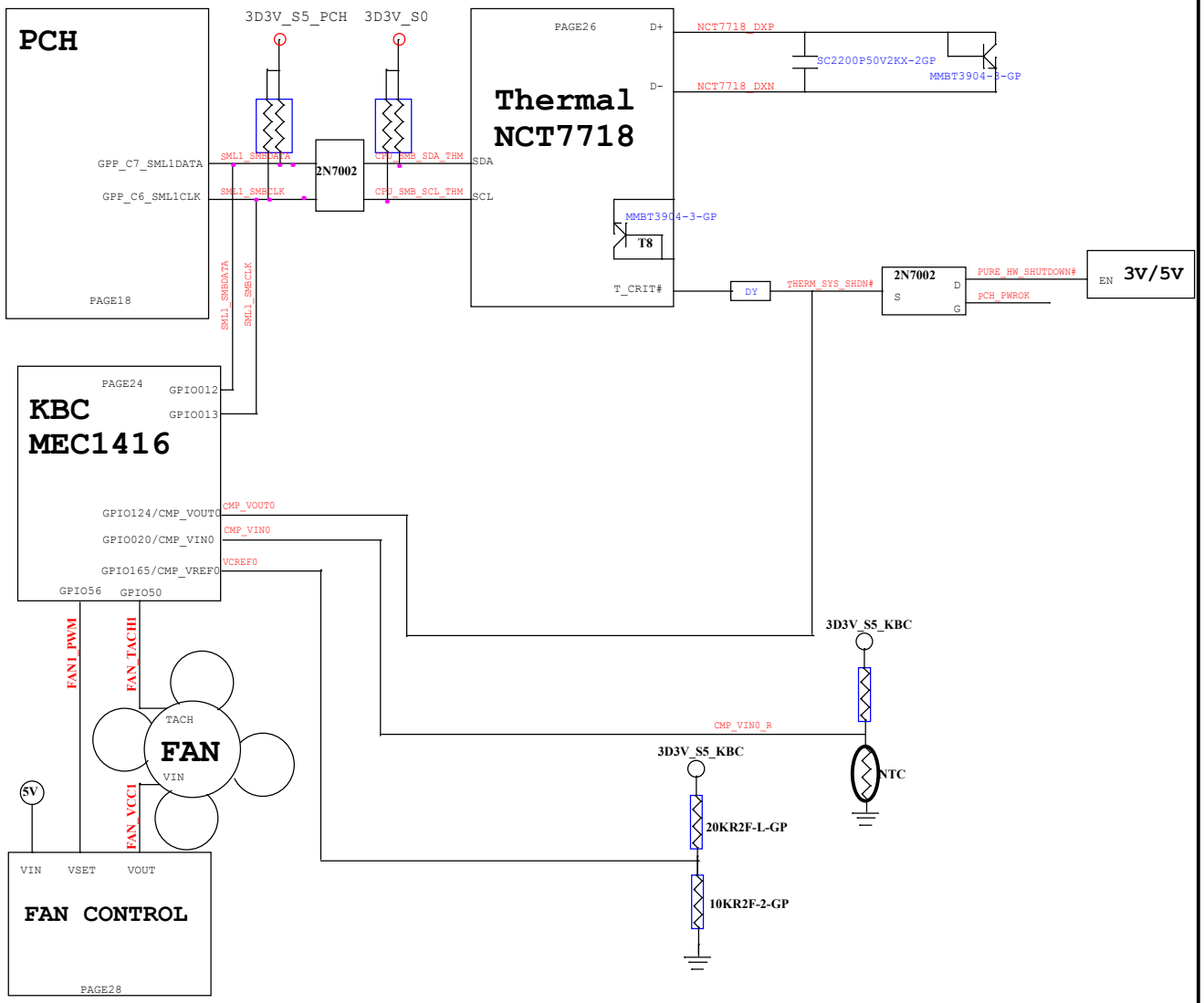
Title: SMBUS Block Diagram

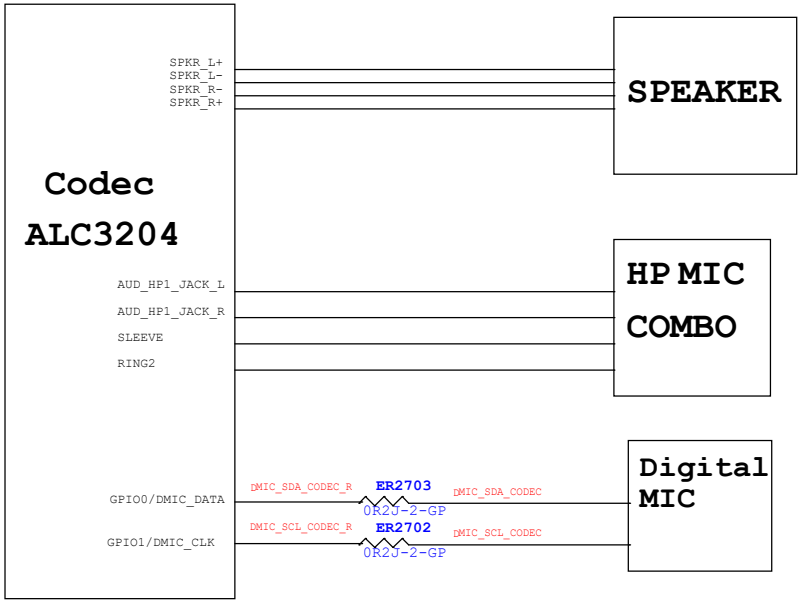
Size	Document Number	Rev
Custom	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 104 of 105

Thermal Block Diagram



Audio Block Diagram



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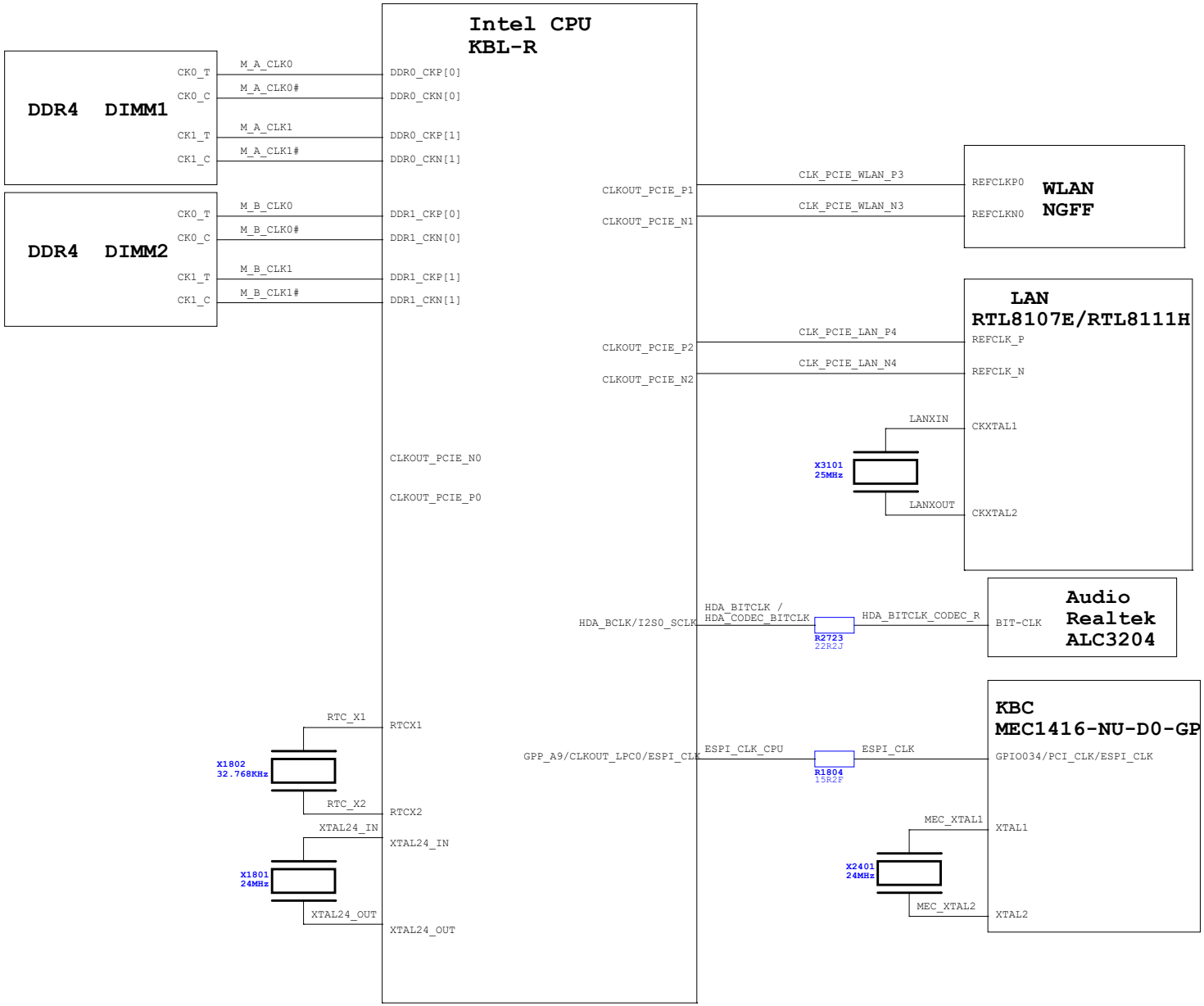
Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
C ustom	BOLT WHL	1

Date: Thursday, December 27, 2018 | Sheet 105 of 105

CLK Block Diagram



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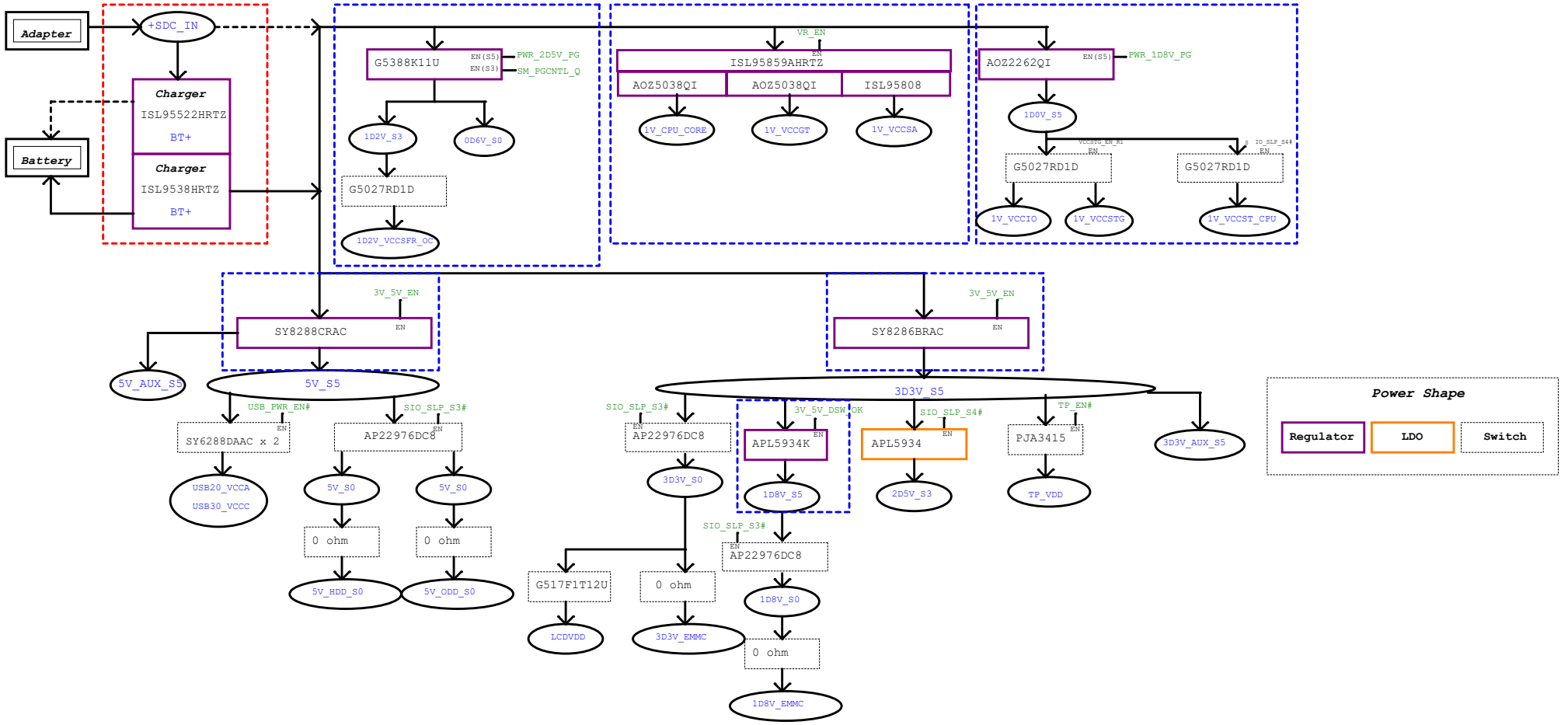
Title: CLK Block Diagram

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 | Sheet 100 of 105



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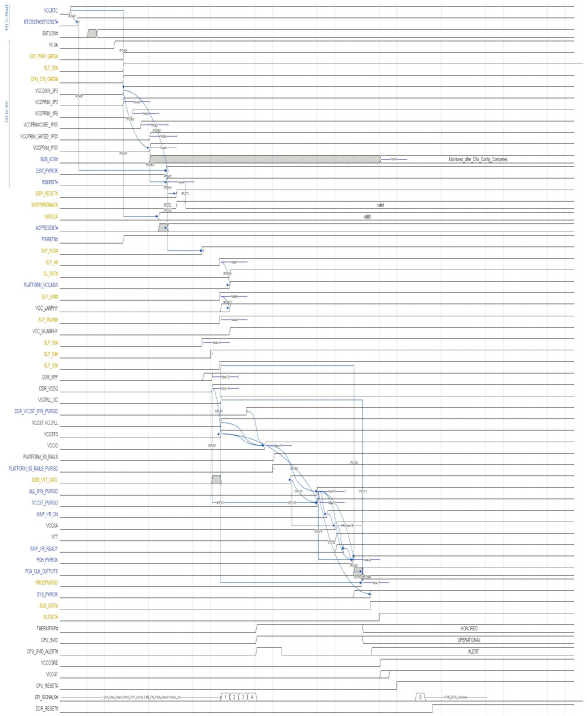
Title: Power Block Diagram

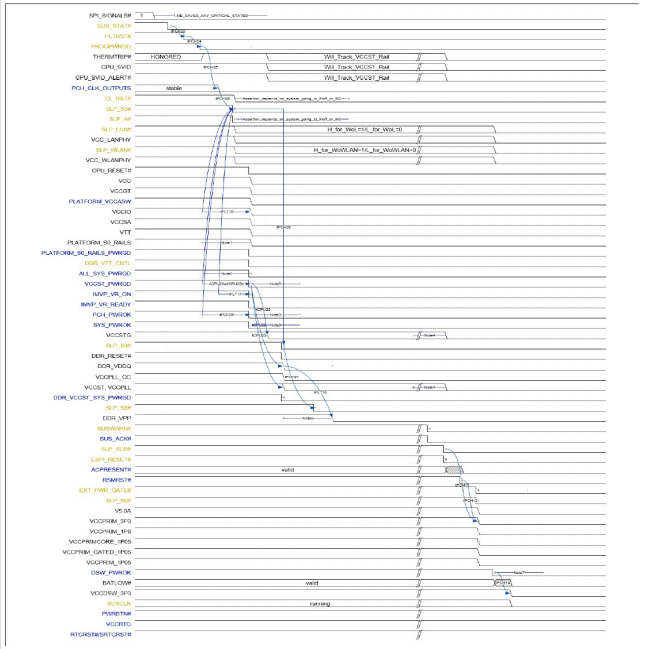
Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 | Sheet 103 of 105

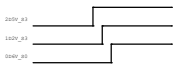
CNL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



WHL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

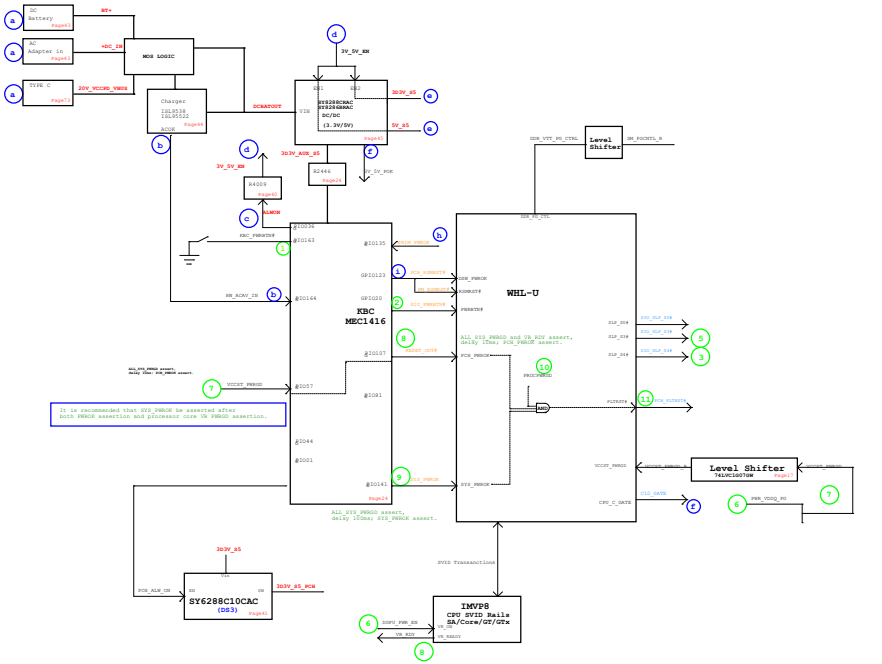


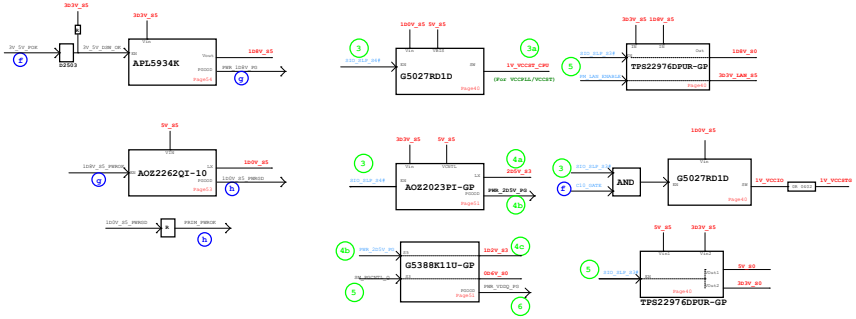
For DDR4 power sequence



Tulip WHL POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

Red: Power Rail
Orange: Output from KBC
Light Blue: Output from CPU

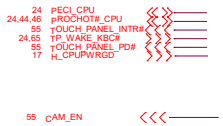


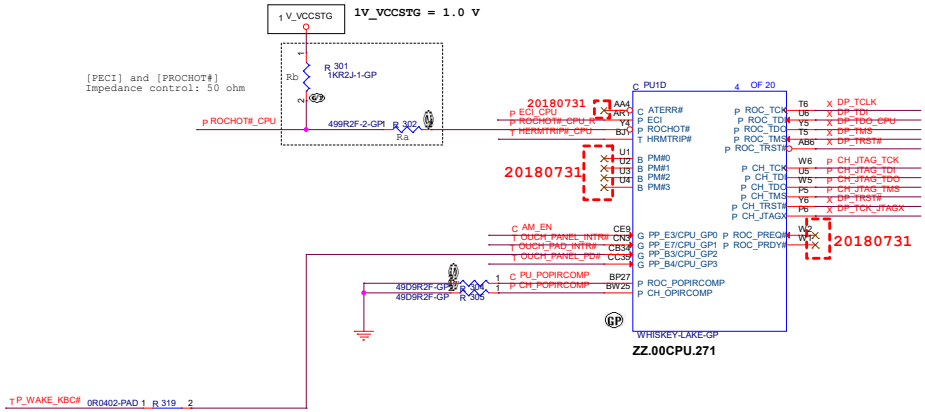


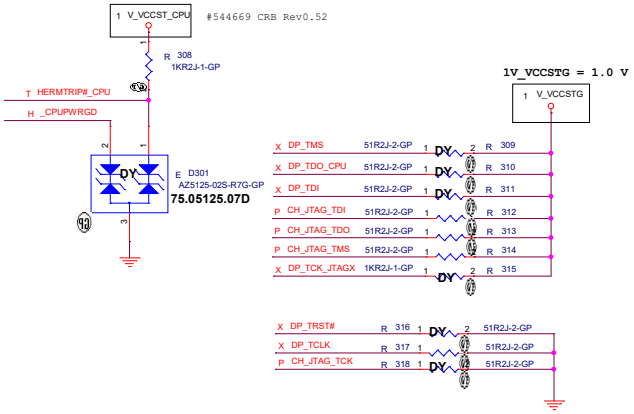
1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 9 → 10 → 11

a → b → c → d → e → f → g → h → i

Main FUNC = CPU







(#575412) PROCHOT# Routing Guidelines

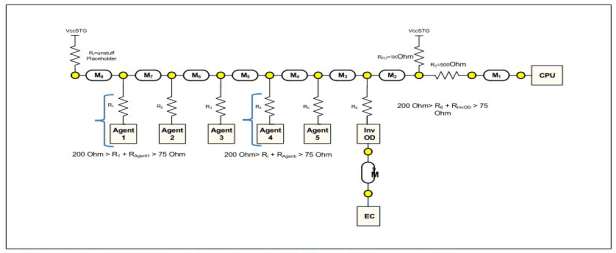


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values		Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω					
Platform resistors tolerances		± 5%					

BOLT L 14 EMMC

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Title: *(Reserved)*

Size: A 2 | Document Number: *B OLT WHL* | Rev: *1*

Date: Thursday, December 27, 2018 | Sheet 3 of 105

Main FUNC = CPU

HDMI 1.4B

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3

57 CPU_DP1_CTRL_CLK
57 CPU_DP1_CTRL_DATA
57 CPU_DP1_HPD

TO DP MUX

58 P2_DDI_TX_N0
58 P2_DDI_TX_P0
58 P2_DDI_TX_N1
58 P2_DDI_TX_P1
58 P2_DDI_TX_N2
58 P2_DDI_TX_P2
58 P2_DDI_TX_N3
58 P2_DDI_TX_P3
58 P2_AUX_CPU_P
58 P2_AUX_CPU_N
58 P2_HPD_CPU

EDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 EDP_HPD
24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN
61 CNVI_EN#

5.2.7 Compensation Signal Routing Guidelines

Table 5-20. eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	500 mils

Note: Must maintain low DC resistance routing (<5.1Ω)

5.2.8 eDP* Disabling and Termination Guidelines

Table 5-21. eDP* Disabling and Termination Guidelines

Pin name	Recommendation
eDP_TXN/P[3:0]	No connect
EDP_AUXN/P	No connect
GPP_E17/EDP_HPD/DISP_MISC#	Pull down to ground via 100k ohm resistor
EDP_RCOMP	Pull up to VCCIO via 100 ohm resistor
EDP_UTILS	No connect

3 D3V_S0
R N401
1 2 3 4 8 7 6 5
C PU_DP2_CTRL_DATA
C PU_DP2_CTRL_CLK
C PU_DP1_CTRL_DATA
C PU_DP1_CTRL_CLK
SRN2K2J-4-GP
SWAP 20180630

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Table 9-1. Pin Straps (Sheet 3 of 4) #566439

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVI disable.

HDMI 1.4B

TO DP MUX

PU1A 1 OF 20
Port B: DI1_TXN0 DI1_TXP0 DI1_TXN1 DI1_TXP1 DI1_TXN2 DI1_TXP2 DI1_TXN3 DI1_TXP3
Port C: DI2_TXN0 DI2_TXP0 DI2_TXN1 DI2_TXP1 DI2_TXN2 DI2_TXP2 DI2_TXN3 DI2_TXP3
Port A: DP_TXN0 DP_TXP0 DP_TXN1 DP_TXP1 DP_TXN2 DP_TXP2 DP_TXN3 DP_TXP3
DP_AUX_N DP_AUX_P DP_DISP_UTIL ISP_UTILS
DI1_AUX_N DI1_AUX_P DI2_AUX_N DI2_AUX_P DI3_AUX_N DI3_AUX_P
P401 TPAD14-OP-GP
P2_AUX_CPU_N P2_AUX_CPU_P
PP_E13/DDPB_HPD0/DISP_MISC
PP_E14/DDPC_HPD1/DISP_MISC
PP_E15/DPPD_HPD2/DISP_MISC
PP_E16/DPPE_HPD3/DISP_MISC
PP_E17/EDP_HPD/DISP_MISC
CN6 PU_DP1_HPD
CM6 PU_DP2_HPD
CP7 IO_EXT_SMI#
CP6
CM7 DP_HPD
CK11 L_BKLT_EN
CG11 DP_VDD_EN
CH11 L_BKLT_CTRL
DP_BKLTEN DP_VDDEN DP_BKLTCTL
ISP_RCOMP
PP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
PP_E19/DPPB_CTRLDATA
PP_E20/DPPC_CTRLCLK
PP_E21/DPPC_CTRLDATA
PP_E22/DPPD_CTRLCLK
PP_E23/DPPD_CTRLDATA
PP_H16/DDPF_CTRLCLK
PP_H17/DDPF_CTRLDATA
WHISKEY-LAKE-GP
ZZ.00CPU.271

DP Demux

1 V_VCCIO
R 4011 24D9R2F-L-GP e DP_RCOMP_CPU AM6
WHL_CNL
2018.03.31 BOM option
R401
CNL:100 Ohm (64.10005.6DL)
WHL:24.9 Ohm (64.24R95.6DL)
C PU_DP1_CTRL_CLK CC8
C PU_DP1_CTRL_DATA CC9
C PU_DP2_CTRL_CLK CH4
C PU_DP2_CTRL_DATA CH5
1 G PP_E23_STRAP CP6
CN7
C NVI_EN# CR28
CP28
TPAD14-OP-GP P402

3 D3V_S0
S IO_EXT_SMI# 1 R 402 2 10KR2J-3-GP
add 20180512

Pin Straps (Sheet 4 of 4) #566439

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

RTC Gen 9 reset circuit_20170814
C PU_DP2_HPD R 4041 0R2J-L-GP D P2_HPD_CPU
NON_RTC_RST
R 403 100KR2J-1-GP
DP for Type-C Mux

Add RTC Gen 9 reset circuit_20170814 leakage issue
3 D3V_S5_PCH
R 406 10KR2J-3-GP
RTC_RST
RTC_RST
Q 401
2N7002KDW-T-GP
3 D3V_S5_PCH
R 405 10KR2J-3-GP
RTC_RST
C PU_DP2_HPD
D P2_HPD_CPU
75.27002.F7C
2nd = 075.27002.0E7C

BOLT L 14 EMMC

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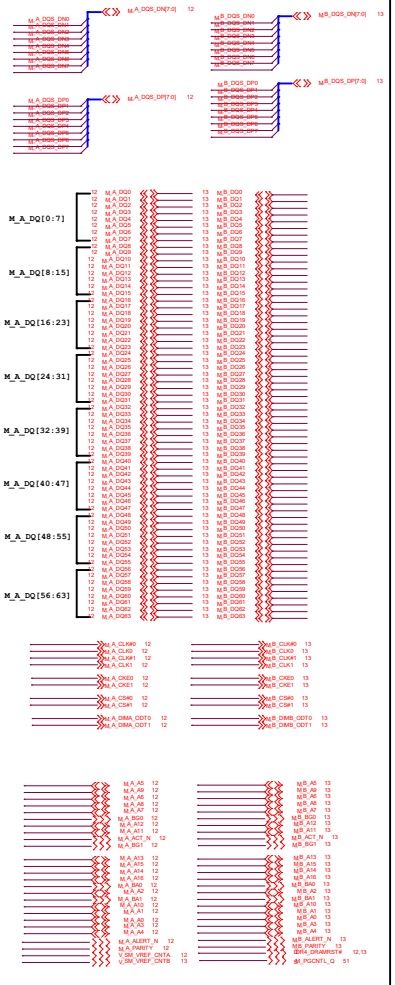
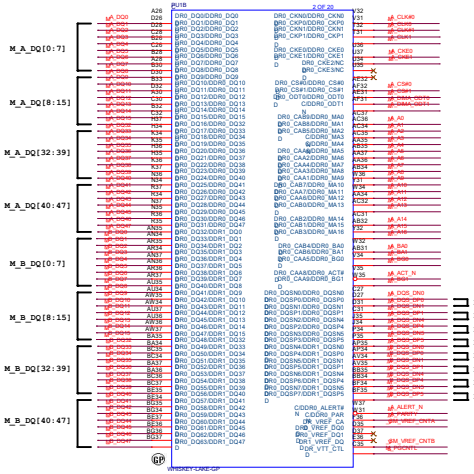
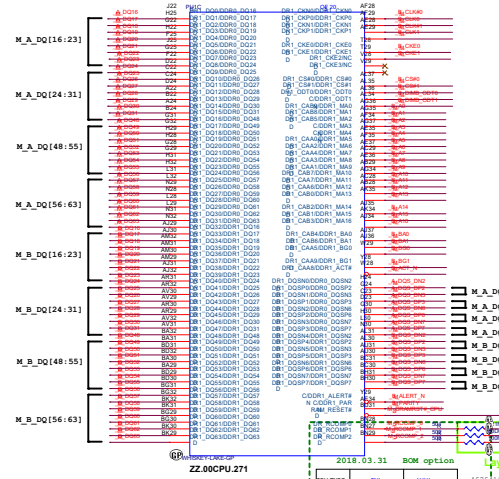
Title: C PU_(JTAG/CPU SIDE BAND)
Size: C Custom | Document Number: B OLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet 4 of 105

Main FUNC = CPU

DDR4 ball type: Non-Interleaved Type







CPU TYPE	CNL	WHL
RS01	100 Ohm 64.10005.6DL	121 Ohm 64.12105.6DL
RS02	100 Ohm 64.10005.6DL	80.6 Ohm 64.80R65.6DL

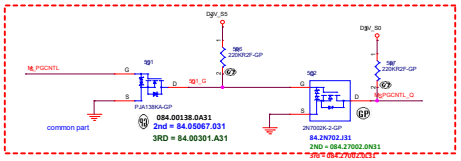
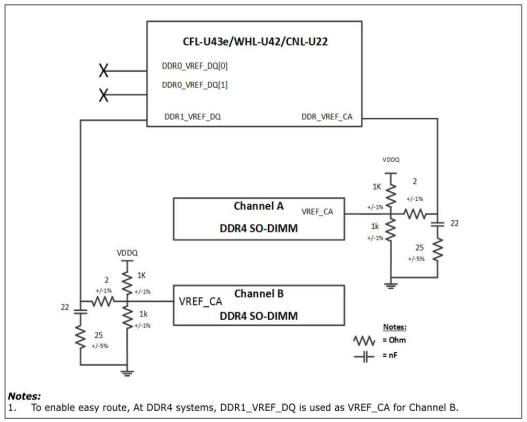
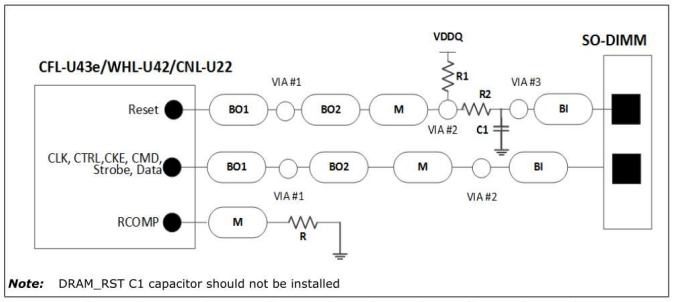


Figure 4-1. WHL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

WHL U DDR4 SODIMM T3/8L Signals Topologies



Note: DRAM_RST C1 capacitor should not be installed

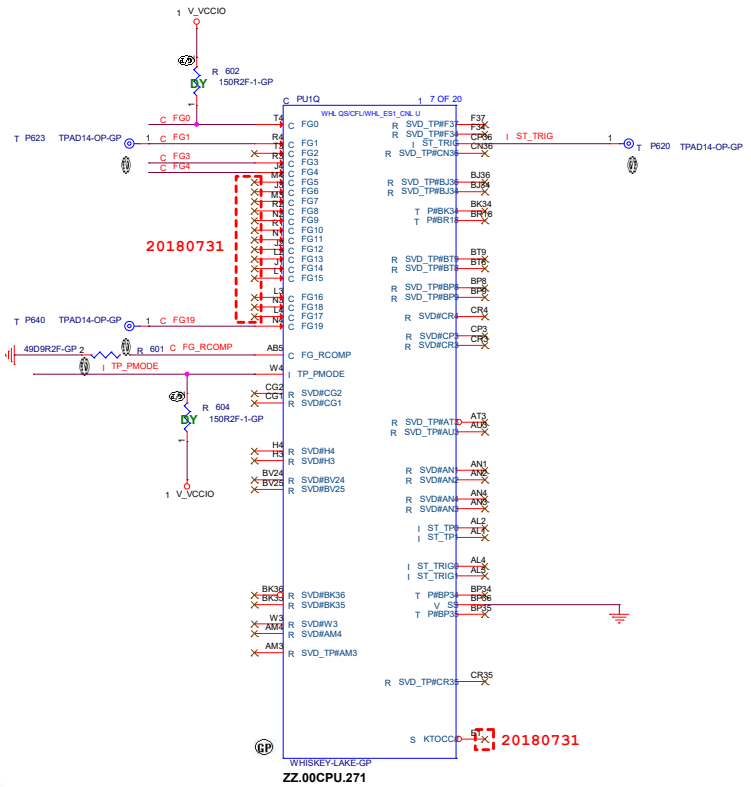
RCOMP (0/1/2)	M	US/SL	500			15	20	25	CFL-U43e/ WHL-U42: 121/80.6/ 100 CNL-U22: 100/100/ 100
Reset	BO1	US	500	8000		3		6	R1=470 [5%] R2=0 C1=0.1uF (no stuff)
	BO2	SL	800-BO1			3.5		12	
	M	SL			50	4		20	
	BI	US				4		20	

BOLT L 14 EMMC

Wistron Corporation			
Title: C PU (DDR)			
Size:	Document Number: BLT WHL		Rev: 1
Date: Thursday, December 27, 2018	Sheet: 5	of: 105	

Main FUNC = CPU

15 CFG3
15 CFG4



ZZ.00CPU.271

Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 162Ω ± 1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

BOLT L 14 EMMC

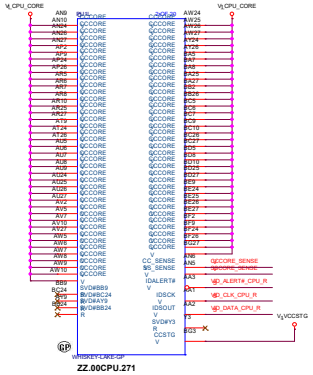
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(RESERVED)

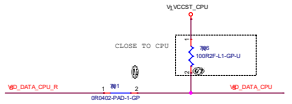
Size: A 2 | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 6 of 105

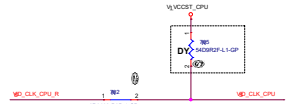
Main FUNC = CPU



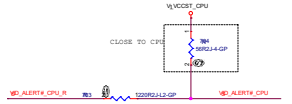
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID DATA



SVID CLOCK



SVID ALERT

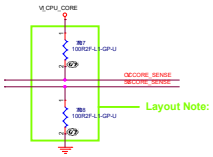


Figure 7-19. Routing Illustration for SVID Topology #575412

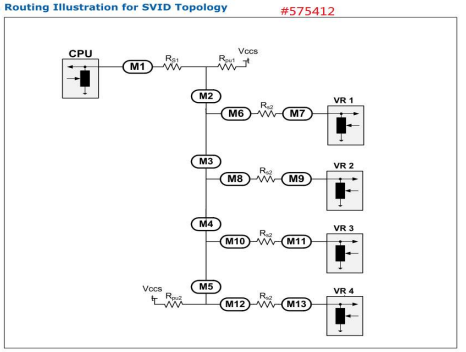
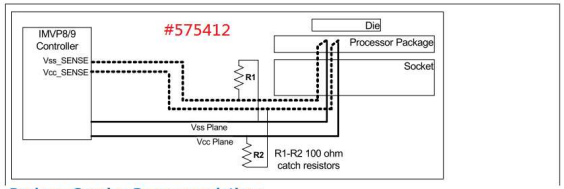


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

12-3. Example of Processor Vcc_SENSE/Vss_SENSE Package Sensing



Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
	100Ω	50Ω	<25 mils
Vcc_SENSE /Vss_SENSE			
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

Note:
1. Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

— R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

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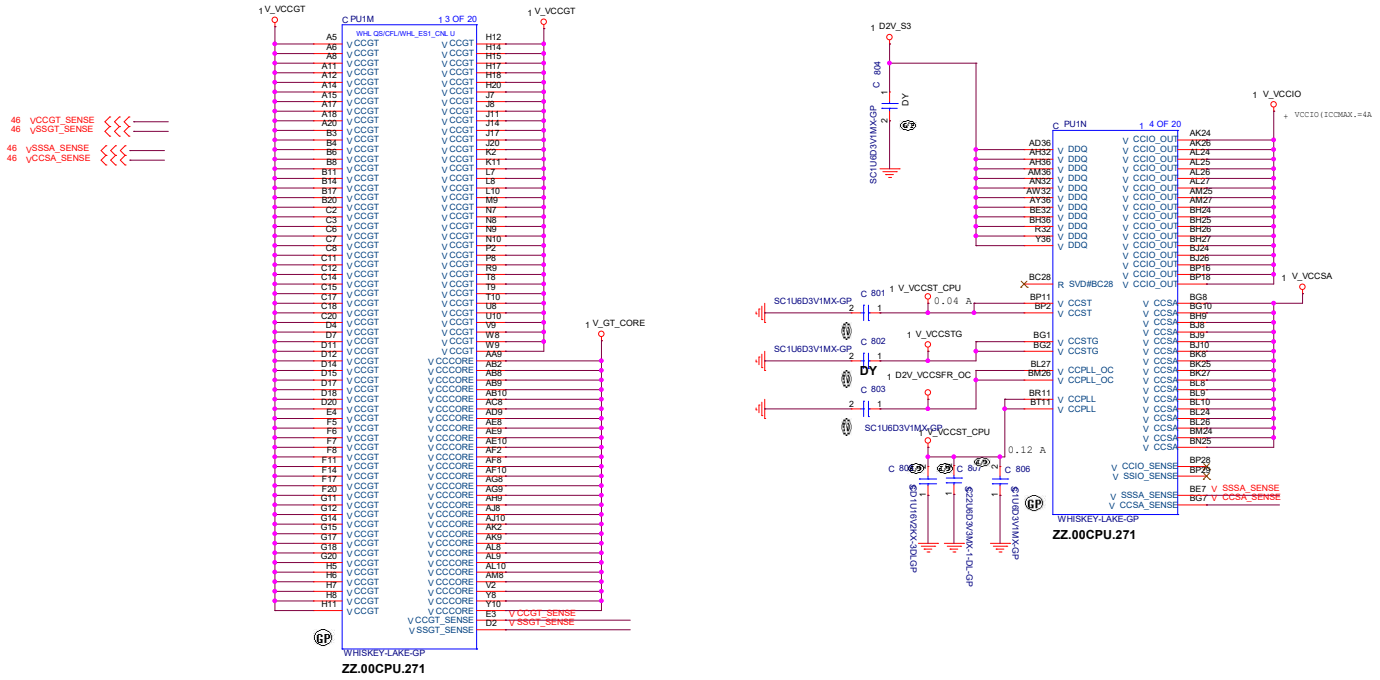
Hsien Pei 221, Taiwan, R.O.C.

Title: C PU(VCC_CORE)

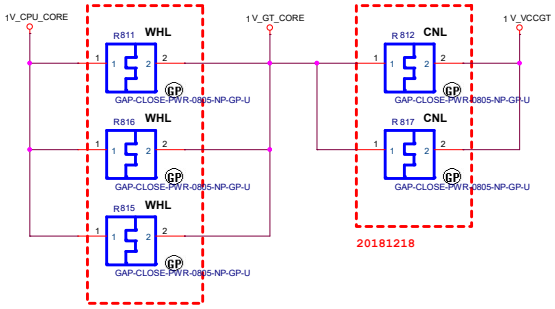
Size: 11 in | Document Number: BLT WHL | Rev: 1

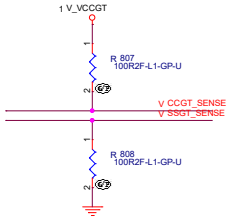
Date: Thursday, December 27, 2018 | Sheet 7 of 105

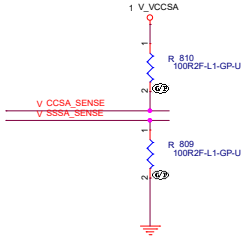
Main FUNC = CPU



Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE







Design Target	CPU support	Stuffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (Ci3 SMB0-ICP)	CNL only	None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (Ci7-Ci3)	WHL only	None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (Ci7-ICP)	WHL and CNL	Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

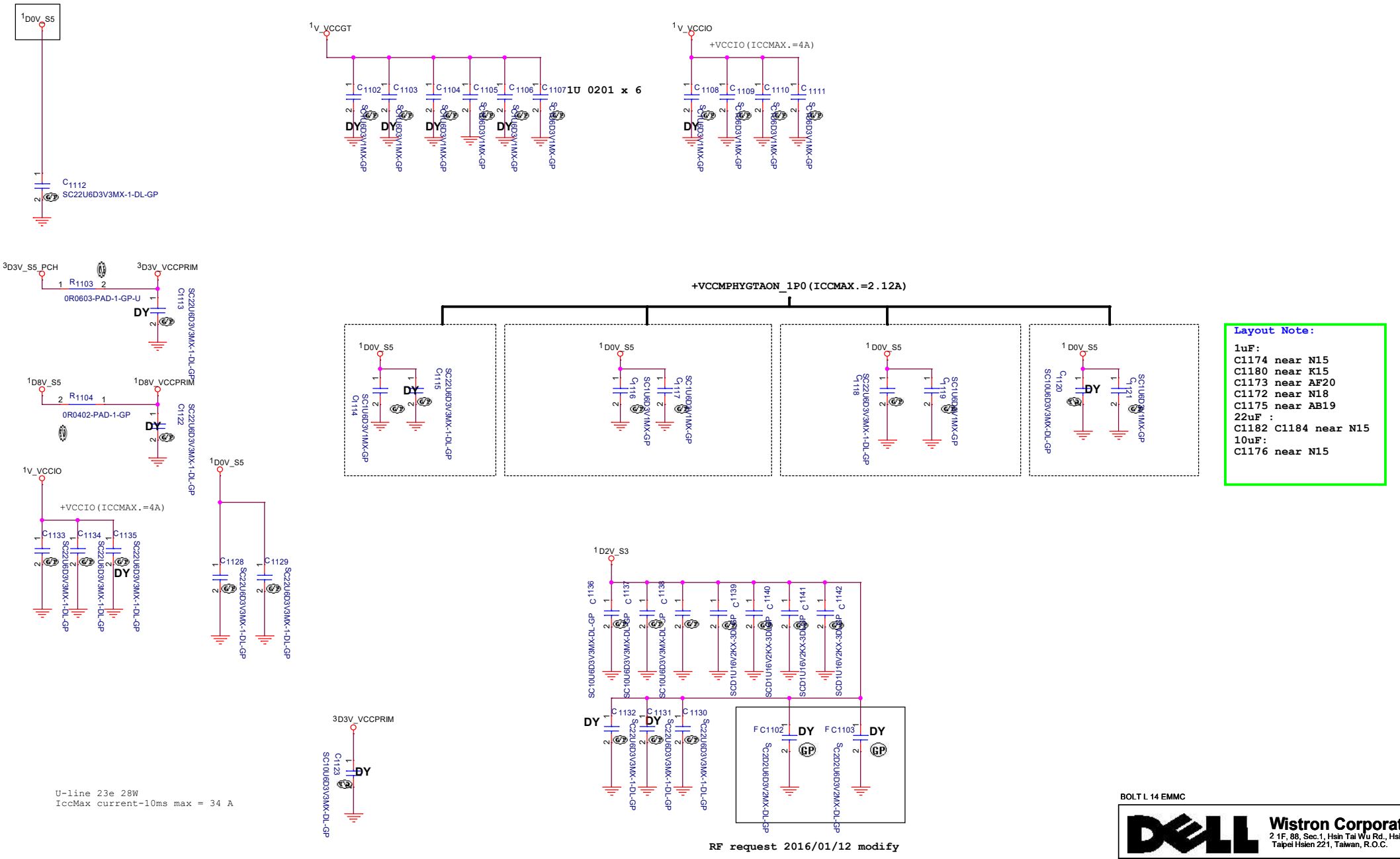
Title: C PU_(DISPLAY)

Size: A 2 | Document Number: B OLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 8 of 105

Main FUNC = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



U-line 23e 28W
IccMax current-10ms max = 34 A

Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

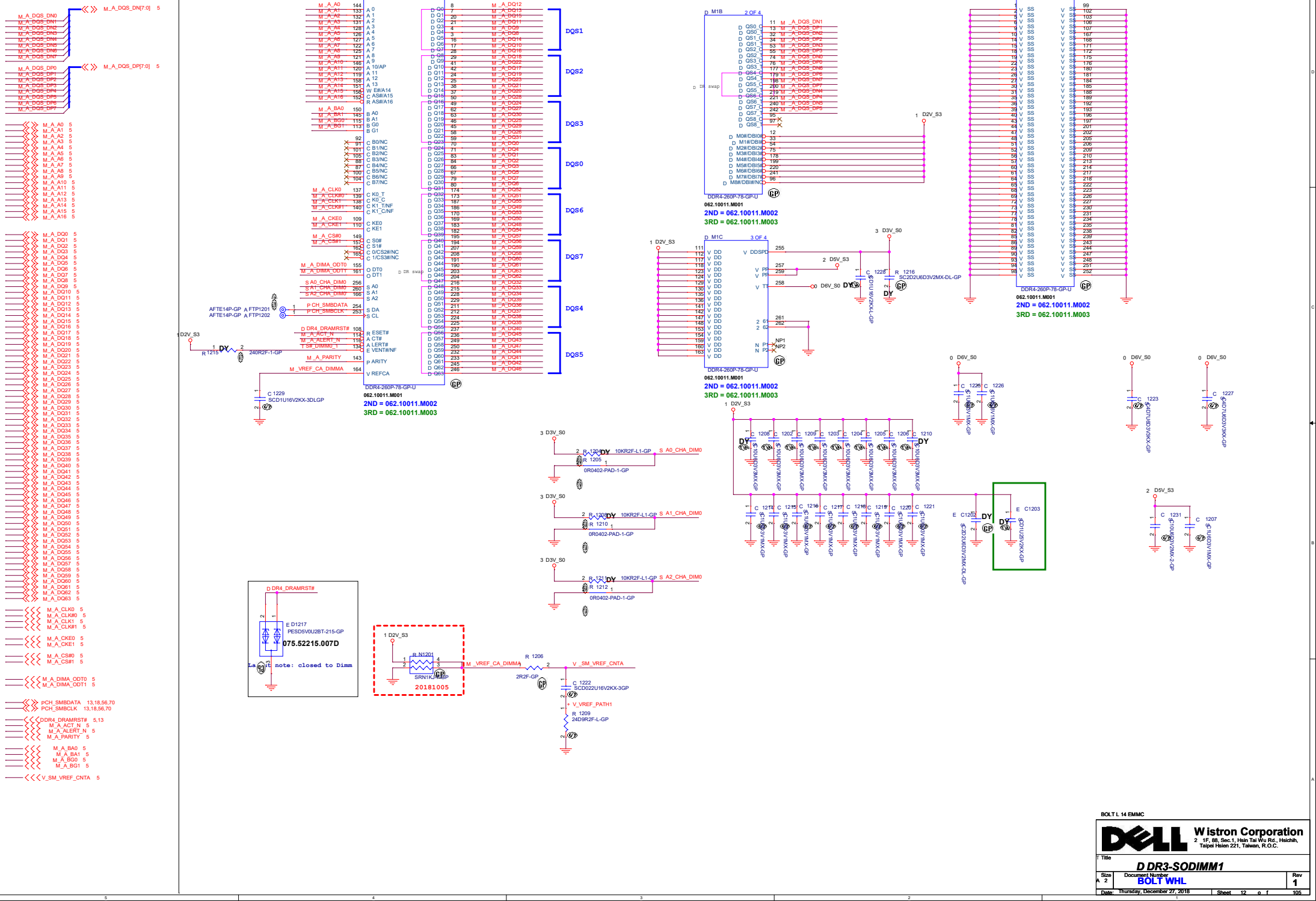
RF request 2016/01/12 modify

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP2)		
Size: A 3	Document Number: B OLT WHL	Rev: 1
Date: Thursday, December 27, 2018	Sheet 11 of 105	

Main Func = MEMORY



BOLT L 14 EMMC

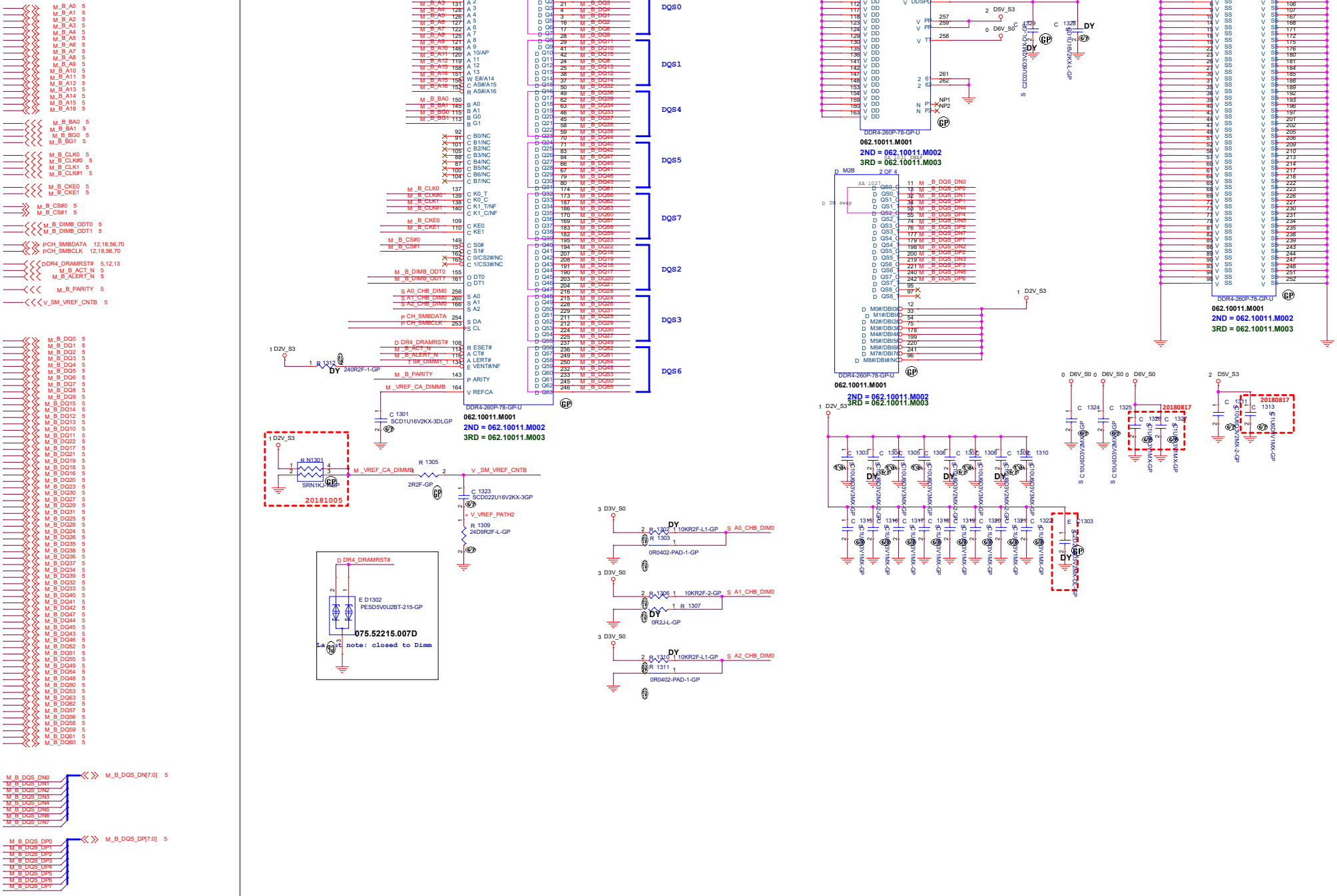
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: D DR3-SODIMM1

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 12 of 105

Main Func
= MEMORY



BOLT L 14 EMMC

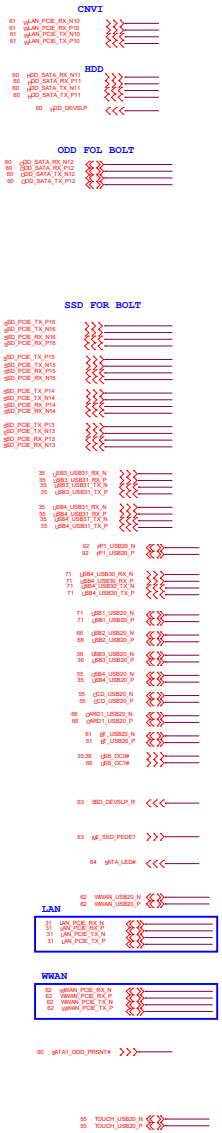
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

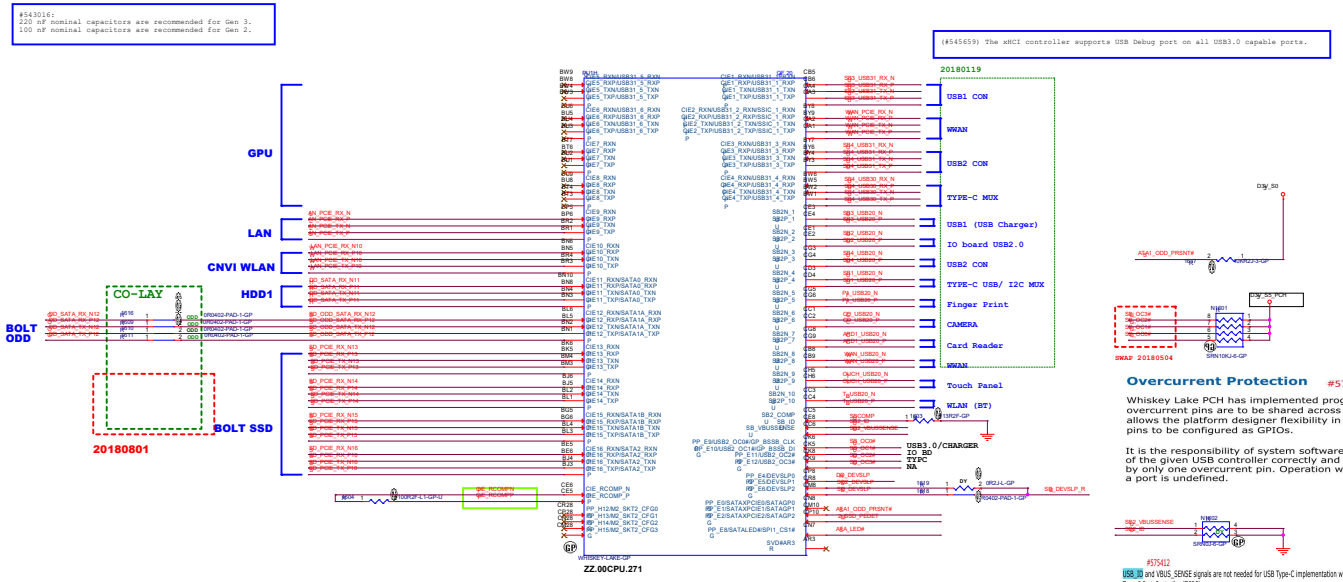
Title: D DR3-SODIMM1

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 13 of 105

Main Func = PCH





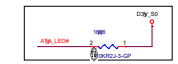
USB 2.0 Table

Pair	Device
1	USB1 (USB Charger)
2	IO board USB2.0
3	USB2 CON
4	TYPE-C USB/ I2C MUX
5	Finger Print
6	CAMERA
7	Card Reader
8	WWAN
9	Touch Panel
10	WLAN (BT)

Overcurrent Protection #575412

Whiskey Lake PCH has implemented programmable USB Overcurrent signals. The 4 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.



#575412

USB_ID and VBUS_SENSE signals are not needed for USB Type-C implementation with Type-C Port Controller (TCPC).

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 162Ω ± 1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

6.4.1 PCH PCI Express* Device Down Guidelines

Figure 6-3. PCH PCI Express* Device Down at 2.5, 5, and 8 GT/s Topology

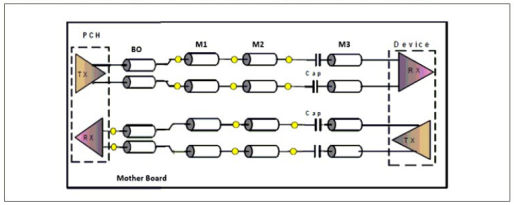


Table 6-6. PCH PCI Express* Device Down Routing Guidelines (Sheet 1 of 2)

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	MS/SL/DSL	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	MS	mm(mils)	8(314.96)	8(314.96)	8(314.96)

BOLT L 14 EMAC

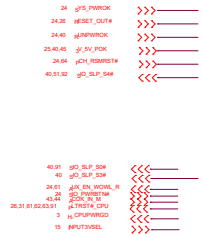
DELL W Istron Corporation
No.88, Sec.1, Hsin Tai Wu Rd., Hsichih, Hsin Hsien 221, Taiwan, R.O.C.

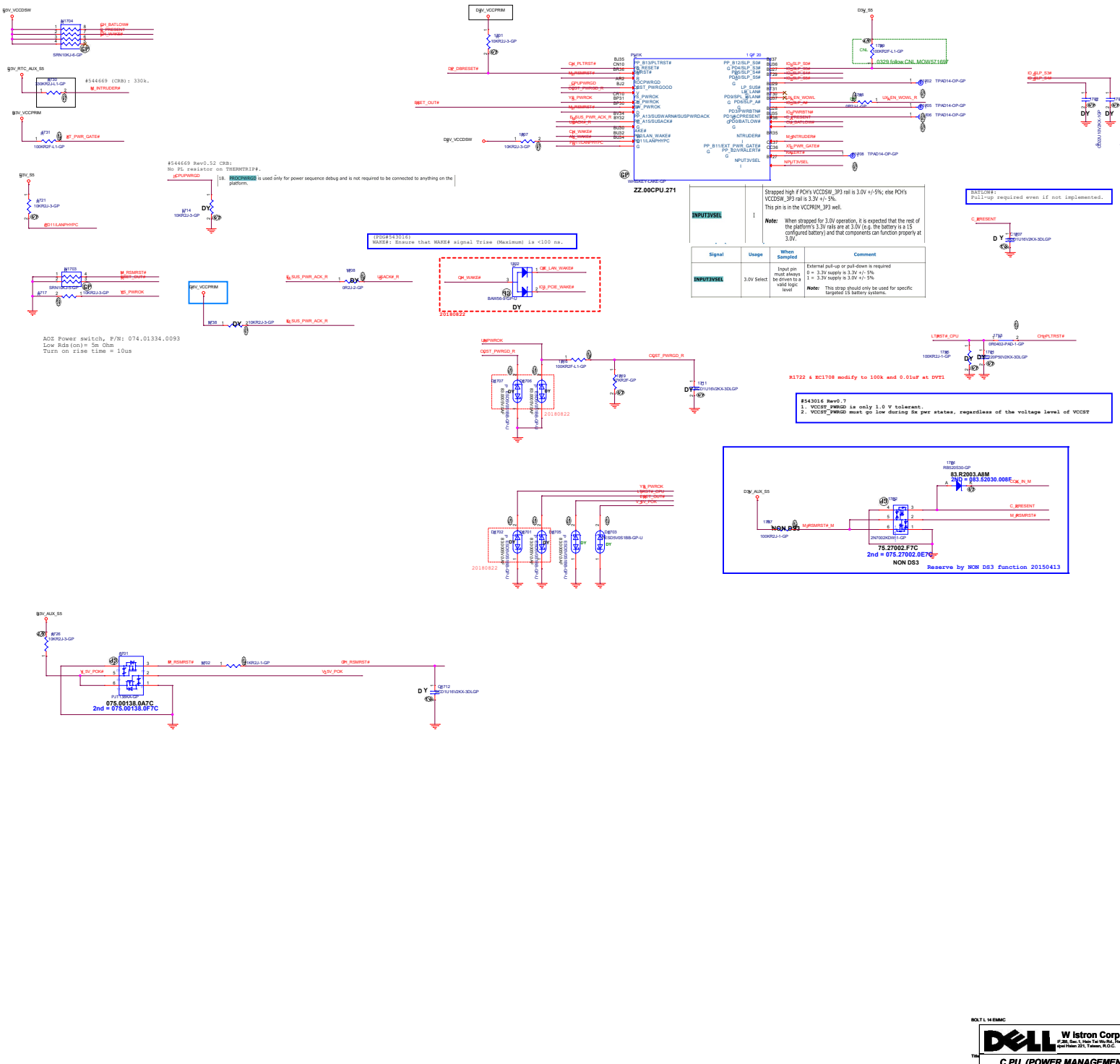
Title: C PU (PCIE/SATA/USB)

Size: A | Document Number: BOLT WHL | Rev: 1

Date: Friday, December 28, 2018 | Sheet 16 of 165

Main Func = PCH





BOLT L 14 EMAC

W Istron Corporation
No.88, Sec.1, Hsin Tai Wu Rd., Hsichih, Hsien Hsien 221, Taiwan, R.O.C.

Title: C PU_(POWER MANAGEMENT)

Size: A | Document Number: BLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 17 of 105

Main Func = PCH

SPI ROM&TPM

25,91 sPI_CLK_CPU
25,91 sPI_SO_CPU
15,25,91 sPI_SI_CPU
15,25 sPI_WP_CPU
15,25 sPI_HOLD_CPU
25 sPI_CS_CPU_N0
25 sPI_CS_CPU_N1
91 sPI_CS_CPU_N2
91 sTPM_SPI_IRQ#

ESPI

24 sESPI_IO[3..0]
sESPI_IO3
sESPI_IO2
sESPI_IO1
sESPI_IO0
24 sESPI_CS#
24 sESPI_CLK
24 sESPI_RESET#

MEM SMBUS,CRT

12,13,56,70 pCH_SMBDATA
12,13,56,70 pCH_SMBCLK

KBC,Thermal/Fan

24,26 sML1_SMBCLK
24,26 sML1_SMBDATA

M.2 SSD

63 sSD_CLK_CPU_P_4
63 sSD_CLK_CPU_N_4
63 cLK_PCIE_NVME_REQ#

GPU

LAN

31 LAN_CLK_CPU_N
31 LAN_CLK_CPU_P
31 CLK_PCIE_LAN_REQ#

WWAN

62 WWAN_CLKREQ_CPU_N
62 WWAN_PCIE_CLK_N
62 WWAN_PCIE_CLK_P

CNVI

61 WLAN_CLK_CPU_N
61 WLAN_CLK_CPU_P
61 CLK_PCIE_WLAN_REQ#
24,61 SUS_CLK
61 WLSAR_39P4M_REFCLK
17,24,61 sO3_PCIE_WAKE#

RTCRST

FREE FALL SENSOR

70 sFS_INT1

STRAP

15 sMB_ALERT#
15 sML0_ALERT#
21 PROJECT_ID0
20,60 sDO_DET#

R1842/R1843/R1844/R1845/R1846		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.10R05.6DL	63.5R134.1DL
Bolt (non TPM)	63.5R134.1DL	64.49R95.6DL

MEM SMBUS,CRT
NA
KBC,Thermal/Fan,GPU
RO13_CFLU_20171228
Intel review item4
SWAP 20180504
change 20180512
20180129
MEM SMBUS
75.27002.F7C
2nd = 075.27002.0E7C
For eSPI
KBC
PCH
ZZ.00CPU.271

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

CPU_SMB_ALERT#_P0

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function5, offset BCh, bit 6). Bit 6: 0 = SPI (Default), 1 = LPC. Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

20180828
082.30003.0301
2nd = 82.30003.0191
20180802
20181102
082.30006.0041
2nd = 82.30004.A01
20180222
20180913
20180129
FC1801 close to EC1803
20180302
Layout: Place at the open door area.

CLKIN_XTAL	I		**XTAL Clock Input:** Single ended integrated CNV (Connectivity) XTAL clock input

Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to disable system if box detected open.
RTC	SRTCRST#	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.
RTC	RTCRST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

Figure 7-11. XCLK Bias Reference Topology

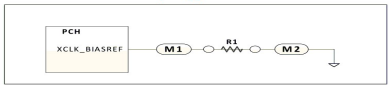


Table 7-8. XCLK Bias Reference Routing Guideline (Sheet 1 of 2)

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max Total Length	M1+M2	MS/SL/DSL	1000mils(25.4mm)
Resistor (R1)			60 Ohm ±1.0%
Max Transition Via Count			2

BOLT L 14 EMAC

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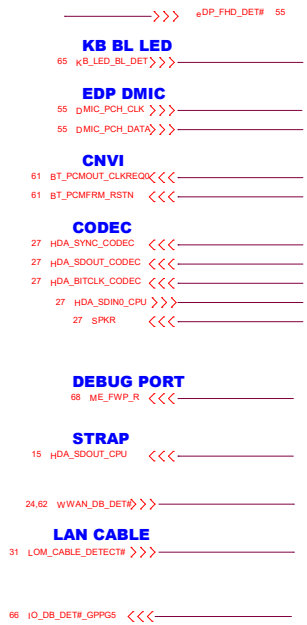
Title: C PU_(LPC/SPI/SMBUS/CL/CLK)
Size: A | Document Number: BLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet 18 of 105

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



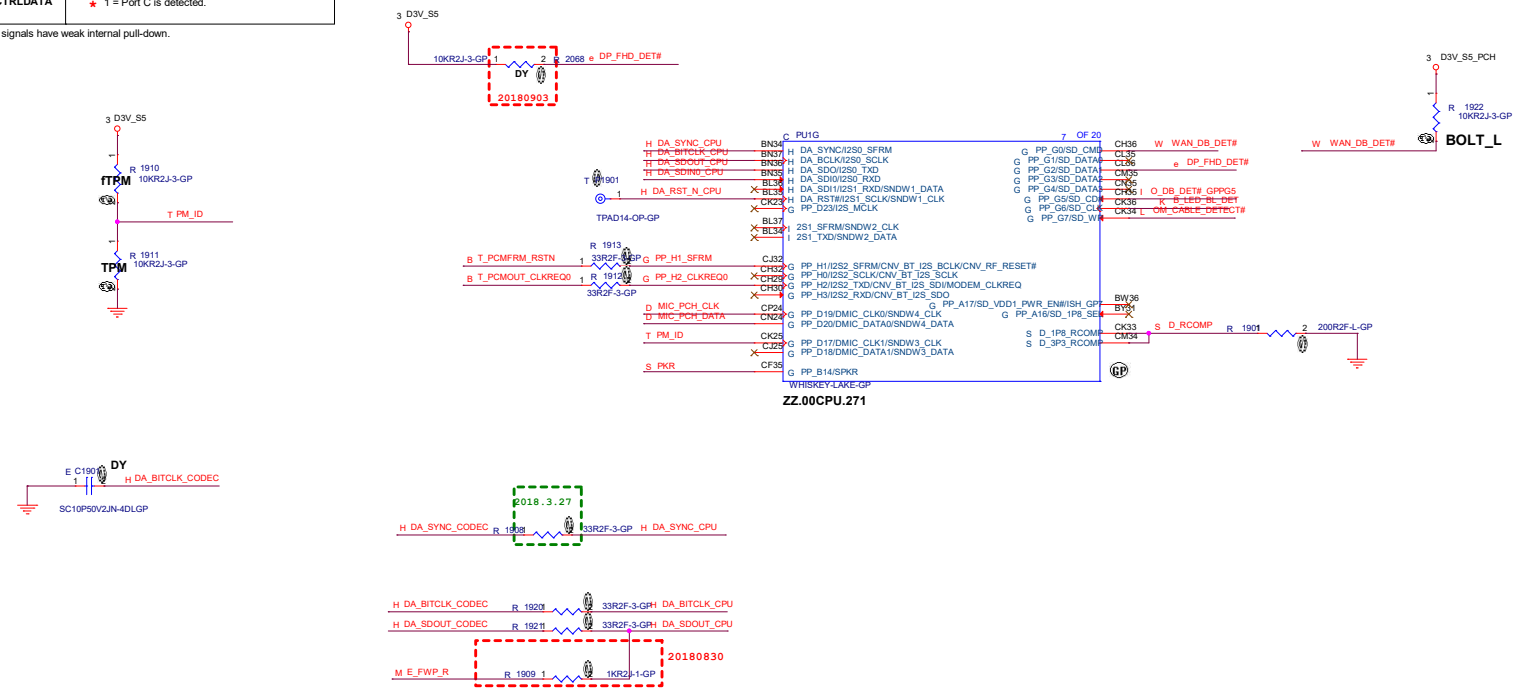


Figure 3-2. RCOMP Recommendation for WHL U42 and CFL U43e - Part 2

	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
	Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.						
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNVi_DPHY					X		

BOLT L 14 EMMC

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Title: C PU (AUDIO/SDIO/SDXC)

Size: A 2 | Document Number: B OLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 19 of 105

Main Func = PCH

55 tOUCH_I2C_DET#

CNVI

61 cNV_RGI_RSP
15,61 cNV_RGI_DT_R
61 cNV_BRI_RSP
61 cNV_BRI_DT_R

TPM INT

91 pIRQA#

BOARD SETTING

STRAP

15 sPI_BIT

SD READ CONTROL

66 sD_READ_MODE#

DEBUG PORT

68 uART_2_CRXD_DTXD
68 uART_2_CTXD_DRXD

EC

24 sCI_EXT_WAKE#

KB DETECT

65 uB_DET#

TPAD I2C IF

65,93 tPC0_SDA_TCH_PAD
65,93 tPC0_SCL_TCH_PAD

PANEL

55 pIC0_SDA_TCH_PNL
55 pIC0_SCL_TCH_PNL
55 tR_CAM_DET#
55 pRC_PANEL_EN
21,55 tLCD_CBL_DET#

GPU

FREE FALL SENSOR

70 tFS_INT2

RTC

15,25 tRTC_DET#

HDD DET

18,60 pHDD_DET#

VGA BD DET

56 vGA_DB_DET#

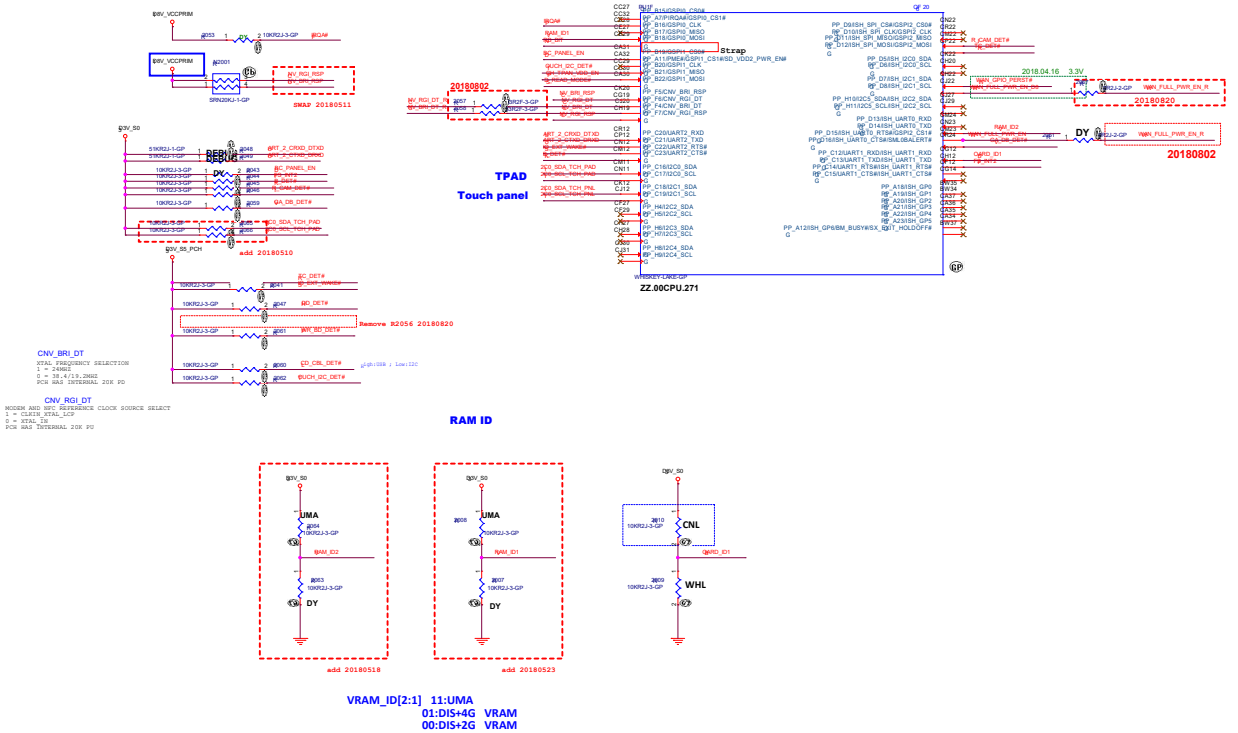
Power Button BD

21,64 PWR_BD_DET#

55 pCH_TPAN_VDD_EN

62 WWAN_GPIO_PERST#

62 WWAN_FULL_PWR_EN_R



VRAM_ID[2:1] 11:UMA
01:DIS+4G VRAM
00:DIS+2G VRAM

17.4.1 Configurable GPIO Voltage

Except for all pads in GPIO F group and GPD group, all other GPIO pads support per-pad configurable voltage, which allows control selection of 1.8V or 3.3V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8V level with 3.3V tolerant.
- Output: defaults to '0', except for the following GPIOs which defaults to '1' via a ~20K pull-up to 3.3V:
  - GPP_B0
  - GPP_B1
  - GPP_B11 / EXT_PWR_GATE#
  - GPP_B12 / SLP_S0#
  - GPP_H18 / CPU_C10_GATE#

A 1.8V device connected to these GPIOs must be capable of taking 20K pull-up to 3.3V.

'arning: GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

otes: - GPIO F group supports 1.8V only.

- GPD group supports 3.3V only.

<Core Design>
W Istron Corporation
Title: C PU (LPSS/ISH)
Size: A Document Number: BLT WHL Rev: 1
Date: Thursday, December 27, 2018 Sheet 20 of 105

Main Func = PCH

61 BLUETOOTH_EN
61 WIFI_RF_EN

20,64 PWR_BD_DET#

15 GPP_H21
15 GPP_H23
15 GPD_7

40 GPPC_H18_VCCIO_LPM
18 PROJECT_ID0

CNvi TX for wifi

61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1

CNvi RX for wifi

61 CNV_WR_CLK_DP
61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1

62 WWAN_BB_RST#

20,55 LCD_CBL_DET#

EMMC

63 EMMC_D7
63 EMMC_D6
63 EMMC_D5
63 EMMC_D4
63 EMMC_D3
63 EMMC_D2
63 EMMC_D1
63 EMMC_D0

63 EMMC_CLK
63 EMMC_CMD

63 EMMC_RCLK
63 EMMC_RESET#

IO BD DET

66 IO_DB_DET#

CNVI FOR WIFI

CPU1I — WHISKEY-LAKE-GP — 9 OF 20

CNV_WR_DN0 CR30
CNV_WR_DP0 CP30
CNV_WR_DN1 CM30
CNV_WR_DP1 CN30
CNV_WT_DN0 CN32
CNV_WT_DP0 CM32
CNV_WT_DN1 CP33
CNV_WT_DP1 CN33
CNV_WR_CLK_DN CN31
CNV_WR_CLK_DP CP31
CNV_WT_CLK_DN CP34
CNV_WT_CLK_DP CN34

R2101 2 1 150R2F-1-GP
CNV_WT_RCOMP CP32
CNV_WT_RCOMP#CP32
CNV_WT_RCOMP#CR32
GPP_F0/CNV_PA_BLANKING CP20
GPP_F1 CK19
GPP_F2 CG17

20180907

PROJECT_ID1
PROJECT_ID2

PWR_BD_DET# CR14
BLUETOOTH_EN CP14
LCD_CBL_DET# CN14
IO_DB_DET# CM14

20180802

GPP_C8/UART0_RXD
GPP_C9/UART0_TXD
GPP_C10/UART0_RTS#
GPP_C11/UART0_CTS#

CJ17
CH17

20180907

WWAN_BB_RST# CF17

2018.04.16
1.8V only

GPP_F8/CNV_MFUART2_RXD
GPP_F9/CNV_MFUART2_TXD
GPP_F23/A4WP_PRESENT

GPP_H18/CPU_C10_GATE# CN27 — GPPC_H18_VCCIO_LPM
GPP_H19/TIMESYNC0 CM27
GPP_H21 CF25 — GPP_H21
GPP_H22 CN26
GPP_H23 CM26 — GPP_H23
GPP_F10 CK17
GPD7 BV35 — GPD_7
GPP_F3 CN20 — PROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 — WIFI_RF_EN
GPP_H20/IMGCLKOUT1 CH25

GPP_F: VCCPGPPF = 1.8V Only

GPP_F12/EMMC_DATA0 CR20 — EMMC_D0
GPP_F13/EMMC_DATA1 CM20 — EMMC_D1
GPP_F14/EMMC_DATA2 CN19 — EMMC_D2
GPP_F15/EMMC_DATA3 CM19 — EMMC_D3
GPP_F16/EMMC_DATA4 CN18 — EMMC_D4
GPP_F17/EMMC_DATA5 CR18 — EMMC_D5
GPP_F18/EMMC_DATA6 CP18 — EMMC_D6
GPP_F19/EMMC_DATA7 CM18 — EMMC_D7

GPP_F20/EMMC_RCLK CM16 — EMMC_RCLK
GPP_F21/EMMC_CLK CP16 — EMMC_CLK
GPP_F11/EMMC_CMD CR16 — EMMC_CMD
GPP_F22/EMMC_RESET# CN16 — EMMC_RESET_N

R2125 1 DY 2 — EMMC_RESET#

EMMC_RCOMP CK15 — EMMC_RCOMP
R2108 2 1 200R2F-L-GP — 0R2J-2-GP

2018.04.09

ZZ.00CPU.271

WWAN_BB_RST

Power Management States for Modern connected standby platform

System States	USB device State	PCIe Device States	PCIe Link states	PERST#	PEWAKE#	CLKREQ#	BB_RESET#	Notes
S0	D0	D0	L0, L1.2	H	H	L0 : L L1.2 : H	H	
	D2	D3cold	L2	L	H	H	H	
S0ix	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem
S4	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	
S5	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem

PROJECT_ID[1:0] 01: 7000 Series

PROJECT_ID[3:2] 11: Inspiron

1 D8V_VCCPRIM

EMMC
R2111 10KR2J-3-GP
PROJECT_ID1
R2112 10KR2J-3-GP
NON EMMC

R2113 10KR2J-3-GP
PROJECT_ID0
DY R2114 10KR2J-3-GP

R2115 10KR2J-3-GP
PROJECT_ID3
DY R2116 10KR2J-3-GP

R2117 10KR2J-3-GP
PROJECT_ID2
DY R2118 10KR2J-3-GP

<Core Design>

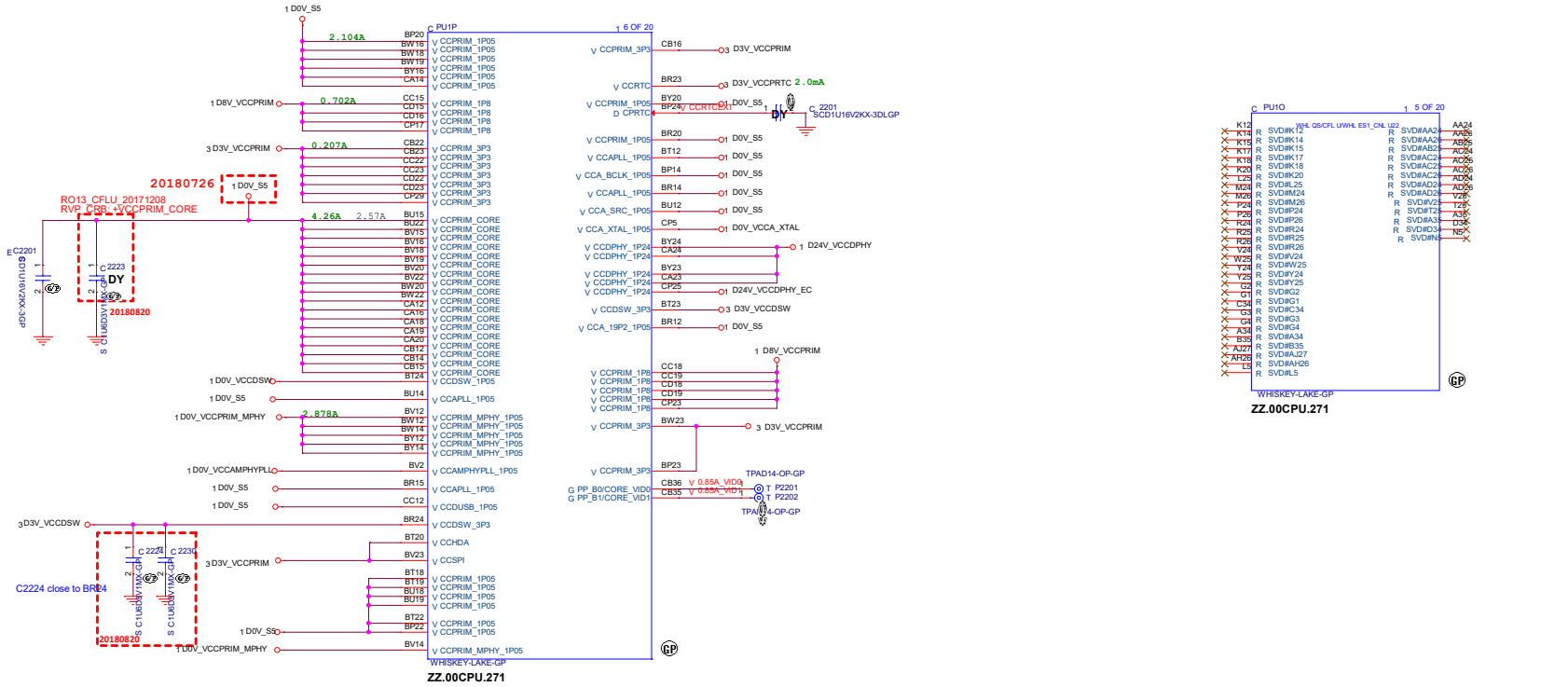
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

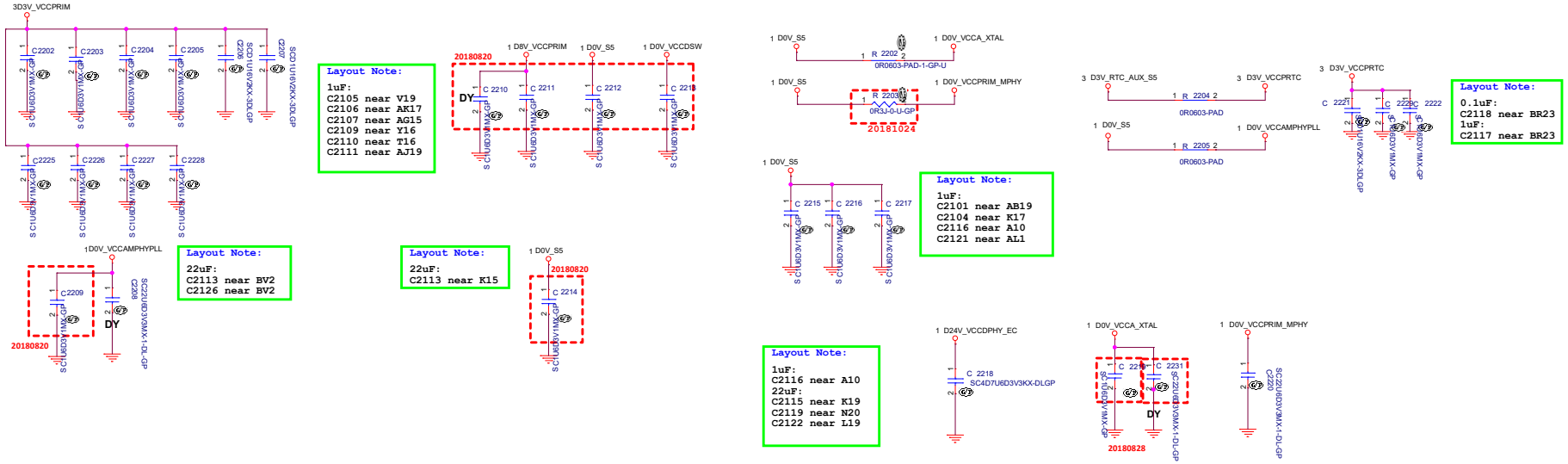
Title: CPU_(POWER1)

Size	Document Number	Rev
A 3	B OLT WHL	1

Date: Thursday, December 27, 2018 | Sheet 21 of 105

Main Func = PCH





BOLT L 14 EMMC

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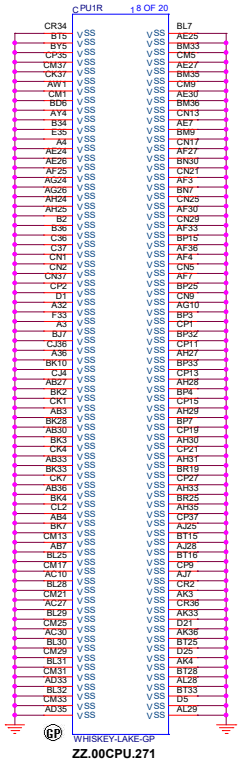
Taipei Hsien 221, Taiwan, R.O.C.

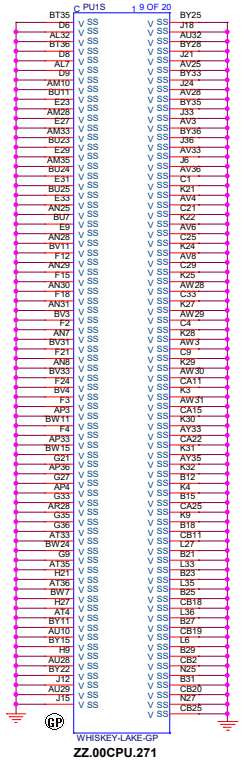
Title: CPU_(RSVD)

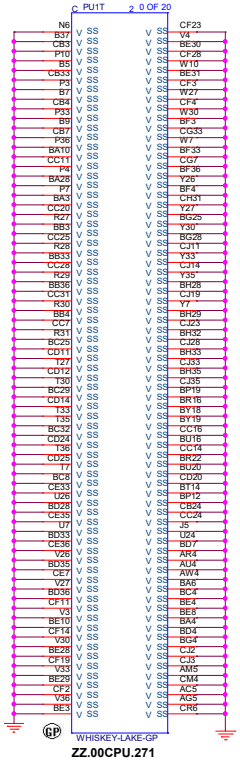
Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 | Sheet 22 of 105

Main Func = PCH







BOLT L 14 EMMC

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(VSS)

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 23 of 105

Main Func = KBC

PCB VERSION A/B(P3V8)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
MB0 (X4)	100.0K	10.0K(64.10025.6DL)	3.0V
MB1 (X0)	100.0K	17.8K(64.17825.6DL)	2.301V
MB2 (NC)	100.0K	27.0K(64.27025.6DL)	2.701V
MB3 (X8)	100.0K	37.4K(064.37425.06DS)	2.402V
MB4 (1)	100.0K	49.9K(64.49925.6DL)	2.201V
MB5	100.0K	64.9K(64.64925.6DL)	2.001V
MB6	100.0K	82.5K(64.82525.6DL)	1.801V
MB7	100.0K	107K(64.10735.6DL)	1.594V
Reserved	100.0K	154K(64.15435.6DL)	1.295V
Reserved	100.0K	200K(64.20035.6DL)	1.1V

Model ID	Project	USB-C Function	Charger	PL	PH	GPU
1	Bolt-L	Full Function	Intersil ISL9538	100.0K	10.0K(64.10025.6DL)	UMA
2	Bolt 2SP/1SP/BT	N/A	Intersil ISL95522	100.0K	17.8K(64.17825.6DL)	UMA
3	Bolt_L Pentium or Celeron	Full Function	Intersil ISL9538	100.0K	27.0K(64.27025.6DL)	UMA
4	Bolt-L	Full Function	Intersil ISL9538	100.0K	37.4K(064.37425.06DS)	N16S-GTR1-S 2GB
5	Bolt 2SP/1SP	Data Only	Intersil ISL95522	100.0K	49.9K(64.49925.6DL)	N16S-GTR1-S 2GB/4GB
6	Reserved			100.0K	64.9K(64.64925.6DL)	

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
1	1	Use 3.3V Shared SPI

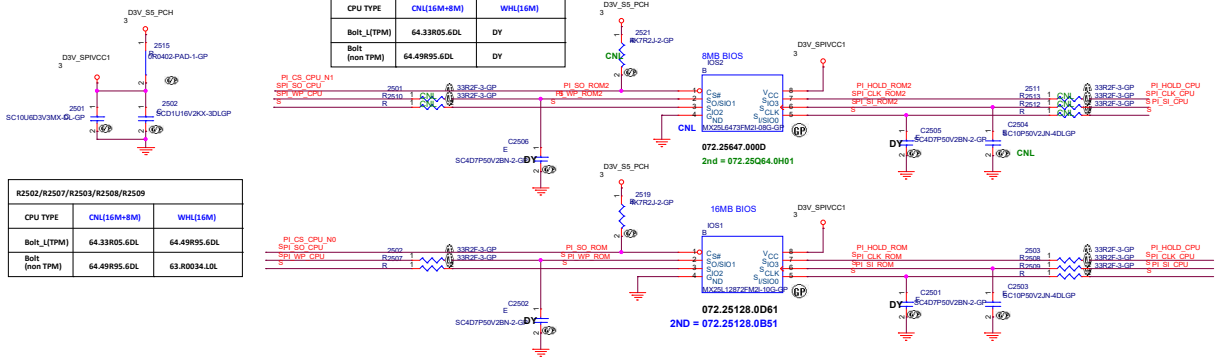
Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Wistron Corporation
Title: HSC Nuvoton NPCE285PA0DX
Size: C
Project Name: BOLT WHL
Rev: 1
Date: Thursday, December 03, 2020
Sheet: 36 of 47

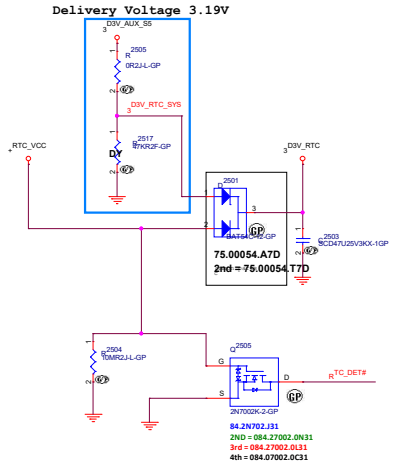
Main Func = SPI Flash

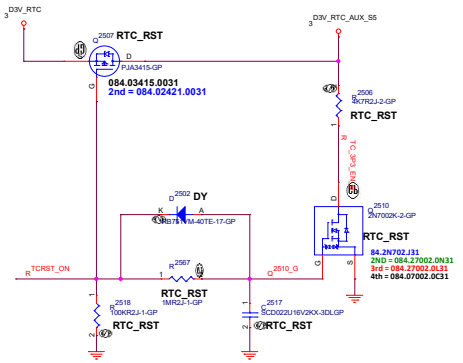
R2501/R2510/R2511/R2513/R2512		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	DY
Bolt (non TPM)	64.49R95.6DL	DY

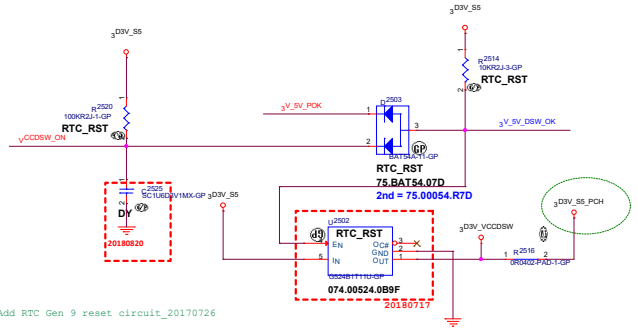
R2502/R2507/R2503/R2508/R2509		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	64.49R95.6DL	63.R0034.L0L



Main Func = RTC







29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

Add RTC Gen 9 reset circuit_20170726

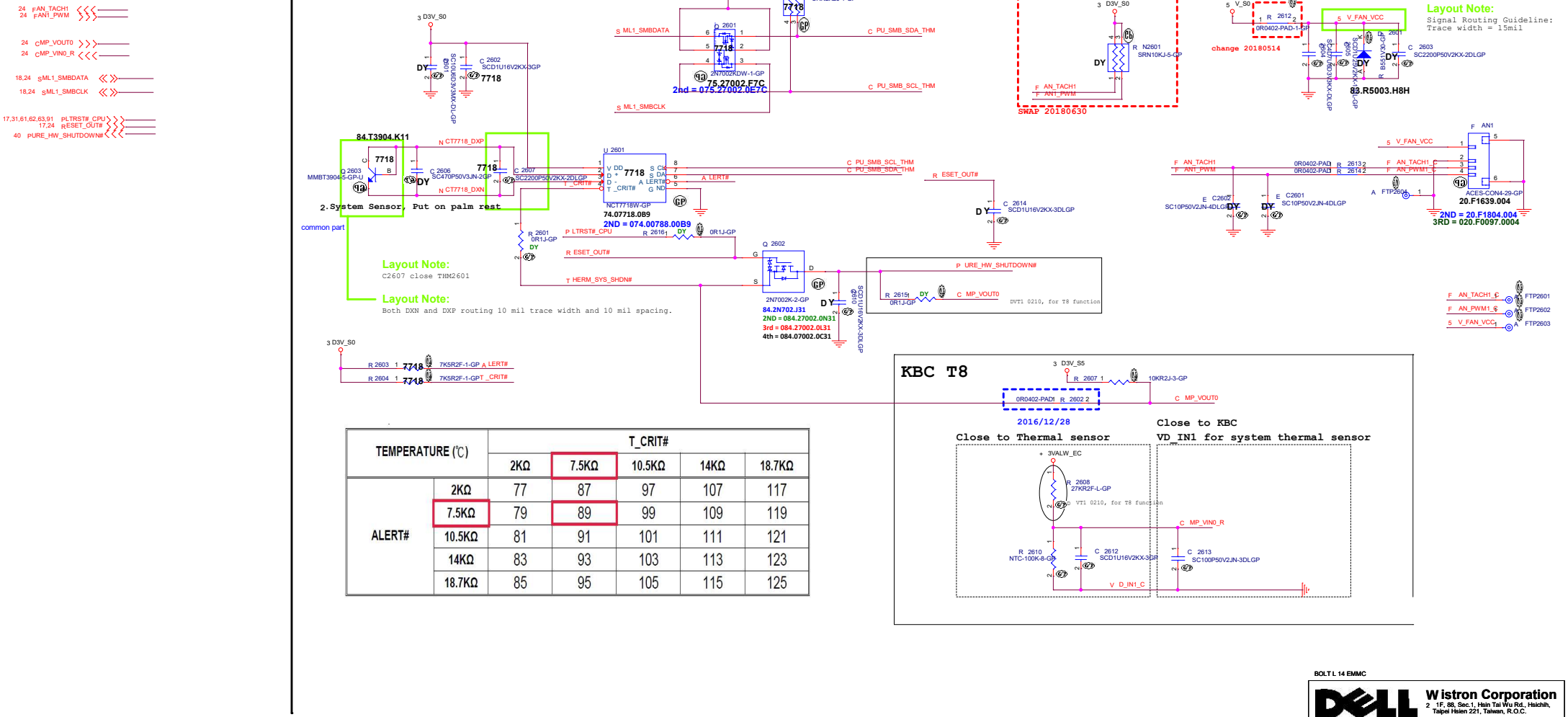
BOLT L 14 EMMC

Wistron Corporation
2 F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: Custom | Document Number: BOLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet: 25 of 105

Main Func = Thermal Sensor

PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: Custom | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 26 of 105

Main Func = Audio

< 2.5A (peak)
When play with 1KHz
sin wave on 2W/4ohm speaker

20181031

<50mA

Layout Note:
Place close to Pin 20

DVDD must >= DVDD_IO

Analog
Digital

ALC3204
Q FN40 (5X5)

ALC3204-CG-GP-U
071.03204.0003

Layout Note:
Speaker trace
width >40mil @
2W4ohm speaker
power

place close to pin1

place close to pin8

Layout Note:
R2704 near HDA27
R2705 near HPMIC1

Add 20180702

100K is used to speed up the discharge for LDO1.
It could solve the pop sound during
system boot up and reboot.

coin battery is used to solve the humming noise
when UAJ port connecting to active speaker and system entering S3/S4/S5
or notebook battery mode or desktop G3 mode.

<10uA

20180903

75.00054.A7D

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

Size	Document Number	Rev
A 2	BOLT WHL	1

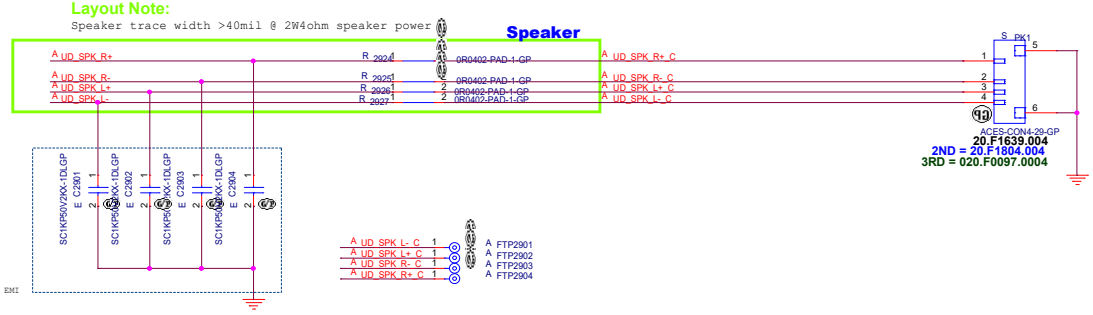
Date: Thursday, December 27, 2018 | Sheet 27 of 105

Main Func = Audio

SPEAKER

27 A UD_SPK_R+
27 A UD_SPK_R-
27 A UD_SPK_L+
27 A UD_SPK_L-

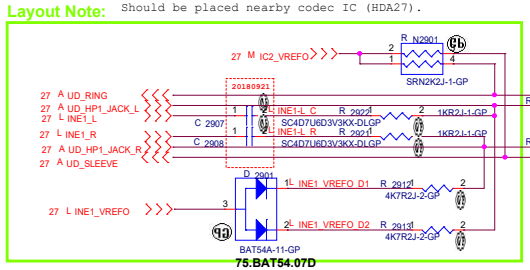
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

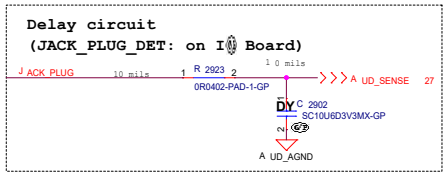


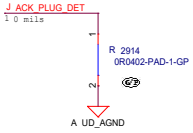
CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON

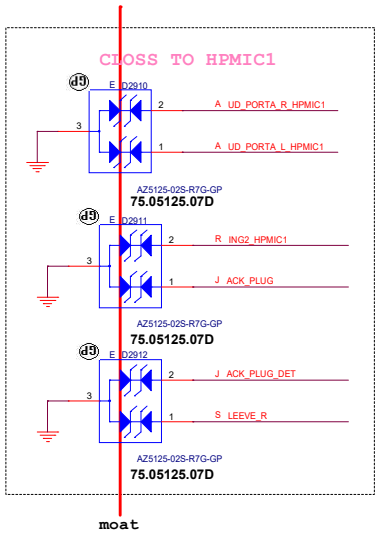
Audio Jack

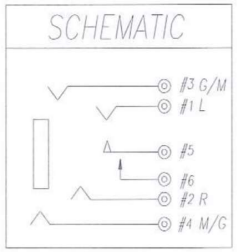
Layout Note: Should be placed nearby codec IC (HDA27).











BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/Universal Jack

Size	Document Number	Rev
Custom	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 29 of 105

Main Func = LAN

LAN CHIP (10/100/1000M & 10/100M co-lay)

PCIE

16 LAN_PCIE_TX_P
16 LAN_PCIE_TX_N
16 LAN_PCIE_RX_P
16 LAN_PCIE_RX_N

PCIE_CLK

18 LAN_CLK_CPU_P
18 LAN_CLK_CPU_N
18 CLK_PCIE_LAN_REQ#

MDI

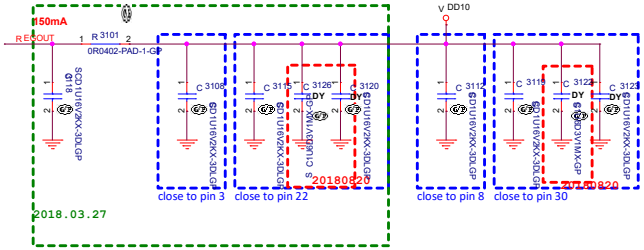
32 LAN_MDI0_P
32 LAN_MDI0_N
32 LAN_MDI1_P
32 LAN_MDI1_N
32 LAN_MDI2_P
32 LAN_MDI2_N
32 LAN_MDI3_P
32 LAN_MDI3_N

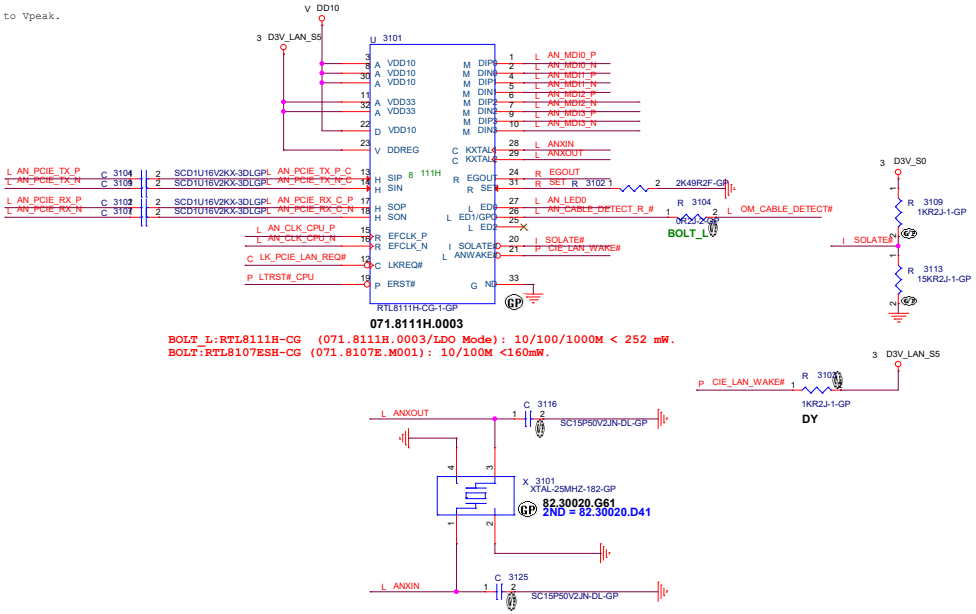
17,24 PCIE_LAN_WAKE#
17,26,61,62,63,91 pLTRST#_CPU
19 LOM_CABLE_DETECT#
32 LAN_LED0

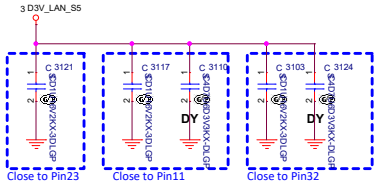
3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.

LAN power Noise 3.3V < 200mV Vpeak to Vpeak.

LAN power Noise 1.0V < 100mV Vpeak to Vpeak.







C3110/C3124 for surge

BOLT L 14 EMMC

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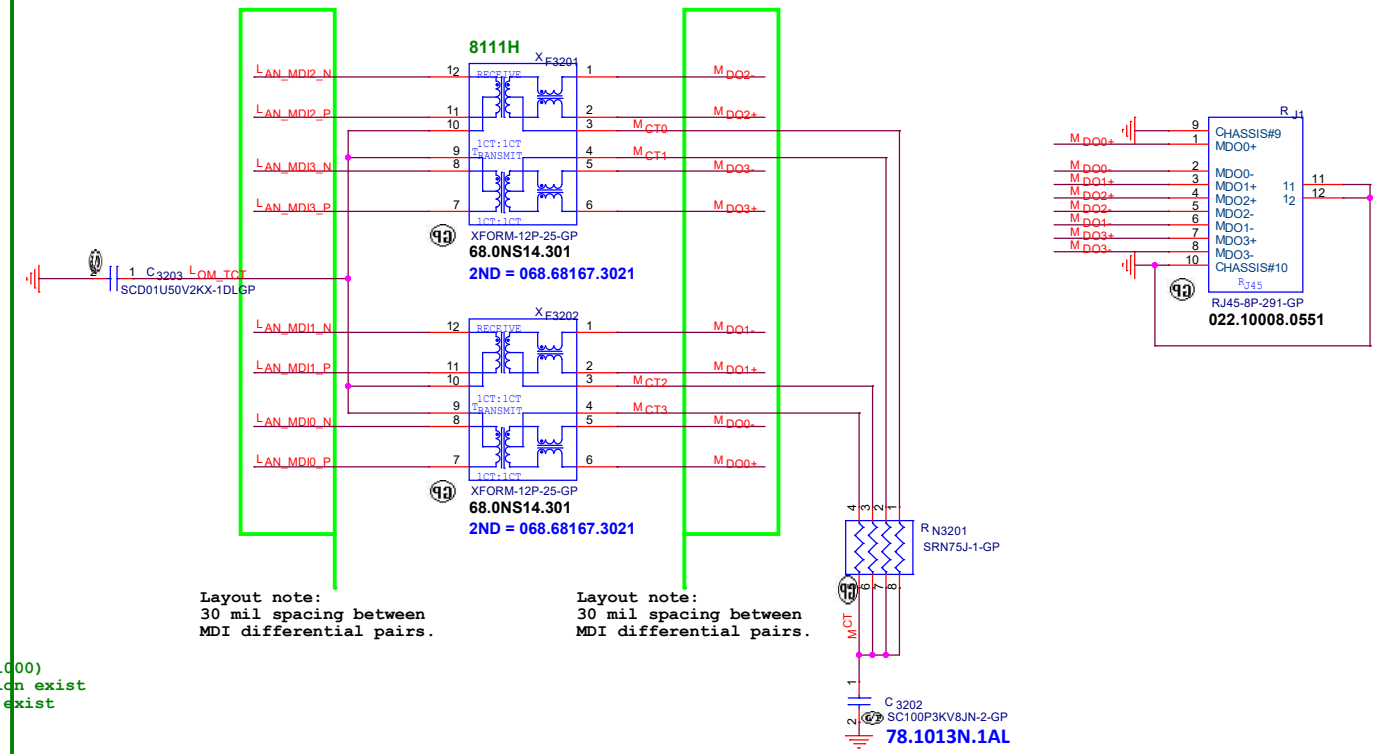
Title: LAN RTL8106

Size: C | Document Number: BOLT WHL | Rev: 1

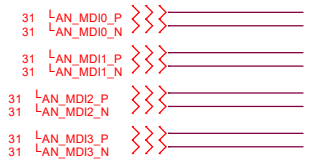
Date: Thursday, December 27, 2018 | Sheet 31 of 105

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)



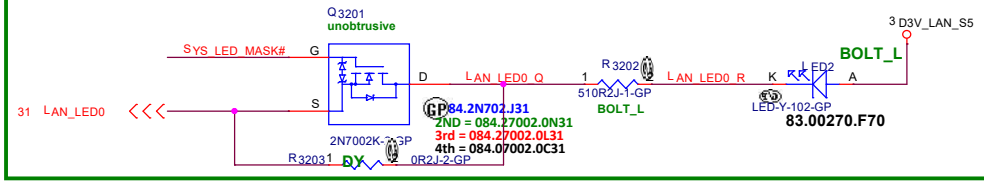
MDI



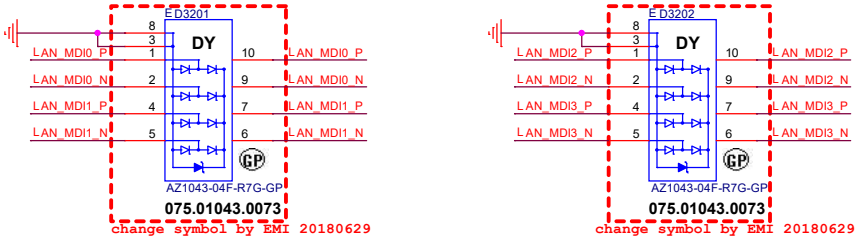
24,64 SYS_LED_MASK#

Green LED Status:
Blinking:Data transmit (10/100/1000)
Always Turn On: Network Connection exist
Turn Off: No network connection exist

LED



LED



TEST PAD

Layout:
Place near RJ45

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Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size	Document Number	Rev
A 3	BOLT WHL	1

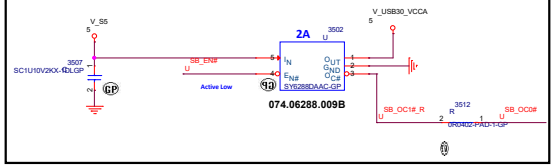
Date: Thursday, December 27, 2018 | Sheet 32 of 105

Main Func = USB3.0

USB Power Switch Enable

24,66 SB_EN#
16,36 SB_OC0#

USB Power Switch



USB Power Sharing

3.1 阻值範圍: ≥ 1Ω & 0Ω

型別	額定功率	最高額定電壓	最高過負荷電壓	T.C.R (ppm/°C) 溫度係數	阻值範圍 B(±0.1%) E-24 ~ E-96	D(±0.5%) E-24 ~ E-96	F(±1%) E-24 ~ E-96	G(±2%) ~ J(±5%) E-24	JUMPER (0Ω) 額定電流 J (±5%)	JUMPER (0Ω) 額定電流 F (±1%)	JUMPER (0Ω) 阻值 J (±5%)	JUMPER (0Ω) 阻值 F (±1%)
RT701 (0201)	1/20 W	25V	50V	-200 ~ +400	------	10Ω≦R<100Ω	10Ω≦R<100Ω	10Ω≦R<100Ω	0.5A	0.5A	50mΩ MAX.	35mΩ MAX.
				±200	47Ω≦R≦1MΩ	100Ω≦R≦10MΩ	100Ω≦R≦10MΩ	100Ω≦R≦10MΩ				
RT702 (0402)	1/16 W	50V	100V	±100	100Ω≦R≦1MΩ	100Ω≦R≦1MΩ	100Ω≦R≦22MΩ	100Ω≦R≦22MΩ	1A	1.5A	50mΩ MAX.	20mΩ MAX.
				±200	------	------	10Ω≦R<100Ω	10Ω≦R<100Ω				
RT703 (0603)	1/10 W	75V	150V	±100	100Ω≦R≦1MΩ	100Ω≦R≦1MΩ	100Ω≦R≦22MΩ	100Ω≦R≦22MΩ	1A	2A	50mΩ MAX.	20mΩ MAX.
				±200	------	10Ω≦R<100Ω	10Ω≦R<100Ω	10Ω≦R<100Ω				
RT705 (0805)	1/8 W	150V	300V	±100	100Ω≦R≦1MΩ	100Ω≦R≦10MΩ	100Ω≦R≦27MΩ	100Ω≦R≦27MΩ	2A	2.5A	50mΩ MAX.	20mΩ MAX.
				±200	------	10Ω≦R<100Ω	10Ω≦R<100Ω	10Ω≦R<100Ω				

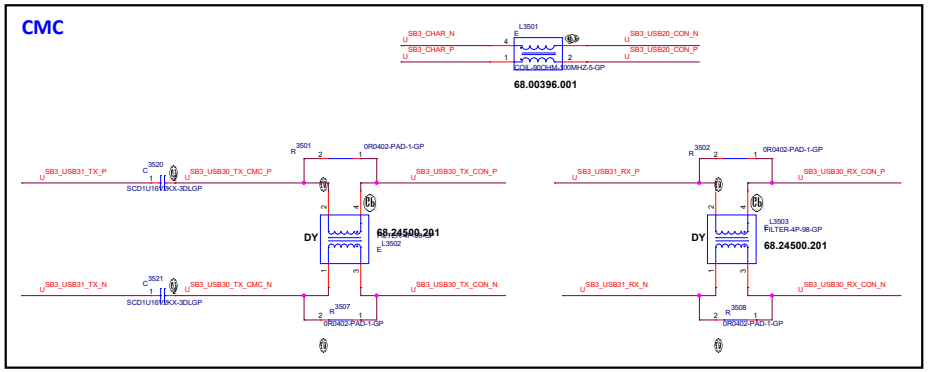
USB2.0 from USB Charger

36 SB3_CHAR_N
36 SB3_CHAR_P

USB3.1

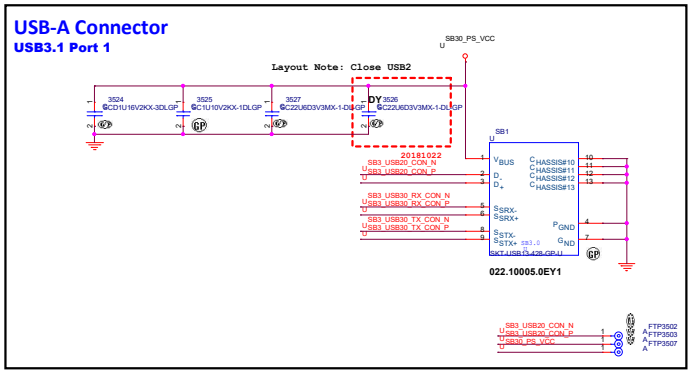
16 SB3_USB31_TX_P
16 SB3_USB31_TX_N
16 SB3_USB31_RX_P
16 SB3_USB31_RX_N

CMC



USB-A Connector

USB3.1 Port 1



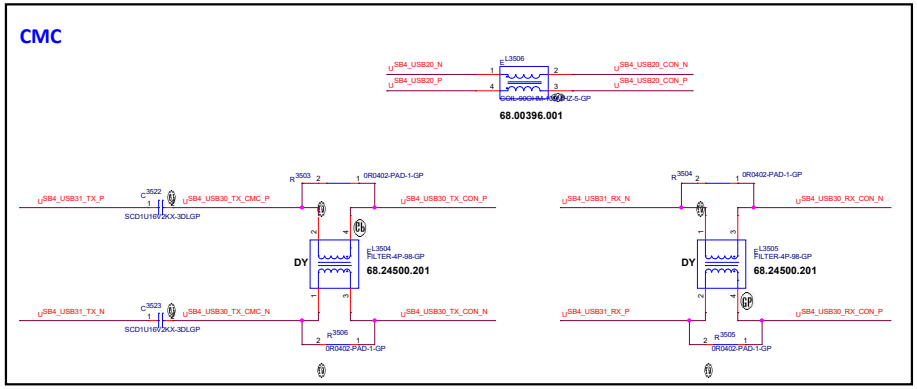
USB2.0

16 SB4_USB20_N
16 SB4_USB20_P

USB3.1

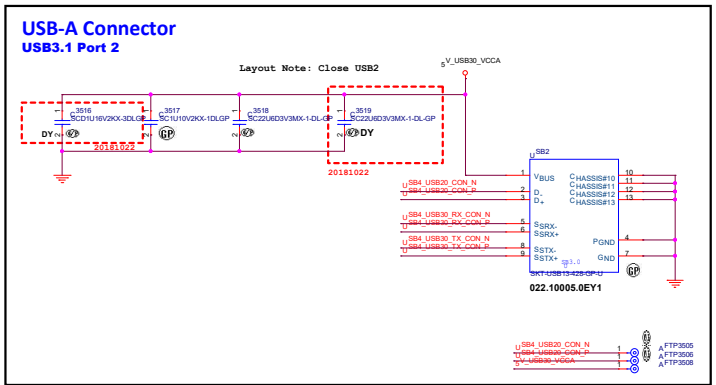
16 SB4_USB31_TX_P
16 SB4_USB31_TX_N
16 SB4_USB31_RX_P
16 SB4_USB31_RX_N

CMC

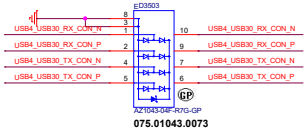


USB-A Connector

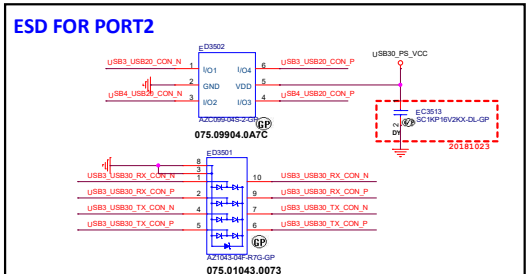
USB3.1 Port 2



ESD FOR PORT1



ESD FOR PORT2



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Title: USB3.0 CONN

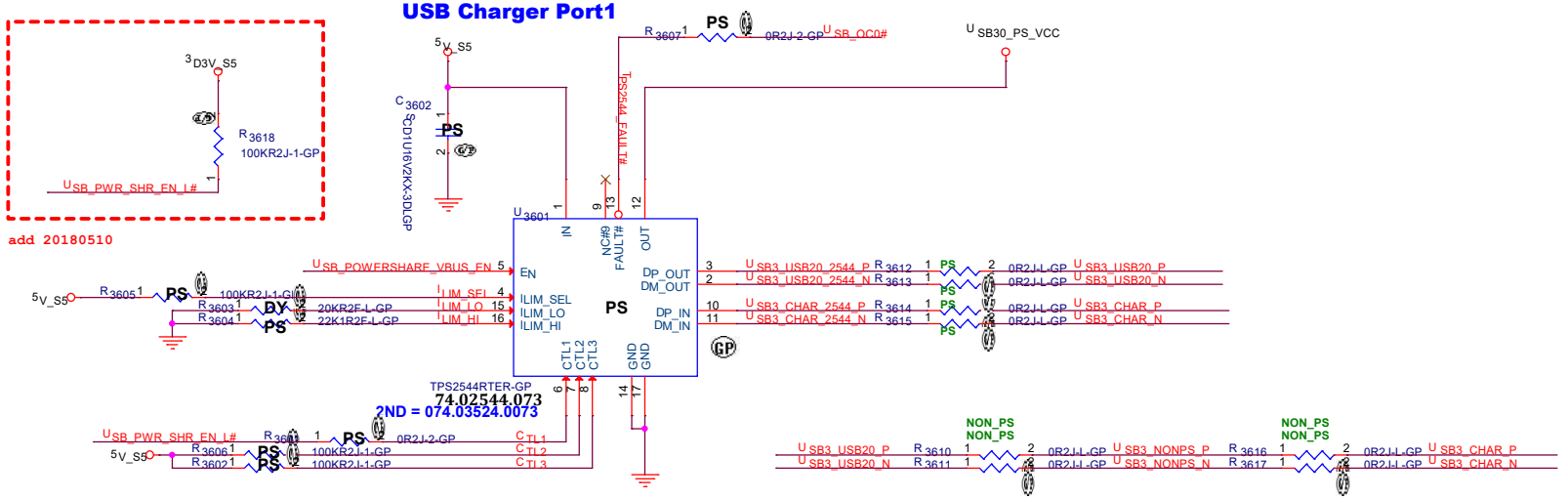
Size: Custom | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 35 of 105

Main Func = USB Charger

Reserved

USB Charger Port1



add 20180510

Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}\,(mA) = \frac{50{,}500}{(R_{ILIM\_XX}\,(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

35 USB3_CHAR_P
35 USB3_CHAR_N
16 USB3_USB20_P
16 USB3_USB20_N
24 USB_POWERSHARE_VBUS_EN
24 USB_PWR_SHR_EN_L#
16,35 USB_OC0#

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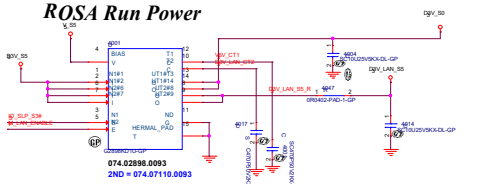
Title: USB Charger
Size: C ustom | Document Number: BOLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet 36 of 105

Main Func = Power Plane & Sequence

3D3V_S0/5V_S0

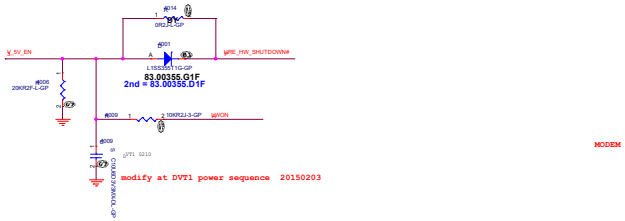
ROSA Run Power

2018.03.28
separate 3D3V_S0/5V_S0 for layout



3D3V_S0/LAN POWER

3D3V_S0 Consumption
Peak current 2.5A



5V_S0/1D8V_S0

5V_S0 Consumption
Peak current 5A

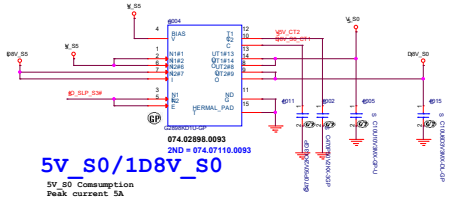
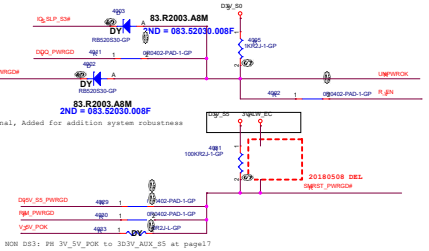


Table 4. Rise Time Values

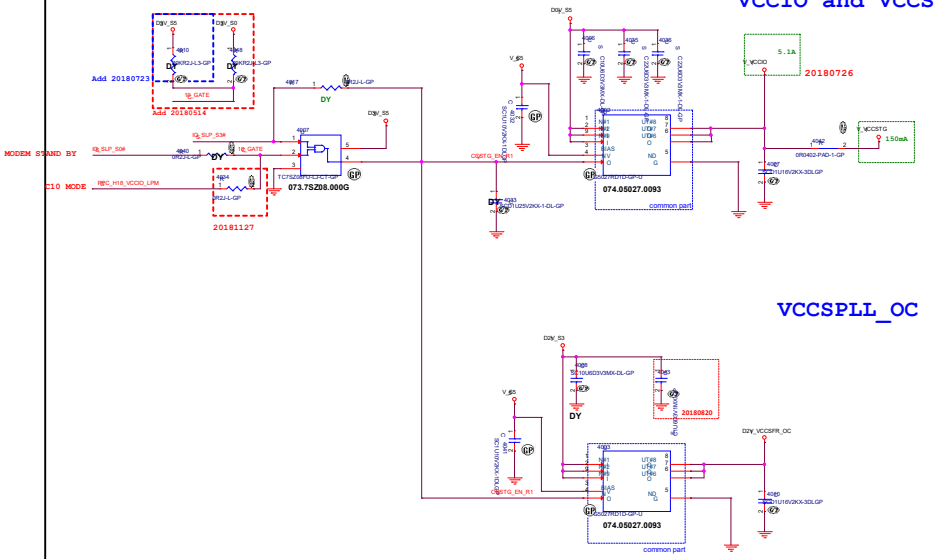
CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω(1)						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1554	1332	1097	949	627
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

Power Good

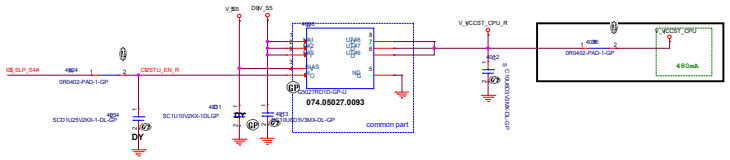


VCCIO and VCCSTG



VCCSPLL_OC

VCCST/VCCPLL



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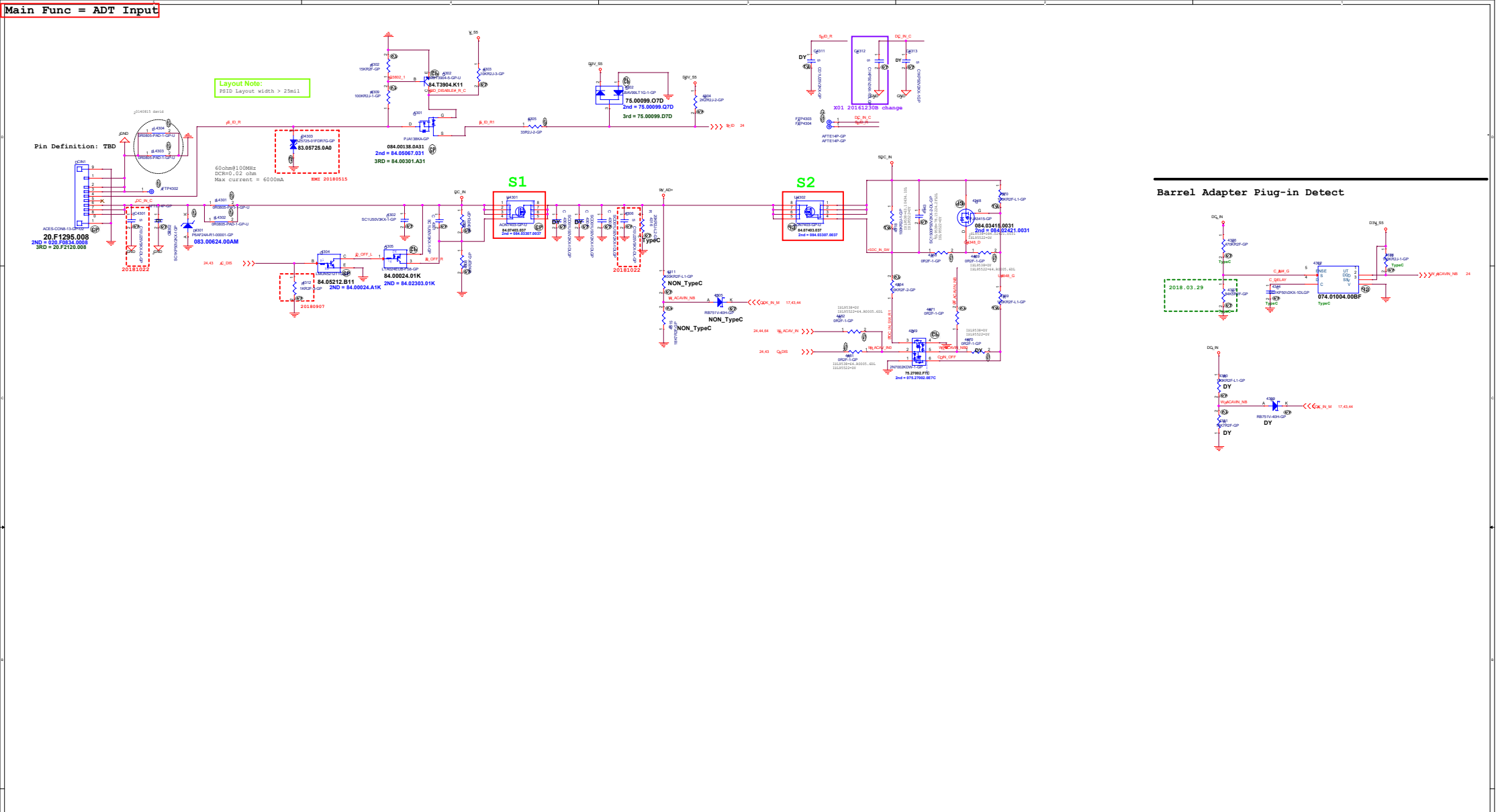
W Istron Corporation
P_3R, Sec.1, Hsin Tai Wu Rd., Hsichih,
Hsin Hsien 221, Taiwan, R.O.C.

Title: P ower Plane Enable

Size: B | Document Number: BOLT WHL | Rev: 1

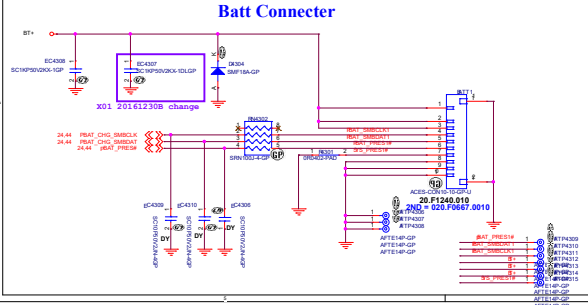
Date: Thursday, December 27, 2018 | Sheet 40 of 55

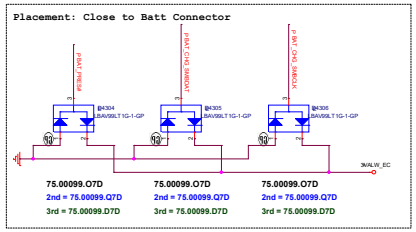
Main Func = ADT Input



Barrel Adapter Piug-in Detect

Main Func = M-BAT Input





BOLT L 14 EMMC

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spei Hsien 221, Taiwan, R.O.C.

Title: D CIN

Size	Document Number	Rev
A	BOLT WHL	1

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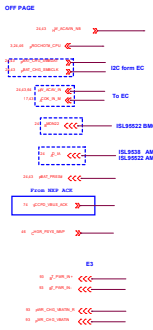
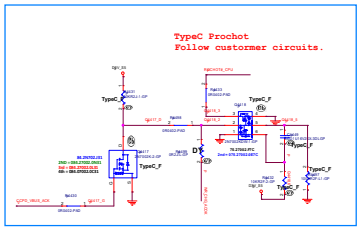
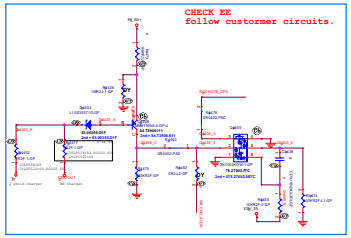
Main Func = Charger

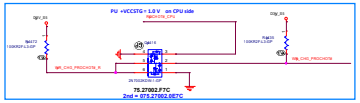
ISL95522 Hybrid Charger

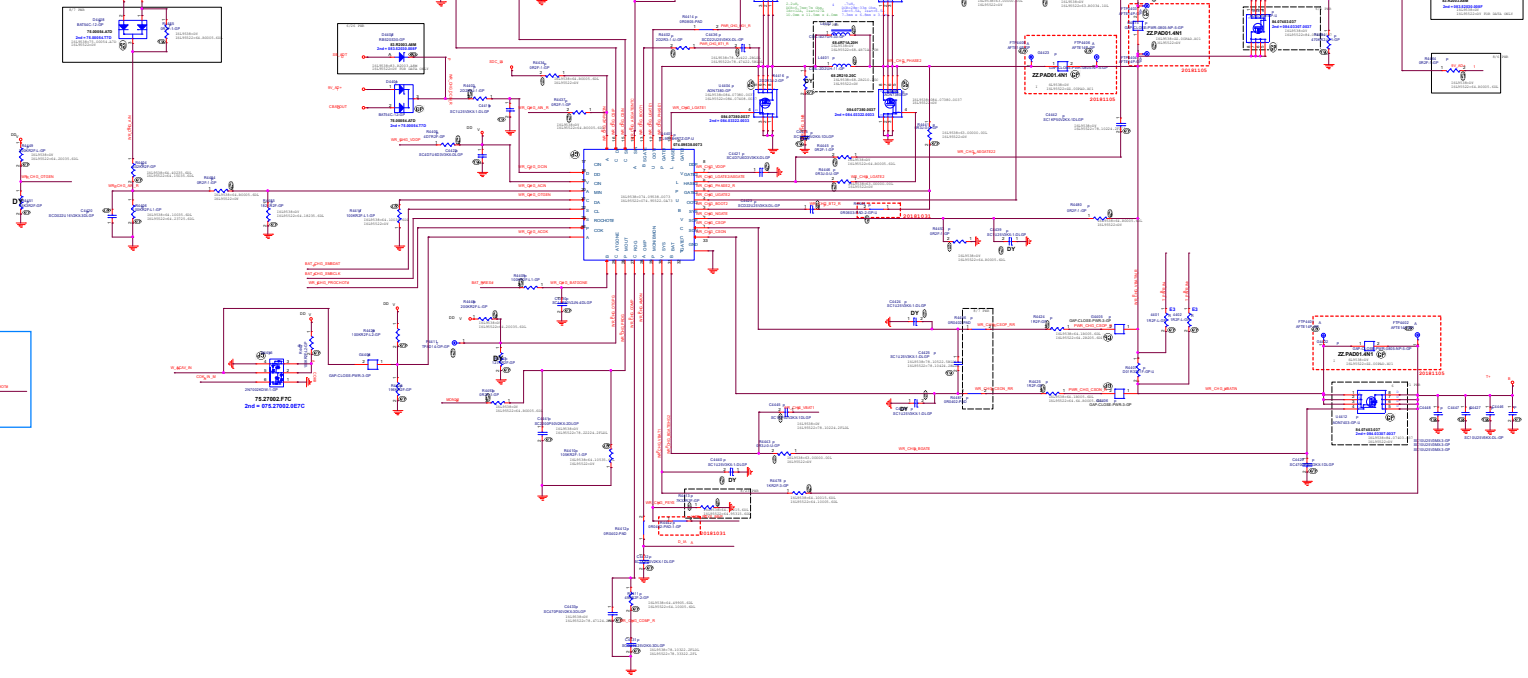
Default **ISL9538 Buck-Boost Charger**











BOM Change List

ISL9538

TABLE 22. PROG PIN PROGRAMMING OPTIONS

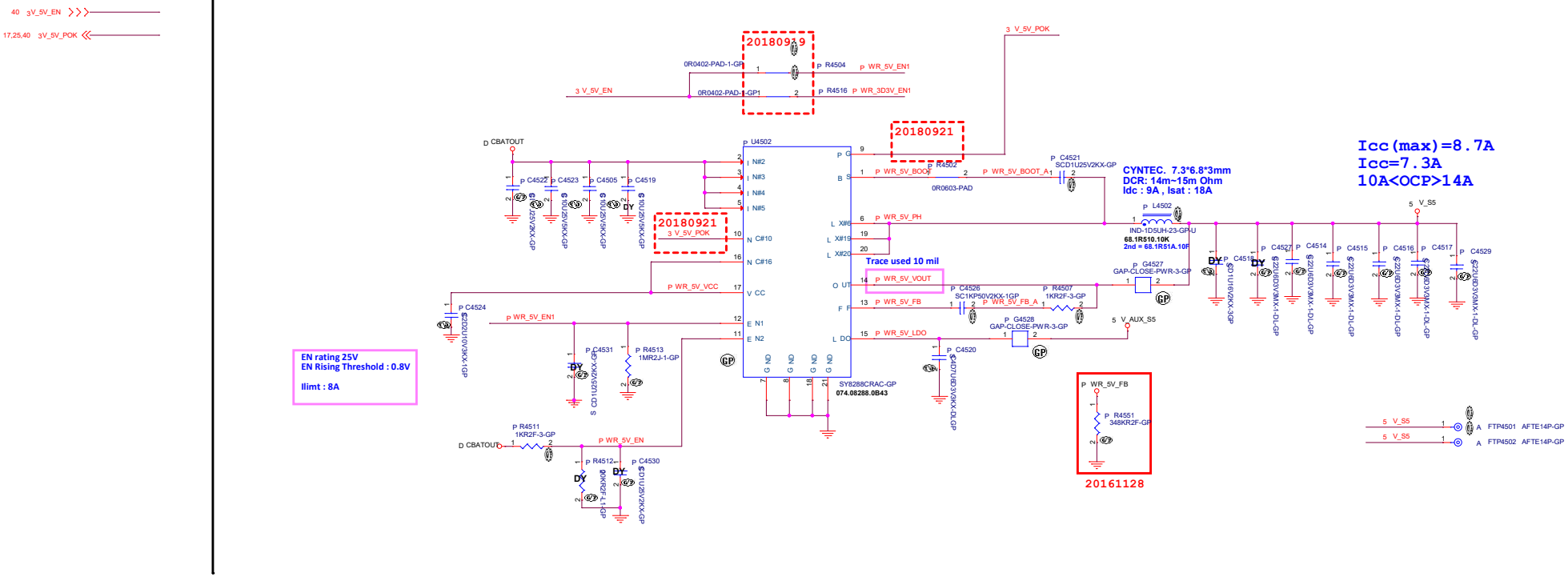
PROG-GND RESISTANCE (kΩ)				DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
MIN	TYP 1%	MAX	CELL #			
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.6				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

ISL95522

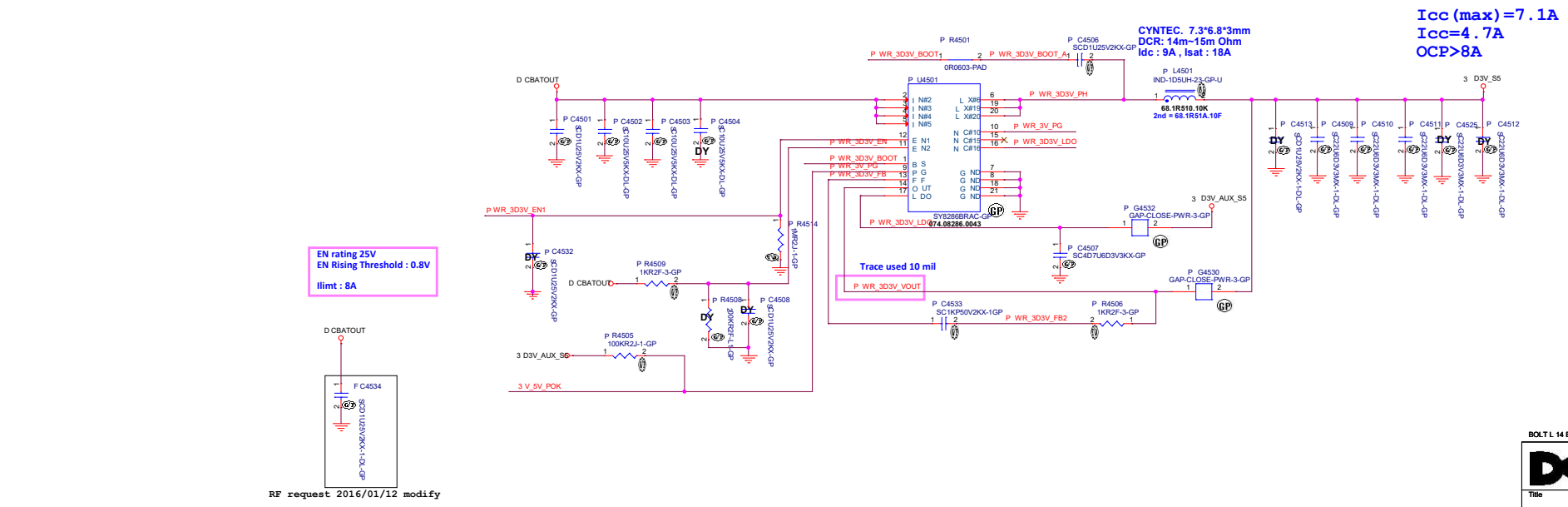
Table 17. Prog Pin Programming Options

Prog-GND Resistance (kΩ)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
Typ (1% Standard Resistor)			
0	NVDC	$R_{S1}:R_{S2}$ = 2:1 R_{S1} = 10mΩ R_{S2} = 5mΩ or R_{S1} = 20mΩ R_{S2} = 10mΩ	3
22.6			4
38.3			2
69.8		$R_{S1}:R_{S2}$ = 1:1 R_{S1} = 10mΩ R_{S2} = 10mΩ or R_{S1} = 20mΩ R_{S2} = 20mΩ	3
86.6			4
102			2
150	HPB		4
165			2
182			3
215		$R_{S1}:R_{S2}$ = 2:1 R_{S1} = 10mΩ R_{S2} = 5mΩ or R_{S1} = 20mΩ R_{S2} = 10mΩ	4
237			2
255			3

Main Func = PWR.Plane.Regulator_5V



SSID = PWR.Plane.Regulator_3D3V



BOLT L 14 EMMC

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2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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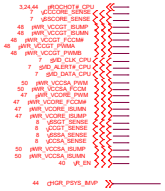
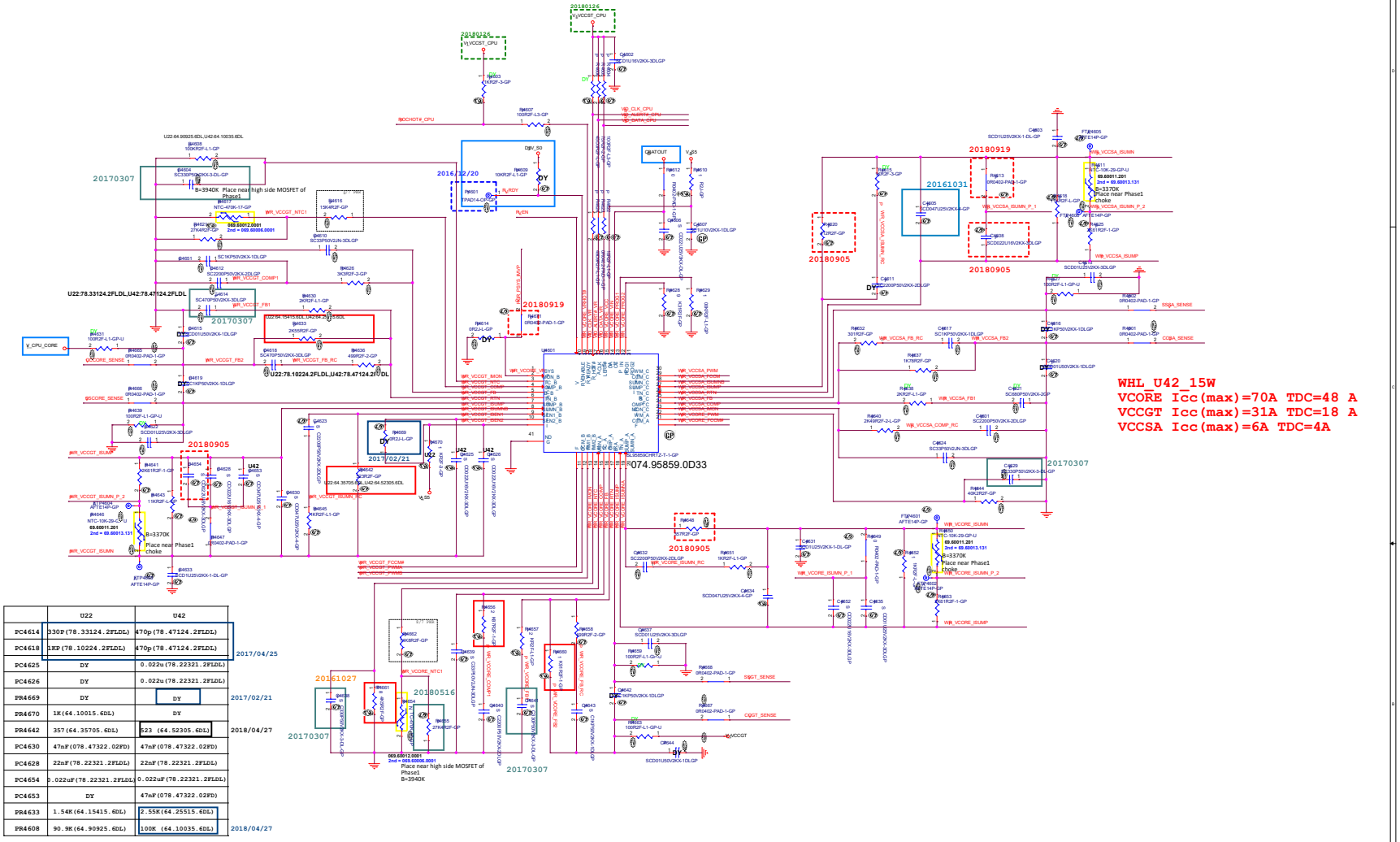
Title: *(Reserved)*

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 45 of 105

Main Func = CPU_CORE





	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4670	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	523 (64.52305.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	0.022uF(78.22321.2FLDL)	0.022uF(78.22321.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PR4608	90.9K(64.90925.6DL)	100K (64.10035.6DL)

BOLT L 14 EMAC

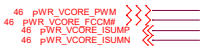
DELL W Istron Corporation
No.88, Sec.1, Hsin Tai Wu Rd., Hsichih, Hsin Hsien 221, Taiwan, R.O.C.

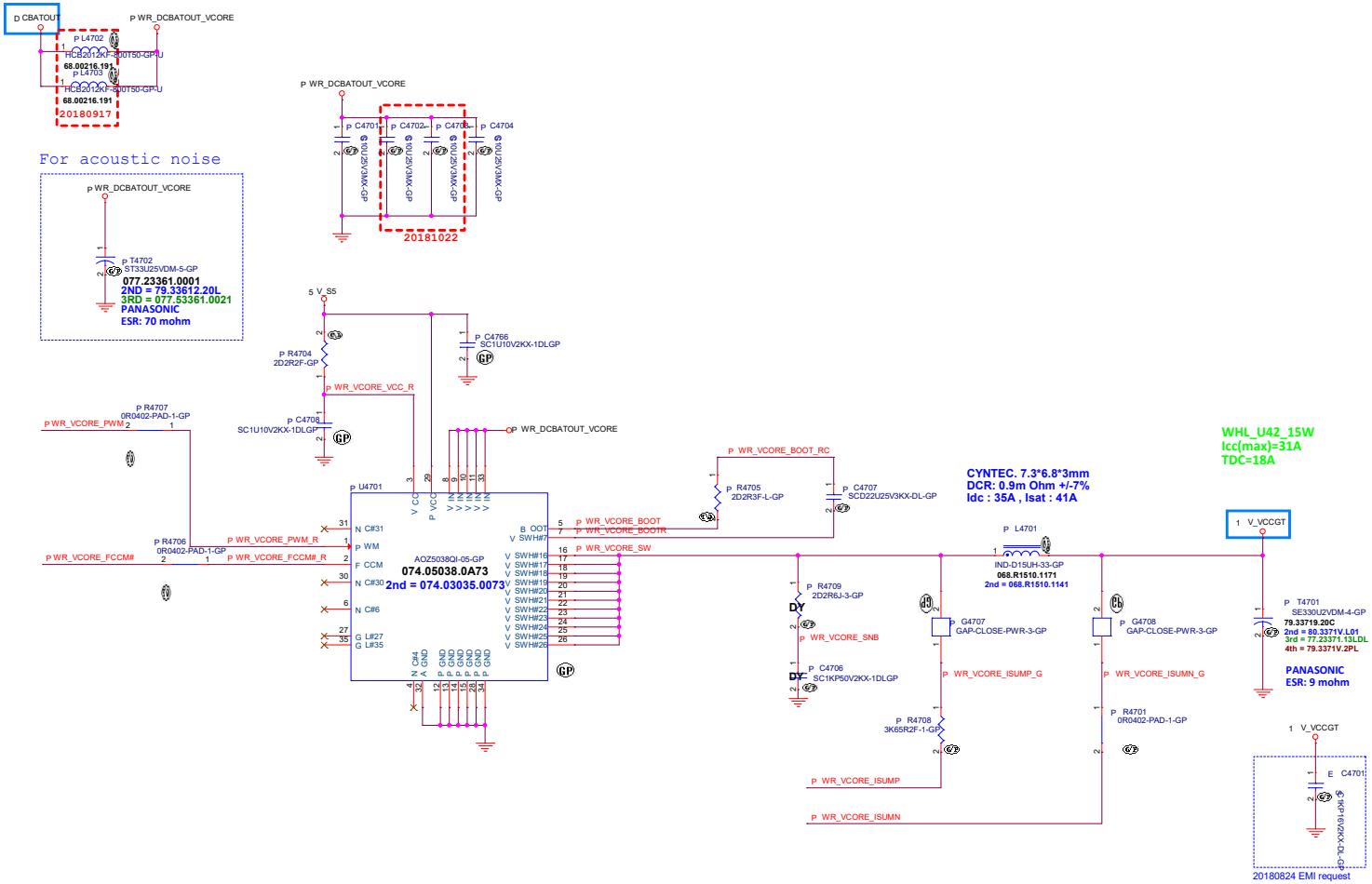
Title: I SL95859_CPUCORE

Size: A | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 46 of 105

Main Func = CPU_CORE





<Core Design>

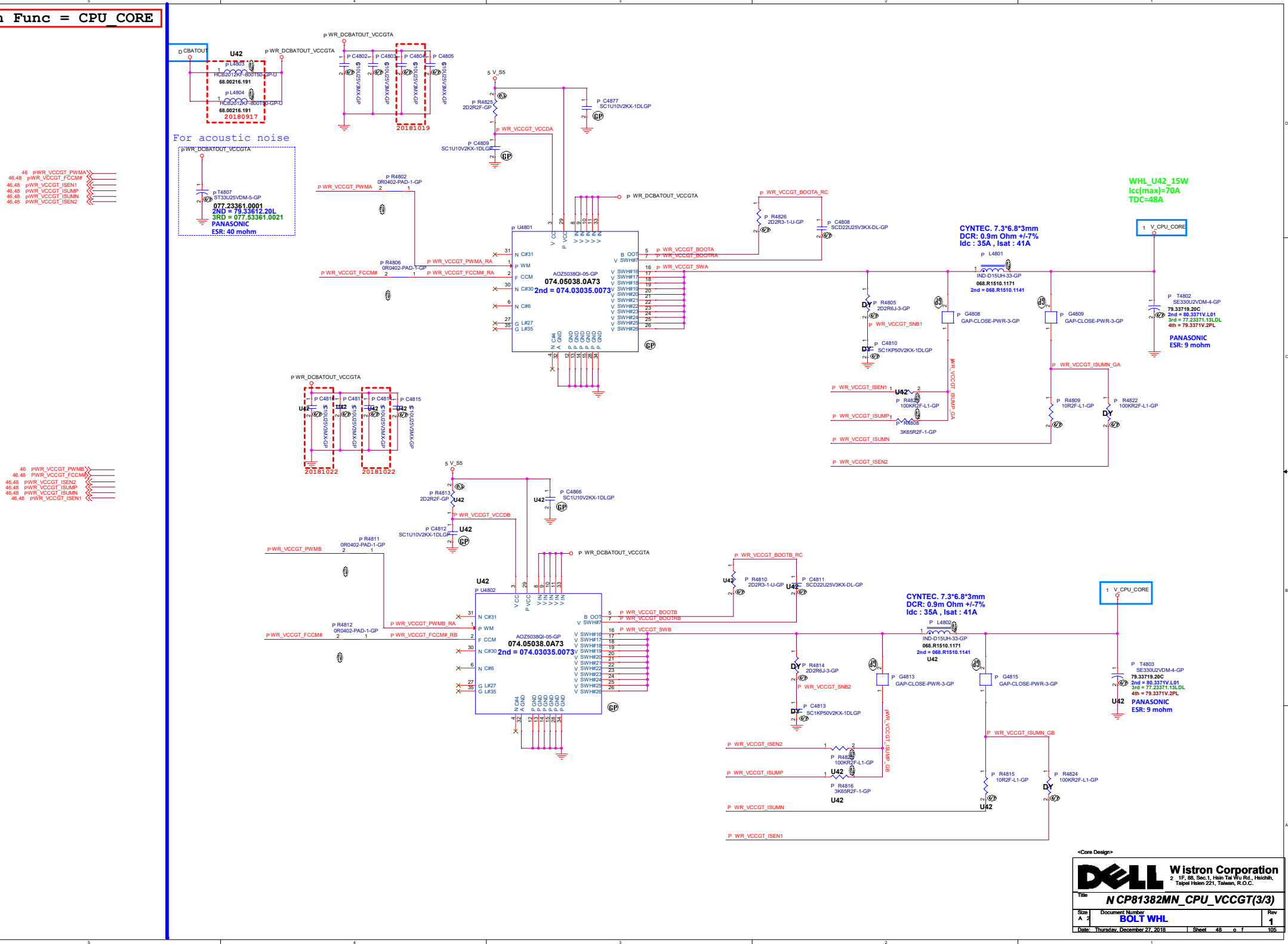
Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N CP81382MN_CPU_VCORE(2/3)

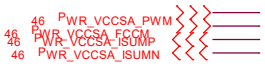
Size	Document Number	Rev
A 2	BOLT WHL	1

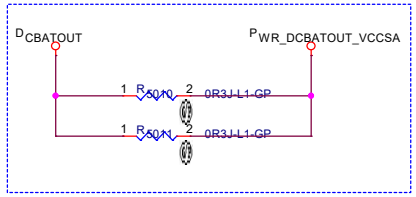
Date: Thursday, December 27, 2018 | Sheet 47 of 105

Main Func = CPU_CORE

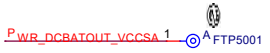


Main Func = CPU_CORE

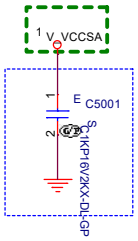




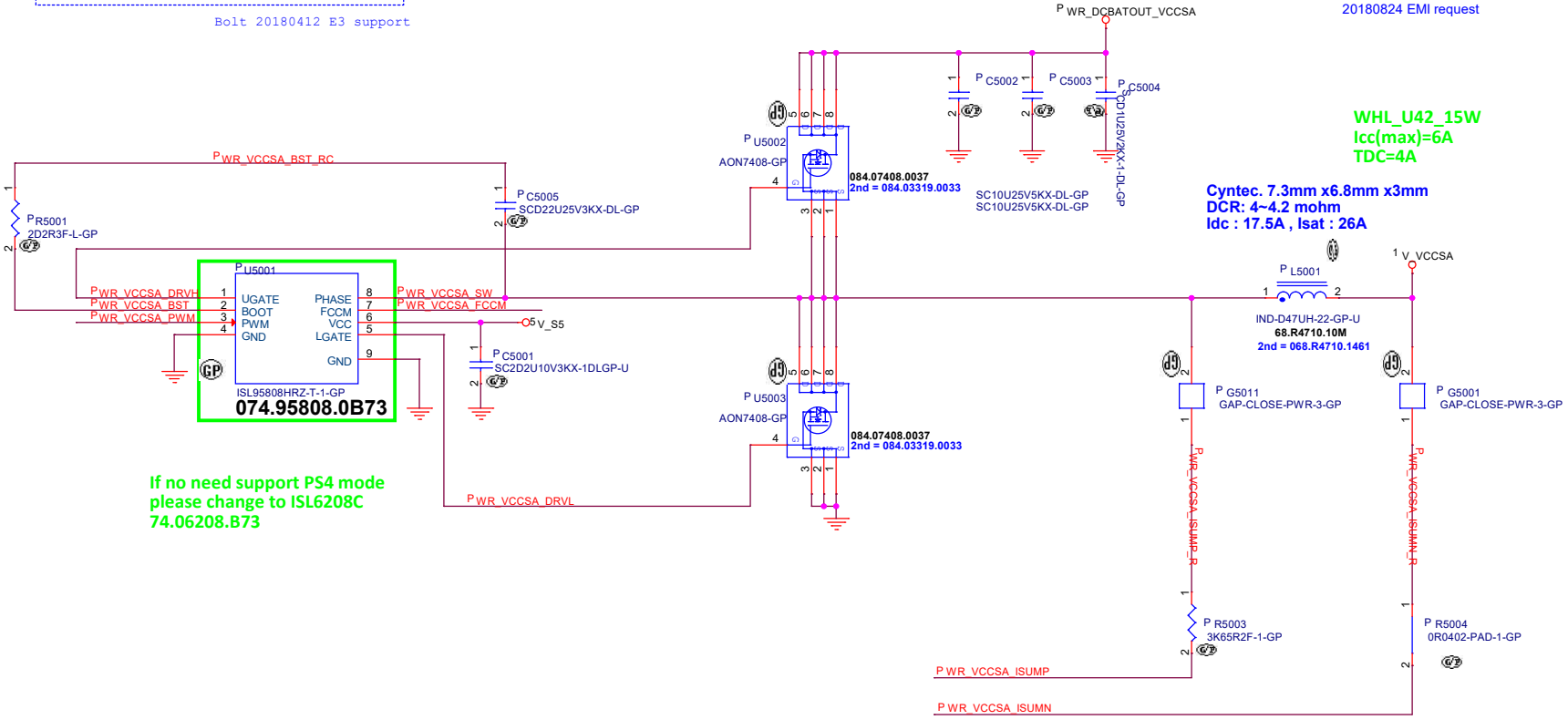
Bolt 20180412 E3 support



20180126



20180824 EMI request



WHL_U42_15W
Icc(max)=6A
TDC=4A

Cyntec. 7.3mm x6.8mm x3mm
DCR: 4~4.2 mohm
Idc : 17.5A , Isat : 26A

If no need support PS4 mode
please change to ISL6208C
74.06208.B73

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

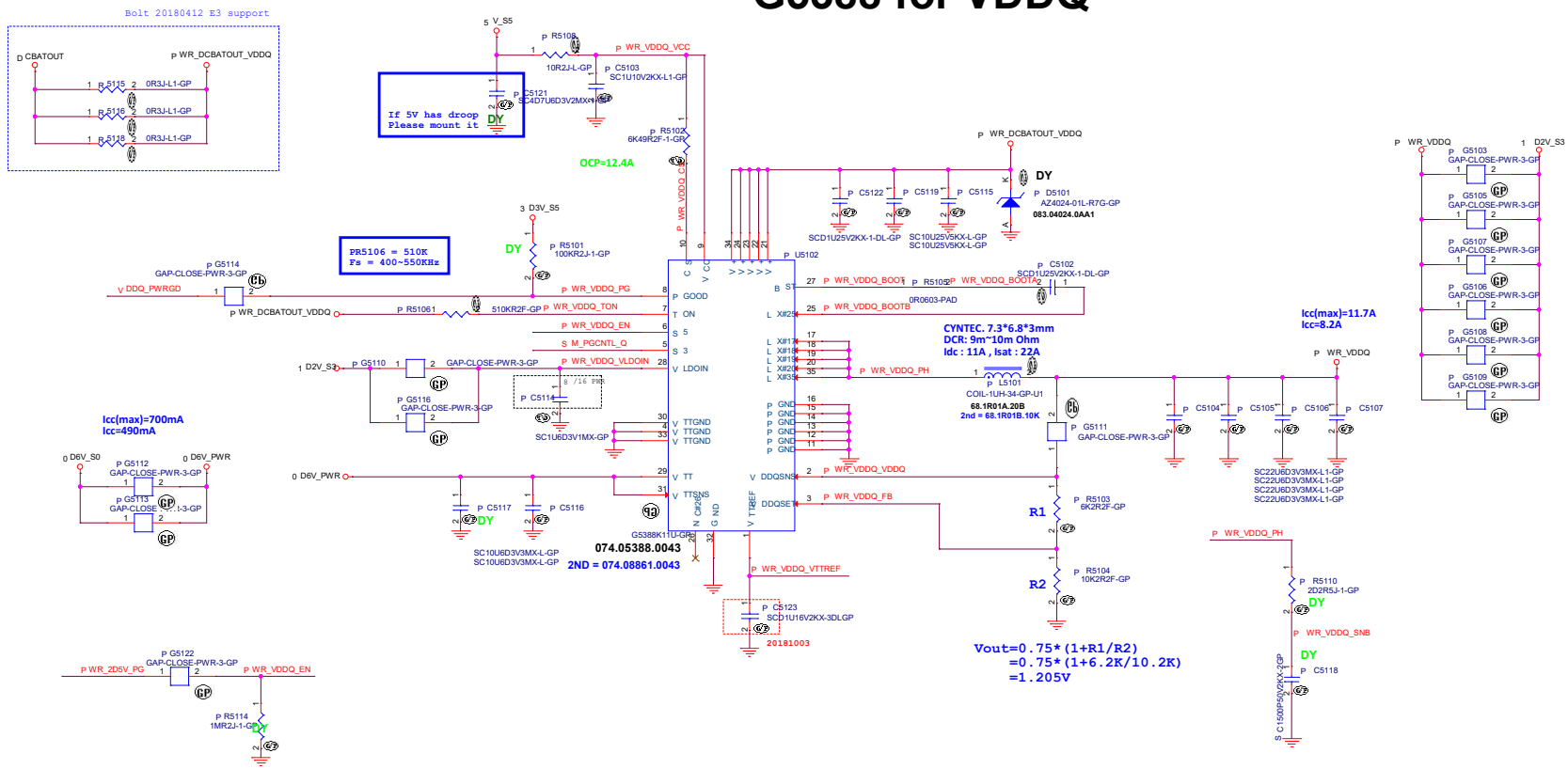
Title: VCCSA

Size	Document Number	Rev
A 3	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 50 of 105

Main Func = PWR.Plane.Regulator_1D2V/0D6V

G5388 for VDDQ

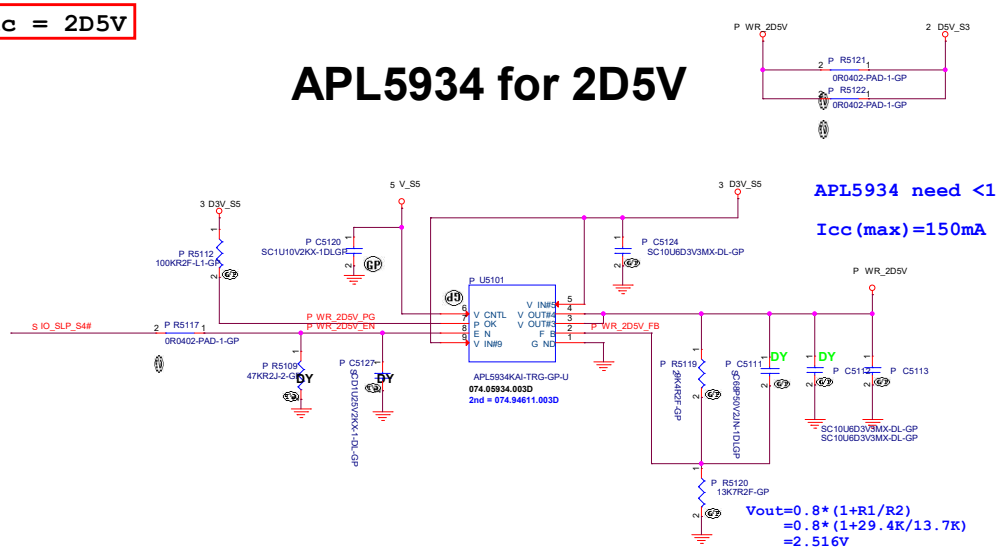


40 vDDQ_PWRGD
EE needs check it!!

5 sM_PGCNTL_Q
17,40,92 sIO_SLP_S4#

Main Func = 2D5V

APL5934 for 2D5V



BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

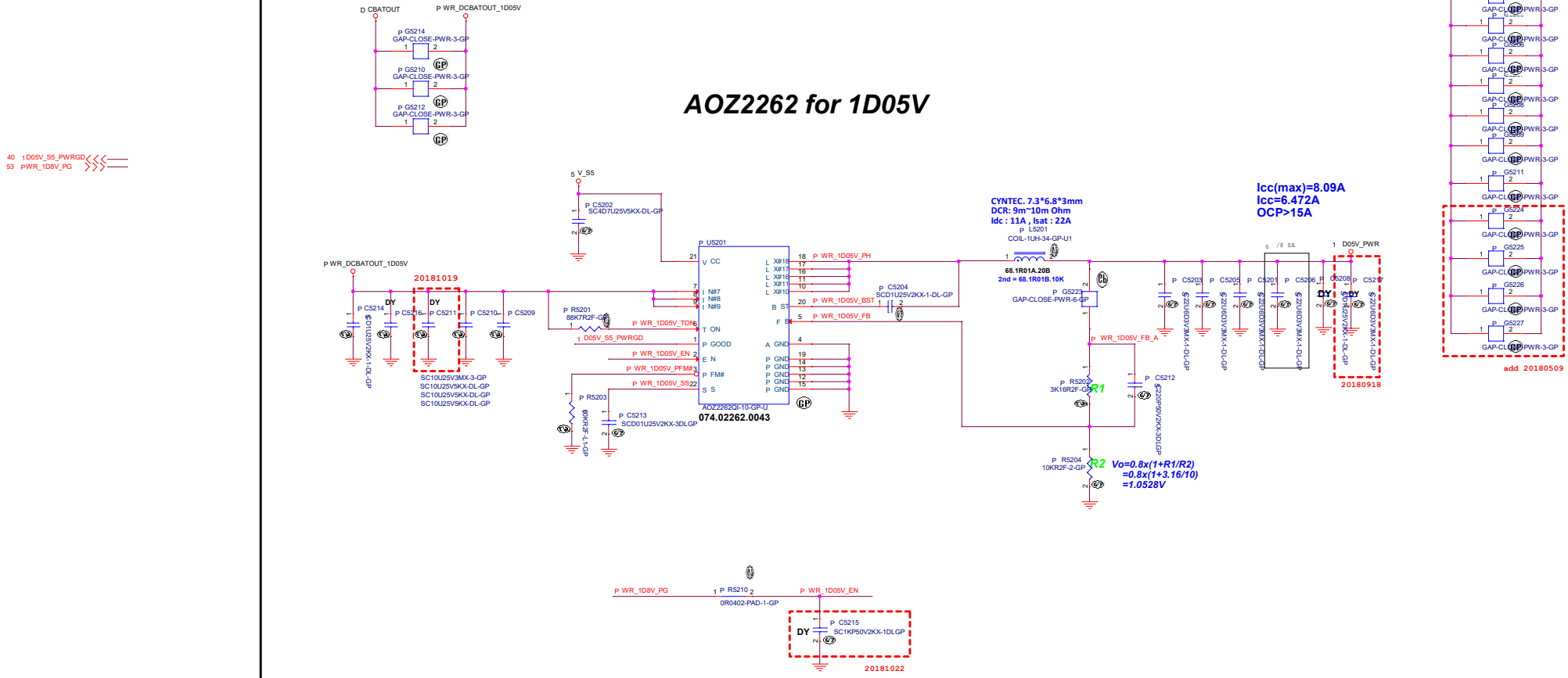
Title: Power_(5388_VDDQ/VTT)

Size	Document Number	Rev
A 2	Bolt WHL-U	1

Date: Thursday, December 27, 2018 Sheet 51 of 105

Main Func = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D05V



BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AOZ2262_1D05V

Size	Document Number	Rev
A 2	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 52 of 105

OFFPAGE

52 PWR_1D8V_PG

25 3V_5V_DSW_OK

PR5308 1 2 PWR_1D8V_EN

0R0402-PAD-1-GP

Main Func = 1D8V

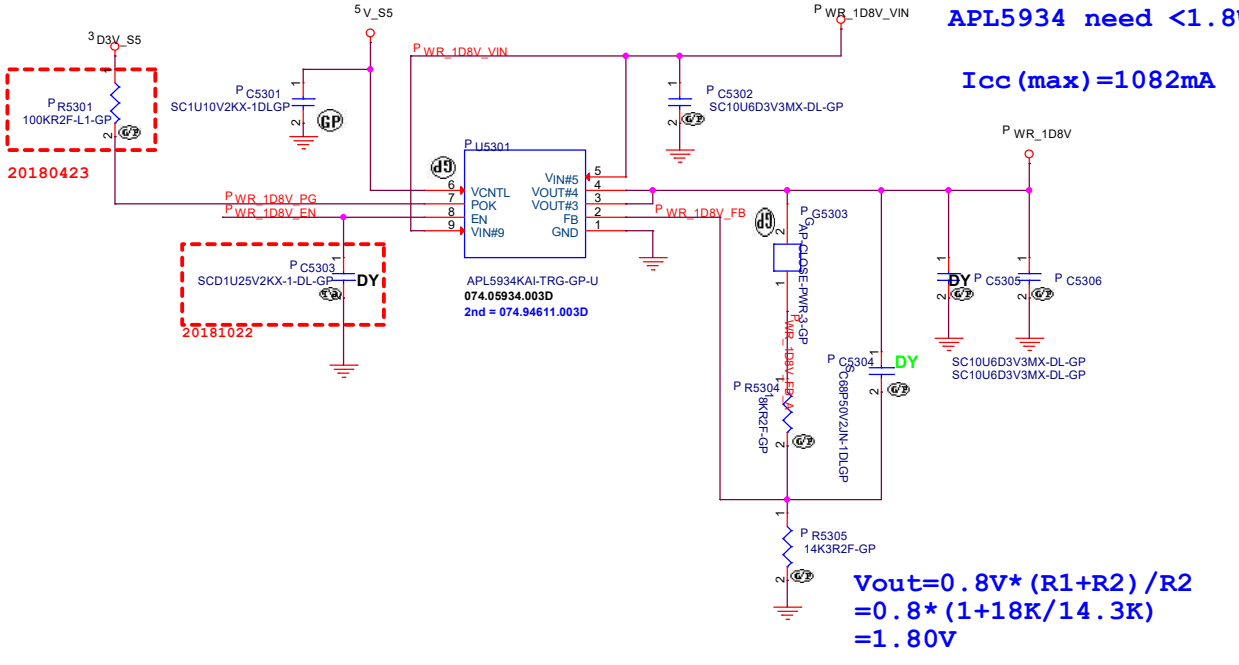
OFFPAGE_GAP

3D3V_S5 — PG5302 GAP-CLOSE-PWR-3-GP — PWR_1D8V_VIN

1D8V_S5 — PG5301 GAP-CLOSE-PWR-3-GP — PWR_1D8V

20181031

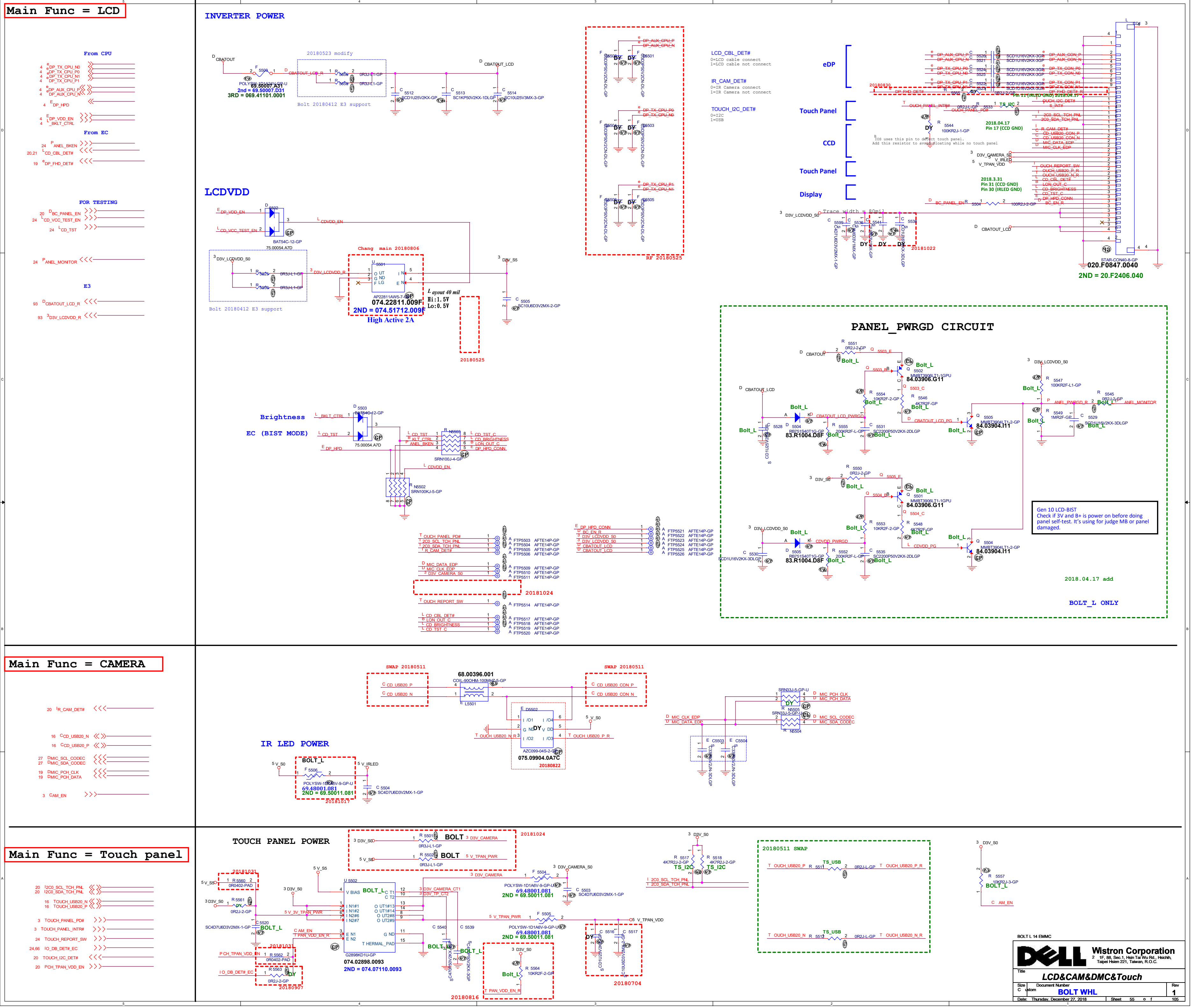
APL5934 for 1D8V



BOLT L 14 EMMC

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

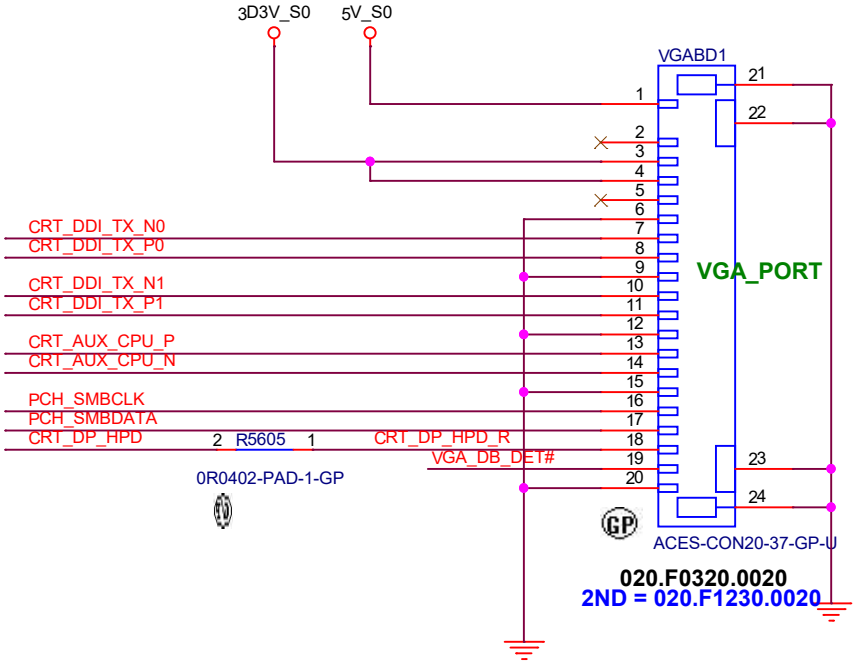
Title			
1D8V			
Size A 3	Document Number BOLT WHL		Rev 1
Date: Thursday, December 27, 2018	Sheet 53	of	105



Main Func = LCD
INVERTER POWER
LCDVDD
From CPU
From EC
FOR TESTING
E3
eDP
Touch Panel
CCD
Touch Panel
Display
Brightness
EC (BIST MODE)
PANEL_PWRGD CIRCUIT
Gen 10 LCD-BIST
Check if 3V and B+ is power on before doing panel self-test. It's using for judge MB or panel damaged.
2018.04.17 add
BOLT_L ONLY
High Active 2A
074.22811.009F
2ND = 074.51712.009F
020.F0847.0040
2ND = 20.F2406.040
Main Func = CAMERA
IR LED POWER
SWAP 20180511
68.00396.001
075.09904.0A7C
Main Func = Touch panel
TOUCH PANEL POWER
074.02898.0093
2ND = 074.07110.0093
20180511 SWAP
Wistron Corporation
LCD&CAM&DMC&Touch
BOLT WHL
Thursday, December 27, 2018
Sheet 55 of 105
Rev 1

Main Func = CRT

58 CRT_DDI_TX_N0
58 CRT_DDI_TX_P0
58 CRT_DDI_TX_N1
58 CRT_DDI_TX_P1
58 CRT_AUX_CPU_P
58 CRT_AUX_CPU_N
12,13,18,70 PCH_SMBCLK
12,13,18,70 PCH_SMBDATA
58 CRT_DP_HPD
20 VGA_DB_DET#



BOLT

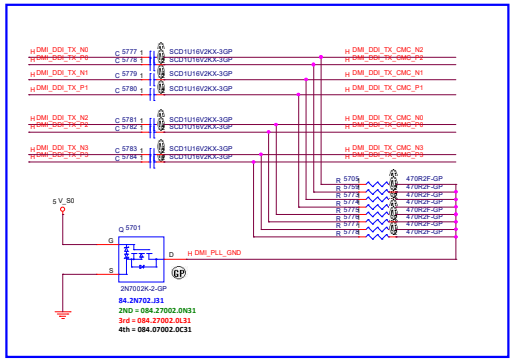
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

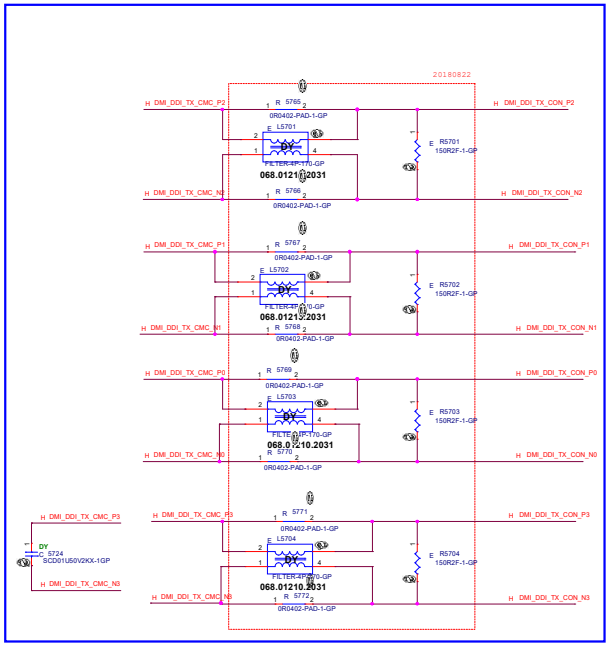
Title: CRT

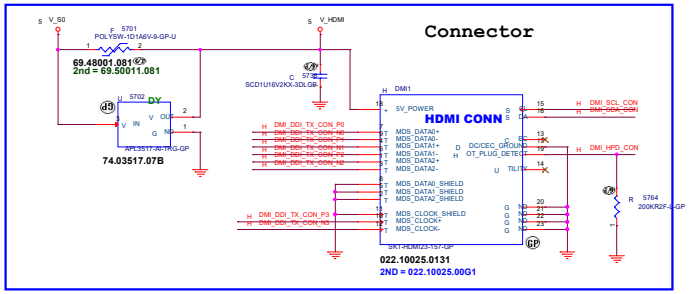
Size	Document Number	Rev
A4	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 56 of 105

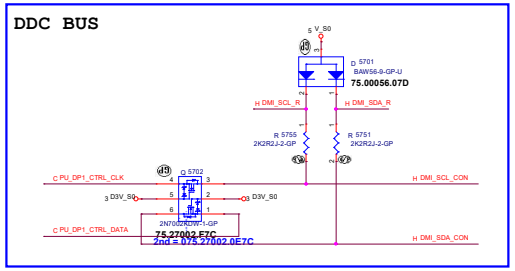
Main Func = HDMI



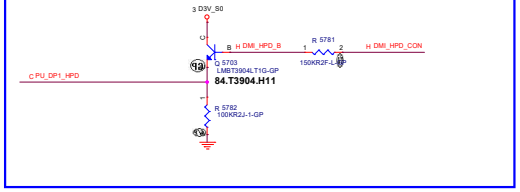




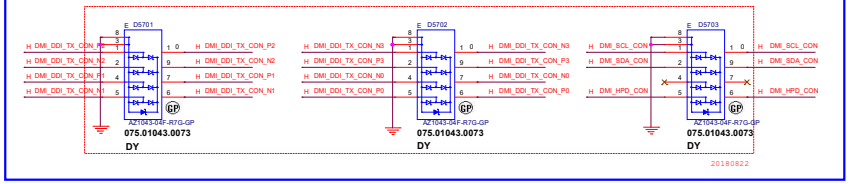
DDC BUS



HOT PLUG



ESD



BOLT L 14 EMMC

DELL	Wistron Corporation 2F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: H DMI		
Size: C	Document Number: BOLT WHL	Rev: 1
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Main Func = DP Demux

CPU DP to DP De-MUX

FOR Type C

FOR VGA

2018.03.24

CPU

CONN

20180827

71.08338.A03

FOR Type C

FOR VGA

For AUX

2018.10.31

close to U5802

20181106

SW	I/O	Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O For *Control Switching Mode (CFG0 = L)*: SW = L: Port1 is selected (default) SW = H: Port2 is selected For *Automatic Switching Mode (CFG0 = H)*: SW = L: Port1 has higher priority when both ports are plugged (default) SW = H: Port2 has higher priority when both ports are plugged ***Overwritten by I2C register in I2C Control Mode***

BOLT L 14 EMMC

Wistron Corporation
5F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DP De-MUX

Size: C (Custom) | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 58 of 105

Main Func = HDD

HDD

16 HDD_SATA_TX_P11
16 HDD_SATA_TX_N11
16 HDD_SATA_RX_P11
16 HDD_SATA_RX_N11

70 FFS_INT2_Q
16 HDD_DEVSLP
18,20 HDD_DET#

SATA RE-DRIVER

20180808

NON HDD re-driver
NON HDD re-driver
NON HDD re-driver
NON HDD re-driver

HDD_SATA_TX_P11 — C 6028 — SCD01U25V2KX-3DLGP — DD2_SATA_TX_CON_P
HDD_SATA_TX_N11 — C 6029 — SCD01U25V2KX-3DLGP — DD2_SATA_TX_CON_N
HDD_SATA_RX_N11 — C 6030 — SCD01U25V2KX-3DLGP — DD2_SATA_RX_CON_N
HDD_SATA_RX_P11 — C 6031 — SCD01U25V2KX-3DLGP — DD2_SATA_RX_CON_P

20180809

HDD POWER

5 V_S0 — 80 mils — R 6005 0R0805-PAD-1-GP-U — 5 V_HDD_S0

C 6006 SC10U10V2MX-DL-GP1 HDD
C 6007 SCD1U16V2KX-3DLGP DY

20181022

SATA HDD Connector

DD1

DD_DET#
5 V_HDD_S0
5 V_HDD_S0
F FS_INT2_Q
DD_DEVSLP
R 6002 0R0402-PAD-1-GP
DD_DEVSLP_R
DD2_SATA_RX_CON_P
DD2_SATA_RX_CON_N
DD2_SATA_TX_CON_N
DD2_SATA_TX_CON_P

HDD_Wire

ACES-CON20-37-GP-U
020.F0320.0020
2ND = 020.F1230.0020

change 20180629

CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

DD2

DD2_SATA_TX_CON_P
DD2_SATA_TX_CON_N
DD2_SATA_RX_CON_N
DD2_SATA_RX_CON_P
DD_DEVSLP_R
5 V_HDD_S0
F FS_INT2_Q

HDD_FFC

STM-CON12-1-GP
020.K0222.0012
2ND = 020.K0158.0012

change 20180629

HDD ESD

Layout Note:
Place near HDD2
Close to HDD1

DY
D6001
AZ1043-04F-R7G-GP
075.01043.0073

DD2_SATA_TX_CON_P
DD2_SATA_TX_CON_N
DD2_SATA_RX_CON_N
DD2_SATA_RX_CON_P

20180822

Main Func = ODD

ODD

16 ODD_SATA_TX_N12
16 ODD_SATA_TX_P12
16 ODD_SATA_RX_P12
16 ODD_SATA_RX_N12
16 SATA1_ODD_PRSNT#

ODD Connector

5 V_S0 — R 6003 — 0R0805-PAD-1-GP-U — 5 V_ODD_S0

C 6018 SC10U10V2MX-DL-GP-U ODD
C 6019 SCD1U16V2KX-3DLGP ODD

ODD

DD_SATA_TX_P12 — C 6014 — SCD01U25V2KX-3DLGP — DD_SATA_TX_CON_P
DD_SATA_RX_P12 — C 6011 — SCD01U25V2KX-3DLGP — DD_SATA_RX_CON_P
SATA1_ODD_PRSNT# — R 6004 — 0R0402-PAD-1-GP — SATA_ODD_PRSNT#_R

ODD DD1

DD_SATA_TX_CON_N — C 6013 — SCD01U25V2KX-3DLGP — DD_SATA_TX_N12
DD_SATA_RX_CON_N — C 6010 — SCD01U25V2KX-3DLGP — DD_SATA_RX_N12

5 V_ODD_S0
5 V_ODD_S0
SATA_ODD_DA#_C — P6001

ACES-CON16-GP
020.K0386.0016

DD_SATA_TX_CON_P
DD_SATA_TX_CON_N
DD_SATA_RX_CON_N
DD_SATA_RX_CON_P
SATA_ODD_PRSNT#_R
5 V_ODD_S0
5 V_ODD_S0

FTP6001 AFTE14P-GP
FTP6002 AFTE14P-GP
FTP6003 AFTE14P-GP
FTP6004 AFTE14P-GP
FTP6005 AFTE14P-GP
FTP6006 AFTE14P-GP
FTP6007 AFTE14P-GP

BOLT L 14 EMMC

Wistron Corporation
2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

Size: A 2 | Document Number: BOLT WHL | Rev: 1

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Main Func = WLAN

BT

21 BLUETOOTH_EN
16 BT_USB20_N
16 BT_USB20_P

WLAN

18 CLK_PCIE_WLAN_REQ#
18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P

16 WLAN_PCIE_RX_N10
16 WLAN_PCIE_RX_P10
16 WLAN_PCIE_TX_N10
16 WLAN_PCIE_TX_P10

CNVI

19 BT_PCMFRM_RSTN
19 BT_PCMOUT_CLKREQ0
18 PULSAR_38P4M_REFCLK

20 CNV_RGI_RSP
15,20 CNV_RGI_DT_R

20 CNV_BRI_RSP
20 CNV_BRI_DT_R

21 CNV_WT_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1

21 CNV_WR_CLK_DP
21 CNV_WR_CLK_DN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1

Others

18,24 SUS_CLK

4 CNVI_EN#
17,24 AUX_EN_WOWL_R

17,18,24 JIO3_PCIE_WAKE#

21 WIFI_RF_EN
17,26,31,62,63,91 PLTRST#_CPU

CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN

3 D3V_WLAN
P LTRST#_CPU
B LUETOOTH_EN
W IFI_RF_EN
C LK_PCIE_WLAN_REQ#
B T_USB20_CON_N
B T_USB20_CON_P
J IO3_PCIE_WAKE#

A FTP6113
FTP6108
FTP6112
FTP6110
FTP6109
FTP6111
FTP6114
FTP6115

DEL 20180523

R 6125 CNVI 0R5J-5-GP
3 D3V_S5
U 6101
GS17F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
C 6102 SC4D7U6D3V3KX-L-GP DY
20181022
C 6106 SCD1U25V2KX-1-DLGP DY
C 6105 SC10U6D3V3MX-DL-GP
20181022
3 D3V_WLAN
non CNVI
R 6124 0R6J-L-GP
3 D3V_S0
C 6104 SCD1U16V2KX-3DLGP
Layout 20180516

C NVI_EN# R 6110 0R2J-L-GP DY
R 6101 75KR2J-GP DY
C NVI_EN#_R
Q 6102 DY
2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0N31
3rd = 084.27002.0L31
4th = 084.07002.0C31
A UX_EN_WOWL_R
W LAN_EN#
R 6103 75KR2J-GP DY

Remove R6118 20180803

3 D3V_WLAN
W LAN1
P ULSAR_38P4M_REFCLK
W IFI_RF_EN_R
B LUETOOTH_EN_R
P LTRST#_CPU
S USCLK_WLAN
S US_CLK
R 6117 33R2J-2-GP
20180907
C NV_BRI_DT_R
C NV_RGI_RSP_R
C NV_RGI_DT_R
C NV_RGI_RSP
R 6120 22R2J-2-GP
C NV_BRI_RSP
R 6123 22R2J-2-GP
C NV_BRI_RSP_R
B T_PCMOUT_CLKREQ0
B T_PCMFRM_RSTN
3 D3V_WLAN
R 6121 DY 71K5R2F-1-GP
R 6122 71K5R2F-1-GP
NP2
SKT-MINI67P-26-GP
062.10007.0511
2ND = 062.10003.0B11
NGFF_KEY_E_75P
NP1
C NV_WT_CLK_DP
C NV_WT_CLK_DN
C NV_WT_DP0
C NV_WT_DN0
C NV_WT_DP1
C NV_WT_DN1
J IO3_PCIE_WAKE#
C LK_PCIE_WLAN_REQ#
W LAN_CLK_CPU_N
W LAN_CLK_CPU_P
W LAN_PCIE_RX_N10
W LAN_PCIE_RX_P10
W LAN_PCIE_TX_CON_N
W LAN_PCIE_TX_CON_P
C 6107 SCD1U16V2KX-3DLGP
C 6108 SCD1U16V2KX-3DLGP
W LAN_PCIE_TX_N10
W LAN_PCIE_TX_P10
C NV_WR_CLK_DP
C NV_WR_CLK_DN
C NV_WR_DP0
C NV_WR_DN0
C NV_WR_DP1
C NV_WR_DN1
B T_USB20_CON_N
B T_USB20_CON_P
R 6105 0R0402-PAD-1-GP
L 6101 DY COIL-90OHM-100MHZ-2-GP
68.00396.001
check with RF
R 6104 0R0402-PAD-1-GP
B T_USB20_N
B T_USB20_P
20180822

3 D3V_WLAN
R 6114 10KR2J-3-GP
W IFI_RF_EN
R 6109 0R2J-L-GP BOLT-L
W IFI_RF_EN_R
20180903
3 D3V_WLAN
R 6115 10KR2J-3-GP
B LUETOOTH_EN
R 6108 0R2J-L-GP BOLT-L
B LUETOOTH_EN_R
20180903

BOLT L 14 EMMC

DELL Wistron Corporation
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Title: N GFF_WLAN CONN
Size: A 2
Document Number: BOLT WHL
Rev: 1
Date: Thursday, December 27, 2018
Sheet 61 of 105

Main Func = WWAN

19,24 WWAN_DB_DET#

Taos NC
24 INT#_ITE8010
24 CLK_ITE8010
24 DAT_ITE8010

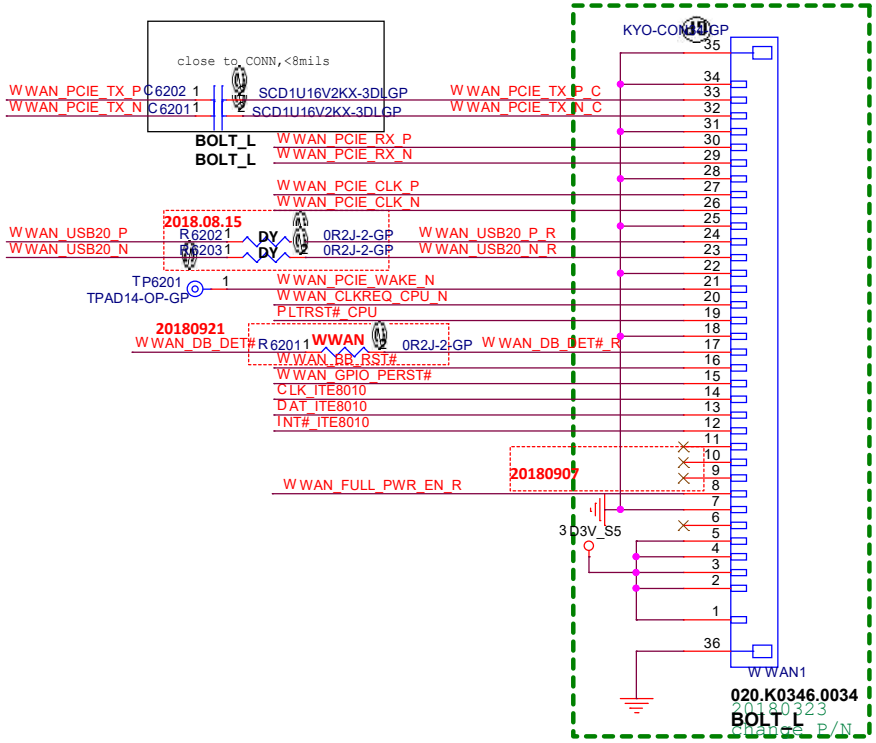
WWAN

16 WWAN_PCIE_RX_N
16 WWAN_PCIE_RX_P
16 WWAN_PCIE_TX_N
16 WWAN_PCIE_TX_P

18 WWAN_CLKREQ_CPU_N
18 WWAN_PCIE_CLK_P
18 WWAN_PCIE_CLK_N

16 WWAN_USB20_N
16 WWAN_USB20_P

17,26,31,61,63,91 PLTRST#_CPU



WWAN_BB_RST# 21

WWAN_FULL_PWR_EN_R 20

WWAN_GPIO_PERST# 20

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Title: **WWAN**

Size	Document Number	Rev
C ustom	BOLT WHL	1

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Main Func = M.2 SSD

M.2 PCIE/SATA FOR BOLT

16 sSD_PCIE_TX_P16
16 sSD_PCIE_TX_N16
16 sSD_PCIE_RX_N16
16 sSD_PCIE_RX_P16
16 sSD_PCIE_TX_P15
16 sSD_PCIE_TX_N15
16 sSD_PCIE_RX_P15
16 sSD_PCIE_RX_N15
16 sSD_PCIE_TX_P14
16 sSD_PCIE_TX_N14
16 sSD_PCIE_RX_P14
16 sSD_PCIE_RX_N14
16 sSD_PCIE_TX_P13
16 sSD_PCIE_TX_N13
16 sSD_PCIE_RX_P13
16 sSD_PCIE_RX_N13
18 sSD_CLK_CPU_P_4
18 sSD_CLK_CPU_N_4
18 cLK_PCIE_NVME_REQ#
26,31,61,62,91 sTRST# _CPU
16 sF_SSD_PEDET
16 sSD_DEVSLP_R
64 sF_PCIE_LED#
24 sSD_SCP#

SSD M.2 CONN

PCIE:1 SATA:0

20180801

ESD FOR ESD_R2 SKU, 千萬計得BOM要手動!

20180809

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	+3.3V	GND	75
72	+3.3V	GND	73
70	+3.3V	GND	71
68	SUS CLK(32kHz) (OPTIONAL)	PORT13/PCIe RX-/SSIC RX-/SATA RX-	69
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	PERST#	57
56	N/C	CLKREQ#	55
54	PEWAKE#/GPIO/SSIC RX+/SATA RX+	REFCLK-	53
52	CLKREQ#/GPIO/SSIC TX+/SATA TX+	REFCLK+	51
50	PERST#/GPIO/SSIC TX-/SATA TX-	GND	49
48	N/C	PETp0/SATA-A+	47
46	N/C	PETn0/SATA-A-	45
44	N/C	GND	43
42	N/C	PERp0/SATA-B-	41
40	N/C	PERn0/SATA-B+	39
38	DEVSLP (I2S)	GND	37
36	N/C	PETp1	35
34	N/C	PETn1	33
32	N/C	GND	31
30	N/C	PERp1	29
28	N/C	PERn1	27
26	N/C	GND	25
24	N/C	PETp2	23
22	N/C	PETn2	21
20	N/C	GND	19
18	3.3V	PERp2	17
16	3.3V	PERn2	15
14	3.3V	GND	13
12	3.3V	PETp3	11
10	DAS/DSS# (I/O)/LED# (OD)	PETn3	9
8	N/C	PERp3	7
6	3.3V	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

062.10003.00X1
2ND = 62.10043.J01

Table 13-11.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:
1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Main Func = eMMC

21 eMMC_D7
21 eMMC_D6
21 eMMC_D5
21 eMMC_D4
21 eMMC_D3
21 eMMC_D2
21 eMMC_D1
21 eMMC_D0

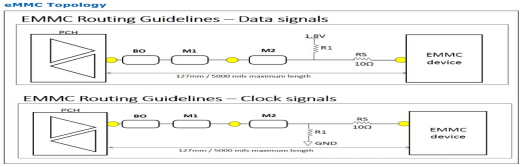
21 eMMC_CLK
21 eMMC_CMD

21 eMMC_RCLK
21 eMMC_RESET#

7.6.3 eMMC Topology Guidelines

External pull-up resistors of 20KΩ are required on the Data lines. A pull-down resistor of 20KΩ is recommended on the Clock and RCLK lines.

Figure 7-23. eMMC Topology



Layout note: R6370 close to CPU

20180508

6.2.1 Power supply: e•MMC

In the e•MMC, V_{CC} is used for the NAND flash device and its interface voltage; V_{CCQ} is for the controller and the MMC interface voltage shown in Figure 9. The core regulator is optional and only required when internal core logic voltage is regulated from V_{CCQ}. A C_{reg} capacitor must be connected to the Vdd terminal to stabilize regulator output on the system.

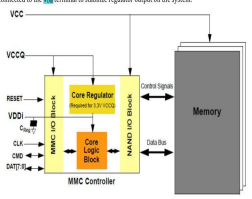


Figure 9 - e•MMC Internal Power Diagram

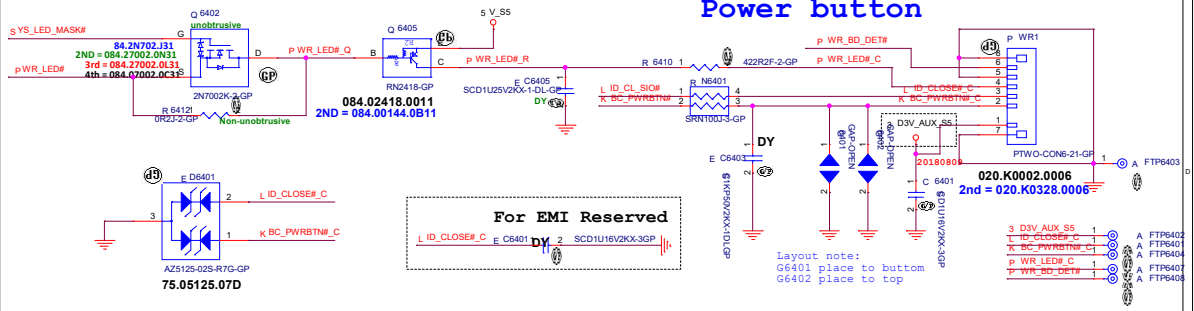
Title: m SATA
Size: A | Document Number: BOLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet: 63 | of: 100

Main Func = Power BTN

24 pWR_LED#
20,21 pWR_BD_DET#
24,92 LID_CL_SIO#
24,92 KBC_PWRBTN#

NONE FINGER PRINT 才會上件

Power button

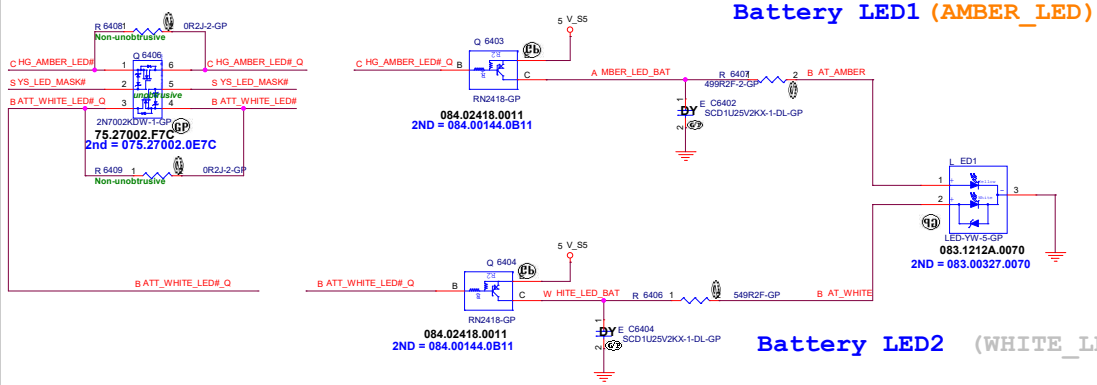


Main Func = Battery LED

Low actived from KBC GPIO

24,32 SYS_LED_MASK#
24 CHG_AMBER_LED#
24 BATT_WHITE_LED#

Battery LED1 (AMBER_LED)

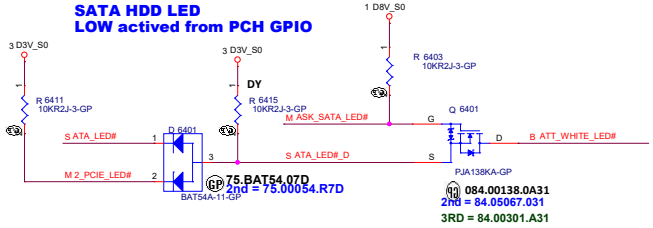


Battery LED2 (WHITE_LED)

Main Func = HDD LED

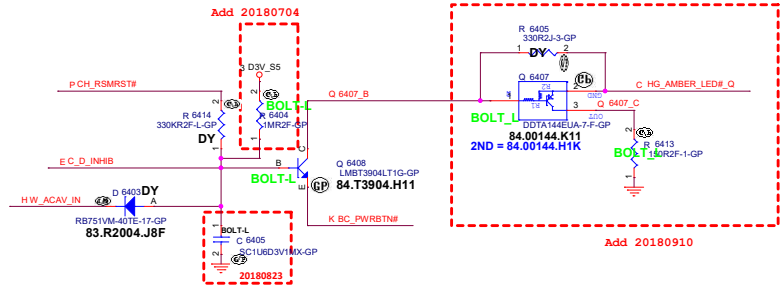
24 MASK_SATA_LED#
16 SATA_LED#
63 M2_PCIE_LED#

SATA HDD LED
LOW actived from PCH GPIO



Main Func = M-BIST

17,24 PCH_RSMRST#
24 EC_D_INHIB
24,43,44 HW_ACAV_IN



BOLT_L ONLY

<Core Design>

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2 1F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board&Power Button

Size	Document Number	Rev
C ustom	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 64 o f 105

Main Func = KB

24 CAP_LED#_R

24 KSI[0..7]

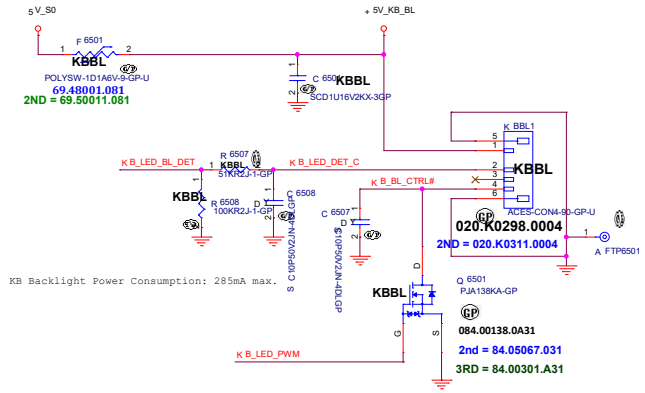
24 KSO[0..16]

20 KB_DET#

19 KB_LED_BL_DET

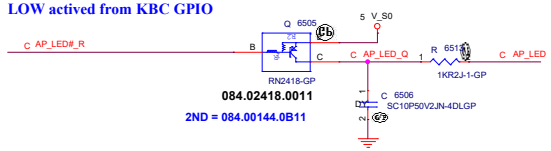
24 KB_LED_PWM

Keyboard Backlight (Reserved)

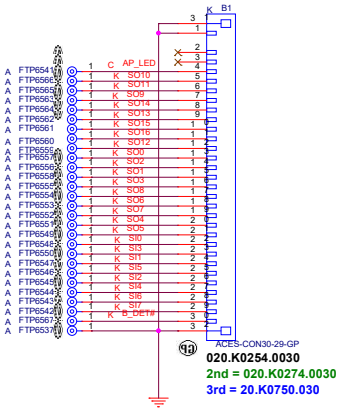


CAP LED Control

LOW actived from KBC GPIO



Internal Keyboard Connector



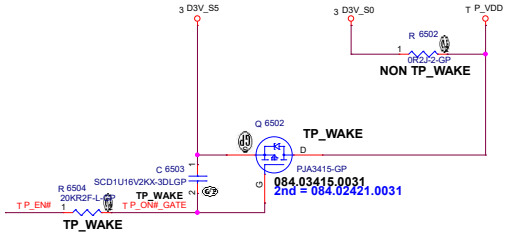
Main Func = TPAD

24 TP_EN#

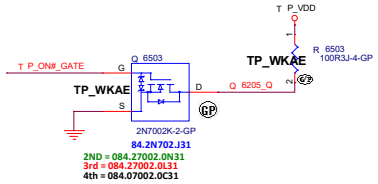
24 CLK_TP_SIO
24 DAT_TP_SIO

20,93 I2C0_SCL_TCH_PAD
20,93 I2C0_SDA_TCH_PAD

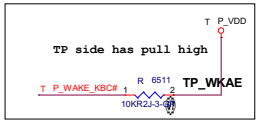
3,24 TP_WAKE_KBC#
24 PTP_DIS#



TP_VDD Discharge Circuit



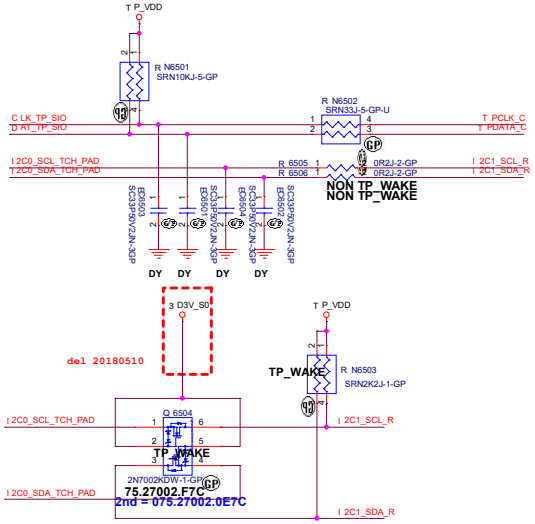
Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



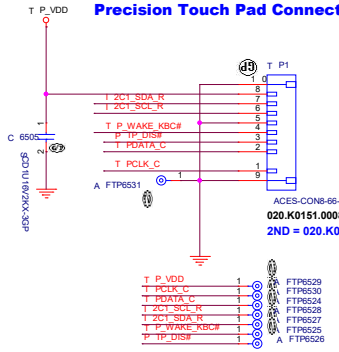
Support PTP

PS2

I2C



Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

BOLT L 14 EMMC

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Title: Key Board&Touch Pad

Size: A 2 | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 65 of 105

Main Func = IO Connector

USB 2.0

16 USB2_USB20_N
16 USB2_USB20_P

16 CARD1_USB20_N
16 CARD1_USB20_P

19 IO_DB_DET#_GPPG5
21 IO_DB_DET#
24,55 IO_DB_DET#_EC
20 SD_READ_MODE#

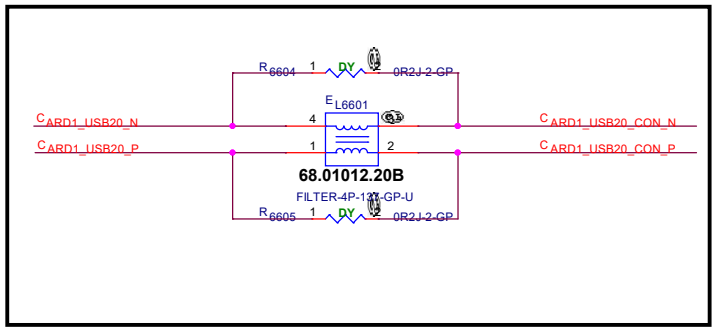
USB OC

16 USB_OC1#

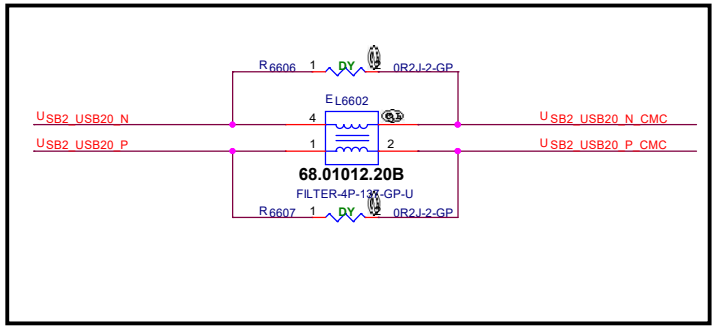
USB Switch Enable

24,35 USB_EN#

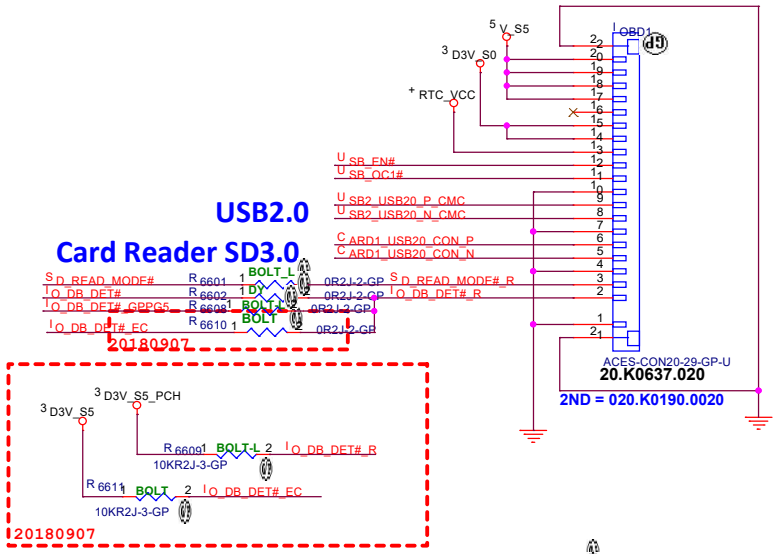
USB2.0 CARD

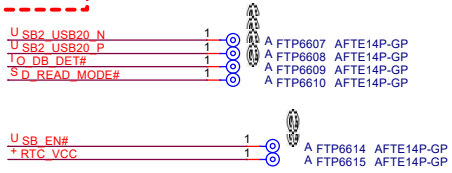


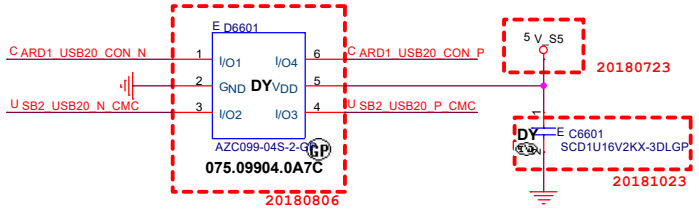
USB2.0



USB2.0 Card Reader SD3.0







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
Custom	BOLT WHL	1

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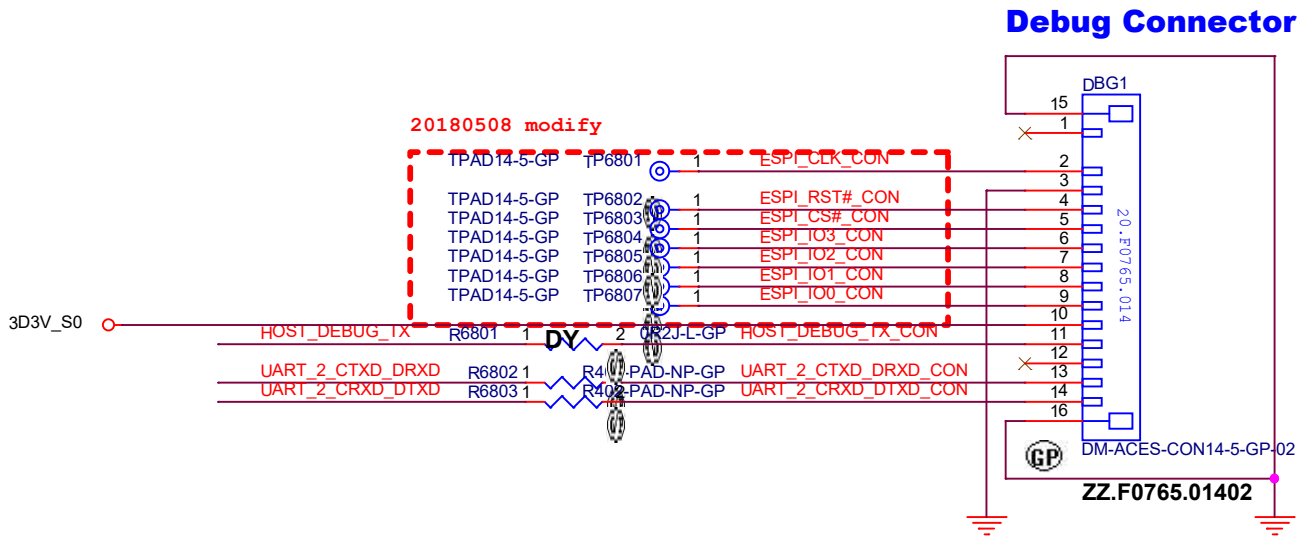
Main Func = Debug

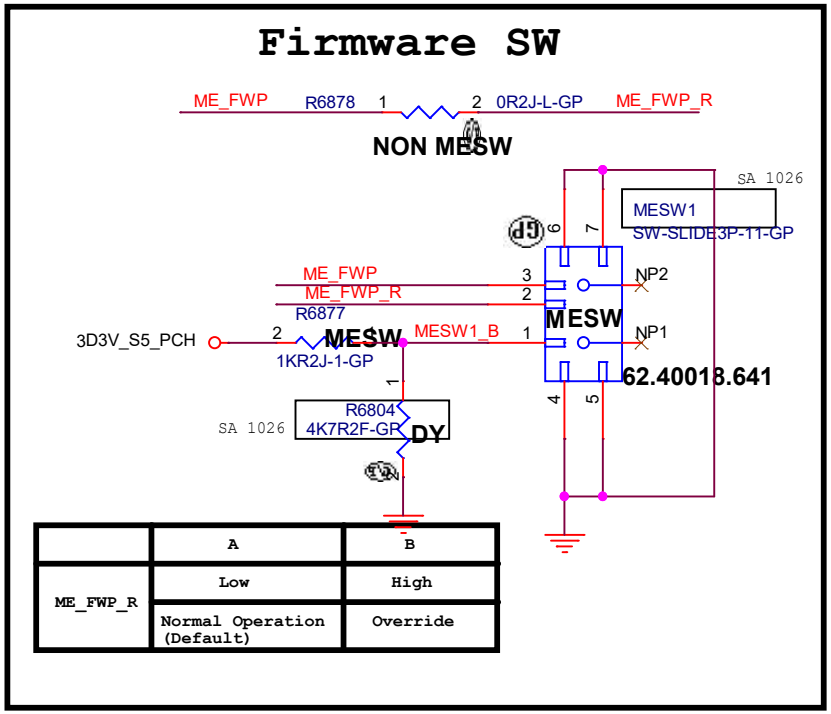
Debug Connector



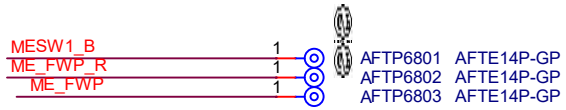
24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

24 ME_FWP
19 ME_FWP_R

Firmware SW



	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override



BOLT L 14 EMMC

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Title: Dubug connector

Size	Document Number	Rev
A4	BOLT WHL	1

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Main Func = Free Fall Sensor

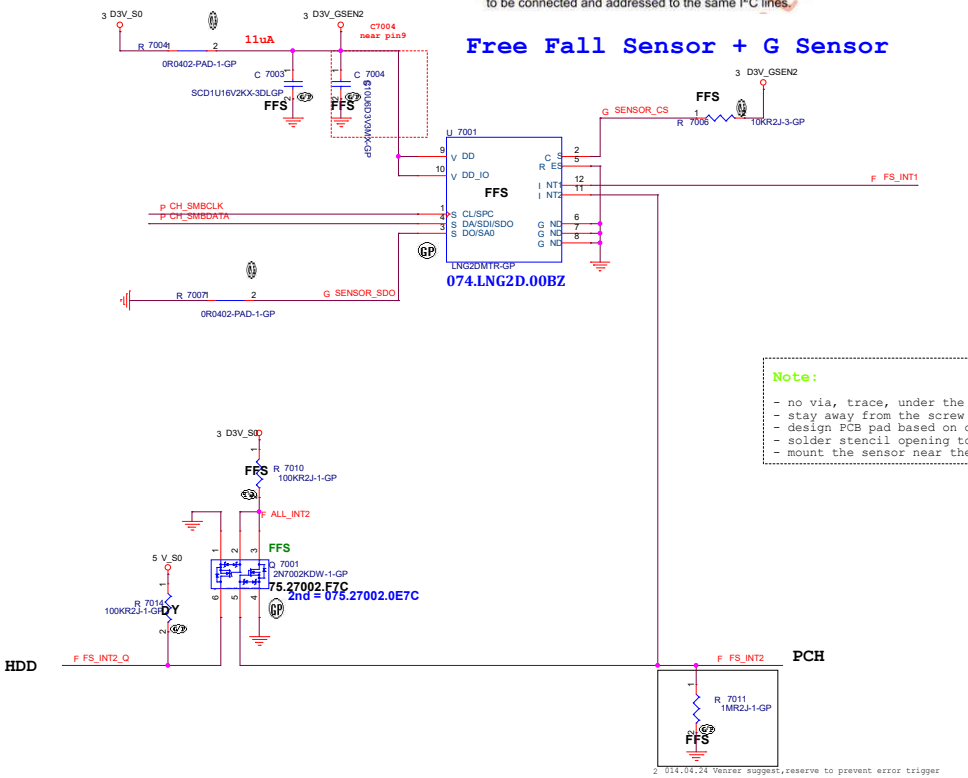
12,13,18,56 PCH_SMBDATA
12,13,18,56 PCH_SMBCLK

18 FFS_INT1
20 FFS_INT2

60 FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

2 014.04.24 Venrer suggest,reserve to prevent error trigger

BOLT L 14 EMMC

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Title: *(Reserved)*

Size	Document Number	Rev
A 2	BOLT WHL	1

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Main Func = TYPEC MUX

From USB HOST

From DP Demux

From CCG4

From CCG4 to MUX & DP Demux

To Type-C CONNECTOR

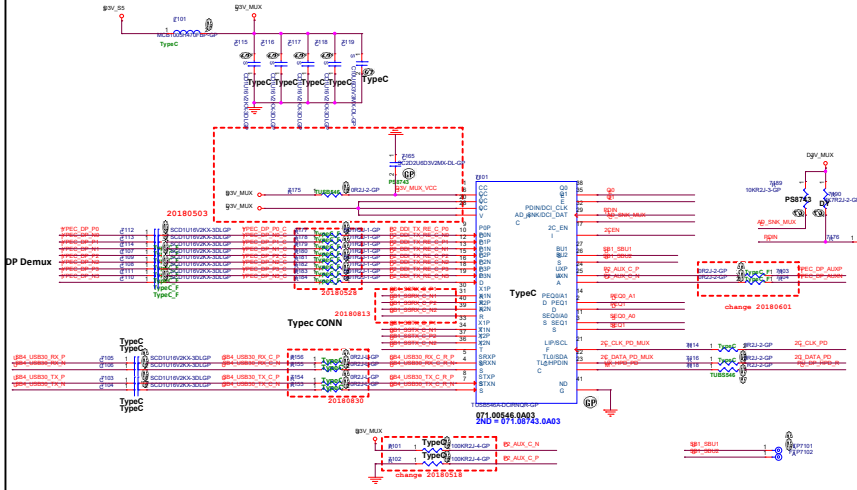
From EC

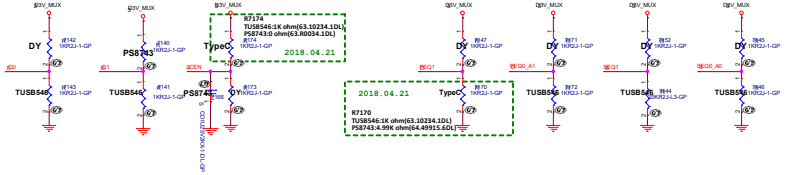
To Type-C CONNECTOR

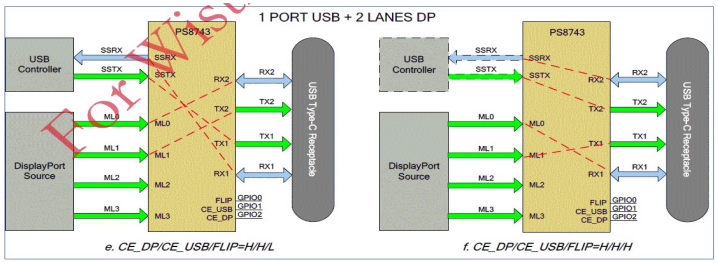
USB HOST

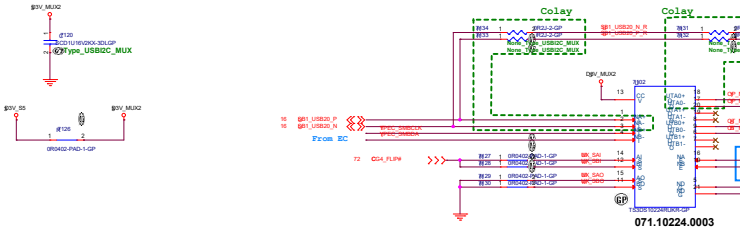
DP Demux

Typec CONN









FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

Table 1. FUNCTION TABLE

ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	–	–
10	–	–	Hi-Z	Hi-Z
11	–	–	–	–

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0010	INB	–	INB	–
1000	INA	–	INA	–
1010	INA	–	INB	–

071.10224.0003
Type_USBI2C_MUX
2ND = 071.33224.0003

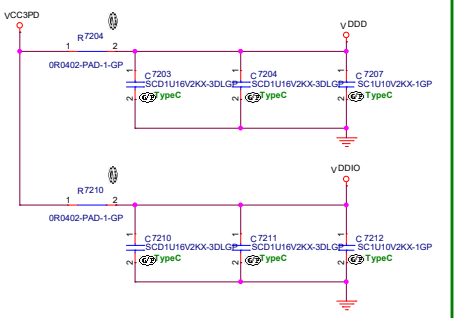
BOLT L 14 EMMC

W istron Corporation
R ESERVED

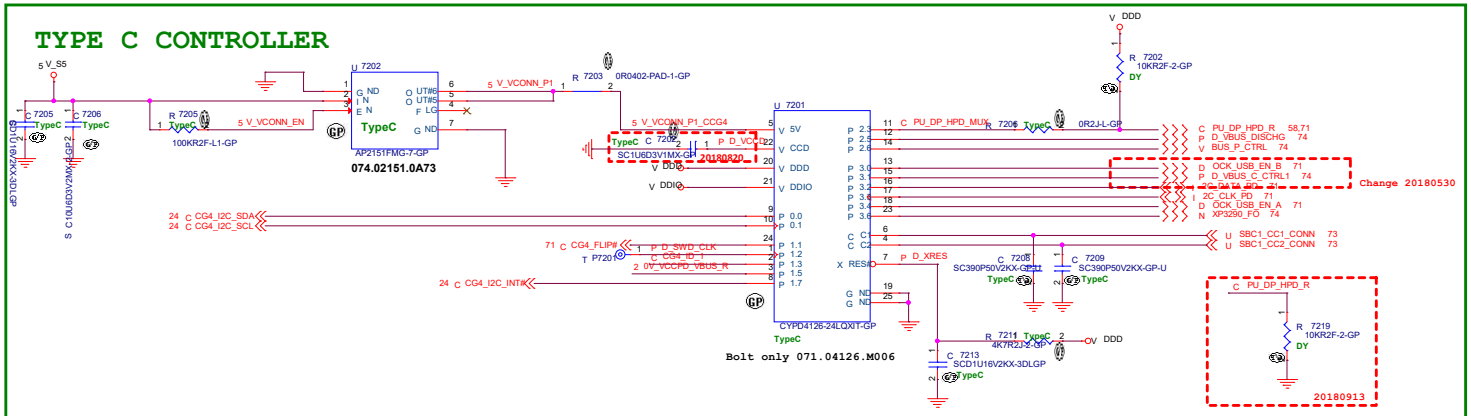
Title: BOLT WHL
Size: A3 | Document Number | Rev: 1
Date: Thursday, December 27, 2018 | Sheet 71 of 105

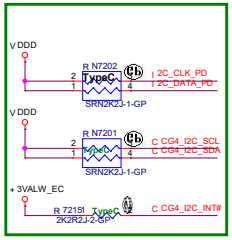
Main Func = TYPEC CONTROLLER

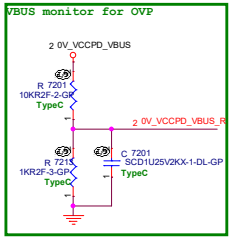
Power

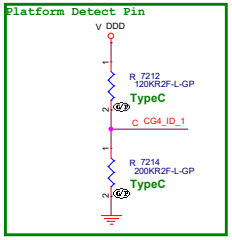


TYPE C CONTROLLER



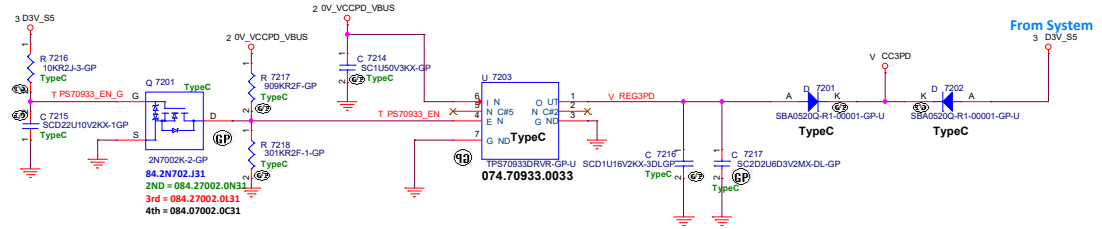






S.No	Project Name	ODM	CCG4_ID_1	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bolt (WHL) Data Only with PS8743B Mux	Wistron	L0	Single	USB	N/A	L0	0V
2	Bolt (WHL) Data Only with TUSB546 Mux	Wistron	L1	Single	USB	N/A	L1	3.3V/8
3	Bolt (CNL) Data Only with PS8743B Mux	Wistron	L2	Single	USB	N/A	L2	2*3.3V/8
4	Bolt (CNL) Data Only with TUSB546 Mux	Wistron	L3	Single	USB	N/A	L3	3*3.3V/8
5	Bolt (WHL) Full Feature with PS8743B Mux	Wistron	L4	Single	USB+DP+ PD Charging	N/A	L4	4*3.3V/8
6	Bolt (WHL) Full Feature with TUSB546 Mux	Wistron	L5	Single	USB+DP+ PD Charging	N/A	L5	5*3.3V/8
7	Bolt (CNL) Full Feature with PS8743B Mux	Wistron	L6	Single	USB+DP+ PD Charging	N/A	L6	6*3.3V/8
8	Bolt (CNL) Full Feature with TUSB546 Mux	Wistron	L7	Single	USB+DP+ PD Charging	N/A	L7	7*3.3V/8

For Dead Battery modify



	CCG4_ID_1	R7212	R7214	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.12035.6DL (120K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

<Core Design>

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Title: USB3.0 PORT

Size: C | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 72 of 105

Main Func = TYPEC CONNECTOR

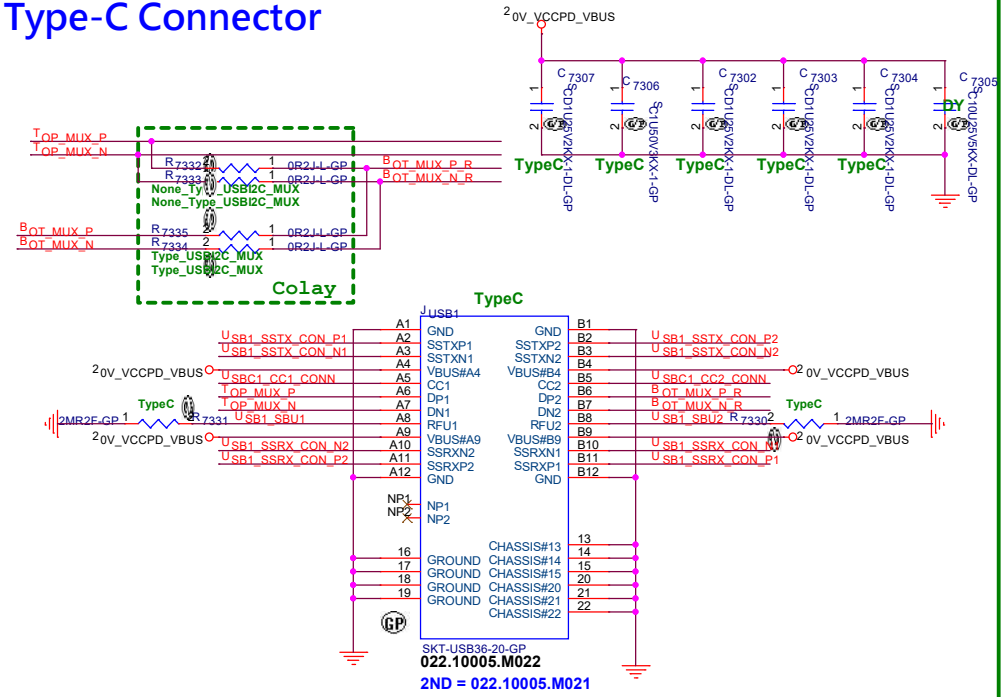
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2

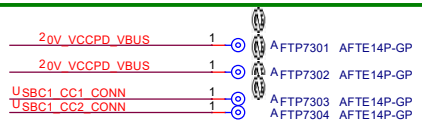
71 USB1_SBU1
71 USB1_SBU2
72 USBC1_CC1_CONN
72 USBC1_CC2_CONN

From USB2.0/ I2C Mux

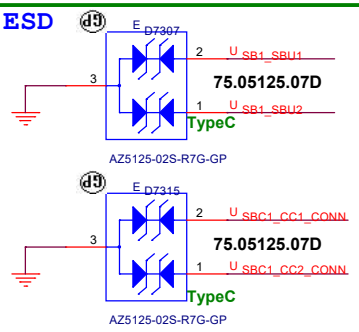
71 TOP_MUX_P
71 TOP_MUX_N
71 BOT_MUX_P
71 BOT_MUX_N

Type-C Connector

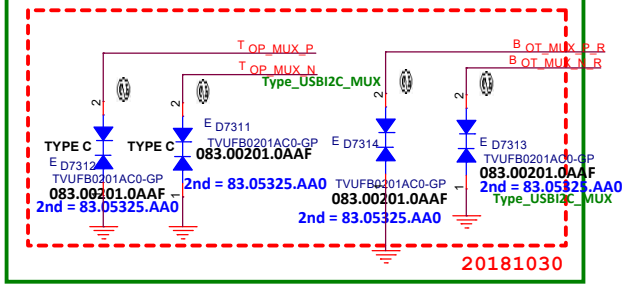




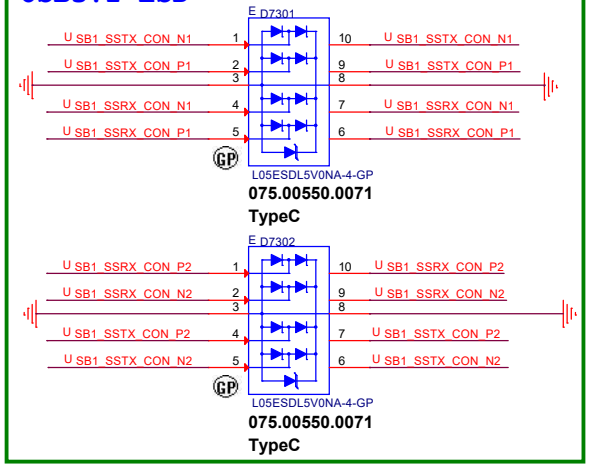
CC & SBU ESD



USB2.0 ESD



USB3.1 ESD



BOLT L 14 EMMC

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Title: TYPEC CONN

Size	Document Number	Rev
A 3	BOLT WHL	1

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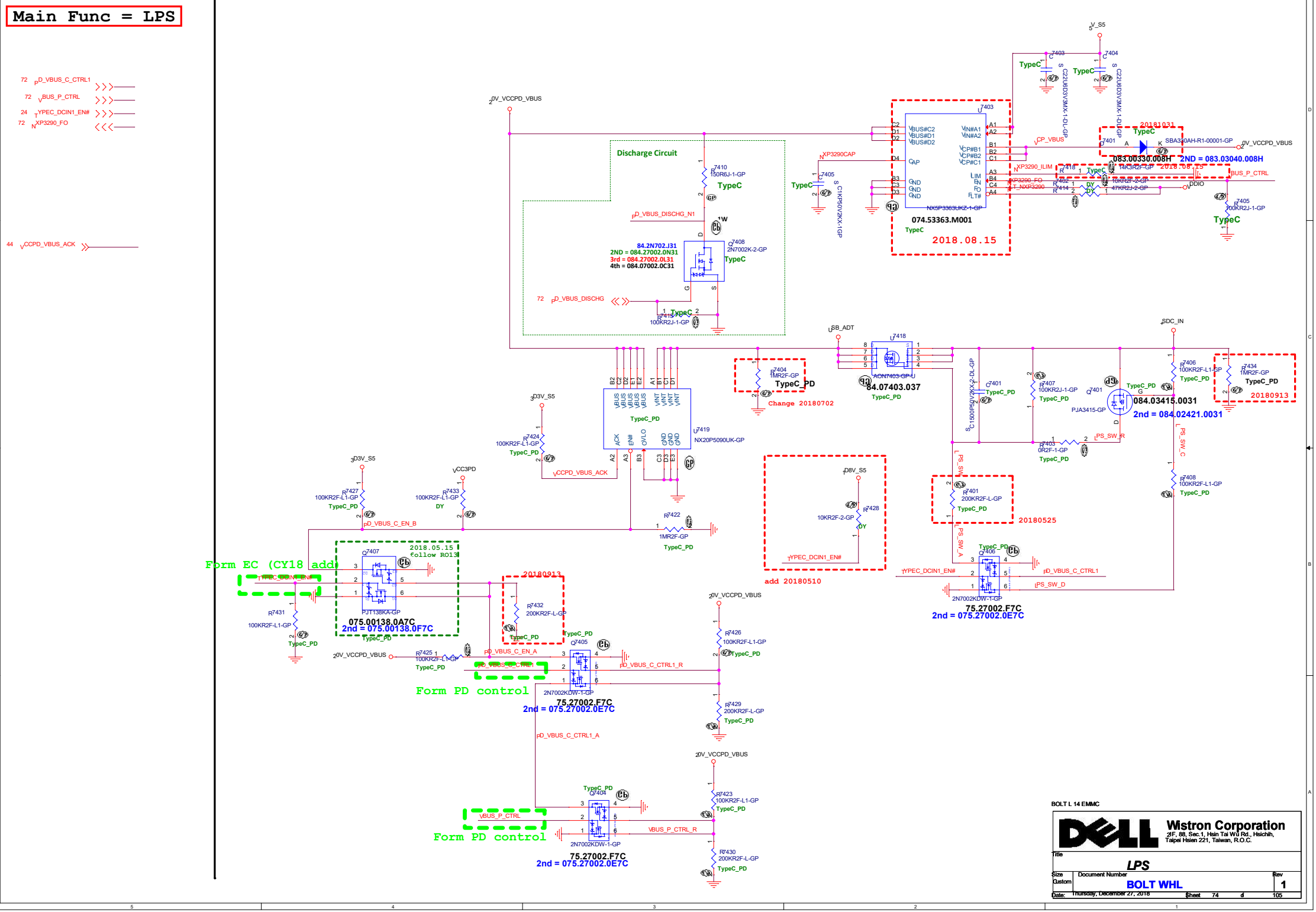
Main Func = LPS



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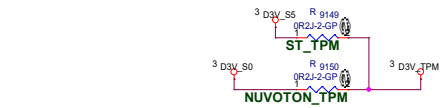
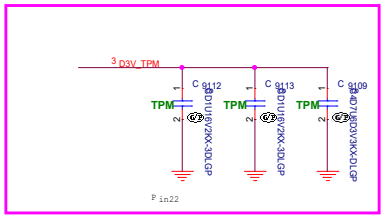
Title	LPS
Size: Custom	Document Number: BOLT WHL
Rev	1
Date: Thursday, December 27, 2018	Sheet 74 of 105

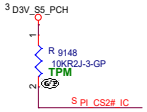
Main Func = TPM

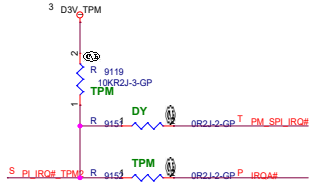
18,25 SPI_SO_CPU
18,25 SPI_CLK_CPU
15,18,25 SPI_SI_CPU
18 SPI_CS_CPU_N2

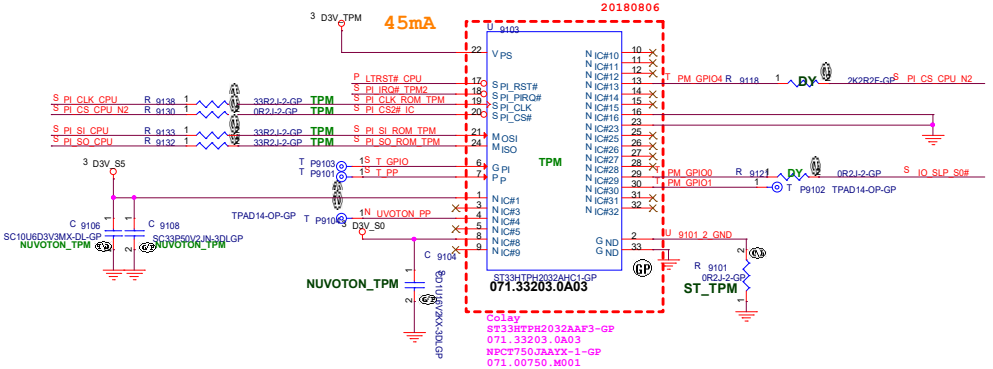
17,26,31,61,62,63 PLTRST#_CPU
17,40 SIO_SLP_S0#
20 PIRQA#
18 TPM_SPI_IRQ#











R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

BOLT L 14 EMMC

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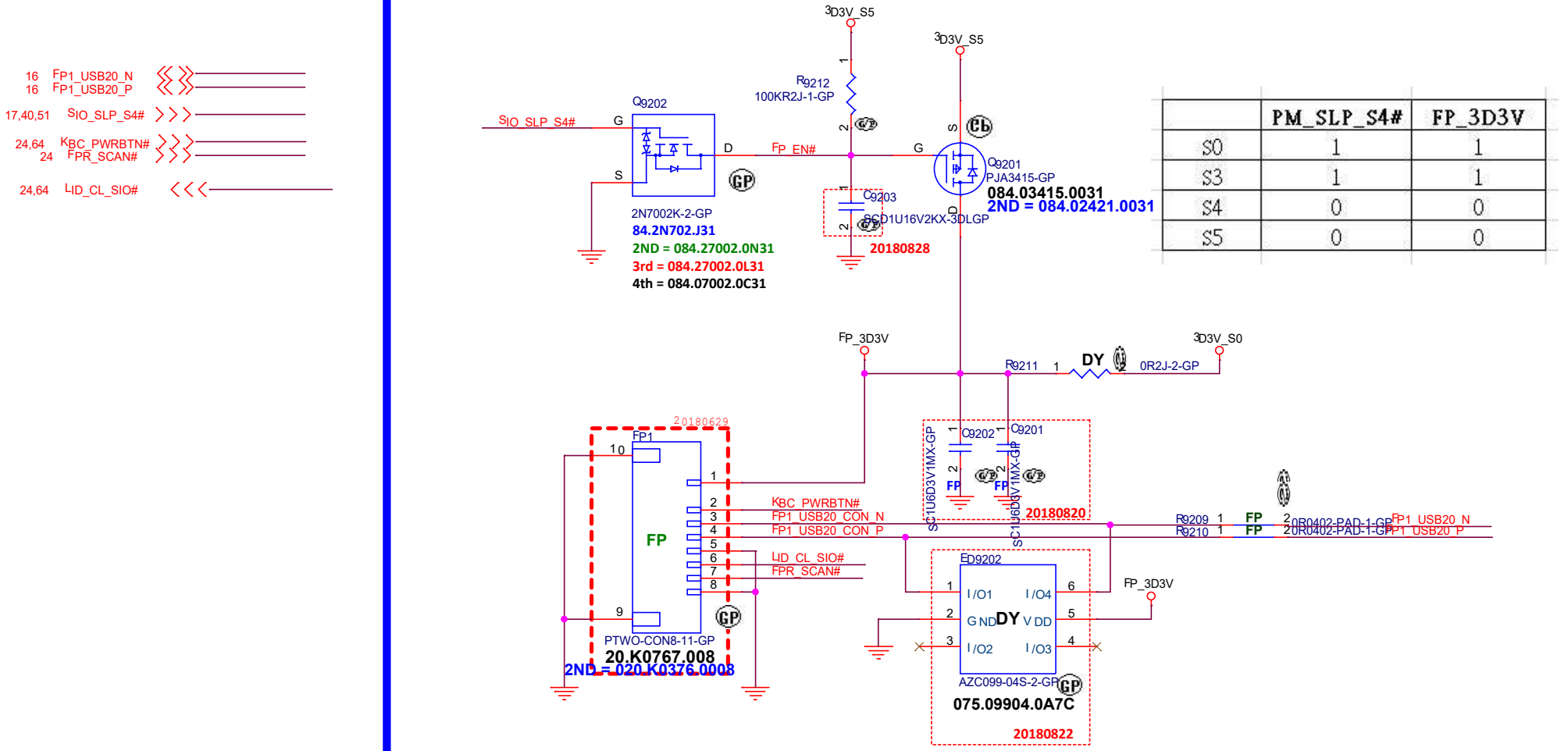
Title: TPM2.0

Size: C ustom | Document Number: BOLT WHL | Rev: 1

Date: Friday, December 28, 2018 | Sheet 91 of 105

Main Func = Finger Print

FBR(Botton side finger Print Sensor)



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

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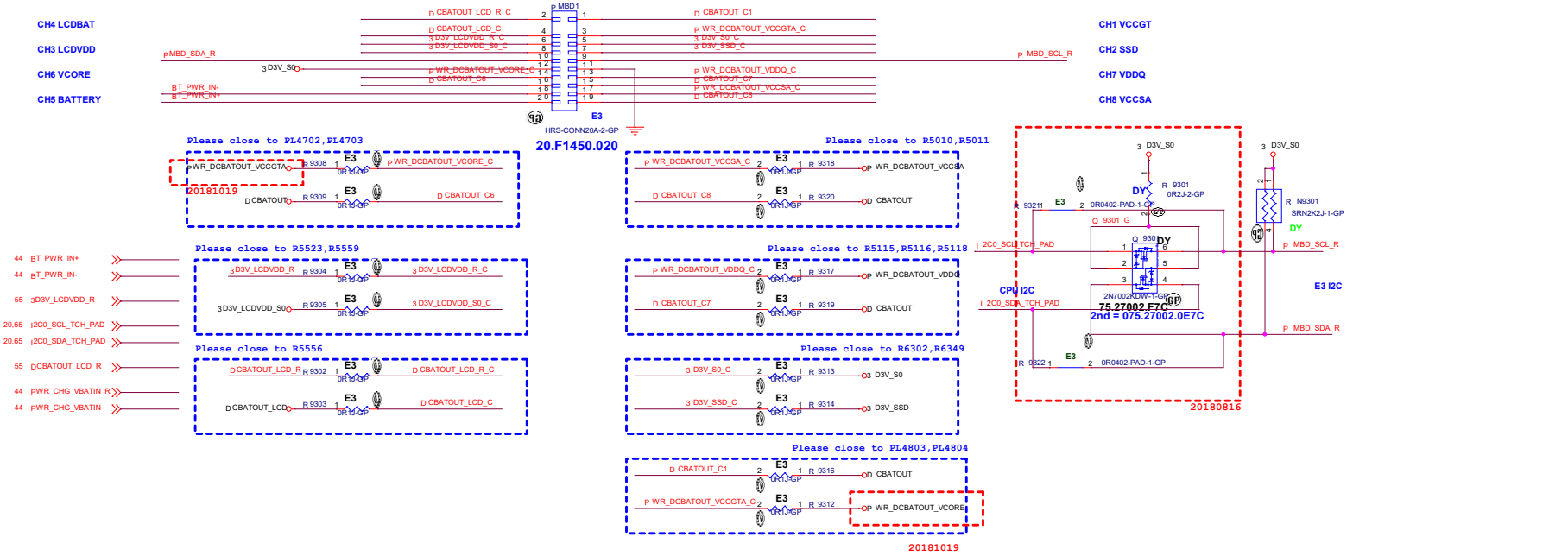
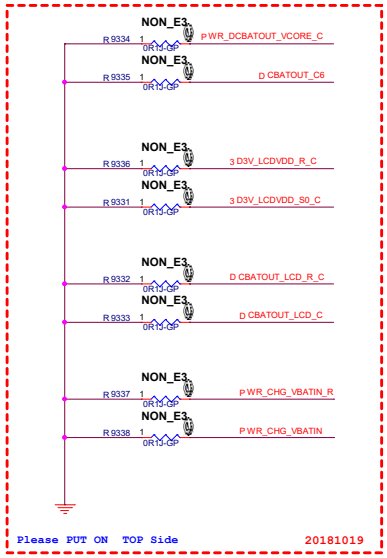
Title: *(Reserved)Finger Print*

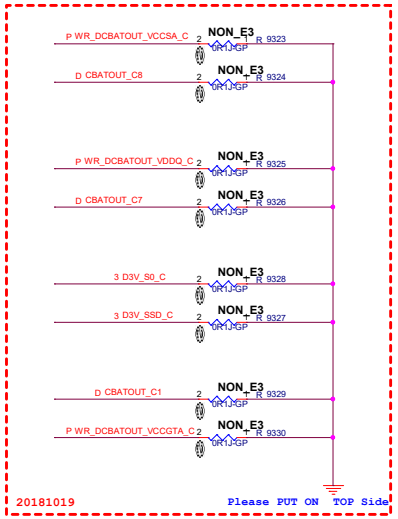
Size	Document Number	Rev
Custom	BOLT WHL	1

Date: Thursday, December 27, 2018 Sheet 92 of 105

Main Func = E3







	WHL
P1+/-	CPU_VCCGT (iGPU Core) <input>
P2+/-	STORAGE (SSD/HDD) <output>
P3+/-	DISPLAY_CTLR <output>
P4+/-	DISPLAY_BACKLIGHT <output>
P5+/-	SYSTEM (battery leads)
P6+/-	CPU_VCORE <input>
P7+/-	CPU_VDDQ (MCU Core) <input>
P8+/-	CPU_VCCSA (PCH Core) <input>

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

BOLT L 14 EMMC

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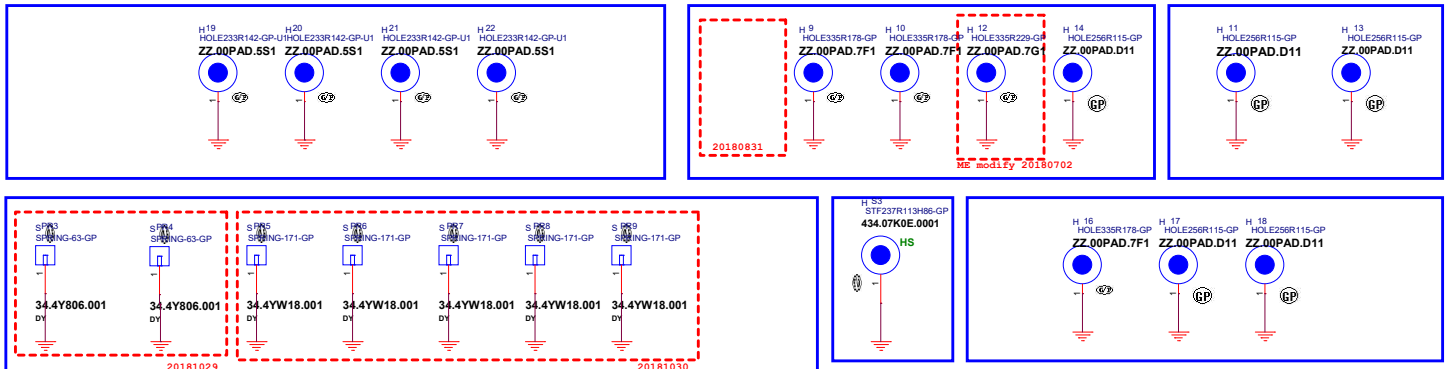
Title: E3

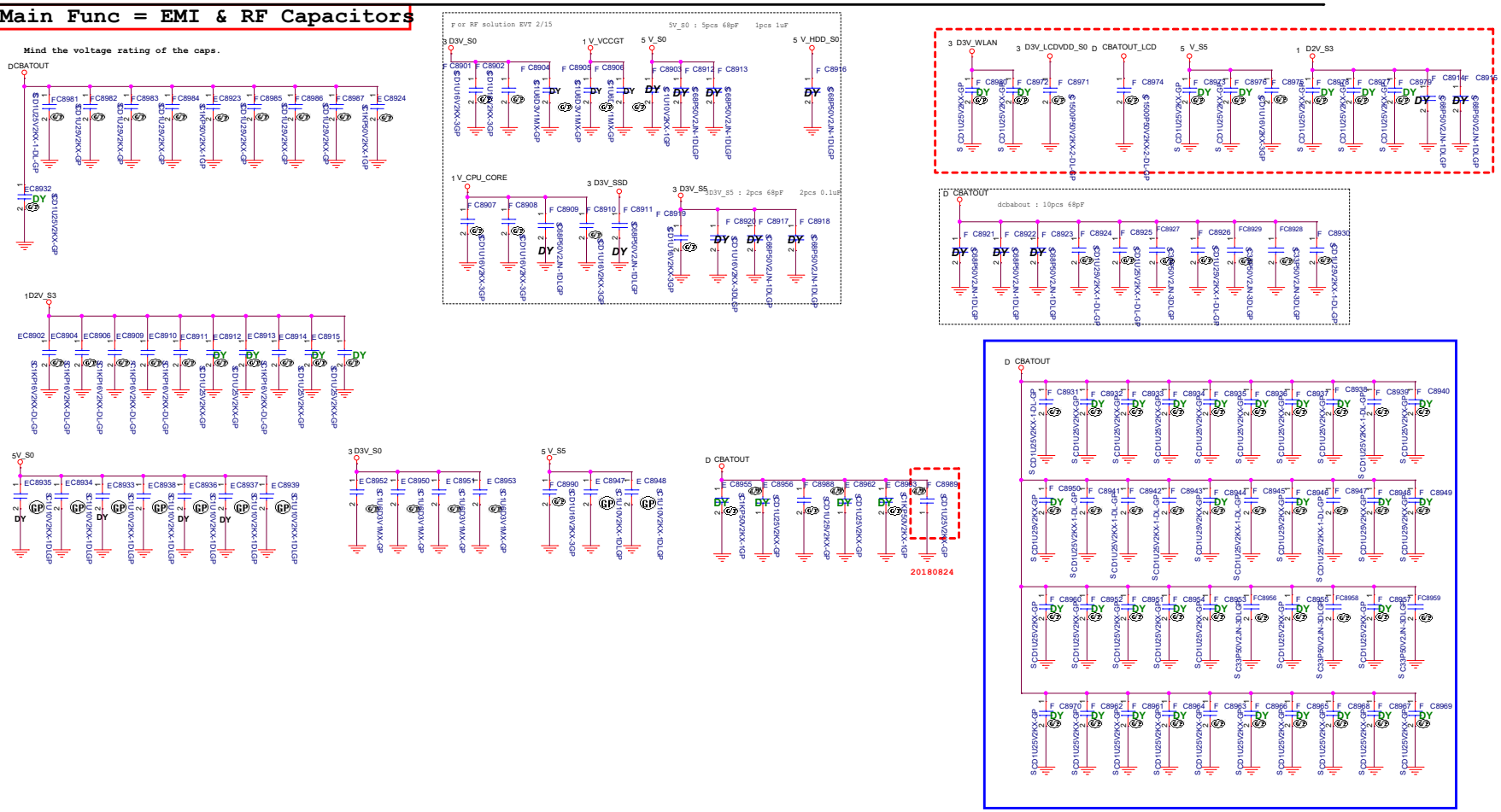
Size: A 2 | Document Number: BOLT WHL | Rev: 1

Date: Thursday, December 27, 2018 | Sheet 93 of 105

Main Func = UnusedParts



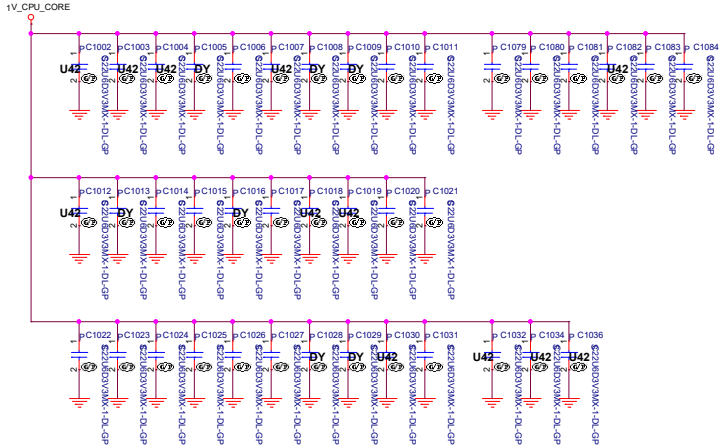
Main Func = EMI & RF Capacitors



Main FUNC = CPU

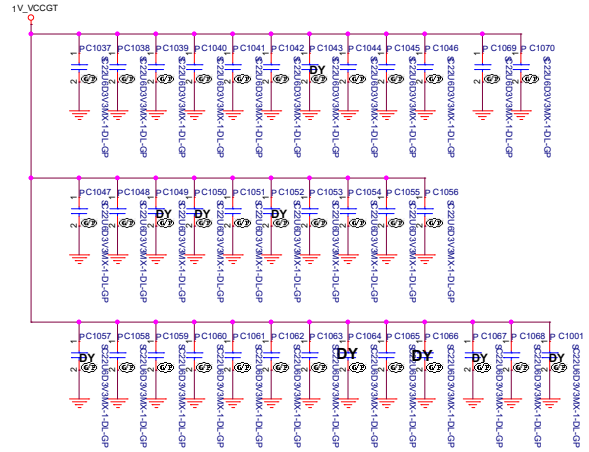
1V_CPU_CORE

22U 0603 x 39 (3DY)



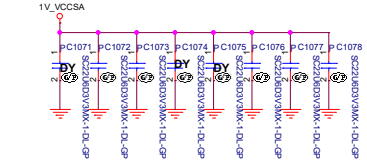
VCCGT

22U 0603 x 35 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)	Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

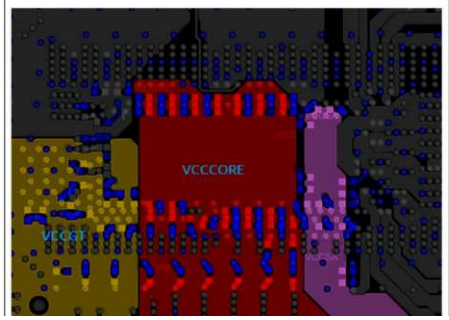
KBL-R U42 Decoupling Requirements (Sheet 1of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

KBL-R U42 Decoupling Requirements (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Diagram of placement for 0201 or 0402 backside caps for CPU decoupling.



BOLT L 14 EMMC

Wistron Corporation
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Title: CPU_(Power CAP1)
Size: A 2 | Document Number: BOLT WHL | Rev: 1
Date: Thursday, December 27, 2018 | Sheet 10 of 105

Main Func = PCH

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18

GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2

GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_R2 / HDA_SDO / I2S0_TXD / SPI1CS0_SDO

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

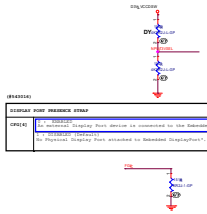
GPP_H21

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select.	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

GPP_R2 / CNV_RGI_DT / SPI1CS_TXD

PCH strap pin:

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

Change notes -

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BOLT L 14 EMMC

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