SYSTEM PAGE REF.

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031_KBC_KB,TP	
032_KBT_Reset Circuit	
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045_CRT_LCD Panel_CMOS_SMIC	
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057_ESD& Discharge	
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060_DC IN & BAT IN	
064_HD_HDD_SATA	
065_SCREW HOLE, ANT HOT	
066_DB_IO_USB*2 & CR & LED	
067_MB_LED	
068_B to B connector	
069_EMI	
070_VGA_NVIDIA_N16V/S_PCIE	
071_VGA_NVIDIA_N16V/S_FB-IF	
072_VGA_NVIDIA_N16V/S_FB-DDR3	
073_VGA_NVIDIA_N16V/S_VDD	
074_VGA_NVIDIA_N16V/S_DISPLAY	
075_VGA_NVIDIA_N16V/S_ROM,STRAL	
076_VGA_NVIDIA_N16V/S_GPIO	
077_VGA_NVIDIA_N16V/S_POWER	
080_PW_BMVP8 (1) (RT3601BCGQW)	
081_PW_BMVP8 (2) (RT3601BCGQW)	
083_PW_+1.0VSUS / +1.8VSUS	
084_PW_+1.2VSUS/+1.2V	
086_PW_1.35V/+0.675VS (UP5011Q)	
087_PW_+3VALDSW/+5VSUS (RT8249C)	
088_PW_LOAD SWITCH	
089 PW_CHARGER(BQ24780)	
090_PW_PROTECTION	
091_PW_DGPU_2PHASE(RT8815A)	

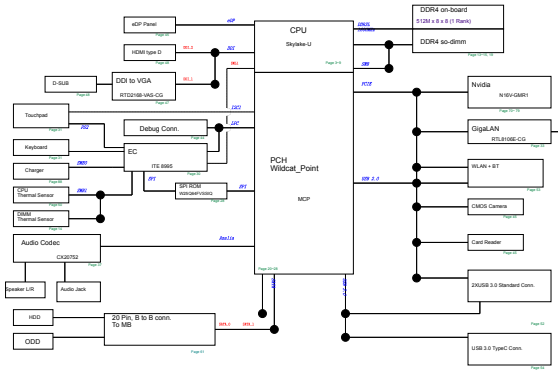
BLOCK DIAGRAM

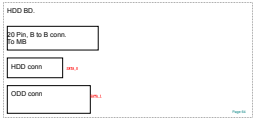
X441UBR SCHEMATIC Revision 2.1

(UA : UMA)

(UV : DGPU = Nvidia N16V-GMR1)

Non Connected Standby





CPU XDP	Discharge Circuit	DC & BATT. Conn.	PWM Fan
	Reset Circuit	Skew Holes	

Power

- +VCCGT +VCCSFR +VCCSA
- +1.0VSUS / +1.8VSUS
- +VCCPRIM_CORE
- +1.35V / +0.675VS
- +3VALDSW/+5VSUS
- Load Switch
- Charger
- +5VS/VDD

Title: Block Diagram

Size: A3 | Document Number: X441UBR | Rev: 2.1

Date: | Sheet: | Engineer: | ASUS

PCH_CPT GPIO

One on GPIO N/A
GPIO setting to GPIO low

PCH_DEG GPIO	Use As	Signal Name	Power on Default State	PCH Int Pull up/ down	Power
GPP_A0	Native	RCIN_N		PCH PU 10K	+3VS
GPP_A1	Native	LPC_AD0			+3VS
GPP_A2	Native	LPC_AD1		PCH PU 10K	+3VS
GPP_A3	Native	LPC_AD2		PCH PU 10K	+3VS
GPP_A4	Native	LPC_AD3			+3VS
GPP_A5	Native	LPC_FRAME#		PCH PU 10K	+3VS
GPP_A6	Native	SMI_ME#(N)		PCH PU 10K	+3VS
GPP_A7	GPI	N/A			
GPP_A8	Native	PM_CLKRUN#		PCH PU10K	+3V3
GPP_A9	Native	CLK_PCI(PCI_PCH			+3VS
GPP_A10	Native	CLK_48M(N)			+3VS
GPP_A11	GPO	N/A			
GPP_A12	GPO	N/A			
GPP_A13	Native	PCH_SUS_STAT#		PCH PU 10K	+3VDUS
GPP_A14	Native	PCH_SUS_STAT#2		PCH PU 10K	
GPP_A15	Native	PCH_SUSACK#			
GPP_A16	GPO	N/A			
GPP_A17	GPO	N/A			
GPP_A18	GPO	N/A			
GPP_A19	GPO	N/A			
GPP_A20	GPO	N/A			
GPP_A21	GPO	N/A			
GPP_A22	GPO	N/A			
GPP_A23	GPO	N/A			
GPP_B0	GPO	N/A (SUSWARN_N(SX))		PCH PU 10K	+3VS
GPP_B1	GPO	N/A (SUSPWRDN_N(SX))		PCH PU 10K	+3VS
GPP_B2	GPO	N/A			
GPP_B3	GPO	N/A			
GPP_B4	GPO	N/A			
GPP_B5	Native	SB_SPKR_PCH	100K PU +3VS	PCH PU 10K	+3VS
GPP_B6	GPO	N/A			
GPP_B7	GPO	N/A			
GPP_B8	GPO	N/A			
GPP_B9	Native	CLKREQ_PCIE#4	10K PU +3VS	PCH PU 10K	+3VS
GPP_B10	Native	CLKREQ_WLAN#0	WLAN Card	PCH PU 10K	+3VS
GPP_B11	Native	EXP2 PWRGD (X/O)		PCH PU 10K	+3VDUS
GPP_B12	Native	PCH_SLP_S3#			
GPP_B13	Native	PLT_RST#			
GPP_B14	GPO	N/A			
GPP_B15	GPO	N/A			
GPP_B16	GPO	N/A			
GPP_B17	GPO	N/A			
GPP_B18	GPO	N/A			
GPP_B19	GPO	N/A			
GPP_B20	GPO	SW_USB_PCH			+3VS
GPP_B21	GPO	USB_OC#2#3	USB OC 2,3 for rear USB		+5VS
GPP_B22	GPO	GPIO_PM_SLEEP_LED(O)	USB OC 0,1 for rear USB		+5VS
GPP_B23	GPO	GPIO PWR_EN#	USB OC 4,5 for rear USB		
GPP_C0	Native	SMB_CLK(PCH)		PCH PU 2.2K	+3VDUS
GPP_C1	Native	SMB_DATA		PCH PU 2.2K	+3VS
GPP_C2	GPO	N/A			
GPP_C3	GPO	N/A			
GPP_C4	GPO	N/A			
GPP_C5	GPO	N/A			
GPP_C6	GPO	N/A			
GPP_C7	GPO	N/A			
GPP_C8	GPO	N/A			+3VS
GPP_C9	GPO	N/A			
GPP_C10	GPO	N/A			
GPP_C11	GPO	N/A			
GPP_C12	GPI	SIM1_HS#0		PCH PU/PD 10K	+3VDUS
GPP_C13	GPI	SIM2_HS#1		PCH PU/PD 10K	+3VDUS
GPP_C14	GPI	SIM3_HS#2		PCH PU/PD 10K	+3VDUS
GPP_C15	GPO	N/A			
GPP_C16	GPO	N/A			
GPP_C17	GPO	N/A			
GPP_C18	GPO	N/A			
GPP_C19	GPO	N/A			
GPP_C20	GPI	UART_CTS#		PCH PU 10K	+3VS
GPP_C21	GPO	UART_RTS#		PCH PU 10K	+3VS
GPP_C22	GPO	GPIO PWR_EN#		PCH PU 10K	+3VS
GPP_C23	GPI	*Touch _int#		PCH PU 10K	+3VS
GPP_D0	GPO	N/A			
GPP_D1	GPO	N/A			
GPP_D2	GPO	N/A			
GPP_D3	GPO	N/A			
GPP_D4	GPO	N/A			
GPP_D5	GPO	N/A			
GPP_D6	GPO	USB_OC#0#1		PCH PU 10K	+3VS
GPP_D7	GPO	USB_USE_EN#2		PCH PU 10K	+3VS
GPP_D8	GPO	N/A			
GPP_D9	GPO	N/A			
GPP_D10	GPO	N/A			
GPP_D11	GPO	N/A			
GPP_D12	GPO	N/A			
GPP_D13	GPO	N/A			
GPP_D14	GPO	N/A			
GPP_D15	GPO	N/A			
GPP_D16	GPO	N/A			
GPP_D17	GPO	N/A			
GPP_D18	GPO	N/A			
GPP_D19	GPO	N/A			
GPP_D20	GPO	N/A			
GPP_D21	GPO	N/A			
GPP_D22	GPO	N/A			
GPP_D23	GPO	N/A			

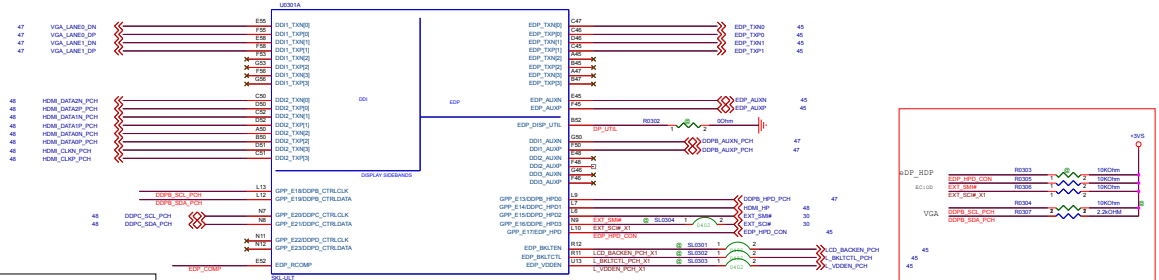
PCH_DEG GPIO	Use As	Signal Name	Power on Default State	PCH Int Pull up/ down	Power
GPP_E0	GPO	N/A			
GPP_E1	GPO	*Touch_panel_sel(PCH_GP		PCH PU 10K	+3VS
GPP_E2	GPI	touch_int(Touch_IN N/A		PCH PU 10K	+3VS
GPP_E3	GPO	N/A			+3VS
GPP_E4	GPO	N/A			
GPP_E5	GPO	N/A			
GPP_E6	GPO	N/A			
GPP_E7	GPO	N/A			
GPP_E8	GPO	N/A			
GPP_E9	GPO	N/A			
GPP_E10	GPO	N/A			
GPP_E11	GPO	N/A			
GPP_E12	GPO	N/A			
GPP_E13	GPO	N/A			
GPP_E14	GPO	N/A			
GPP_E15	GPO	N/A			
GPP_E16	GPO	N/A			
GPP_E17	GPO	N/A			
GPP_E18	GPO	N/A			
GPP_E19	GPO	N/A			
GPP_E20	GPO	N/A			
GPP_E21	GPO	N/A			
GPP_E22	GPO	N/A			
GPP_E23	GPO	N/A			
GPP_F0	GPO	N/A			
GPP_F1	GPO	N/A			
GPP_F2	GPO	N/A			
GPP_F3	GPO	N/A			
GPP_F4	GPO	N/A			
GPP_F5	GPO	N/A			
GPP_F6	GPO	N/A			
GPP_F7	GPO	N/A			
GPP_F8	GPO	N/A			
GPP_F9	GPO	N/A			
GPP_F10	GPO	N/A			
GPP_F11	GPO	N/A			
GPP_F12	GPO	N/A			
GPP_F13	GPO	N/A			
GPP_F14	GPO	N/A			
GPP_F15	GPO	N/A			
GPP_F16	GPO	N/A			
GPP_F17	GPO	N/A			
GPP_F18	GPO	N/A			
GPP_F19	GPO	N/A			
GPP_F20	GPO	N/A			
GPP_F21	GPO	N/A			
GPP_F22	GPO	N/A			
GPP_F23	GPO	N/A			
GPP_G0	GPO	N/A (SMB_MB)			
GPP_G1	GPO	N/A (SMB_DQ)			
GPP_G2	GPO	N/A (SMB_CK)			
GPP_G3	GPO	N/A (SMB_DQ)			
GPP_G4	GPO	N/A (SMB_CK)			
GPP_G5	GPO	N/A (SMB_DQ)			
GPP_G6	GPO	N/A (SMB_CK)			
GPP_G7	GPO	N/A (SMB_DQ)			
GPP_H0	GPO	N/A (SMB_CK)			
GPP_H1	GPO	N/A (SMB_DQ)			
GPP_H2	Native	SM_INTRUDER#		PCH PU 10K	+3VS_SUS
GPP_H3	Native	SM_BC_PRESENT		PCH PU 10K	+3VS_SUS
GPP_H4	GPI	SMB_CPU(S)		PCH PU 10K	+3VS_SUS
GPP_H5	Native	SM_SPKR#		PCH PU 10K	+3VS_SUS
GPP_H6	Native	SM_PWRBTN#		PCH PU 10K	+3VS_SUS
GPP_H7	Native	SMB_ALERT#		PCH PU 10K	+3VS_SUS
GPP_H8	Native	SML0_CLK		PCH PU 10K	+3VS_SUS
GPP_H9	Native	SML0_DAT		PCH PU 10K	+3VS_SUS
GPP_H10	Native	SML1_CLK		PCH PU 10K	+3VS_SUS
GPP_H11	Native	SML1_DAT		PCH PU 10K	+3VS_SUS
GPP_H12	GPO	N/A			
GPP_H13	GPO	N/A			
GPP_H14	GPO	N/A			
GPP_H15	GPO	N/A			
GPP_H16	GPO	N/A			
GPP_H17	GPO	N/A			
GPP_H18	GPO	N/A			
GPP_H19	GPO	N/A			
GPP_H20	GPO	N/A			
GPP_H21	GPO	N/A			
GPP_H22	GPO	N/A			
GPP_H23	GPO	N/A			

Main Board

Display Port

A	EDP
B	VGA
C	HDMI

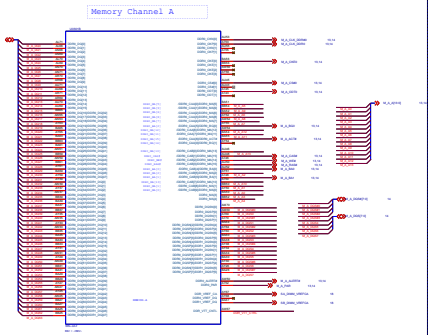
Intel Version	ASUS P/N

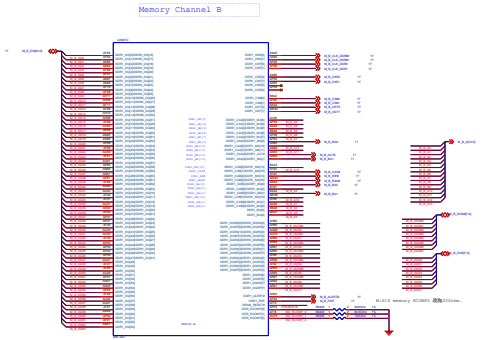


PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC
DDI0 port A

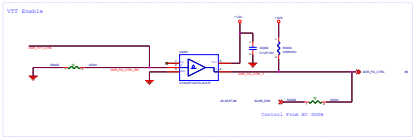
BOM

ASUS	Project Name: X441UBR	Rev: R2.1
Title : CPU_DISPBA		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: SZ/EE	
Date: Friday, April 27, 2018	Sheet 3 of 102	



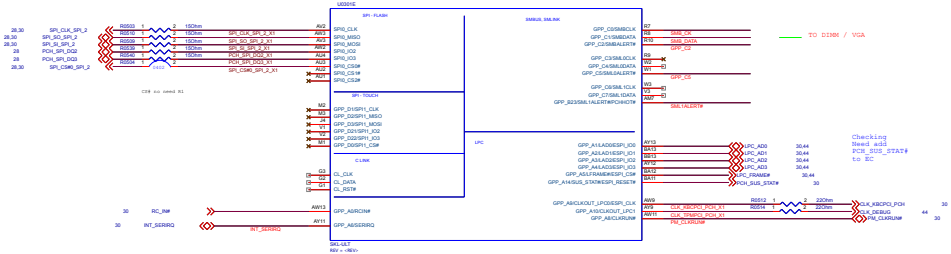


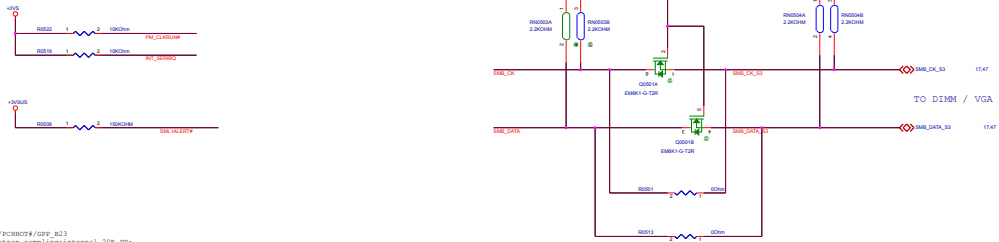
DDR_VTT_CTRL:
Control Memory Power Gate Control
Disable the ptx_vtrm memory VTT regulator
in C8 snd deeper and S3.
Ref:546504_546824_Skylake_63A_Vol_1_Rev0.9.pdf P.120



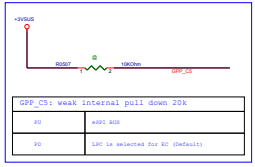
ASUS	Project Name: X441UBBK		Rev: 0.1
Title:	CPU_DDR4		
Size: A3	Page:	Engineer: SEAN	
Date: Friday, June 07, 2019		Sheet 4 of 46	

Main Board

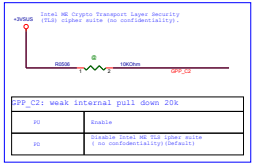




SML1ALERT# /PCHHOT#/GPP_B23
LOW during strap sampling:internal 20K PD;
When used as PCHHOT#, a 150k weak board
pull-up is recommended ;



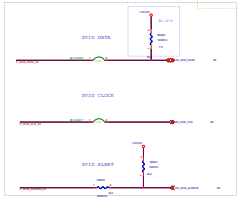
GPP_C5: weak internal pull down 20k	
PU	eSPI BOS
PD	LPC is selected for EC (Default)

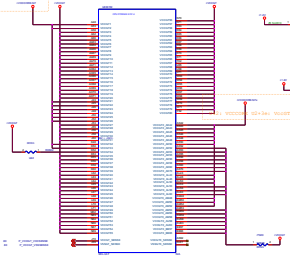


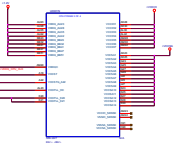
GPP_C2: weak internal pull down 20k	
PU	Enable
PD	Disable Intel ME TLS cipher suite (no confidentiality)(Default)

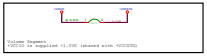
BOM

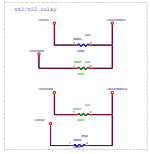
ASUS	Project Name: X441UBR	Rev: R2.1
Title :	CPU_LPC,SPI,SMB,CLINK	
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: SZ/EE
Date: Friday, April 27, 2018	Sheet: 5 of: 102	

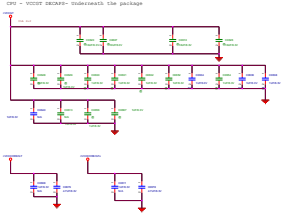


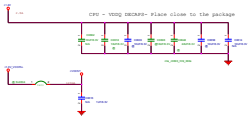


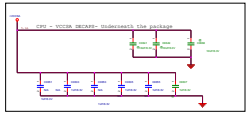




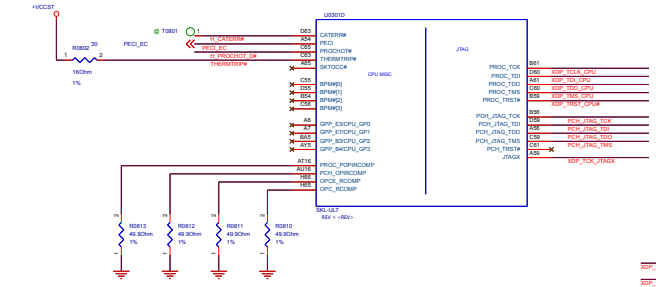


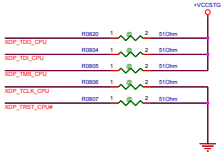


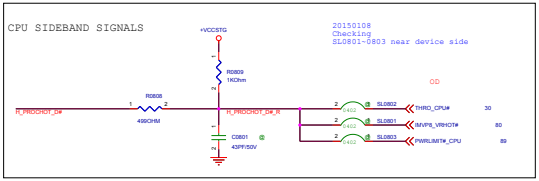




Main Board



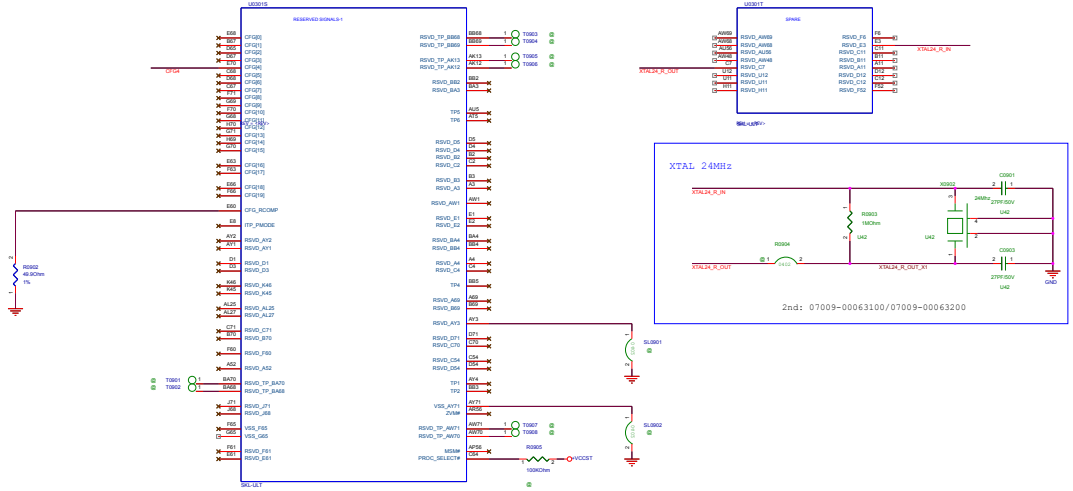


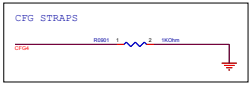


BOM

ASUS	Project Name: X441UBR	Rev: R2.1
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: SZ/EE
Date: Friday, April 27, 2018	Sheet: 8 of 102	

Main Board



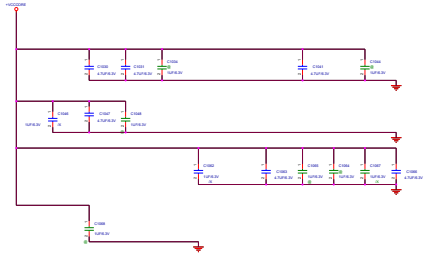


	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

BOM

ASUS	Project Name: X441UBR	Rev: R2.1
Title :	CPU_CFG,RSVD	
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: SZ/EE
Date: Friday, April 27, 2018	Sheet 9 of 102	

CPU - VCC DECAPS- Underneath the package



Disable: C1034, C1044, C1046, C1048, C1042, C1044, C1065, C1067
Del:0402,4.7uF: C1035, C1031, C1041, C1047, C1053, C1058

CPU - VCC DECAPS- Place close to the package

CAP above 22UF move to PWR page

Add option check 0K

ASUS	Project Name: X441UBR			Rev: X01
Title: CPU_POWER_CAP				
Size: D	Dept: MOBILITY COMPUTER SBU	Engineer: SJ EE		
Date: Friday, April 27, 2018		Sheet 15	of 102	

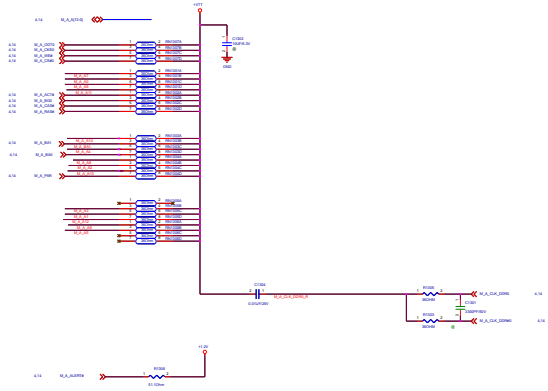
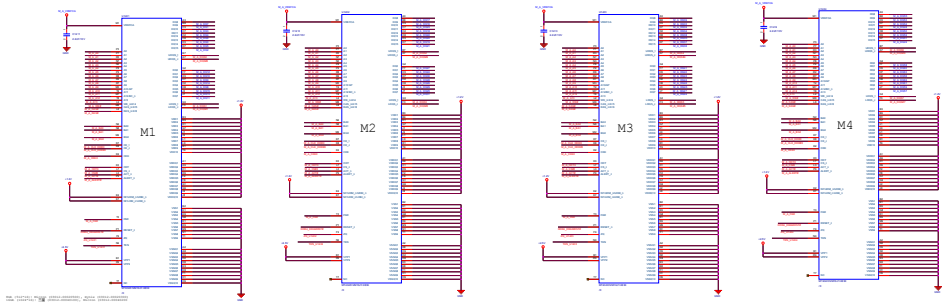


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

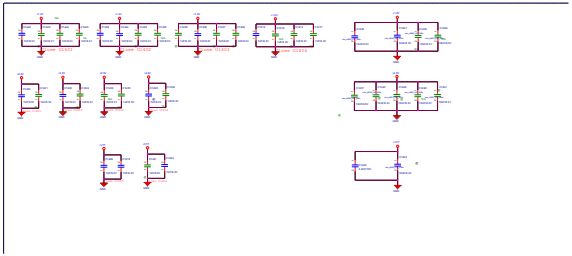
961 Processor and Memory Type	SKL-H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CK0[1:0], CK1[1:0]	CA0[1:0], CA1[1:0]	CA0[1:0], CA1[1:0]	CA1[1:0], CA0[1:0]
Control (CTRL)	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[1:0]	CKE[1:0]	CKE[1:0]	CKE[1:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, RAS	MA[16:0], BG[1:0], BA[1:0],ACT#, RAS	MA[16:0], BG[1:0], BA[1:0], ACT#, RAS	CA0[9:0], CA0[9:0]
Strobe	DQS0P[7:0], DQS0N[7:0]	DQS0P[7:0], DQS0N[7:0]	DQS0P[7:0], DQS0N[7:0]	DQS0[7:0], DQS1#[7:0]
ECC strobe	DQS0P[8], DQS0N[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[31:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

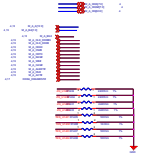
Title :	DDR4_TERMINATION_A		
Engineer:	SZEE		
Size: D	Project Name: X441UBR		Rev: 0G1
Date: Friday, June 07, 2019		Sheet 13 of 48	

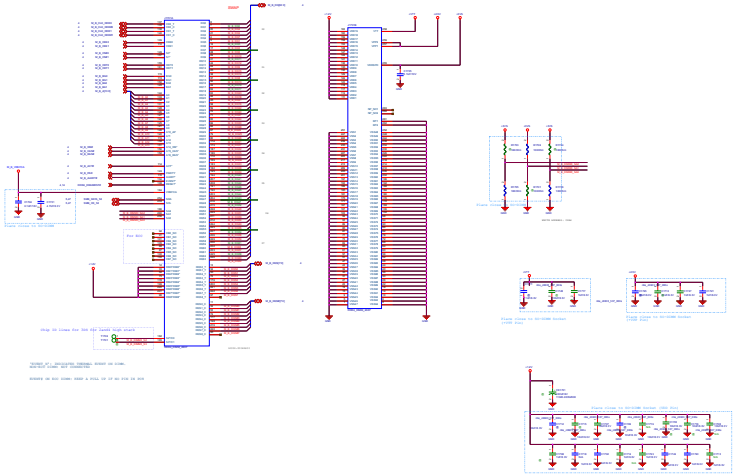


Onboard Memory Source

MEMORY_TYPE	Capacity	Description
DDR4_SDRAM_U1	8G Bytes	MT40A4G16RA-062E:F TRAY
DDR4_SDRAM_U2	8G Bytes	K4A8G165WB-BIRB TR/BR







ASUS	Title:	DDR4_SO-DIMM_1		
	Size:	Document Number:		Rev:
		90HB0DB0		
	Date:	Sheet of		

Figure 4-53. KBL U DDR4 x16 Devices Memory Down V_{REF_CA} Overview

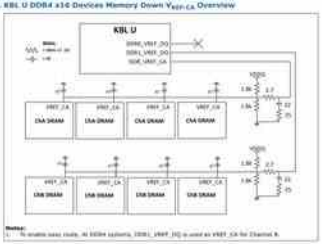
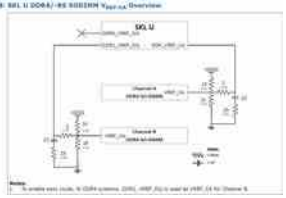
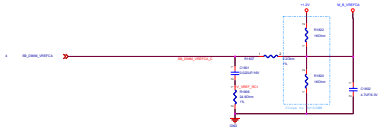
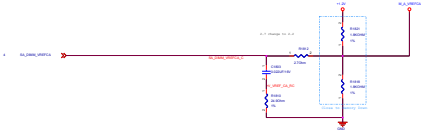


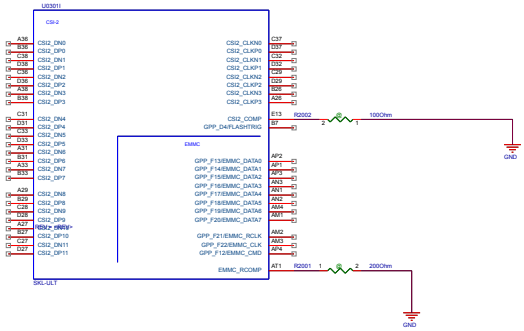
Figure 4-48. KBL U DDR4/-RS SODIMM V_{REF_CA} Overview



All Vref trace must be 20 mils width



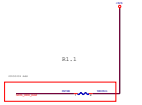


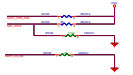


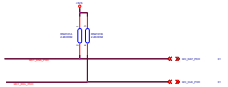
BOM

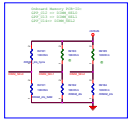
ASUS	Project Name: X441UBR	Rev: R2.1
Title : CPU_PCH_CSI2,EMMC		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: SZ/EE
Date: Friday, April 27, 2018	Sheet 20 of 102	

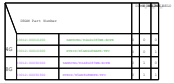
Main Board

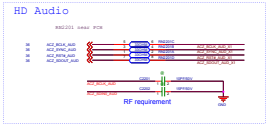




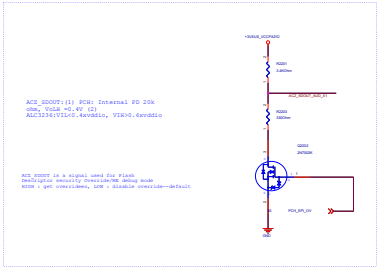


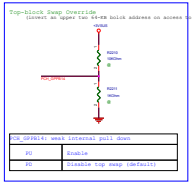




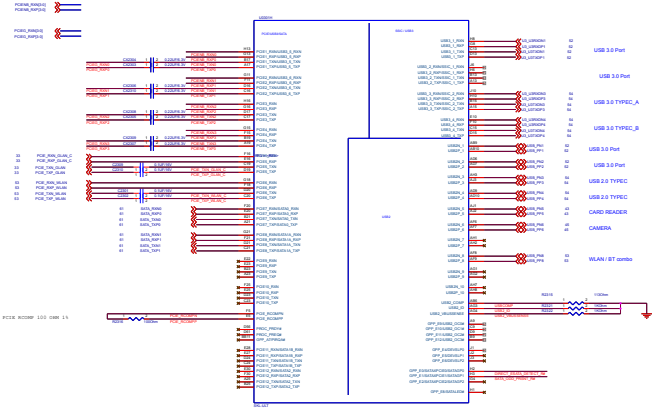

HD Audio
RM2201 near PCH
RF requirement
GND


audio
GPP_D4/SD_PWR_EN
GPP_D5/SD_CMD
GPP_D6/SD_DAT0
GPP_D7/SD_DAT1
GPP_D8/SD_DAT2
GPP_D9/SD_DAT3
GPP_D10/SD_CLK
GPP_D11/SD_CD
GPP_A7/SD_PWR_EN#/SM_CD1
GPP_A8/SD_1P8_SEL
SD_RCOMP
GPP_F23
GND


ACE_SDOUT:(1) PCH: Internal PD 20k
GSPI, Vcc1d =0.6V (2)
ALC3236:VIL<0.4xvddio, VIH>0.6xvddio
ACE_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
NOTE : pec overridemn, 1=M : disable override--default
+3VALW_VCCPADSD
PCH_SPI_CS#
GND


Top-block Swap Override
(inverst an upper two 4K=KB bolck address on access to SPI and PRM)
PCH_GPP9/14: weak internal pull down
PD Enable
PU Disable top swap (default)

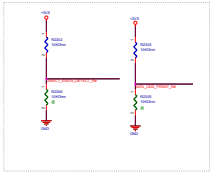

ASUS
X441UBR
Title : CPU_PCH_AUDIO.SCH1.SCH2
Engineer: EE
Date: Friday, April 27, 2018



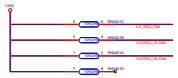
USB 2.0		Mapping	USB 3.0	
1	USB2.0 FOR USB3.0 Port		1	USB 3.0 Port
2	USB2.0 FOR USB3.0 Port		2	USB 3.0 Port
3	USB 2.0 TYPEC_A		3	USB 3.0 TYPEC_A
4	USB 2.0 TYPEC_B		4	USB 3.0 TYPEC_B
5	CARD READER			
6	CAMERA			
7				
8	WLAN / BT combo			

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-Lay	Clock
PCIE 1	GBE		PCIE3
PCIE 2	GBE		
PCIE 3	GBE		
PCIE 4	GBE		
PCIE 5	WLAN		PCIE4
PCIE 6	WLAN		PCIE5
PCIE 7 (x4)	HDD		
PCIE 8 (x4)	SSD		
PCIE 9	N/A		
PCIE 10 (x4)	N/A		

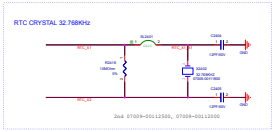
SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD
PORT 2	N/A
PORT 3	N/A

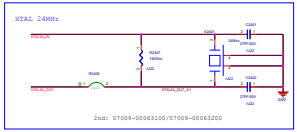


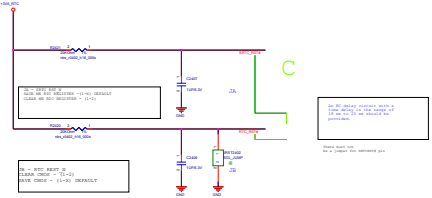
Offset Byte #	Bits	Description	Usage
0x1B0h	7	**Reserved. Set to 0x0.**	
	6	**SATA / PCIe GPIO Polarity Port 3 (SPP3):** 0=# GPIO Polarity Port 3 is an to PCIe mode when the SATAXPCIE3 pin is "0" and SATA when SATAXPCIE3 pin is "1" (default) 1=> # GPIO Polarity Port 3 is set to SATA mode when the SATAXPCIE3 pin is 0 and PCIe when SATAXPCIE3 pin is "1"	This strap must also be configured if PCIe/SATA Combo Port 3 Strap (PCH_SATA_P3_Pres) is configured to "1". Note: This setting only has effect when SATA / PCIe select for Port 3 (SATA_PCIE_SP3) is configured to "1". Note: The close and the Polarity Select (SPP) / PCIe Combo Port 3 (PCHPCIE_P3_STRP) must match for proper port functions.
	5	**SATA / PCIe GPIO Polarity Port 1 (SPA1):** 0=# GPIO Polarity Port 1 is an to PCIe mode when the SATAXPCIE1 pin is "0" and SATA when SATAXPCIE1 pin is "1" (default) 1=> # GPIO Polarity Port 1 is set to SATA mode when the SATAXPCIE1 pin is "1"	This strap must also be configured if PCIe/SATA Combo Port 1 Strap (PCH_SATA_P1_Pres) of PCIe/SATA Combo Port 1 Strap (PCH_SATA_P1_Pres) is configured to "1". Note: This setting only has effect when SATA / PCIe select for Port 1 (SATA_PCIE_SP1) is configured to "1". Note: The close and the Polarity Select SATA / PCIe Combo Port 1 (PCHPCIE_P1_STRP) must match for proper port functions.
	4	**SATA / PCIe GPIO Polarity Port 0 (SPE0):** 0=# GPIO Polarity Port 0 is an to PCIe mode when the SATAXPCIE0 pin is "0" and SATA when SATAXPCIE0 pin is "1" (default) 1=> # GPIO Polarity Port 0 is set to SATA mode when the SATAXPCIE0 pin is "1"	This strap must also be configured if PCIe/SATA Combo Port 0 Strap (PCH_SATA_P0_Pres) is configured to "1". Note: This setting only has effect when SATA / PCIe select for Port 0 (SATA_PCIE_SP0) is configured to "1". Note: The close and the Polarity Select SATA / PCIe Combo Port 0 (PCHPCIE_P0_STRP) must match for proper port functions.

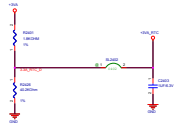


CHECK PCIEG CLK

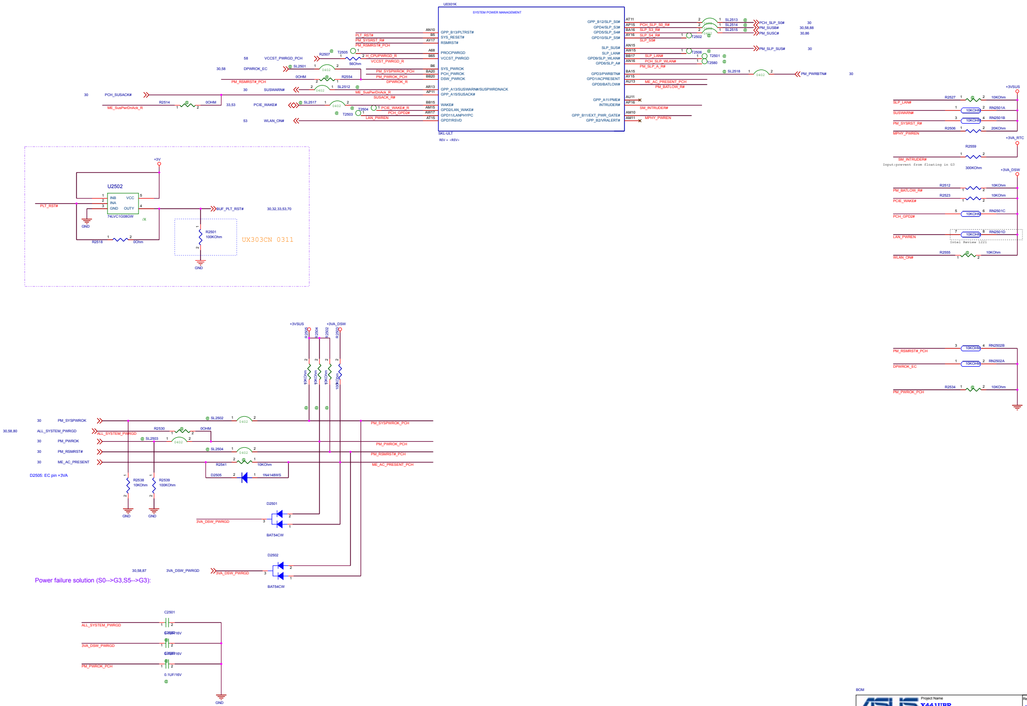






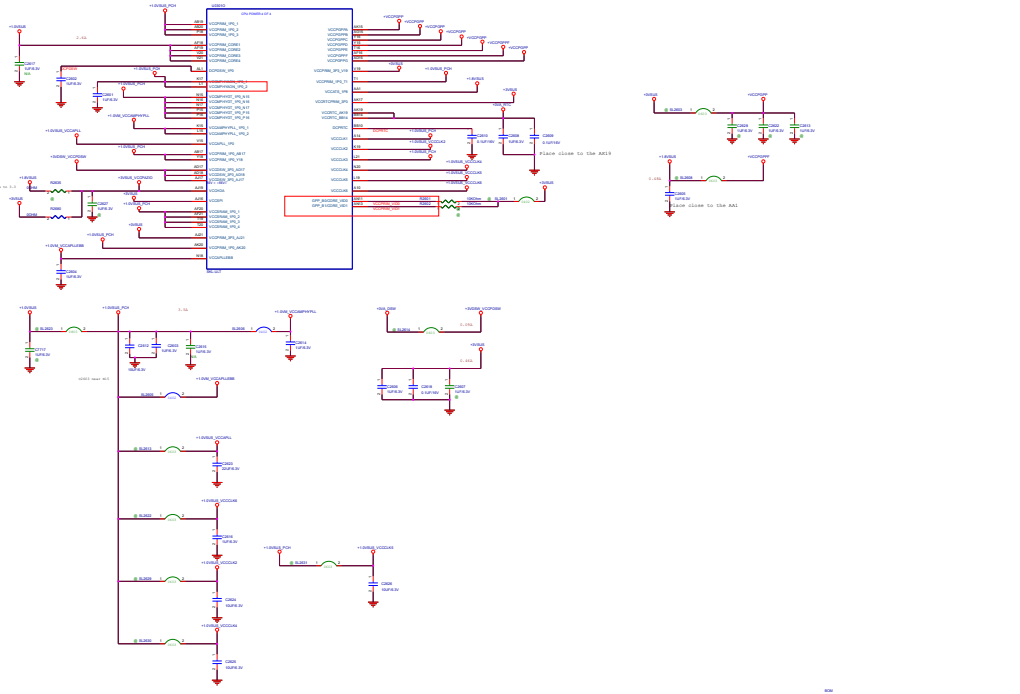


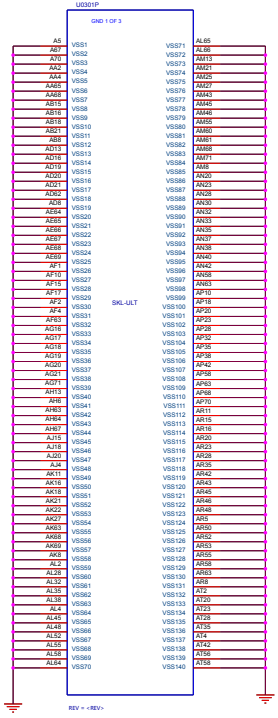
Main Board

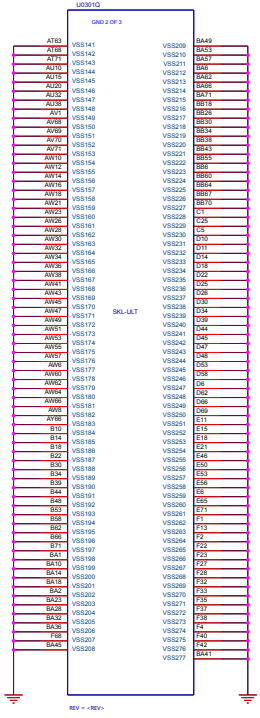


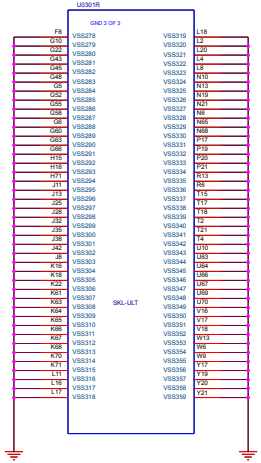
BOM

ASUS	Project Name X441UBR	Rev R2.1
Title : CPU_PCH_SYS_POWER		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, April 27, 2018	Sheet 25 of 102	


Place close to the AX19
Place close to the AX1
Project Name
X441UBR
Title :
CPU_PCH_POWR,GND
Engineer:
Checked
Friday, April 27, 2018





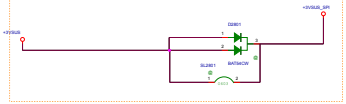


BOM

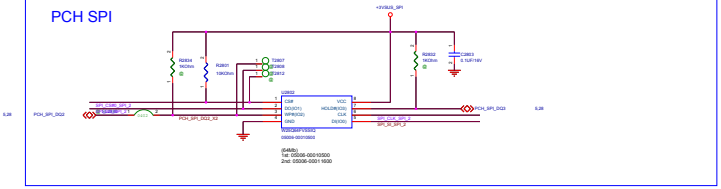
REV	Project Name: X441UBR		Rev: R2.1
Title : CPU_PCH_POEWR,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Friday, April 27, 2018	Sheet 27 of 102		

SPI PCH Power

UX303 0814

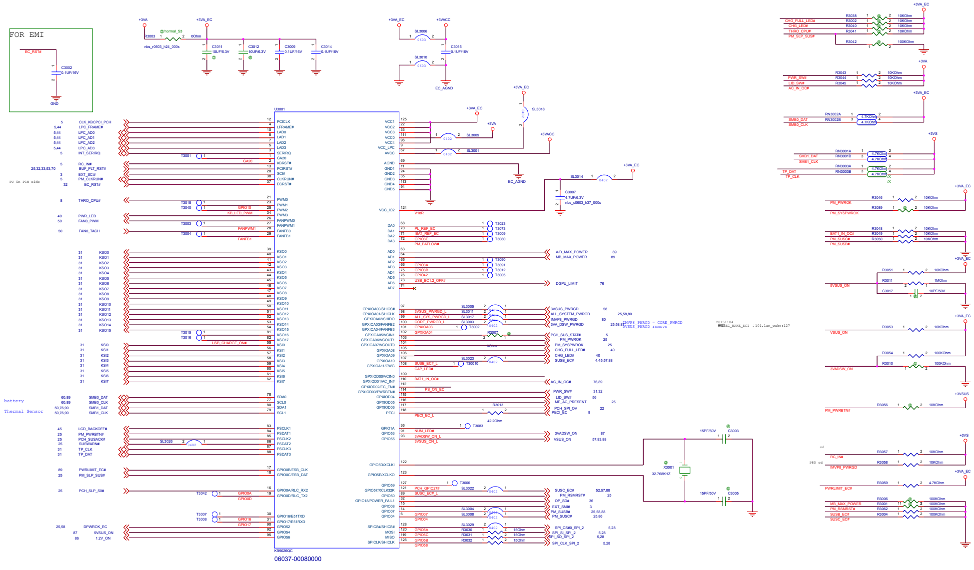


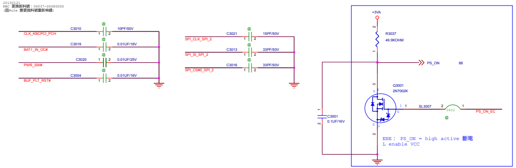
PCH SPI



BOM

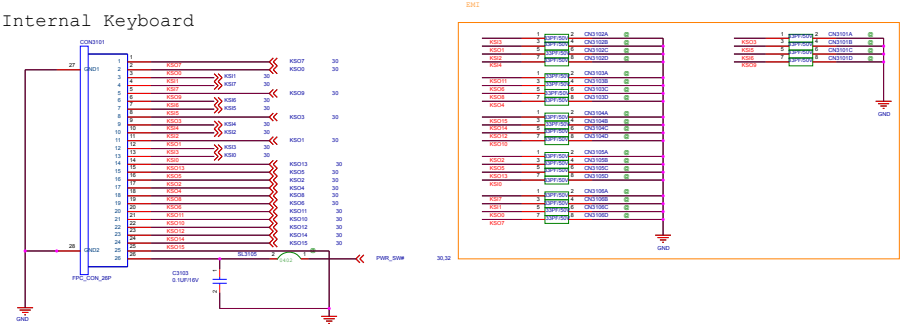
ASUS	Project Name: X441UBR		Rev: Rb 1
Title : PCH-SPI ROM.OTH			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Friday, April 27, 2018		Sheet 29 of 102	



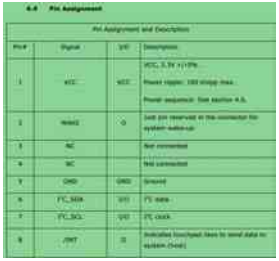


State	LPC	eSPI
902X	/non-eSPI	NA
903X	/non-eSPI /903X_non-eSPI	/eSPI

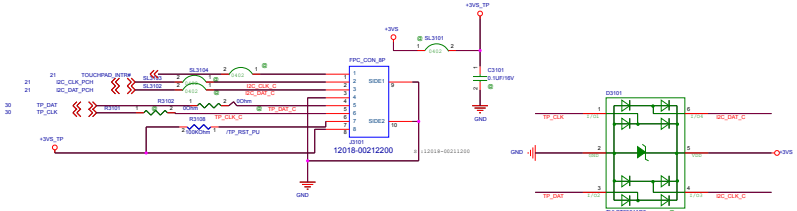
Internal Keyboard



Touch PAD



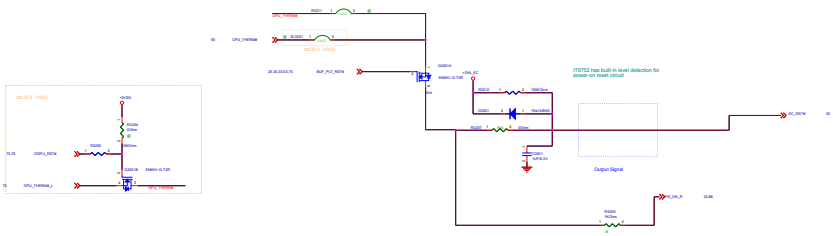
Pin #	Signal	I/O	Description
1	VCC	VCC	VCC, 3.3V +/-10% ... Power ripple: 100 mVpp max ... Power sequence: See section 4.5.
2	Reset	O	Set pin reserved in the connector for system wake-up.
3	NC		Not connected
4	NC		Not connected
5	GND	GND	Ground
6	I2C_SDA	I/O	I2C data
7	I2C_SCL	I/O	I2C clock
8	/INT	O	Indicates touchpad has to send data to system. (Intel)



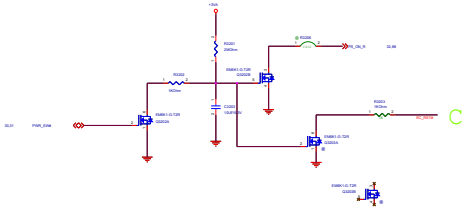
BOM

ASUS	Project Name: X441UBR	Rev: R2.1
Title :	EC-IT8572(2)_KB,TP	
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: EE	
Date: Friday, April 27, 2018	Sheet 31 of 102	

Thermal Policy



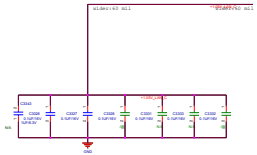
battery embedded (press pwr_sw 10sec, then reset ec)

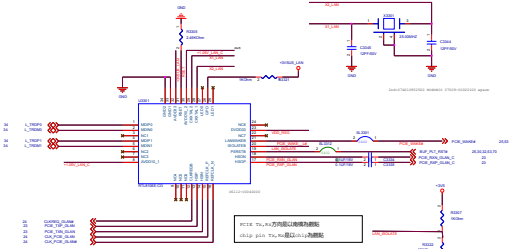


ASUS	Project Name: X441UBR		Rev: 1.0
Title: RST_Reset Circuit			
Size:	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Friday, April 27, 2018	Sheet: 32	of: 100	

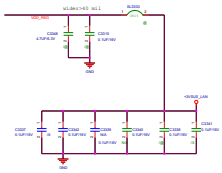
The distance from u3301.36 to L3301 within 200 mil.

The distance from L3301 to +1.05V_LAN_C within 200 mil.





The distance from U3301.34, U3301.35 , VDD_REG net to SL3303 within 200 mil.



RTK建議TV_LAN raise time >0.5ns

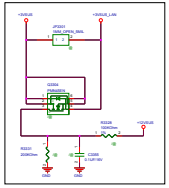
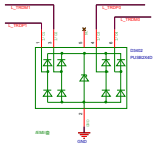
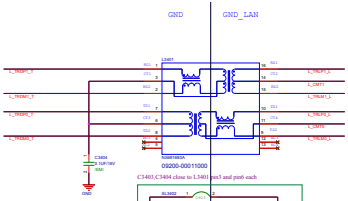


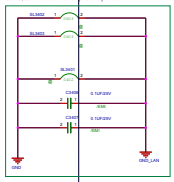
Table 17. Power Sequence Parameter

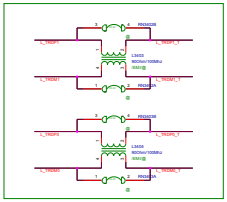
Symbol	Description	Min	Typical	Max	Unit
T1	3.3V Rise Time	0.1		10	ms
T2	1.8V Rise Time	0.1		10	ms
T3	3.3V to 1.8V Delay	0			ms
T4	1.8V to 3.3V Delay	0			ms

Note: The Power Sequence must comply with this requirement.



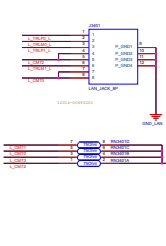




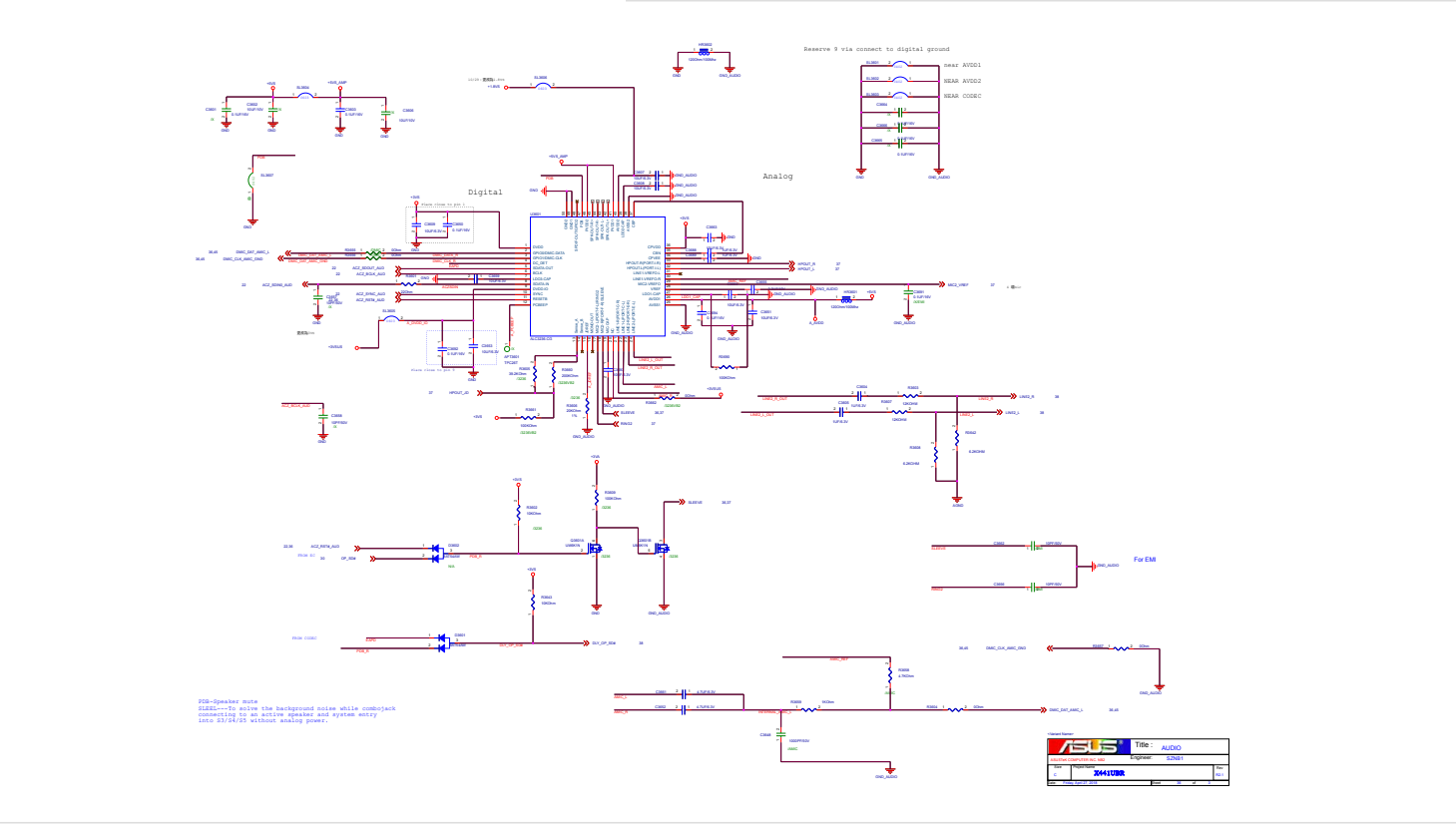


X540SA R2.0 EMI 換到L3401前

Transformer RJ-45腳
LAN GND

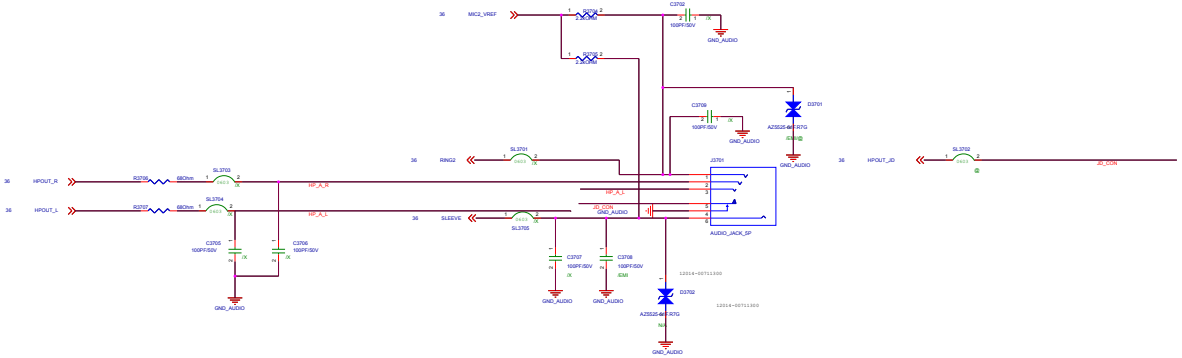


1	Tx +
2	Tx -
3	Rx +
4	No Singal
5	No Singal
6	Rx -
7	No Singal
8	No Singal

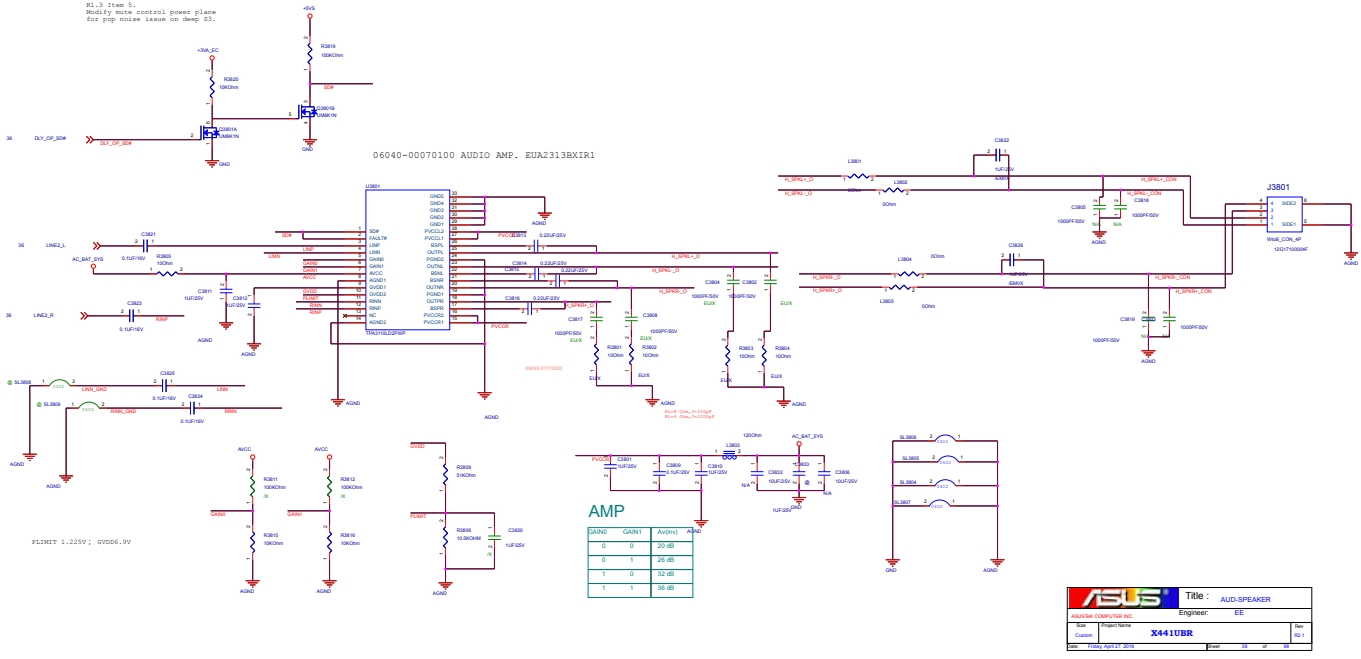

Digital
Analog
Reserve 9 via connect to digital ground
near AVDD1
NEAR AVDD2
NEAR CODEC
For EMI
PDB-Speaker mute
SIZE:---To solve the background noise while combojack
connecting to an active speaker and system entry
into S3/S4/S5 without analog power.
Title : AUDIO
Engineer: S2NB1
X441UBR

AUDIO JACK

Apple & NOKIA & HP & 4pole MIC



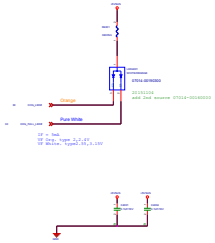
ASUSTeK COMPUTER INC.	Title : PHONEJACK		
	Engineer:		
Size: Custom	Project Name: X441UBR		Rev: 82.1
Date: Friday, April 27, 2018	Sheet 37 of 86		



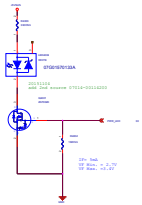
Title :	AUD-SPEAKER
Engineer:	EE
ASUSTeK COMPUTER INC	
Size: Custom	Project Name: X441UBR
Rev:	R2.1
Date: Friday, April 27, 2018	Sheet 39 of 98

LED indicator 1104 LED 測光

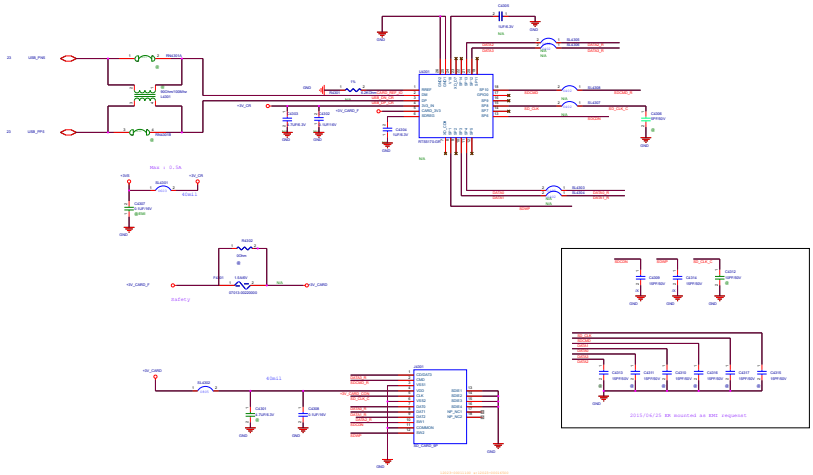
Charger LED



POWER LED



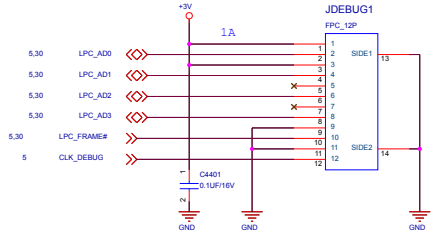
Title:			IO Board_USB Conn_LED
Engineer:			Kelsey
Size	Number		Rev
B	94K41006		
Date:	Sheet	of	

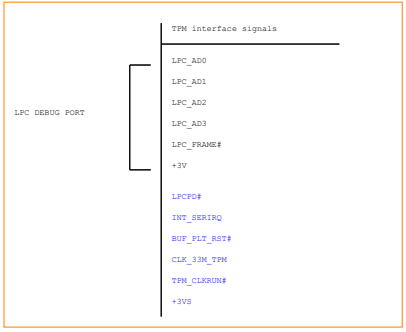


BOM

ASUS	Project Name: K441UBR	Rev: 0.1
Title: CB****		
Size: A3	Dept: MB/PWR COMPUTER INC.	Engineer: EE
Date: Friday, April 27, 2018	Sheet 43 of 102	

LPC DEBUG PORT

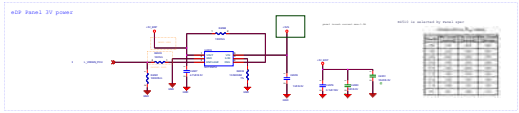


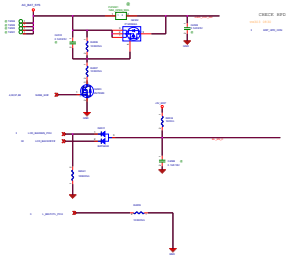


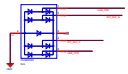
BOM

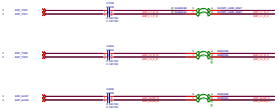
ASUS	Project Name: X441UBR	Rev: R2.1
Title : DEBUG PORT		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, April 27, 2018	Sheet 44 of 102	

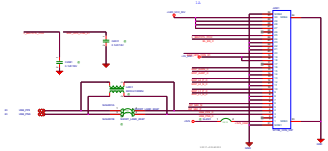
eDP Panel

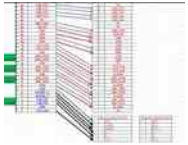




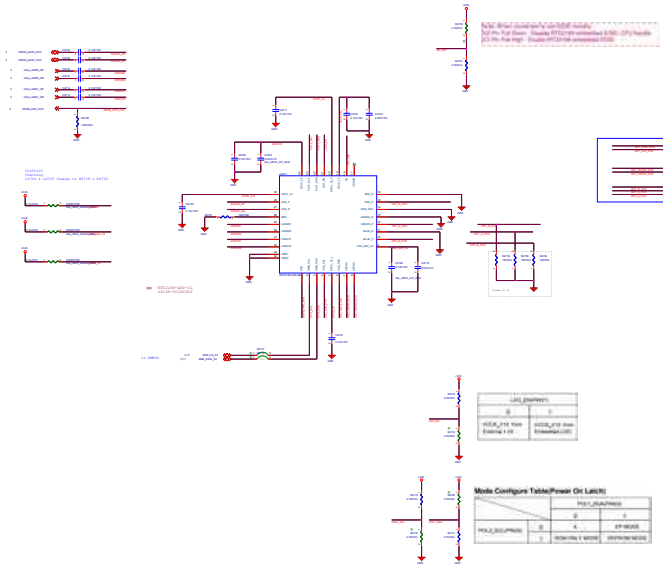




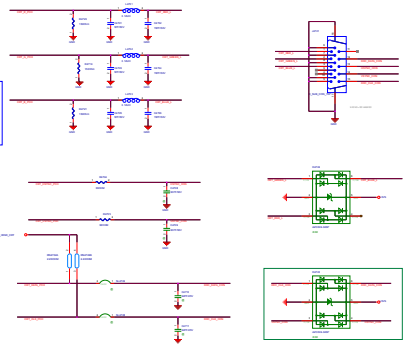


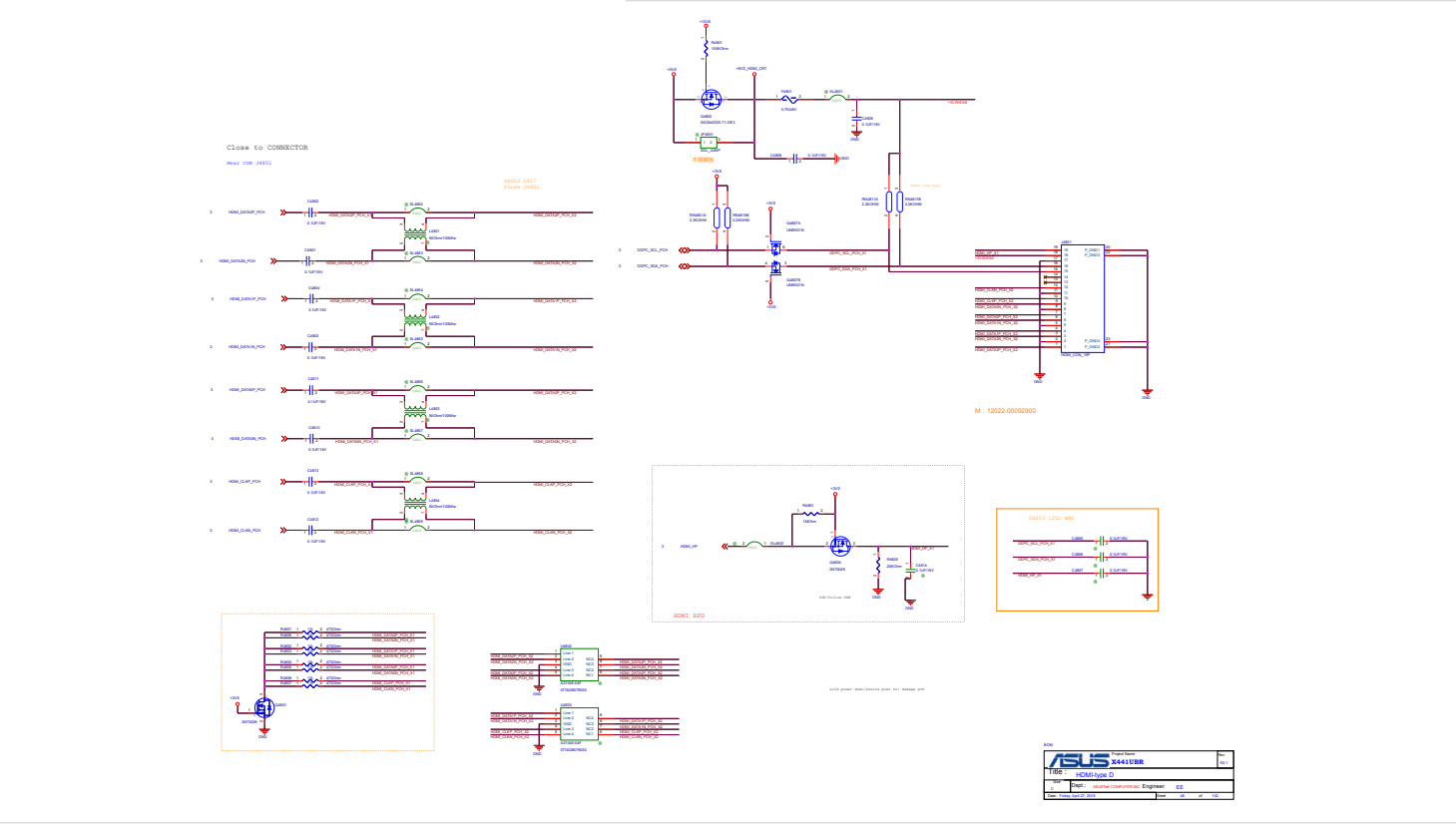


eDP to VGA



CRT D-SUB

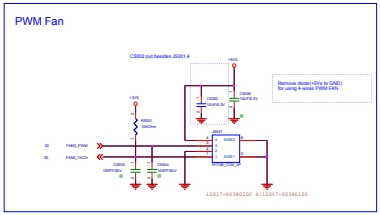



Close to CONNECTOR
Short CON J4801
0x203 0917
Close J4801
M : 12022-00092900
HDMI HPD
0x203 1202 RM1
X441UBR
HDMI-type D

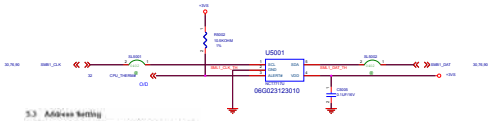
GPU Thermal Sensor

Tung, 0302-4 Add GPU Thermal Sensor (PSS)

PWM Fan



CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001100b (a is R/W bit).

5.4. ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin

PULL-UP RESISTOR	TEMPERATURE (°C)
ALERT#	2KΩ: 72
	7.5KΩ: 90
	10.5KΩ: 100
	14KΩ: 105
	19.7KΩ: 110

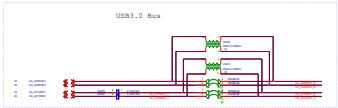
Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

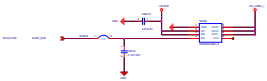
----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========D_THERMDA(10 mils)
10 mils
==========D_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

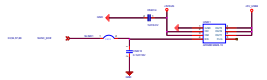
BOM

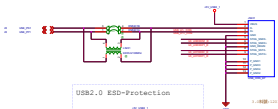
ASUS	Project Name: X441UBR		Rev: R2.1
Title :	FAN_Fan & Sensor		
Size: D	Dept.:	ASUSTeK COMPUTER INC.	Engineer: EE
Date: Friday, April 27, 2018		Sheet: 66	of: 107

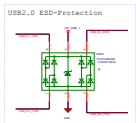
USB 3.0 con.

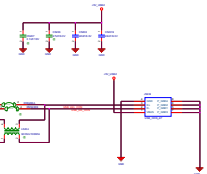






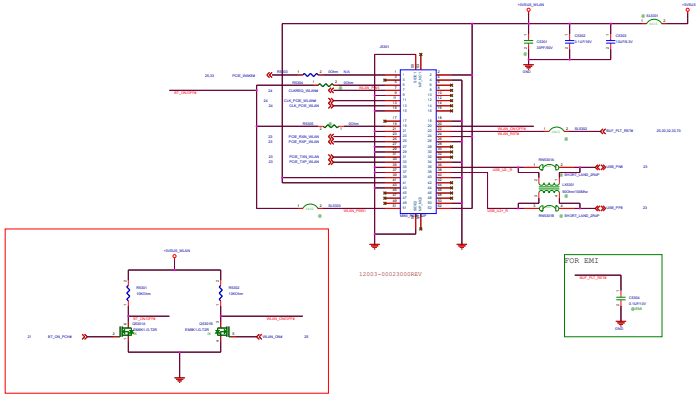




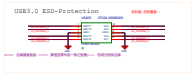


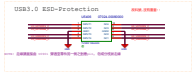
ASUS	Compal Electronics, Inc.			
Title	USB 3.0 + 2.0 CONN.			
Size	Document Number	Rev		
Date:	Sheet of			

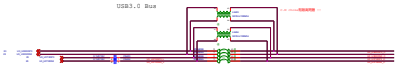
WLAN con.

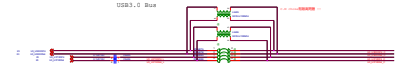


Title :	WLAN	
Engineer	Ed.	
Size	Project Name	Rev
Custom	X441UBR	Rev 1

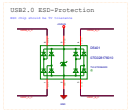

USB3.0 ESD-Protection

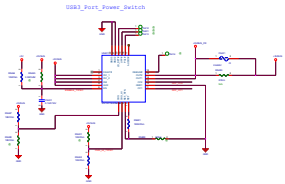

USB3.0 ESD-Protection

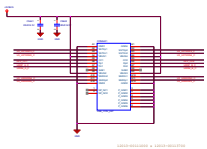

USB3.0 Bus

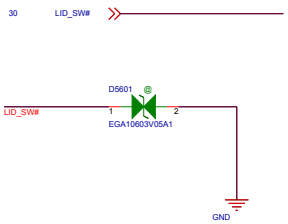

USB3.0 Bus


USB2.0
USB2.0

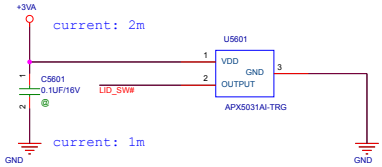

USB2.0 ESD-Protection


USB3_Port_Power_Switch





Hall effect switch

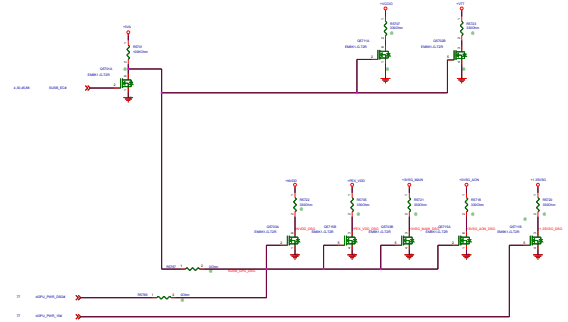


1109:06033-00140000

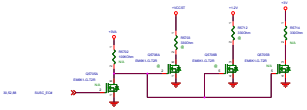
BOM

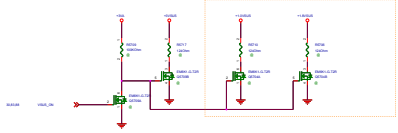
Project Name: X441UBR		Rev: R2.1
Title : PWR_SW&HALL_SW		
Size: A	Dept.: ASUSTeK COMPUTER INC. Engineer: EE	
Date: Friday, April 27, 2018	Sheet 56 of 102	

Main Board



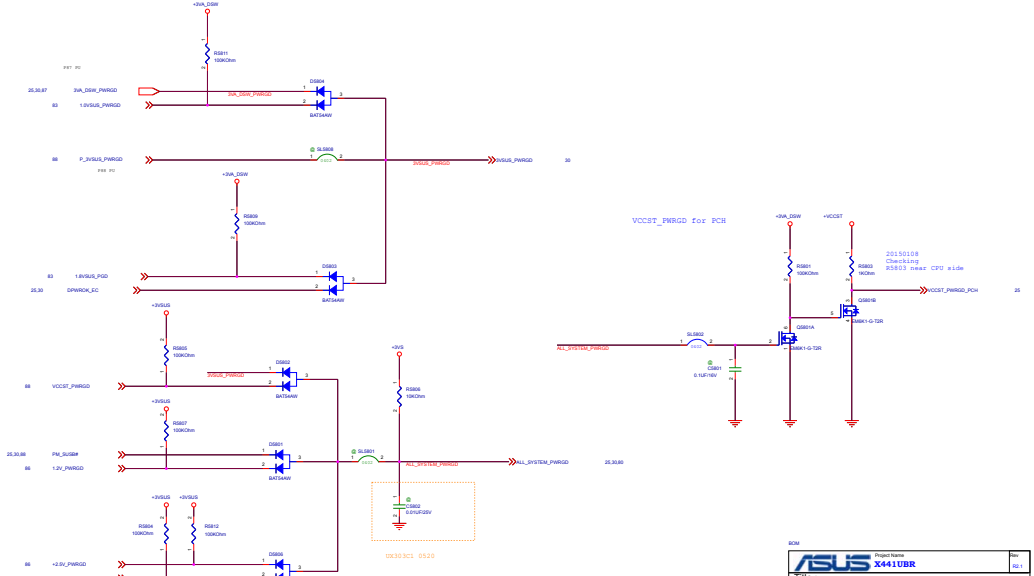
4/20 Stuff R5710 and R5711

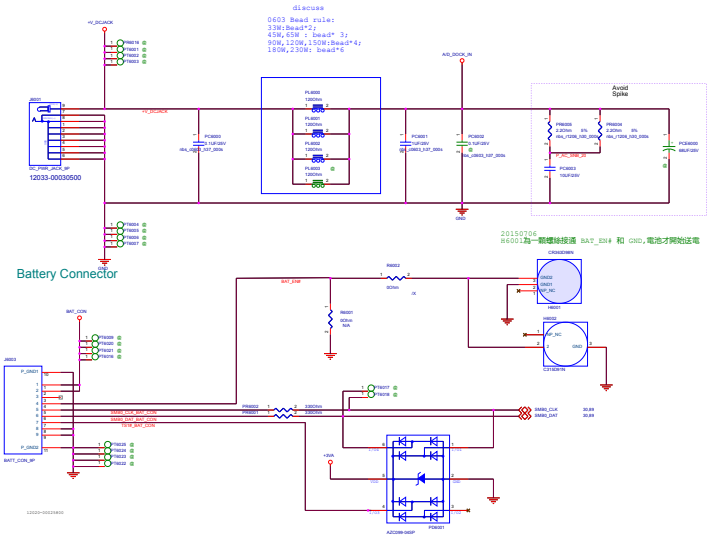


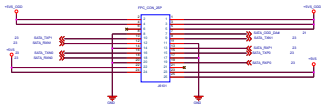


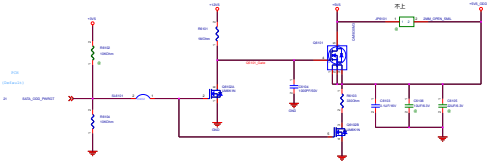
ASUS

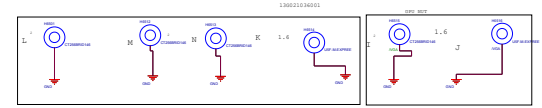
Project Name	X441UBR
Title	VSIG_Discharge
Size	Rev
Date	Sheet of

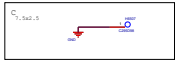

+3VA_DSW
RS811
100KOhm
PBT PD
25,30,87
3VA_DSW_PWRGD
3VA_DSW_PWRGD
DS804
BAT54AW
83
1.05VSUS_PWRGD
88
P_3VSUS_PWRGD
SLS808
3VSUS_PWRGD
3VSUS_PWRGD
30
PBS PD
+3VA_DSW
RS809
100KOhm
83
1.8VSUS_PGD
25,30
DPWROK_EC
DS803
BAT54AW
+3VSUS
RS805
100KOhm
3VSUS_PWRGD
DS802
BAT54AW
88
VCCST_PWRGD
+3VSUS
RS807
100KOhm
25,30,88
PM_SUS#
86
1.2V_PWRGD
DS801
BAT54AW
+3VS
RS806
10KOhm
SLS801
0402
ALL_SYSTEM_PWRGD
ALL_SYSTEM_PWRGD
25,30,80
C0402
0.01UF/25V
UX303CI 0520
+3VSUS
+3VSUS
RS804
150KOhm
RS812
150KOhm
86
+2.5V_PWRGD
88
VCCIO_PWRGD
DS806
BAT54AW
VCCST_PWRGD for PCH
+3VA_DSW
+VCCST
RS821
100KOhm
RS803
0Ohm
20150108
Checking
RS803 near CPU side
VCCST_PWRGD_PCH
25
DS801B
DS801A
BSS84 Y-G-T2R
ALL_SYSTEM_PWRGD
SLS802
0402
CS801
0.1UF/16V
BOM
Project Name
X441UBR
Rev
R2.1
Title :
PRO_Protect
Size
B
Dept.:
ASUSTeK COMPUTER INC
Engineer:
EE
Date
Friday, April 27, 2018
Sheet
68
of
102

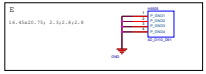

discuss
0603 Bead rule:
33W:Bead*2;
45W,65W : bead* 3;
90W,120W,150W:Bead*4;
180W,230W: bead*6
+V_DCJACK
AVS_DIODE_IN
Avoid Spike
20150706
H6001為一顆螺絲接通 BAT_EN# 和 GND,電池才開始送電
Battery Connector
BAT_CON
BAT_CON_IP
SMB_CLK_BAT_CON
SMB_DAT_BAT_CON
TP/B_BAT_CON
SMB_CLK
SMB_DAT
+3VA
AZC099-04SP
DC_PWR_JACK_IP
12033-00030500

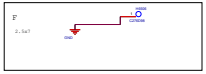

+5VS_OSS
FPC_OSS_90P
+5VS_OSS
SATA_TXP1
SATA_RXN1
SATA_TXN0
SATA_RXP0
SATA_OSS_RXP
SATA_OSS_RXN
SATA_TXN1
SATA_TXP0
+3VS
GND
GND
JHDD1

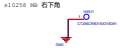

不上
+3VS
+5VS
+5VS_OSS
R8432
100Ohm
R8433
100Ohm
R8434
100Ohm
R8435
100Ohm
Q8430
SSM3K15AMFV
Q8431
SSM3K15AMFV
Q8432
SSM3K15AMFV
R8436
330Ohm
C8433
0.047UF/16V
C8434
0.47UF/6.3V
C8435
0.047UF/6.3V
JP8433
JUMP_CMOS_1MM
SATA_OSS_PWRDET
SATA_OSS_RXP
SATA_OSS_RXN
SATA_OSS_TXP
SATA_OSS_TXN
GND
GND
GND

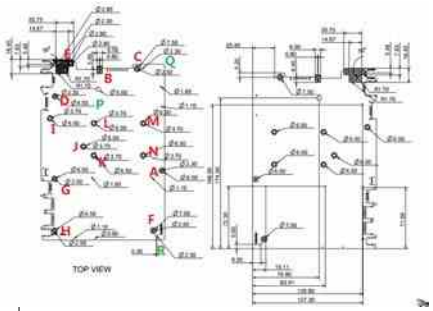












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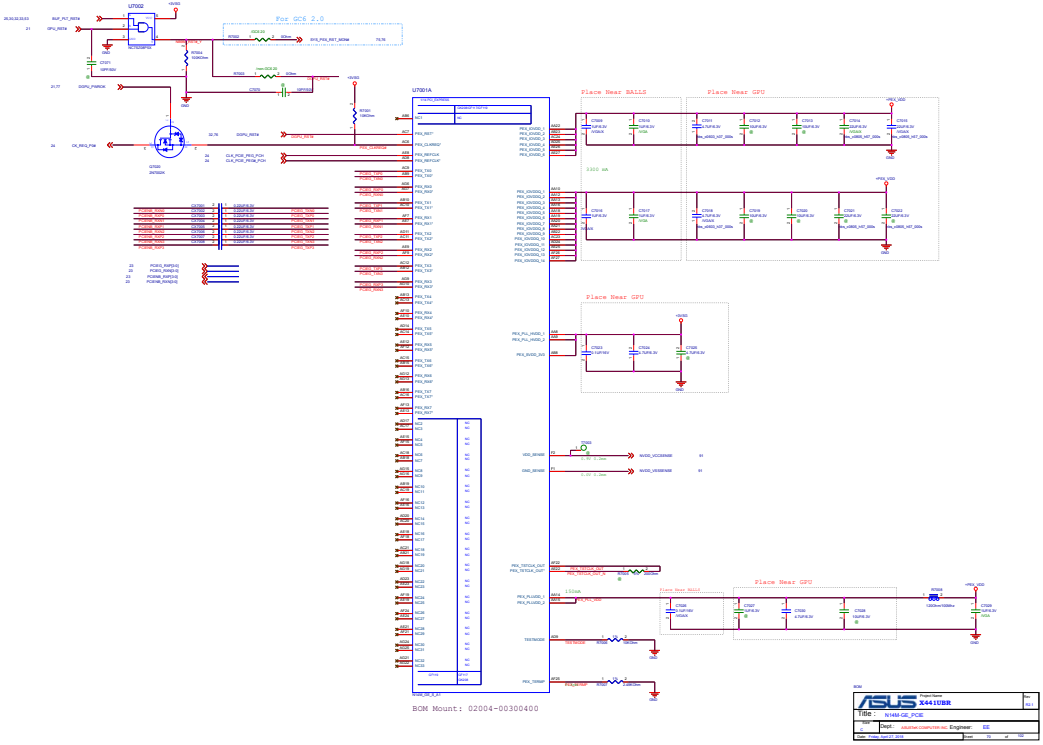
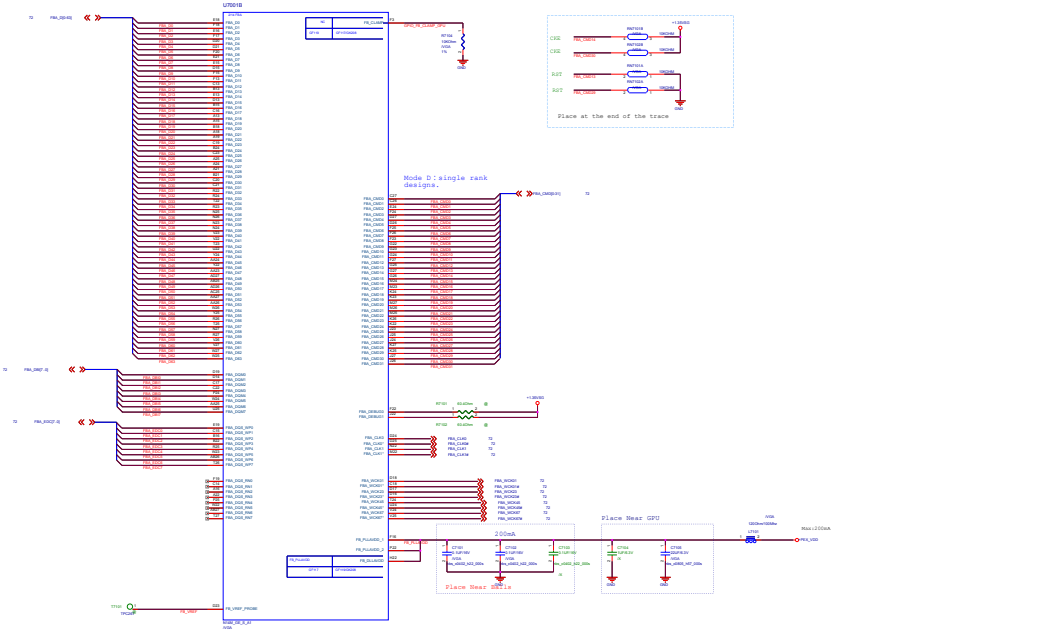
				ASUS X441UBR	A01
				Title : SCREW HOLE & NUT	
Size					
Custom			Dept. :	Engineer:	EE
Date: Friday, April 27, 2018			Sheet	65 of 102	


For GC6 2.0
Place Near BALLS
Place Near GPU
Place Near GPU
Place Near GPU
2300 mA
150mA
U7001A
BOM Mount: 02004-00300400
X441UBR
N14M-GE_PCIE
ASUSTeK COMPUTER INC.
Engineer:
EE
Friday, April 27, 2018



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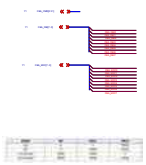
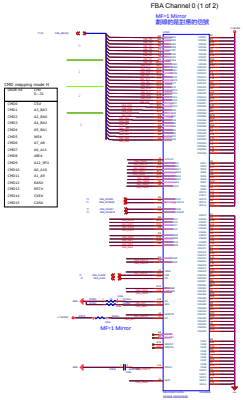
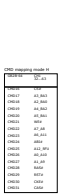
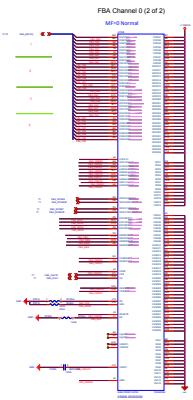
A	Dept.: ASUS Tech COMPUTER INC.	Engineer:	EE
Date: Friday, April 27, 2012		Sheet 11 of 103	

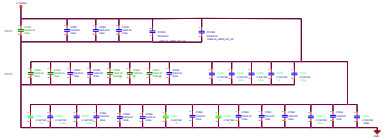


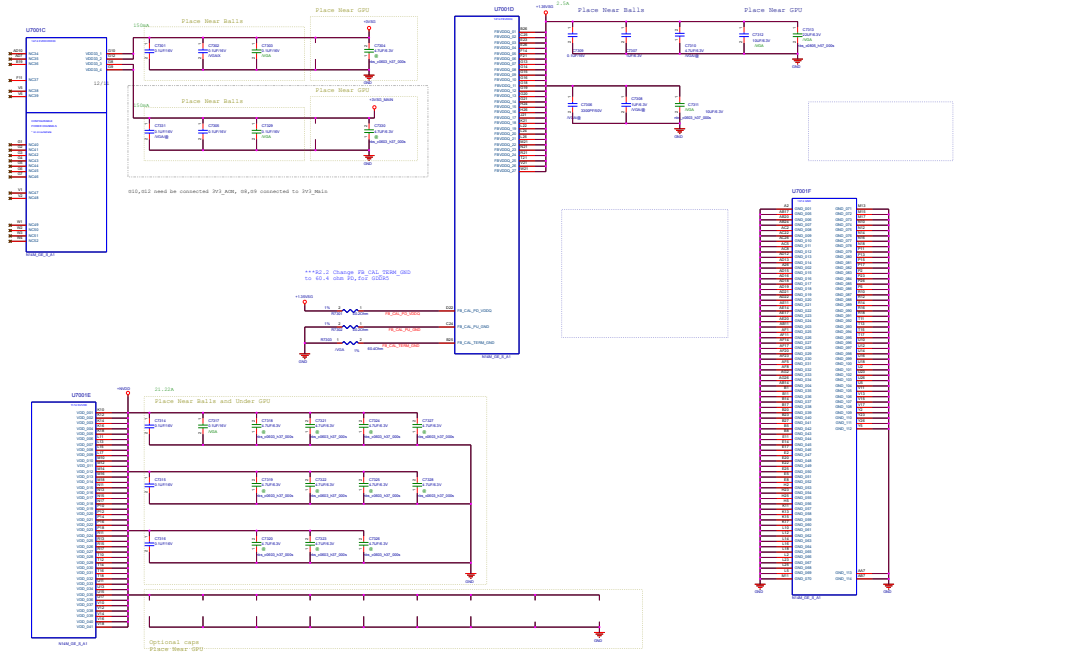






GDD5 MODE SELECTION





ASUS	Project Name: X441UBR		Rev: REV_1
Title:	N14M-GE-VDD		
Size: C	Docum	Engineer: EE	
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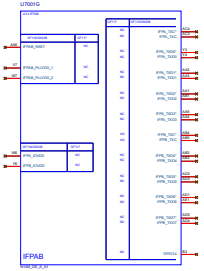
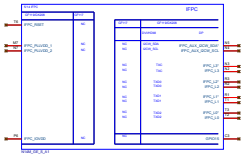
LVDS


U7001G
IFPAB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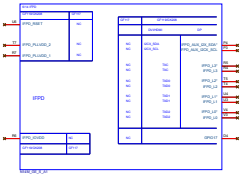
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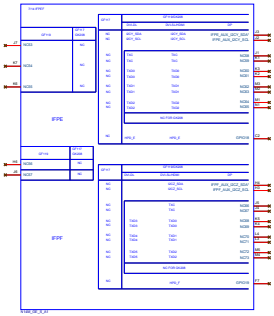
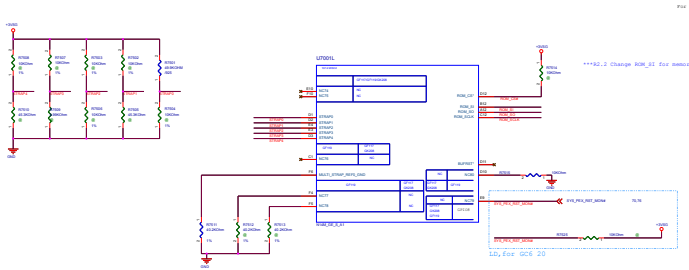
IFPD


U7001J
IFPE
IFPF

CRT


U7001K



VRAM	2Gb(128M*16)	81007-00030900-	gDDR3 128M*16 1.35V FBGA-96-	MICRON/MT41J128M16JT-093G-K-	EK4 158 PU-
顯[illegible]	4Gb (256M*16)	81007-00021500-	GDDR3 256M*16 1.35V FBGA96-	HYNIX/H5TC4G63CFR-N0C-	EK2 158 PD-
		81007-00021XXX-	GDDR3 256M*16 1.35V FBGA96-	MICRON/MT41J256M16JT-093(K)-	EK6 14.8K PS-

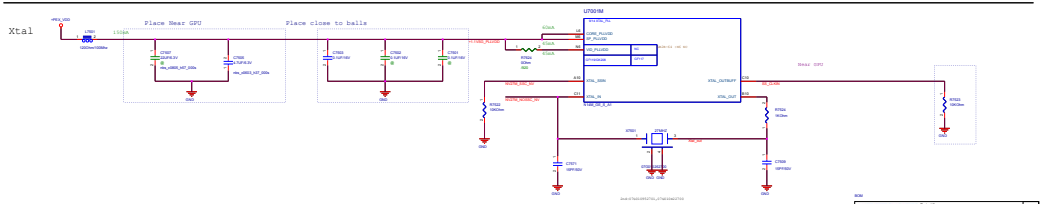
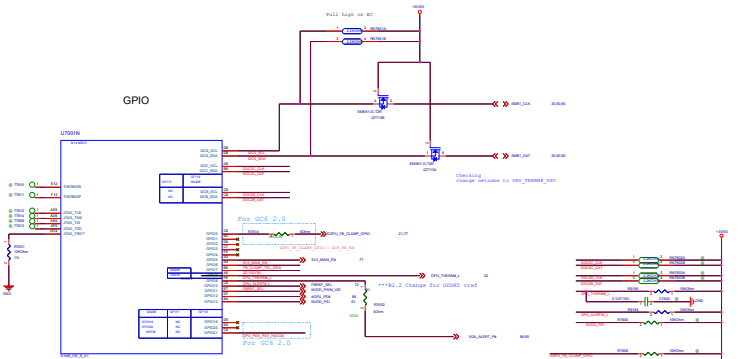
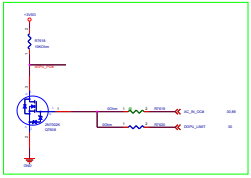
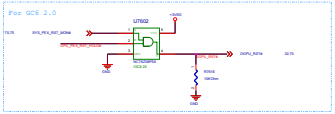


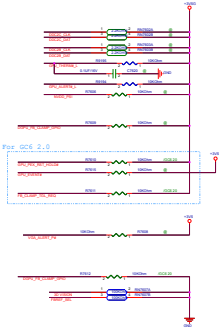
Table 12-1. GB25-b4 and GB49-118 GPIO Description

Pin Name	General Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPI00	PB_CLAMP_MON	I	PB Clamp monitor for GC6 1.0	PB pull-down on @MP
GPI01	SATA_PB_EN MISO_GSPI_CS	O O	PB Enable for GC6 2.0 Memory HDD CS	PB pull-down on @MP eDP_TX+ pull-up to 3+3_3DVP at @MP device is GMB, or pull down if EEPROM is enabled
GPI02	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPI03	LCD_VCC	O	Panel Power Enable	LCD_VCC : 100k pull-down
GPI04	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPI05	SYS_RAPE_EN	O	CPU power sequence log	100K pull up to 3+3_AON
GPI06	PB_CLAMP_THG_REQ	O	Clamp/Isolate request for GC6 1.0	100K pull up to system 3.3V
GPI07	GPU_EVENT#	I	GPU wake signal for GC6 2.0	100K pull up to 3+3_AON
GPI08	SPI1SIo	O, I	SI / Slave / R signal	100K pull-down
GPI09	SYS_RST_BOT_MON#	I	System side PCIe reset monitor	
GPI10	HI_DET	I/O	active low Thermal short	10K pull-up to 3+3_AON
GPI11	WOL_GSPI_CS	O	Memory HDD Control	100K pull-down
GPI12	PWRLIMIT	I	GPU Cross VRT PWM control signal	
GPI13	PWM_LEVEL	I	AC power detect or power supply monitor input	100K pull-up to 3+3_AON
GPI14	Rx	O	Power Shedding	10K pull up to 3+3_AON to enable from @MP
GPI15	MPE_IL	I	Hot Plug Detect for RTK card to Display Port in the BTW other card on Dual Link TV)	See Figure 12-1
GPI16	MPE_L	I	Hot Plug Detect for SPI	See Figure 12-1
GPI17	MC3CD1C2			
GPI18	MPI_D	I	Hot Plug Detect for SPI	See Figure 12-1
GPI19	MPI_I	I	Hot Plug Detect for SPI	See Figure 12-1
GPI20	MPI_F or SPI_B	I	Hot Plug Detect for IFPF or for IFPB other card in DisplayPort	See Figure 12-1
GPI22	Reserved			
GPI23	GPU_I2C3_SCL GPU_I2C3_SDA	O	GPU I2C3 for SPI read control	10K pull-up to 3+3_AON
GPI24	I2C0 Thermal Catastrophic Over Temperature		active Low Thermal Catastrophic Over Temperature	10K pull-up to 3+3_AON

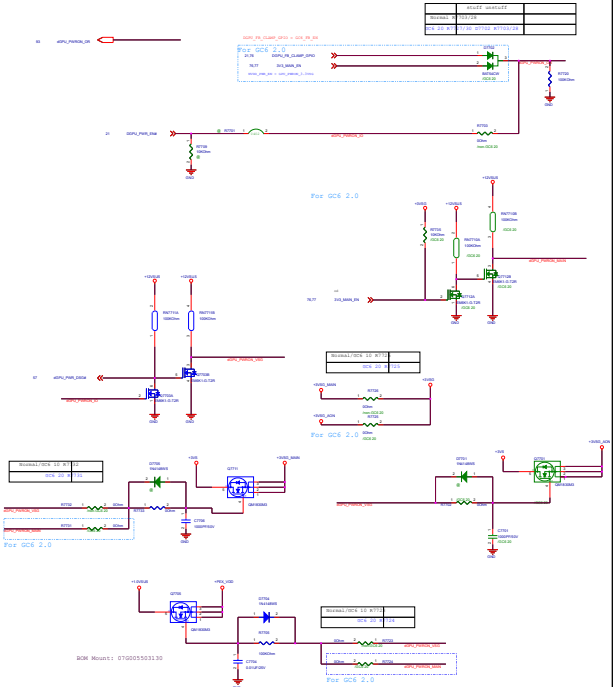




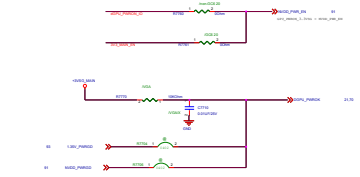


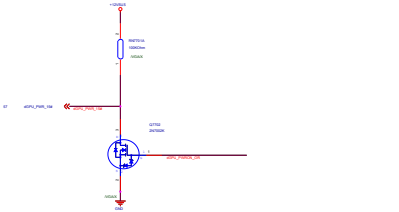


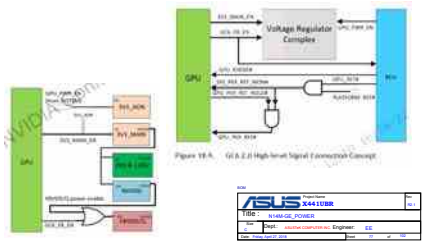
dGPU IO Power Sequence

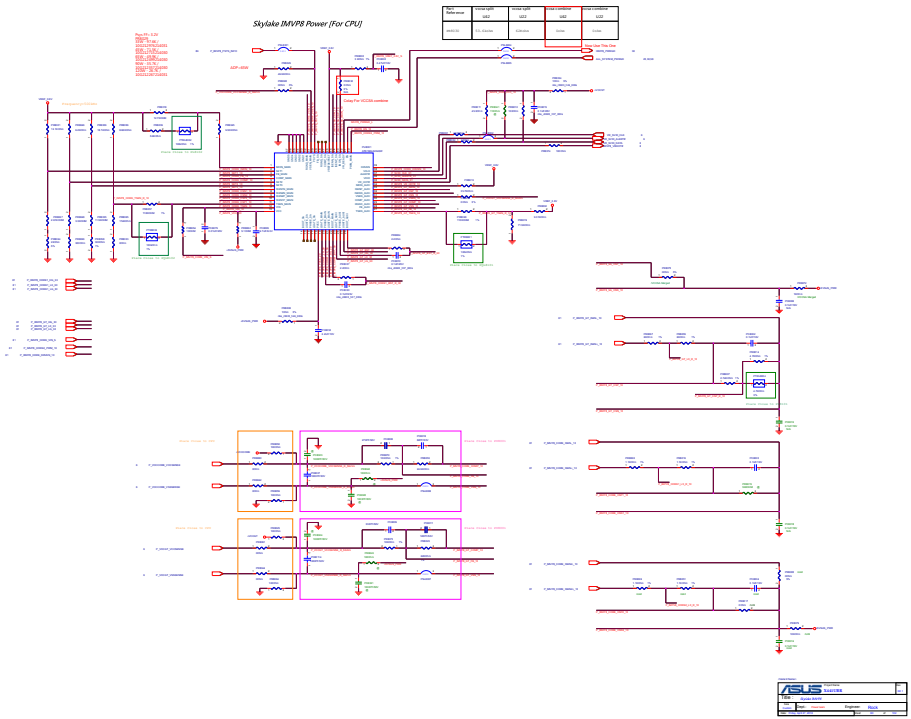


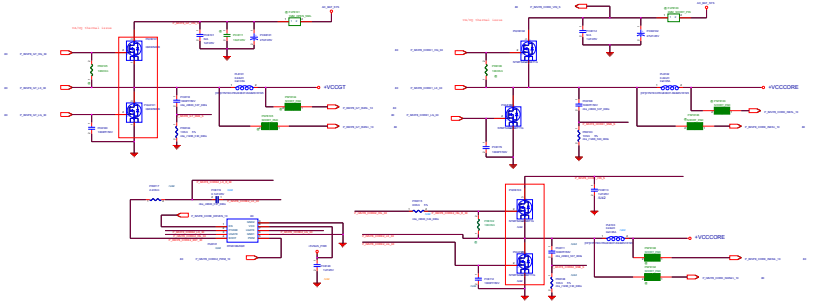
dGPU Core Power Sequence

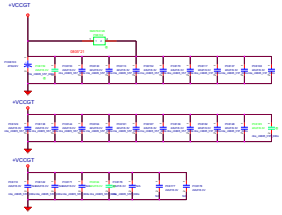


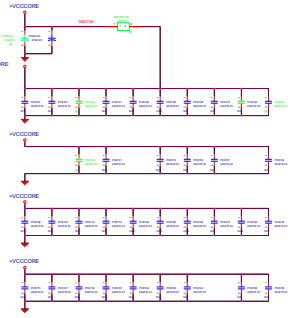





Skylake IMVP8 Power [For CPU]

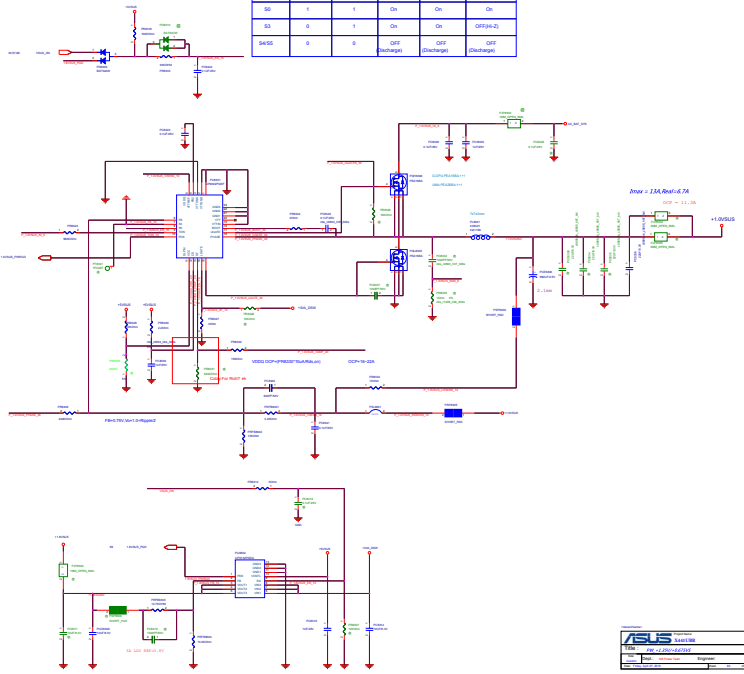






S3 And S5 Truth Table

State	PinY(S3)	PinA(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)



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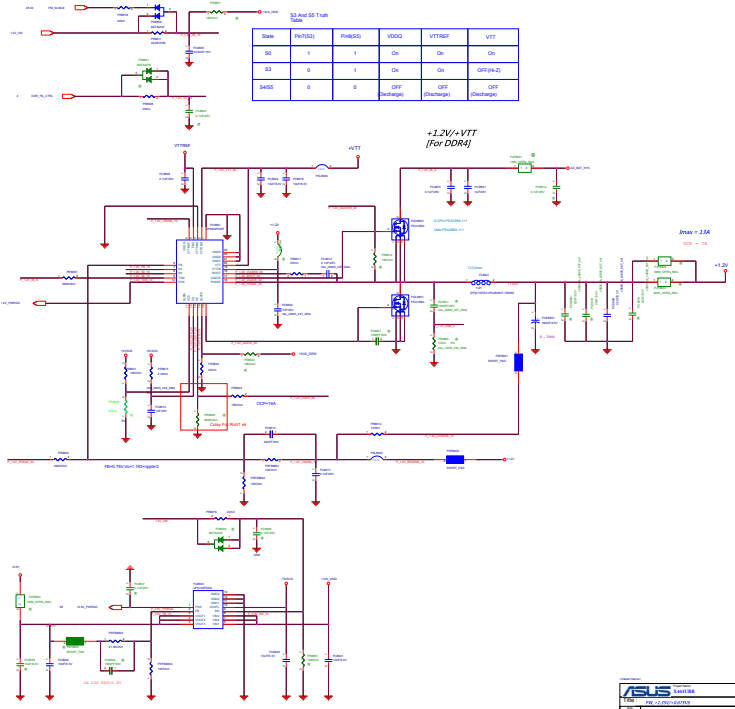
Title: PM_+1.0V/+1.2V/+2.5V			
Size:	Date: Last Issue Date:	Engineer:	
Sheet: Sheet1 of Sheet1			



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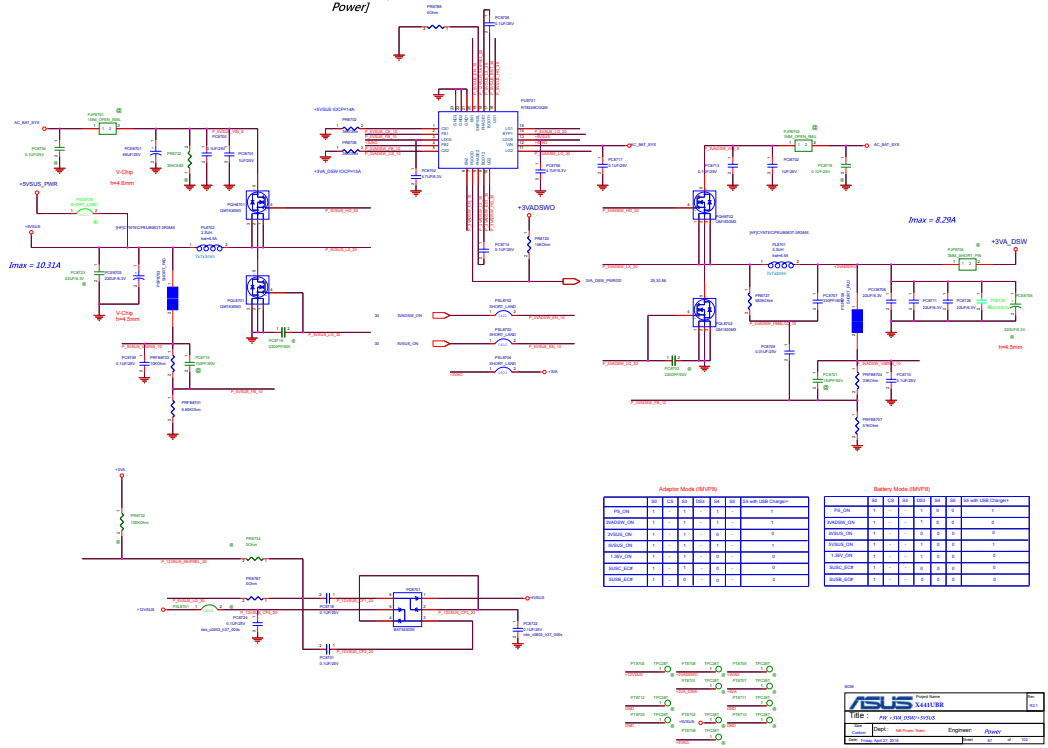
Date: 2024-08-29					


+3VA_DSW /
+5VSUS [System
Power]
Imax = 10.31A
Imax = 8.29A
V-Chip
h=4.6mm
V-Chip
h=4.5mm
h=4.5mm
+5VSUS_PWR
+3VA_DSW
+3VADSWO
AC_BAT_SYS
+3VA
+5VSUS
Adaptor Mode (M/VP8)
Battery Mode (M/VP8)
PS_ON
3VADSW_ON
3VSUS_ON
5VSUS_ON
1.05V_ON
SUSC_EC#
SUSB_EC#
S0 with USB Charger+
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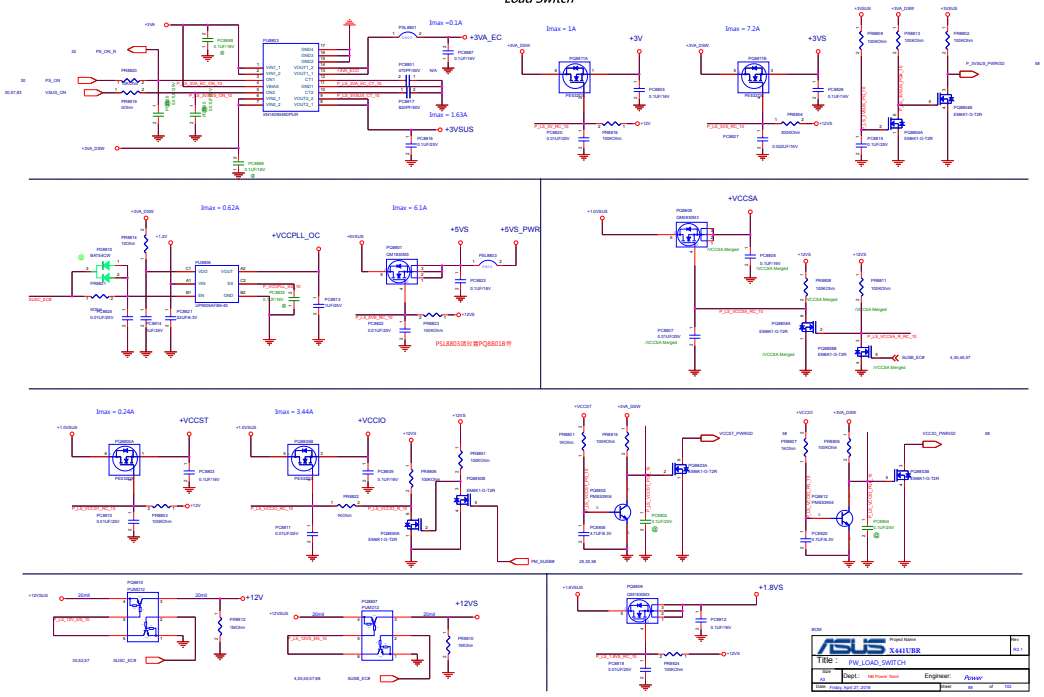
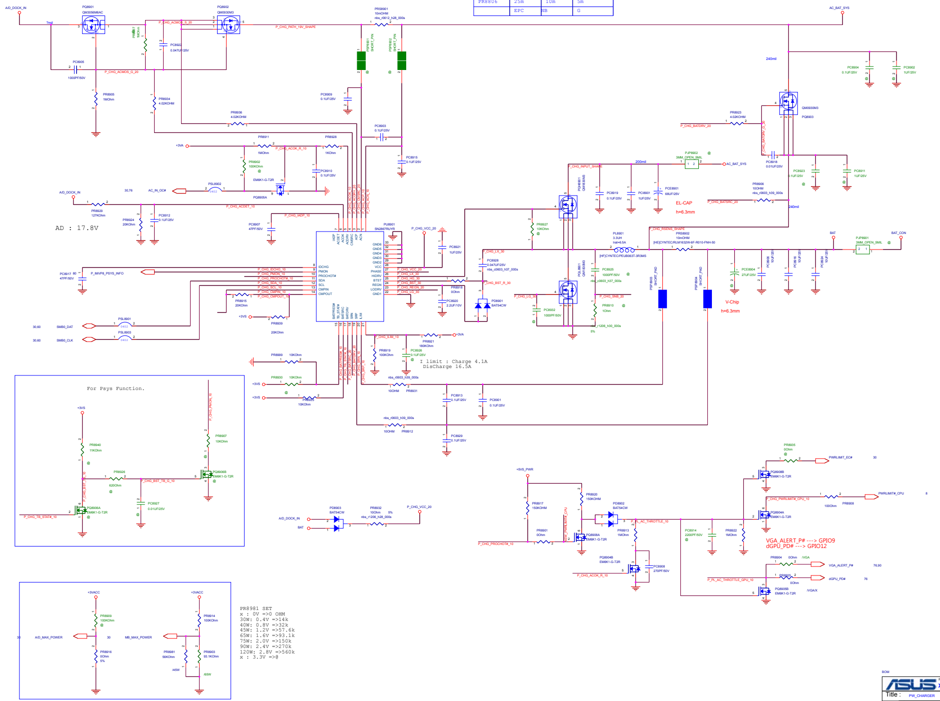
X441UBR
Title :
PW_+3VA_DSW/+5VSUS
Engineer:
Power
Date:
Friday, April 27, 2018

Load Switch


Imax =0.1A
+3VA_EC
Imax = 1A
+3V
Imax = 7.2A
+3VS
Imax = 1.63A
+3VSUS
Imax = 0.62A
+VCCPLL_OC
Imax = 6.1A
+5VS
+5VS_PWR
+VCCSA
Imax = 0.24A
+VCCST
Imax = 3.44A
+VCCIO
+12V
+12VS
+1.8VS
PSL88031放置PQ88018开
X441UBR
PW_LOAD_SWITCH
Power

	<=40W	<=120W	>=120W
PR8806	25m	10m	5m
	EPC	NB	G



BOM

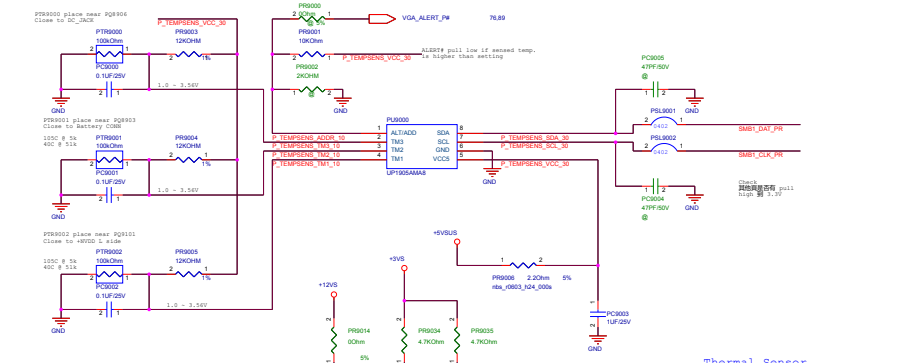
ASUS	Project Name X441UBR		Rev R2.1
Title : PW_CHARGER			
Size A2	Dept.: NB Power Team	Engineer: Power	
Date: Friday, April 27, 2018		Sheet 89 of 102	

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	5.6k	2.7k	2k

Register Address

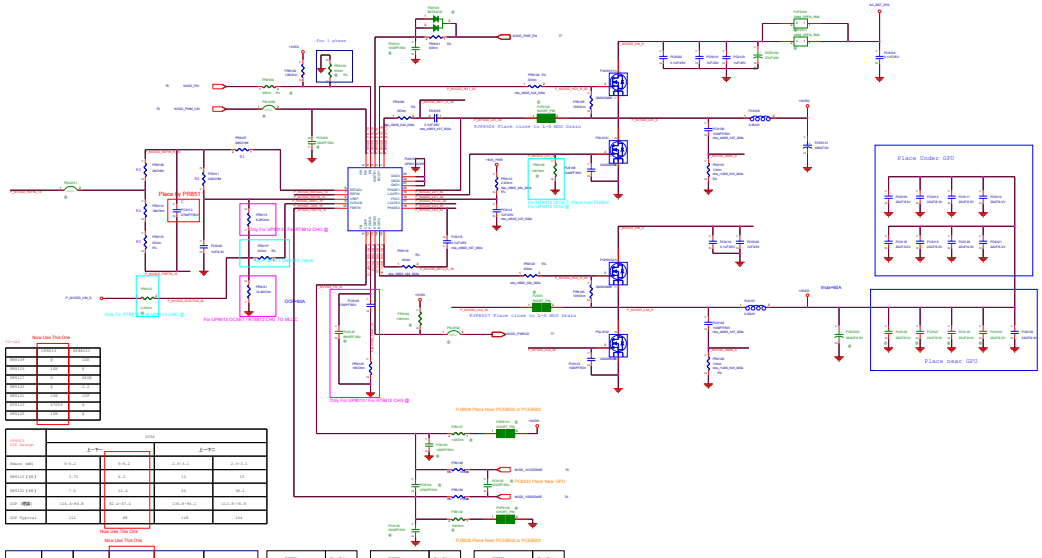
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



Thermal Sensor

<Variant Name>

ASUS	Project Name: X441UBR	Rev: R2.1
Title : PW_PROTECTION		
Size: A4	Dept.: NB Power Team	Engineer: Power
Date: Friday, April 27, 2018	Sheet 90 of 102	



Now Use This One

	Vendor1	Vendor2
3V/5V	N	ASE
3V/5V	ASE	N
3V/5V	N	ASE
3V/5V	N	ASE
3V/5V	ASE	N
3V/5V	ASE	N
3V/5V	ASE	N

	Vendor1		Vendor2	
	上一代		上一代C	
Volume (uM)	0.6.2	0.6.2	2.0.0.1	2.0.0.1
铜厚(1/0z)	0.7z	0.2	10	10
铜厚(1/0z)	1.1	11.4	20	20.1
孔径 (mil)	116.2~64.8	92.4~67.4	136.8~96.1	112.8~76.4
孔径 Typical	112	80	128	104

Now Use This One

Now Use This One

	Units	Config A	Config B	Config C	Config D
VBOOT	V	0.975	0.9	0.9	1.029
VBAT	V	1.2	1.2	1.13	1.15
VBIAS	V	0.6	0.6	0.63	0.9
PR9127	Kohm	39	20	39	27
PR9111	Kohm	39	20	20	7.5
PR9128	Kohm	1.5	2	1	0
PR9114	Kohm	33	18	16	6.2
PR9113	Kohm	1.5	0	0	1.74
PCH113	uF	1.5	2.7	1.8	5.6

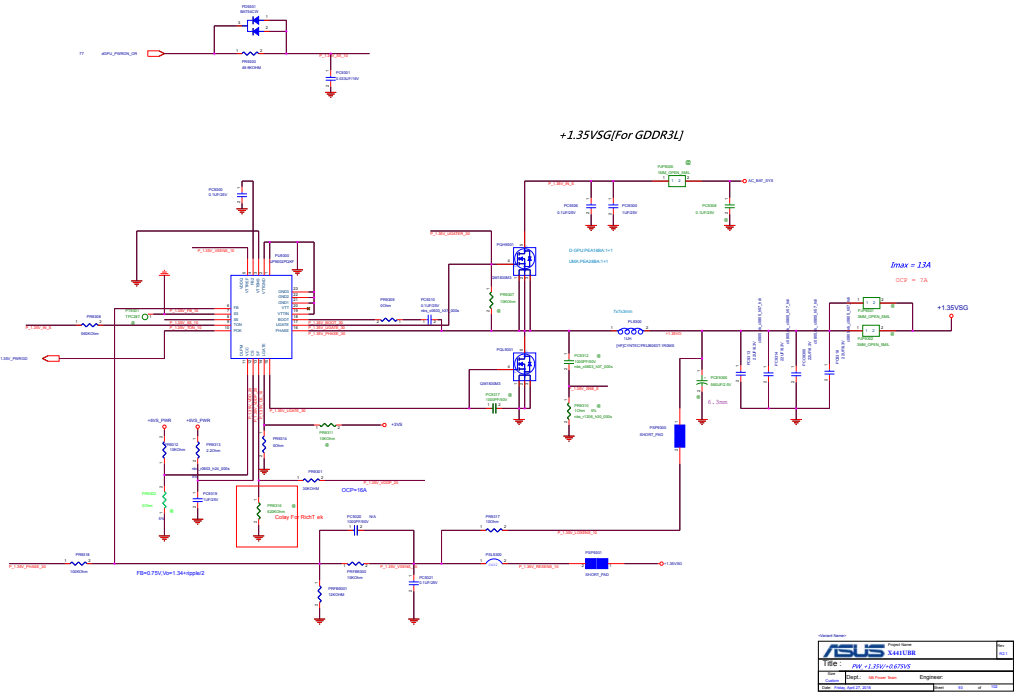
DDR3	Config
511-00-DE	C
511-00-LE	B
511-00-DL	C
511-00-GS	B
511-00-GT	B
511-00-GU	B
511-00-GV	B
511-00-LF	B
511-00-GW	B
511-00-GY	B

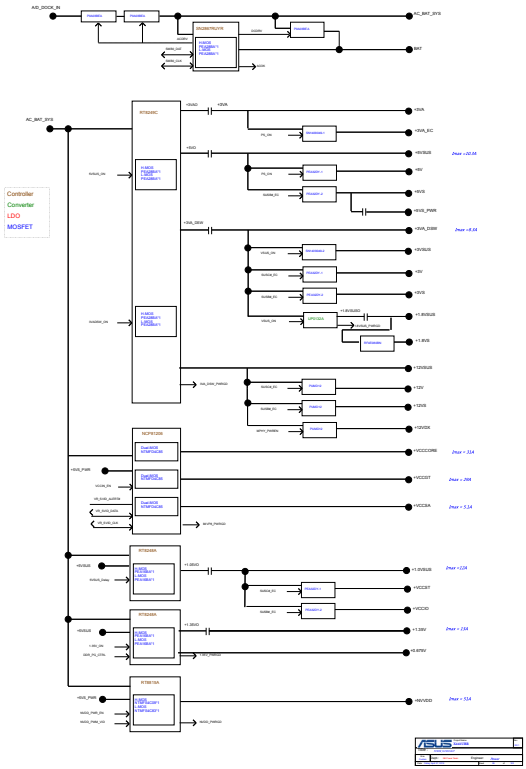
DDR3	Config
511-00-GZ	C
511-00-GA	C
511-00-GB	B
511-00-GC	B
511-00-GD	B
511-00-GE	B
511-00-GG	B
511-00-GH	A
511-00-GJ	A

DDR3	Config
511-00-GK	B
511-00-GR	B
511-00-GT	B
	B
511-00-GU	B
511-00-GV	B
511-00-GW	A
511-00-GX	A

Now Use This One

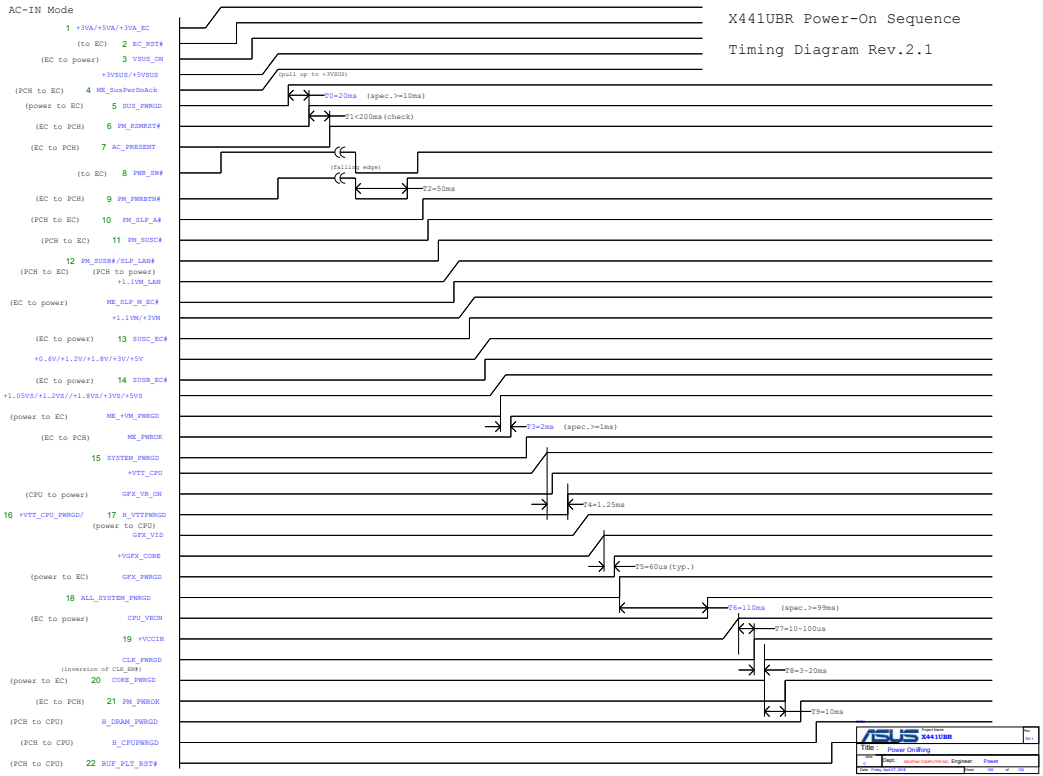
Title :	NVDD
Engineer:	Hunt_Zhang
Size:	Document Number: 2041[illegible]
Date:	Sheet of


+1.35VSG[For GDDR3L]
Imax = 13A
OCP = 7A
+1.35VSG
OCP=16A
Coley For Rich? ok
FB=0.75V,Vo=1.34+ripple2
ASUS
X441UBR
PW +1.25V+0.675VS
Engineer:


AIO_DOCK_IN
AC_BAT_SYS
BAT
Controller
Converter
LDO
MOSFET
+5VALW
+3VALW
+1.8VSUS
+1.05VSUS
+1.2VSUS
+12VDC
+VCCCORE
+VCCSXT
+VCCSA
+VCCIO
+1.15V
+0.675V
+5VDUAL
+VDDQ
+1.2VDDQ

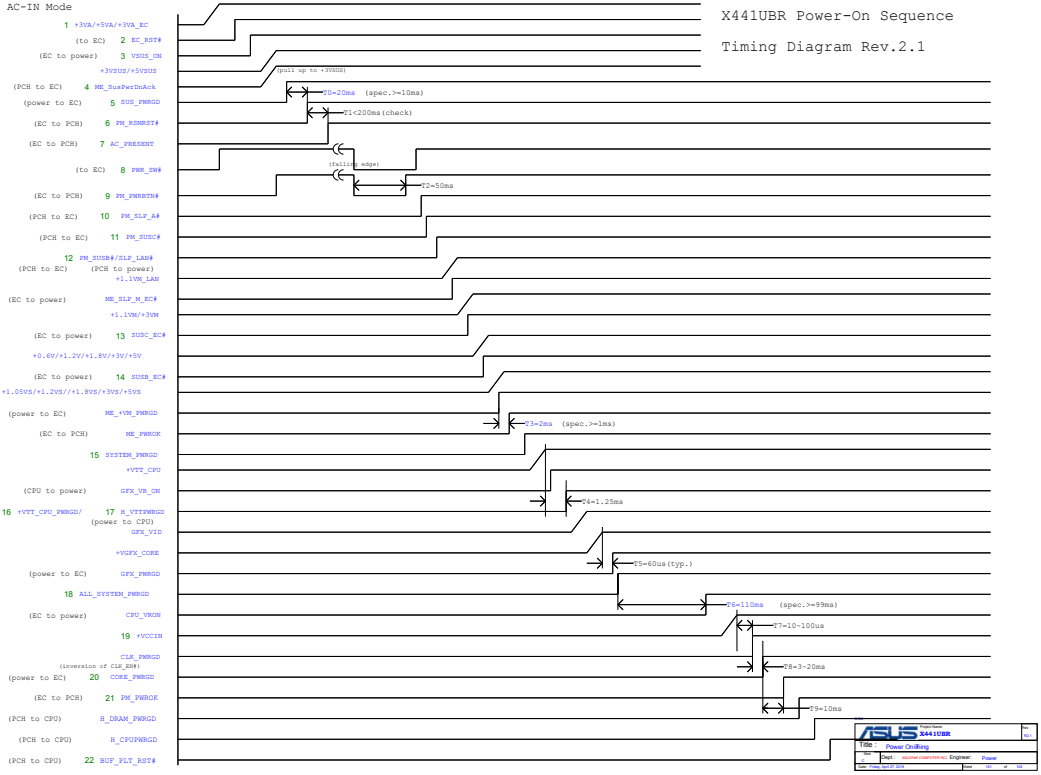
X441UBR Power-On Sequence

Timing Diagram Rev.2.1



X441UBR Power-On Sequence

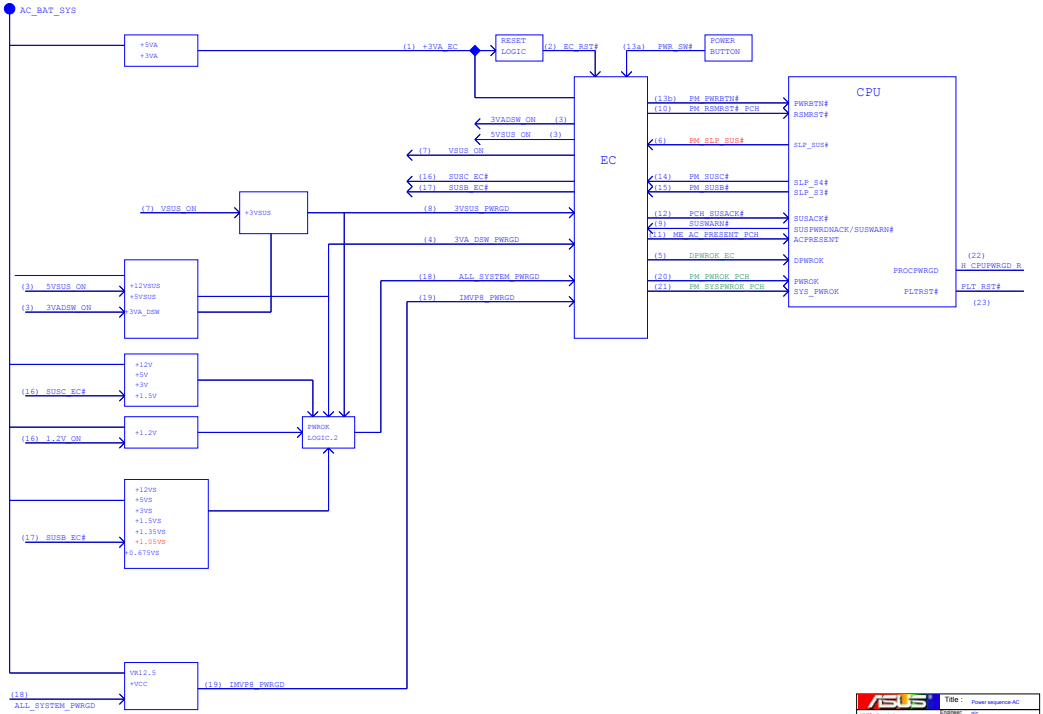
Timing Diagram Rev.2.1



ASUS	Project Name: X441UBR		Rev: 2.1
Title : Power On/Sling			
Size:	Project:	Document Number:	Engineer: Power
Date: Friday, April 25, 2014		Sheet: 50 of 100	

AC-IN Mode

X441UBR Power On Sequence Diagram



Title : Power sequence-AC

Engineer:

X441UBR