S0031

Version 1.1

CPU:

Intel Pineview-D Processor

System Chipset:

Intel ICH9R

On Board Chipset:

Clock Generator - REALTEK (RTM875T-605-VD-GR)
Giga LAN -- LAN1 - Intel 82574L
Giga LAN -- LAN2 - Intel 82567LM
SIO-Fintek F71882FG
USB 3.0 CTRL NEC uPD720200
Flash CTRL PHISON PS2251-33
BIOS -- SPI

Main Memory:

DDR III SO-DIMM x 2 (Max 4GB)

Intersil PWM:

Controller: ISL6314

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Size: Custom | Document Description: COVER SHEET | Rev: 1.1

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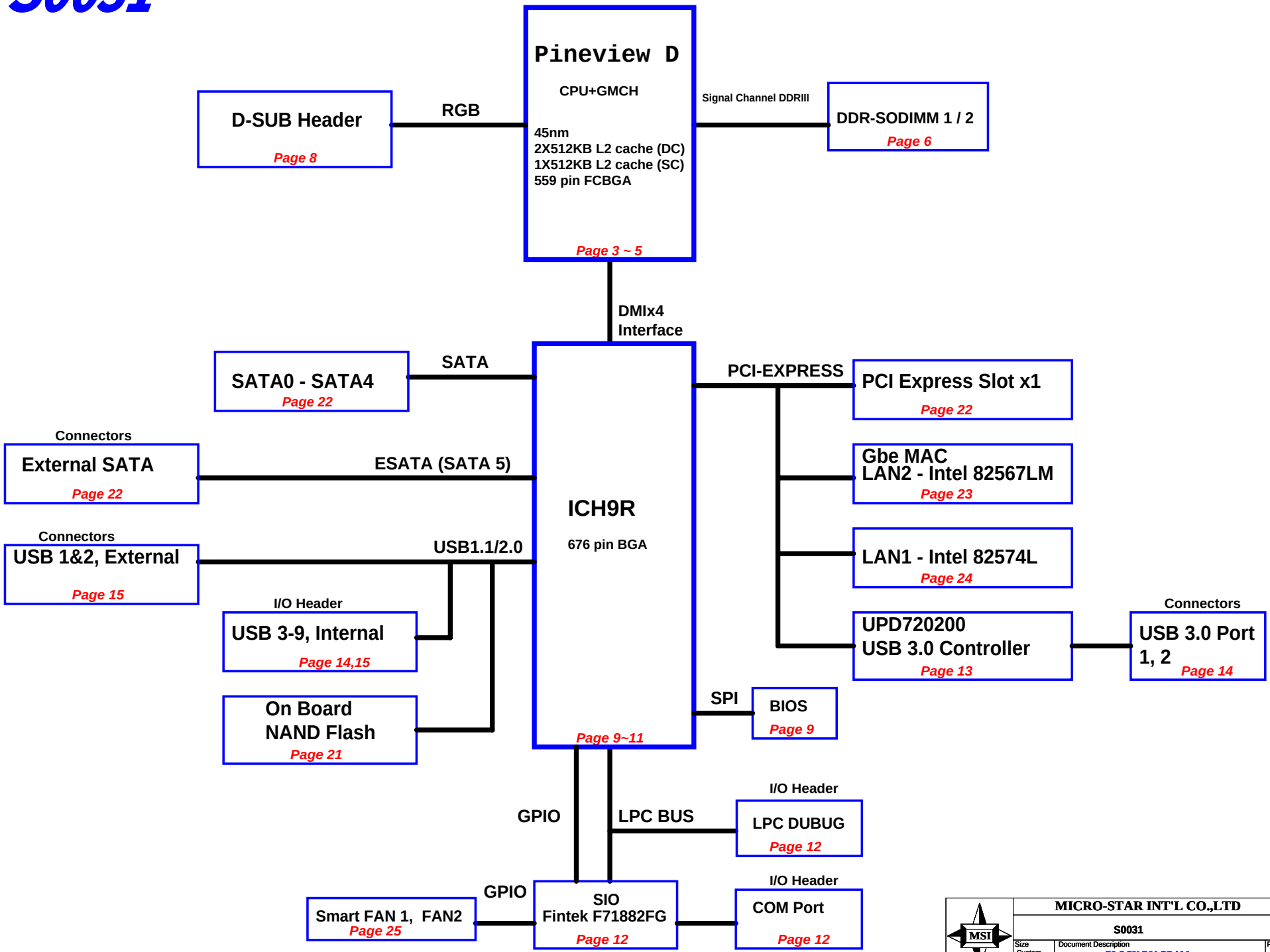
S0031



MSI	MICRO-STAR INT'L CO.,LTD	
	S0031	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.1
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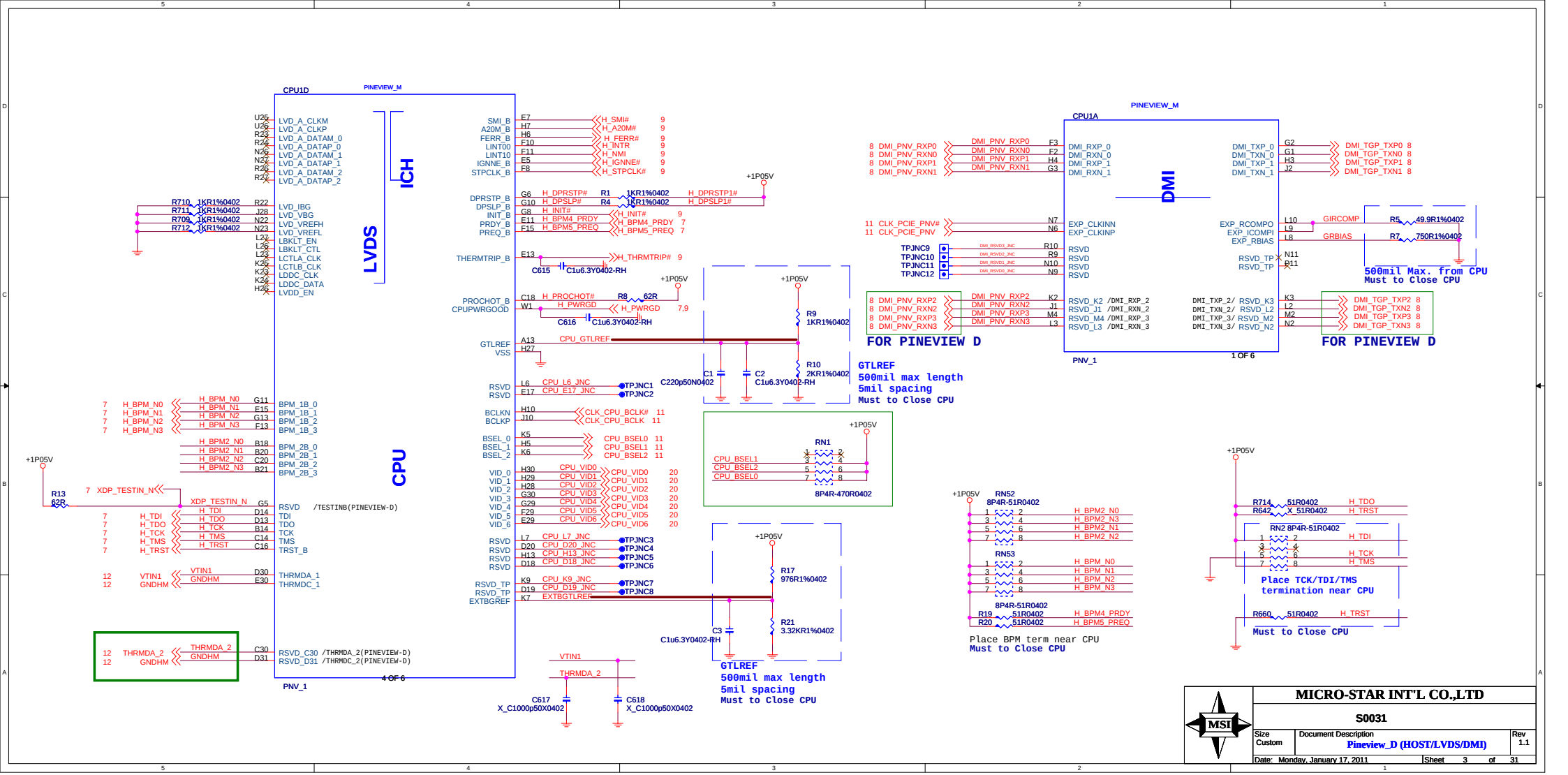
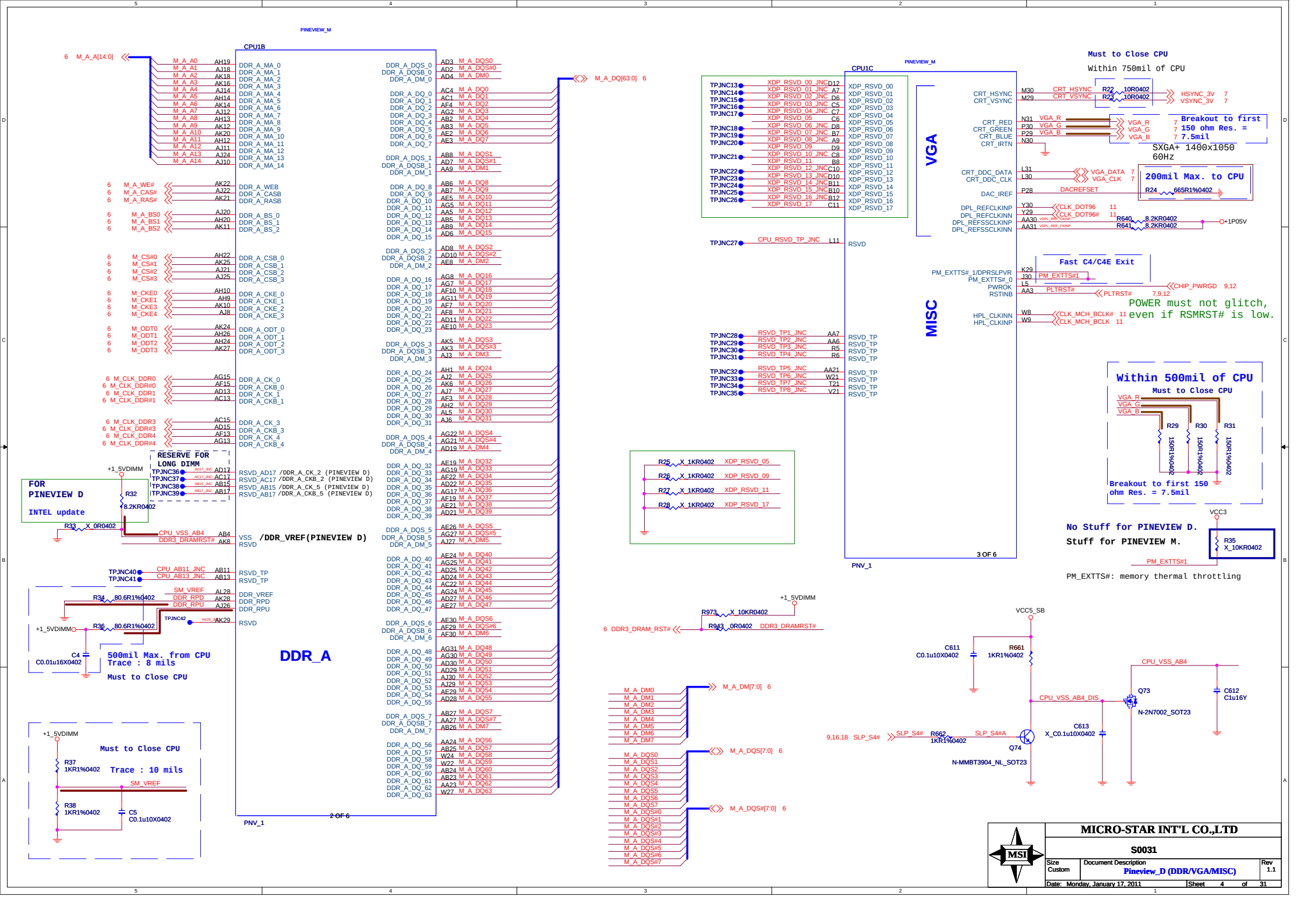


MICRO-STAR INT'L CO.,LTD

S0031

Size	Document Description	Rev
Custom	Pineview_D (HOST/LVDS/DMI)	1.1

Date: Monday, January 17, 2011 Sheet 3 of 31


PINEVIEW_M
CPU1B
DDR_A
2 OF 6
PNV_1
RESERVE FOR LONG DIMM
FOR PINEVIEW D
INTEL update
500mil Max. from CPU
Trace : 8 mils
Must to Close CPU
Must to Close CPU
Trace : 10 mils
CPU1C
VGA
MISC
3 OF 6
PNV_1
Must to Close CPU
Within 750mil of CPU
SXGA+ 1400x1050
60Hz
Breakout to first
150 ohm Res. =
7.5mil
200mil Max. to CPU
Fast C4/C4E Exit
POWER must not glitch,
even if RSMRST# is low.
Within 500mil of CPU
Must to Close CPU
Breakout to first 150
ohm Res. = 7.5mil
No Stuff for PINEVIEW D.
Stuff for PINEVIEW M.
PM_EXTTS#: memory thermal throttling
MICRO-STAR INT'L CO.,LTD
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Pineview_D (DDR/VGA/MISC)
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GFX_1.05V

Current Max 1.38A

sustained current, 1.05A

1.1V, 8.511A (C4 state,0.51A)

+1P05V=> 2.13A
+0_89VGFX=> 1.38A
+1_5VRUN=>0.08A
+1_8VDIMM=> 2.27A
+1_8VRUN=> 0.318A
+3VRUN=> 0.006A

CPU1E PINEVIEW_M

CPU1F PINEVIEW_M

GFX/MCH | CPU | DDR | POWER | EXPICRTIPLL | LVDS | DMI

1.8V, 2.27A

1.05V, 1.32A

1.5V, 0.08A

1.05V, 0.048A

1.05V, 0.33A

1.8V, 0.154A

1.8V, 0.06A

1.8V, 0.104A

3.3V, 0.006A

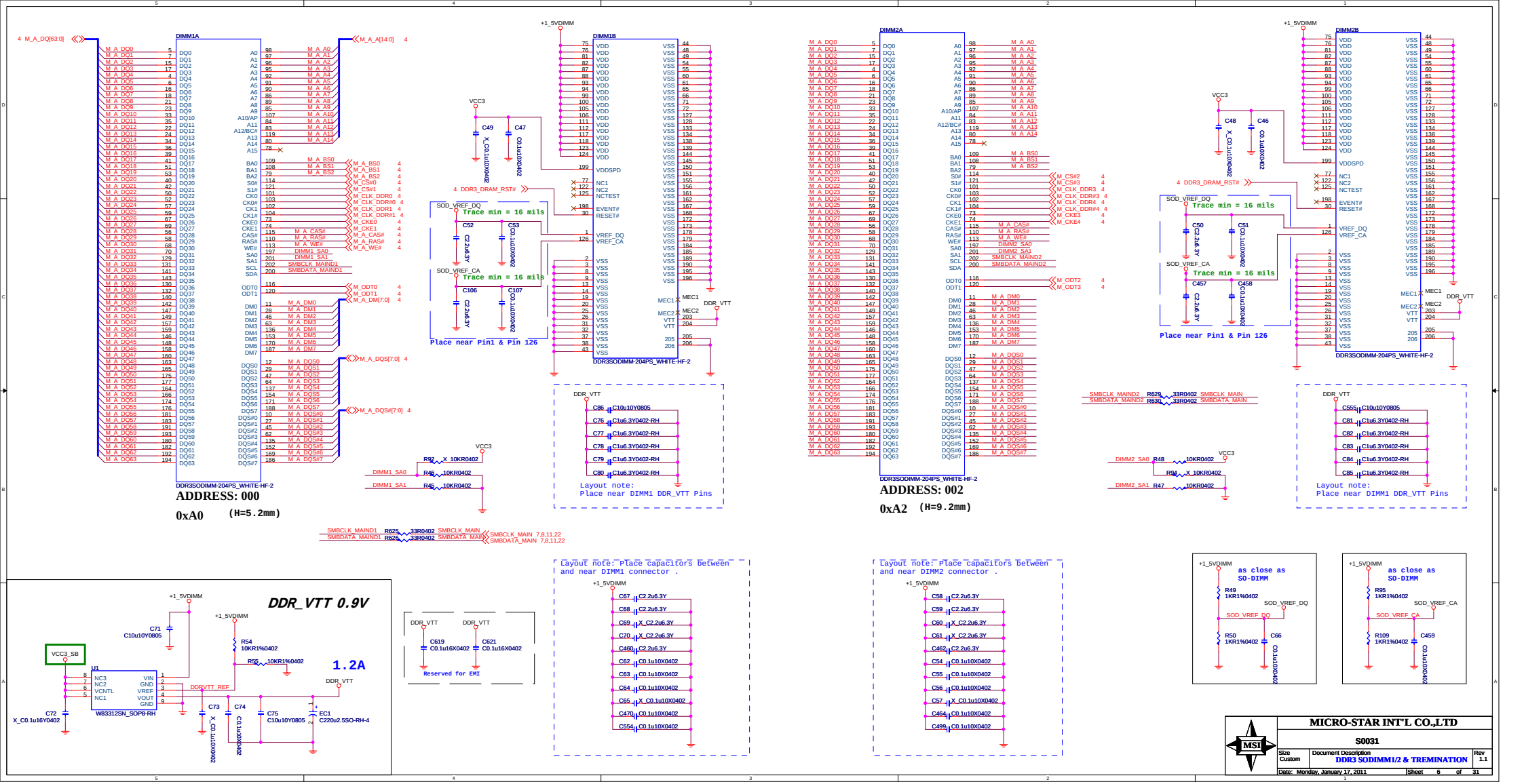
1.05V, 0.48A

Place CAP close to CPU

5 OF 6

6 OF 6

PNV_1



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S0031	
Size: Custom	Document Description: DDR3 SODIMM1/2 & TREMINATION
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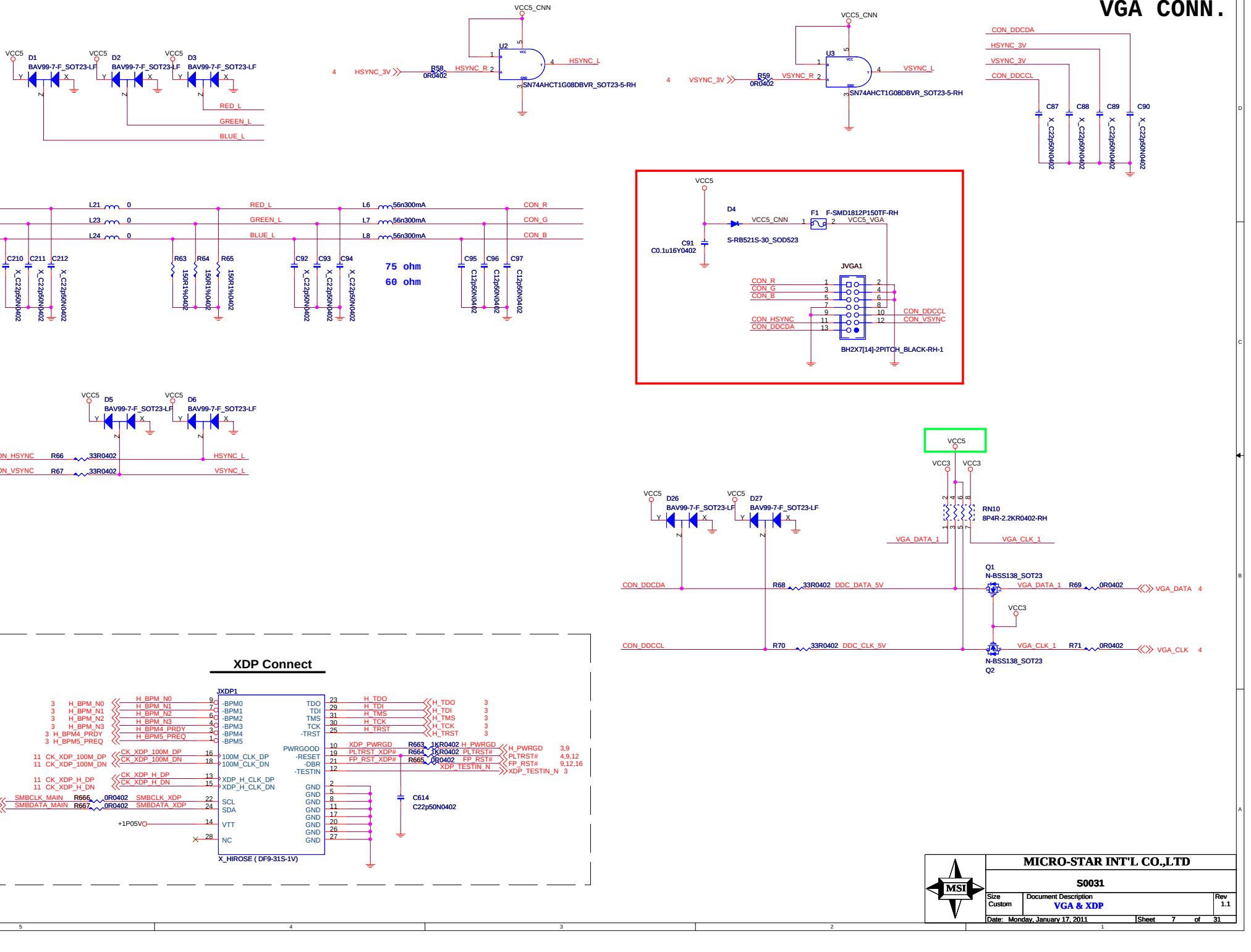
VGA CONN.



MICRO-STAR INT'L CO.,LTD	
S0031	
Size: Custom	Document Description: VGA & XDP
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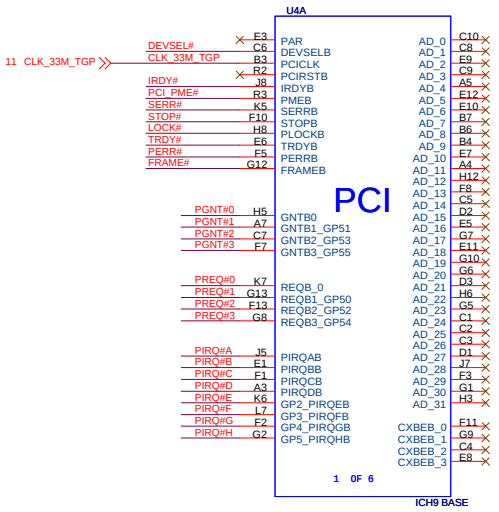
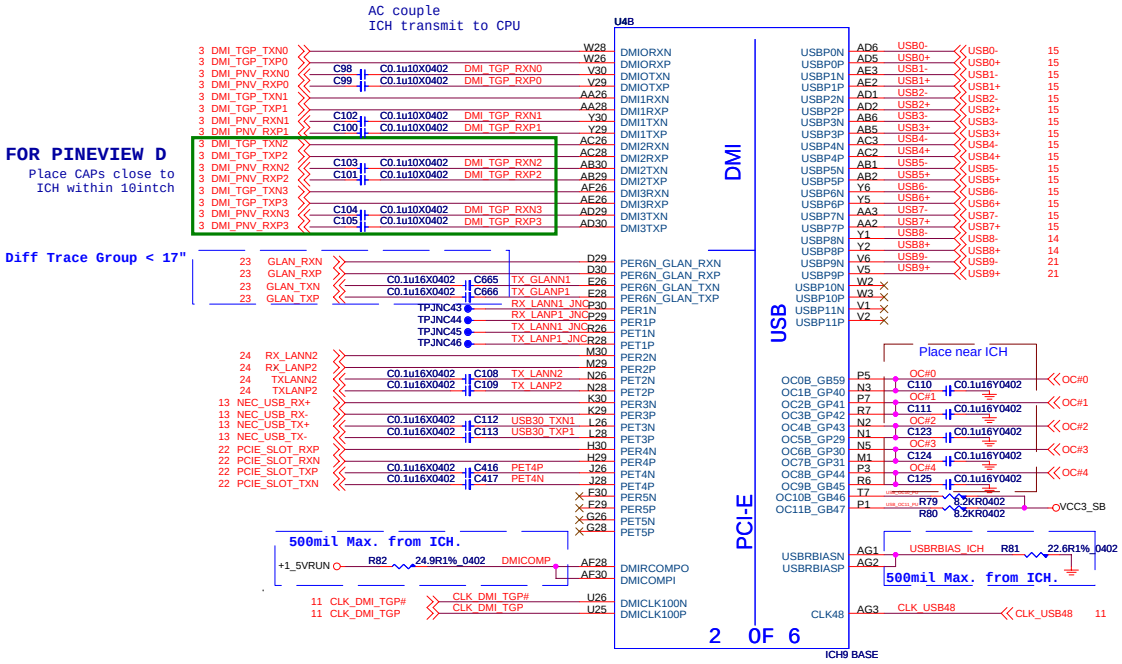
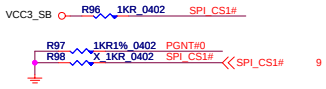




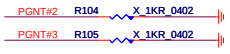
teknisi indonesia

SB STRAPPING RESISTOR



BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

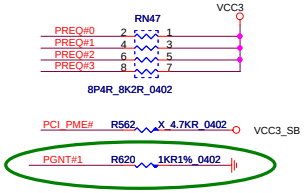
PGNT#[3:0]Internal Pull-up

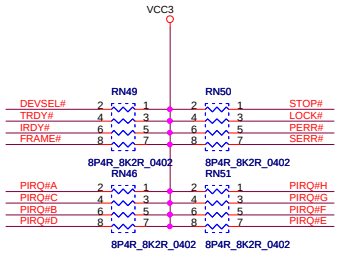


SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X

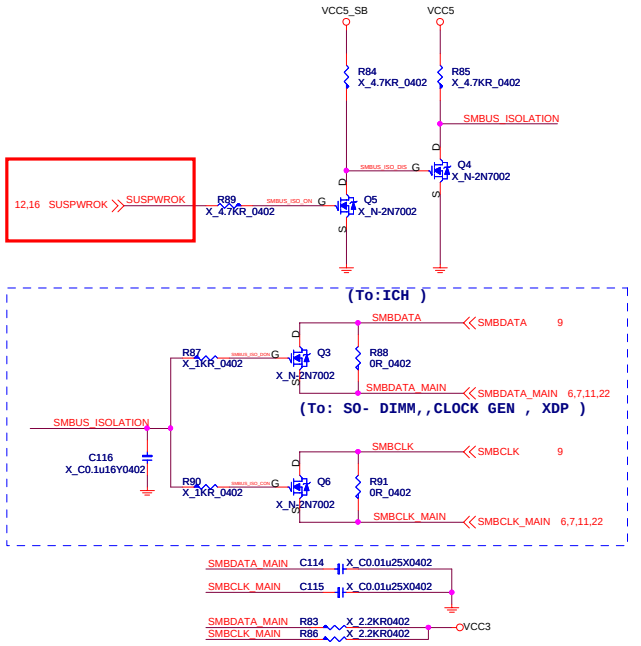
PCI PULL-UP / DOWN RESISTORS





ICH9R GPIO51 NEED TO PULL DOWN BY 1K-OHM TO STRAP ICH9R DMI INTO AC COUPLE MODE

SM BUS ISOLATION



MICRO-STAR INT'L CO.,LTD	
S0031	
Size: Custom	Document Description: ICH9_PCI,USB,DMI,TPM,EEPROM
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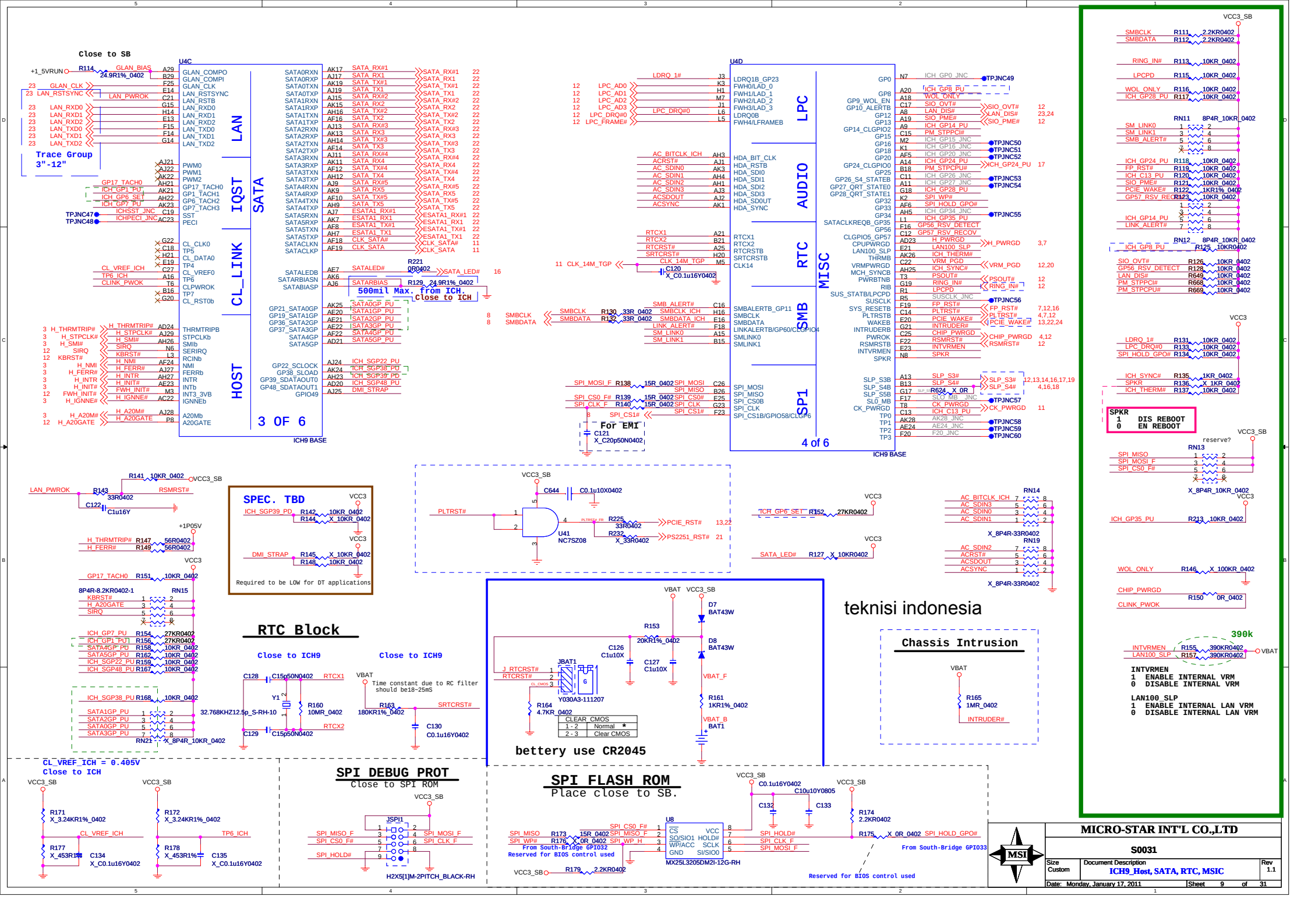
Close to SB
U4C
GLAN_COMPO
GLAN_COMPI
GLAN_CLK
LAN_RSTSYNC
LAN_RSTB
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN
PWM0
PWM1
PWM2
GP17_TACH0
GP1_TACH1
GP6_TACH2
GP7_TACH3
SST
PECI
IQST
CL_CLK0
TP5
CL_DATA0
TP4
CL_VREF0
TP6
CLPWROK
TP7
CL_RST0b
CL_LINK
THRMTRIPB
STPCLKb
SMIb
SERIRQ
RCINb
NMI
FERRb
INTR
INTb
INT3_3VB
IGNNEb
A20Mb
A20GATE
HOST
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATACLKN
SATACLKP
SATA
SATALEDB
SATARBIASN
SATABIASP
SATA0GP_PU
SATA1GP_PU
SATA2GP_PU
SATA3GP_PU
SATA4GP_PU
SATA5GP_PU
GP21_SATA0GP
GP19_SATA1GP
GP36_SATA2GP
GP37_SATA3GP
SATA4GP
SATA5GP
GP22_SCLOCK
GP38_SLOAD
GP39_SDATAOUT0
GP48_SDATAOUT1
GPIO49
3 OF 6
ICH9 BASE
Trace Group 3"-12"
500mil Max. from ICH.
Close to ICH
U4D
LDRQ1B_GP23
FWH0/LAD_0
FWH1/LAD_1
FWH2/LAD_2
FWH3/LAD_3
LDRQ0B
FWH4/LFRAMEB
LPC
HDA_BIT_CLK
HDA_RSTB
HDA_SDI0
HDA_SDI1
HDA_SDI2
HDA_SDI3
HDA_SD0UT
HDA_SYNC
AUDIO
RTCX1
RTCX2
RTCRST#
SRTCRSTB
CLK14
RTC
GP0
GP8
GP9_WOL_EN
GP10_ALERTB
GP12
GP13
GP14_CLGPIO2
GP15
GP16
GP18
GP20
GP24_CLGPIO0
GP25
GP26_S4_STATEB
GP27_QRT_STATE0
GP28_QRT_STATE1
GP32
GP33
GP34
SATACLKREQB_GP35
GP56
CLGPIO5_GP57
CPUPWRGD
LAN100_SLP
THRMB
VRMPWRGD
MCH_SYNCB
PWRBTNB
RIB
SUS_STATB/LPCPD
SUSCLK
SYS_RESETB
PLTRSTB
WAKEB
INTRUDERB
PWROK
RSMRSTB
INTVRMEN
SPKR
MISC
SMB_ALERT#
SMBALERTB_GP11
SMBCLK
SMBDATA
LINKALERTB/GP60/CLGPIO4
SMLINK0
SMLINK1
SMB
SPI_MOSI
SPI_MISO
SPI_CS0B
SPI_CLK
SPI_CS1B/GPIO58/CLGP6
SPI1
4 of 6
ICH9 BASE
SPI_MOSI_F R138 15R_0402
SPI_CS0_F# R139 15R_0402
SPI_CLK_F R140 15R_0402
For EMI
C121 X_C20p50N0402
R221 0R0402
C120 X_C0.1u16Y0402
R129 24.9R1%_0402
R130 33R_0402
R132 33R_0402
R141 10KR_0402
R143 33R0402
C122 C1u16Y
R147 56R0402
R149 56R0402
R151 10KR_0402
8P4R-8.2KR0402-1 RN15
R154 27KR0402
R156 27KR0402
R158 10KR_0402
R162 10KR_0402
R159 10KR_0402
R167 10KR_0402
R168 10KR_0402
SATA1GP_PU
SATA2GP_PU
SATA0GP_PU
SATA3GP_PU
RN21 X_8P4R_10KR_0402
SPEC. TBD
R142 10KR_0402
R144 X_10KR_0402
R145 X_10KR_0402
R148 10KR_0402
Required to be LOW for DT applications
RTC Block
Close to ICH9
C128 C15p50N0402
C129 C15p50N0402
Y1
32.768KHZ12.5p_S-RH-10
R160 10MR_0402
R163 180KR1%_0402
C130 C0.1u16Y0402
Time constant due to RC filter should be18~25mS
C644 C0.1u10X0402
U41 NC7SZ08
R225 33R0402
R232 X_33R0402
PLTRST#
PCIE_RST#
PS2251_RST#
R152 27KR0402
R127 X_10KR0402
RN14
X_8P4R-33R0402
RN19
X_8P4R-33R0402
D7 BAT43W
D8 BAT43W
R153 20KR1%_0402
C126 C1u10X
C127 C1u10X
JBAT1
Y030A3-111207
R164 4.7KR_0402
R161 1KR1%_0402
CLEAR_CMOS
Normal
Clear CMOS
bettery use CR2045
teknisi indonesia
Chassis Intrusion
R165 1MR_0402
INTRUDER#
CL_VREF_ICH = 0.405V
Close to ICH
R171 X_3.24KR1%_0402
R172 X_3.24KR1%_0402
R177 X_453R1%
R178 X_453R1%
C134 X_C0.1u16Y0402
C135 X_C0.1u16Y0402
SPI DEBUG PROT
Close to SPI ROM
JSPI1
H2X5[1]M-2PITCH_BLACK-RH
SPI FLASH ROM
Place close to SB.
U8
MX25L3205DM2I-12G-RH
C0.1u16Y0402
C10u10Y0805
C132
C133
R174 2.2KR0402
R175 X_0R_0402
R173 15R_0402
R176 X_0R_0402
R179 2.2KR0402
From South-Bridge GPI032
From South-Bridge GPI033
Reserved for BIOS control used
SMBCLK R111 2.2KR0402
SMBDATA R112 2.2KR0402
RING_IN# R113 10KR_0402
LPCPD R115 10KR_0402
WOL_ONLY R116 10KR_0402
ICH_GP28_PU R117 10KR_0402
RN11 8P4R_10KR_0402
ICH_GP24_PU R118 10KR_0402
FP_RST# R119 10KR_0402
ICH_C13_PU R120 10KR_0402
SIO_PME# R121 10KR_0402
PCIE_WAKE# R122 1KR1%_0402
GP57_RSV_RECOV R123 10KR_0402
ICH_GP14_PU R124 10KR_0402
LINK_ALERT# R125 10KR_0402
RN12 8P4R_10KR_0402
ICH_GP8_PU R125 10KR0402
SIO_OVT# R126 10KR_0402
GP56_RSV_DETECT R128 10KR_0402
LAN_DIS# R649 10KR_0402
PM_STPPCI# R668 10KR_0402
PM_STPCPU# R669 10KR_0402
LDRQ_1# R131 10KR_0402
LPC_DRQ#0 R133 10KR_0402
SPI_HOLD_GPO# R134 10KR_0402
ICH_SYNC# R135 1KR_0402
SPKR R136 X_1KR_0402
ICH_THERM# R137 10KR_0402
SPKR
1 DIS REBOOT
0 EN REBOOT
RN13 X_8P4R_10KR_0402
ICH_GP35_PU R213 10KR_0402
WOL_ONLY R146 X_100KR_0402
CHIP_PWRGD R150 0R_0402
CLINK_PWOK
390k
INTVRMEN R155 390KR0402
LAN100_SLP R157 390KR0402
INTVRMEN
1 ENABLE INTERNAL VRM
0 DISABLE INTERNAL VRM
LAN100_SLP
1 ENABLE INTERNAL LAN VRM
0 DISABLE INTERNAL LAN VRM
MICRO-STAR INT'L CO.,LTD
S0031
Size Custom
Document Description ICH9_Host, SATA, RTC, MSIC
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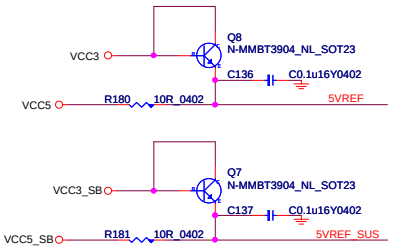
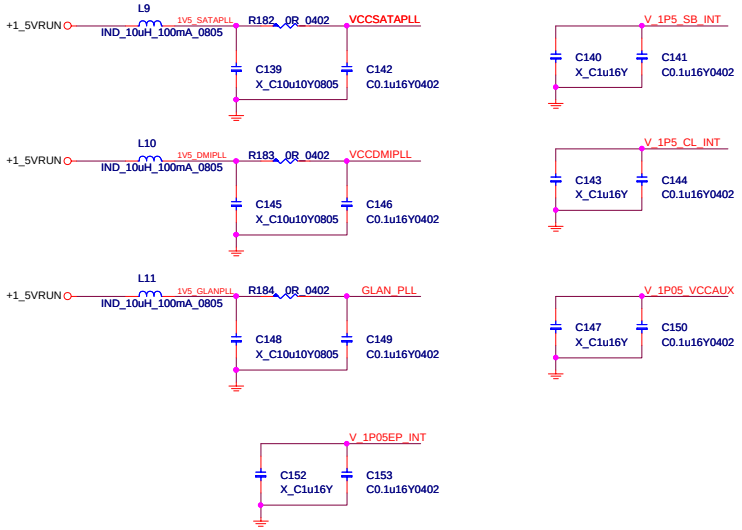
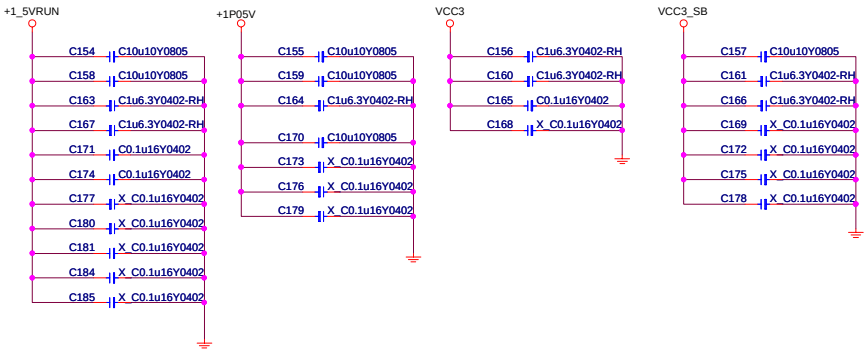
5VREF & 5VREF_SUS Sequencing Circuit

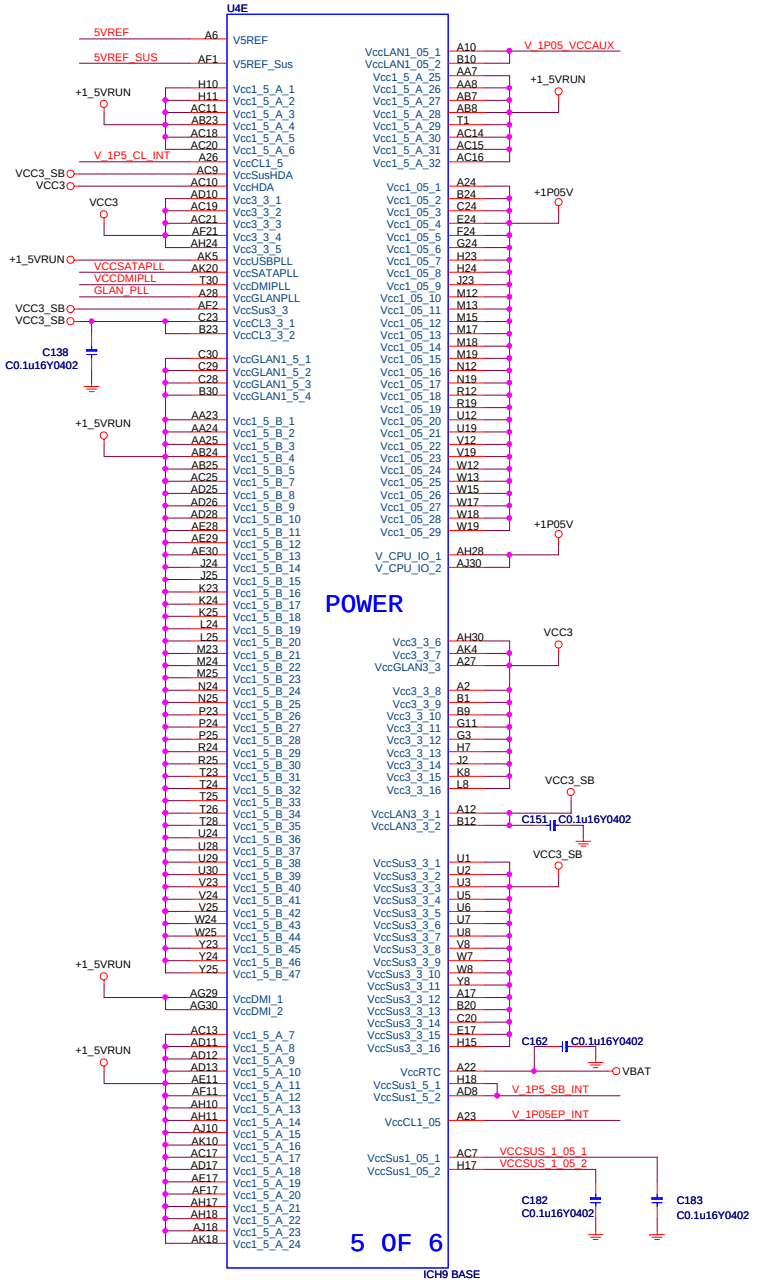
V5REF must be powered up before VCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.

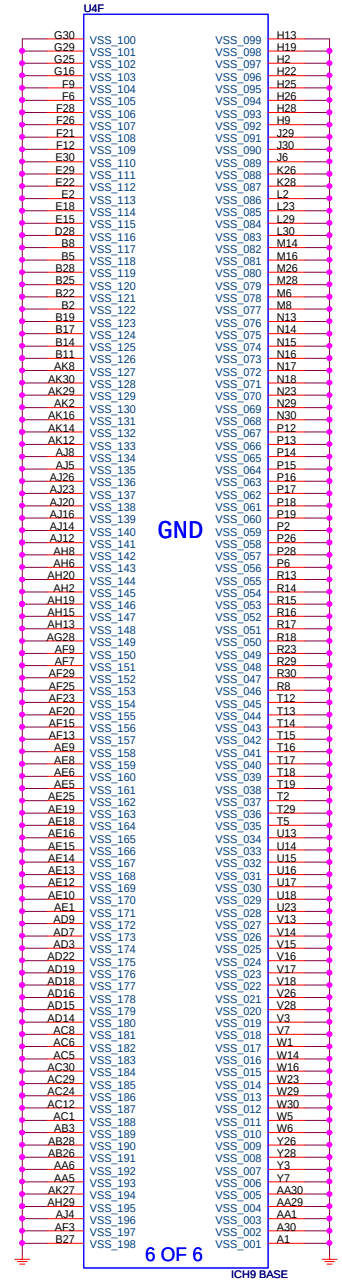


SB POWER









AC7, H17 & H18, AD8
For VccSus1_5 spec TBD

MICRO-STAR INT'L CO.,LTD		
S0031		
Size: Custom	Document Description: ICH9_Power, GND	Rev: 1.1
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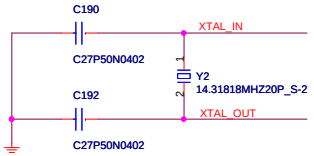
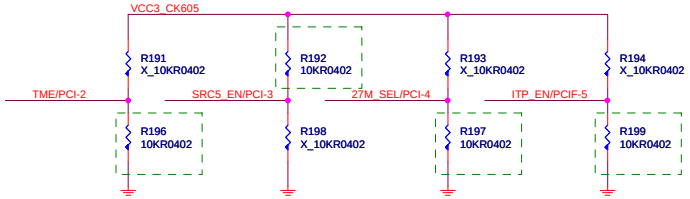
CLK Gen REALTEK/RTM875T-605

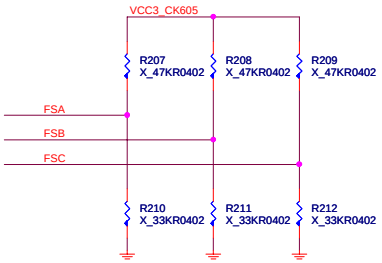


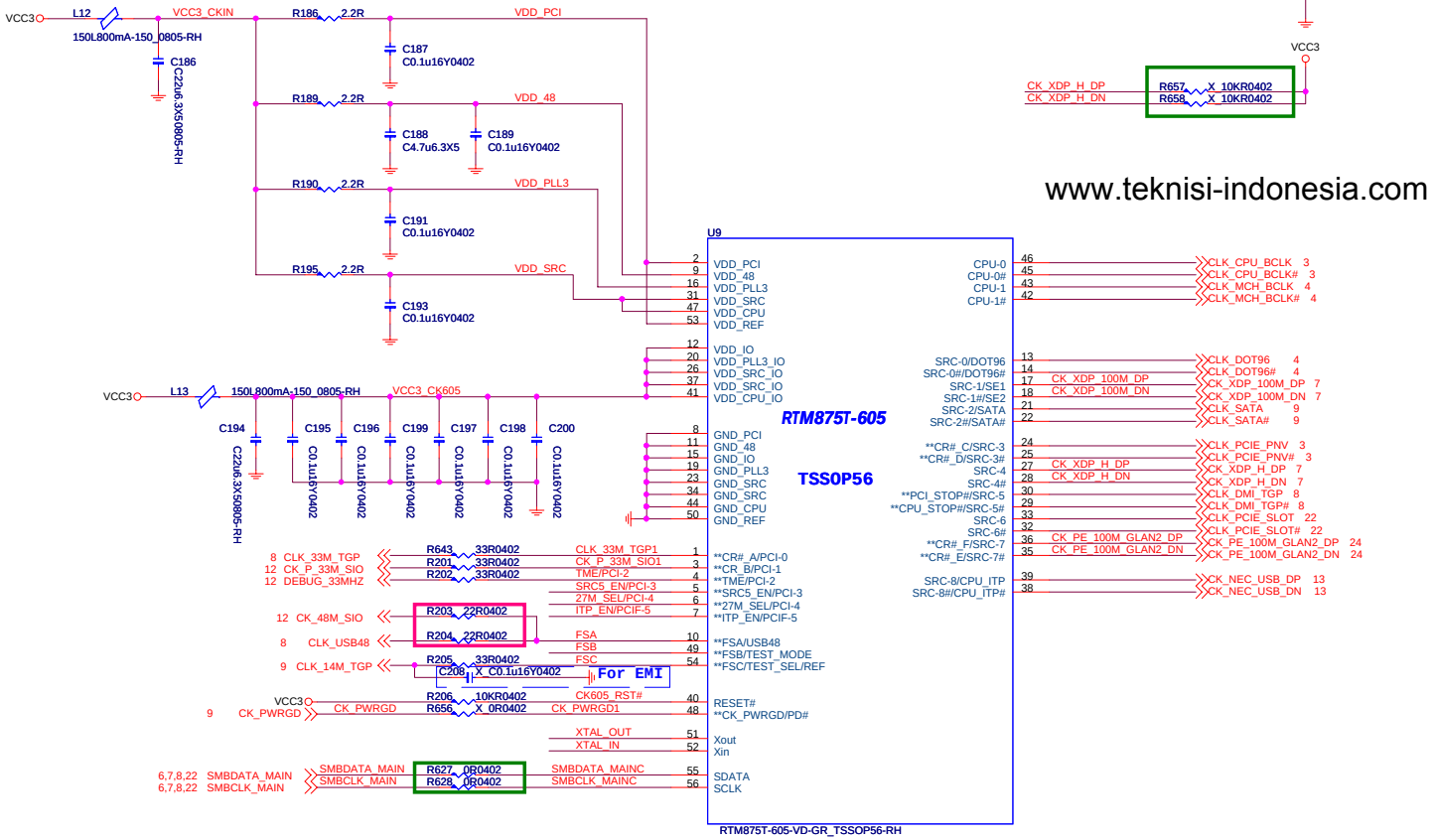


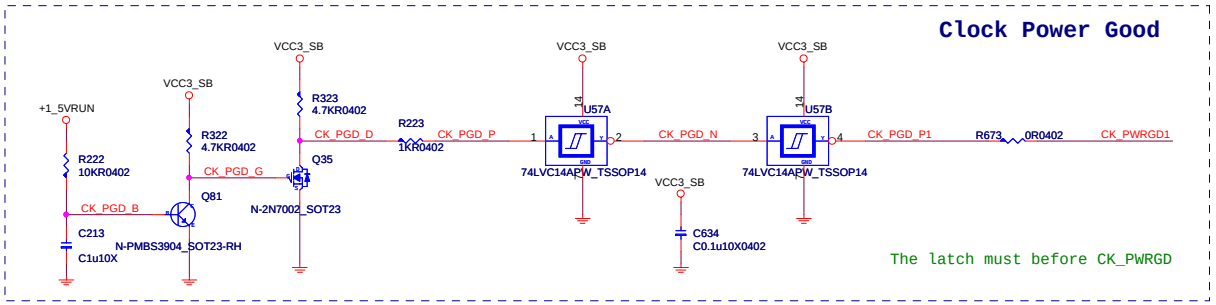
	PULL High	PULL Low
TME/PCI-2	NO OVERCLOCKING	NORMAL RUN
SRC5_EN/PCI-3	Pin29/30 IS SRC5	Pin29/30 IS CPU_STOP#/ PCI_STOP#
27M_SEL/PCI-4	Pin17/18 IS 27MHz	Pin17/18 IS DOT96/DOT96#
ITP_EN/PCIF-5	Pin38/39 IS CPU_ITP	Pin38/39 IS SRC8

CPU Table

FSC	FSB	FSA	BCLK
L	H	H	166MHZ
L	H	L	200MHZ
H	H	H	200MHZ







MSI	MICRO-STAR INT'L CO.,LTD		
	S0031		
Size: Custom	Document Description: ICLK GEN] REALTEK/RTM875T		Rev: 1.1
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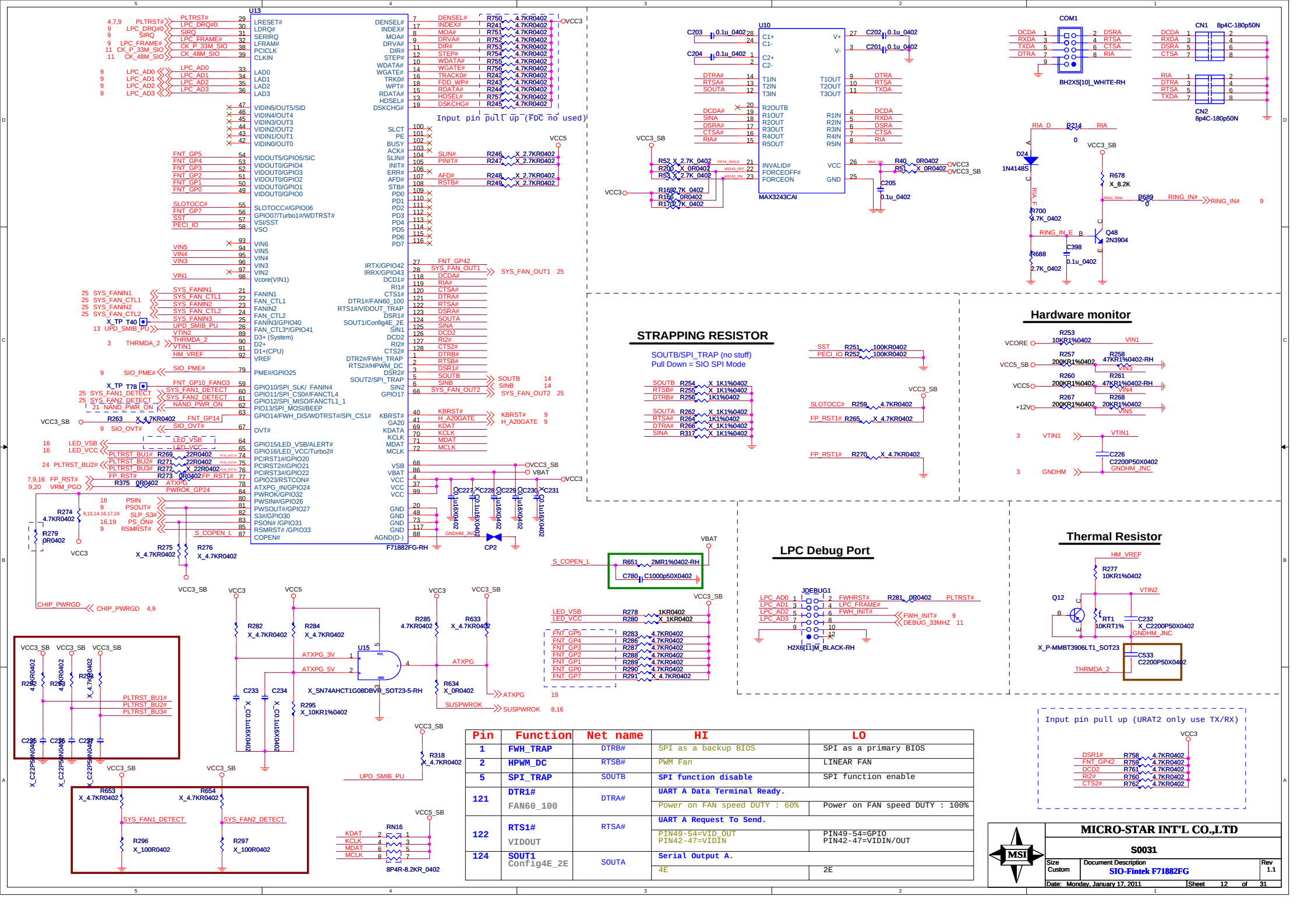
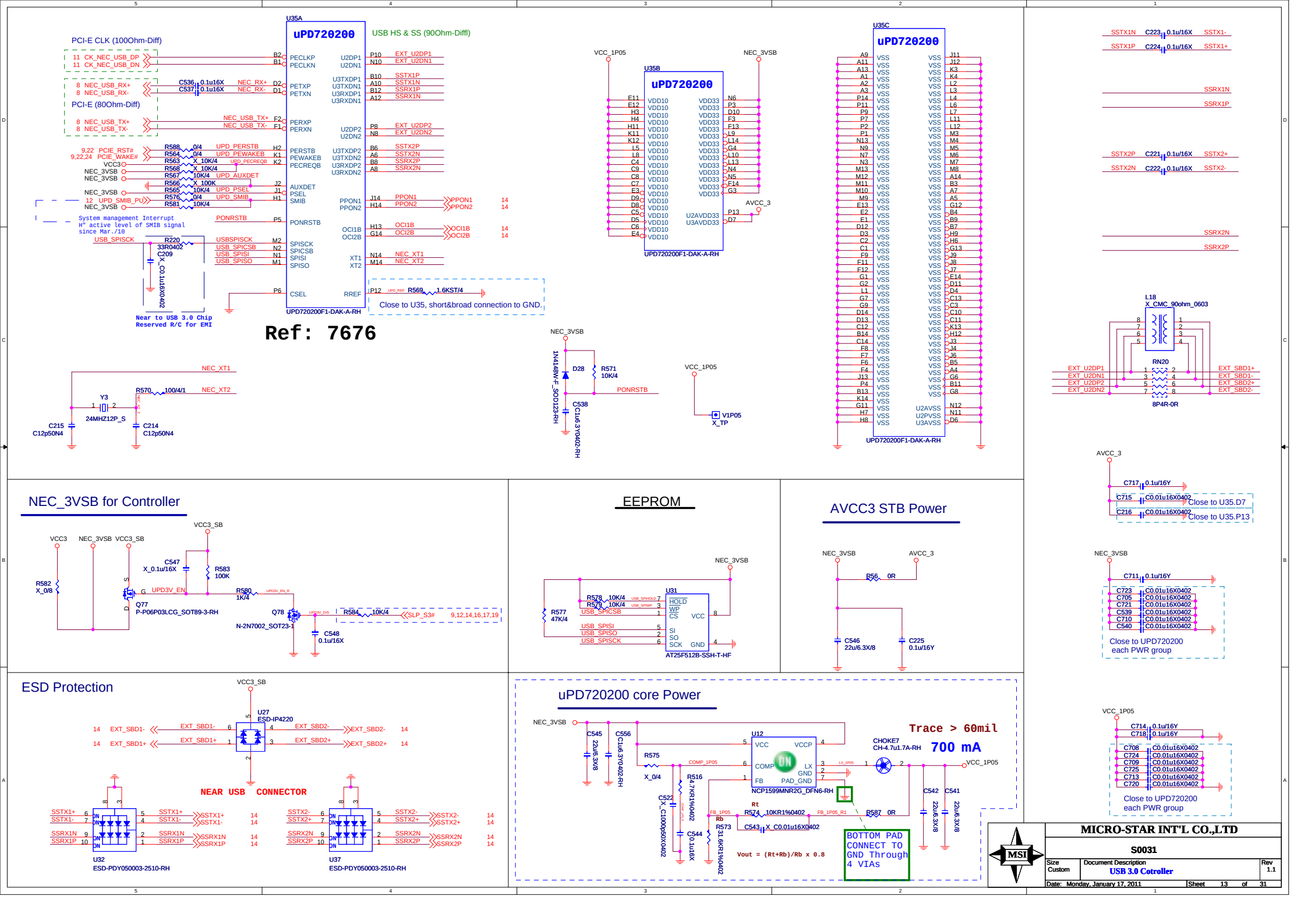


Pin	Function	Net name	HI	LO
1	FWH_TRAP	DTRB#	SPI as a backup BIOS	SPI as a primary BIOS
2	HPWM_DC	RTSB#	PWM Fan	LINEAR FAN
5	SPI_TRAP	SOUTB	SPI function disable	SPI function enable
121	DTR1# FAN60_100	DTRA#	UART A Data Terminal Ready. Power on FAN speed DUTY : 60%	Power on FAN speed DUTY : 100%
122	RTS1# VIDOUT	RTSA#	UART A Request To Send. PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
124	SOUT1 Config4E_2E	SOUTA	Serial Output A. 4E	2E


PCI-E CLK (100Ohm-Diff)
PCI-E (80Ohm-Diff)
U35A
uPD720200
USB HS & SS (90Ohm-Diffl)
U35B
uPD720200
U35C
uPD720200
UPD720200F1-DAK-A-RH
UPD720200F1-DAK-A-RH
UPD720200F1-DAK-A-RH
System management Interrupt
H" active level of SMIB signal
since Mar./10
Near to USB 3.0 Chip
Reserved R/C for EMI
Close to U35, short&broad connection to GND.
Ref: 7676
NEC_XT1
NEC_XT2
Y3
24MHZ12P_S
C215
C12p50N4
C214
C12p50N4
NEC_3VSB
D28
1N4148W-F_SOD123-RH
R571
10K/4
PONRSTB
C538
C1u6.3Y0402-RH
VCC_1P05
V1P05
X_TP
SSTX1N
SSTX1P
SSRX1N
SSRX1P
SSTX2P
SSTX2N
SSRX2N
SSRX2P
L18
X_CMC_90ohm_0603
RN20
8P4R-0R
EXT_U2DP1
EXT_U2DN1
EXT_U2DP2
EXT_U2DN2
EXT_SBD1+
EXT_SBD1-
EXT_SBD2+
EXT_SBD2-
AVCC_3
Close to U35.D7
Close to U35.P13
NEC_3VSB for Controller
VCC3_SB
VCC3
NEC_3VSB
R582
X_0/8
C547
X_0.1u/16X
R583
100K
Q77
P-P06P03LCG_SOT89-3-RH
R580
1K/4
Q78
N-2N7002_SOT23-1
R584
10K/4
SLP_S3#
9,12,14,16,17,19
C548
0.1u/16X
EEPROM
U31
AT25F512B-SSH-T-HF
R577
47K/4
R578
10K/4
R579
10K/4
USB_SPICSB
USB_SPISI
USB_SPISO
USB_SPISCK
AVCC3 STB Power
R56
0R
C546
22u/6.3X/8
C225
0.1u/16Y
C711
0.1u/16Y
C723
C705
C721
C539
C710
C540
C0.01u16X0402
Close to UPD720200
each PWR group
ESD Protection
U27
ESD-IP4220
NEAR USB CONNECTOR
U32
ESD-PDY050003-2510-RH
U37
ESD-PDY050003-2510-RH
uPD720200 core Power
U12
NCP1599MNR2G_DFN6-RH
CHOKE7
CH-4.7u1.7A-RH
Trace > 60mil
700 mA
C545
22u/6.3X/8
C556
C1u6.3Y0402-RH
R575
X_0/4
R516
4.7/K1%/0402
C522
X_C1000p50X0402
C544
C0.1u16X
R574
10K/R1%0402
C543
X_C0.01u16X0402
R573
31.6K/R1%/0402
R587
0R
C542
22u/6.3X/8
C541
22u/6.3X/8
Vout = (Rt+Rb)/Rb x 0.8
BOTTOM PAD
CONNECT TO
GND Through
4 VIAs
C714
0.1u/16Y
C718
0.1u/16Y
C708
C724
C709
C725
C713
C720
C0.01u16X0402
Close to UPD720200
each PWR group
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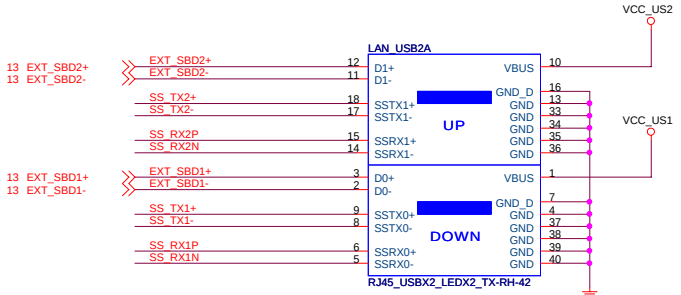
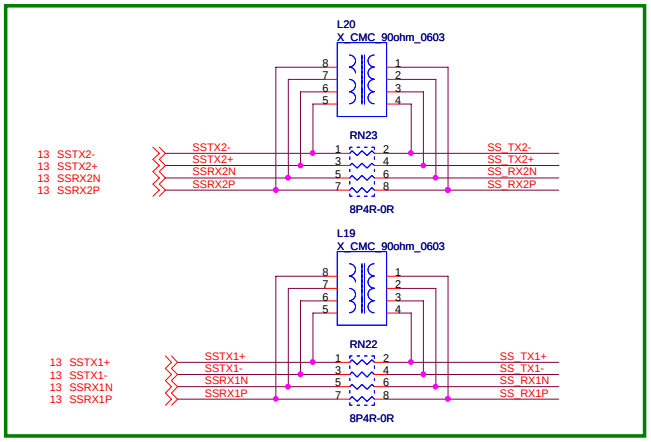
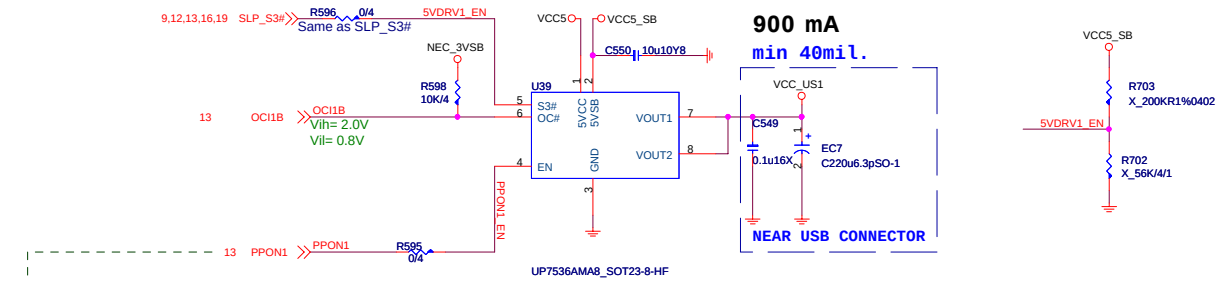
USB 3.0 CONNECTOR

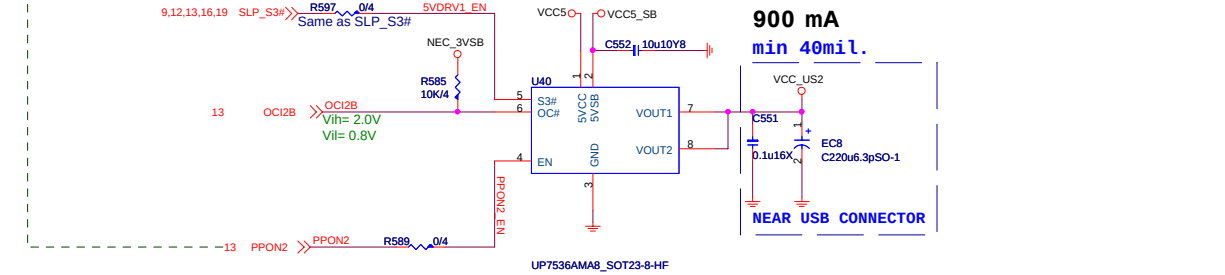


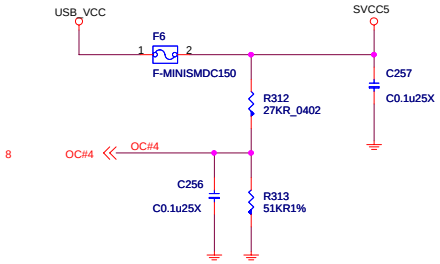
Confirm PN:
Current: N58-32F0031-F02
TBC: N58-32F0041-I60

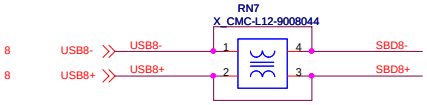


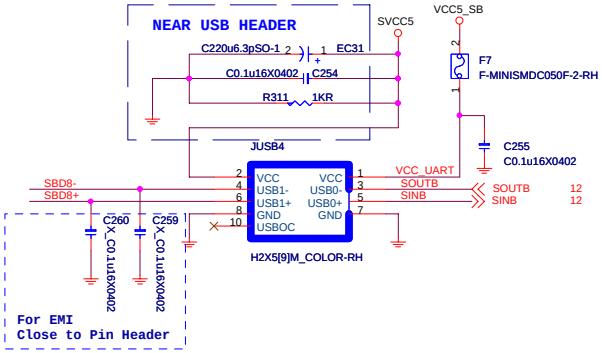


All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OCIx going to low.









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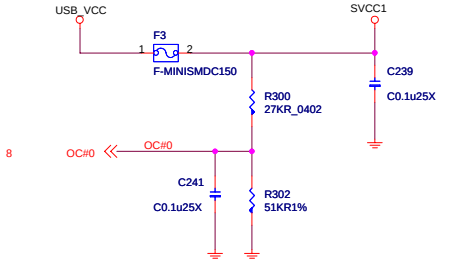
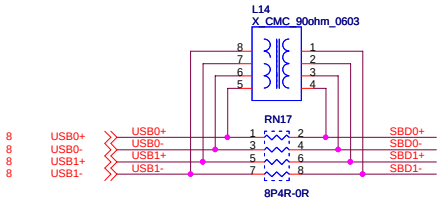
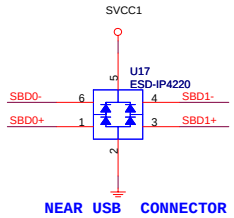
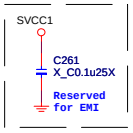
POWER CIRCUIT FOR USB PORT 0,1

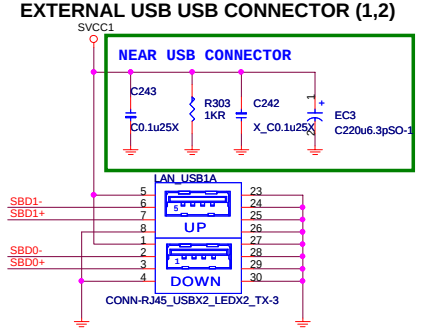




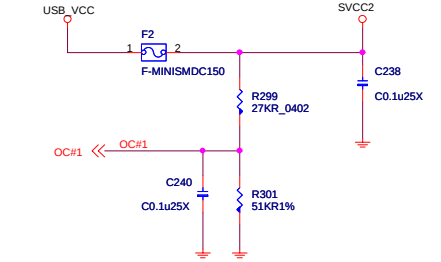


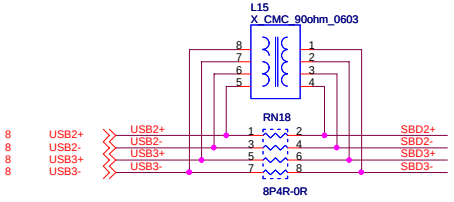


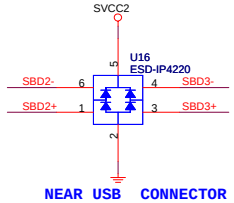
EXTERNAL USB USB CONNECTOR (1,2)



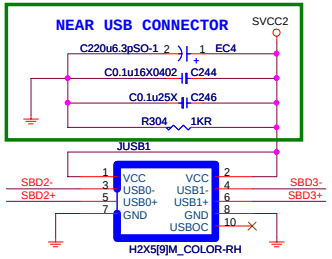
POWER CIRCUIT FOR USB PORT 2,3



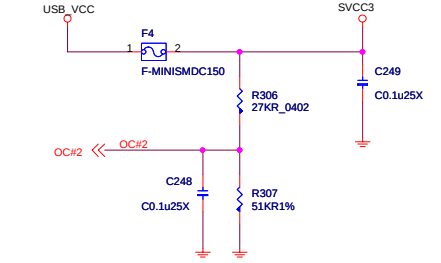


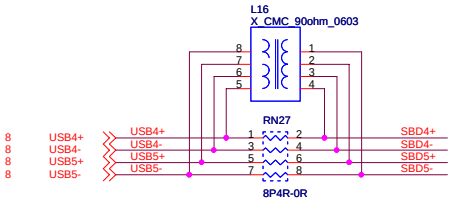


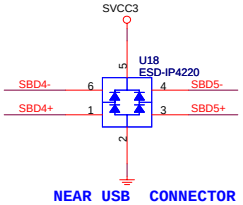
REAR PANEL USB Header FOR USB PORT (3,4)



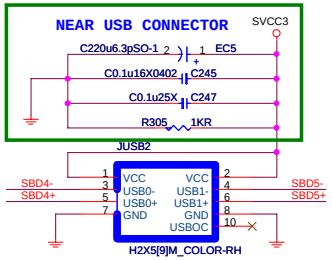
POWER CIRCUIT FOR USB PORT 4,5



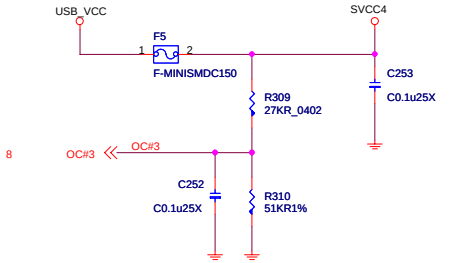


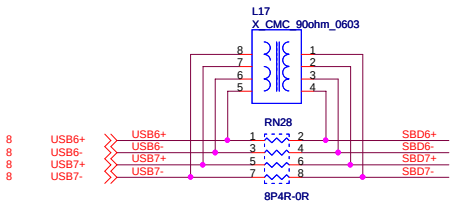


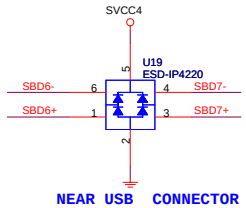
REAR PANEL USB Header FOR USB PORT (5,6)



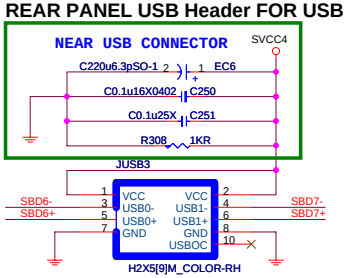
POWER CIRCUIT FOR USB PORT 6,7







REAR PANEL USB Header FOR USB PORT (7,8)



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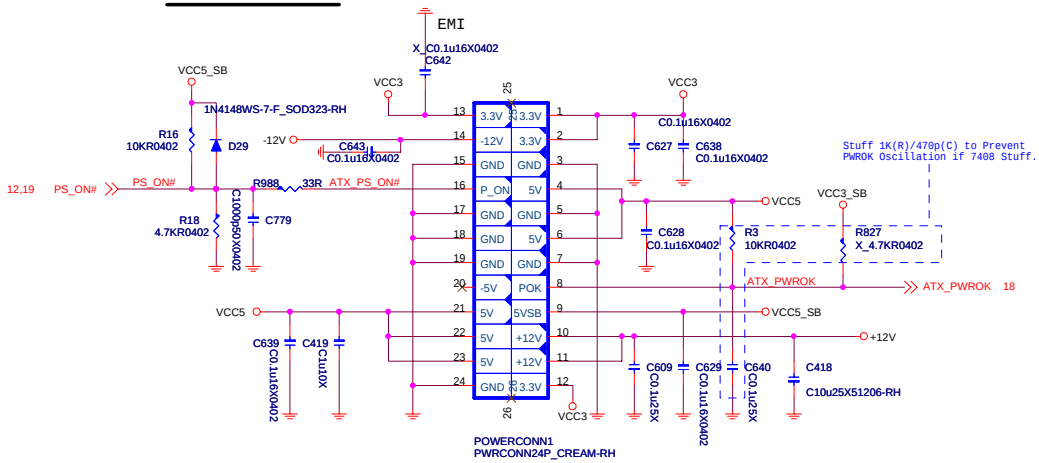
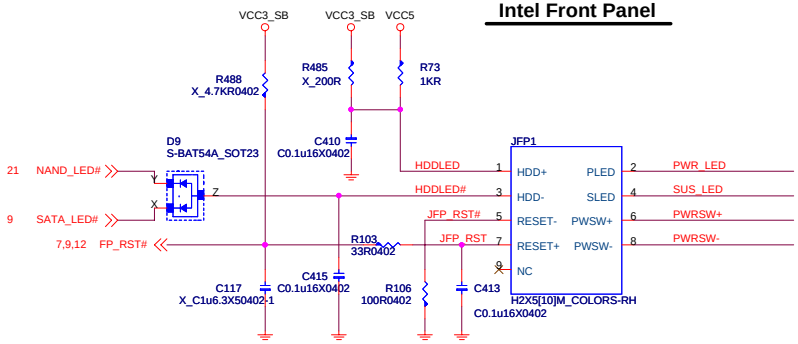
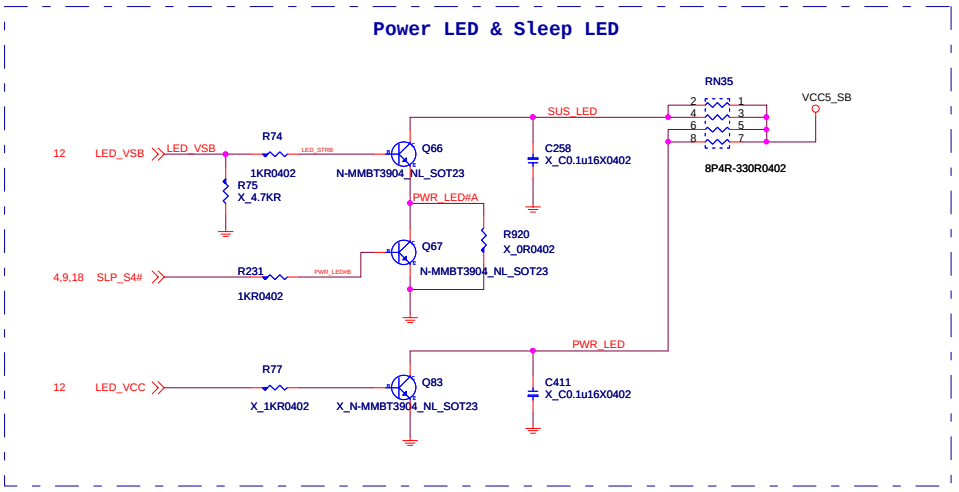
ATX Connector

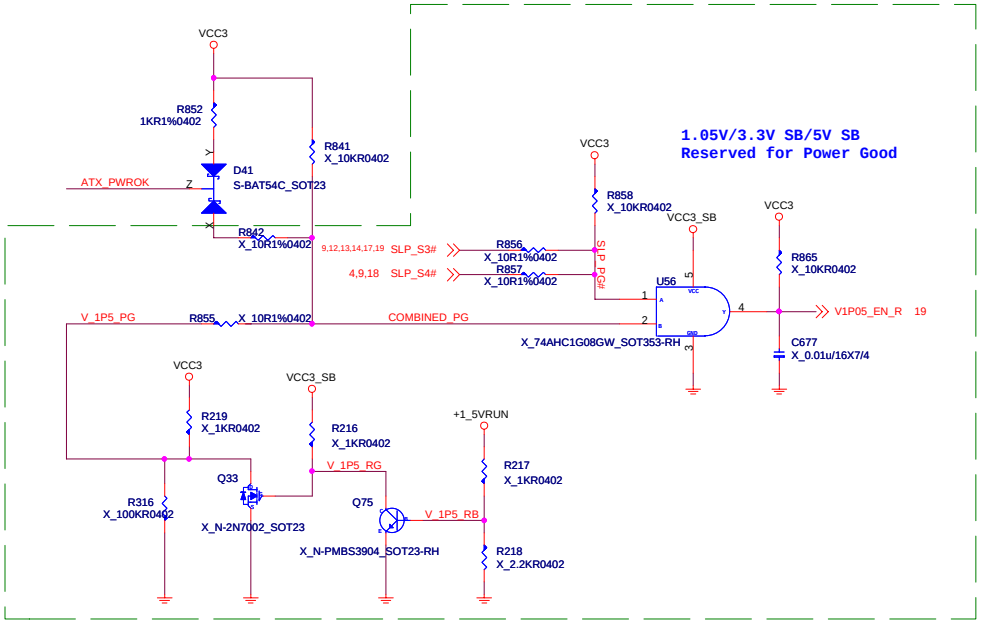


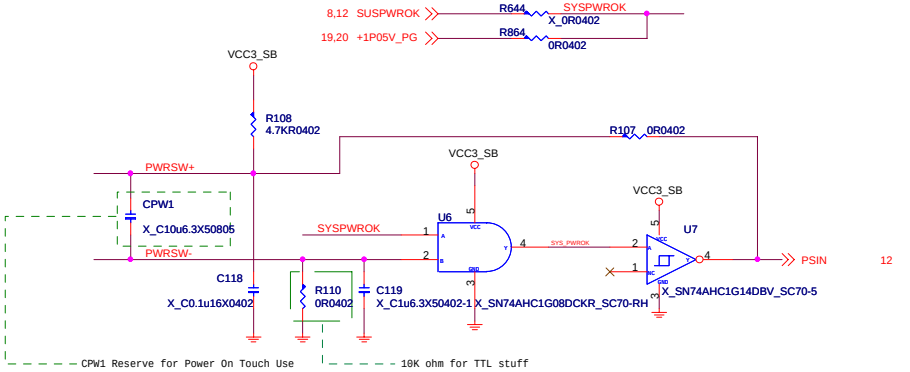
Intel Front Panel

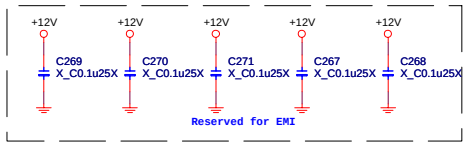


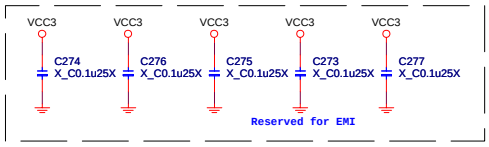
Power LED & Sleep LED

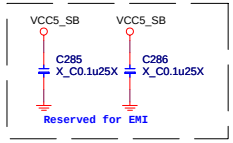


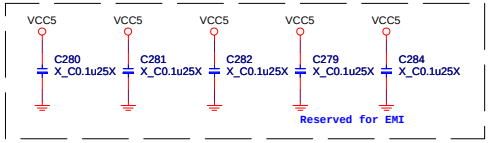












MICRO-STAR INT'L CO.,LTD

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Custom	DC-IN System Power	1.1

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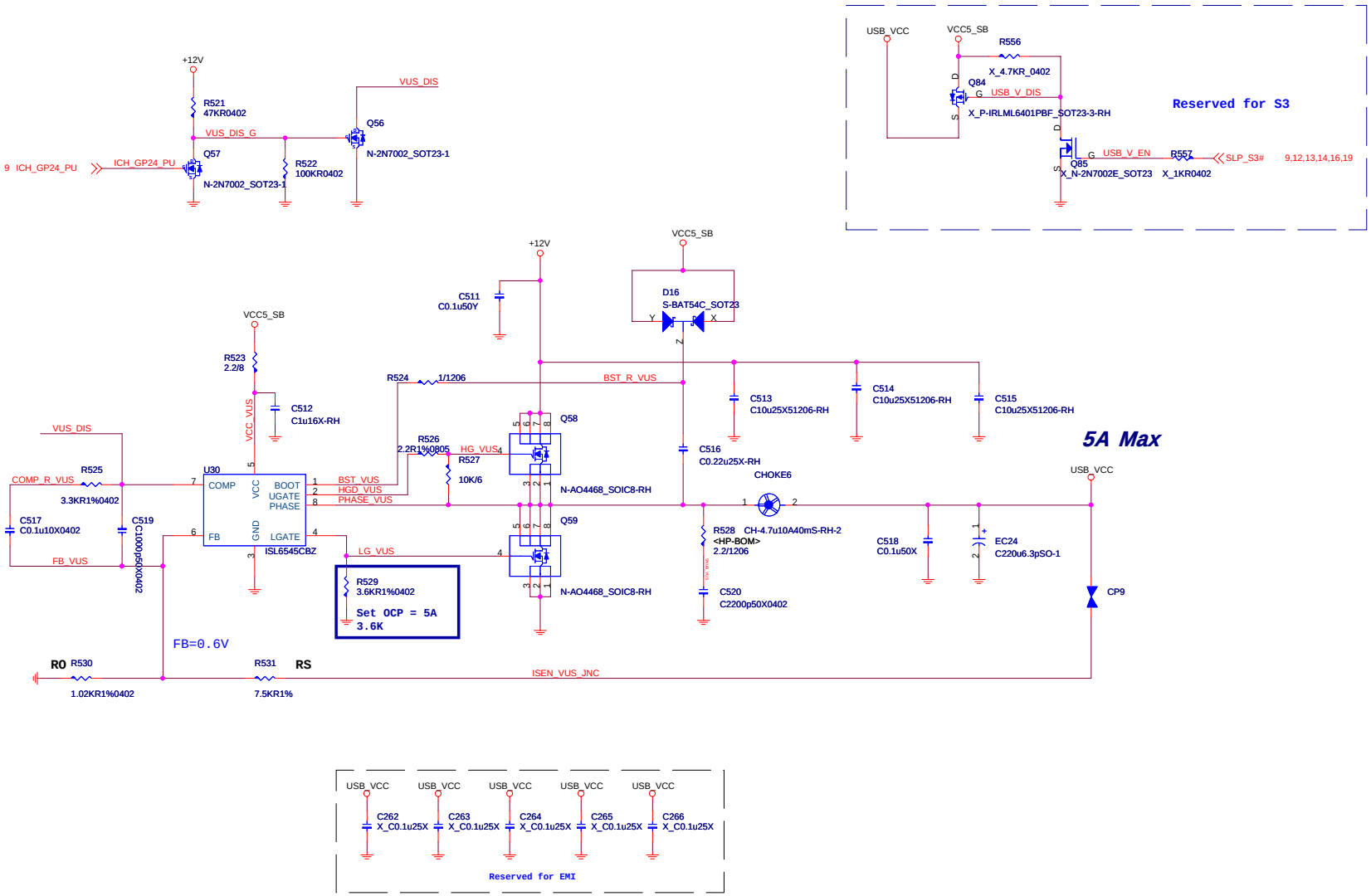

MSI	MICRO-STAR INT'L CO.,LTD	
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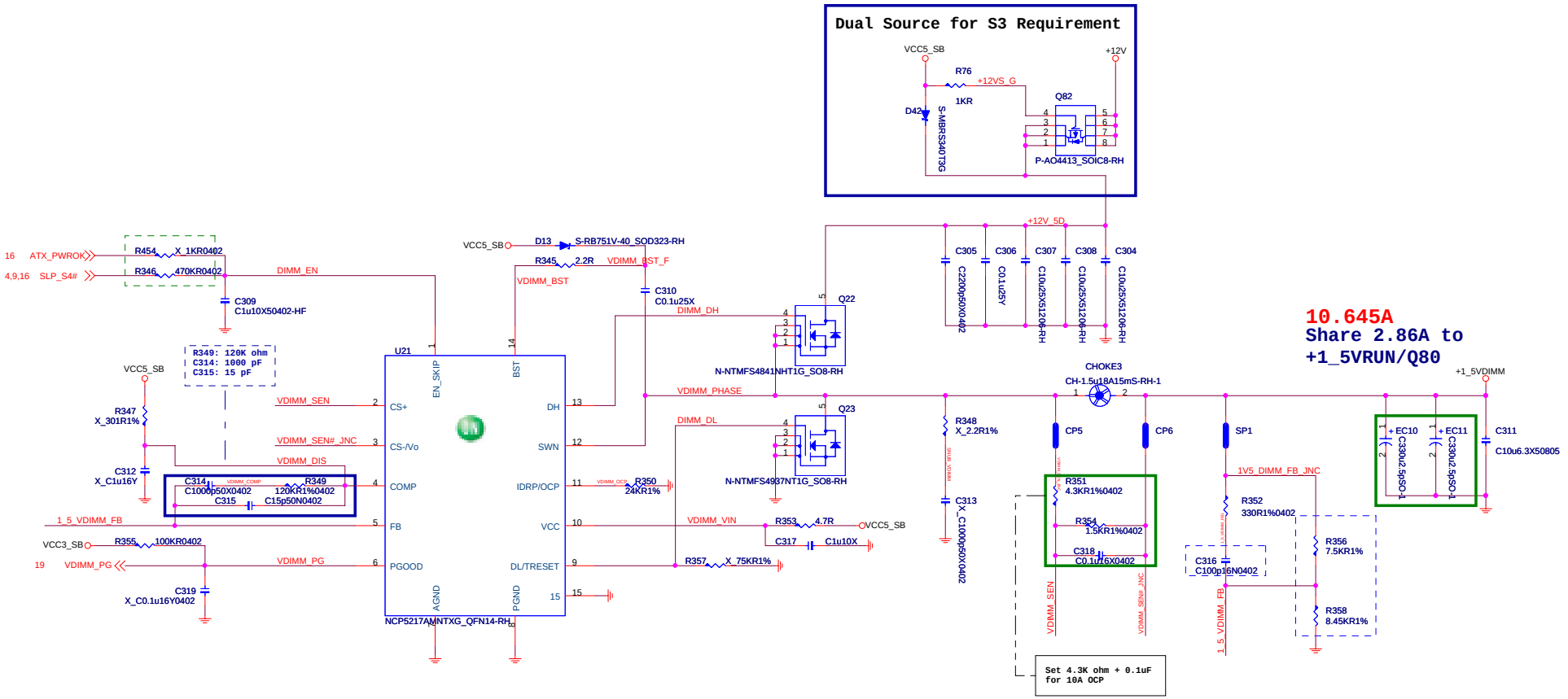

MICRO-STAR INT'L CO.,LTD	
S0031	
Size: Custom	Document Description: +1_5VDIMM & VCC3_SB
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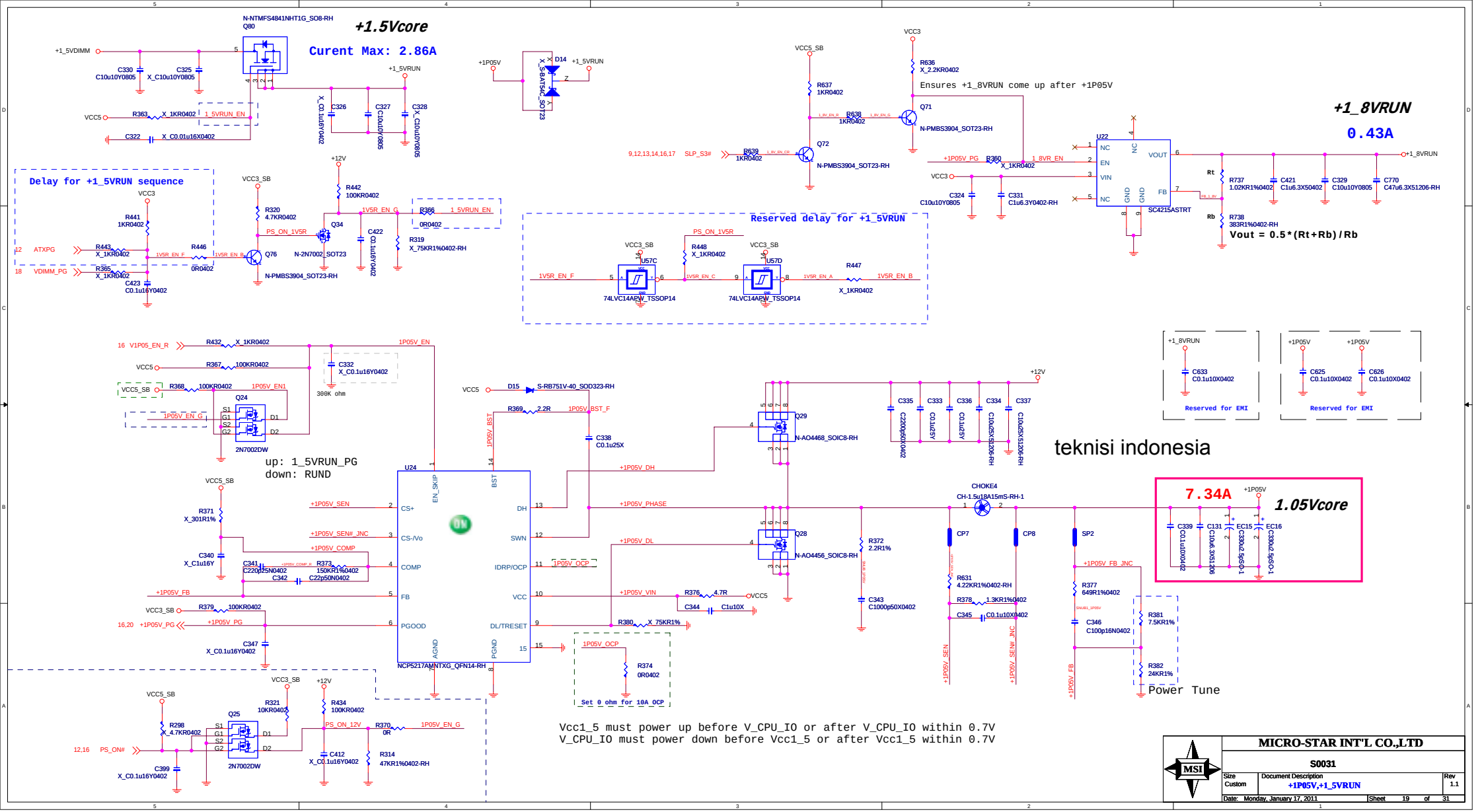
+1.5Vcore
Curent Max: 2.86A
N-NTMFS4841NHT1G_SO8-RH
Q80
+1_5VDIMM
C330 C10u10Y0805
C325 X_C10u10Y0805
+1_5VRUN
C326 X_C0.01u16Y0402
C327 C10u10Y0805
C328 X_C10u10Y0805
VCC5
R363 X_1KR0402
1_5VRUN_EN
C322 X_C0.01u16X0402
+1P05V
D14 X_S8ATS4C_SOT23
Delay for +1_5VRUN sequence
VCC3
R441 1KR0402
12 ATXPG
R443 X_1KR0402
R446 0R0402
18 VDIMM_PG
R365 X_1KR0402
C423 C0.1u16Y0402
VCC3_SB
R320 4.7KR0402
PS_ON_1V5R
Q34
Q76 N-PMBS3904_SOT23-RH
N-2N7002_SOT23
C422 C0.1u16Y0402
R319 X_75KR1%0402-RH
+12V
R442 100KR0402
1V5R_EN_G
R366 0R0402
1_5VRUN_EN
Reserved delay for +1_5VRUN
U57C 74LVC14APW_TSSOP14
U57D 74LVC14APW_TSSOP14
R448 X_1KR0402
R447 X_1KR0402
1V5R_EN_F
1V5R_EN_C
1V5R_EN_A
1V5R_EN_B
VCC5_SB
R637 1KR0402
R636 X_2.2KR0402
Ensures +1_8VRUN come up after +1P05V
Q71 N-PMBS3904_SOT23-RH
R638 1KR0402
9,12,13,14,16,17 SLP_S3#
R639 1KR0402
Q72 N-PMBS3904_SOT23-RH
+1P05V_PG
R360 X_1KR0402
1_8VR_EN
U22 SC4215ASTRT
NC EN VIN NC VOUT GND GND FB
C324 C10u10Y0805
C331 C1u6.3Y0402-RH
+1_8VRUN
0.43A
Rt R737 1.02KR1%0402
Rb R738 383R1%0402-RH
Vout = 0.5*(Rt+Rb)/Rb
C421 C1u6.3X50402
C329 C10u10Y0805
C770 C47u6.3X51206-RH
+1_8VRUN
C633 C0.1u10X0402
Reserved for EMI
+1P05V
C625 C0.1u10X0402
C626 C0.1u10X0402
Reserved for EMI
16 V1P05_EN_R
R432 X_1KR0402
1P05V_EN
VCC5
R367 100KR0402
C332 X_C0.1u16Y0402
300K ohm
VCC5_SB
R368 100KR0402
1P05V_EN1
Q24 2N7002DW
1P05V_EN_G
up: 1_5VRUN_PG
down: RUND
VCC5
D15 S-RB751V-40_SOD323-RH
R369 2.2R
1P05V_BST_F
C338 C0.1u25X
1P05V_BST
+12V
Q29 N-AO4468_SOIC8-RH
C335 C2200p50X0402
C333 C0.1u25Y
C336 C0.1u25Y
C334 C10u25X5R206-RH
C337 C10u25X5R206-RH
+1P05V_DH
+1P05V_PHASE
+1P05V_DL
Q28 N-AO4456_SOIC8-RH
R372 2.2R1%
C343 C1000p50X0402
CHOKE4 CH-1.5u18A15mS-RH-1
CP7
CP8
SP2
R631 4.22KR1%0402-RH
R378 1.3KR1%0402
C345 C0.1u10X0402
+1P05V_SEN
+1P05V_SEN#_JNC
+1P05V_FB
+1P05V_FB_JNC
R377 649R1%0402
C346 C100p16N0402
R381 7.5KR1%
R382 24KR1%
Power Tune
7.34A
1.05Vcore
C339 C0.1u10X0402
C131 C10u6.3X51206
EC15 C330u2.5vSO-1
EC16 C330u2.5vSO-1
VCC5_SB
R371 X_301R1%
C340 X_C1u16Y
C341 C220p25N0402
C342 C22p50N0402
R373 150KR1%0402
+1P05V_COMP
+1P05V_SEN
+1P05V_SEN#_JNC
+1P05V_FB
U24 NCP5217ANTXG_QFN14-RH
EN_SKIP
BST
CS+
CS-/Vo
COMP
FB
PGOOD
AGND
PGND
DH
SWN
IDRP/OCP
VCC
DL/TRESET
+1P05V_VIN
R376 4.7R
C344 C1u10X
R380 X_75KR1%
1P05V_OCP
R374 0R0402
Set 0 ohm for 10A OCP
VCC3_SB
R379 100KR0402
16,20 +1P05V_PG
C347 X_C0.1u16Y0402
VCC5_SB
R298 X_4.7KR0402
Q25 2N7002DW
12,16 PS_ON#
C399 X_C0.1u16Y0402
VCC3_SB
R321 10KR0402
+12V
R434 100KR0402
PS_ON_12V
R370 0R
1P05V_EN_G
C412 X_C0.1u16Y0402
R314 47KR1%0402-RH
teknisi indonesia
Vcc1_5 must power up before V_CPU_IO or after V_CPU_IO within 0.7V
V_CPU_IO must power down before Vcc1_5 or after Vcc1_5 within 0.7V
MICRO-STAR INT'L CO.,LTD
S0031
Size Custom
Document Description +1P05V,+1_5VRUN
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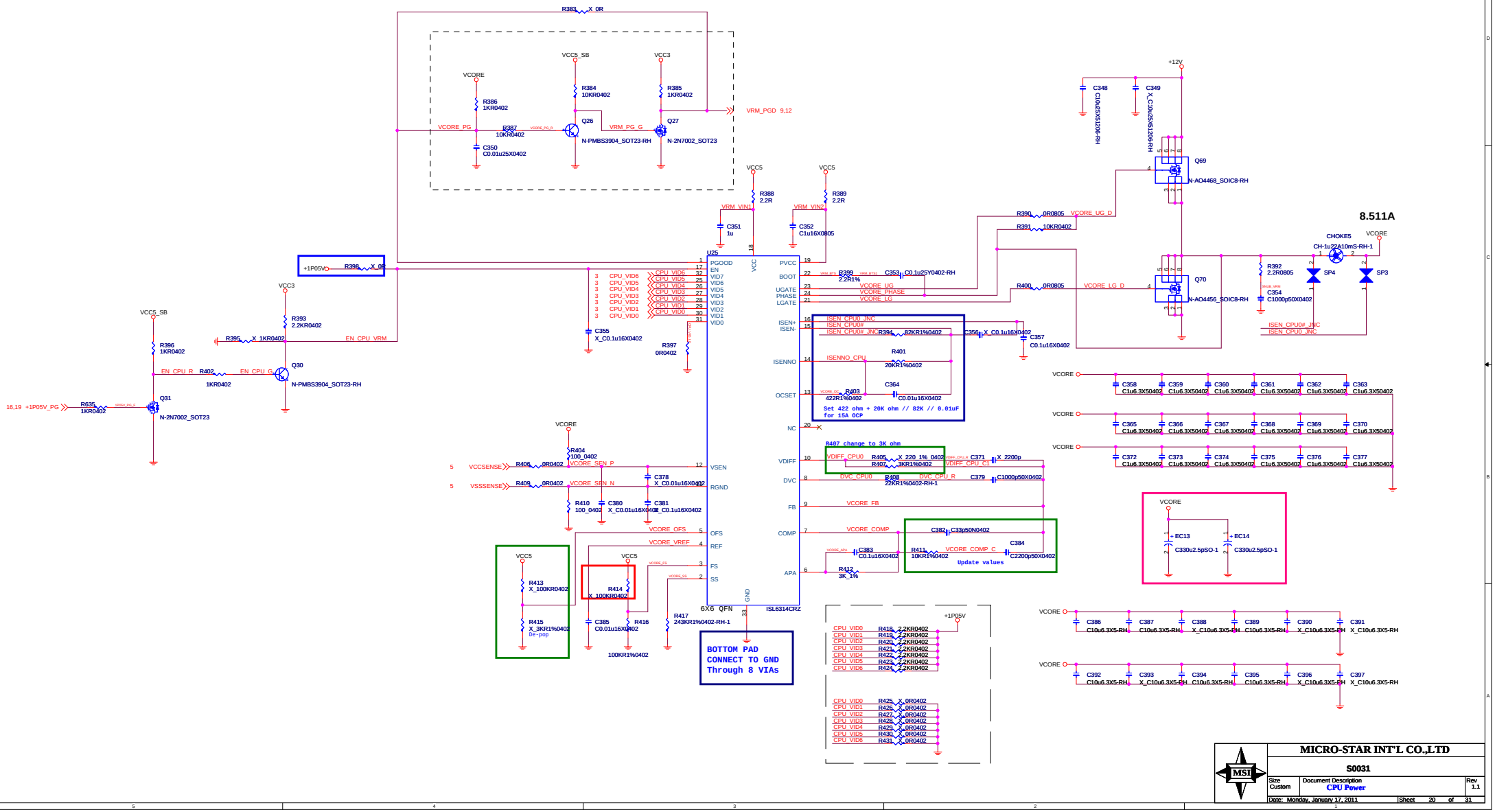
8.511A
U25
ISL6314CRZ
6X6 QFN
PGOOD
EN
VID7
VID6
VID5
VID4
VID3
VID2
VID1
VID0
PVCC
BOOT
UGATE
PHASE
LGATE
ISEN+
ISEN-
ISENNO
OCSET
NC
VDIFF
DVC
FB
COMP
APA
VSEN
RGND
OFS
REF
FS
SS
GND
VCC
VRM_PGD 9,12
VRM_VIN
VCORE_UG
VCORE_PHASE
VCORE_LG
ISEN_CPU0_JNC
ISEN_CPU0#
ISEN_CPU0#_JNC
ISENNO_CPU
VCORE_OCS
VDIFF_CPU0
DVC_CPU0
VCORE_FB
VCORE_COMP
VCORE_APA
VCCSENSE
VSSSENSE
VCORE_SEN_P
VCORE_SEN_N
VCORE_OFS
VCORE_VREF
VCORE_FS
VCORE_SS
CPU_VID6
CPU_VID5
CPU_VID4
CPU_VID3
CPU_VID2
CPU_VID1
CPU_VID0
EN_CPU_VRM
EN_CPU_R
EN_CPU_G
VCORE_PG
VCORE_PG_R
VRM_PG_G
+1P05V_PG
+1P05V
+12V
VCC5
VCC3
VCC5_SB
VCORE
R383 X_0R
R384 10KR0402
R385 1KR0402
R386 1KR0402
R387 10KR0402
R388 2.2R
R389 2.2R
R390 0R0805
R391 10KR0402
R392 2.2R0805
R393 2.2KR0402
R394 82KR1%0402
R395 X_1KR0402
R396 1KR0402
R397 0R0402
R398 X_0R
R399 2.2R1%
R400 0R0805
R401 20KR1%0402
R402 1KR0402
R403 422R1%0402
R404 100_0402
R405 X_220_1%_0402
R406 0R0402
R407 3KR1%0402
R408 22KR1%0402-RH-1
R409 0R0402
R410 100_0402
R411 10KR1%0402
R412 3K_1%
R413 X_100KR0402
R414 X_100KR0402
R415 X_3KR1%0402
DE-pop
R416 100KR1%0402
R417 243KR1%0402-RH-1
R418 2.2KR0402
R419 2.2KR0402
R420 2.2KR0402
R421 2.2KR0402
R422 2.2KR0402
R423 2.2KR0402
R424 2.2KR0402
R425 X_0R0402
R426 0R0402
R427 0R0402
R428 0R0402
R429 0R0402
R430 0R0402
R431 0R0402
C348 C10u25X5X20R-RH
C349 X_C10u25X5X20R-RH
C350 C0.01u25X0402
C351 1u
C352 C1u16X0805
C353 C0.1u25Y0402-RH
C354 C1000p50X0402
C355 X_C0.1u16X0402
C356 X_C0.1u16X0402
C357 C0.1u16X0402
C358 C1u6.3X50402
C359 C1u6.3X50402
C360 C1u6.3X50402
C361 C1u6.3X50402
C362 C1u6.3X50402
C363 C1u6.3X50402
C364 C0.01u16X0402
C365 C1u6.3X50402
C366 C1u6.3X50402
C367 C1u6.3X50402
C368 C1u6.3X50402
C369 C1u6.3X50402
C370 C1u6.3X50402
C371 X_2200p
C372 C1u6.3X50402
C373 C1u6.3X50402
C374 C1u6.3X50402
C375 C1u6.3X50402
C376 C1u6.3X50402
C377 C1u6.3X50402
C378 X_C0.01u16X0402
C379 C1000p50X0402
C380 X_C0.01u16X0402
C381 X_C0.1u16X0402
C382 C33p50N0402
C383 C0.1u16X0402
C384 C2200p50X0402
C385 C0.01u16X0402
C386 C10u6.3X5-RH
C387 C10u6.3X5-RH
C388 X_C10u6.3X5-RH
C389 C10u6.3X5-RH
C390 X_C10u6.3X5-RH
C391 X_C10u6.3X5-RH
C392 C10u6.3X5-RH
C393 X_C10u6.3X5-RH
C394 C10u6.3X5-RH
C395 C10u6.3X5-RH
C396 X_C10u6.3X5-RH
C397 X_C10u6.3X5-RH
EC13 330u2.5pSO-1
EC14 330u2.5pSO-1
Q26 N-PMBS3904_SOT23-RH
Q27 N-2N7002_SOT23
Q30 N-PMBS3904_SOT23-RH
Q31 N-2N7002_SOT23
Q69 N-AO4468_SOIC8-RH
Q70 N-AO4456_SOIC8-RH
CHOKE5 CH-1u22A10mS-RH-1
SP4
SP3
R407 change to 3K ohm
Set 422 ohm + 20K ohm // 82K // 0.01uF for 15A OCP
Update values
BOTTOM PAD CONNECT TO GND Through 8 VIAS
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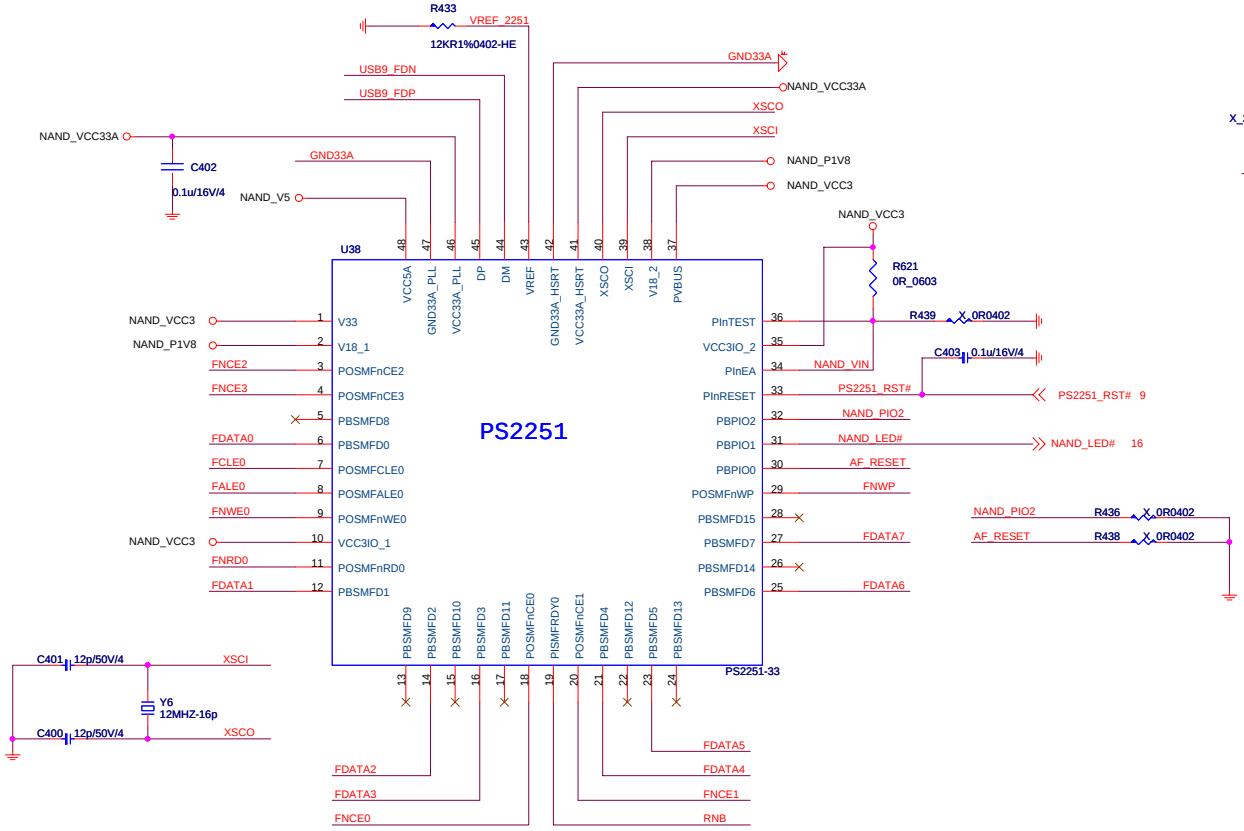
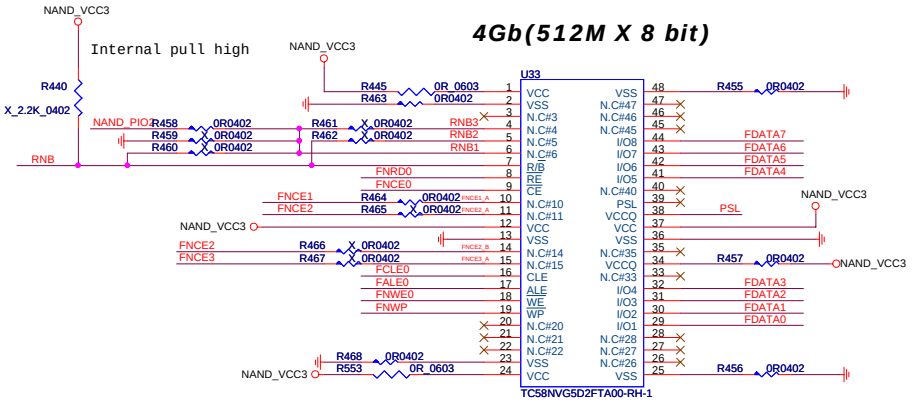
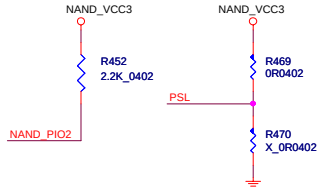
R433:PS2232,PS2233 don't need pull low
PS2231 need pull low

NAND Pin 2,23,24,25,34,38,48
for 45nm Flash Setting

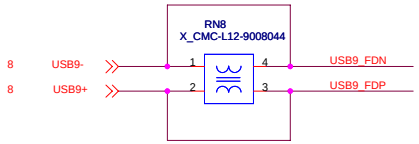


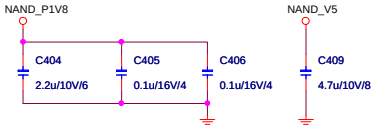


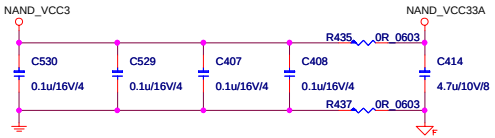
PN Confirm:
Toshiba TC58NVG5D2FTA00/(MLC)

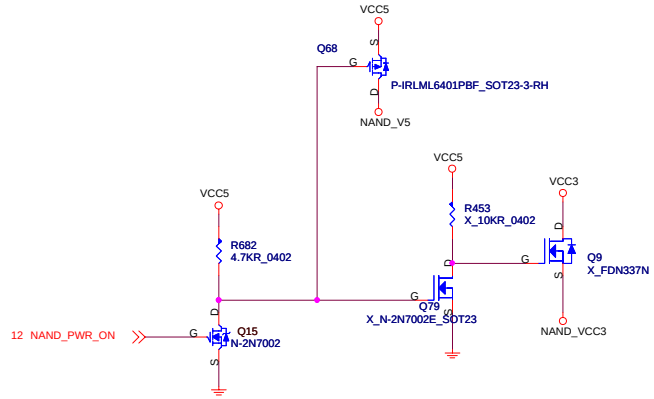


Depend on FLASH define:
1.PRE:pull to GND
2.VCCQ:pull to 3.3V
3.NC:Left as no connect









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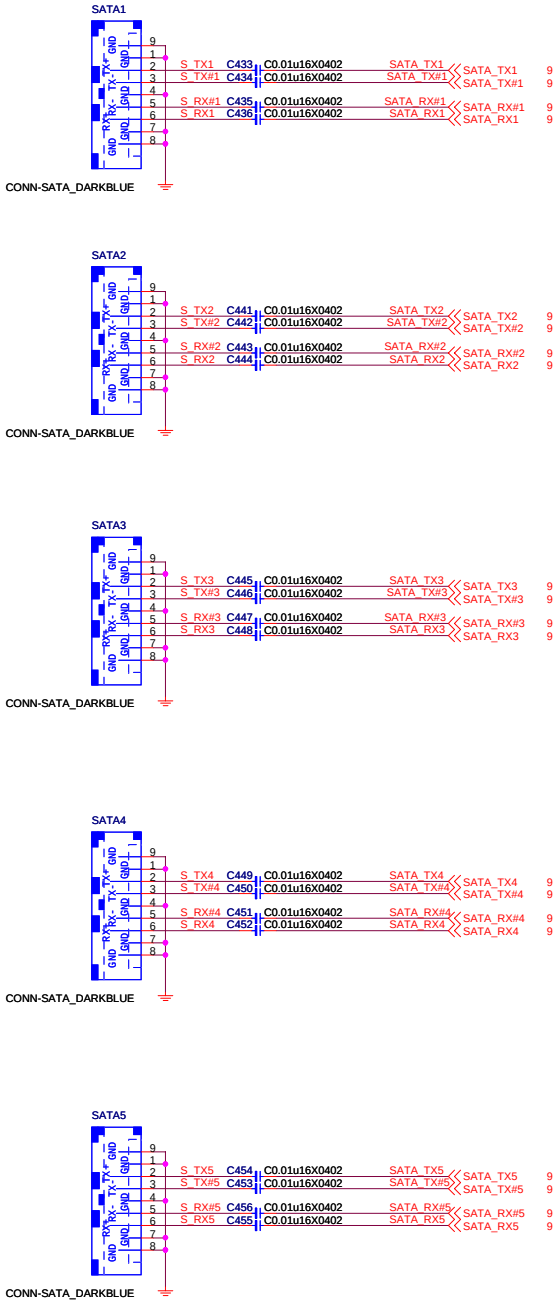
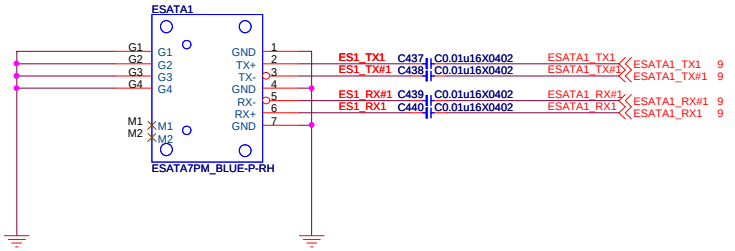
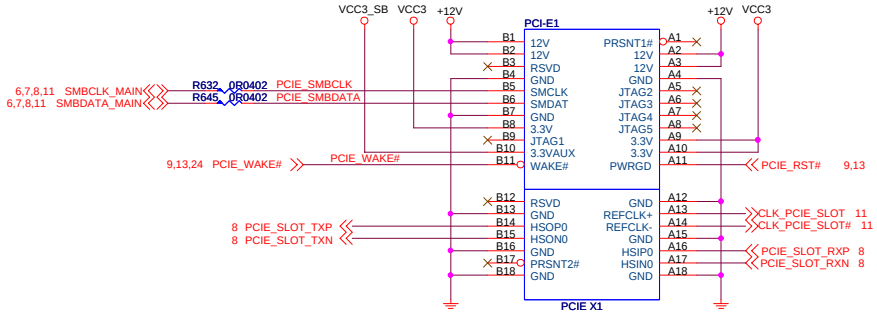
SATA Port 1 - 4

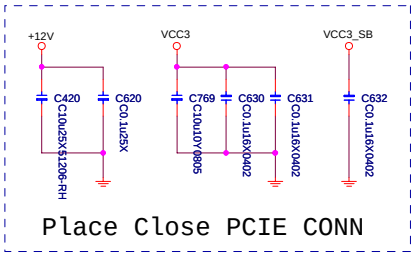


eSATA Port



PCI Express Slot





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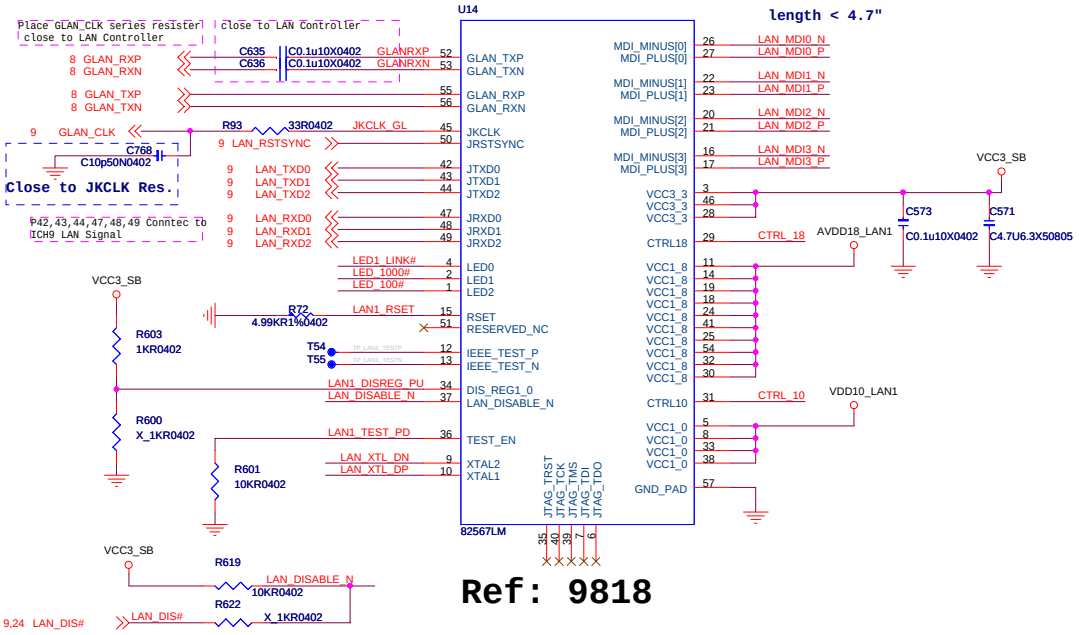
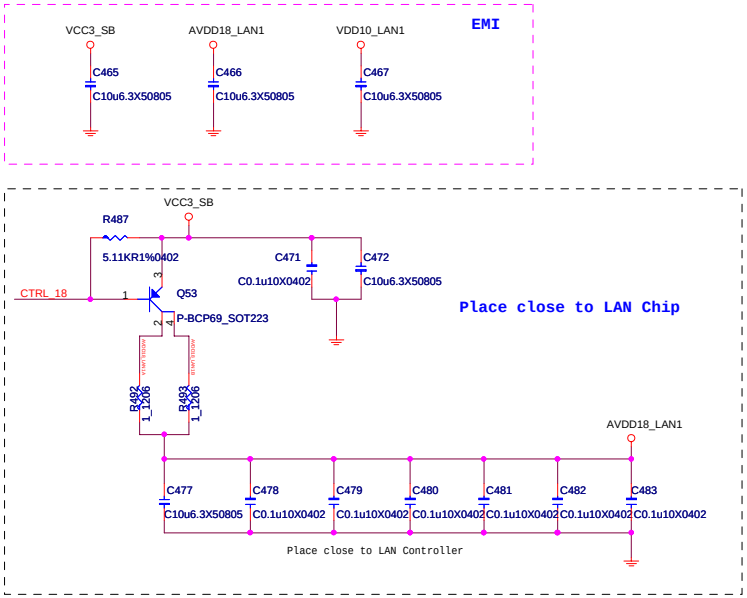
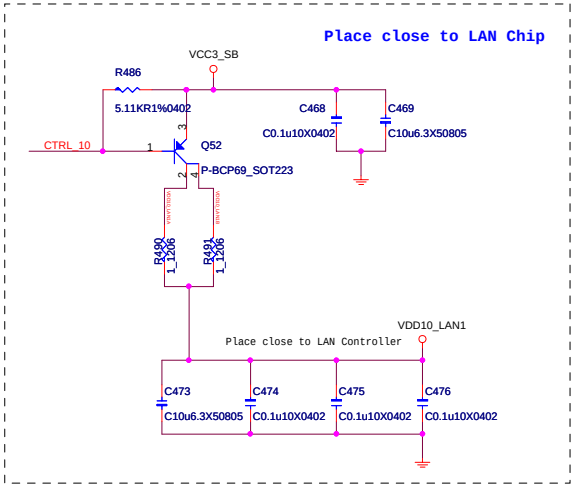
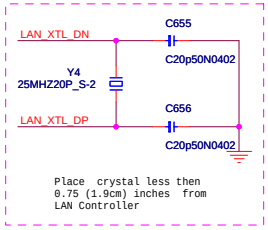
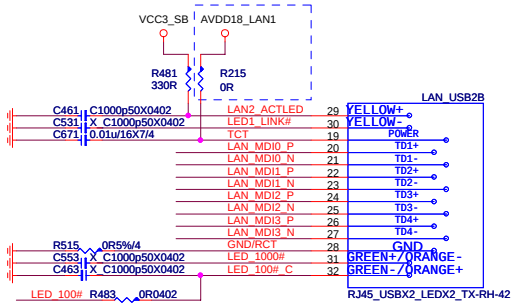


Ref: 9818









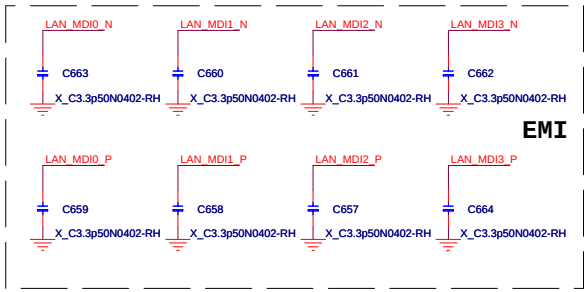
Giga-Lan

N58-32F0031-F02

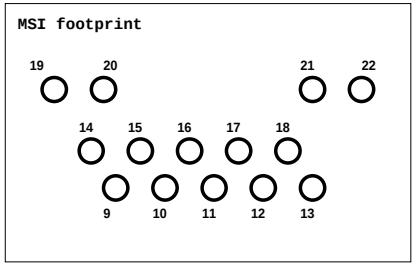
Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

29 — 30 Yellow

31 Orange — 22 Green



MSI footprint



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	S0031	
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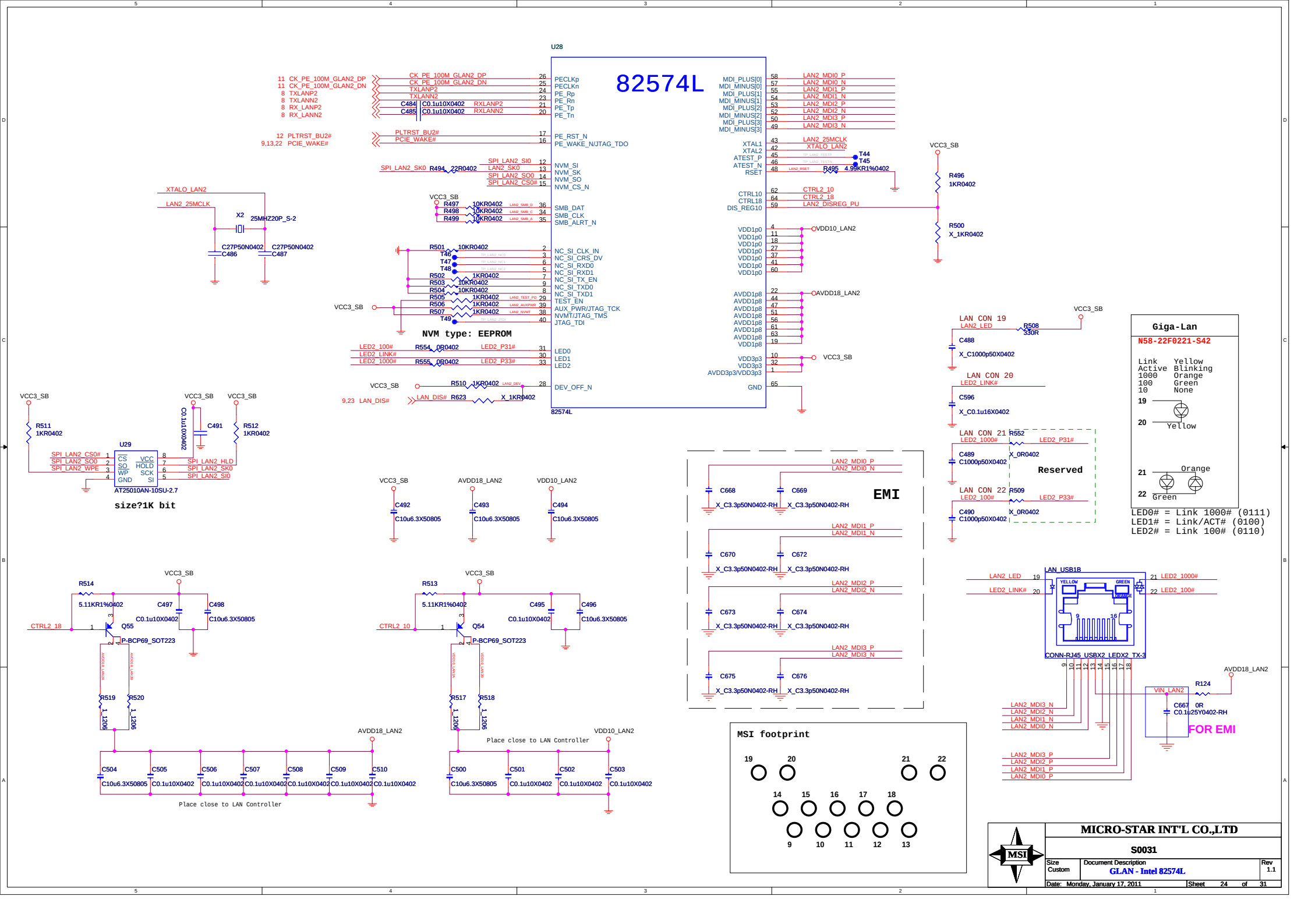
U28
82574L
NVM type: EEPROM
U29
AT25010AN-10SU-2.7
size?1K bit
EMI
MSI footprint
Giga-Lan
N58-22F0221-S42
Link Yellow
Active Blinking
1000 Orange
100 Green
10 None
Yellow
Orange
Green
LED0# = Link 1000# (0111)
LED1# = Link/ACT# (0100)
LED2# = Link 100# (0110)
Reserved
FOR EMI
Place close to LAN Controller
Place close to LAN Controller
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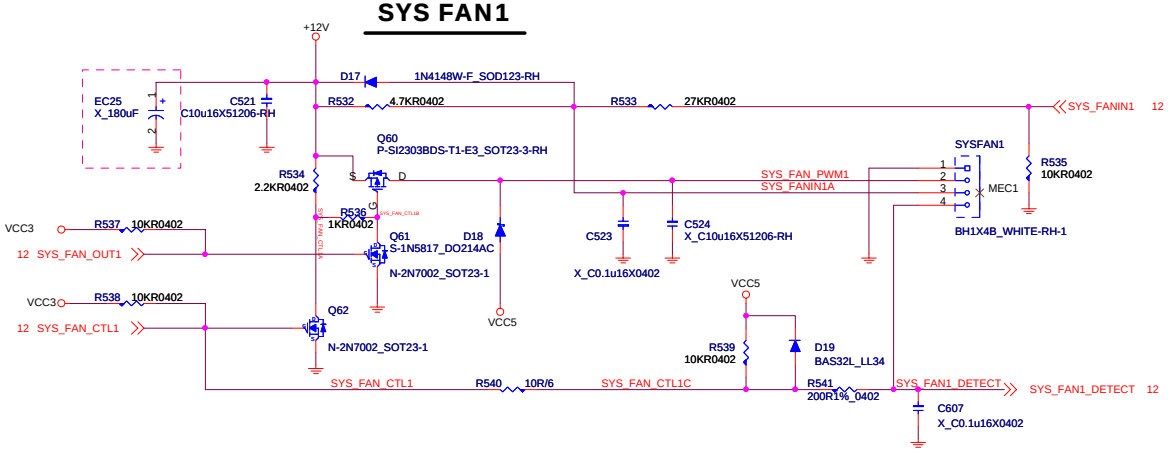
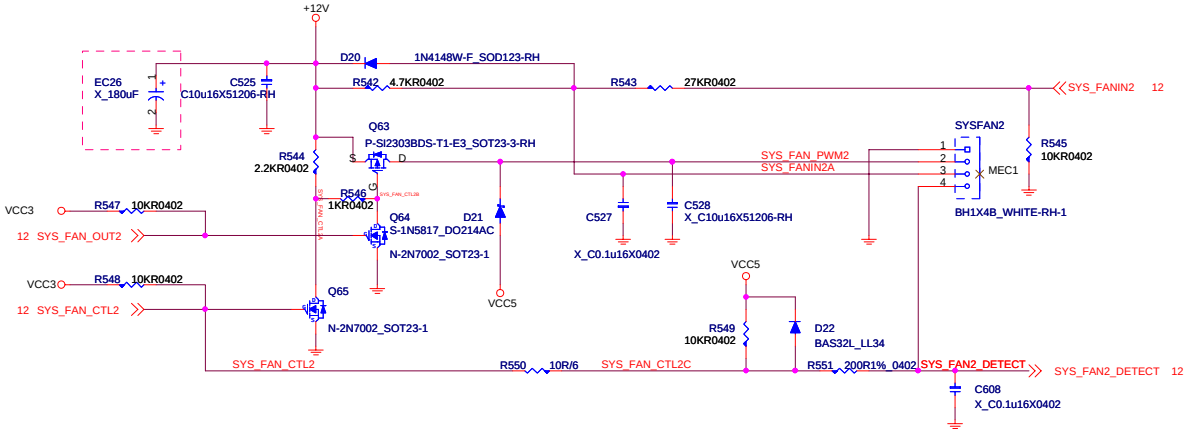
SYS FAN1



SYS FAN2



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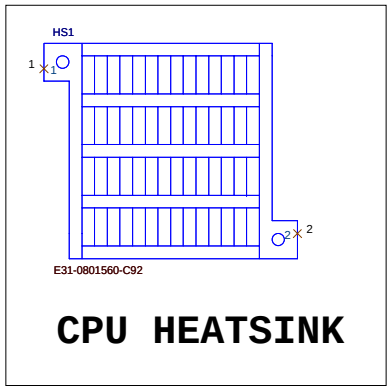
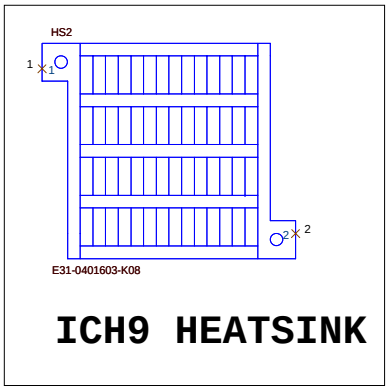
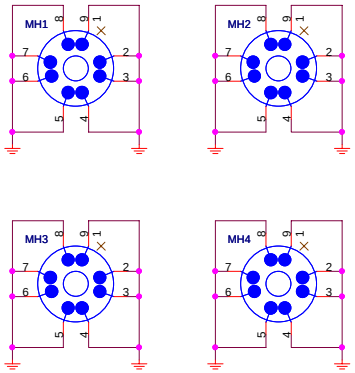
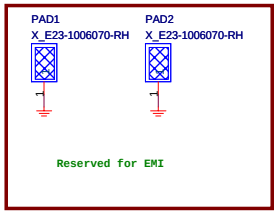
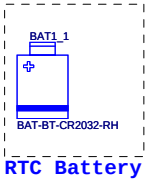


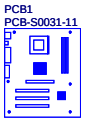


Mounting Holes







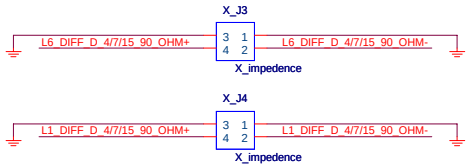


Optics Orientation Holes

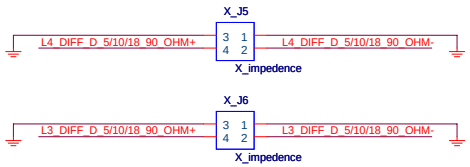
Simulation

50 Ohm±10%; MS=4 mil, S=5mil

40 Ohm±10%; MS=6.5 mil, S=8.5mil



90 Ohm±15%4/7/15(mil) for L1/L6



CLK 90 Ohm±10%5/10/18(mil) for L3/L4

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ICH9

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Setting	Signal Name	Default	Mark
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	GPO		H	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI			H	
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI		PIRQ#[H:E]	H	Low Active
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI			H	Low Active
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	GPI	ICH_GP8_PU	H	High Active
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	Native	WOL_ONLY	H	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	GPI	SIO_OVT#	H	Low Active
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native		SMB_ALERT#	H	Low Active
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	GPO	LAN_DIS#	H	Low Active
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	GPI	SIO_PME#	H	Low Active
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	GPI	ICH_GP14_PU	H	High Active
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	Native	PM_STPPCI#	H	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	GPO		H	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI		GP17_TACH0	H	
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	GPO	SATA2_ACT	H	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	GPI		H	Low Active
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO				
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	GPI		H	Low Active
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI		ICH_SGP22_PU	H	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native		LDRQ_1#	H	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	GPO	ICH_GP24_PU	H	High Active
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	Native	PM_STPCPU#	H	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native				
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	GPO		H	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	GPO	ICH_GP27_PU	H	
GPIO[29]	OC[5]#	I/O	Resume	3.3V	Native		OC2#	H	
GPIO[30]	OC[6]#	I/O	Resume	3.3V	Native		OC3#	H	
GPIO[31]	OC[7]#	I/O	Resume	3.3V	Native		OC5#	H	
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	GPO	SPI_WP#	H	
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	GPO	SPI_HOLD_GPO#	H	Low Active
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	GPO		H	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	GPO	ICH_GP35_PU	H	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	GPI		H	Low Active
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	GPI		H	Low Active
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	GPI	ICH_SGP38_PU	H	Low Active
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI		ICH_SGP39_PD	H	
GPIO[40]	OC[1]#	I/O	Resume	3.3V	Native		OC#0	H	
GPIO[42:41]	OC[3:2]#	I/O	Resume	3.3V	Native		OC#1	H	
GPIO[43]	OC[4]#	I/O	Resume	3.3V	Native		OC2#	H	
GPIO[45:44]	OC[9:8]#	I/O	Resume	3.3V	Native		OC4#		
GPIO[47:46]	OC[11:10]#	I/O	Resume	3.3V	Native		VCC3_SB		
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI		ICH_SGP48_PU	H	High Active
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO		DMI_STRAP	L	Strap pin
GPIO[50]	REQ1#	I/O	Core	5V	Native		PREQ#1	H	
GPIO[51]	GNT1#	I/O	Core	3.3V	Native		PGNT#1	H	
GPIO[52]	REQ2#	I/O	Core	5V	Native		PREQ#2	H	
GPIO[53]	GNT2#	I/O	Core	3.3V	Native		PGNT#2	H	
GPIO[54]	REQ3#	I/O	Core	5V	Native		PREQ#3	H	
GPIO[55]	GNT3#	I/O	Core	3.3V	Native		PGNT#3	H	
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	GPI	GP56_RSV_DETECT	H	For CFG Use
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	GPI	GP57_RSV_RECOV	H	Reserved
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI		SPI_CS1#	H	Low Active
GPIO[59]	OC[0]#	I/O	Resume	3.3V	Native		OC#0	H	
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native		LINK_ALERT#	H	Low Active

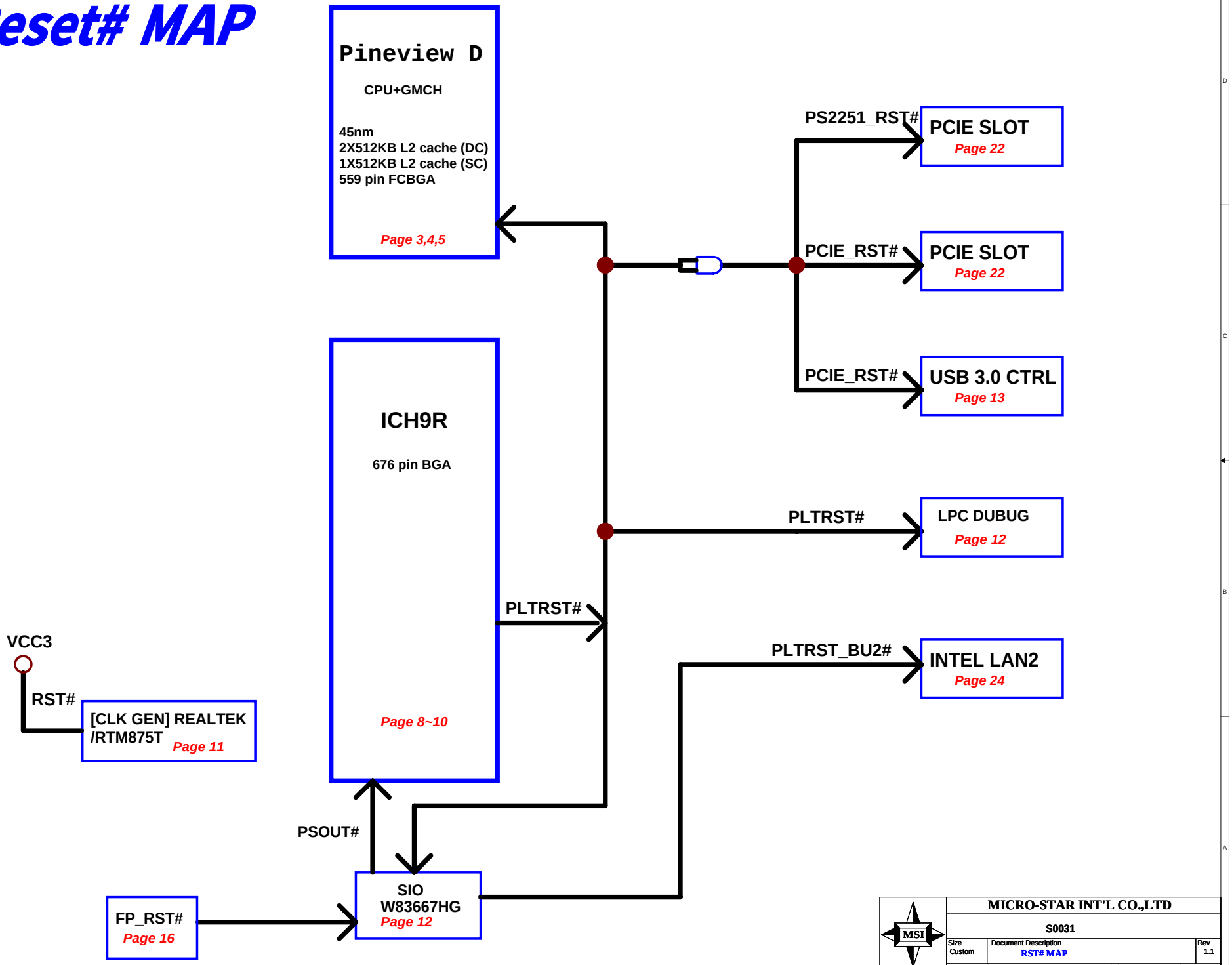
SIO(F71882)

PIN NAME	USAGE	Input/Output	Default	Mark
GPIO0	FNT_GP0	Reserved	H	
GPIO1	FNT_GP1	Reserved	H	
GPIO2	FNT_GP2	Reserved	H	
GPIO3	FNT_GP3	Reserved	H	
GPIO4	FNT_GP4	Reserved	H	
GPIO5	FNT_GP5	Reserved	H	
GPIO6	SLOTOCC#		H	
GPIO7	FNT_GP7	Reserved	H	
GPIO10	SYS_FAN_OUT3	N/A		
GPIO11	SYS_FAN1_DETECT	INPUT	H	
GPIO12	SYS_FAN2_DETECT	INPUT	H	
GPIO13	NAND_PWR_ON	OUTPUT	H	NAND POWER ON
GPIO14	GPIO_14	Reserved	H	
GPIO15	LED_VSB	OUTPUT	H	SLEEP LED
GPIO16	LED_VCC	OUTPUT	H	POWER LED
GPIO17	SYS_FAN_OUT2	OUTPUT	H	
GPIO20	PLTRST_BU1#	OUTPUT		PLTRST_BU1#
GPIO21	PLTRST_BU2#	OUTPUT		82574L PERST#
GPIO22	PLTRST_BU3#	OUTPUT		PLTRST_BU3#
GPIO23	FP_RST#	OUTPUT		RSTCON#
GPIO24	ATXPG	INPUT		ATXPG
GPIO26	PSIN	INPUT		PWSIN#
GPIO27	PSOUT#	OUTPUT		PWSOUT#
GPIO30	SLP_S3#	INPUT		S3#
GPIO31	PS_ON#	OUTPUT		PS_ON#
GPIO32	CHIP_PWRGD	OUTPUT		PWROK
GPIO33	RSMRST#	OUTPUT		RSMRST#
GPIO40	NS SYS_FANIN3	Test Point		
GPIO41	UPD_SMIB_PU	OUTPUT	H	USB3.0 SMIB
GPIO42	UNUSED			
GPIO43	SYS_FAN_OUT1	OUTPUT	H	

DDR-II DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	M_CLK_DDR0/#0	M_CLK_DDR1/#1
DIMM 2	02	M_CLK_DDR3/#3	M_CLK_DDR4/#4

Reset# MAP



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	S0031	
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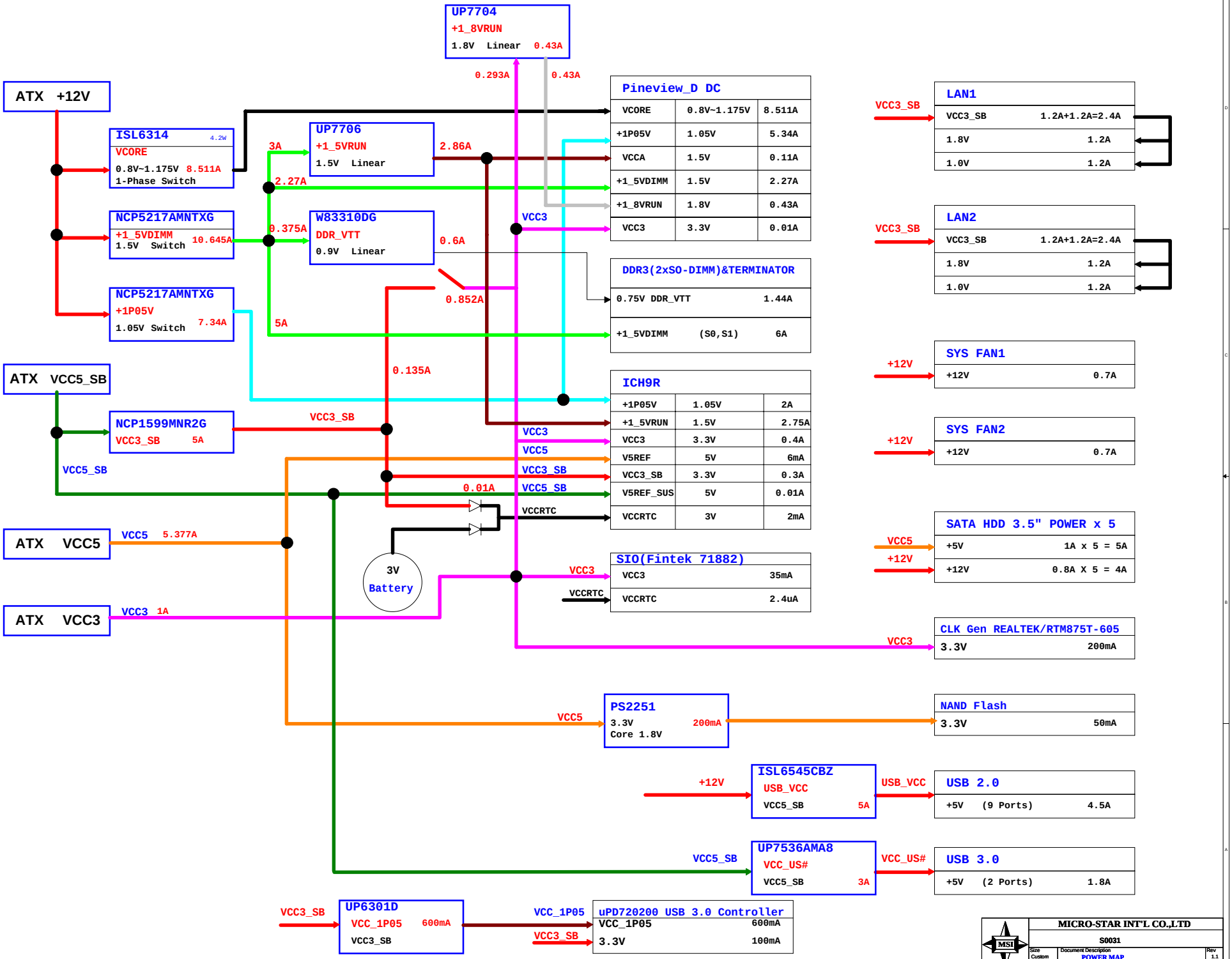
UP7704
+1_8VRUN
1.8V Linear 0.43A
0.293A
0.43A
ATX +12V
ISL6314 4.2W
VCORE
0.8V~1.175V 8.511A
1-Phase Switch
3A
UP7706
+1_5VRUN
1.5V Linear
2.86A
2.27A
NCP5217AMNTXG
+1_5VDIMM
1.5V Switch 10.645A
0.375A
W83310DG
DDR_VTT
0.9V Linear
0.6A
0.852A
5A
NCP5217AMNTXG
+1P05V
1.05V Switch 7.34A
ATX VCC5_SB
0.135A
NCP1599MNR2G
VCC3_SB 5A
VCC5_SB
ATX VCC5
VCC5 5.377A
ATX VCC3
VCC3 1A
3V
Battery
Pineview_D DC
VCORE 0.8V~1.175V 8.511A
+1P05V 1.05V 5.34A
VCCA 1.5V 0.11A
+1_5VDIMM 1.5V 2.27A
+1_8VRUN 1.8V 0.43A
VCC3 3.3V 0.01A
DDR3(2xSO-DIMM)&TERMINATOR
0.75V DDR_VTT 1.44A
+1_5VDIMM (S0,S1) 6A
ICH9R
+1P05V 1.05V 2A
+1_5VRUN 1.5V 2.75A
VCC3 3.3V 0.4A
V5REF 5V 6mA
VCC3_SB 3.3V 0.3A
V5REF_SUS 5V 0.01A
VCCRTC 3V 2mA
0.01A
SIO(Fintek 71882)
VCC3 35mA
VCCRTC 2.4uA
VCC3
VCC5
VCC3_SB
VCC5_SB
VCCRTC
LAN1
VCC3_SB 1.2A+1.2A=2.4A
1.8V 1.2A
1.0V 1.2A
LAN2
VCC3_SB 1.2A+1.2A=2.4A
1.8V 1.2A
1.0V 1.2A
SYS FAN1
+12V 0.7A
SYS FAN2
+12V 0.7A
SATA HDD 3.5" POWER x 5
+5V 1A x 5 = 5A
+12V 0.8A X 5 = 4A
CLK Gen REALTEK/RTM875T-605
3.3V 200mA
PS2251
3.3V 200mA
Core 1.8V
NAND Flash
3.3V 50mA
ISL6545CBZ
USB_VCC
VCC5_SB 5A
USB 2.0
+5V (9 Ports) 4.5A
UP7536AMA8
VCC_US#
VCC5_SB 3A
USB 3.0
+5V (2 Ports) 1.8A
UP6301D
VCC_1P05 600mA
VCC3_SB
uPD720200 USB 3.0 Controller
VCC_1P05 600mA
3.3V 100mA
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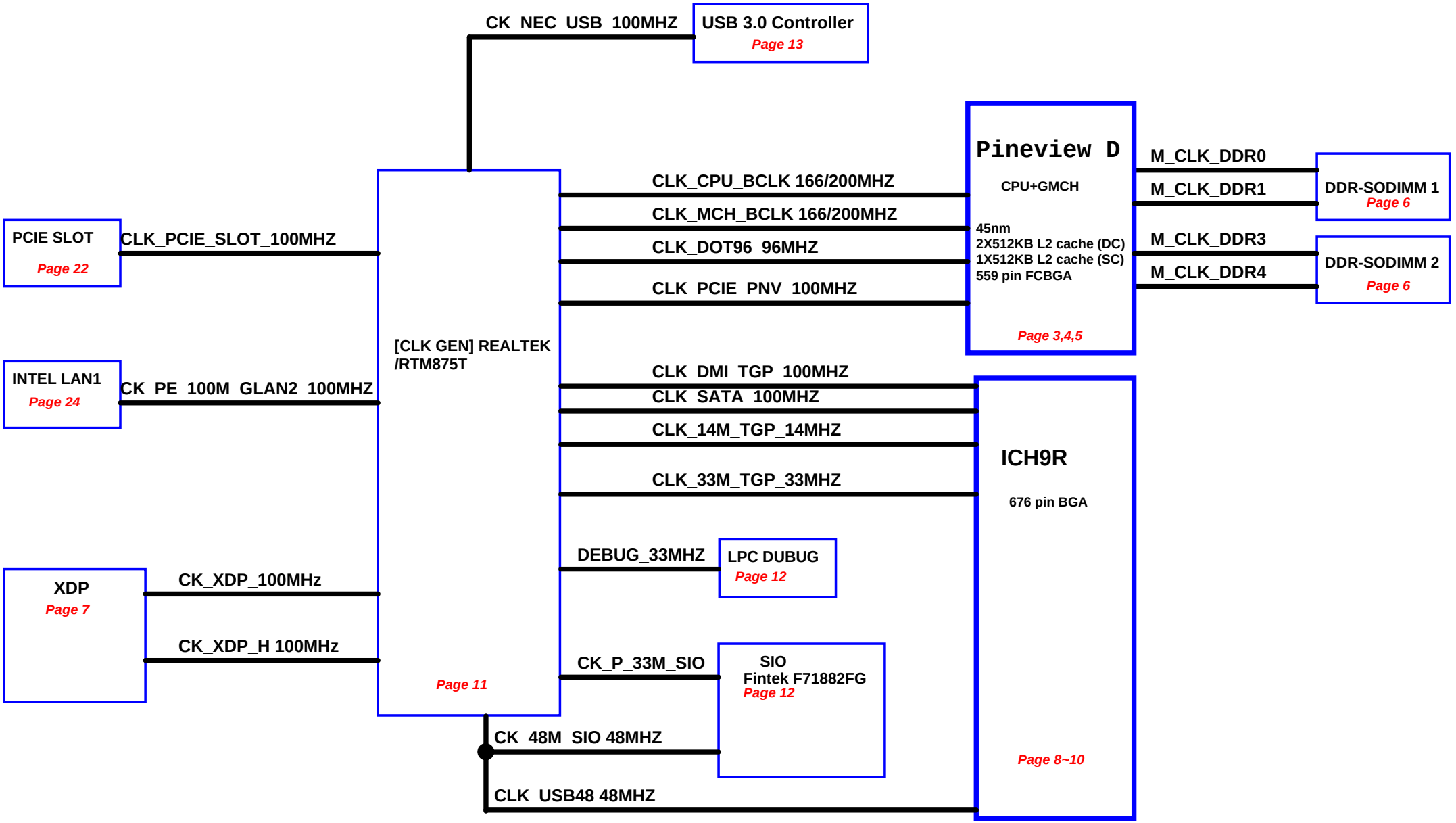

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2010/09/27 Version Change to 1.0 (MVT Build 1)

* Update power solution

VCORE: R403 was 330 ohm change to 422 ohm, (OCP=15.5A)
+1_5VDIMM : R349 was 150K change to120K, C314 was 220pF change to 330pF
VCC3_SB: R671 was 3.24K change to 3.16K ohm, R659 was 2K change to12K ohm,
C580 was 0.01uF change to 0.1uF
USB_VCC: R529 was 2K change to 4.53K

*Modify CK_PWRGD Circuit

To change CK_PWRGD after CPU_BSEL (FSA,B,C)
Add RC delay & Smith trigger after +1_5VRUN

* Add LAN2 LED Reserved Resistor

To meet the LAN LED Spec:
Add 0 ohm, R554 & R555 (Stuff), R522, R509 (Reserved)

* Add LAN1 CON Power

Add LAN1 power 1.8V & 0 ohm, R215

* Update SIO F71882FG Setting

Net: S_COPEN_L add MLCC 1000pF to GND
No Stuff R254, GPIO13 used for GPIO function
Input pin pull up to 3VCC for FDC/URAT2 No Used

* Add Dual Source for S3 Requirement

Add diode SS34 at VCC5_SB and P-MOS at +12V for +1_5VDIMM source
Change: Stuffing R346; No Stuff R454,R363

* PROCHOT# Resistor Update

Change: R8 = Ohm

* Front Panel LED Update

Change: Modify RES array RN35 to replace R39,R315,R484,R516
Add Q83 & R77 for Power LED control by LED_VCC
Add F71882 pin65 for LED_VCC control, No Stuff R278,R280

* LAN_USB Connector Update

Swapping Reference on connector LAN_USB1 & LAN_USB2

2010/11/11 1.0 (MVT Build 2)

L21, L23, L24 update package to 0603
R319 change to 75K ohm for +1_5VRUN turn on
R346 change to 470K ohm, add C309 1uF/10V,C422 0.1uF/16V for POS solution.

2010/12/07 1.0 (MP BOM)

* Update power solution fine tune

+1_5VDIMM : C314 was 220pF change to 1000pF,C315 was 22pF change to 15pF
USB_VCC: R529 was 4.53K change to 3.6K

* Update EMI solution

No stuff: C463,C488,C531,C553

2010/12/27 1.1

* Change power solution

Add alternate circuit on +1_5VRUN enable for POS

* Change power solution

Remove UPI solution at U35 (for VCC_1P05)
Add U12 (for VCC_1P05)

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