HELLCAT 13" Schematics
Comet Lake-U

2019-10-27

REV : DVT1

DY : None Installed
UMA: UMA only installed

<Core Design>

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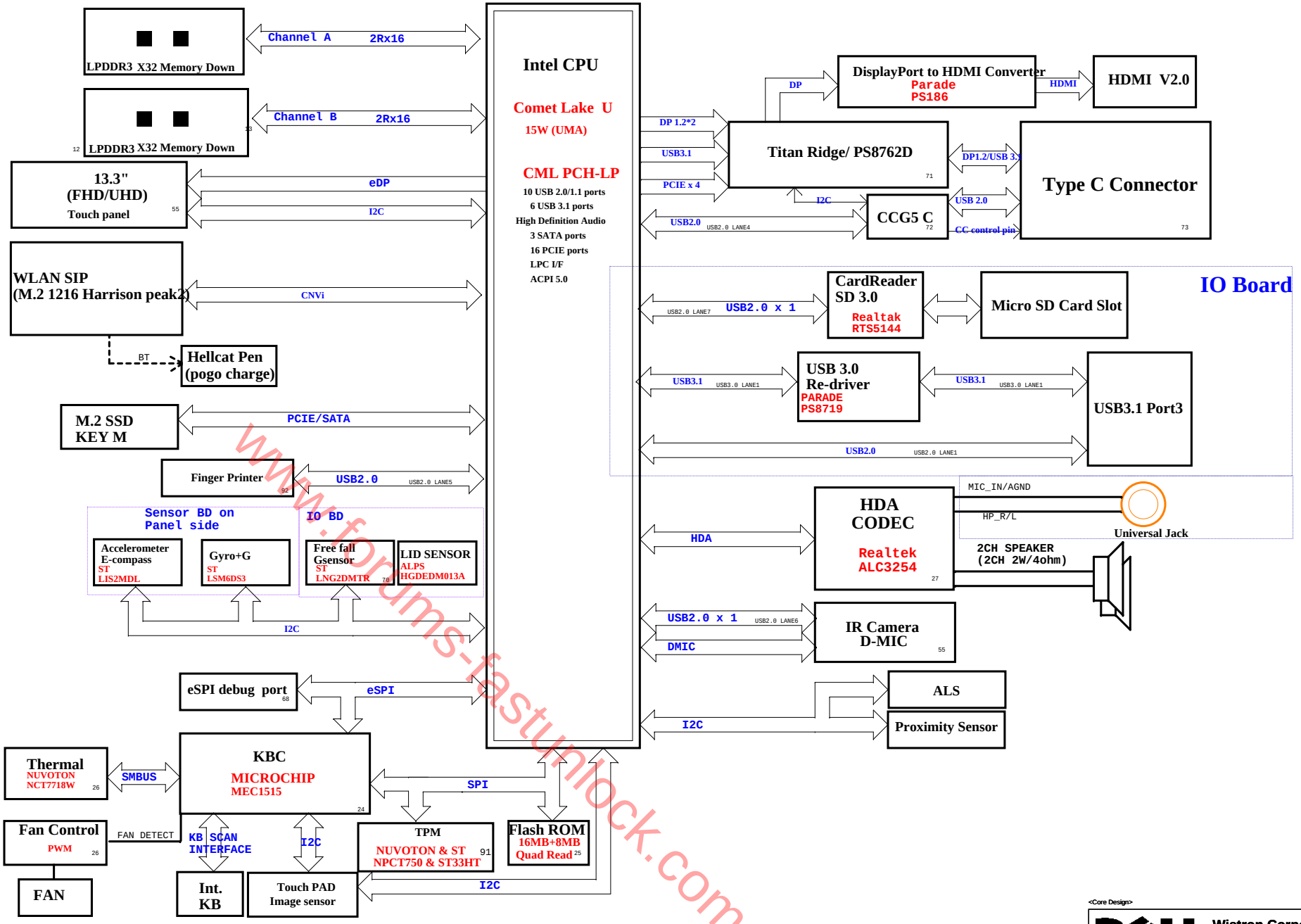
Title	Cover Page	
Size: A3	Document Number: JEDI 13"	Rev: SC
Date: Monday, October 28, 2019	Sheet 1 of 106	

CML-U 13" CPU 15W Block Diagram

Project code:
PCB P/N: 19721
Revision: SA



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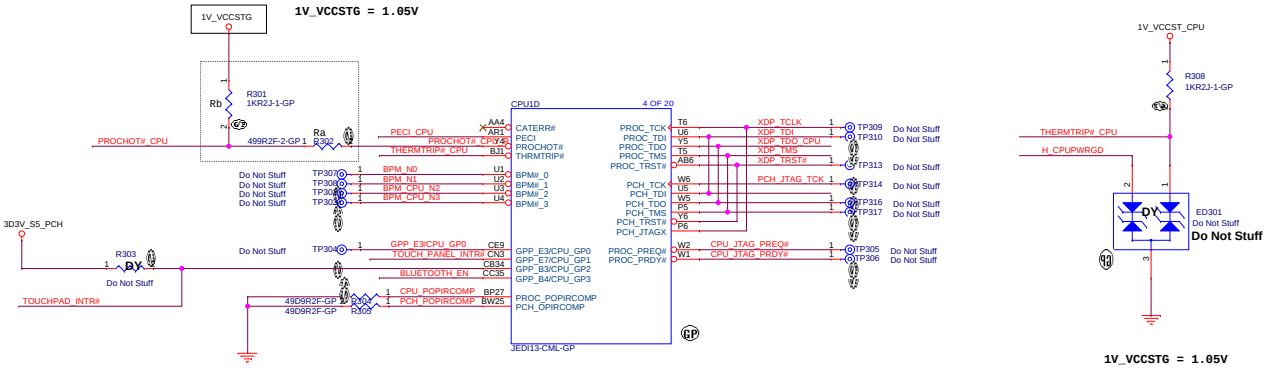
Title: Block Diagram

Size	Document Number	Rev
C	JEDI 13"	SC

Date: Monday, October 28, 2019 Sheet 2 of 106

Main Func = CPU

61 BLUETOOTH_EN
24 PECI_CPU
24,44,46,72 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TOUCHPAD_INTR#
17 H_CPUPWRGD



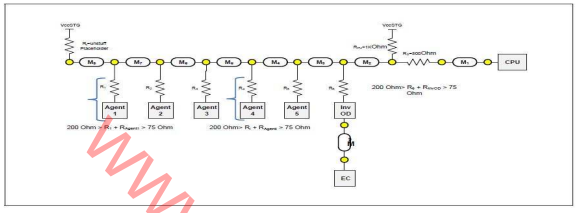


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

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Title: THML/JTAG
Size: A2
Document Number: JEDI 13"
Rev: SC
Date: Monday, October 28, 2019
Sheet 3 of 106

Main Func = CPU

Edp

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU

24 L_BKLT_EN
55 EDP_VDD_EN
55 L_BKLT_CTRL

DP to MUX

71 DP1_DDI_TX_N0
71 DP1_DDI_TX_P0
71 DP1_DDI_TX_N1
71 DP1_DDI_TX_P1
71 DP1_DDI_TX_N2
71 DP1_DDI_TX_P2
71 DP1_DDI_TX_N3
71 DP1_DDI_TX_P3

71 DP1_AUX_CPU_N
71 DP1_AUX_CPU_P

71 DP_HPD_CPU

DP to AR

71 DP2_DDI_TX_N0
71 DP2_DDI_TX_P0
71 DP2_DDI_TX_N1
71 DP2_DDI_TX_P1
71 DP2_DDI_TX_N2
71 DP2_DDI_TX_P2
71 DP2_DDI_TX_N3
71 DP2_DDI_TX_P3

71 DP2_AUX_CPU_P
71 DP2_AUX_CPU_N

71 DP2_HPD_CPU

15 GPP_H17_STRAP

55 CAM_SHUTTER#

eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 or 100 Ω ±1%	600 mils

Note: Must maintain low DC resistance routing (<0.1Ω)

CPU1A — 1 OF 20 — JEDI13-CML-GP

DP to AR

DP1_DDI_TX_N0 AL5 — DDI1_TXN_0
DP1_DDI_TX_P0 AL6 — DDI1_TXP_0
DP1_DDI_TX_N1 AJ5 — DDI1_TXN_1
DP1_DDI_TX_P1 AJ6 — DDI1_TXP_1
DP1_DDI_TX_N2 AF6 — DDI1_TXN_2
DP1_DDI_TX_P2 AF5 — DDI1_TXP_2
DP1_DDI_TX_N3 AE5 — DDI1_TXN_3
DP1_DDI_TX_P3 AE6 — DDI1_TXP_3

DP to AR

DP2_DDI_TX_N0 AC4 — DDI2_TXN_0
DP2_DDI_TX_P0 AC3 — DDI2_TXP_0
DP2_DDI_TX_N1 AC1 — DDI2_TXN_1
DP2_DDI_TX_P1 AC2 — DDI2_TXP_1
DP2_DDI_TX_N2 AE4 — DDI2_TXN_2
DP2_DDI_TX_P2 AE3 — DDI2_TXP_2
DP2_DDI_TX_N3 AE1 — DDI2_TXN_3
DP2_DDI_TX_P3 AE2 — DDI2_TXP_3

EDP_TXN_0 AG4 — eDP_TX_CPU_N0
EDP_TXP_0 AG3 — eDP_TX_CPU_P0
EDP_TXN_1 AG2 — eDP_TX_CPU_N1
EDP_TXP_1 AG1 — eDP_TX_CPU_P1
EDP_TXN_2 AJ4 — eDP_TX_CPU_N2
EDP_TXP_2 AJ3 — eDP_TX_CPU_P2
EDP_TXN_3 AJ2 — eDP_TX_CPU_N3
EDP_TXP_3 AJ1 — eDP_TX_CPU_P3

EDP_AUX_N AH4 — eDP_AUX_CPU_N
EDP_AUX_P AH3 — eDP_AUX_CPU_P

DISP_UTILS AM7

DDI1_AUX_N AC7 — DP1_AUX_CPU_N
DDI1_AUX_P AC6 — DP1_AUX_CPU_P
DDI2_AUX_N AD4 — DP2_AUX_CPU_N
DDI2_AUX_P AD3 — DP2_AUX_CPU_P
DDI3_AUX_N AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 — DP1_HPD_CPU_R
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 — DP2_HPD_CPU_R
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 — SIO_EXT_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 — IR_CAM_DET#
GPP_E17/EDP_HPD/DISP_MISC4 CM7 — eDP_HPD_CPU

EDP_BKLTEN CK11 — L_BKLT_EN
EDP_VDDEN CG11 — EDP_VDD_EN
EDP_BKLTCTL CH11 — L_BKLT_CTRL

1V_VCCIO
R401 24D9R2F-L-GP
eDP_RCOMP_CPU AM6 — DISP_RCOMP

PH/PL on TBT Page
CPU_DP1_CTRL_CLK CC8 — GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
CPU_DP1_CTRL_DATA CC9 — GPP_E19/DPPB_CTRLDATA
CPU_DP2_CTRL_CLK CH4 — GPP_E20/DPPC_CTRLCLK
CPU_DP2_CTRL_DATA CH3 — GPP_E21/DPPC_CTRLDATA

CAM_SHUTTER# CP4 — GPP_E22/DPPD_CTRLCLK
CN4 — GPP_E23/DPPD_CTRLDATA

CR26 — GPP_H16/DDPF_CTRLCLK
GPP_H17_STRAP CP26 — GPP_H17/DDPF_CTRLDATA

For AR

3D3V_S0
SIO_EXT_SMI# — R402 10KR2J-3-GP
3D3V_S0
MS — R409 10KR2J-3-GP
IR_CAM_DET#
UPSELL — R411 Do Not Stuff

3D3V_S0 — RN401 SRN2K2J-5-GP — CPU_DP2_CTRL_CLK, CPU_DP2_CTRL_DATA
3D3V_S0 — RN402 SRN2K2J-5-GP — CPU_DP1_CTRL_CLK, CPU_DP1_CTRL_DATA

3D3V_S5_PCH
R405 10KR2J-3-GP
Q401 2N7002KDW-1-GP
R406 10KR2J-3-GP
CPU_DP_HPD_P
DP1_HPD_CPU_R
DP_HPD_CPU
R403 100KR2J-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

3D3V_S5_PCH
R407 10KR2J-3-GP
Q402 2N7002KDW-1-GP
R408 10KR2J-3-GP
CPU_DP2_HPD_P
DP2_HPD_CPU_R
DP2_HPD_CPU
R410 100KR2J-1-GP
75.27002.F7C
2nd = 075.27002.0E7C

Hynix 16G MS SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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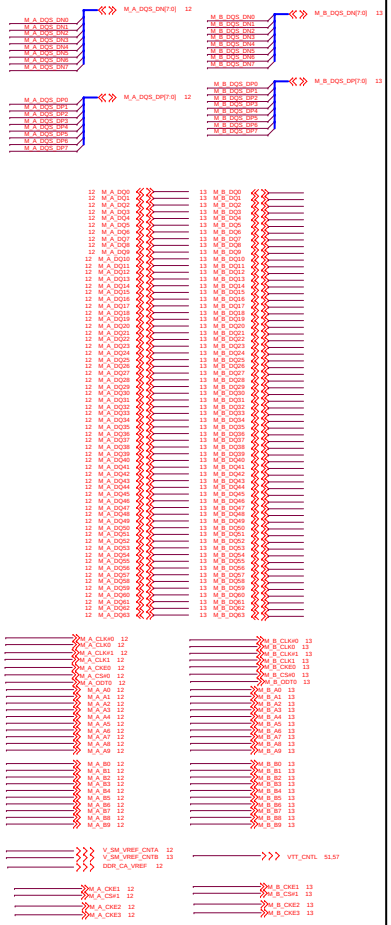
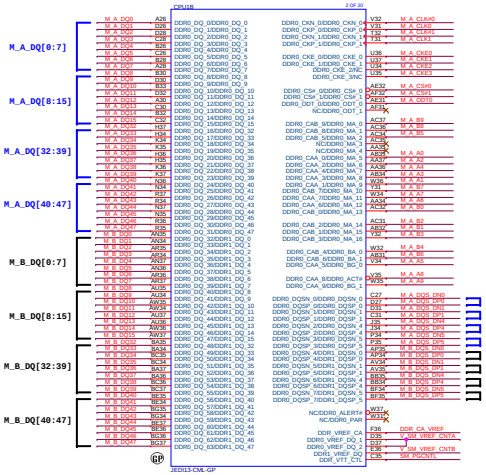
Title: CPU_(JTAG/CPU SIDE BAND)
Size: A3 | Document Number: Jedi CML | Rev: SC
Date: Monday, October 28, 2019 | Sheet 4 of 106

Main Func = CPU

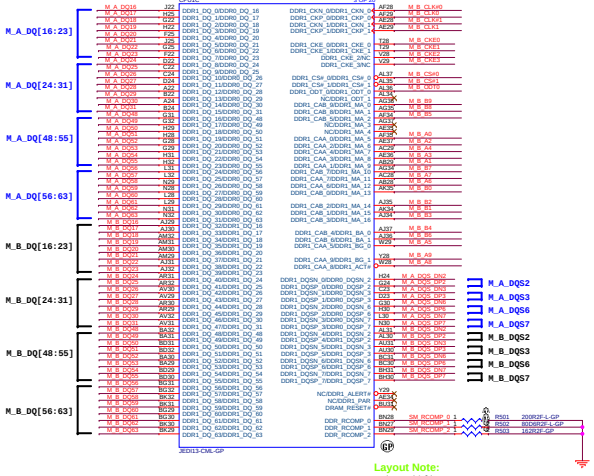
DDR4 ball type: Non-Interleaved Type





M_A_DQ[0:7]
M_A_DQ[8:15]
M_A_DQ[32:39]
M_A_DQ[40:47]
M_B_DQ[0:7]
M_B_DQ[8:15]
M_B_DQ[32:39]
M_B_DQ[40:47]

M_A_DQS0
M_A_DQS1
M_A_DQS4
M_A_DQS5
M_B_DQS0
M_B_DQS1
M_B_DQS4
M_B_DQS5



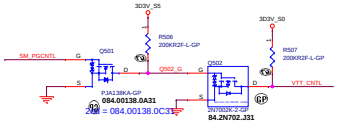
M_A_DQ[16:23]
M_A_DQ[24:31]
M_A_DQ[48:55]
M_A_DQ[56:63]
M_B_DQ[16:23]
M_B_DQ[24:31]
M_B_DQ[48:55]
M_B_DQ[56:63]

M_A_DQS2
M_A_DQS3
M_A_DQS6
M_A_DQS7
M_B_DQS2
M_B_DQS3
M_B_DQS6
M_B_DQS7

Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

	Resistor Value	Length
RCOMP[0]	200R_1%	Max = 500 mils
RCOMP[1]	80.6R_1%	Max = 500 mils
RCOMP[2]	162R_1%	Max = 500 mils

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



84.00138.0A31
2nd = 084.00138.0C31

84.2N702.J31
2nd = 084.27002.0N31

Hynix 16G MS SKU1

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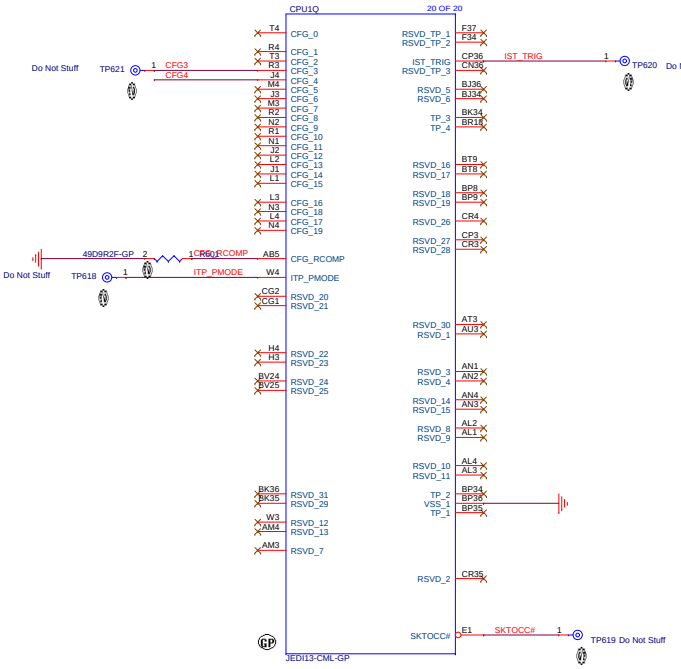
Title: CPU (DDR)

Size	Document Number	Rev
A1	JEDI 13"	SC

Date: Monday, October 29, 2018 Sheet 5 of 58

Main Func = CPU



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Title: CPU (CFG/IST)

Size	Document Number	Rev
A2	JEDI 13"	SC

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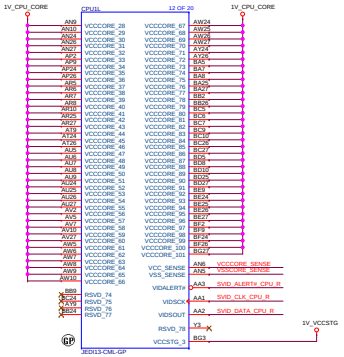
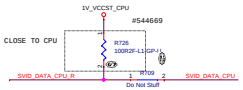
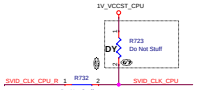


Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA



SVID CLOCK



#544669
CLOSE TO VR

SVID ALERT

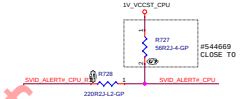
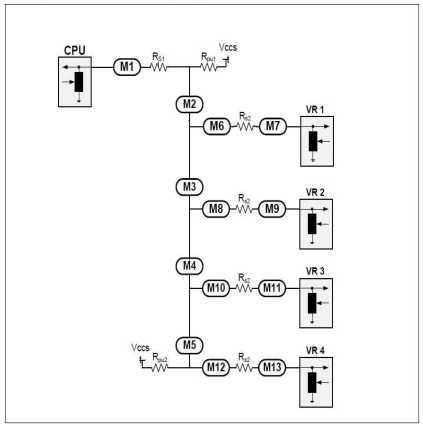
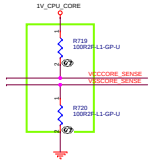


Figure 7-19. Routing Illustration for SVID Topology



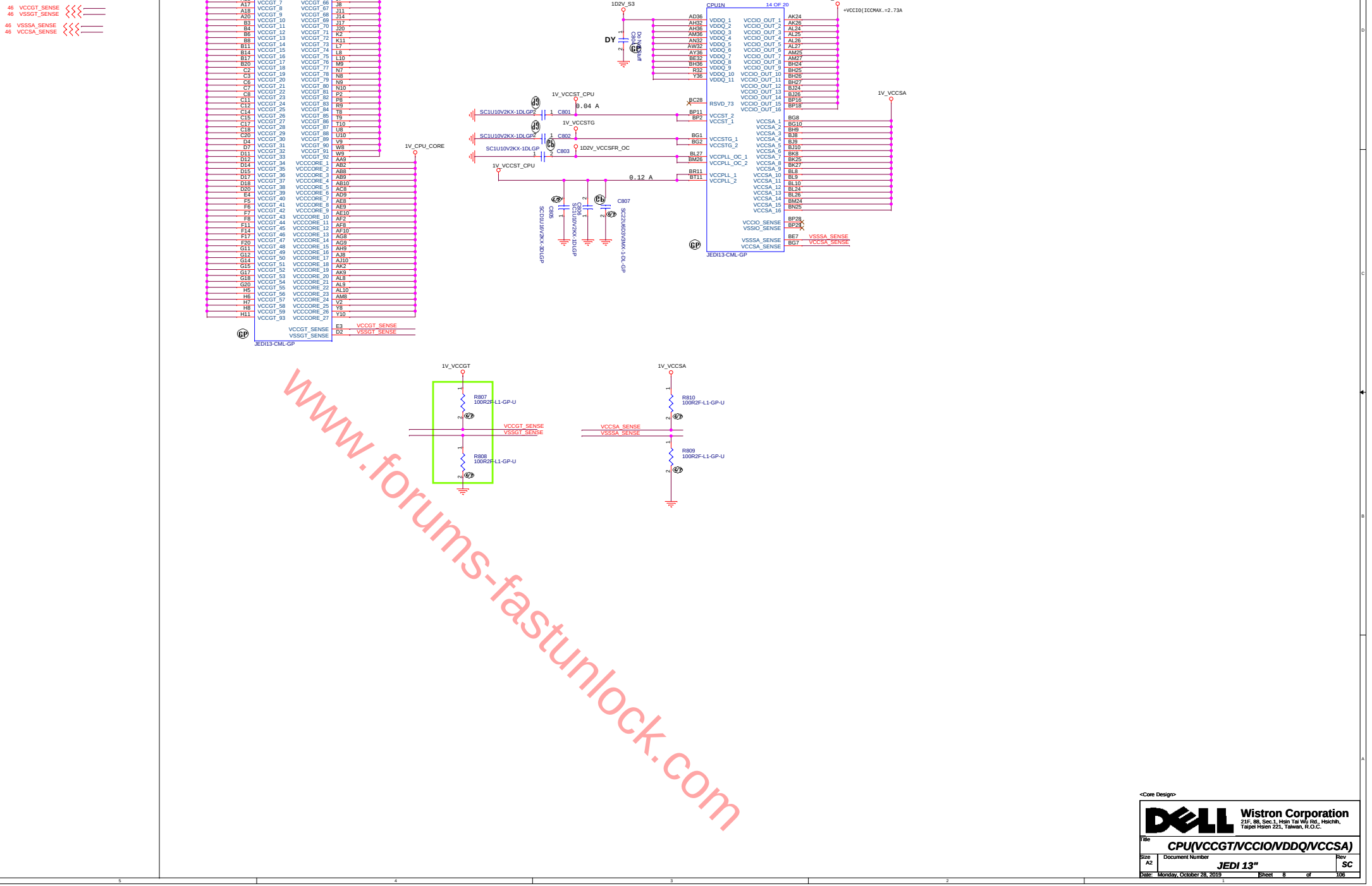


Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11
Topology Guidelines							
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#						
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω						
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω						
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω						
Platform resistors tolerances	± 5%						
Route ordering	When routing at minimum spacing route Alert between Data and Clock						
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK	± 100mils						

Main Func = CPU



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Title: CPU(VCCGT/VCCIO/VDDQ/VCCSA)

Size	Document Number	Rev
A2	JEDI 13"	SC

Date: Monday, October 28, 2019 Sheet 8 of 106

(Blanking)

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Title: *(Reserved)*

Size: A3 | Document Number: *JEDI 13"* | Rev: *SC*

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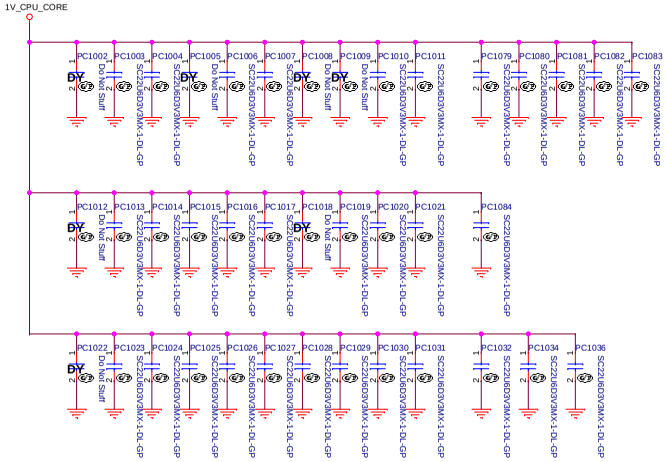
Main Func = CPU

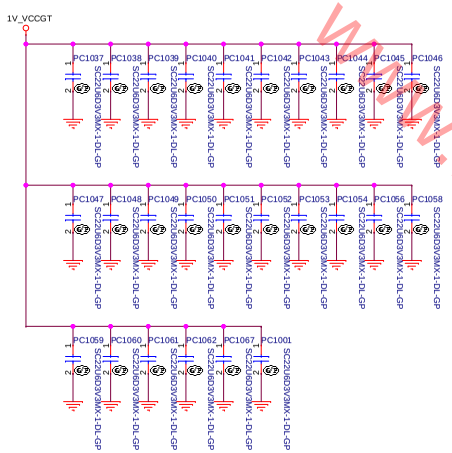
1V_CPU_CORE

22U 0603 x 42



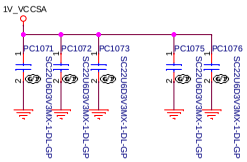
VCCGT

22U 0603 x 26



VCCSA

22U 0603 x 5



Hynix 16G MS SKU1

Wistron Corporation
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Title: CPU (Power CAP1)

Size: A2 | Document Number: Jedi15"/17" CML | Rev: SC

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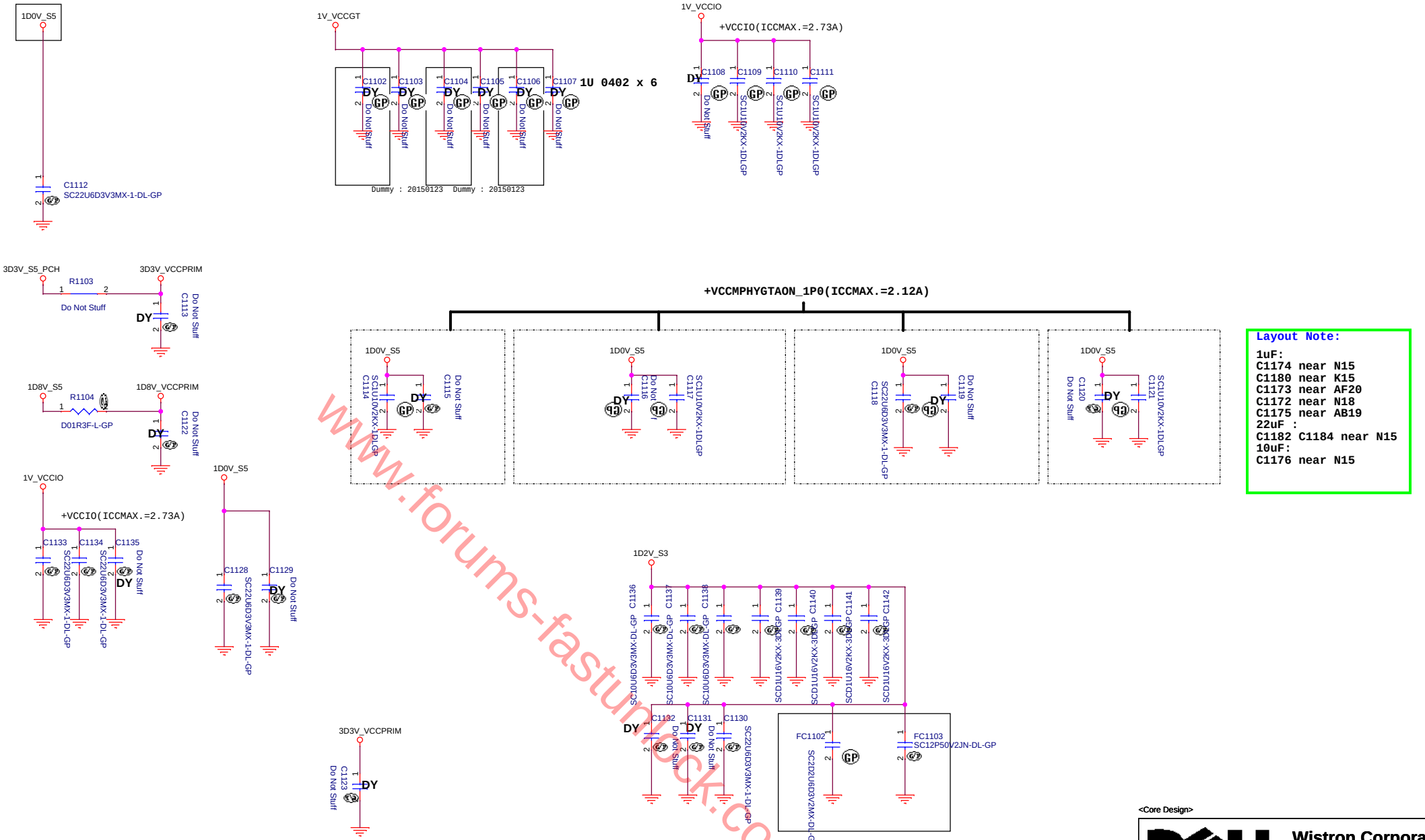
Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

<Core Design>

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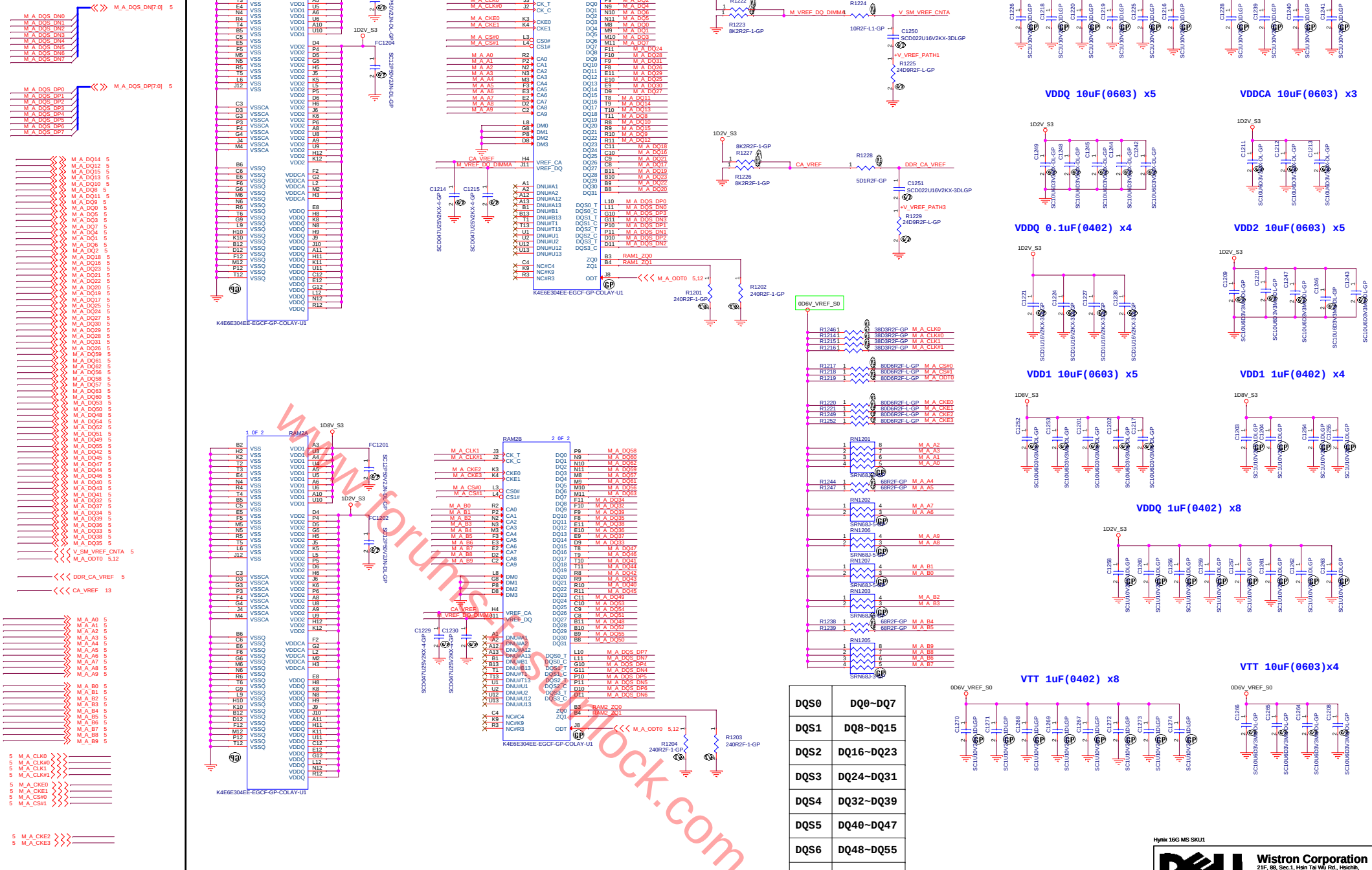
Title	CPU (Power CAP2)	
Size A3	Document Number JEDI 13"	Rev SC
Date: Thursday, October 31, 2019	Sheet 11 of 106	

Main Func = MEMORY



DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

VDD2 1uF(0402) x6

VDDCA 1uF(0402) x4

VDDQ 10uF(0603) x5

VDDCA 10uF(0603) x3

VDDQ 0.1uF(0402) x4

VDD2 10uF(0603) x5

VDD1 10uF(0603) x5

VDD1 1uF(0402) x4

VDDQ 1uF(0402) x8

VTT 1uF(0402) x8

VTT 10uF(0603)x4

Hynix 16G MS SKU1

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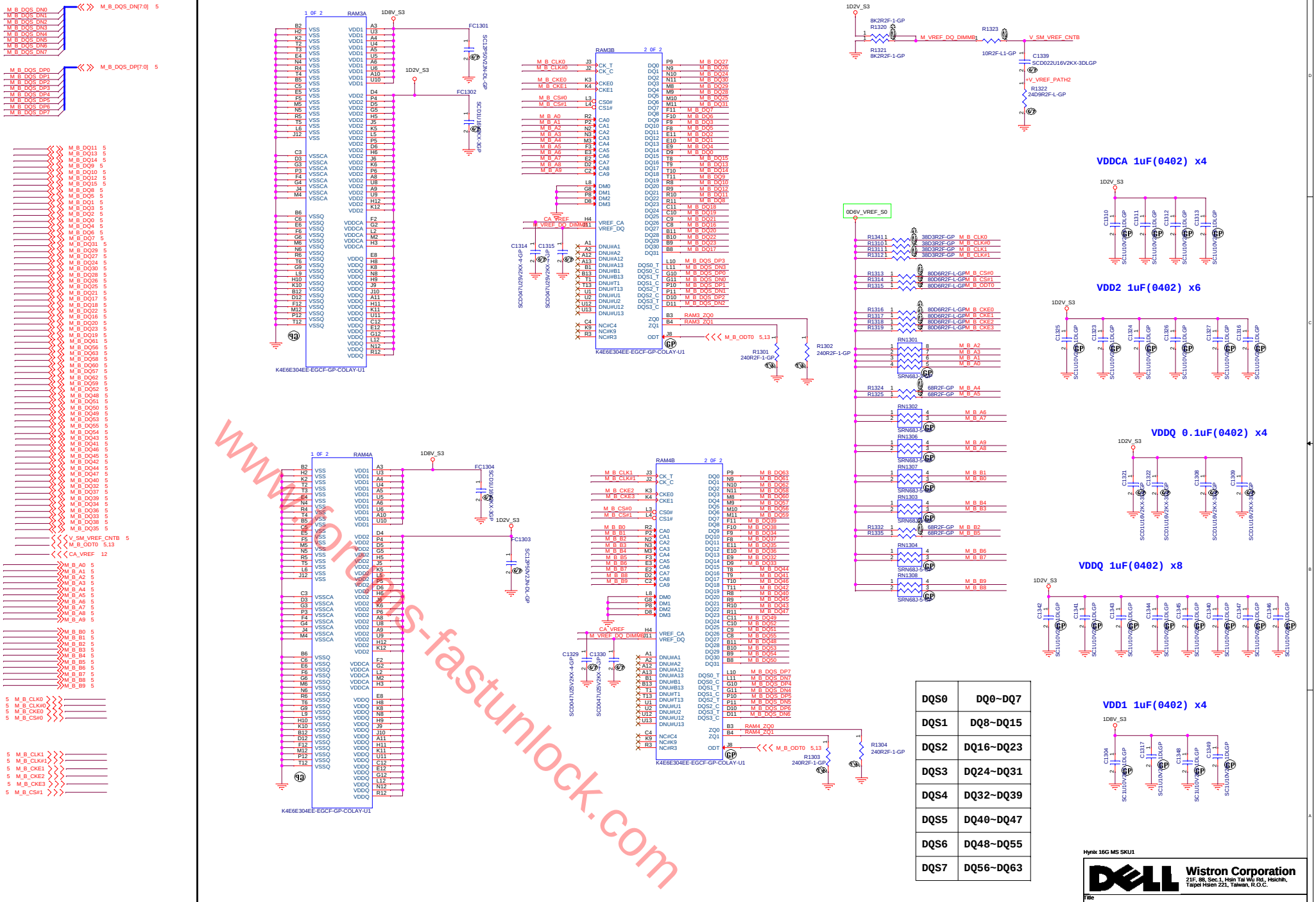
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPDDR3

Size: A2 | Document Number: JEDI 13" | Rev: SC

Date: Monday, October 28, 2019 | Sheet 12 of 106

Main Func = MEMORY



DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

Hynix 16G MS SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPDDR3

Size: A2 | Document Number: JEDI 13" | Rev: SC

Date: Monday, October 28, 2019 | Sheet 13 of 106

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

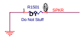
Size	Document Number	Rev
A4	*JEDI 13"*	*SC*

Date: Monday, October 28, 2019 Sheet 14 of 106

Main Func = PCH

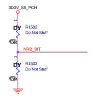
19,27 SPKR
20 NRB_BIT
18 CPU_SMB_ALERT#_P0
18 SPI_SI_CPU
18 SPI_WP_CPU
18 SPI_HOLD_CPU
19 HDA_SDOUT_CPU
20,61 CNV_RGI_DT
6 CFG3
6 CFG4
18 CPU_SMB_ALERT#
20 GPP_B22_GSPI1_MOSI
18 CPU_SMB_ALERT#_P1
21 GPP_H21
17 INPUT3VSEL
21 GPP_H23
21 GPD_7
20,25 RTC_DET#
4 GPP_H17_STRAP

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.



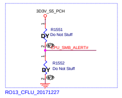
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18

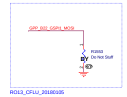


GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2

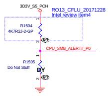


GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.



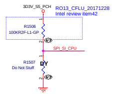
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5



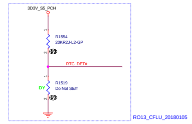
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI



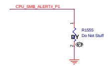
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12



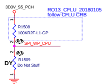
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

GPP_B23



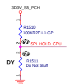
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2



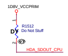
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3



HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

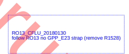
GPP_R2 / HDA_SDO / I2S0_TXD / HDACPU_SDO



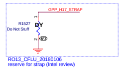
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

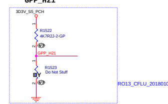


GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.



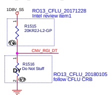
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

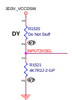


GPP_F6 / CNV_RGI_DT	M.2 CNVi Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

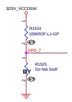
GPP_F2 / CNV_RGI_DT / UART0_TXD



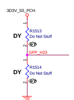
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5%	**Note:** This strap should only be used for specific targeted 1S battery systems.



GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

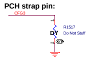


GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**



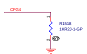
[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

PCH strap pin:



(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



Wistron Corporation
CPU (STRAP)
JEDI 13"

Main Func = PCH

USB3.0

66 USB1_USB30_RX_N
66 USB1_USB30_RX_P
66 USB1_USB30_TX_N
66 USB1_USB30_TX_P

71 USB4_USB30_RX_N
71 USB4_USB30_RX_P
71 USB4_USB30_TX_P
71 USB4_USB30_TX_N

USB2.0

72 USB4_USB20_N
72 USB4_USB20_P
66 USB1_USB20_N
66 USB1_USB20_P
55 CCD_USB20_N
55 CCD_USB20_P
66 CARD1_USB20_N
66 CARD1_USB20_P

92 FP1_USB20_N
92 FP1_USB20_P

71 TBT_CIO_PLUG_EVB
71 TBT_FORCE_PWR

66 USB_OCD#
63 SSD_DEVSLP
63 M2_SSD_PEDET
64 PCH_SATA_LED#
20,24 TABLE_MODE#

PCIE

63 SSD_PCIE_RX_N3
63 SSD_PCIE_RX_P3
63 SSD_PCIE_TX_N3
63 SSD_PCIE_TX_P3
63 SSD_PCIE_RX_N2
63 SSD_PCIE_RX_P2
63 SSD_PCIE_TX_N2
63 SSD_PCIE_TX_P2
63 SSD_PCIE_RX_N1
63 SSD_PCIE_RX_P1
63 SSD_PCIE_TX_N1
63 SSD_PCIE_TX_P1
63 SSD_SATA_RX_N
63 SSD_SATA_RX_P
63 SSD_SATA_TX_N
63 SSD_SATA_TX_P

71 TBT_PCIE_TX_CON_P8
71 TBT_PCIE_TX_CON_N8
71 TBT_PCIE_TX_CON_P7
71 TBT_PCIE_TX_CON_N7
71 TBT_PCIE_TX_CON_P6
71 TBT_PCIE_TX_CON_N6
71 TBT_PCIE_TX_CON_P5
71 TBT_PCIE_TX_CON_N5
71 TBT_PCIE_RX_P8
71 TBT_PCIE_RX_N8
71 TBT_PCIE_RX_P7
71 TBT_PCIE_RX_N7
71 TBT_PCIE_RX_P6
71 TBT_PCIE_RX_N6
71 TBT_PCIE_RX_P5
71 TBT_PCIE_RX_N5

WLAN

TBT

SSD

CPU1H 8 OF 20

IO board USB3.1

TYPE-C USB3.1

IO board USB3.1

USB3.1 Type C Fingerprint

CAMERA

Card Reader

WLAN (BT)

When used as DEVSLP_ no external pull-up or pull-down termination required from SATA Host DEVSLP.

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

USB 2.0 Table

Pair	Device
1	USB3.0 port1 (IOBD)
2	N/A
3	N/A
4	Type-c
5	FingerPrint
6	CAMERA
7	Card Reader
8	N/A
9	N/A
10	WLAN (BT)

	USB2.0 (10 Ports)									
Premium / Base	USB2 #1	USB2 #2	USB2 #3	USB2 #4	USB2 #5	USB2 #6	USB2 #7	USB2 #8 (Premium-U only)	USB2 #9 (Premium-U only)	USB2 #10
CY18 Port Mapping	External Port /Type-C #1	External Port /Type-C #2	External Port /Type-C #3	External Port /Type-C #4	FingerPrint	Camera	Card Reader			BT
RO13_WHL	USB2.0 (IO board)			TYPE-C	FingerPrint	Camera				BT

Hynix 16G MS SKU1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A1 | Document Number: Jedi CML | Rev: SC

Date: Monday, October 29, 2018 | Sheet 16 of 38

Main Func = PCH

24 SYS_PWROK
24,26 IMVP_VR_ON
24,40,44,46 VCCST_PWRGD
24,64 PCH_RSMRST#
25,45 3V_5V_PWRGD
40 PM_SLP_S3#
40,51,55,71 PM_SLP_S3#
40,51 PM_SLP_S4#
24 SIO_PWRBTN#
44 AC_IN#
40,61,63,71 PLTRST#_CPU
3 H_CPUPWRGD
15 INPUT3VSEL
71 PCIE_WAKE#_CPU

3D3V_VCCDSW
RN1704
PCIE_WAKE#_CPU
AC_PRESENT
SRN10KJ-5-GP
RTC_AUX_S5
R1730
330KR2J-L1-GP
SM_INTRUDER#
3D3V_VCCPRIM
R1731
100KR2F-L1-GP
EXT_PWR_GATE#
3D3V_S5
R1721
10KR2J-3-GP
GPD11/LANPHYPC
1D8V_VCCPRIM
R1738
ME_SUS_PWR_ACK_R
Do Not Stuff

3D3V_VCCDSW
R1722
10KR2J-3-GP
PCH_BATLOW#
R1723
Do Not Stuff

3D3V_VCCPRIM
R1701
10KR2J-3-GP
XDP_DBRESET#
Do Not Stuff
TP1712
TP1713
PCH_PLTRST#
PM_RSMRST#
H_CPUPWRGD
VCCST_PWRGD_R
TP1705
IMVP_VR_ON
PM_RSMRST#
R1705 1
R1704 1
0R2J-2-GP
0R2J-2-GP
SYS_PWROK
PCH_PWROK
DSW_PWROK
ME_SUS_PWR_ACK_R
SUSACK#_R
PCIE_WAKE#_CPU
LAN_WAKE#
GPD11/LANPHYPC
3D3V_VCCDSW
R1707
10KR2J-3-GP
CPU1K
11 OF 20
GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGDOD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
JEDI13-CML-GP
BJ37 PM_SLP_S0#
BU36 PM_SLP_S3#
BU27 PM_SLP_S4#
BT26 PM_SLP_S5#
BU26
BT19
BU28 SIO_PWRBTN#
BU38 AC_PRESENT
BV36 PCH_BATLOW#
BR35 SM_INTRUDER#
CC37 EXT_PWR_GATE#
CC36 VRALERT#
BT27 INPUT3VSEL
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#
INPUT3VSEL
TP1711 Do Not Stuff
TP1707 Do Not Stuff
TP1709 Do Not Stuff
TP1710 Do Not Stuff
TP1715 Do Not Stuff
TP1706 Do Not Stuff
TP1714 Do Not Stuff
TP1708 Do Not Stuff

BATLOW#:
Pull-up required even if not implemented.

AC_PRESENT
EC1707
Do Not Stuff

PLTRST#_CPU
R1713
0R2J-2-GP
PCH_PLTRST#
R1715
Do Not Stuff
C1701
Do Not Stuff

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

RN1703
PM_RSMRST#
PM_PCH_PWROK
SRN100KJ-6-GP
SYS_PWROK
R1717
100KR2F-L1-GP
R1714
H_CPUPWRGD
Do Not Stuff

ME_SUS_PWR_ACK_R
R1708
SUSACK#_R
Do Not Stuff

3D3V_S0
R1718
Do Not Stuff
VCCST_PWRGD
R1710
100KR2F-L1-GP
VCCST_PWRGD_R
R1719
47KR2F-GP
C1711
Do Not Stuff

3D3V_AUX_S5
R1727
100KR2J-L-GP
R1726
10KR2J-3-GP
Q1701
3V_5V_POK#
PJT138KA-GP
PM_RSMRST#
1KR2J-1-GP
R1702
PCH_RSMRST#
3V_5V_PWRGD
075.00138.047C
2nd = 075.00138.047C

XDP_DBRESET#
SYS_PWROK
PCH_RSMRST#
PLTRST#_CPU
ED1702
AZ5125-02S-R7G-GP
ED1701
AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.52215.007D
75.05125.07D
2nd = 075.52215.007D

3D3V_AUX_S5
D1701
RB520S30-GP
81.R0903.A8M
2ND = 083.52030.008F
AC_IN#
R1737
100KR2J-1-GP
PM_RSMRST#_M
Q1702
AC_PRESENT
PM_RSMRST#
common part
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
Reserve by NON DS3 function 20150413

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (POWER MANAGEMENT)
Size Custom
Document Number
JEDI 13"
Rev SC
Date: Monday, October 28, 2019
Sheet 17 of 105

Main Func = PCH

15 CPU_SMB_ALERT#_P1

63 SSD_CLK_CPU_N
63 SSD_CLK_CPU_P
63 SSD_CLKREQ_CPU_N

24,25 SPI_CLK_ROM
24,25 SPI_SO_ROM
24,25 SPI_SI_ROM
24,25 SPI_WP_ROM
24,25 SPI_HOLD_ROM

15 SPI_SI_CPU
15 SPI_WP_CPU
15 SPI_HOLD_CPU
24,25 SPI_CS_CPU_N0
24,25 SPI_CS_CPU_N1

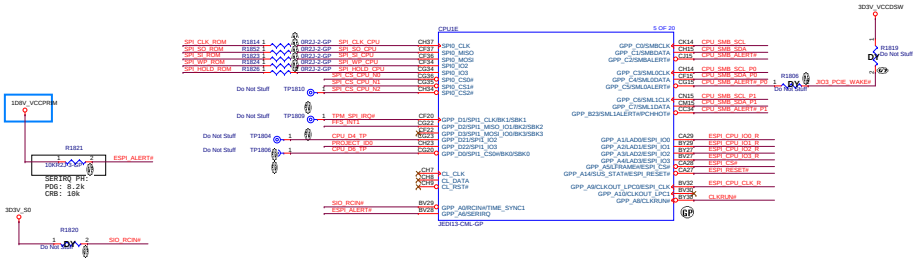
24,68 ESPI_IO[3..0]
ESPI_IO3
ESPI_IO1
ESPI_IO2
ESPI_IO0

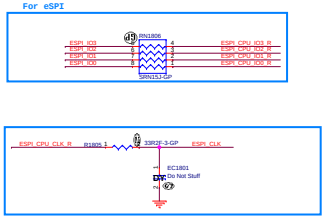
24,26,92 CPU_SMB_SCL_P0
24,26,92 CPU_SMB_SDA_P0
24,68 ESPI_CS#
24,68 ESPI_RESET#

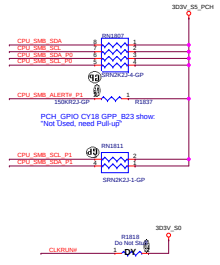
24,61 SUS_CLK_R
24,68 ESPI_CLK
66 FFS_INT1

15 CPU_SMB_ALERT#_P0
21 PROJECT_ID0
15 CPU_SMB_ALERT#_P1
61 PULSAR_38P4M_REFCLK

71 TBT_CLK_CPU_N
71 TBT_CLK_CPU_P
71 TBT_CLKREQ_CPU_N







For eSPI

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

CPU_SMB_ALERT#_P0

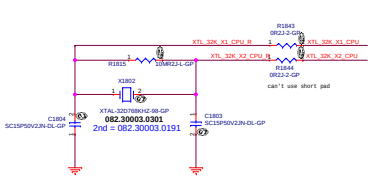
PCH strap pin:

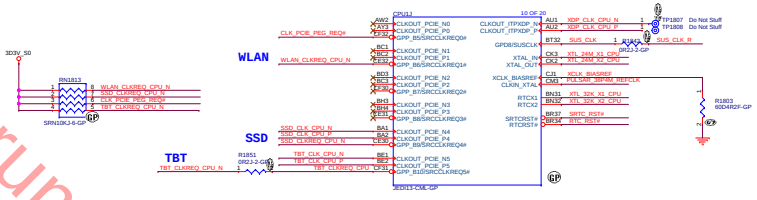
eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

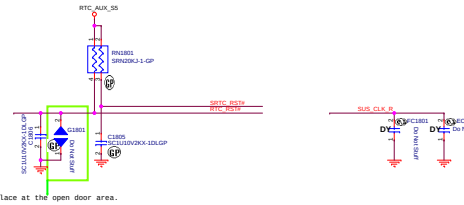
This signal has a weak internal pull-down.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit B8S	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6: 0 = SPI (Default); 1 = LPC. Notes: 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GBE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC. Notes: 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.







Layout: Place at the open door area.

Hynix 16G MS SKU1

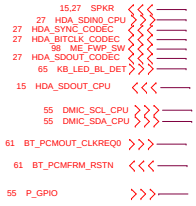
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

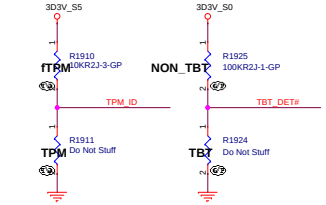
Title: CPU (LPC/SPI/SMBUS/CL/CLK)

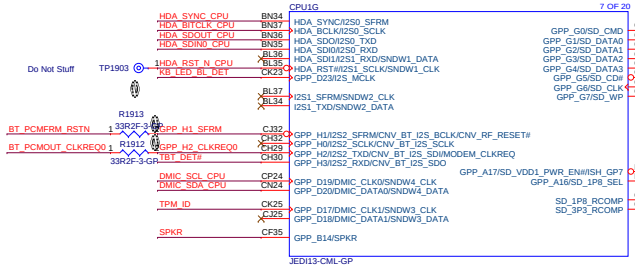
Size: A1 | Document Number: Jedi CML | Rev: SC

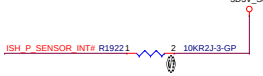
Date: Monday, October 29, 2018 | Sheet 18 of 105

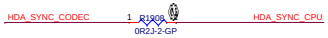
Main Func = PCH

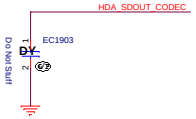




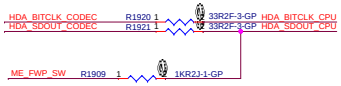








R1920~R1921 need to close for merge prepare



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (HDA/I2S/SD/DMIC)

Size: A2 | Document Number: JEDI 13" | Rev: SC

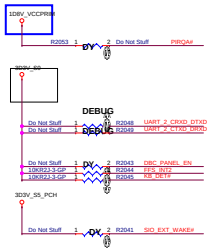
Date: Monday, October 28, 2019 | Sheet 19 of 106

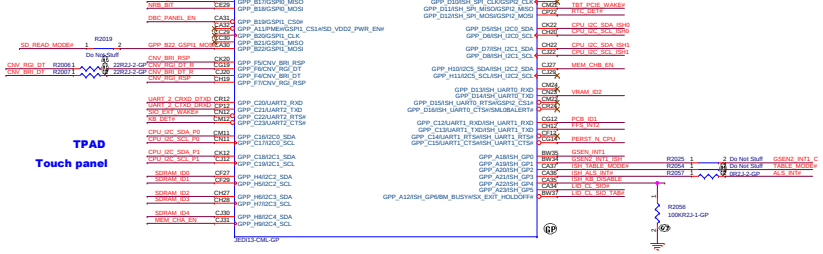
Main Func = PCH

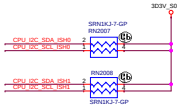
55 CPU_I2C_SDA_P1
55 CPU_I2C_SCL_P1
65,66 CPU_I2C_SDA_P0
65,66 CPU_I2C_SCL_P0
55 DBC_PANEL_EN
68 UART_2_CTXD_DTXD
68 UART_2_CTXD_DRXD

65 KB_DET#
55 GSEN_INT1
66 GSEN2_INT1_C
71 TBT_PCIE_WAKE#
15,25 RTC_DET#
55,66 CPU_I2C_SDA_ISH#
55,66 CPU_I2C_SCL_ISH#
66 FFS_INT2
66 SD_READ_MODE#

21 PCB_ID2
61 CNV_BRI_DT
61 CNV_RGI_RSP
15,61 CNV_RGI_DT
61 CNV_BRI_RSP
15 NRB_BIT
15 GPP_B22_GSPI1_MOSI
16,24 TABLE_MODE#
24,67 LID_CL_SIO_TAB#
24,67,92 LID_CL_SIO#
71 PERST_N_CPU
55 ALS_INT#
55 CPU_I2C_SDA_ISH#
55 CPU_I2C_SCL_ISH#





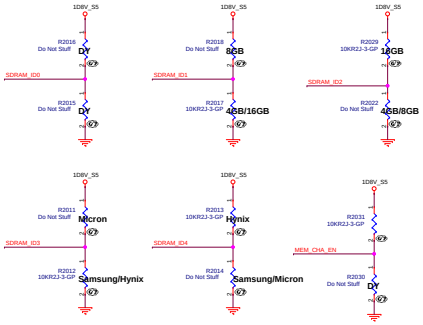


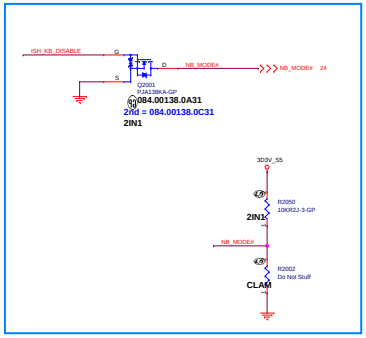
Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

RAM ID

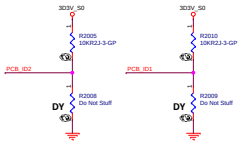
Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron. P/N	Capacity
Samsung	NA	01	00	K4AAG165WB-MCRC	TBD	16G
Micron	NA	01	10	MT40A1G16KNR-075E	TBD	16G
Hynix	NA	01	01	H5ANAG6NAMR-UHC	TBD	16G
Samsung	NA	10	00	K4A8G165WB-BCRC	TBD	8G
Micron	NA	10	10	MT40A512M16LY-075E	TBD	8G
Hynix	NA	10	01	H5AN8G6NAFR-UHC	TBD	8G
Samsung	NA	00	00	K4A4G165WE-BCRC	072.44165.0B0U	4G
Micron	NA	00	10	MT40A256M16GE-083E	072.40256.0A0U	4G
Hynix	NA	00	01	H5AN4G6NBJR-UHC	TBD	4G

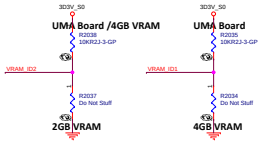




	BOARD_ID2	BOARD_ID1
15" mainstream UMA NON-Interleaved SO-DIMM	0	0
15" mainstream DIS Interleaved SO-DIMM	0	1
15" upsell Interleaved SO-DIMM	1	0
13" upsell/mainstream on-board LPDDR3	1	1

MEM_CONFIG[4:3]	On-board memory config for chip vendor	11	DIMM Design
		10	Hynix
		01	Micron
		00	Samsung
MEM_CONFIG[2:1]	On-board memory config for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	Reserved (non-use)		





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: CPU (UART/I2C/ISH)

Size	Document Number	Rev
A1	JEDI 13"	SC

Date: Monday, October 28, 2013 Sheet 20 of 108

Main Func = PCH

55 TOUCH_PANEL_PD#
61 WIFI_RF_EN
29 SPK_ID
55 TOUCH_DETECT
20 PCB_ID2
15 GPP_H21
15 GPP_H23
15 GPD_7
61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WR_CLK_DP
61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1
GPPC_H18_VCCIO_LPM
PROJECT_ID0
71 RTD3_CIO_PWR_EN
66 STYLUS_PWR_OCP#

CPU1I 9 OF 20
JEDI13-CML-GP

CNV_WR_DN0 CR30 / CNV_WR_DP0 CP30 → CNV_WR_D0N / CNV_WR_D0P
CNV_WR_DN1 CM30 / CNV_WR_DP1 CN30 → CNV_WR_D1N / CNV_WR_D1P
CNV_WT_DN0 CN32 / CNV_WT_DP0 CM32 → CNV_WT_D0N / CNV_WT_D0P
CNV_WT_DN1 CP33 / CNV_WT_DP1 CN33 → CNV_WT_D1N / CNV_WT_D1P
CNV_WR_CLK_DN CN31 / CNV_WR_CLK_DP CP31 → CNV_WR_CLKN / CNV_WR_CLKP
CNV_WT_CLK_DN CP34 / CNV_WT_CLK_DP CN34 → CNV_WT_CLKN / CNV_WT_CLKP
CNV_WT_RCOMP CP32 → CNV_WT_RCOMP_1
CR32 → CNV_WT_RCOMP_2
PROJECT_ID1 CP20 → GPP_F0/CNV_PA_BLANKING
PROJECT_ID2 CK19 → GPP_F1
CG17 → GPP_F2
SPK_ID CR14 → GPP_C8/UART0_RXD
TOUCH_PANEL_PD# CP14 → GPP_C9/UART0_TXD
TOUCH_DETECT_R CN14 → GPP_C10/UART0_RTS#
PCB_ID2 CM14 → GPP_C11/UART0_CTS#
CJ17 → GPP_F8/CNV_MFUART2_RXD
CH17 → GPP_F9/CNV_MFUART2_TXD
CF17 → GPP_F23/A4WP_PRESENT

GPP_H18/CPU_C10_GATE# CN27 → GPPC_H18_BOOTMFC
GPP_H19/TIMESYNC_0 CM27
GPP_H21/XTAL_FREQ_SELECT CF25 → GPP_H21
GPP_H22 CN26 → RTD3_CIO_PWR_EN
GPP_H23 CM26 → GPP_H23
GPP_F10 CK17
GPD7 BV35 → GPD_7
GPP_F3 CN20 → PROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25 → WIFI_RF_EN
GPP_H20/IMGCLKOUT1 CH25 → STYLUS_PWR_OCP#
GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18
GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16
EMMC_RCOMP CK15 → EMMC_RCOMP

GPP_F: VCCPGPPF = 1.8V Only

R2101 1 150R2F-1-GP
R2102 DY Do Not Stuff
R2103 DY Do Not Stuff SB 0124
R2119 Do Not Stuff
R2108 200R2F-1-GP
R2110 10KR2J-3-GP
3D3V_S0

PROJECT_ID[1:0] 01: 7000 Series
PROJECT_ID[3:2] 11: Inspiron

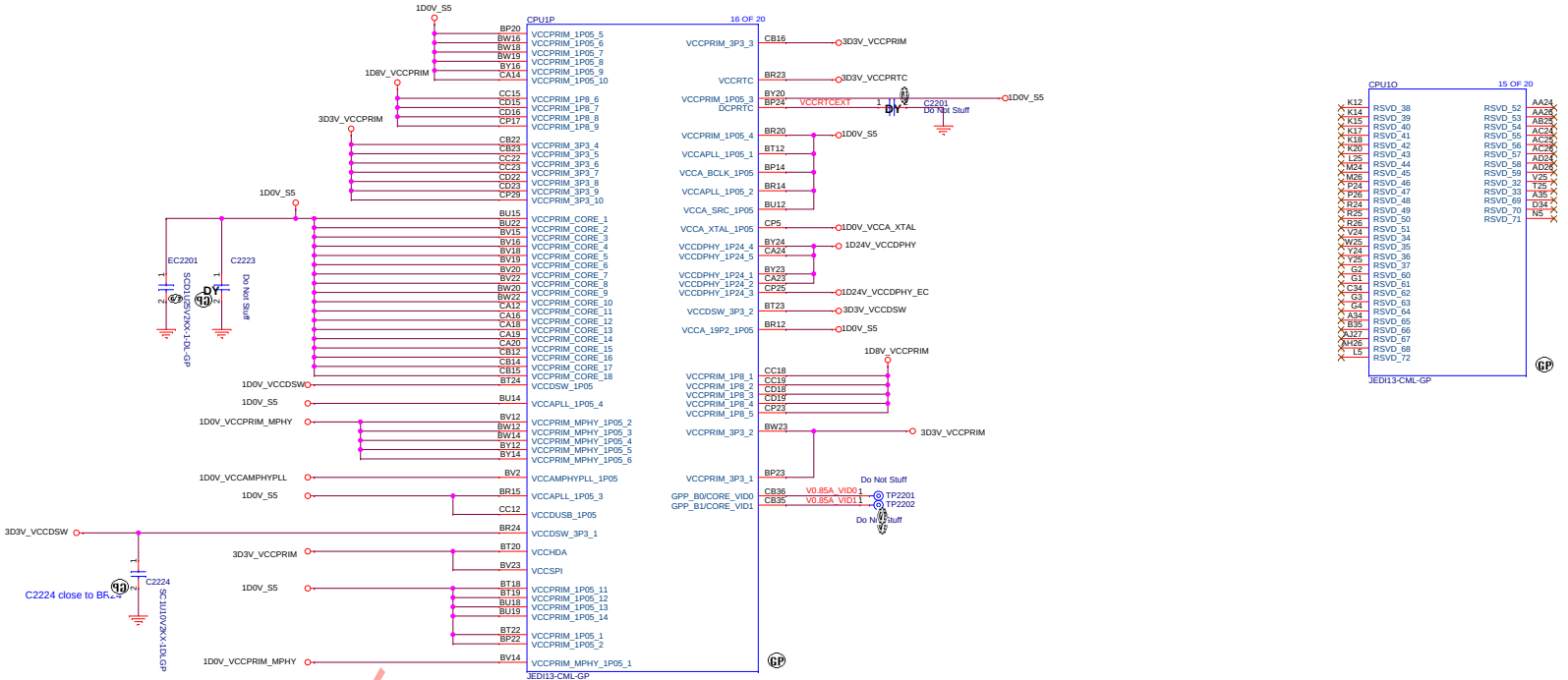
1D8V_VCCPRIM
R2111 DY Do Not Stuff
R2112 10KR2J-3-GP
PROJECT_ID1
R2113 MS 10KR2J-3-GP
R2114 UPSELL Do Not Stuff
PROJECT_ID0
R2115 10KR2J-3-GP
R2116 DY Do Not Stuff
PROJECT_ID3
R2117 10KR2J-3-GP
R2118 DY Do Not Stuff
PROJECT_ID2

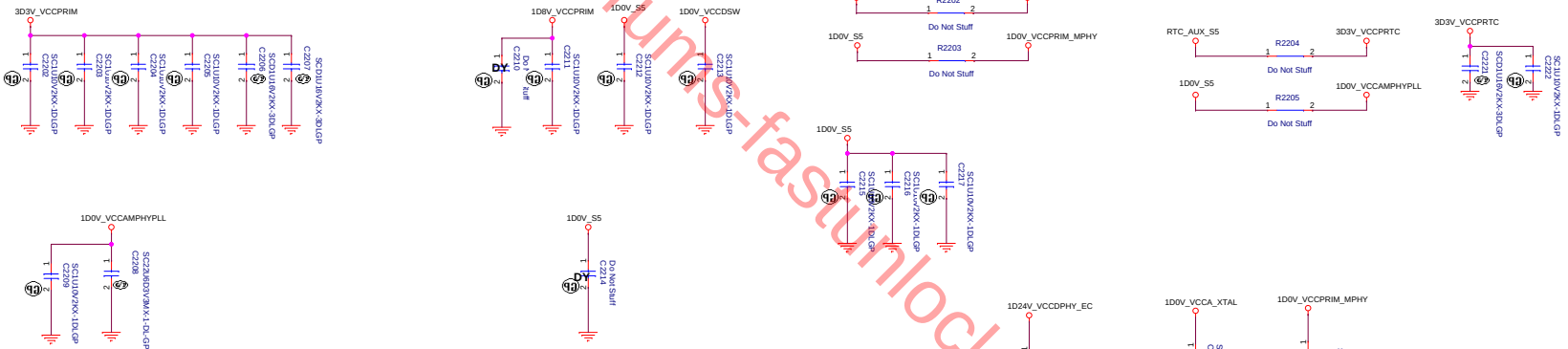
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVi)
Size: A3 | Document Number: JEDI 13" | Rev: SC
Date: Monday, October 28, 2019 | Sheet 21 of 106

Main Func = PCH





<Core Design>

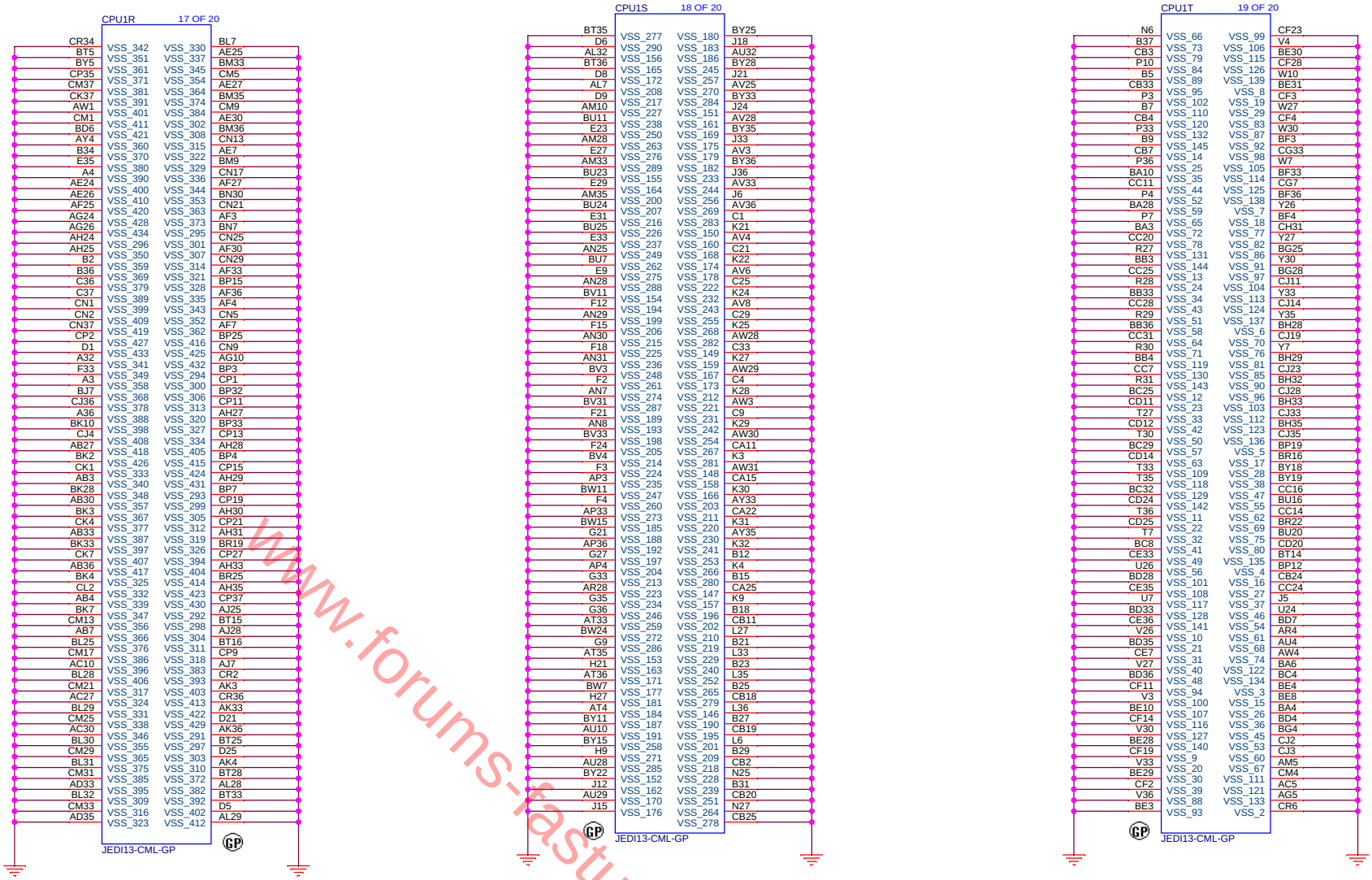
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

Size: A2 | Document Number: JEDI 13" | Rev: SC

Date: Thursday, October 31, 2019 | Sheet 22 of 106

Main Func = PCH



<Core Design>

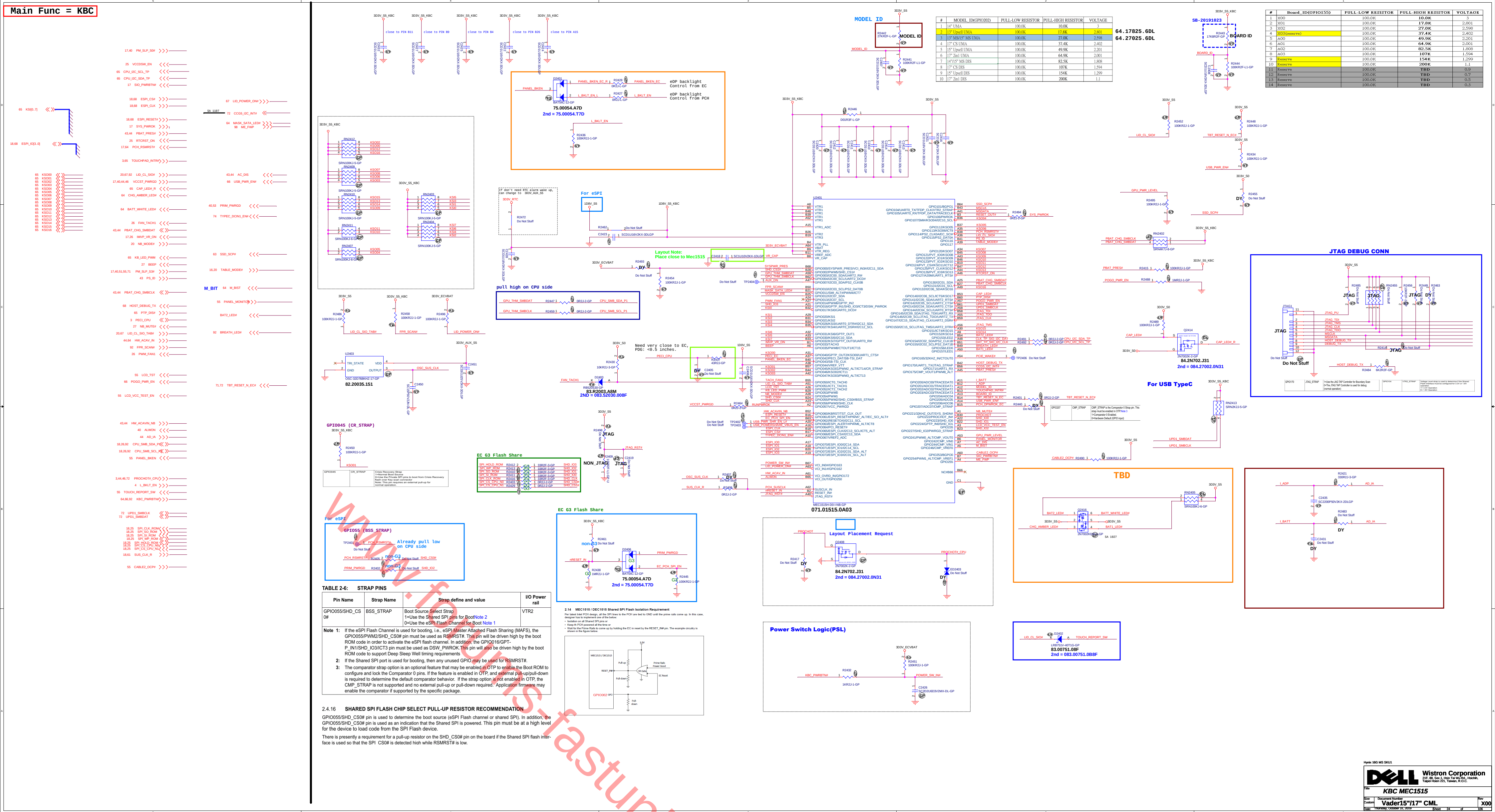
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	JEDI 13"	SC

Date: Monday, October 28, 2019 Sheet 23 of 106

Main Func = KBC



#	MODEL_ID(GPIO202)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	14" UMA	100.0K	10.0K	3
2	13" Upsell UMA	100.0K	17.8K	2.801
3	13" MS/15" MS UMA	100.0K	27.0K	2.598
4	17" CS UMA	100.0K	37.4K	2.402
5	15" Upsell UMA	100.0K	49.9K	2.201
6	17" 2in1 UMA	100.0K	64.9K	2.001
7	14"/15" MS DIS	100.0K	82.5K	1.808
8	17" CS DIS	100.0K	107K	1.594
9	15" Upsell DIS	100.0K	154K	1.299
10	17" 2in1 DIS	100.0K	200K	1.1

64.17825.6DL
64.27025.6DL

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected high while RSMRST# is low.

Hynix 16G MS SKU1

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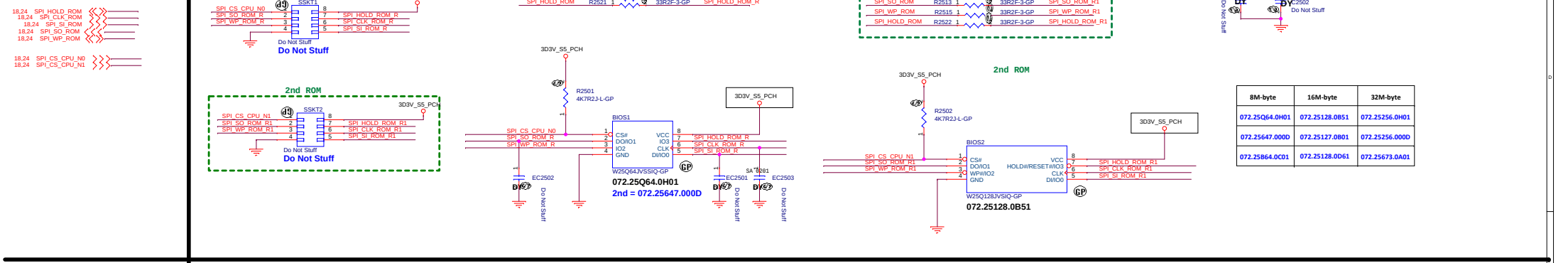
Title: KBC MEC1515

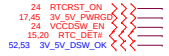
Size: Custom | Document Number: Vader15"/17" CML | Rev: X00

Main Func = SPI Flash

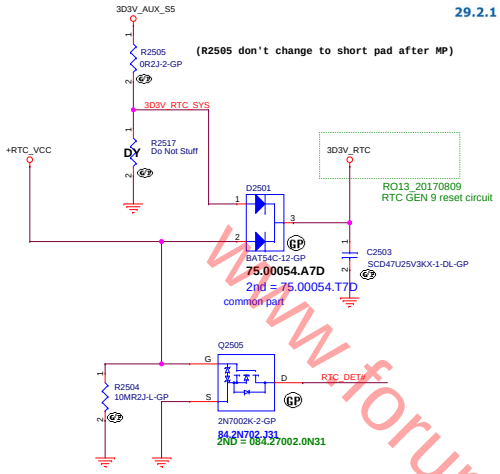


8M-byte	16M-byte	32M-byte
072.25Q64.0H01	072.25128.0B51	072.25256.0H01
072.25647.000D	072.25127.0B01	072.25256.000D
072.25864.0C01	072.25128.0D61	072.25673.0A01

Main Func = RTC



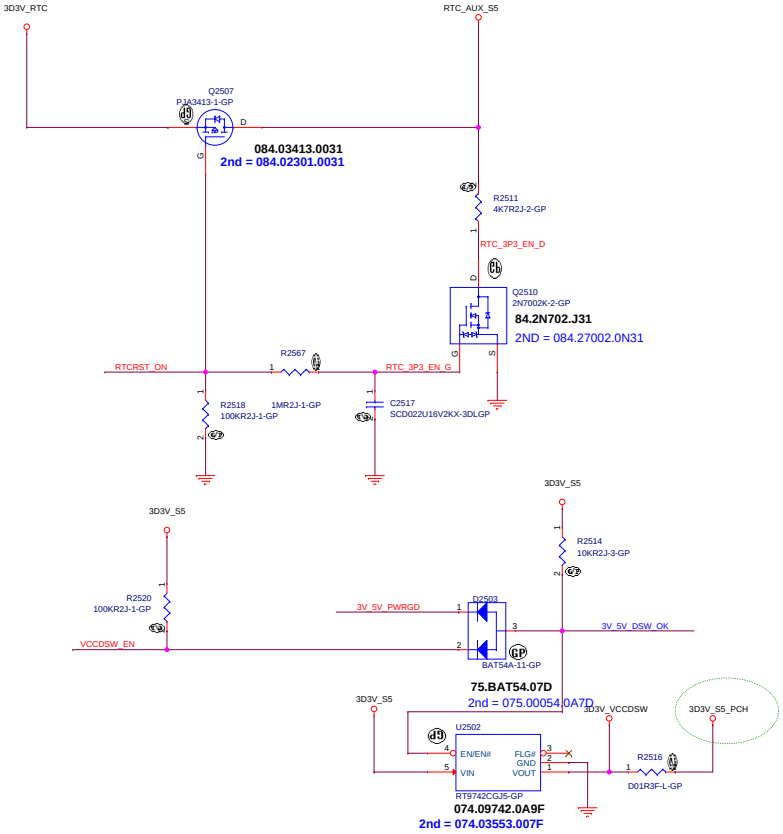
Delivery Voltage 3.19V



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

RTC



Add RTC GEN 9 reset circuit_20170809

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Title: Flash/RTC
Size: A2
Document Number: JEDI 13"
Rev: SC
Date: Monday, October 28, 2019
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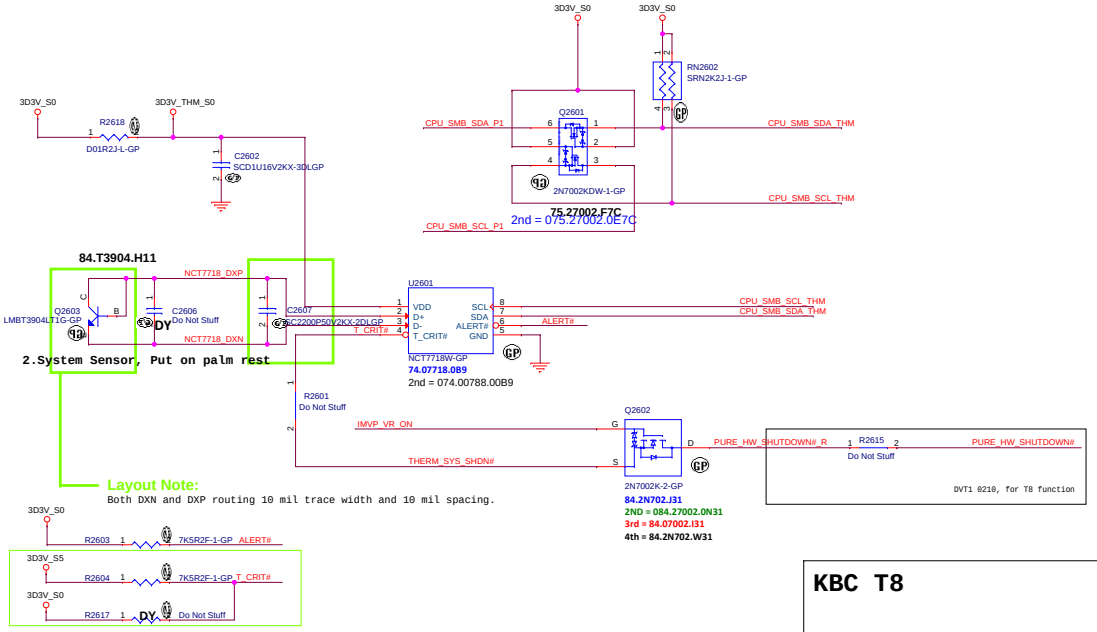
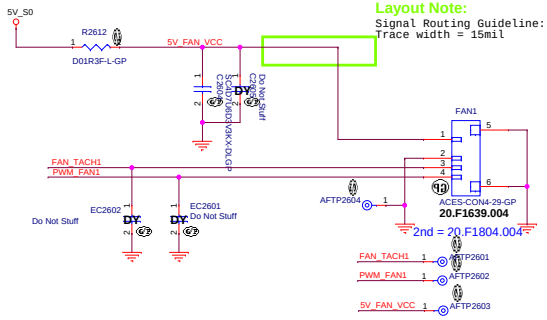
Main Func = Thermal Sensor





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8

Close to KBC

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Title: THERMAL NCT7718W/Fan

Size: A2 | Document Number: JEDI 13" | Rev: SC

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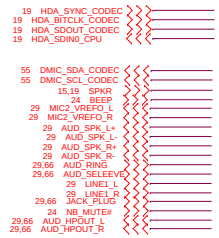
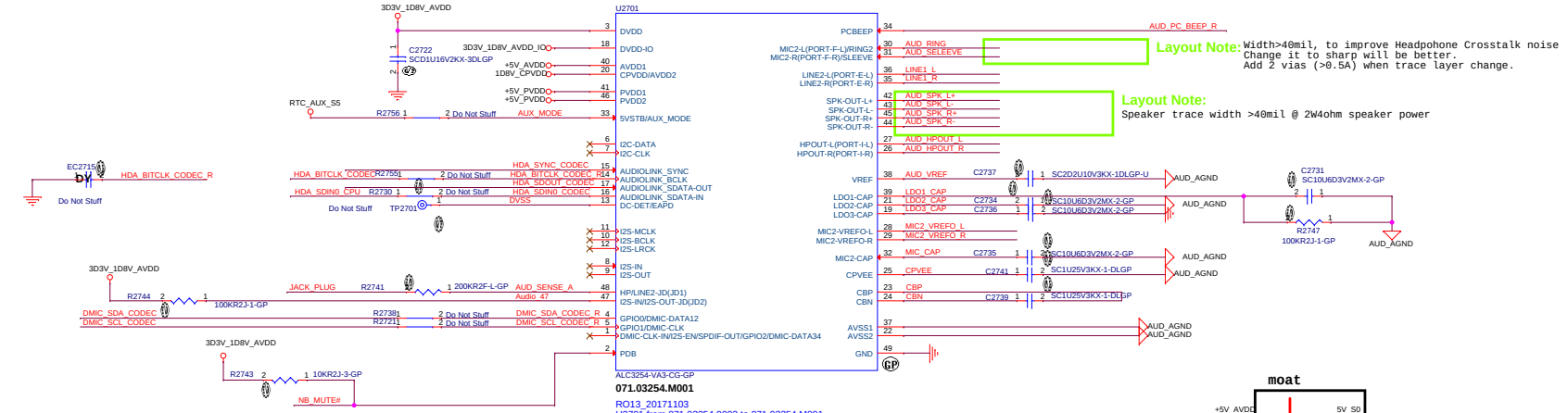
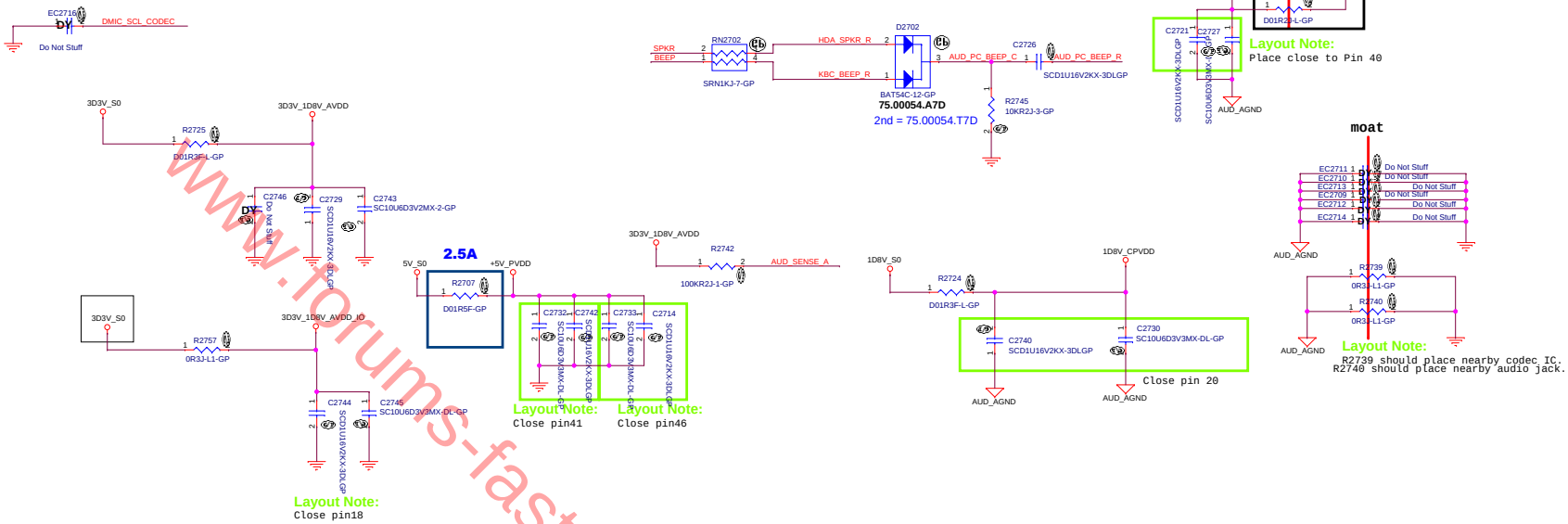
Main Func = Audio





Close pin5



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Title: Audio Codec ALC3254

Size	Document Number	Rev
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Title

(Reserved)

Size	Document Number	Rev
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Main Func = Audio

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

21 SPK_ID
27 MIC2_VREFO_R
27 MIC2_VREFO_L
27,66 AUD_RING
27,66 AUD_HPOUT_L
27 LINE1_L
27,66 AUD_HPOUT_R
27 LINE1_R
27,66 AUD_SELEEVE

27,66 JACK_PLUG

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

RO13_20171002
follow ME connector list

AUD_SPK_L+ — ER2902 0R2J-L-GP — AUD_SPK_L+_C
AUD_SPK_L- — ER2901 0R2J-L-GP — AUD_SPK_L-_C
AUD_SPK_R+ — ER2904 0R2J-L-GP — AUD_SPK_R+_C
AUD_SPK_R- — ER2903 0R2J-L-GP — AUD_SPK_R-_C

SPK_ID

SPK1
ACES-CON6-20-GP-U
20.F1639.006
2nd = 020.F1263.0006

CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON

AUD_SPK_L+_C
AUD_SPK_L-_C
AUD_SPK_R+_C
AUD_SPK_R-_C

ED2908 ED2907 ED2906 ED2905 — DY — Do Not Stuff

AUD_SPK_L-_C — AFTP2901
AUD_SPK_L+_C — AFTP2902
AUD_SPK_R-_C — AFTP2903
AUD_SPK_R+_C — AFTP2904

SC1KP50V2KX-1DLGP EC2901
SC1KP50V2KX-1DLGP EC2902
SC1KP50V2KX-1DLGP EC2903
SC1KP50V2KX-1DLGP EC2904

RN2901
SRN2K2J-1-GP

MIC2_VREFO_R
MIC2_VREFO_L
AUD_RING
AUD_HPOUT_L
LINE1_L
AUD_HPOUT_R
LINE1_R
AUD_SELEEVE

C2907 SC10U6D3V3MX-DL-GP
C2908 SC10U6D3V3MX-DL-GP

Delay circuit

(JACK_PLUG_DET: on IO Board)

JACK_PLUG 10 mils — 10 mils
JEDI 13_20180706
C2909 DY Do Not Stuff
AUD_AGND

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Title: Audio IO
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Size	Document Number	Rev
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Main Func = Power Plane & Sequence

17,51,55,71 PM_SLP_S3#
45 3V_5V_EN
26 PURE_HW_SHUTDOWN#
24 ALWON
17,51 PM_SLP_S4#
51 VDDQ_PWRGD
17,24,44,46 VCCST_PWRGD
52 1D0V_S5_PWRGD
24,53 PRIM_PWRGD
17 PM_SLP_S0#
21 GPPC_H18_VCCIO_LPM
17,61,63,71 PLTRST#_CPU

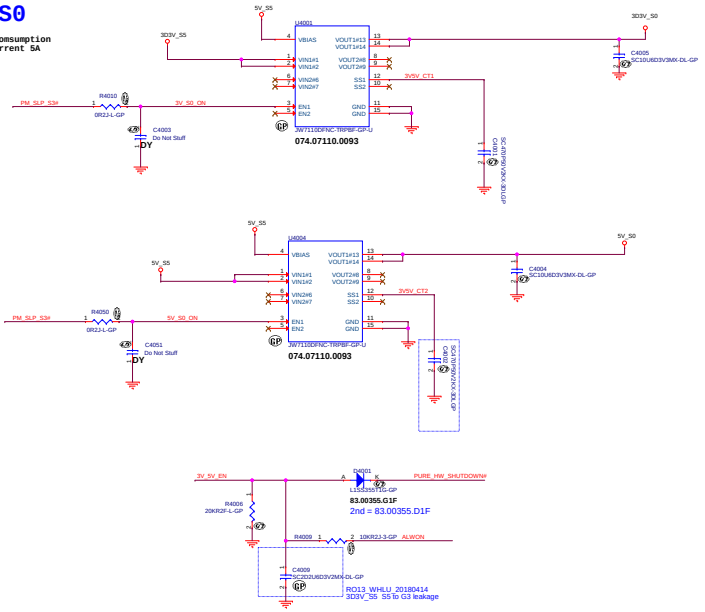
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

5V_S0

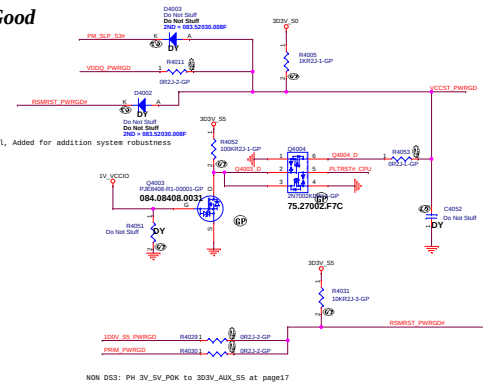
5V_S0 Comsumption
Peak current 5A

ROSA Run Power



074.07110.0093
83.00355.G1F
2nd = 83.00355.D1F
074.07110.0093

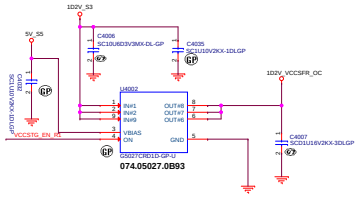
Power Good



084.08408.0031
75.27002.F7C

NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

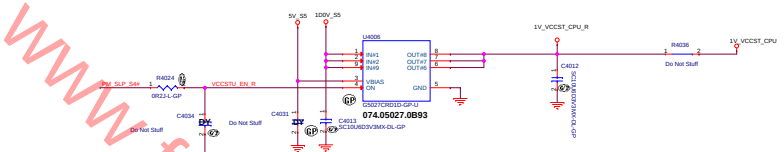
VCCSFR_OC



074.05027.0B93

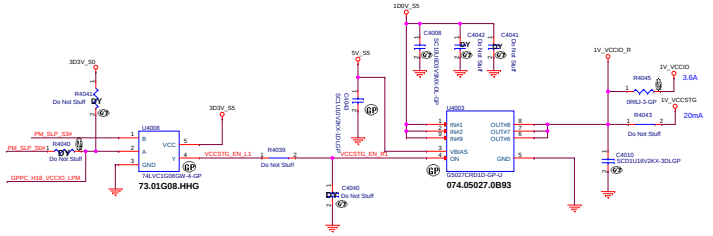
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.



074.05027.0B93

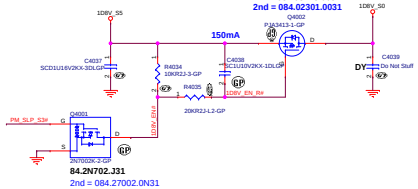
VCCIO and VCCSTG



73.01G08.HHG
074.05027.0B93

+V1.8V_VDD1 LPDDR3

+V1.8V_S0



084.03413.0031
2nd = 084.02301.0031
84.2N702.J31
2nd = 084.27002.0N31

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Title: Power Plane Enable

Size: A1 | Document Number: JEDI 13" | Rev: SC

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<Core Design>

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Title
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Title: *(Reserved)*

Size	Document Number	Rev
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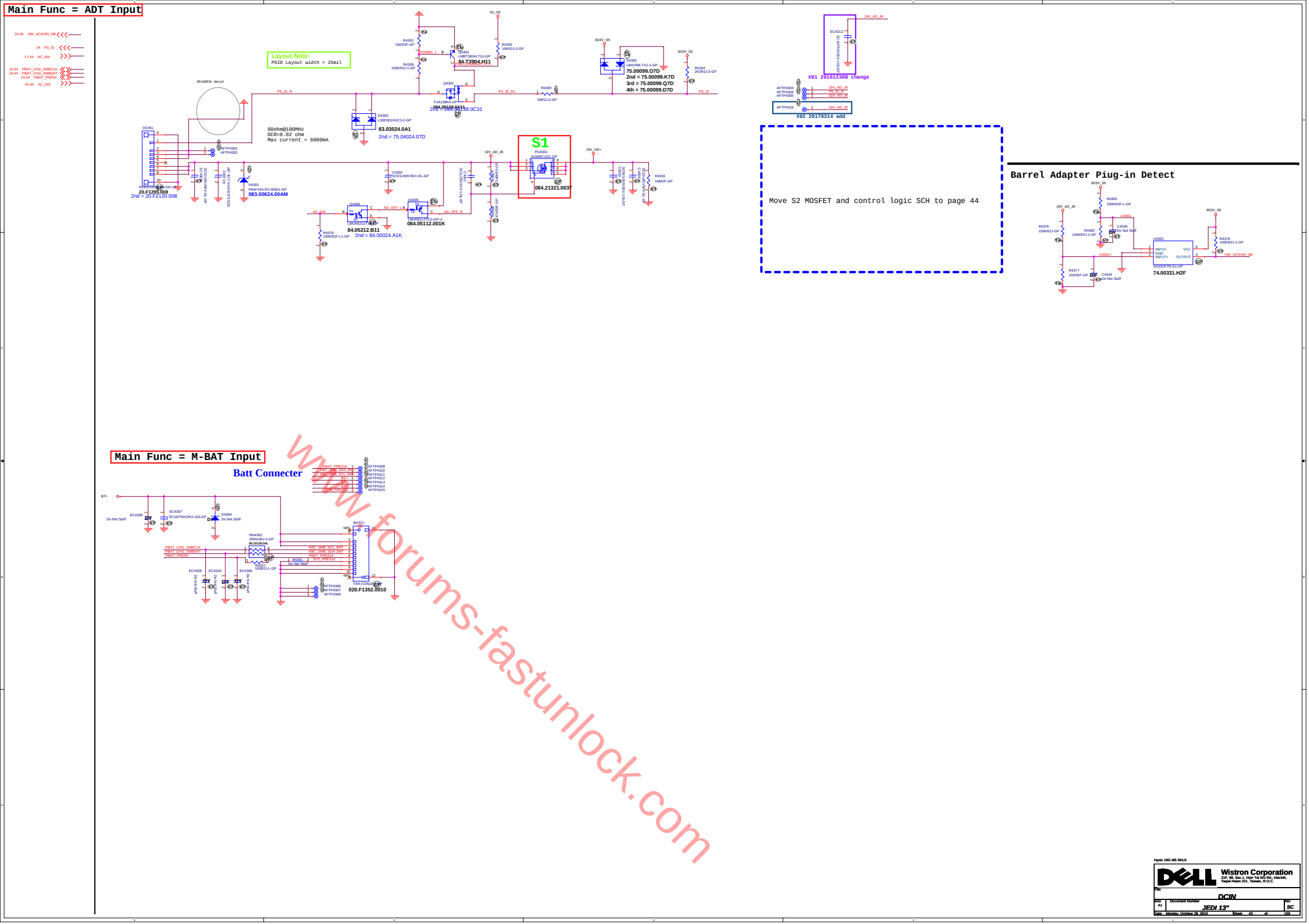
Main Func = ADT Input



Main Func = M-BAT Input

Hynix 16G MS SKU1

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Title	DCIN	
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ISL9538H For Charger

Main Func = Charger

OFFPAGE

EE needs check !!!!

From KKP ACK

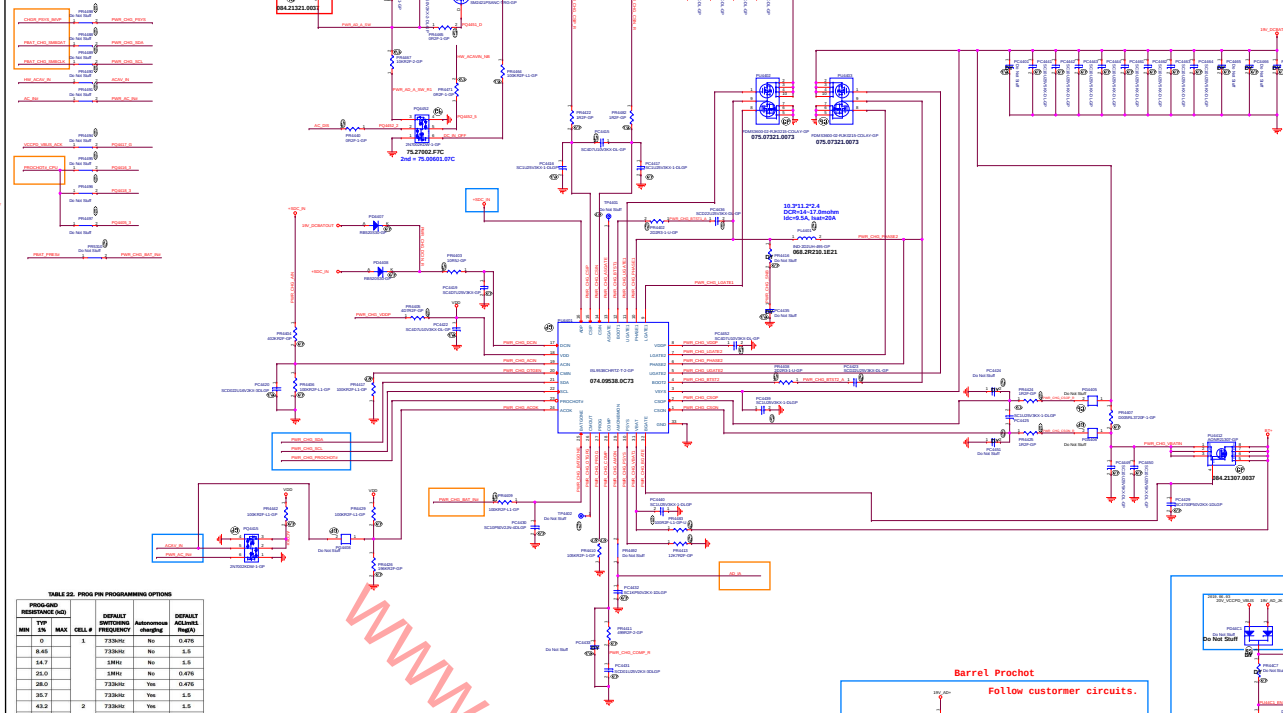


TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)				DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLim#1 Reg(A)
MIN	TYP 1%	MAX	CELL #			
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

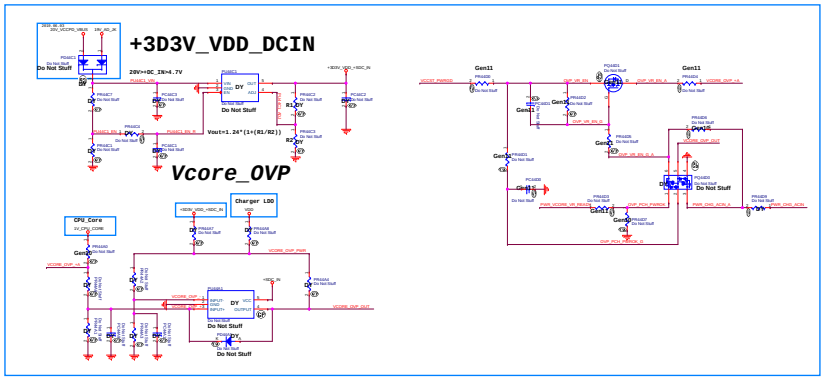
PU +VCCSTG = 1.0 V on CPU side

TypeC Prochot

Follow custormer circuits.

Barrel Prochot

Follow custormer circuits.



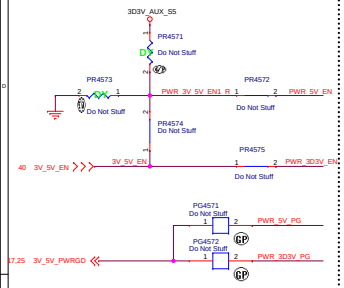
Wistron Corporation

Power (Charger_ISL9538)

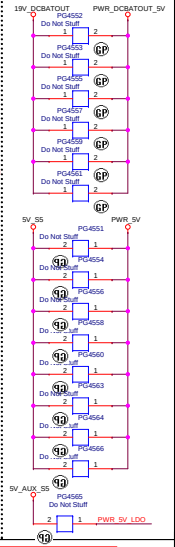
ROSA NB PWR STD

SSID = PWR.Plane.Regulator_5V

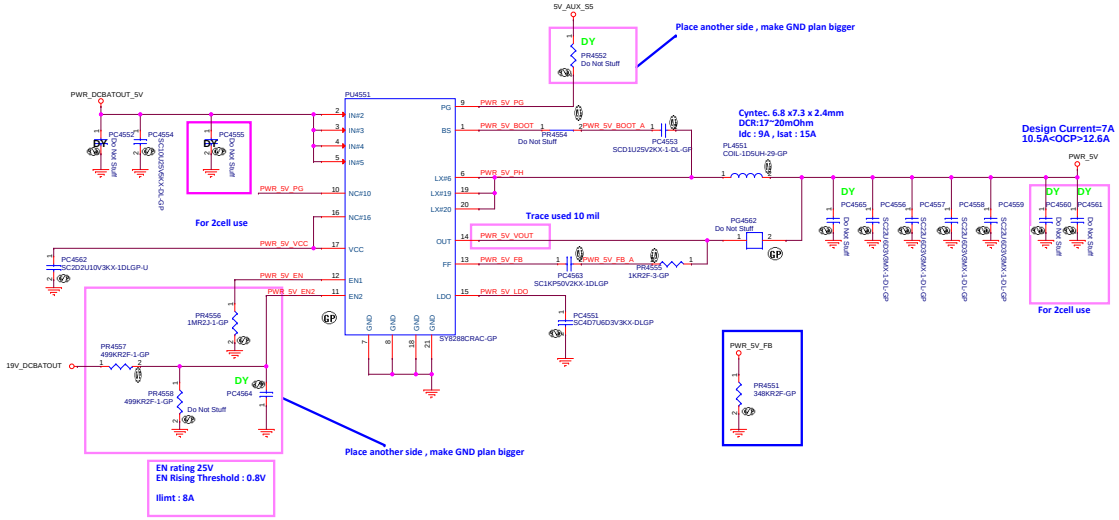
OFFPAGE-Signal



OFFPAGE-GAP



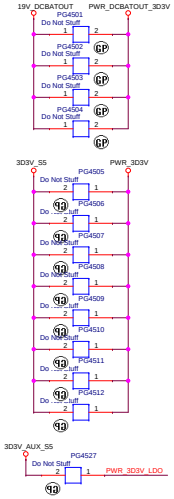
SY8288C For 5V



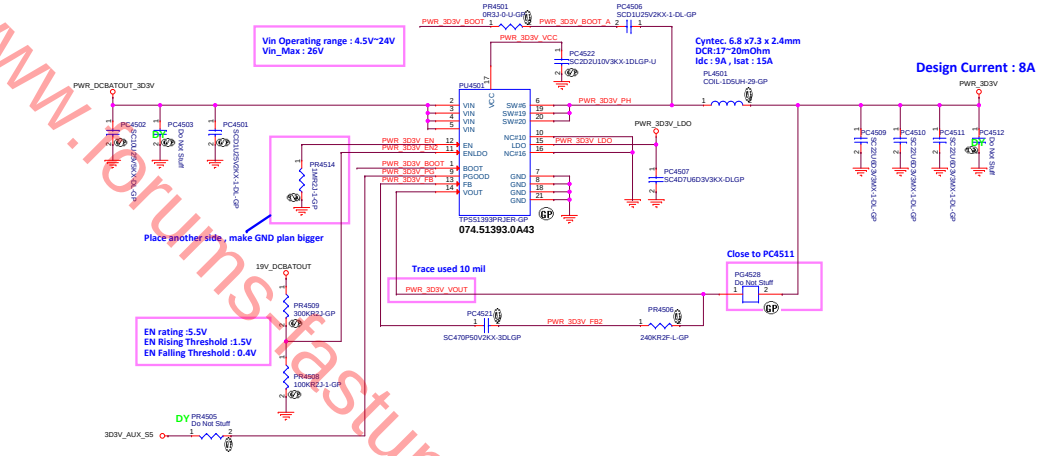
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

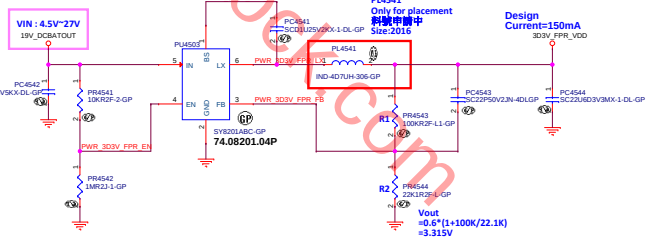
OFFPAGE-GAP



TPS51393 For 3D3V



FPR S5 SSO



40 PWR_3D3V_FPR_EN PWR_3D3V_FPR_EN

Hynix 16G MS SKU1

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Title: POWER (SY8286_5V/3D3V)

Size	Document Number	Rev
Custom	STD	A00

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ISL95859C For CPUCORE

Main Func = CPU_CORE

OFFPAGE

PH on CPU side

PH on EE side

For VCCGT Sense

For Vcore Sense

For VCCSA Sense

OFFPAGE-GAP

EE side Link
SVID Pull High V

	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4635	1K(64.10015.6DL)	DY
PR4642	357(64.35705.6DL)	499 (64.49905.6DL)
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)
PC4654	10nF(78.10322.2FLDL)	10nF78.10322.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.49K(64.24915.6DL)
PR4608	76.8K(64.76825.6DL)	95.3K (64.95325.6DL)

Hynix 16G MS SKU1

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Title: POWER (95859_CPUCORE(1/3))

Size: A1 | Document Number: STD | Rev: A00

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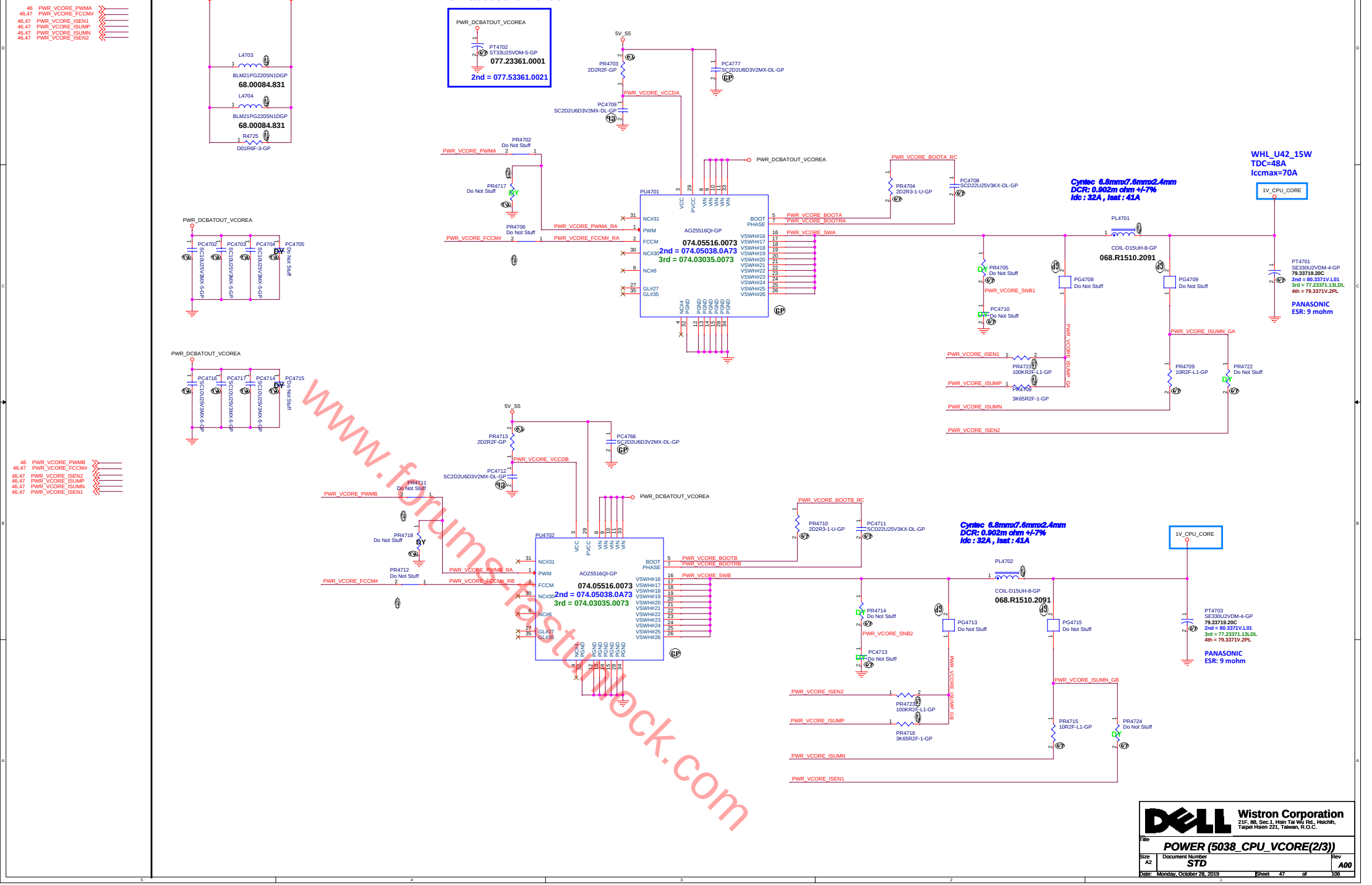
Main Func = CPU_CORE

OFFPAGE

AOZ5038QI For VCORE

For acoustic noise



Title: POWER (5038_CPU_VCORE(2/3))

Size: A2 | Document Number: STD | Rev: A00

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Main Func = CPU_CORE

Offpage-Signal

46 PWR_VCCGT_PWM
46 PWR_VCCGT_FCCM#
46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN

AOZ5038QI For VCCGT

19V_DCBATOUT
PWR_DCBATOUT_VCCGT
PWR_DCBATOUT_VCCGT

PC4801 SC10U25V3MX-5-GP
PC4802 SC10U25V3MX-5-GP
PC4803 SC10U25V3MX-5-GP
PC4804 SC10U25V3MX-5-GP

L4803 BLM21PG220SN1DGP 68.00084.831
L4802 BLM21PG220SN1DGP 68.00084.831
R4809 D01R6F-3-GP

For acoustic noise

PWR_DCBATOUT_VCCGT
PT4805 ST33U25VDM-5-GP
077.23361.0001
2nd = 077.53361.0021

5V_S5
PR4804 2D2R2F-GP
PC4866 SC2D2U6D3V2MX-DL-GP
PWR_VCCGT_VCC_R
PC4808 SC2D2U6D3V2MX-DL-GP
PWR_DCBATOUT_VCCGT

PR4802 Do Not Stuff
PWR_VCCGT_PWM
PR4812 DY Do Not Stuff
PR4806 Do Not Stuff
PWR_VCCGT_FCCM#

PU4801
AOZ5516QI-GP
074.05516.0073
2nd = 074.05038.0A73
3rd = 074.03035.0073

NC#31
PWM → PWR_VCCGT_PWM_R
FCCM → PWR_VCCGT_FCCM#_R
NC#30
NC#6
GL#27
GL#35
NC#4
PGND
VCC
PVCC
VIN
BOOT → PWR_VCCGT_BOOT
PHASE → PWR_VCCGT_SW
VSWH#16 … VSWH#26

PWR_VCCGT_BOOT_RC
PR4805 2D2R3F-L-GP
PC4807 SCD22U25V3KX-DL-GP
PWR_VCCGT_BOOTR

Cyntec 6.8mmx7.6mmx2.4mm
DCR: 0.902m ohm +/-7%
Idc : 32A , Isat : 41A

WHL_U22_15W
TDC=18A
Iccmax=31A

PL4801
COIL-D15UH-8-GP
068.R1510.2091

1V_VCCGT

PR4803 Do Not Stuff DY
PWR_VCCGT_SNB
PC4806 Do Not Stuff DY
PR4808 3K65R2F-1-GP
PWR_VCCGT_ISUMP

PG4807 Do Not Stuff
PWR_VCCGT_ISUMP_G

PG4808 Do Not Stuff
PWR_VCCGT_ISUMN_G
PR4801 Do Not Stuff
PWR_VCCGT_ISUMN

PT4801 SE330U2VDM-4-GP
79.33719.20C
2nd = 80.3371V.L01
3rd = 77.23371.13LDL
4th = 79.3371V.2PL
PANASONIC
ESR: 9 mohm

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Title: POWER (5038_CPU_VCORE(3/3))
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Hynix 16G MS SKU1

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Title	CPU_VCCGTUS	
Size A4	Document Number Unicorn_LV530_KBL_MB14	Rev SC
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Main Func = CPU_CORE

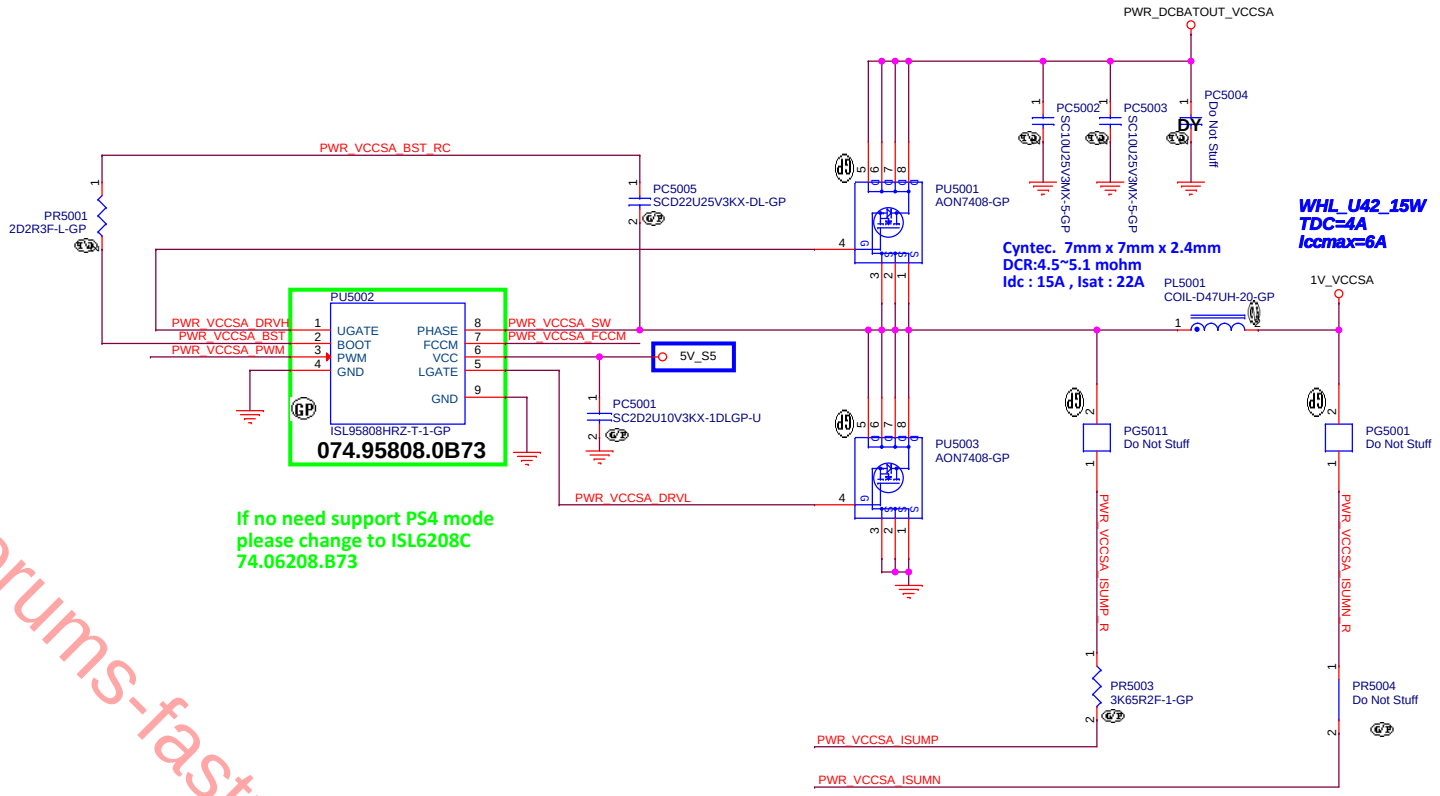
OFFPAGE-Signal

46 PWR_VCCSA_PWM
46 PWR_VCCSA_FCCM
46 PWR_VCCSA_ISUMP
46 PWR_VCCSA_ISUMN

OFFPAGE-GAP

19V_DCBATOUT
PWR_DCBATOUT_VCCSA
R5005
D01R6F-3-GP

ISL95808 For VCCSA



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Title: POWER (ISL95808_VCCSA)

Size	Document Number	Rev
A3	STD	A00

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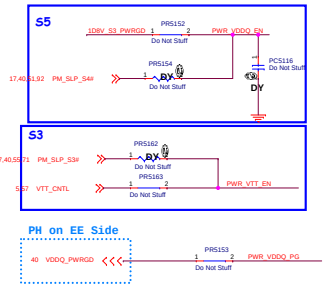
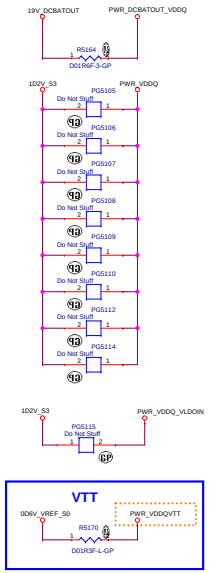
OFFPAGE



OFFPAGE_GAP



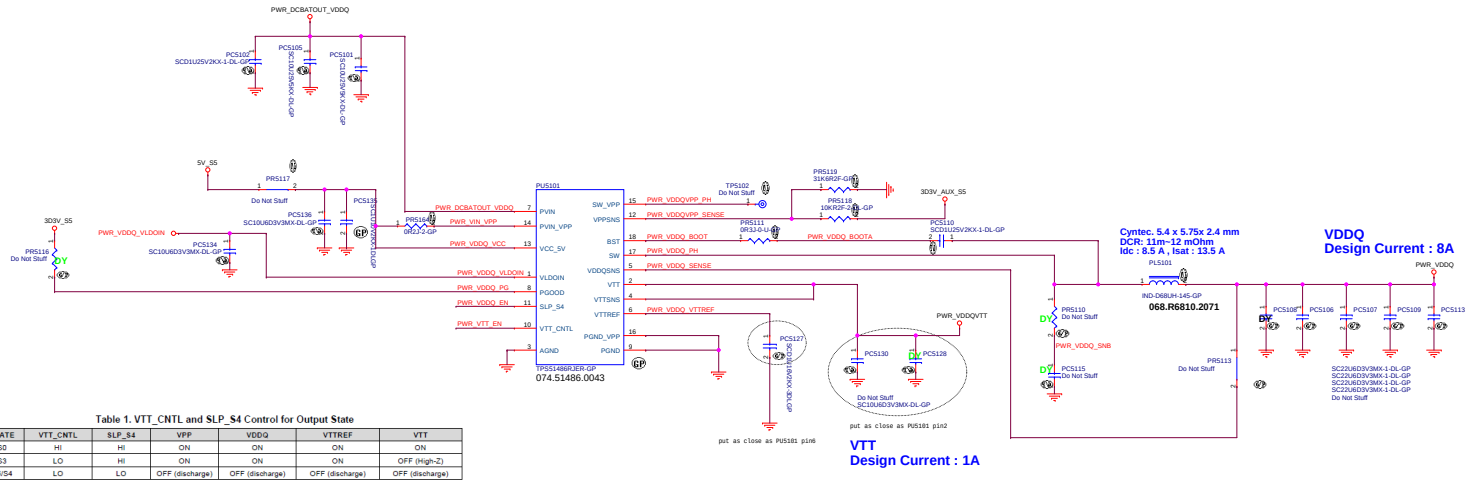
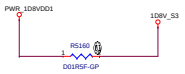


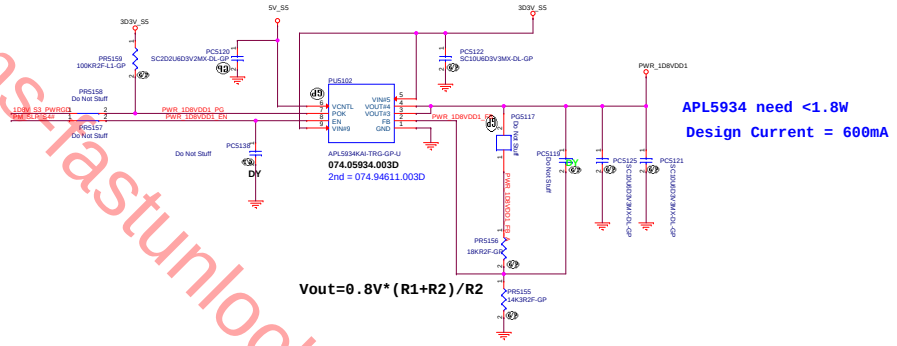
Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

OFFPAGE-Signal

OFFPAGE-GAP





Hynix 16G MS SKU1

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Title: TPS51486_VDDQ/VTT/VPP

Size: Custom | Document Number: Rosa NB STD POWER | Rev: SA

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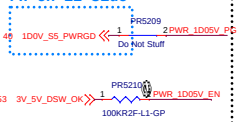
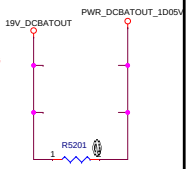
SSID = PWR.Plane.Regulator_1D05V

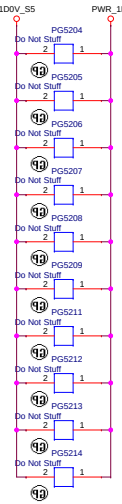
OFFPAGE-Signal

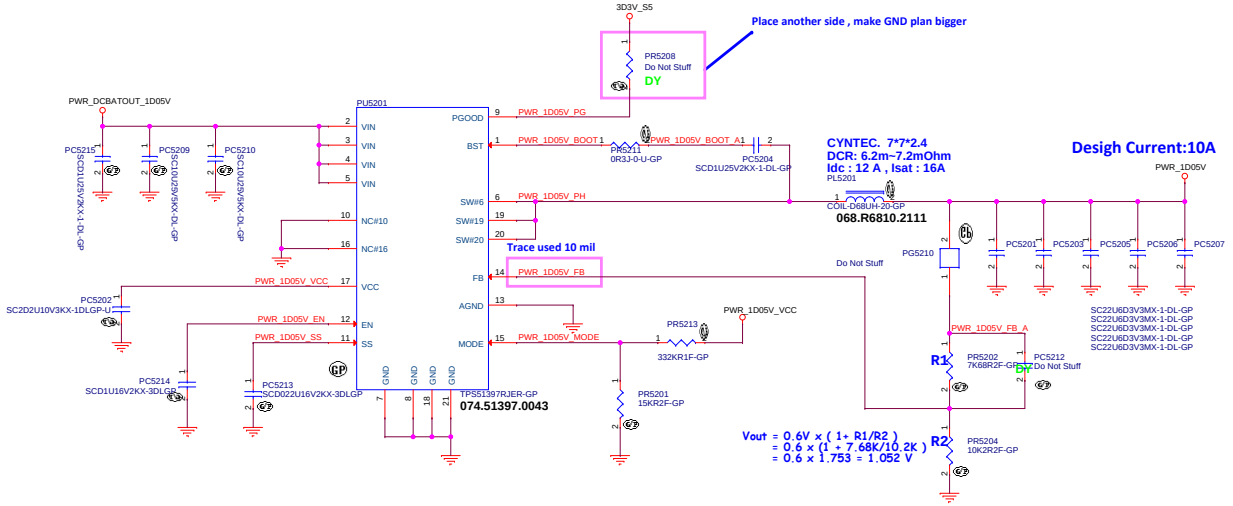
PH on EE Side



OFFPAGE-GAP







Hynix 16G MS SKU1

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Title: POWER (AOZ2262_1D05V)

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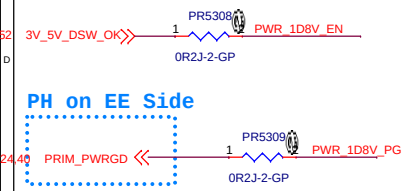
Main Func = 1D8V

OFFPAGE



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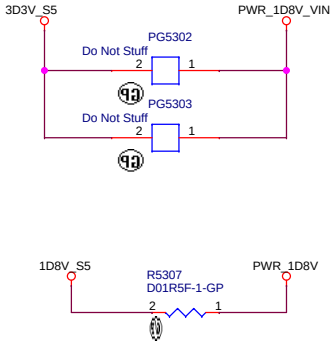
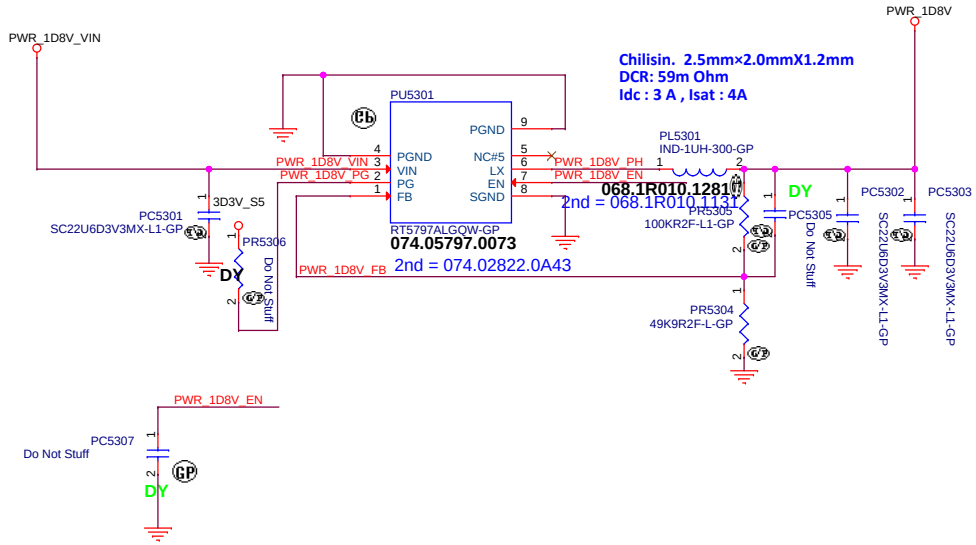


RT5797AL for 1D8V

Design Current=1.965A
Icc(max)=2.165A
OCP>3A



Hynix 16G MS SKU1

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Title: POWER (APL5934_1D8V)

Size	Document Number	Rev
A3	JEDI 13"	SC

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Title

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Size	Document Number	Rev
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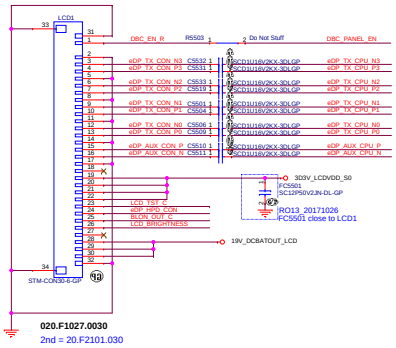
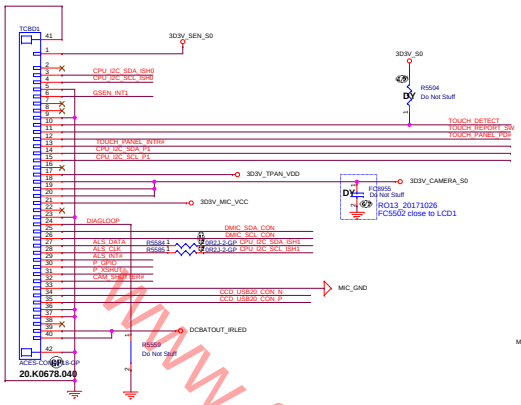
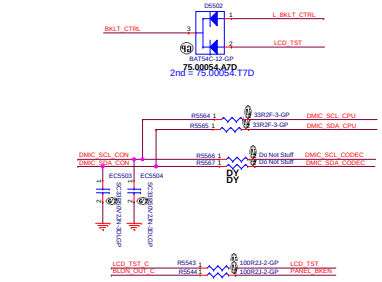
Main Func = LCD

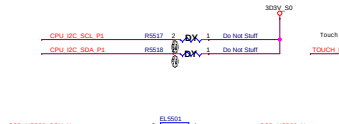
eDP Panel

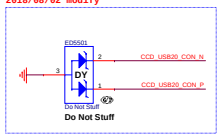


Sensor/TOUCH PANEL/IR Camera

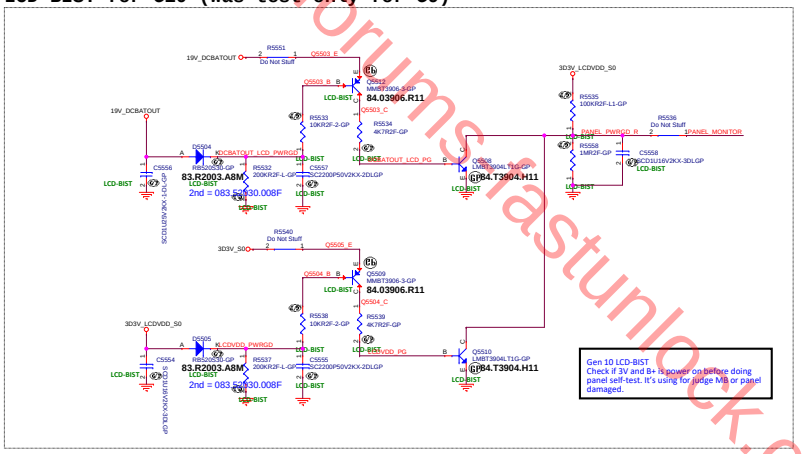




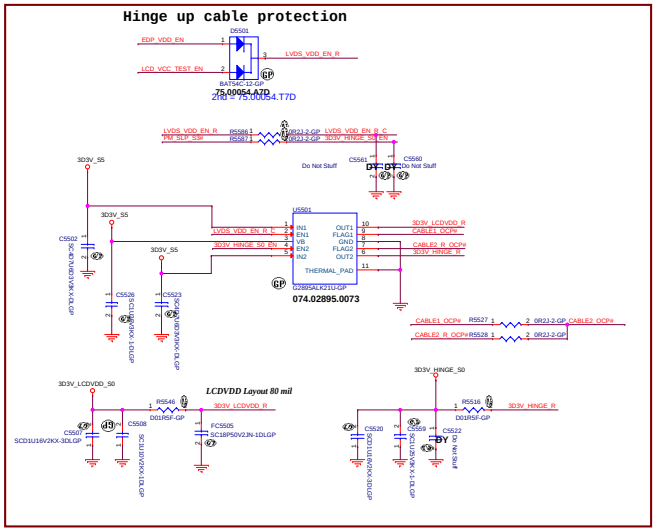




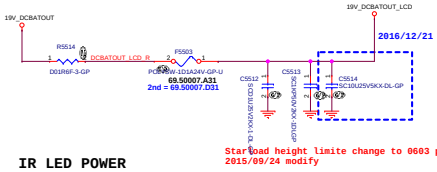
LCD BIST for G10 (Was test only for G9)



Hinge up cable protection

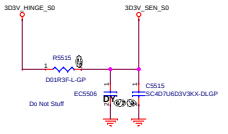


INVERTER POWER

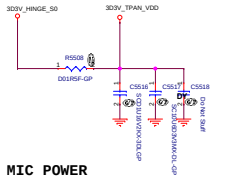


IR LED POWER

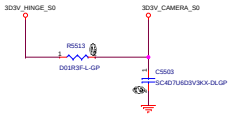
SENSOR POWER



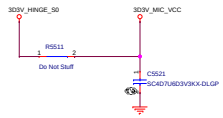
TOUCH PANEL POWER



CAMERA POWER



MIC POWER



Hynix 16G MS SKU1

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Title: LCD&CAM&DMC&Touch

Size: Custom | Document Number: JEDI 13" | Rev: SC

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<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
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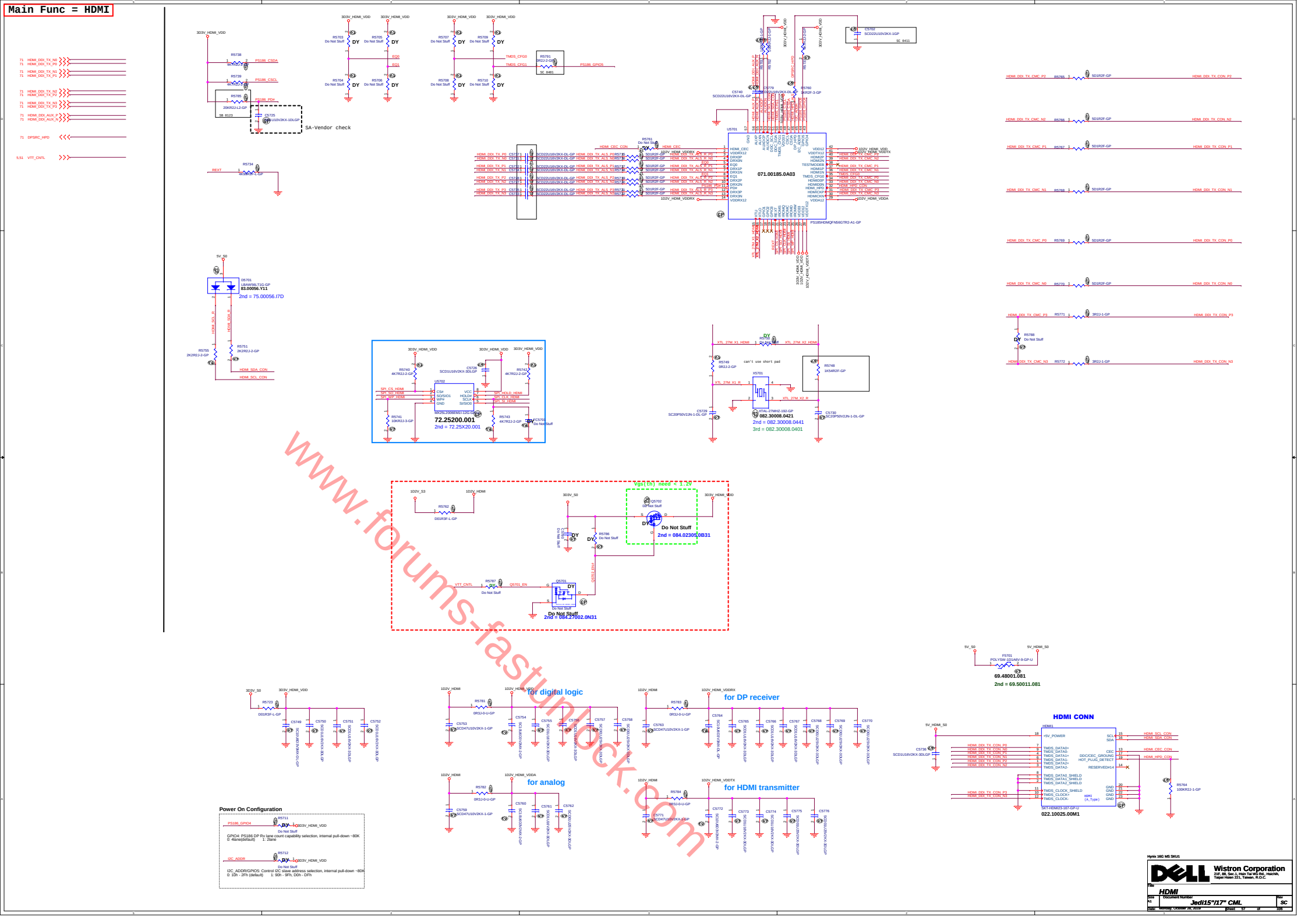
Main Func = HDMI



<Core Design>

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Size	Document Number	Rev
A2	*JEDI 13"*	*SC*

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<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
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<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
A2	JEDI 13"	SC

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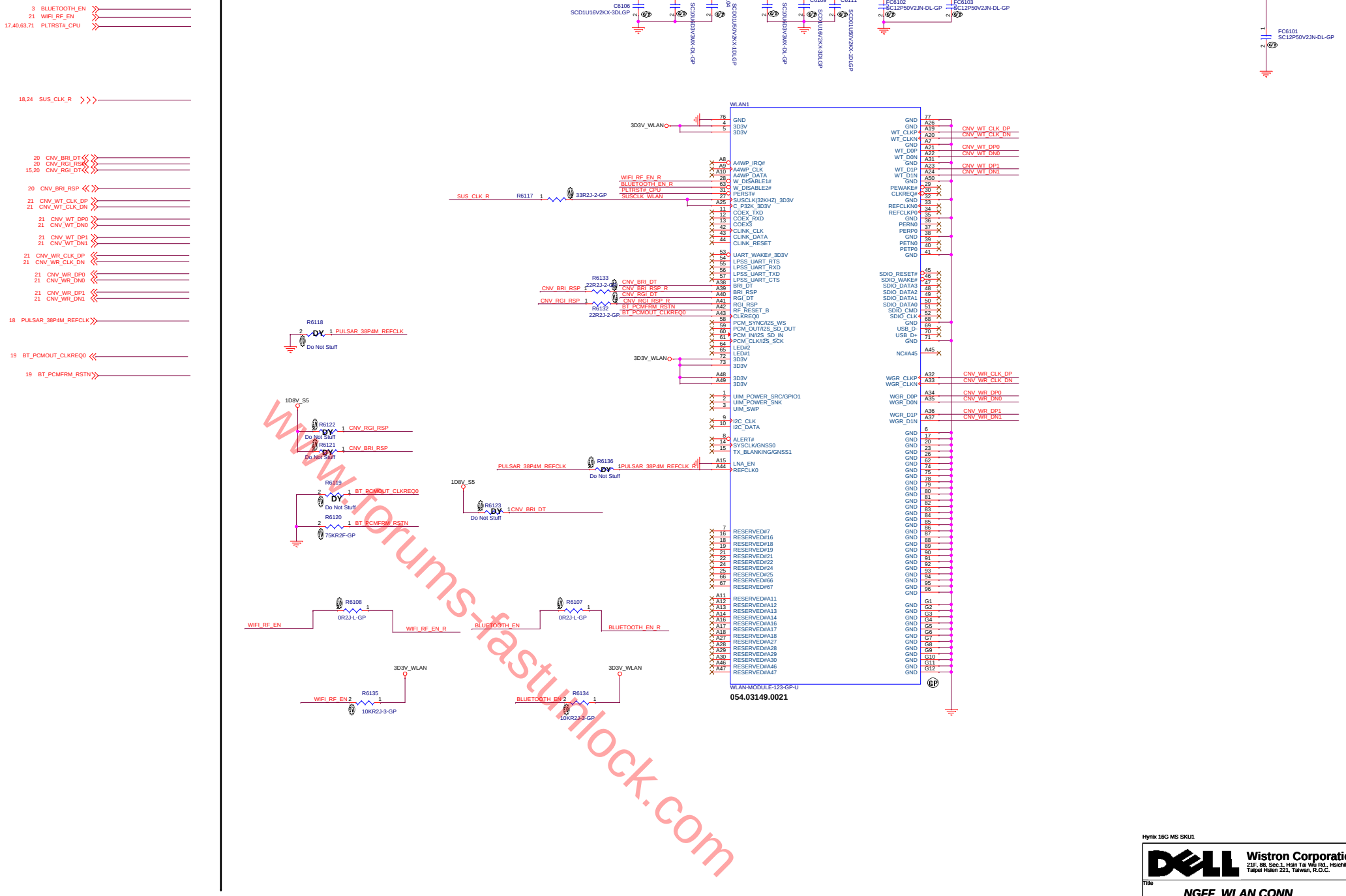
Main Func = WLAN



Hynix 16G MS SKU1

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Title: NGFF WLAN CONN

Size: A2 | Document Number: JEDI 13" | Rev: SB

Date: Monday, October 28, 2019 | Sheet 61 of 106

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	***JEDI 13"***	***SC***

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Main Func = SSD M.2

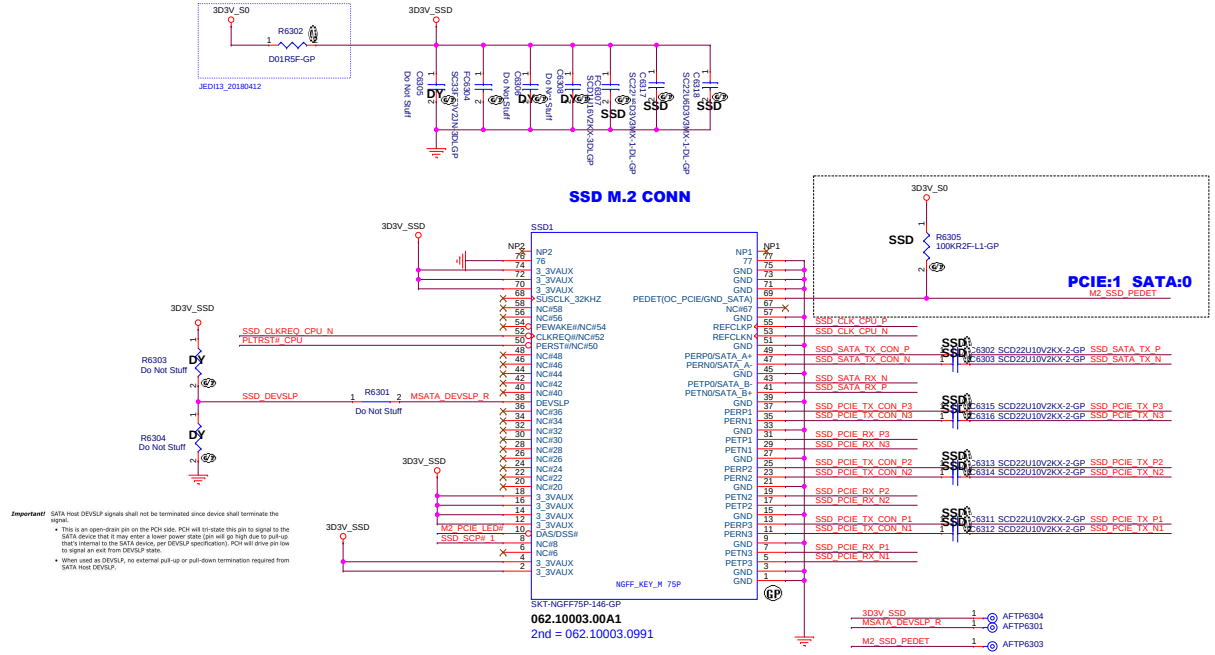
16 SSD_PCIE_TX_N3
16 SSD_PCIE_TX_P3
16 SSD_PCIE_RX_N3
16 SSD_PCIE_RX_P3

16 SSD_PCIE_TX_N2
16 SSD_PCIE_TX_P2
16 SSD_PCIE_RX_N2
16 SSD_PCIE_RX_P2

16 SSD_PCIE_TX_N1
16 SSD_PCIE_TX_P1
16 SSD_PCIE_RX_N1
16 SSD_PCIE_RX_P1

16 SSD_SATA_TX_N
16 SSD_SATA_TX_P
16 SSD_SATA_RX_N
16 SSD_SATA_RX_P

18 SSD_CLK_CPU_P
18 SSD_CLK_CPU_N
16 M2_SSD_PEDET
18 SSD_CLKREQ_CPU_N
17,40,61,71 PLTRST# CPU
16 SSD_DEVSLP
64 M2_PCIE_LED#
24 SSD_SCP#



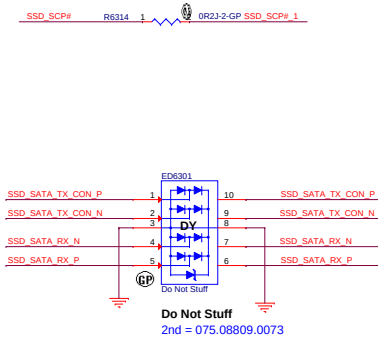


Table 13-11.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

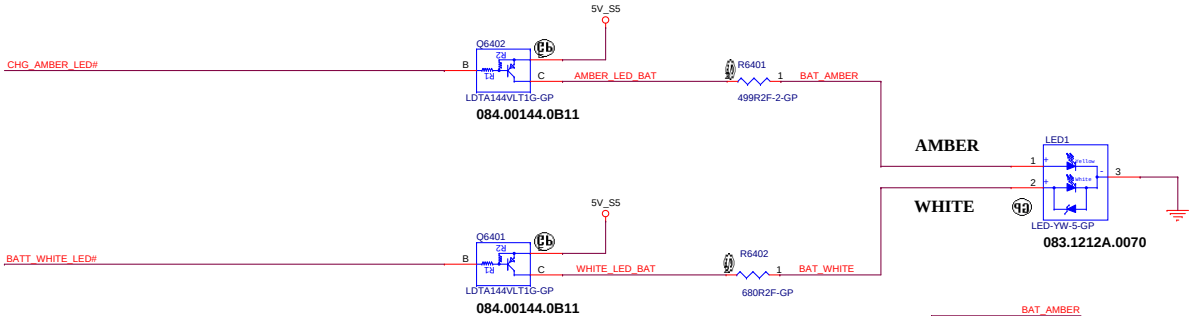
Title: INT IO (SSD M.2/ eMMC)

Size	Document Number	Rev
A2	JEDI 13"	SC

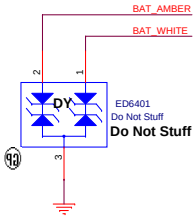
Date: Monday, October 28, 2019 Sheet 63 of 106

Main Func = Power BTN

Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

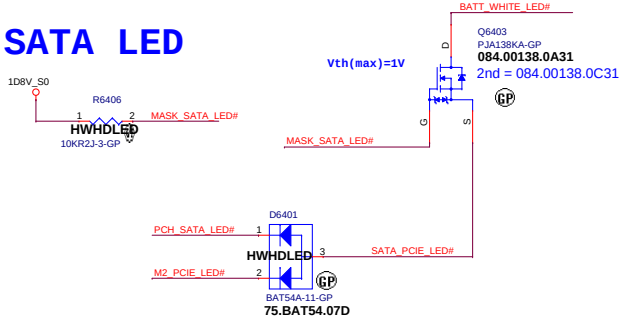


24 CHG_AMBER_LED#
24 BATT_WHITE_LED#
16 PCH_SATA_LED#
63 M2_PCIE_LED#
20,24,67,92 LID_CL_SIO#
24 MASK_SATA_LED#
17,24 PCH_RSMRST#
24,66,92 KBC_PWRBTN#
24,44 HW_ACAV_IN
24 M_BIST
24 BAT2_LED#

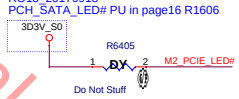
check

JEDI 13_20180709

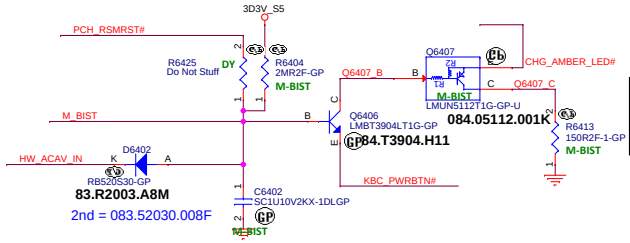
SATA LED



RO13_20170918
PCH_SATA_LED# PU in page16 R1606



M-BIST for G10 (Proposed schematic)



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

Hynix 16G MS SKU1

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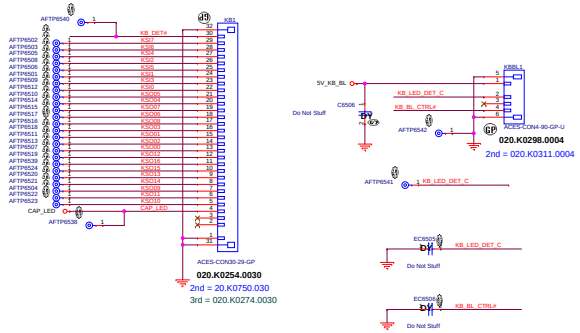
Title: LED / Button / Power Button

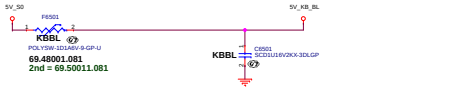
Size: Custom | Document Number: JEDI 13" | Rev: SC

Date: Monday, October 28, 2019 | Sheet 64 of 106

SSID = KB

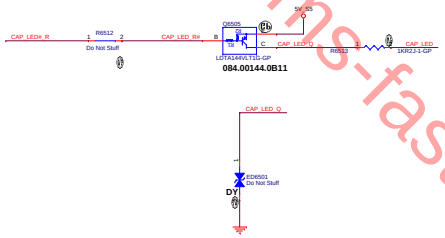
Main Func = Keyboard



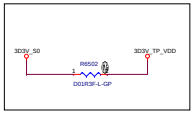


KB Backlight Power Consumption: 285mA max.

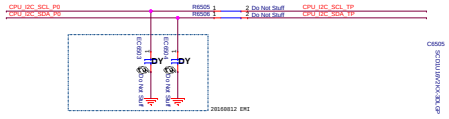
CAP LED Control
LOW actived from KBC GPIO

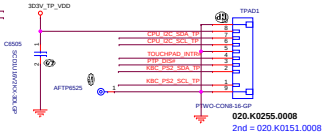


Main Func = TPAD

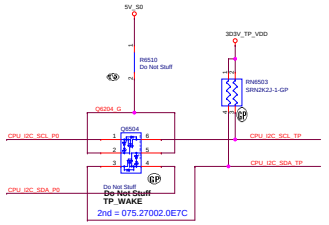


I2C

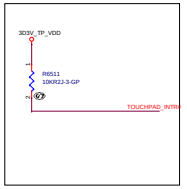




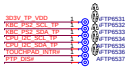
Change pindefine DVT1 0210 1330



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



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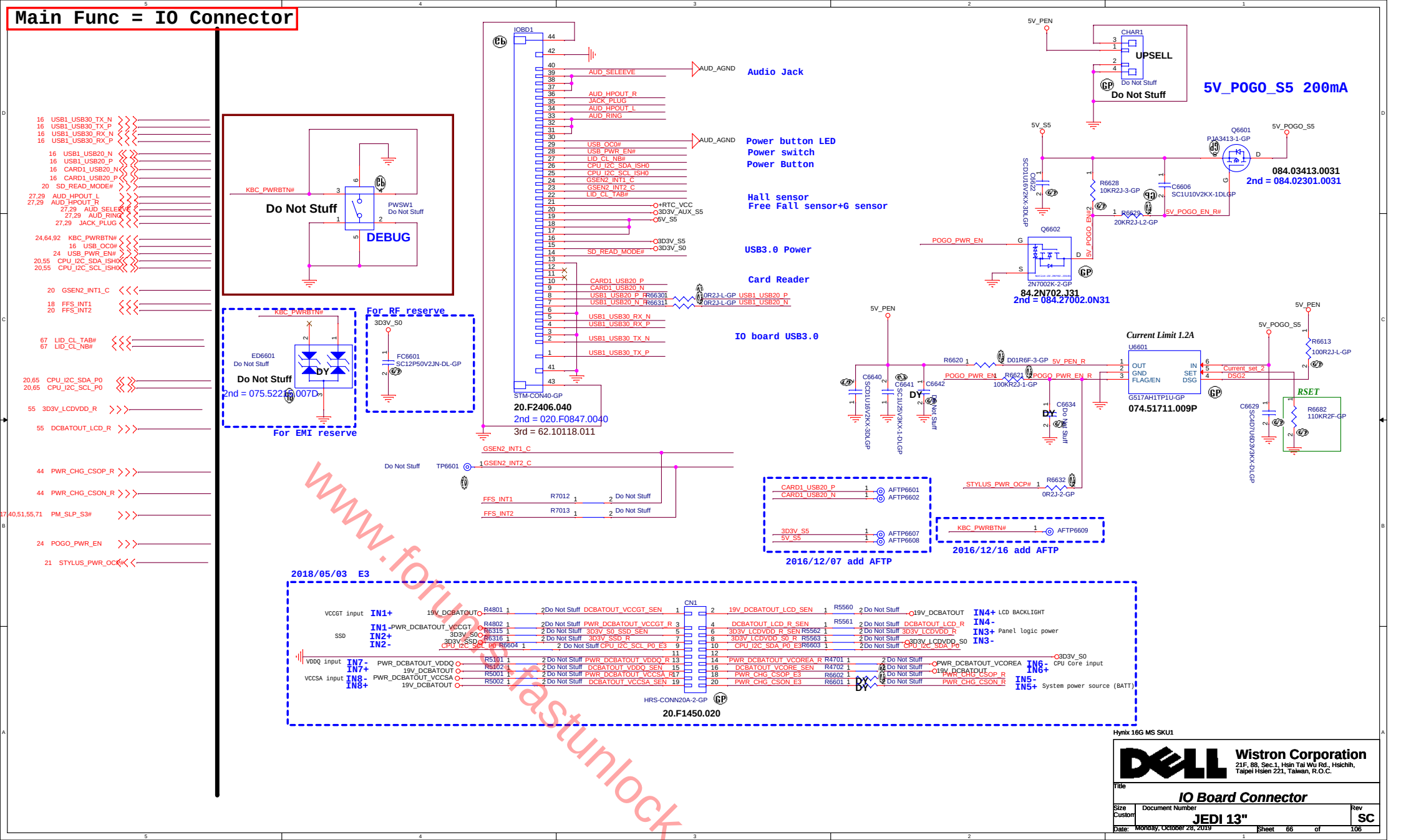
Title: Key Board&Touch Pad

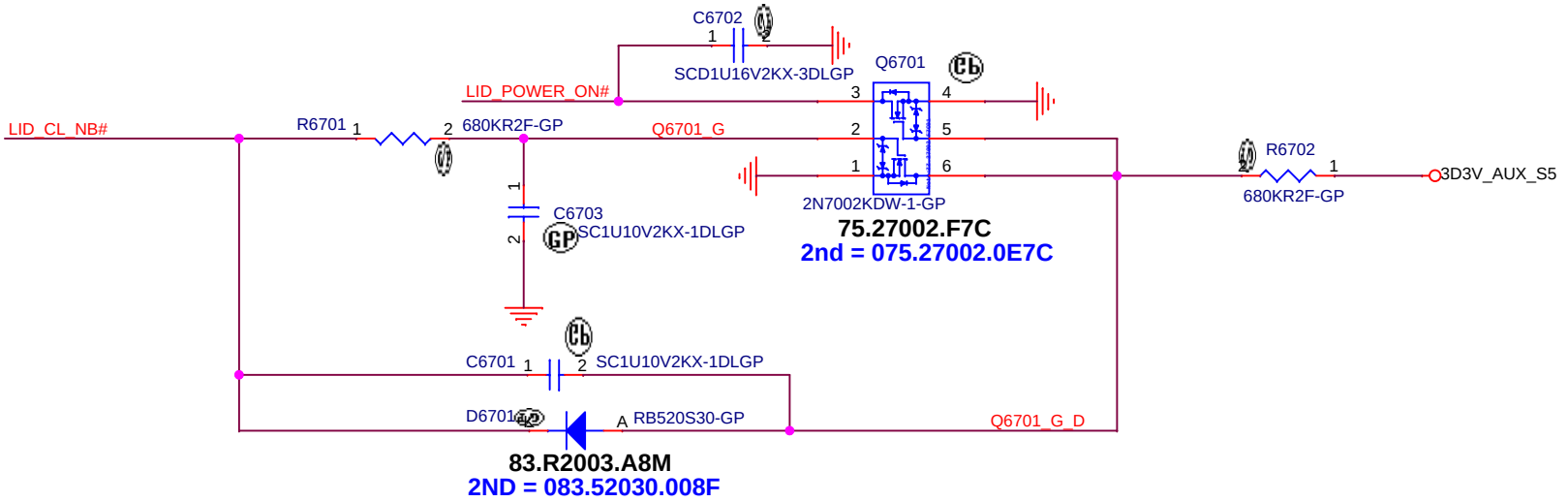
Size: A1 | Document Number: JEDI 13" | Rev: SC

Date: Monday, October 29, 2012 | Sheet 65 of 88

Main Func = IO Connector



Main Func = HALL SENSOR



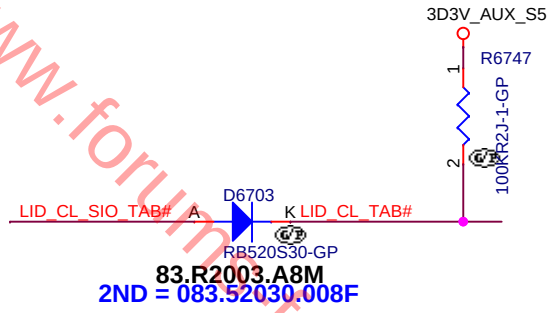
24 LID_POWER_ON#

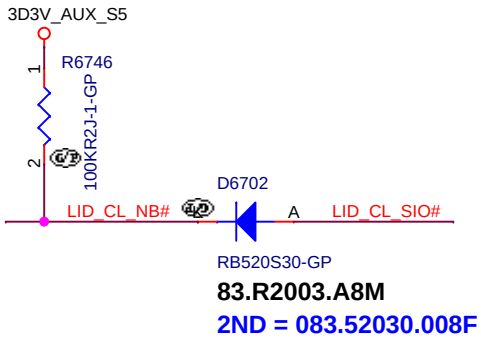
20,24 LID_CL_SIO_TAB#

20,24,92 LID_CL_SIO#

66 LID_CL_TAB#

66 LID_CL_NB#





<Core Design>

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Title: Sensor (Hall-Sensor)

Size	Document Number	Rev
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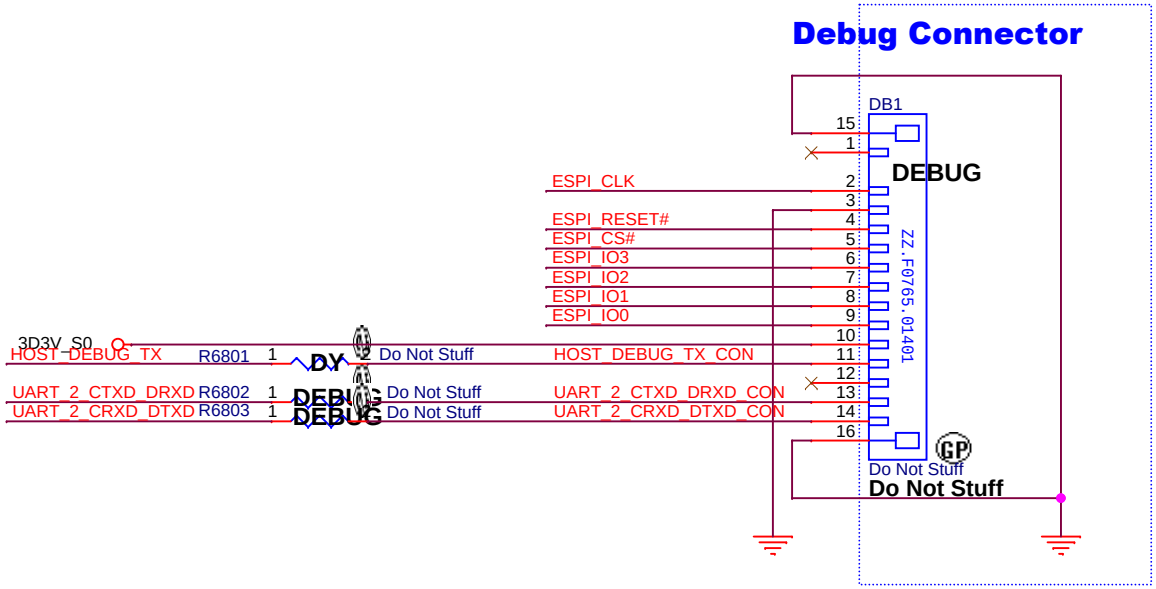
Main Func = Debug

18,24 ESPI_IO[3..0] → ESPI_IO3, ESPI_IO2, ESPI_IO1, ESPI_IO0

18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#
24 HOST_DEBUG_TX
20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD



RO13_20170822
DUMMY PAD to CONNECTOR 20.F0765.014

<Core Design>

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Title: Dubug connector

Size	Document Number	Rev
A4	JEDI 13"	SC

Date: Monday, October 28, 2019 Sheet 68 of 106

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Title

Reserved

Size	Document Number	Rev
A4	***JEDI 13"***	***SC***

Date: Monday, October 28, 2019 Sheet 69 of 106

<Core Design>

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Title
(Reserved)

Size	Document Number	Rev
A2	*JEDI 13"*	*SC*

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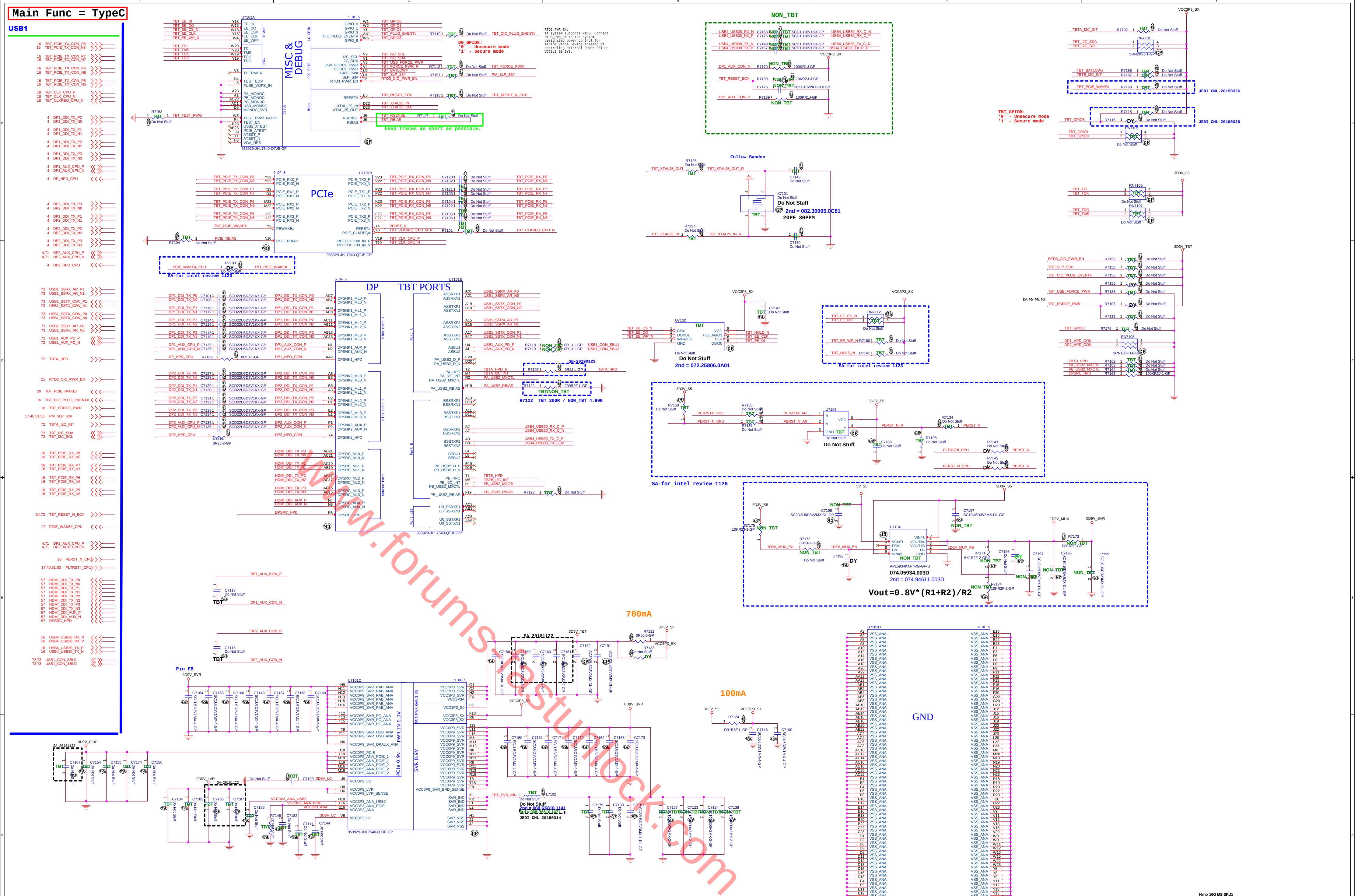
Main Func = TypeC
USB1
MISC & DEBUG
RTD3_PWR_EN:
If system supports RTD3, Connect RTD3_PWR_EN to the system designated power control for Alpine Ridge device instead of controlling external Power FET on VCC3v3_S0_SYS.
DG_GPIO8:
'0' - Unsecure mode
'1' - Secure mode
keep traces as short as possible.
PCIe
SA-for intel review 1123
DP
TBT PORTS
NON_TBT
Follow Bandon
Do Not Stuff
2nd = 082.30005.0C81
20PF 30PPM
2nd = 072.25806.0A01
SA-for intel review 1126
074.05934.003D
2nd = 074.94611.003D
Vout=0.8V*(R1+R2)/R2
JEDI CML-20190326
TBT_GPIO8:
'0' - Unsecure mode
'1' - Secure mode
700mA
100mA
GND
JEDI CML-20190314

Hynix 16G MS SKU1

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Title	EXT IO (Thunderbolt(1/3)/Type C Re-driver)
Size	A1
Document Number	Vader15"/17" CML
Rev	X00
Date	Monday, October 28, 2019
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Main Func = TypeC

24 UPD1_SMBCLK
24 UPD1_SMBDAT
24 CCG5_I2C_INT#
74 PD_VBUS_C_CTRL1
74 VBUS_P_CTRL
73 USB1_CON_CC1
73 USB1_CON_CC2
3,24,44,46 PROCHOT#_CPU
74 NXP3290_FO
74 CCG5_ILIM#
16 USB4_USB20_P
16 USB4_USB20_N
73 USB1_USB20_CMCT_P
73 USB1_USB20_CMCT_N
73 USB1_USB20_CMCB_P
73 USB1_USB20_CMCB_N
71 USB1_AUX_PD_P
71 USB1_AUX_PD_N
71,73 USB1_CON_SBU1
71,73 USB1_CON_SBU2
24,71 TBT_RESET_N_EC#
71 TBTA_HPD
71 TBT_I2C_SDA
71 TBT_I2C_SCL
71 TBTA_I2C_INT

Close to Pin32
Close to Pin31
From System
For Dead battery
083.00520.0F8F
083.00520.0F8F
PD Function
Normal: High
Avtive : Low
Un-used-> Floating
PULL-UP on TBT side
SA-for intel review 1123
TBT Reset signal
DY
EC I2C
MOD ID 2 Settings
MOD ID 1 Settings
NON_TBT Sku
R7216 & R7618 change to 100K
0x08
2nd = 075.27002.0E7C
2ND = 083.52030.008F
For Debug
Hynix 16G MS SKU1

CCG5's I2C address is decided by the SWD clock pin.
Don't mount R8 and R9 for the I2C address 0x08. This is the default one.
Mount only R9 for the I2C address 0x40.
Mount only R8 for the I2C address 0x42.

	CCG5_ID	R7216	R7218	計算值	理論值	Project Name
0/8	L0	DY	64.10035.6DL(100K)	0	0	Jedi
1/8	L1	064.71535.06D1(715K)	64.10035.6DL(100K)	0.123	0.125	
2/8	L2	64.30035.6DL(300K)	64.10035.6DL(100K)	0.25	0.25	
3/8	L3	64.20035.6DL(200K)	64.12035.6DL(120K)	0.375	0.375	
4/8	L4	64.10035.6DL(100K)	64.10035.6DL(100K)	0.5	0.5	
5/8	L5	64.12035.6DL(120K)	64.20035.6DL(200K)	0.625	0.625	
6/8	L6	64.22035.6DL(220K)	64.59035.6DL(590K)	0.728	0.75	
7/8	L7	64.10035.6DL(100K)	064.71535.06D1(715K)	0.877	0.875	

MOD_ID Mux Allocations

- These configurations are based on v2 of the Dell notebook reference schematics

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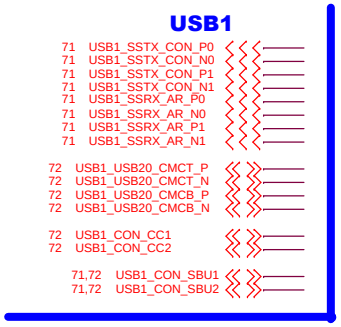
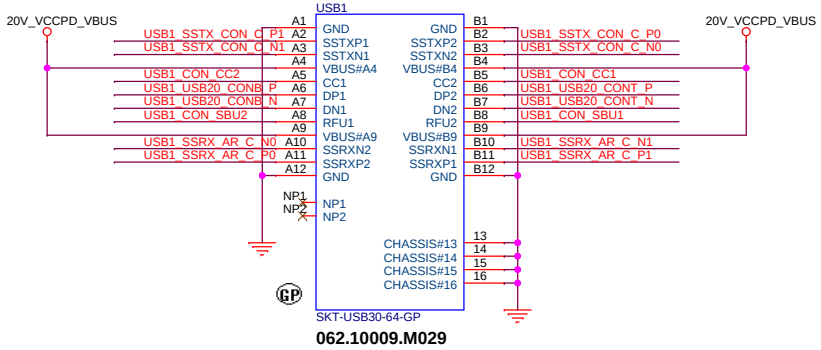
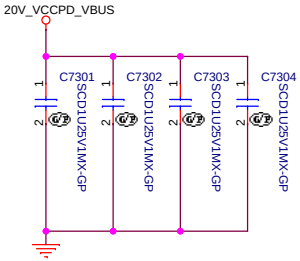
Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)
Size: A3
Document Number: Jedi15"/17" CML
Rev: SC
Date: Monday, October 28, 2019
Sheet 72 of 106

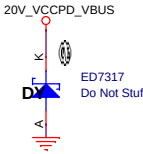
Main Func = TypeC

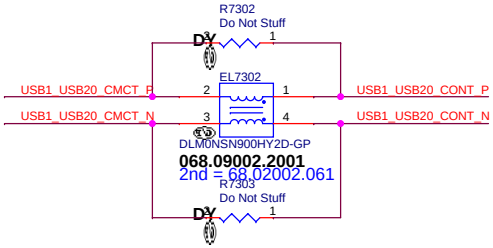


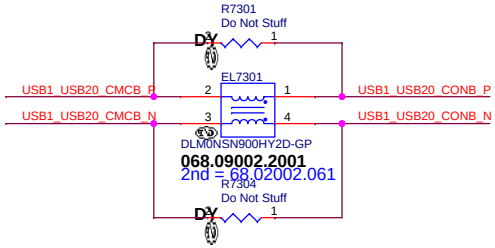


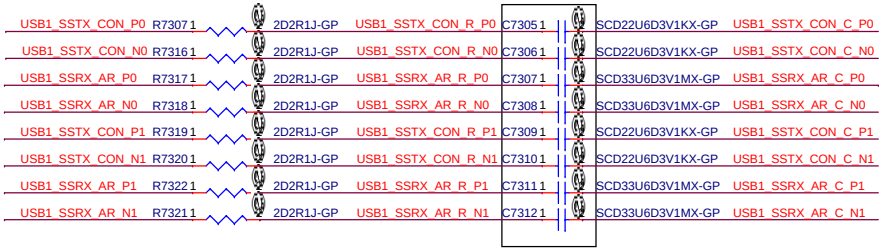


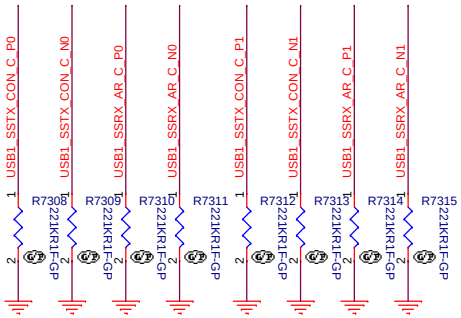
Bom to [078.47412.05S1]

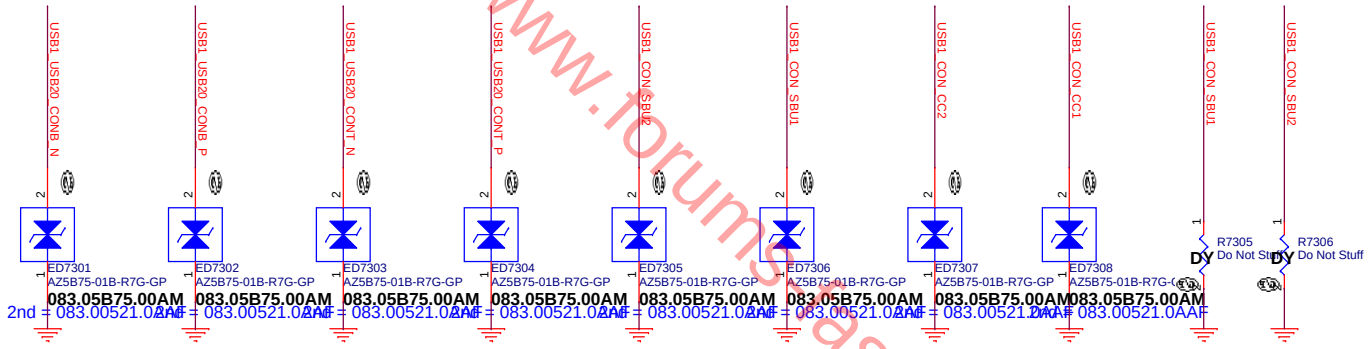


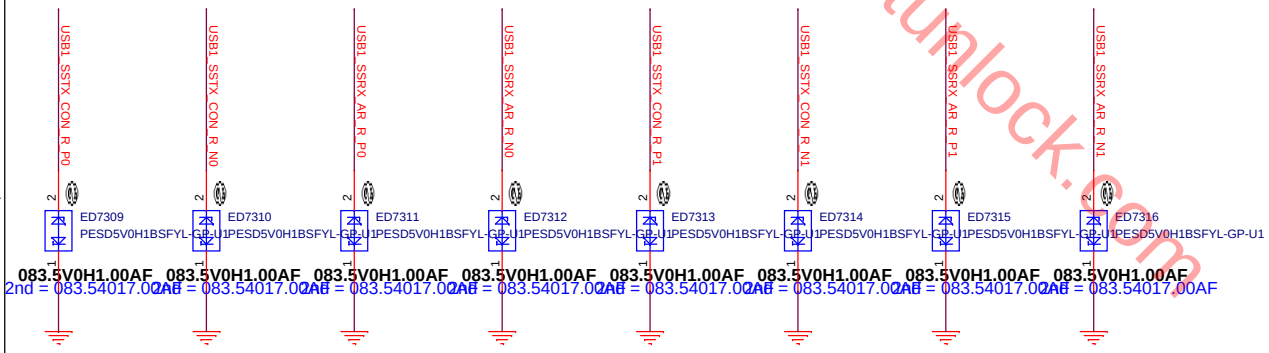












Hynix 16G MS SKU1

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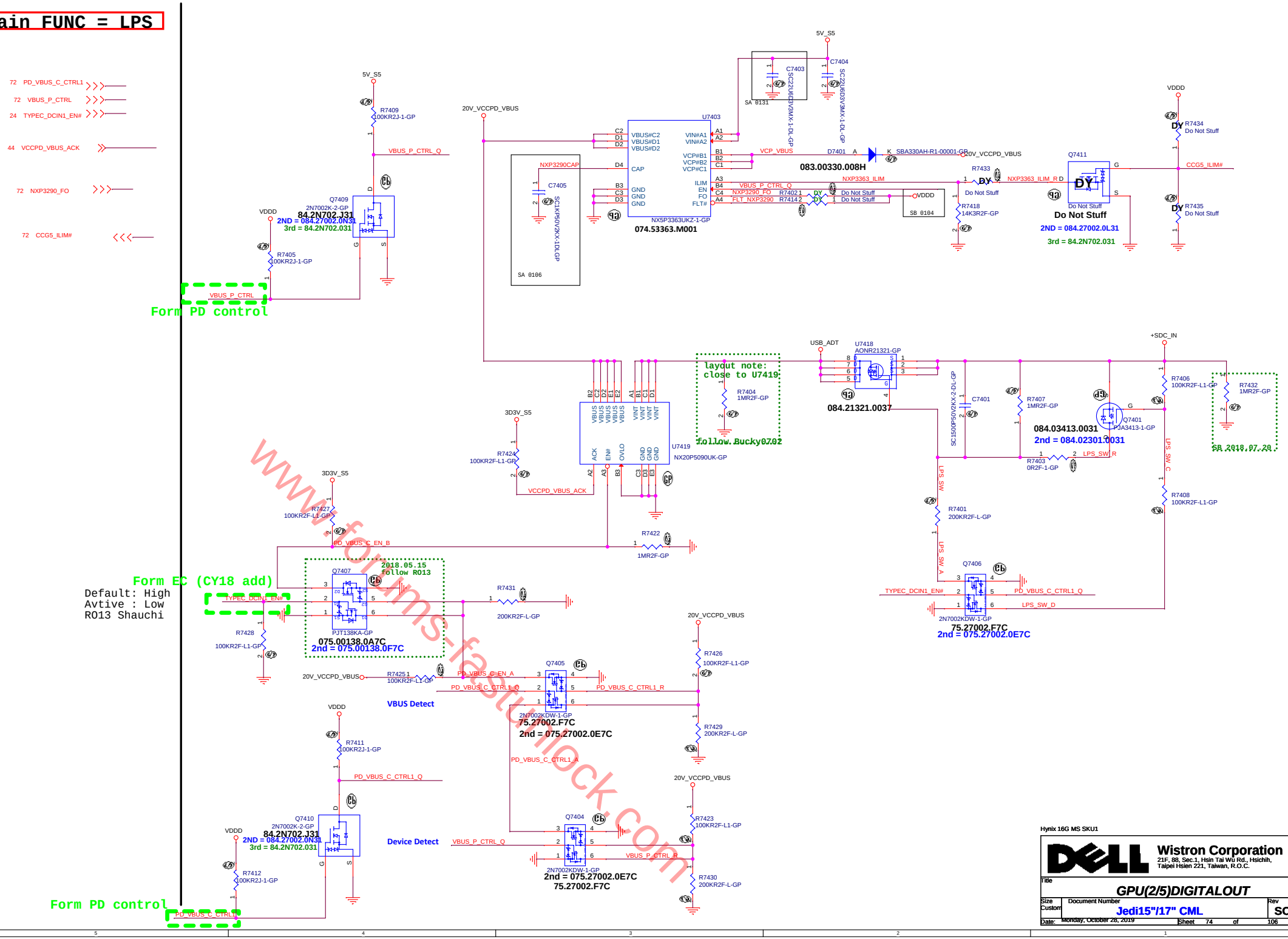
Title: EXT IO (Thunderbolt(3/3)/Type C Conn)

Size: A3 | Document Number: Jedi15"/17" CML | Rev: SC

Date: Monday, October 28, 2019 | Sheet 73 of 106

Main FUNC = LPS



Hynix 16G MS SKU1

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Title	GPU(2/5)DIGITALOUT	
Size: Custom	Document Number: Jedi15"/17" CML	Rev: SC
Date: Monday, October 28, 2019	Sheet 74 of 106	

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
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Main Func = dGPU

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
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Date: Monday, October 28, 2019 Sheet 77 of 106

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A2	*JEDI 13"*	*SC*

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
Custom	JEDI 13"	SC

Date: Monday, October 28, 2019 Sheet 80 of 108

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A3	JEDI 13"	SC

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A2	*JEDI 13"*	*SC*

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
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Main Func = UnusedParts

34.4YW18.001

SB 0129 just footprint

HS1
STFT237B158R128H48-GP
434.0FD01.0001

H1 Do Not Stuff — Do Not Stuff
H2 Do Not Stuff — Do Not Stuff
H3 Do Not Stuff — Do Not Stuff
H4 Do Not Stuff — Do Not Stuff
H5 Do Not Stuff — Do Not Stuff
H12 Do Not Stuff — Do Not Stuff
H9 Do Not Stuff — Do Not Stuff

2016/12/14 move from P.10 to P.89

1V_VCCGT
2017/03/21
EC8905 DY
EC8906 DY Do Not Stuff

1V_CPU_CORE
EMI reserve , 20141118
EC8902 DY Do Not Stuff
EC8903 DY Do Not Stuff
EC8904 DY Do Not Stuff

1V_VCCSA
EC8907 DY Do Not Stuff
EC8901 DY Do Not Stuff

1V_CPU_CORE
EC8937 DY Do Not Stuff
EC8938 DY Do Not Stuff

3D3V_S0
EC8980 DY Do Not Stuff
EC8981 DY Do Not Stuff
EC8982 DY Do Not Stuff
EC8983 DY Do Not Stuff
EC8984 DY Do Not Stuff
EC8985 DY Do Not Stuff
EC8987 DY Do Not Stuff
EC8986 DY Do Not Stuff
EC8988 DY Do Not Stuff
EC8989 DY Do Not Stuff

PWR_DCBATOUT_VCOREA
EC8995 DY Do Not Stuff
EC8996 DY Do Not Stuff

PWR_DCBATOUT_VCCGT
EC8997 DY Do Not Stuff

5V_S0
EC8970 DY Do Not Stuff
EC8971 DY Do Not Stuff
EC8972 DY Do Not Stuff
EC8973 DY Do Not Stuff
EC8974 DY Do Not Stuff
EC8975 DY Do Not Stuff
EC8977 DY Do Not Stuff
EC8976 DY Do Not Stuff
EC8978 DY Do Not Stuff
EC8979 DY Do Not Stuff

BT+
EC8990 DY SC1K50V2KX-1DLGP
EC8991 DY Do Not Stuff
EC8992 DY Do Not Stuff
EC8993 SC1K50V2KX-1DLGP
EC8994 SC1K50V2KX-1DLGP

3D3V_S5
EC8921 DY Do Not Stuff
EC8922 DY Do Not Stuff
EC8923 DY Do Not Stuff
EC8924 DY Do Not Stuff
EC8925 DY Do Not Stuff
EC8926 DY Do Not Stuff
EC8956 DY Do Not Stuff
EC8957 DY Do Not Stuff
EC8958 DY Do Not Stuff
EC8959 DY Do Not Stuff

+SDC_IN
EC8960 DY SC1K50V2KX-1DLGP
EC8961 DY Do Not Stuff
EC8962 DY Do Not Stuff
EC8963 SC1K50V2KX-1DLGP
EC8964 DY SC1K50V2KX-1DLGP
EC8965 DY Do Not Stuff
EC8966 SC1K50V2KX-1DLGP
EC8967 DY Do Not Stuff
EC8968 SC1K50V2KX-1DLGP
EC8969 DY Do Not Stuff

SSID = EMI

Mind the voltage rating of the caps.

19V_DCBATOUT
EC8908 DY Do Not Stuff
EC8909 SC1K50V2KX-1DLGP
EC8910 SC1K50V2KX-1DLGP
EC8911 SC1K50V2KX-1DLGP
EC8912 SC1K50V2KX-1DLGP
EC8913 DY Do Not Stuff
EC8914 SC1K50V2KX-1DLGP
EC8915 SC1K50V2KX-1DLGP
EC8916 DY Do Not Stuff
EC8917 SC1K50V2KX-1DLGP

5V_S5
EC8918 DY Do Not Stuff
EC8919 DY Do Not Stuff
EC8920 DY Do Not Stuff
EC8927 DY Do Not Stuff
EC8928 DY Do Not Stuff
EC8929 DY Do Not Stuff
EC8952 DY Do Not Stuff
EC8953 DY Do Not Stuff
EC8954 DY Do Not Stuff
EC8955 DY Do Not Stuff

1D2V_S3
EC8930 SC1K50V2KX-1DLGP
EC8931 SC1K50V2KX-1DLGP
EC8932 DY Do Not Stuff
EC8933 SC1K50V2KX-1DLGP
EC8934 DY Do Not Stuff
EC8939 DY Do Not Stuff
EC8940 SC1K50V2KX-1DLGP
EC8941 SC1K50V2KX-1DLGP
EC8942 DY Do Not Stuff
EC8951 SC1K50V2KX-1DLGP

SSID = RF

19V_DCBATOUT
FC8905 SC12P50V2JN-DL-GP
FC8906 SC12P50V2JN-DL-GP
FC8907 SC12P50V2JN-DL-GP
FC8908 SC12P50V2JN-DL-GP
FC8909 SC12P50V2JN-DL-GP
FC8910 SC12P50V2JN-DL-GP
FC8911 SC12P50V2JN-DL-GP
FC8912 SC12P50V2JN-DL-GP
FC8913 SC12P50V2JN-DL-GP
FC8914 SC12P50V2JN-DL-GP
FC8915 SC12P50V2JN-DL-GP
FC8916 Do Not Stuff
FC8917 SC12P50V2JN-DL-GP
FC8918 SC12P50V2JN-DL-GP
FC8819 SC12P50V2JN-DL-GP
FC8820 SC12P50V2JN-DL-GP
FC8821 SC12P50V2JN-DL-GP
FC8922 SC12P50V2JN-DL-GP
FC8823 SC12P50V2JN-DL-GP
FC8824 SC12P50V2JN-DL-GP

5V_S5
FC8825 SC12P50V2JN-DL-GP
FC8926 SC12P50V2JN-DL-GP
FC8827 SC12P50V2JN-DL-GP
FC8829 SC12P50V2JN-DL-GP
FC8828 SC12P50V2JN-DL-GP
FC8831 SC12P50V2JN-DL-GP
FC8833 SC12P50V2JN-DL-GP
FC8830 SC12P50V2JN-DL-GP
FC8834 SC12P50V2JN-DL-GP
FC8832 SC12P50V2JN-DL-GP

3D3V_S5
FC8835 SC12P50V2JN-DL-GP
FC8836 SC12P50V2JN-DL-GP
FC8837 SC12P50V2JN-DL-GP
FC8839 SC12P50V2JN-DL-GP
FC8838 SC12P50V2JN-DL-GP
FC8941 SC12P50V2JN-DL-GP
FC8843 SC12P50V2JN-DL-GP
FC8940 SC12P50V2JN-DL-GP
FC8944 SC12P50V2JN-DL-GP
FC8942 SC12P50V2JN-DL-GP

1D0V_S5
FC8945 SC12P50V2JN-DL-GP

Hynix 16G MS SKU1

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Main Func = TPM

Hynix 16G MS SKU1

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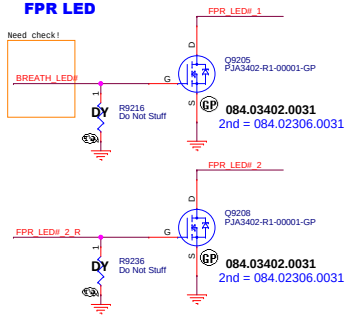
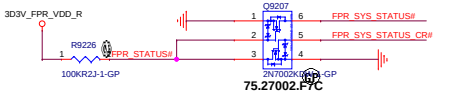
Main Func = FPR

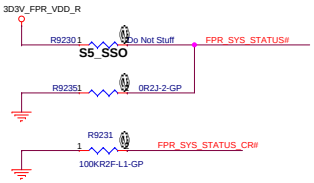
16 FP1_USB20_N
16 FP1_USB20_P
24 FPR_SCAN#
17,40,51 PM_SLP_S4#
24,64,66 KBC_PWRBTN#
20,24,67 LID_CL_SIO#
24 BREATH_LED#
Need check!
18,24,26 CPU_SMB_SDA_P1
C18,24,26 CPU_SMB_SCL_P1

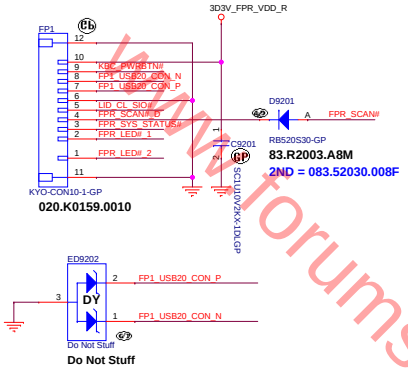
FPR LED



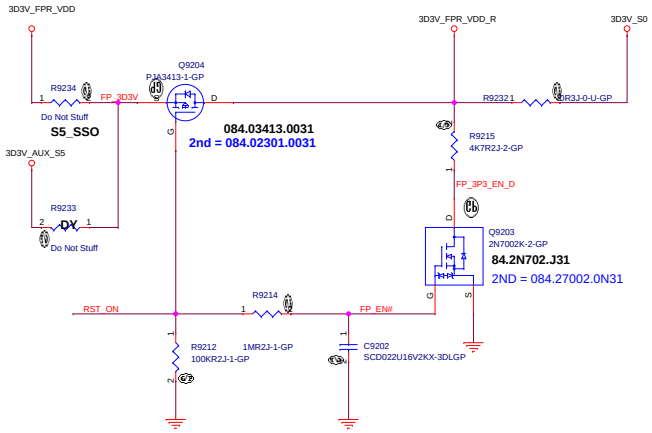
FPR SYSTEM STATUS



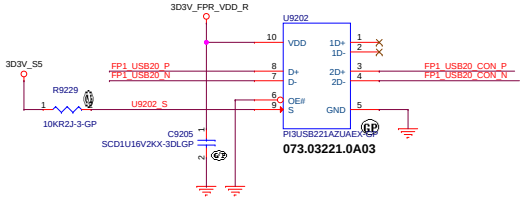




FPR POWER RESET



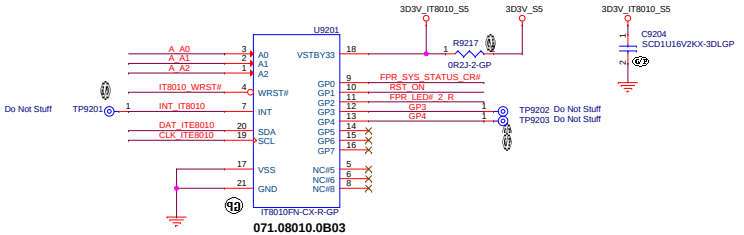
FPR USB CURRENT LEAKAGE

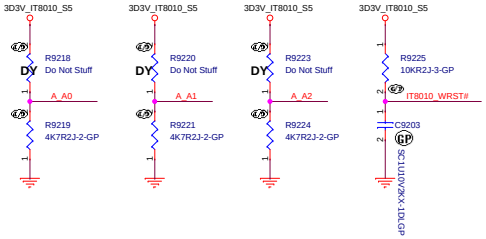


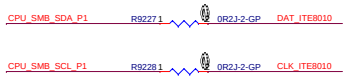
Truth Table

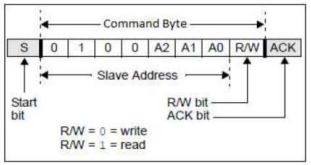
S	OE	Function
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

GPIO EXPANDER









I2C SAD+Read/Write patterns

Command SAD[7:4]	A[2]	A[1]	A[0]	R/W=	SAD+R/W
Read	0100	0	0	0	1	01000001 (41h)
Write	0100	0	0	0	0	01000000 (40h)
Read	0100	0	0	1	1	01000011 (43h)
Write	0100	0	0	1	0	01000010 (42h)
Read	0100	1	1	1	1	01001111 (4Fh)
Write	0100	1	1	1	0	01001110 (4Eh)

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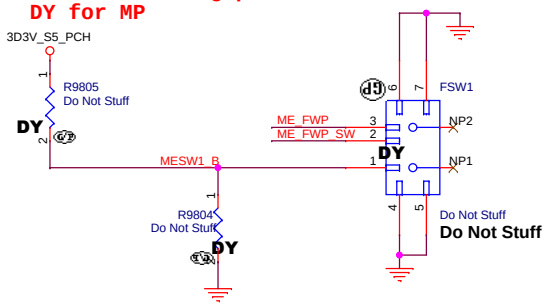
Main Func = SWITCH

ME_FWP — R9806 (2 / 1) — ME_FWP_SW
Do Not Stuff

24 ME_FWP
19 ME_FWP_SW

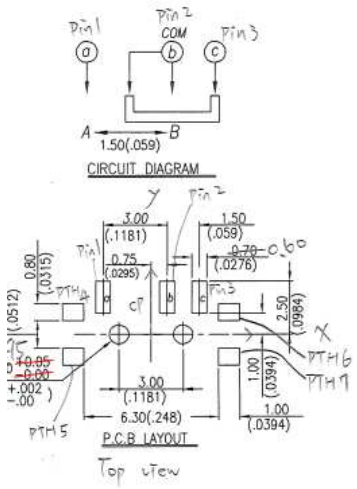
Firmware SW

Default setting:pull LOW
DY for MP



	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

*Symbol same as 62.40018.461.



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Title: CRT_Switch

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SSID = Debug

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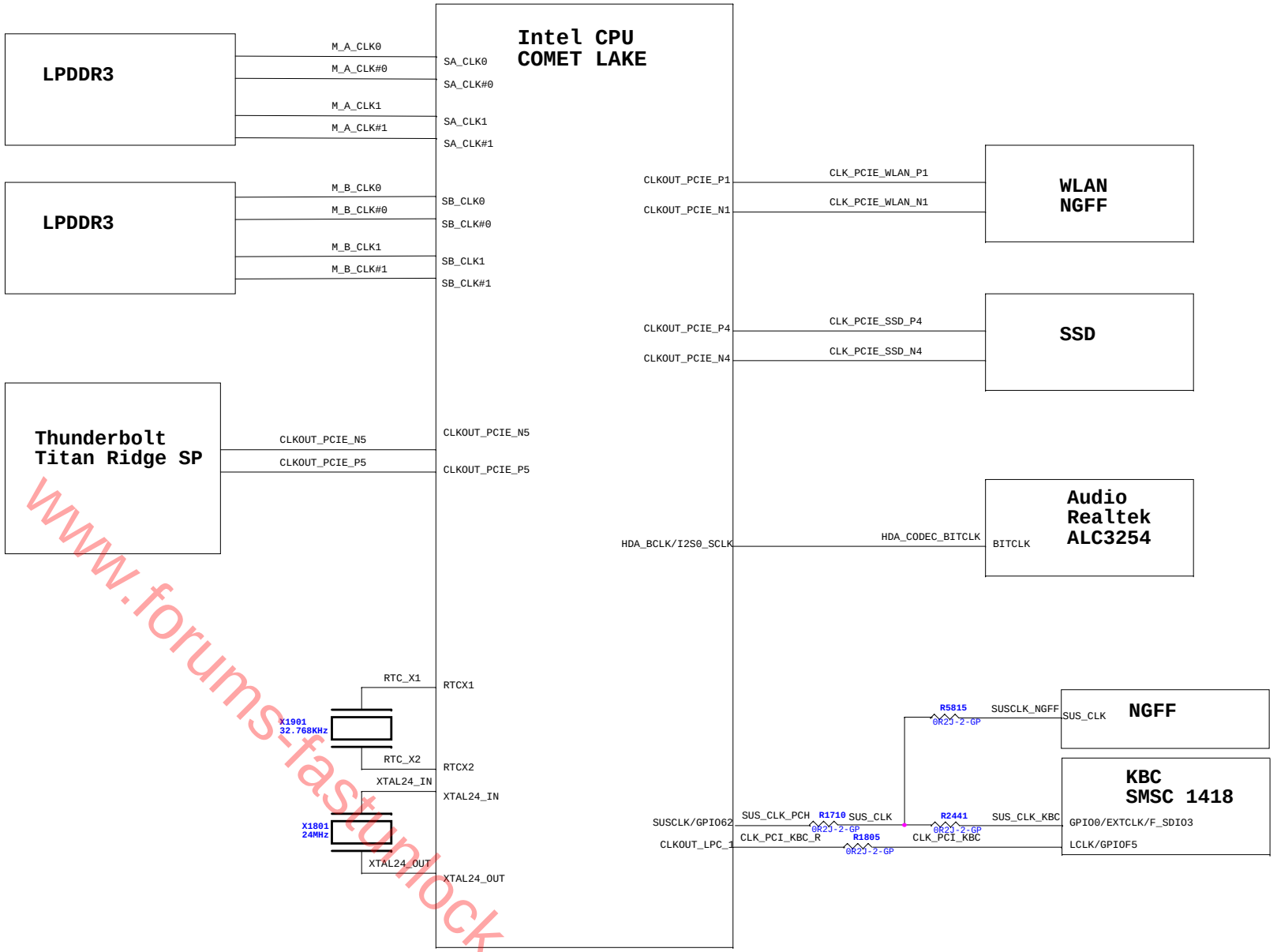
CLK Block Diagram



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Title: CLK Block Diagram

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER
	X01	01/17	57	R5785 change from 10K to 20K ohm	
	X01	01/17	44	Vcore_OVP & Vsys_UVP circuits DY	
	X01	01/17	21	Reserve R2103(75k ohm) pull down	
	X01	01/23	24	R2443 Change to 17.8K Ohm	
	X01	01/29	18	C1807 & C1808 Change 15pF to 12pF	
	X01	01/29	71	TBTA_HPD add R7107(0 Ohm)	
	X01	01/29	3~23	Change CPU P/N to ZZ.00CPU.361(Intel CML)	

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Title: Change History

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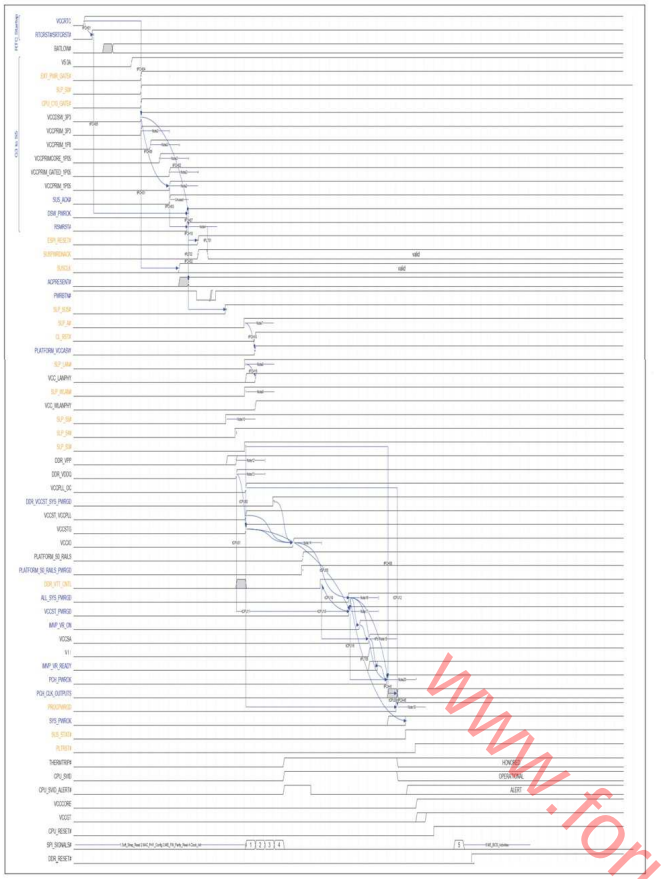
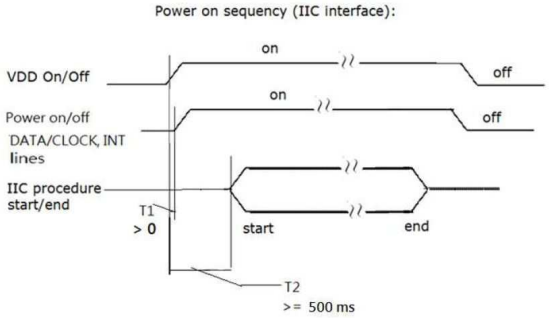
CML-U Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



[TP] Power-Up Sequence



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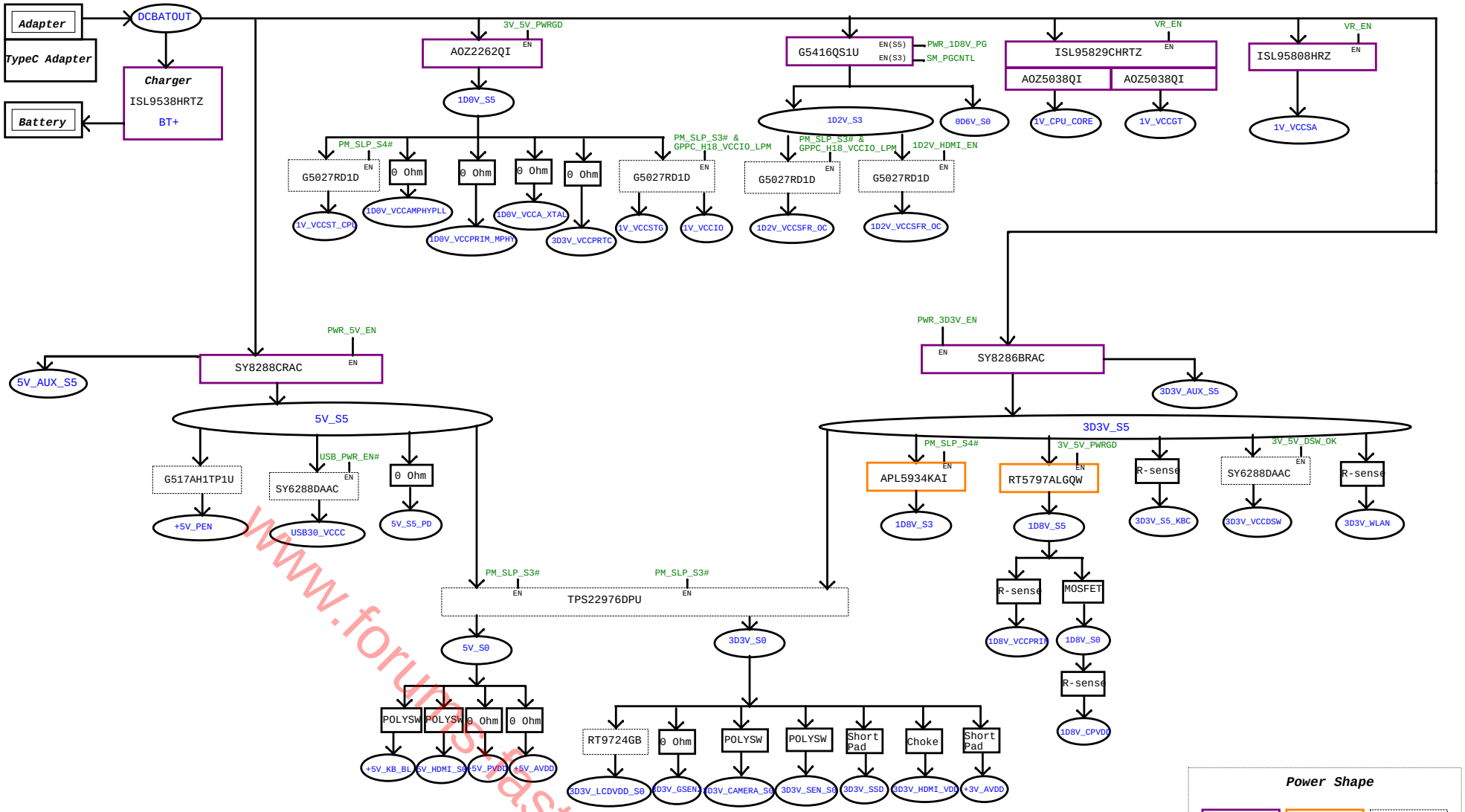

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Title: Power Block Diagram

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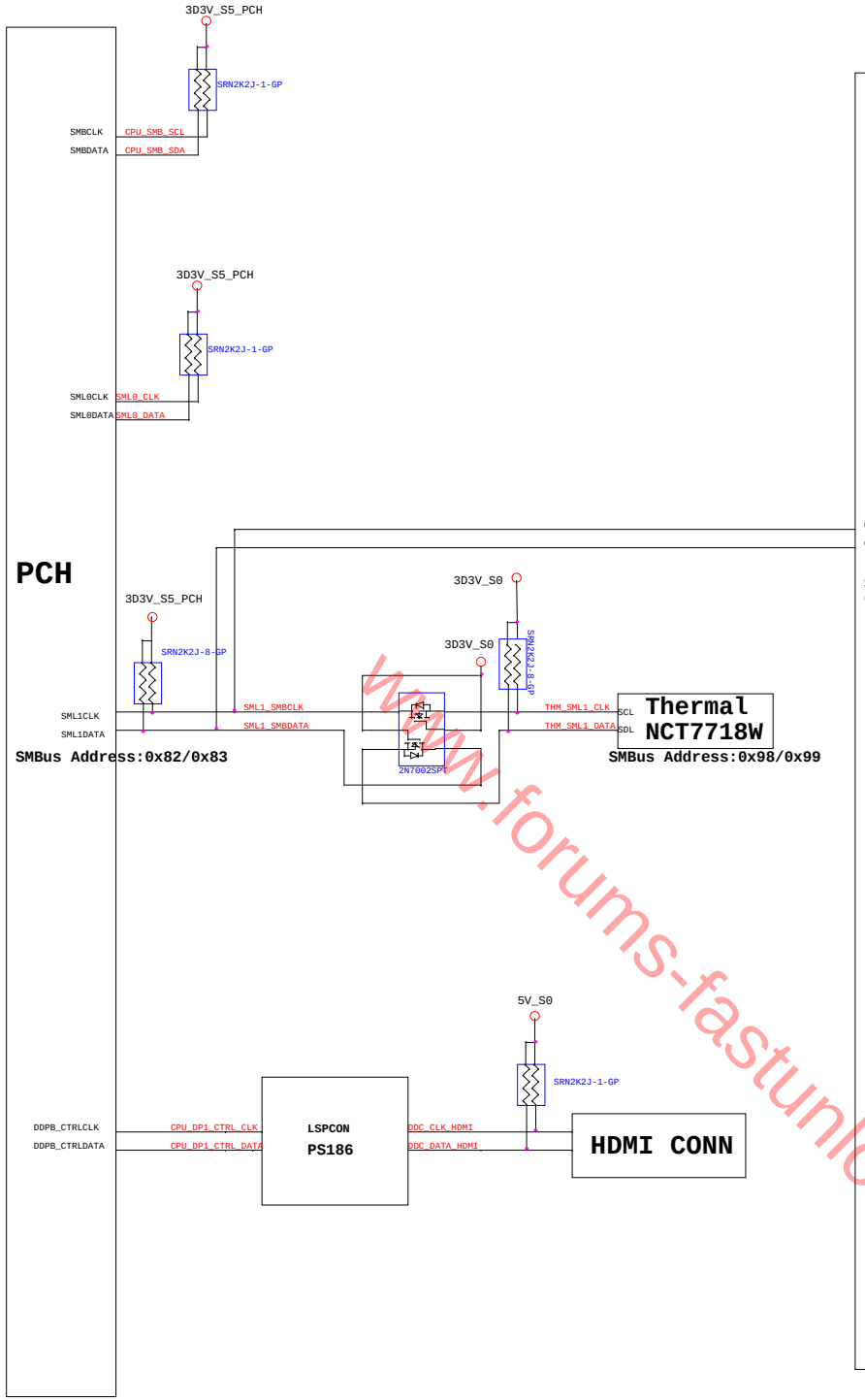
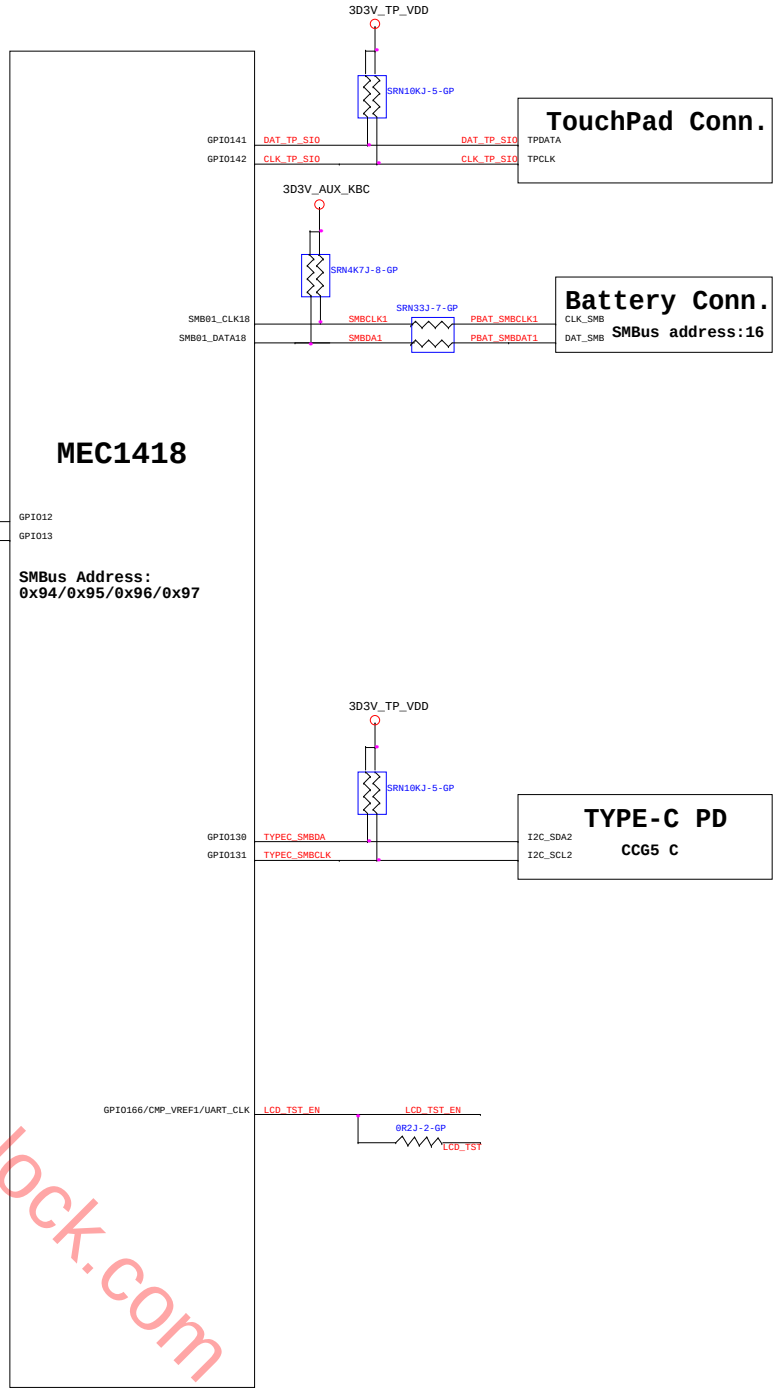
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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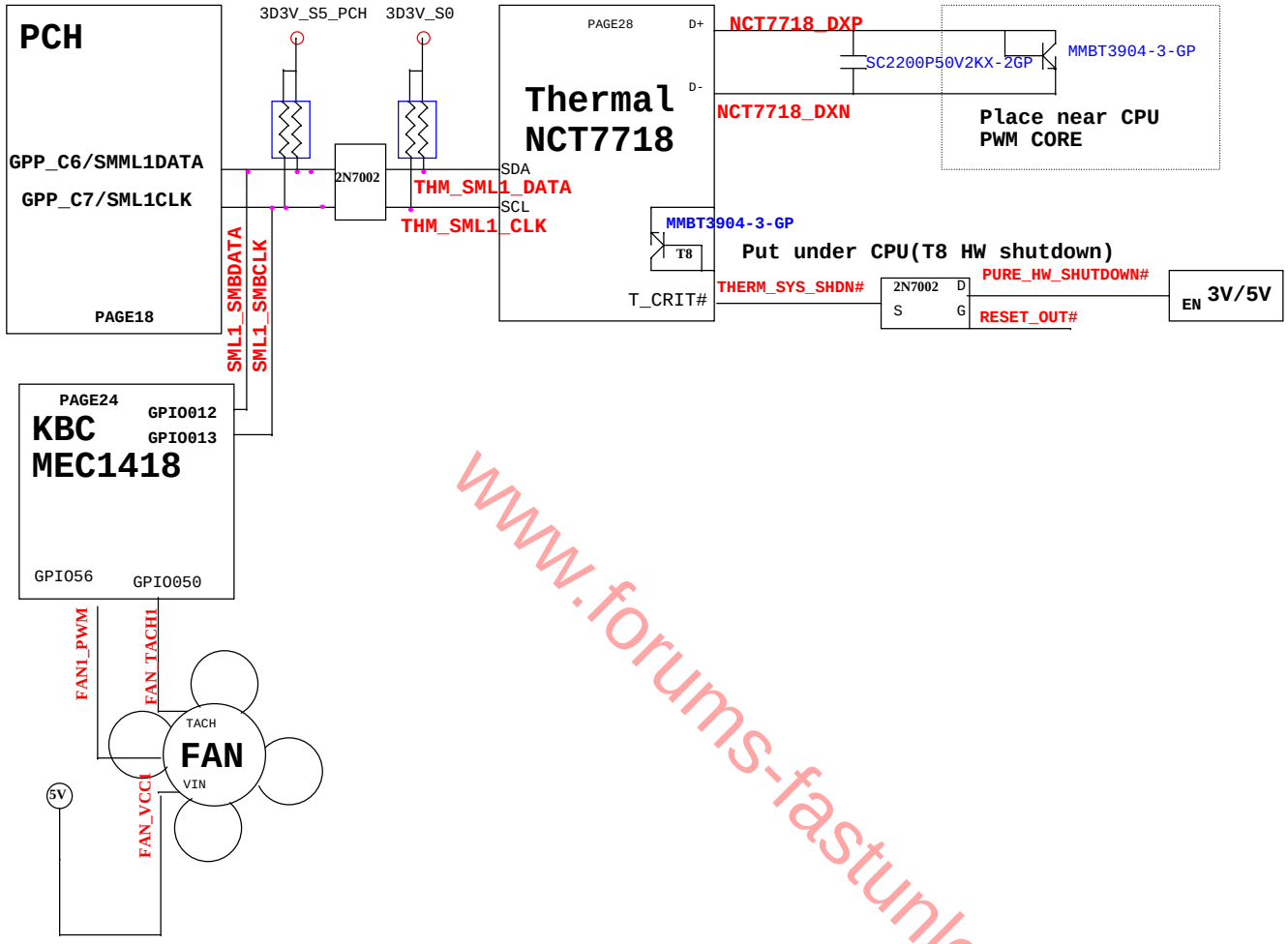
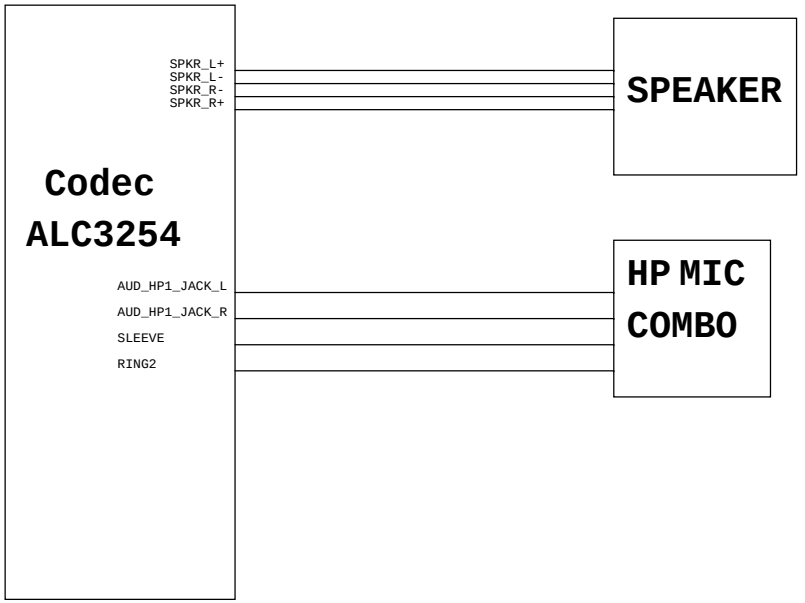
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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SIP connector

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