
GF10x/11x Design Overview
NVIDIA
2011.2.21
NVIDIA CONFIDEN

Agenda

- Schematic Design Overview
  - PCI-Express
  - Memory Controller Interface
  - Display Interface
  - MIO(SLI)
  - I2C
  - GPIO
  - Straps
  - Power
  - Others

Schematic Design Overview

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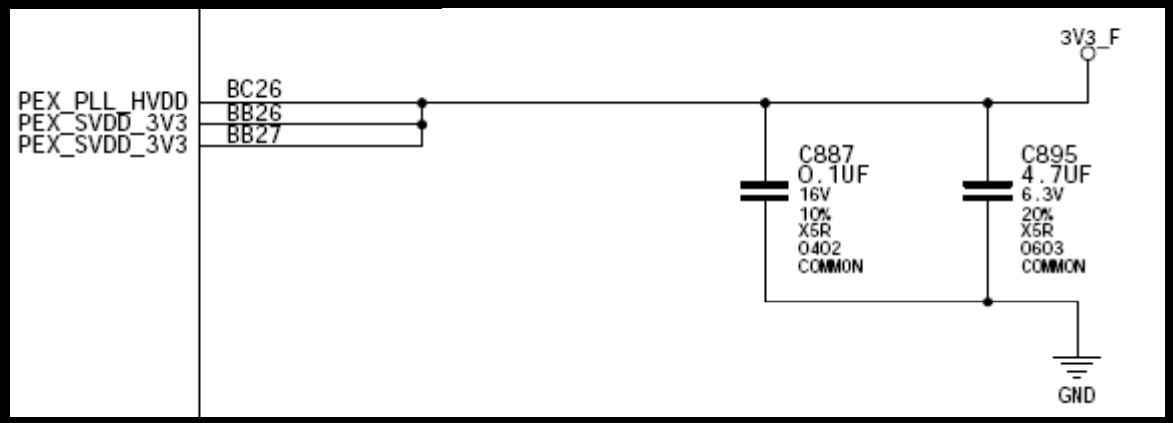
PCI-Express

- Ensure PEX_RST* and PEX_REFCLK are connected.
- PEX_TSTCLK_OUT should be terminated with a 200 ohm resistor and made easily accessible for probing, default can be unstuffed.
- PEX_TEMP is used for internal calibration, pull-down this signal with a 2.49Kohm 1% resistor.
- PEX_CLK_REQ* is an open-drain bi-directional signal, by default it should have a 10Kohm pull-up to 3.3V, This signal is an active low signal.
- For default and production, PD TestMode to Gnd with 10K.

PCI-Express

- Interface Power Rails
  - PEX_IOVDD/Q – PEX_VDD
  - PEX_PLLVDD – PEX_VDD
  - PEX_SVDD_3V3 – 3.3V
  - PEX_PLL_HVDD - 3.3V

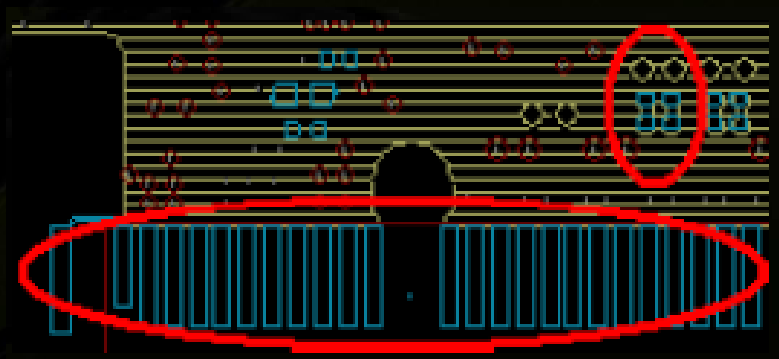


PCI-Express

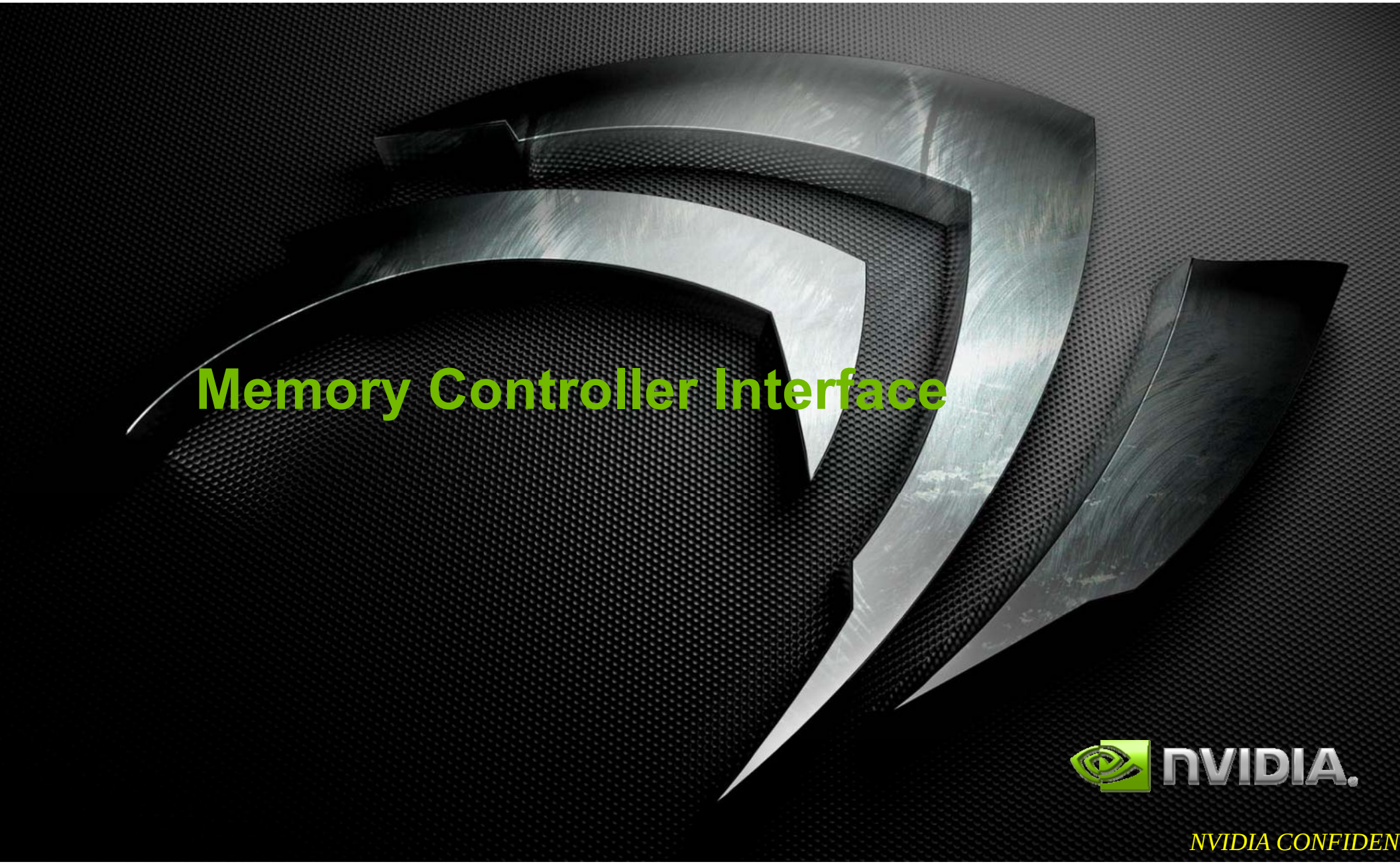
- Routing Layers: Top, Bottom
- Reference: GND
- Trace Impedance: 90Ω Diff.
- Termination: On die.
- Place the caps within 0.3 inches from the connector and void the GND plane underneath.

PCI-Express

- Plane voiding beneath AC coupling capacitor
- Plane voiding beneath PCI express edge fingers (only for signal pads is for thickness consideration)
- PCB thickness and alignment affecting edge finger contact



Memory Controller Interface

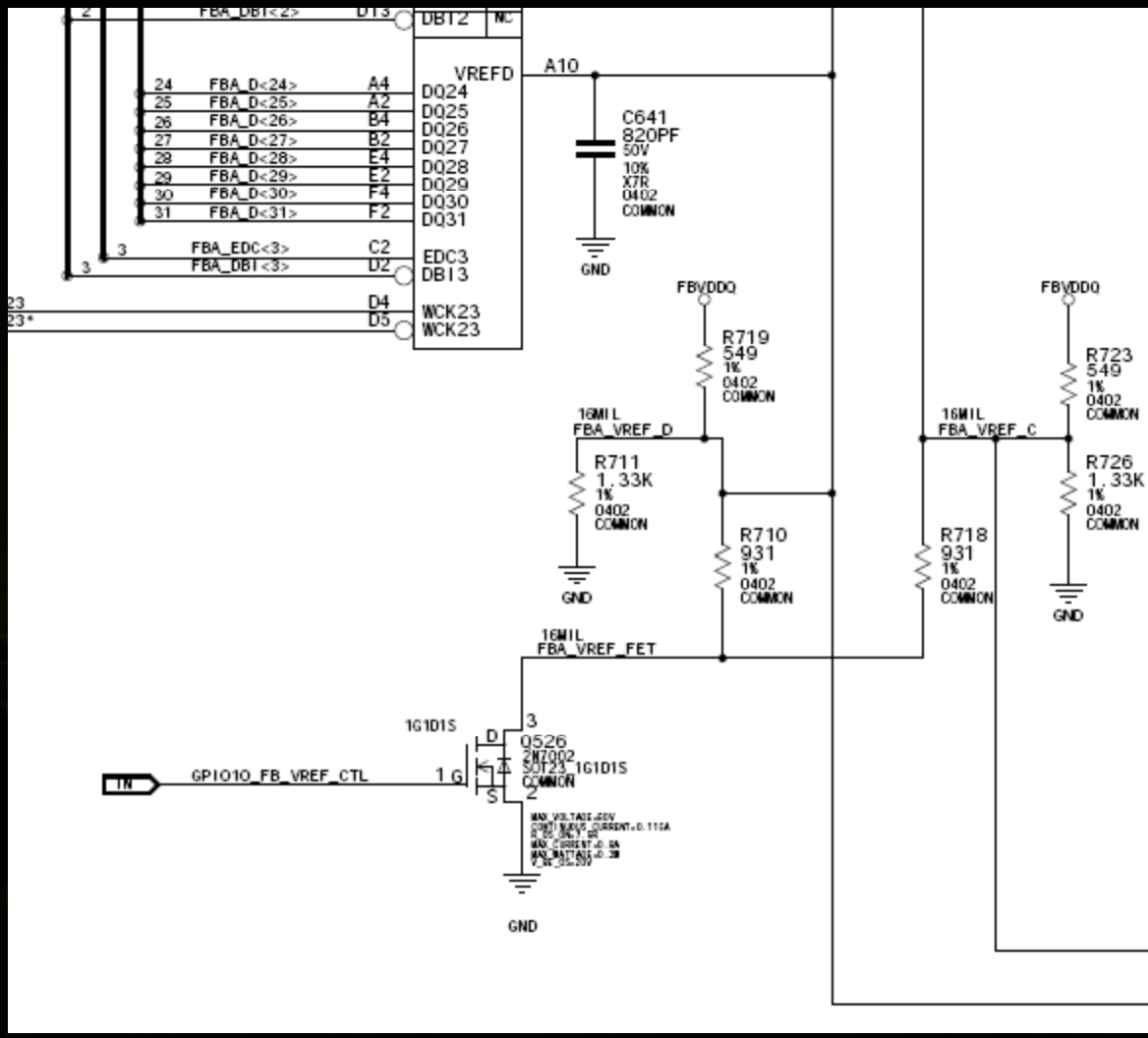


Memory Controller Interface

- To improve performance, Fermi GPUs divide the frame buffer interface into Channels, These channels are 32bits slices made up of 4 bytes, each channel can be implemented with a single 32bit wide DRAM component or with two 16bit wide parts.
  - Every channel can issue different commands
  - Every channel can read/write to independent addresses.
- Each channel contains a fully independent memory controller.
- All memories within a channel share the same command bus and the address bus.
- The different channels in a GPU are completely Asynchronous to each other
- Only BL8 is supported.
- Support both x32 and x16 GDDR5 and DDR3 DRAM modes of operation.

Memory Controller Interface

- Memory Voltage Reference
- Use GPIO10 for Vref Ctrl



Memory Controller Interface

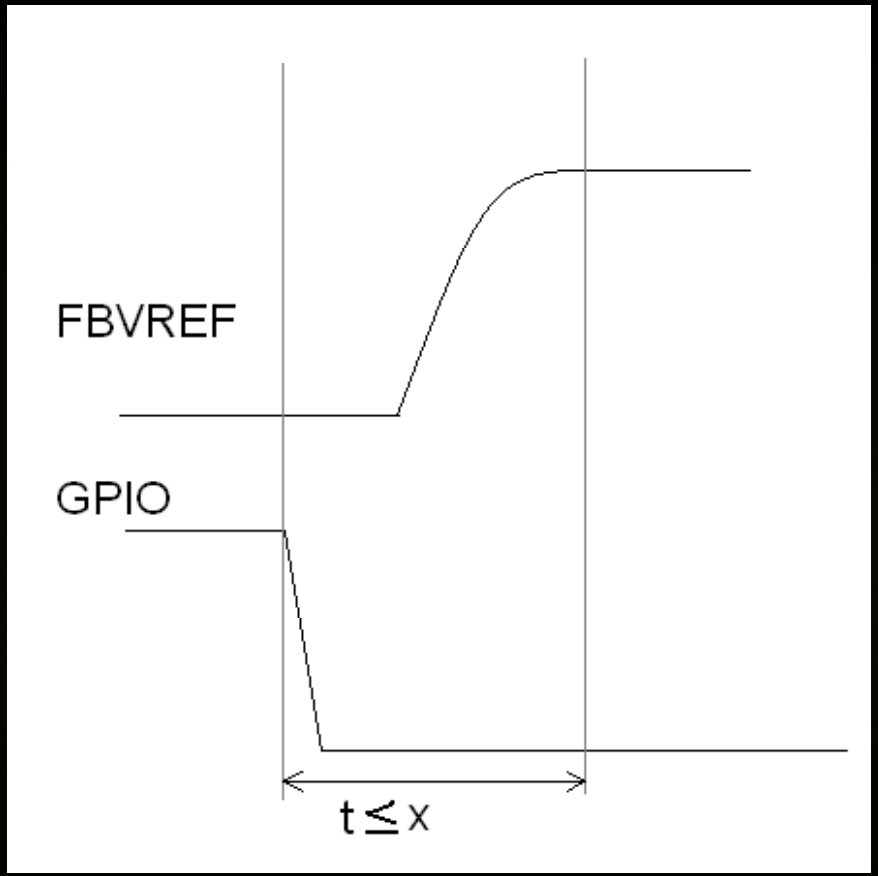
- Memory Voltage Reference (Vref)
  - Internal Vref is applied in Fermi GPUs so external Vref provision is not required, the Vref pin on GPU can be left unconnected.
  - GDDR5 memory components also have internal Vref for DQ and DBI signals, external Vref is recommended.
  - Memory Voltage Reference Switching

Voltage Name	Un-terminated	Terminated
FBVREF at RAM	50%	70%

Memory Controller Interface

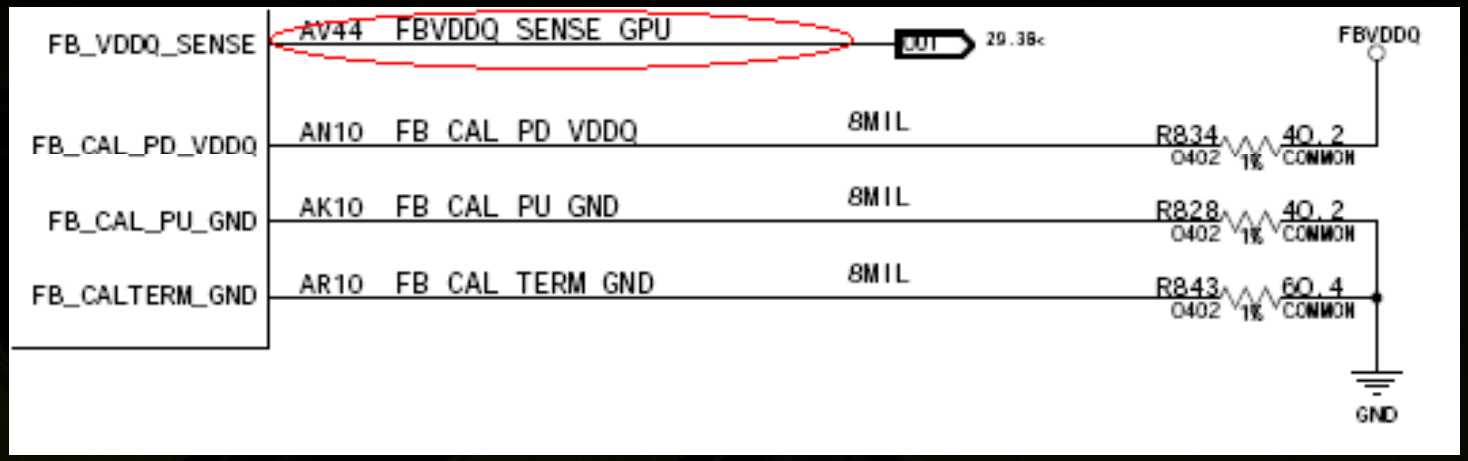
- **FBVREF Maximum Switching Time**

Rail	Maximum Switching Time
FBVREF	X=20uS



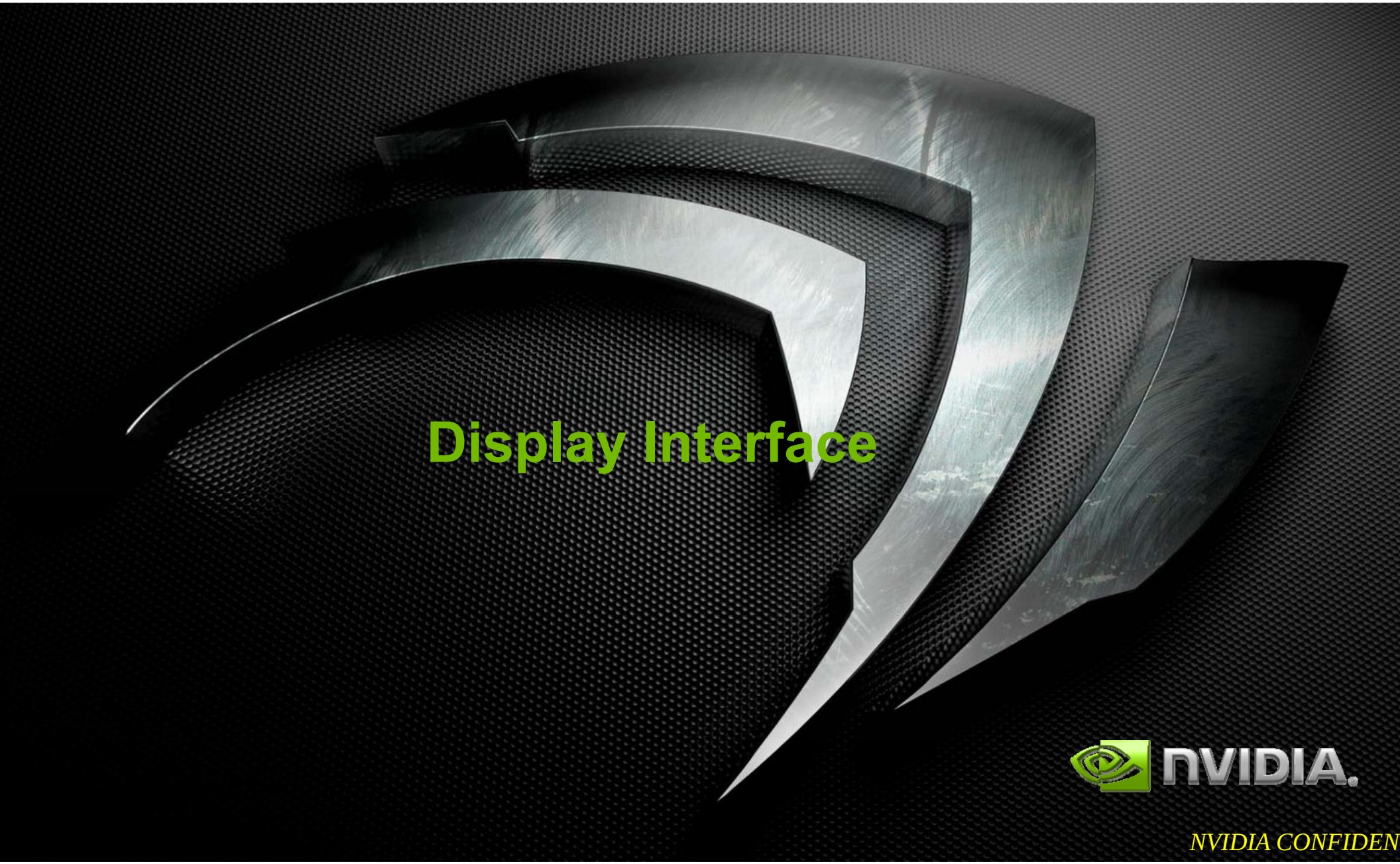
Memory Controller Interface

- **GPU Driver Calibration**



- **Default GPU Driver Calibration for Frame Buffer Interface**

Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω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Display Interface

- Digital Displays
  - DVI-I
  - HDMI
  - DisplayPort
- Analog Displays
  - DAC A
  - DAC B

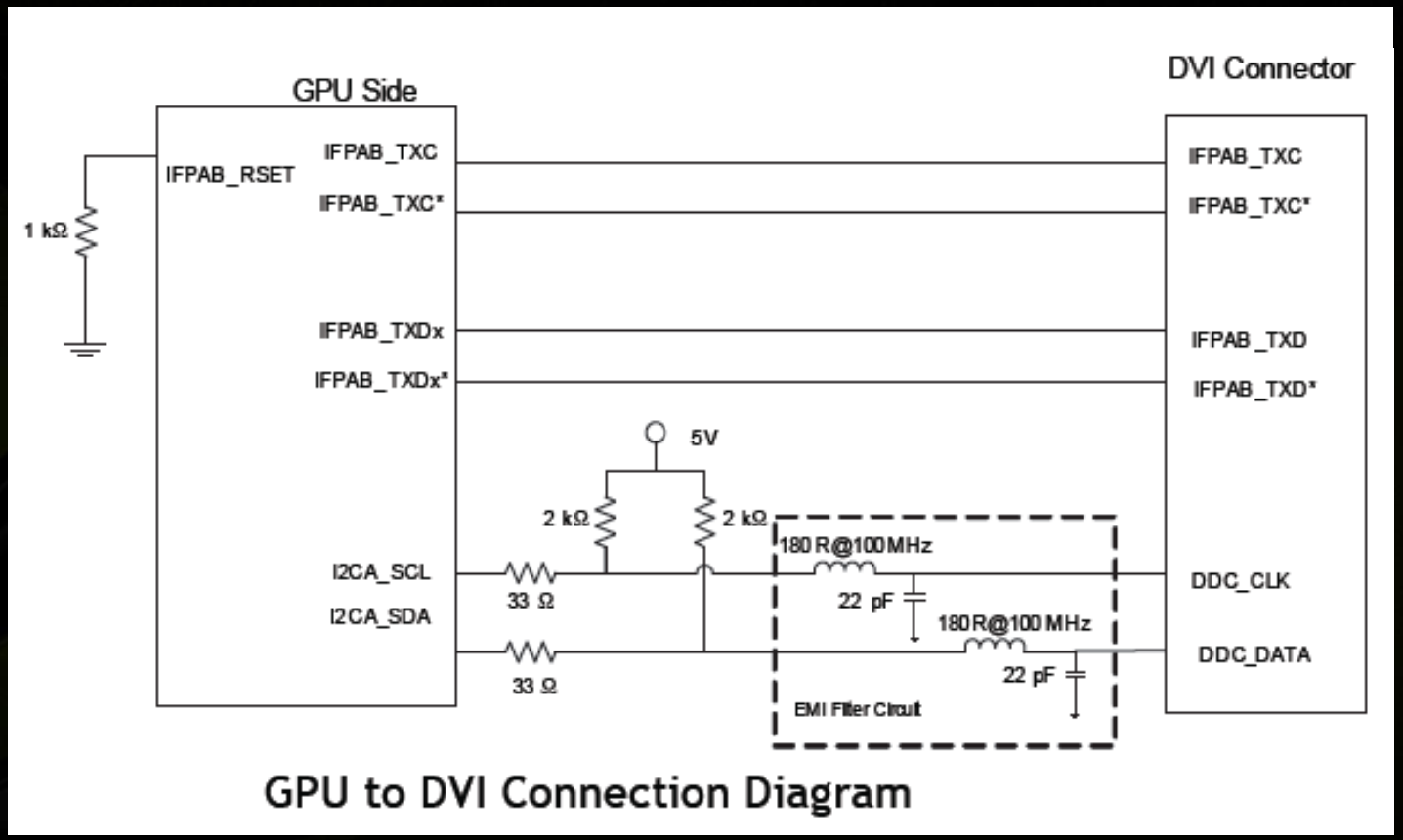
Display Interface

- **Digital Display**
  - **DVI is only supported on Links A,B,E and F, Dual-Links DVI is supported on links A/B and E/F.**
  - **For I2C/DDC lines, because the IFPx_AUX_I2Cx lines are not 5V tolerance, a Level Shifter must be used to support I2C.DDC.**
  - **For unused IFP Marco, pull-down IFPxyIOVDD and IFPxy_PLLVDD with a 10Kohm resistor, the other IO pins can be left not connected (NC).**

ital Display Link	IFPA(LinkA)	IFPB(LinkB)	IFPC(LinkC)	IFPD(LinkD)	IFPE(LinkE)	IFPF(LinkF)
DVI	√ (Dual Link with IFPB)	√ (Dual Link with IFPA)	x	x	√(Dual Link with IFPF)	√ (Dual Link with
HDMI	√	x	√	√	√	x
Mini-HDMI	√	x	√	√	√	x
Display Port	x	x	√	√	√	x
Mini-DP	x	x	√	√	√	x

Display Interface

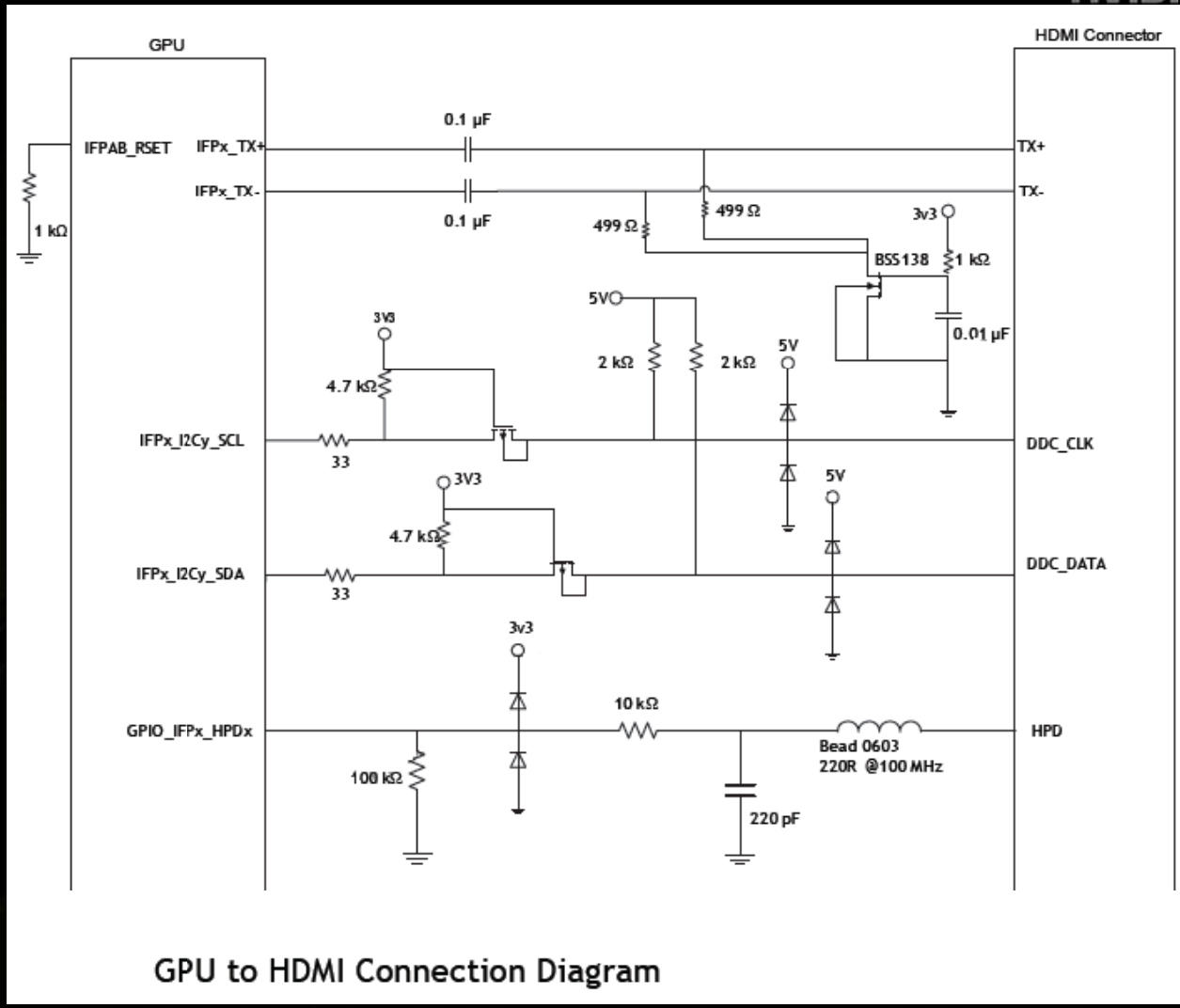
- DVI connection at IFPAB



GPU to DVI Connection Diagram

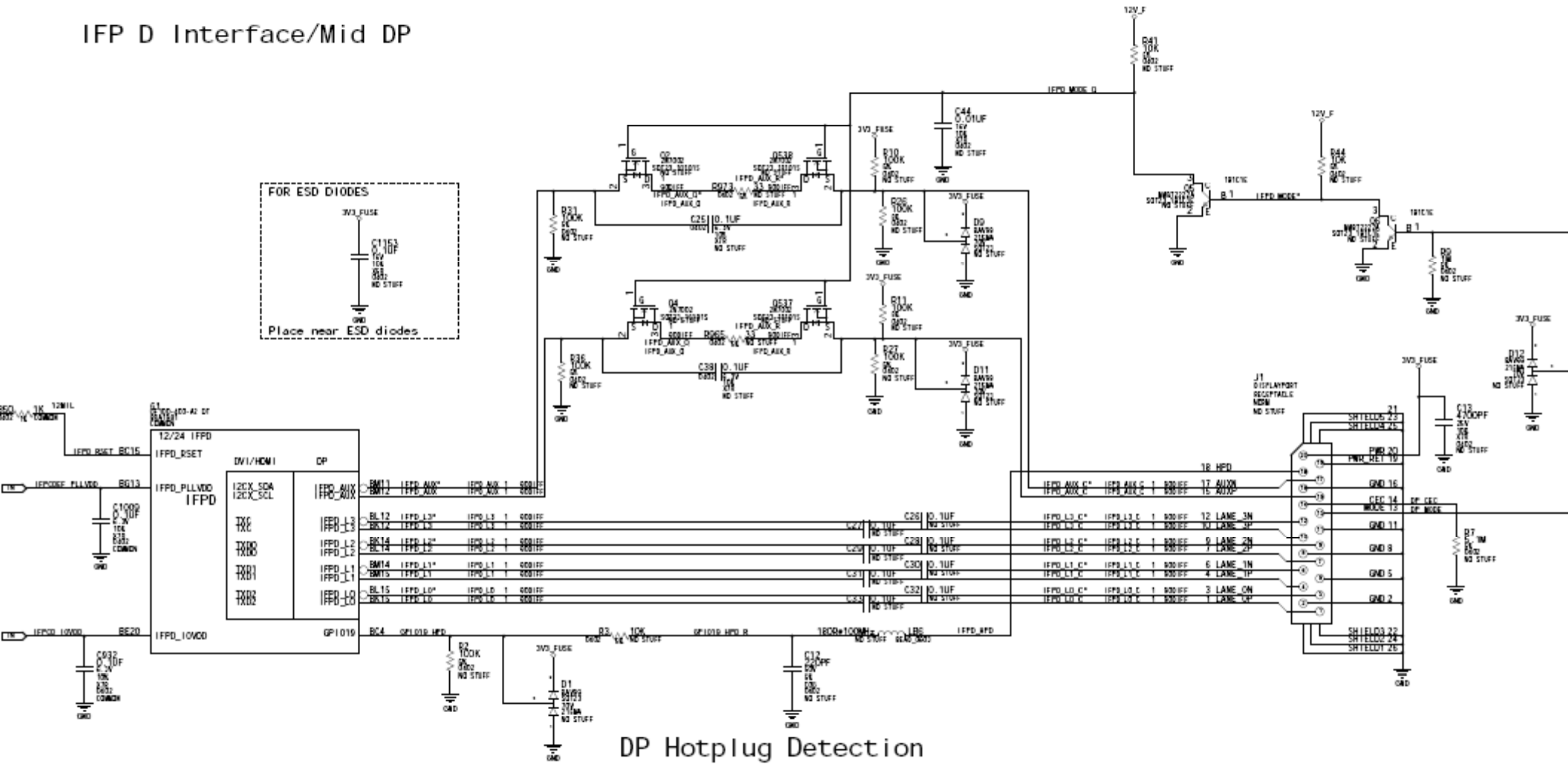
Display Interface

- HDMI at IFPx
- AC Coupling Caps
- 499 ohm PD
- I2C 3V3 to 5V LevelShift



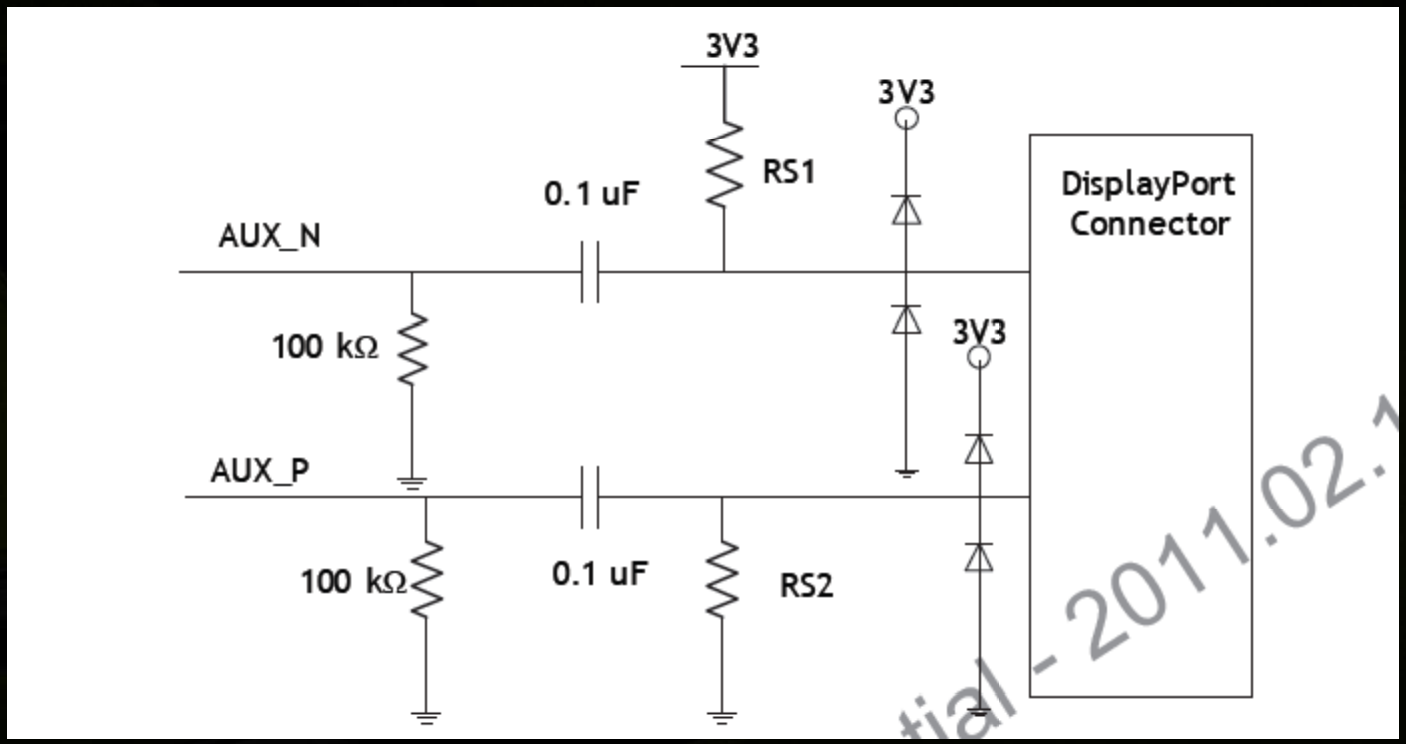
GPU to HDMI Connection Diagram

Display Interface - DisplayPort



Display Interface - DisplayPort

- AUX Link in native mode



Display Interface

- **Digital Display Interface Power Rails**
  - **TMDS Power Rails**

Power Rails	Voltage	Maximum Current Draw
IFPx_IOVDD	3.3V±5%	IFPA_IO: 300mA IFPB_IO: 200mA
IFPx_PLLVDD	1.05V±5%	200mA

  - **HDMI Power Rails**

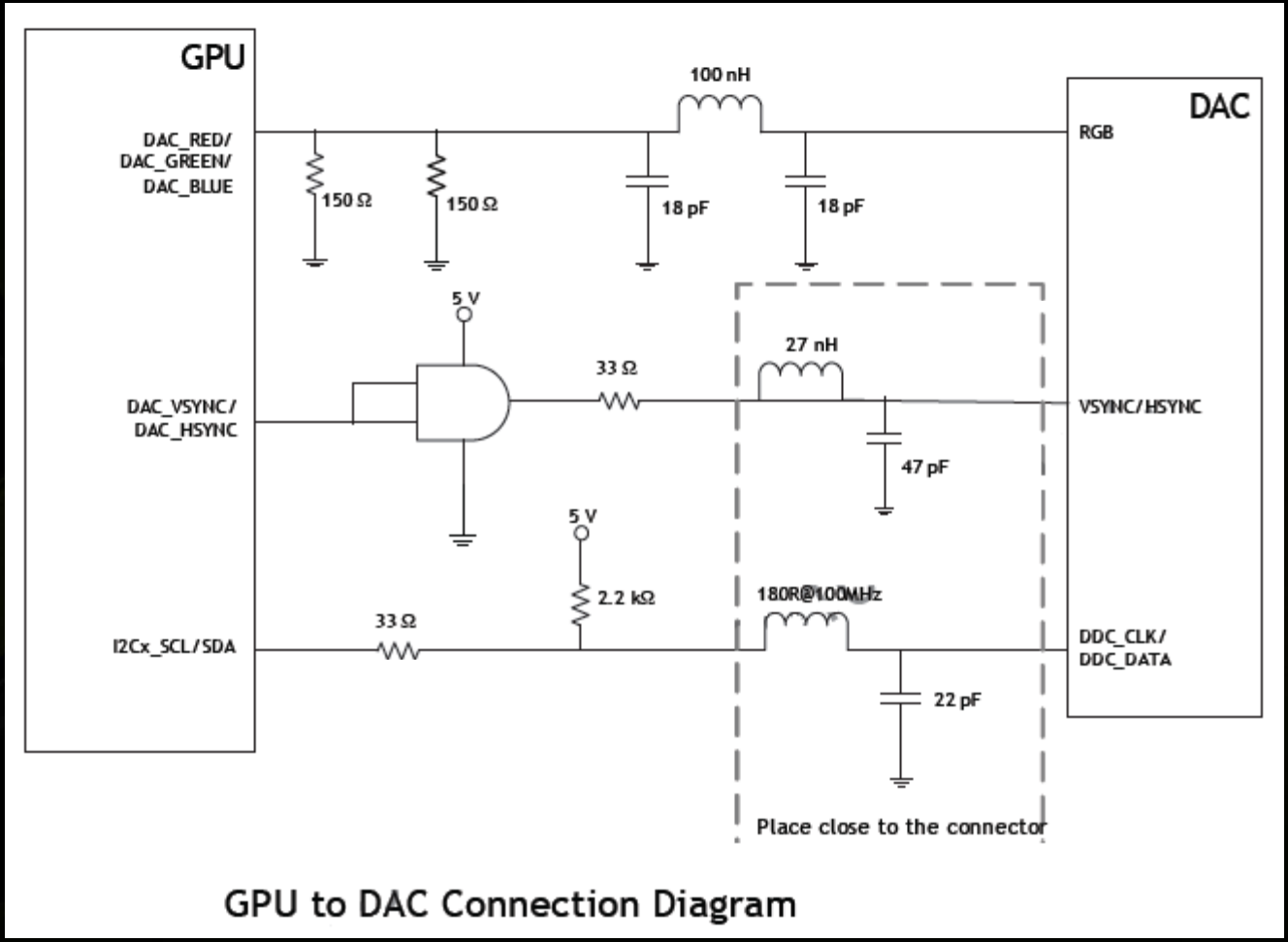
Power Rails	Voltage	Maximum Current Draw
IFPx_IOVDD	1.05V±5%	285mA
IFPy_PLLVDD	3.3V±5%	200mA

  - **Display Port Power Rails**

Power Rails	Voltage	Maximum Current Draw
IFPx_IOVDD	1.05V±5%	300mA
IFPy_PLLVDD	3.3V±5%	200mA

Display Interface

- Analog Displays



GPU to DAC Connection Diagram

Display Interface

- Analog Display
  - The D12x GPUs feature two RGB DACs that support legacy connectors. The two DACs are named DAC A and DAC B. There is no Macrovision support in this family GPUs.
  - DAC VREF requires 0.1uF decoupling capacitor.

DAC	Analog RGB	Microvision
DAC A	Supported	Not supported
DAC B	Supported	Not supported

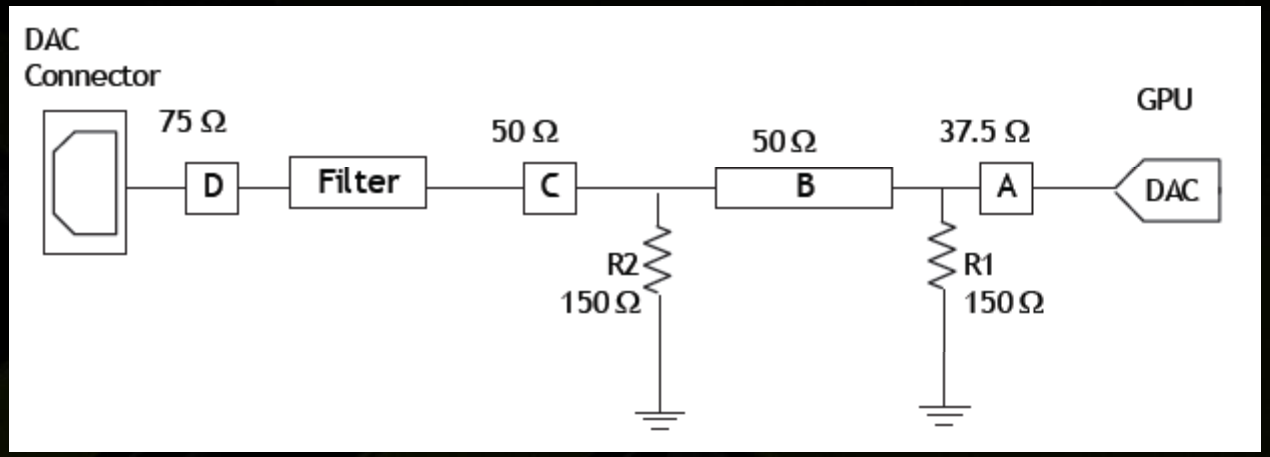
Display Interface

- Analog Display Interface Power Rails

Power Rails	Voltage	Maximum Current Draw
DACx_VDD	3.3V±5%	120mA

Display Interface

- VGA Signal Terminations



- **Use a 37.5 Ω ± 2% trace impedance between the GPU and the first 150 Ω resistor (R1) if the trace length is not short. The trace length should not exceed 600 mil. Next, use a 50Ω ± 2% trace impedance between the resistor R1 and the resistor R2. The trace length should not exceed 6000 mil.**
- **Place the filter after the second termination resistor, R2. The trace length should not exceed120 mil and have an impedance of 50 Ω.**
- **The trace length (75 Ω trace) between the filter and the connector should not exceed 600 mil.**

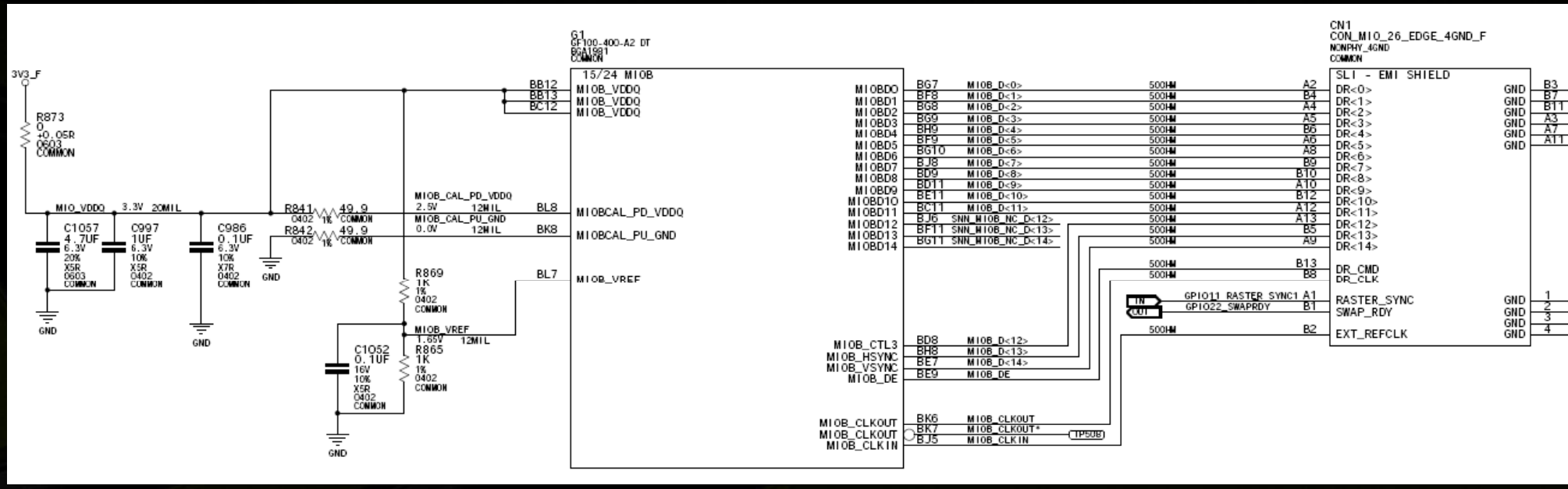
Display Interface

- Analog Display
  - If the DAC interface is not required, it should be disabled by:
    - Adding a pull-down to the DACx_VDD with a 10 kΩ resistor to GND.
    - Unused DDC clock and data signals should be connected to a 5 V pull-up.
    - All other I/O pins (including DACx_VREF and DACx_RSET) can be left unconnected (NC)

MULTI-USE I/O (MIO) AND SLI

MULTI-USE I/O (MIO) AND SLI

- MIO(SLI)



- MIOA/B Calibration Resistors

	MIOx_CAL_PD_VDDQ	MIOx_CAL_PU_GND
Calibration Resistor	50 ohm 1% 0402 tied to MIOx_VDDQ	50 ohm 1% 0402 tied to GND

MULTI-USE I/O (MIO) AND SLI

- Interface Power Rails.

Power Rails	Voltage	MaximumCurrent Draw
VDD33	3.3V±5%	120mA/non-SLI, 285mA/SLI

- Unconnected Signals(NC)
  - For unused MIOS interfaces, MIOx_VDDQ must be powered with 3.3V for compatible designs (For GF104, must connect to 3V3 even it's no use) or pulled down to GND.
  - For each unused MIO interface that is powered by 3.3V, provide one 0.1uF capacitor. For MIO interfaces that have MIOx_VDDQ that are pulled down to GND that capacitor is not needed.
  - MIOxCLKIN signals should have 10Kohm pull-down resistors.

I2C

I2C Specification

Parameter	Specificatioin	Notes
Overview	A two-write(SCL and SDA) I/O BUS for miscellaneous chip to chip communication	
Operating Frequency	Standard Mode: Up to 100KHz Fast Mode: 400KHz	
Topology	Single-ended Bi-directional	
Termination	2.2Kohm pull-up resistor on I2C CLK and DATA	
Max Capacitive Load for BUS Line(CL)	Standard mode: 400pF Fast Mode: 100pF	

I2C

I2C Availability

BUS ID	Signal Name	Type	Application	Associated Display Link	Voltage Tolerance
A	I2CA_SDA I2CA_SCL	Bus Master	DDC	DAC A-CRT	5V
B	I2CB_SDA I2CB_SCL	Bus Master	DDC	DAC B-CRT	5V
C	I2CC_SDA I2CC_SCL	Bus Master	DDC and External Devices	IFPA, IFPB-LVDS	5V
S	I2CS_SDA I2CS_SCL	Slave	Internal Thermal Sensor		5V
W	IFPC_AUX_I2CW_SDA_N, IFPC_AUX_I2CW_SCL	Bus Master	AUX/DDC	IFPC	3.3V
X	IFPC_AUX_I2CX_SDA_N, IFPC_AUX_I2CX_SCL	Bus Master	AUX/DDC	IFPD	3.3V
Y	IFPC_AUX_I2CY_SDA_N, IFPC_AUX_I2CY_SCL	Bus Master	AUX/DDC	IFPE	3.3V
Z	IFPC_AUX_I2CZ_SDA_N, IFPC_AUX_I2CZ_SCL	Bus Master	AUX/DDC	IFPF	3.3V

I2C

- Please don’t connect SMBus to I2C unless the PU in SMBus is not from standby power.
- Unconnected Signals (NC)
  - For unused dedicated (Non-AUX) I2C pins, pull up both the I2Cx_SCL, I2CxSDA to 3.3V using 2.2Kohm resistors.

GENERAL PURPOSE I/O (GPIO)

GENERAL PURPOSE I/O (GPIO)

- The D12x family of GPUs uses up to 25 General Purpose I/O (GPIO) pins to control and monitor GPU status. Some of these pins are available to partners for custom functions, while some built-in functions are accessible through the NVAPI software interface.

GENERAL PURPOSE I/O (GPIO)

Pin description

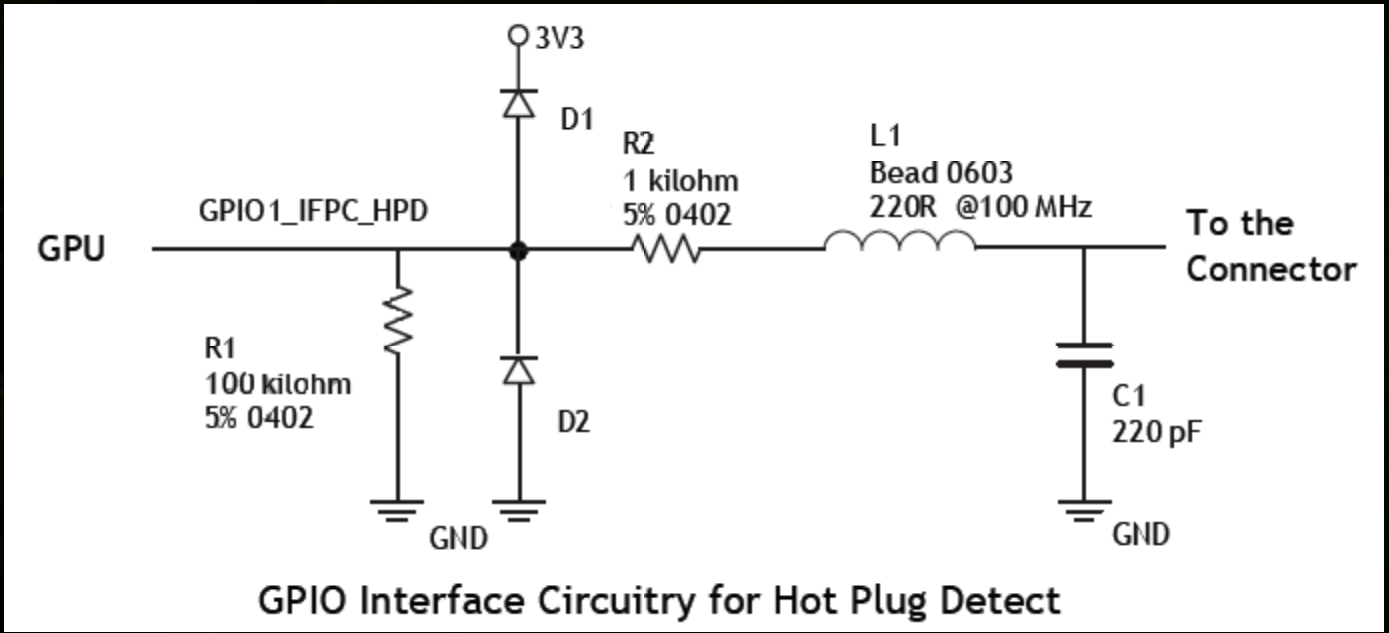
GPIOx Pin	Function	I/O Type	Description
GPIO[0]	HPD-AB	Input	Hot-Plug Detect for Link A/B
GPIO[1]	HPD-C	Input	Hot-Plug Detect for Link C
GPIO[2]	GPU_VID[2]	Output	GPU Voltage Control
GPIO[3]	RASTER_SYNC_A	Input/Output	SLI Control
GPIO[4]	FAN_TACH	Input	Fan Tachometer
GPIO[5]	GPU_VID[3]	Output	GPU Voltage Control
GPIO[6]	GPU_VID[4]	Output	GPU Voltage Control
GPIO[7]	GPU_VID[5]	Output	GPU Voltage Control
GPIO[8]	THERM_OVERT	Input	Thermal Shutdown
GPIO[9]	THERM_ALERT	Input	Thermal Slowdown
GPIO[10]	MEM_VREF	Output	Memory VREF Control Switch
GPIO[11]	RASTER_SYNC _B	Input/Output	SLI Control
GPIO[12]	NVVDD_PSI	Output	NVVDD Phase Shed Control
GPIO[13]	NVRESERVED_0	Input/Output	Reserved for NVIDIA Use
GPIO[14]	NVRESERVED_1	Input/Output	Reserved for NVIDIA Use
GPIO[15]	HPD-E	Input	Hot-Plug Detect for Link E
GPIO[16]	FAN_PWM	Output	Programmable Fan Control
GPIO[17]	GPU_VID[1]	Output	GPU Voltage Control
GPIO[18]	GENERAL_PURPOSE_0	Input/Output	Reserved for Customer Use
GPIO[19]	HPD-D	Input	Hot-Plug Detect for Link D
GPIO[20]	GENERAL_PURPOSE_1	Input/Output	Reserved for Customer Use
GPIO[21]	HPD-F	Input	Hot-Plug Detect for Link F
GPIO[22]	SWAP_READY	Input/Output	SLI Control
GPIO[23]	MEM_VDD_CTL	Output	Memory Voltage Switch
GPIO[24]	FAN_SELECT	Output	Fan Control Source Select

GENERAL PURPOSE I/O (GPIO)

- Unconnected Signals (NC)
  - Unused GPIOs may be left as NC or floating on the board design.

GENERAL PURPOSE I/O (GPIO)

- Electrical Guideline -HPD



GPIO Interface Circuitry for Hot Plug Detect

Straps

Straps

- Fermi GPUs support two different strapping modes: Mult-Level Strapping Mode & Binary Production Strapping Mode.
- Strap Mode Selection

Mode	Multi_Strap_Ref1_GND	Multi_Strap_Ref0_GND	Strapping Resistor Value for other strap pins
Binary Production	40.2K 1% to GND	NC	10K 5%
Multi-Level	40.2K 1% to GND	40.2K 1% to GND	See Multi-Level Straps

Straps

Multi-Level Straps

Physical Strapping Pin	Power Rail	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	VDD33	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVCID[1]	PCI_DEVCID[0]
STRAP1	VDD33	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-uip to VDD	Pull-down to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Straps

Binary Mode Straps

Physical Strapping Pin	Power Rail	Name
ROM_SO	VDD33	PCI_DEVID_EXT
ROM_SCLK	VDD33	XCLK_417
ROM_SI	VDD33	PCI_DEVID[3]
STRAP2	VDD33	RAMCFG[2]
STRAP1	VDD33	RAMCFG[1]
STRAP0	VDD33	RAMCFG[0]

Straps

- Sub_Vendor, 0 : no VBIOS, 1 : VBIOS rom is present (default)
- RAMCFG, memory strapping table
- XCLK_417, Internal PCI-E Clock, 0 : 277MHz (default)
- FB_0_BAR_Size, SysFB aperture size used by GPU, 0 : 256MB (default)
- PCI_DEVID, determine DID bit [4:0]
- User Straps, It's use for panel selection
- 3GIO_PADCFG, determine the PCI-E signal swing, 0 : default (high swing)
- PEX_PLL_EN_Term, used to set PCI-E PLL Term, 1 : Enable, 0 : Disable (default)
- SLOT_CLK_CFG, 1 : GPU & MCH share a common PCI-E reference clock.
- SMBus_ALT_Addr, 0 : 0x9E (default), 1 : 0x9C (Multi-GPU)
- VGA_Device, 0 : 3D device , 1 : VGA device (default)

Power

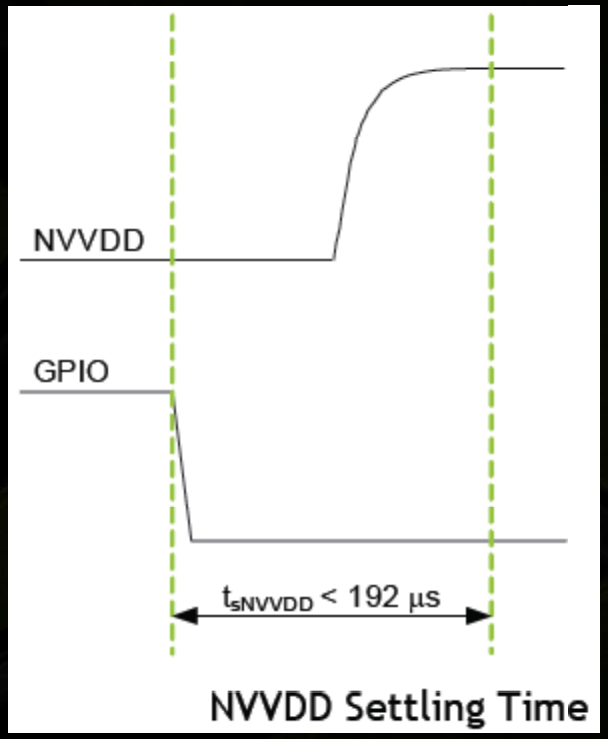
Power

- MVS (Multi-Voltage Set Point)
- Must be compatible with VRM11.
- NVVDD Voltage Switching Requirement

Constraint Parameter	Requirement	Notes
Voltage ramp time	< 192 us	Applies to any voltage switching; measured from controlling GPIO assertion to when the power supply is stabilized at the desired voltage level.
Positive/Negative overshoot	< 30 mV	This is measured from the target nominal voltage level up or down. Target voltage is the resulting NVVDD voltage after the switch.
Positive/Negative overshoot	< 30 mV	This is measured from the target nominal voltage level up or down. Target voltage is the resulting NVVDD voltage after the switch.

Power

- **NVVDD Settling Time**



NVVDD Settling Time

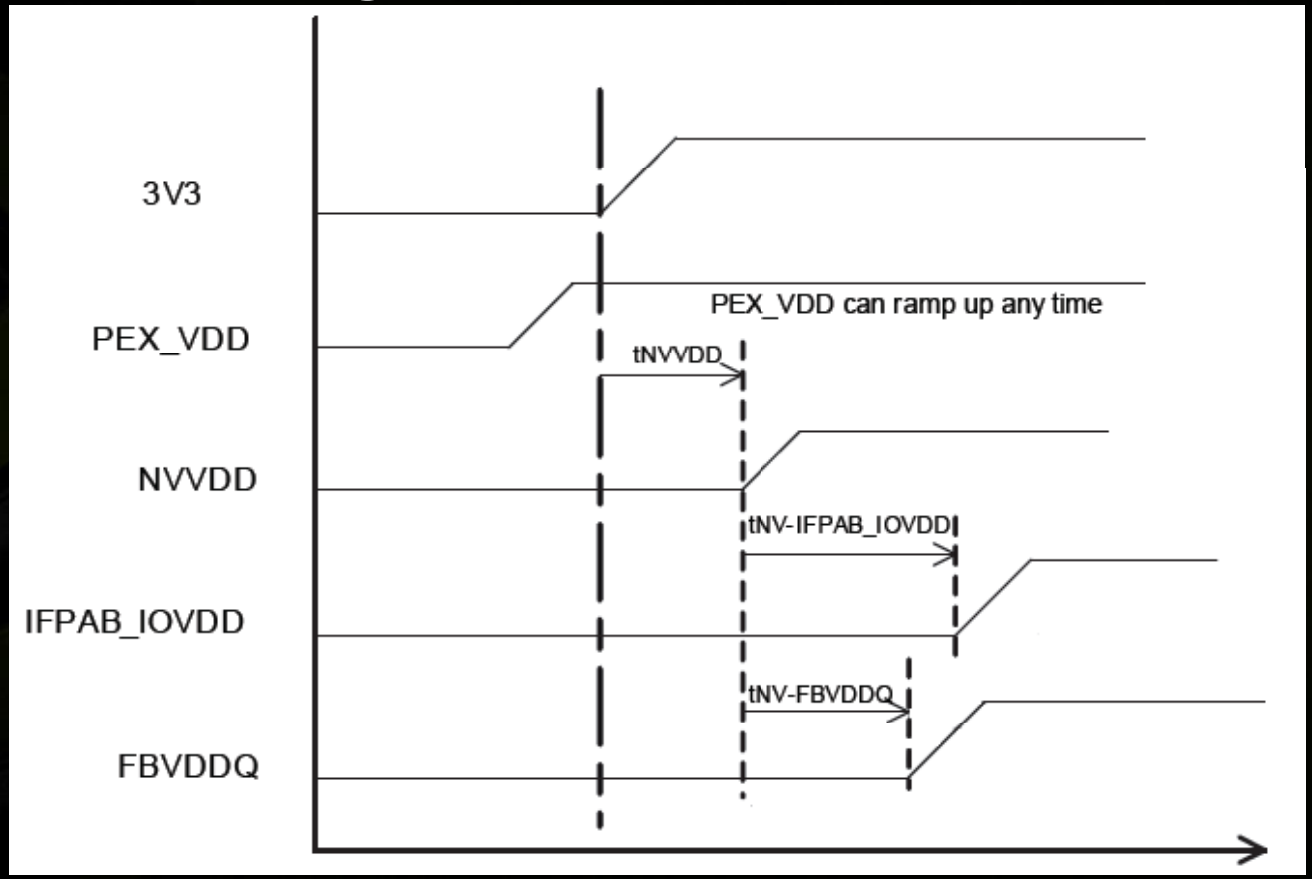
Power

- Power Sequencing
  - Power Up/Down States

    This section discusses power sequencing considerations. The following power sequencing rules must be satisfied at all times:
    - Cold boot
    - Resuming from a suspend state
    - Entering a suspend state
    - Power off

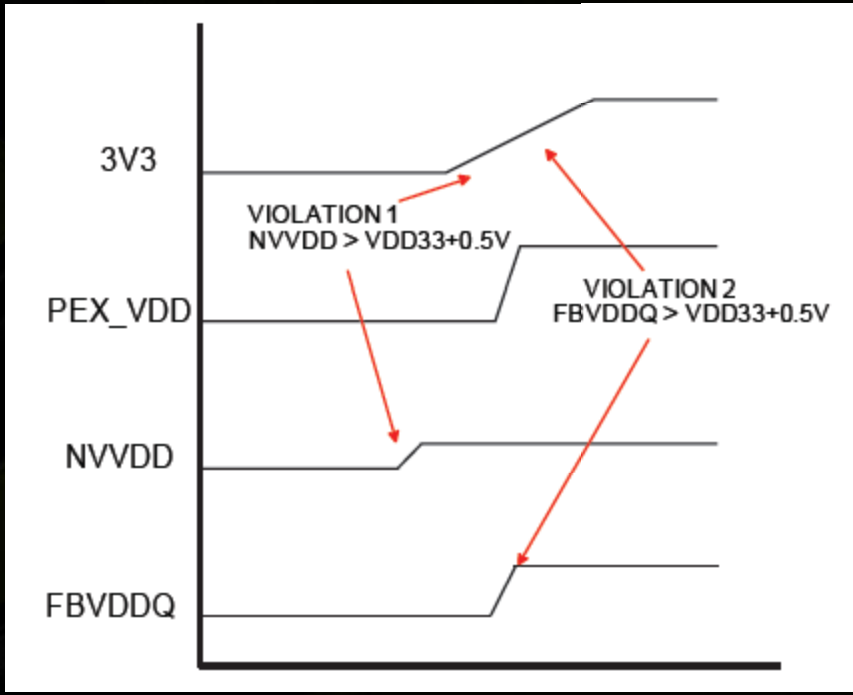
Power

- **Power Sequencing Recommendations**



Power

- Power sequencing Violation



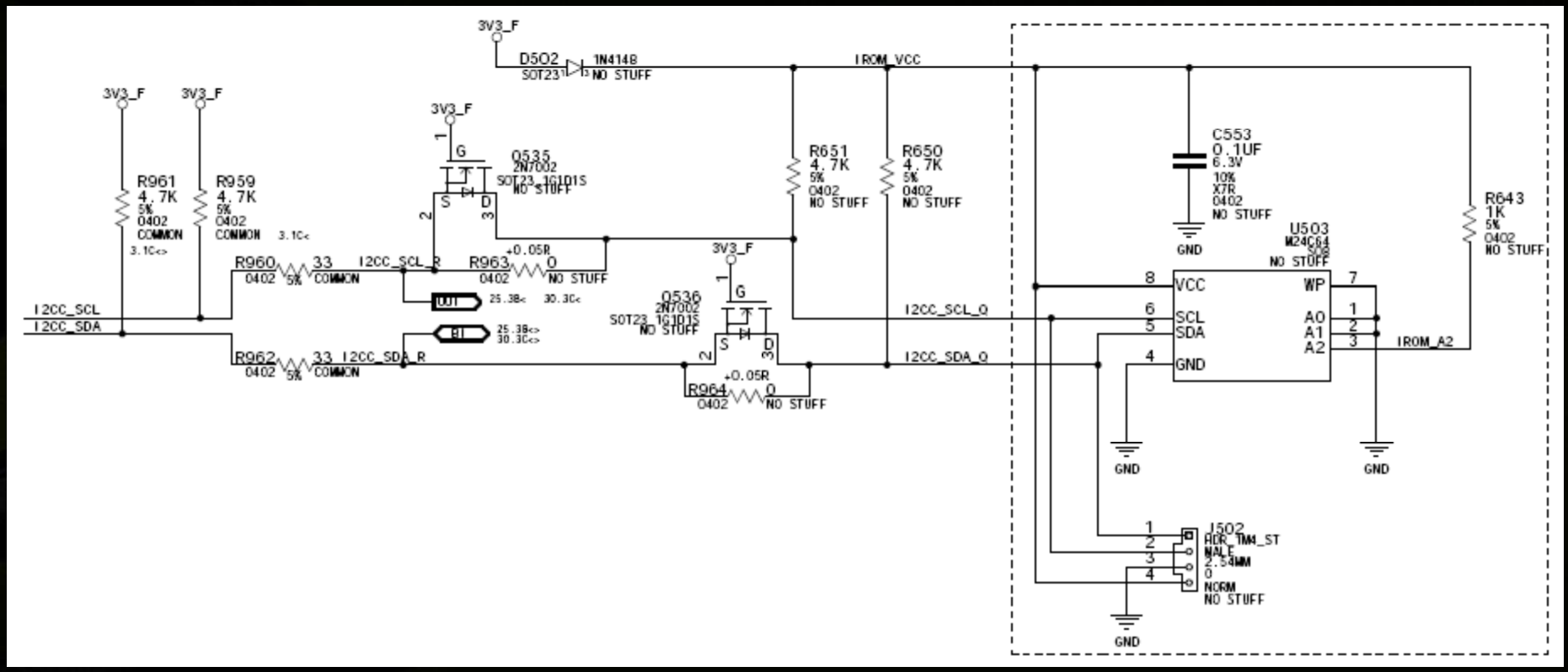
Power

- Note
  - 3V3 includes all rails that uses 3.3V (DACVDD, IFPVDD, MIO, etc…)
  - PEXVDD includes all rails that share it (PLLs, etc.)
  - FBVDD and FBVDDQ can be combined
  - From IOSI perspective, the GPU has no sequencing requirements. So these are only recommendations for notebook GPU designs. Although deviations from this should be documented and approved.
  - NVVDD -> FBVDD/Q: was historically required due to an issue with IO glitch during startup that caused some memories to go into TestMode. But should be Optional today
  - PEXVDD: There are concerns from GT21x that PEXVDD must follow NVVDD due to issue with state machine init in the PEX block on GT21x. It's unknown if GF1xx will have this issue.
  - IFP_IOVDD follows NVVDD for IFPABIOVDD only in the cases of LVDS, we have seen in notebook designs that IFPABIOVDD would glitch of it ramped before NVVDD, to avoid this glitch we thus have to ramp IFPABIOVDD after NVVDD.

Others

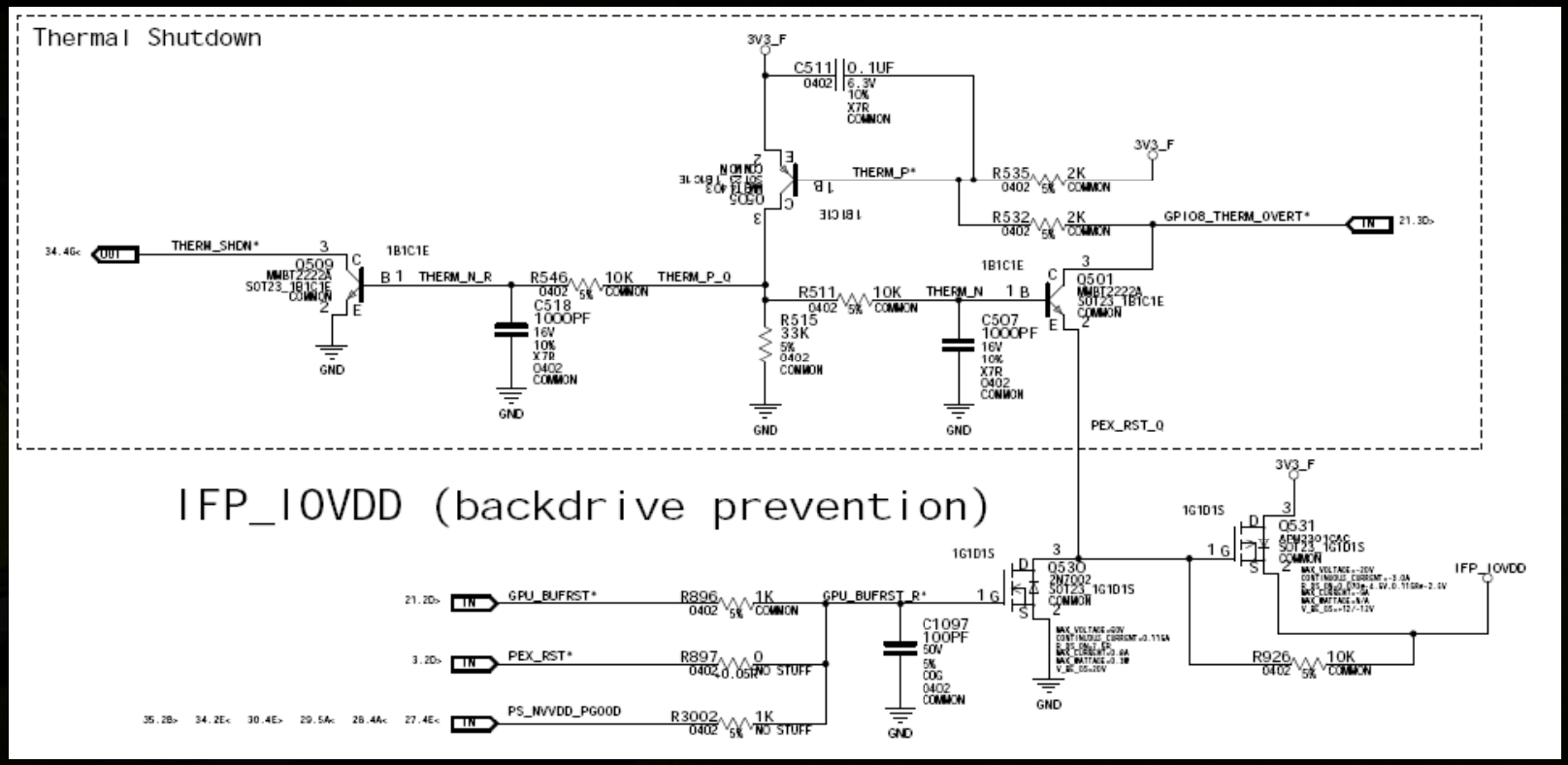
Others

- INFO ROM (Can be removed at CDP project)



Others

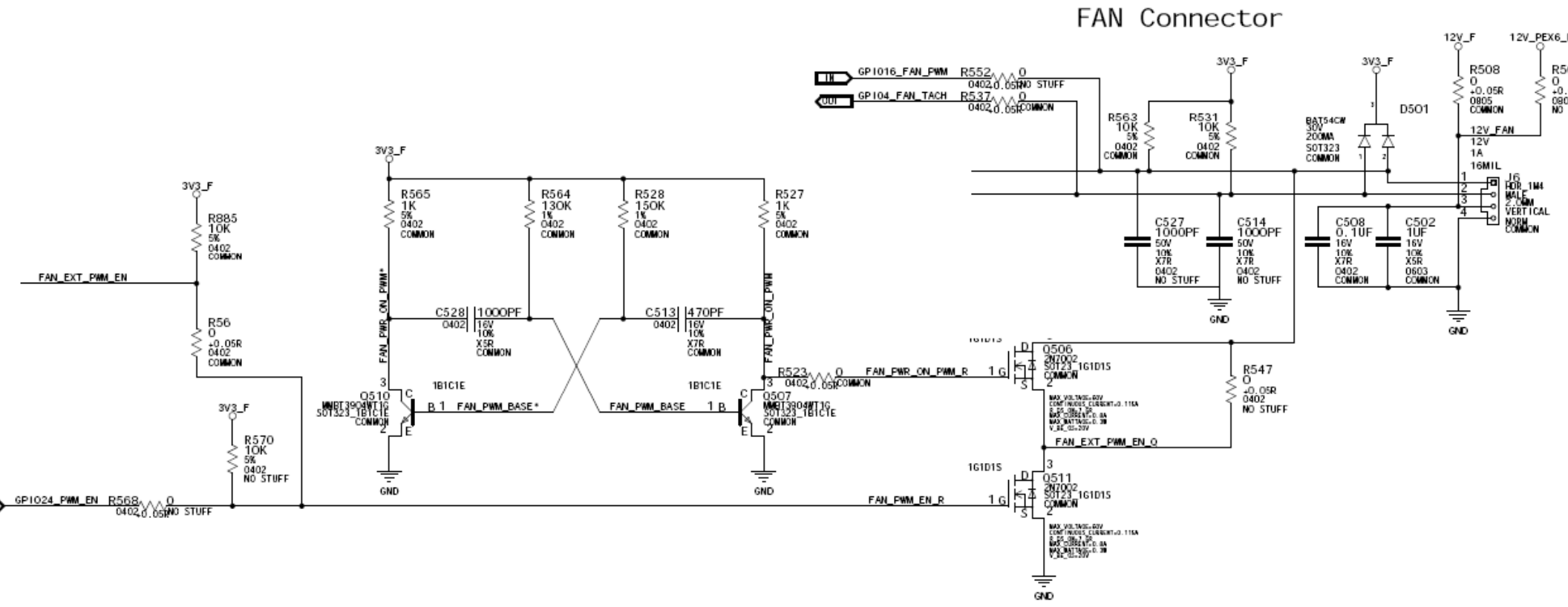
- **Thermal Shutdown and Backdrive Prevention**



- **Reserving a weak pull-down 100Kohm for (GPU_BUFRST*) is recommended.**

Others

- Fan Control –False safe mechanism




Thanks & Question
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