**amd**
**am4**

| | |
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| 17 Promontory-CLK/ACPI/GPIO | 53 Prom- SY8288RAC / 1.05V |
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Title: COVER SHEET

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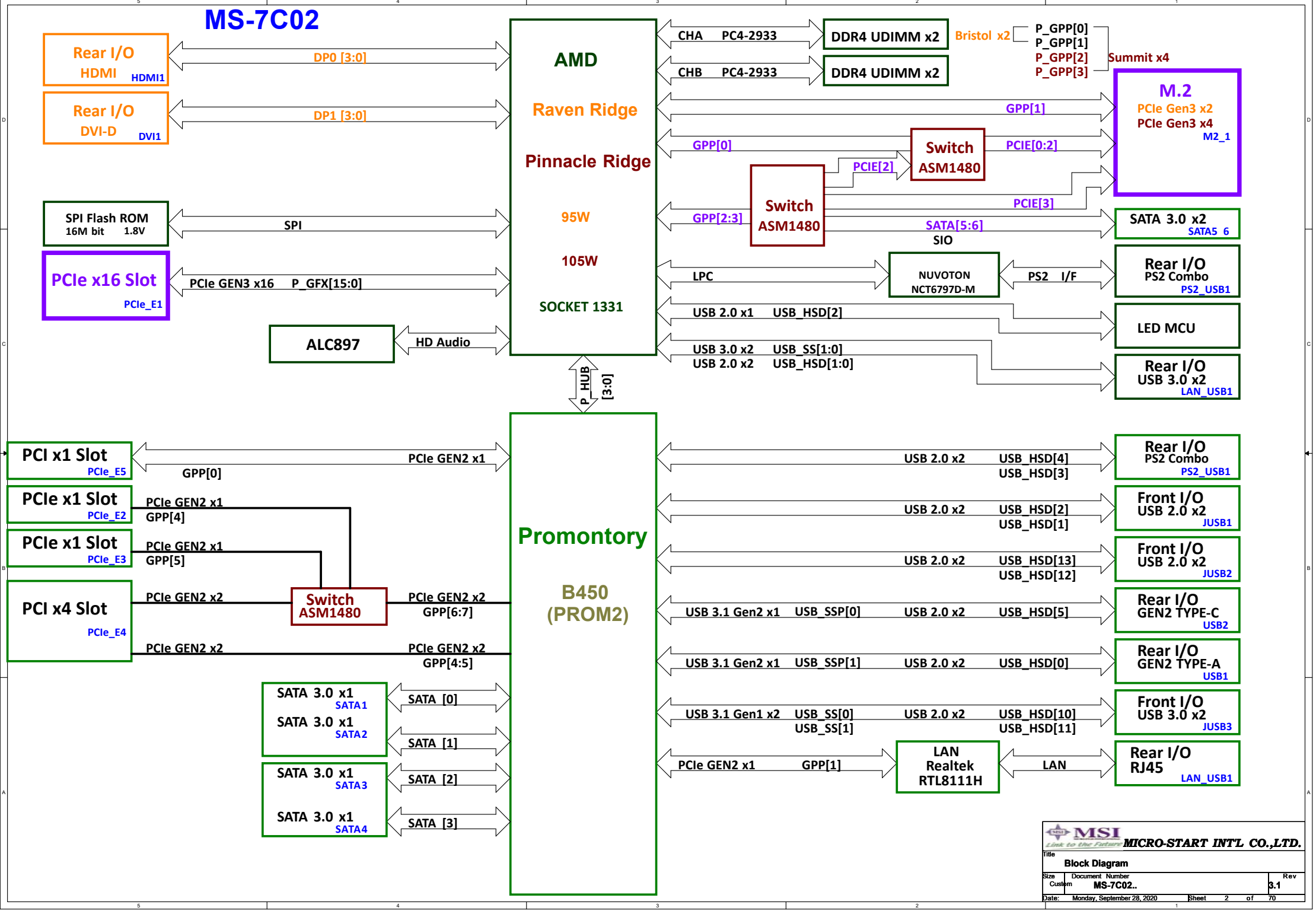
# MS-7C02

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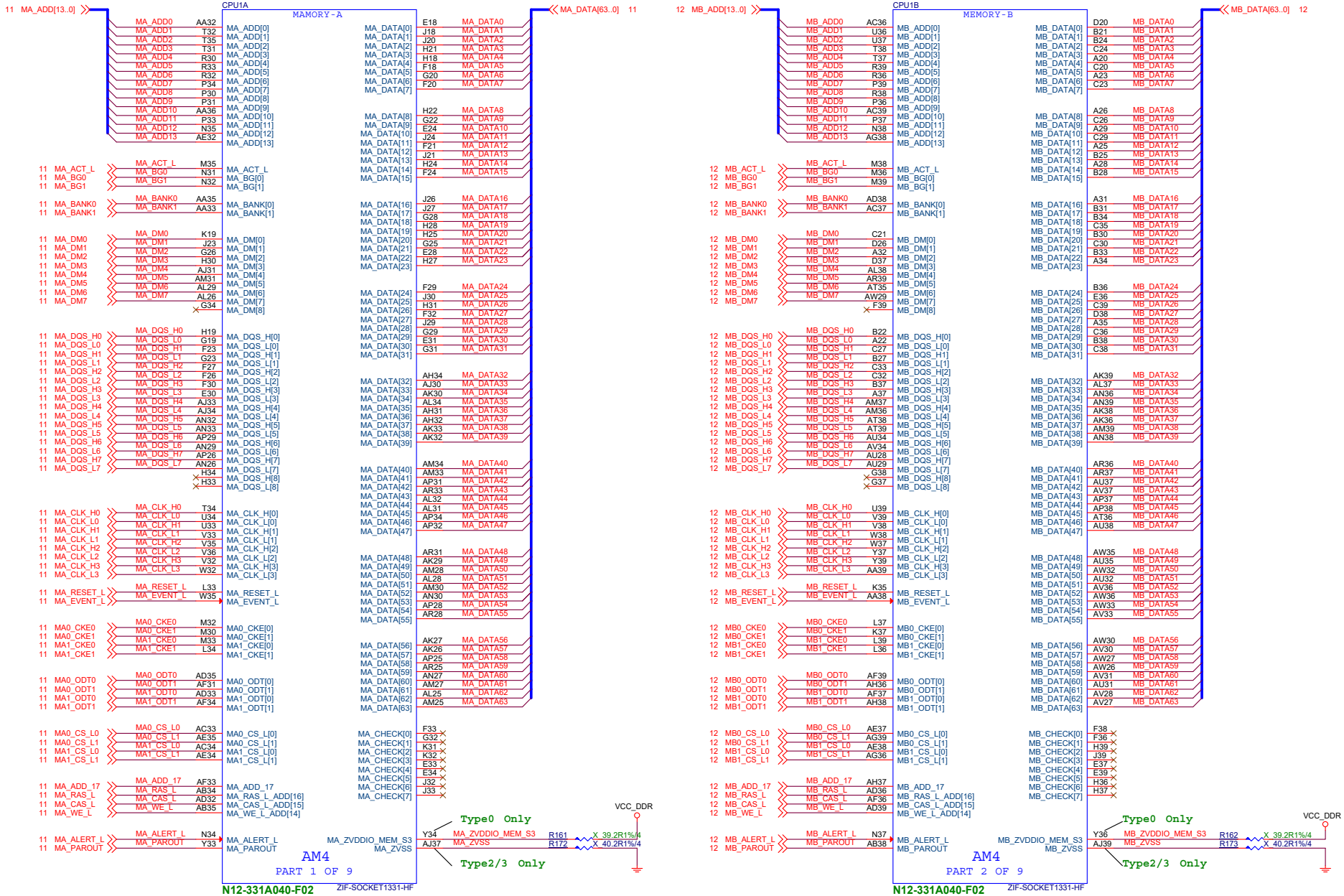
| | | |
|---|---|---|
| Title: Block Diagram | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 2 of 70 | |




| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |

MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F

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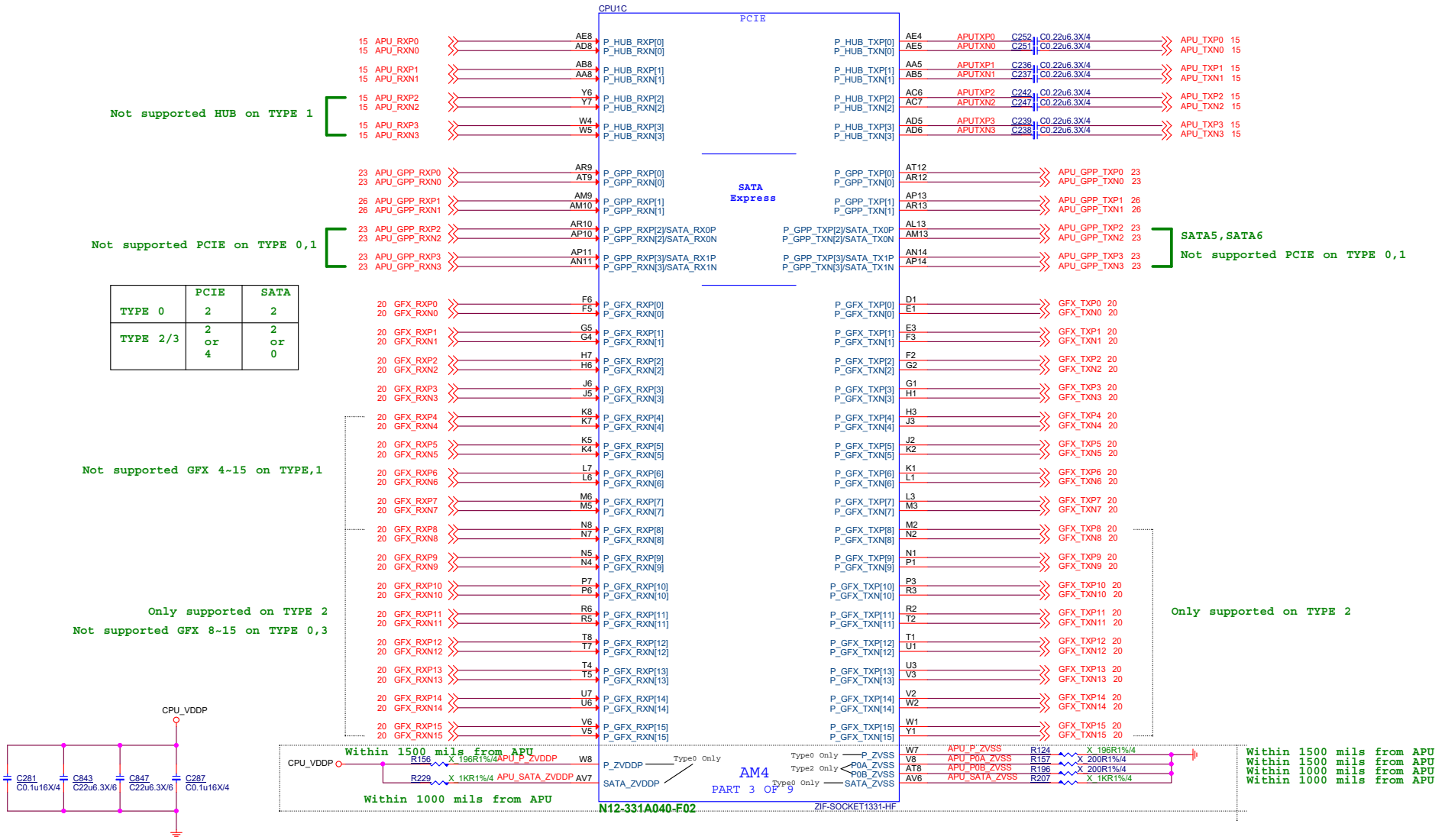


| | PCIE | SATA |
|---|---|---|
| TYPE 0 | 2 | 2 |
| TYPE 2/3 | 2 or 4 | 2 or 0 |

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |

MICRO-STAR INT'L CO.,LTD.

Title: AM4 PCIE/SATAE

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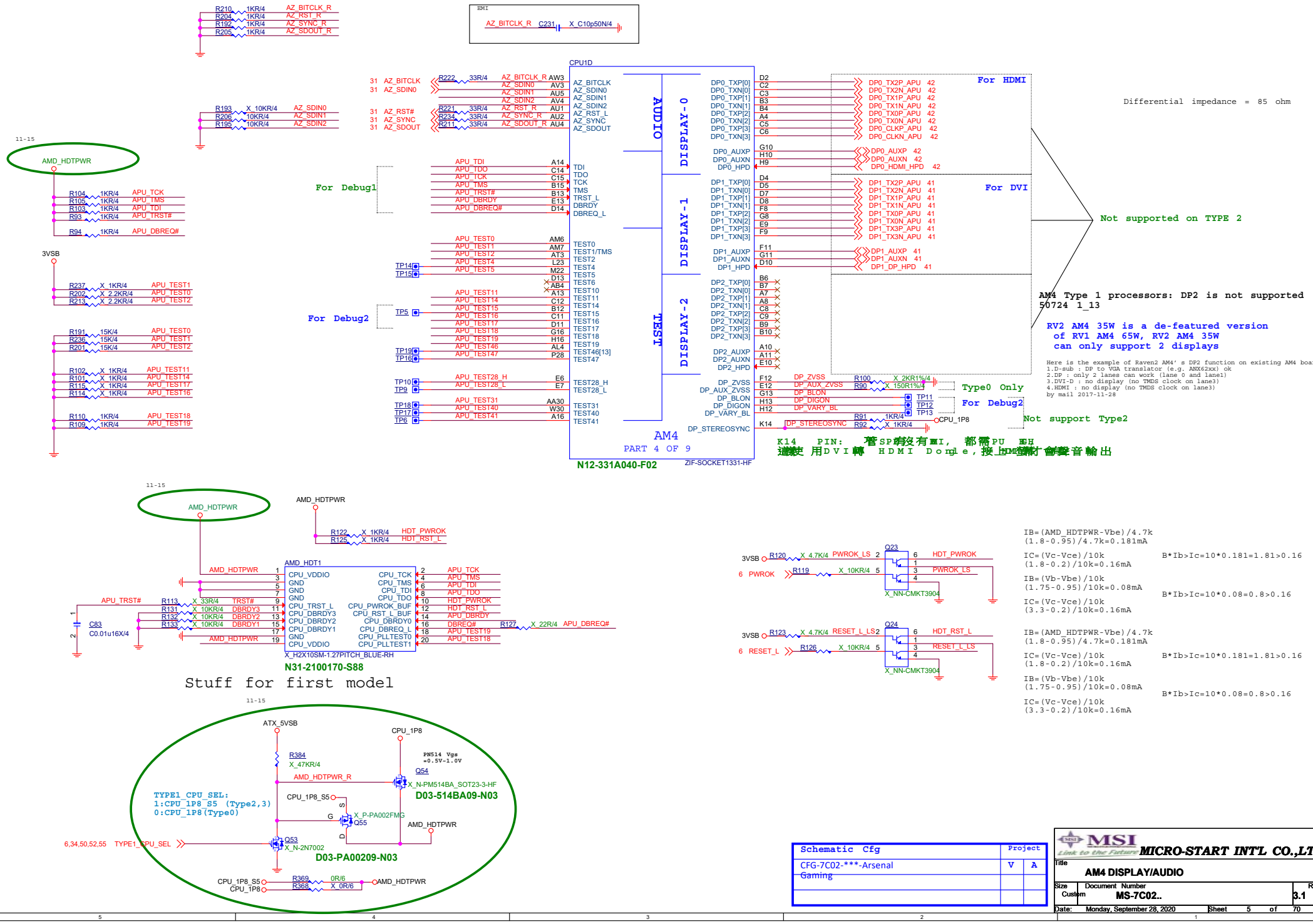
AM4 DISPLAY/AUDIO
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
AM4
PART 4 OF 9
N12-331A040-F02
ZIF-SOCKET1331-HF
For HDMI
For DVI
For Debug1
For Debug2
Type0 Only
Not supported on TYPE 2
Not support Type2
Differential impedance = 85 ohm
AM4 Type 1 processors: DP2 is not supported
50724 1_13
RV2 AM4 35W is a de-featured version
of RV1 AM4 65W, RV2 AM4 35W
can only support 2 displays
Here is the example of Raven2 AM4' s DP2 function on existing AM4 board :
1.D-sub : DP to VGA translator (e.g. ANX62xx) ok
2.DP : only 2 lanes can work (lane 0 and lane1)
3.DVI-D : no display (no TMDS clock on lane3)
4.HDMI : no display (no TMDS clock on lane3)
by mail 2017-11-28
K14 PIN: 若SPEC沒有HDMI, 都需PU 3K
建議使用DVI轉HDMI Dongle, 接上HDMI螢幕才會聲音輸出
AMD_HDTPWR
AMD_HDT1
X_H2X10SM-1.27PITCH_BLUE-RH
N31-2100170-S88
Stuff for first model
TYPE1_CPU_SEL:
1:CPU_1P8_S5 (Type2,3)
0:CPU_1P8(Type0)
D03-514BA09-N03
D03-PA00209-N03
IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA
IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA
B*Ib>Ic=10*0.181=1.81>0.16
IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA
IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA
B*Ib>Ic=10*0.08=0.8>0.16
Schematic Cfg
CFG-7C02-***-Arsenal
Gaming
Project
V
A
MICRO-START INTL CO.,LTD.
Title
AM4 DISPLAY/AUDIO
Size
Custom
Document Number
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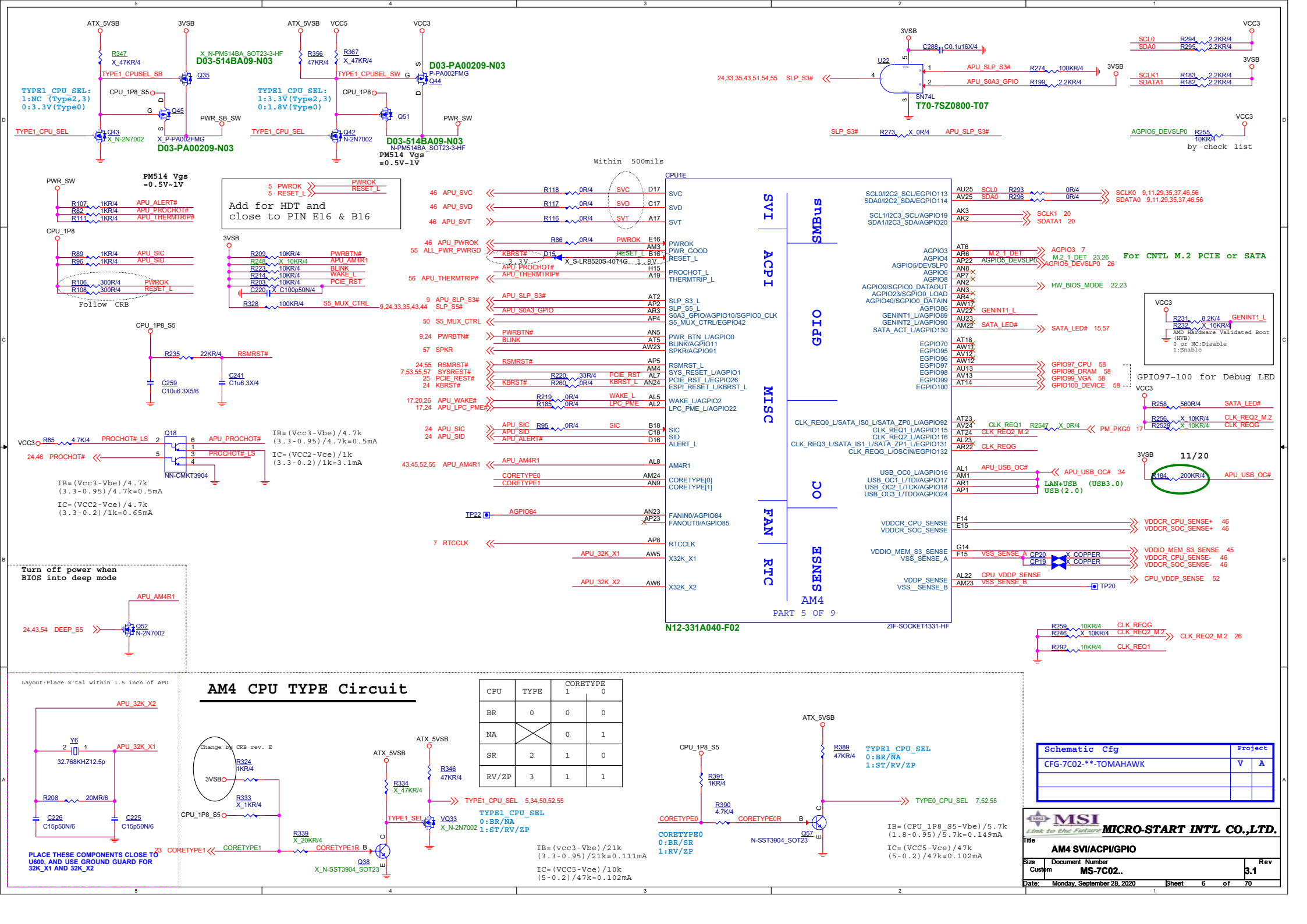


| CPU | TYPE | CORETYPE 1 | 0 |
|---|---|---|---|
| BR | 0 | 0 | 0 |
| NA | X | 0 | 1 |
| SR | 2 | 1 | 0 |
| RV/ZP | 3 | 1 | 1 |

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-**-TOMAHAWK | V | A |
| | | |
| | | |

| Size | Document Number | Rev |
|---|---|---|
| Custom | MS-7C02.. | 3.1 |

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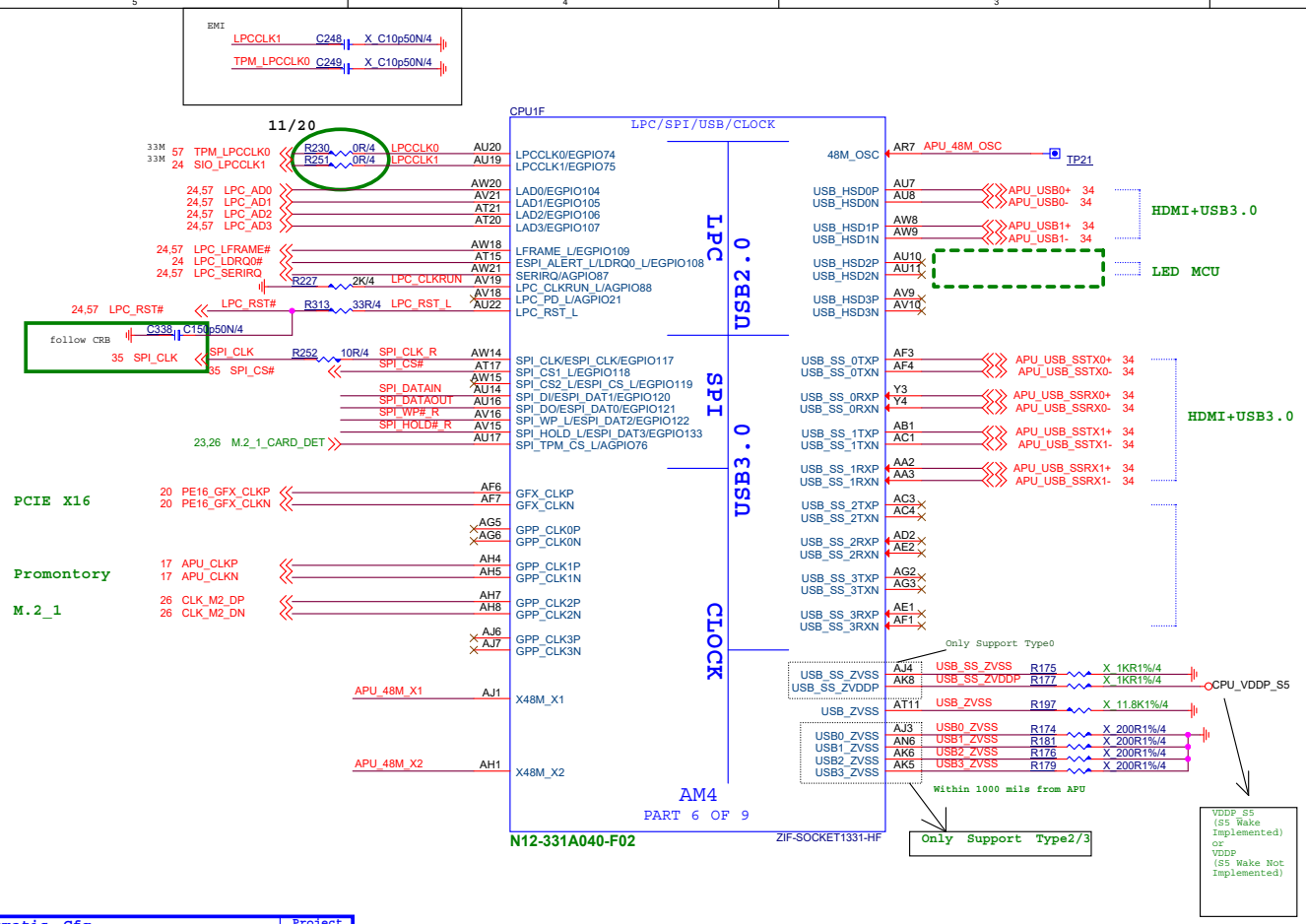
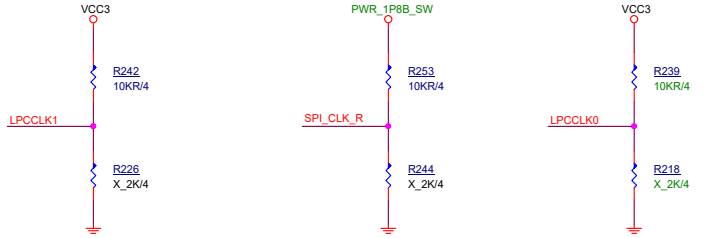
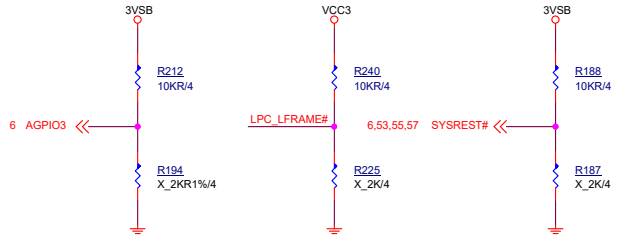


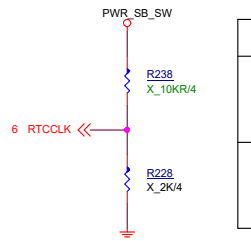

# Strapping Options




| | LPCCLK1 | SPI_CLK | LPCCLK0 |
|---|---|---|---|
| PULL HIGH | Configured for Internal clock generator (Default) | Use 48Mhz crystal clock and generate both internal and external clocks (Default) | LPC device Boot Fail Timer Enabled |
| PULL LOW | Configured for External clock generator ????? | Use 100Mhz PCIE clock as reference clock and generate internal clocks only | LPC device Boot Fail Timer Disabled (Default) |

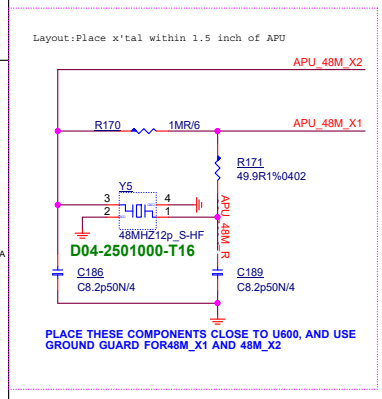



| | AGPIO3 | SIO_LFRAME | SYSREST# |
|---|---|---|---|
| PULL HIGH | Enhanced Reset logic (Default) | SPI ROM (Default) | Normal reset mode (Default) |
| PULL LOW | Traditional Reset logic | LPC ROM | short reset mode |

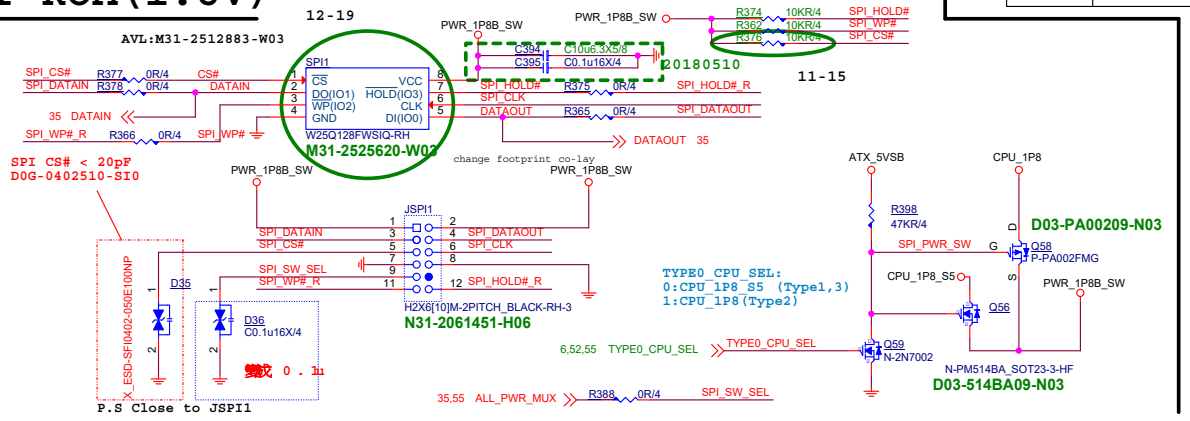



| | RTCCLK |
|---|---|
| PULL HIGH | RTC Coin Battery is on board (Default) |
| PULL LOW | RTC Coin Battery is not on board |

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-**-Arsenal Gaming | V | A |
| | | |




# SPI ROM(1.8V)

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Title: AM4 LPC/SPI/USB/CLK/STRAP

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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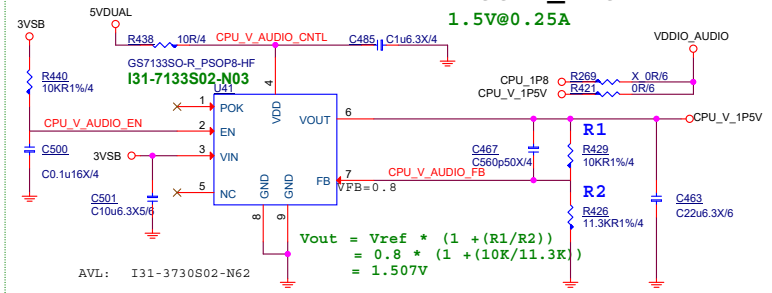
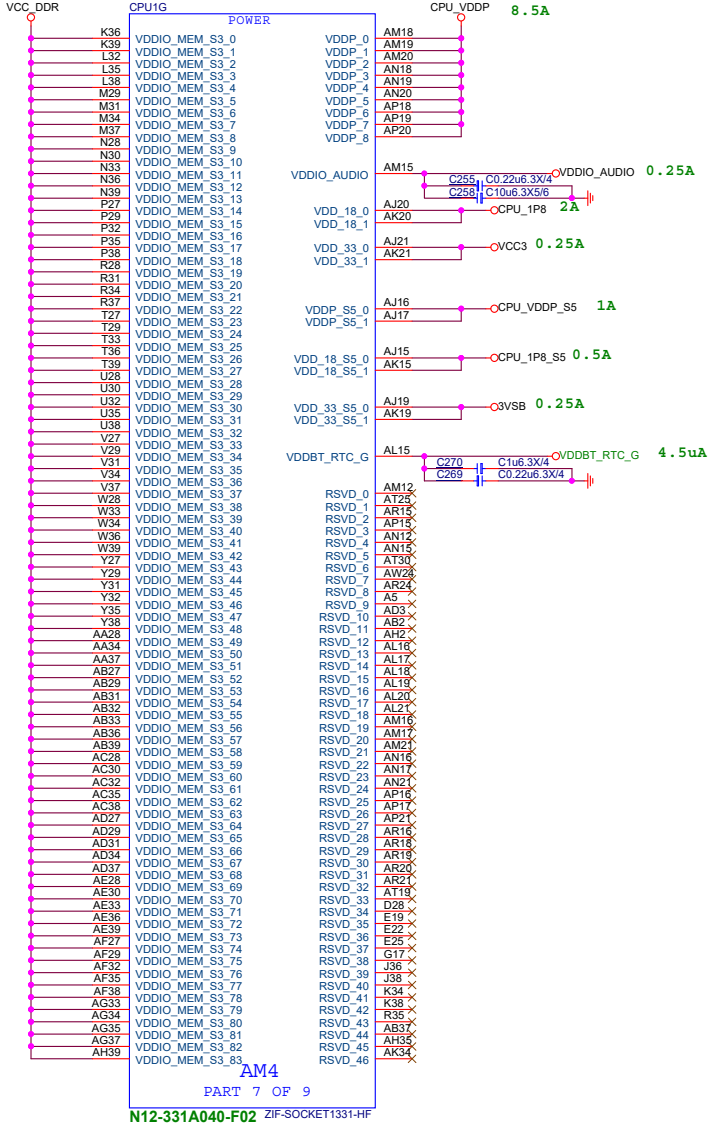
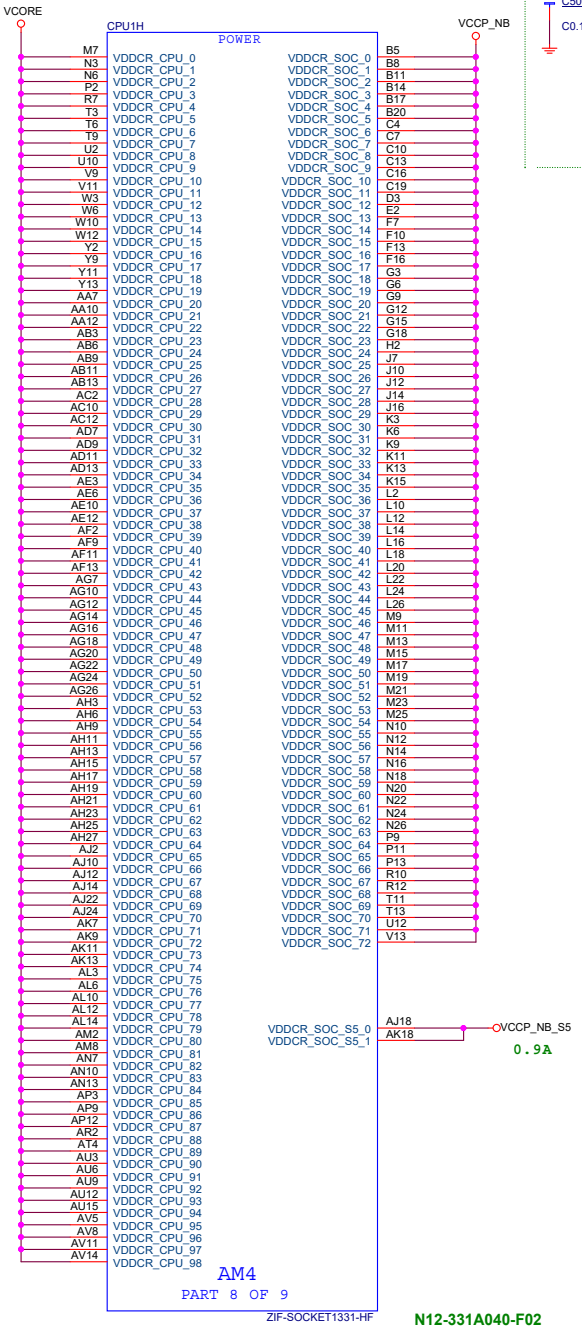
# VDDIO_AUDIO Circuit

1.5V@0.25A

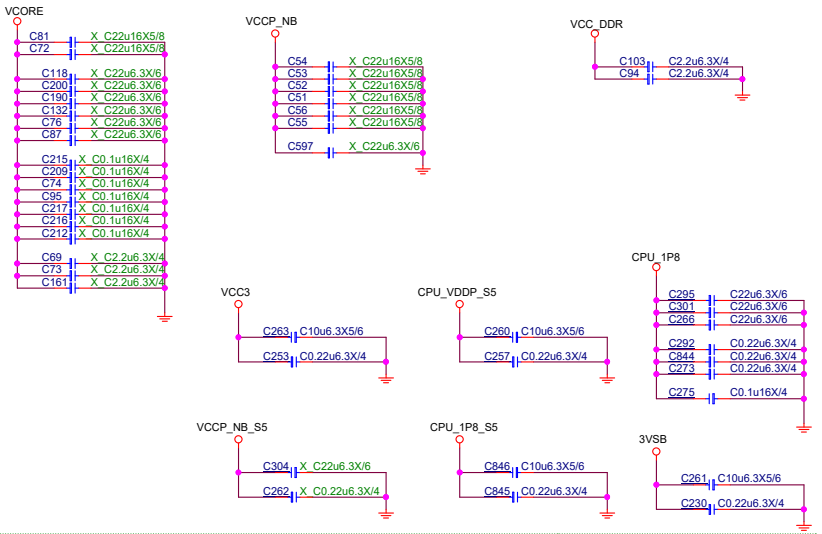



15.5A

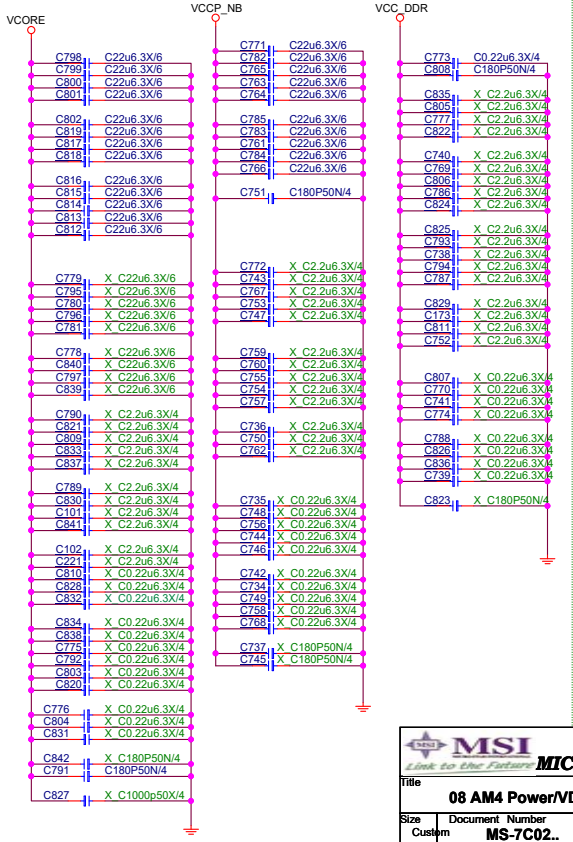


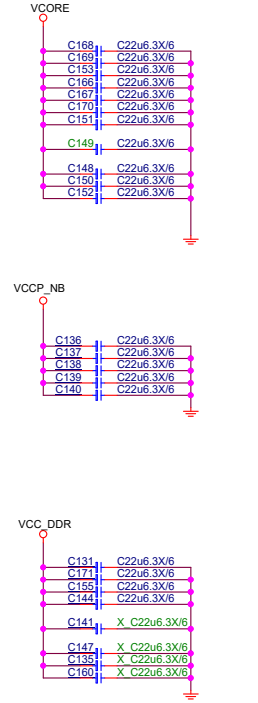

# TOP SIDE




# BOTTOM SIDE




# TOP CAVITY




| | | | |
|---|---|---|---|
| MSI Link to the Future | MICRO-START INTL CO.,LTD. | | |
| Title | 08 AM4 Power/VDDIO_AUDIO Power | | |
| Size: Custom | Document Number: MS-7C02.. | | Rev: 3.1 |
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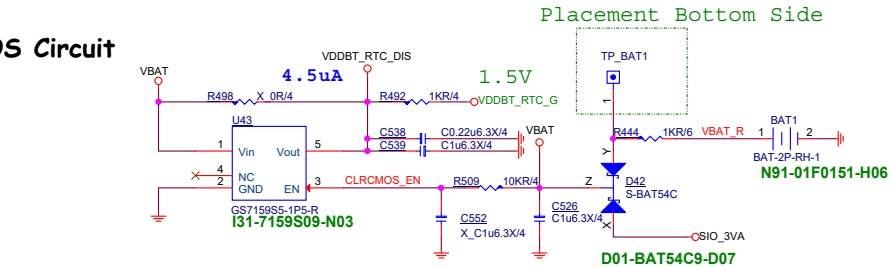
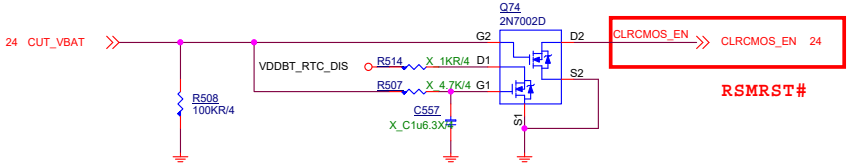
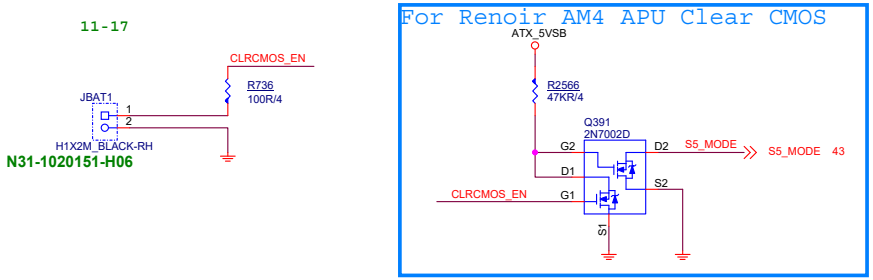
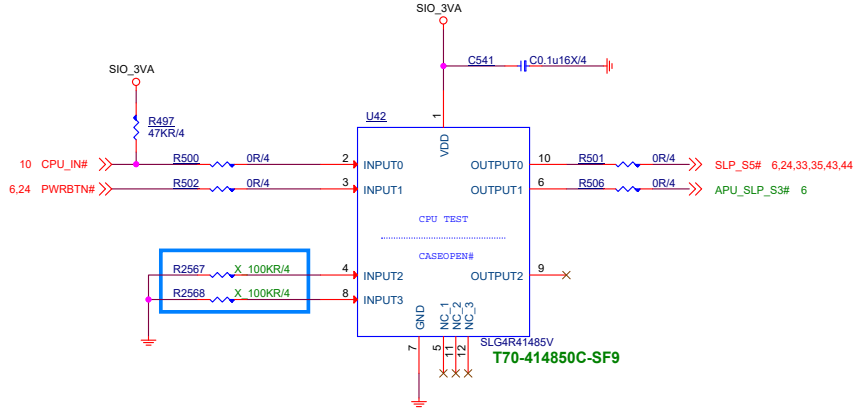
# RTC & Clear CMOS Circuit



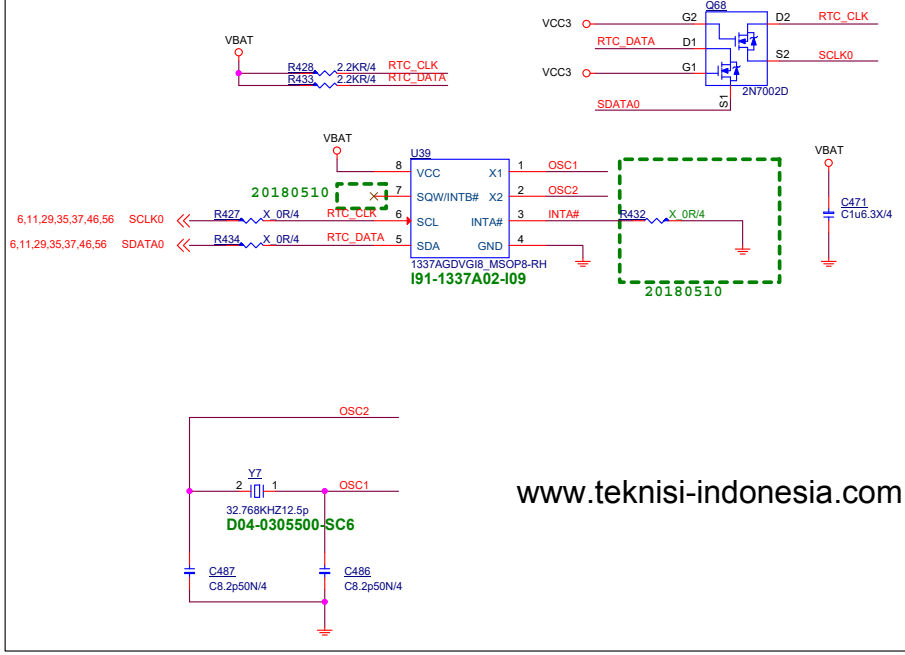




11-17




## RTC Backup

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| | | |
|---|---|---|
| Title | RTC/Clear CMOS/RTC Power | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
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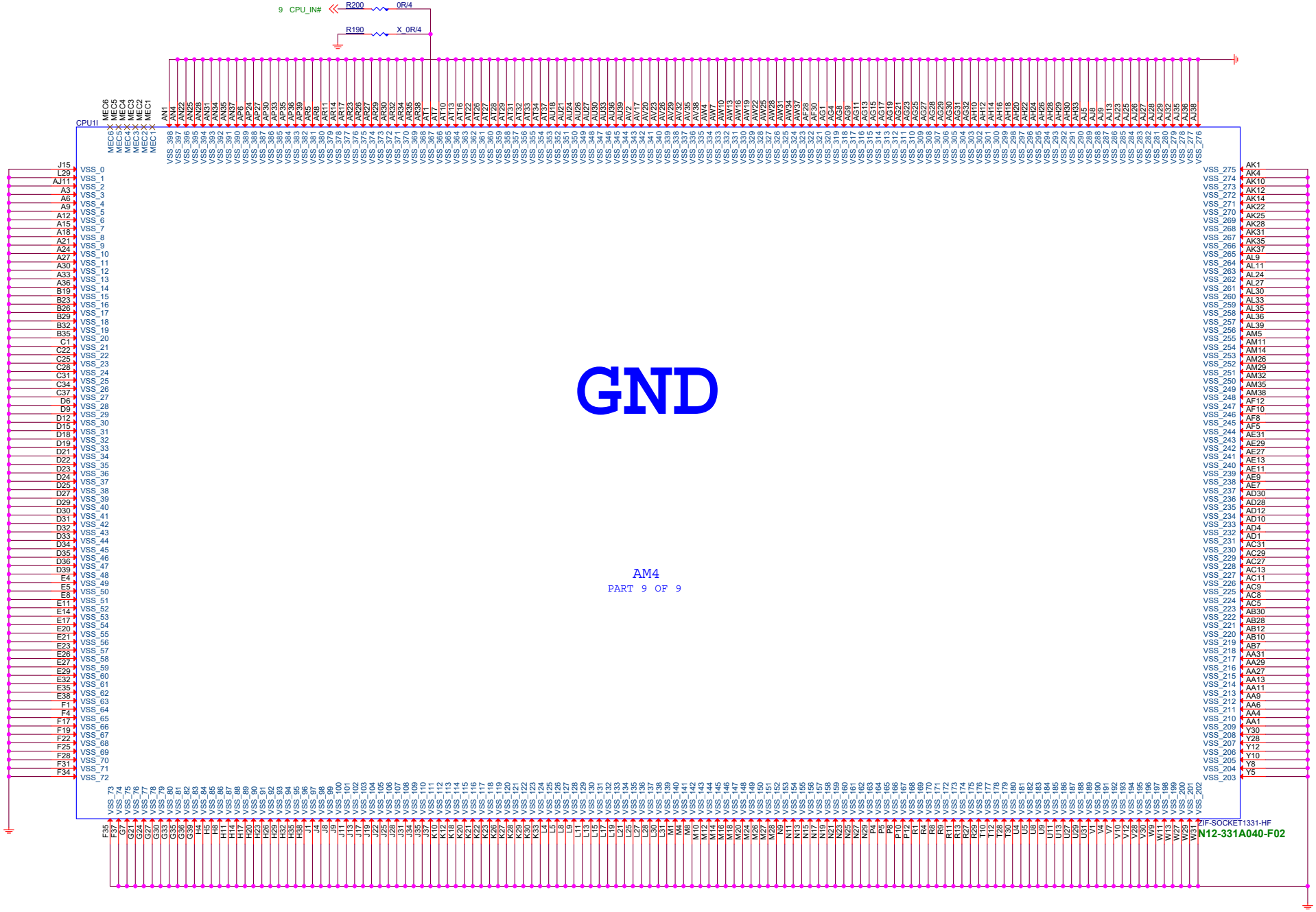


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| | | | |
|---|---|---|---|
| Title | AM4 GND | | |
| Size | Document Number | | Rev |
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DIMMA1A

DIMMA2A

| SMBus 0 | |
|---|---|
| Device | 8-bit Address (hex) |
| DIMMA0 | A0 |
| DIMMA1 | A4 |
| DIMMB0 | A2 |
| DIMMB1 | A6 |

DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]

DIMM2(CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]

DDRIV-288P_BLACK-RH-21
N13-2880581-L06

DDRIV-288P_BLACK-RH-21
N13-2880581-L06

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |

MICRO-START INTL CO.,LTD.

Title: DDR4 DIMM CH-A

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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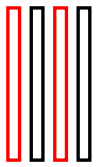


DIMMB1A

DDRIV-288P_BLACK-RH-21

N13-2880581-L06

DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]

DIMMB2A

DDRIV-288P_BLACK-RH-21

N13-2880581-L06

DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |
| | | |
| | | |

MICRO-START INT'L CO.,LTD.

Title: DDR4 DIMM CH-B

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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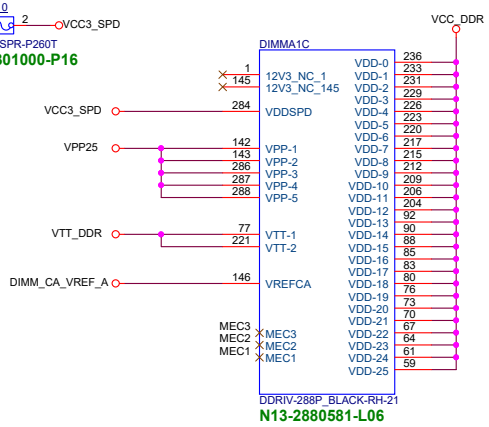
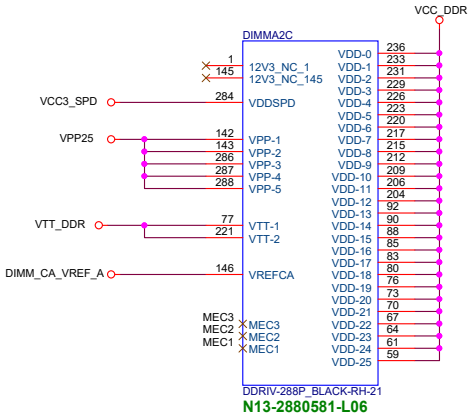
avl:D08-0301100-B07

F10
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC



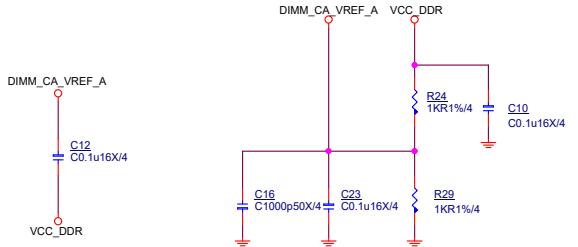
N13-2880581-L06

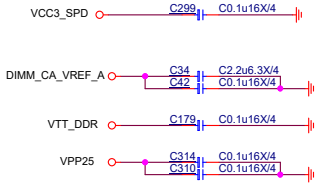


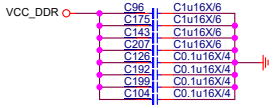
N13-2880581-L06

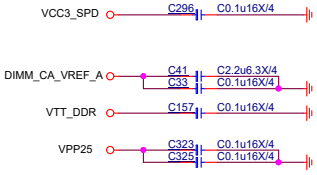
# DDR VREF

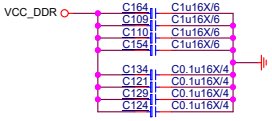
(place resistors close to DIMMs)

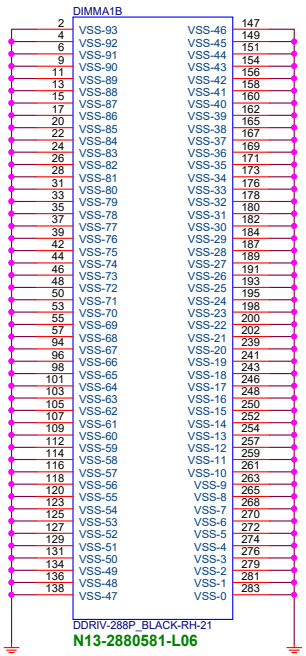


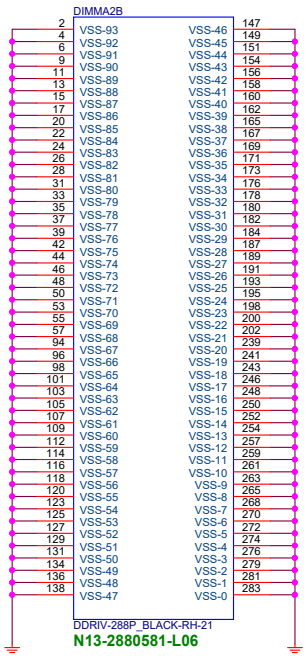



N13-2880581-L06



N13-2880581-L06

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| | | |
|---|---|---|
| Title | DDR4-POWER/GND-1 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
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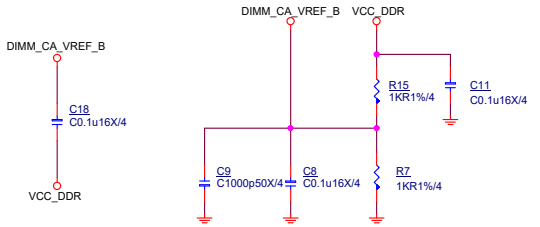
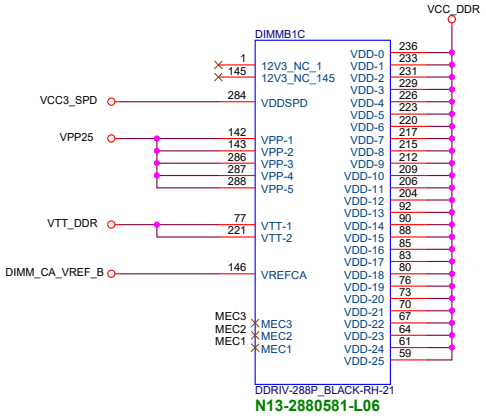
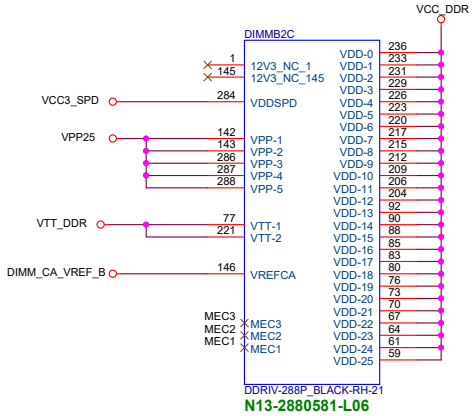
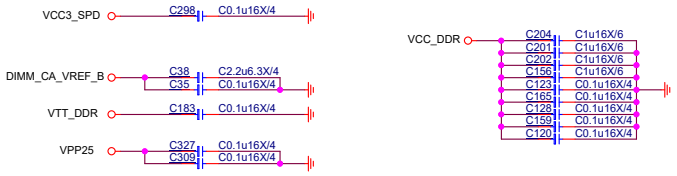
# DDR VREF

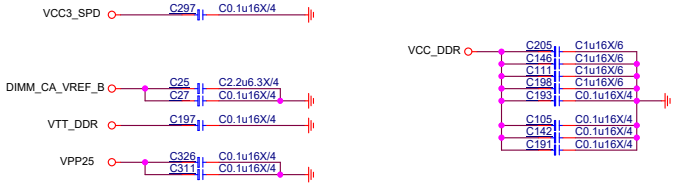
(place resistors close to DIMMs)

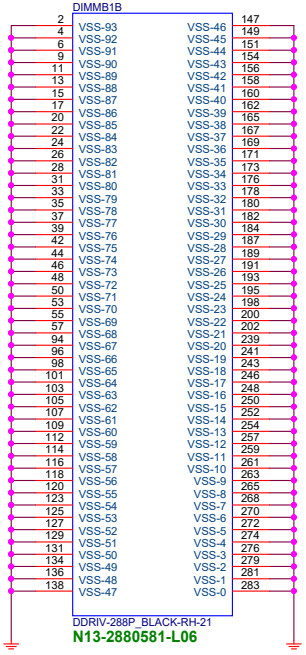


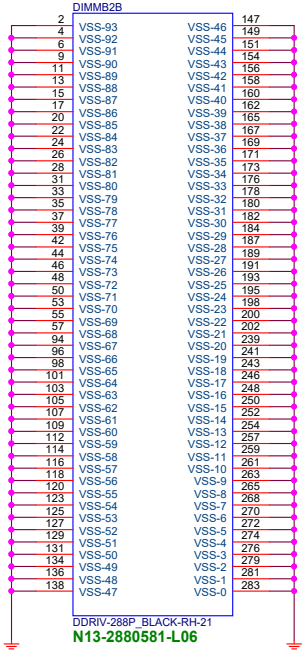



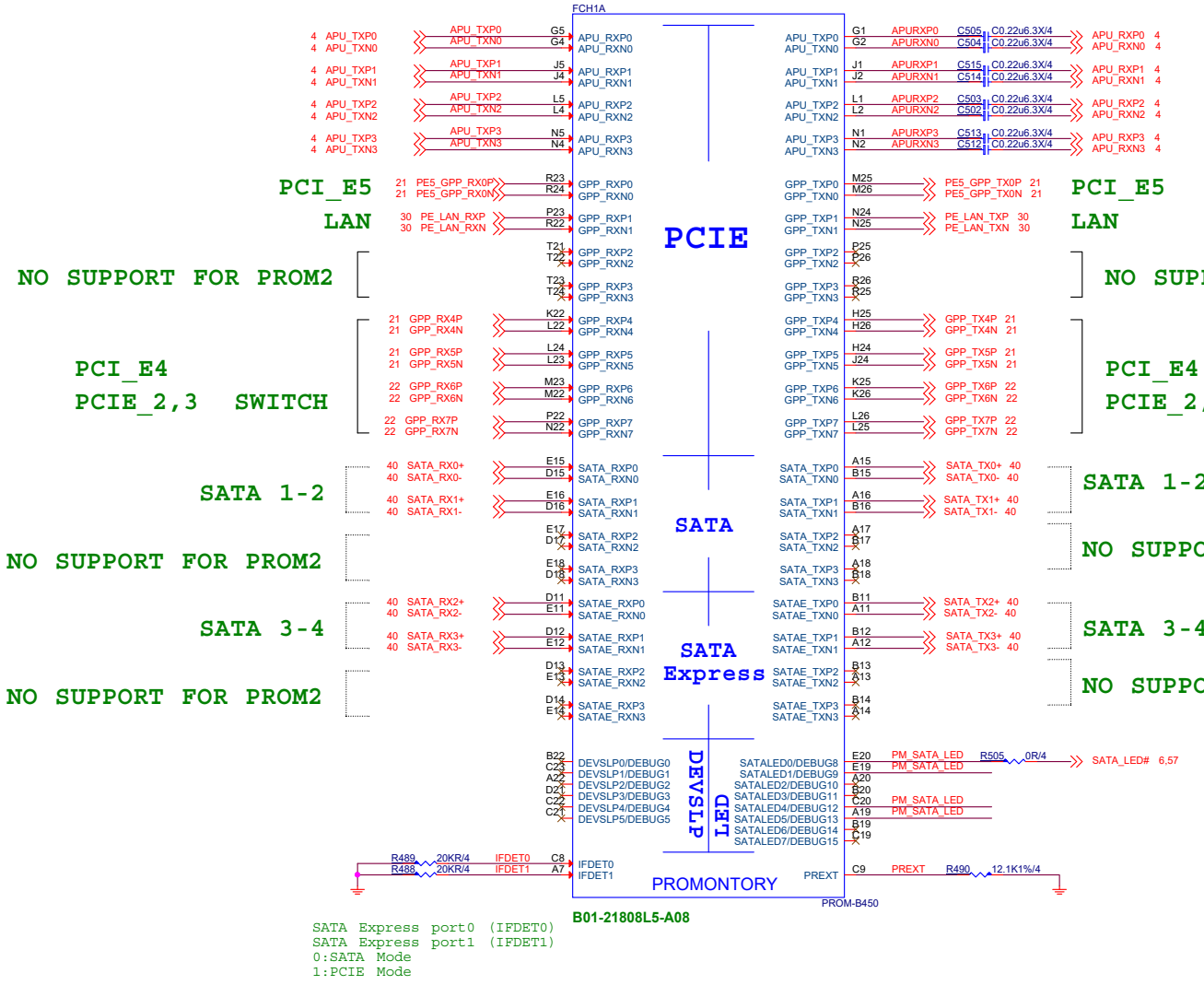




MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | DDR4-POWER/GND-2 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 14 of 70 | |




## Appendix C Port Mapping for Different Bus Models

| BUS Model | USB | | | |
|---|---|---|---|---|
| | 3.1 Gen2 10 Gbps | 3.1 Gen1 5 Gbps | 2.0 | Debug Port |
| PROM4 | USB_SSP Port0~1 | USB_SS Port 0~5 | USB_HSD Port0~13 | USB_SSP Port0 |
| PROM2 | USB_SSP Port0~1 | USB_SS Port 0~1 | USB_HSD Port0~5<br>USB_HSD Port10~13 | USB_SSP Port0 |
| PROM1 | USB_SSP Port0 | USB_SS Port0<br>USB_SSP Port1 | USB_HSD Port0~5<br>USB_HSD Port10, 12~13 | USB_SSP Port0 |

| BUS Model | SATA 3.0 | SATA Express | PCI Express® Gen2 GPP | PCI Express® CLK |
|---|---|---|---|---|
| PROM4 | SATA port0~3 | SATAE port0~3 | GPP lane0~7 | CLK0~7 |
| PROM2 | SATA port0~1 | SATAE port0~1 | GPP lane0~1<br>GPP lane4~7 | CLK0~1<br>CLK4~7 |
| PROM1 | SATA port0~1 | SATAE port0~1 | GPP lane4~7 | CLK4~7 |

CLK2.3不能用
CLK1-3不能用

MSI MICRO-START INTL CO.,LTD.

Title: Promontory-PCIE/SATA/SATAE

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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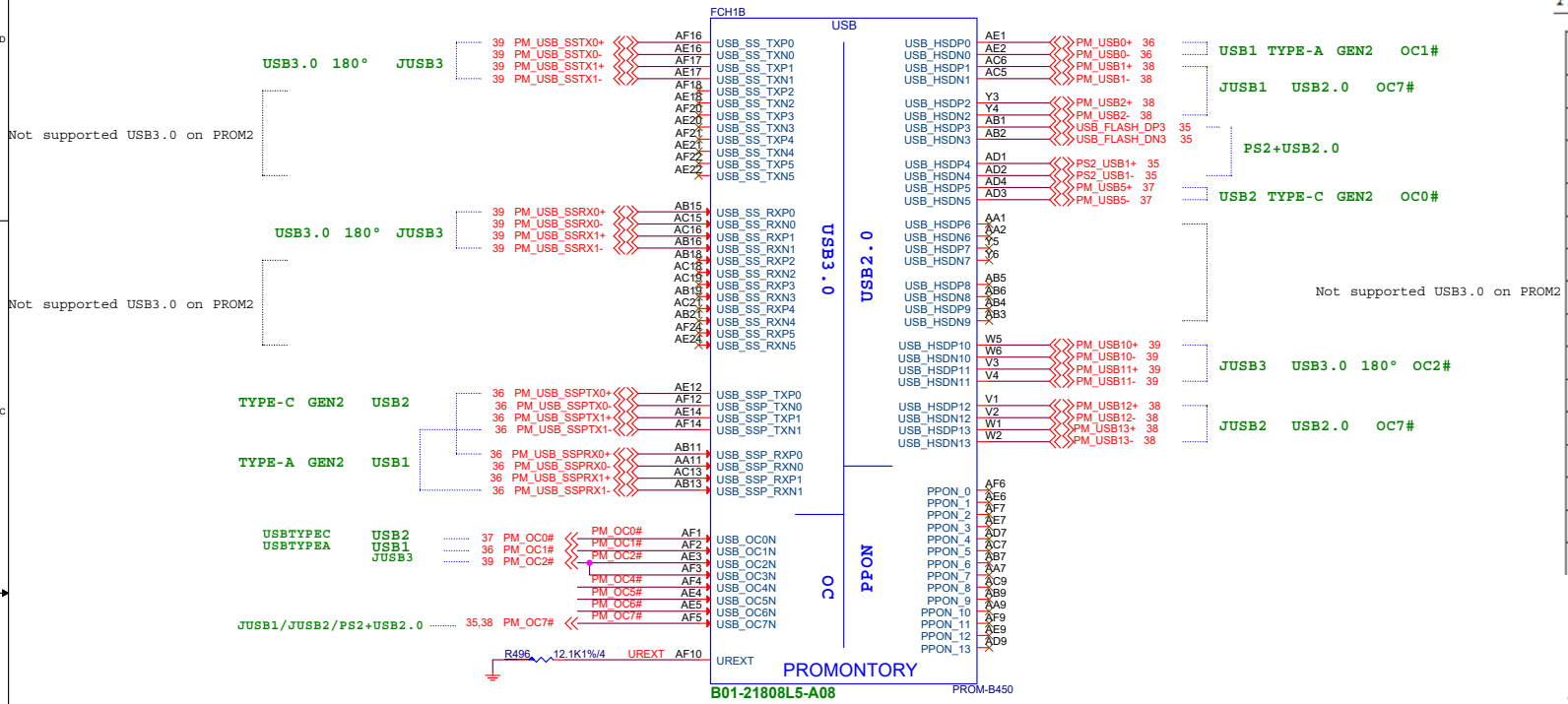


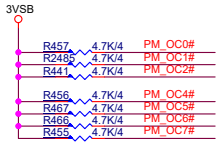


# Appendix D USB Port to OC Pin Mapping

| USB3.1 | USB2.0 | USB_OC |
|---|---|---|
| USB_SSP_TX/RXP/N[0] | USB_HSDP/N[5] | USB_OC0N |
| USB_SSP_TX/RXP/N[1] | USB_HSDP/N[0] | USB_OC1N |
| **USB3.0** | **USB2.0** | **USB_OC** |
| USB_SS_TX/RXP/N[0] | USB_HSDP/N[10] | USB_OC2N |
| USB_SS_TX/RXP/N[1] | USB_HSDP/N[11] | USB_OC3N |
| USB_SS_TX/RXP/N[2] | USB_HSDP/N[6] | USB_OC4N |
| USB_SS_TX/RXP/N[3] | USB_HSDP/N[7] | USB_OC5N |
| USB_SS_TX/RXP/N[4] | USB_HSDP/N[8] | USB_OC6N |
| USB_SS_TX/RXP/N[5] | USB_HSDP/N[9] | USB_OC7N |
| | USB_HSDP/N[1] | USB_OC7N |
| | USB_HSDP/N[2] | USB_OC7N |
| | USB_HSDP/N[3] | USB_OC7N |
| | USB_HSDP/N[4] | USB_OC7N |
| | USB_HSDP/N[12] | USB_OC7N |
| | USB_HSDP/N[13] | USB_OC7N |

# Appendix C Port Mapping for Different Bus Models

| BUS Model | USB | | | |
|---|---|---|---|---|
| | 3.1 Gen2 10 Gbps | 3.1 Gen1 5 Gbps | 2.0 | Debug Port |
| PROM4 | USB_SSP Port0~1 | USB_SS Port 0~3 | USB_HSD Port0~13 | USB_SSP Port0 |
| PROM2 | USB_SSP Port0~1 | USB_SS Port 0~1 | USB_HSD Port0~5<br>USB_HSD Port10~13 | USB_SSP Port0 |
| PROM1 | USB_SSP Port0 | USB_SS Port0<br>USB_SSP Port1 | USB_HSD Port0~5<br>USB_HSD Port10, 12~13 | USB_SSP Port0 |

| BUS Model | SATA 3.0 | SATA Express | PCI Express® Gen2 GPP | PCI Express® CLK |
|---|---|---|---|---|
| PROM4 | SATA port0~3 | SATAE port0~3 | GPP lane0~7 | CLK0~7 |
| PROM2 | SATA port0~1 | SATAE port0~1 | GPP lane0~1<br>GPP lane4~7 | CLK0~1<br>CLK4~7 |
| PROM1 | SATA port0~1 | SATAE port0~1 | GPP lane4~7 | CLK4~7 |

CLK2.3不能用
CLK1-3不能用

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: Promontory-USB/OC

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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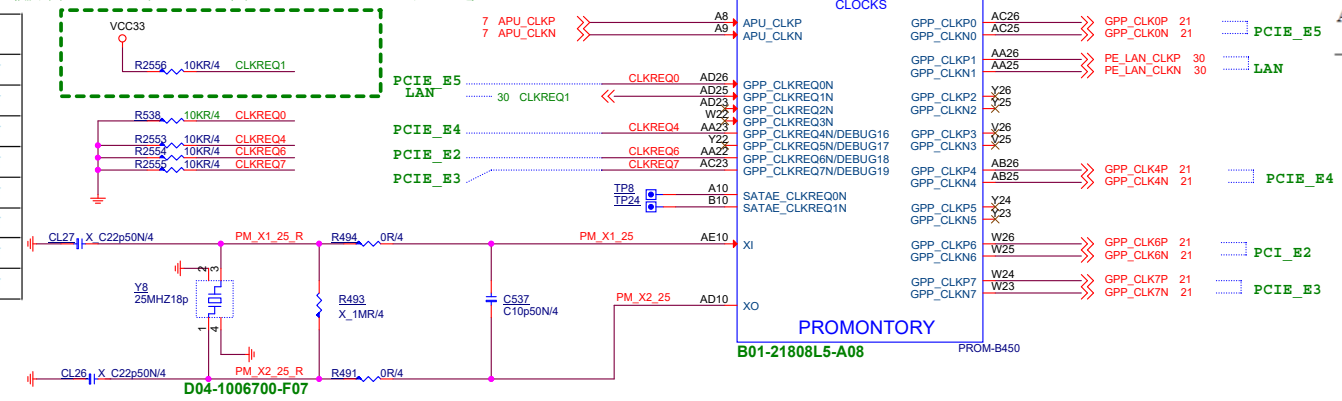
| GPP Clock | CLKREQ# |
|---|---|
| GPP_CLKP/N[0] | GPP_CLKREQ0N |
| GPP_CLKP/N[1] | GPP_CLKREQ1N |
| GPP_CLKP/N[2] | GPP_CLKREQ2N |
| GPP_CLKP/N[3] | GPP_CLKREQ3N |
| GPP_CLKP/N[4] | GPP_CLKREQ4N |
| GPP_CLKP/N[5] | GPP_CLKREQ5N |
| GPP_CLKP/N[6] | GPP_CLKREQ6N |
| GPP_CLKP/N[7] | GPP_CLKREQ7N |

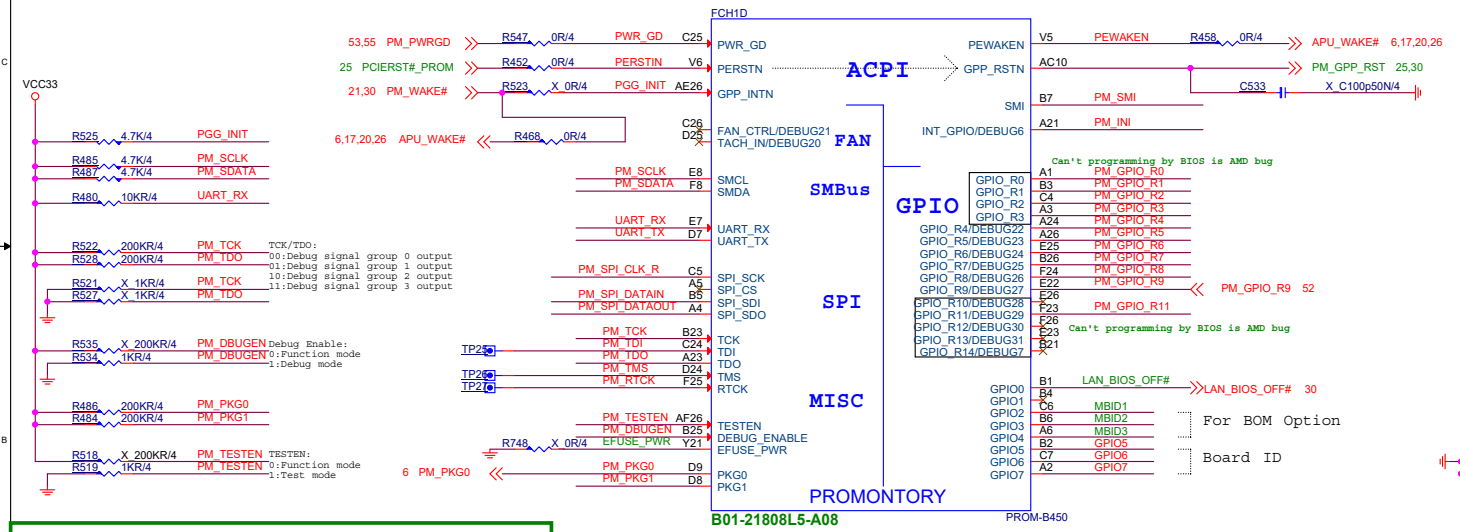


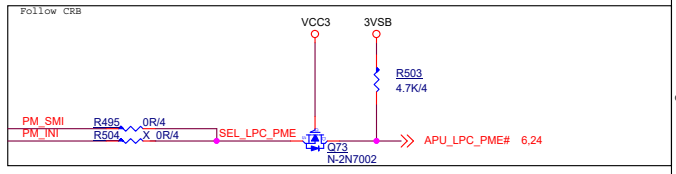

## Appendix C Port Mapping for Different Bus Models

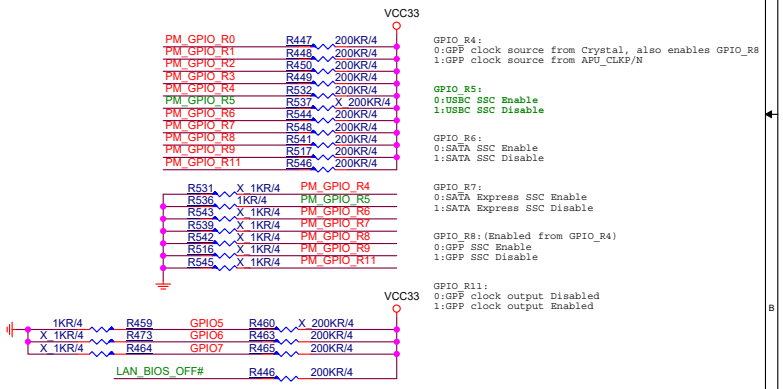
| BUS Model | USB | | | |
|---|---|---|---|---|
| | 3.1 Gen2 10 Gbps | 3.1 Gen1 5 Gbps | 2.0 | Debug Port |
| PROM4 | USB_SSP Port0~1 | USB_SS Port 0~5 | USB_HSD Port0~13 | USB_SSP Port0 |
| PROM2 | USB_SSP Port0~1 | USB_SS Port 0~1 | USB_HSD Port0~5<br>USB_HSD Port10~13 | USB_SSP Port0 |
| PROM1 | USB_SSP Port0 | USB_SS Port0<br>USB_SSP Port1 | USB_HSD Port0~5<br>USB_HSD Port10, 12~13 | USB_SSP Port0 |

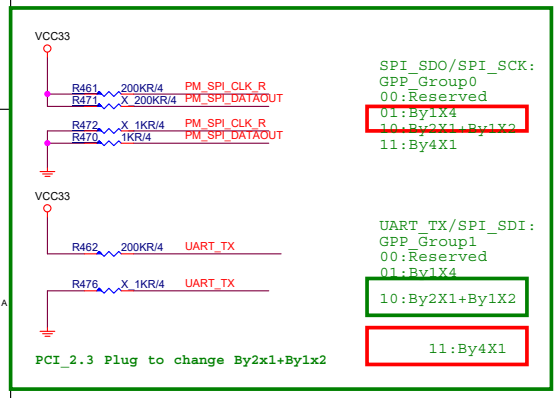
| BUS Model | SATA 3.0 | SATA Express | PCI Express® Gen2 GPP | PCI Express® CLK |
|---|---|---|---|---|
| PROM4 | SATA port0~3 | SATAE port0~3 | GPP lane0~7 | CLK0~7 |
| PROM2 | SATA port0~1 | SATAE port0~1 | GPP lane0~1<br>GPP lane4~7 | CLK0~1<br>CLK4~7 |
| PROM1 | SATA port0~1 | SATAE port0~1 | GPP lane4~7 | CLK4~7 |

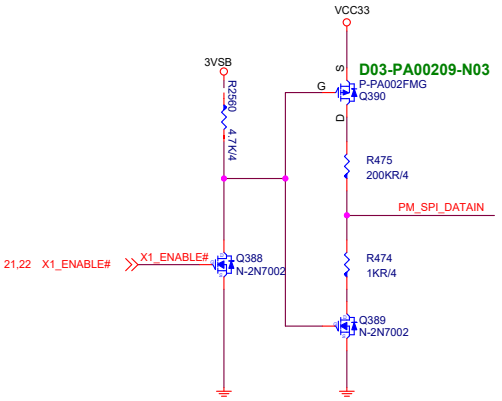
CLK2.3不能用
CLK1-3不能用



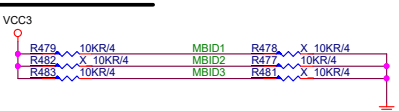




## BOM OPTION




| | MBID1 | MBID2 | MBID3 |
|---|---|---|---|
| 601-7C02-080 | 1 | 0 | 0 |
| 601-7C02-XXX | 1 | 0 | 1 |
| | | | |

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-** | V | A |
| | | |
| | | |

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Title: Promontory-CLK/ACPI/GPIO

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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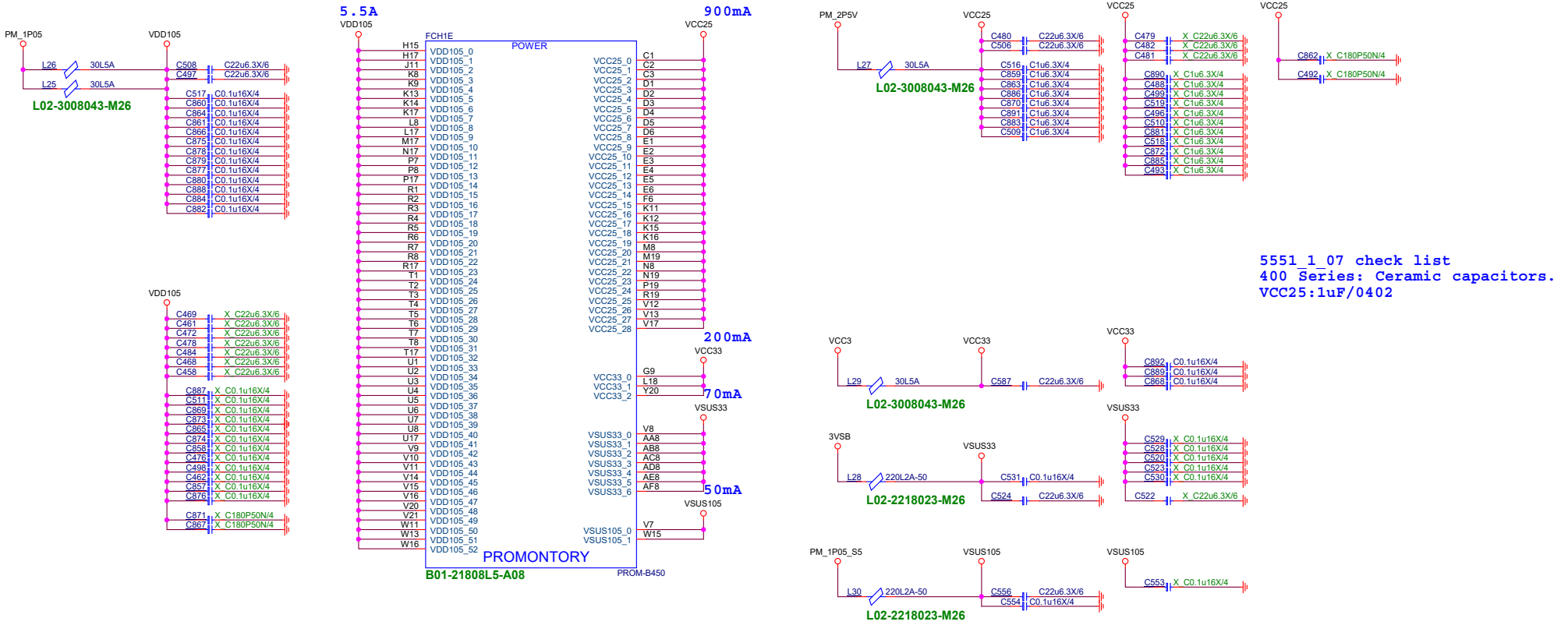
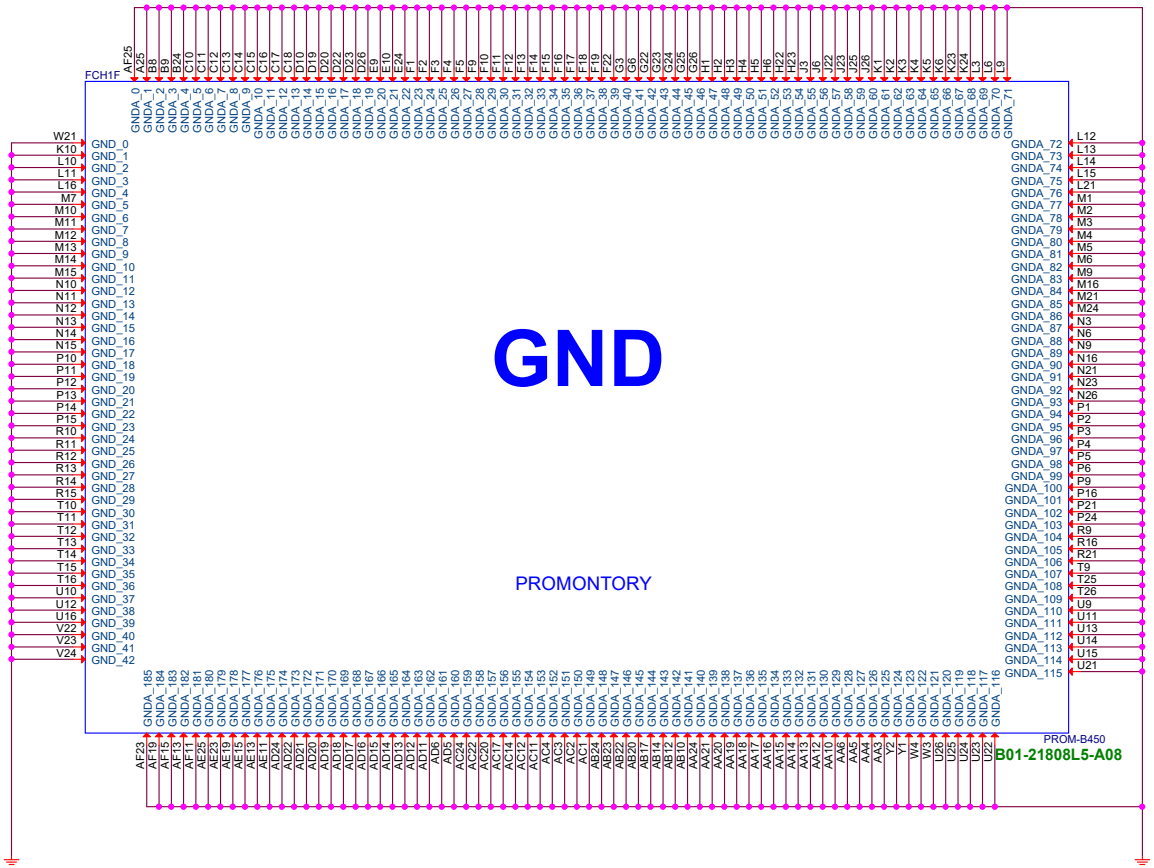


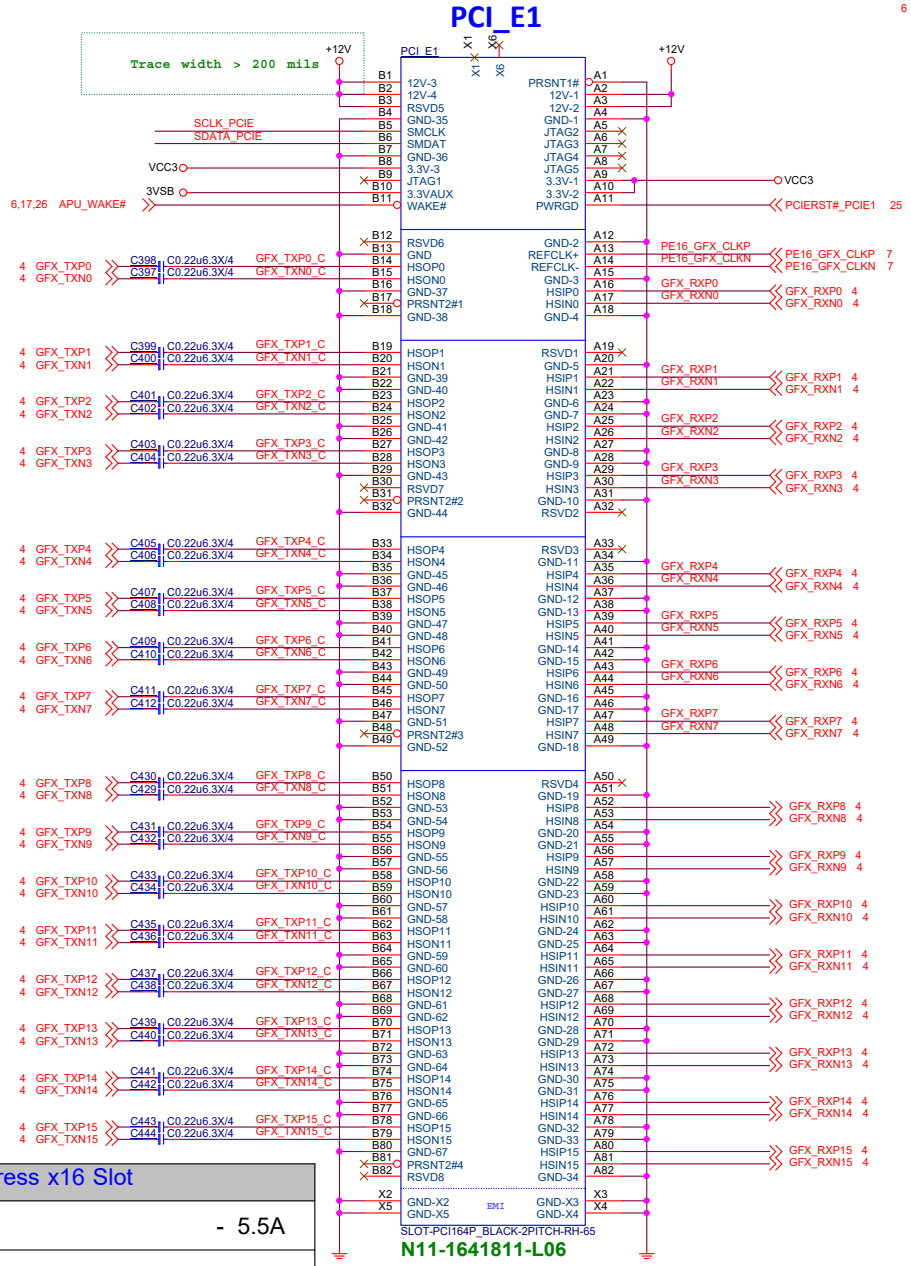

MICRO-START INTL CO.,LTD.

| | | | |
|---|---|---|---|
| Title | Promontory-Power | | |
| Size: Custom | Document Number: MS-7C02.. | | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 18 of 70 | | |

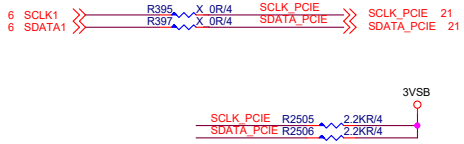


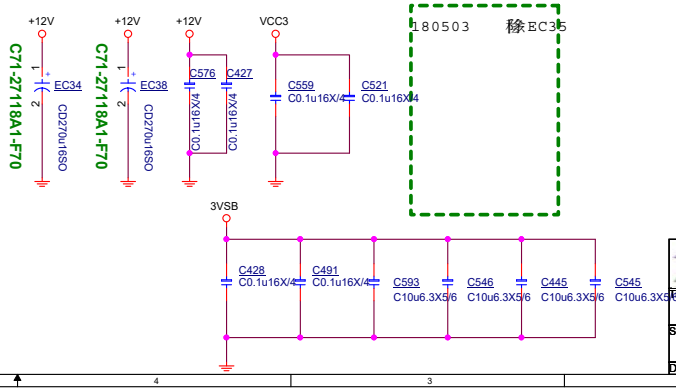

| | |
|---|---|
| MSI MICRO-STAR INT'L CO.,LTD. | |
| Title | Promontory-GND |
| Size: Custom | Document Number: MS-7C02.. |
| Rev | 3.1 |
| Date: Monday, September 28, 2020 | Sheet 19 of 70 |

# PCI EXPRESS x16 Slot




| PCI Express x16 Slot | | |
|---|---|---|
| +12V | | - 5.5A |
| +VCC3 | | - 3A |
| +3V3_S5 | (wake) | - 375mA |
| +3V3_S5 | (no wake) | - 20mA |




| PCI Express x8 Slot | | |
|---|---|---|
| +12V | | - 5.5A |
| +VCC3 | | - 3A |
| +3V3_S5 | (wake) | - 375mA |
| +3V3_S5 | (no wake) | - 20mA |

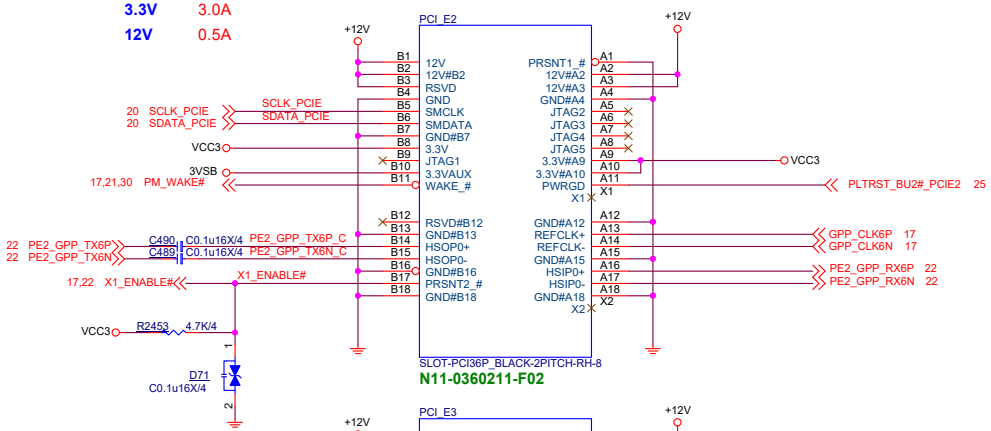
MSI Link to the Future MICRO-START INTL CO.,LTD.

| | | | |
|---|---|---|---|
| Title | PCI_E1/E4 X16/X8 | | |
| Size: Custom | Document Number: MS-7C02.. | | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 20 of 70 | | |

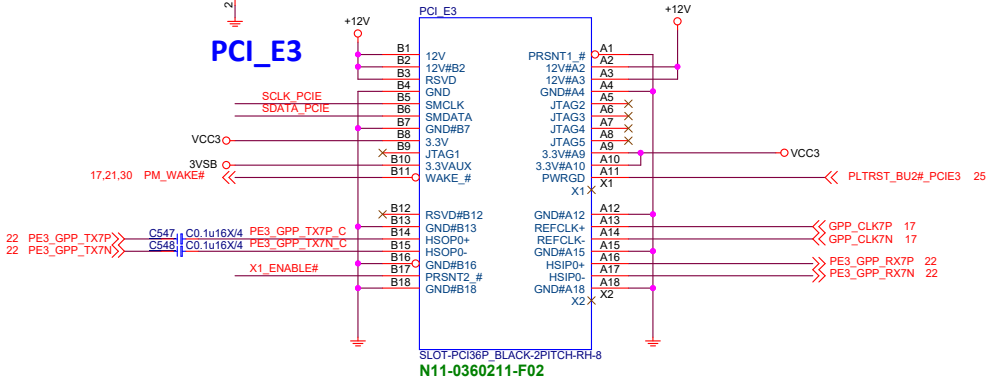
PCIEX1 12V 0.5A
3.3V weak 375mA

## PCI_E2

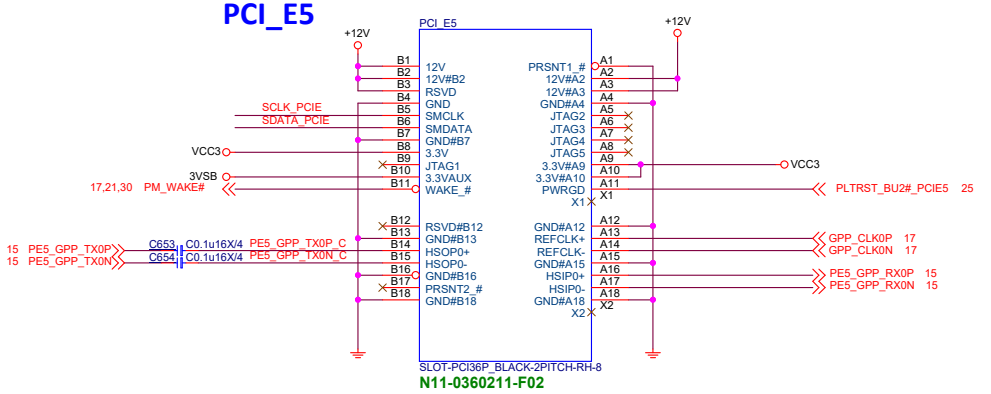
3.3V 3.0A
12V 0.5A



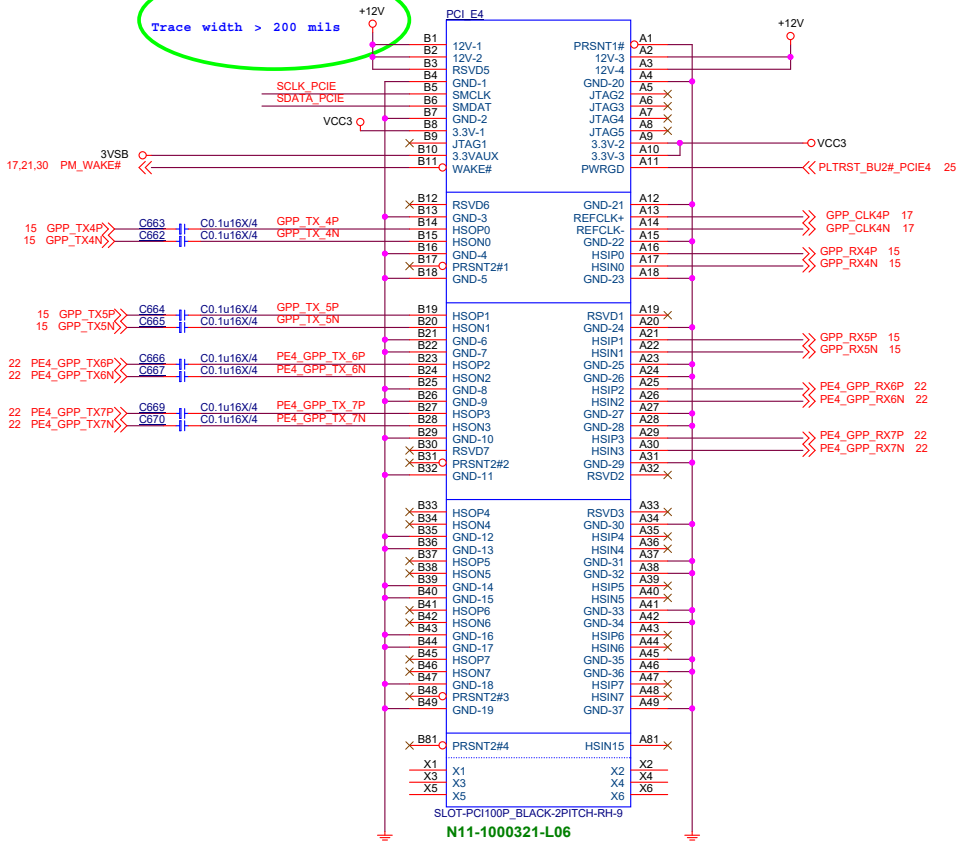

## PCI_E3

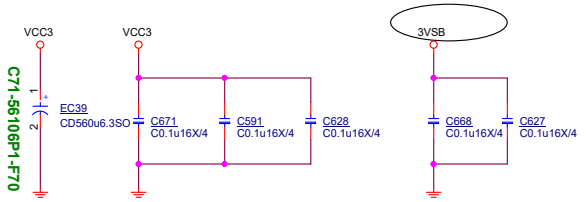



## PCI_E5




Trace width > 200 mils




| PCI Express x4 Slot *1 | | |
|---|---|---|
| +12V | | - 2.1A |
| +VCC3 | | - 3A |
| +3V3_S5 | (wake) | - 375mA |
| +3V3_S5 | (no wake) | - 20mA |
| **PCI Express x1 Slot *3** | | |
| +12V | | - 1.5 A |
| +VCC3 | | - 9A |
| +3V3_S5 | (wake) | - 1125mA |
| +3V3_S5 | (no wake) | - 60mA |

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |
| | | |

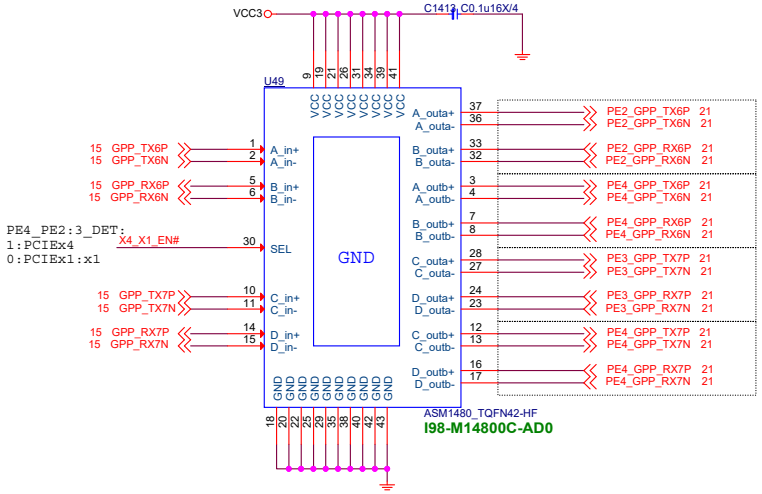
MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: PCI_E2_E3_E5/E4 X1/X4

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

Date: Monday, September 28, 2020 | Sheet 21 of 70

# PCI_E4 and PCIE_2 :3 and Switch




PCIE_2

PE4

PCIE_3

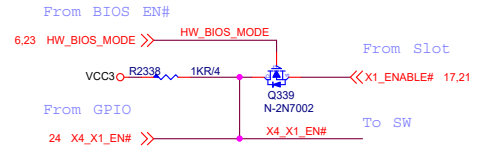
PE4

UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4

10:By2X1+By1X2
11:By4X1 (def)

| SEL | Function |
|---|---|
| L | N_in +/1 to N_outa+/- |
| H | N_in +/1 to N_outb+/- |

## PCIE Lanes control circuit




| | HW_BIOS_MODE | Q339 | Q381 | X1_ENABLE# | PM_SPI_DATAIN |
|---|---|---|---|---|---|
| Manual x4 | L | OFF | OFF | X | 11:By4x1 (def) |
| Manual x2, x1 ,x1 | L | OFF | OFF | L | 10:By2x1+By1x2 |
| HW x4 | H | ON | ON | H | 11:By4X1 (def) |
| H/W x2,x1,x1 | H | ON | ON | L (Stuff PCIE_1) | 10:By2x1+By1x2 |

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: PCIE Switch X4 / M2_2

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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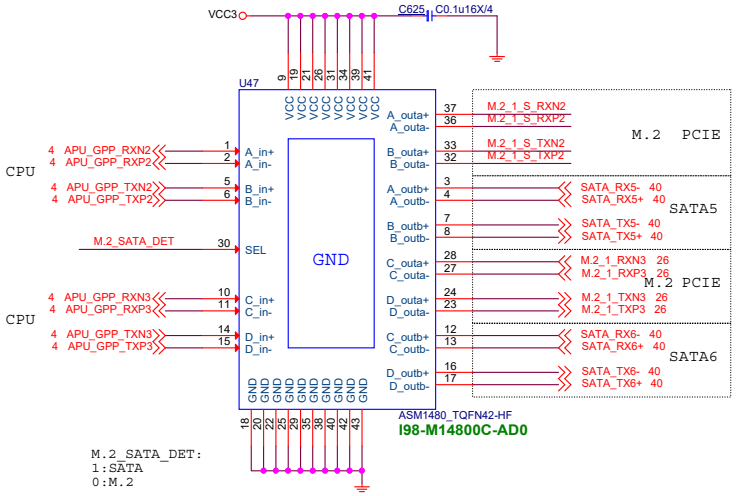
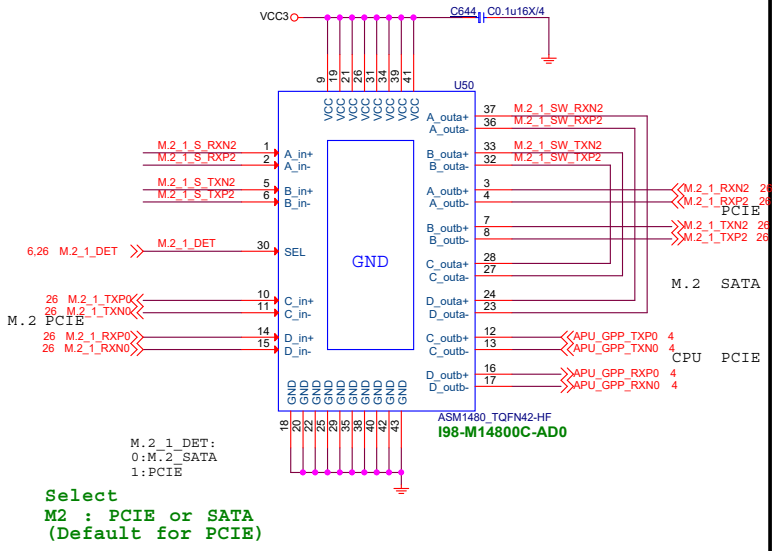
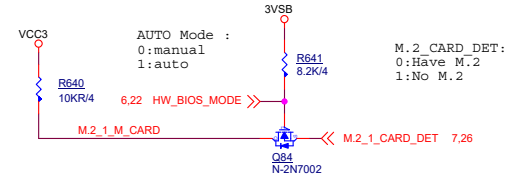
# M2_1 and SATA5 6 Switch

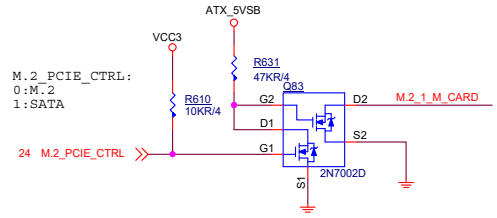


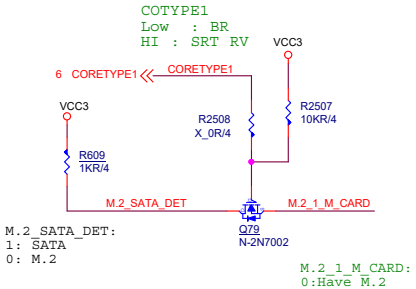

| SEL | Function |
|---|---|
| L | N_in +/1 to N_outa+/- |
| H | N_in +/1 to N_outb+/- |




| | AUTO Mode | SATA CON | M.2(PCIE) | M.2(SATA) |
|---|---|---|---|---|
| **HW_BIOS_MODE** | 1 | | 0 | 0 |
| M.2_PCIE_CTRL | 1 | | 0 | 0 |
| M.2_1_CARD_DET | | 1 | 0 | 0 |
| M.2_DET | | X | 1 | 0 |




| CPU | TYPE | CORETYPE 1 | CORETYPE 0 |
|---|---|---|---|
| BR | 0 | 0 | 0 |
| NA | | 0 | 1 |
| SR | 2 | 1 | 0 |
| RV/ZP | 3 | 1 | 1 |

MICRO-START INTL CO.,LTD.

Title: 23 PCIE Switch M2_2/SATA

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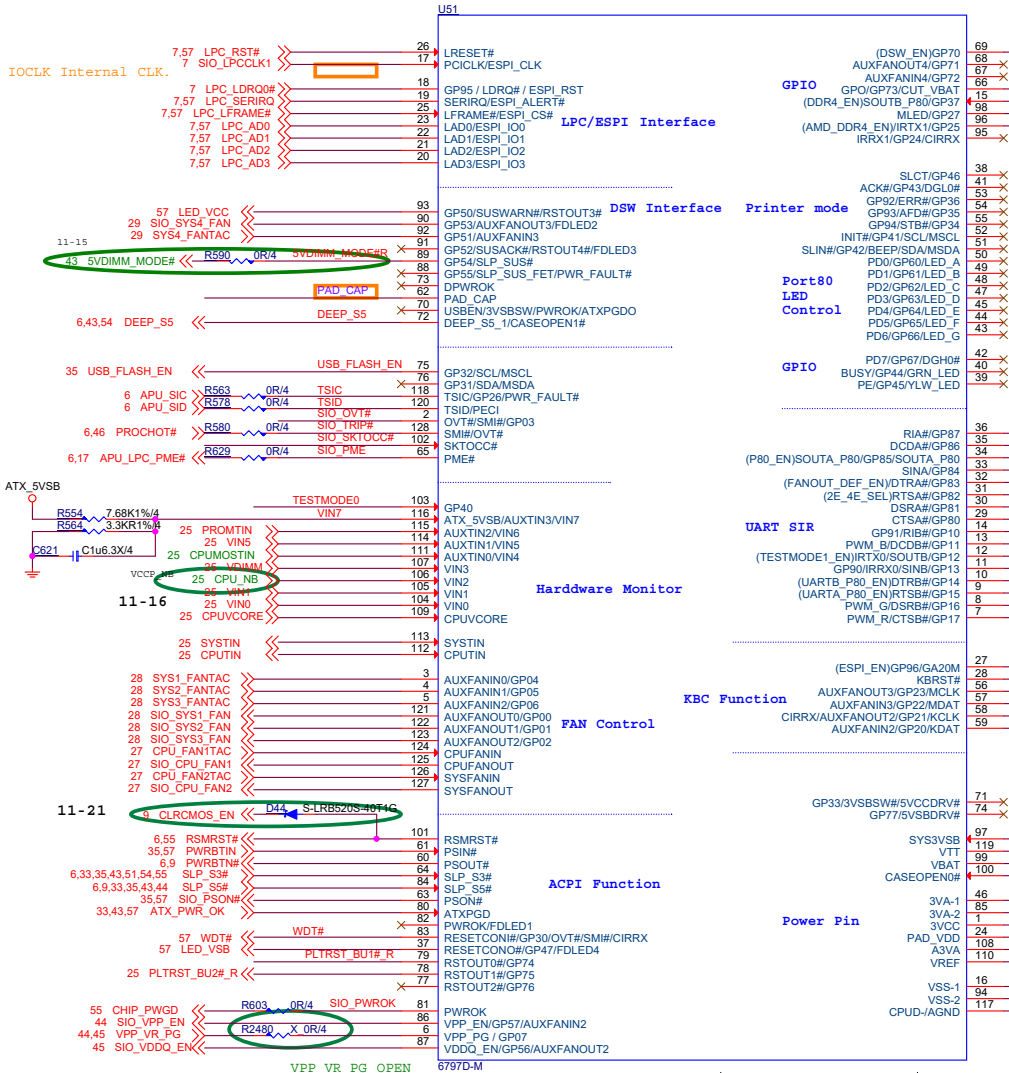
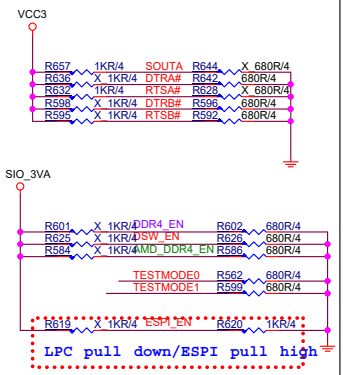



## POWER ON STRAPPING PIN FOR NCT6797/6795

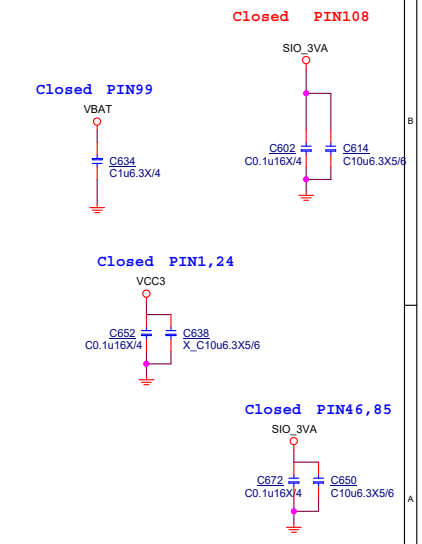
| PIN | 6797/6795 NAME | Circuit NAME | 0 | 1 | Strap Point |
|---|---|---|---|---|---|
| 9 | UARTA_P80_EN | RTSB# | DISABLE UARTA80 | ENABLE UARTA80 | LRESET |
| 10 | UARTB_P80_EN | DTRB# | DISABLE UARTB80 | ENABLE UARTB80 | LRESET |
| 12 | TESTMODE1_EN | TESTMODE1_EN | DISABLE TEST1MODE | ENABLE TEST1MODE | LRESET |
| 15 | DDR4_EN | DDR4_EN | Disable | Enable | |
| 27 | ESPI_EN | ESPI_EN | LPC | ESPI | |
| 31 | 2E_4E_SEL | RTSA# | I/O ADDRESS 2E | I/O ADDRESS 4E | LRESET |
| 32 | FANOUT_DEF_EN | DTRA# | default 50% | default 100% | INTERNAL PWROK |
| 34 | P80_EN | SOUTA | ENABLE Non_PORT80 | ENABLE PORT80 | LRESET |
| 69 | DSW_EN | DSW_EN | DISABLE INTEL DSW | ENABLE INTEL DSW | INTERNAL RSMRST |
| 96 | AMDPWR_EN | AMDPWR_EN | DISABLE AMD PWR SEQ | ENABLE AMD PWR SEQ | INTERNAL RSMRST |
| 103 | 6795 TESTMODE_EN<br>6797 GP40 | 6795 WDT#<br>6797 WDT# | 6795 DISABLE TESTMODE | 6795 ENABLE TESTMODE | INTERNAL RSMRST |

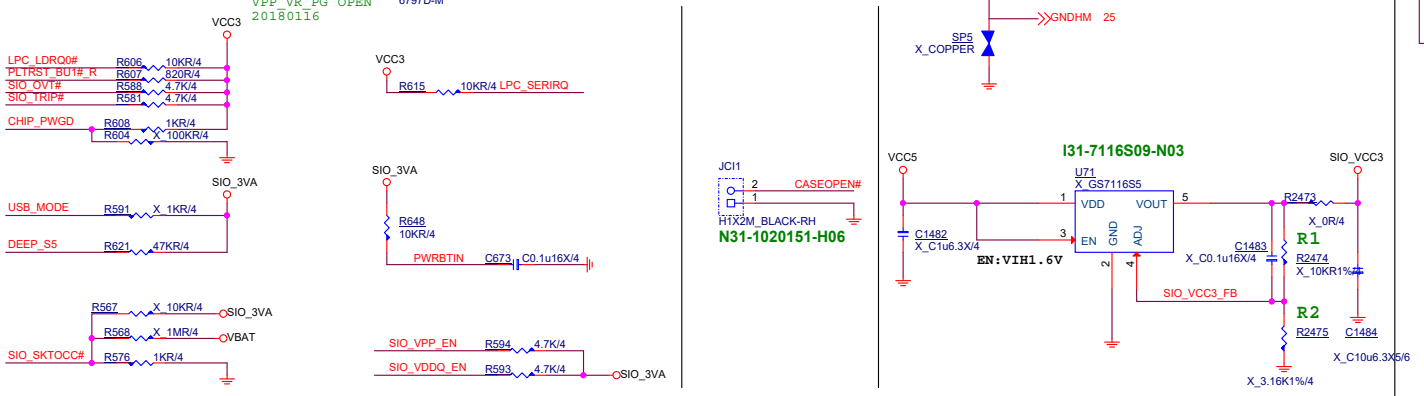
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

DTRA# high FAN 100% LOW FAN 50%




3V Analog Power




MSI MICRO-START INTL CO.,LTD.
Title: SIO NCT6797D
Size: Custom
Document Number: MS-7C02..
Rev: 3.1
Date: Monday, September 28, 2020
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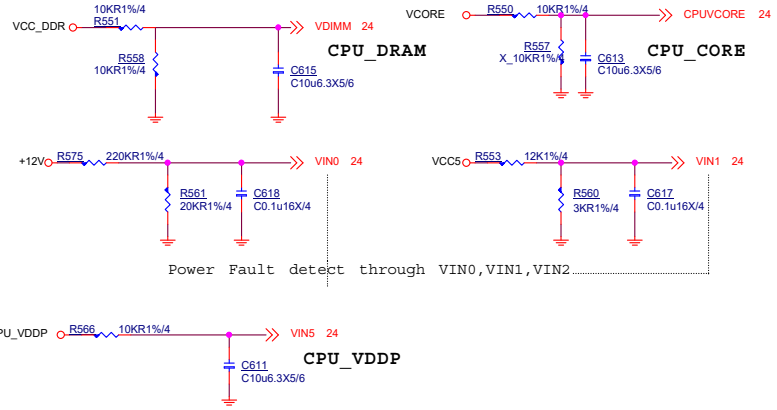
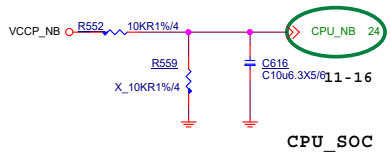
# HW Monitor - Voltage

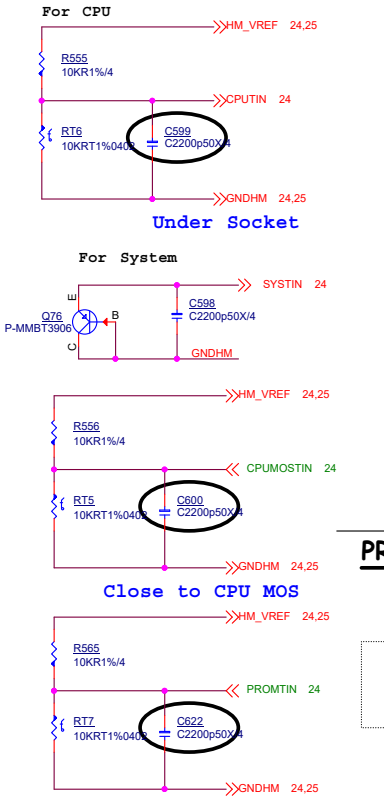
SIO HM Voltage over 2.048V will not detect



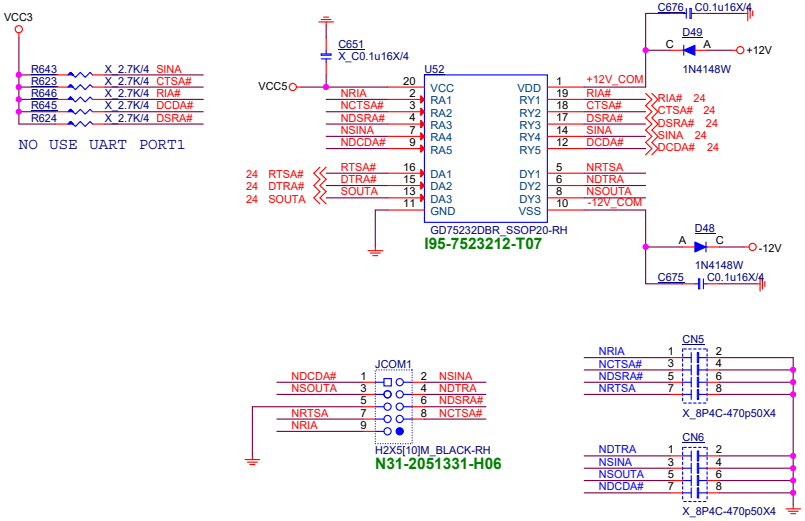

Inform BIOS disable VIN2 with Power Fault



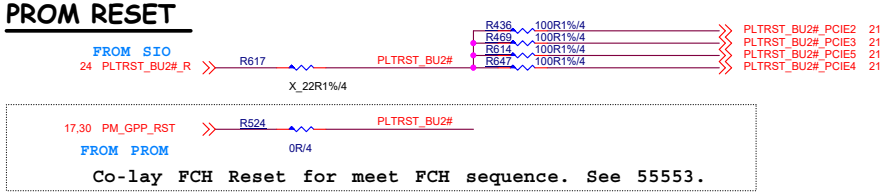

# TEMP SENSOR



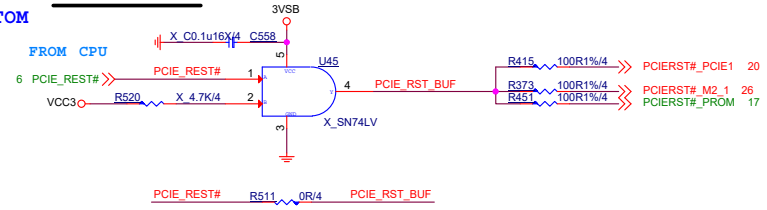

# COM PORT



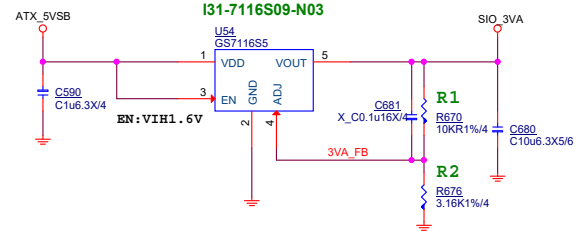

# PROM RESET




# CPU RESET




# SIO_3VA




Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

# PARALLAL PORT

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Title: SIO HWM/COM

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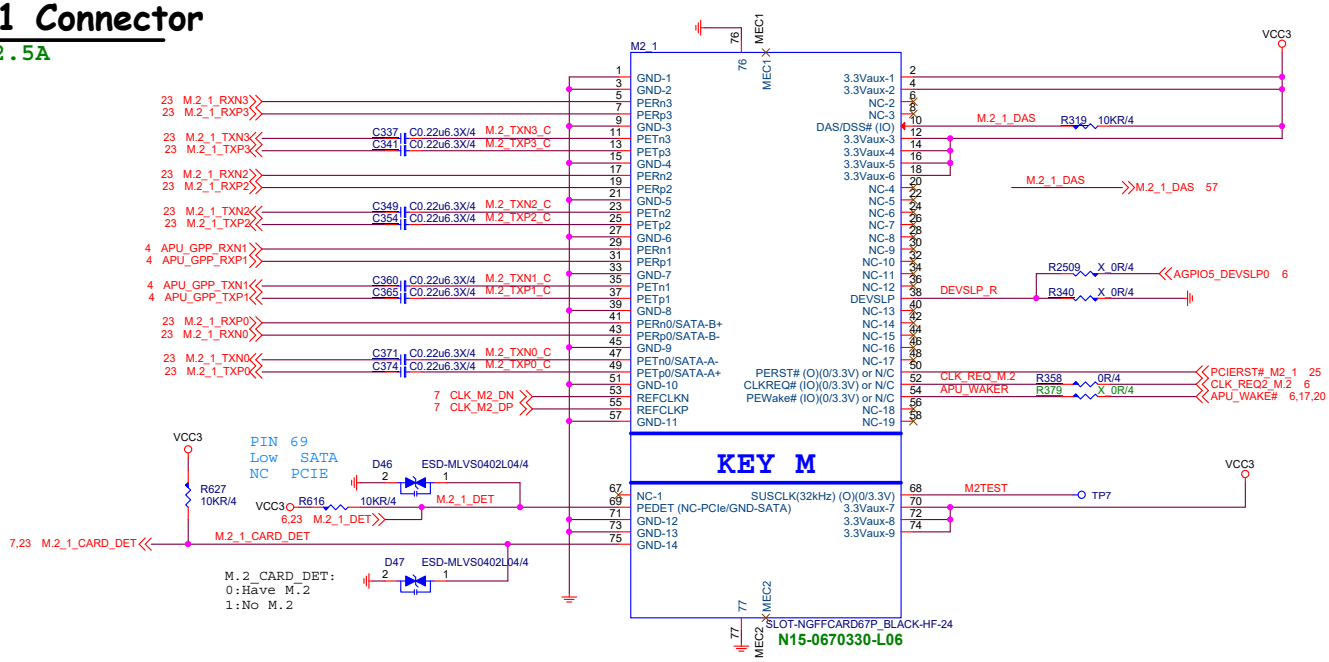
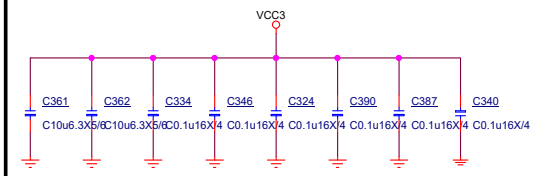
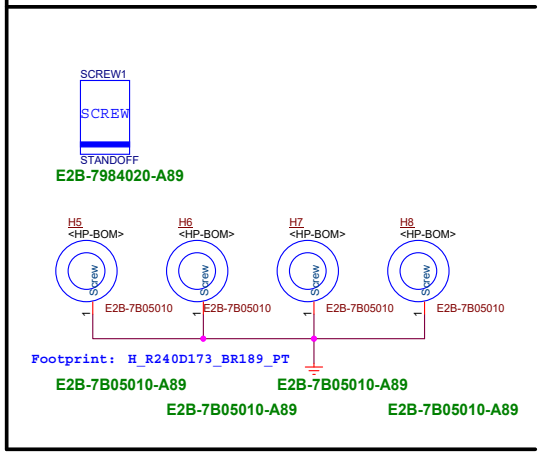
# M.2_1 Connector

3.3V@2.5A




| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-**-Arsenal Gaming | V | A |
| | | |
| | | |

MICRO-START INTL CO.,LTD.

Title: M.2_1

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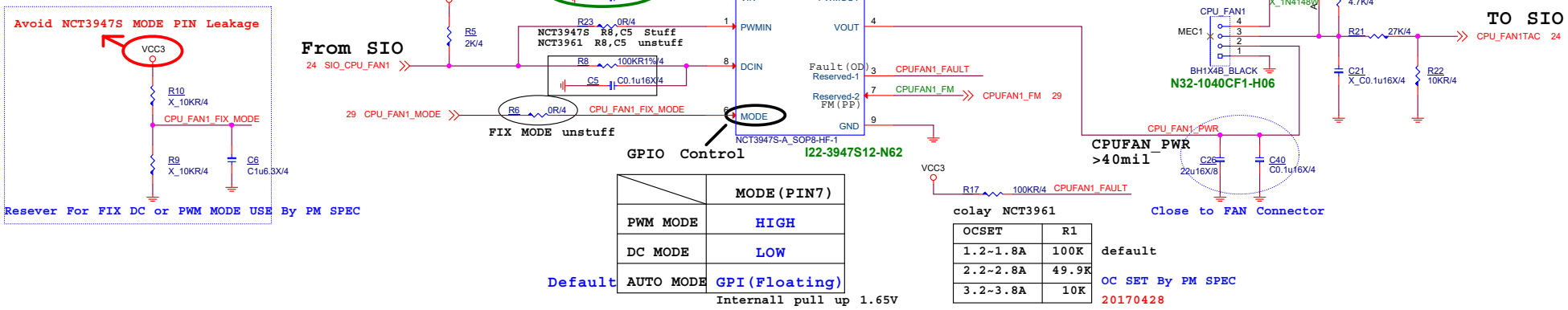
# TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE
2.FM:BIOS can read FAN PWM/DC MODE

## CPU_FAN1

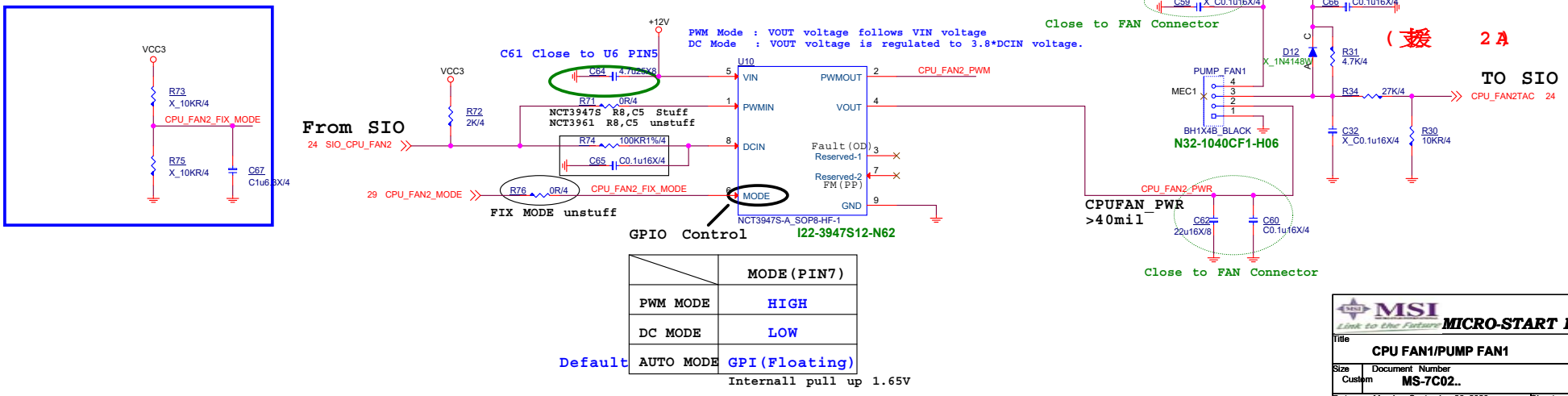



| | MODE(PIN7) |
|---|---|
| PWM MODE | HIGH |
| DC MODE | LOW |
| Default AUTO MODE | GPI(Floating) |

Internall pull up 1.65V

| OCSET | R1 | |
|---|---|---|
| 1.2~1.8A | 100K | default |
| 2.2~2.8A | 49.9K | OC SET By PM SPEC |
| 3.2~3.8A | 10K | 20170428 |

## PUMP_FAN1




| | MODE(PIN7) |
|---|---|
| PWM MODE | HIGH |
| DC MODE | LOW |
| Default AUTO MODE | GPI(Floating) |

Internall pull up 1.65V

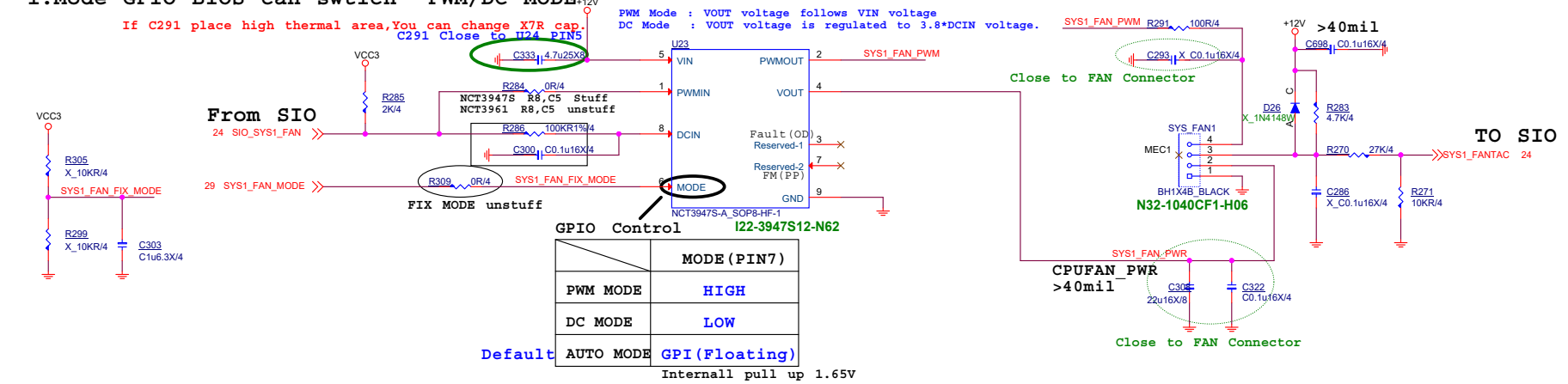
MSI MICRO-START INTL CO.,LTD.

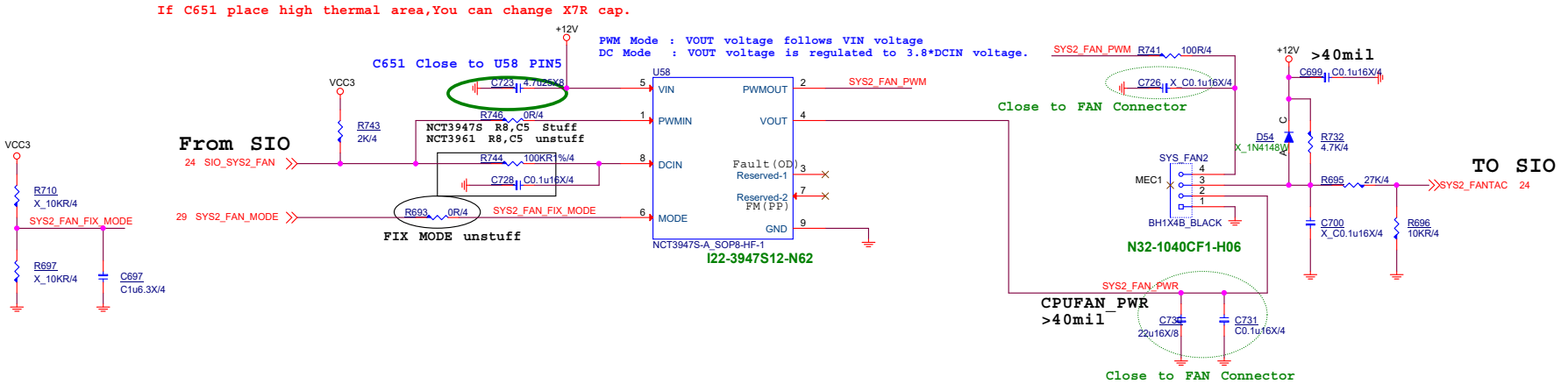
| | | |
|---|---|---|
| Title | CPU FAN1/PUMP FAN1 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 27 of 70 | |

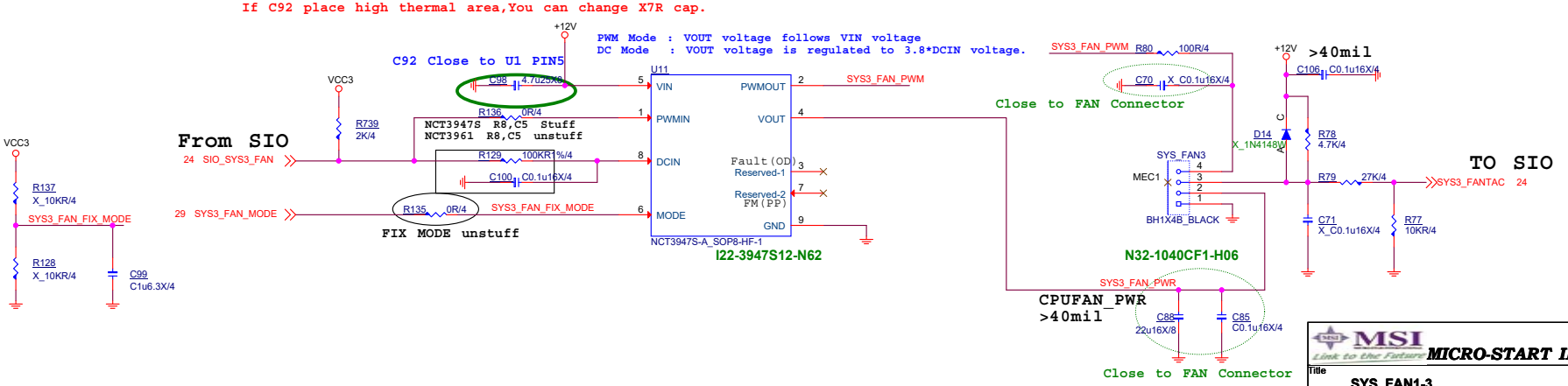
# SYSFAN

## TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

### 1.Mode GPIO BIOS can swtich PWM/DC MODE




MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
| Title | SYS_FAN1-3 | |
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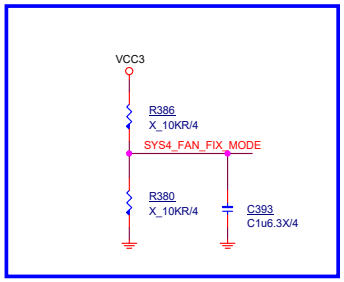
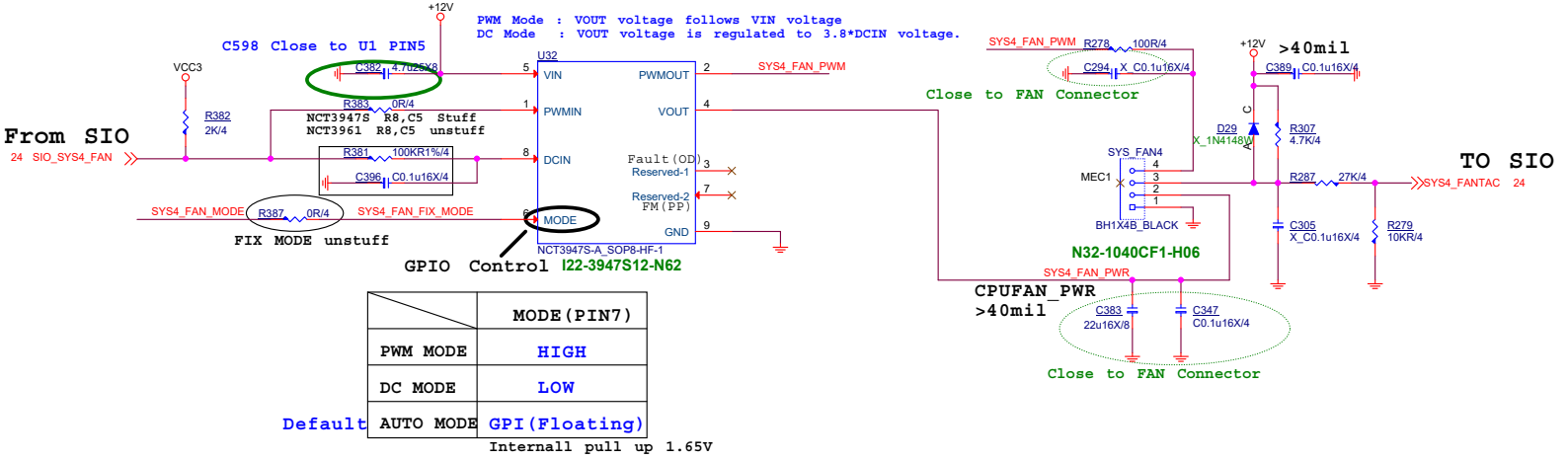
# SYSFAN 4

## TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area,You can change X7R cap.

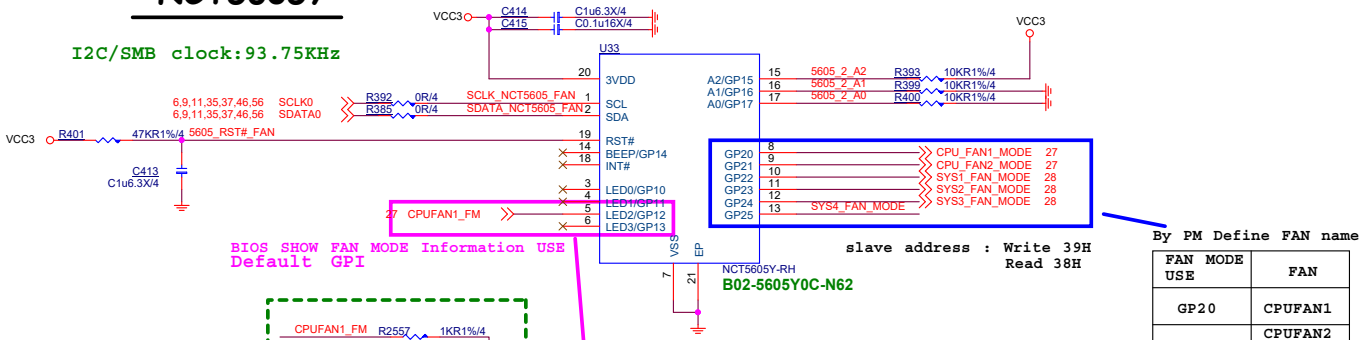



| | MODE(PIN7) |
|---|---|
| PWM MODE | HIGH |
| DC MODE | LOW |
| Default AUTO MODE | GPI(Floating) |

Internall pull up 1.65V

## NCT5605Y




By PM Define FAN name

| SHOW FAN MODE USE | FAN |
|---|---|
| GP12 | CPUFAN1 |
| GP13 | CPUFAN2 PUMPFAN |

By PM Define FAN name

| FAN MODE USE | FAN |
|---|---|
| GP20 | CPUFAN1 |
| GP21 | CPUFAN2 PUMPFAN |
| GP22 | SYSFAN1 |
| GP23 | SYSFAN2 |
| GP24 | SYSFAN3 |
| GP25 | SYSFAN4 |

## 1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

| 0 | 0 | 1 | 1 | A2 | A1 | A0 | R/W |
|---|---|---|---|---|---|---|---|

0 = Write, 1 = Read

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Title: SYS_FAN4/NCT5605Y

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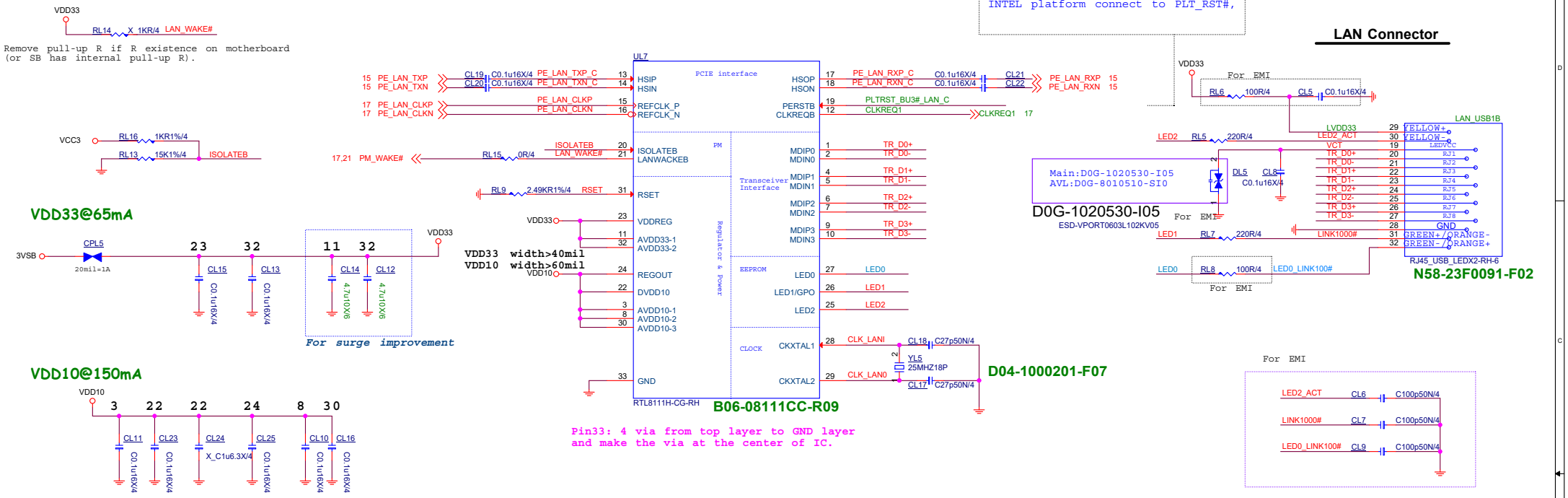
# RTL8111H Giga LAN




**8111H POWER Consumption**

| | 3.3V @ mA | mW |
|---|---|---|
| 10 M Idle/TxRx | 9.9/84.69 | 32.67/279.48 |
| 100 M Idle/TxRx | 48.11/92.44 | 158.76/305.05 |
| Giga Idle/TxRx | 124.5/177.57 | 410.85/585.98 |
| ALDPS | 5.50 | 18.15 |

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| | | |
|---|---|---|
| Title | LAN 8111H | |
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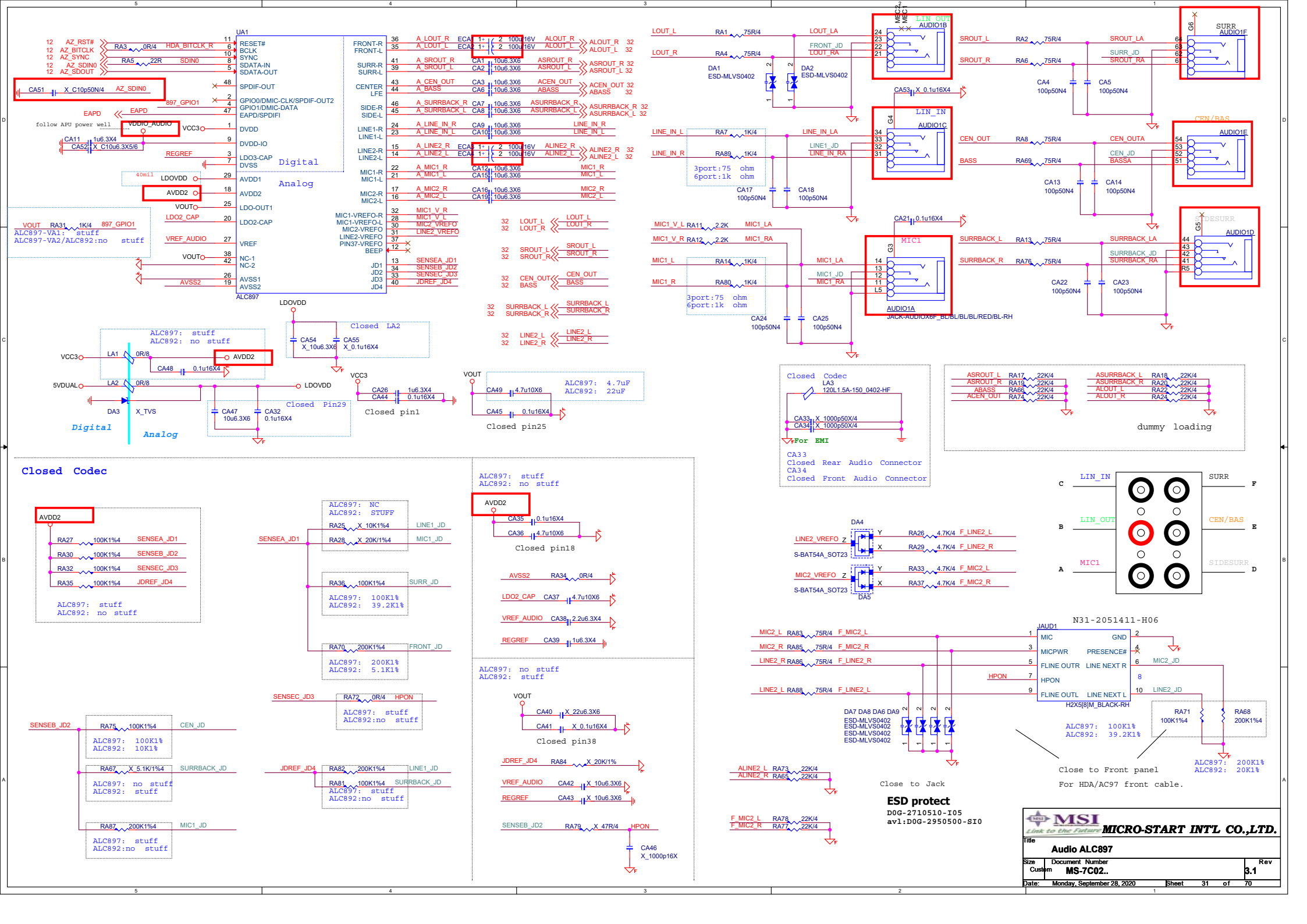
UA1
ALC897
Digital
Analog
AZ_RST#
AZ_BITCLK
AZ_SYNC
AZ_SDIN0
AZ_SDOUT
SDIN0
EAPD
follow APU power well
VDDIO_AUDIO
VCC3
LDOVDD
AVDD2
VOUT
REGREF
LDO2_CAP
VREF_AUDIO
5VDUAL
DA3
X_TVS
ALC897: stuff
ALC892: no stuff
Closed LA2
Closed Pin29
Closed pin1
Closed pin25
ALC897: 4.7uF
ALC892: 22uF
Closed Codec
LA3
120L1.5A-150_0402-HF
For EMI
CA33
Closed Rear Audio Connector
CA34
Closed Front Audio Connector
dummy loading
LIN_OUT
AUDIO1B
LIN_IN
AUDIO1C
MIC1
AUDIO1A
JACK-AUDIOX6F_BL/BL/BL/RED/BL-RH
SURR
AUDIO1F
CEN/BAS
AUDIO1E
SIDESURR
AUDIO1D
3port:75 ohm
6port:1k ohm
ESD-MLVS0402
S-BAT54A_SOT23
N31-2051411-H06
JAUD1
H2X5[8]M_BLACK-RH
Close to Front panel
For HDA/AC97 front cable.
Close to Jack
ESD protect
D0G-2710510-I05
avl:D0G-2950500-SI0
MICRO-START INTL CO.,LTD.
Audio ALC897
MS-7C02..
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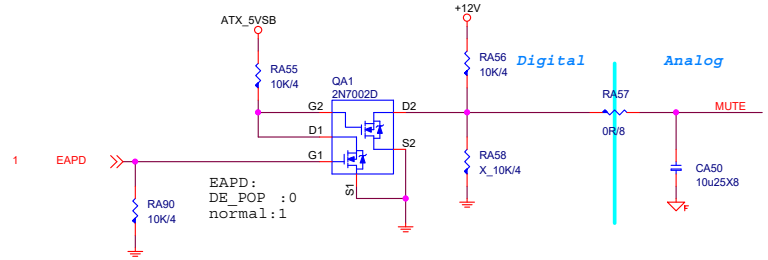
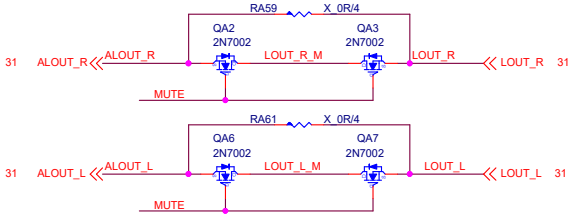
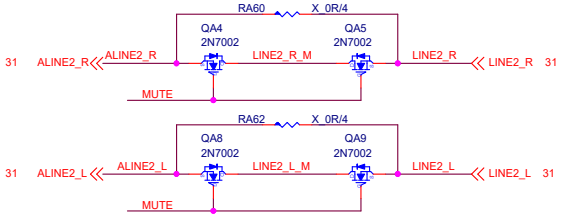
## De-POP circuit



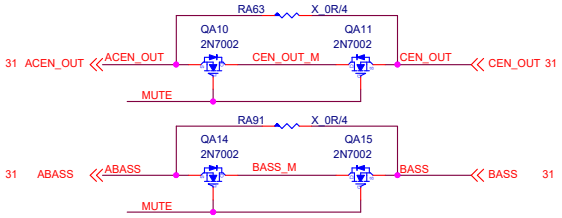



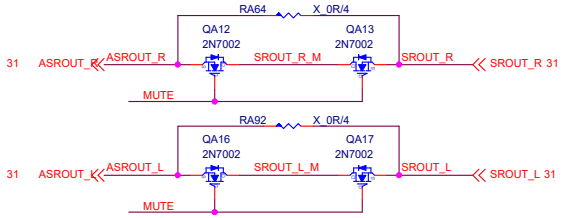









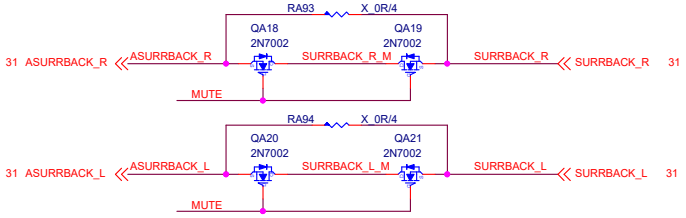







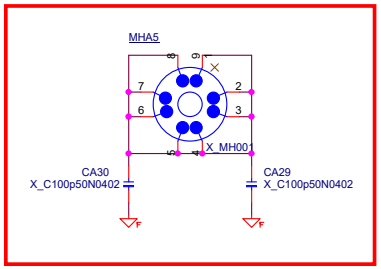


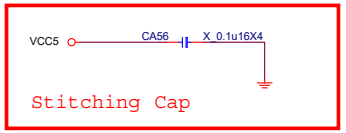




## History:

2020/8/17
1.add RA69/RA70
2.RA17-->RA24 ,RA49,RA50 : connect prior to de-pop side

2020/9/01
1.add RA71

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| | | |
|---|---|---|
| Title | Audio De-POP | |
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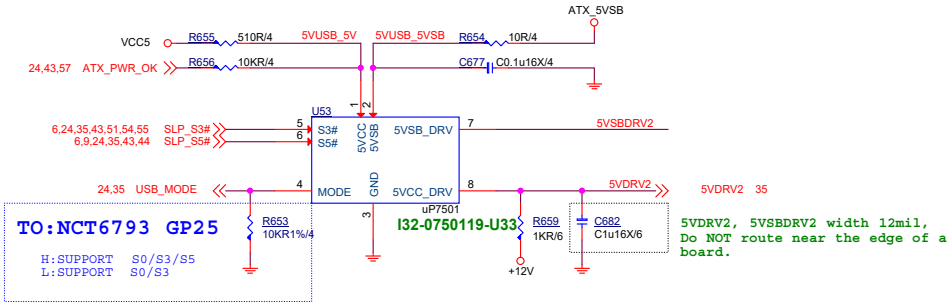
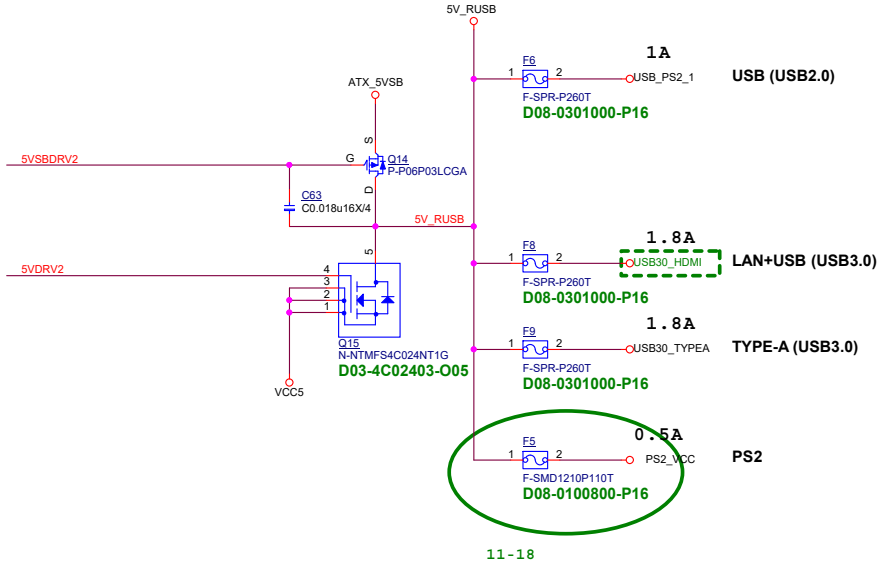
# USB Power

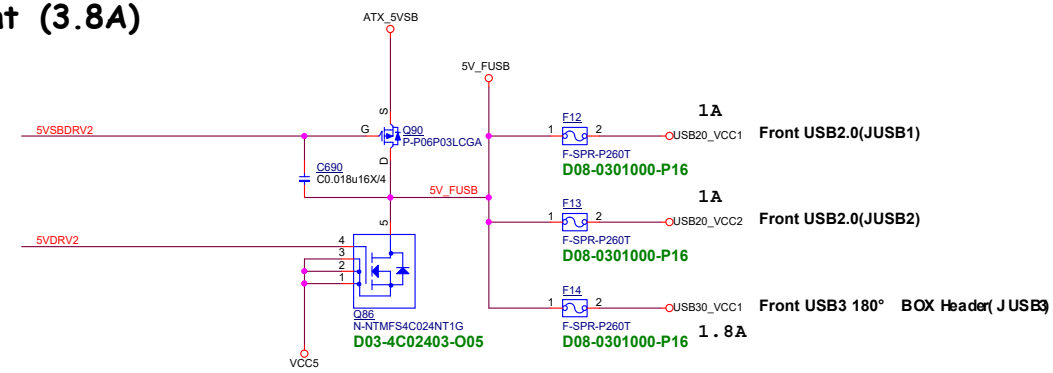



## Rear (8.1A)

---

## Front (3.8A)

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| | | |
|---|---|---|
| Title | USB Power | |
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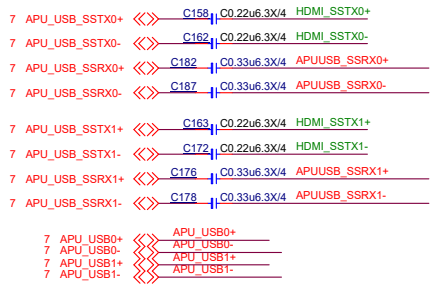
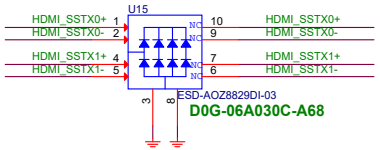
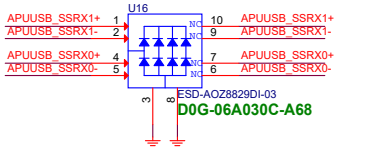
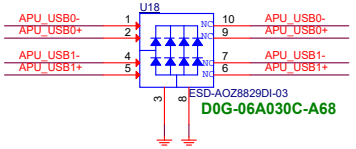
# HDMI+USB (USB3.0)

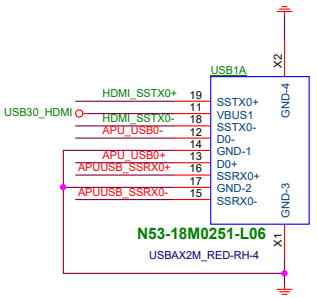
5V@1A

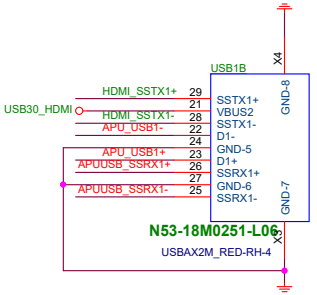


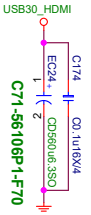



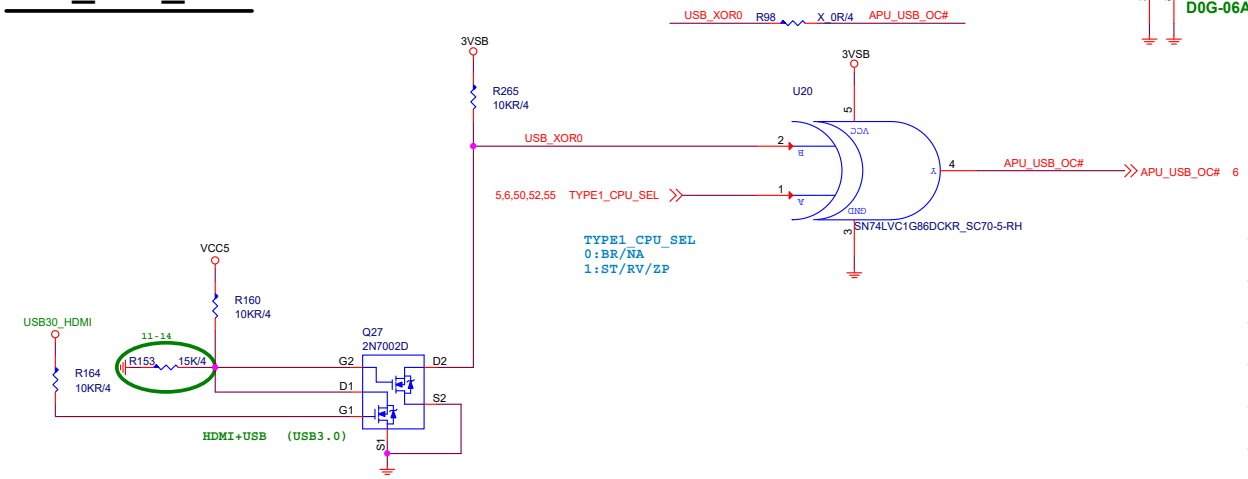




## APU_USB_OC




| | CORETYPE1(A) | USB_PWR(B) | APU_USB_OC(Y) |
|---|---|---|---|
| BR | 0 | 0 | 0 |
| Act. Low | 0 | 1 | 1 |
| SR | 1 | 0 | 1 |
| Act. High | 1 | 1 | 0 |

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Title: Rear LAN_USB3.0

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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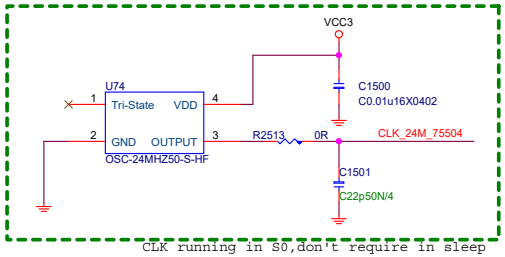
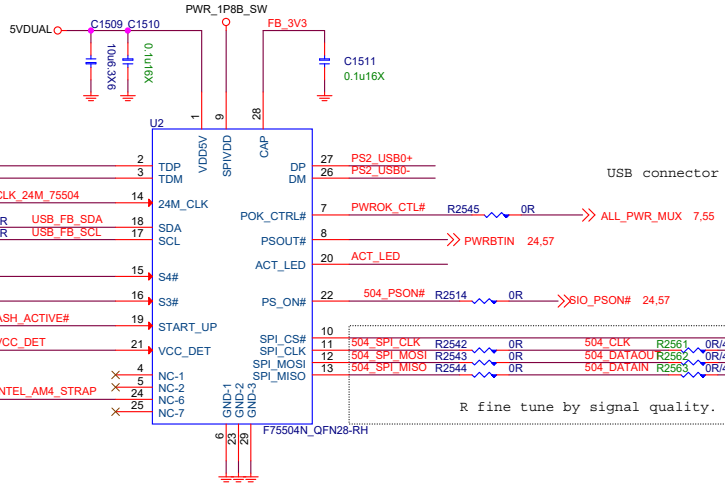
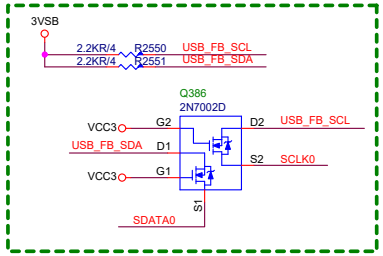
# PS2+USB Flash BIOS (USB2.0)

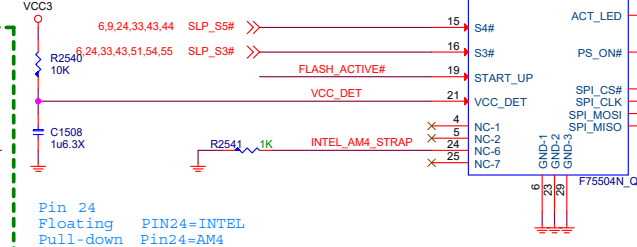



CLK running in S0,don't require in sleep

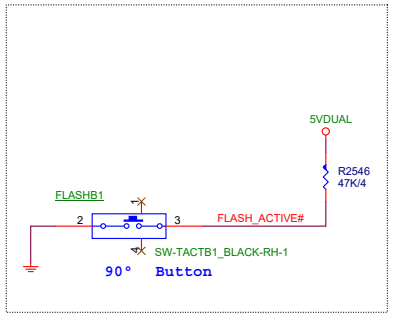
**F75504 layout placement must meet to spi/usb trace length spec with host.**
**As for as possible place near to host.**

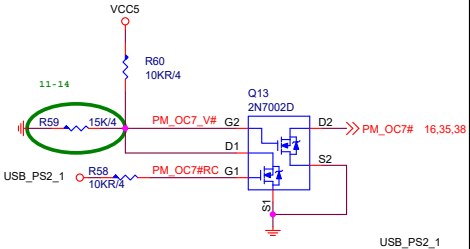


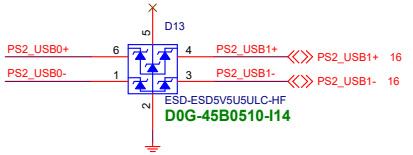



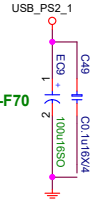



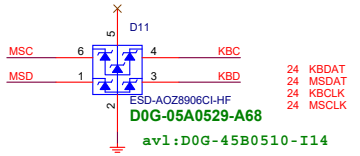

Pin 24
Floating PIN24=INTEL
Pull-down Pin24=AM4

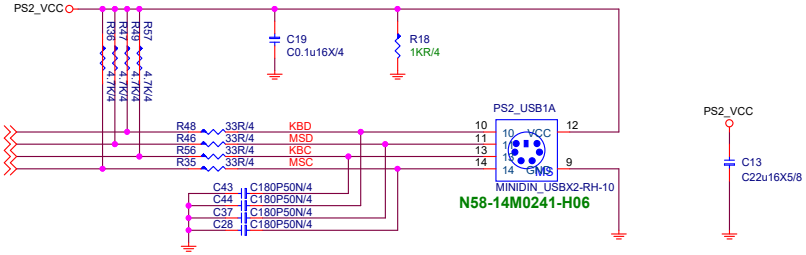


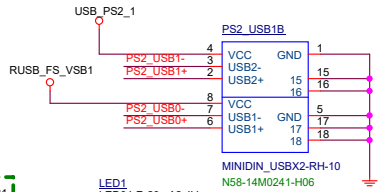



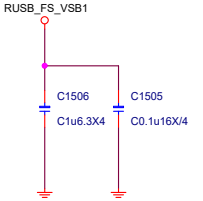



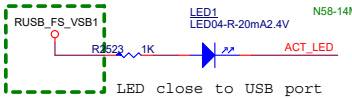



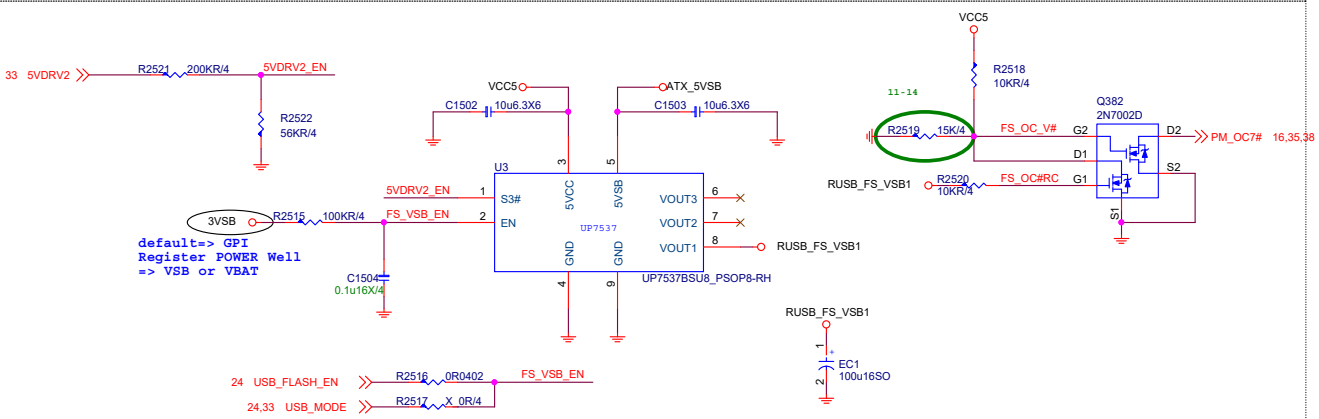

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch




LED close to USB port




default=> GPI
Register POWER Well
=> VSB or VBAT

| MICRO-STAR INT'L CO.,LTD | | |
|---|---|---|
| MS-7C02.. | | |
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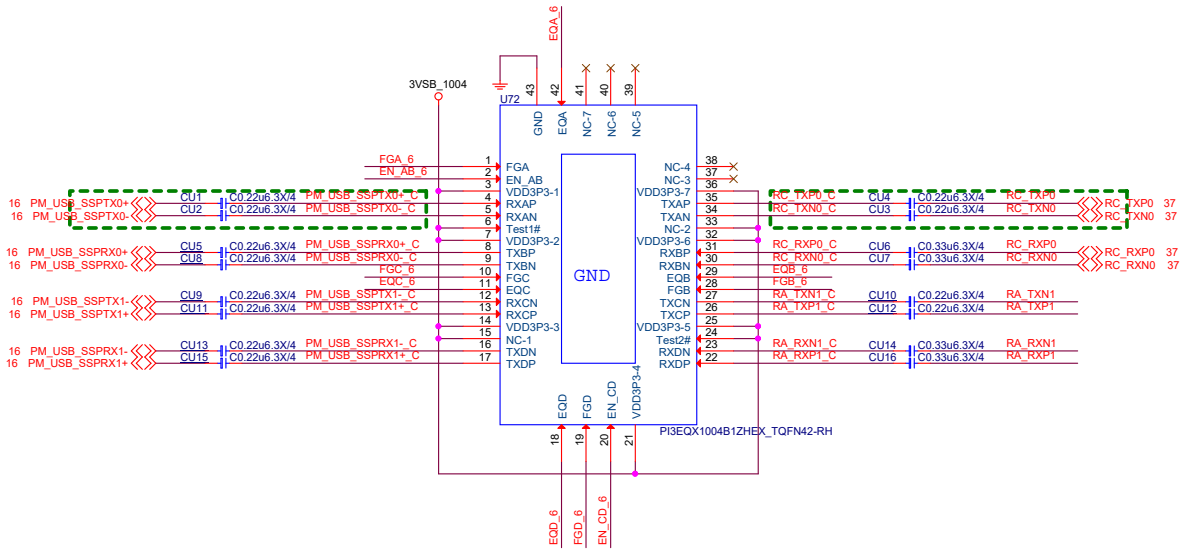
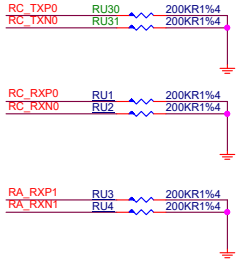
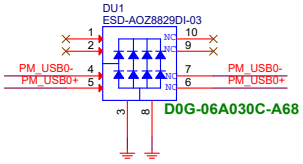
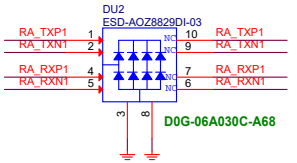
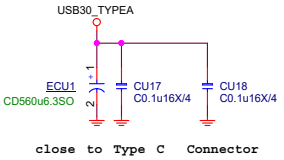
# TYPE-A PI3EQX1004 Redriver

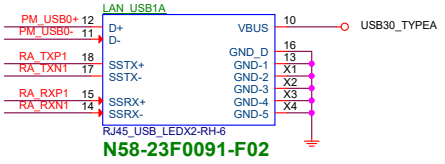


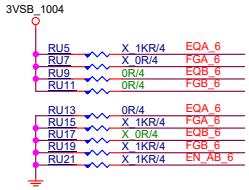


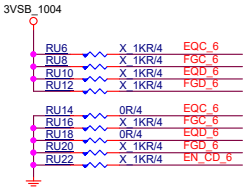



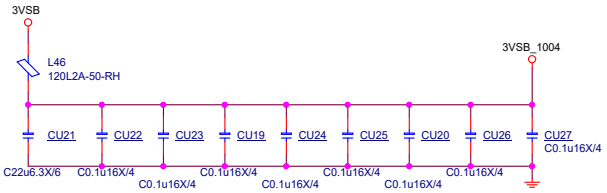



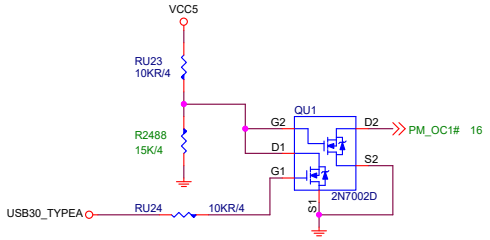




| EQ | dB | |
|---|---|---|
| 0 | 10.9 | 0 to GND |
| R | 6.7 | 68K to GND |
| F | 8.9 | NC |
| 1 | 13.1 | 0 to VDD |

| FG | dB | |
|---|---|---|
| 0 | -3 | 0 to GND |
| R | -1.5 | 68K to GND |
| F | 0 | NC |
| 1 | 2 | 0 to VDD |

MSI MICRO-START INTL CO.,LTD.

Title: Rear USB3.1 Type A / redrive

| Size | Document Number | Rev |
|---|---|---|
| Custom | MS-7C02.. | 3.1 |

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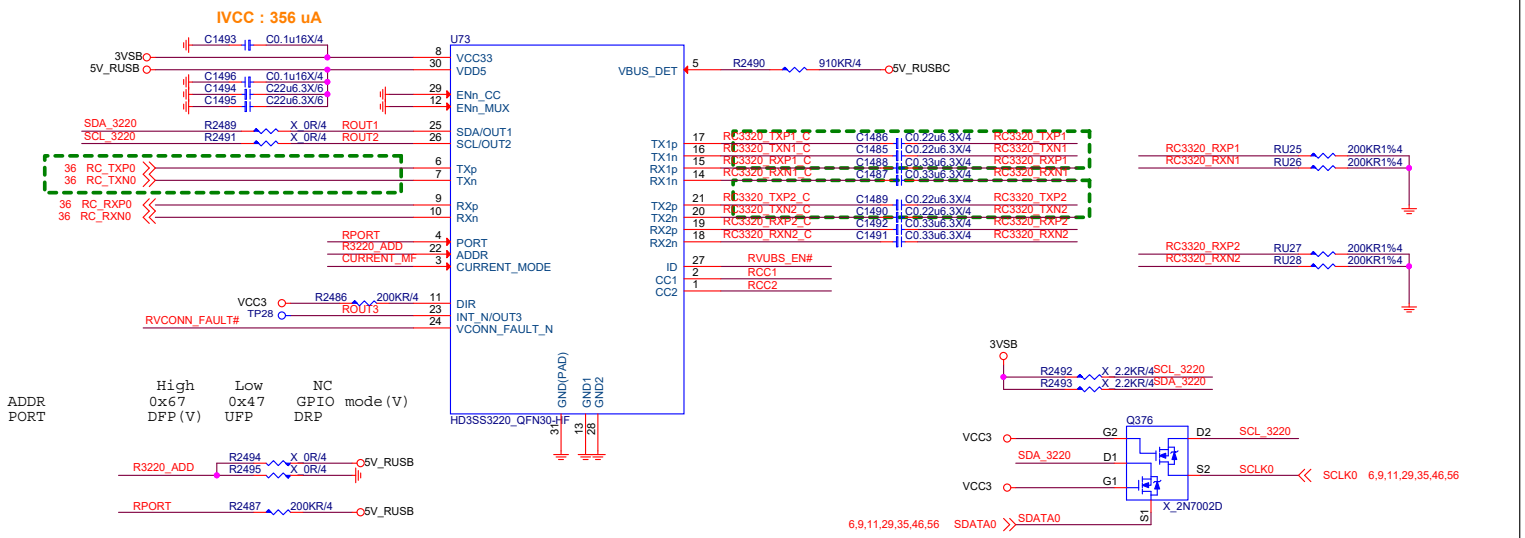
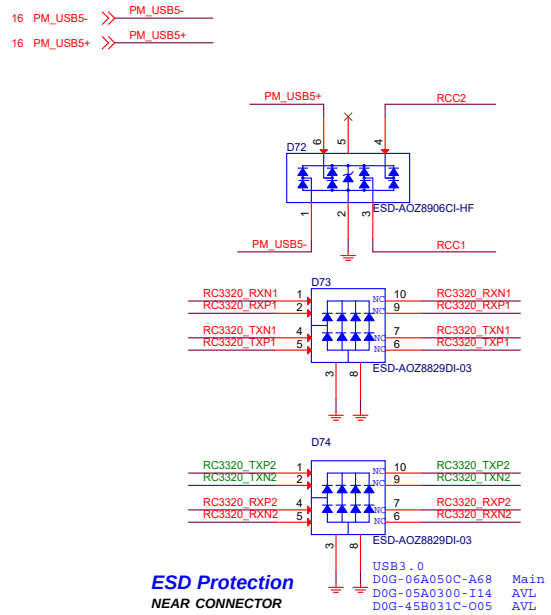
# USB 3.1-Type-C

## USB Type-C MUX with Configuration Channel (CC)

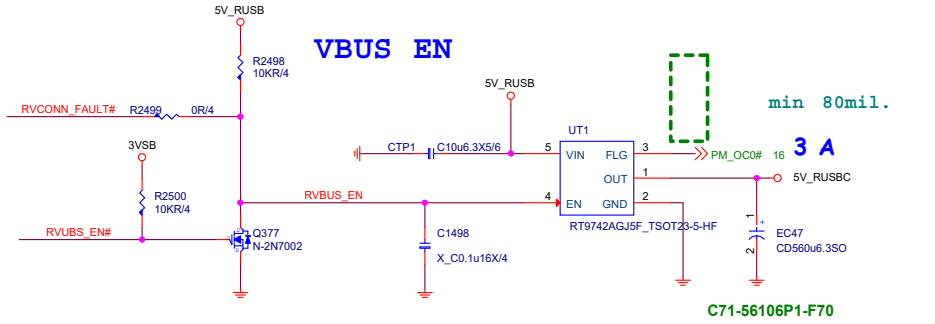


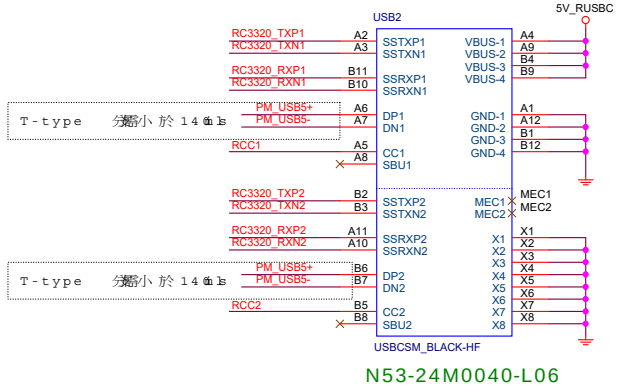




## VBUS OC# LEVEL SHIFT

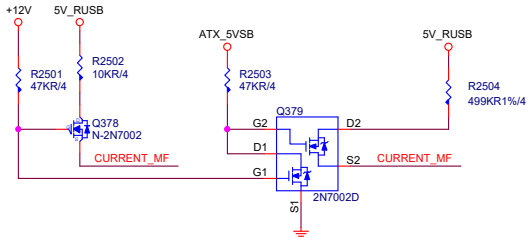
## VCOM OC#

## VBUS EN




## Current Mode




MSI MICRO-START INTL CO.,LTD.

Title: Front USB3.0 90° Header

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

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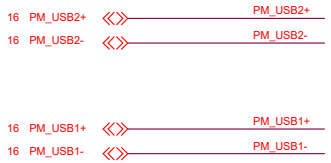
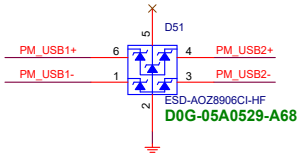
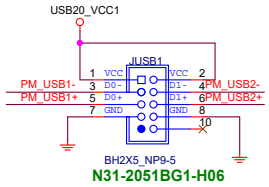
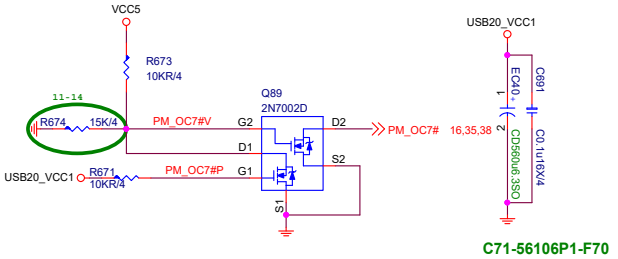
# Front USB2.0(JUSB1)

5V@1A



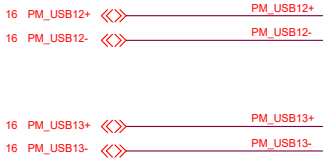



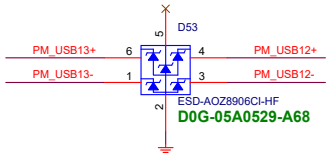



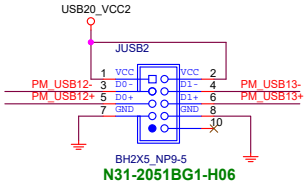



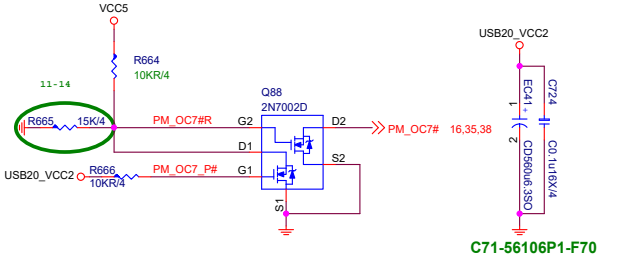

# Front USB2.0(JUSB2)

5V@1A

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| | | |
|---|---|---|
| Title: Front USB2.0 | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 38 of 70 | |

## Front USB3 180° BOX Header( JUSB4)

5V@1.8A

16 PM_USB_SSTX0+ — C695 C0.22u6.3X/4 — PM_SSTX0+
16 PM_USB_SSTX0- — C694 C0.22u6.3X/4 — PM_SSTX0-

16 PM_USB_SSRX0+ — C693 C0.33u6.3X/4 — PMUSB_SSRX0+
16 PM_USB_SSRX0- — C692 C0.33u6.3X/4 — PMUSB_SSRX0-

16 PM_USB10+ — PM_USB10+
16 PM_USB10- — PM_USB10-

16 PM_USB11+ — PM_USB11+
16 PM_USB11- — PM_USB11-

16 PM_USB_SSTX1+ — C689 C0.22u6.3X/4 — PM_SSTX1+
16 PM_USB_SSTX1- — C688 C0.22u6.3X/4 — PM_SSTX1-

16 PM_USB_SSRX1+ — C687 C0.33u6.3X/4 — PMUSB_SSRX1+
16 PM_USB_SSRX1- — C686 C0.33u6.3X/4 — PMUSB_SSRX1-

U57 ESD-AOZ8829DI-03
PM_SSTX0- 1 / PM_SSTX0+ 2 — 10 PM_SSTX0- / 9 PM_SSTX0+
PM_SSTX1- 4 / PM_SSTX1+ 5 — 7 PM_SSTX1- / 6 PM_SSTX1+
3, 8
D0G-06A030C-A68

D56
PM_USB10- 1 / PM_USB10+ 2 — 10 PM_USB10- / 9 PM_USB10+
PM_USB11- 4 / PM_USB11+ 5 — 7 PM_USB11- / 6 PM_USB11+
ESD-AOZ8829DI-03
D0G-06A030C-A68

U56
PMUSB_SSRX0- 1 / PMUSB_SSRX0+ 2 — 10 PMUSB_SSRX0- / 9 PMUSB_SSRX0+
PMUSB_SSRX1- 4 / PMUSB_SSRX1+ 5 — 7 PMUSB_SSRX1- / 6 PMUSB_SSRX1+
ESD-AOZ8829DI-03
D0G-06A030C-A68

USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL

JUSB3
PM_USB11+ 11 D2+
PM_USB11- 12 D2-
PM_SSTX1+ 14 TX2+
PM_SSTX1- 15 TX2-
PMUSB_SSRX1+ 17 RX2+
PMUSB_SSRX1- 18 RX2-
USB30_VCC1 19 VBUS2
16 GND
13 GND
PM_USB10+ 9 D1+
PM_USB10- 8 D1-
PM_SSTX0+ 6 TX1+
PM_SSTX0- 5 TX1-
PMUSB_SSRX0+ 3 RX1+
PMUSB_SSRX0- 2 RX1-
7 GND
USB30_VCC1 1 VBUS1
4 GND
10 NC
2X10_CONNECTOR
BH2X10[20]-2PITCH_BLACK-RH-1

VCC5 11-14
R667 10KR/4
11-14
R668 15K/4 — PM_OC2#R — Q87 2N7002D G2 D2 — PM_OC2# 16
D1
USB30_VCC1 — R669 10KR/4 — PM_OC2#V — G1 S2
S1

USB30_VCC1
EC442 1 / 2 CD560-6.3SO
C2725
C0.1u16X4
C71-56106P1-F70

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| | | |
|---|---|---|
| Title | Front USB3.0 180° Header | |
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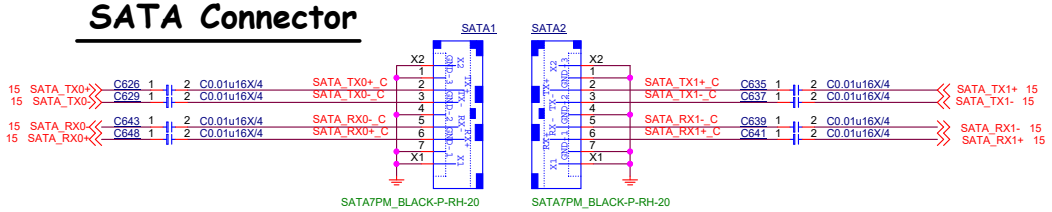
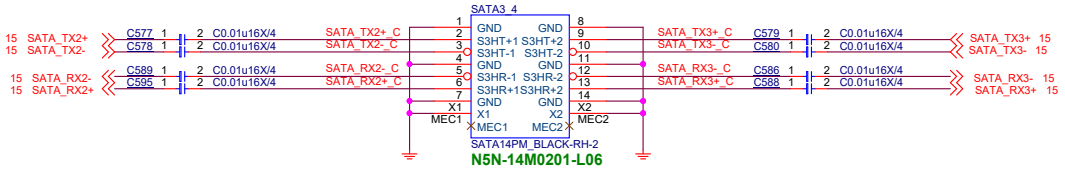
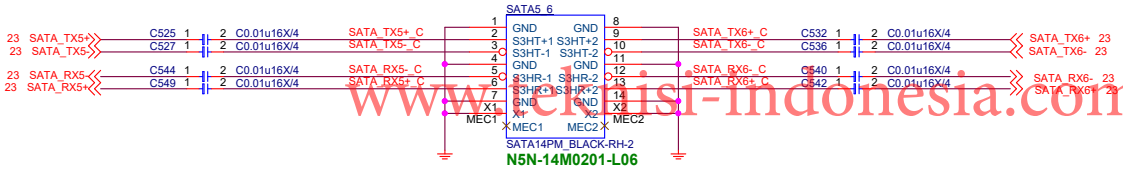
# SATA Connector




www.elektronisi-indonesia.com

| Schematic Cfg | Project | |
|---|---|---|
| CFG-7C02-***-Arsenal Gaming | V | A |
| | | |
| | | |

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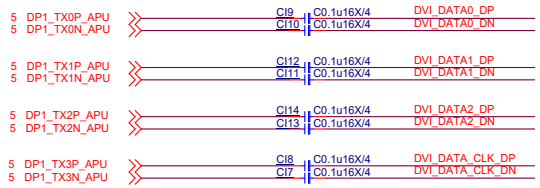
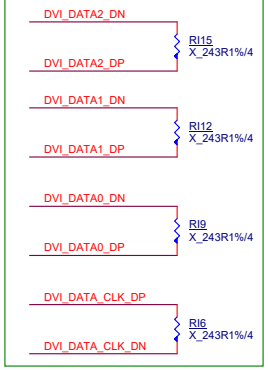
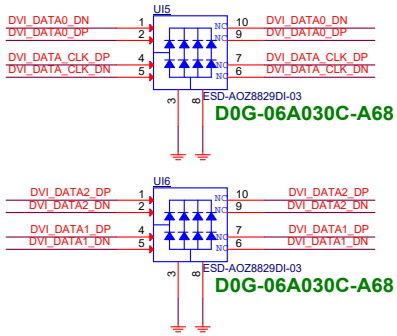
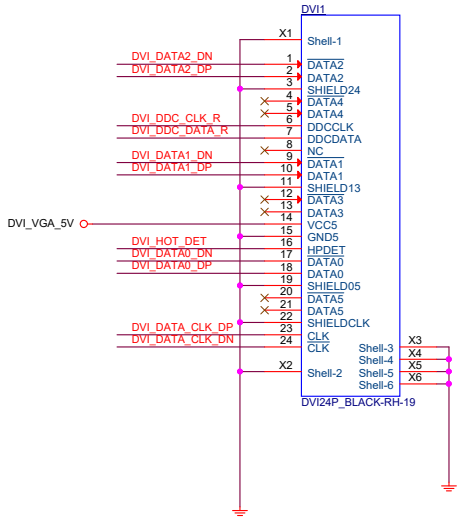
# DVI CONNECTOR

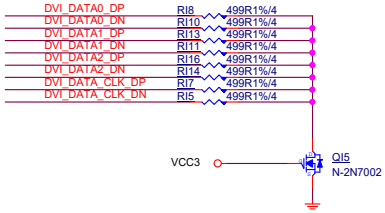



## For EMI

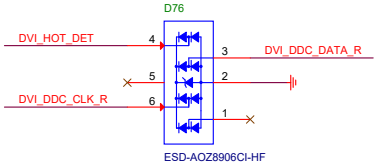


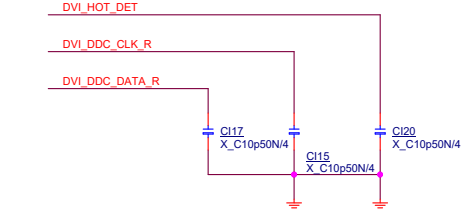




## 注意耐壓V零件

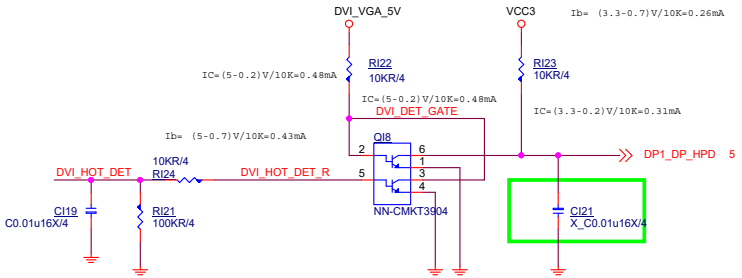


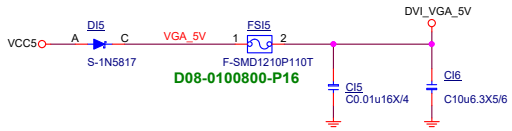

180427 10pin改6pin

## For EMI

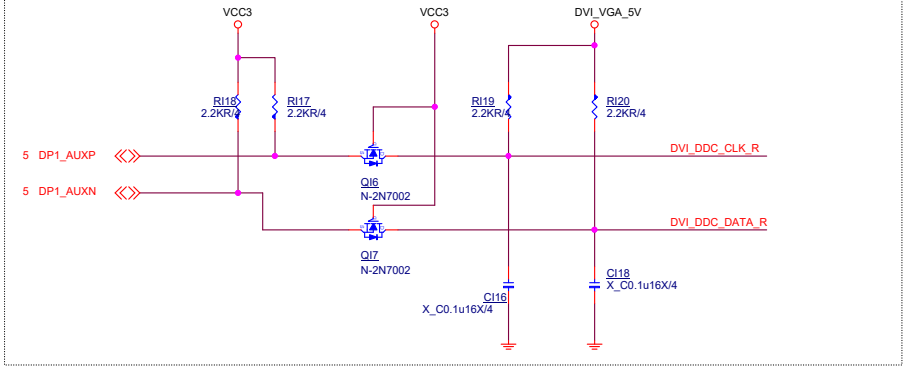



## HPD




## LEVEL SHIFT using I2C Repeater

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| | | |
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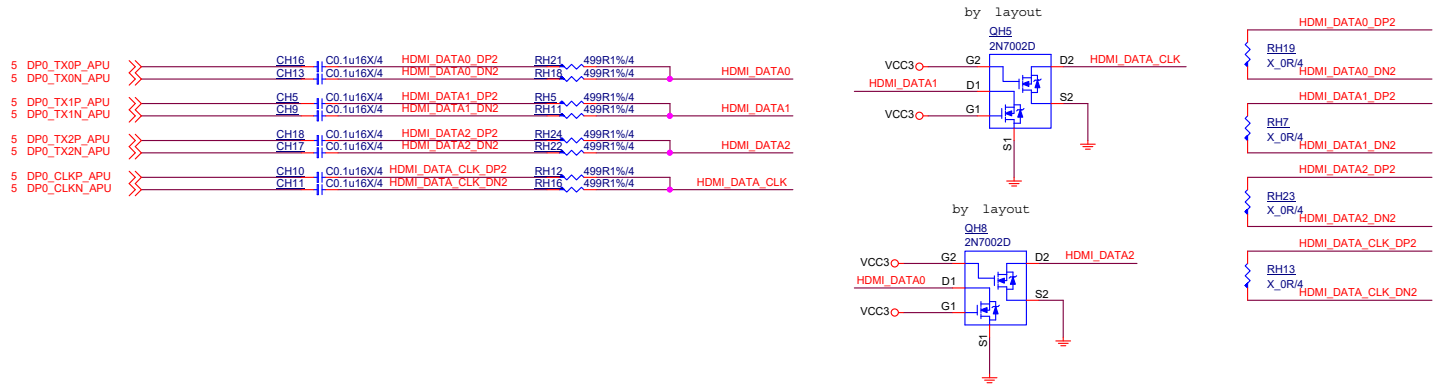
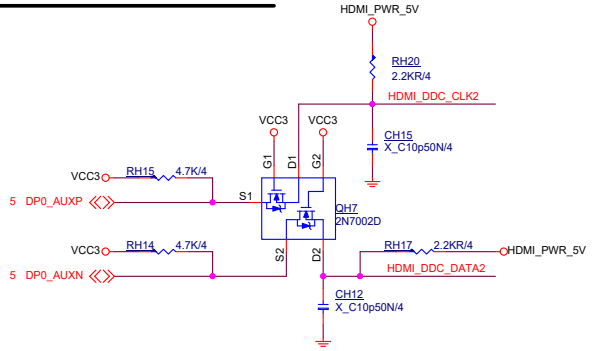
# HDMI CONNECTOR

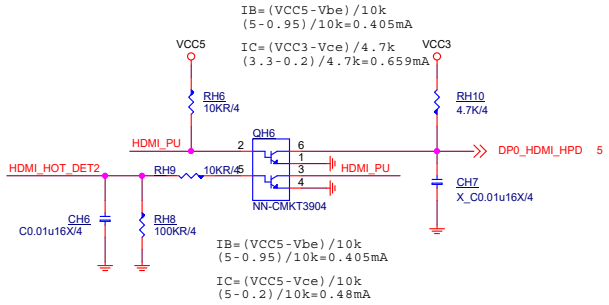
For HDMI 1.4



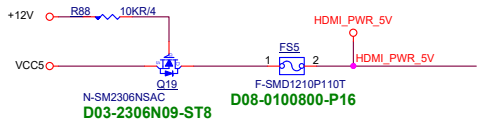

# AUX Level Shifter




# HPD Circuit

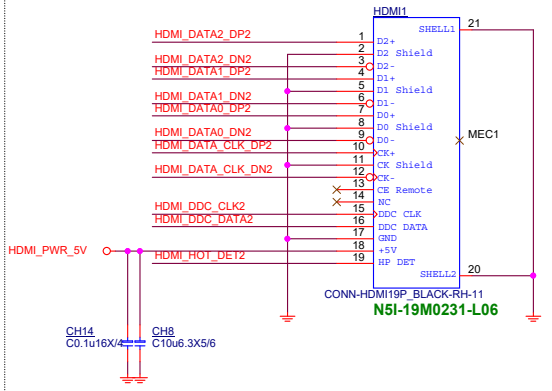



# Connector Power

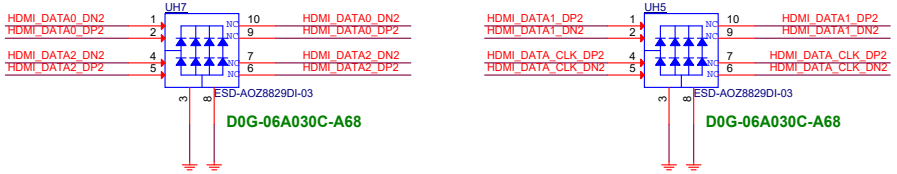



如果用 DIO DE 為防護電壓會不過

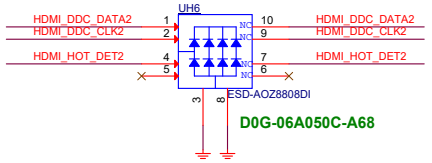
# Connector




# For EMI




注意耐壓V零件

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| | | |
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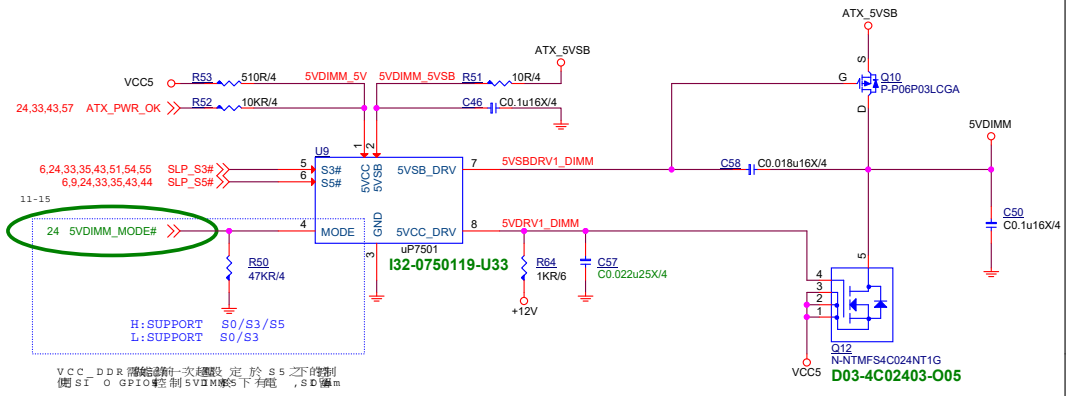
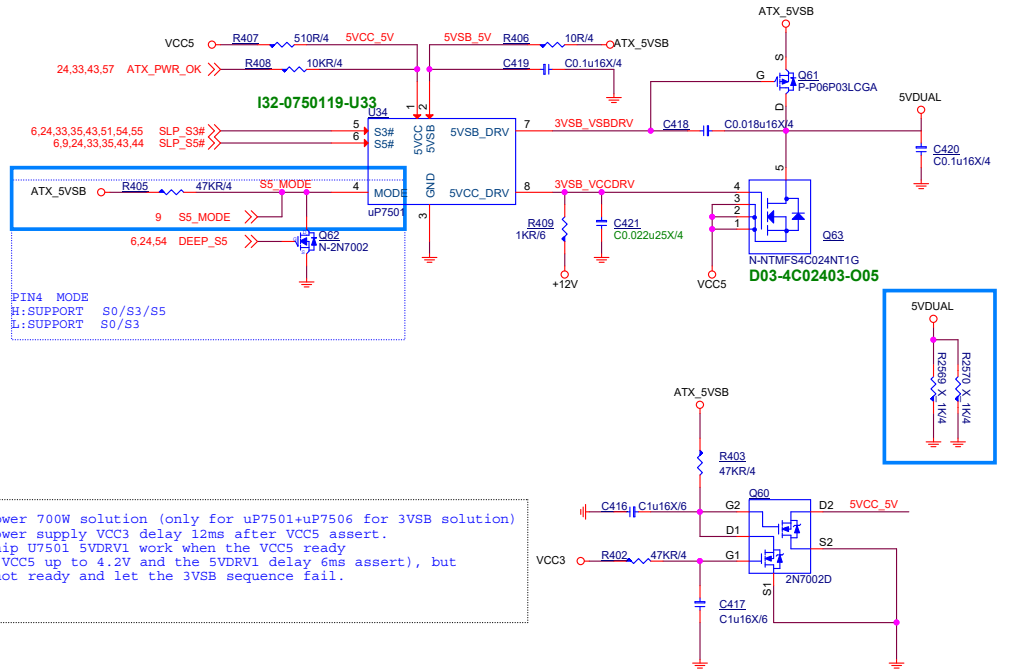
# 5VDIMM FOR DDR




# 5VDUAL For 3VSB、CPU 1.8V、 VDDP

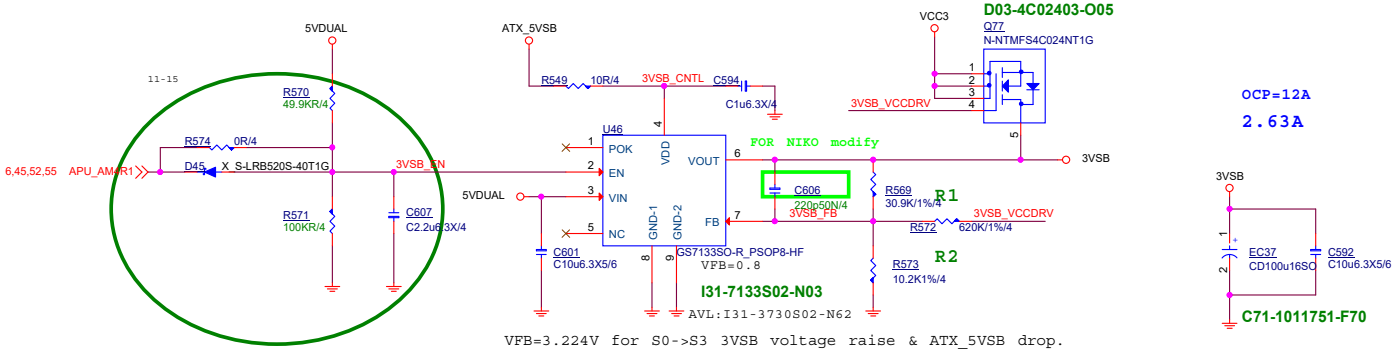



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

# 3VSB cost down

**3.3V@2.63A**

*1.05V@0.05A*
*VDDBT_RTC_G@4.5uA*
*FCH@0.07A*
*CPU@0.25A*
*PCIE*6 @2.25A*




VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(30.9K/10.2K))
= 3.22V

OCP=12A
2.63A

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| | | |
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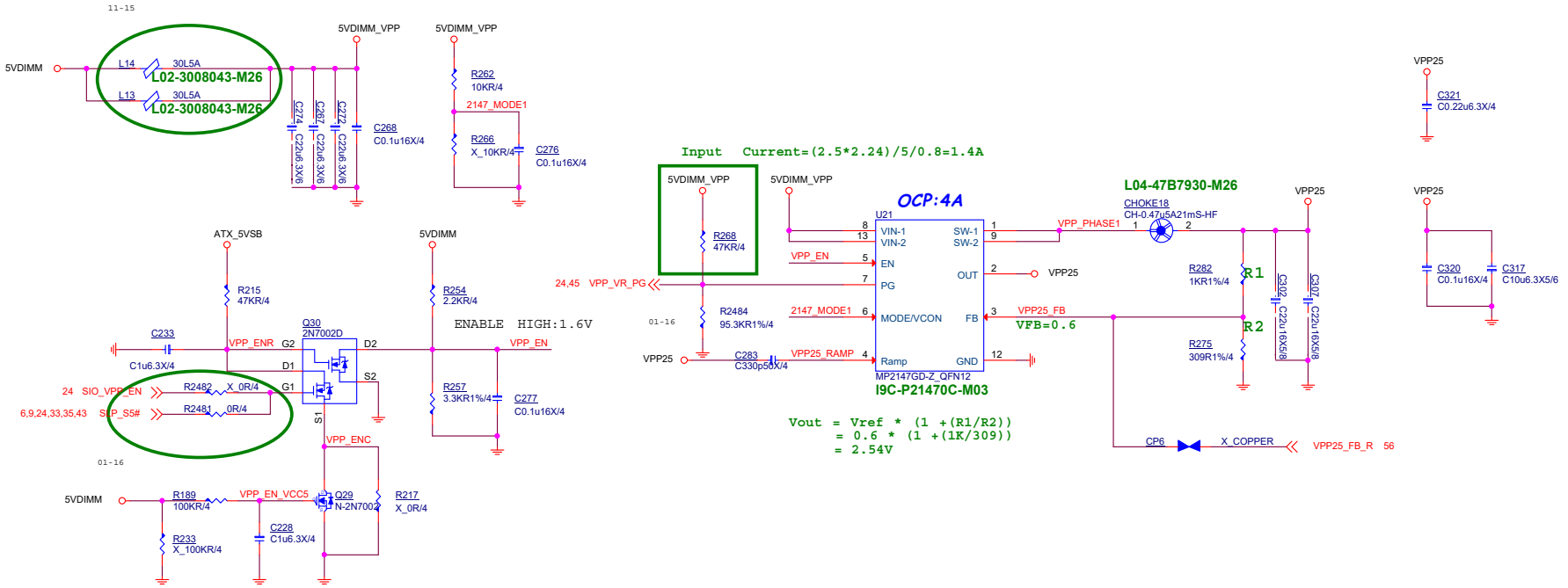
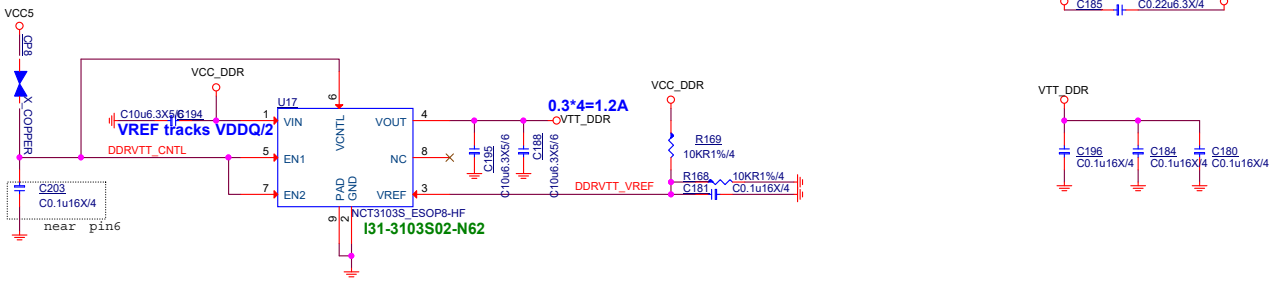
# 4DIMM : VPP25

## 2.5V@2.24A




## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

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| | | |
|---|---|---|
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# DDR4_1.2V@26.2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

5VDIMM
R142 X_2.2KR/4 EN:VIH2.4V
DDR_EN
R143 X_3.3KR1%/4
C122 X_C0.1u16X/4

6,43,52,55 APU_AM4R1 >> D34 S-LRB520S-40T1G DDR_EN
24 SIO_VDDQ_EN >> R372 X_0R/4 DDR_EN 3.12V
24,44 VPP_VR_PG >> R2483 0R/4

EN:VIH2.4V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

Follow CRB
20180410
5VDIMM
R134 47K/4
EN:VIH1.6V
EN pin Maximum:6.5V

5VDIMM
R130 10R/8
DDR_VCC C97 4.7u10X/6

OCP=35A

51,55 DDR_PWRGD
DDR_EN
DDR_REFOUT
DDR_REFIN

U12
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
DDR_BOOT1
DDR_PH1
DDR_UG1
DDR_LG1
DDR_FB
R121 0R/4 DDR_BOOT1_R C92 C0.1u16X/4
FB:0.8V
RT8125EGQW_WDFN10-HF
I32-8125E0C-R11

20180410
C1507 C0.22u6.3X/4
C115 C1000p50X/4
R140 665R1%/4
C114 C1000p50X/4

VCC_DDR
close to DIMM side
R138 10R/4
R1
10KR1%/4
R139
DDR_VSENP R144 0R/4 VDDIO_MEM_S3_SENSE 6
C116 X_C0.1u16X/4
R2
R145 19.1K1%/4

Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/19.1K))
= 1.218V

56 DDR_OV
CP7 X_COPPER

Input Current=(26.2*1.2)/5/0.8=7.86A

L04-12A7811-T15
CHOKE8 CH-1.2u15A2m-HF
5VDUAL_IN_DDR
5VDIMM
C68 C1u16X/6
C61 C10u6.3X5/6
EC10 CD560u6.3SO
EC11 CD560u6.3SO
C117 C0.1u16X/4
C71-56106P1-F70
C71-56106P1-F70

DDR_UG1
R81 0R/6 DDR_UG1_R
Q16
Q17
N-NTMFS4C029NT1G
D03-4C02903-O05
N-NTMFS4C029NT1G
D03-4C02903-O05
R83 X_10KR/4

L04-47B7981-T15
CHOKE12 CH-0.47u42A0.81m-HF
DDR_PH1
VCC_DDR

DDR_LG1
20180702
R97 7.87KR1%/4
Rocpset
Q21
Q22
N-NTMFS4C024NT1G
D03-4C02403-O05
N-NTMFS4C024NT1G
D03-4C02403-O05
R112 2.2R/8
snubber
C82 C3300p50X/4
C112 C1u6.3X/4
C91 C22u6.3X/6
EC22 CD560u6.3SO
EC19 CD560u6.3SO
EC25 CD560u6.3SO
C71-56106P1-F70
C71-56106P1-F70
C71-56106P1-F70

20180517 Rocpset:7.15K
OCP=Rocset*10uA/Rdson(Low side)
=7.15K*10uA/1.65~2mohm
=43.33A~35.75A
(really:35.76A)

20180702 Rocpset:7.87K
OCP=Rocset*10uA/Rdson(Low side)
=7.87K*10uA/1.65~2mohm
=47.697A~39.35A
(really:38.4A)

VCC_DDR
EC29 CD560u6.3SO
EC17 CD560u6.3SO
C71-56106P1-F70
C71-56106P1-F70

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VCORE: ICCMax 140A
OCP: 200A

SOC: ICCMax 75A
OCP: 90A

CPU_1P8

design check

(6) APU_SVC — VR44 X_R/2 — VRM_SVC
(6) APU_SVD — VR43 X_R/2 — VRM_SVD
(6) APU_SVT — VR42 X_R/2 — VRM_SVT
(6) APU_PWROK — VR156 X_R/2 — VRM_POK

VR142 X_1K/4 VR140 X_1K/4 VR141 1K/4 VR4 X_2.2K/4
VR17 X_220R/4 VR143 X_220R/4 VR8 X_220R/4

Note: VID Override Circuit

| SVC | SVD | BOOT VOLTAGE Pre_PWROK Metal VID |
|---|---|---|
| 0 | 0 | 1.1 |
| 0 | 1 | 1.0 |
| 1 | 0 | 0.9 |
| 1 | 1 | 0.8 |

VCC3 VR2 10K/4 VRM_VRDY

JSMB1: SCLK0 1 2 SDATA0, 3, H2X2[4]M_BLACK-RH

VC106 X_22p50N4 SCLK_229004
VC105 X_22p50N4 SDATA_229004

VCC PIN
POR : Rising 2.95V
POR : Falling 2.8V

VCC3 RAA229004_VCC3

Remove colay 3VSB.
Close IC

VR153 X_0R/6 VR155 0R/6
RAA229004_VCC
VC25 1u6.3X4
VC30 0.1u16X4
VCCS
VC27 4.7u10X6 NC

12VIN
VC132 X_0.1u16X4
VC14 0.1u16X4

VU3
15 VINSEN
(57,63) RAA229004_EN — VR12 X_R/2 VRMEN — 11 EN
VRM_POK — 12 PWROK
(57) VRM_VRDY — VR3 X_R/2 VRDY1 — 13 PG0
VR153 X_R/2 VRDY2 — 14 PG1

Condition as TSEN point

(6,27,62) SCLK0 — R2565 X_R/2 SCLK_229004 — 43 PMSCL
(6,27,62) SDATA0 — R2564 X_R/2 SDATA_229004 — 44 PMSDA
RAA229004_VCC — VR30 4.7K/4 SMBALERT_229004 — 42 nPMALERT

CPU_1P8 — VR64 X_0R/4 — VC19 1u6.3X4 — 7 VDDIO
QV2 N-SM2408NSANC-TRG_SOT23N3-HF
VDDIO_EN

VRM_SVC — 10 SVC
VRM_SVD — 8 SVD
VRM_SVT — 9 SVT

SMBUS address:0X60(7 bit)
0XC0(8 bit)

VR147 0R/4 229004_SM_ADDR — 39 ADDR
(6,27) PROCHOT# — VR148 X_R/2 VR_HOT# — 6 nVRHOT
TP3 — 5 CFP

VCORE — VR26 49.9R1%4 — VCP2 X_COPPER — VSEN_CORE — 34 VSEN0
(6,28) VDDCR_CPU_SENSE+
Diff pair
(6) VDDCR_CPU_SENSE- — VCP1 X_COPPER — VRTN_CORE — 33 RGND0
VR25 49.9R1%4
VC20 3300p50X4
Close IC

VCCP_NB — VR149 49.9R1%4 — VCP3 X_COPPER — VSEN_SOC — 37 VSEN1
(6) VDDCR_SOC_SENSE+
Diff pair
(6) VDDCR_SOC_SENSE- — VCP4 X_COPPER — VRTN_SOC — 36 RGND1
VR35 49.9R1%4
VC24 3300p50X4
Close IC

VCORE_TSEN — 35 TEMP0
VGT_TSEN — 38 TEMP1

GND 16 EPAD 49 RAA229004

0603 Size

PWM0 CS0 CSRTN0 — VCORE_ISEN1_R — VR157 2.15KR1%6 — VCORE_PWM1 (50) VCORE_ISEN1 (51)
VC34 C0.22u16X4
VC126 C0.1u16X4 — VCORE_IRTN1 (51)

PWM1 CS1 CSRTN1 — VCORE_ISEN2_R — VR158 2.15KR1%6 — VCORE_PWM2 (50) VCORE_ISEN2 (51)
VC33 C0.22u16X4
VC127 C0.1u16X4 — VCORE_IRTN2 (51)

PWM2 CS2 CSRTN2 — VCORE_ISEN3_R — VR159 2.15KR1%6 — VCORE_PWM3 (50) VCORE_ISEN3 (52)
VC35 C0.22u16X4
VC128 C0.1u16X4 — VCORE_IRTN3 (52)

PWM3 CS3 CSRTN3 — VCORE_ISEN4_R — VR160 2.15KR1%6 — VCORE_PWM4 (50) VCORE_ISEN4 (52)
VC36 C0.22u16X4
VC129 C0.1u16X4 — VCORE_IRTN4 (52)

PWM4 CS4 CSRTN4
PWM5 CS5 CSRTN5

0603 Size

PWM6 CS6 CSRTN6 — VNB_ISEN1_R — VR161 2.15KR1%6 — VCCP_NB_PWM1 (53) VCCP_NB_ISEN1 (53)
VC18 C0.22u16X4
VC130 C0.1u16X4 — VCCP_NB_IRTN1 (53)

PWM7 CS7 CSRTN7 — VNB_ISEN2_R — VR162 2.15KR1%6 — VCCP_NB_PWM2 (53) VCCP_NB_ISEN2 (53)
VC22 C0.22u16X4
VC131 C0.1u16X4 — VCCP_NB_IRTN2 (53)

3VSB VR81 10K/4
12VIN VR80 200K1%4
VQ38 2N7002D: G2 D2 D1 S2 G1 S1
RAA229004_VCC3
VDDIO_EN
VC104 0.1u16X4

I31-7116S09-N03

VCC5 VC17 1u6.3X4
VU4 GS7116S5: VDD VOUT EN GND ADJ
EN:VIH1.6V
VC109 X_0.1u16X4
RAA229004_FB
R1 VR27 10K1%4
R2 VR29 3.16K1%4
VC110 10u6.3X6
RAA229004_VCC3

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

Close to PHASE1 CHOKE
RT8 10KRT1%4
VCORE_TSEN_GND
SP6 X_COPPER
VCORE_TSEN
VR50 22K1%4
VC21 C47p50N4
Close to PWM

Close to PHASE1 CHOKE
RT9 10KRT1%4
VGT_TSEN_GND
SP7 X_COPPER
VGT_TSEN
VR164 22K1%4
VC125 C47p50N4
Close to PWM

MSI MICRO-START INTL CO.,LTD.

| | | | |
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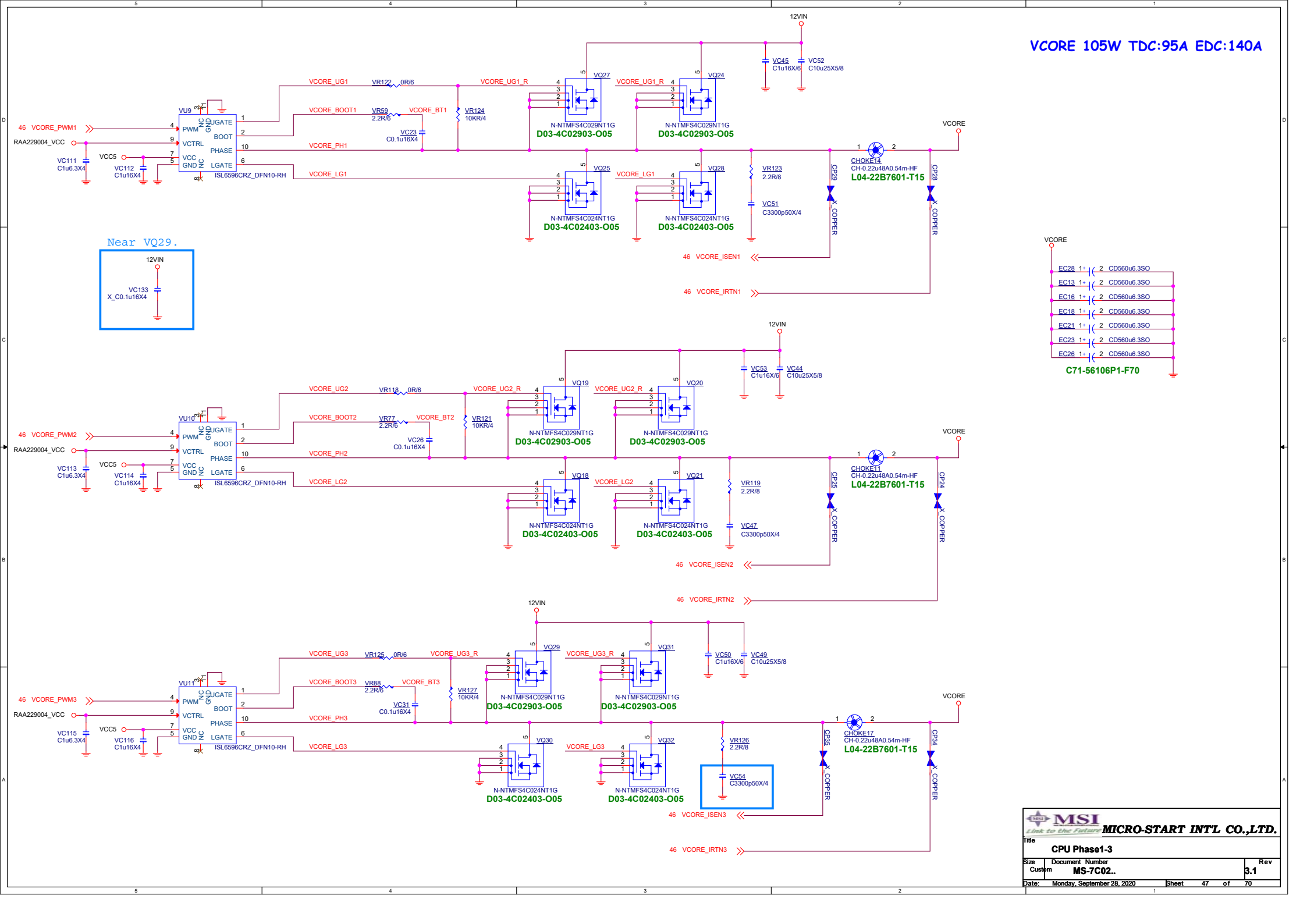
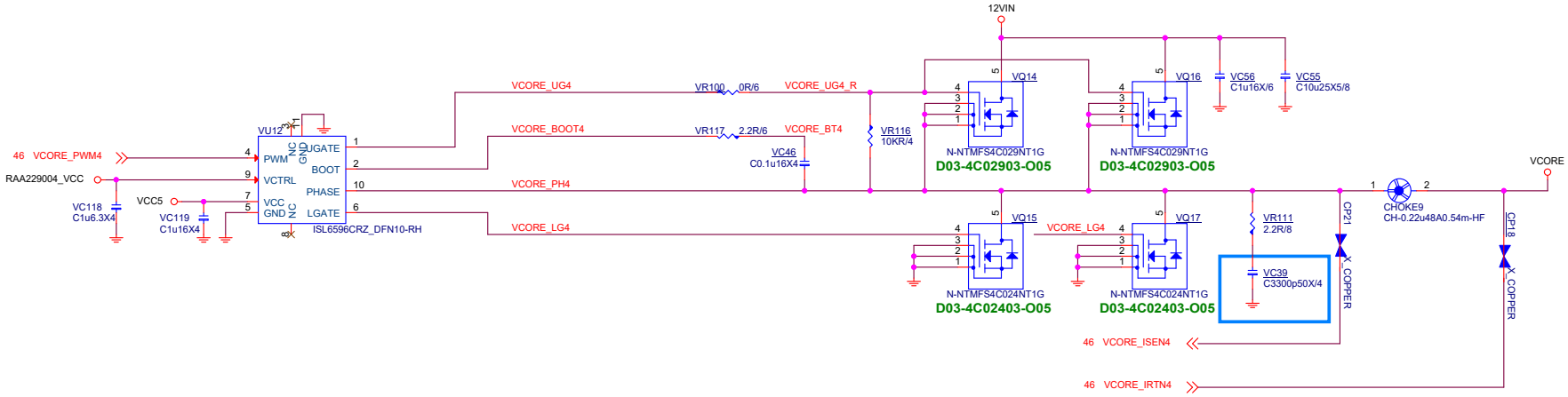
# VCORE 105W TDC:95A EDC:140A




MICRO-START INTL CO.,LTD.

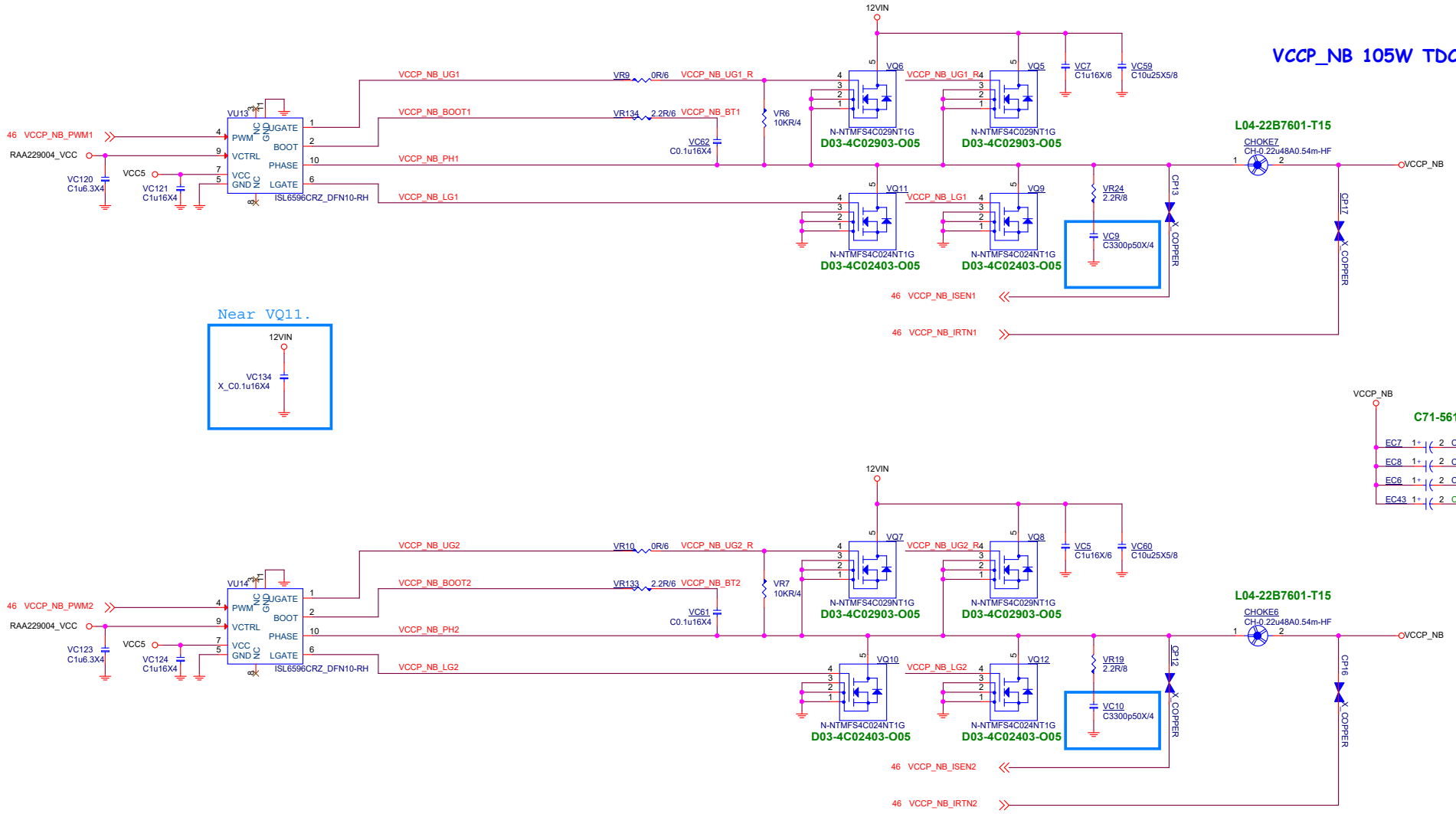
| | | |
|---|---|---|
| Title | CPU Phase1-3 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 47 of 70 | |




MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
| Title | CPU Phase4 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 48 of 70 | |

## VCCP_NB 105W TDC:50A EDC:75A

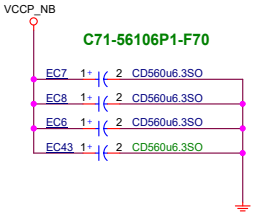



Near VQ11.







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| | | |
|---|---|---|
| Title: CPU NB | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 49 of 70 | |

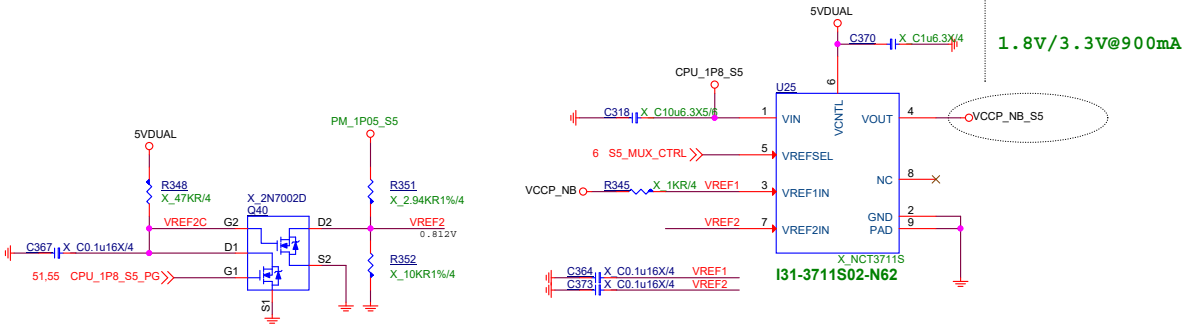
# FOR VCCP_SOC_S5

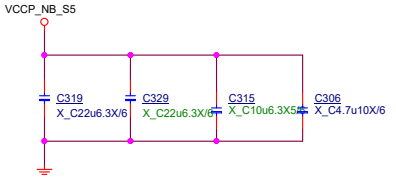
## 0.9A

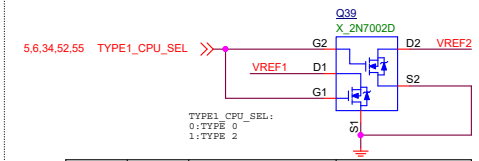
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

*(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)*




| CPU | TYPE | TYPE1_CPU_SEL | TYPE0_CPU_SEL |
|---|---|---|---|
| BR | 0 | 0 | 1 |
| NA | | 0 | 0 |
| SR | 2 | 1 | 1 |
| RV/ZP | 3 | 1 | 0 |

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

MICRO-START INTL CO.,LTD.

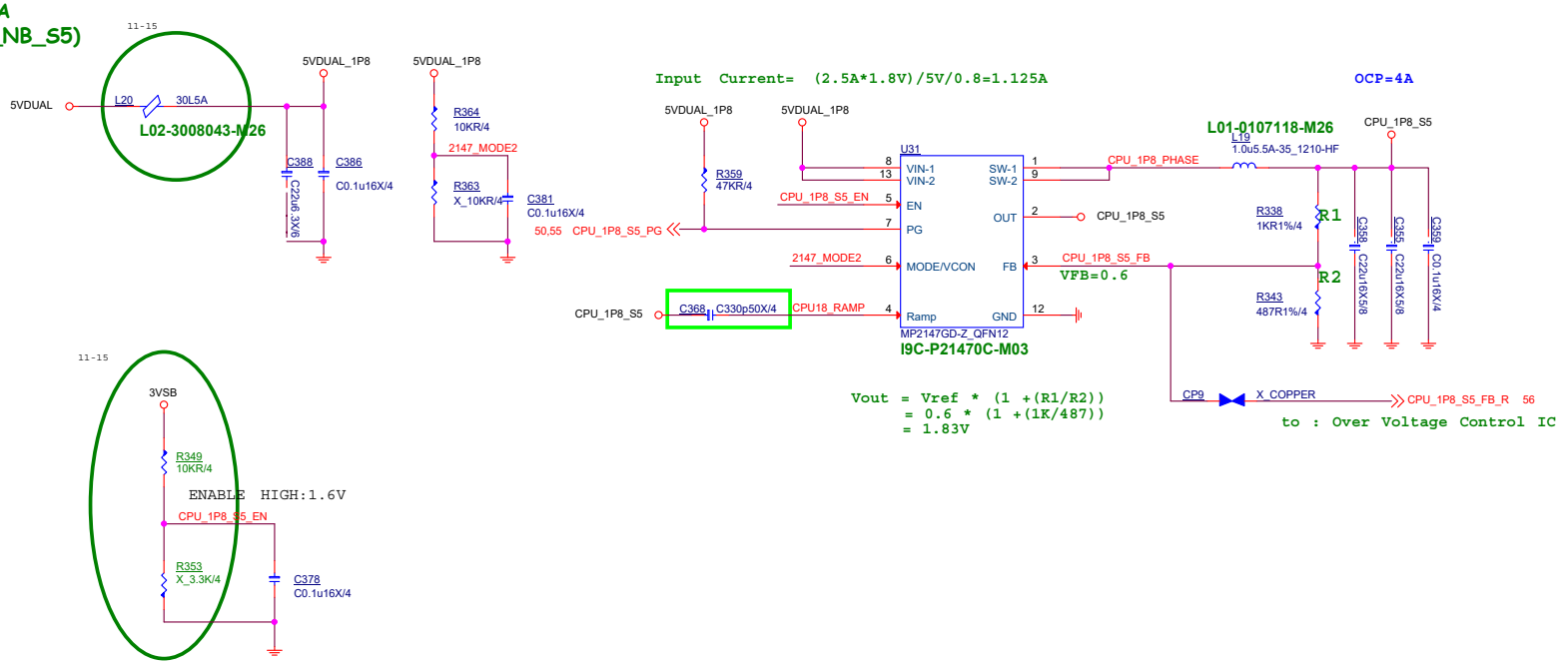
Title: CPU NB_S5

Size: Custom | Document Number: MS-7C02.. | Rev: 3.1

Date: Monday, September 28, 2020 | Sheet 50 of 70

# CPU 1.8V S5 @3.4A

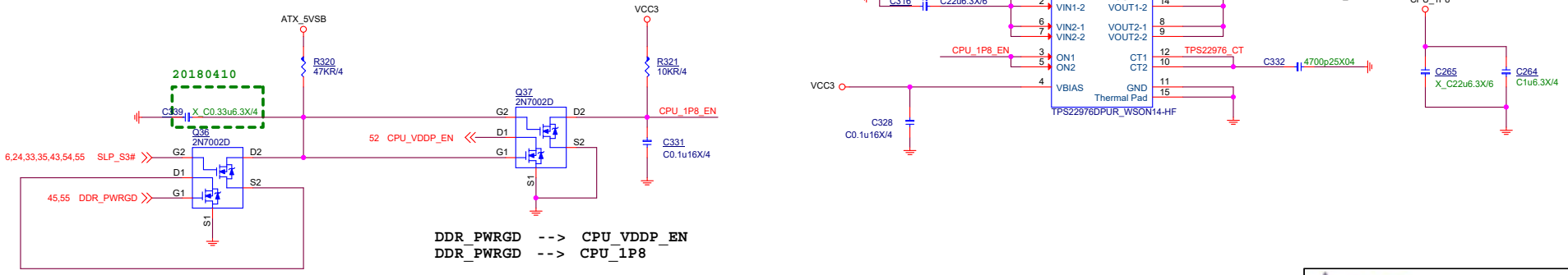
1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP_NB_S5)




# CPU 1.8V S0

1.8V@2A

*FOR VCCP_SOC@0.9A*

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| | | |
|---|---|---|
| Title | CPU 1.8_S0/S5 | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 51 of 70 | |

# CPU_VDDP_S0

Input Current= (8.5A*1.05V)/12V/0.8=0.93A

**1.05V/0.9V@S0:8.5A**

**S0:8.5A**
**S5:1A**

OCP=14A

+12V → CHOKE21 0.47u5A21 → +12V_VDDP

L04-47B7930-M26

C352 C0.1u16X/4, C375 22u16X/8, C366 22u16X/8, C357 22u16X/8

VCC3

R337 10KR/4

55 CPU_VDDP_PG ← R2511 0R/4 ← CPU_VDDP_PG_R

20171215
VCCSA_PG disconnect
MP8712_VCC, pull up VCC3

C356 C0.1u16X/4

VDDP_VCC (3.5V output)

C335 C0.47u16X5/4, C336 C0.022u25X/4

U27 MP8712

| | | | |
|---|---|---|---|
| 9 | VIN | BST | 1 |
| 5 | EN (EN H 1.2V) | SW | 2 |
| 7 | PG | VOUT | 10 |
| 13 | VCC | FB | 11 |
| 12 | SS | PGND | 8 |
| 3 | NC-1 | AGND | 14 |
| 4 | NC-2 | | |
| 6 | NC-3 | | |

CPU_VDDP_EN (EN H 1.2V)

CPU_VDDP_BOOT R312 0R/6 CPU_VDDP_BOOT_R C330 C0.1u25X/4

CPU_VDDP_SW

CPU_VDDP_SENSE_R

CPU_VDDP_FB_R R325 10KR/4 CPU_VDDP_FB

I9C-8712G0C-M03

L04-68B7350-T15

CHOKE19 → CH-0.68u15A5mS-HF-1

R2510 X_1R1%/6

C1499 X_C3300p50X/4

OCP=14A

1.05V,8.5A

CPU_VDDP

C282 C0.1u16X/4, C278 C22u6.3X6, C280 C22u6.3X6, C284 C22u6.3X6, C279 C22u6.3X6, C285 C22u6.3X6

+12V_VDDP

R332 100KR1%/4

6,43,45,55 APU_AM4R1 → D33 S-LRB520S-40T1G → CPU_VDDP_EN (12-27)

R327 39.2KR1%/4

C348 C0.1u16X/4

TYPE0_CPU_SEL: 1:TYPE 0 0:TYPE 2
CPU_VDDP_EN: 0:TYPE 2 1:TYPE 0

Q46 2N7002D

6,7,55 TYPE0_CPU_SEL → G2; D2 → CPU_VDDP_EN → CPU_VDDP_EN 51

VDDP_SEL → D1; S2 → VDDP_SEL

6,34,50,52,55 TYPE1_CPU_SEL → G1

TYPE1_CPU_SEL: 0:TYPE 0 1:TYPE 2

S1

| CPU | TYPE | TYPE0_CPU_SEL | TYPE1_CPU_SEL | CPU_VDDP_EN |
|---|---|---|---|---|
| BR | 0 | 1 | 0 | 1 |
| NA | X | 0 | 0 | 0 |
| SR | 2 | 1 | 0 | 1 |
| RV/ZP | 3 | 0 | 1 | 1 |

CPU VDDP NOT SUPPORT TYPE2

CPU_VDDP

R317 6.8R1%/4

C350 X_C22p50N/4 CPU_VDDP_SENSE_R R316 0R/4 CPU_VDDP_SENSE 6

R1 R323 1KR1%/4

CP10 X_COPPER → CPU_VDDP_OV 56

CPU_VDDP_FB

ATX_5VSB

R370 X_47KR/4

Q47 X_2N7002D

R3 R330 X_3.83KR1%/4

R2 R329 2KR1%/4

AM4_CPU_SEL
0:Type 0/1 =>1.053V
1:Type 2/3 =>0.9V

C391 X_C0.1u16X/4

5,6,34,50,52,55 TYPE1_CPU_SEL

17 PM_GPIO_R9

PM_GPIO_R9
Page 17 pull high
1:Type 0/1 1.05V
0:Type 2/3 0.9V

Q49 X_N-2N7002

01-04

Type 2/3:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/2K))
= 0.9V

# CPU_VDDP_S5

**1.05V/0.9V**
**S5:1A**

Input Current=0.04A

12-27

5VDUAL 5VSB

5VDUAL → L18 30L5A → L02-3008043-M26

R357 X_10KR/4

R361 10KR/4 11-15

C377 C22u6.3X/6

C385 C1u6.3X/4

55 VDDP_VSB_PG

I9C-2143D09-M03

U30 MP2143DJ

| | | | |
|---|---|---|---|
| 2 | VIN | SW | 3 |
| 8 | EN | OUT | 5 |
| 1 | PG | FB | 7 |
| 4 | PGND | | |
| 6 | AGND | | |

VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PHASE
VDDP_VSB_FB

FB: 0.6V

MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

default:0.775V,0.2A

L01-0107118-M26

L15 1.0u5.5A-35_1210-HF

CPU_VDDP_S5

R1 R355 1KR1%/4

R2 R354 2KR1%/4

C369 C22u6.3X/6, C376 C22u6.3X/6, C363 C0.22u6.3X/4

VDDP_VSB_FB

VDDP_VSB_FB

ATX_5VSB

R3 R360 X_3.83KR1%/4

R371 X_47KR/4

Q48 X_2N7002D

C392 X_C0.1u16X/4

VDDP_VSBFB

5,6,34,50,52,55 TYPE1_CPU_SEL

AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

Type 0/1:
Vout = Vref * (1 +(R1/(R2//R3))
= 0.6 * (1 +(1K/(2K//3.83K))
= 1.058V

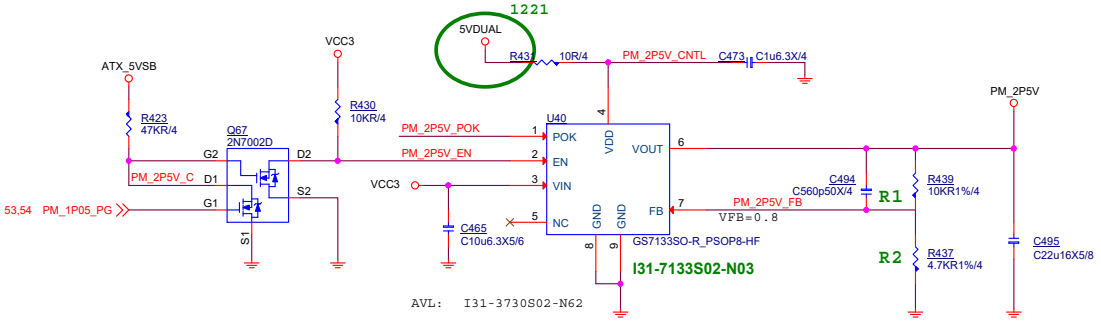
Type 2/3:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/2K))
= 0.9V

MSI Link to the Future MICRO-START INTL CO.,LTD.

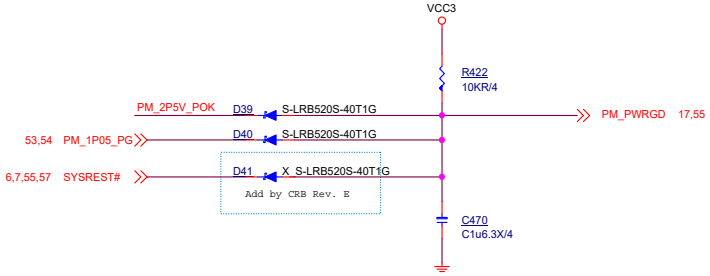
| | | | |
|---|---|---|---|
| Title | CPU Power VDDP | | |
| Size | Document Number | | Rev |
| Custom | MS-7C02.. | | 3.1 |
| Date: | Monday, September 28, 2020 | Sheet 52 of 70 | |

# Promontory-2.5V

2.5V@900mA




Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V

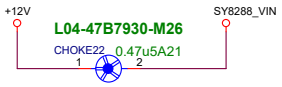



MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
| Title: Prom-GS7133/2.5V | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 53 of 70 | |

# FOR Promontory 1.05V_S0

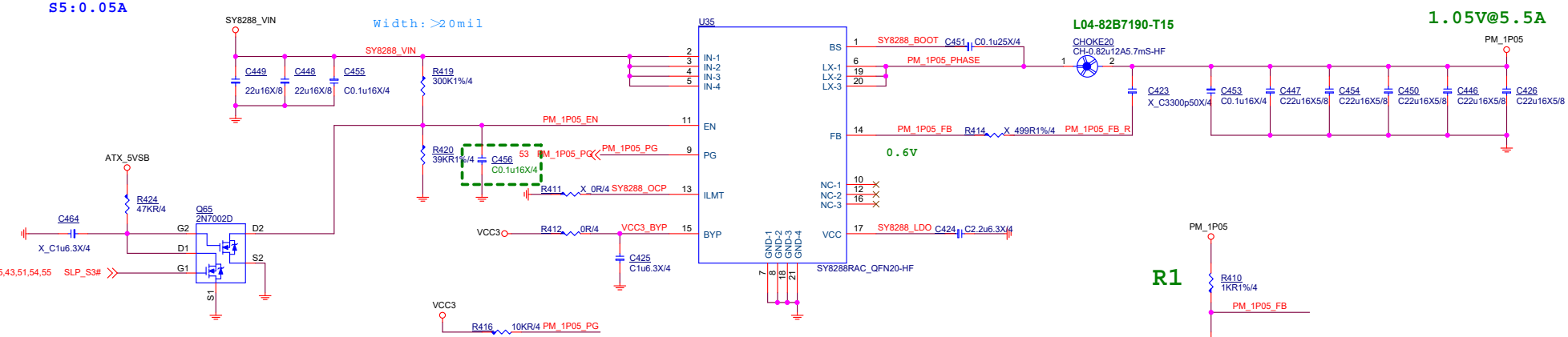
1.05V
S0:5.5A
S5:0.05A

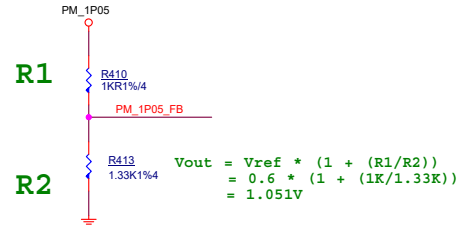



Input Current= (5.5A*1.05V)/12V/0.8=0.6A

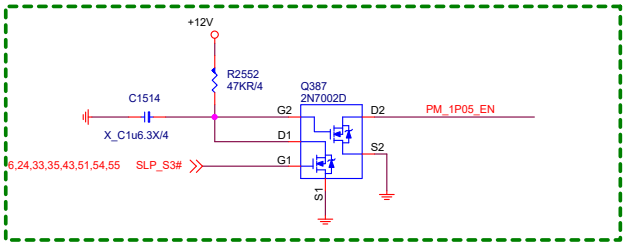
OCP=12A

1.05V@5.5A



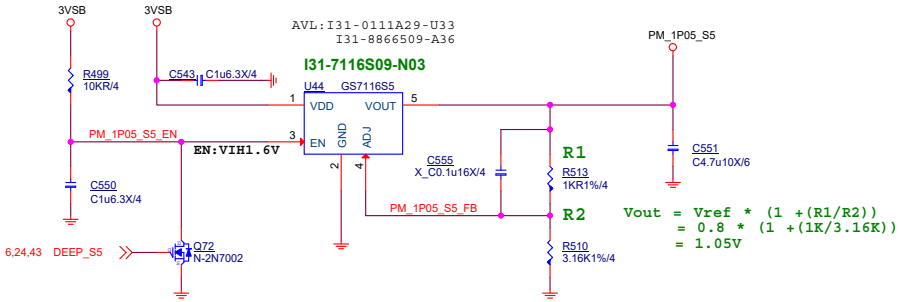




| SY8288_OCP | OCP |
|---|---|
| 0 | 8A |
| floating | 12A |
| 1 | 16A |




# FOR Promontory 1.05V_S5

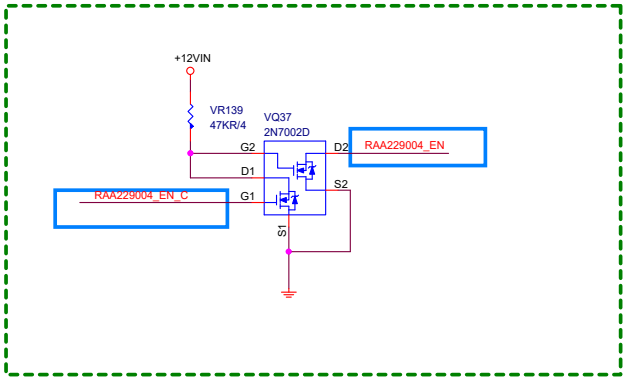
*1.05V@0.05A*

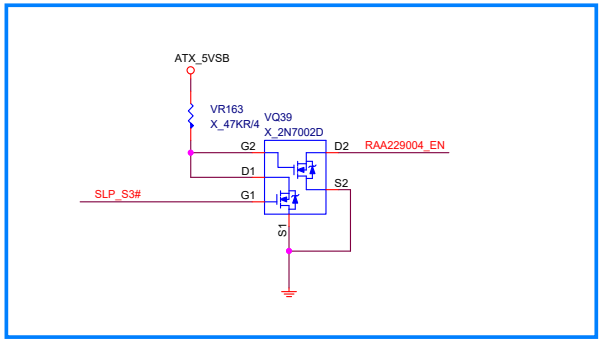


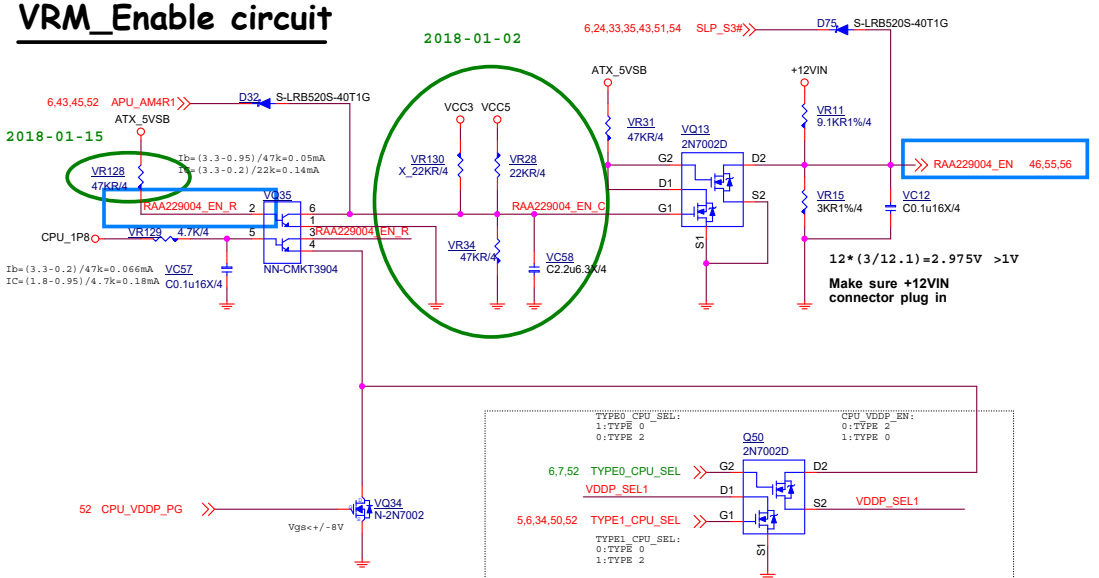

MSI Link to the Future MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
| Title: Prom- SY8288RAC / 1.05V | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 54 of 70 | |

# VRM_Enable circuit





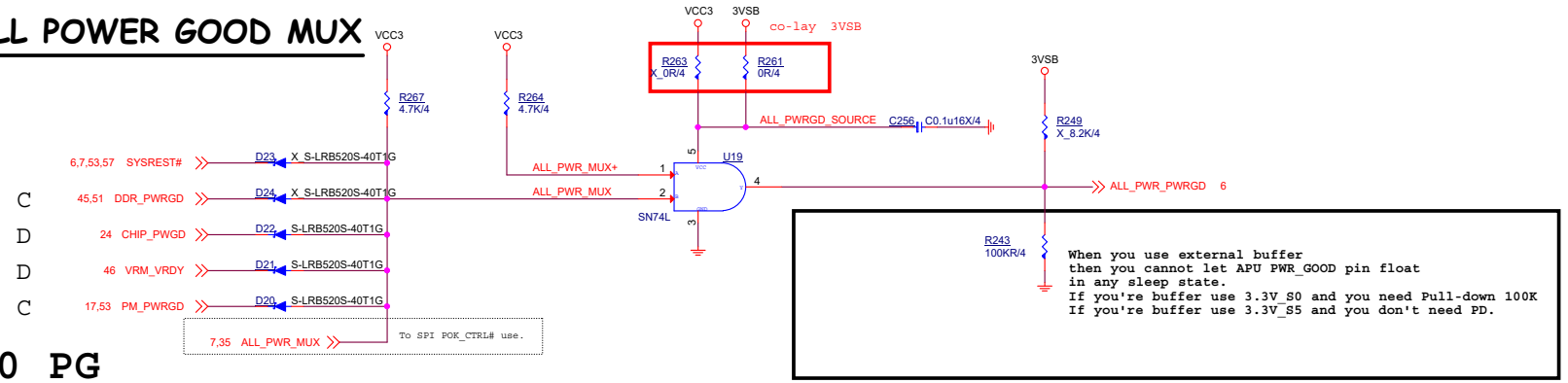





| CPU | TYPE | TYPE1_CPU_SEL | TYPE0_CPU_SEL |
|---|---|---|---|
| BR | 0 | 0 | 1 |
| NA | X | 0 | 0 |
| SR | 2 | 1 | 1 |
| RV/ZP | 3 | 1 | 0 |

CPU VDDP NOT SUPPORT TYPE2

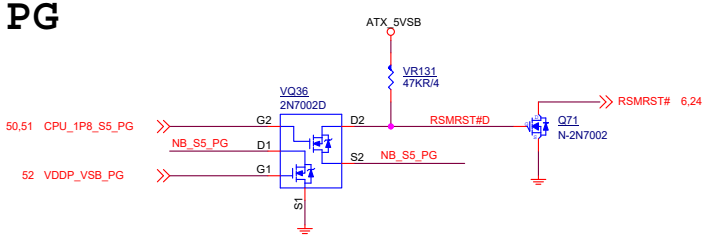
# ALL POWER GOOD MUX




When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

# S0 PG

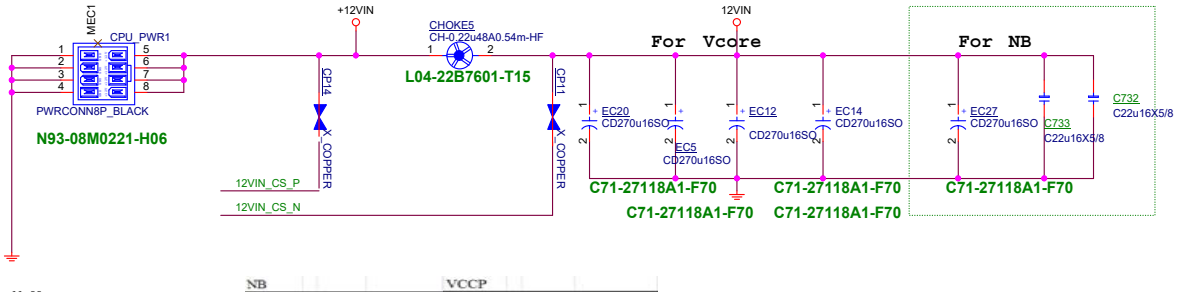
# S5 PG




MSI MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
| Title | VRM-EN/PWRGD | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
| Date: Monday, September 28, 2020 | Sheet 55 of 70 | |

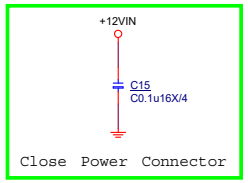
# CPU POWER CONNECTOR




11-22

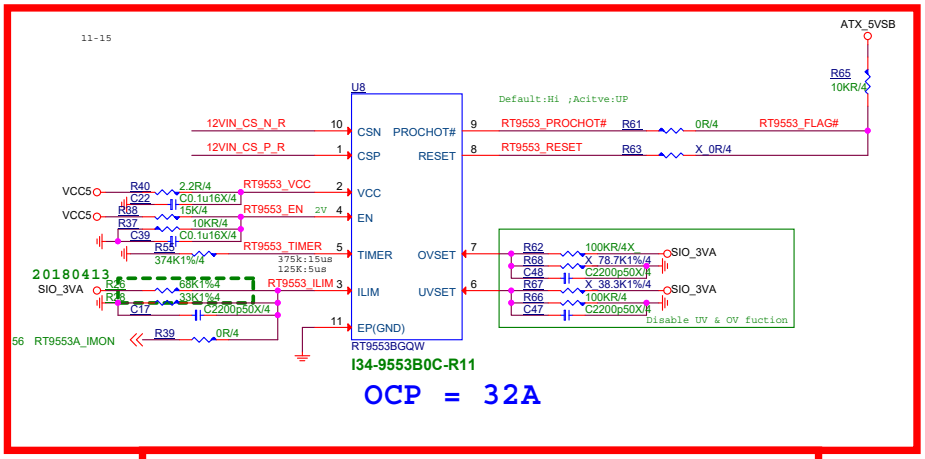
| NB | | VCCP | |
|---|---|---|---|
| D=Vout/Vin | | D=Vout/Vin | |
| Vin = | 12 | Vin = | 12 |
| Vout = | 1.4 | Vout = | 1.4 |
| D = | 0.116667 | D = | 0.116667 |
| Io = Icoremax)*0.8 | | Io = Icoremax)*0.8 | |
| I core(max) = | 75 | I core(max) = | 125 |
| I avg = | 75 A | I avg = | 125 A |
| Iripple=(Io*√D*√(1-D)) / Phase | | Iripple=(Io*√D*√(1-D)) / Phase | |
| Phase = | 2 | Phase = | 4 |
| I ripple = | 12.03835 A | I ripple = | 10.03196 A |
| How many pcs. Of Cap. | | How many pcs. Of Cap. | |
| I ripple(cap) = | 5000 m A | I ripple(cap) = | 5000 m A |
| COEmax = | 1 | COEmax = | 1 |
| Input Cap. = | 3 pcs. | Input Cap. = | 3 pcs. |

11-15




# RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

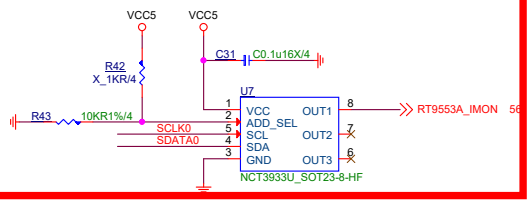



# Over Voltage Control IC

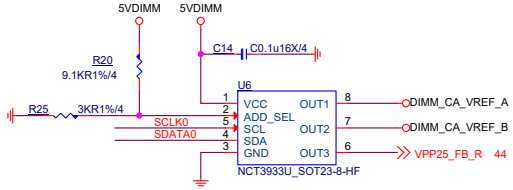
## UPI VOLTAGE CONSOLE

| ADDRESS | 0x2A | 0X28 | 0x26 | 0x24 | 0x22 | 0x20 |
|---|---|---|---|---|---|---|
| RH (KOhm) | OPEN | 3.9 | 3 | 2.2 | 1.3 | 10 |
| RL (KOhm) | 10 | 1.3 | 2.3 | 3 | 3.9 | OPEN |
| BUS_SEL | 0% | 25% | 40% | 60% | 75% | 100% |

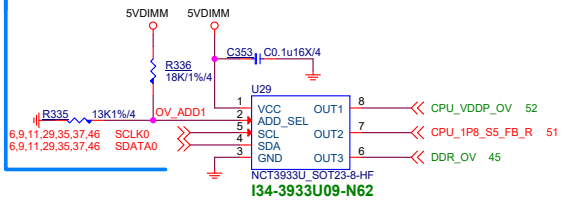
### 0x2A:RH=OPEN,RL=10K

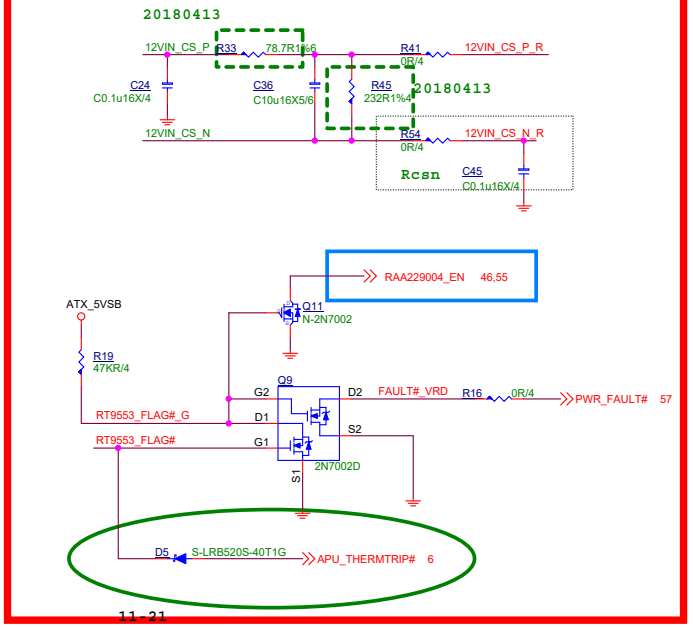



### 0x28:RH=9.1K,RL=3K




### 0x26:RH=18K,RL=13K




MSI MICRO-START INTL CO.,LTD.

Title: RT9553B CURRENT SENSE/OV Control

| Size | Document Number | Rev |
|---|---|---|
| Custom | MS-7C02.. | 3.1 |

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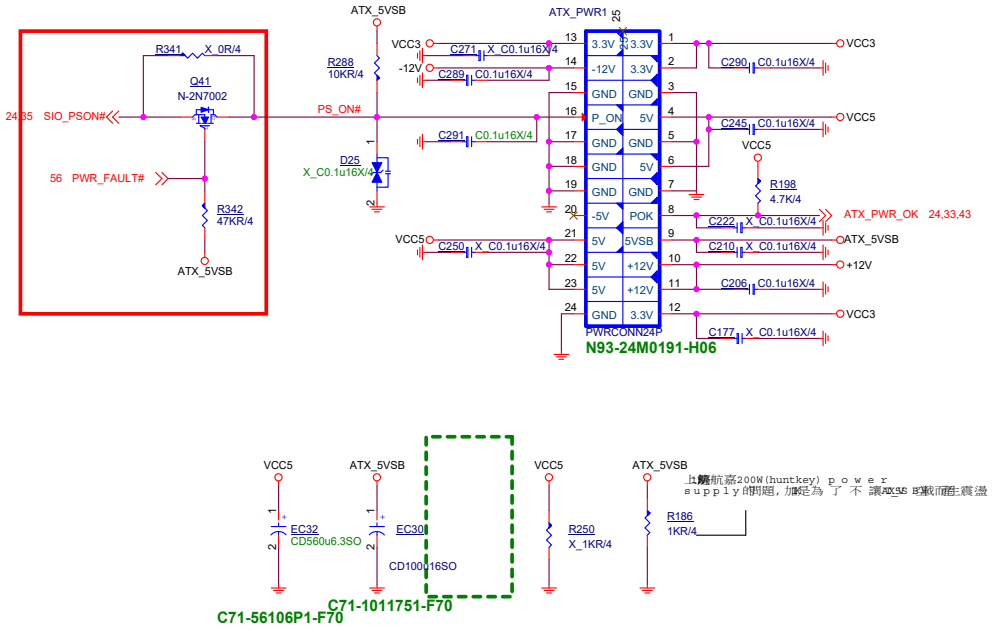
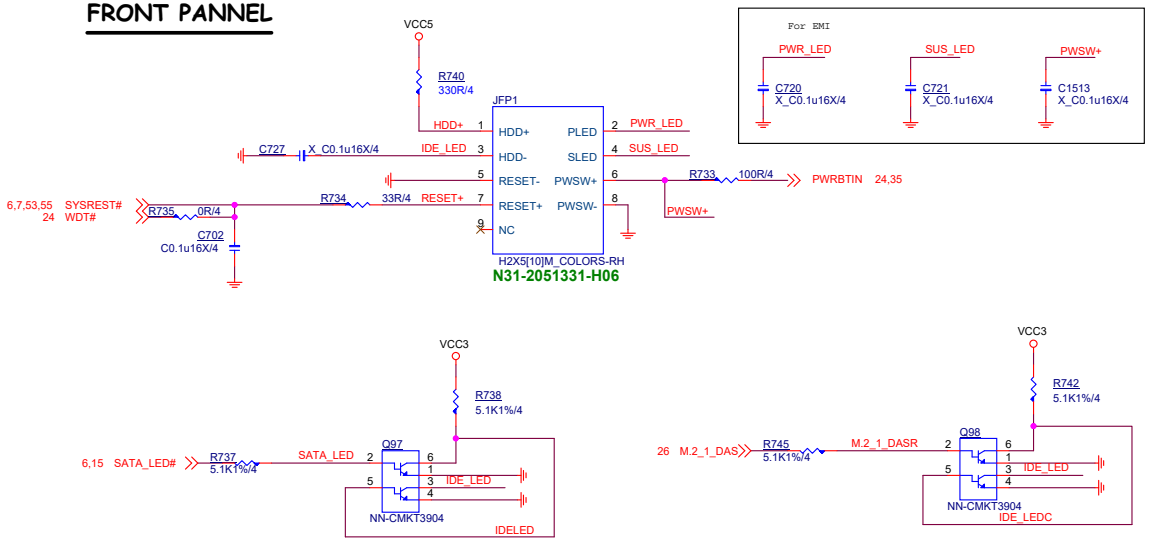
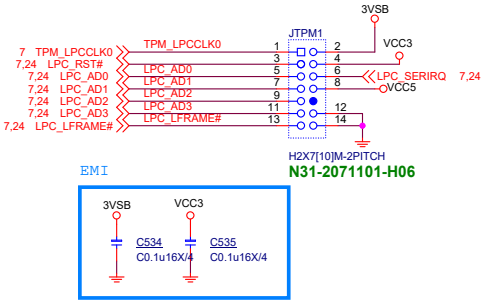
## ATX POWER CONNECTOR



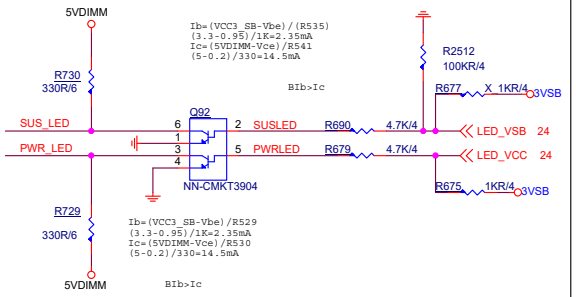

## FRONT PANNEL




## TPM

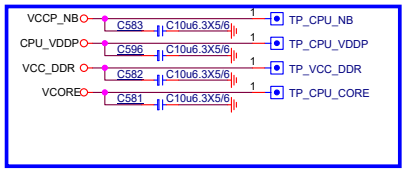


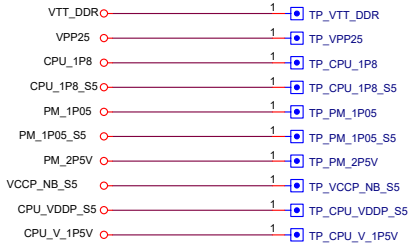

## LED ( for NCT6797)




## Voltage Mearsure Point

TP close to SIO
Cap close to TP



MSI MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | ATX/Front Panel | |
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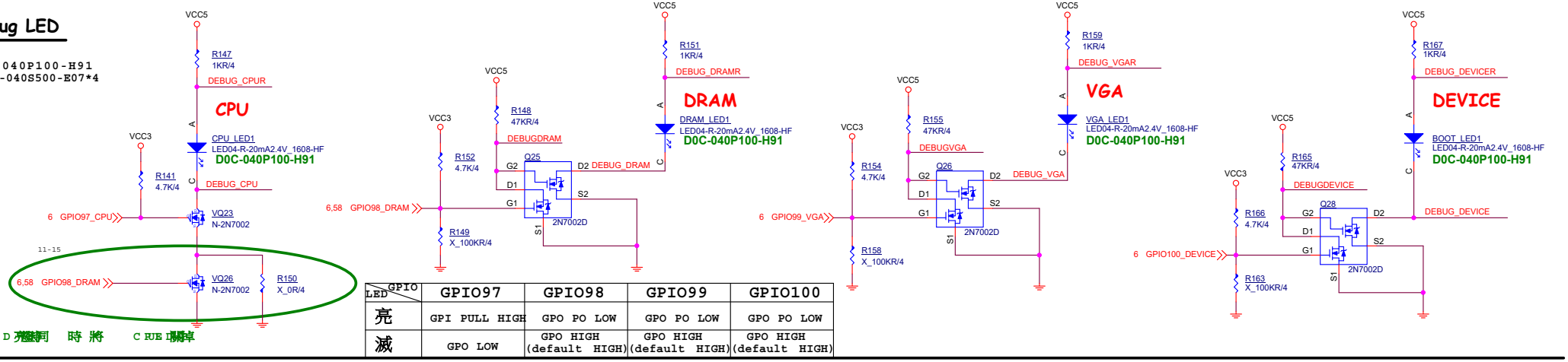
# EZ Debug LED

紅:D0C-040P100-H91
S:D0C-040S500-E07*4




LED亮滅同 時 將 CRUE關掉

| LED \ GPIO | GPIO97 | GPIO98 | GPIO99 | GPIO100 |
|---|---|---|---|---|
| 亮 | GPI PULL HIGH | GPO PO LOW | GPO PO LOW | GPO PO LOW |
| 滅 | GPO LOW | GPO HIGH (default HIGH) | GPO HIGH (default HIGH) | GPO HIGH (default HIGH) |

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: ALL LED Control

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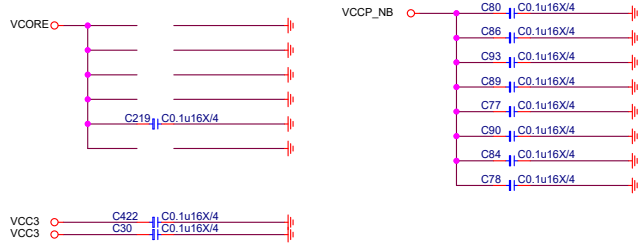
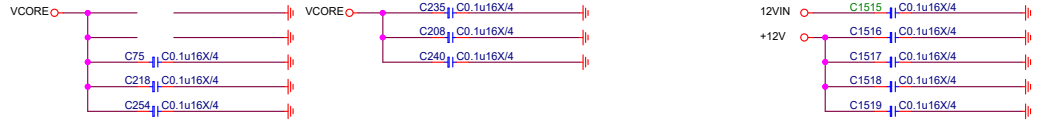
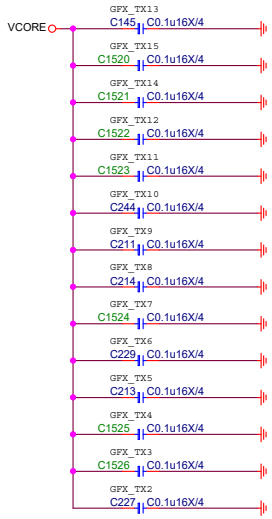
## Add for EMI




## return path




MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | NCT7718W temp sensor /EMI CAP | |
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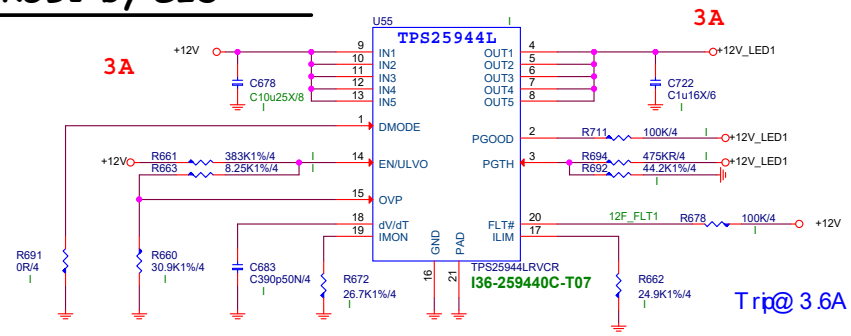
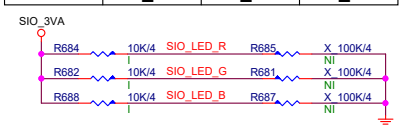
# JRGB1 by SIO

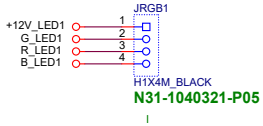
2016.07.06 Use TPS25944L



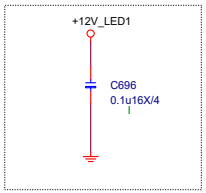

| Color | SIO_LED_R | SIO_LED_G | SIO_LED_B |
|---|---|---|---|
| RED | 1 | 0 | 0 |
| GREEN | 0 | 1 | 0 |
| BLUE | 0 | 0 | 1 |
| WHITE | 1 | 1 | 1 |

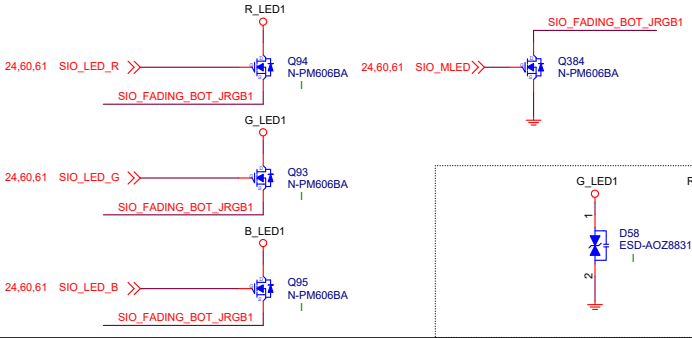


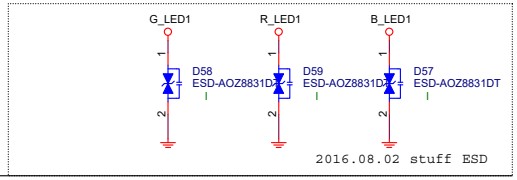

PM SPEC Default WHITE Color




2016.08.02 Add +12V_LED 0.1uF



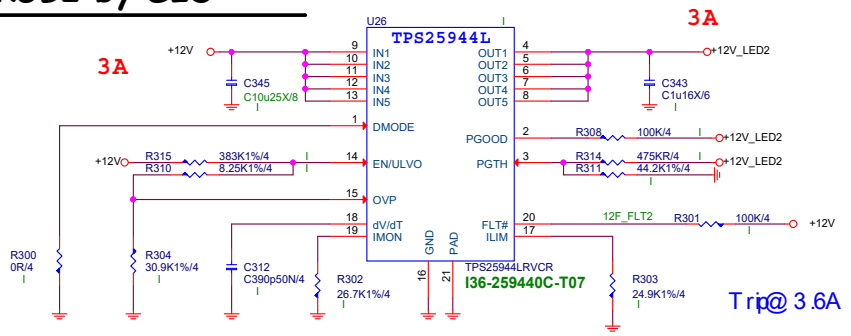



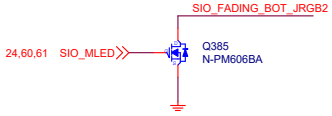



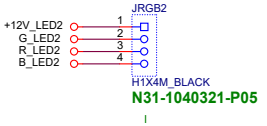

2016.08.02 stuff ESD

# JRGB2 by SIO

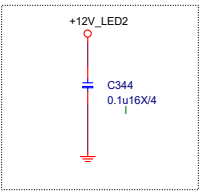
2016.07.06 Use TPS25944L

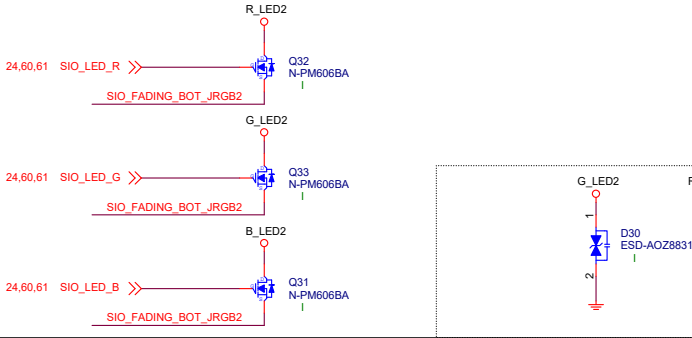


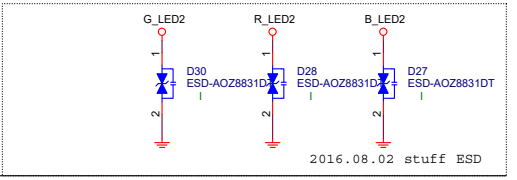




2016.08.02 Add +12V_LED 0.1uF




2016.08.02 stuff ESD

MICRO-START INTL CO.,LTD.

| | | |
|---|---|---|
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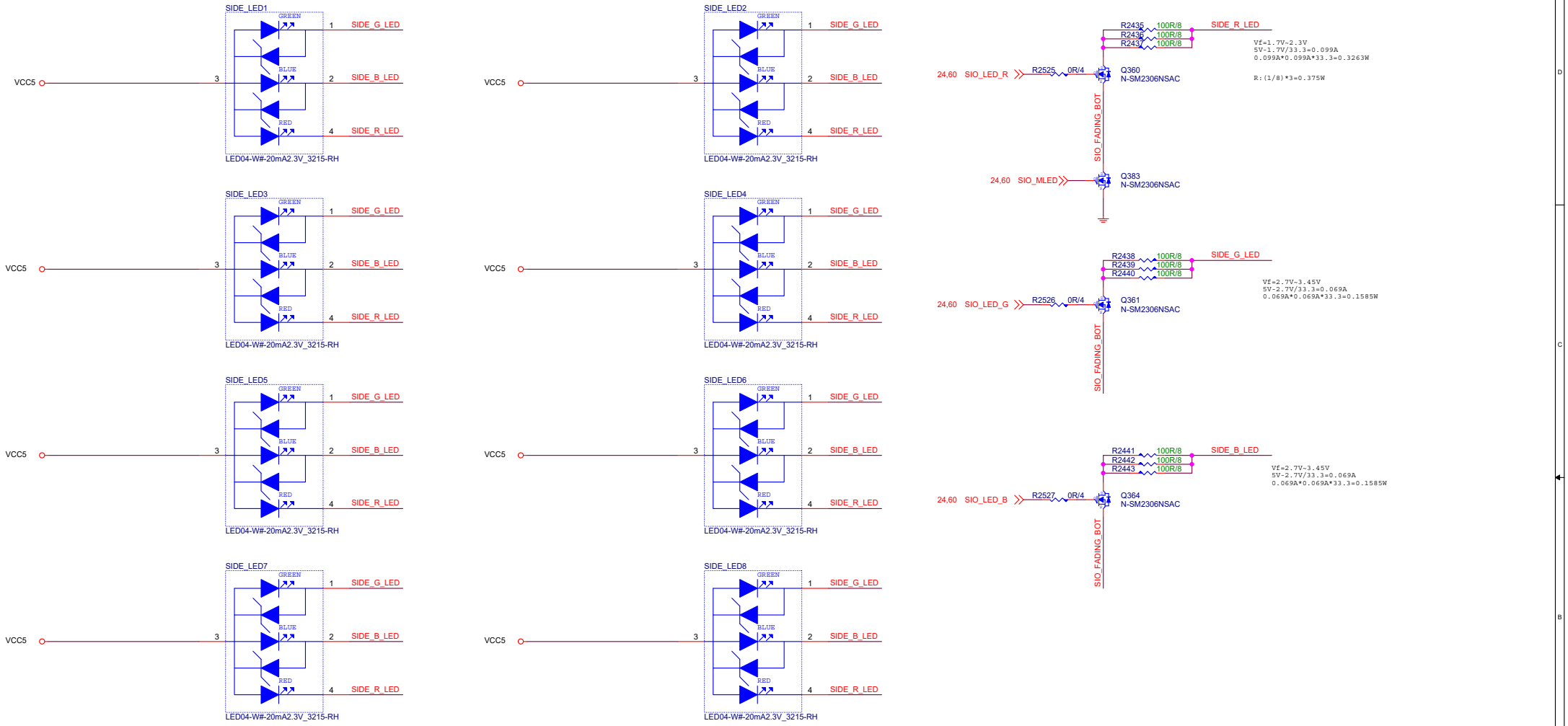
# BOARD SIDE LED

*8




MICRO-START INT'L CO.,LTD.

| | | |
|---|---|---|
| Title: RGB LED Control | | |
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Title: BOM Option

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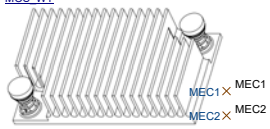
11-16

RM: E95-0000022-C22/ E95-0000022-A91

## MOS SINK

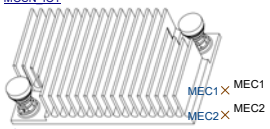
MOS_W1




HS-0505781-RH

E31-0505781-A87

MOSN_IO1



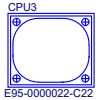

HS-0505771-RH

E31-0505771-A87

## DDR Cover

## CPU Socket

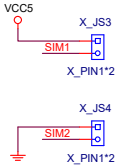
CPU3



E95-0000022-C22

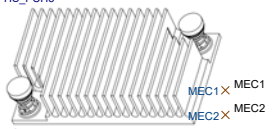
E95-0000022-C22

## Simulation




## PCH SINK

HS_PCH5




HS-0410220-RH

E31-0410220-A87

## AUDIO COVER

## MANUAL PART

BAT1_X1

BATI-SOSCR2032-RH

AVL:
D06-0100161-F52
D06-0100101-K26

PCB1

7C02-3.1

## BIOS LABEL

UEFI1

Label

UEFI_BIOS

G51-M1SPXXA-A09

G51-M1SPXXA-A09

## MKTG name Label

MKTG1

Label

MKTG_NAME

G51-M1SPQ45-Q13

## ROYALTY

HDMI_LA1

Y01-RHDMI03-000

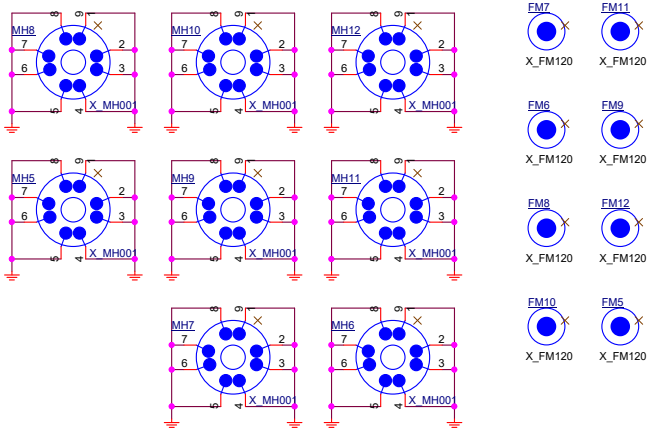
Y01-RHDMI03-000

NAHIMIC

Y02-MU00100-NAH

X_Y02-MU00100-NAH

## Optics Orientation Holes




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: Manual Parts | | |
| Size: Custom | Document Number: MS-7C02.. | Rev: 3.1 |
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