AMD AM4

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MS-7C02 BOM List

	Schematic Cfg	ERP NO.	Remark	BOM
*	CFG-7C02-**-Arsenal Gaming	601-7C02-***		A

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Title: COVER SHEET

Size: C | Document Number: MS-7C02 | Rev: 1.0

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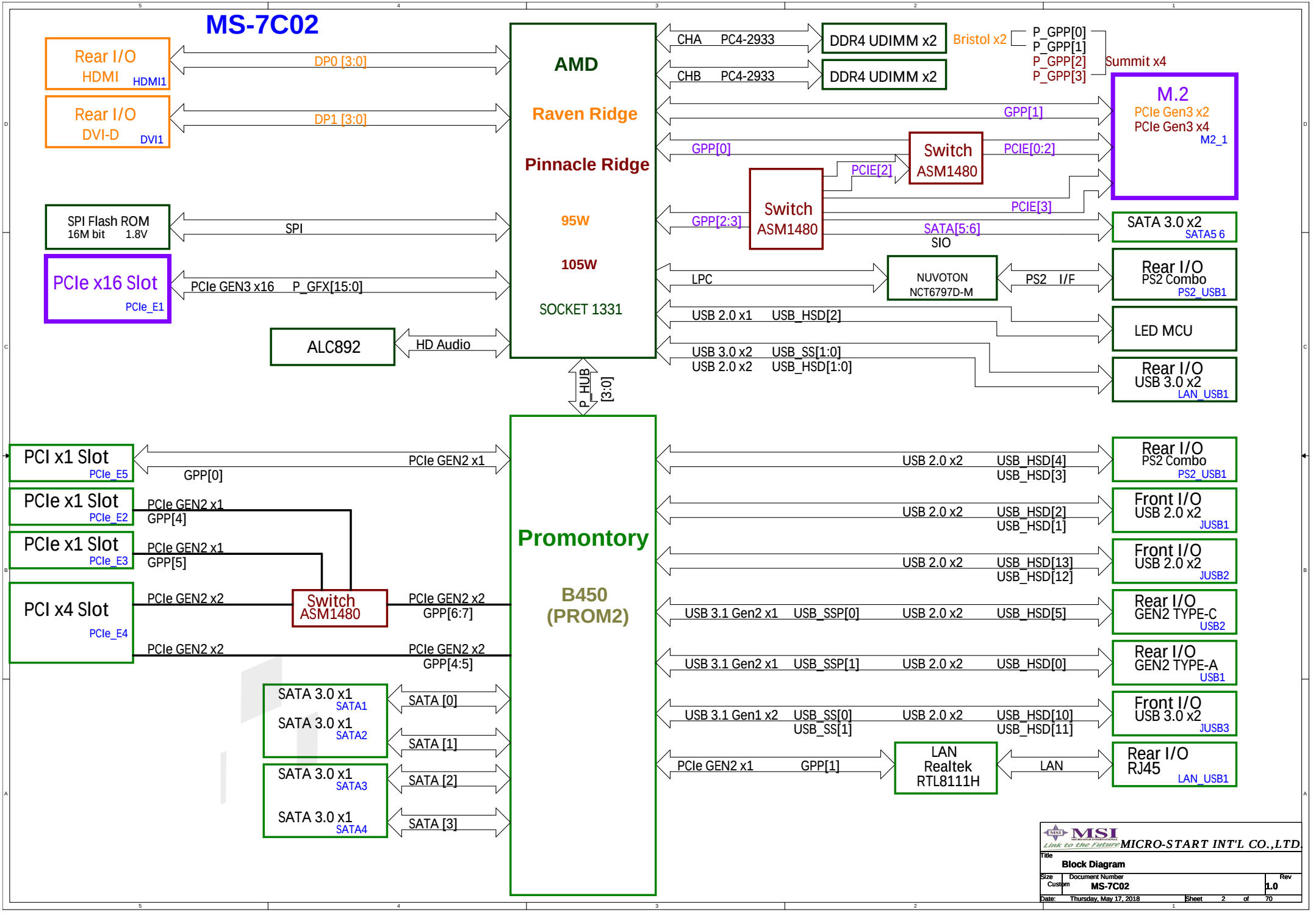

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Link to the Future

Title: Block Diagram		
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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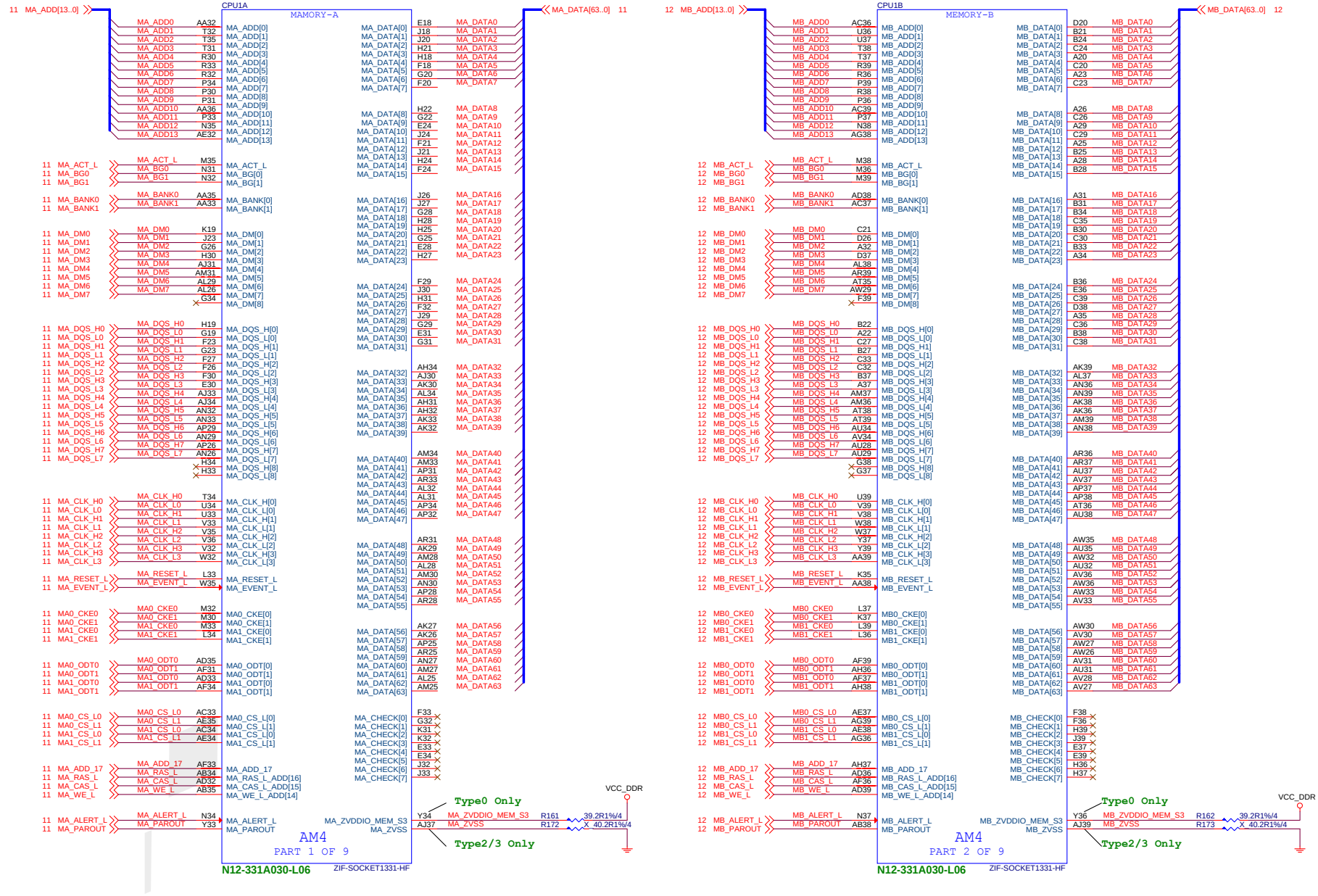

Schematic Cfg	Project	
CFG-7C02-***-Arsenal Gaming	V	A

MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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Schematic Cfg	Project	
CFG-7C02-***-Arsenal Gaming	V	A

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Title: AM4 PCIE/SATAE		
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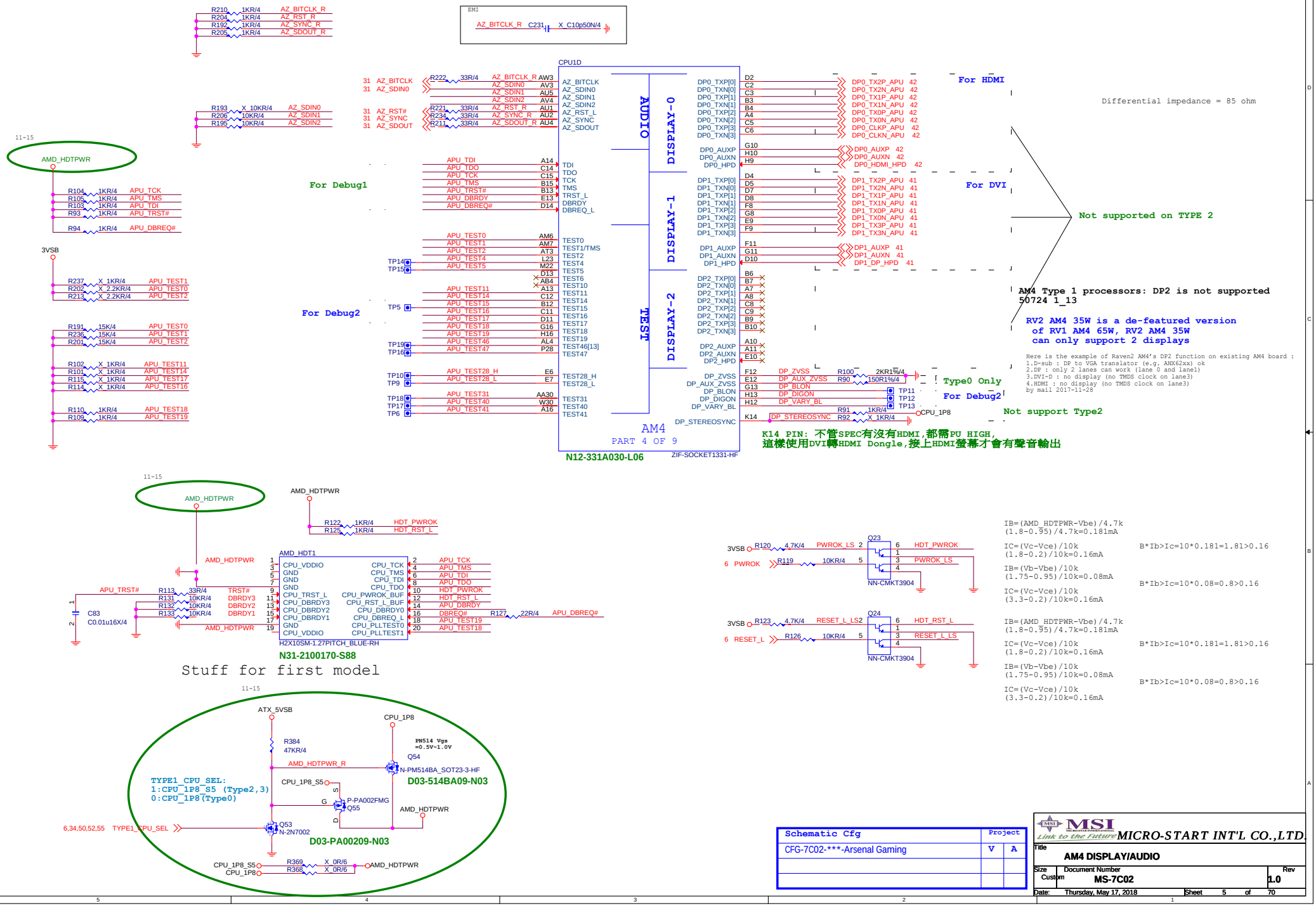
R210 1KR/4 AZ_BITCLK_R
R204 1KR/4 AZ_RST_R
R192 1KR/4 AZ_SYNC_R
R205 1KR/4 AZ_SDOUT_R
EMI
AZ_BITCLK_R C231 X_C10p50N/4
CPU1D
31 AZ_BITCLK
31 AZ_SDIN0
R222 33R/4
AZ_BITCLK_R AW3
AZ_SDIN0 AV3
AZ_SDIN1 AU5
AZ_SDIN2 AV4
R193 X_10KR/4 AZ_SDIN0
R206 10KR/4 AZ_SDIN1
R195 10KR/4 AZ_SDIN2
31 AZ_RST#
31 AZ_SYNC
31 AZ_SDOUT
R221 33R/4 AZ_RST_R AU1
R234 33R/4 AZ_SYNC_R AU2
R211 33R/4 AZ_SDOUT_R AU4
AZ_BITCLK
AZ_SDIN0
AZ_SDIN1
AZ_SDIN2
AZ_RST_L
AZ_SYNC
AZ_SDOUT
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
DP0_TX[0] D2
DP0_TXN[0] C2
DP0_TX[1] C3
DP0_TXN[1] B3
DP0_TX[2] B4
DP0_TXN[2] A4
DP0_TX[3] C5
DP0_TXN[3] C6
DP0_AUXP G10
DP0_AUXN H10
DP0_HPD H9
DP0_TX2P_APU 42
DP0_TX2N_APU 42
DP0_TX1P_APU 42
DP0_TX1N_APU 42
DP0_TX0P_APU 42
DP0_TX0N_APU 42
DP0_CLKP_APU 42
DP0_CLKN_APU 42
DP0_AUXP 42
DP0_AUXN 42
DP0_HDMI_HPD 42
For HDMI
DP1_TX[0] D4
DP1_TXN[0] D5
DP1_TX[1] D7
DP1_TXN[1] D8
DP1_TX[2] F8
DP1_TXN[2] G8
DP1_TX[3] E9
DP1_TXN[3] F9
DP1_AUXP F11
DP1_AUXN G11
DP1_HPD D10
DP1_TX2P_APU 41
DP1_TX2N_APU 41
DP1_TX1P_APU 41
DP1_TX1N_APU 41
DP1_TX0P_APU 41
DP1_TX0N_APU 41
DP1_TX3P_APU 41
DP1_TX3N_APU 41
DP1_AUXP 41
DP1_AUXN 41
DP1_DP_HPD 41
For DVI
DP2_TX[0] B6
DP2_TXN[0] B7
DP2_TX[1] A7
DP2_TXN[1] A8
DP2_TX[2] C8
DP2_TXN[2] C9
DP2_TX[3] B9
DP2_TXN[3] B10
DP2_AUXP A10
DP2_AUXN A11
DP2_HPD E10
DP_ZVSS F12
DP_AUX_ZVSS E12
DP_BLON G13
DP_DIGON H13
DP_VARY_BL H12
DP_STEREOSYNC K14
DP_ZVSS R100 2KR1%/4
DP_AUX_ZVSS R90 150R1%/4
TP11
TP12
TP13
R91 1KR/4
R92 X_1KR/4
CPU_1P8
Type0 Only
For Debug2
Not support Type2
Differential impedance = 85 ohm
Not supported on TYPE 2
AM4 Type 1 processors: DP2 is not supported
50724 1_13
RV2 AM4 35W is a de-featured version
of RV1 AM4 65W, RV2 AM4 35W
can only support 2 displays
Here is the example of Raven2 AM4's DP2 function on existing AM4 board :
1.D-sub : DP to VGA translator (e.g. ANX62xx) ok
2.DP : only 2 lanes can work (lane 0 and lane1)
3.DVI-D : no display (no TMDS clock on lane3)
4.HDMI : no display (no TMDS clock on lane3)
by mail 2017-11-28
K14 PIN: 不管SPEC有沒有HDMI,都需PU HIGH,
這樣使用DVI轉HDMI Dongle,接上HDMI螢幕才會有聲音輸出
AM4
PART 4 OF 9
N12-331A030-L06
ZIF-SOCKET1331-HF
11-15
AMD_HDTPWR
R104 1KR/4 APU_TCK
R105 1KR/4 APU_TMS
R103 1KR/4 APU_TDI
R93 1KR/4 APU_TRST#
R94 1KR/4 APU_DBREQ#
3VSB
R237 X_1KR/4 APU_TEST1
R202 X_2.2KR/4 APU_TEST0
R213 X_2.2KR/4 APU_TEST2
R191 15K/4 APU_TEST0
R236 15K/4 APU_TEST1
R201 15K/4 APU_TEST2
R102 X_1KR/4 APU_TEST11
R101 X_1KR/4 APU_TEST14
R115 X_1KR/4 APU_TEST17
R114 X_1KR/4 APU_TEST16
R110 1KR/4 APU_TEST18
R109 1KR/4 APU_TEST19
For Debug1
For Debug2
APU_TDI A14
APU_TDO C14
APU_TCK C15
APU_TMS B15
APU_TRST# B13
APU_DBRDY E13
APU_DBREQ# D14
TDI
TDO
TCK
TMS
TRST_L
DBRDY
DBREQ_L
APU_TEST0 AM6
APU_TEST1 AM7
APU_TEST2 AT3
APU_TEST4 L23
APU_TEST5 M22
D13
AB4
A13
C12
B12
C11
D11
G16
H16
AL4
P28
E6
E7
AA30
W30
A16
TP14
TP15
TP5
TP19
TP16
TP10
TP9
TP18
TP17
TP6
TEST0
TEST1/TMS
TEST2
TEST4
TEST5
TEST6
TEST10
TEST11
TEST14
TEST15
TEST16
TEST17
TEST18
TEST19
TEST46[13]
TEST47
TEST28_H
TEST28_L
TEST31
TEST40
TEST41
11-15
AMD_HDTPWR
AMD_HDTPWR
R122 1KR/4 HDT_PWROK
R125 1KR/4 HDT_RST_L
AMD_HDTPWR
APU_TRST# R113 33R/4 TRST#
R131 10KR/4 DBRDY3
R132 10KR/4 DBRDY2
R133 10KR/4 DBRDY1
C83 C0.01u16X/4
AMD_HDTPWR
AMD_HDT1
CPU_VDDIO
GND
GND
GND
CPU_TRST_L
CPU_DBRDY3
CPU_DBRDY2
CPU_DBRDY1
GND
CPU_VDDIO
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TDO
CPU_PWROK_BUF
CPU_RST_L_BUF
CPU_DBRDY0
CPU_DBREQ_L
CPU_PLLTEST0
CPU_PLLTEST1
APU_TCK
APU_TMS
APU_TDI
APU_TDO
HDT_PWROK
HDT_RST_L
APU_DBRDY
DBREQ#
APU_TEST19
APU_TEST18
R127 22R/4 APU_DBREQ#
H2X10SM-1.27PITCH_BLUE-RH
N31-2100170-S88
Stuff for first model
11-15
ATX_5VSB
CPU_1P8
R384 47KR/4
PN514 Vgs =0.5V~1.0V
Q54
AMD_HDTPWR_R
N-PM514BA_SOT23-3-HF
D03-514BA09-N03
TYPE1_CPU_SEL:
1:CPU_1P8_S5 (Type2,3)
0:CPU_1P8(Type0)
CPU_1P8_S5
P-PA002FMG
Q55
AMD_HDTPWR
6,34,50,52,55 TYPE1_CPU_SEL
Q53
N-2N7002
D03-PA00209-N03
CPU_1P8_S5 R369 X_0R/6
CPU_1P8 R368 X_0R/6
AMD_HDTPWR
3VSB R120 4.7K/4 PWROK_LS
6 PWROK R119 10KR/4
Q23
HDT_PWROK
PWROK_LS
NN-CMKT3904
IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA
IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA
B*Ib>Ic=10*0.181=1.81>0.16
IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA
IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA
B*Ib>Ic=10*0.08=0.8>0.16
3VSB R123 4.7K/4 RESET_L_LS
6 RESET_L R126 10KR/4
Q24
HDT_RST_L
RESET_L_LS
NN-CMKT3904
IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA
IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA
B*Ib>Ic=10*0.181=1.81>0.16
IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA
IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA
B*Ib>Ic=10*0.08=0.8>0.16
Schematic Cfg
CFG-7C02-***-Arsenal Gaming
Project
V
A
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
AM4 DISPLAY/AUDIO
Size
Custom
Document Number
MS-7C02
Rev
1.0
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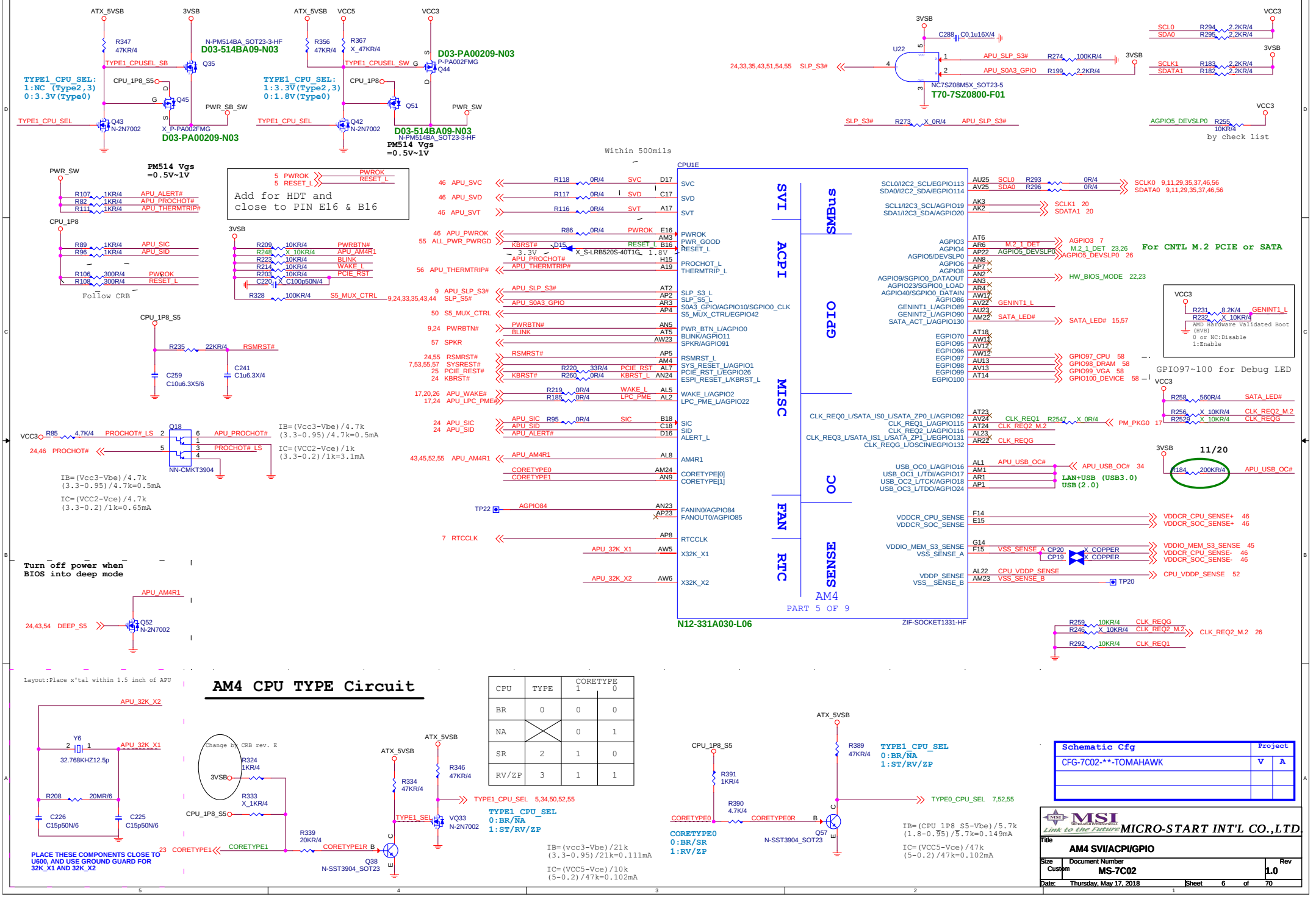

CPU	TYPE	CORETYPE 1	0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

Schematic Cfg	Project	
CFG-7C02-**-TOMAHAWK	V	A

MICRO-START INT'L CO.,LTD.

Title: AM4 SVI/ACPI/GPIO

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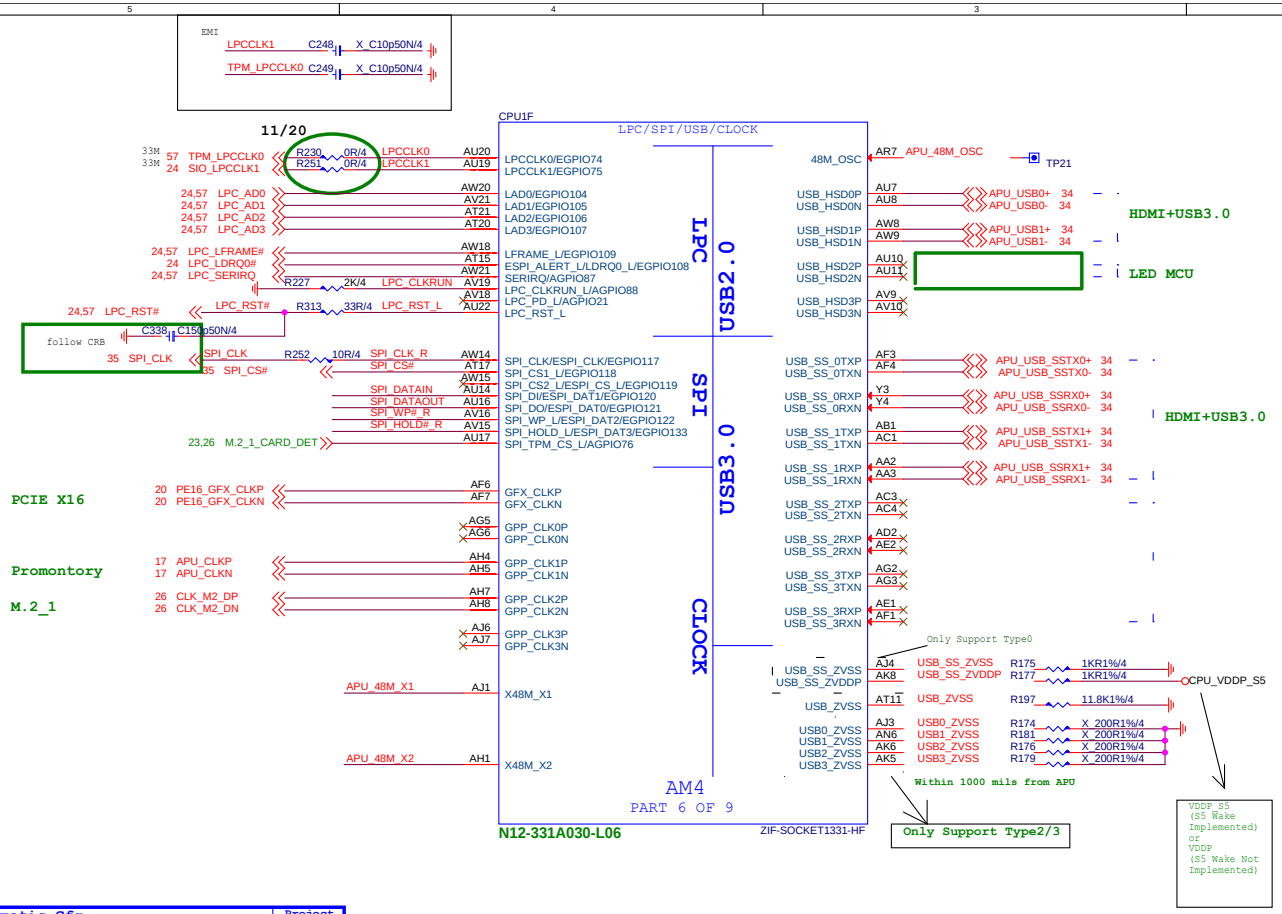
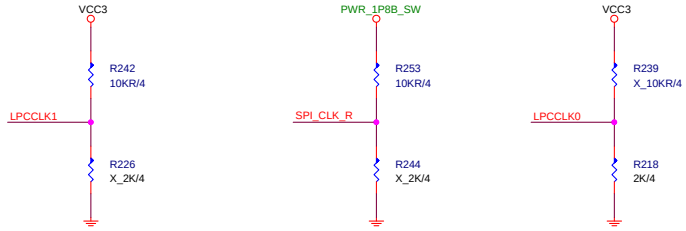
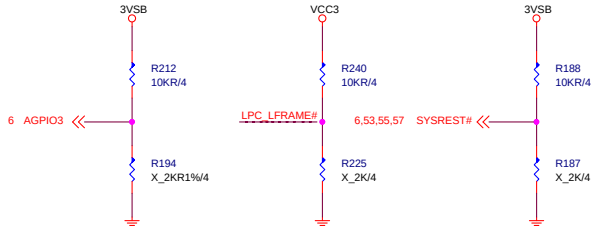


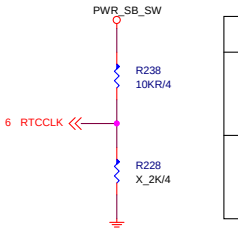
Strapping Options



	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled **(Default)**

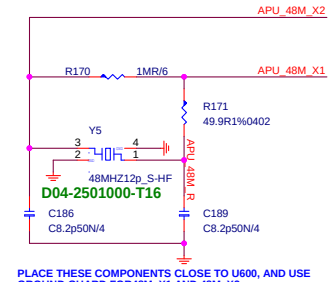


	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

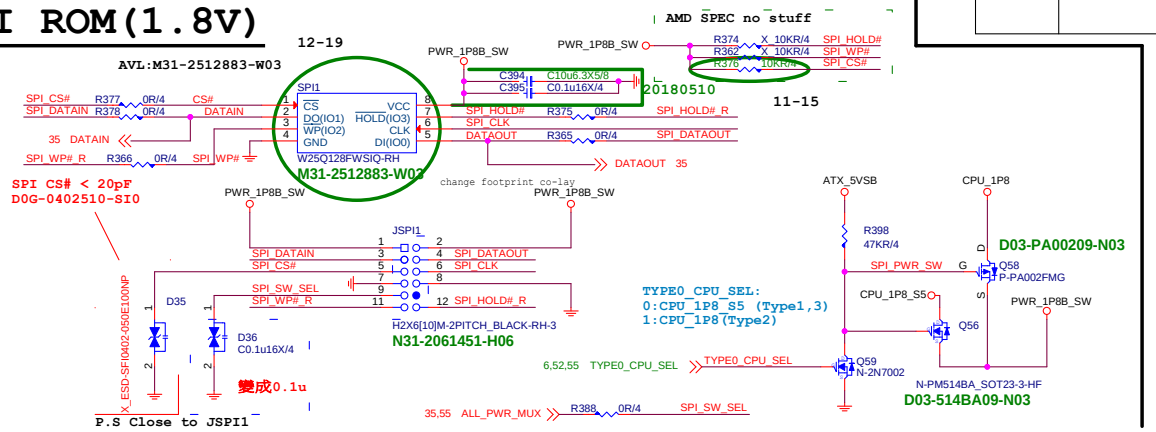


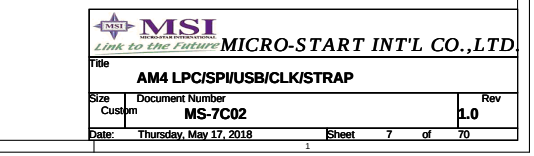
	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

Schematic Cfg	Project	
CFG-7C02-**-Arsenal Gaming	V	A



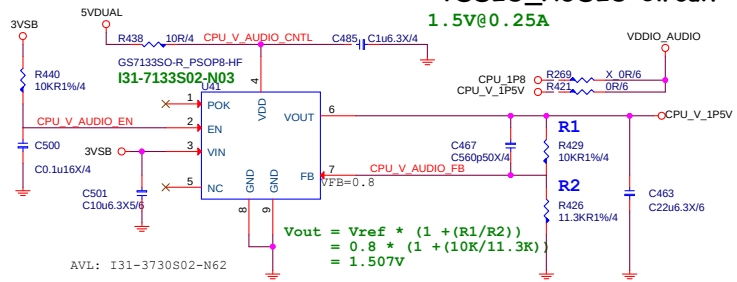
SPI ROM(1.8V)

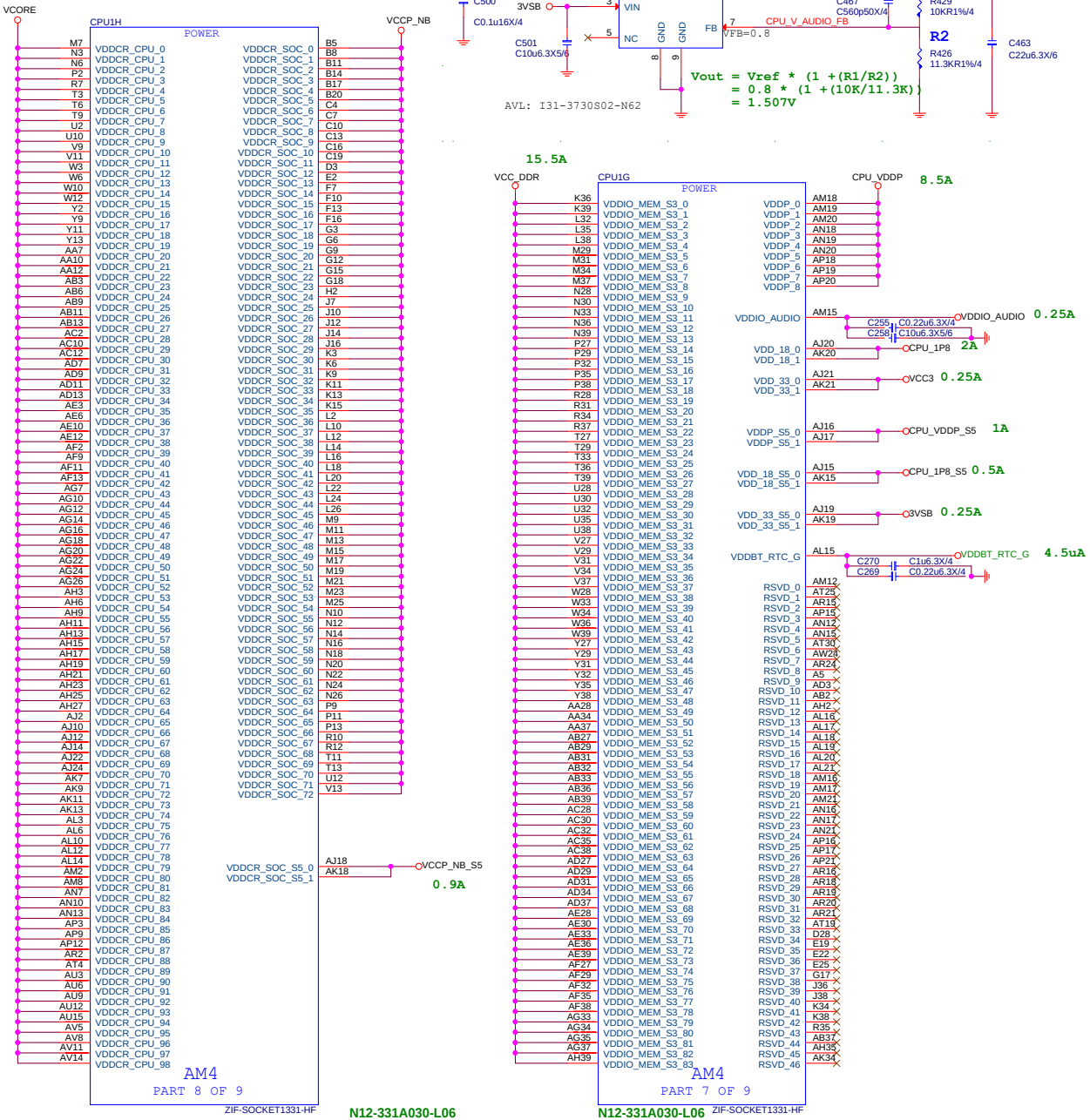




VDDIO_AUDIO Circuit

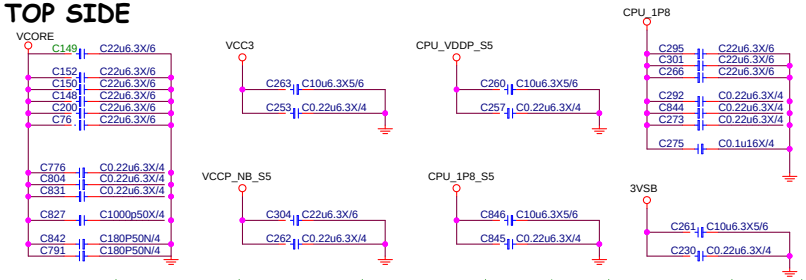
1.5V@0.25A



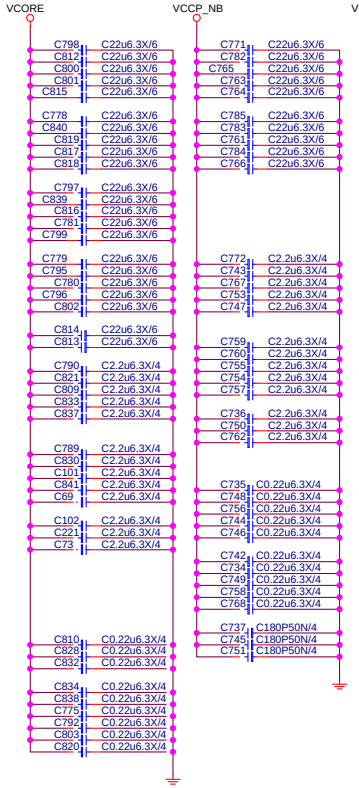


15.5A

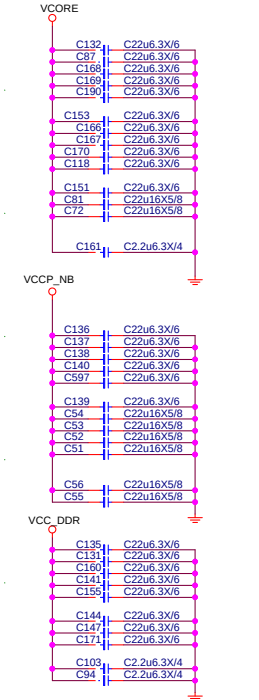
TOP SIDE



BOTTOM SIDE



TOP CAVITY



MICRO-START INT'L CO.,LTD.

Link to the Future

Title	08 AM4 Power/VDDIO_AUDIO Power	
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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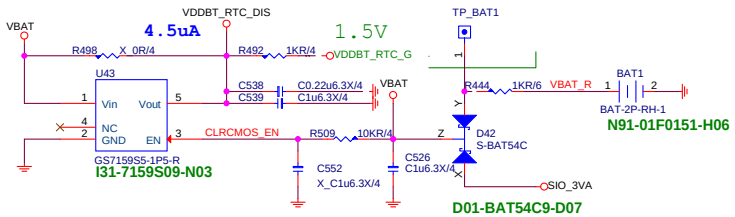
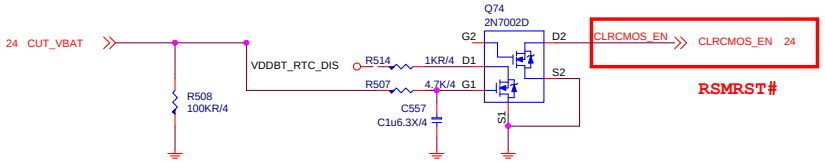
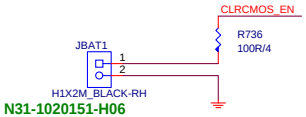
RTC & Clear CMOS Circuit

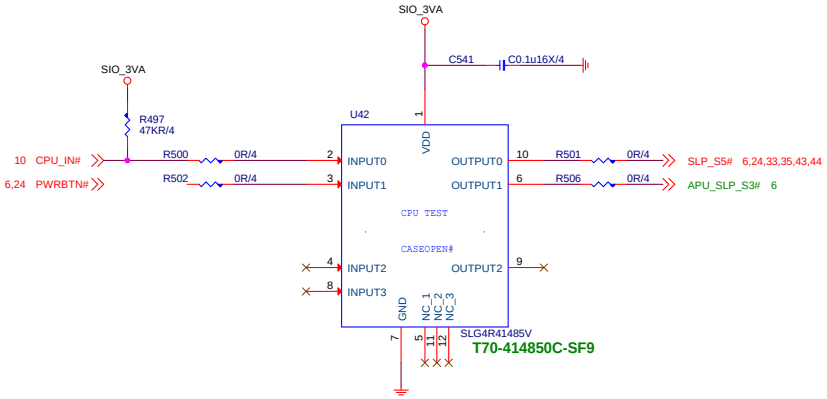
Placement Bottom Side



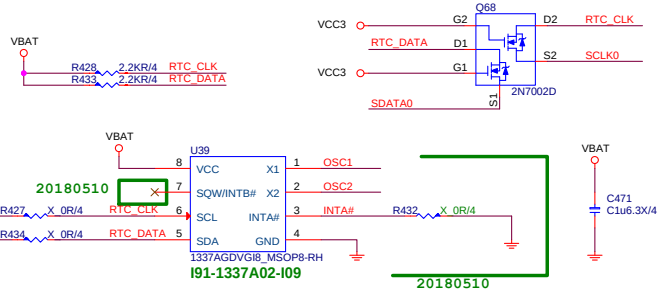


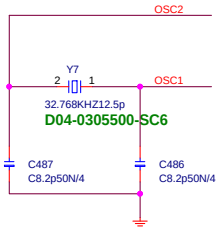
11-17





RTC Backup





MICRO-START INT'L CO.,LTD.

Title: RTC/Clear CMOS/RTC Power		
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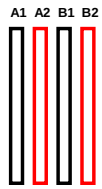
MSI MICRO-STAR INTERNATIONAL
Link to the Future MICRO-START INT'L CO.,LTD.

Title	AM4 GND	
Size: Custom	Document Number: MS-7C02	Rev: 1.0
Date: Thursday, May 17, 2018	Sheet 10 of 70	



DIMMA1A

DIMMA2A

DDRIV-288P_BLACK-RH-21

N13-2880581-L06

DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

Schematic Cfg	Project	
CFG-7C02-***-Arsenal Gaming	V	A

MICRO-START INT'L CO.,LTD.

Title: DDR4 DIMM CH-A

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A1 A2 B1 B2
DIMMB1A
DDRIV-288P_BLACK-RH-21
N13-2880581-L06
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMMB2A
DDRIV-288P_BLACK-RH-21
N13-2880581-L06
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
VCC_DDR
VCC3_SPD
Schematic Cfg
Project
CFG-7C02-***-Arsenal Gaming
V
A
MSI
Link to the Future
MICRO-START INT'L CO.,LTD
Title
DDR4 DIMM CH-B
Size
Custom
Document Number
MS-7C02
Rev
1.0
Date: Thursday, May 17, 2018
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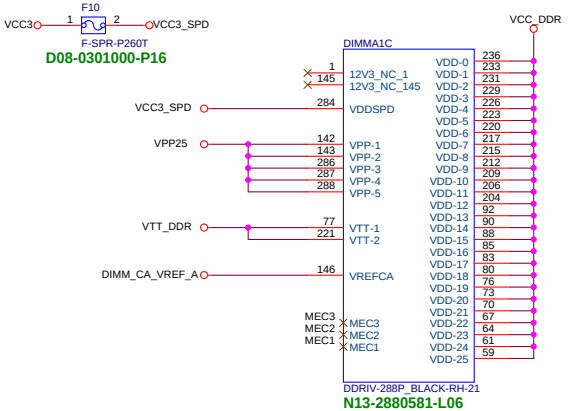
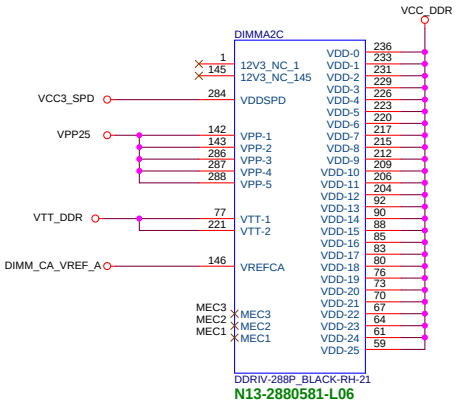
avl:D08-0301100-B07

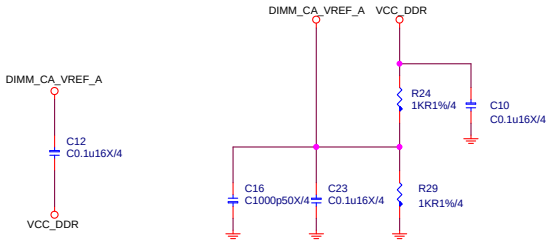


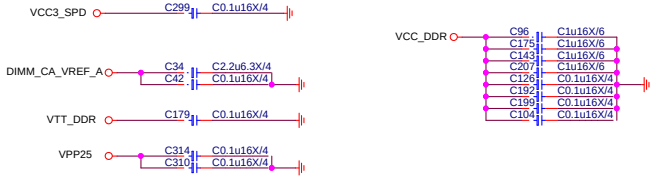
DIMM SLOT PN BY SPEC

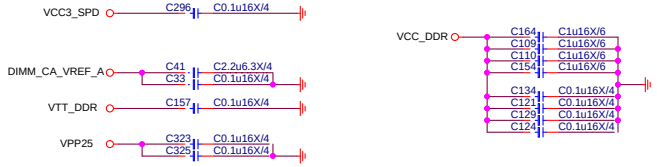


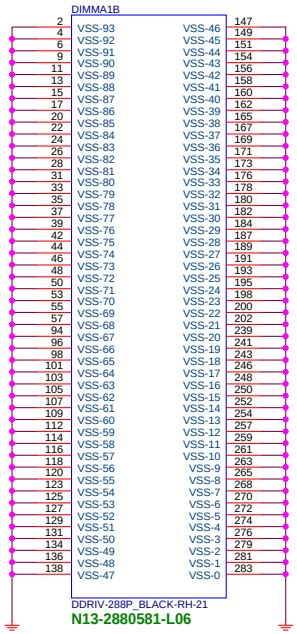
DDR VREF

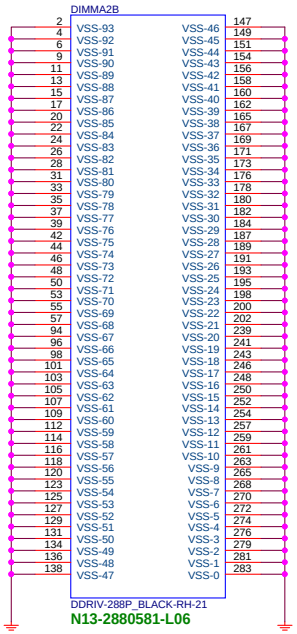
(place resistors close to DIMMs)











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Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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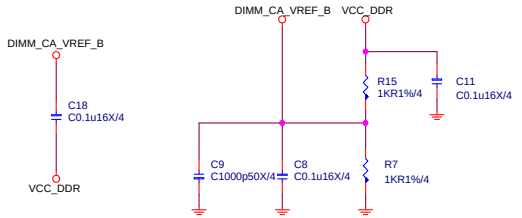
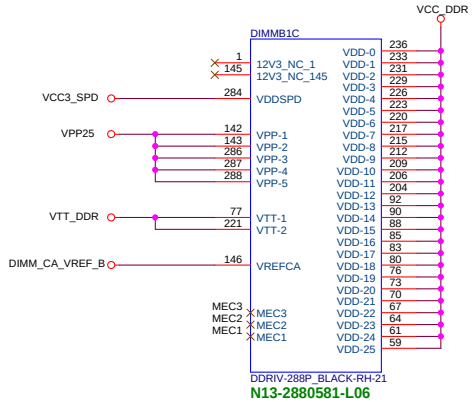
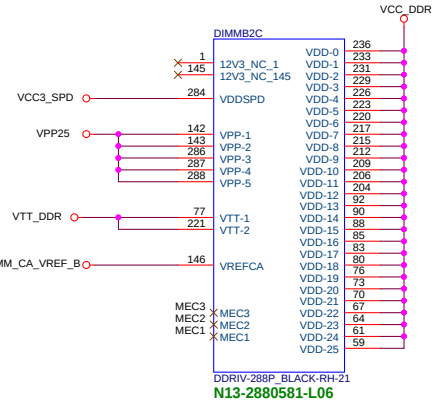
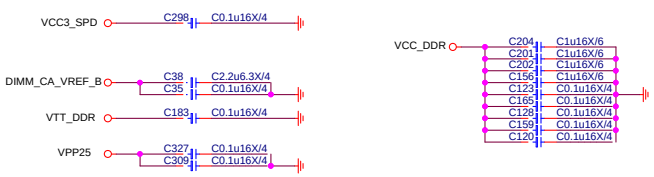
DDR VREF

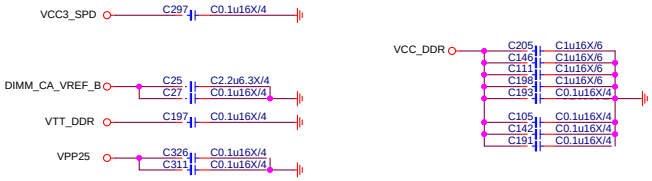
(place resistors close to DIMMs)

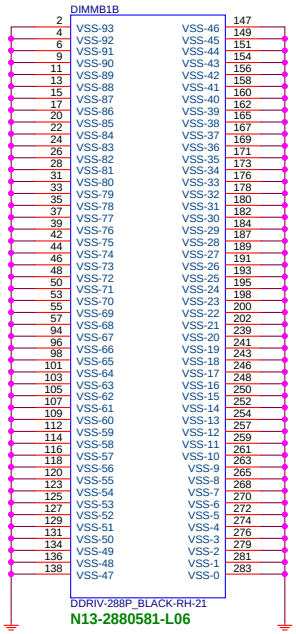


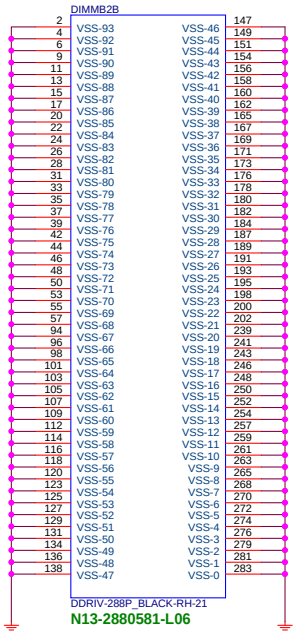












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Title	DDR4-POWER/GND-2	
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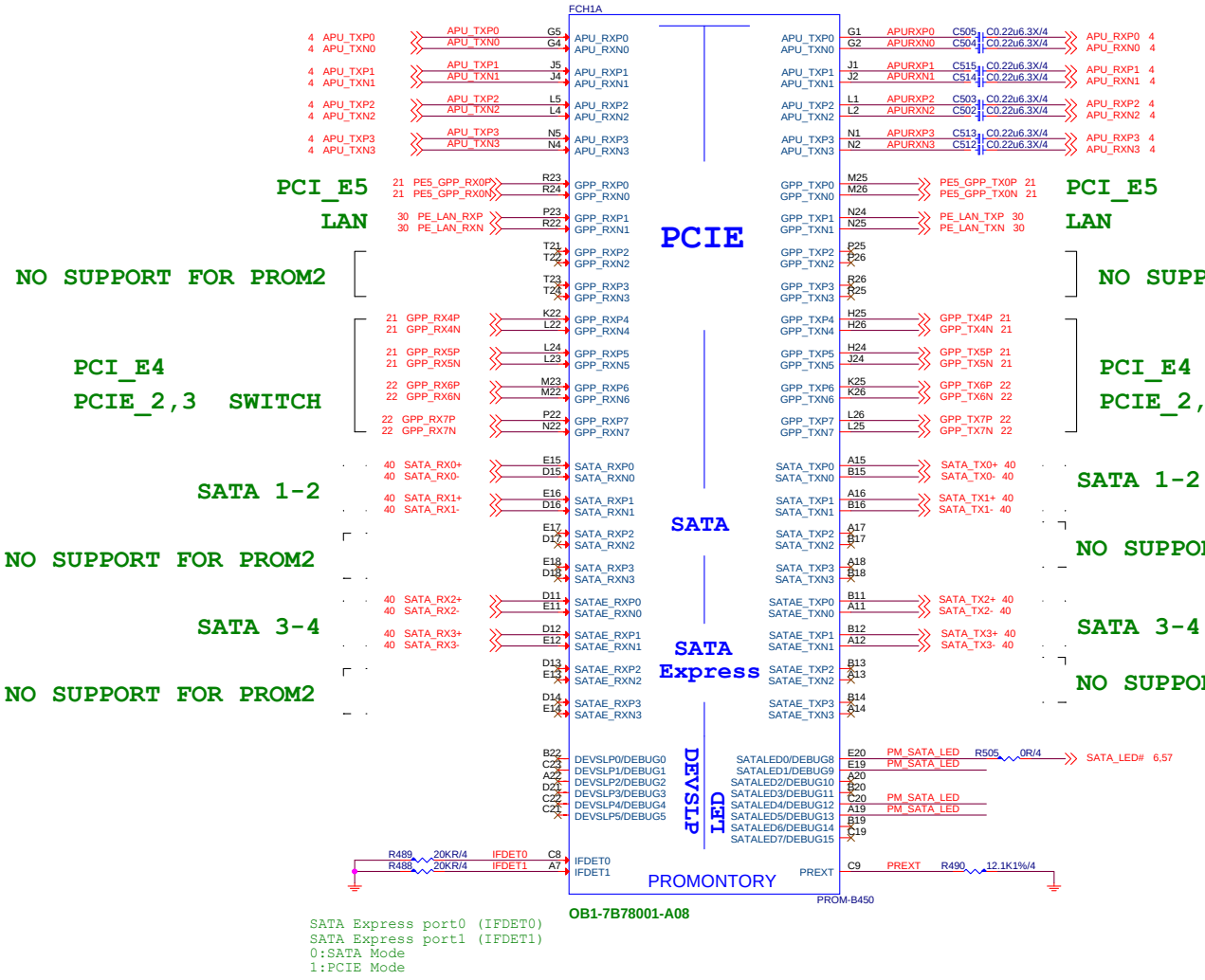

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

MSI MICRO-START INT'L CO.,LTD.

Title: Promontory-PCIE/SATA/SATAE

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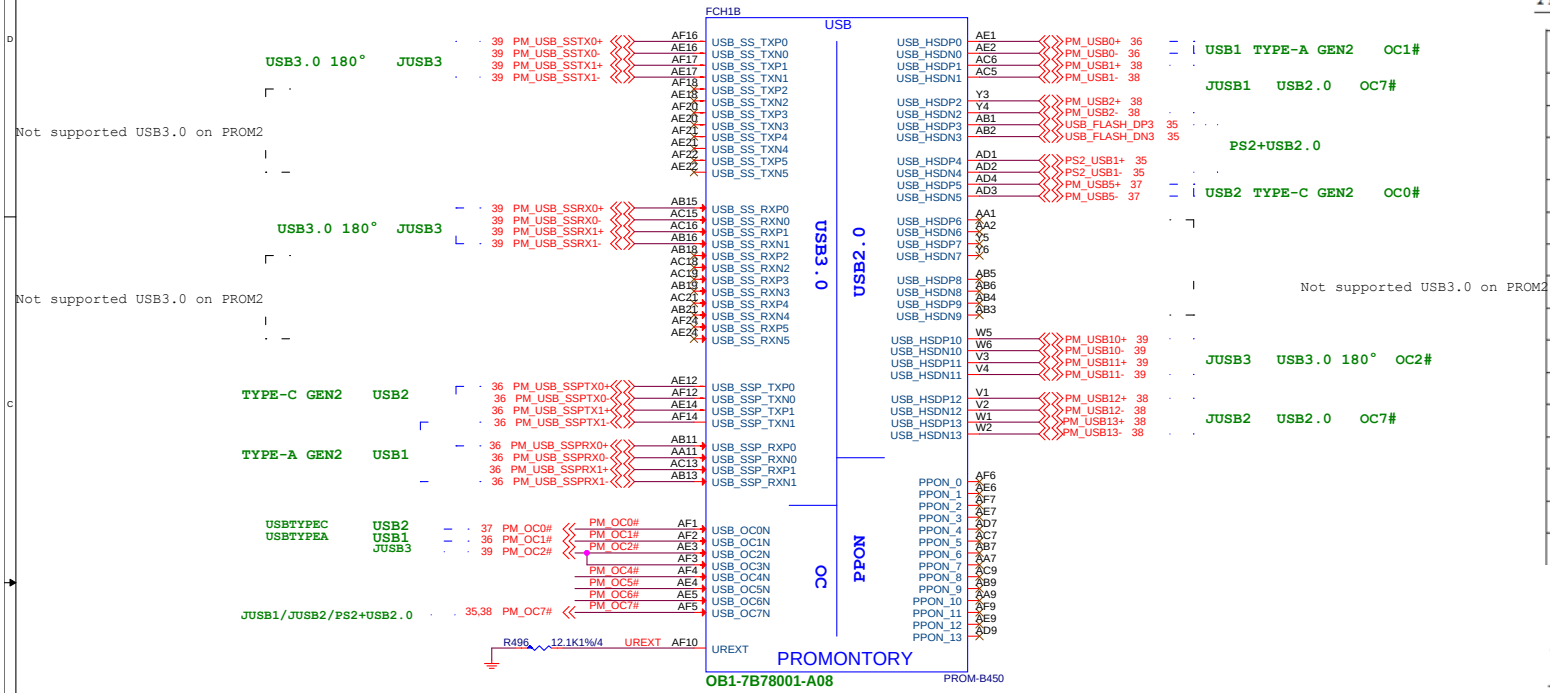

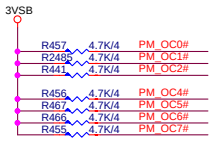

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

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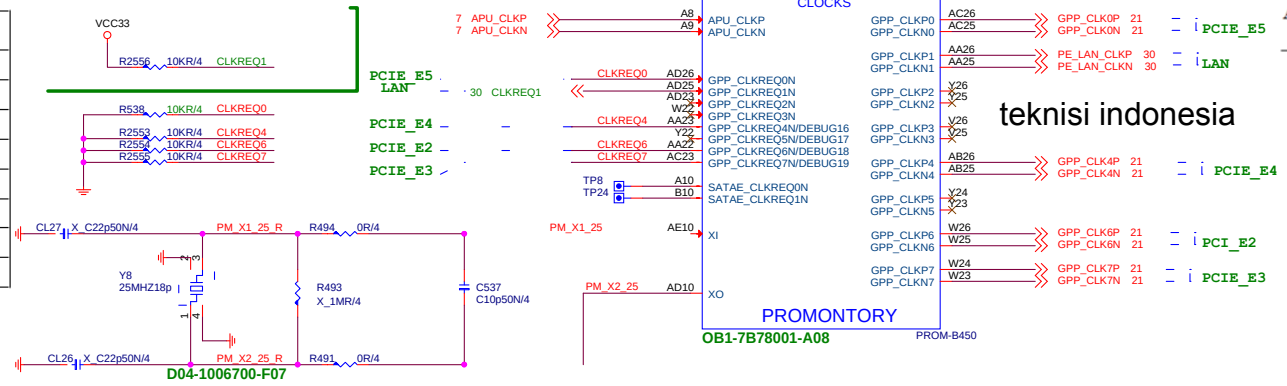
移除預留CLKREQ到solt之間 PULL HIGH/PULL LOW電阻

GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N



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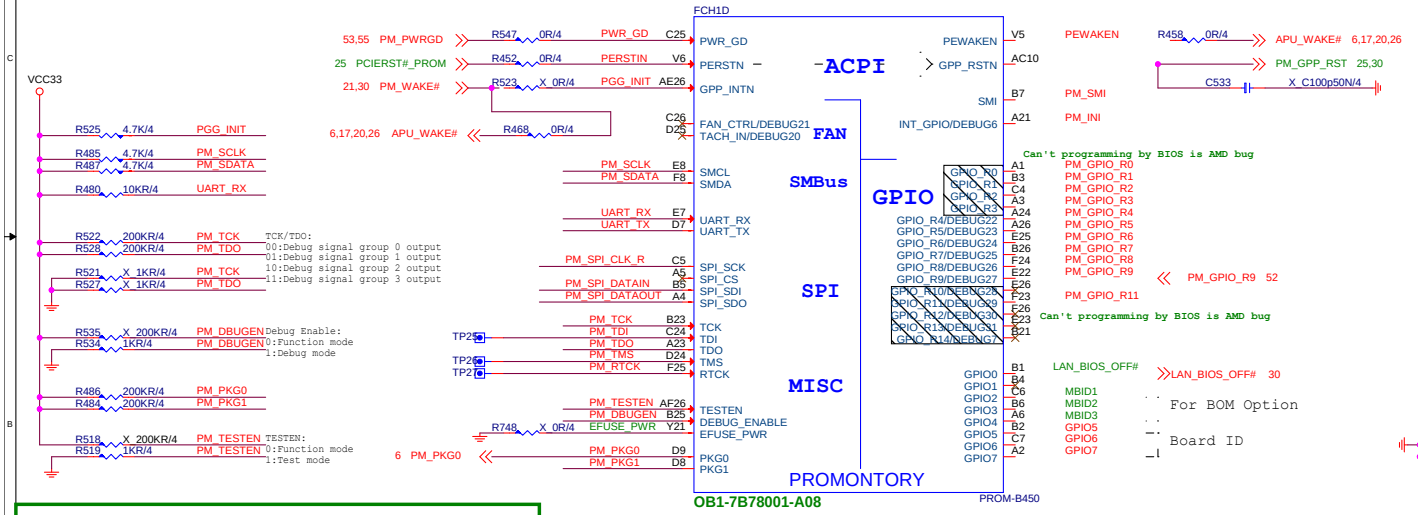
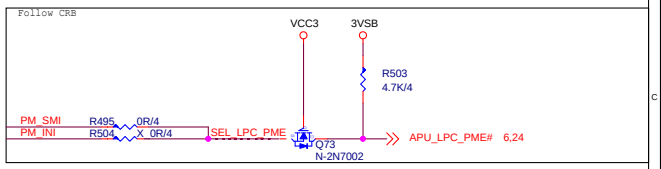
Appendix C Port Mapping for Different Bus Models

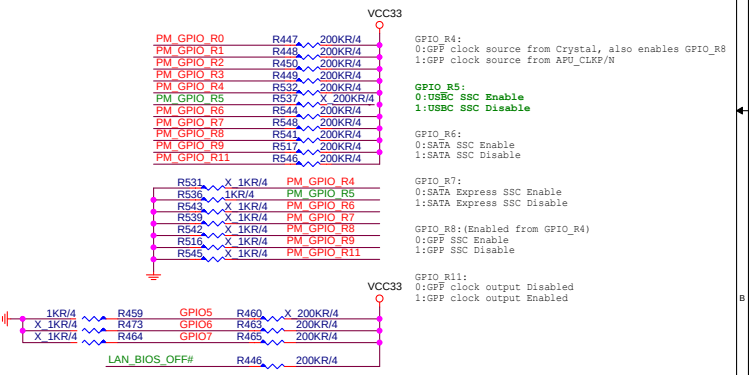
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

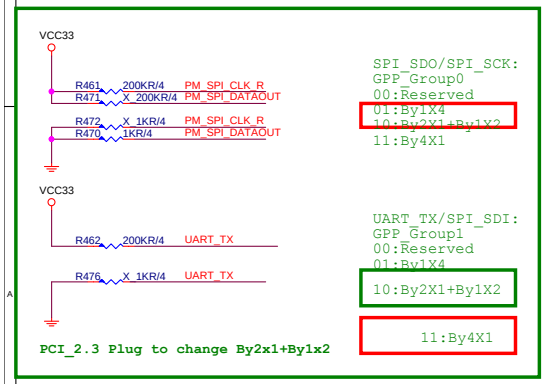
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

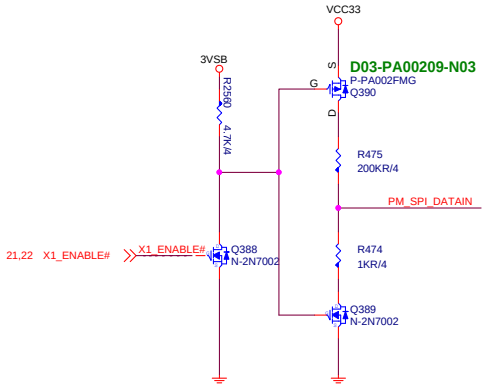
CLK2.3不能用
CLK1-3不能用



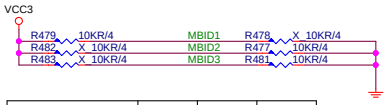








BOM OPTION



	MBID1	MBID2	MBID3
B45-TOMAHAWK 601-7C02-A01	1	0	0
	0	0	0
	1	1	0

Schematic Cfg	Project	
CFG-7C02-**	V	A

MICRO-START INT'L CO.,LTD.

Title: Promontory-CLK/ACPI/GPIO

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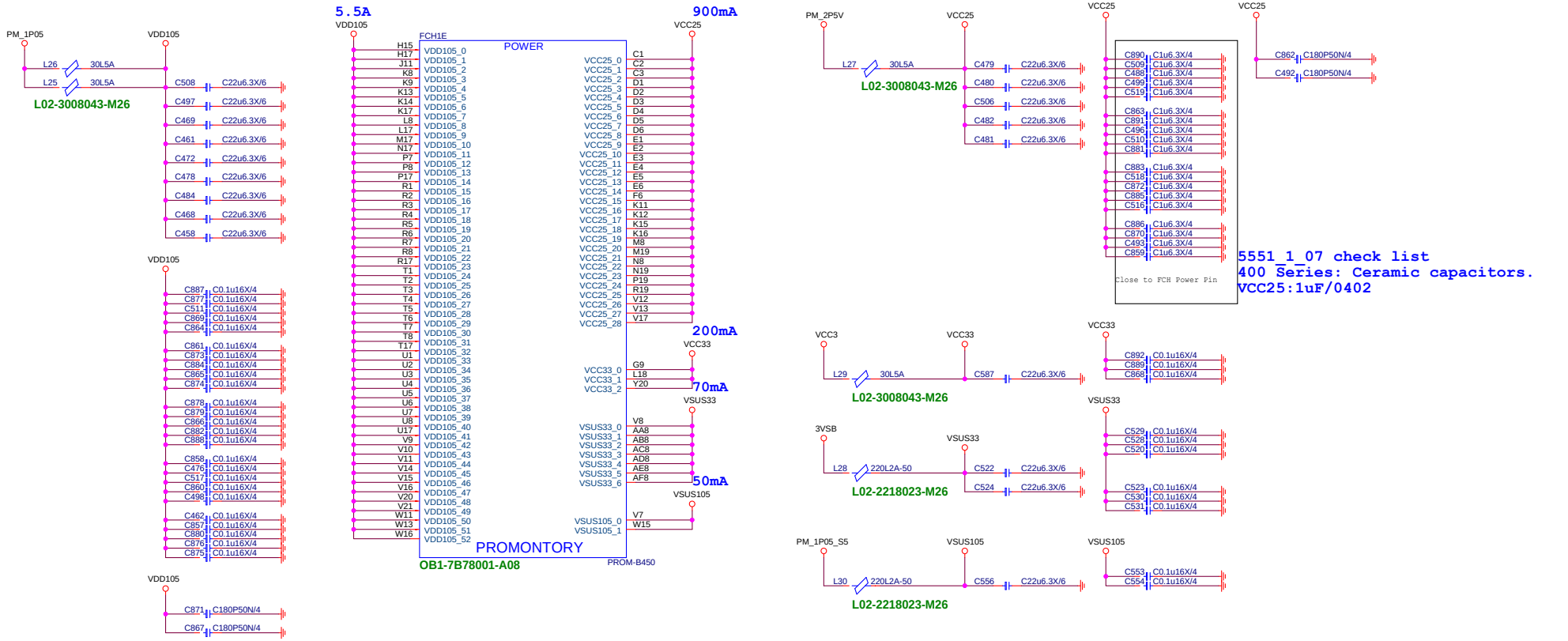

MICRO-START INT'L CO.,LTD.

Title: Promontory-Power		
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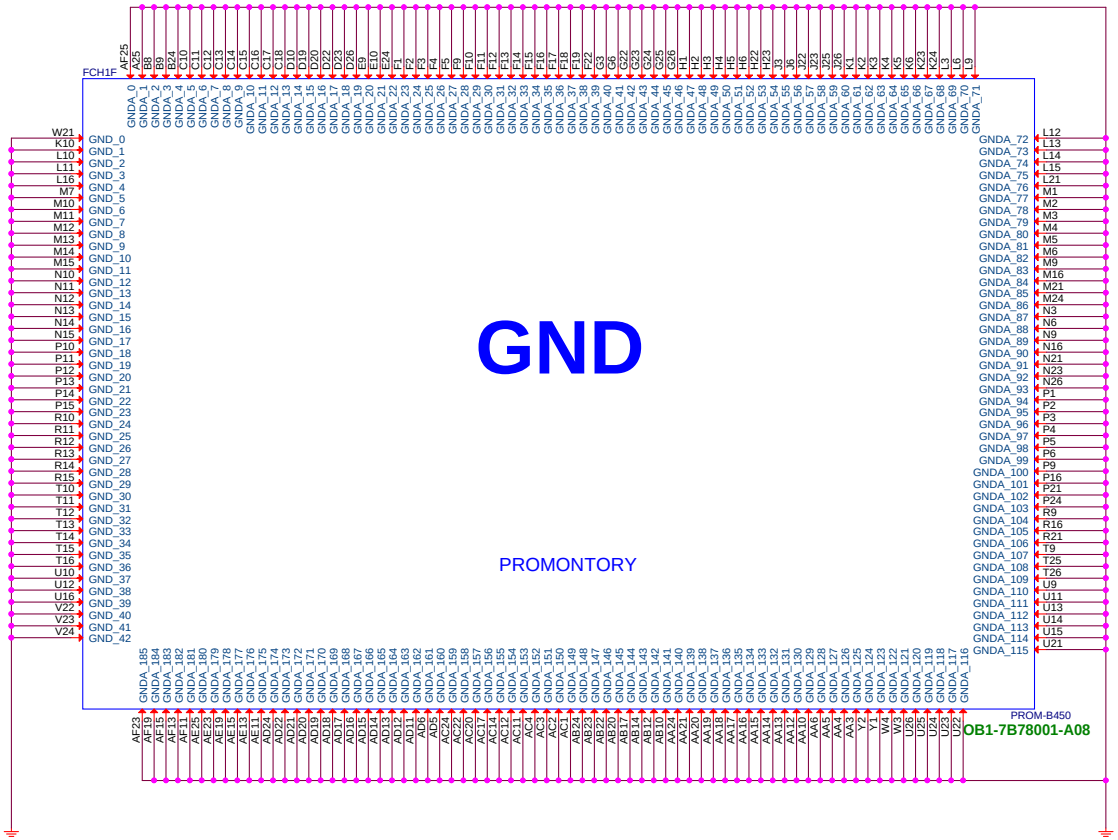

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Title: Promontory-GND			
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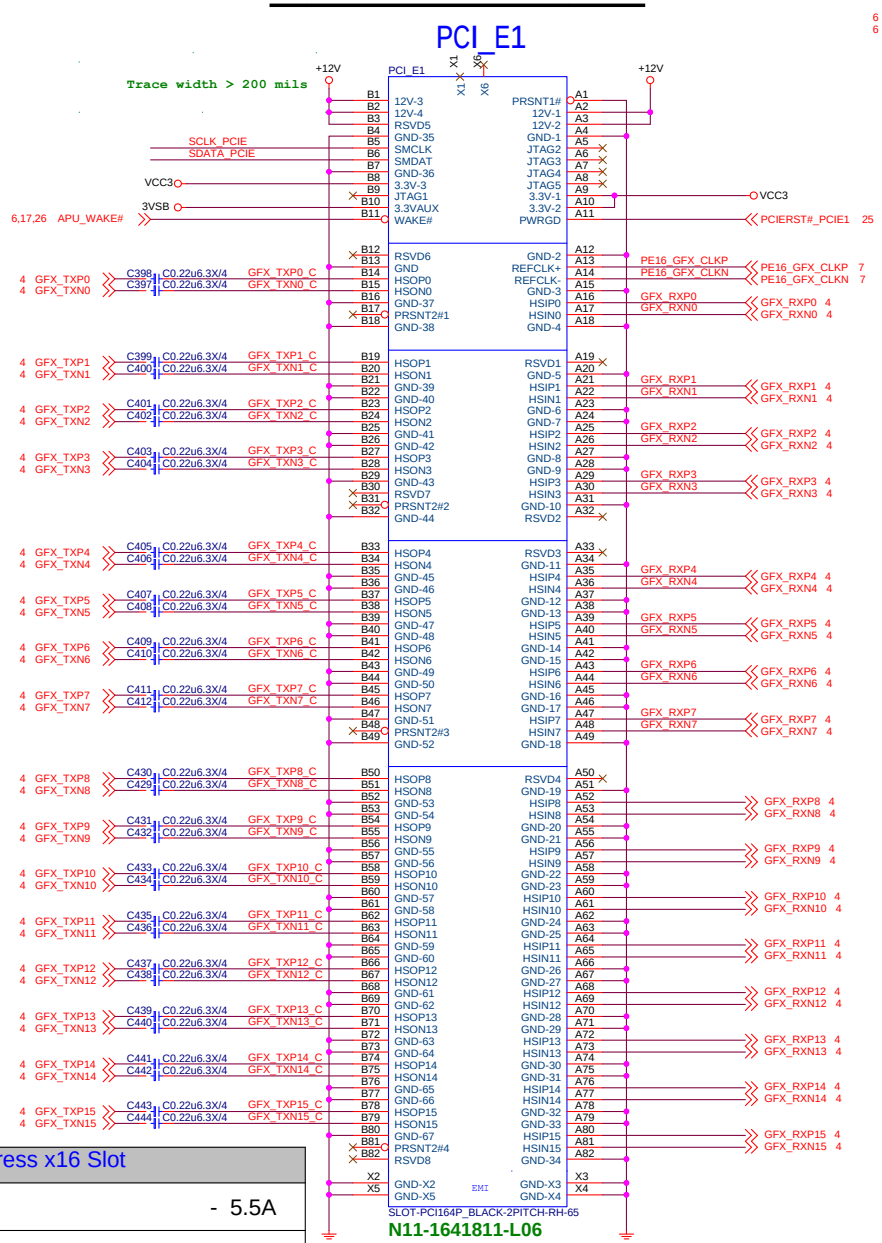
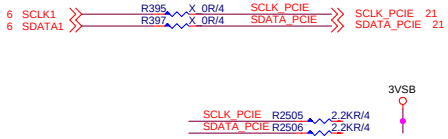
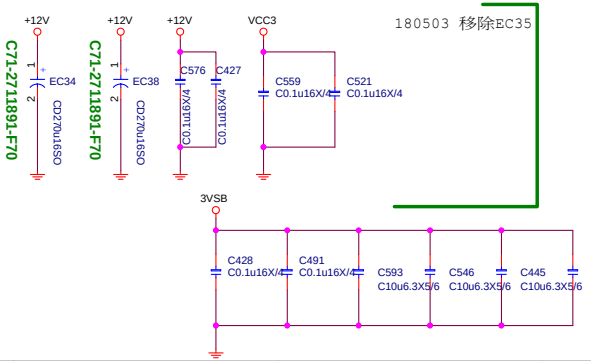
PCI EXPRESS x16 Slot







PCI Express x16 Slot		
+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

PCI Express x8 Slot		
+12V		- 5.5A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Title	PCI_E1/E4 X16/X8	
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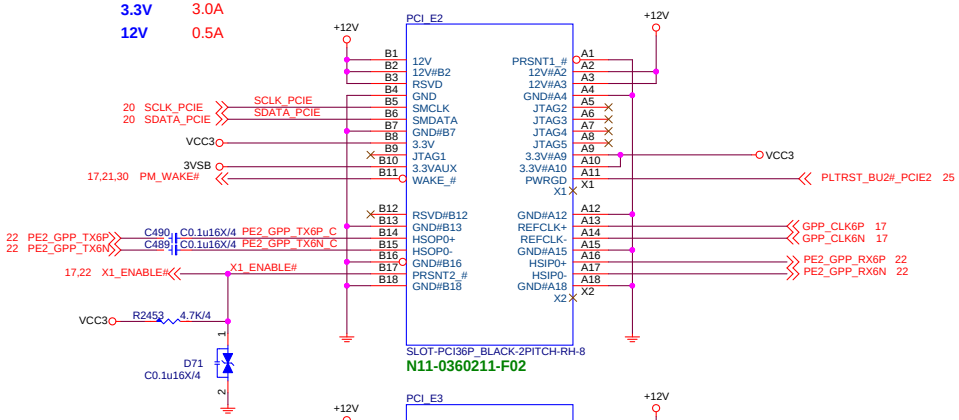
PCIEX1 12V 0.5A
3.3V weak 375mA

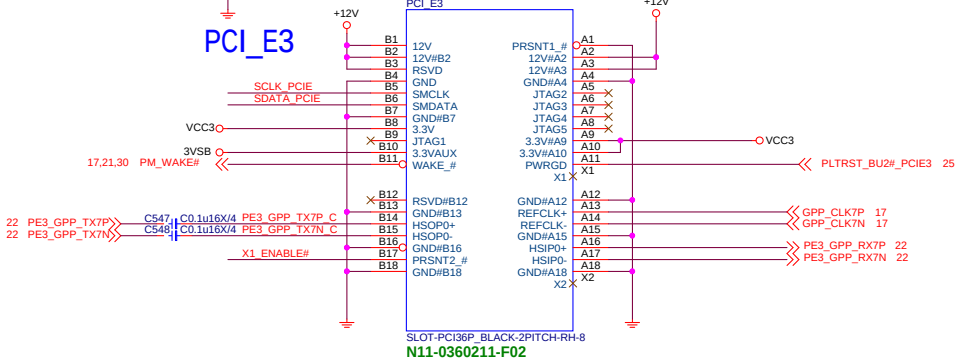
PCI_E2

3.3V 3.0A
12V 0.5A



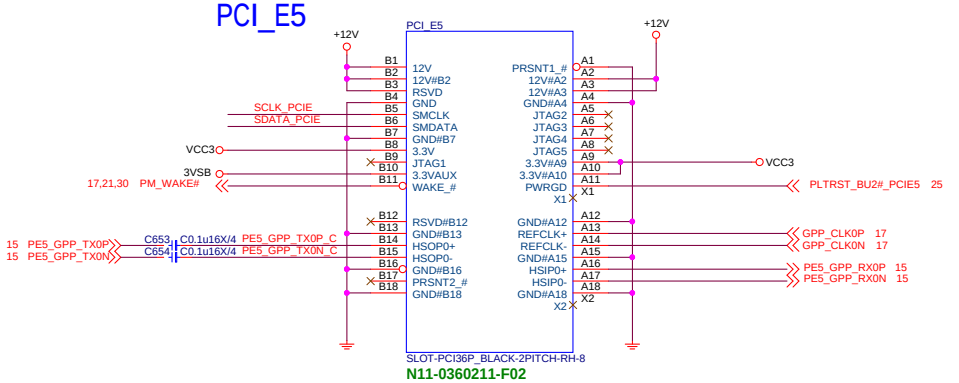
N11-0360211-F02

PCI_E3



N11-0360211-F02

PCI_E5



N11-0360211-F02

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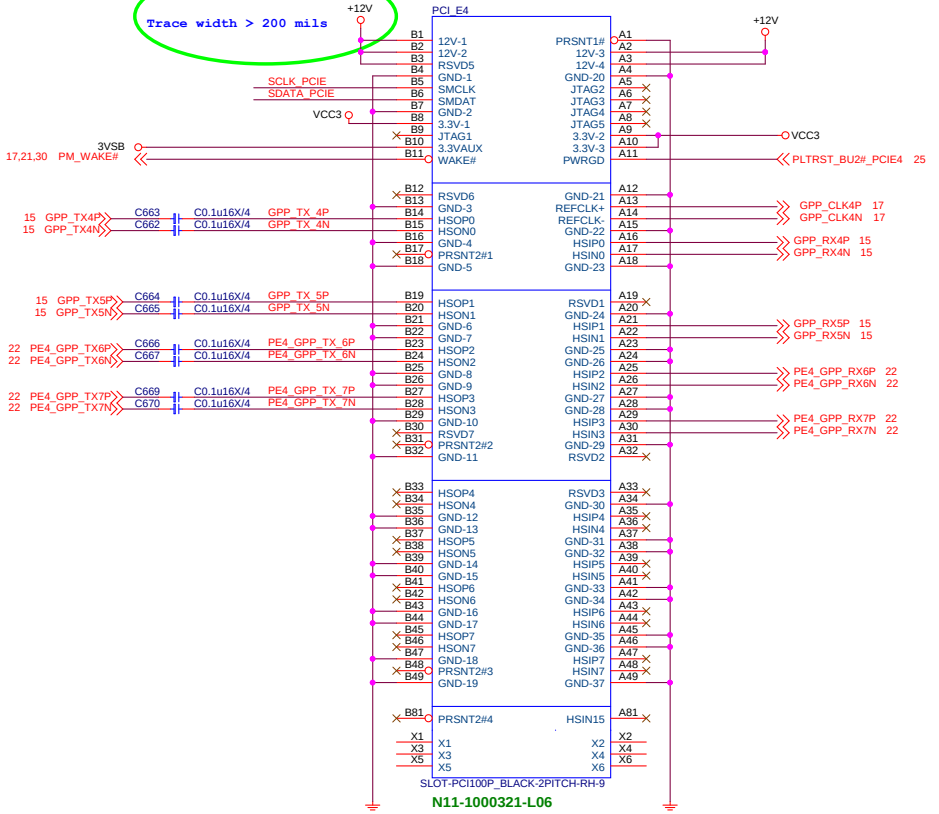

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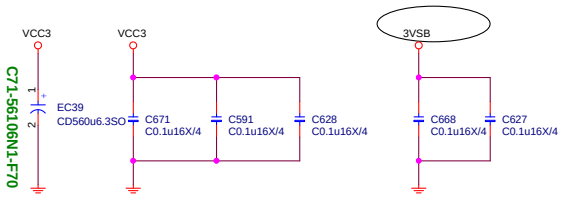

PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

Schematic Cfg	Project	
CFG-7C02-***-Arsenal Gaming	V	A

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Title	PCI_E2_E3_E5/E4 X1/X4	
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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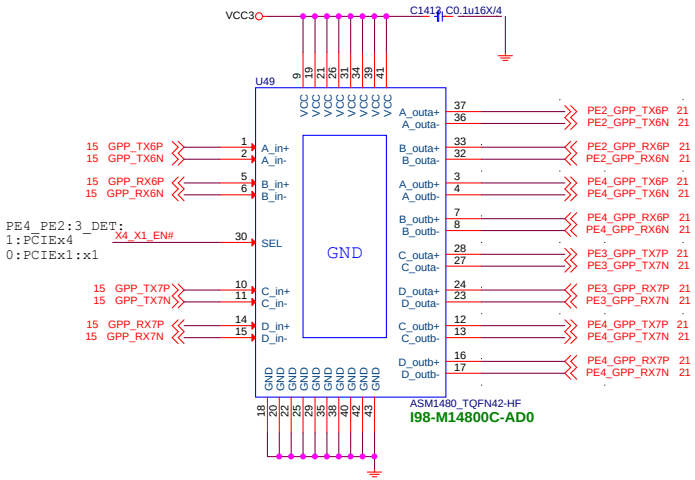
PCI_E4 and PCIE_2 :3 and Switch



SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-

PCIE_2

PE4

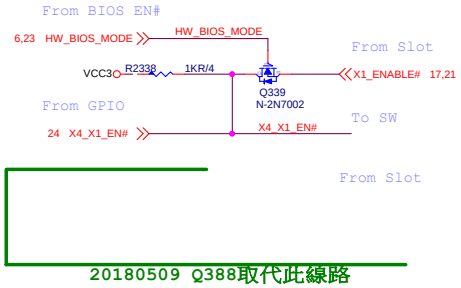
PCIE_3

PE4

UART_TX/SPI_SDI:
GPP_Group1
00:Reserved
01:By1X4

10:By2X1+By1X2
11:By4X1 (def)

PCIE Lanes control circuit



	HW_BIOS_MODE	Q339	Q381	X1_ENABLE#	PM_SPI_DATAIN
Manual x4	**L**	OFF	OFF	**X**	11:By4x1 (def)
Manual x2, x1 ,x1	**L**	OFF	OFF	**L**	10:By2x1+By1x2
HW x4	**H**	ON	ON	H	11:By4X1 (def)
H/W x2,x1,x1	H	ON	ON	**L (Stuff PCIE_1)**	10:By2x1+By1x2

MICRO-START INT'L CO.,LTD.

Title	PCIE Switch X4 / M2_2	
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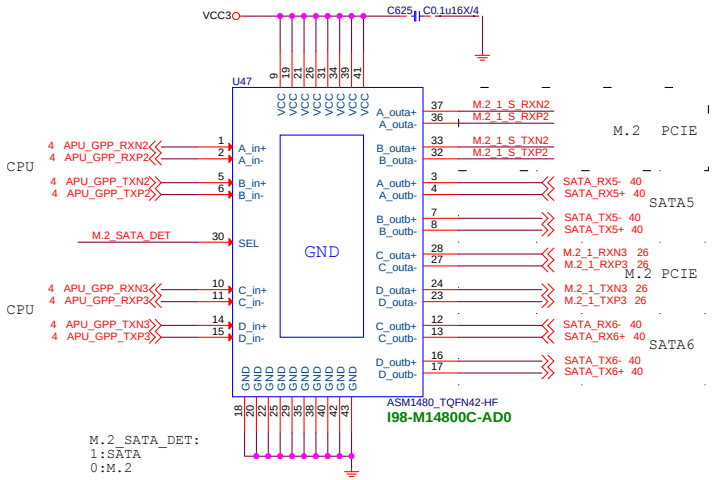
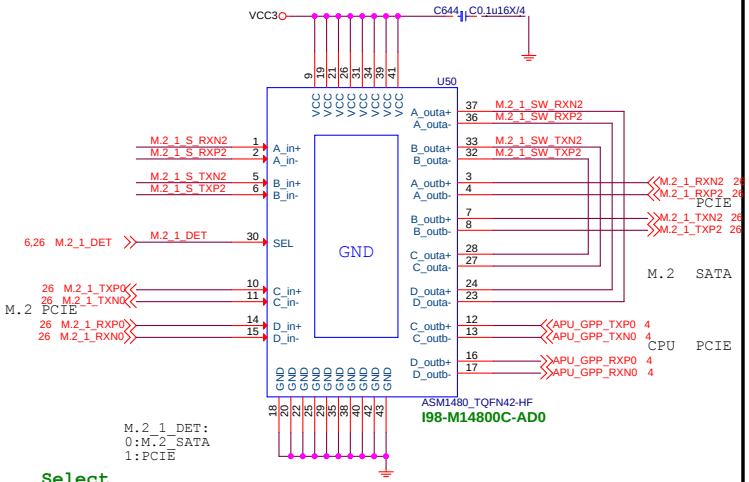
M2_1 and SATA5 6 Switch



M.2_SATA_DET:
1:SATA
0:M.2

(Default for SATA)

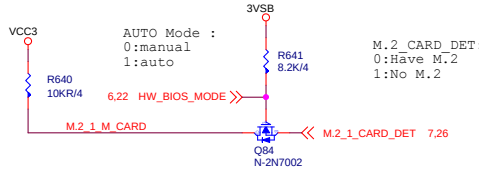
SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-

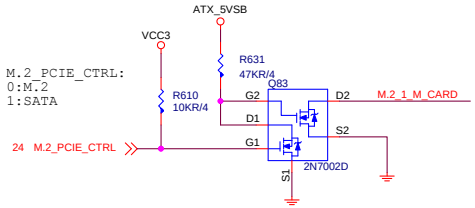


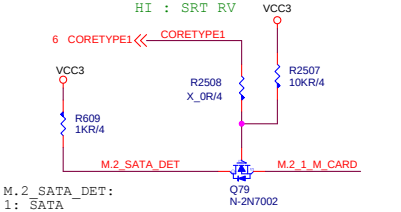
M.2_1_DET:
0:M.2_SATA
1:PCIE

Select
M2 : PCIE or SATA
(Default for PCIE)

	AUTO Mode	SATA CON	M.2(PCIE)	M.2(SATA)
HW_BIOS_MODE	1		0	0
M.2_PCIE_CTRL	1		0	0
M.2_1_CARD_DET		1	0	0
M.2_DET		X	1	0







CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1

MICRO-START INT'L CO.,LTD.

Title	23 PCIE Switch M2_2/SATA	
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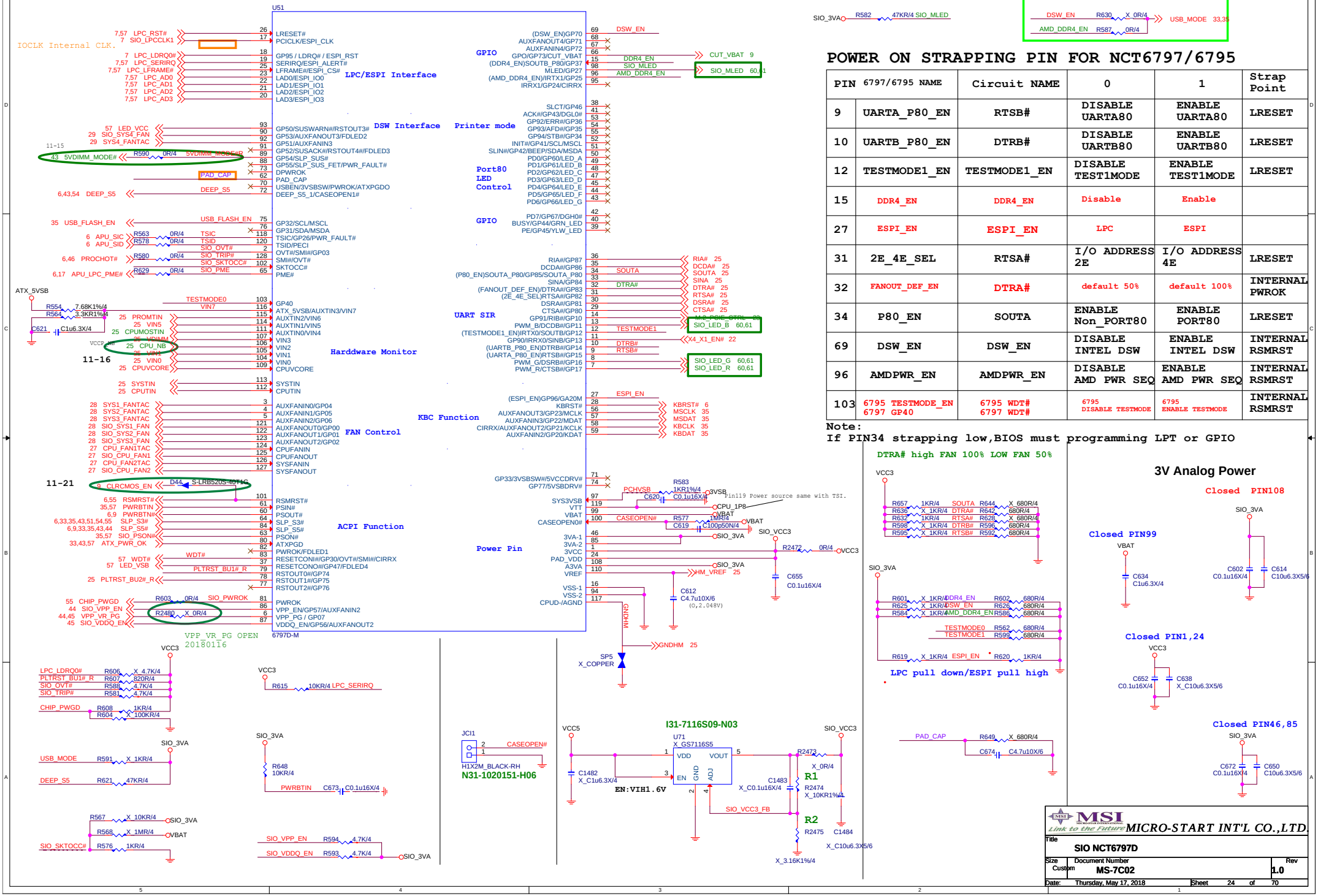

POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

Title	SIO NCT6797D
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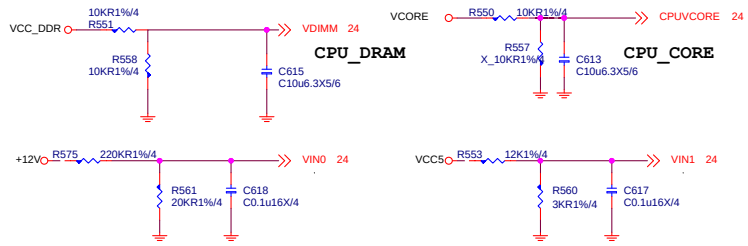
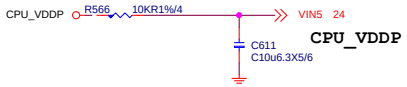
MICRO-START INT'L CO.,LTD.

HW Monitor - Voltage

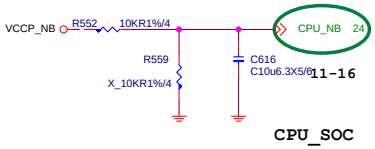
SIO HM Voltage over 2.048V will not detect



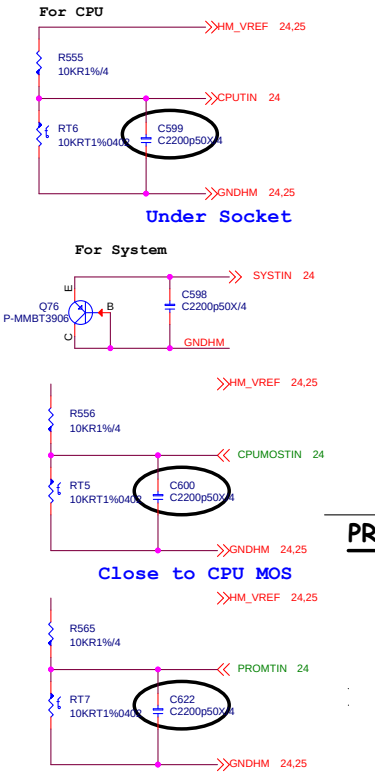
Power Fault detect through VIN0,VIN1,VIN2



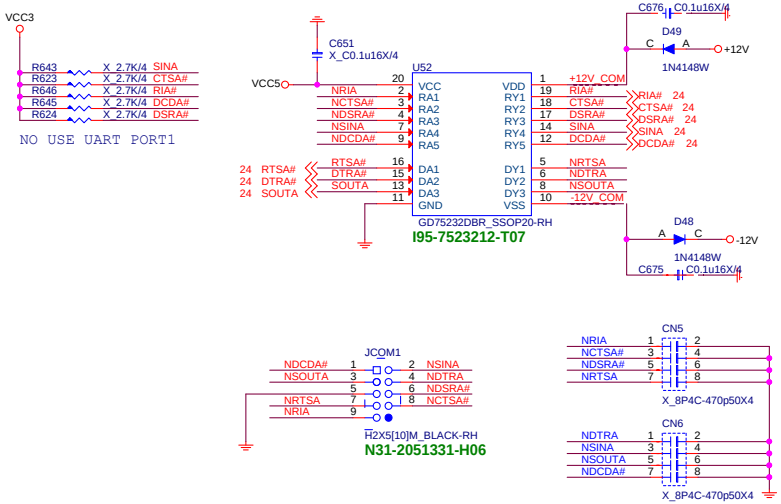
Inform BIOS disable VIN2 with Power Fault



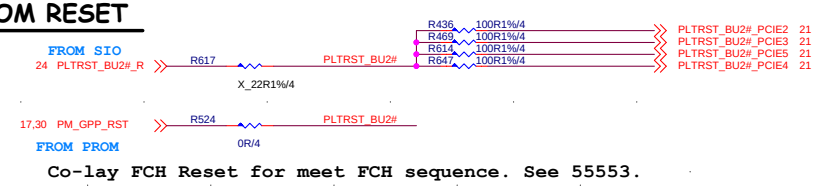
TEMP SENSOR



COM PORT

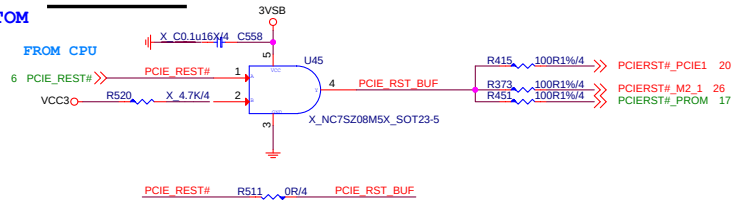


PROM RESET

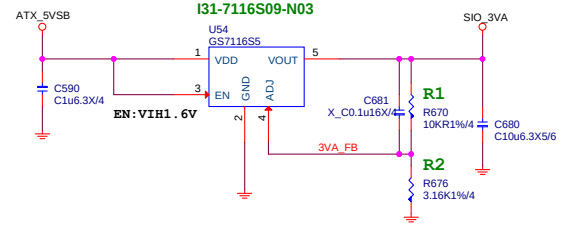


Co-lay FCH Reset for meet FCH sequence. See 55553.

CPU RESET



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

PARALLAL PORT

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Title	SIO HWM/COM		
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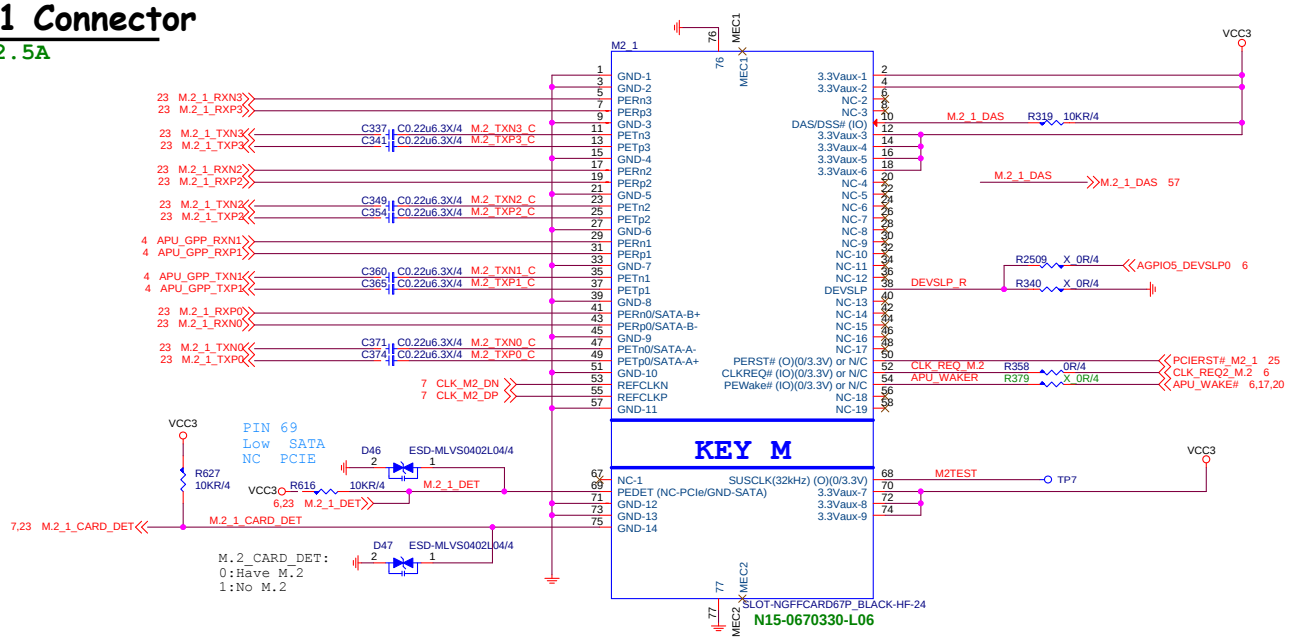
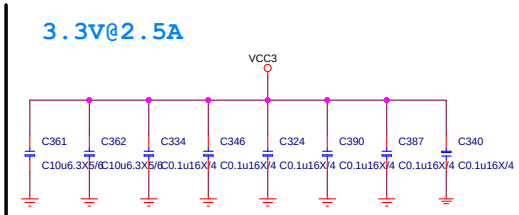
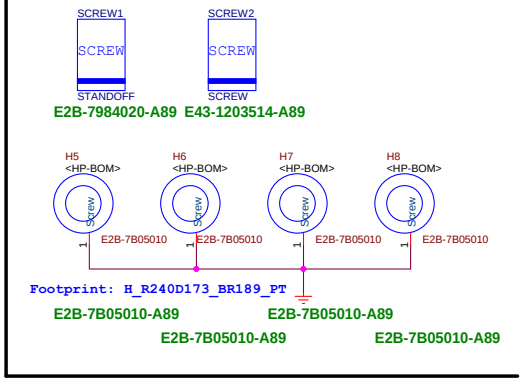
M.2_1 Connector

3.3V@2.5A







Schematic Cfg	Project	
CFG-7C02-**-Arsenal Gaming	V	A

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MICRO-START INT'L CO.,LTD.

Title: M.2_1		
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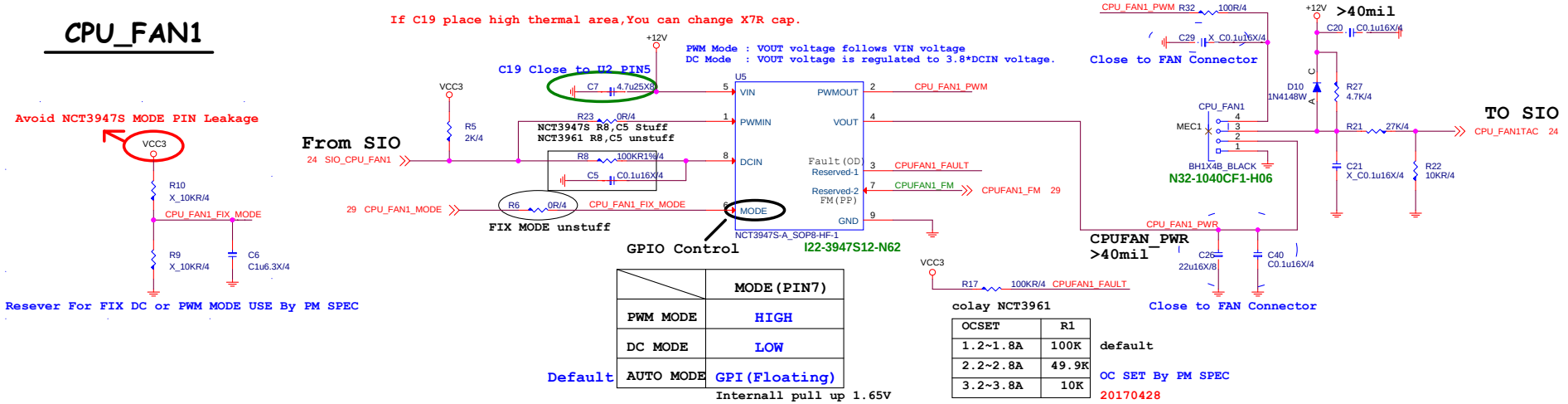
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE
2.FM:BIOS can read FAN PWM/DC MODE

CPU_FAN1



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

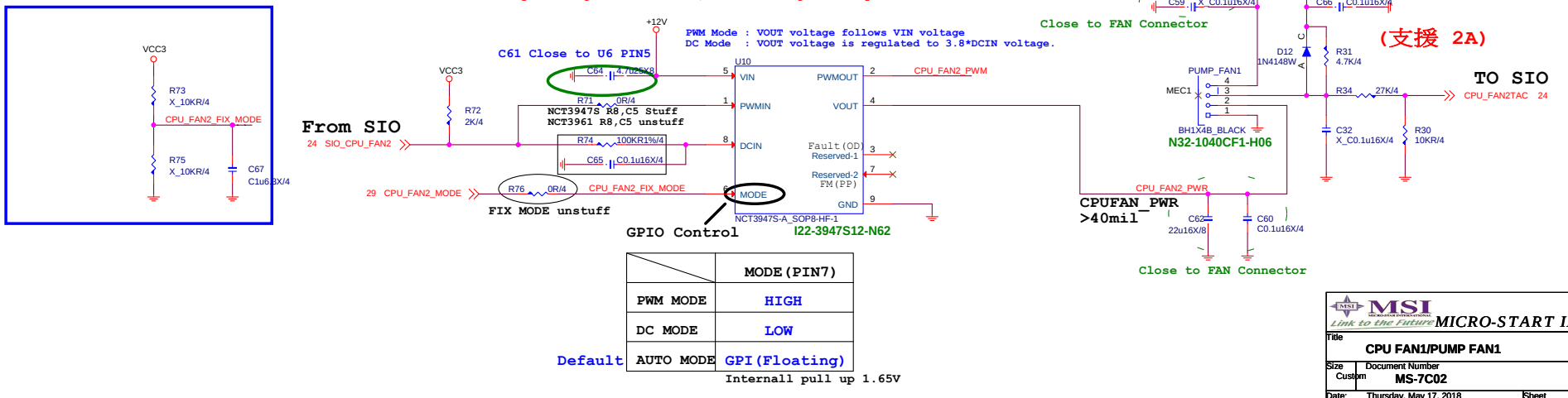
Internall pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	
3.2~3.8A	10K	OC SET By PM SPEC

20170428

PUMP_FAN1



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-START INT'L CO.,LTD.

Title	CPU FAN1/PUMP FAN1	
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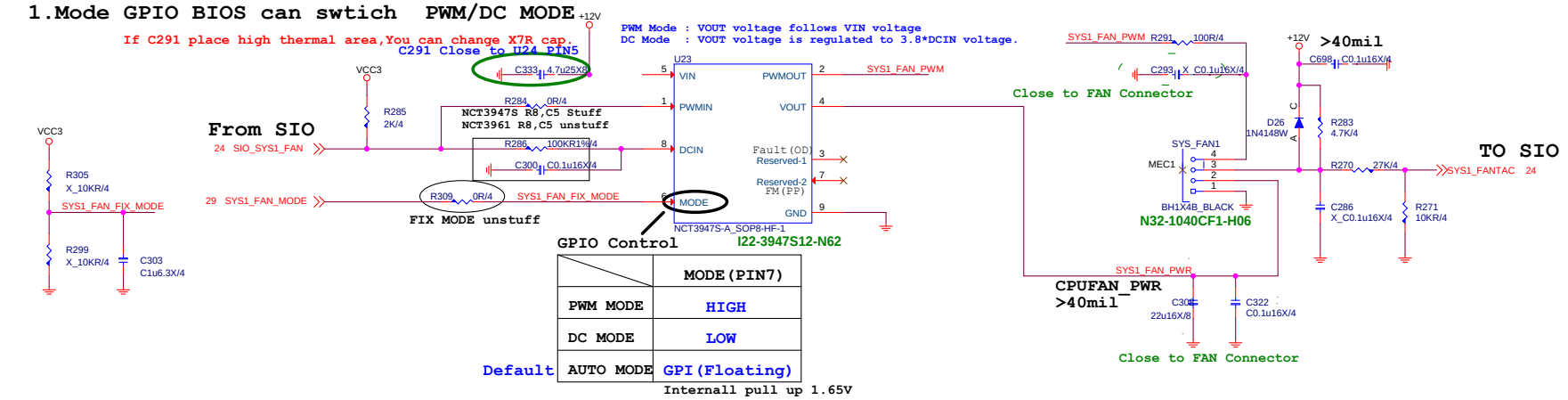
SYSFAN

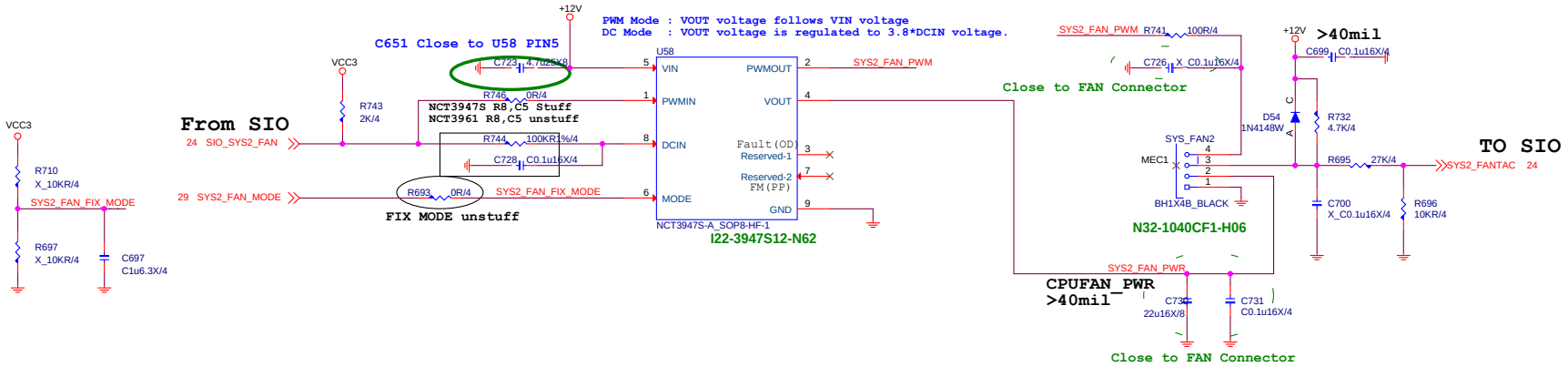
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

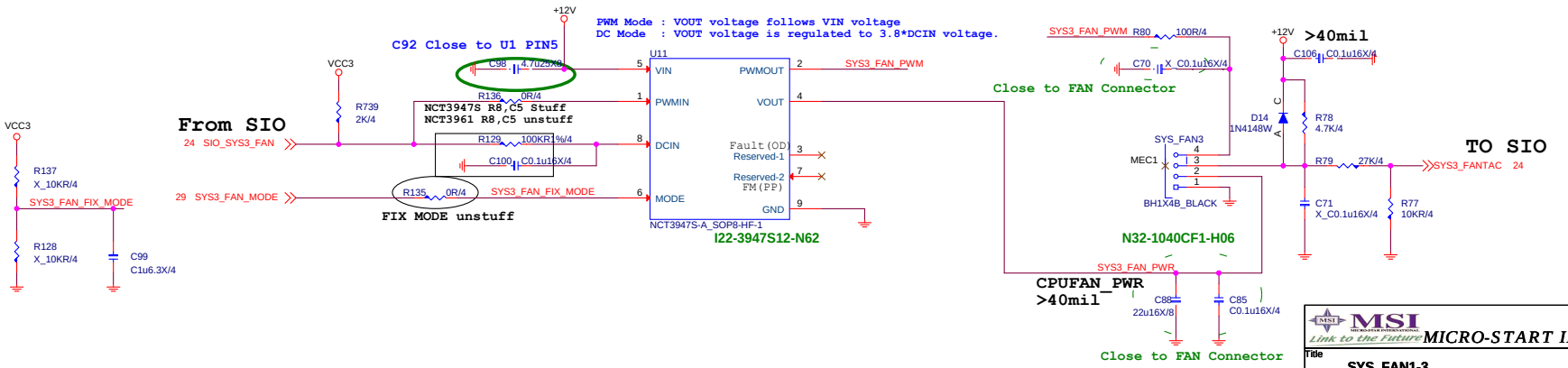
1.Mode GPIO BIOS can swtich PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





MICRO-START INT'L CO.,LTD.

Title	SYS_FAN1-3	
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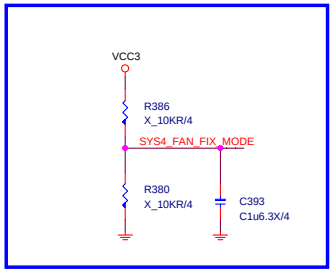
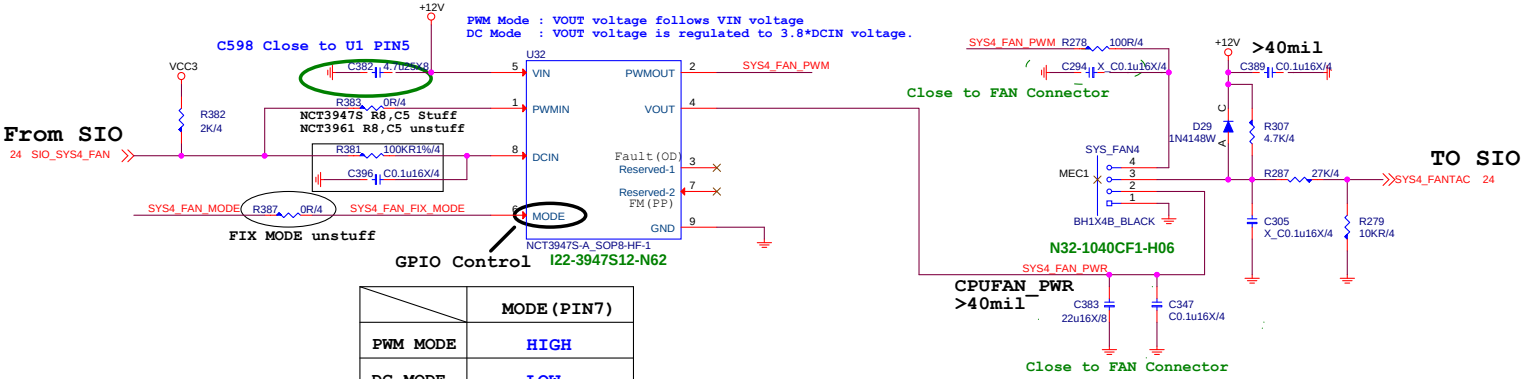
SYSFAN 4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area,You can change X7R cap.



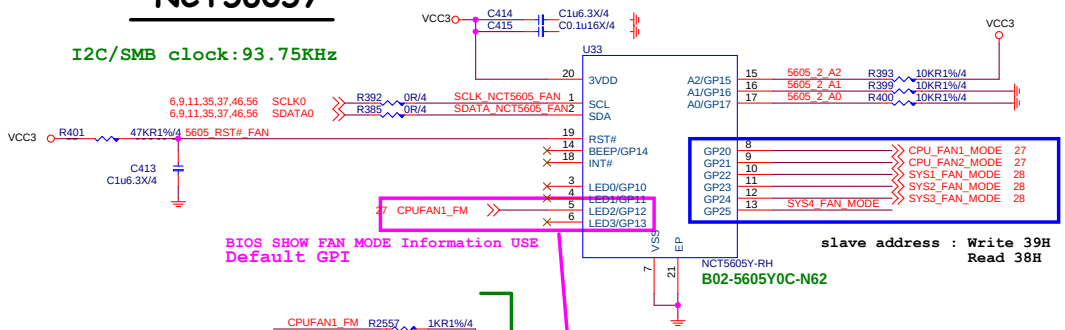


	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

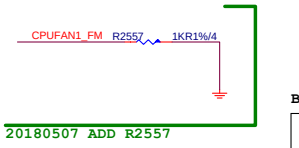
NCT5605Y

I2C/SMB clock:93.75KHz



BIOS SHOW FAN MODE Information USE
Default GPI

slave address : Write 39H
Read 38H



By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

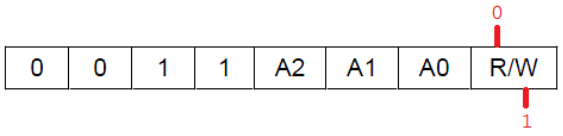
By PM Define FAN name

FAN MODE USE	FAN
GP20	CPUFAN1
GP21	CPUFAN2 PUMPFAN
GP22	SYSFAN1
GP23	SYSFAN2
GP24	SYSFAN3
GP25	SYSFAN4

1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:



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Title	SYS_FAN4/NCT5605Y	
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RTL8111H Giga LAN

VDD33 — RL14 X_1KR/4 LAN_WAKE#

Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).

VCC3 — RL16 1KR1%/4 — RL13 15K1%/4 — ISOLATEB

PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

LAN Connector

UL7

15 PE_LAN_TXP — CL19 C0.1u16X/4 — PE_LAN_TXP_C 13 HSIP
15 PE_LAN_TXN — CL20 C0.1u16X/4 — PE_LAN_TXN_C 14 HSIN
17 PE_LAN_CLKP — PE_LAN_CLKP 15 REFCLK_P
17 PE_LAN_CLKN — PE_LAN_CLKN 16 REFCLK_N
17,21 PM_WAKE# — RL15 0R/4 — ISOLATEB LAN_WAKE# 20 ISOLATEB / 21 LANWACKEB
RL9 2.49KR1%/4 — RSET 31 RSET
VDD33 — 23 VDDREG
11 AVDD33-1 / 32 AVDD33-2
VDD10 — 24 REGOUT
22 DVDD10
3 AVDD10-1 / 8 AVDD10-2 / 30 AVDD10-3
33 GND

PCIE interface
PM
Transceiver Interface
EEPROM
CLOCK
Realtek Power

17 PE_LAN_RXP_C — C0.1u16X/4 — CL21 — PE_LAN_RXP 15
18 PE_LAN_RXN_C — C0.1u16X/4 — CL22 — PE_LAN_RXN 15
19 PLTRST_BU3#_LAN_C
12 CLKREQ1 — CLKREQ1 17

1 MDIP0 — TR_D0+ / 2 MDIN0 — TR_D0-
4 MDIP1 — TR_D1+ / 5 MDIN1 — TR_D1-
6 MDIP2 — TR_D2+ / 7 MDIN2 — TR_D2-
9 MDIP3 — TR_D3+ / 10 MDIN3 — TR_D3-
27 LED0 — LED0
26 LED1/GPO — LED1
25 LED2 — LED2
28 CKXTAL1 — CLK_LANI — CL18 C27p50N/4
29 CKXTAL2 — CLK_LAN0 — CL17 C27p50N/4
2 — YL5 25MHZ18P

RTL8111H-CG-RH

B06-08111CC-R09

D04-1000201-F07

Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

VDD33@65mA

3VSB — CPL5 (20mil=1A) — 23 — CL15 C0.1u16X/4 — 32 — CL13 C0.1u16X/4

VDD33 — 11 — CL14 4.7u0X/6 — 32 — CL12 4.7u0X/6

For surge improvement

VDD33 width>40mil
VDD10 width>60mil

VDD10@150mA

VDD10 — 3 — CL11 C0.1u16X/4 — 22 — CL23 C0.1u16X/4 — 22 — CL24 X_C1u6.3X/4 — 24 — CL25 C0.1u16X/4 — 8 — CL10 C0.1u16X/4 — 30 — CL16 C0.1u16X/4

Pull-up resister RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

VDD33 — For EMI — RL6 100R/4 — CL5 C0.1u16X/4

LAN_USB1B

LED2 — RL5 220R/4 — LED2_ACT 30 YELLOW+ / 29 YELLOW-
LVDD33 29 / VCT 19 / TR_D0+ 20 / TR_D0- 21 / TR_D1+ 22 / TR_D1- 23 / TR_D2+ 24 / TR_D2- 25 / TR_D3+ 26 / TR_D3- 27 / GND 28
LED1 — RL7 220R/4 — LINK1000# 31 GREEN+/ORANGE- / 32 GREEN-/ORANGE+
LED0 — RL8 100R/4 — LED0_LINK100#
For EMI

Main:D0G-1020530-I05
AVL:D0G-8010510-SI0
D0G-1020530-I05
ESD-VPORT0603L102KV05
DL5 — CL8 C0.1u16X/4

RJ45_USB_LEDX2-RH-6

N58-23F0091-F02

For EMI
LED2_ACT — CL6 C100p50N/4
LINK1000# — CL7 C100p50N/4
LED0_LINK100# — CL9 C100p50N/4

3VSB — C452 C0.1u16X/4
U36 NC7SZ08M5X_SOT23-5
PLTRST_BU3#_LAN_C — R417 22R/4 — PLTRST_BU3#_LAN_R 4
1 — REMOVE R418 180502 — PM_GPP_RST 17,25 — FROM PROM
2 — LAN_BIOS_OFF# 17 — FROM PROM GPIO

ESD Protect
close to connector

D0G-0200529-A68
D0G-0100619-I05

UL6
TR_D0- 6 / 5 / 4 TR_D1-
TR_D0+ 1 / 2 / 3 TR_D1+
ESD-AOZ8906CI-HF
D0G-05A0529-A68

UL5
TR_D2- 6 / 5 / 4 TR_D3-
TR_D2+ 1 / 2 / 3 TR_D3+
ESD-AOZ8906CI-HF
D0G-05A0529-A68

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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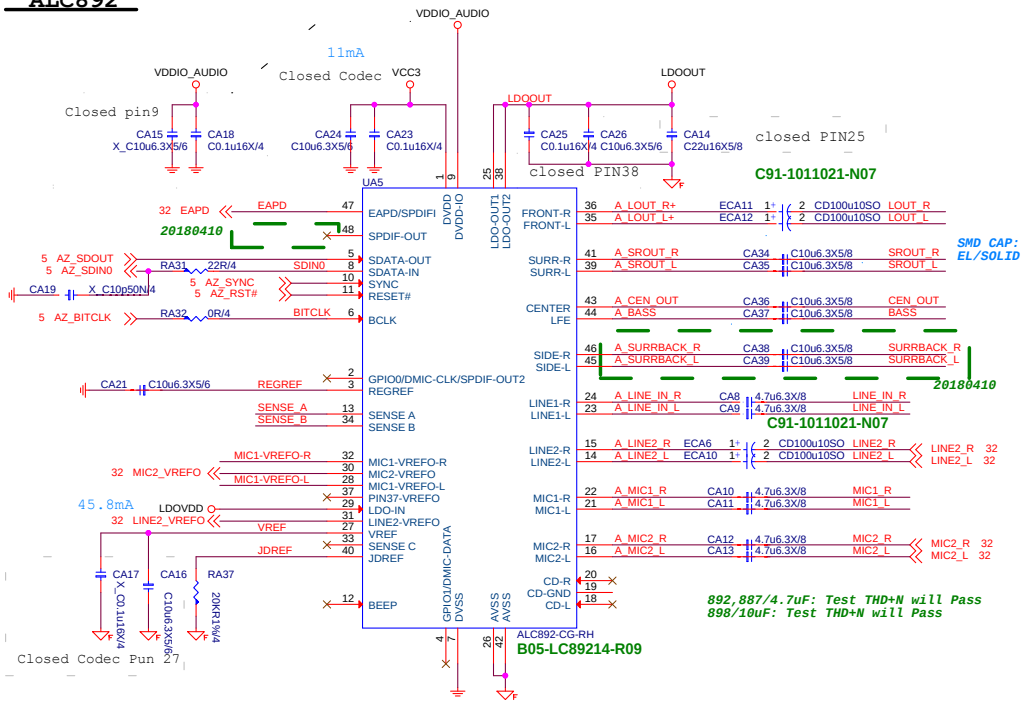
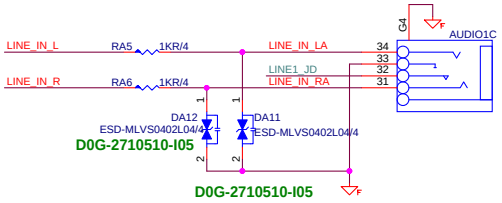
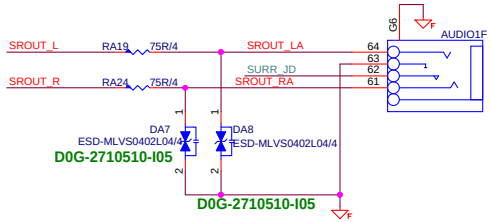
ALC892

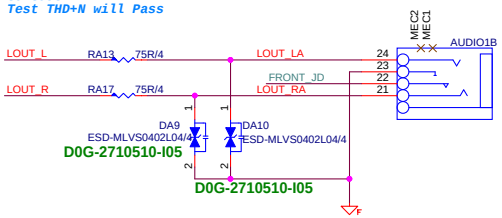
Follow APU power well

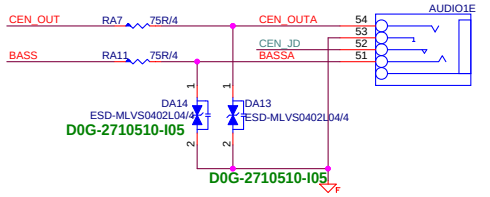


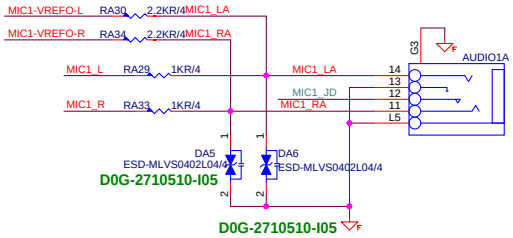
SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

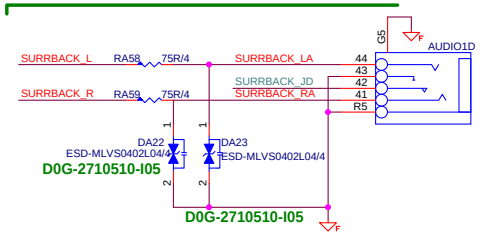




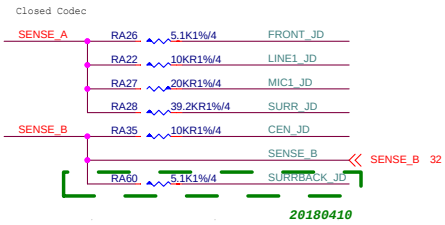






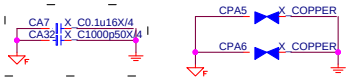


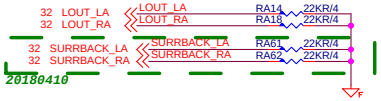
20180410



20180410

EMI





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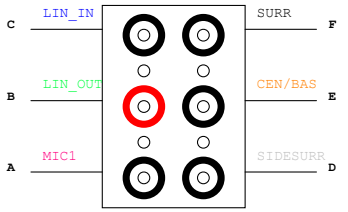

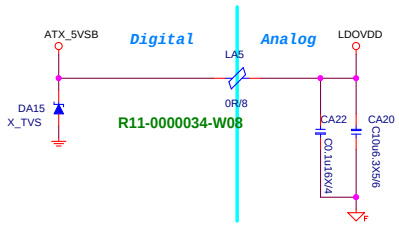

CA22,CA20 close to LA5

MSI MICRO-STAR INTERNATIONAL Link to the Future MICRO-START INT'L CO.,LTD.

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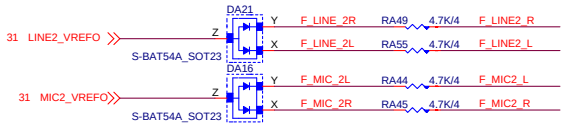
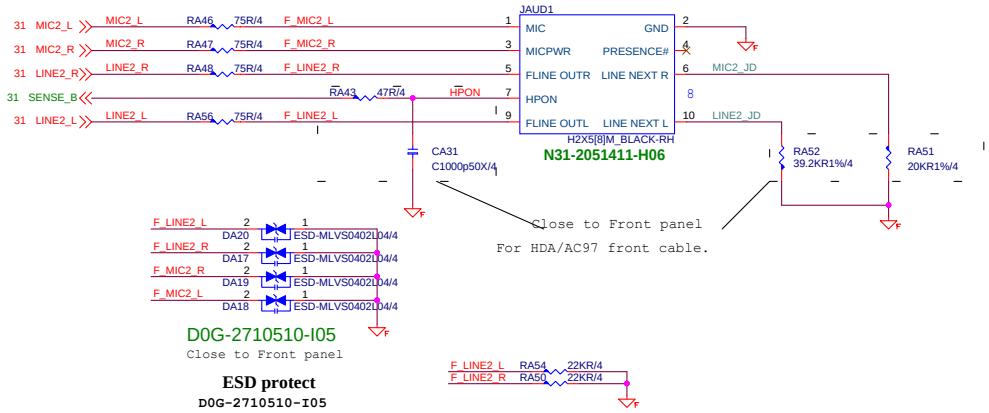
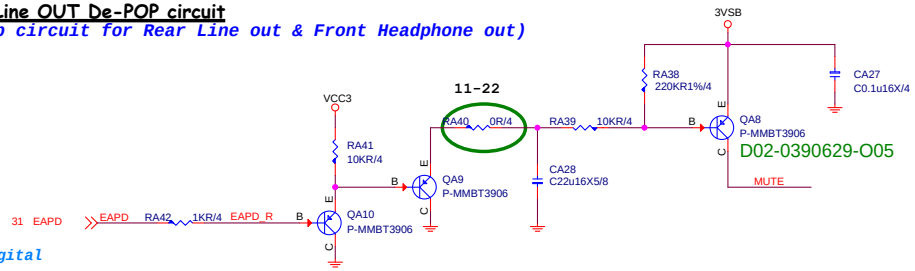




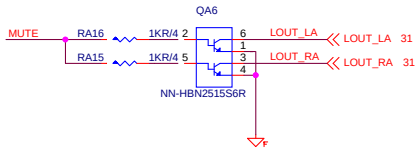
Rear Line OUT De-POP circuit

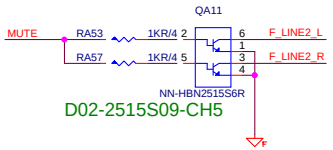
(De-pop circuit for Rear Line out & Front Headphone out)

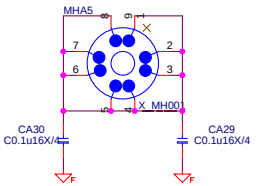


Digital

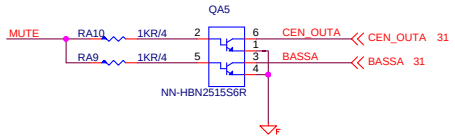
Analog

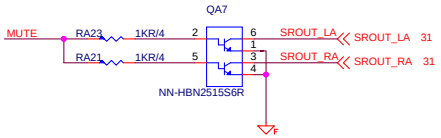


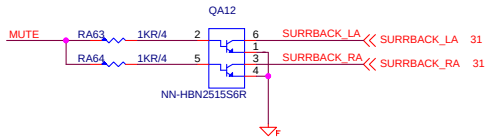




(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA6, CA7, CA9,to TVS)







MSI MICRO-START INT'L CO.,LTD.
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Title: Audio De-POP		
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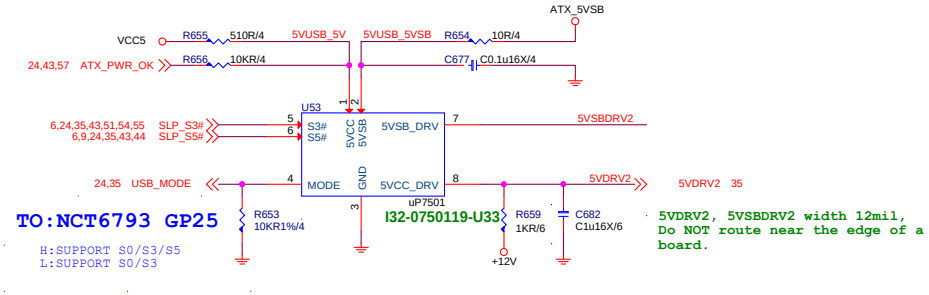
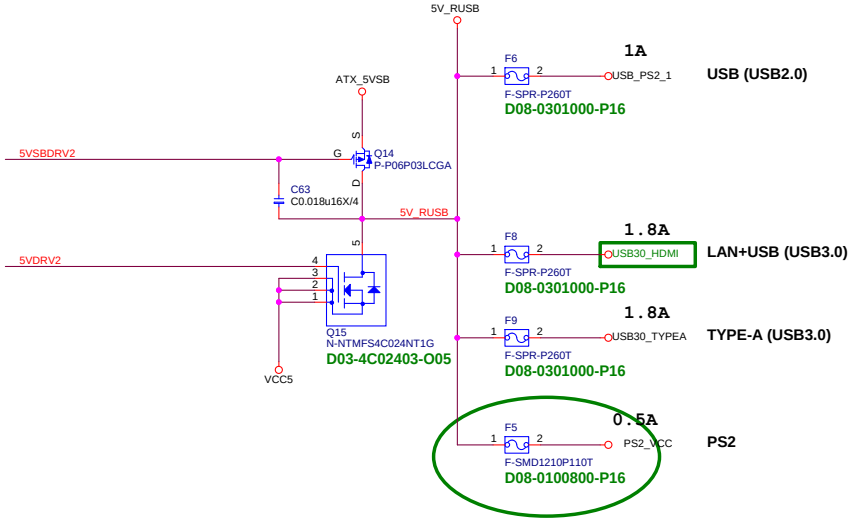
USB Power

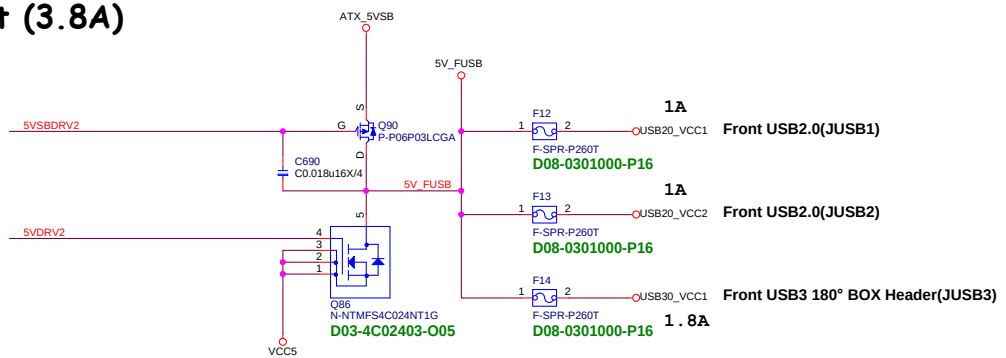


5VDRV2, 5VSBDRV2 width 12mil, Do NOT route near the edge of a board.



Rear (8.1A)

Front (3.8A)



MICRO-START INT'L CO.,LTD.

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HDMI+USB (USB3.0)

5V@1A

7 APU_USB_SSTX0+ — C158 C0.22u6.3X/4 — HDMI_SSTX0+
7 APU_USB_SSTX0- — C162 C0.22u6.3X/4 — HDMI_SSTX0-
7 APU_USB_SSRX0+ — C182 C0.33u6.3X/4 — APUUSB_SSRX0+
7 APU_USB_SSRX0- — C187 C0.33u6.3X/4 — APUUSB_SSRX0-
7 APU_USB_SSTX1+ — C163 C0.22u6.3X/4 — HDMI_SSTX1+
7 APU_USB_SSTX1- — C172 C0.22u6.3X/4 — HDMI_SSTX1-
7 APU_USB_SSRX1+ — C176 C0.33u6.3X/4 — APUUSB_SSRX1+
7 APU_USB_SSRX1- — C178 C0.33u6.3X/4 — APUUSB_SSRX1-

7 APU_USB0+ — APU_USB0+
7 APU_USB0- — APU_USB0-
7 APU_USB1+ — APU_USB1+
7 APU_USB1- — APU_USB1-

U15: HDMI_SSTX0+ 1 / HDMI_SSTX0- 2 / HDMI_SSTX1+ 4 / HDMI_SSTX1- 5 → 10 HDMI_SSTX0+ / 9 HDMI_SSTX0- / 7 HDMI_SSTX1+ / 6 HDMI_SSTX1-
ESD-AOZ8829DI-03
D0G-06A030C-A68

U16: APUUSB_SSRX1+ 1 / APUUSB_SSRX1- 2 / APUUSB_SSRX0+ 4 / APUUSB_SSRX0- 5 → 10 APUUSB_SSRX1+ / 9 APUUSB_SSRX1- / 7 APUUSB_SSRX0+ / 6 APUUSB_SSRX0-
ESD-AOZ8829DI-03
D0G-06A030C-A68

U18: APU_USB0- 1 / APU_USB0+ 2 / APU_USB1- 4 / APU_USB1+ 5 → 10 APU_USB0- / 9 APU_USB0+ / 7 APU_USB1- / 6 APU_USB1+
ESD-AOZ8829DI-03
D0G-06A030C-A68

USB1A (X2)
USB30_HDMI
HDMI_SSTX0+ 19 / HDMI_SSTX0- 18 / APU_USB0- 12 / APU_USB0+ 13 / APUUSB_SSRX0+ 16 / APUUSB_SSRX0- 15
SSTX0+ 11 / VBUS1 / SSTX0- 18 / D0- 12 / GND-1 14 / D0+ 13 / SSRX0+ 16 / GND-2 17 / SSRX0- 15 / GND-4 / GND-3
N53-18M0251-L06 (X1)
USBAX2M_RED-RH-4

USB1B (X4)
USB30_HDMI
HDMI_SSTX1+ 29 / HDMI_SSTX1- 28 / APU_USB1- 22 / APU_USB1+ 23 / APUUSB_SSRX1+ 26 / APUUSB_SSRX1- 25
SSTX1+ 29 / VBUS2 21 / SSTX1- 28 / D1- 22 / GND-5 24 / D1+ 23 / SSRX1+ 26 / GND-6 27 / SSRX1- 25 / GND-8 / GND-7
N53-18M0251-L06 (X3)
USBAX2M_RED-RH-4

USB30_HDMI
EC24 1 2 C174 C0.1u8X/4
C71-56106N1-F70 CD560u6.3SO

APU_USB_OC

USB_XOR0 — R98 X_0R/4 — APU_USB_OC#

3VSB
R265 10KR/4
USB_XOR0
5,6,50,52,55 TYPE1_CPU_SEL

U20 SN74LVC1G86DCKR_SC70-5-RH
APU_USB_OC# → APU_USB_OC# 6

TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP

VCC5
R160 10KR/4
USB30_HDMI
11-14
R153 15K/4
R164 10KR/4
Q27 2N7002D (G2, D2, D1, S2, G1, S1)
HDMI+USB (USB3.0)

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

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Title	Rear LAN_USB3.0	
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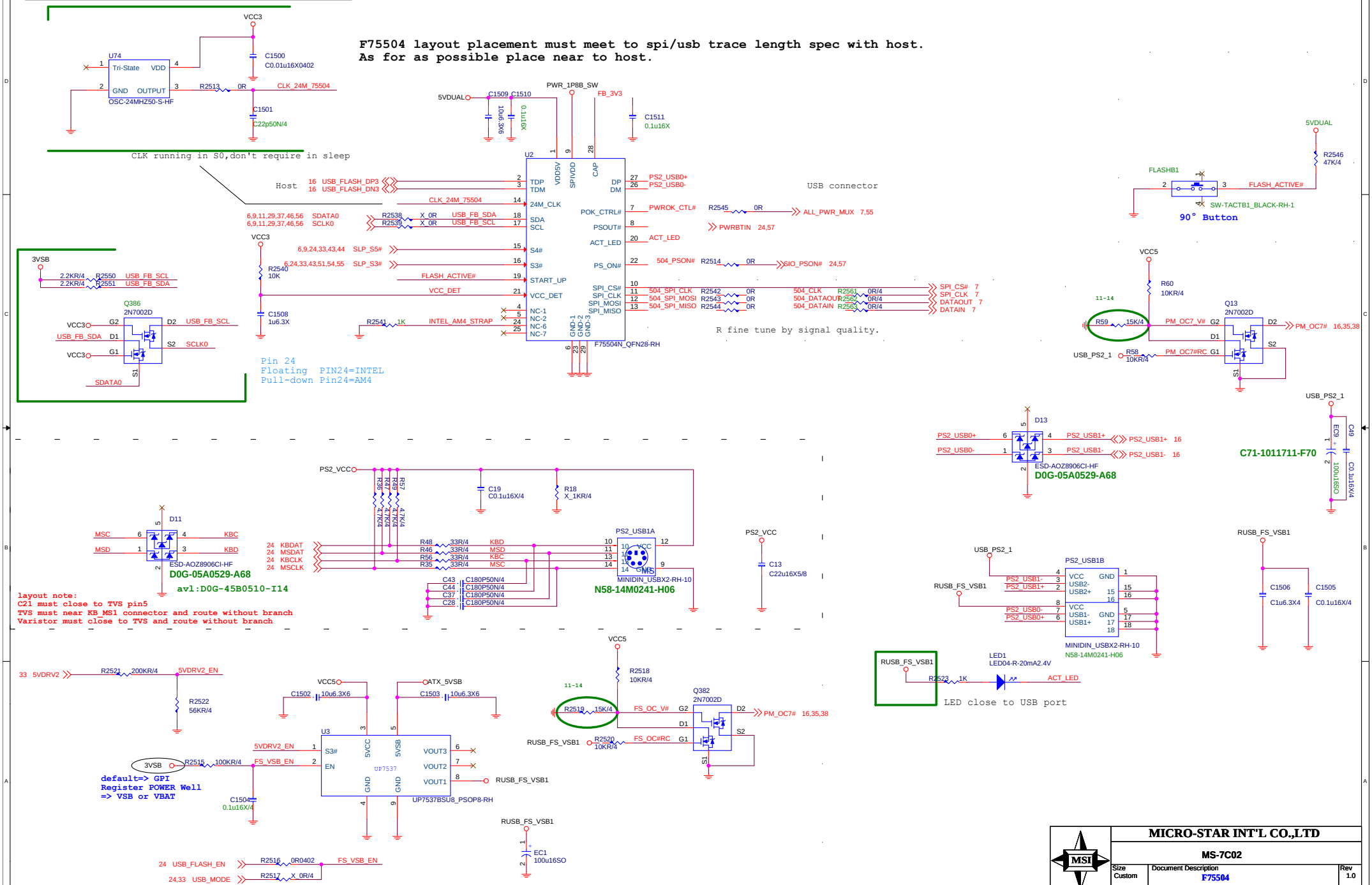
PS2+USB Flash BIOS (USB2.0)



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	MS-7C02	
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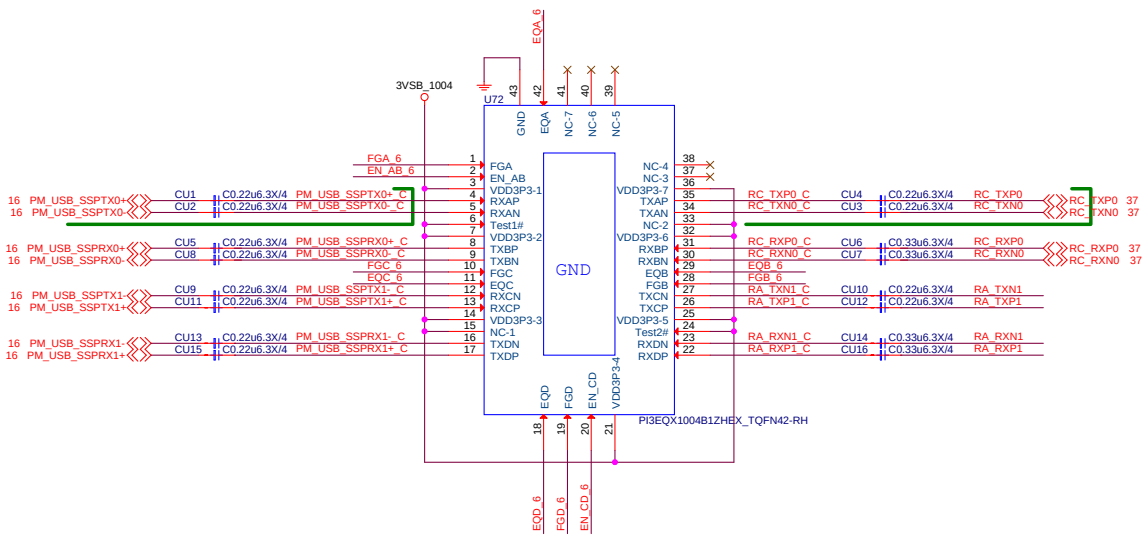
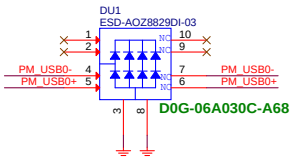
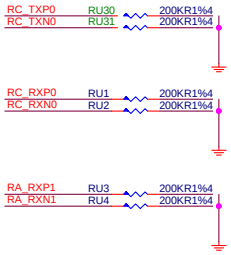
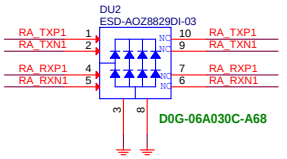
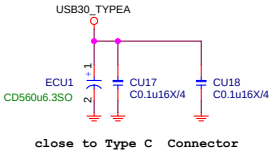
TYPE-A PI3EQX1004 Redriver

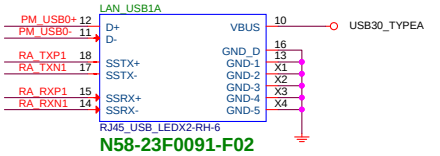


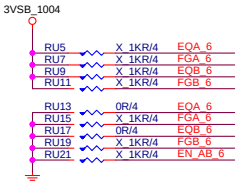


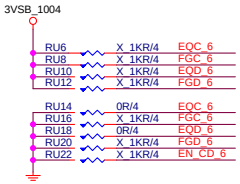


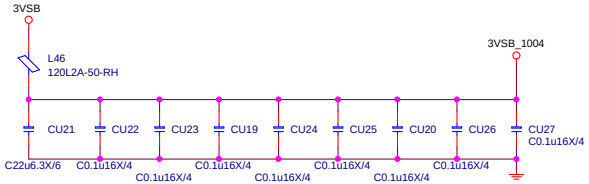


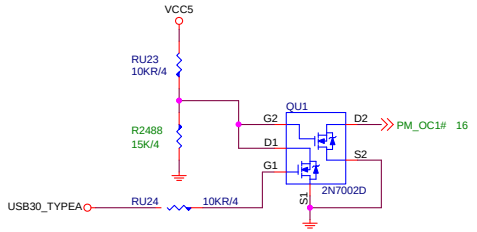












EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

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Title	Rear USB3.1 Type A / redrive	
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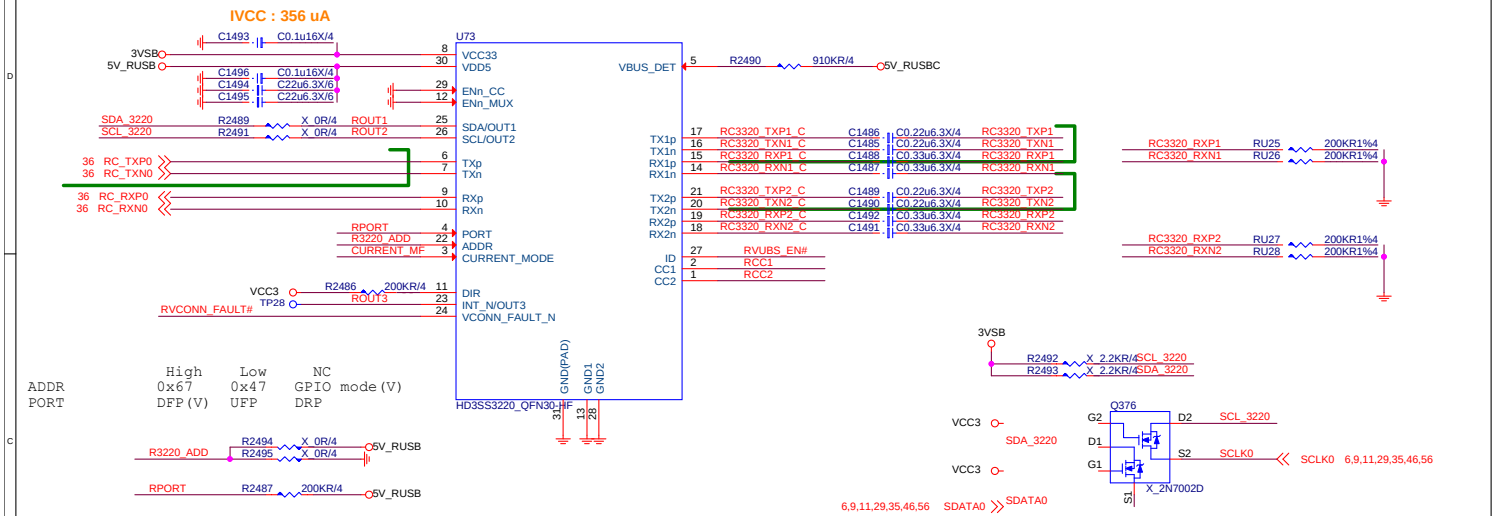
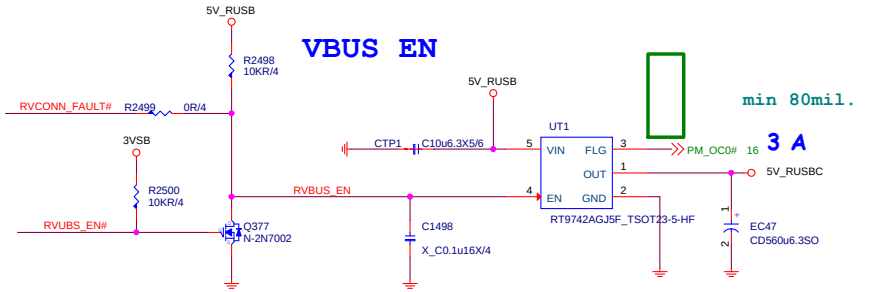
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

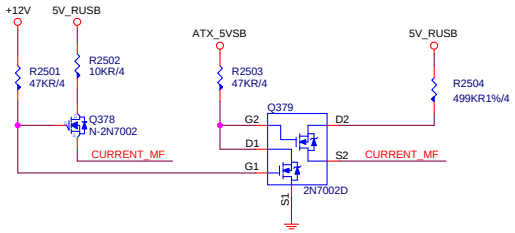


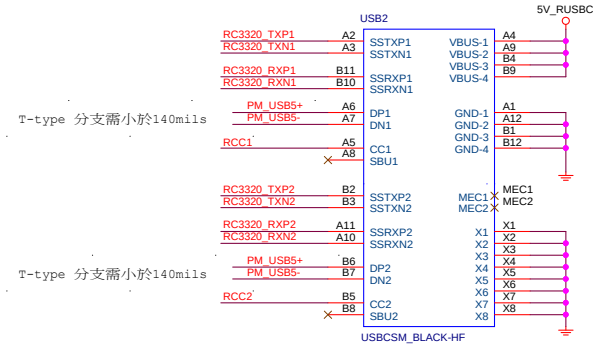
VBUS OC# LEVEL SHIFT

VCOM OC#

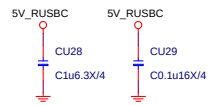


Current Mode





close to Type C Connector



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title: Front USB3.0 90° Header			
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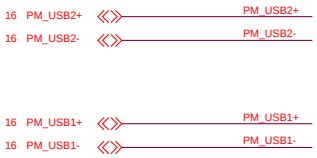
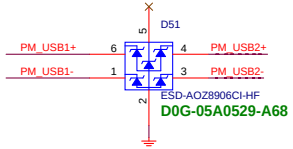
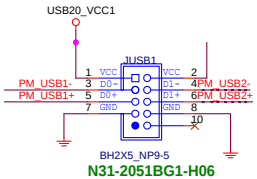
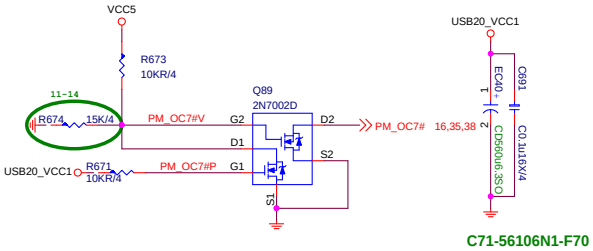
Front USB2.0(JUSB1)

5V@1A



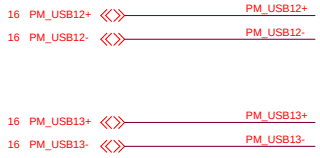


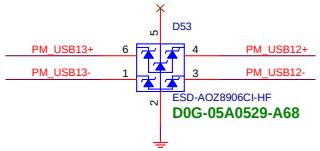


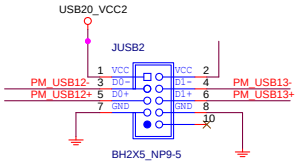


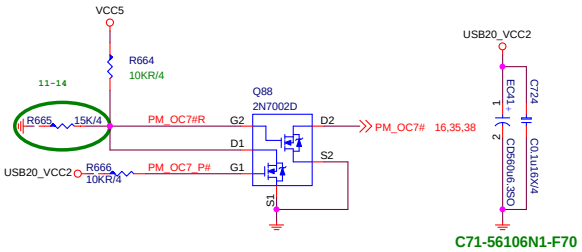
Front USB2.0(JUSB2)

5V@1A









MSI MICRO-STAR INT'L CO.,LTD.
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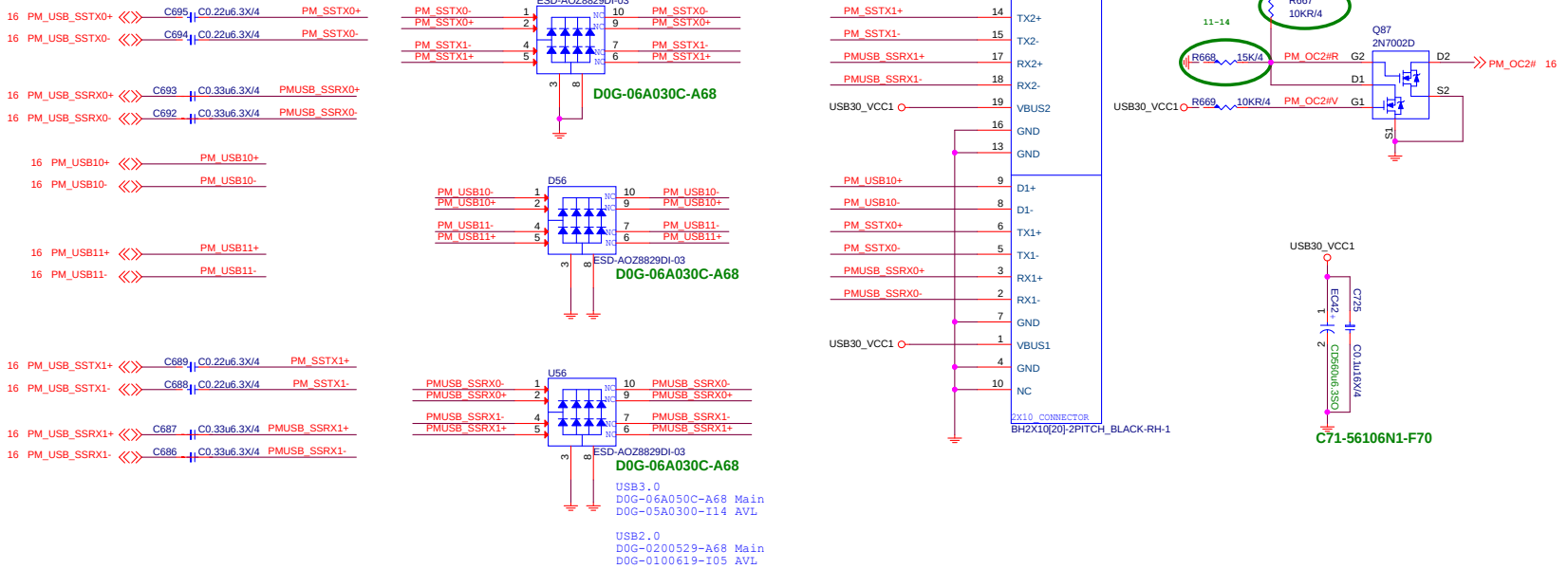
Front USB3 180° BOX Header(JUSB4)

5V@1.8A



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Title: Front USB3.0 180° Header			
Size: Custom	Document Number: MS-7C02		Rev: 1.0
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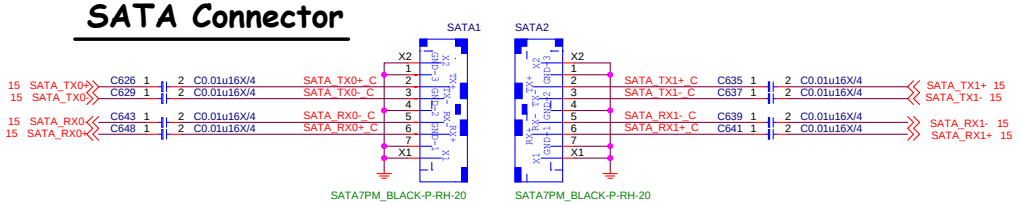
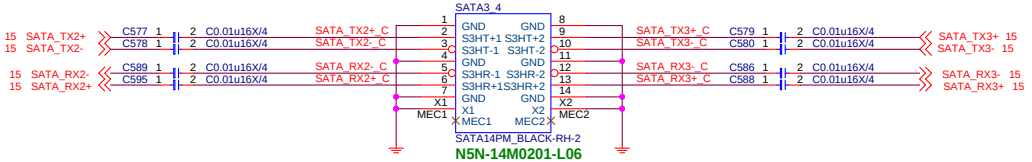
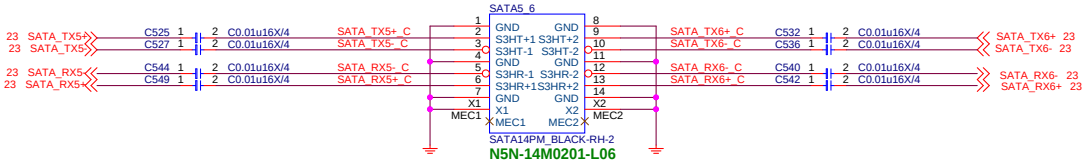
SATA Connector







Schematic Cfg	Project	
CFG-7C02-***-Arsenal Gaming	V	A

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: SATA		
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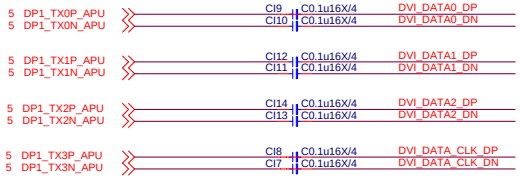
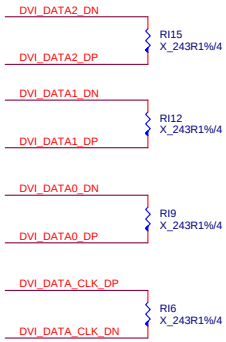
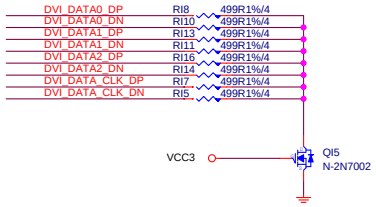
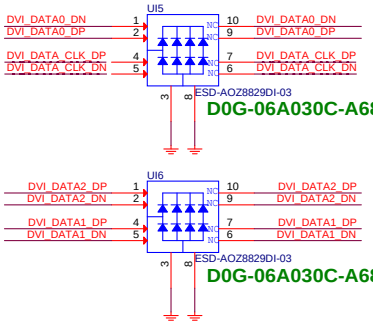
DVI CONNECTOR

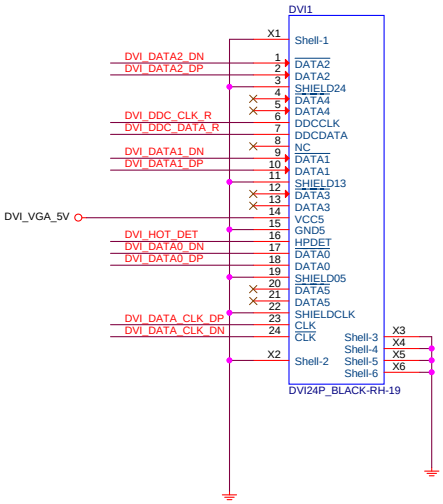


For EMI

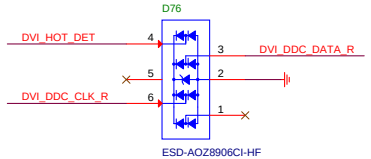






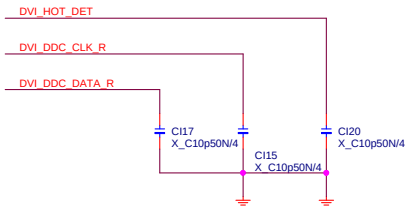


注意:耐壓5V零件

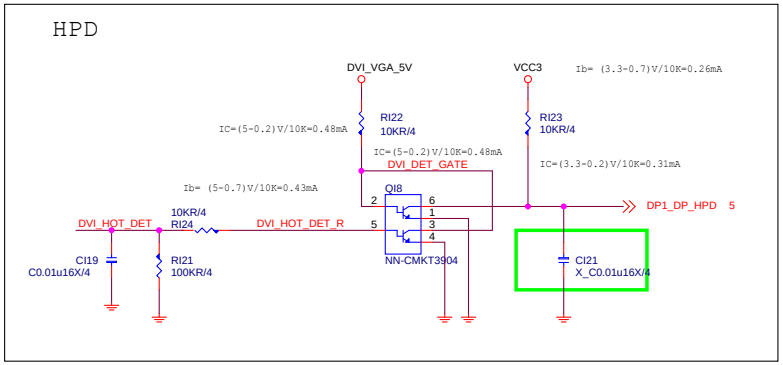


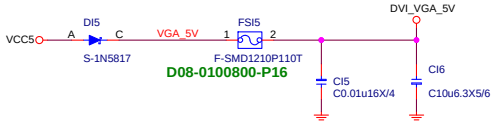
180427 10pin換6pin

For EMI

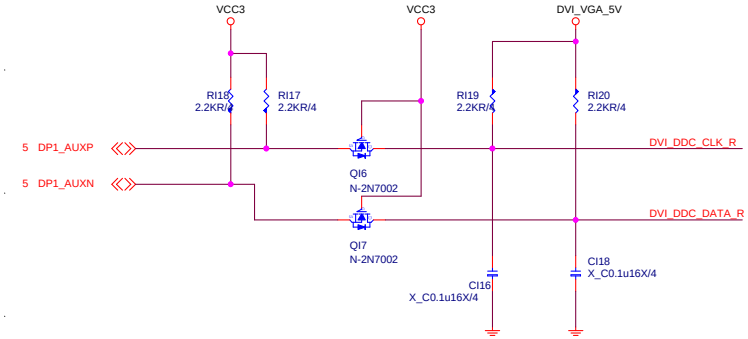


HPD





LEVEL SHIFT using I2C Repeater



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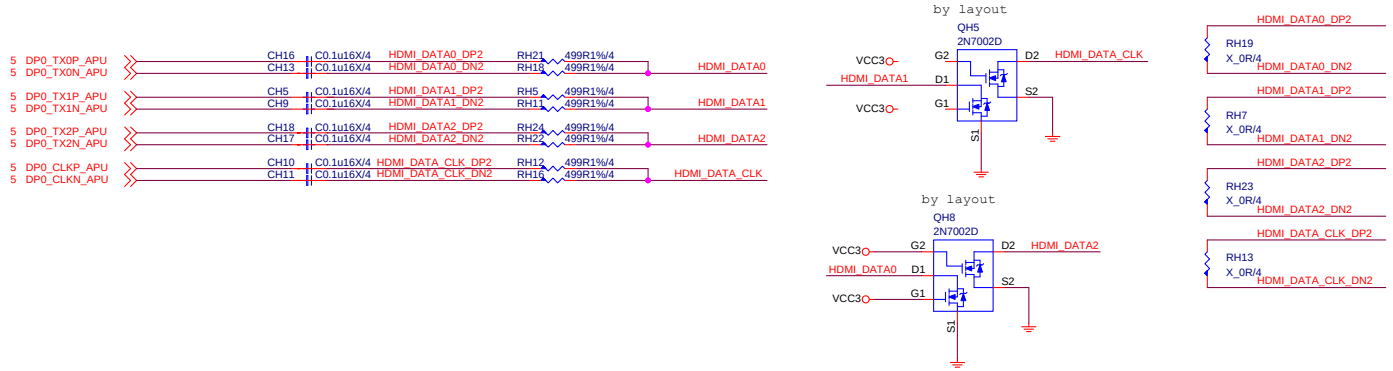
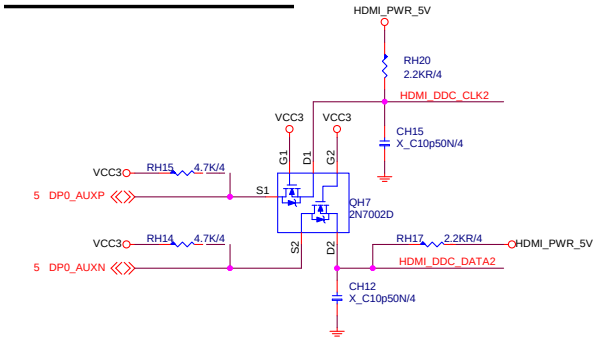
HDMI CONNECTOR

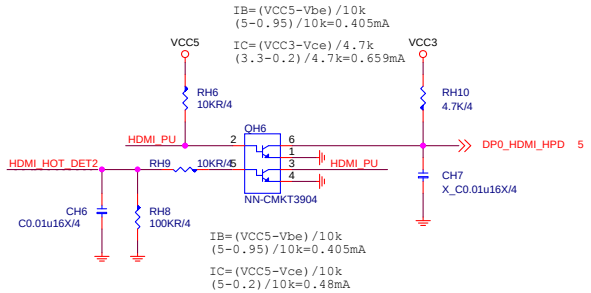
For HDMI 1.4



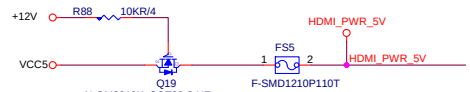
AUX Level Shifter



HPD Circuit

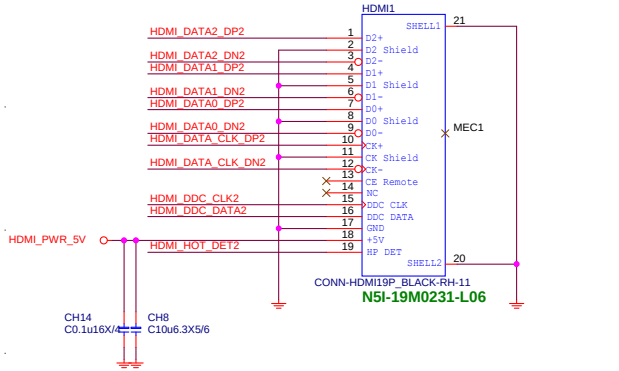


Connector Power

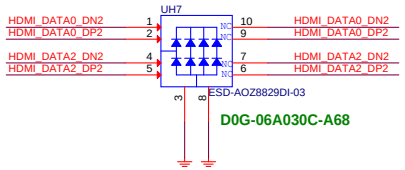


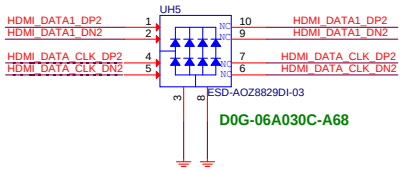
如果用DIODE SA測試電壓會不過

Connector

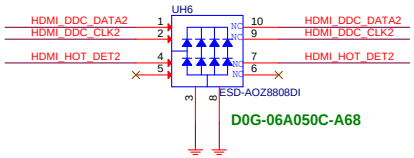


For EMI





注意:耐壓5v零件



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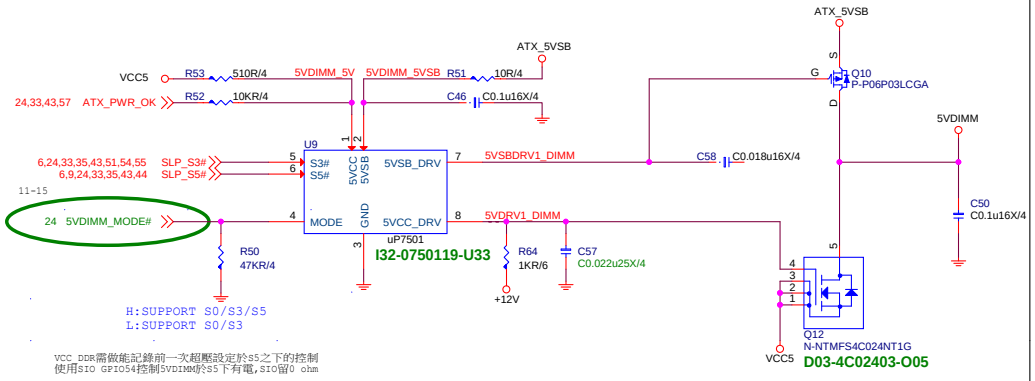
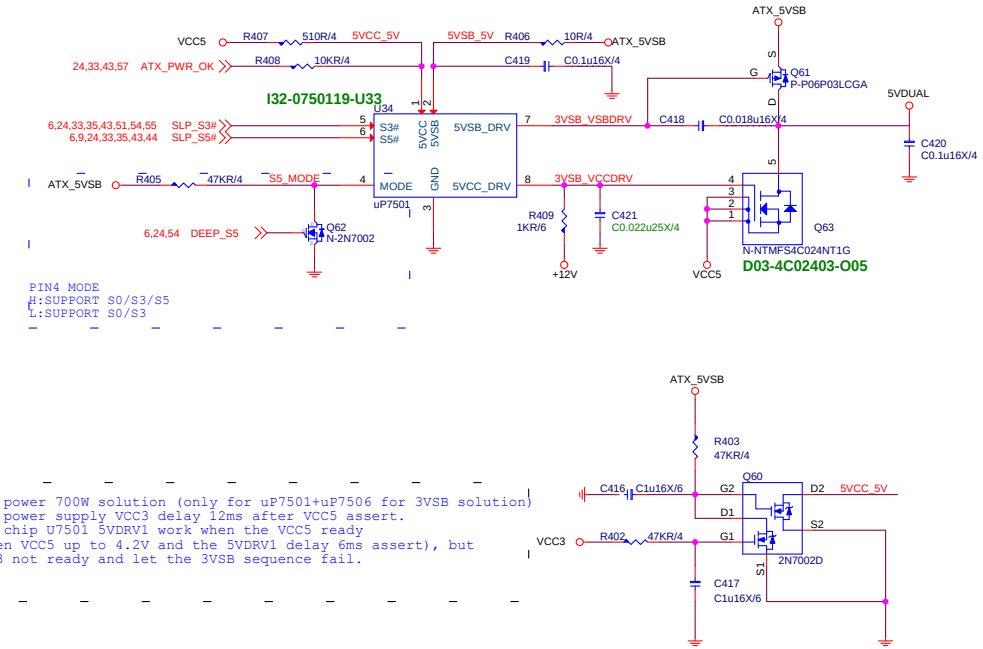
5VDIMM FOR DDR



5VDUAL For 3VSB、CPU 1.8V 、 VDDP

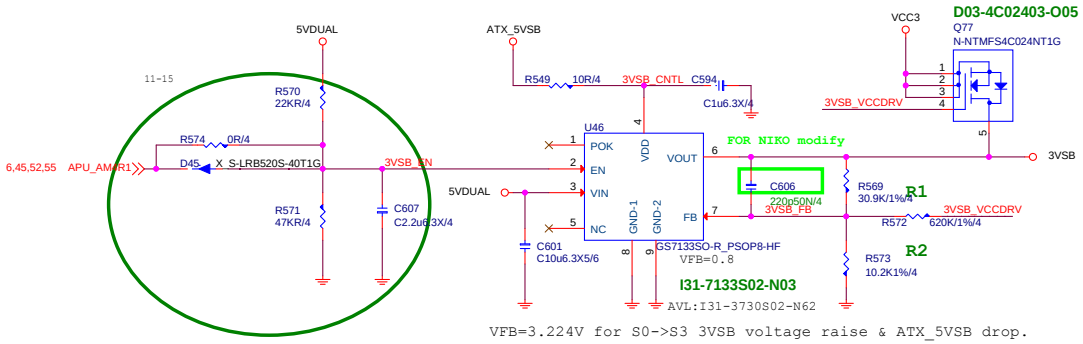


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@2.63A

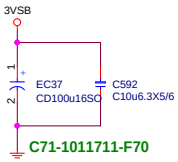
1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
*PCIE*6 @2.25A*



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(30.9K/10.2K))
= 3.22V

OCP=12A
2.63A



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Title	ACPI 5VDIMM/3VSB	
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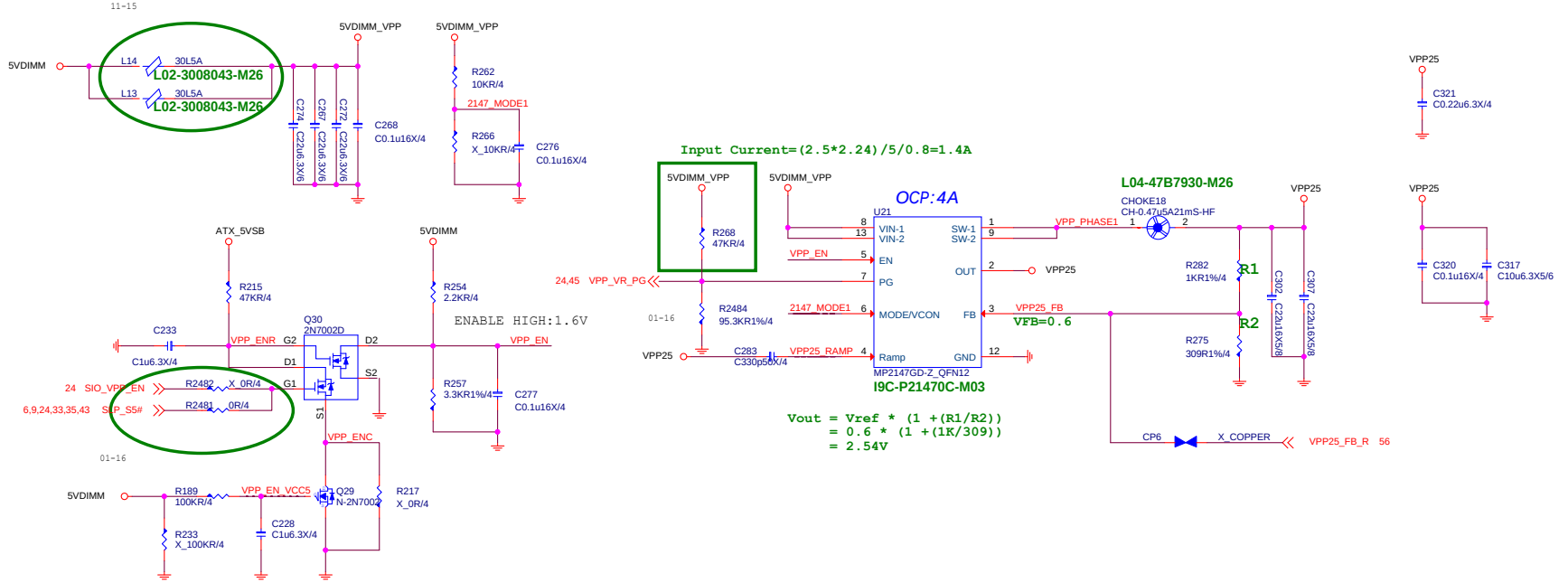
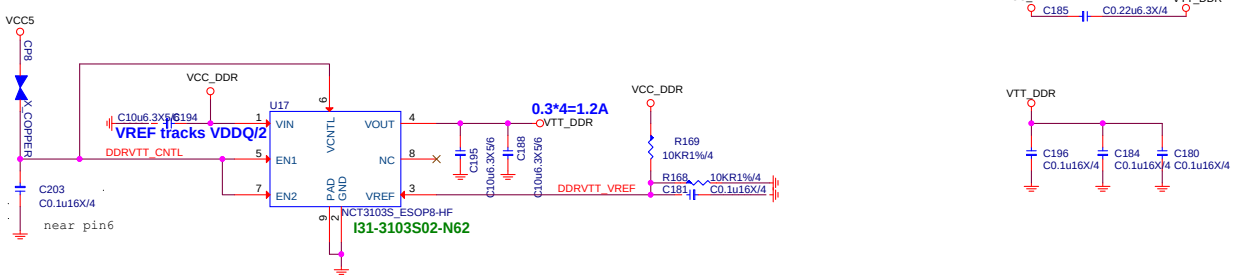
4DIMM : VPP25

2.5V@2.24A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MICRO-START INT'L CO.,LTD.

Title: DDR VPP25/VTT		
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DDR4_1.2V@26.2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

5VDIMM
R142 X_2.2KR/4 EN:VIH2.4V
DDR_EN
R143 X_3.3KR1%/4
C122 X_C0.1u16X/4

6,43,52,55 APU_AM4R1 D34 S-LRB520S-40T1G DDR_EN
24 SIO_VDDQ_EN R372 X_0R/4 DDR_EN 3.12V
24,44 VPP_VR_PG R2483 0R/4

EN:VIH2.4V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

Follow CRB

5VDIMM
20180410
R134 47K/4
EN:VIH1.6V
EN pin Maximum:6.5V

5VDIMM
R130 10R/8
DDR_VCC C97 4.7u10X/6

OCP=35A

U12
DDR_EN 7 EN
51,55 DDR_PWRGD 8 PGOOD
DDR_REFOUT 10 REFOUT
9 REFIN
VCC 5
GND 11
BOOT 1 DDR_BOOT1 R121 0R/4 DDR_BOOT1_R C92 C0.1u16X/4
PHASE 3 DDR_PH1
UGATE 2 DDR_UG1
LGATE/OCSET 4 DDR_LG1
FB 6 DDR_FB
RT8125EGQW_WDFN10-HF
I32-8125E0C-R11
FB:0.8V

20180410
C1507 C0.22u6.3X/4
C115 C1000p50X/4
R140 665R1%/4
DDR_REFIN
C114 C1000p50X/4

56 DDR_OV CP7 X_COPPER

VCC_DDR
close to DIMM side
R138 10R/4
R1
R139 10KR1%/4
DDR_VSENP R144 0R/4 VDDIO_MEM_S3_SENSE 6
C116 X_C0.1u16X/4
R2
R145 19.1K1%/4

Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/19.1K))
= 1.218V

Input Current=(26.2*1.2)/5/0.8=7.86A
L04-12A7811-T15
CHOKE8 CH-1.2u15A2m-HF
5VDUAL_IN_DDR
C68 C1u16X/6
C61 C10u6.3X5/6
EC10 CD560u6.3SO
EC11 CD560u6.3SO
C117 C0.1u16X/4
5VDIMM
C71-56106N1-F70
C71-56106N1-F70

DDR_UG1 R81 0R/6 DDR_UG1_R
Q16 N-NTMFS4C029NT1G D03-4C02903-O05
Q17 N-NTMFS4C029NT1G D03-4C02903-O05
R83 X_10KR/4
DDR_PH1
L04-47B7981-T15
CHOKE12 CH-0.47u42A0.81m-HF
VCC_DDR
DDR_LG1
20180517
R97 7.15KR1%/4
Rocpset
Q21 N-NTMFS4C024NT1G D03-4C02403-O05
Q22 N-NTMFS4C024NT1G D03-4C02403-O05
R112 2.2R/8
snubber
C82 C3300p50X/4
C112 C1u6.3X/4
C91 C22u6.3X/6
EC22 CD560u6.3SO
EC19 CD560u6.3SO
EC25 CD560u6.3SO
C71-56106N1-F70
C71-56106N1-F70
C71-56106N1-F70

20180517 Rocpset:7.15K
OCP=Rocset*10uA/Rdson(Low side)
=7.15K*10uA/1.65~2mohm
=43.33A~35.75A

VCC_DDR
EC29 CD560u6.3SO
EC17 CD560u6.3SO
C71-56106N1-F70
C71-56106N1-F70

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Title	DDR Power-RT8125E	
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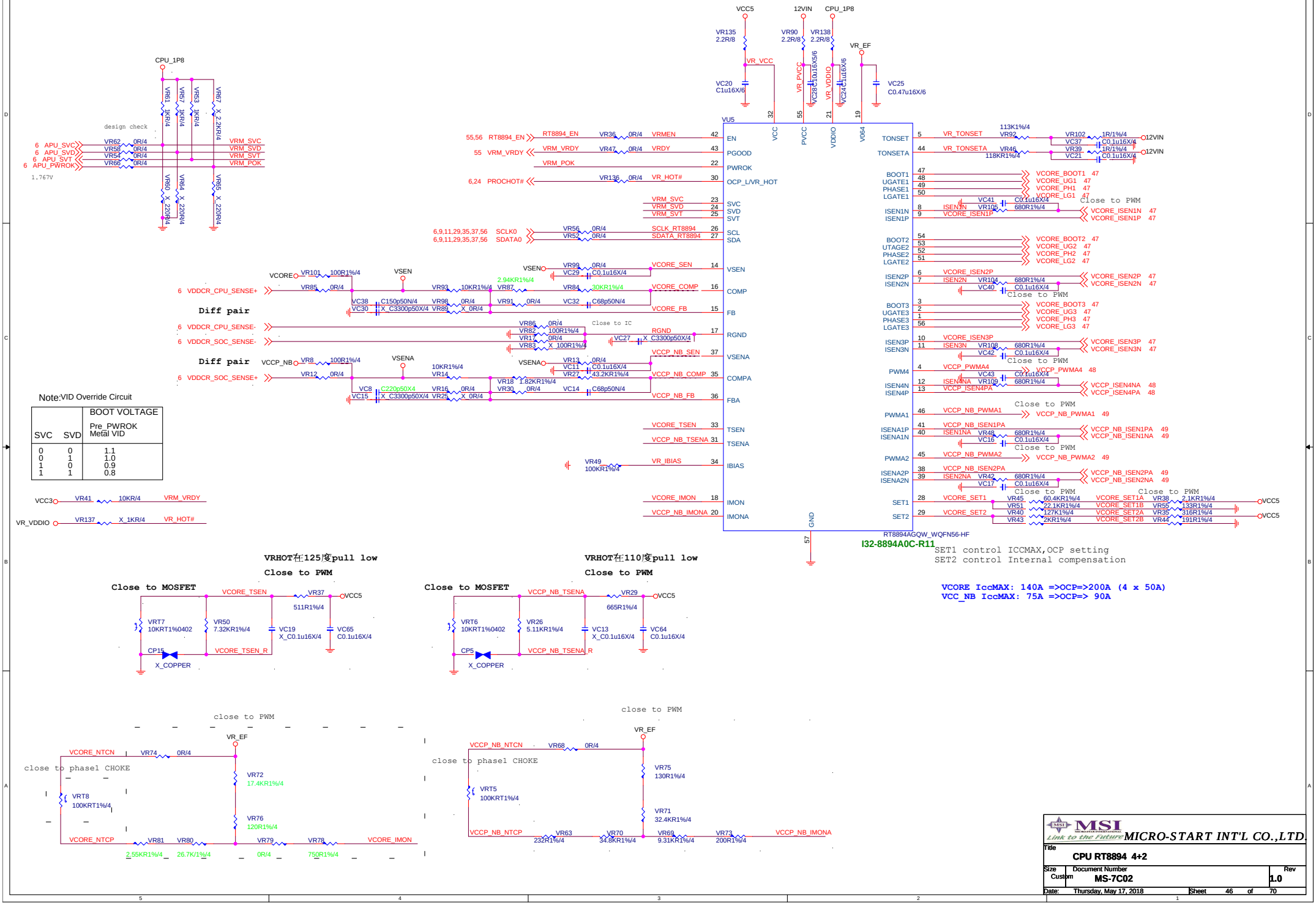

Title	CPU RT8894 4+2
Size	Custom
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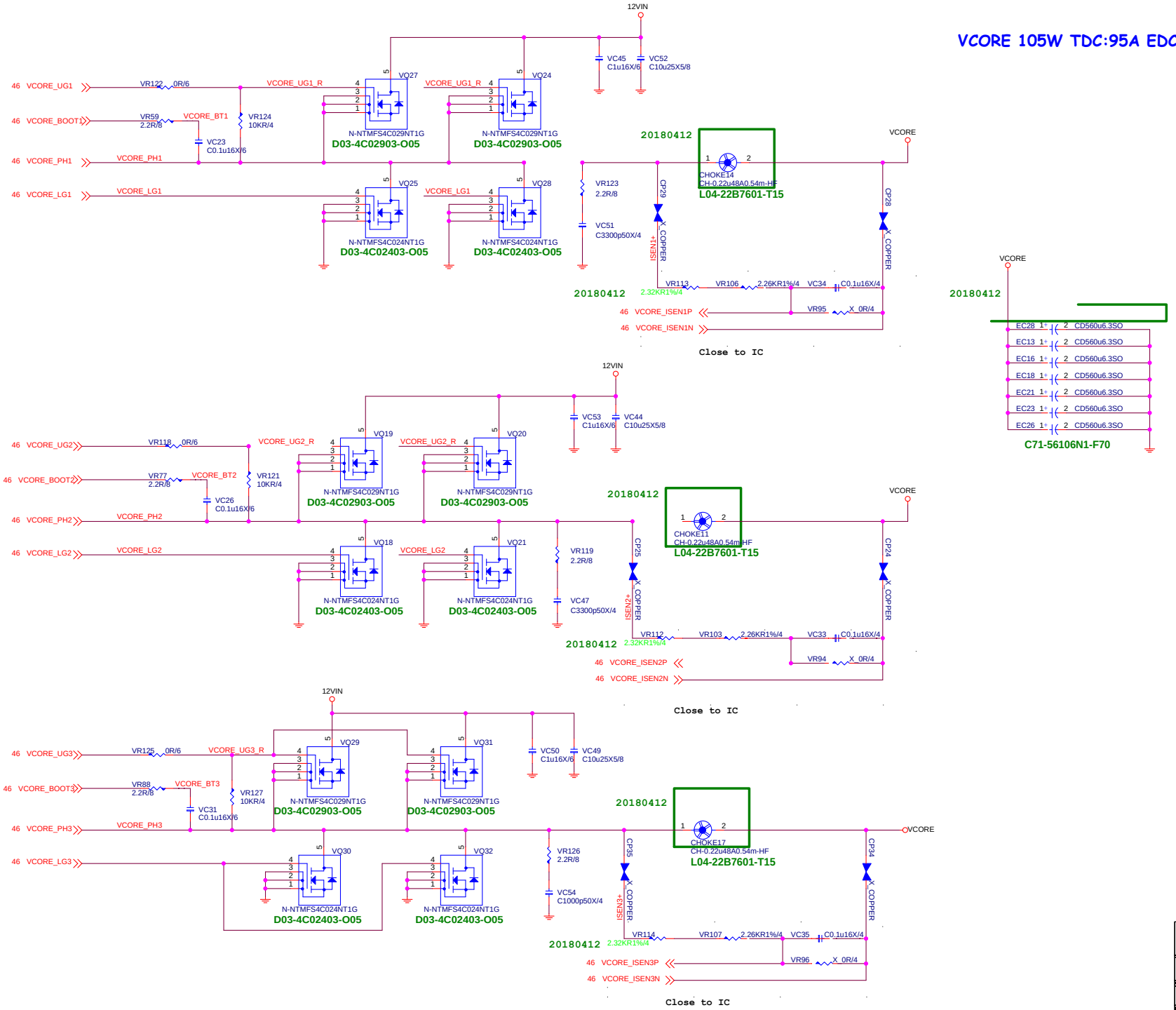
VCORE 105W TDC:95A EDC:140A



MICRO-START INT'L CO.,LTD.

Title	CPU Phase1-3	
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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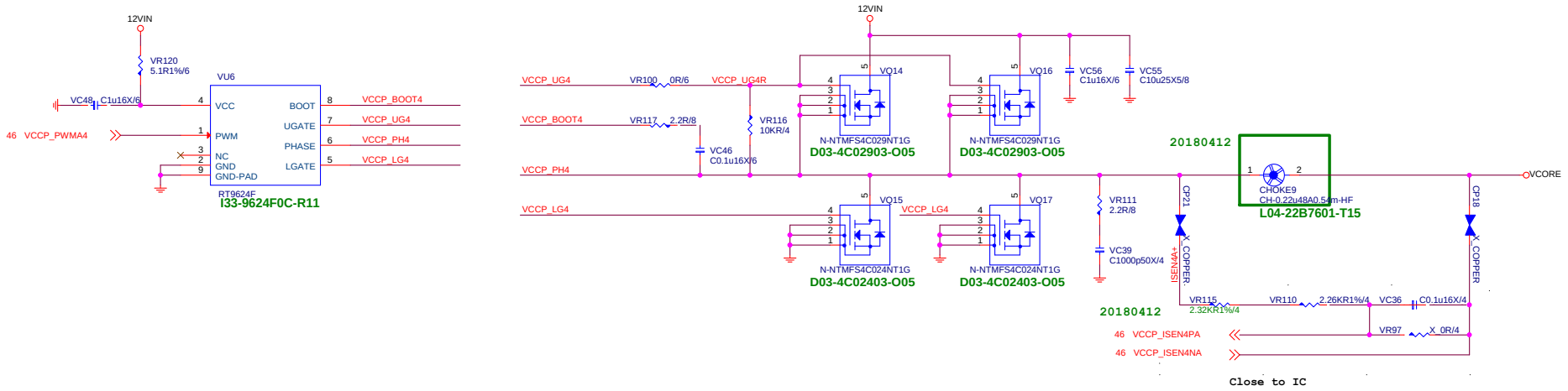

MICRO-START INT'L CO.,LTD.

Title: CPU Phase4		
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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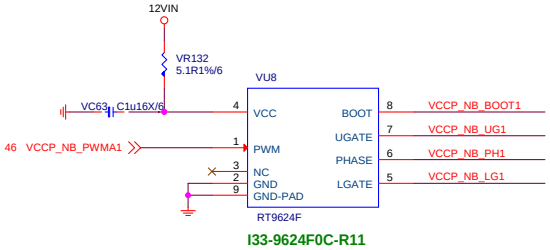
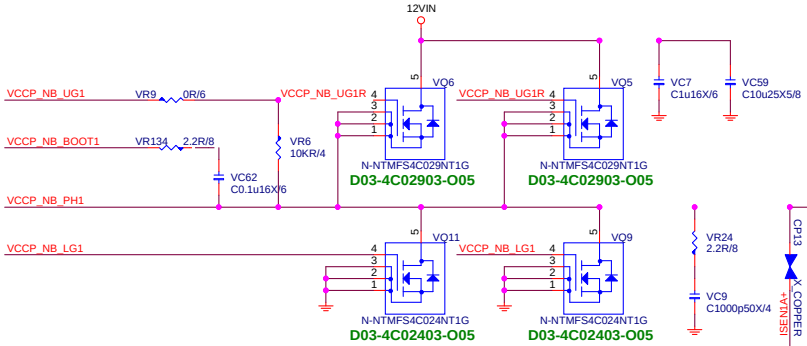
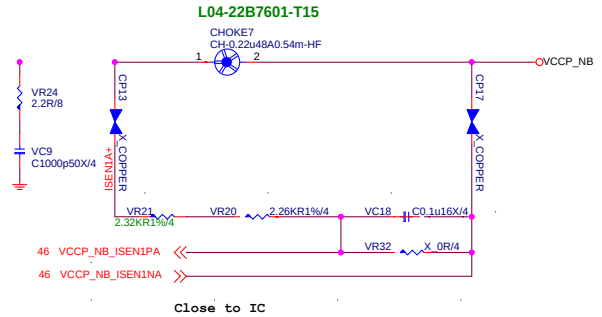
VCCP_NB 105W TDC:50A EDC:75A

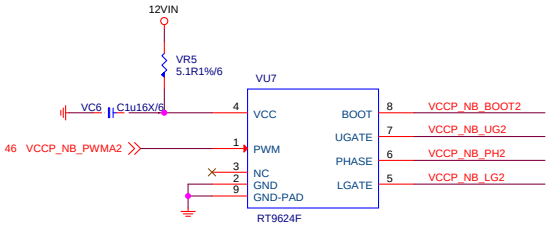


I33-9624F0C-R11

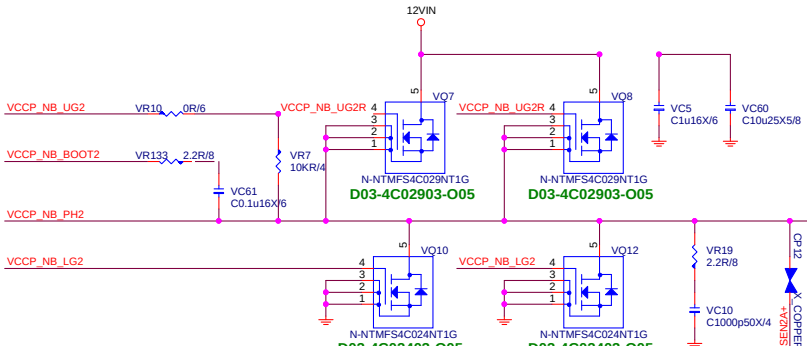


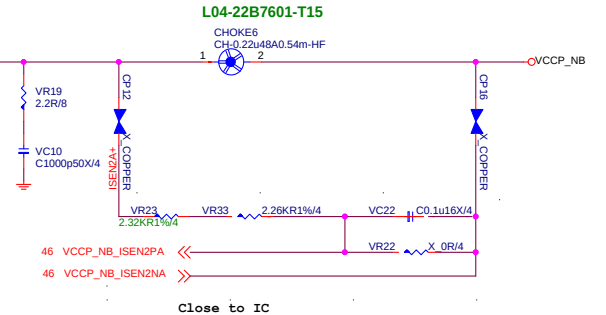
VCCP_NB 105W TDC:50A EDC:75A

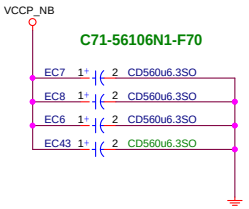




I33-9624F0C-R11







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Title: CPU NB		
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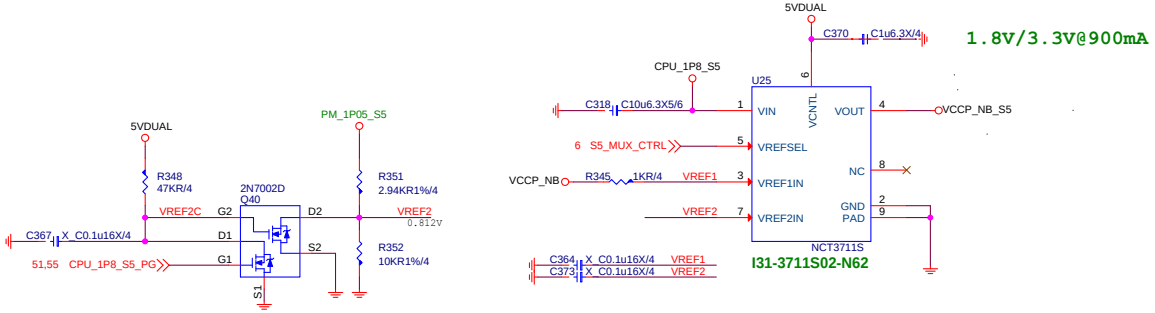
FOR VCCP_SOC_S5

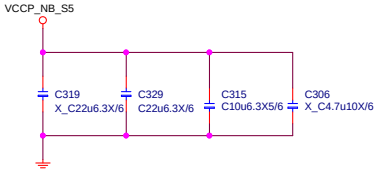
0.9A

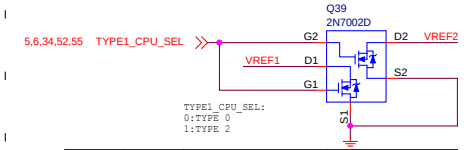
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)







CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

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Title: CPU NB_S5		
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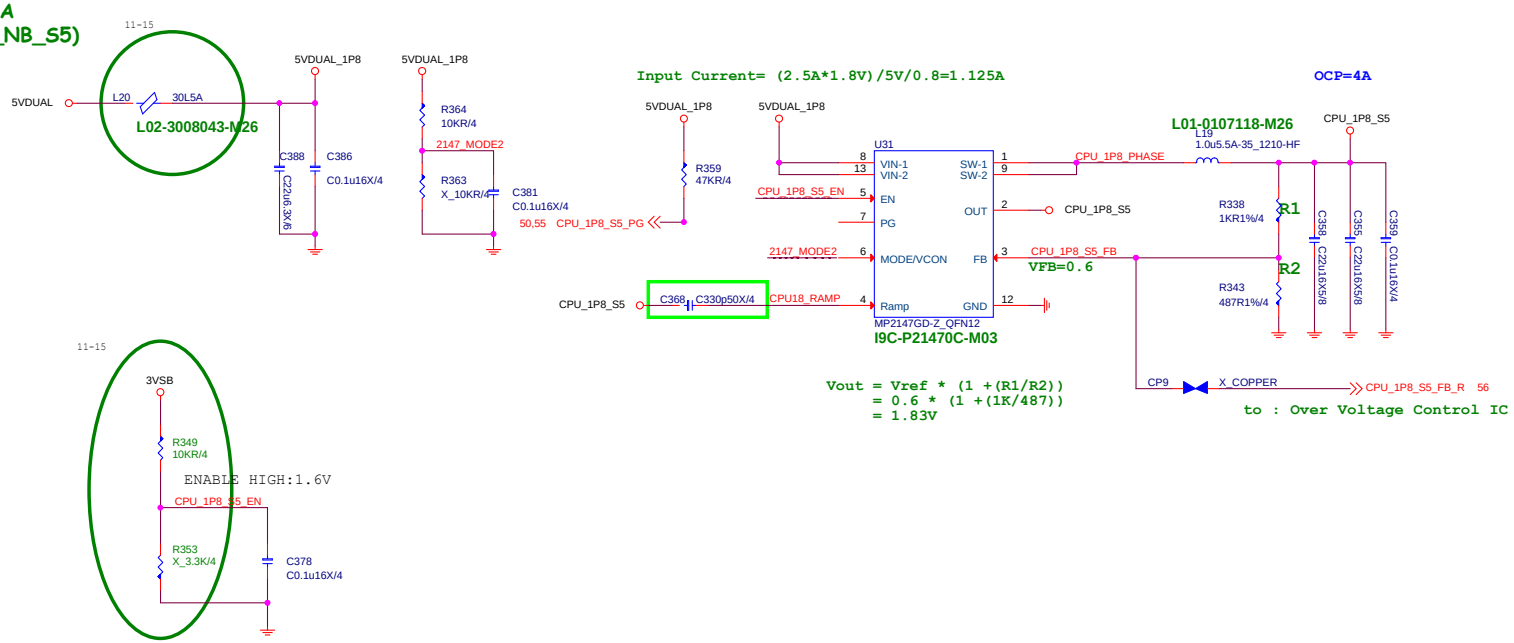
CPU 1.8V S5 @3.4A

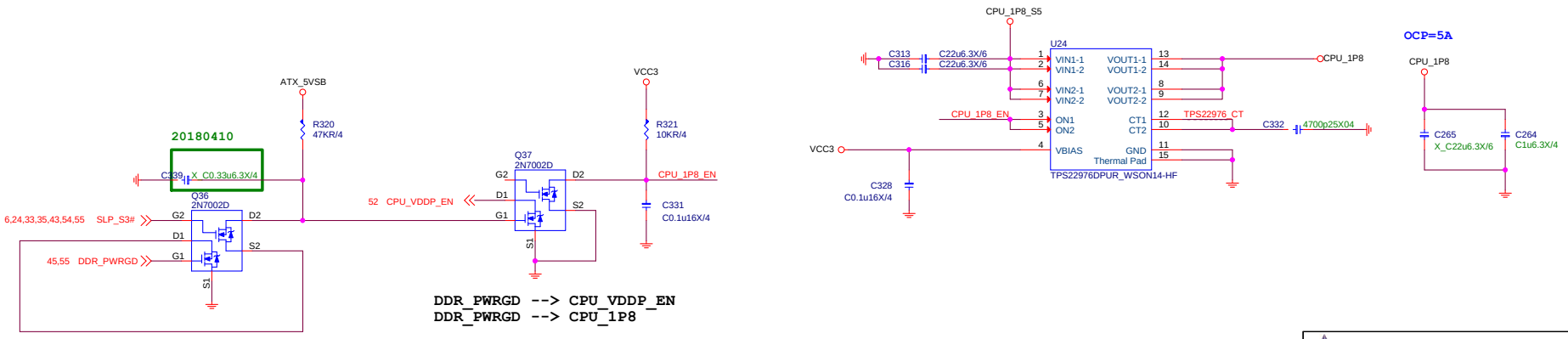
1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP_NB_S5)



CPU 1.8V S0

1.8V@2A

FOR VCCP_SOC@0.9A



MSI MICRO-STAR INT'L CO.,LTD.		
Title: CPU 1.8_S0/S5		
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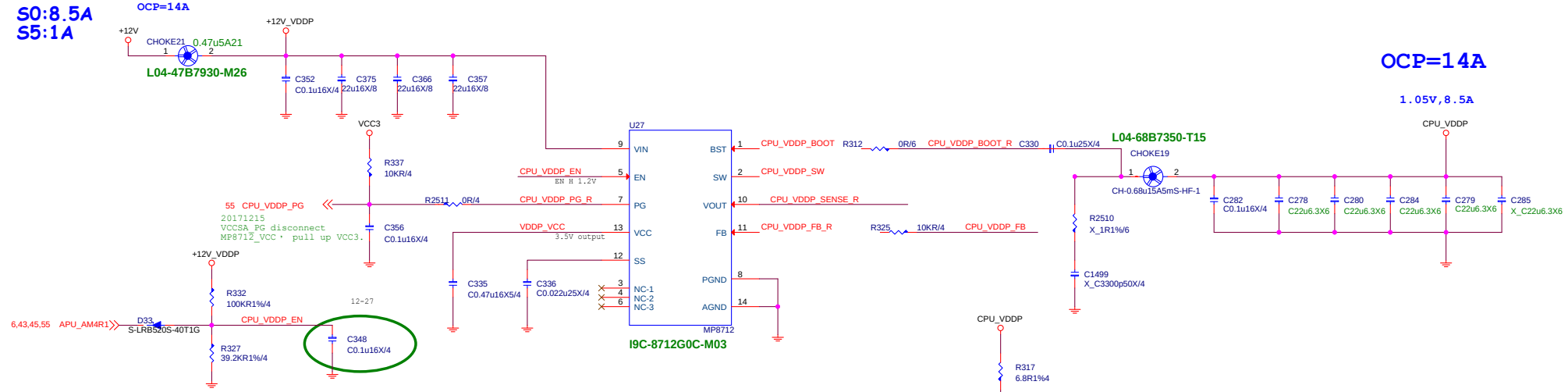
CPU_VDDP_S0

Input Current= (8.5A*1.05V)/12V/0.8=0.93A

1.05V/0.9V@S0:8.5A

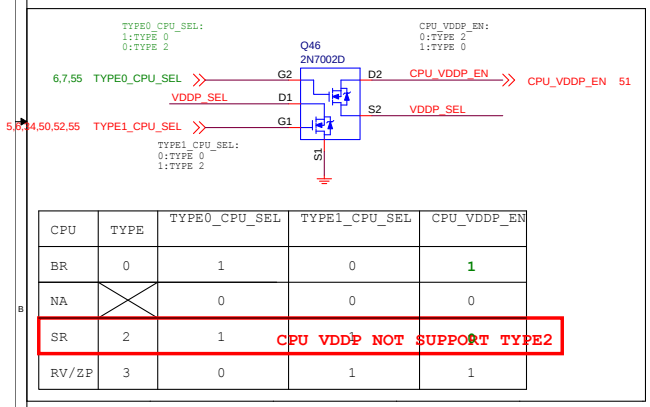
S0:8.5A
S5:1A

OCP=14A



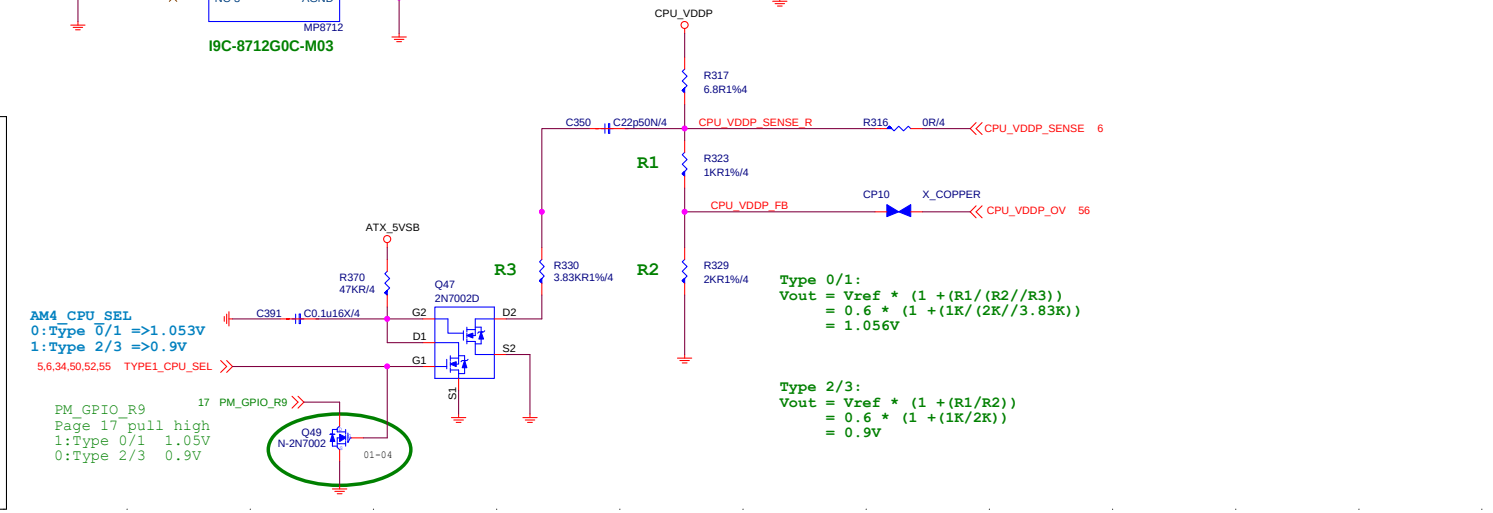
OCP=14A

1.05v,8.5A



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	1
NA		0	0	0
SR	2	1	1	1
RV/ZP	3	0	1	1

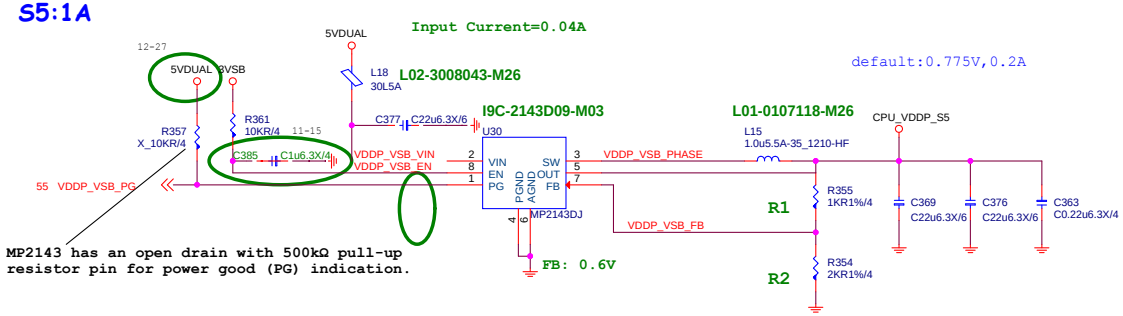
CPU VDDP NOT SUPPORT TYPE2



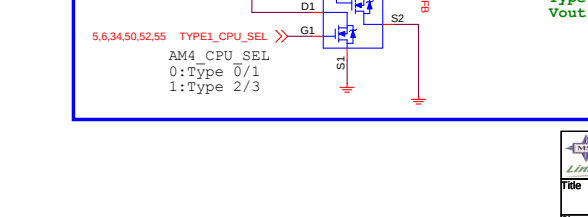
CPU_VDDP_S5

1.05V/0.9V
S5:1A

Input Current=0.04A



default:0.775V,0.2A



MICRO-START INT'L CO.,LTD.

Title: CPU Power VDDP

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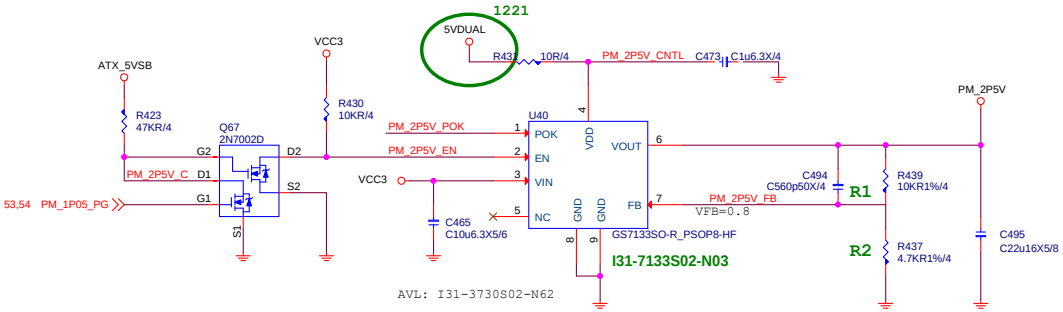
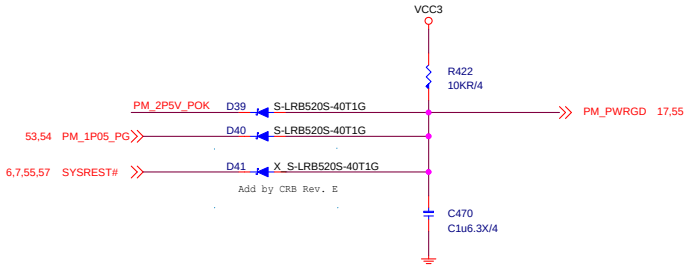
Promontory-2.5V

2.5V@900mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V



MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title: Prom-GS7133/2.5V		
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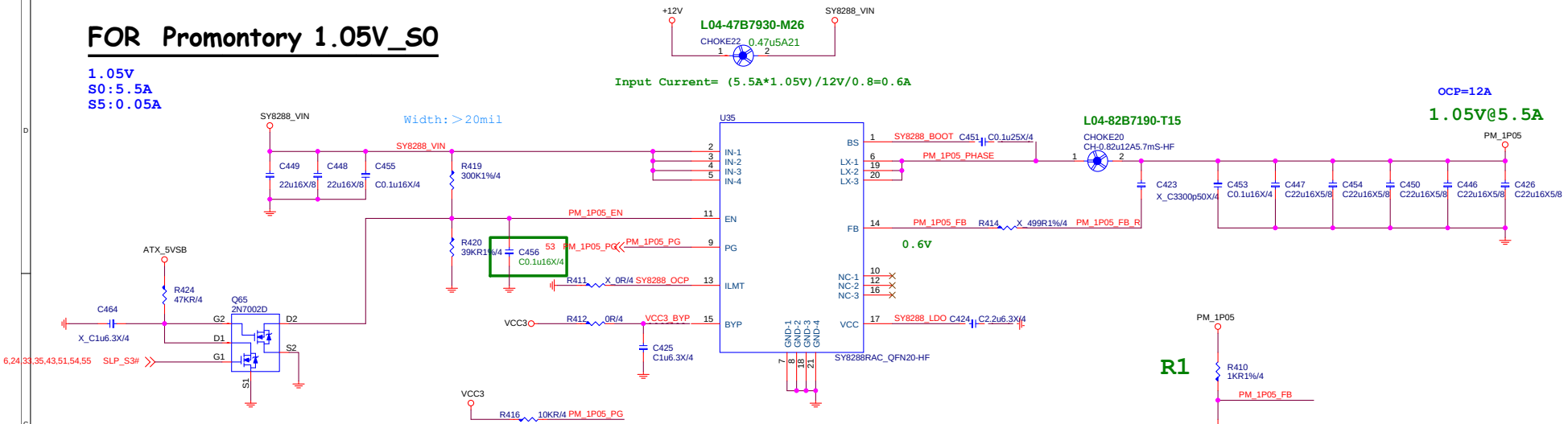
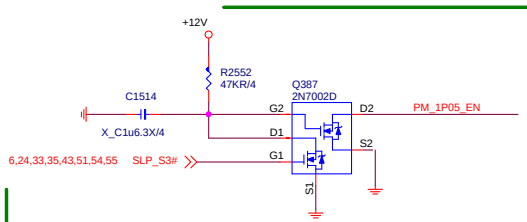
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

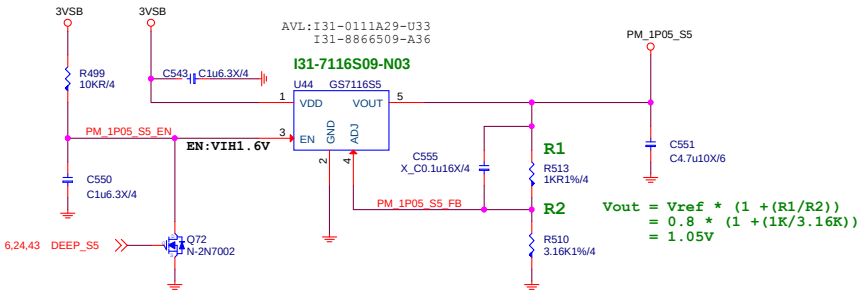


SY8288_OCP	OCP
0	8A
floating	12A
1	16A



FOR Promontory 1.05V_S5

1.05V@0.05A



MICRO-START INT'L CO.,LTD.

Title	Prom- SY8288RAC / 1.05V	
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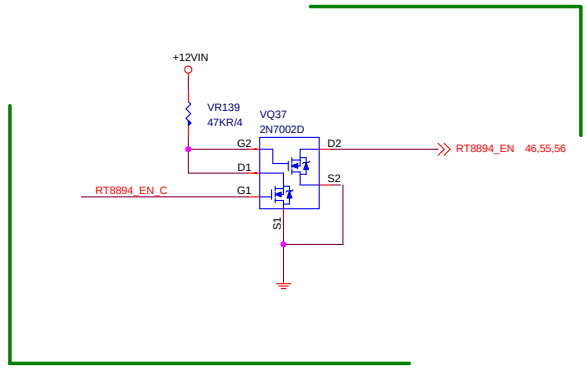
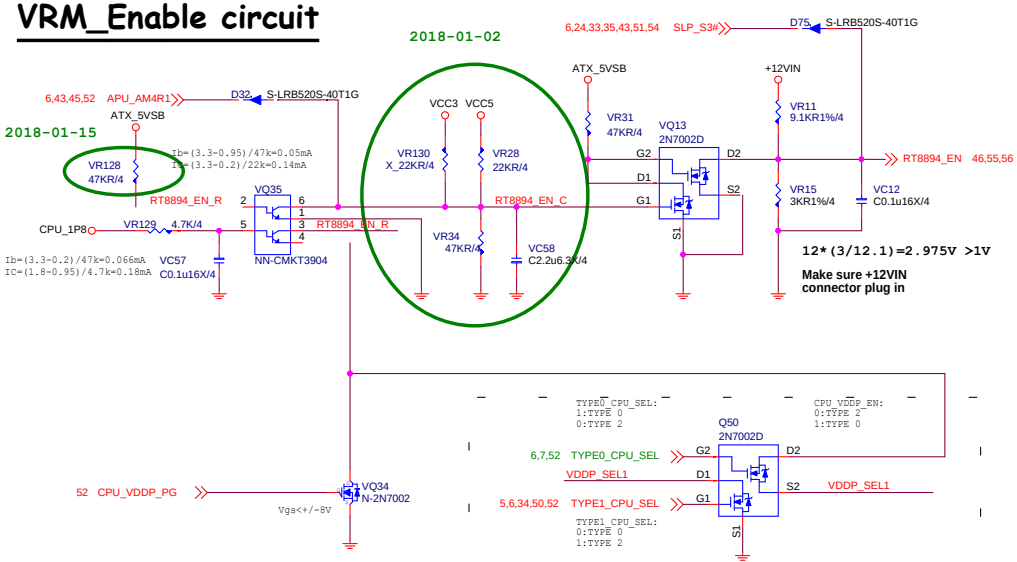
VRM_Enable circuit

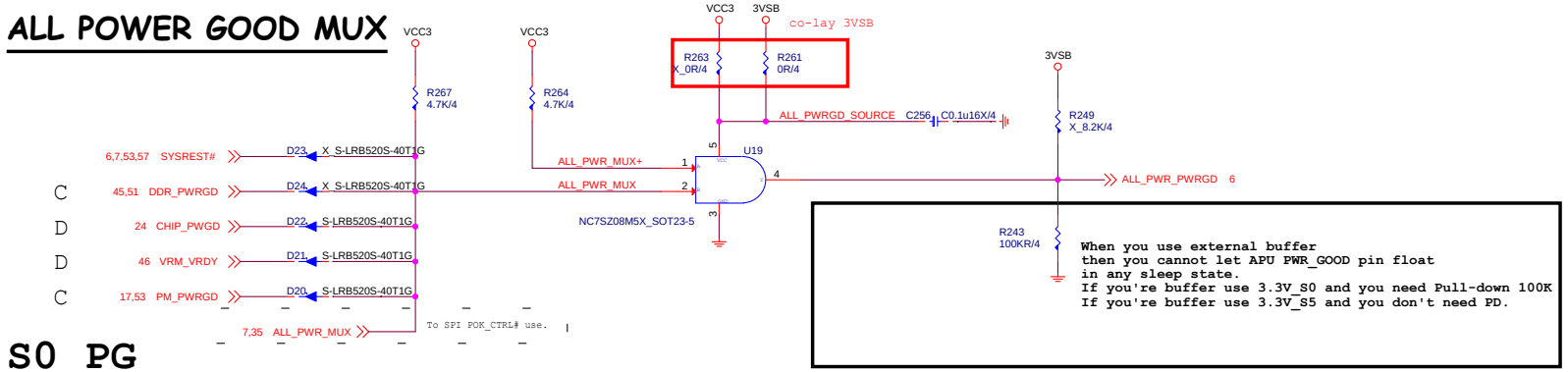




CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

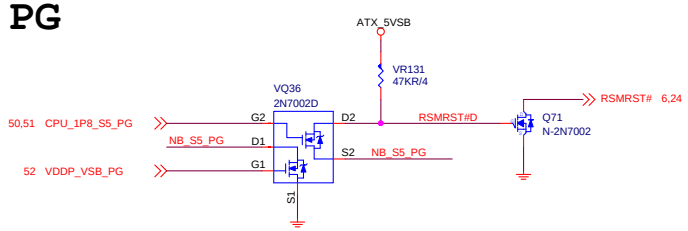
ALL POWER GOOD MUX



When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	VRM-EN/PWRGD	
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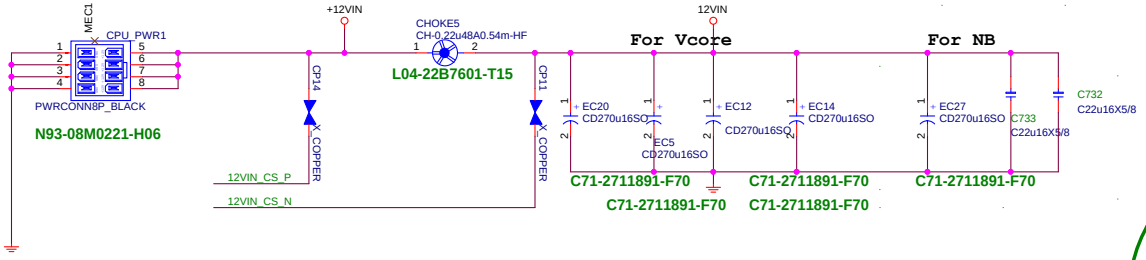
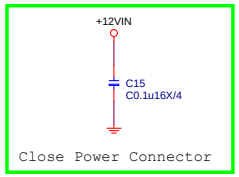
CPU POWER CONNECTOR



11-22

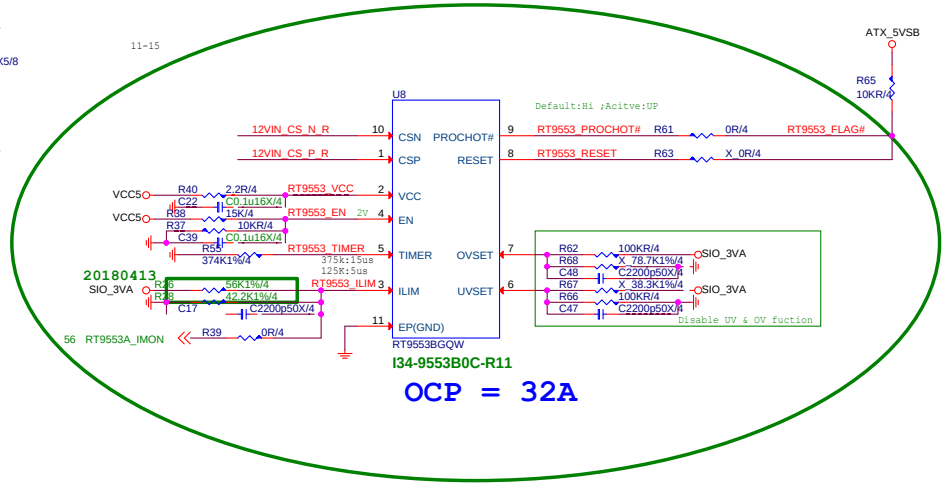
NB				VCCP			
D=Vout/Vin				D=Vout/Vin			
Vin	= 12	> input voltage		Vin	= 12	> input voltage	
Vout	= 1.4	> output Vcore		Vout	= 1.4	> output Vcore	
D	= 0.116667			D	= 0.116667		
Io = Icore(max)*0.8				Io = Icore(max)*0.8			
I core(max)	= 75	> Vcore current		I core(max)	= 125	> Vcore current	
I avg.	= 75	A		I avg.	= 125	A	
Iripple={ Io*√ D*√ (1-D)} / Phase				Iripple={ Io*√ D*√ (1-D)} / Phase			
Phase	= 2	phase		Phase	= 4	phase	
I ripple	= 12.03835	A		I ripple	= 10.03196	A	
How many pcs. Of Cap.				How many pcs. Of Cap.			
I ripple(cap)	= 5000	m A		I ripple(cap)	= 5000	m A	
COETEMP	= 1			COETEMP	= 1		
Input Cap.	= 3	pcs.		Input Cap.	= 3	pcs.	



11-15

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

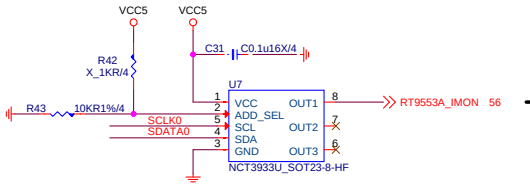


Over Voltage Control IC

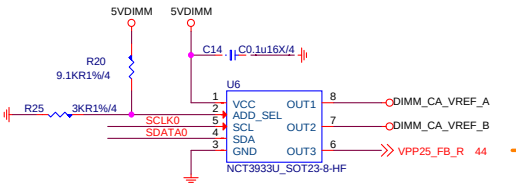
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

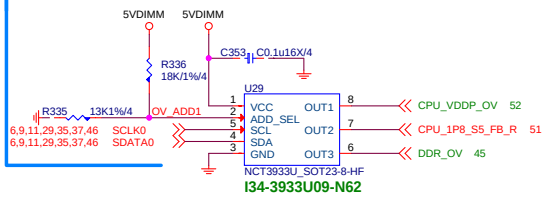
0x2A:RH=OPEN,RL=10K

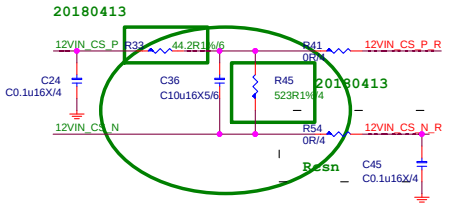


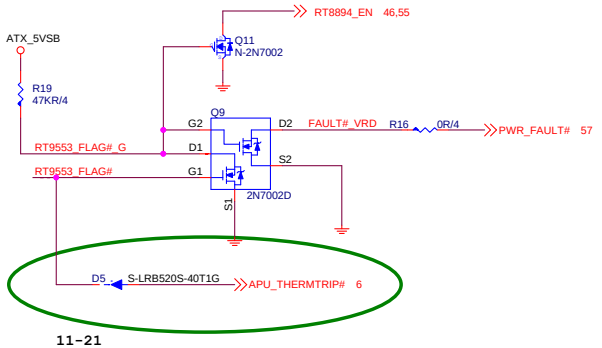
0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K







11-21

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	RT9553B CURRENT SENSE/OV Control	
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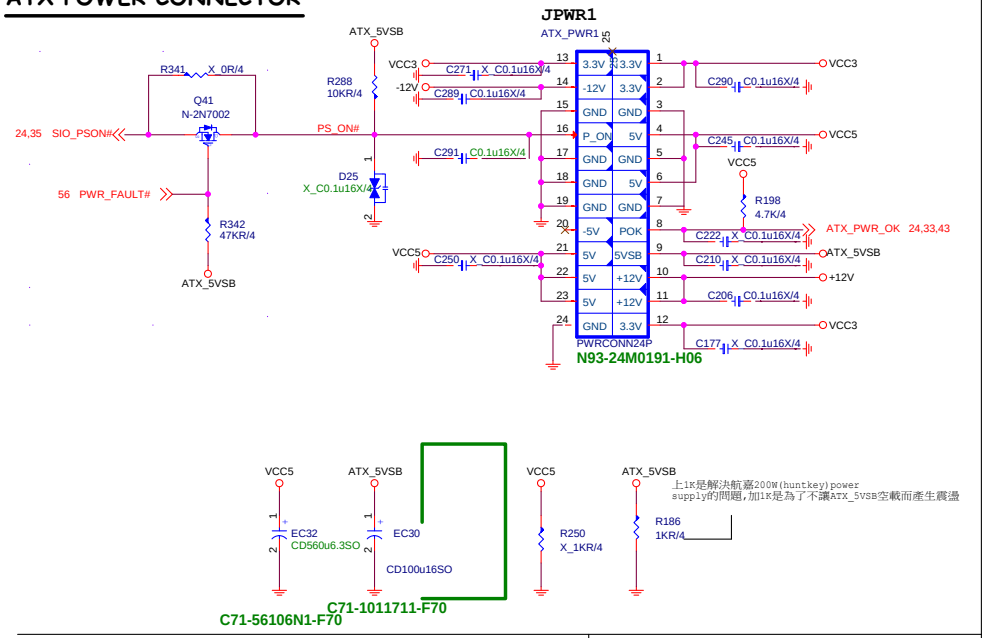
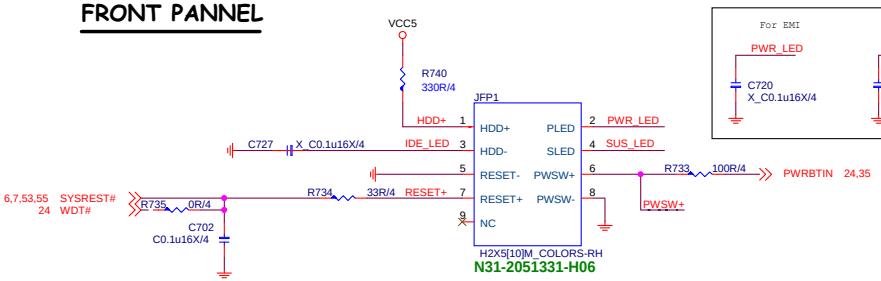
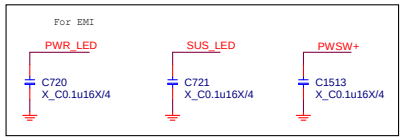
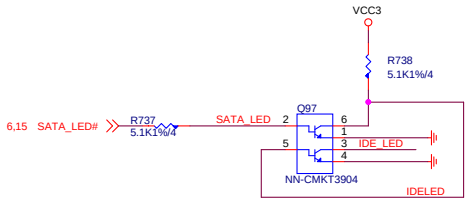
ATX POWER CONNECTOR

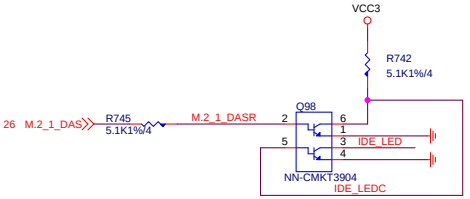


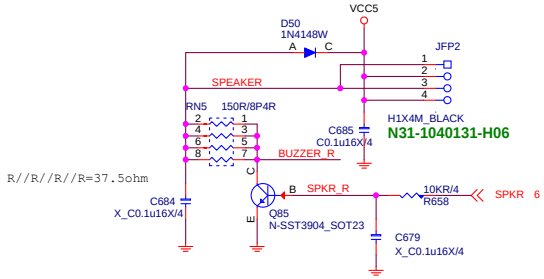
FRONT PANNEL



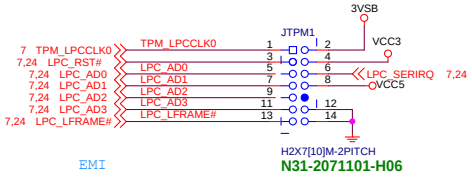




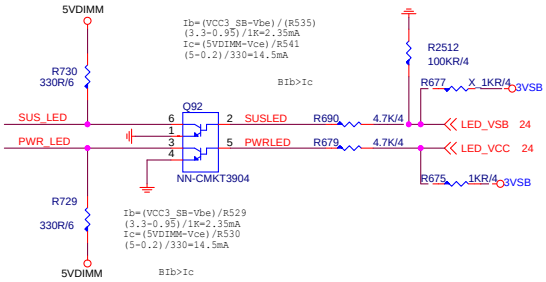




TPM

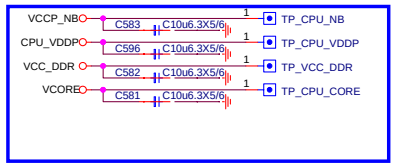


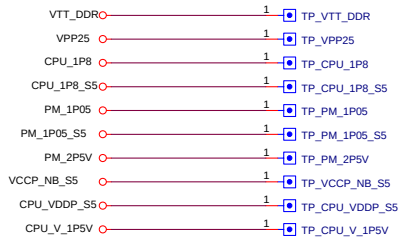
LED (for NCT6797)



Voltage Mearsure Point

TP close to SIO
Cap close to TP





MICRO-START INT'L CO.,LTD.

Title: ATX/Front Panel		
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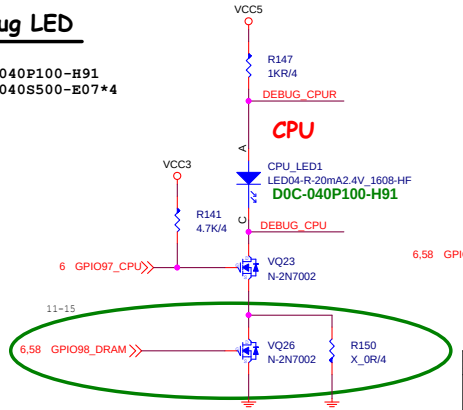
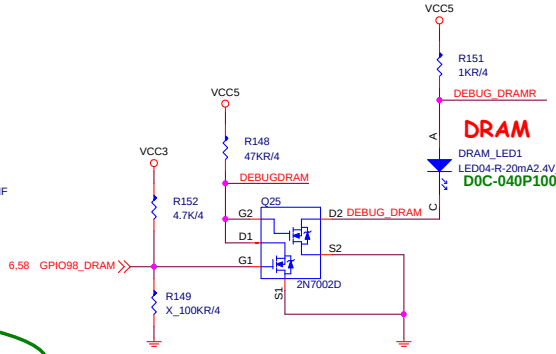
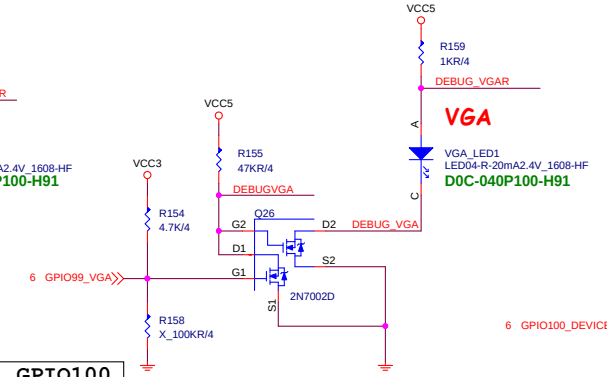
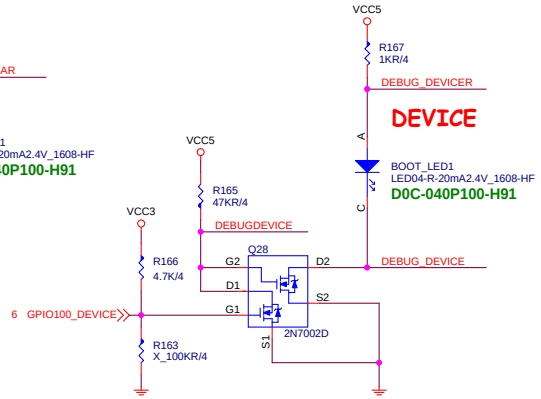
EZ Debug LED

紅:M:D0C-040P100-H91
S:D0C-040S500-E07*4









LED亮燈時同時將 CPU LED關掉

LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

MSI MICRO-STAR INT'L CO.,LTD.
Link to the Future

Title	ALL LED Control		
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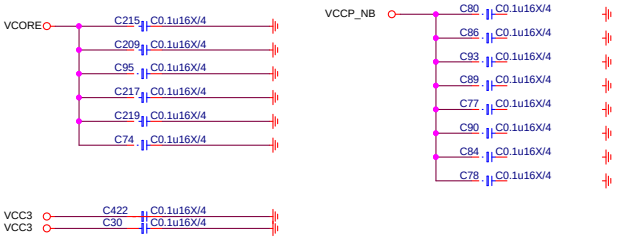
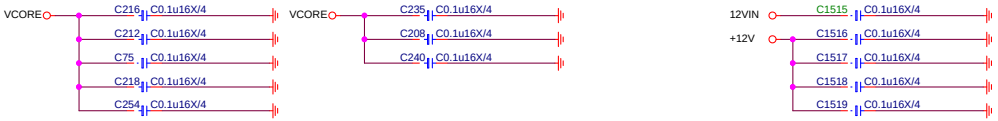
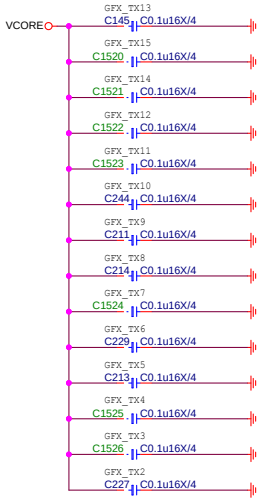
Add for EMI



return path





MICRO-START INT'L CO.,LTD.

Title: NCT7718W temp sensor /EMI CAP		
Size: Custom	Document Number: MS-7C02	Rev: 1.0
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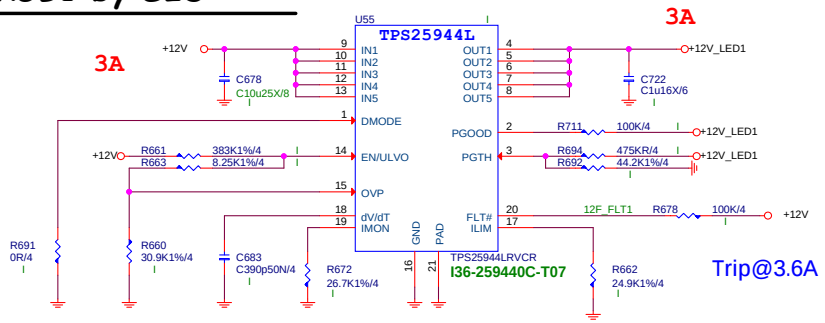
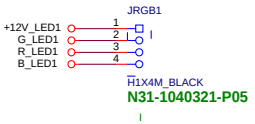
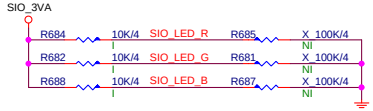
JRGB1 by SIO

2016.07.06 Use TPS25944L



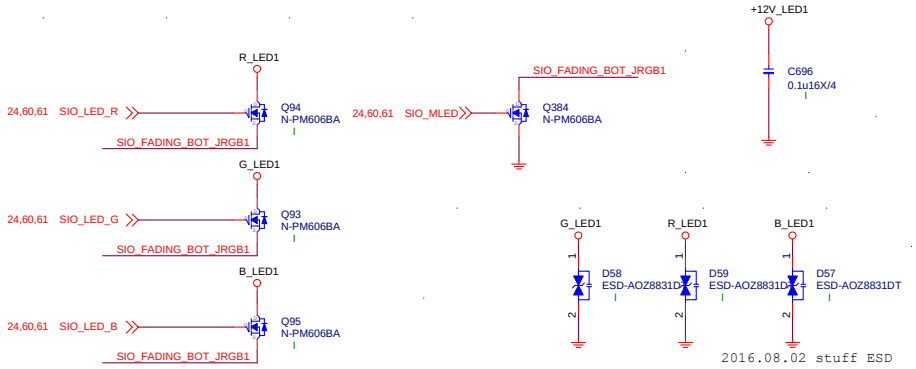
Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1





PM SPEC Default WHITE Color

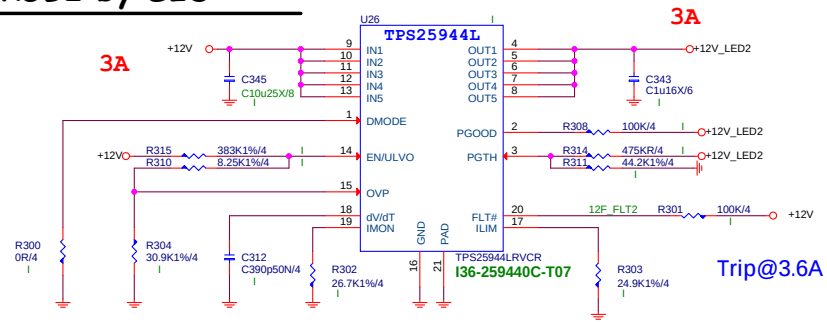
2016.08.02 Add +12V_LED 0.1uF

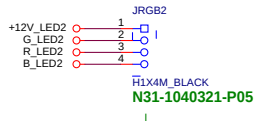


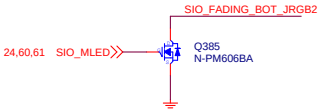
2016.08.02 stuff ESD

JRGB2 by SIO

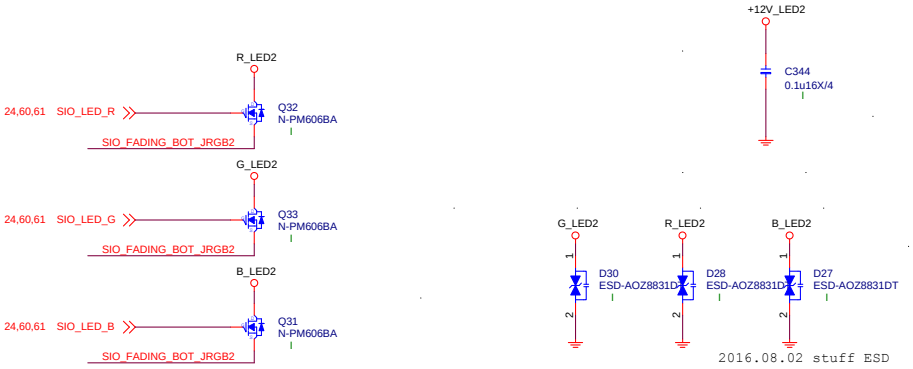
2016.07.06 Use TPS25944L







2016.08.02 Add +12V_LED 0.1uF



2016.08.02 stuff ESD

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Link to the Future

Title: JRGB1/JRGB2			
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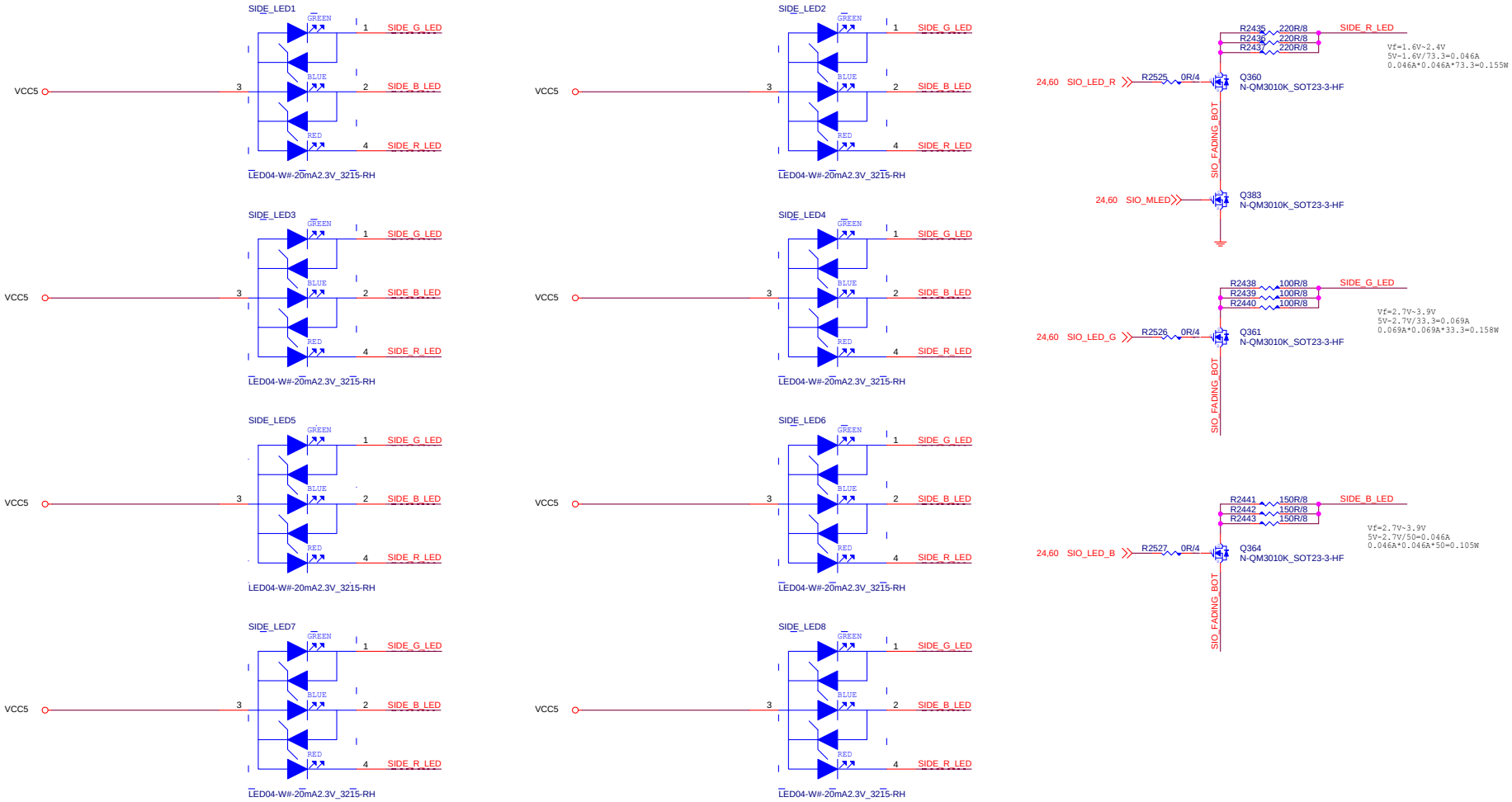
BOARD SIDE LED *8



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Link to the Future

Title: RGB LED Control		
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OPTION BOM PARTS

60 Level

A	B	C	D	E
PCIE X16 SLOT				
PCIE X8 SLOT			FOOTPRINT SLOT_PCIEXP100_5 可包容 SLOT_PCIEXP100_3	
REAL USB Type A			鍍金	
SOLID CAP 270u16			FOOTPRINT C_P3_5_D8_H12 因為機構無法使用 請注意! C_P3_5_D8_H9 可包容 C_P3_5_D8_H8	
SOLID CAP 560u6.3			FOOTPRINT C_P2_5_D6_3_H9_5 可包容 C_P2_5_D6_3_H9	
SOLID CAP 470u6.3			FOOTPRINT C_P2_5_D6_3_H9_5 可包容 C_P2_5_D6_3_H9	
SOLID CAP 100u16			FOOTPRINT C_P2_5_D6_3_H6 可包容 C_P2_5_D6_3_H5	
MEM SLOT			FOOTPRINT DDRIV_D288_1_T 可包容 DDRIV_D288	
MKTG Label				
PCH SINK				
MOSN +IO				
MOSW				
PS2_USB				
HDMI_USB				
LAN_USB				

5010 Level

A	B	C	D	E
FCH				
M.2 SLOT			FOOTPRINT SLOT_NGFFCARD67_31 可包容 SLOT_NGFFCARD67_2	
REAL USB Type C				
PCB				
0 Ohm (0402)				
LED				

5020 Level

A	B	C	D	E
LED				

60 Level

A	B	C	D	E
Audio cover				
Audio Jack				
M.2 SCREW				
PCIE X4 SLOT				

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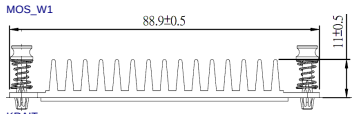
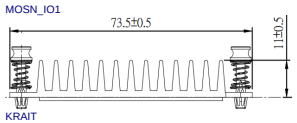
11-16

RM: E95-0000022-C22/ E95-0000022-A91

MOS SINK



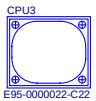
OE3-7C02001-A87



OE3-7C02002-A87

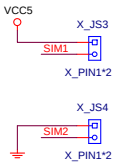
DDR Cover

CPU Socket

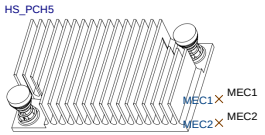


E95-0000022-C22

Simulation



PCH SINK



OE3-7C02003-A87

AUDIO COVER

MANUAL PART

AVL:
D06-0100161-F52
D06-0100101-K26

PD0-07C0210-G37,精成-深圳,1,台北微星廠(MSI)
PD0-07C0210-G37,精成-深圳,9,寶安恩斯邁廠(MSIS)

BIOS LABEL

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

MKTG name Label

MKTG1

G51-M1SPK15-Q13

ROYALTY

HDMI_LA1

Y01-RHDMI03-000

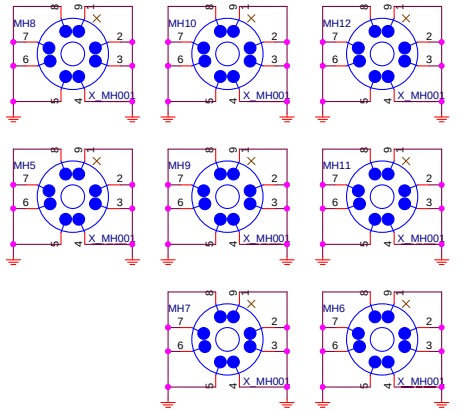
Y01-RHDMI03-000

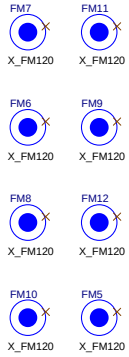
NAHIMIC

Y02-MU00100-NAH

Y02-MU00100-NAH

Optics Orientation Holes





Schematic Cfg	Project	
CFG-7C02-xx	V	A
CFG-7xxxxxxx-Arsenal Gaming		

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