LCFC Confidential

330 CFL-H +N17P MB Schematics Document

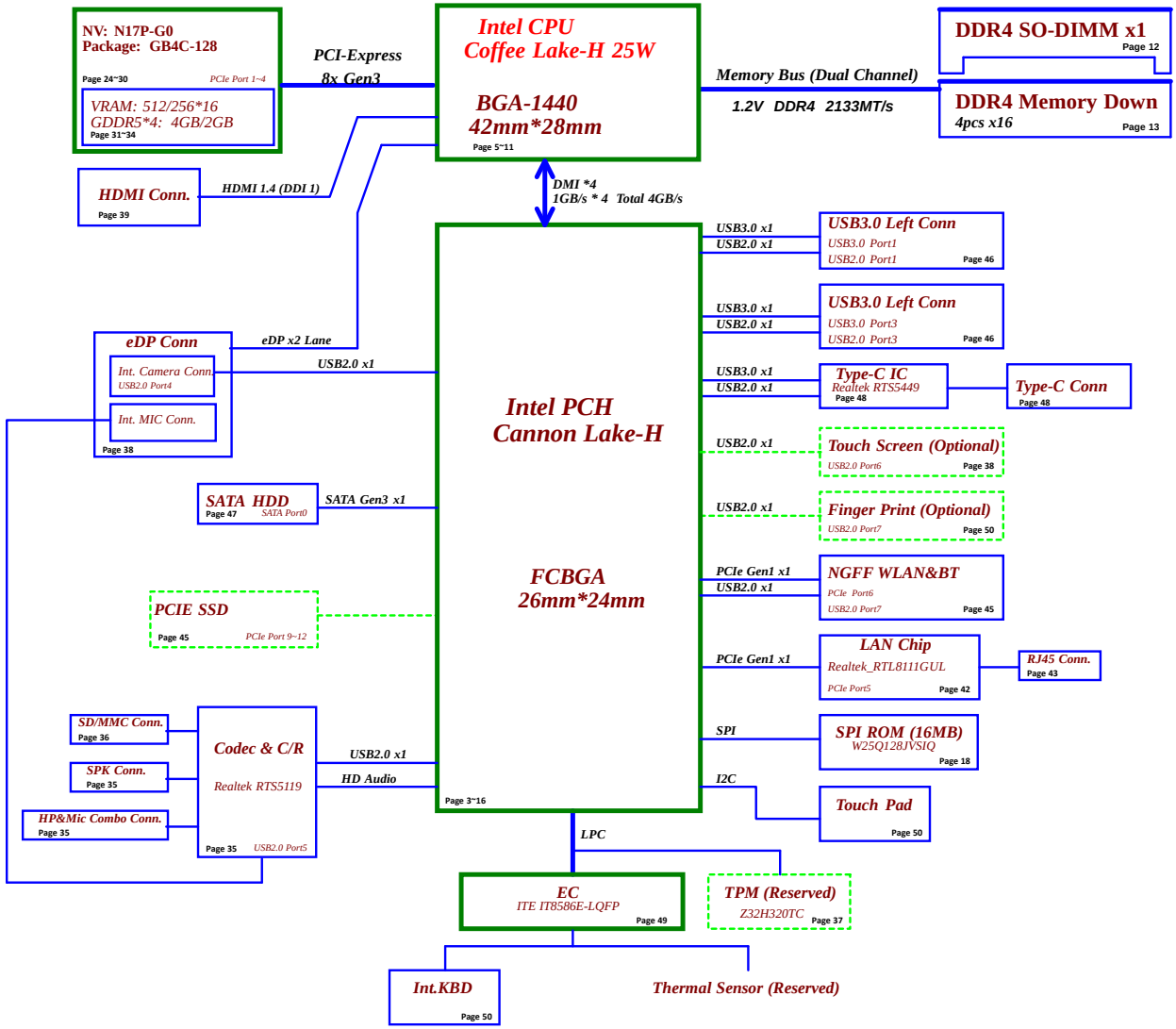
Coffee Lake-H with DDR4 + Nvidia N17P-G0

2018-03-20

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page			
Size: Custom	Document Number: EG530		Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 1 of 68		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Block Diagram

Size: Custom	Document Number: E6539	Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 2 of 68	

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	0	0	0	0
S3	0	0	0	X
S3 Battery only	0	0	0	X
S5 S4 AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
17@	For 17" part
15or17@	For 15" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
TS@	For touch screen part
TS_NS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TPM@	For TPM part
UMA@	For UMA part

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

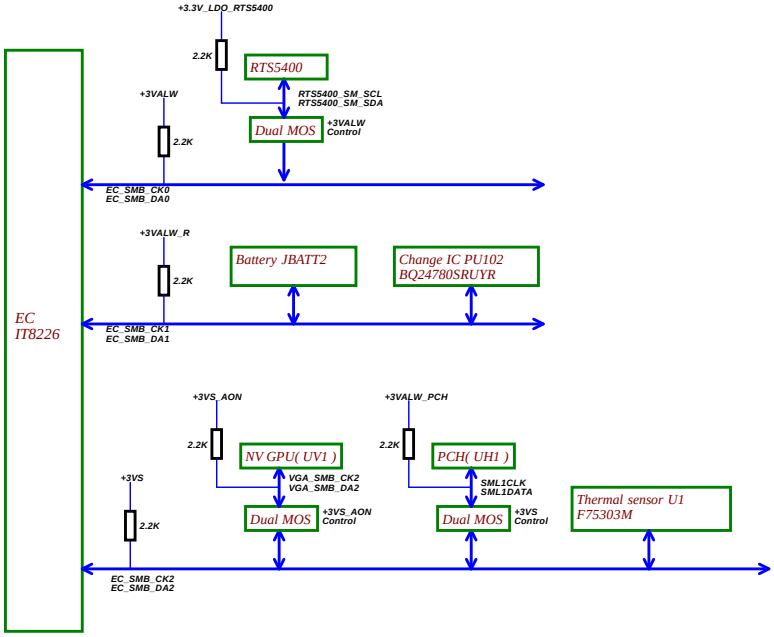
PCH SM Bus address

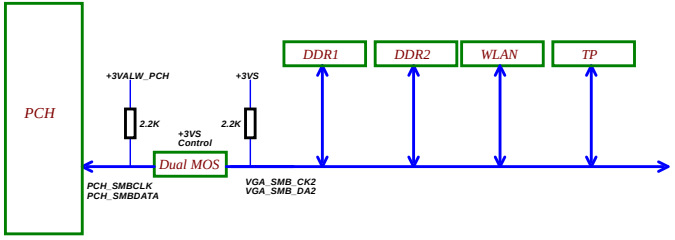
Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

Title: Notes List

Size: Custom | Document Number: EG530 | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 3 of 68





SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8226 +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8226 +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100xb
VGA	0x41(default)
PCH	need to update
RTS5400	0xD4

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
WLAN	Rsvd

Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Blank4

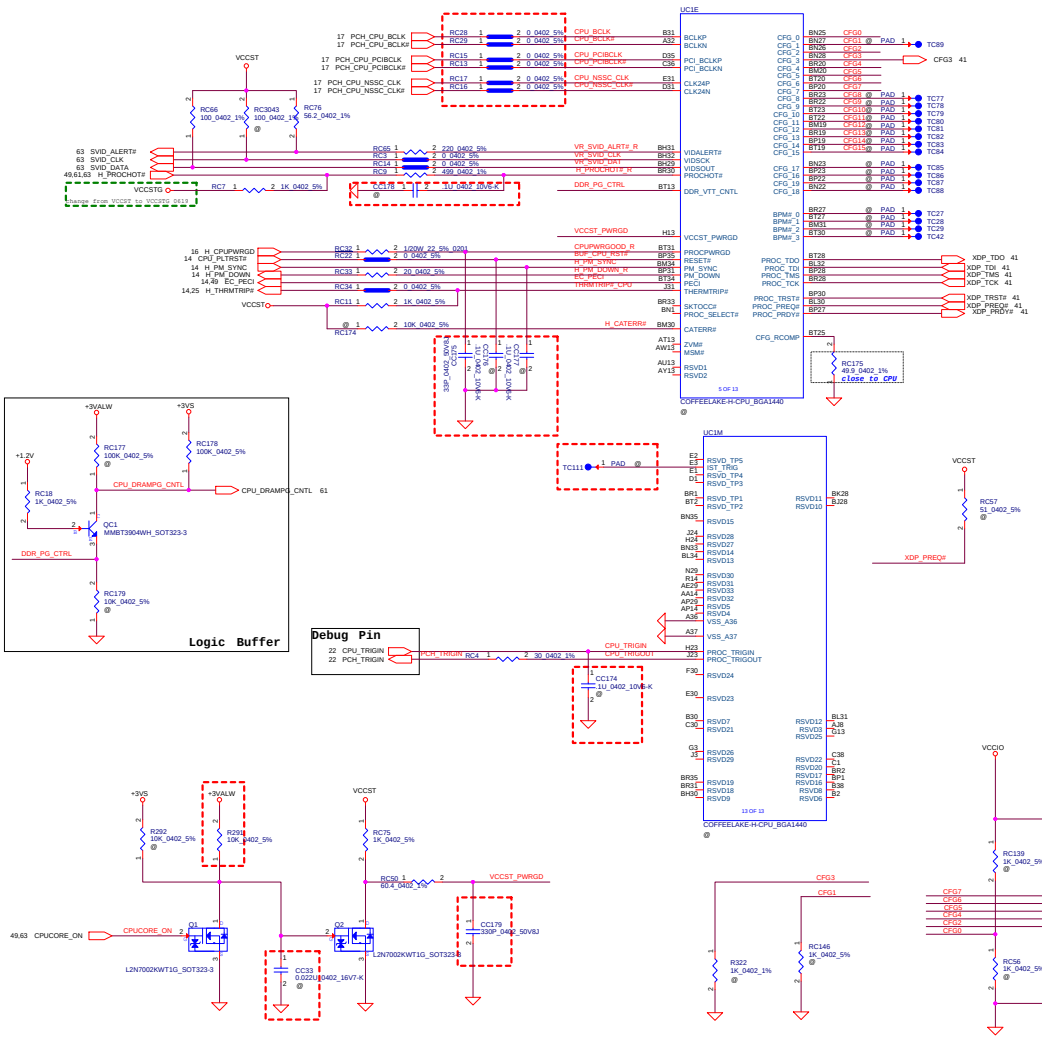
Size	Document Number		Rev
Custom		E6530	1.0
Date:	Thursday, March 24, 2016	Sheet	4 of 46

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (1/7) DMI,PEG

Size	Document Number	Rev
Custom	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 5 of 68



CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

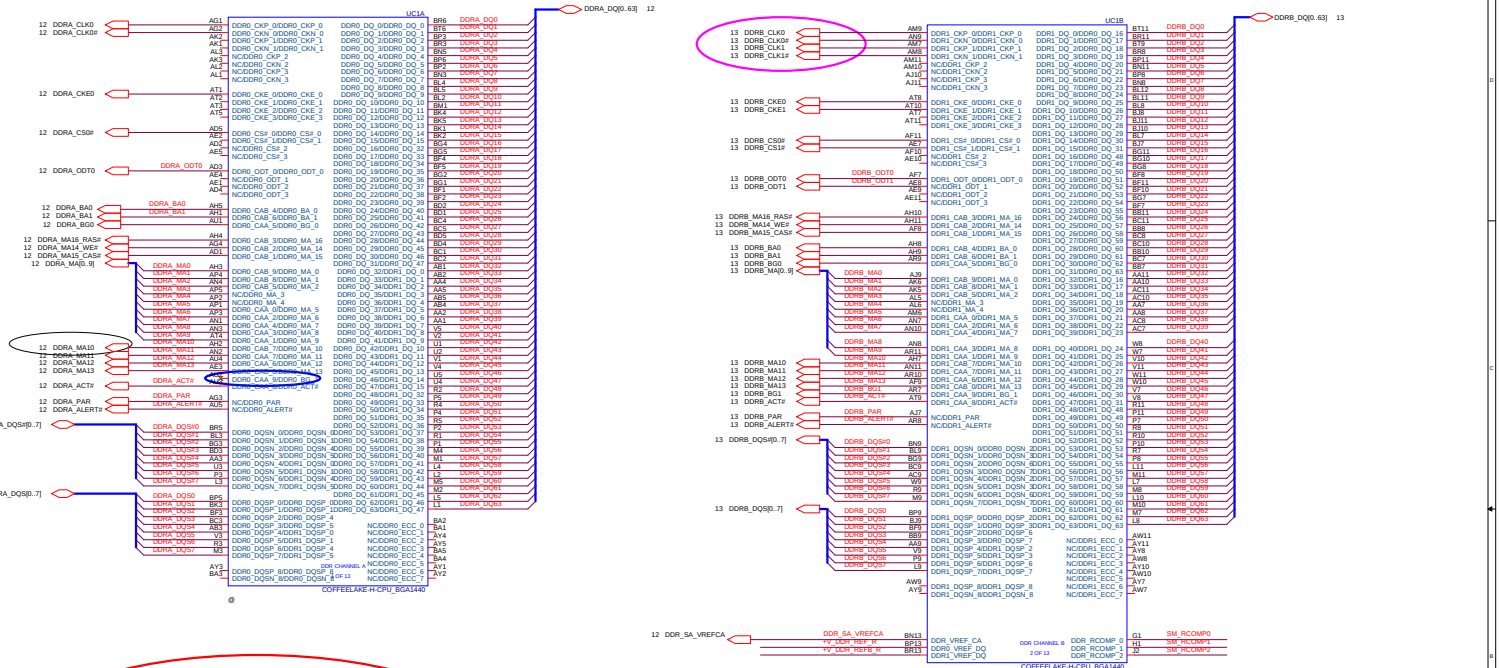
eDP enable	
CFG4	1 = Disabled. ★ 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* ★ 11 = 1 x16 PCI Express*

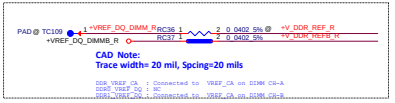
PEG Training	
CFG7	★ 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.

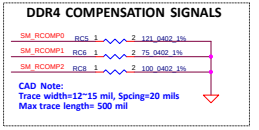
Reserved configuration lane.	
CFG[19:8]	N/A

Title			
CPU (2/7) PM, XDP, CLK, CFG			
Size: Custom	Document Number: E6530		Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 6 of 68		



Follow 1.0PDG to reserve 3.3P_0201 capacitor between DDRA_CLK0 and DDRA_CLK0# --SF0904



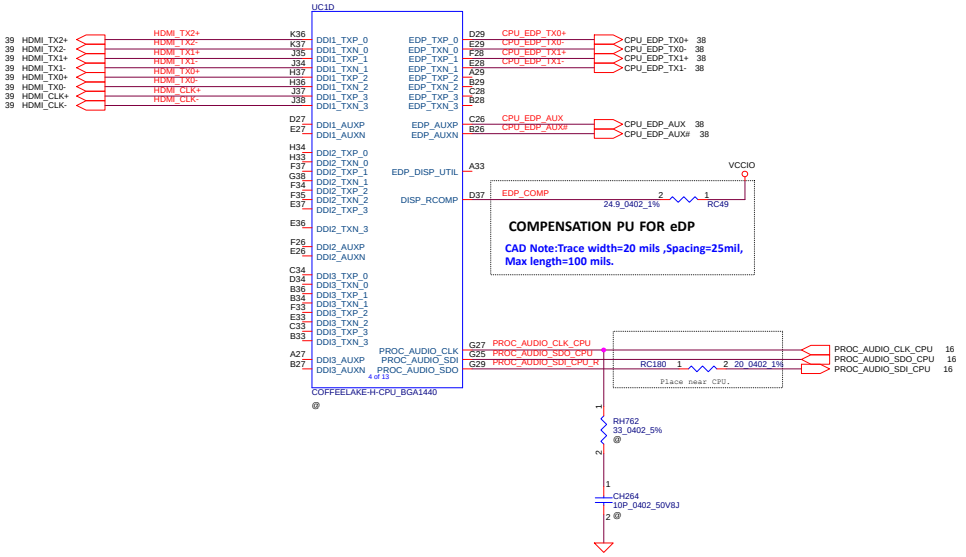


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 7 of 68

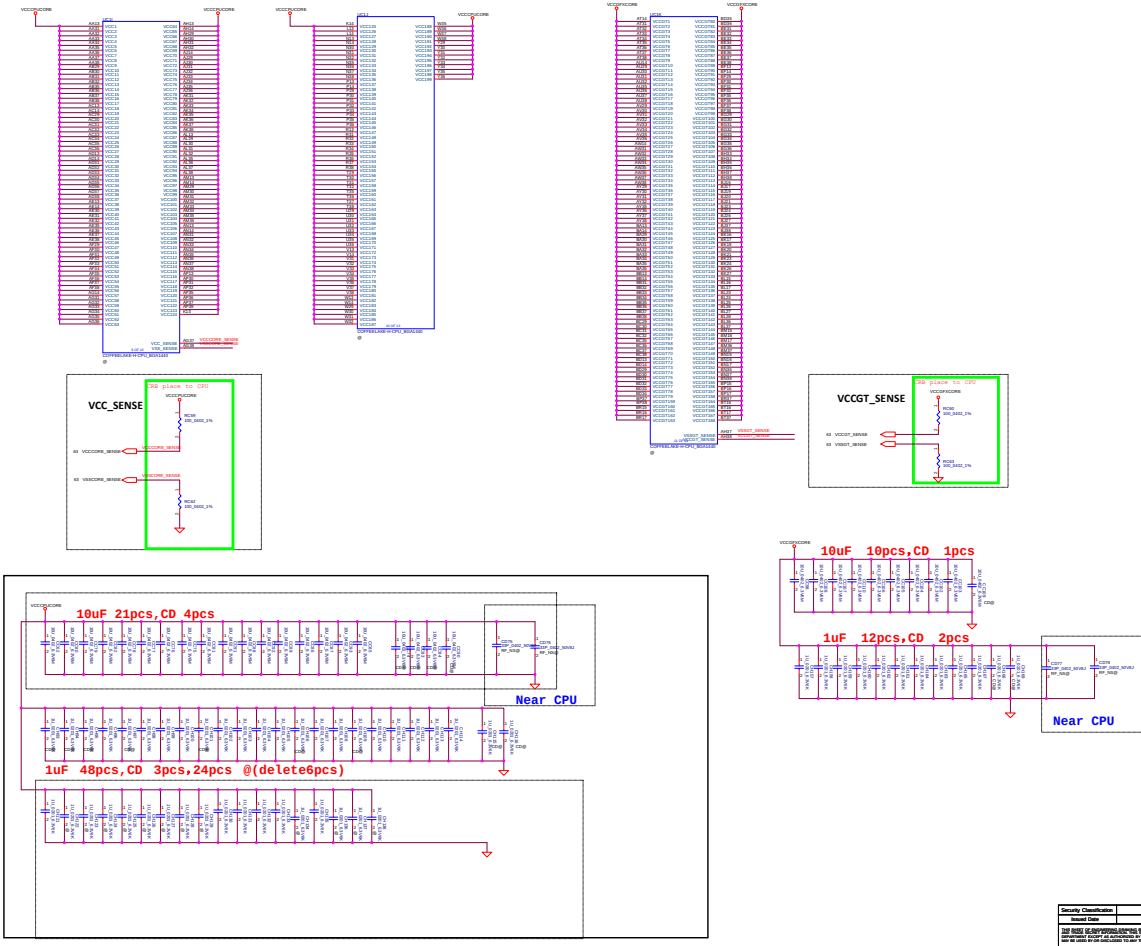


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

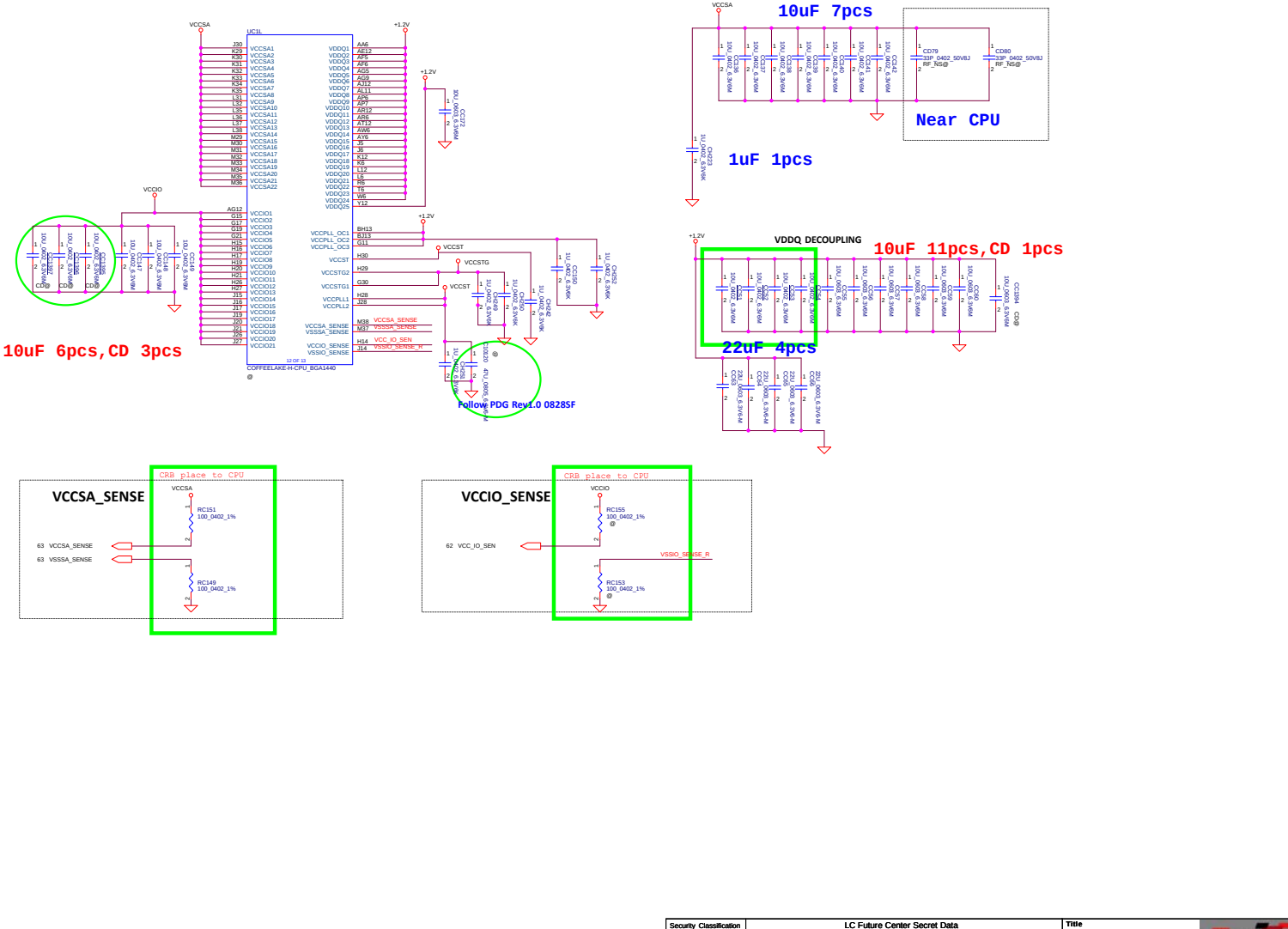
Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
A3	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 8 of 68



Security Classification	LC Future Center Secret Data		Title: CPU (5/7) PWR, BYPASS
Issued Date: 2015/02/26	Deciphered Date: 2016/02/26		
Size: D	Document Number: E6536		Rev: 14
Date: Tuesday, March 29, 2016	Sheet: 9 of 49		



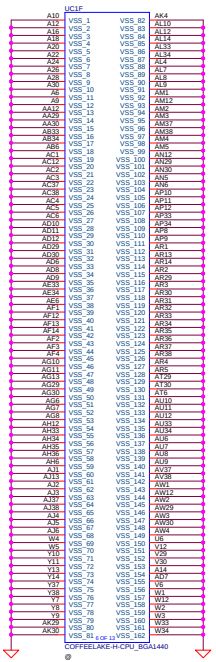
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

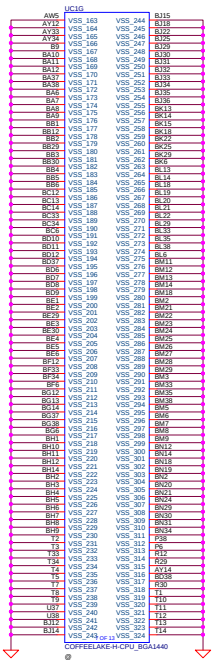
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

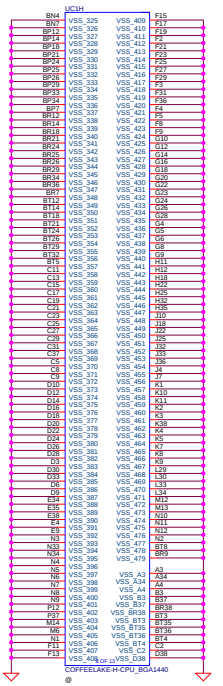
Title: CPU (6/7) PWR, BYPASS

Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 10 of 68

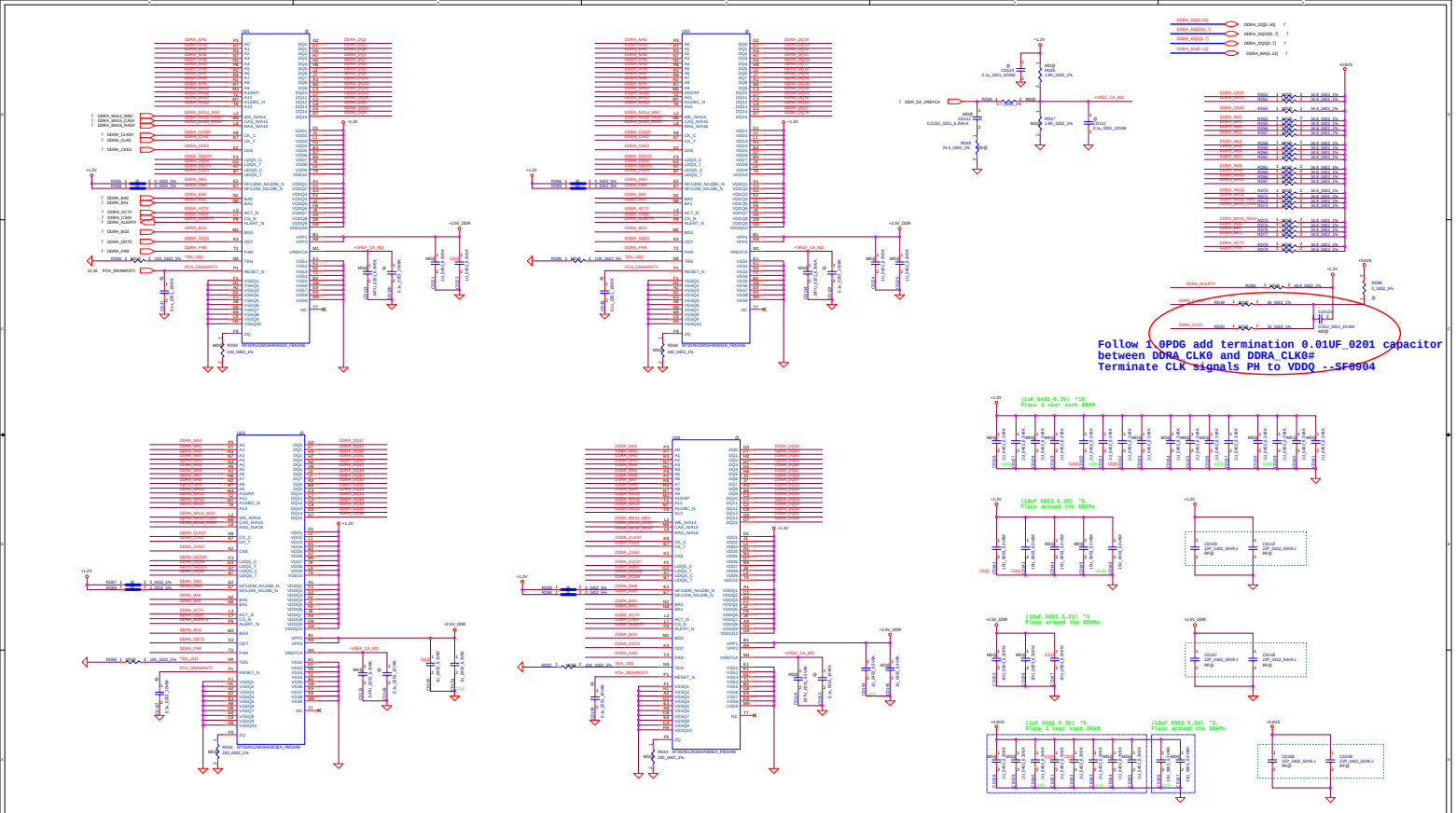






Security Classification	LC Future Center Secret Data		Title: CPU (6/7) PWR, VSS
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Size	Document Number	Rev
C	E6530	1.0
Date: Thursday, March 29, 2018	Sheet 11 of 68	



Security Classification	LC Future Center Secret Data		Title
Issued Date	2016/12/14	Deciphered Date	2017/12/13

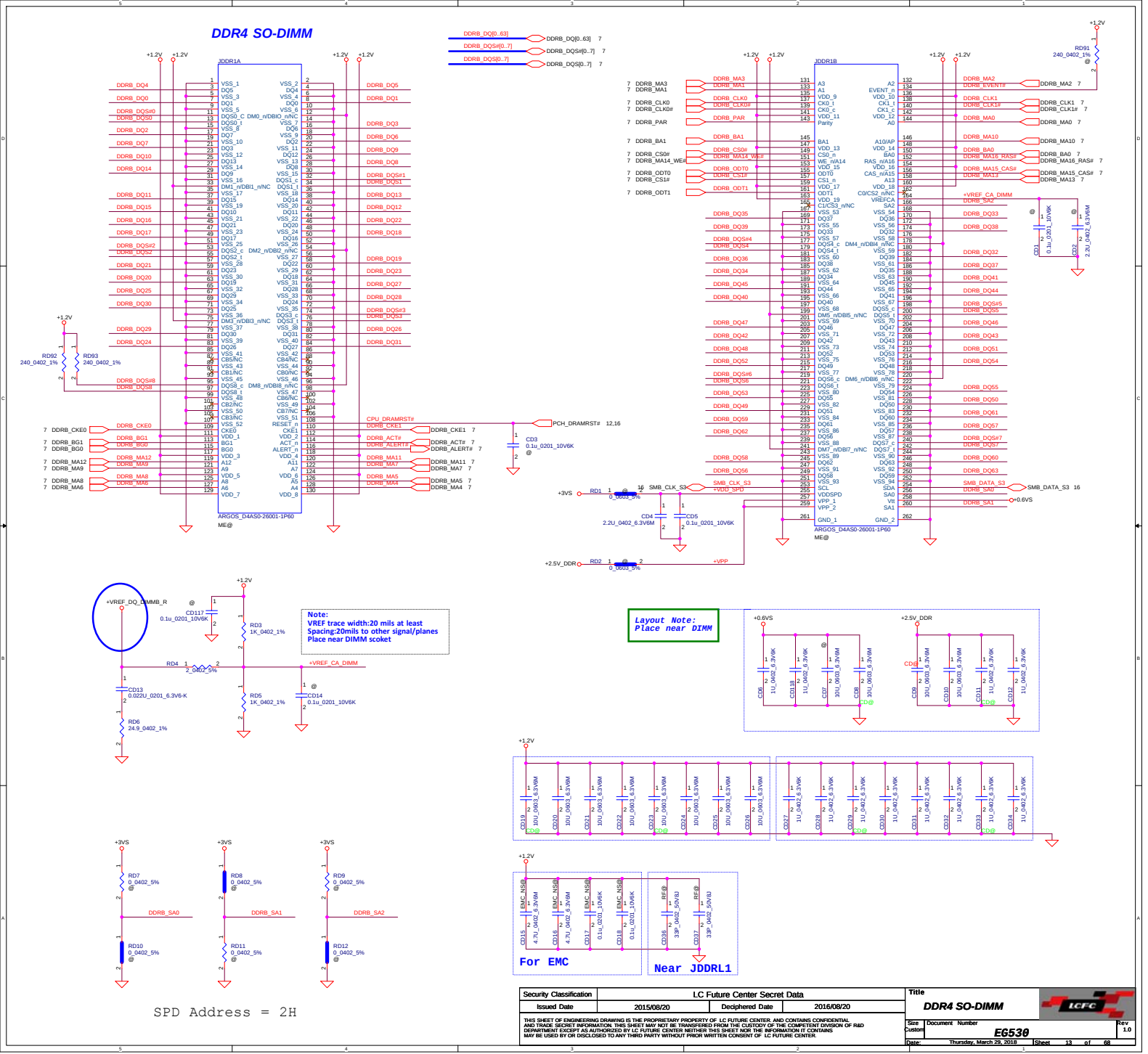
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D EXCEPT AS AUTHORIZED BY LC FUTURE CENTER MANAGEMENT, NEITHER IT NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

DDR4 Memory Down

Size	Document Number	Rev
Custom	E6530	1.0

Date: Thursday, March 15, 2018 Sheet 27 of 38

DDR4 SO-DIMM



Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM

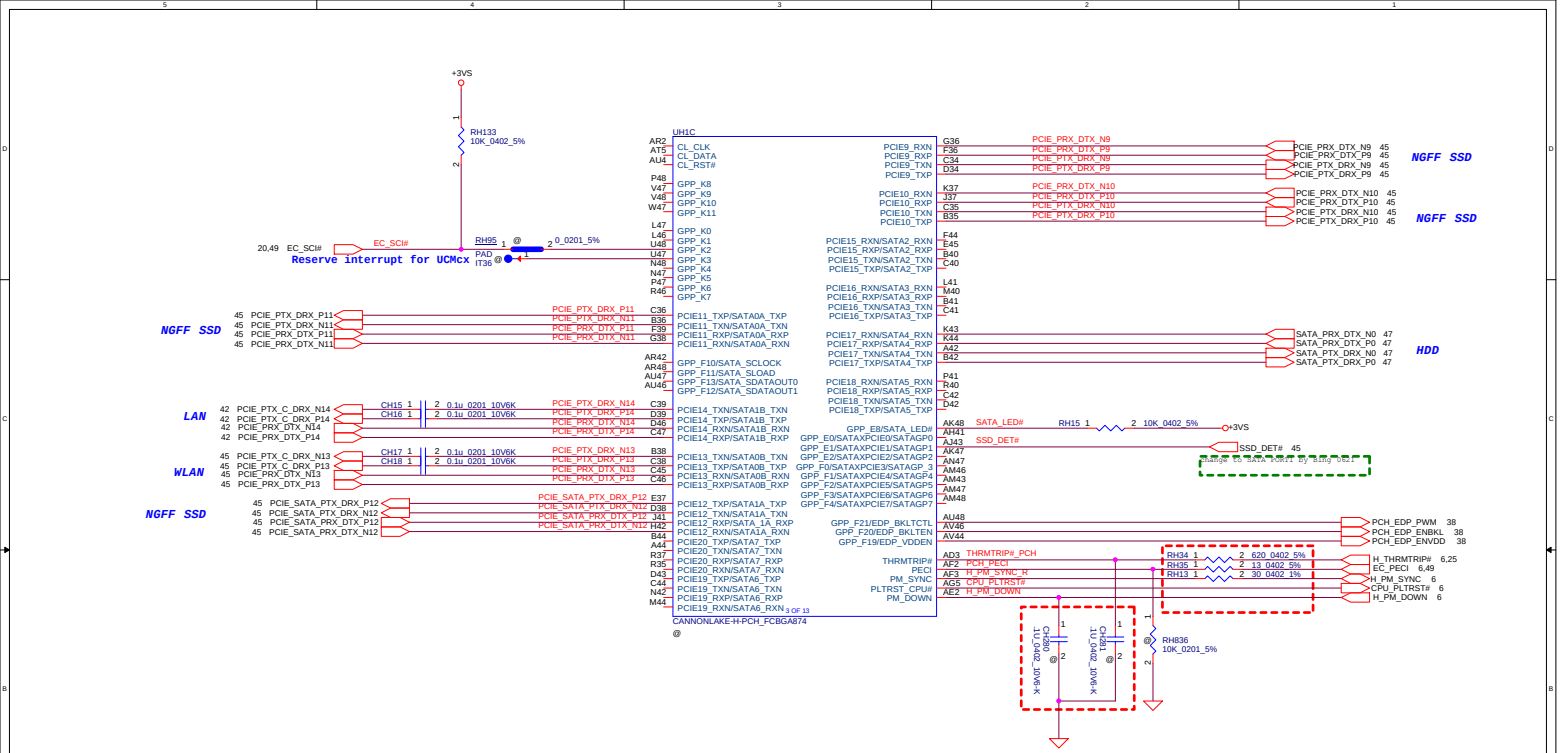
For EMC

Near JDDRL1

SPD Address = 2H

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

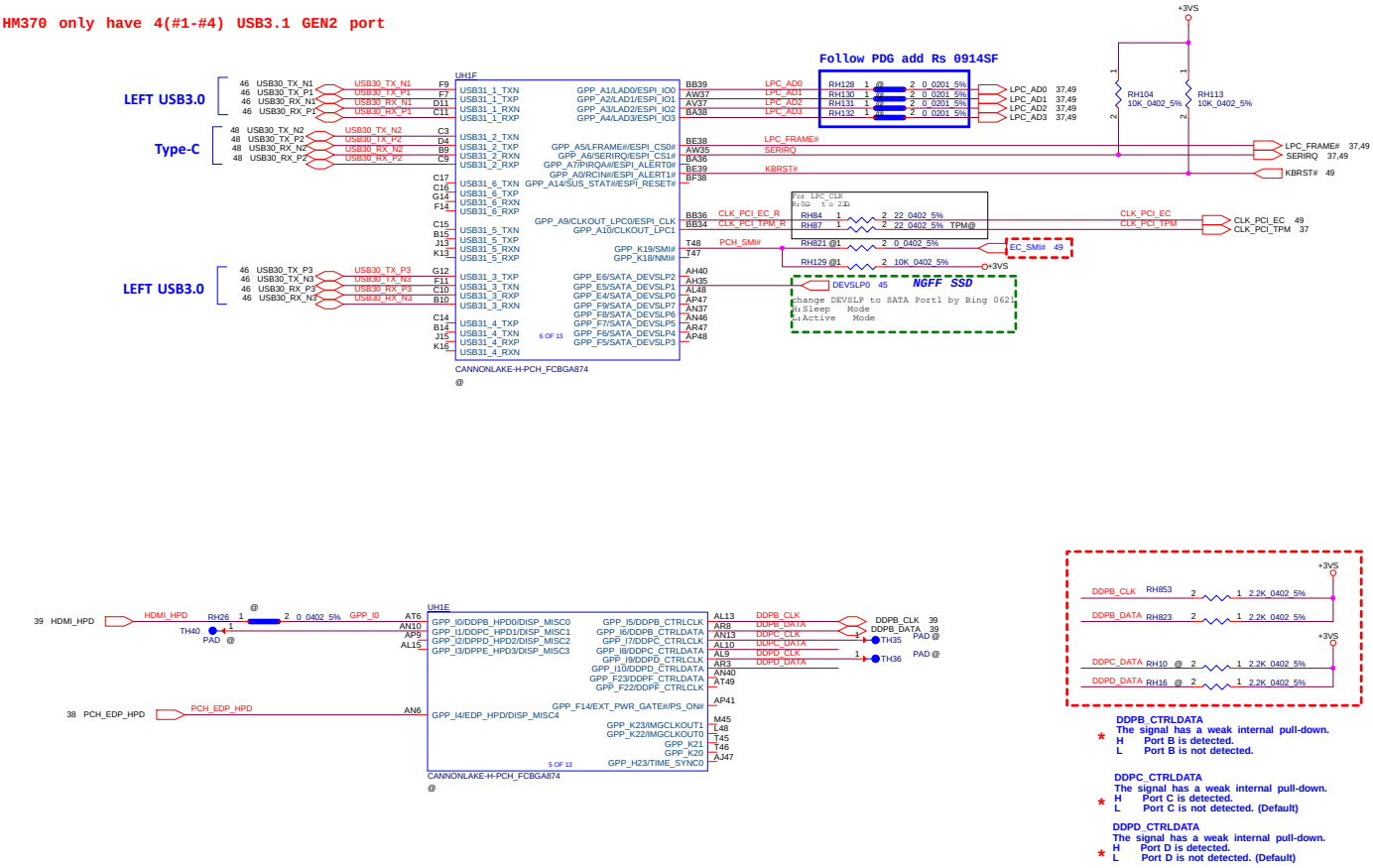
Title	DDR4 SO-DIMM		
Size	Document Number		Rev
Custom	EG530		1.0
Date:	Thursday, March 29, 2018	Sheet	13 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (1/9) PCIe/SATA/GPPFG		
Size A3	Document Number EG530		Rev 1.0
Date: Thursday, March 29, 2018	Sheet 14 of 68		

HM370 only have 4(#1-#4) USB3.1 GEN2 port

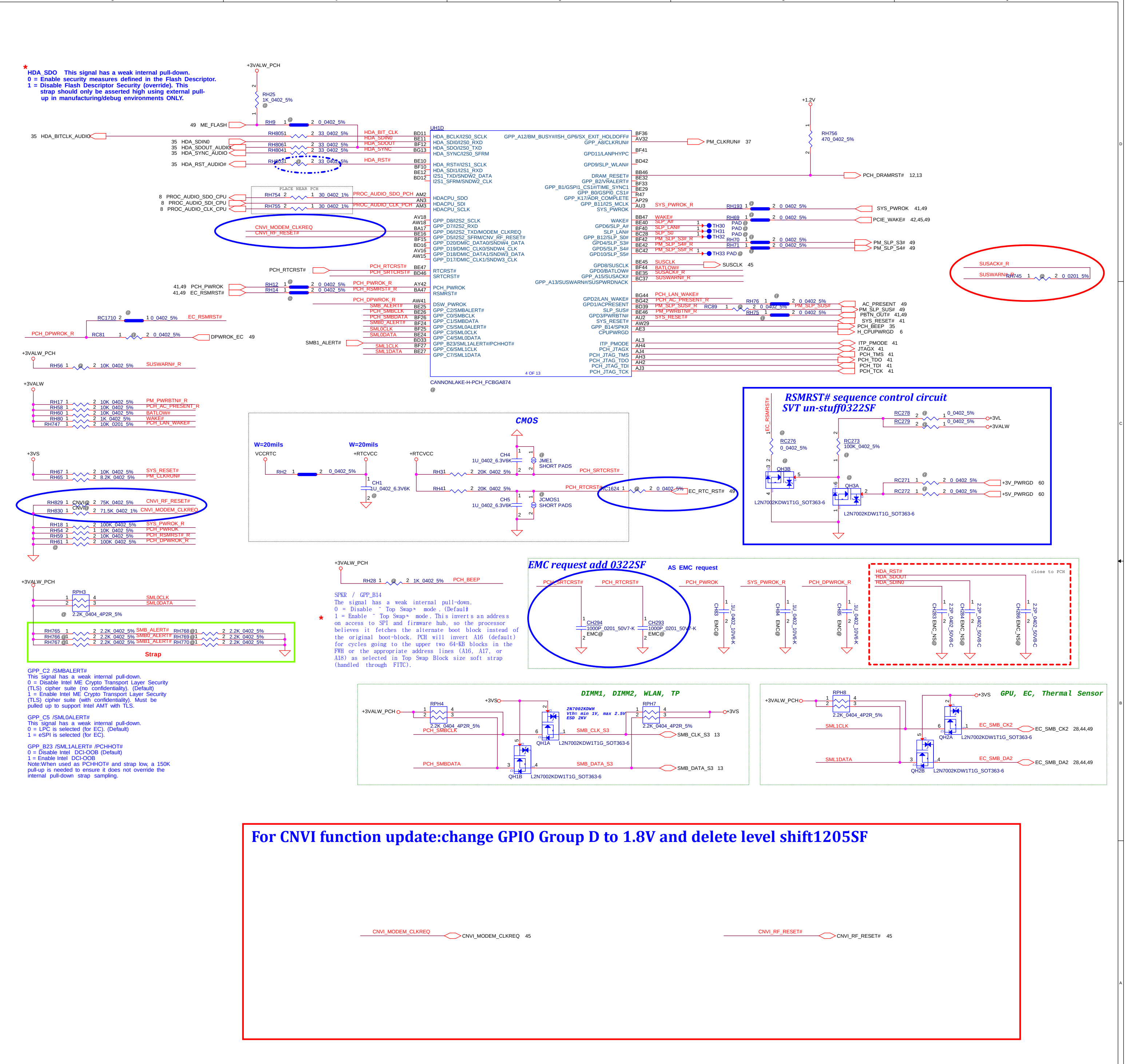


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
A3	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 15 of 68



* HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable " Top Swap" mode. (Default)
* 1 = Enable " Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).

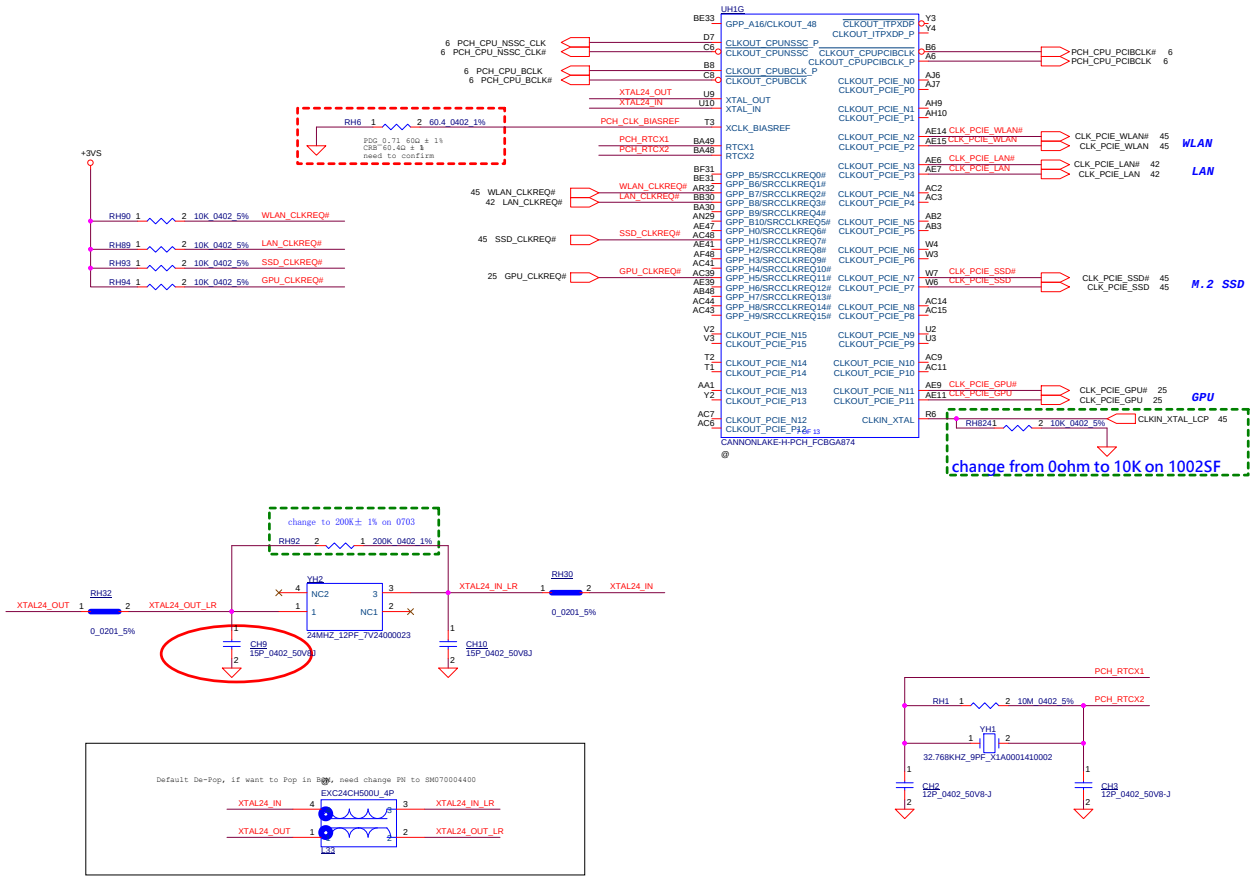
GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

GPP_B23 /SML1ALERT# /PCHHOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

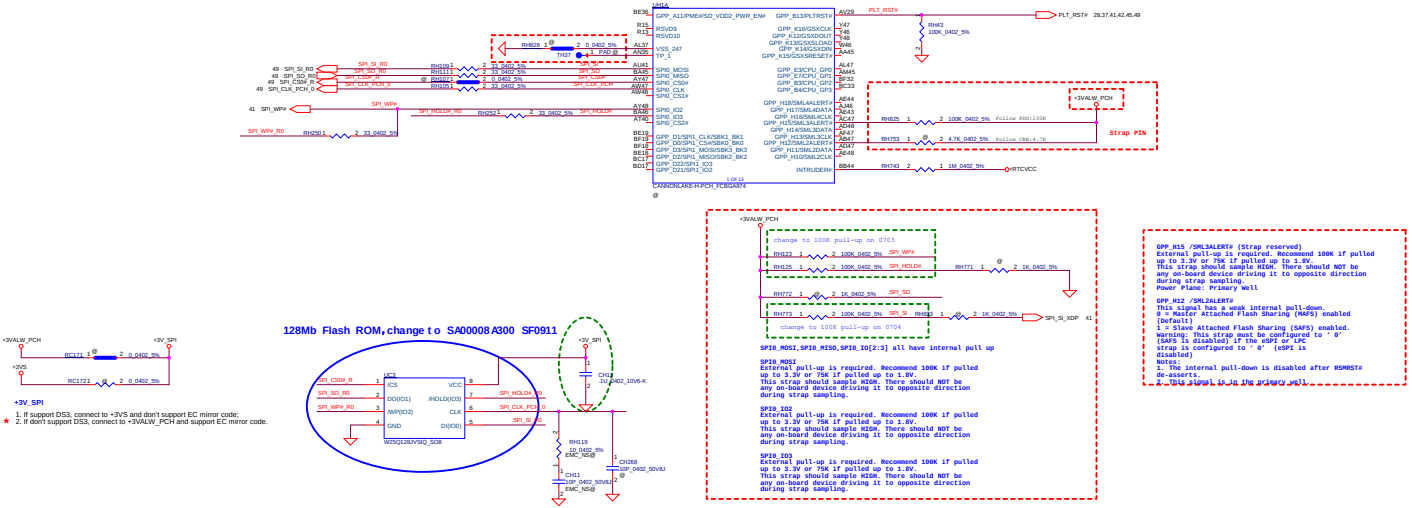
Security Classification	LC Future Center Secret Data	Title
Issued Date: 2015/02/26	Deciphered Date: 2016/02/26	PCH (3/9) HDA,RTC,SMBUS,PM

Size: Custom | Document Number: EG530 | Rev 1.0
Date: Thursday, March 29, 2018 |



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (3/9) CLOCK,GPPBH		
Size A3	Document Number E6530		Rev 1.0
Date: Thursday, March 29, 2018	Sheet 17 of 68		



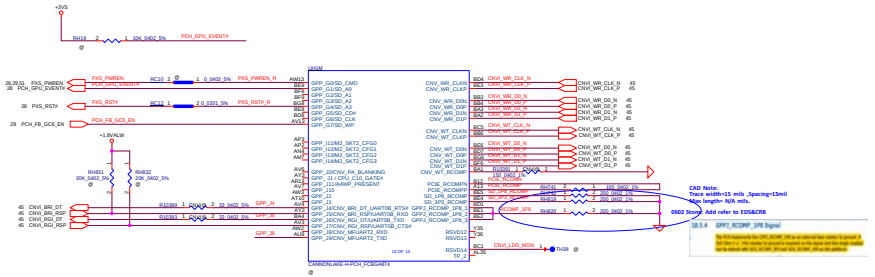
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
A2	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 38 of 68

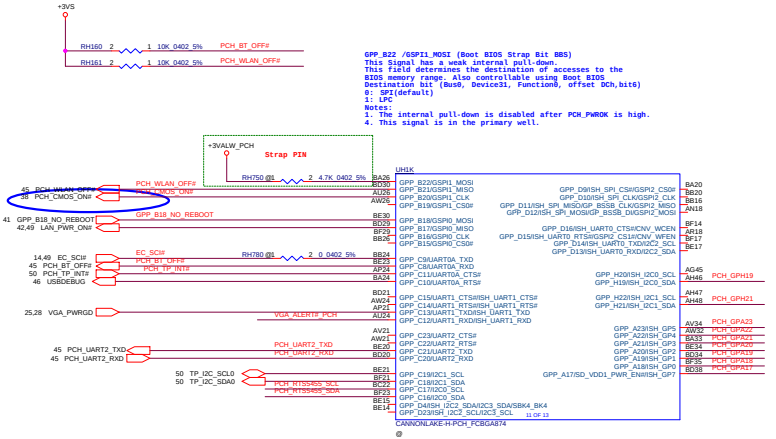


Primary Well Group J (1.8 V Only)

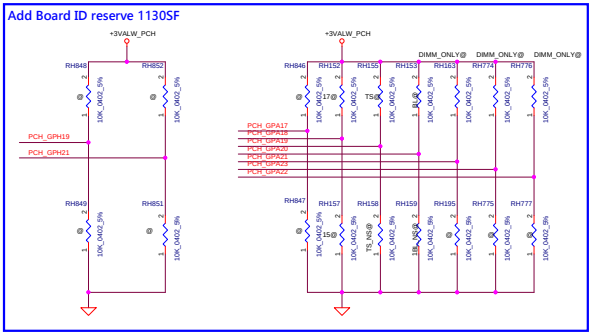
Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	This signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail ***Note:*** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

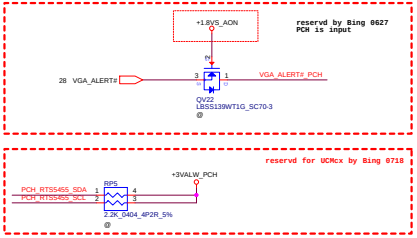
Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/26	Deciphered Date	2015/02/26	Blank

Size	Document Number	Rev
Custom	EG530	1.0
Date:	Thursday, March 26, 2015	Sheet 19 of 68



Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





SKU ID

Board ID	Description	Stuff R
PCH_GPA18	0 15" EG530	RH157
	1 17" EG730	RH152
PCH_GPA19	0 non-touch	RH158
	1 touch	RH155
PCH_GPA20	0 non-KB BL	RH159
	1 KB BL	RH153
PCH_GPA17	0 Reserved	RH847
	1 Reserved	RH846
PCH_GPH19	0 Reserved	RH849
	1 Reserved	RH848
PCH_GPH21	0 Reserved	RH851
	1 Reserved	RH852

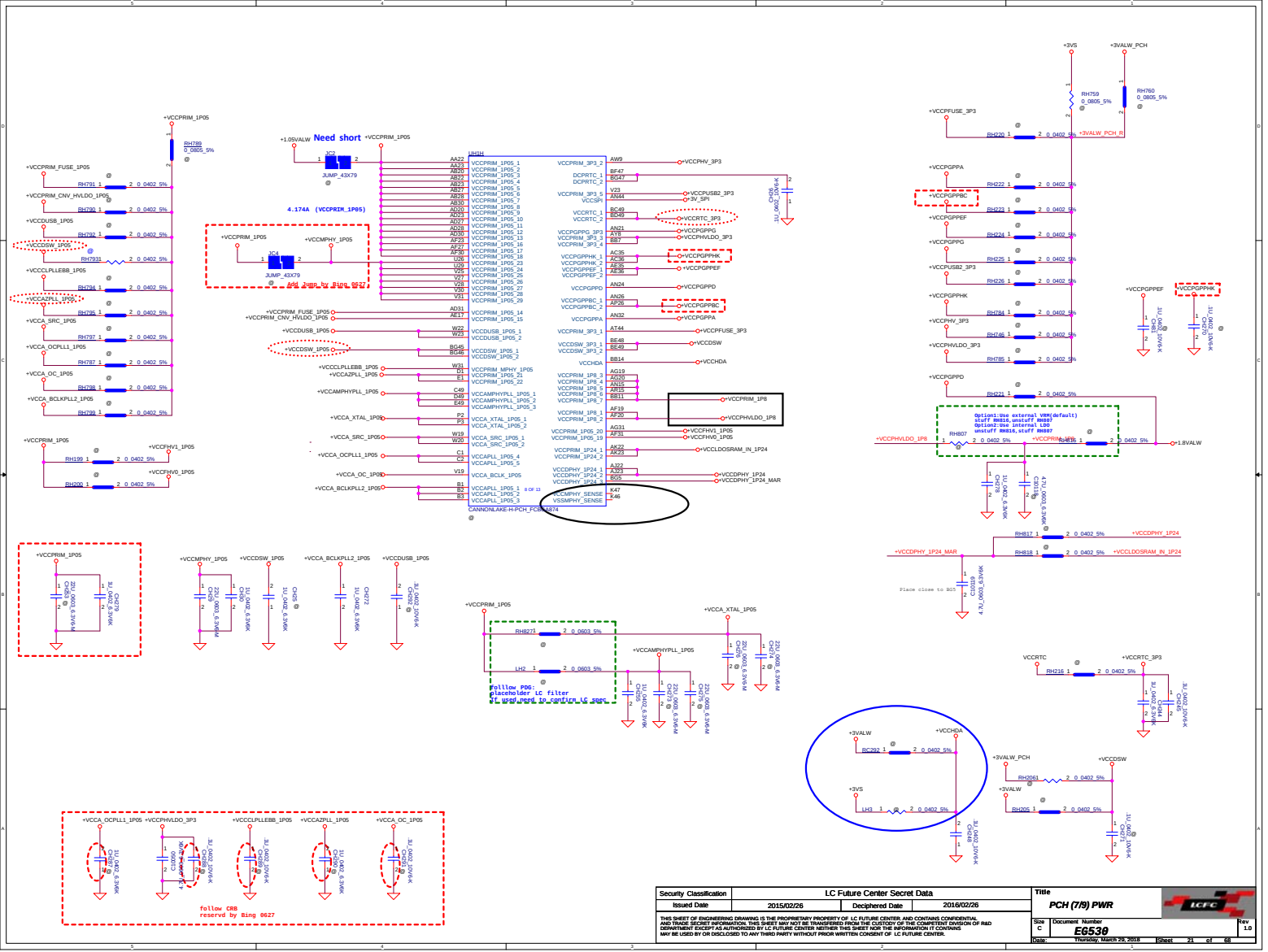
DRAM	Memory Down(DDR4)		DRAMCFG	PCH_GPA23	PCH_GPA22	PCH_GPA21
	Samsung 8Gb 2666 MT/s		0(0x000)	L/RH775	L/RH777	L/RH195
8Gb	Hynix 8Gb 2666 MT/s		1(0x001)	L/RH775	L/RH777	H/RH163
	Micron 8Gb 2666 MT/s		2(0x010)	L/RH775	H/RH776	L/RH195
	Samsung 4Gb 2400 MT/s		3(0x011)	L/RH775	H/RH776	H/RH163
8Gb	Hynix 4Gb 2400 MT/s		4(0x100)	H/RH774	L/RH777	L/RH195
	Micron 4Gb 2400 MT/s		5(0x101)	H/RH774	L/RH777	H/RH163
	X		6(0x110)	H/RH774	H/RH776	L/RH195
	SO-DIMM		7(0x111)	H/RH774	H/RH776	H/RH163

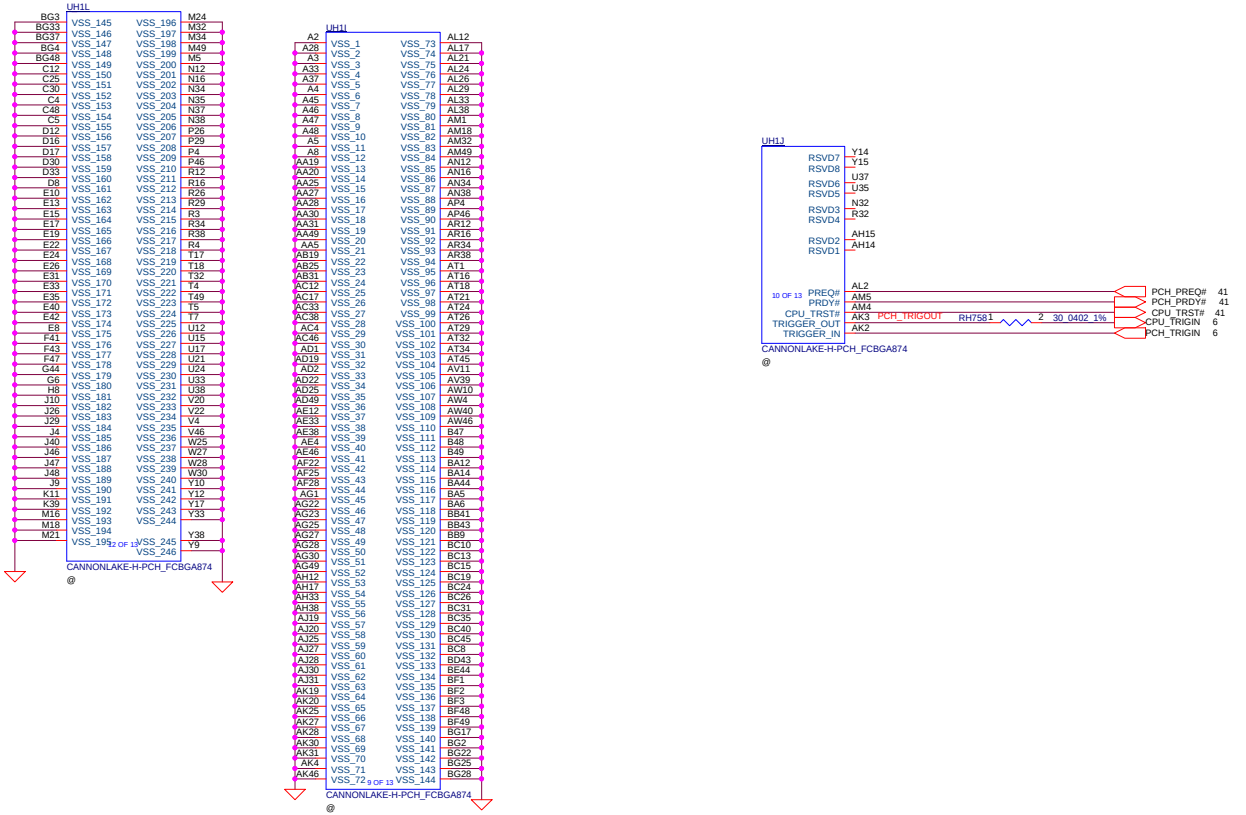
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (6/9) GPPPABCD, I2C

Size: C | Document Number: E6530 | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 20 of 68


Need short
4.174A (VCCPRIM_1P05)
Add Jump by Bing 0627
Option1:Use external VRM(default)
stuff RH816,unstuff RH807
Option2:Use internal LDO
unstuff RH816,stuff RH807
Follow PDG:
placeholder LC filter
rf wpad need to confirm LC spec
follow CRB
reserved by Bing 0627
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
PCH (7/9) PWR
Size
C
Document Number
E6530
Rev
1.0
Date:
Thursday, March 29, 2018
Sheet
21
of
68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (9/9) VSS

Size	Document Number	Rev
B	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 22 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

Cover Page

Size	Document Number	Rev
C	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 23 of 68

N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

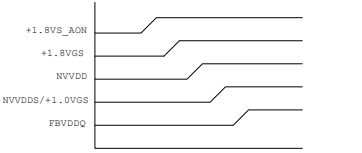
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

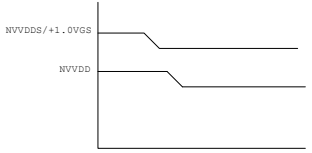


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

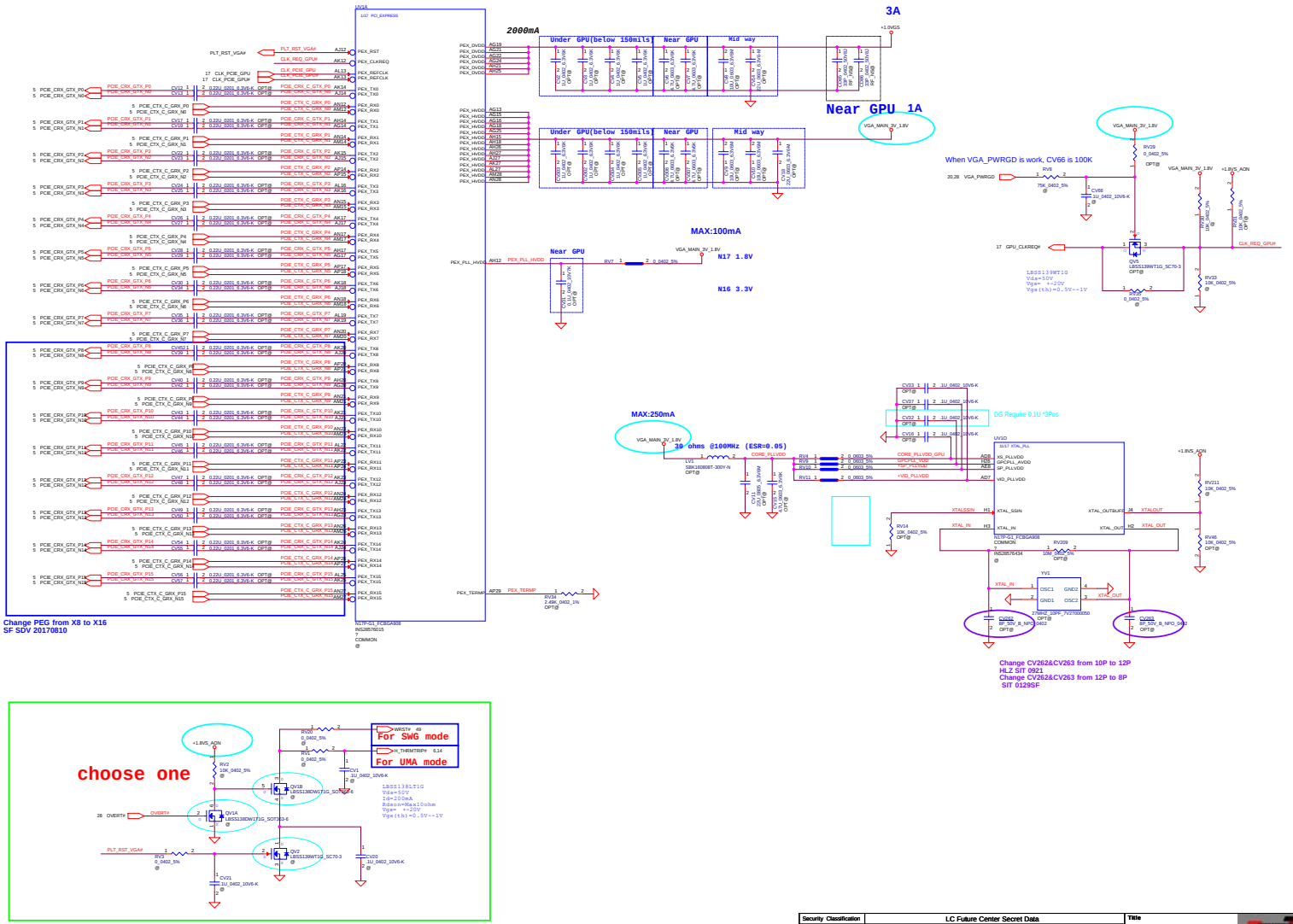
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: VGA Notes List

Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 24 of 68



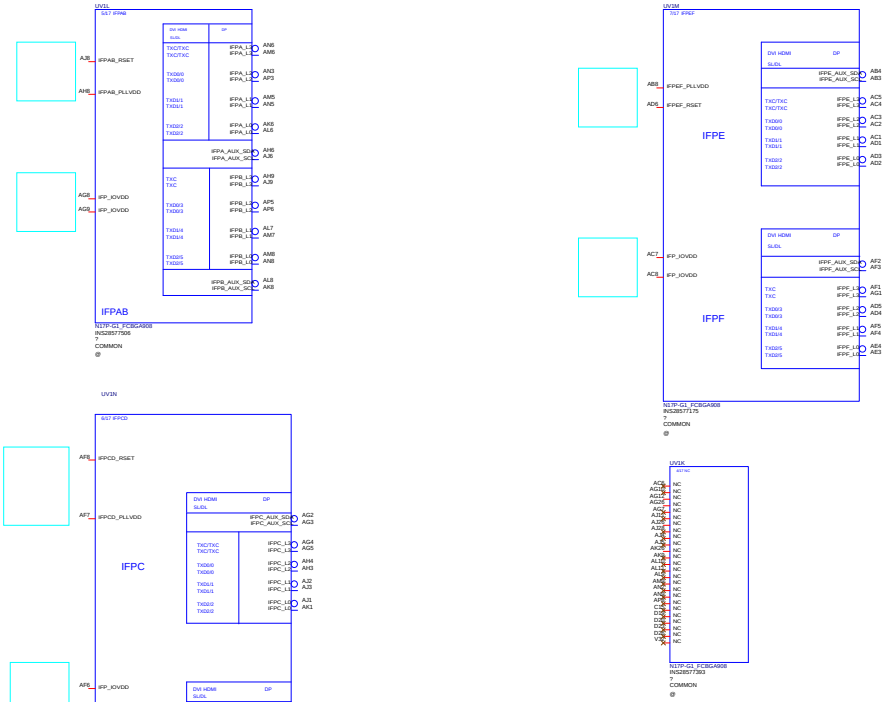
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: N17P_(1/6):PEG I/F

Size: Custom | Document Number: E6530 | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 25 of 68



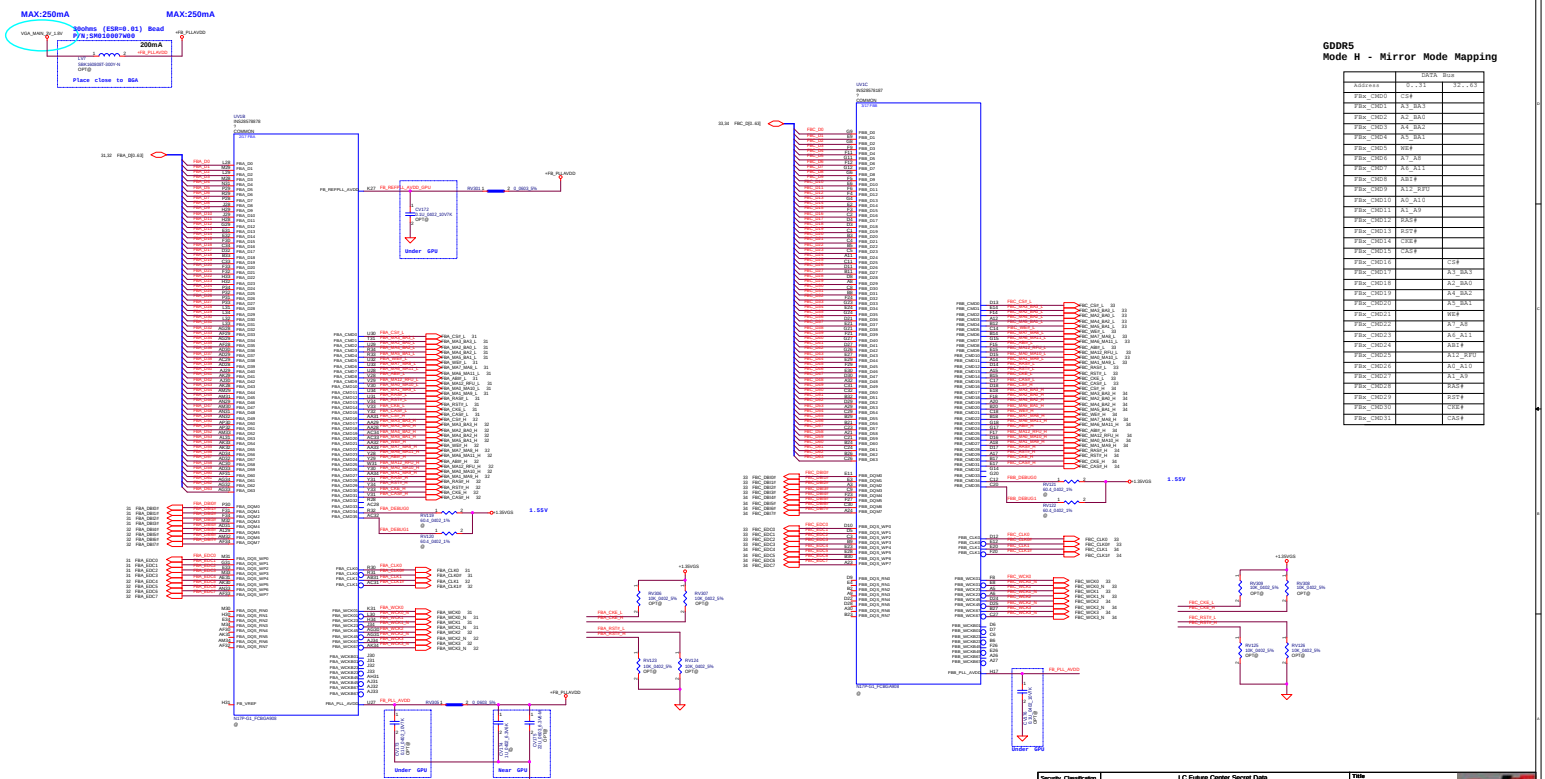
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

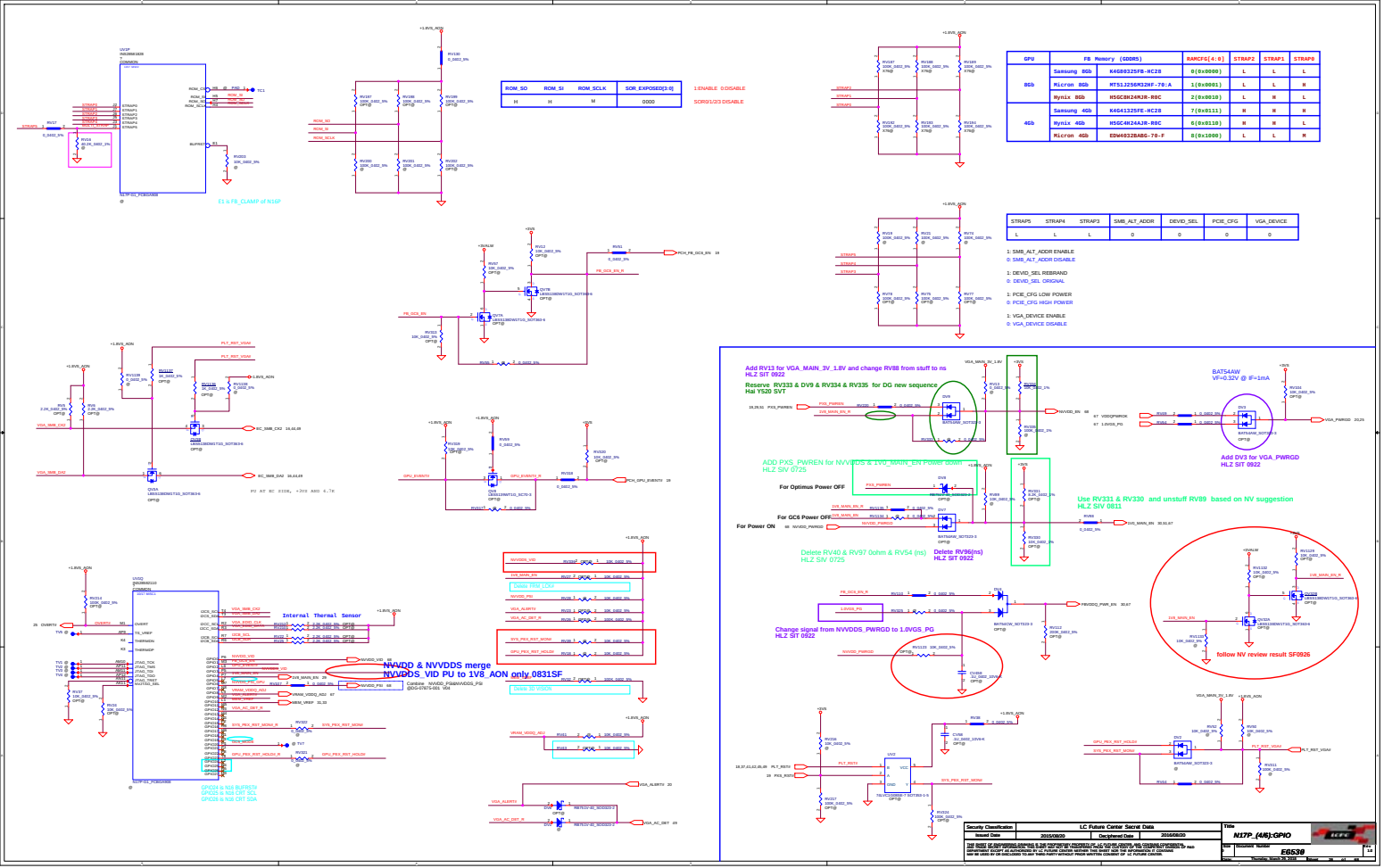
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: N17P_(2/6):DIGITAL OUT

Size	Document Number	Rev
Custom	E6539	1.0

Date: Thursday, March 26, 2015 Sheet 26 of 68


MAX:250mA
MAX:250mA
30ohms (ESR=0.01) Bead
P/N:SM010007W00
200mA
+FB_PLLAVDD
Place close to BGA
GDDR5
Mode H - Mirror Mode Mapping
DATA Bus
Address
0..31
32..63
FBx_CMD0
C4#
FBx_CMD1
A3_BA3
FBx_CMD2
A2_BA2
FBx_CMD3
A4_BA2
FBx_CMD4
A5_BA1
FBx_CMD5
WE#
FBx_CMD6
A7_A8
FBx_CMD7
A6_A11
FBx_CMD8
ABI#
FBx_CMD9
A12_EPU
FBx_CMD10
A0_A10
FBx_CMD11
A1_A9
FBx_CMD12
RAS#
FBx_CMD13
RST#
FBx_CMD14
CKE#
FBx_CMD15
CAS#
FBx_CMD16
CS#
FBx_CMD17
A7_BA3
FBx_CMD18
A2_BA0
FBx_CMD19
A4_BA2
FBx_CMD20
A5_BA1
FBx_CMD21
WE#
FBx_CMD22
A7_A8
FBx_CMD23
A6_A11
FBx_CMD24
ABI#
FBx_CMD25
A12_EPU
FBx_CMD26
A0_A10
FBx_CMD27
A1_A9
FBx_CMD28
RAS#
FBx_CMD29
RST#
FBx_CMD30
CKE#
FBx_CMD31
CAS#
Under GPU
Near GPU
1.55V
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
Title
N17P_(3/6):VRAM I/F
Size
Document Number
Rev
A0
E6530
1.0
Date: Thursday, March 24, 2016
Sheet 6 of 18


ROM_SO
ROM_SI
ROM_SCLK
SOR_EXPOSED[3:0]
H H M 0000
1:ENABLE 0:DISABLE
SOR0/1/2/3 DISABLE
E1 is FB_CLAMP of N16P
GPU
FB Memory (GDDR5)
RAMCFG[4:0]
STRAP2
STRAP1
STRAP0
8Gb
Samsung 8Gb K4G80325FB-HC28 0(0x0000) L L L
Micron 8Gb MT51J256M32HF-70:A 1(0x0001) L L H
Hynix 8Gb H5GC8H24MJR-R0C 2(0x0010) L H L
4Gb
Samsung 4Gb K4G41325FE-HC28 7(0x0111) H H H
Hynix 4Gb H5GC4H24AJR-R0C 6(0x0110) H H L
Micron 4Gb EDW4032BABG-70-F 8(0x1000) L L M
STRAP5 STRAP4 STRAP3 SMB_ALT_ADDR DEVED_SEL PCIE_CFG VGA_DEVICE
L L L 0 0 0 0
1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL
1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE
Add RV13 for VGA_MAIN_3V_1.8V and change RV88 from stuff to ns
HLZ SIT 0922
Reserve RV333 & DV9 & RV334 & RV335 for DG new sequence
Hai YS20 SVT
ADD PXS_PWREN for NVVDDS & 1VO_MAIN_EN Power down
HLZ SIV 0725
For Optimus Power OFF
For GC6 Power OFF
For Power ON
Delete RV40 & RV97 0ohm & RV54 (ns)
HLZ SIV 0725
Delete RV96(ns)
HLZ SIT 0922
BAT54AW
VF=0.32V @ IF=1mA
Add DV3 for VGA_PWRGD
HLZ SIT 0922
Use RV331 & RV330 and unstuff RV89 based on NV suggestion
HLZ SIV 0811
Change signal from NVVDDS_PWRGD to 1.0VGS_PG
HLZ SIT 0922
follow NV review result SF0926
Internal Thermal Sensor
NVVDD & NVVDDS merge
NVVDDS_VID PU to 1V8_AON only 0831SF
Combine NVVDD_PSAVENVDDS_PSI @DG-07NT1-GE3_V04
Delete 3D VSOP
GPIO24 is NV3 BUFRST#
GPIO25 is N16 CRT SCL
GPIO26 is N18 CRT SDA
Security Classification: LC Future Center Secret Data
Issued Date: 2015/08/20
Deciphered Date: 2016/08/20
Title: N17P_(4/6):GPIO
Size: C
Document Number: E6539
Rev: 1A
Date: Thursday, March 24, 2016
Sheet 38 of 48

5A Peak 8A

Under GPU(below 150mils)

Cost down list:
1U 3Pcs

Near GPU

1.8V Total 1A (AON+MAIN)

0.5A

Under GPU

Near GPU

0.5A

Under GPU

Near GPU

NVVDD & NVVDDS merge test point only 0831SF

trace width: 16mils
differential voltage sensing.
differential signal routing.

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

19A Peak 42A

Cost down list:
4.7U 1Pcs
1U 1Pcs

POSCAP

Near GPU

Under GPU

Follow NV suggestion for NVVDDS Hai Y520 SVT

2A

Delete +3.3V_AON

Change QV18 from LBSS138LT1G_SOT-23-3 to LBSS139WT1G_SC70-3 Hai Y520 SVT

V20B+

Vg=16.4V@AC
Vg=7.38V@Battery

AON7408L
Vds=30V
Ids=15A
Rdson=28mohm@Vgs=4.66V
=20mohm@Vgs=6V
=18mohm@Vgs>10V
Vgs=+-20V
Vgsth=1~3V

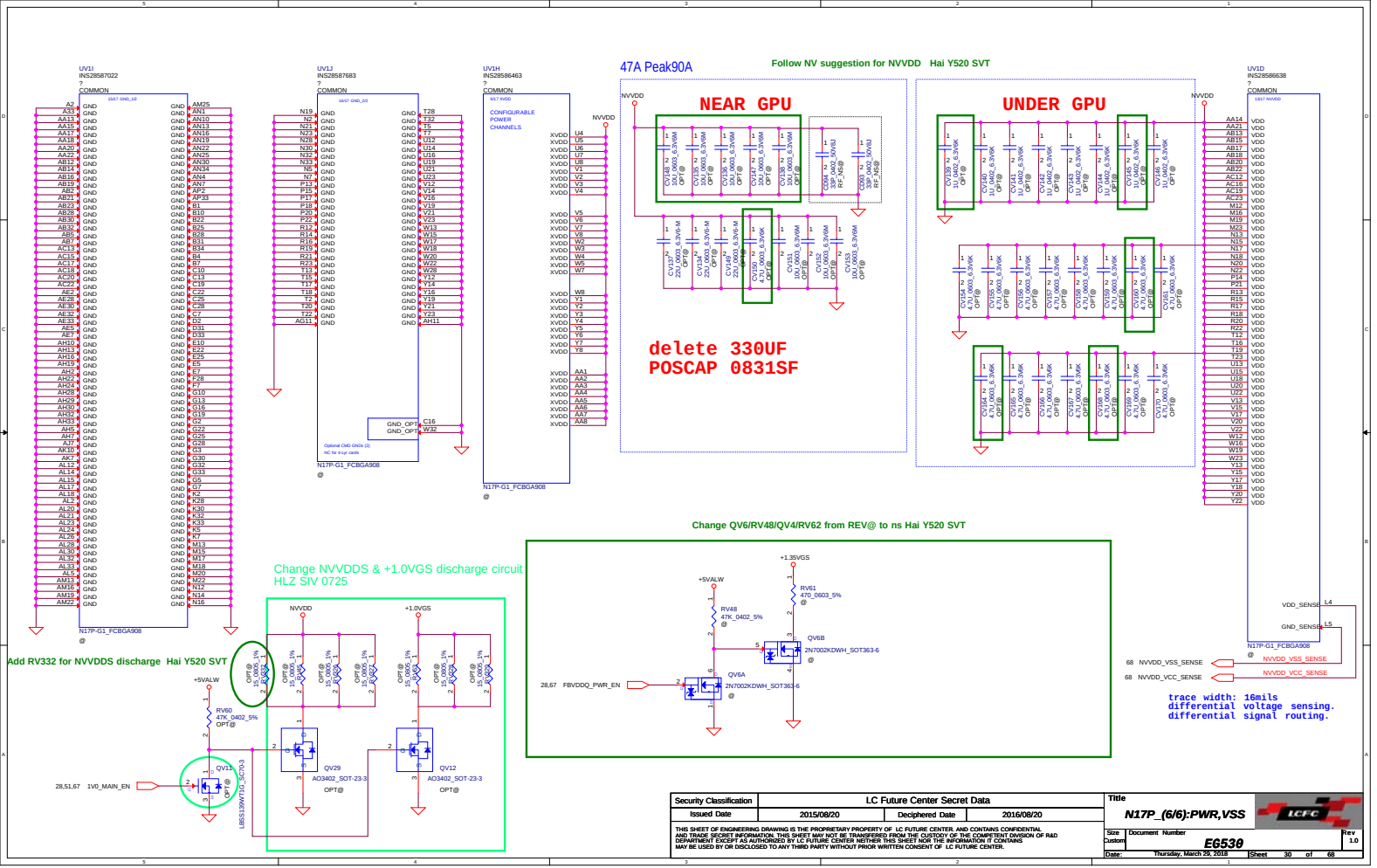
Add +1.8V_MAIN discharger circuit
HLZ SIT 0928

Delete PD3503 and Reserve PD3/PR4/PR5/CV38
HLZ SIT 0923

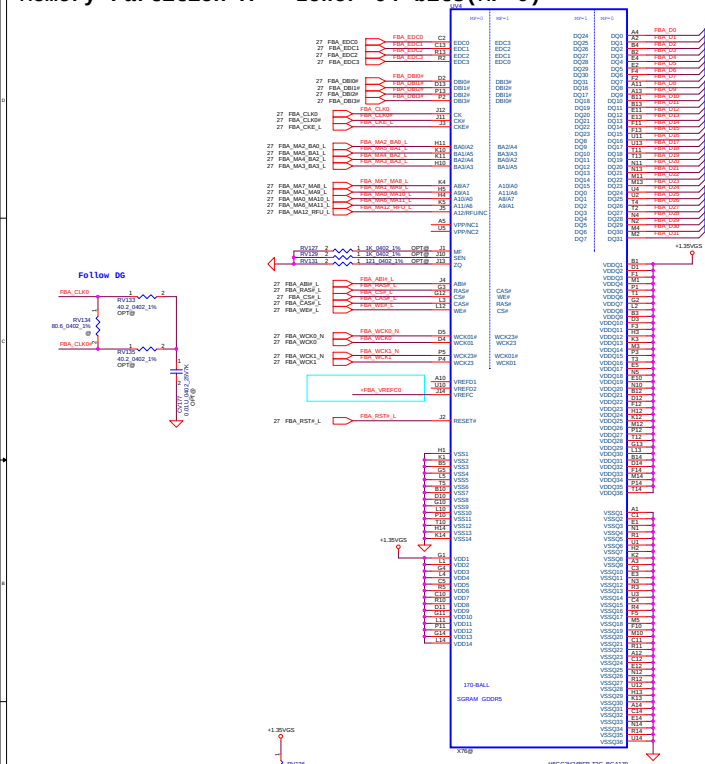
Add +1.8V-AON discharger circuit HLZ SIV 0811

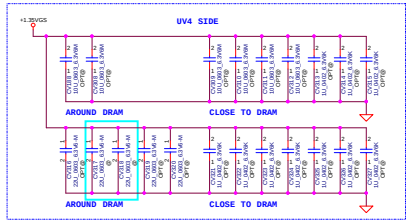
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

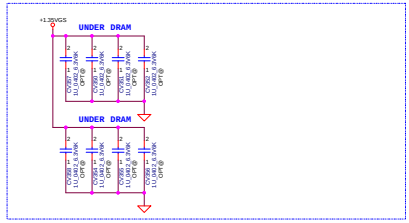
Title	N17P_(5/6):PWR
Size	Custom
Document Number	E6530
Rev	1.0
Date:	Thursday, March 29, 2018
Sheet	29 of 68


47A Peak90A
Follow NV suggestion for NVVDD Hai Y520 SVT
NEAR GPU
UNDER GPU
delete 330UF
POSCAP 0831SF
Change QV6/RV48/QV4/RV62 from REV@ to ns Hai Y520 SVT
Change NVVDDS & +1.0VGS discharge circuit
HLZ SIV 0725
Add RV332 for NVVDDS discharge Hai Y520 SVT
trace width: 16mils
differential voltage sensing.
differential signal routing.
N17P_(6/6):PWR,VSS
EG530

Memory Partition A - Lower 64 bits(MF=0)







GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

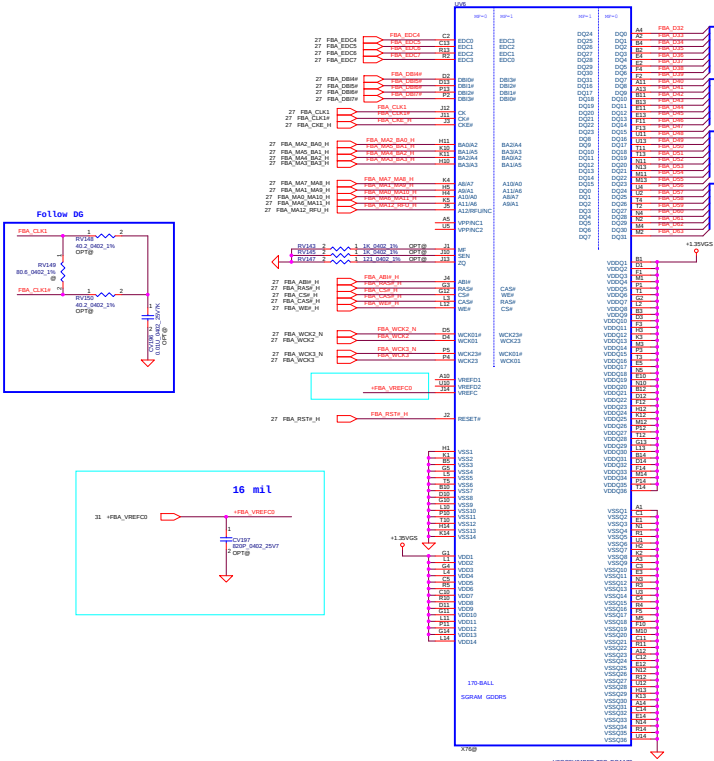
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

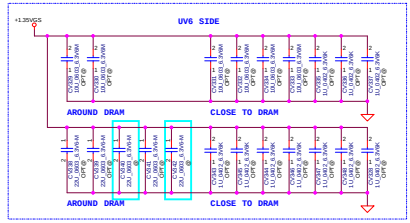
Title: N17P_GDDR5_A Lower

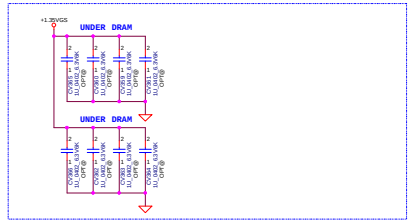
Size: Custom | Document Number: E6530 | Rev: 1.0

Date: Thursday, March 30, 2016 | Sheet 34 of 68

Memory Partition A- Upper 64 bits(MF=0)







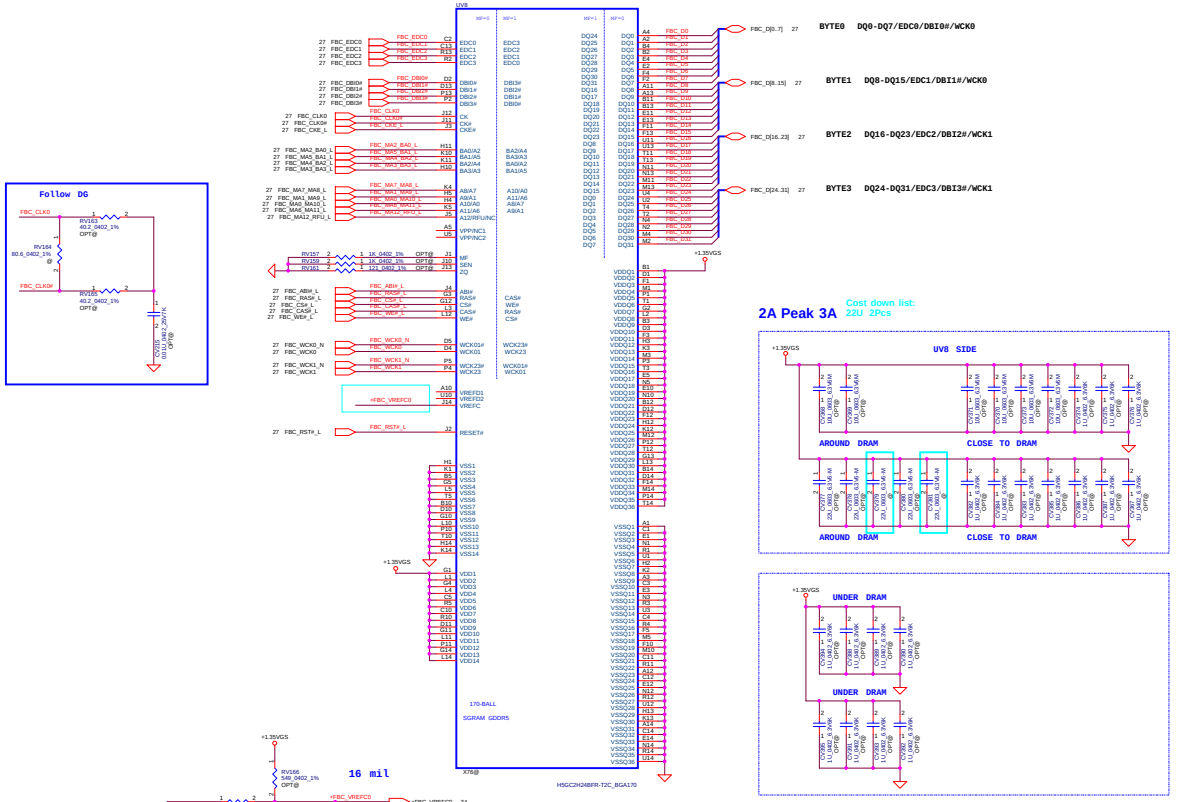
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	RE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		RE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	N17P_GDDR5_A Upper		
Size	Document Number		Rev
Custom	E6530		1.0
Date:	Thursday, March 30, 2016	Sheet	32 of 68

Memory Partition B - Lower 32 bits(MF=0)

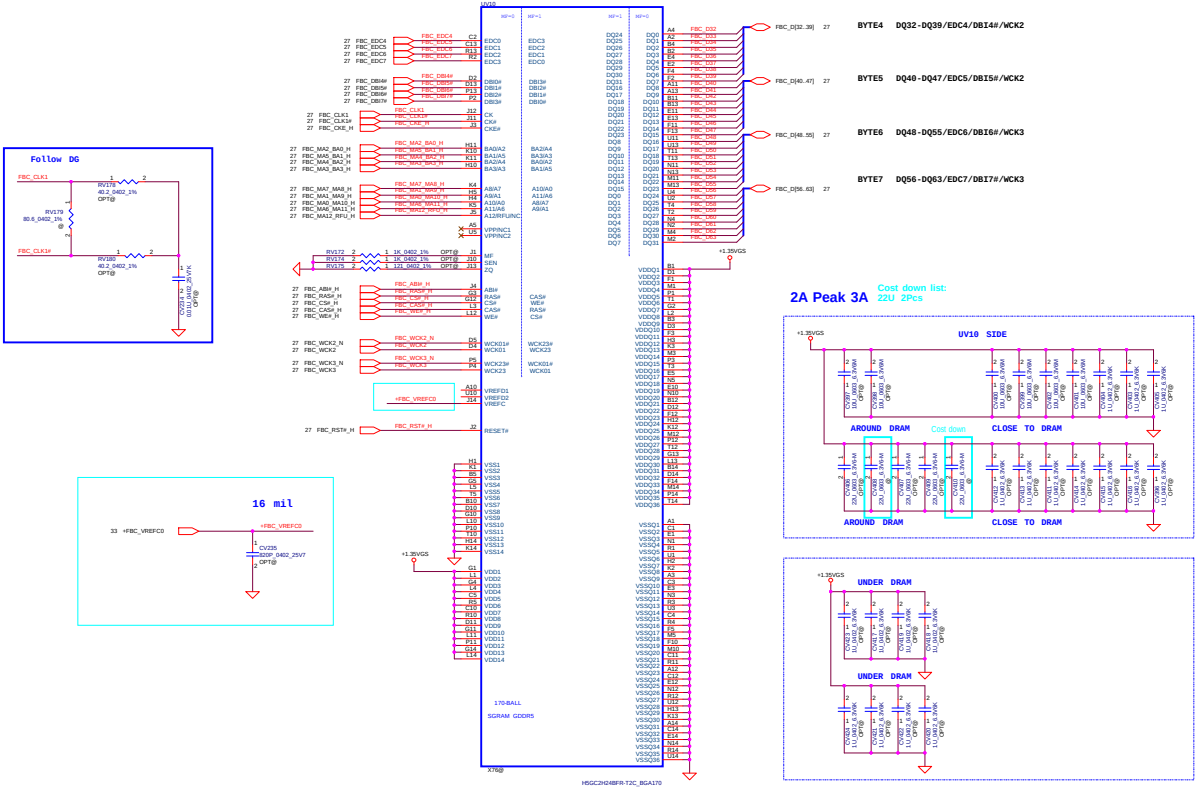


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title		
N17P_GDDR5_B Lower		
Size: Custom	Document Number: E6530	Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 33 of 68	

Memory Partition B - Upper 32 bits(MF=0)



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: N17P_GDDR5_B Upper

Size: Custom | Document Number: E6530 | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 34 of 68

Digital power for HDA link

Close to Pin1

8/29 Add +1.8VS Circuit for Audio wei

Analog power for mixers, & IO ports

Power supply for full-bridge left/Right channel

Power for card reader controller

Power for combo jack depop circuit at system shutdown mode

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

Analog power for DACs, ADCs

Digital power for digital I/O circuit

11/8 SIT Vendor suggestion form 47 ohm change to 51om wei

11/8 SIT Cost down to 0ohm wei

8/16 Update Audio Jack P/N SP011509163 wei

FOR EMI

Audio Jack

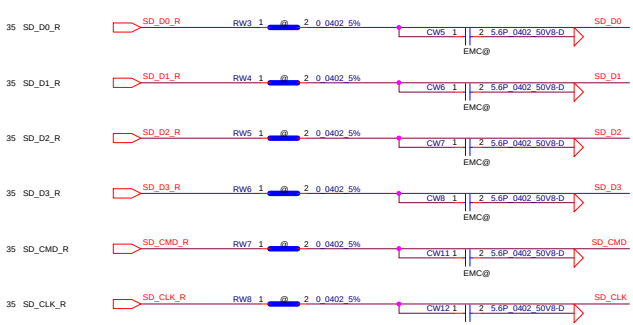
8/16 Update Audio Jack P/N DC021608101 wei

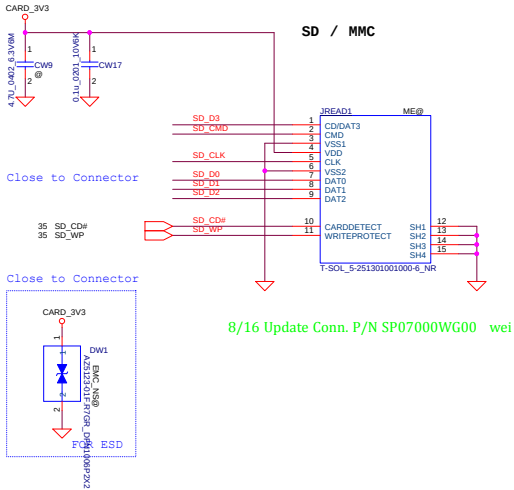
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Codec & CR_RTS5199

Size: C | Document Number: E6530 | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 35 of 68



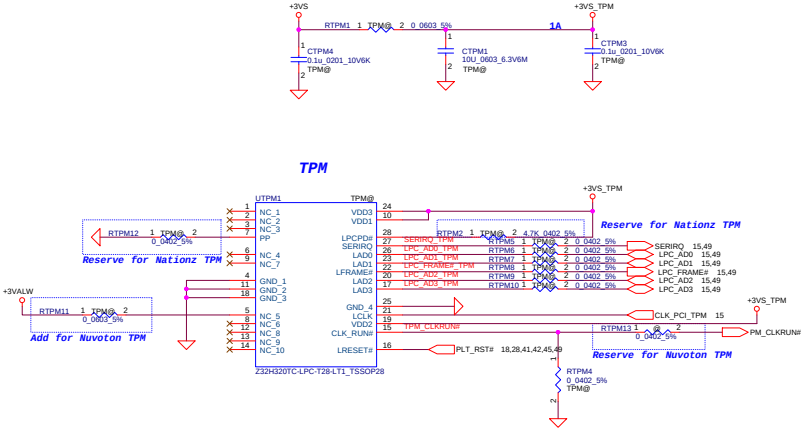


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cardreader**

Size	Document Number	Rev
Custom	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 36 of 68

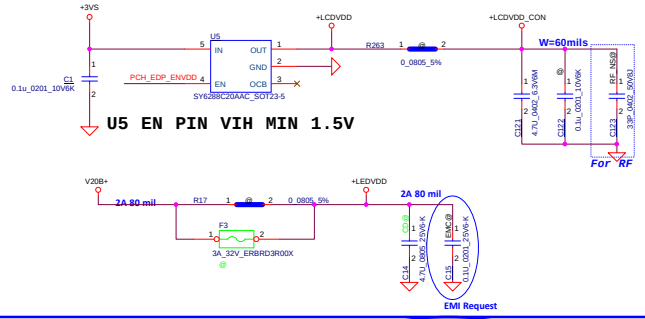


	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

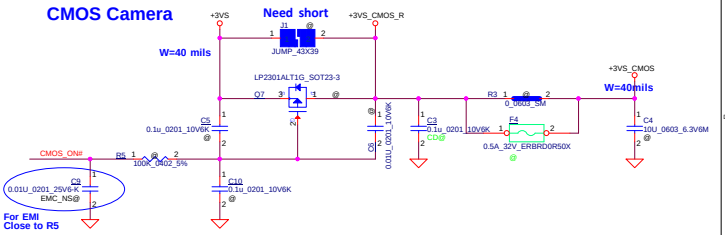
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

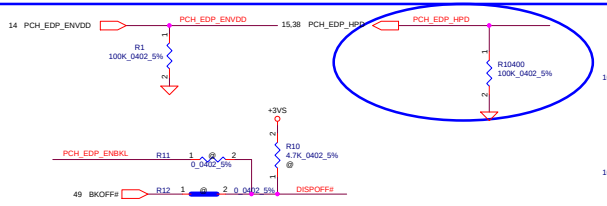
Title	TPM		
Size	Document Number		Rev
Custom	EG530		1.0
Date:	Thursday, March 29, 2018	Sheet	37 of 68

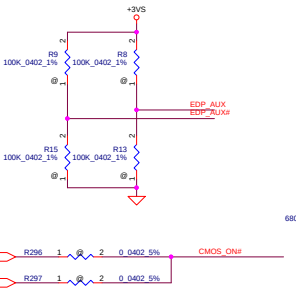
LCD POWER CIRCUIT

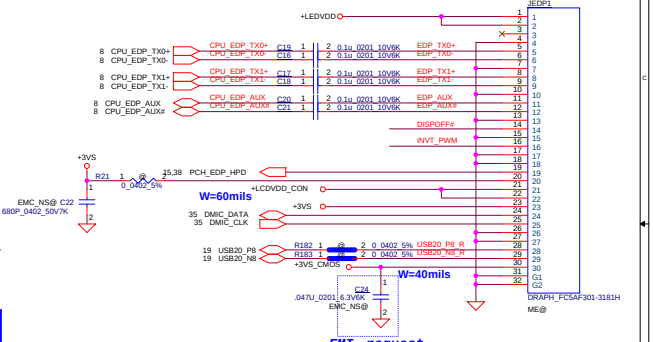


CMOS Camera

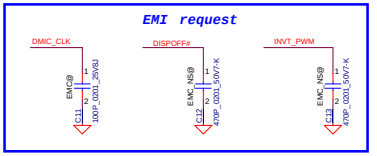




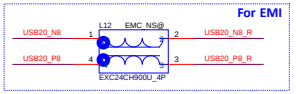




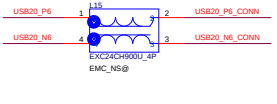
EMI request



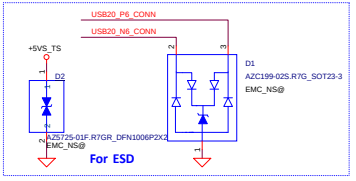
EMI request

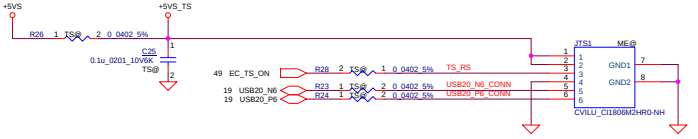


Touch Screen



Touch Screen

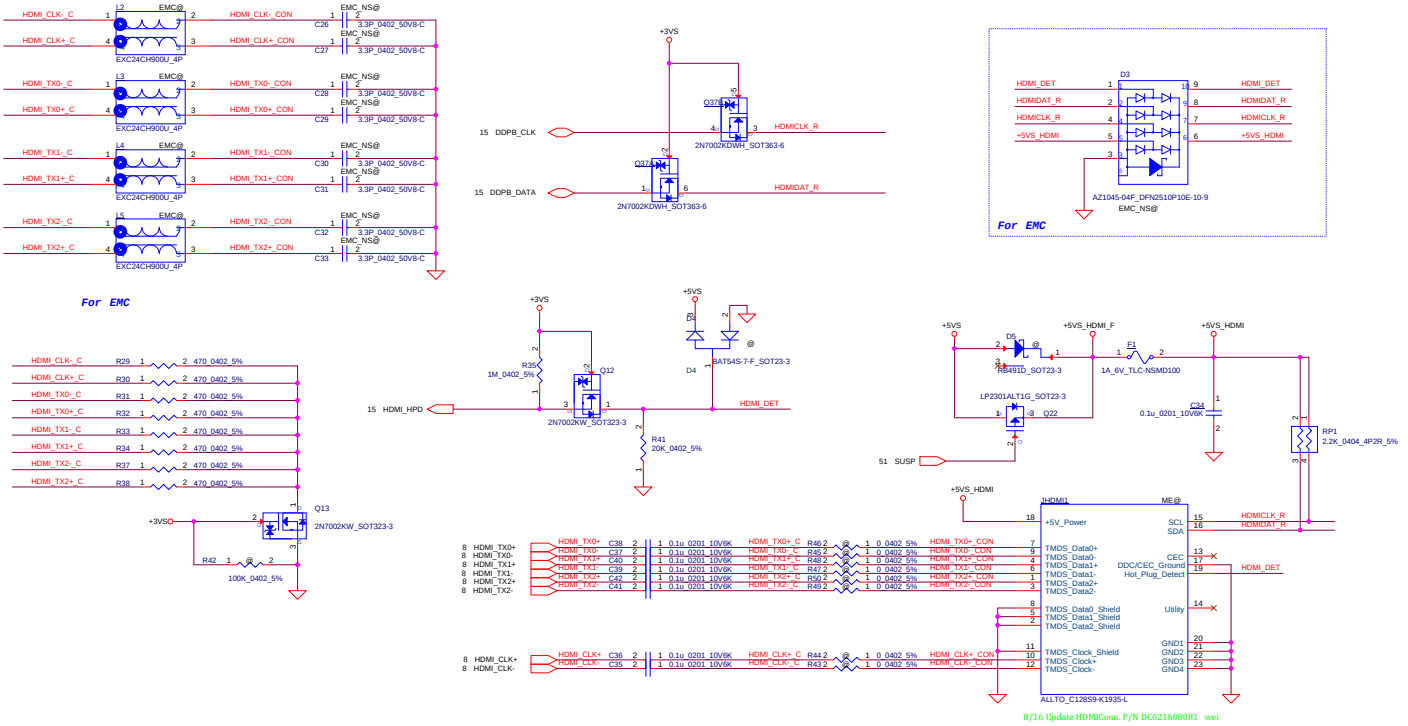




Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: eDP/CMOS/Touch screen

Size	Document Number	Rev
Custom	E6530	1.0
Date: Thursday, March 29, 2018	Sheet 38 of 68	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title			
HDMI_CONN			
Size: Custom	Document Number: EG530		Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 39 of 68		

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

P35-Blank

Size	Document Number	Rev
Custom	***EG530***	1.0

Date: Thursday, March 29, 2018 Sheet 40 of 68

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

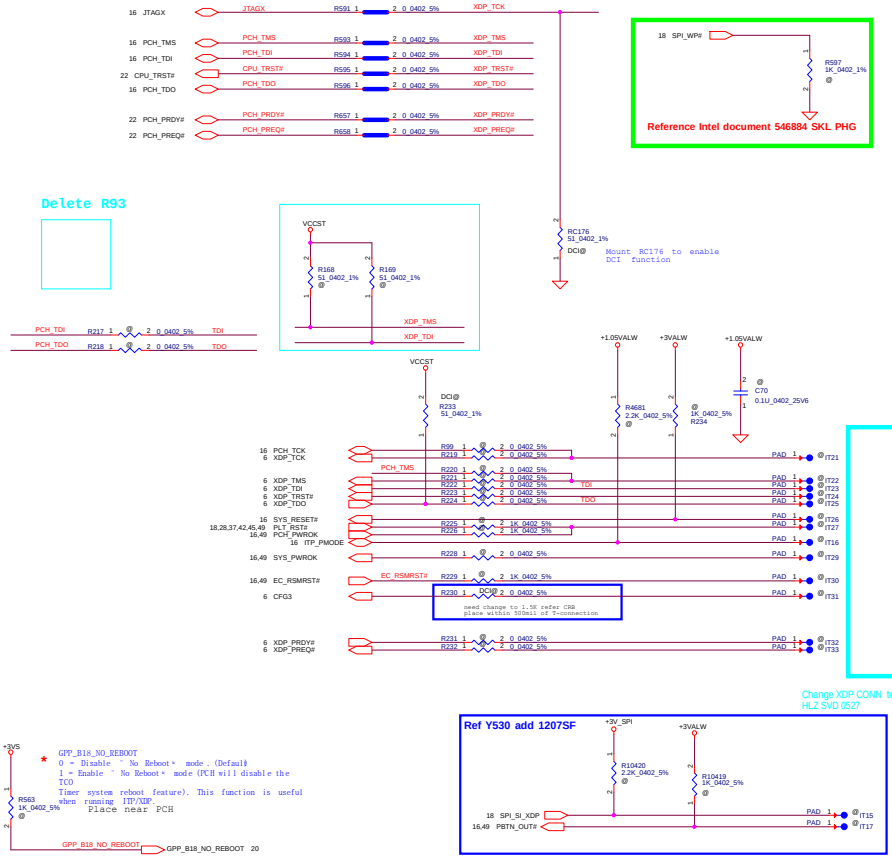
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

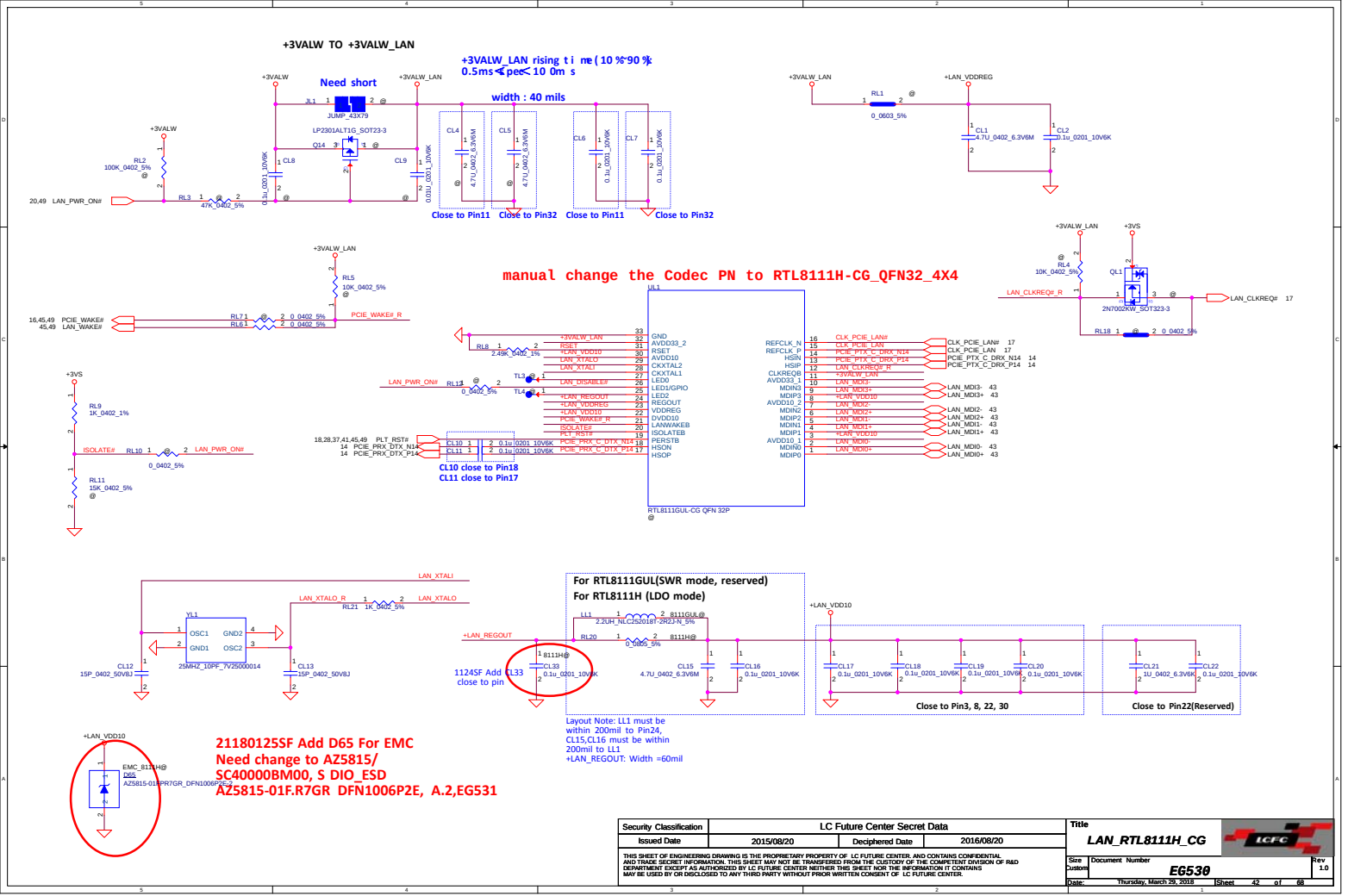


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Blank

Size	Document Number	Rev
-	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 41 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

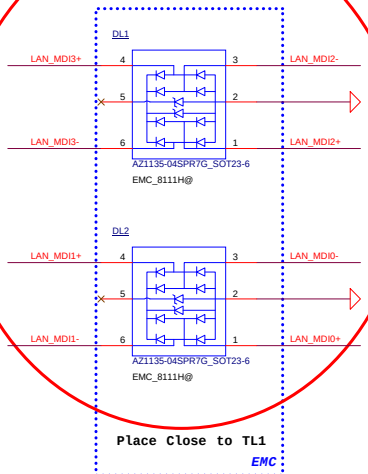
Title: LAN_RTL8111H_CG

Size: Custom | Document Number: EG530 | Rev: 1.0

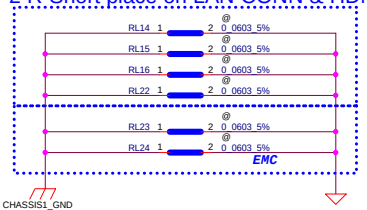
Date: Thursday, March 29, 2018 | Sheet 42 of 68

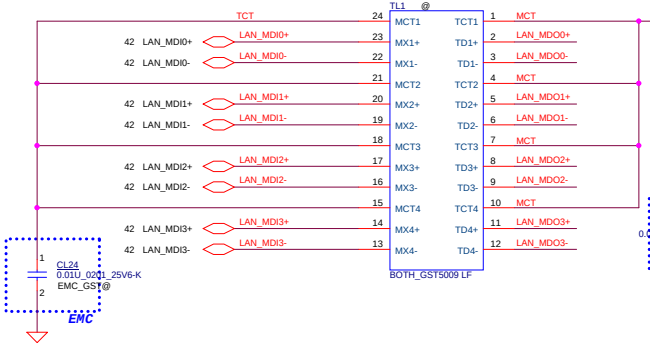
0907SF change DL1/DL2 to
S DIO(BR) AZ1215-04S.R7G SOT23-6L
PN:SC300005900 for 8111H

20180125SF:For EMC debug DL1 & DL2
Need change to SC300006100,
S DIO(BR) AZ1135-04S.R7G SOT23, A.1,EG531

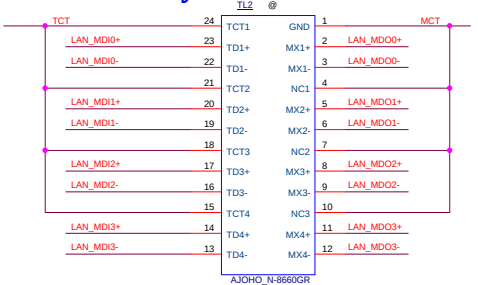


1204SF update,
4 R-Short place on DC-IN CONN & LAN CONN,
2 R-Short place on LAN CONN & HDMI CONN

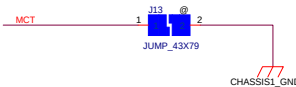


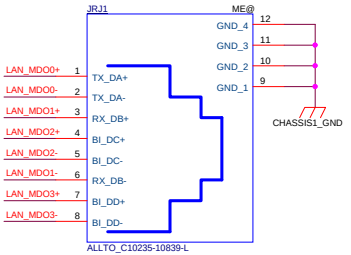


Add TL2 co-lay TL1 1009SF



Need short



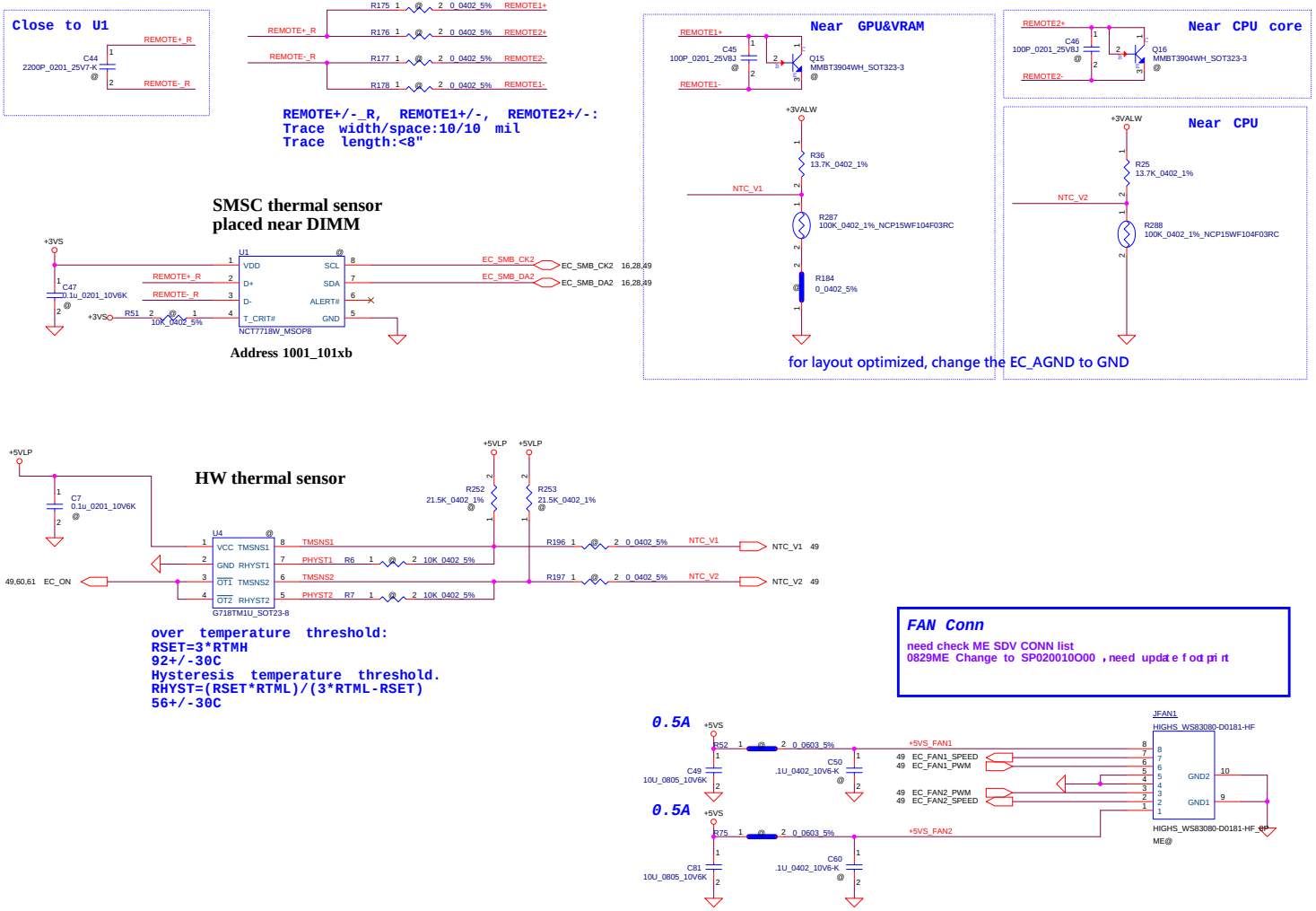


8/16 Update RJ45 P/N DC021608091 wei

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: LAN_Transformer

Size	Document Number	Rev
B	EG530	1.0
Date: Thursday, March 29, 2018	Sheet 43 of 68	



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	Thermal sensor/FAN CONN		
Size: Custom	Document Number: EG530		Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 44 of 68		

Mini-Express Card(WLAN/WiMAX)

SDV Add CNVi Function 0913SF

Need short

Don't short

ref Y530 for wlan data transmission issue 0323SF

change WLAN CLKREQ# PH power source 0329SF

If support AOAC, NC R61;
If not support AOAC, stuff R61.

8/16 Update Conn. P/N SP070013200 wei

M.2 SSD(SATA/PCIE)

2A

Change 0805 to Jump HLZ SDV 0615

NEW HLZ_SDV_0681

Add C827 due to signal waveform abnormal HLZ SV 0811

For option

Ac coupling-Cap place near MGFF CONN within 500mil

PEDET (PE_DTCT)
SATA Device GND
PCIe Device Open

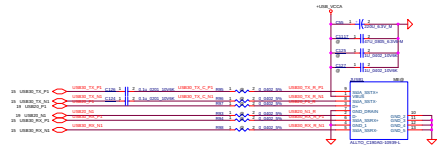
SSD_DET#
0 - SATA
1 - PCIE

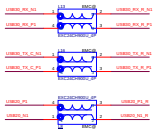
Security Classification	LC Future Center Secret Data		
Issued Date	2016/12/14	Deciphered Date	2017/12/13

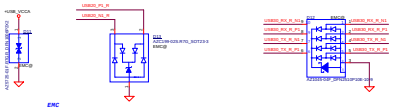
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	MGFF WLAN&SSD		
Size	Document Number		Rev
	E6539		1A
Date: Friday, March 16, 2018	Sheet 49 of 61		

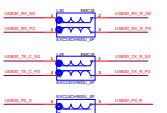
LEFT SIDE USB3.0 PORT x2

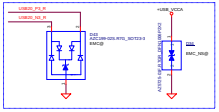






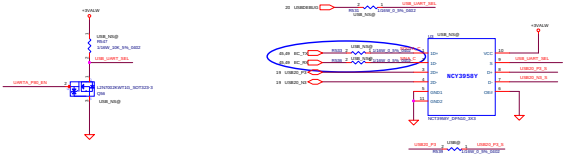
FOR ESD





For USB Debug Function

09/20SF add USB debug follow TINY5
change from SA00007WL0D to SA00007WL00 SF1001
SVT non-staff0322SF



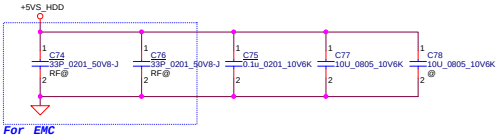
USBDEBUG	Kernel debug
Pin1 status	Pin1 status
Pin2 status	disable

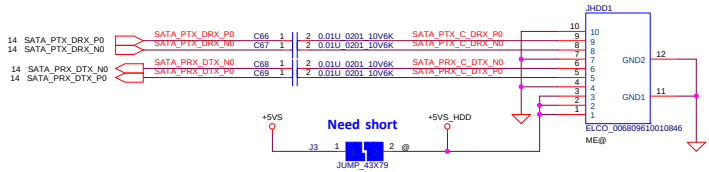
UARTA_P80_EN	POST 80
Pin status	disable
Pin2 status low	disable

DEF	S	FUNCTION
L	L	disable
L	H	Uart-A to Uart-C
L	H	Uart-C to Uart-A

Security Classification	LC Future Center Secret Data		Title	USB3.0 PORT (LEFT)	
Issued Date	2015/08/20	Deciphered Date	2016/08/20		
Size	Document Number				Rev 1A
C	E6539				
Date: Friday, March 18, 2016		Sheet 49 of 61			

SATA HDD Conn.





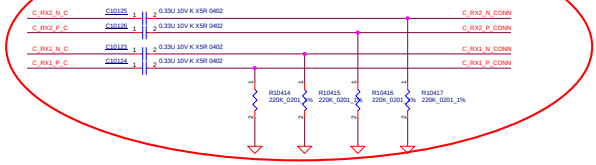
Delete SATA ODD

8/14 Update SF

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

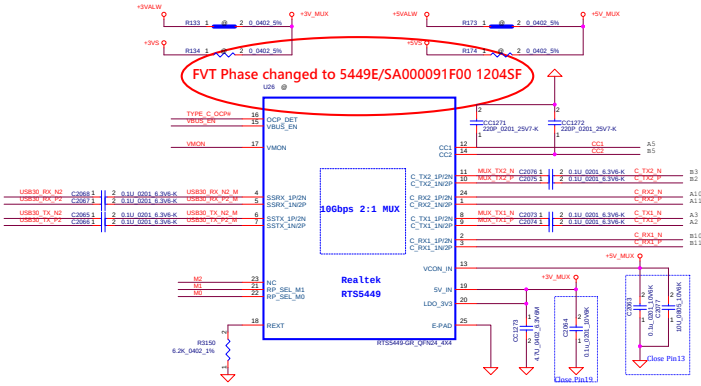
Title	HDD/ODD CONN	
Size: Custom	Document Number: E6530	Rev: 1.0
Date: Thursday, March 29, 2018	Sheet 47 of 68	

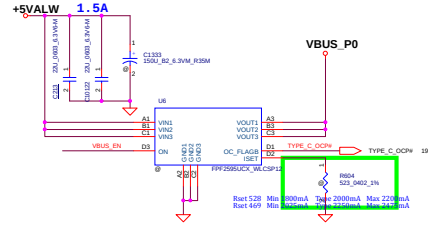
0.33UF change to SE00000Y700/0402,220K PD stuff 0323SF
For intel MOW(575549) ww46 USB3.1 Type-C USB-IF ENC update 1127SF

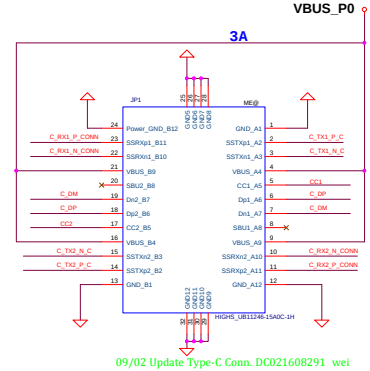


optimaze design, and serach low cost power switch 0906SF
change to SY6288C20AAC_SOT23-5 1207SF

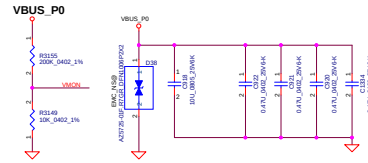
FVT Phase changed to 5449E/SA000091F00 1204SF



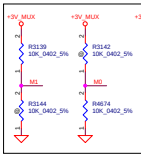




09/02 Update Type-C Conn. DC021608291 wei

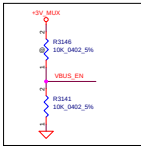


Rp configuration



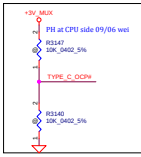
Rp:1.5A (now)

	M1	M0	M2	Note
Rp:900mA	0	1		R3144/R3142 mount
Rp:1.5A	1	0		R3139/R3143 mount
Rp:3.0A	1	1		R3139/R3142 mount
Rp:NA				R10410 mount for RTS5449E



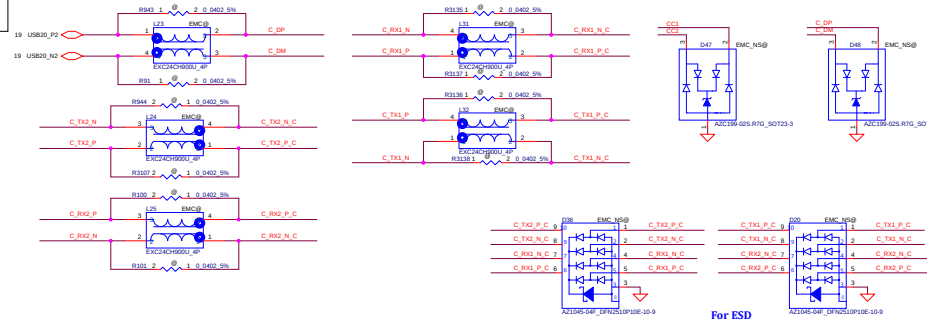
For C_VBUS
power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount



For C_VBUS
power switch OCP pin

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

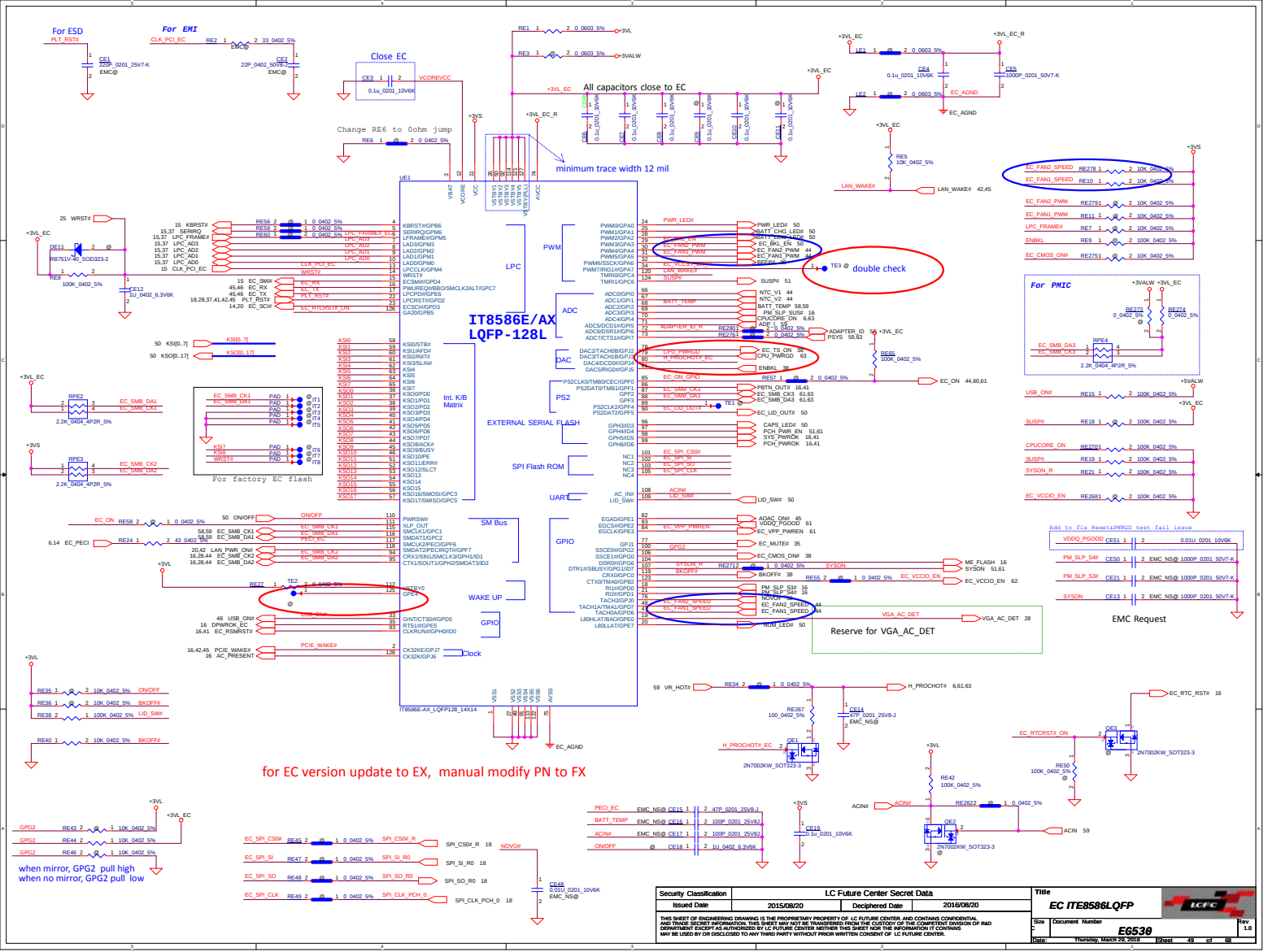


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: 3D Camera

Size	Document Number	Rev
Custom	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 48 of 68



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

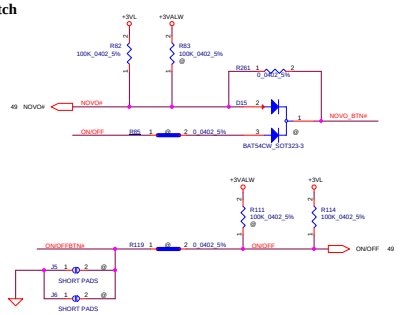
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: EC ITE8586LQFP

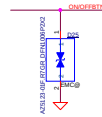
Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 49 of 68

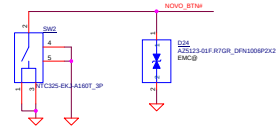
ON/OFF switch



8/16 Del Power Button wei

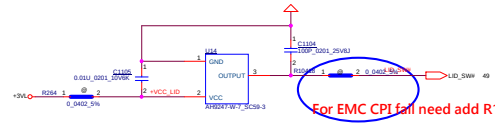


Novo button



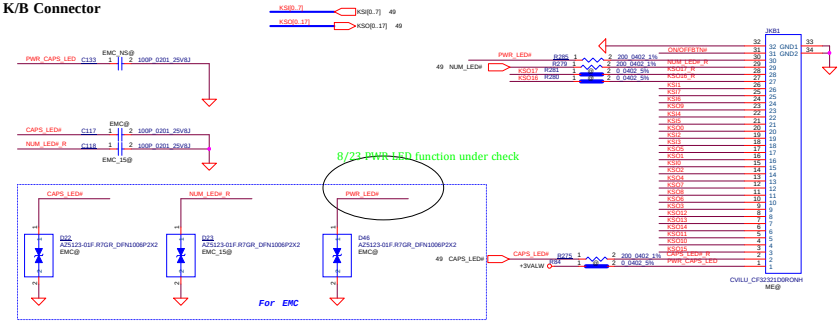
8/31 Update the P/N SN100008W00 wei

LID switch



For EMC CPI fail need add R10418---1204SF

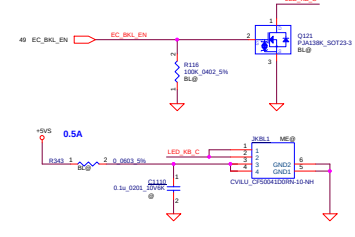
K/B Connector



8/23 PWR LED function under check

KB Backlight Connector

update BL circuit and need too be confirm conn pin define 0925SF

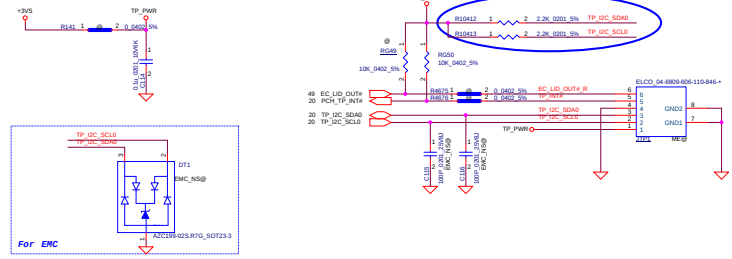


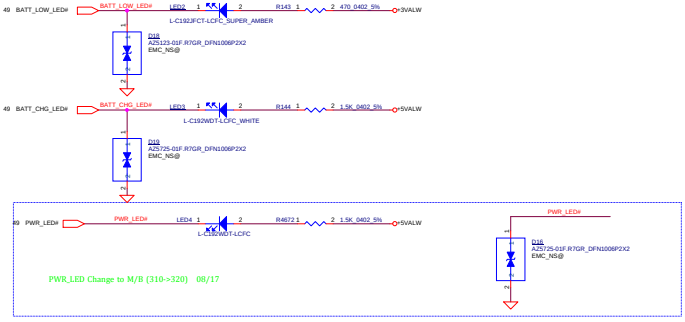
8/31 Update KBL Conn. P/N SP011608241 wei

Finger Print Connector

follow OD V1.5 delete finger print function 0927SF

TP/B Connector





PWR_LED Change to M/B (310->320) 08/17

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: KBD/PWR/IO/LED/TP Conn

Size	Document Number	Rev
Custom	E6530	1.0

Date: Thursday, March 26, 2015 Sheet 50 of 68

Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

Need Short

Need Short

Change the main source to SA000067600 (GMT) 7/16

ERC

Need short

8/29 Add +1.8VS Circuit for Audio wei

For DisCharge

08/29: Need double check enable signal and the resistance

+1.8VALW to +1.8VS_AON

V20B+

delete reserved for VCCSTG & VCCST 0928SF

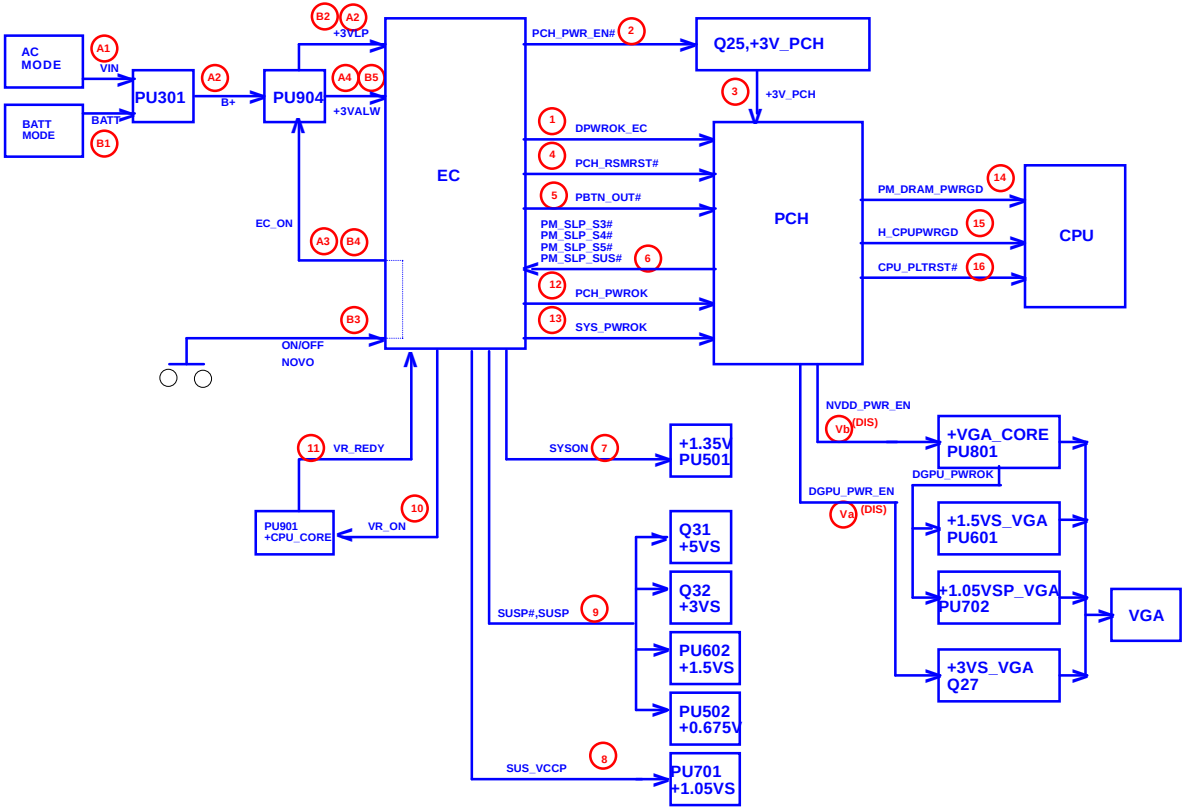
VCCSTG & VCCST change to Dual Switch 0906SF

+1.0VALW TO +1.0VGS

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, INC. CONTAINS INFORMATION THAT IS PROPRIETARY TO LC FUTURE CENTER, INC. AND MAY BE CONFIDENTIAL. ANY UNAUTHORIZED USE, DISCLOSURE OR REPRODUCTION IS PROHIBITED. THIS SHEET OF ENGINEERING DRAWING MAY NOT BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	DC V TO VS INTERFACE
Size	Document Number
Custom	E6539
Date:	Thursday, March 29, 2018
Sheet	44 of 48



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 52 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Virtual symbol

Size	Document Number	Rev
C	E6521	0.1

Date: Friday, March 30, 2018 Sheet 53 of 68

GPU Thermal Holex2 Close to RJ45 DC-IN x2

CPU Thermal Holex3 WLAN Standoff

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

H1 HOLEA — PAD_O3p2x2p7d3P2x2P7N

H2 HOLEA — PAD_C2P7D2P7N

H3 HOLEA — PAD_C6P0D2P4

H4 HOLEA — PAD_C6P0D2P4

H5 HOLEA — PAD_C6P0D2P4

H6 HOLEA — PAD_C6P0D3P0 CHASSIS1_GND

H7 HOLEA — PAD_CT6P0B6P5D3P0

H8 HOLEA — PAD_CT5P5B6P0D4P0

H9 HOLEA — PAD_CT5P5B6P0D4P0

H10 HOLEA — PAD_CT5P5B6P0D4P0

H11 HOLEA — PAD_CT5P5B6P0D4P0

H12 HOLEA — PAD_CT5P5B6P0D4P0

H13 HOLEA — PAD_C6P0D3P3

H14 HOLEA — PAD_C5P5D3P3

H15 HOLEA — PAD_C6P0D3P3

H17 HOLEA — PAD_C5P5D3P0

H18 HOLEA — PAD_C6P0D2P4

H20 HOLEA — PAD_C5P5D3P0

follow layout list update 0925SF

Close to Audio jack

SH1 ME@ — SPRING_FINGER_6.2X1.64

SH2 ME@ — SPRING_FINGER_6.2X1.64

SH3 ME@ — SPRING_FINGER_6.2X1.64

SH4 ME@ — SPRING_FINGER_6.2X1.64

SH5 ME@ — SPRING_FINGER_6.2X1.64

SH6 ME@ — SPRING_FINGER_6.2X1.64

USB3.0 Shielding

SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

SH7 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

SH8 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

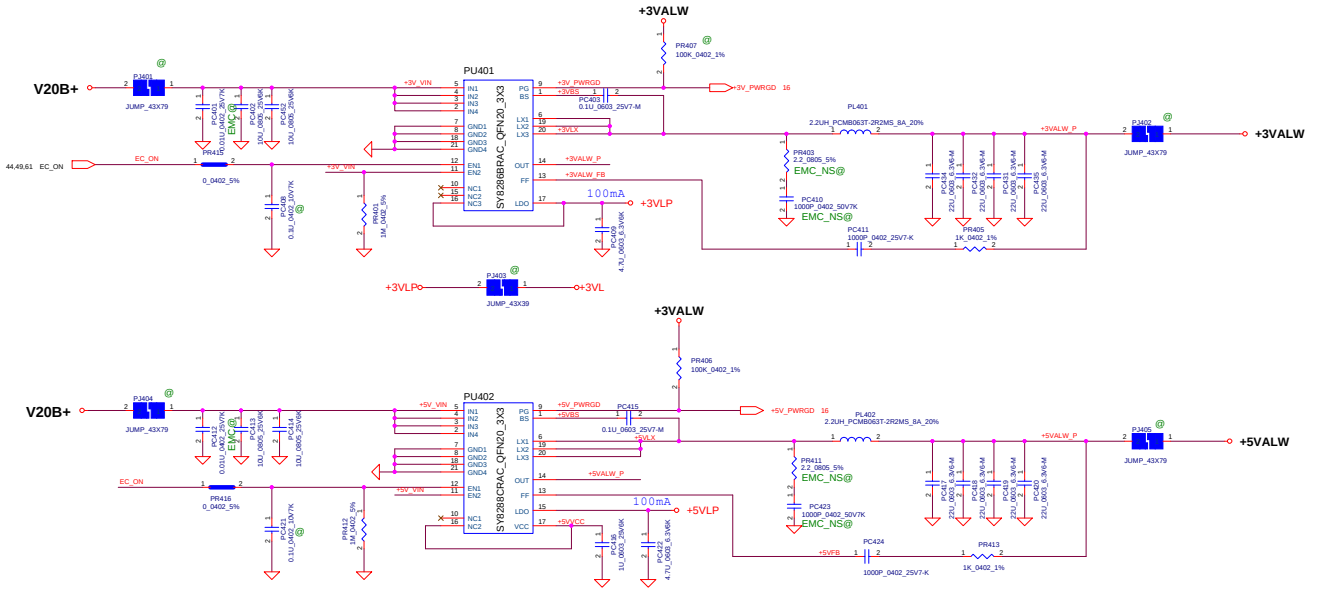
DDR4 Shielding

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Hole

Size	Document Number	Rev
B	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 54 of 68



VOUT=3.07V
TDC=6A
OCP=10A
Fsw=600Khz

VOUT=5.01V
TDC=8A
OCP=12A
Fsw=600Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *Cover Page*

Size: C | Document Number: *E6530* | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 60 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: *PWR_3VALW/5VALW*

Size: C | Document Number: *E6530* | Rev: 1.0

Date: Thursday, March 29, 2018 | Sheet 54 of 60

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

Cover Page

Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 55 of 68

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

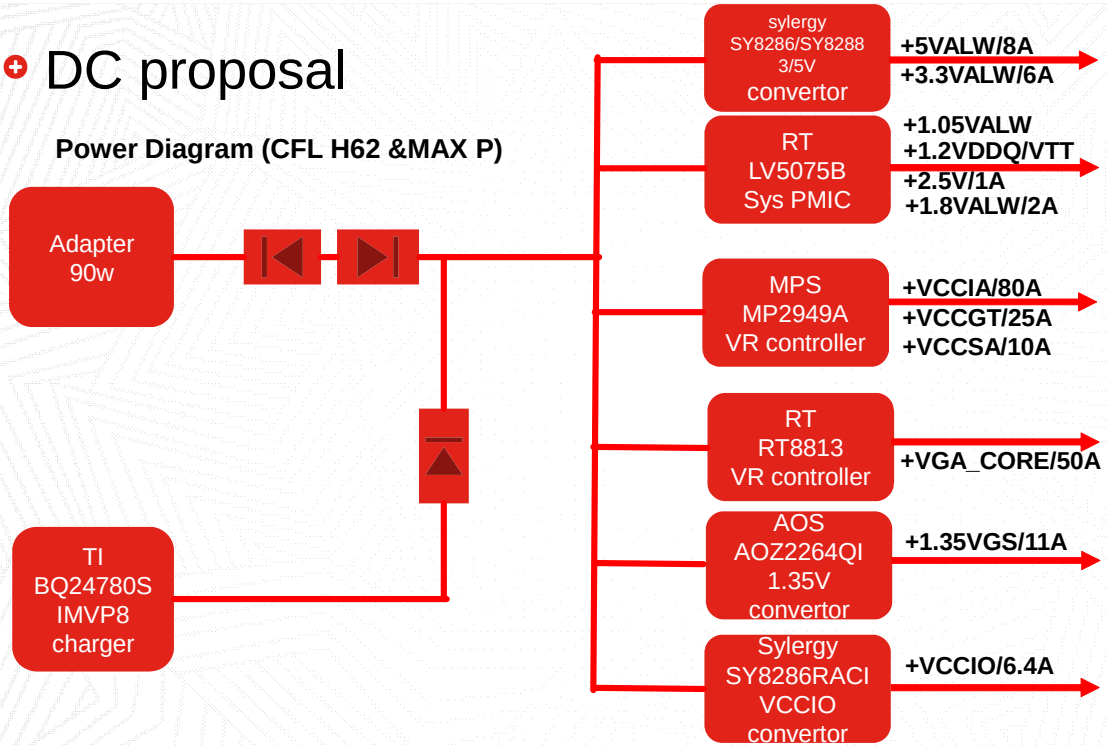
Cover Page

Size	Document Number	Rev
B	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 56 of 68

DC proposal

Power Diagram (CFL H62 &MAX P)



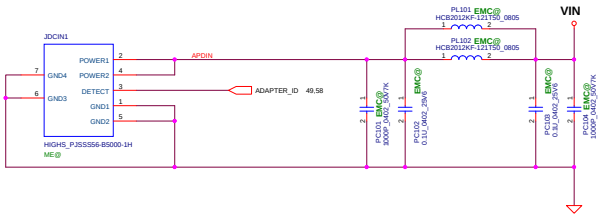
LCFC

1

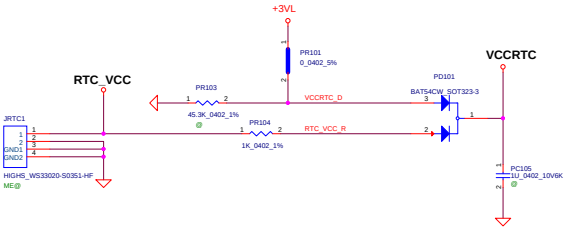
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cover Page**

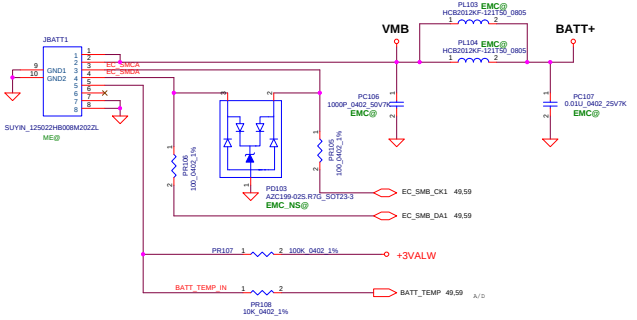
Size	Document Number	Rev
B	EG530	1.0
Date: Thursday, March 29, 2018	Sheet 57 of 68	



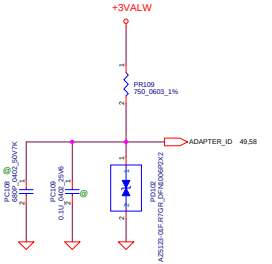
DC IN:1.DC IN connect apply for PN HIGHS_PJSSS56-B5000-1H_5P-T ,need replace connector rate current 7A



RTC:1. 0ohm delete
2.the max VCCRTC < 3.2V specification
3.RTC cable 35mm



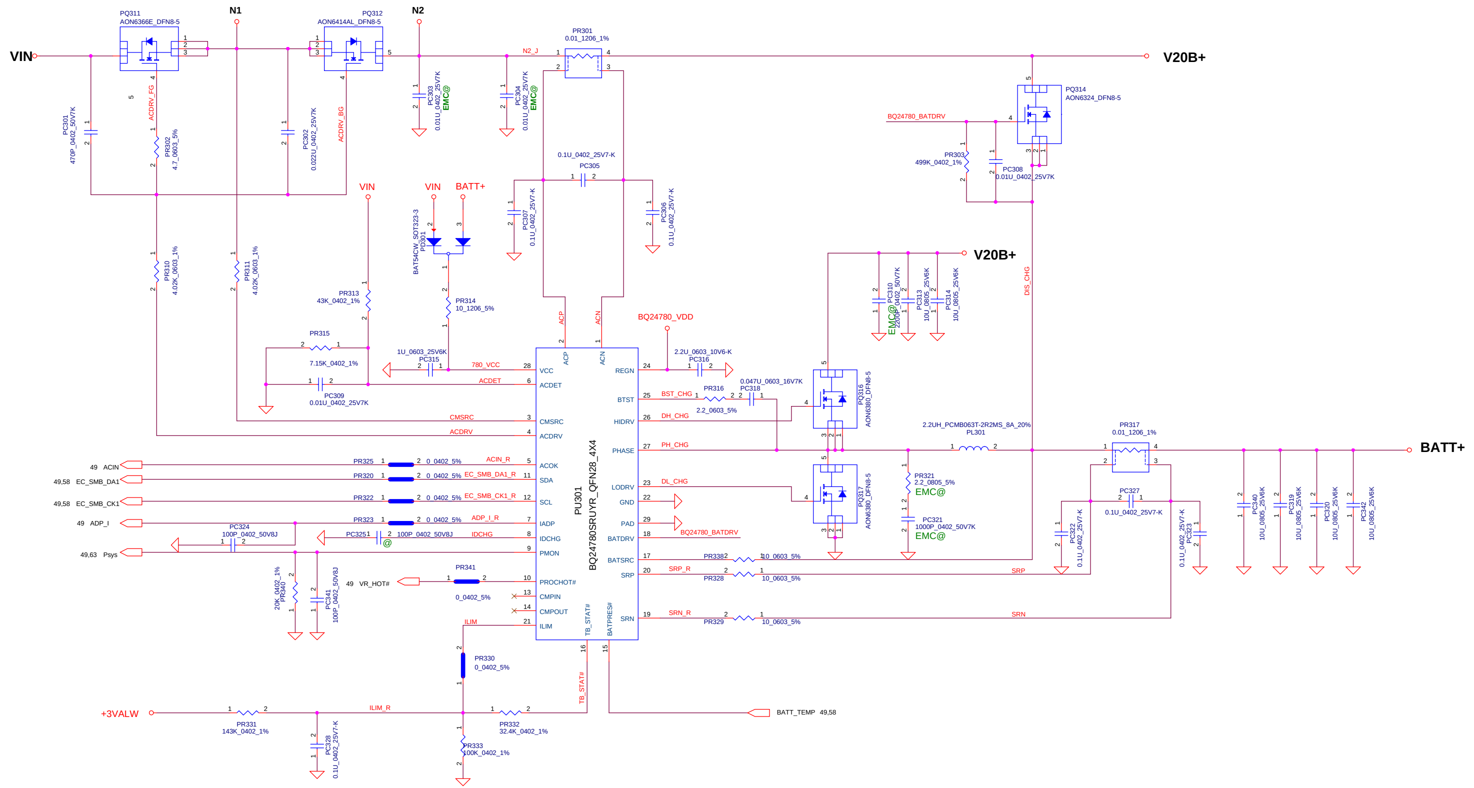
battery IN:
1.battery connector 8pin per pin 4.5A



ADP_ID:1. cost down solution
2.EC initial ID function

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

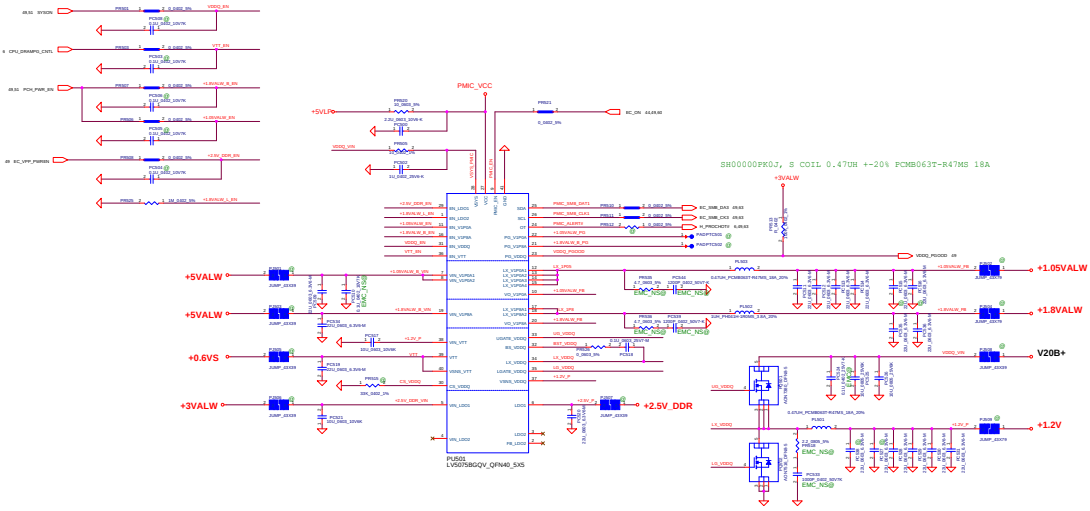
Title	Cover Page		
Size	Document Number		Rev
C	EG530		1.0
Date:	Thursday, March 29, 2018	Sheet	58 of 68



charge current:1C 5A
charge voltage:12.6V
charge frequency:800K
ILIM pin:charge7A, turbo-discharge-10A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

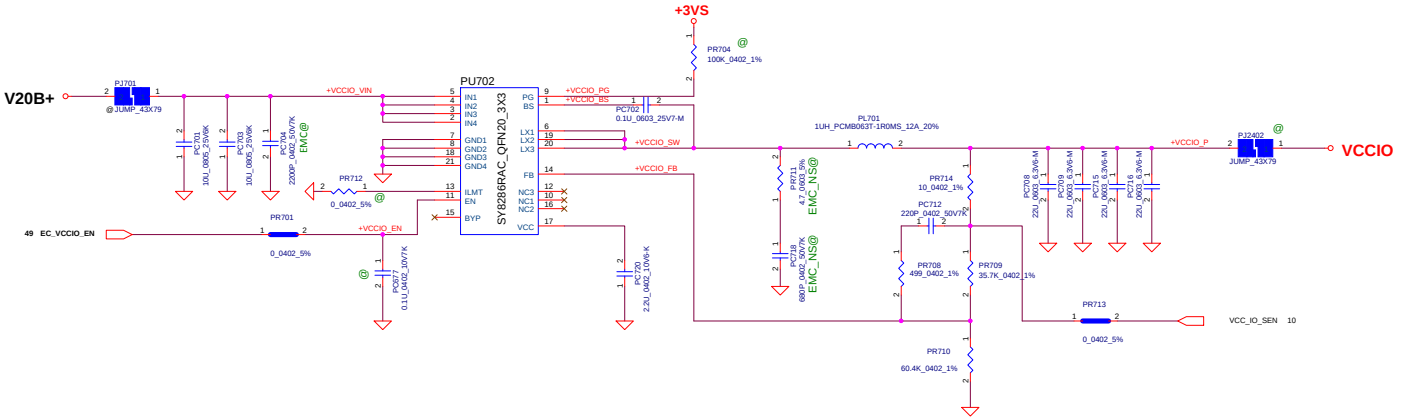
Title			
Cover Page			
Size: Custom	Document Number: EG530		Rev: 1.0
Date: Thursday, March 29, 2018		Sheet 59 of 68	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2015/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE ENGINEERING DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER MANAGEMENT AND NEITHER IT NOR THE INFORMATION IT CONTAINS MAY BE USED, REPRODUCED OR DISCLOSED TO OTHERS EXCEPT AS AUTHORIZED BY LC FUTURE CENTER MANAGEMENT.

Title	Cover Page		
Size	Document Number		Rev
A		E6539	1.0
Date:	Thursday, August 20, 2015	Sheet	41 of 41



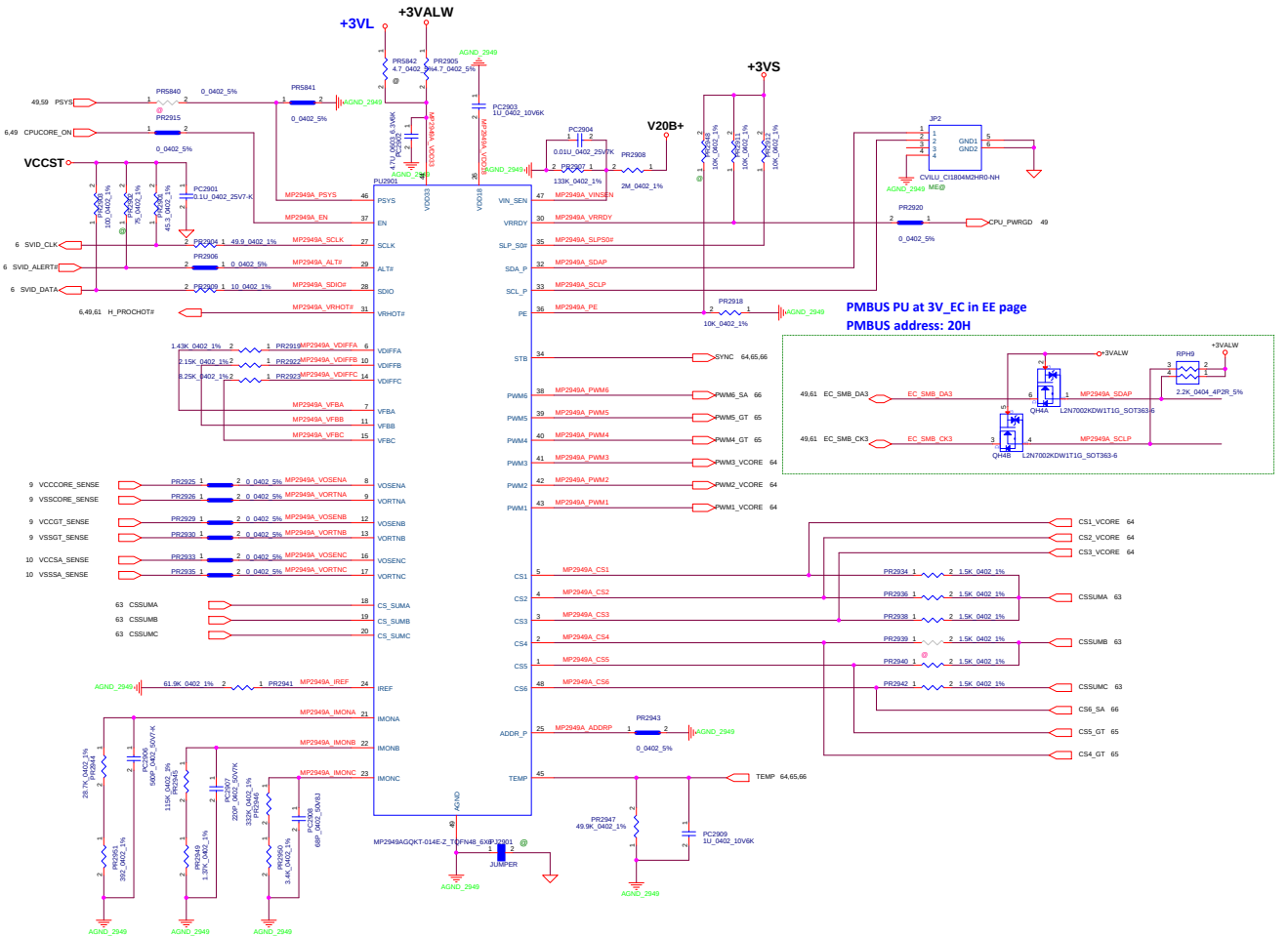
VCCIO:FB=0.6V/0.954V
TDC=6A
OCP:10A
OVP:120%
frequency:500Khz
remove sense pull high in power side

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cover Page**

Size	Document Number	Rev
Custom	EG5308	1.0

Date: Thursday, March 29, 2018 Sheet 62 of 68

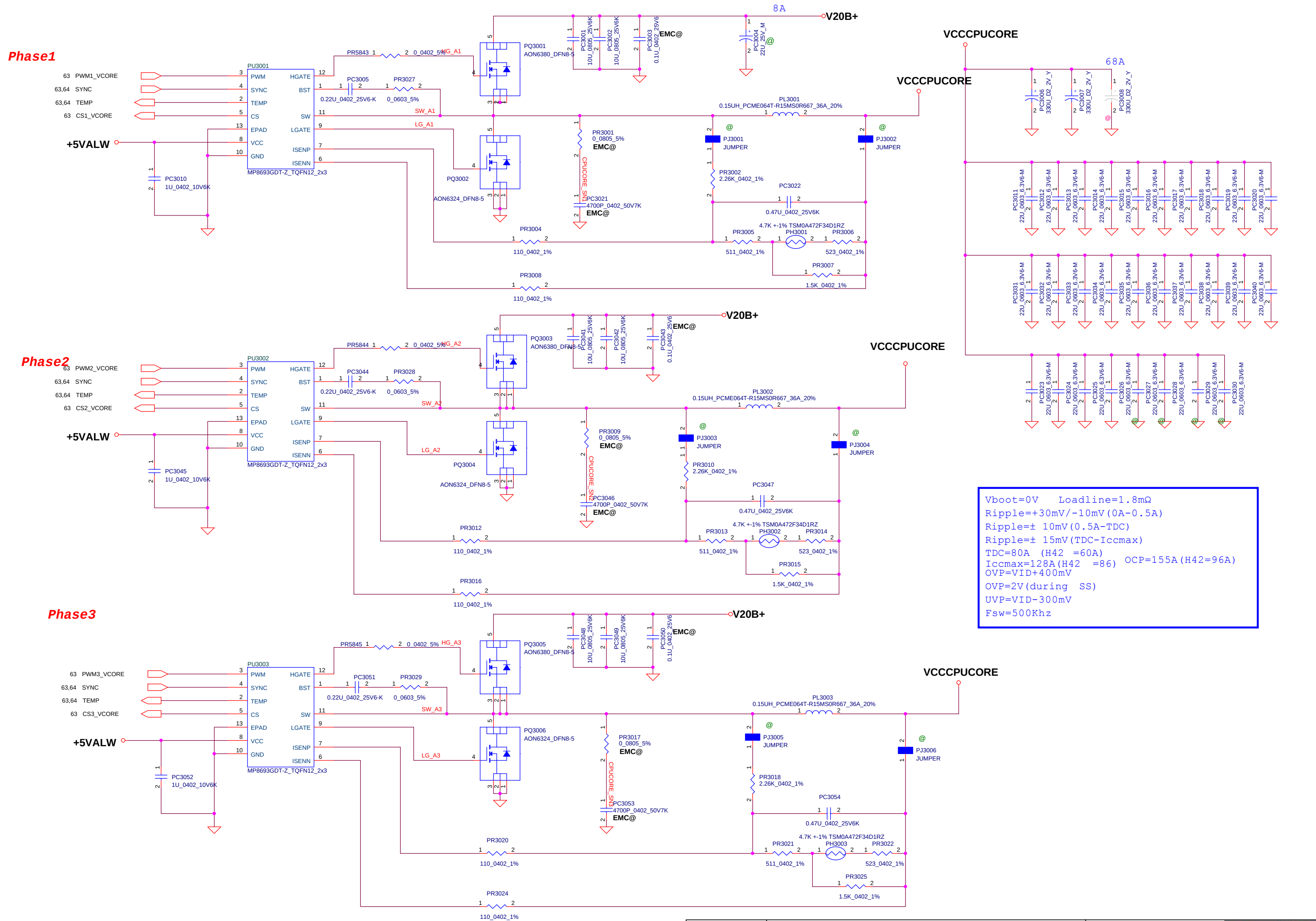


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cover Page**

Size	Document Number	Rev
C	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 63 of 68



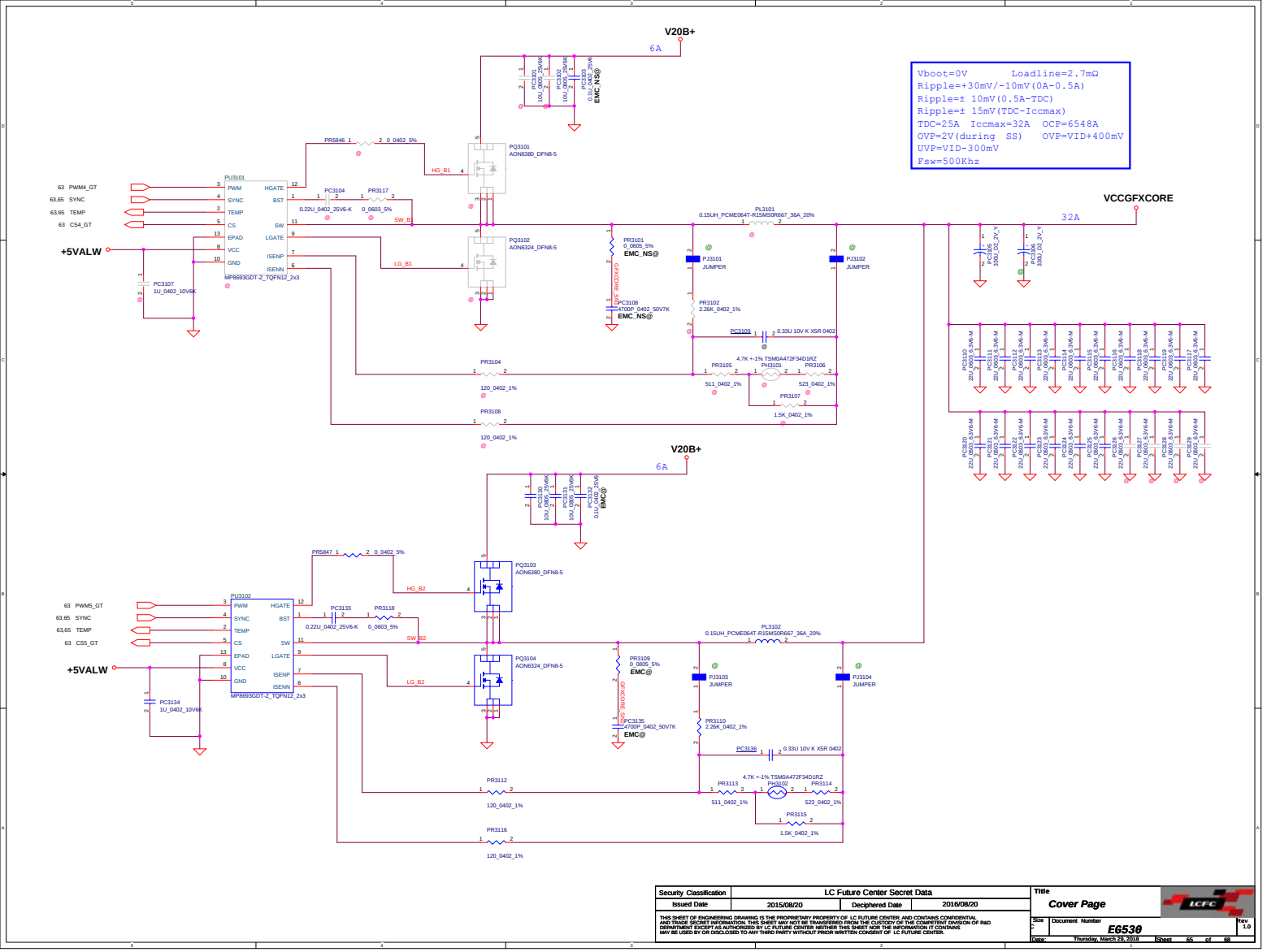
Vboot=0V Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=80A (H42 =60A)
Iccmax=128A(H42 =86) OCP=155A(H42=96A)
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page

Size: C | Document Number: EG530 | Rev 1.0

Date: Thursday, March 29, 2018 |



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

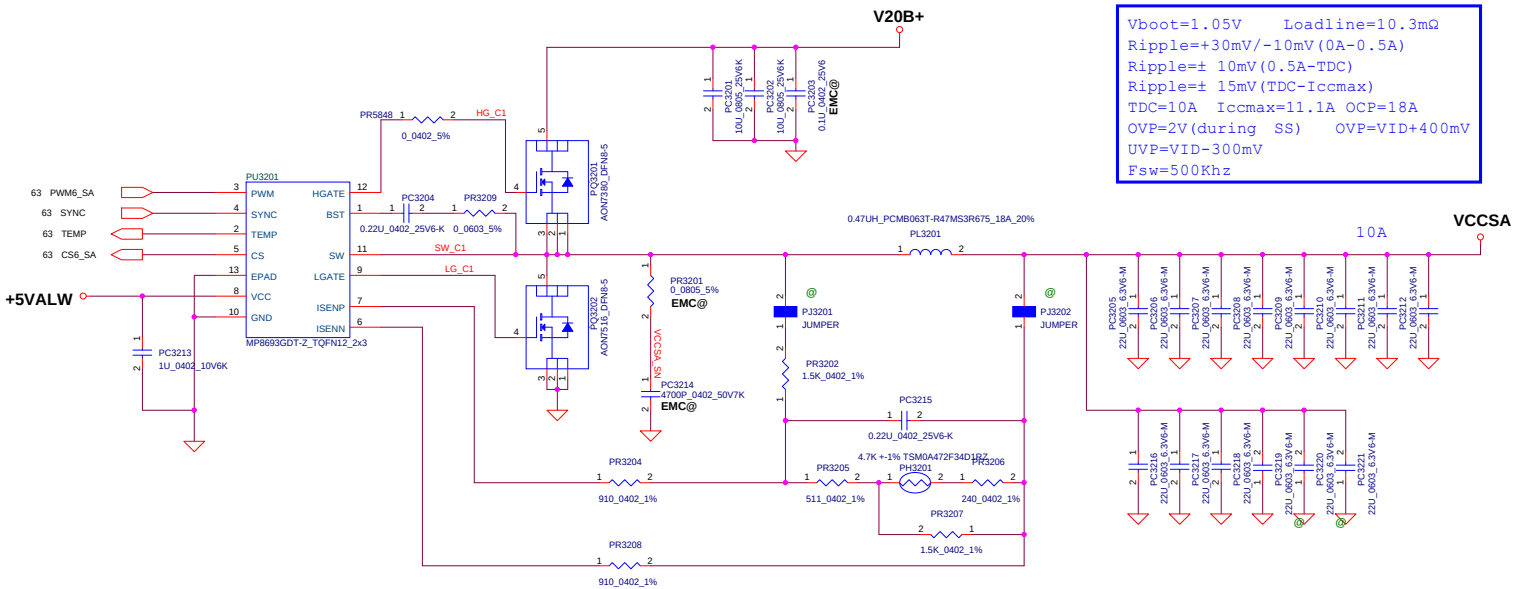
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: **Cover Page**

Size	Document Number	Rev
C	E6530	1.0

Date: Thursday, March 29, 2018 Sheet 65 of 68

VER1.10

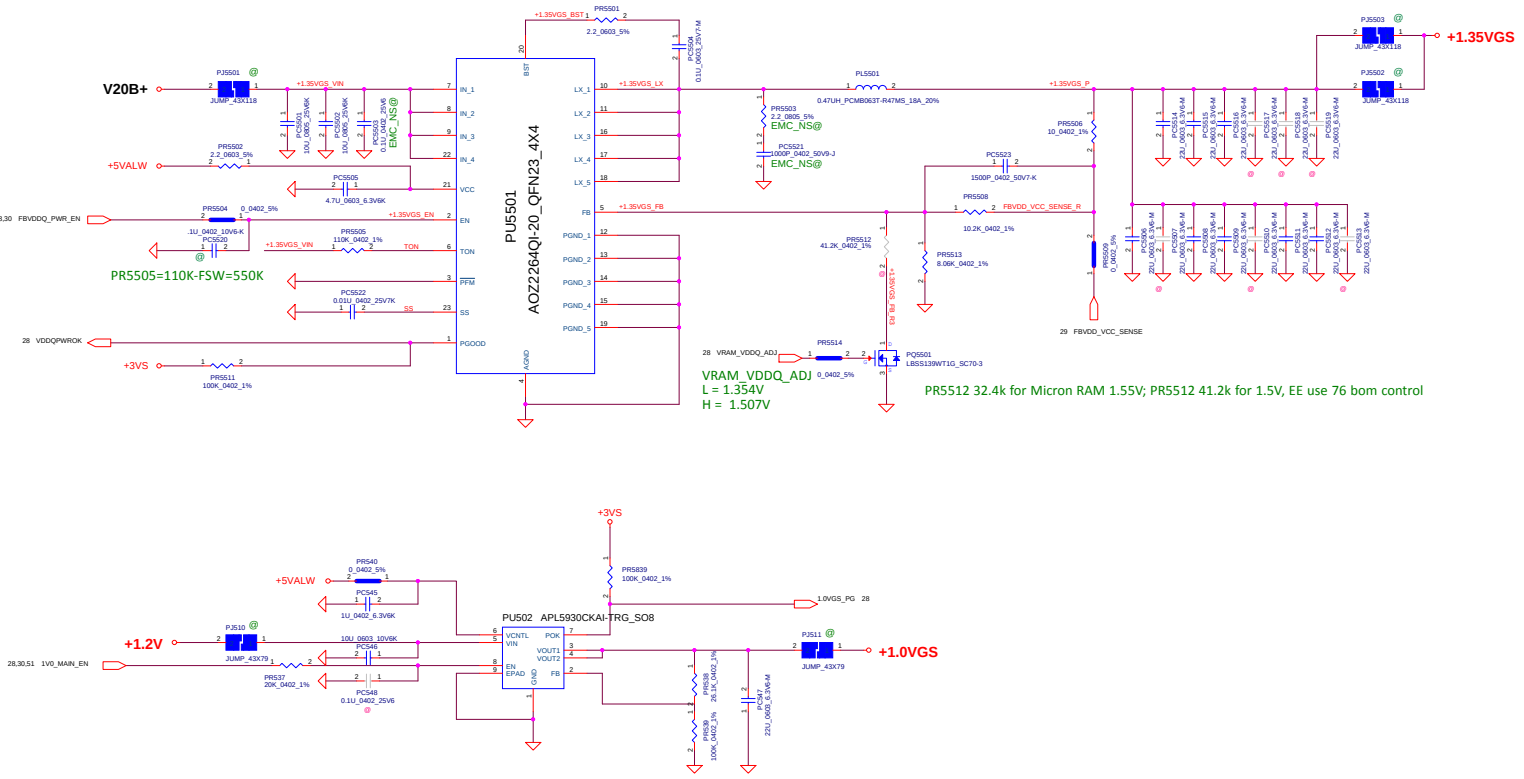


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Cover Page**

Size	Document Number	Rev
B	EG530	1.0

Date: Thursday, March 29, 2018 Sheet 66 of 68

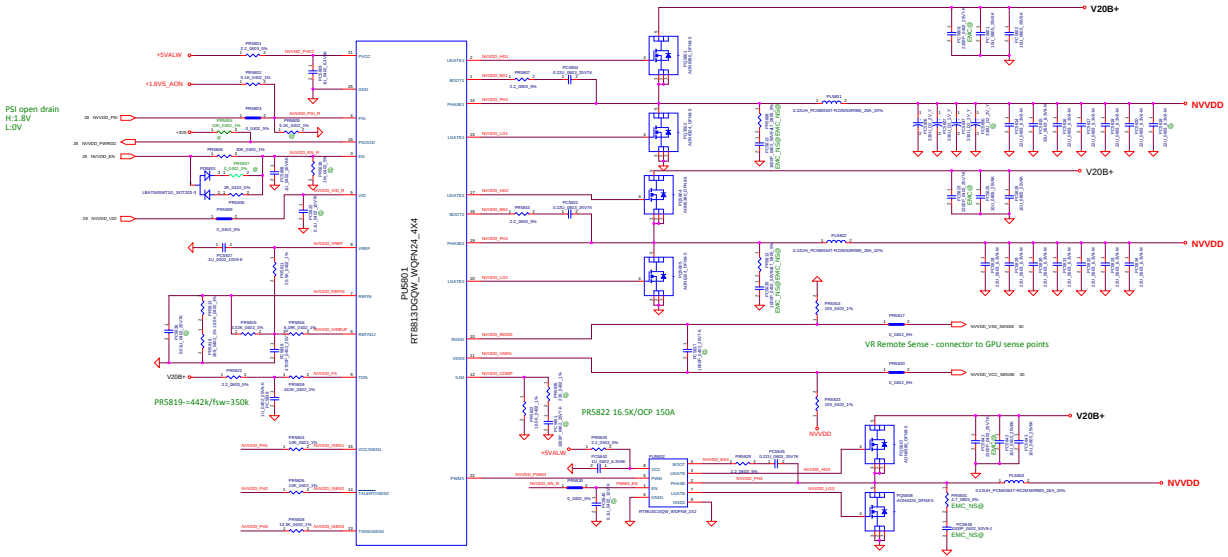


1.35VGS
FB:0.6V/1.35V
TDC=11A
ICCMAX=20A
OCP=25A
FSW=550K

LDO-1.0VGS
TDC:1A
iccmax:1.1A
FB:0.8V/1.0V

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	Cover Page		
Size	Document Number		Rev 1.0
C	E6539		
Date:	Thursday, March 29, 2018	Sheet 67 of 68	



VBOOT:0.8V
VID voltage:0.3V~1.3V
TDC:50A
ICCMAX:100A
OCP:50A*3=150A
frequency:350K*3=1050khz

Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page

Size	Document Number	Rev
	E6530	1A

Date:	Thursday, March 31, 2016	Sheet	48	of	48