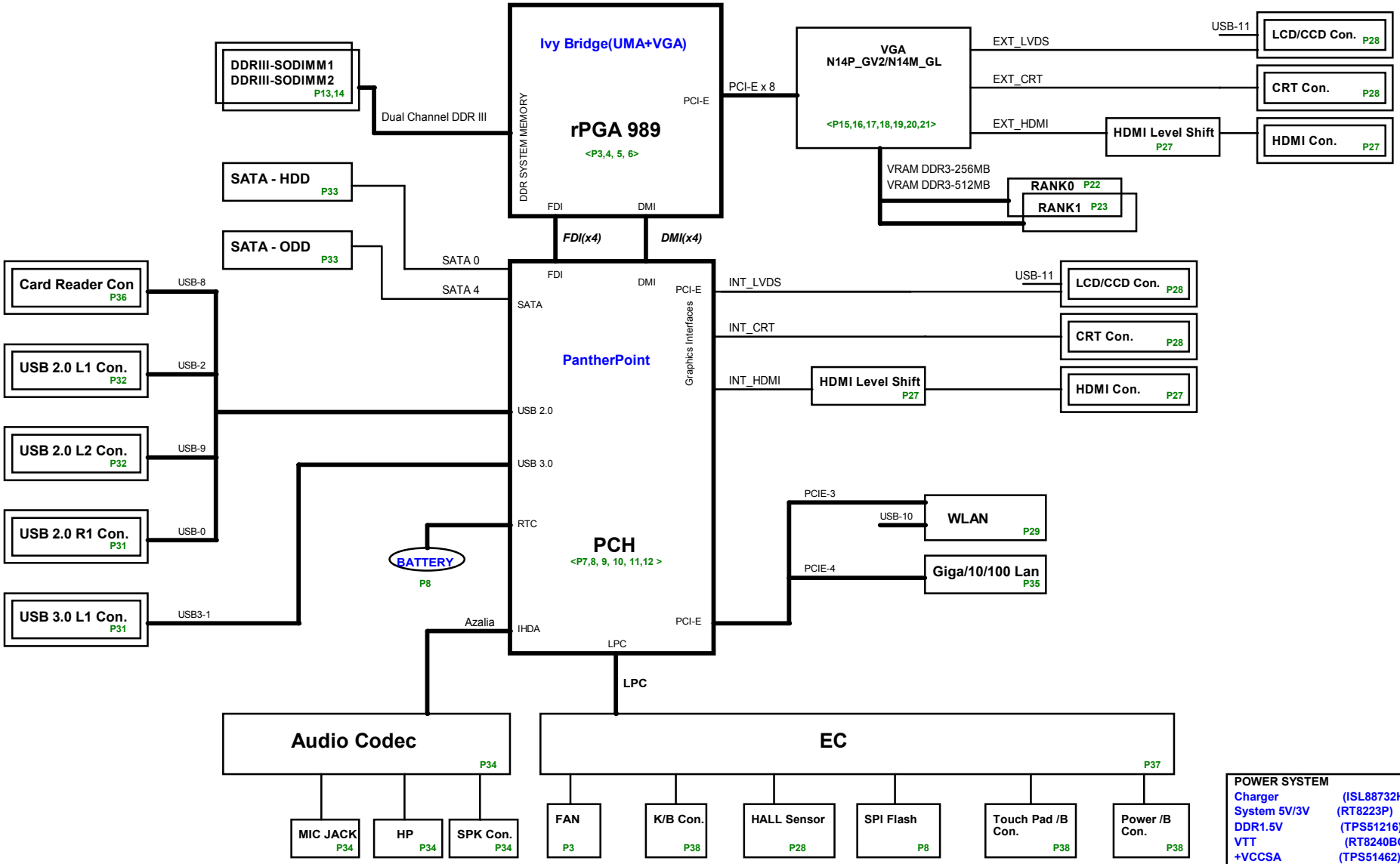
# Chief River Block Diagram






| POWER SYSTEM | | |
|---|---|---|
| Charger | (ISL88732HRTZ-T) | P40 |
| System 5V/3V | (RT8223P) | P41 |
| DDR1.5V | (TPS51216) | P42 |
| VTT | (RT8240BGQW) | P43 |
| +VCCSA | (TPS51462) | P44 |
| +VCORE+VGFX | (ISL95836) | P45 |
| +1.8V | (G966A) | P46 |
| nVDIA_GPU | (RT8812A) | P47 |

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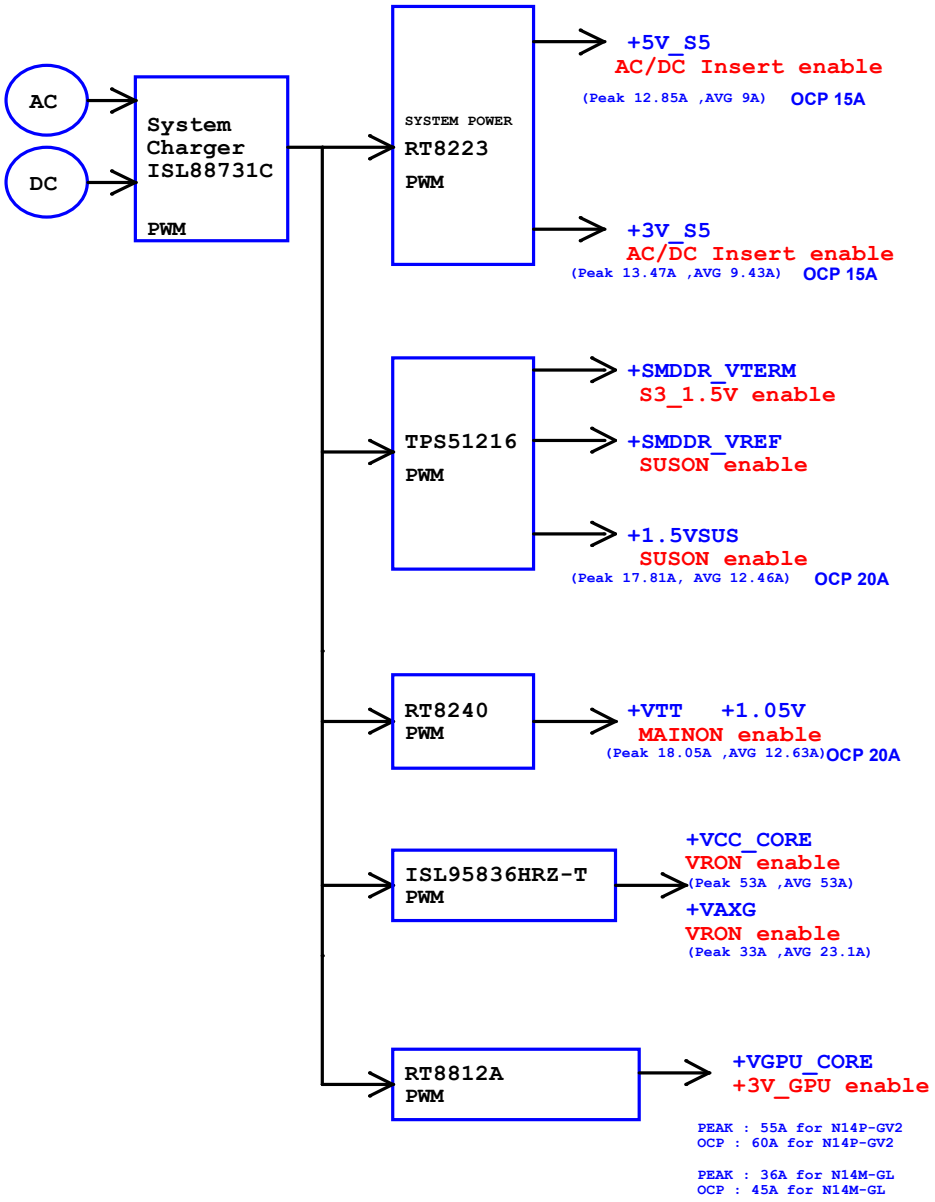
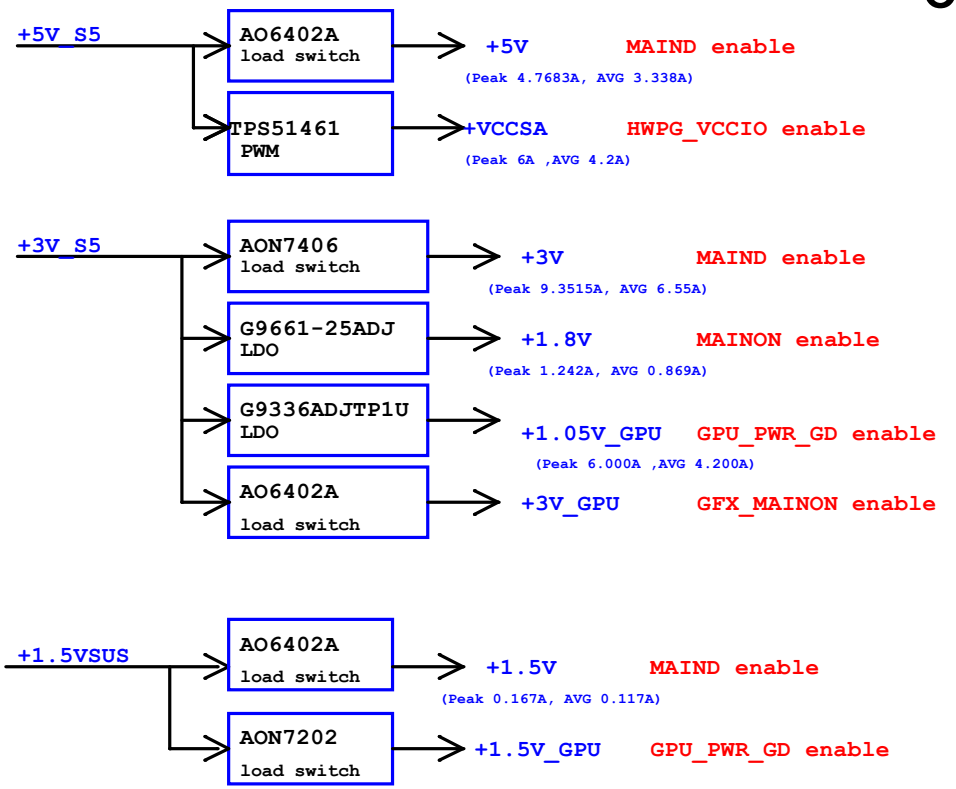
| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | A1A |

Date: Friday, December 28, 2012 Sheet 1 of 49

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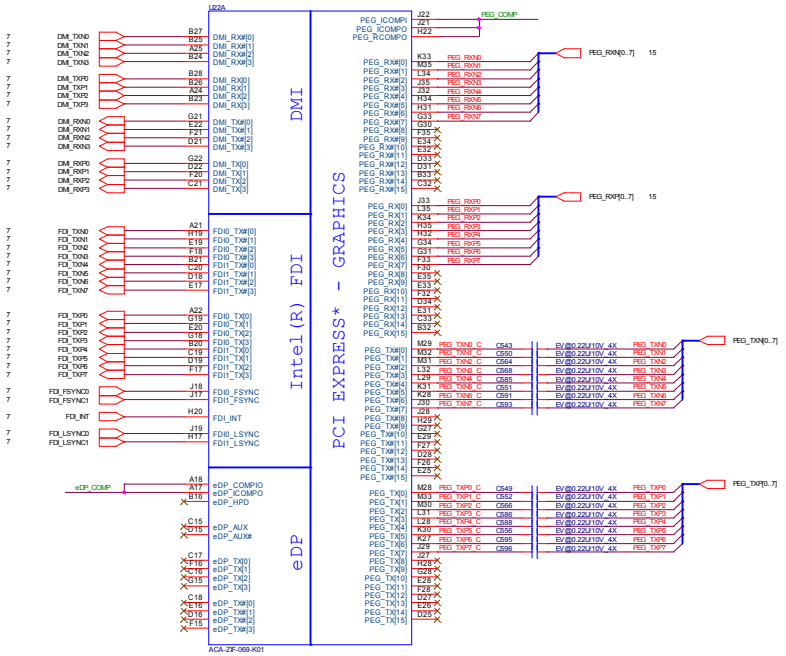
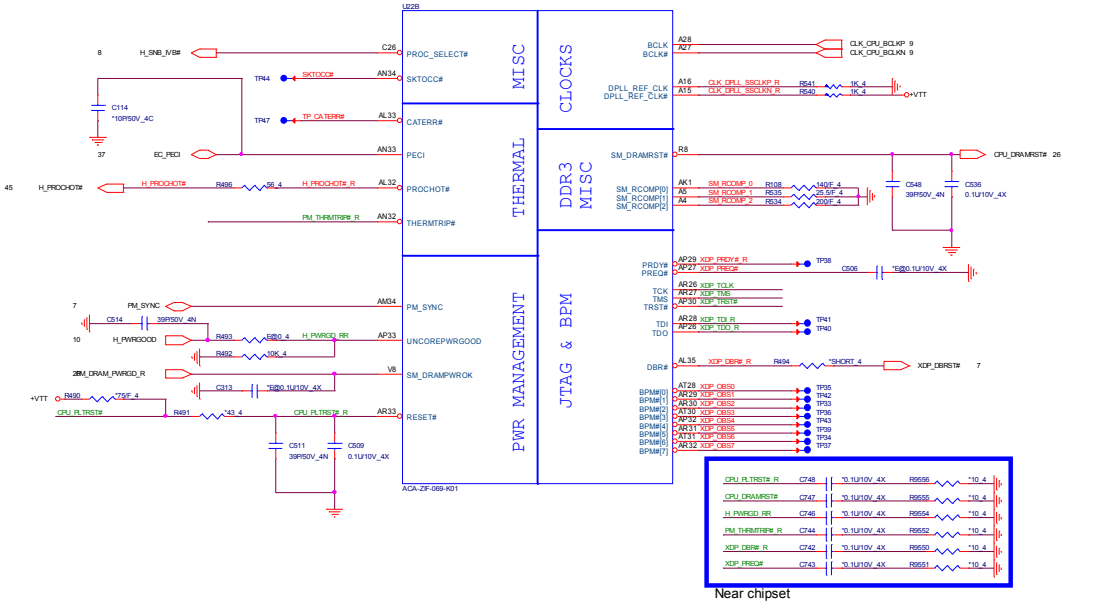
| Size | Document Number | Rev |
|---|---|---|
| | POWER TREE TABLE | A1A |

Date: Friday, December 28, 2012 Sheet 2 of 49

# Ivy Bridge Processor (DMI,PEG,FDI) CPU/VGA

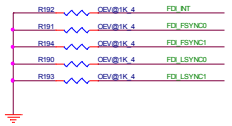



# Ivy Bridge Processor (CLK,MISC,JTAG)CPU

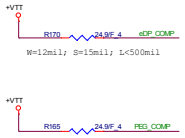



03

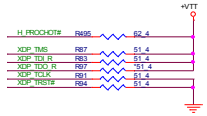
## FDI Disabling (Discrete Only) OEV



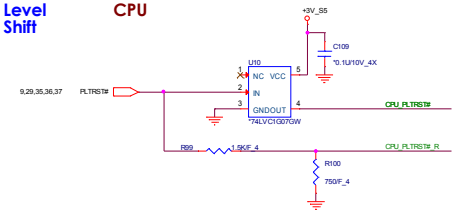
## DP & PEG Compensation CPU



## Processor pull-up CPU

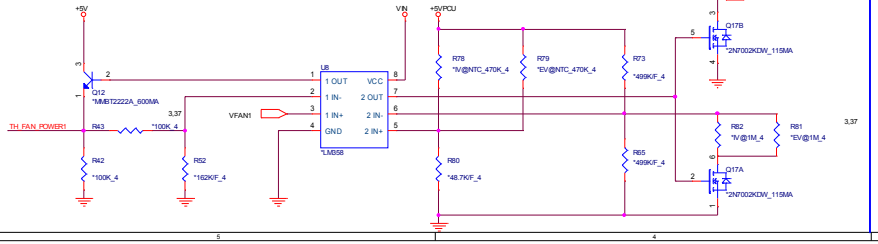


## Level Shift CPU

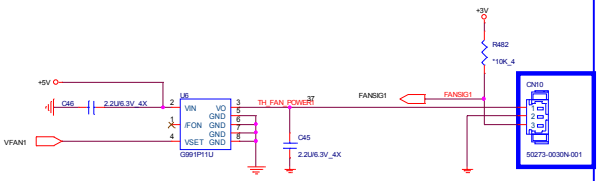


## Thermal Trip & Process HOT CPU

## Intel Turbo mode only CPU

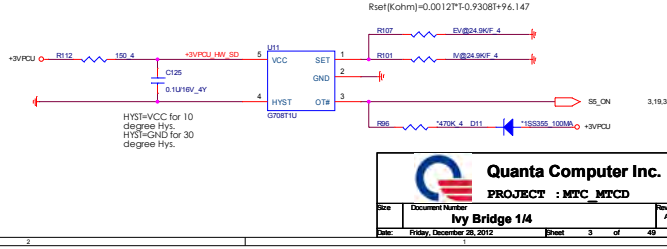


## FAN Control-->For one FAN solution THC



## CPU Thermal sensor / MB Local TEMP

## THP/UGA/VGA

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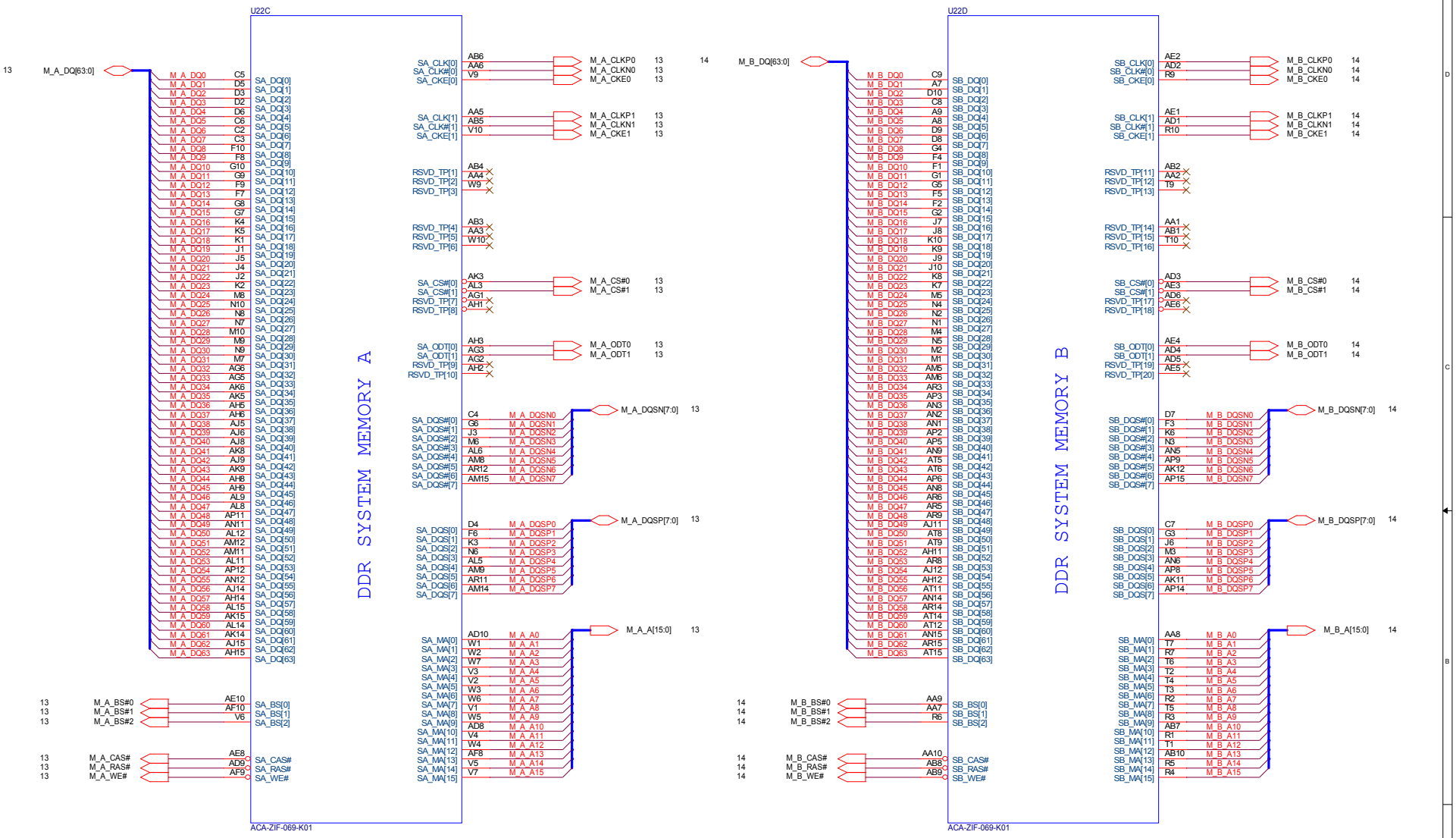
PROJECT : MTC_MTCD

Size: Document Number: Ivy Bridge 1/4 Rev: A1A

Date: Friday, December 28, 2012 Sheet 3 of 49

# Ivy Bridge Processor (DDR3)CPU

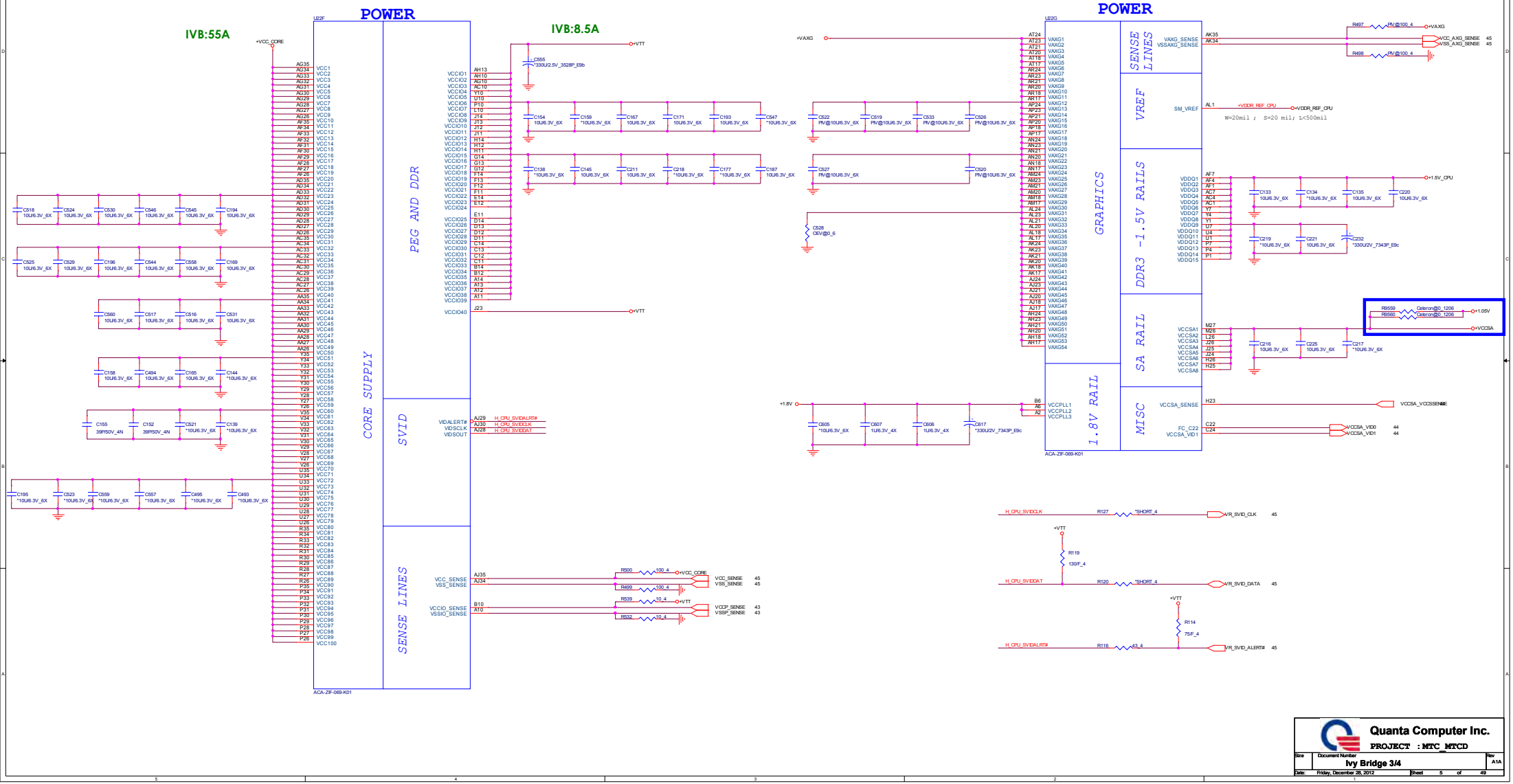





| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : MTC_MTCD | | |
| Size | Document Number: Ivy Bridge 2/4 | Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 4 of 49 | |

# Ivy Bridge Processor (POWER) CPU

# Ivy Bridge Processor (GRAPHIC POWER) CPU/OEV/PIV

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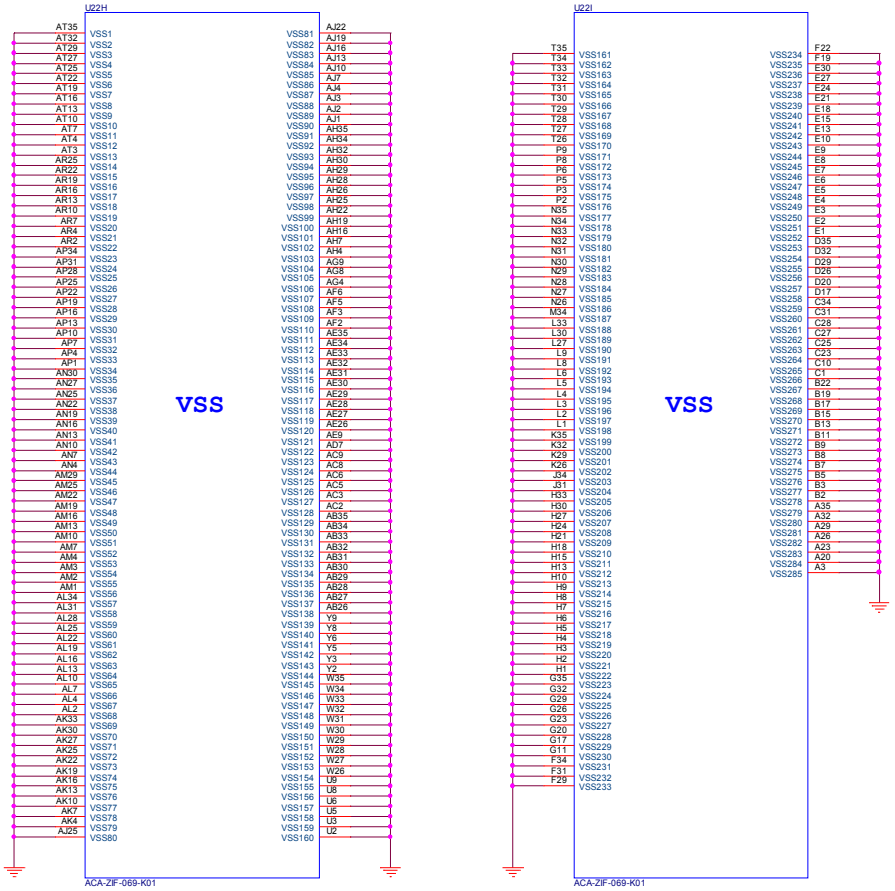
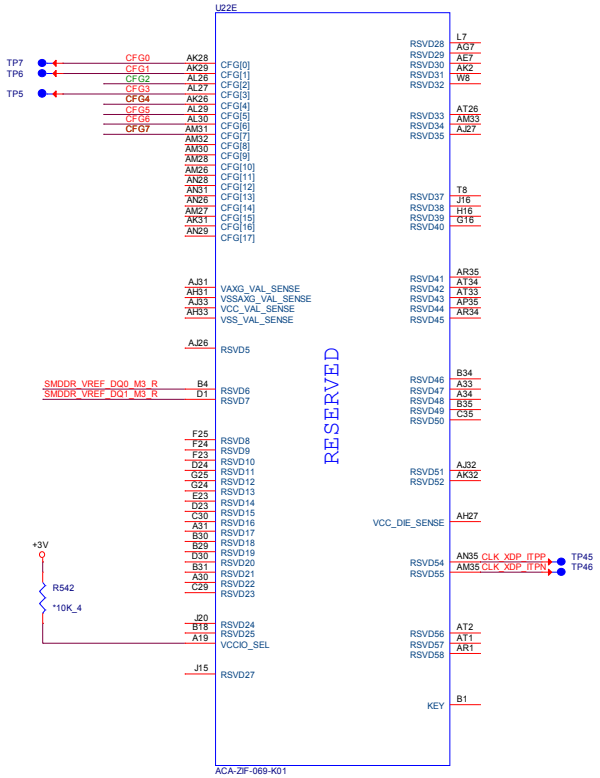
| Size | Document Number | Rev |
|---|---|---|
| | Ivy Bridge 3/4 | A1A |
| Date: Friday, December 28, 2012 | Sheet 5 of 49 | |

# Ivy Bridge Processor (GND) CPU




# Ivy Bridge Processor (RESERVED, CFG) CPU

06

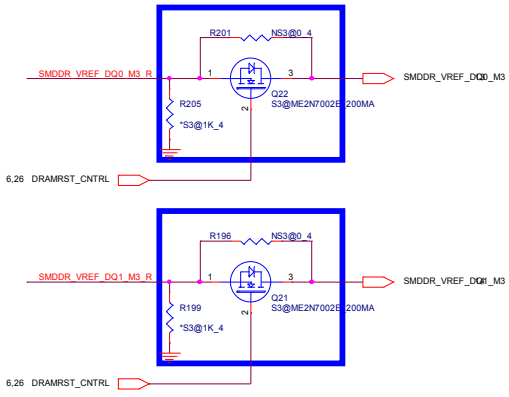



## Processor Strapping CPU/VGA

The CFG signals have a default value of '1' if not terminated on the board.

| Pin Name | Configuration | |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal --> 16 Lane) | 1=Normal Operation<br>0=Lane Reversed | CFG2 R85 *EV@1K_4 |
| CFG3<br>(Reserved) | | |
| CFG4<br>(DP Presence Strap) | 1=Disable; No physical DP attached to eDP<br>0=Enable; An ext DP device is connected to eDP | CFG4 R88 *1K_4 |
| CFG5<br>CFG6<br>(PCIE Bifurction) | 00=x8,x4,x4 - Device 1 function 1 and 2 enable<br>01=Reserved - (Device 1 function 1 disable ; function 2 enable)<br>10=x8,x8 -Device 1 function 1 enable ; function 2 enable<br>11=(Default) x16 -Device 1 function 1 and 2 disable | CFG5 R93 EV@1K_4<br>CFG6 R95 *EV@1K_4 |
| CFG7<br>(PEG Defer Training) | 1=PEG train immediately following xxRESETB de assertion<br>0=PEG wait for BIOS training | CFG7 R98 *1K_4 |

## DDR3 VREF DQ (M3) S3P

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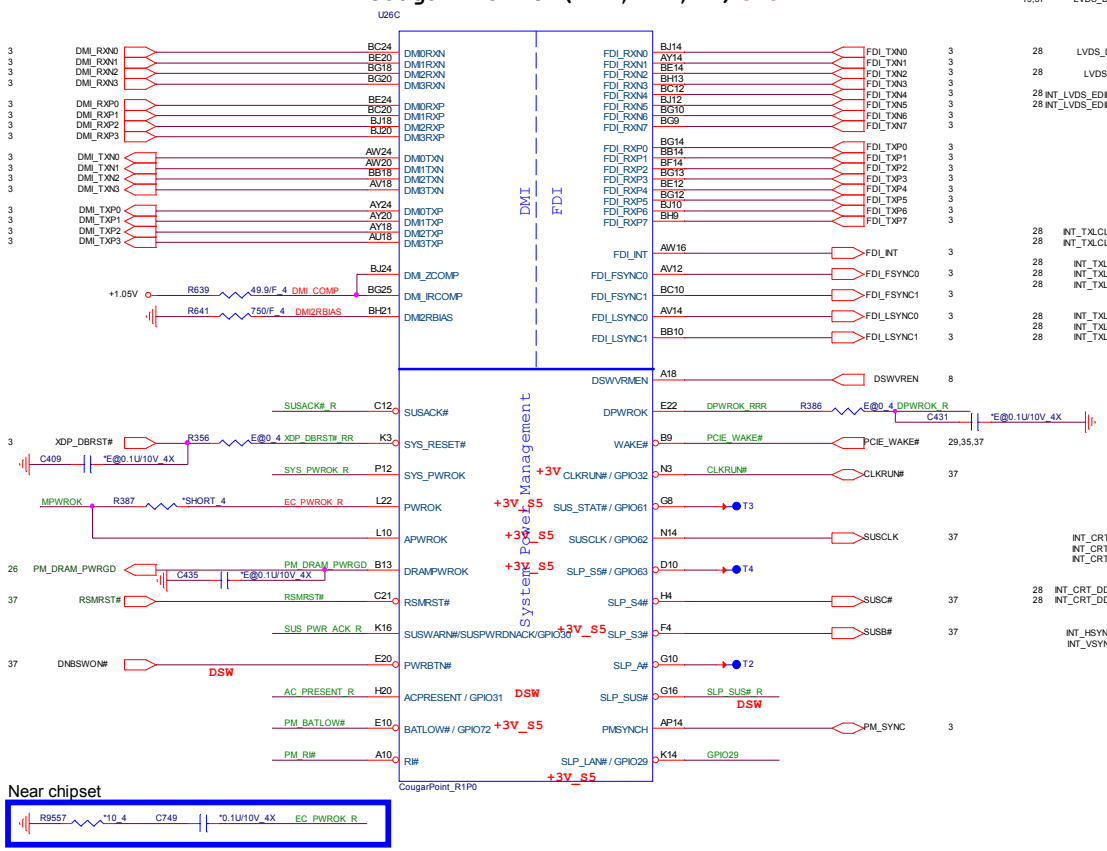
PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | Ivy Bridge 4/4 | A1A |
| Date: Friday, December 28, 2012 | Sheet 6 of 49 | |

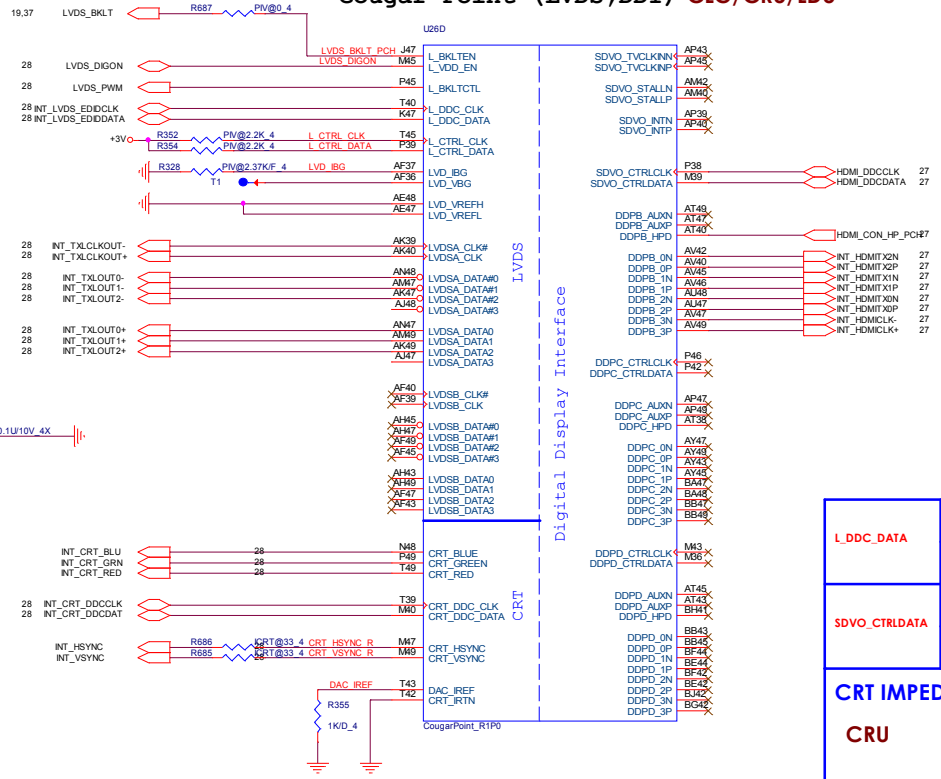
# Cougar Point (DMI,FDI,PM) CLG




Near chipset



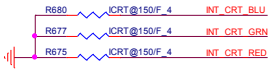

# Cougar Point (LVDS,DDI) CLG/CRU/LDU



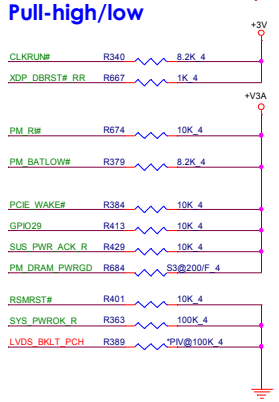

| | |
|---|---|
| L_DDC_DATA | 1 -- LVDS ENABLE |
| | 0 -- LVDS DISABLE |
| SDVO_CTRLDATA | 1 -- PORT B Detected |
| | 0 -- PORT B Disable |

## CRT IMPEDANCE MATCHING

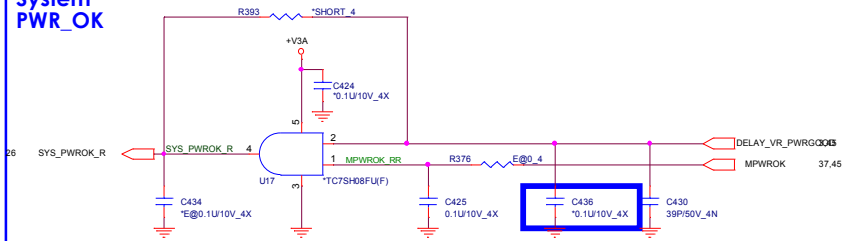
## CRU



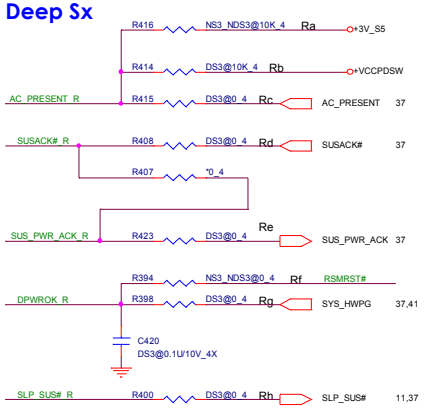

## PCH Pull-high/low CLG/PIV/S3P




## System PWR_OK




## Deep Sx




| Net Name | Deep Sx Support | Deep Sx No Support |
|---|---|---|
| AC_PRESENT | Rb,Rc stuff | Ra stuff |
| SUS_PWR_ACK | Re stuff | Re stuff |
| SUSACK#_R | Rd stuff | |
| DPWROK | Rg stuff | Rf stuff |
| SLP_SUS | Rh stuff | Rh No stuff |

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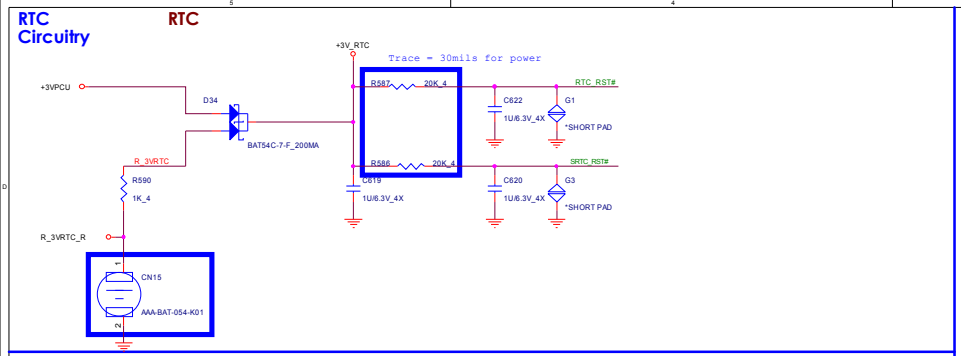
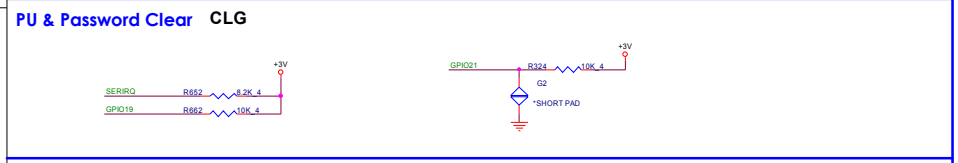
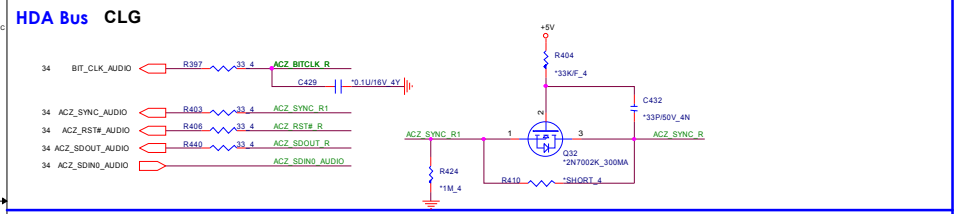
PROJECT : MTC_MTCD

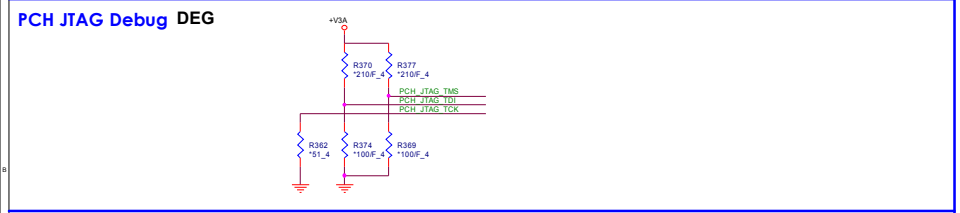
| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 1/6 | A1A |

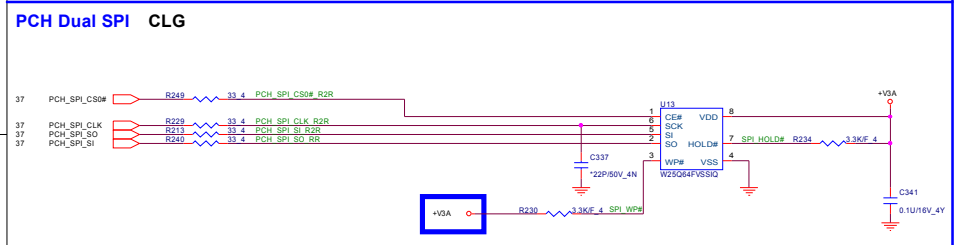
Date: Friday, December 28, 2012 Sheet 7 of 49

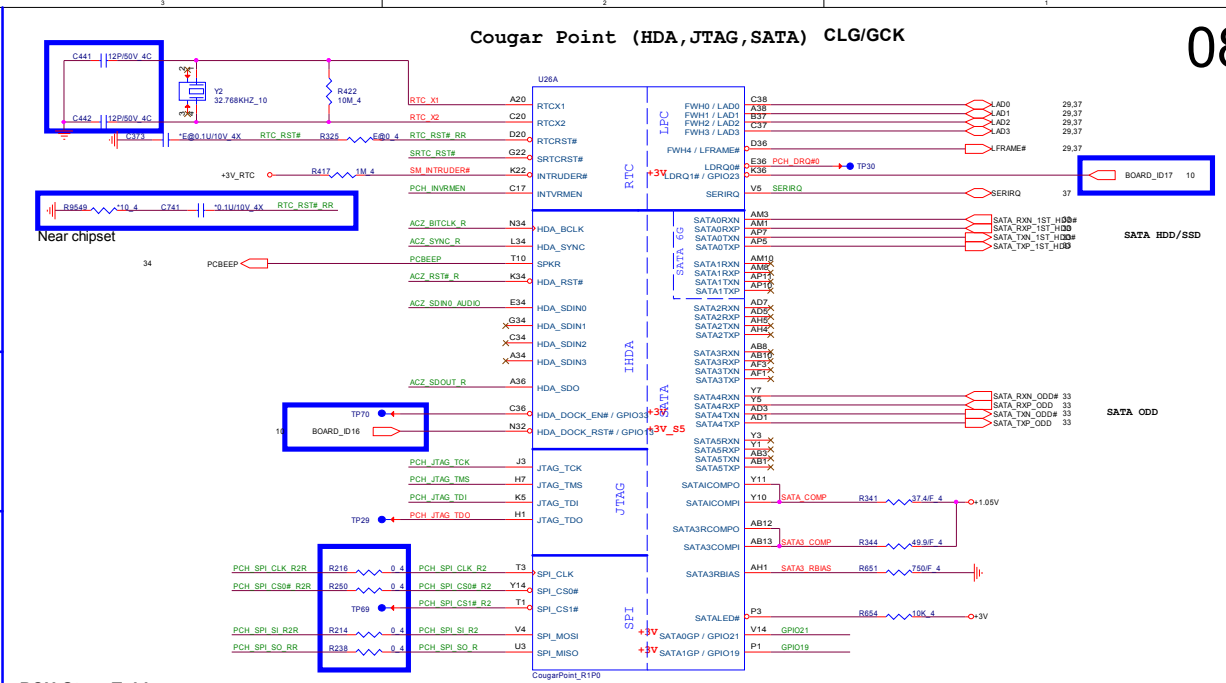


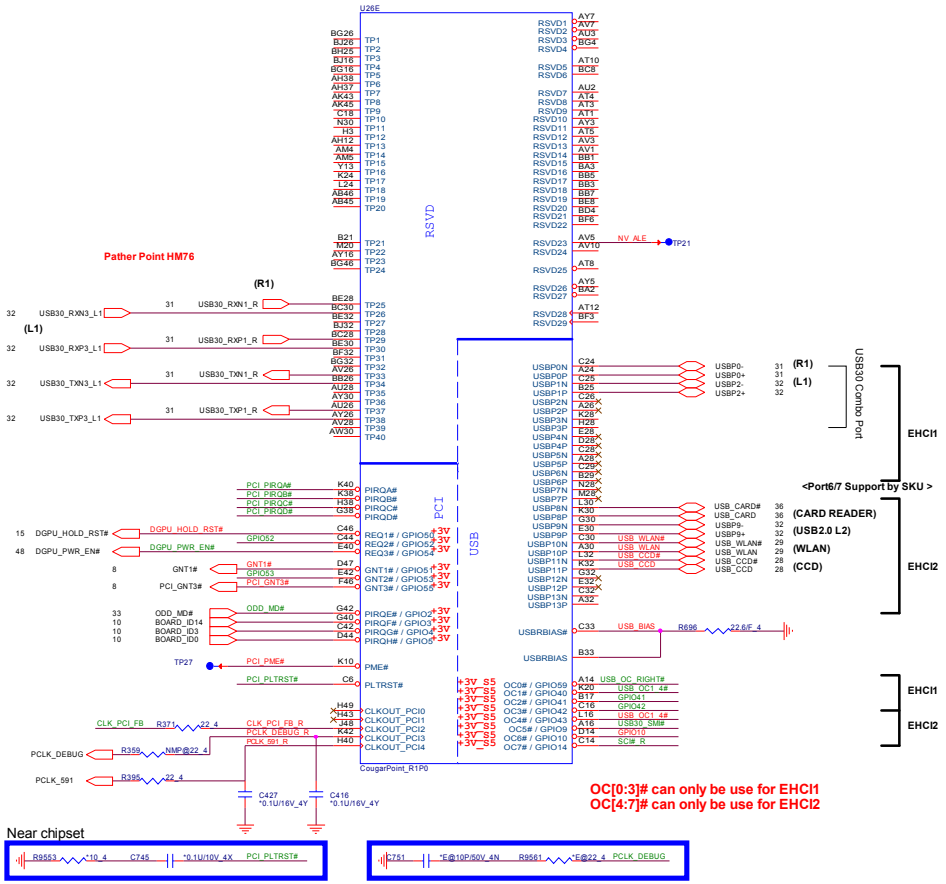

## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration |
|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI ★; 0 / 0 / LPC |
| GPIO19 | Boot BIOS Selection 0 [bit-0] | PWROK | |
| HDA_SDO | Flash Descriptor Security | RSMRST | 0 = Override<br>1 = Default (weak pull-up 20K) |
| DF_TVS | DMI/FDI Termination voltage | PWROK | **0 = Set to Vss**<br>**1 = Set to Vcc (weak pull-down 20K)** |
| GPIO28 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | **0 = Support by 1.8V (weak pull-down)**<br>**1= Support by 1.5V** |
| INIT3_3V# | Reserved | PWROK | 1 = Default (weak pull-up 20K) |
| GNT2#/ GPIO53 | ESI Strap (Server Only) | PWROK | 1 = Default. Should not be pulled low for desktop and mobile |
| GPIO15 | TLS Confidentiality | RSMRST | 0 = Default. TLS no Confidentiality<br>1 = TLS Confidentiality |
| L_DDC_DATA | LVDS Detected | PWROK | 0 = Default. Not Detected<br>1 = Detected |
| SDVO_CTRLDATA | Port B Detected | PWROK | 0 = Default. Not Detected<br>1 = Detected |
| DDPC_CTRLDATA | Port C Detected | PWROK | 0 = Default. Not Detected<br>1 = Detected |
| DDPD_CTRLDATA | Port D Detected | PWROK | 0 = Default. Not Detected<br>1 = Detected |
| SATA3GP/ GPIO37 | Reserved | PWROK | 0 = Default |
| SATA2GP/ GPIO36 | Reserved | PWROK | 0 = Default |
| DSWVRMEN | Deep S4/S5 Well On -Die Voltage Regulator Enable | ALWAYS | 0 = Disable<br>1 = Enable |

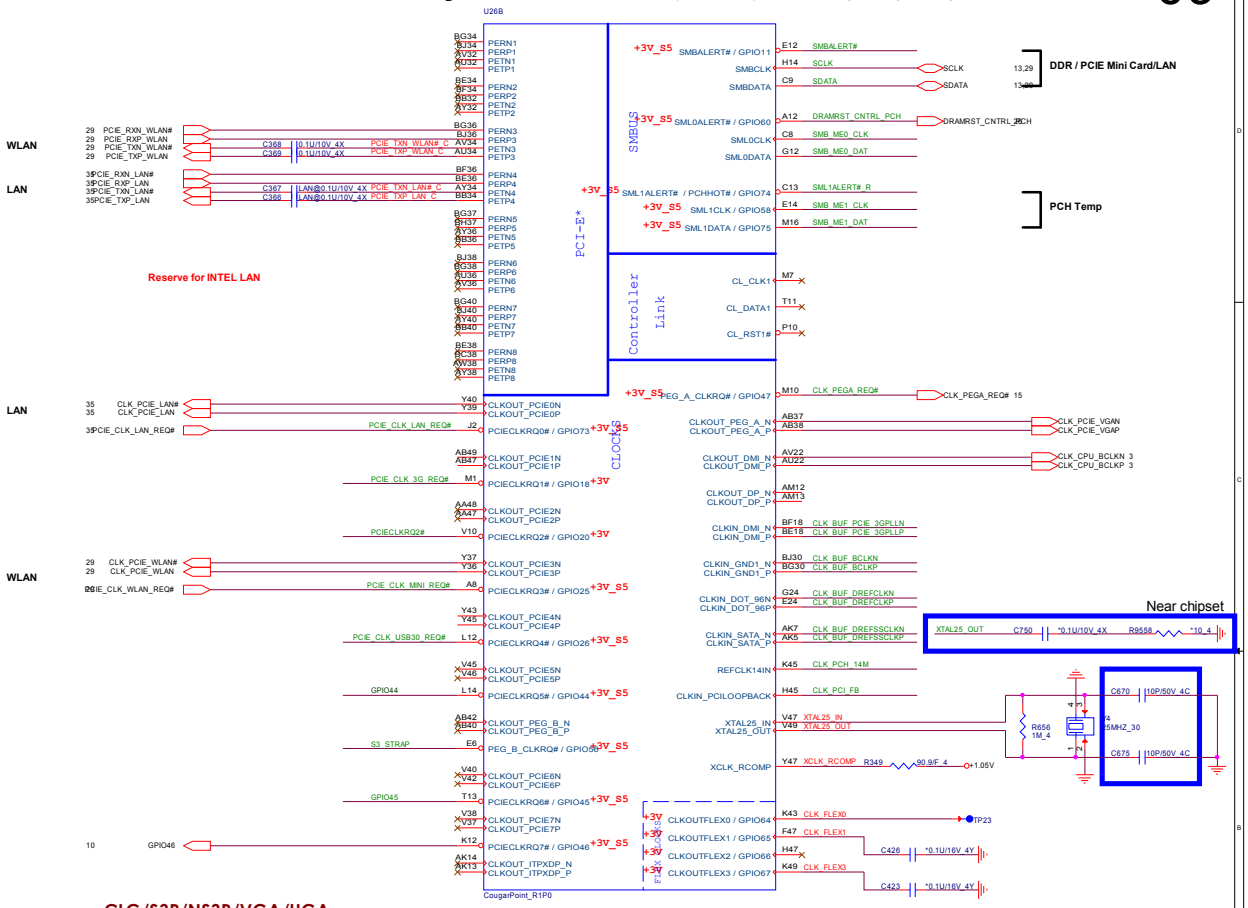
| | | |
|---|---|---|
| | | 1= PU to 3V |
| | | 1= PU to 3V |
| | | 0=NC |
| | | 0=NC |
| | | **Should not be pulled high when strap is sampled** |
| | | **Should not be pulled high when strap is sampled** |
| | | +3V_RTC R452 330K_4 DSWVREN 7 R456 *330K_4 |

Quanta Computer Inc.
PROJECT : MTC_MTCD
Size: Document Number: Cougar Point 2/6 Rev: A1A
Date: Friday, December 28, 2012 Sheet 8 of 49

# Cougar Point-M (PCI,USB,NVRAM) CLG/DEG

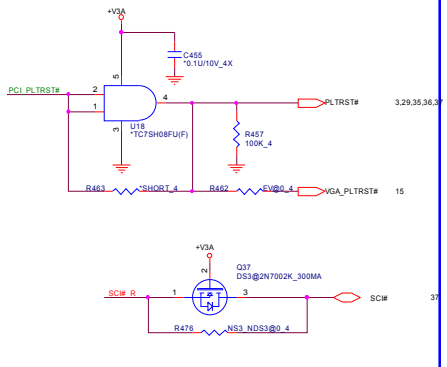



# Cougar Point-M (PCI-E,SMBUS,CLK)CLG/GCK/MNG/U3C

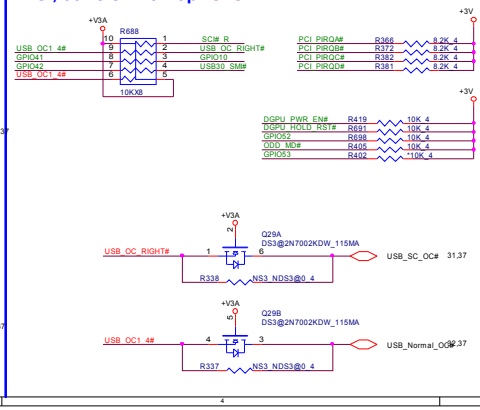



# CLG/S3P/NS3P/VGA/UGA

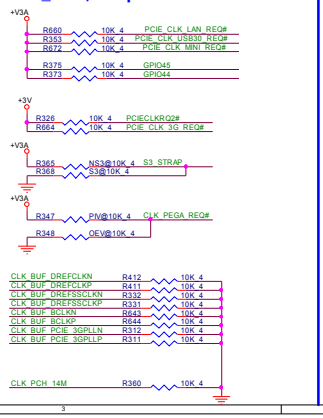
## PLTRST# CLG



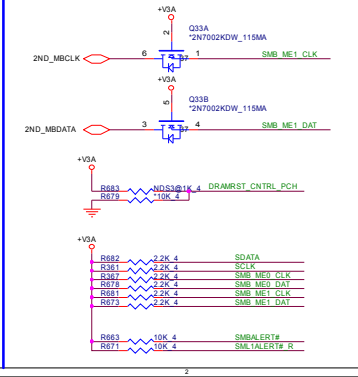
## PCI/USBOC# Pull-up CLG



## CLK_REQ/Strap Pin



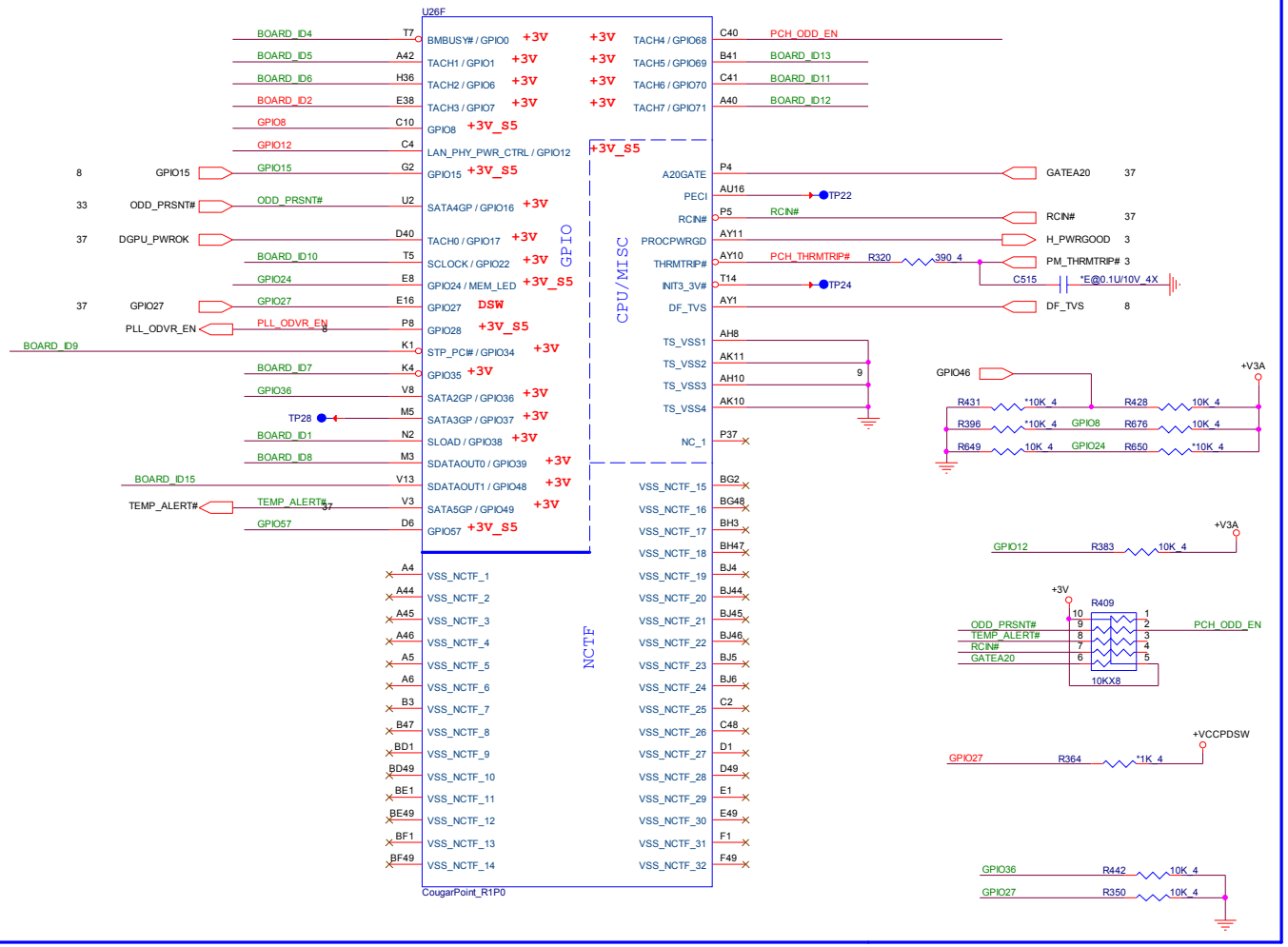
## SMBus/Pull-up CLG



| | 33MHz | 27MHz | 48/24MHz | 14.318MHz | 25MHz |
|---|---|---|---|---|---|
| CLK_FLEX0 | ● | ● | ● | ● | |
| CLK_FLEX1 | | ● | ● | ● | |
| CLK_FLEX2 | ● | ● | ● | ● | ● |
| CLK_FLEX3 | | ● | ● | ● | |

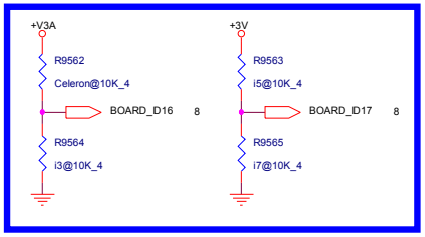
Quanta Computer Inc.
PROJECT : MTC_MTCD
Size: Document Number: Cougar Point 3/6 Rev: A1A
Date: Friday, December 28, 2012 Sheet 9 of 49

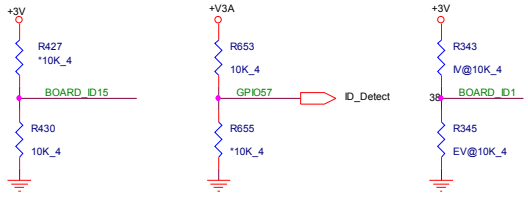
# Cougar Point (GPIO,VSS_NCTF,RSVD) CLG

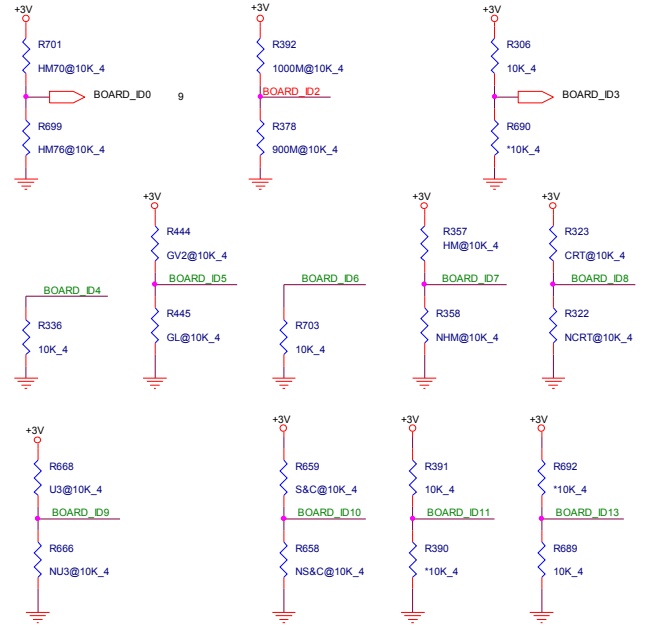



## BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

| Board ID | ID0 | ID1 | ID2 | ID3 | ID4 | ID5 | ID6 | ID7 | ID8 | ID12 | ID13 | ID14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HM70<br>HM76 | H<br>L | | | | | | | | | | | |
| UMA SKU<br>VGA SKU | | H<br>L | | | | | | | | | | |
| VRAM-1000MHz<br>VRAM-900MHz | | | H<br>L | | | | | | | | | |
| CF SV<br>CF ULT | | | | H<br>L | | | | | | | | |
| 17"<br>14" | | | | | H<br>L | | | | | | | |
| GV2<br>GL | | | | | | H<br>L | | | | | | |
| W/ G-sensor<br>W/O G-sensor | | | | | | | H<br>L | | | | | |
| W/ HDMI<br>W/O HDMI | | | | | | | | H<br>L | | | | |
| w CRT<br>wo CRT | | | | | | | | | H<br>L | | | |
| Only VGA<br>Optimus | | | | | | | | | | H<br>L | | |
| Win7(Reserve)<br>Win8(Reserve) | | | | | | | | | | | H<br>L | |
| HM70_76<br>NM70 | | | | | | | | | | | | H<br>L |




| | Description | ID9 | ID10 | ID11 |
|---|---|---|---|---|
| ~~NU3@/NSC@/NUR@~~ | ~~ULU-2 and W/O R-USB Port~~ | ~~L~~ | ~~L~~ | ~~L~~ |
| NU3@/NSC@/UR@ | ULU-2 and W/O S&C UR-2 | L | L | H |
| U3@/NSC@/UR@ | ULU-2 and W/O S&C UR-3 | H | L | H |
| ~~NU3@/SC@/UR@~~ | ~~ULU-2 and W/S&C UR-2~~ | ~~L~~ | ~~H~~ | ~~H~~ |
| U3@/SC@/UR@ | ULU-2 and W/S&C UR-3 | H | H | H |

| | U3@ | S&C@ | UR@ |
|---|---|---|---|
| | NU3@ | NS&C@ | NUR@ |

| Board ID 16 | default |
|---|---|
| Celeron CPU | H |
| i3 CPU | L |

| Board ID 17 | default |
|---|---|
| i5 CPU | H |
| i7 CPU | L |

| BOARD_ID15 | default |
|---|---|
| EDP | H |
| LVDS | L |

| ID_Detect | default |
|---|---|
| Metal/IMR | H |
| TEXTURE | L |

Quanta Computer Inc.

PROJECT : MTC_MTCD

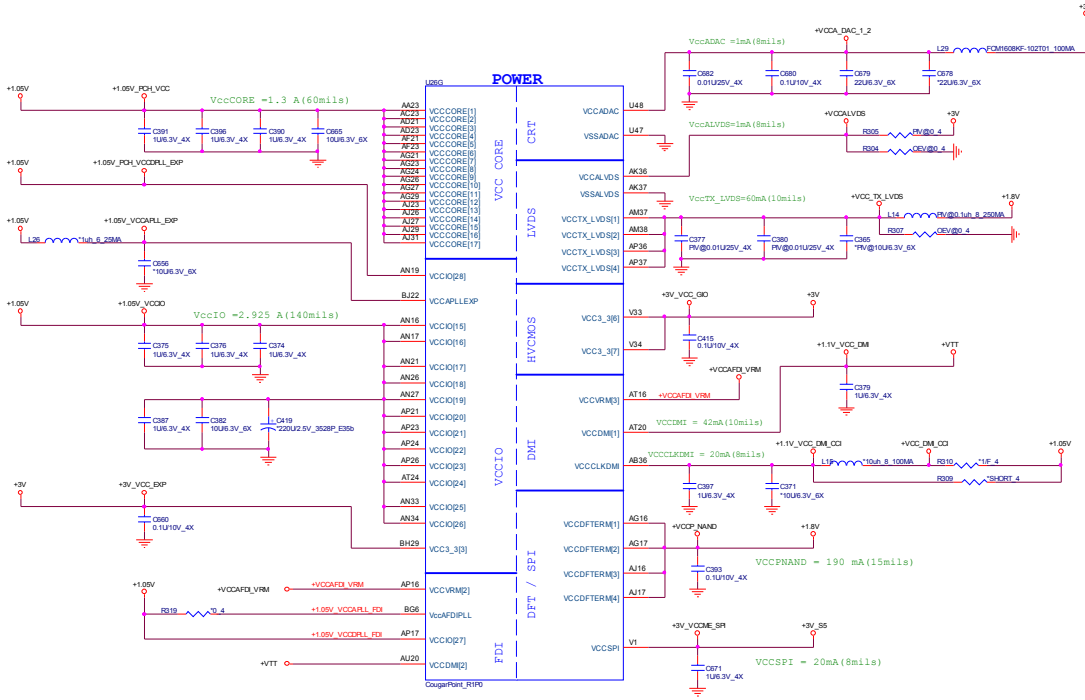
| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 4/6 | A1A |
| Date: Friday, December 28, 2012 | Sheet 10 of 49 | |

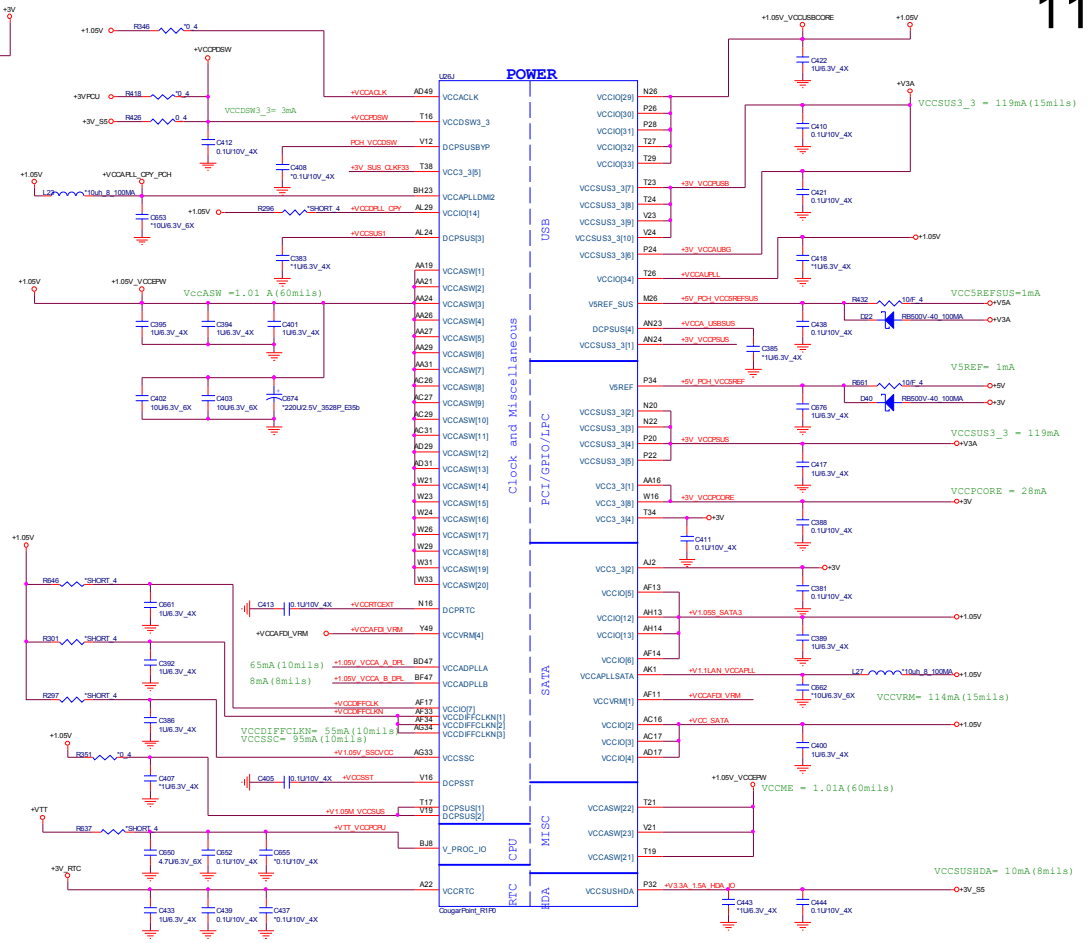
# COUGAR POINT (POWER) CLG

CLG/PIV/OEV

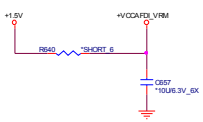
CLG

CLG

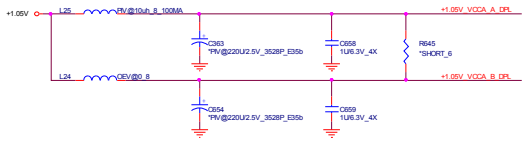


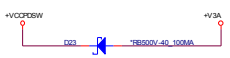

## Internal PLL and VRMS CLG



## Display PLL A/B Analog Power CLG/PIV/OEV

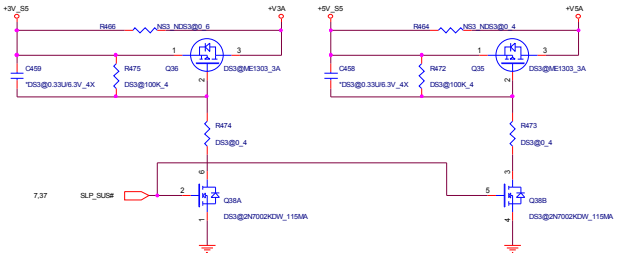


## Deep Sx power well CLG



## Clock power on core well CLG

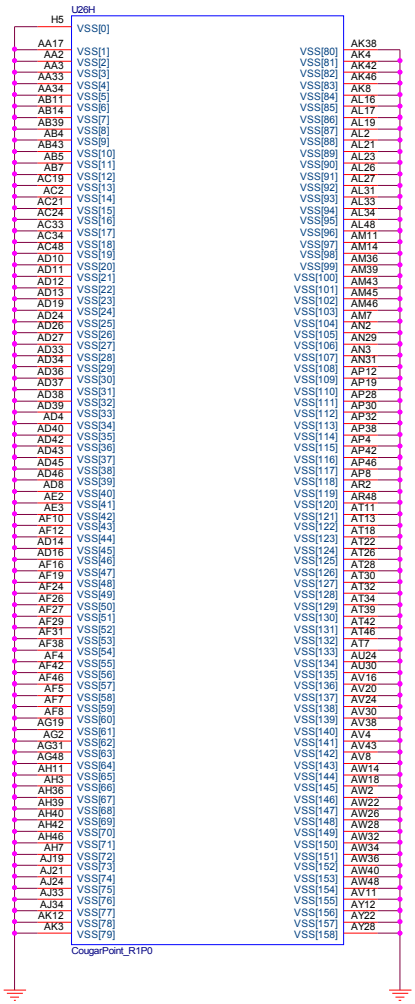


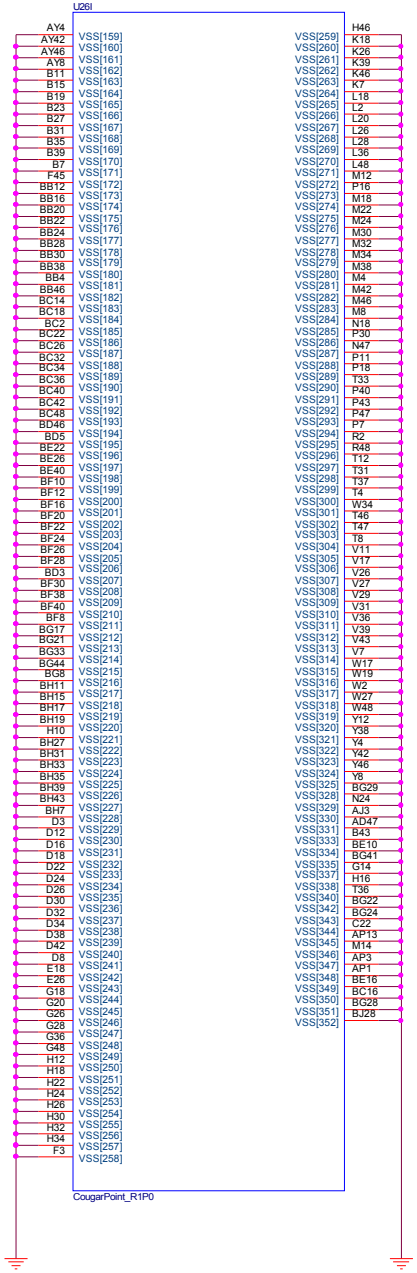



Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | Cougar Point 5/6 | A1A |
| Date: Friday, December 28, 2012 | Sheet 11 of 49 | |

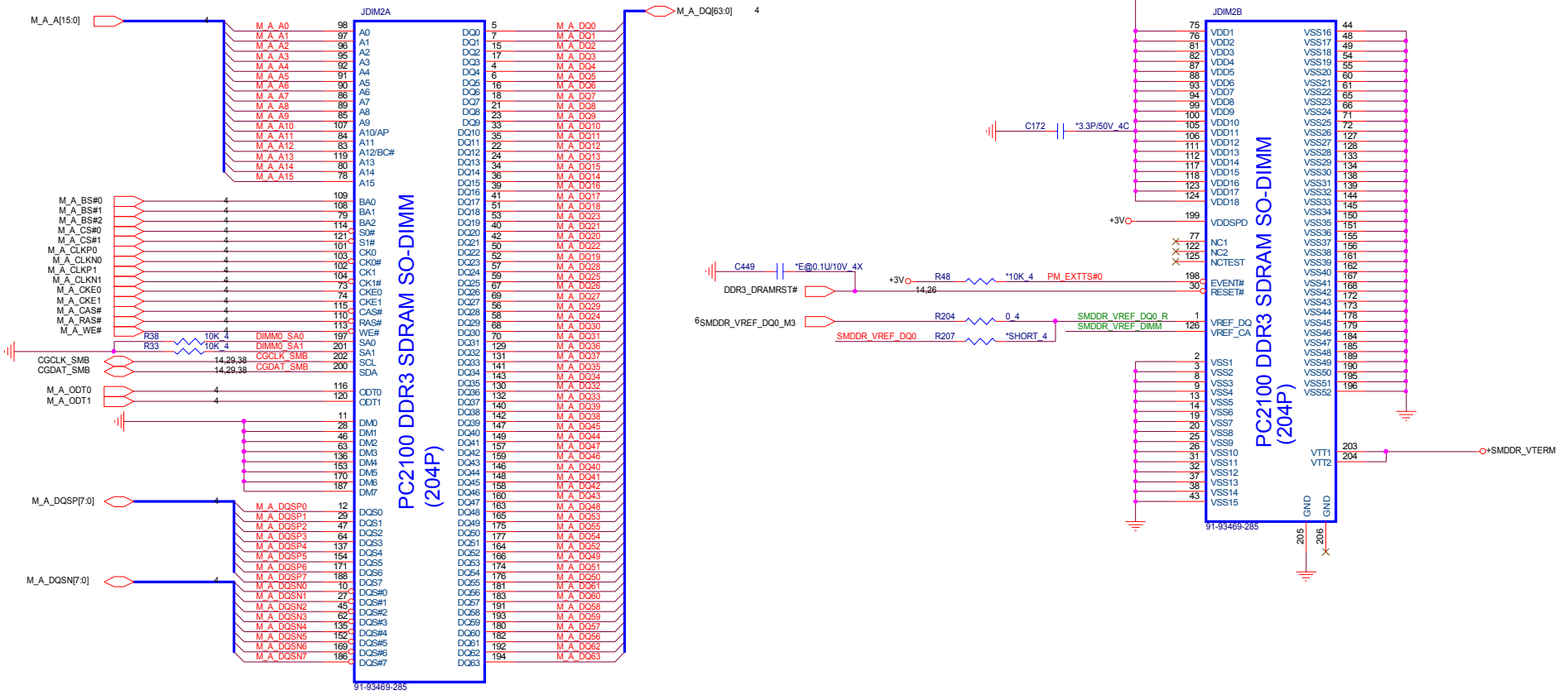


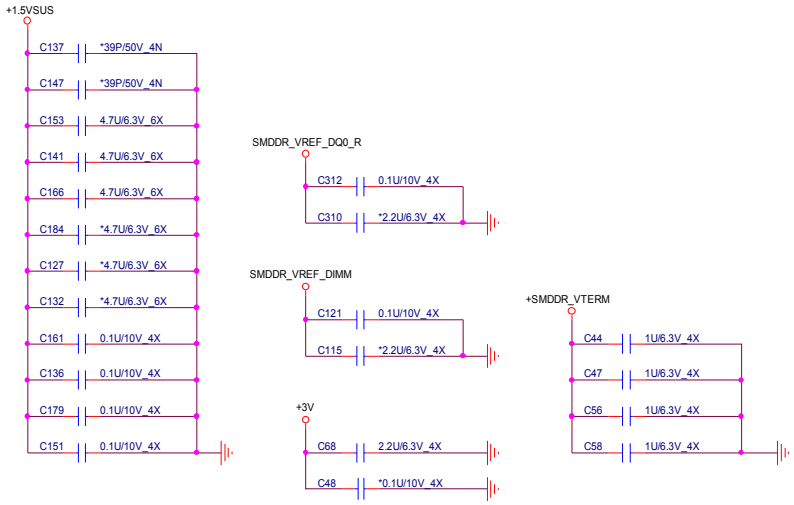

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : MTC_MTCD | | |
| Size | Document Number: Cougar Point 6/6 | Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 12 of 49 | |

# DDR

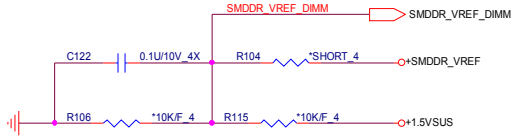
H=8 (Rev)



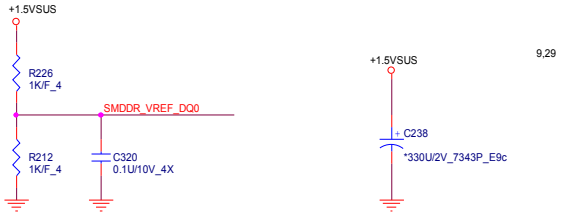

## DDR Power Decoupling DDR



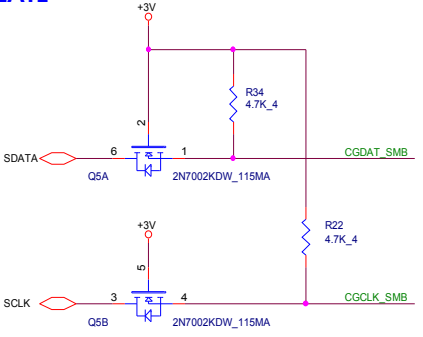

## DDR3 VREF CA DDR




## DDR3 VREF DQ (M1) DDR




## SMBUS ISOLATE DDR



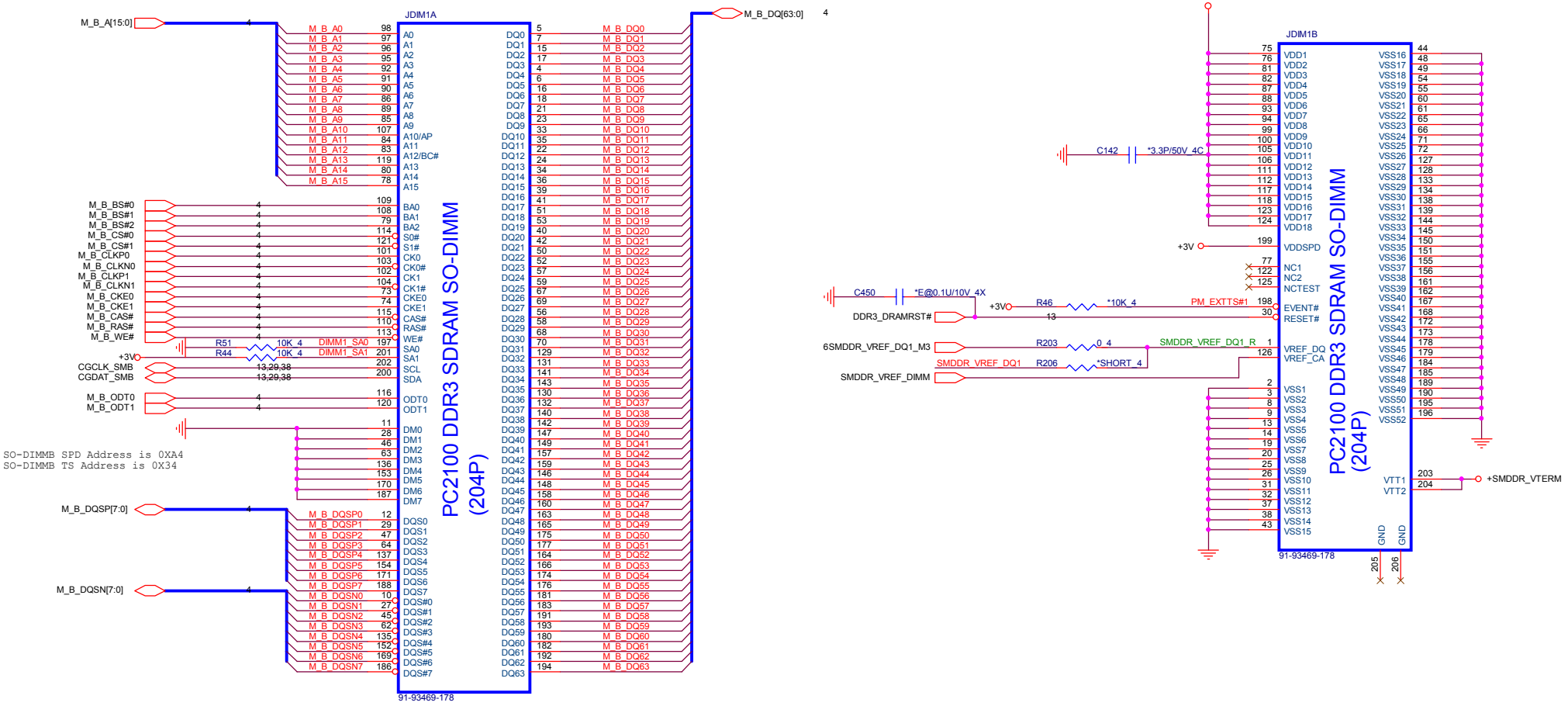

Quanta Computer Inc.

PROJECT : MTC_MTCD

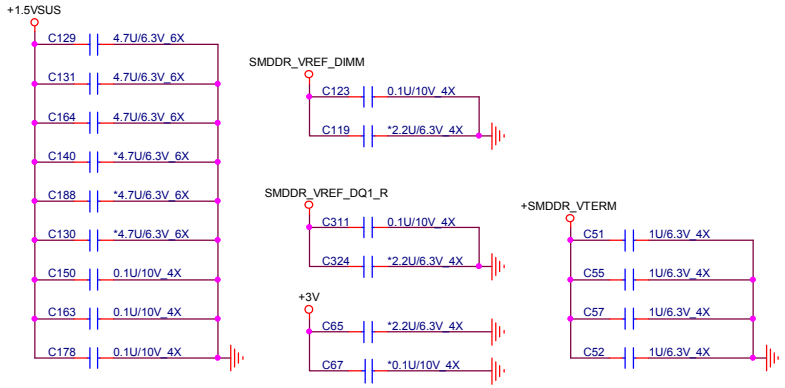
| Size | Document Number | Rev |
|---|---|---|
| | DDR3 DIMM-0 | A1A |

Date: Friday, December 28, 2012 Sheet 13 of 49

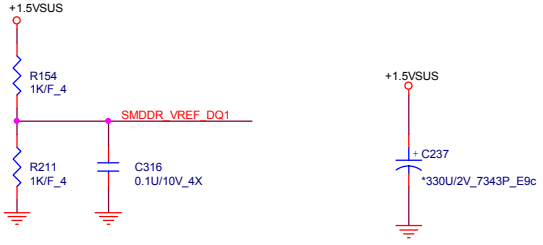
H=4 (Rev)




## DDR Power Decoupling DDR



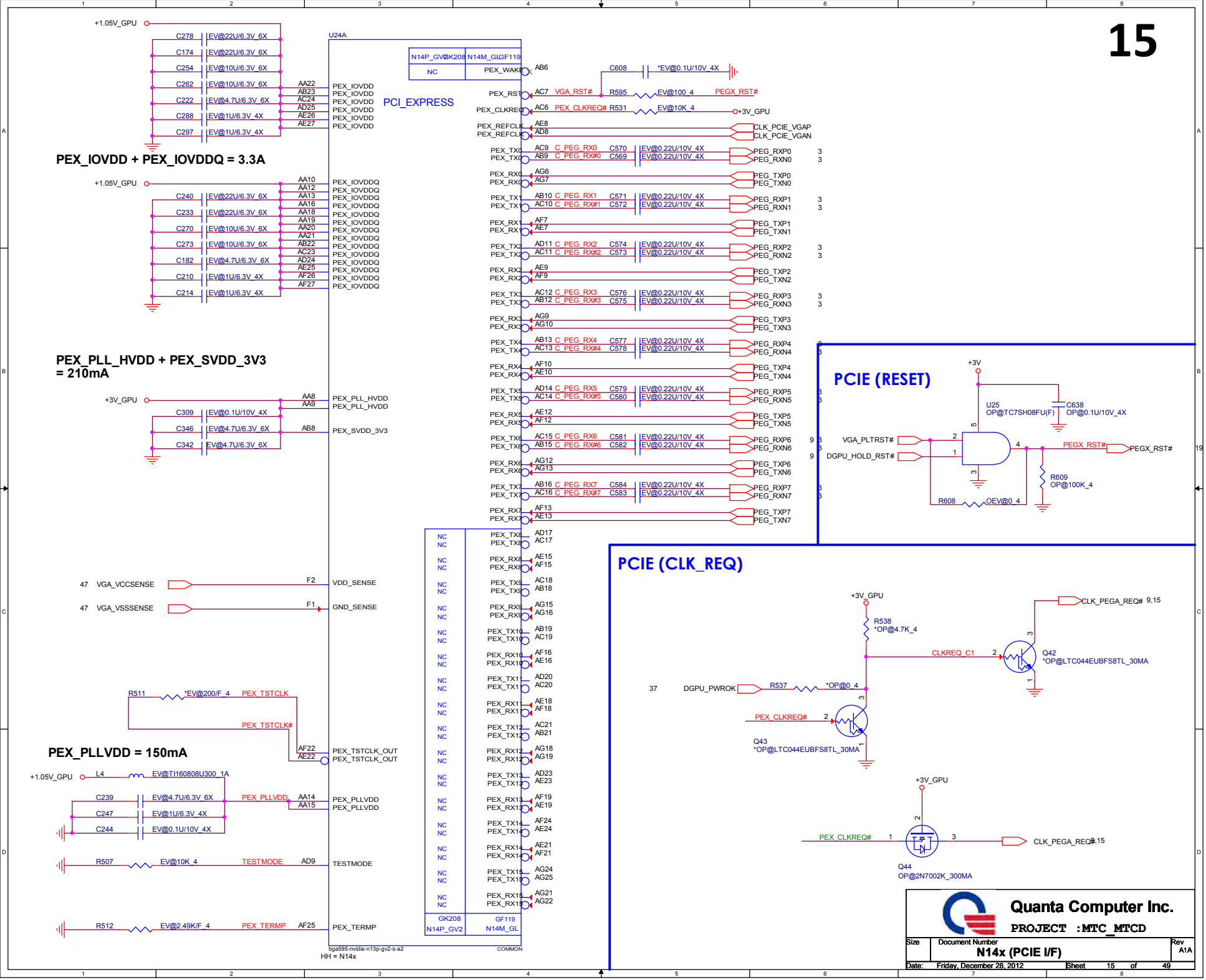

## DDR3 VREF DQ (M1) DDR




Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | DDR3 DIMM-1 | A1A |
| Date: Friday, December 28, 2012 | Sheet 14 of 49 | |


PEX_IOVDD + PEX_IOVDDQ = 3.3A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 210mA
PEX_PLLVDD = 150mA
PCI_EXPRESS
U24A
PCIE (RESET)
PCIE (CLK_REQ)
Quanta Computer Inc.
PROJECT : MTC_MTCD
N14x (PCIE I/F)
Friday, December 28, 2012
Sheet 15 of 49

FBA

DUAL RANK (Mode E)

FBVDDQ + FBVDD = 4.88A

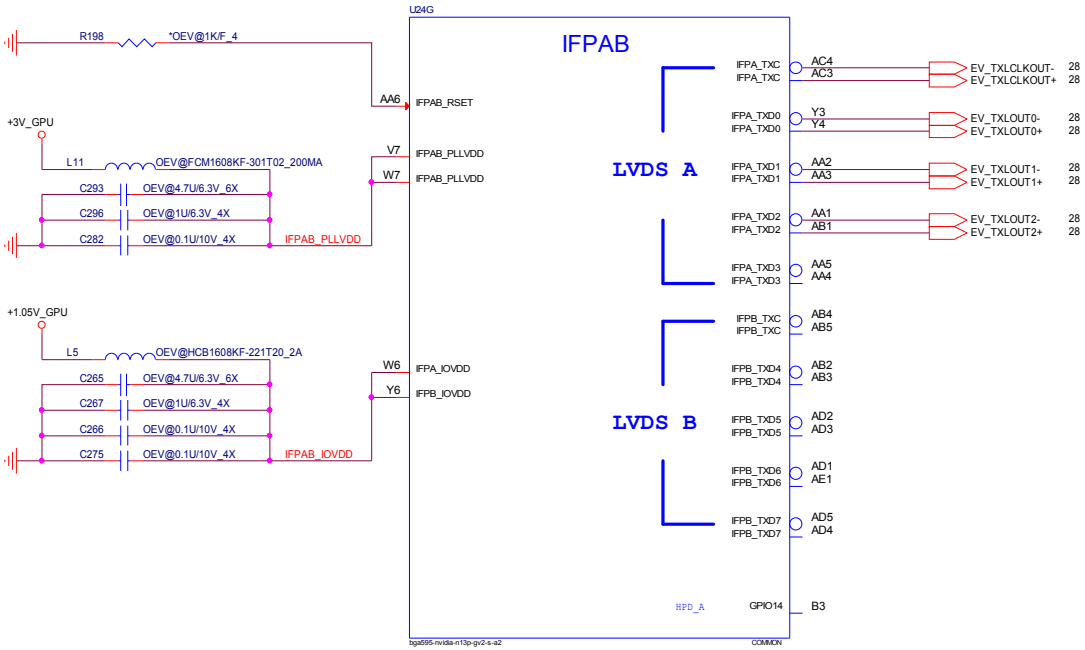
ODTx, CKEx,RST (Termination)

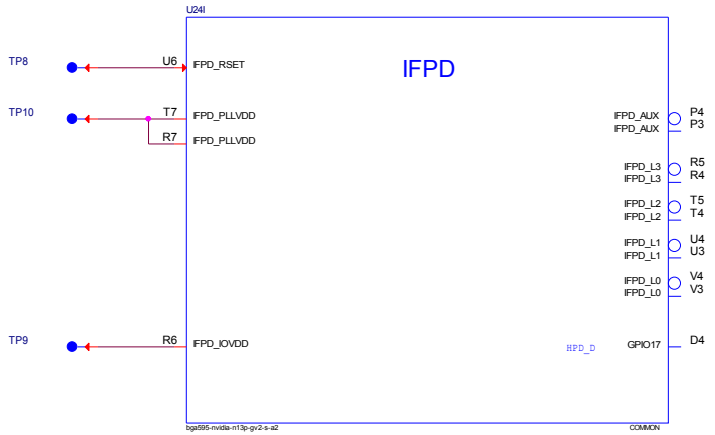
Check PUN for Fianl Value on M.P

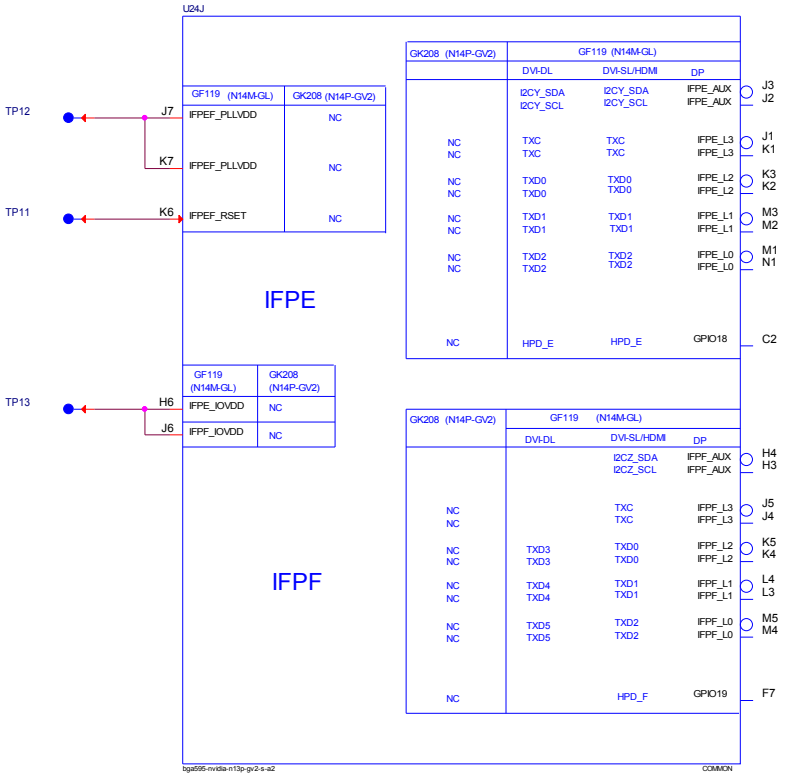
FB_PLLAVDD = 62mA

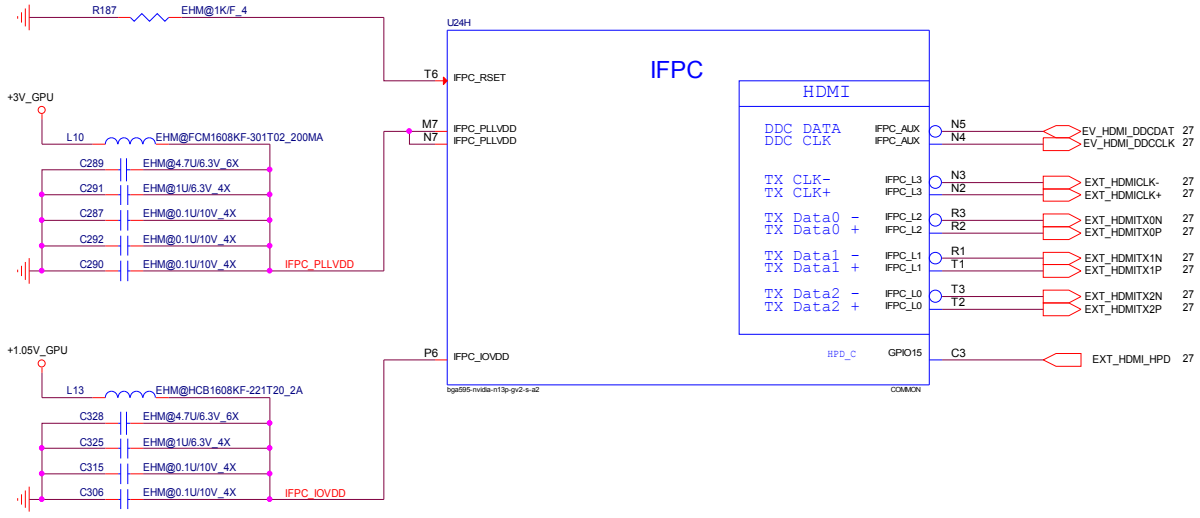
FB_DLLAVDD = 35mA

| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : MTC_MTCD | |
| Size | Document Number: N14x (Memory I/F) — Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 16 of 49 |

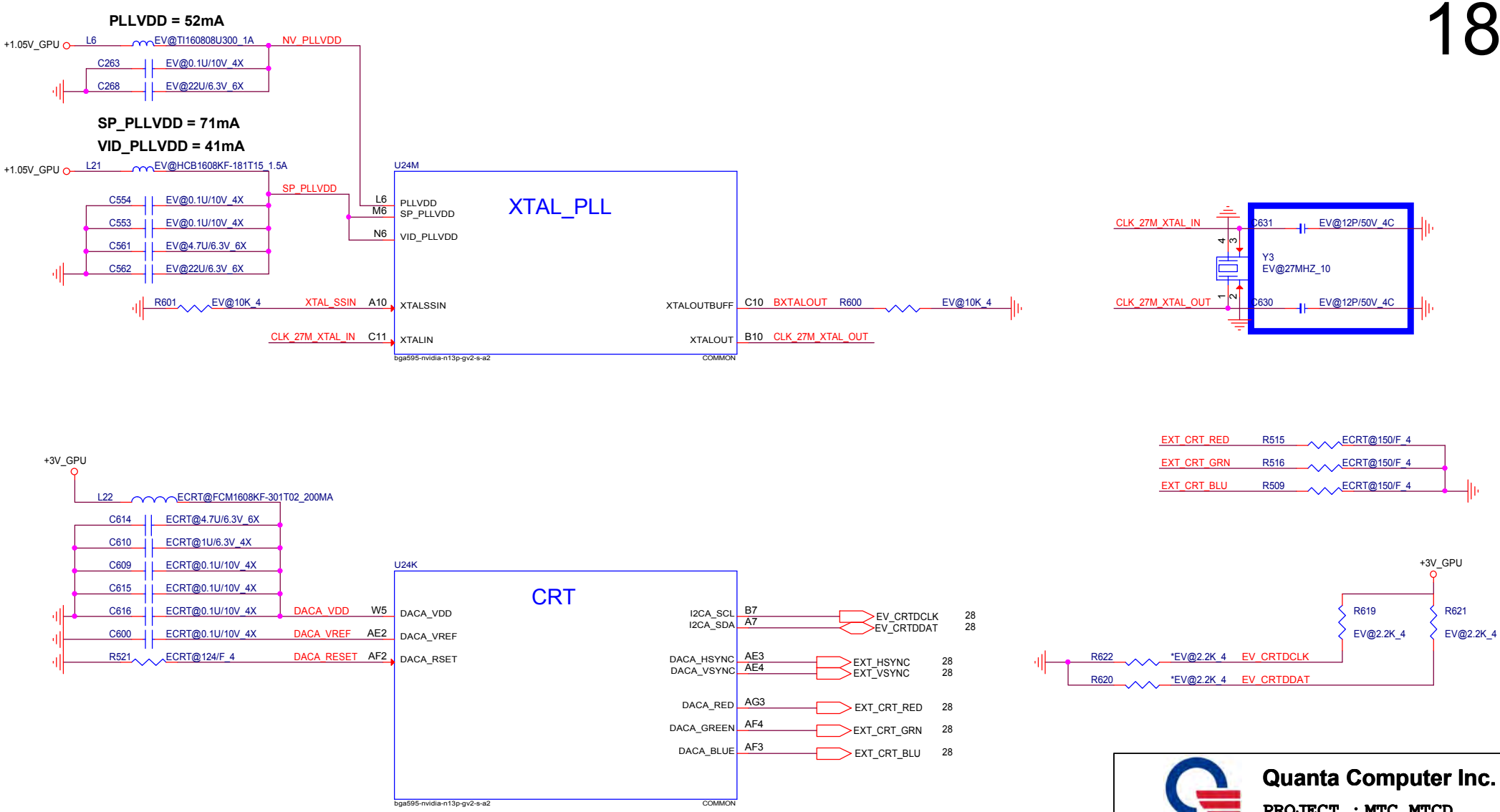


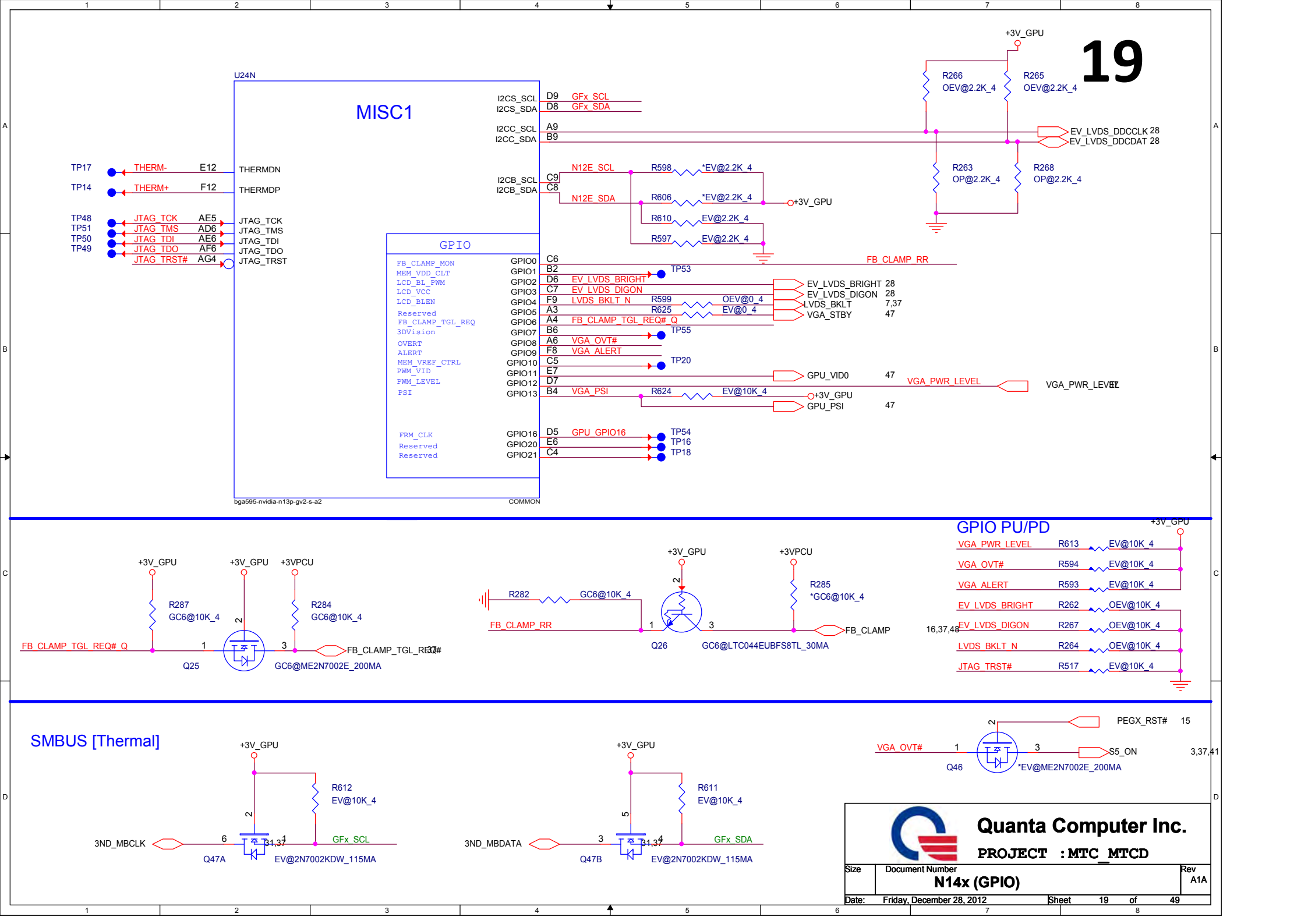



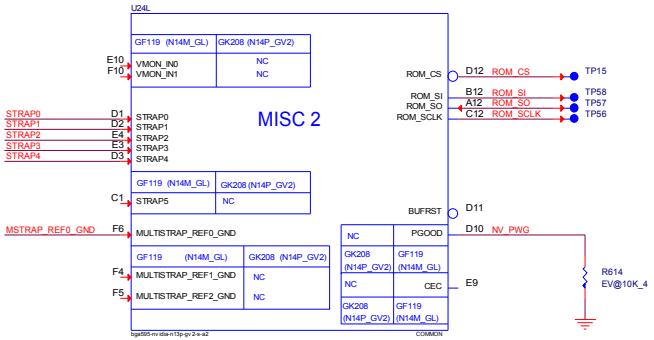




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : MTC_MTCD | | |
| Size | Document Number: N14x (Display I/F) | Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 17 of 49 | |




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : MTC_MTCD | | |
| Size | Document Number: N14x (XTAL/CRT I/F) | Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 18 of 49 | |


19
MISC1
U24N
GPIO
THERM-
THERM+
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
GFx_SCL
GFx_SDA
N12E_SCL
N12E_SDA
+3V_GPU
EV_LVDS_DDCCLK 28
EV_LVDS_DDCDAT 28
FB_CLAMP_RR
EV_LVDS_BRIGHT
EV_LVDS_DIGON
LVDS_BKLT_N
VGA_STBY
VGA_OVT#
VGA_ALERT
VGA_PSI
FB_CLAMP_TGL_REQ# Q
GPU_GPIO16
GPU_VID0
GPU_PSI
VGA_PWR_LEVEL
FB_CLAMP_MON
MEM_VDD_CLT
LCD_BL_PWM
LCD_VCC
LCD_BLEN
Reserved
FB_CLAMP_TGL_REQ
3DVision
OVERT
ALERT
MEM_VREF_CTRL
PWM_VID
PWM_LEVEL
PSI
FRM_CLK
Reserved
Reserved
bga595-nvidia-n13p-gv2-s-a2
COMMON
GPIO PU/PD
SMBUS [Thermal]
3ND_MBCLK
3ND_MBDATA
Q25
Q26
Q46
Q47A
Q47B
GC6@ME2N7002E_200MA
GC6@LTC044EUBFS8TL_30MA
EV@2N7002KDW_115MA
*EV@ME2N7002E_200MA
PEGX_RST#
S5_ON
Quanta Computer Inc.
PROJECT : MTC_MTCD
Size
Document Number
N14x (GPIO)
Rev
A1A
Date: Friday, December 28, 2012
Sheet 19 of 49




## MULT STRIP [N14P_GV2]

| | | | |
|---|---|---|---|
| **PCI_DEVID STRAP** | PCI DEVICE ID 0x1292 -->QS 0x12AD -->ES | **DP_PLL_VDD33** | 1 [Default] |
| **RAM_CFG** | RAM_CFG[3:0] for memory configuration | **PEX_PLL_EN_TERM** | PCIE PLL termination 0:Disable [Default] ; 1:Enable |
| **SUB_VENDOR** | 0:No VBIOS ROM ; 1 BIOS ROM [Default] | **3GIO_PADCFG** | [0000] --> Gen3 support |
| **FB[1:0]** | [1:0] --> 256MB | **PCIE_MAX_SPEED** | [1] -->Allow boot to PCIE Gen3 |
| **VGA_DEVICE** | 0:3D Device ; 1:VGA Device | **PCIE_SPEED_CHANG_ GEN3** | [1] -->Enable Gen3 |
| **SMB_ALT_ADDR [Slave address]** | 0:9E [Default] ; 1:9C | **SORx_EXPOSED** | SOR0_EXP=0,SOR1_EXP=1 [IFPA/B:LVDS] ; [IFPC:HDMI] |
| **USER STRAP** | Panel EDID Support [0X1111] | | |

| Strap Pin name | Strapping Bits 3 | Strapping Bits 2 | Strapping Bits 1 | Strapping Bits 0 | SETTING | NOTE |
|---|---|---|---|---|---|---|
| ROM_SCLK | PCI_DEVID[4] | SUB_VENDER | PCI_DEVID[5] | PEX_PLL_EN_TERM | ROM_SCLK +3V_GPU R626 GV2@4.99K/F_4 R602 *GV2@15K/F_4 | |
| ROM_SI | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] | ROM_SI +3V_GPU R630 GV2@XXXX R617 GV2@XXXX | |
| ROM_SO | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE | ROM_SO +3V_GPU R9548 GV2_OEV@10K/F_4 +3V_GPU R628 GV2_OP@4.99K/F_4 R616 *GV2@15K/F_4 | |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | STRAP0 +3V_GPU R543 GV2@45.3K/F_4 R553 *GV2@15K/F_4 | |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | STRAP1 +3V_GPU R565 *GV2@15K/F_4 R566 GV2@45.3K/F_4 | |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | STRAP2 +3V_GPU R549 *GV2@15K/F_4 R558 GV2@15K/F_4 | |
| STRAP3 | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED | STRAP3 +3V_GPU R545 *GV2_OEV@15K/F_4 R555 GV2_OEV@24.9K/F_4 STRAP3 +3V_GPU R546 *GV2_OP@15K/F_4 R556 GV2_OP@4.99K/F_4 | |
| STRAP4 | RESERVED | PCIE_SPEED_CHANCE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V | STRAP4 +3V_GPU R580 *GV2@15K/F_4 R571 GV2@45.3K/F_4 | |

| | | | | | |
|---|---|---|---|---|---|
| 4.99K | 1000 | 0000 | 24.9K | 1100 | 0100 |
| 10K | 1001 | 0001 | 30.1K | 1101 | 0101 |
| 15K | 1010 | 0010 | 34.8K | 1110 | 0110 |
| 20K | 1011 | 0011 | 45.3K | 1111 | 0111 |
| Resistor Value | VDD33 | GND | Resistor Value | VDD33 | GND |

MSTRAP_REF0_GND R272 GV2@40.2K/F_4

## Binary Strap [N14M_GL]

| Strap Pin name | Strap Mapping | Polarity | SETTING |
|---|---|---|---|
| ROM_SCLK | SMB_ALT_ADDR | Pull-down to GND | ROM_SCLK +3V_GPU R615 *GL@10K/F_4 R603 GL@10K_4 |
| ROM_SI | SUB_VENDER | Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIO ROM | ROM_SI +3V_GPU R629 *GL@10K/F_4 R605 GL@10K_4 |
| ROM_SO | VGA_DEVICE | Pull-down to GND ( no dispaly ) | ROM_SO +3V_GPU R627 *GL@10K/F_4 R604 GL@10K_4 |
| STRAP0 | RAMCFG[0] | USER defined | STRAP0 +3V_GPU R544 GL@XXXX R554 GL@XXXX |
| STRAP1 | RAMCFG[1] | USER defined | STRAP1 +3V_GPU R568 GL@XXXX R569 GL@XXXX |
| STRAP2 | RAMCFG[2] | USER defined | STRAP2 +3V_GPU R548 GL@XXXX R559 GL@XXXX |
| STRAP3 | RAMCFG[3] | USER defined | STRAP3 +3V_GPU R547 GL@XXXX R557 GL@XXXX |
| STRAP4 | PCIE_MAX_SPEED | Pull-down to GND | STRAP4 R581 GL@10K_4 |

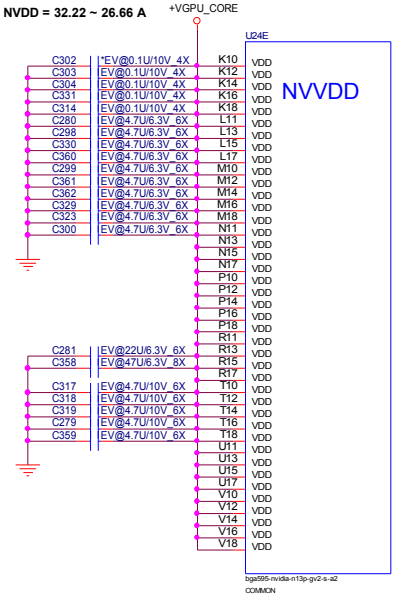
| | | Vendor P/N | STN B/S P/N | Size | Strap | | Note |
|---|---|---|---|---|---|---|---|
| 128M | Hynix | H5TQ2G63DFR-N0C (128M*16) GL/GV2 | | 128x4=1GB | GL:0x06 | GV2:0x06 | |
| | | | | 128x8=2GB | | GV2:0x06 | |
| | | H5TQ2G63DFR-11C (128M*16) GL/GV2 | | 128x4=1GB | GL:0x06 | GV2:0x06 | |
| | | | | 128x8=2GB | | GV2:0x06 | |
| | Samsung | K4W2G1646E-BC1A (128M*16) GL/GV2 | | 128x4=1GB | GL:0x05 | GV2:0x07 | |
| | | | | 128x8=2GB | | GV2:0x07 | |
| | | K4W2G1646E-BC11 (128M*16) GL/GV2 | | 128x4=1GB | GL:0x05 | GV2:0x07 | |
| | | | | 128x8=2GB | | GV2:0x07 | |
| | Micron | MT41J128M16JT-107G:K (128M*16) GL/GV2 | | 128x4=1GB | GL:0x01 | GV2:0x05 | |
| | | | | 128x8=2GB | | GV2:0x05 | |
| | | MT41J128M16JT-093G:K (128M*16) GL/GV2 | | 128x4=1GB | GL:0x01 | GV2:0x05 | |
| | | | | 128x8=2GB | | GV2:0x05 | |
| 256M | Micron | MT41K256M16HA-107G:E (256M*16) GL/GV2 | | 256x4=2GB | GL:0x0D | GV2:0x01 | |
| | | | | 256x8=4GB | | GV2:0x01 | |
| | Samsung | K4W4G1646B-HC11 (256M*16) GL/GV2 | | 256x4=2GB | GL:0x0B | GV2:0x03 | |
| | | | | 256x8=4GB | | GV2:0x03 | |
| | Hynix | H5TQ4G63MFR-11C (256M*16) GL | | 256x4=2GB | GL:0x03 | | |
| | | | | N/A | | | |
| | | H5TQ4G63AFR-11C (256M*16) GL | | 256x4=2GB | GL:0x04 | | |
| | | | | N/A | | | |

Quanta Computer Inc.
PROJECT : MTC_MTCD

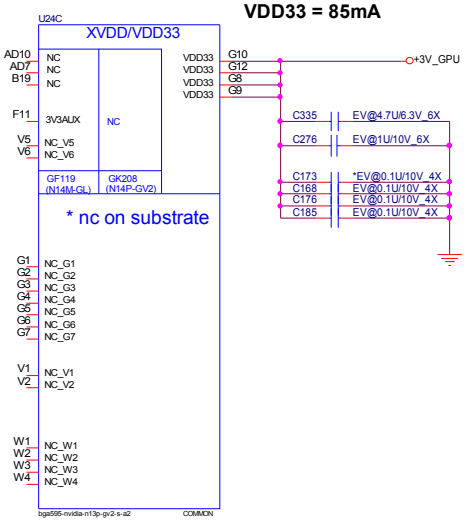
| Size | Document Number | Rev |
|---|---|---|
| | MSIC & STRAP | A1A |

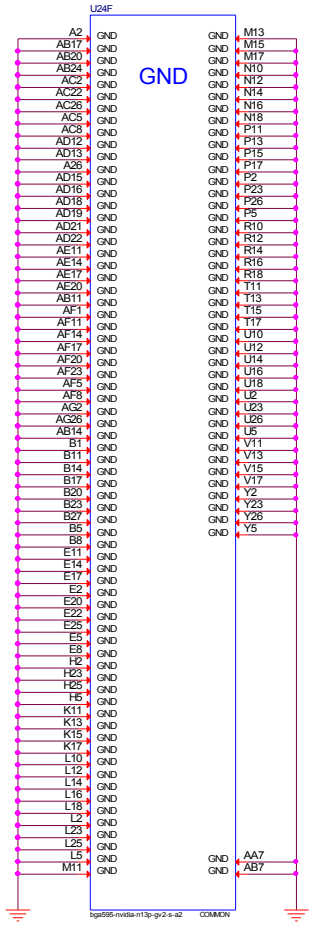
Date: Friday, December 28, 2012 Sheet 20 of 49

NVDD = 32.22 ~ 26.66 A



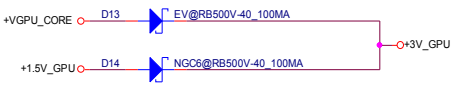

VDD33 = 85mA

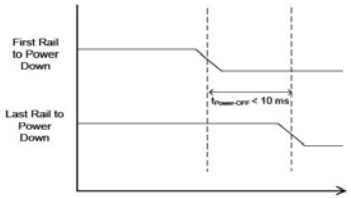


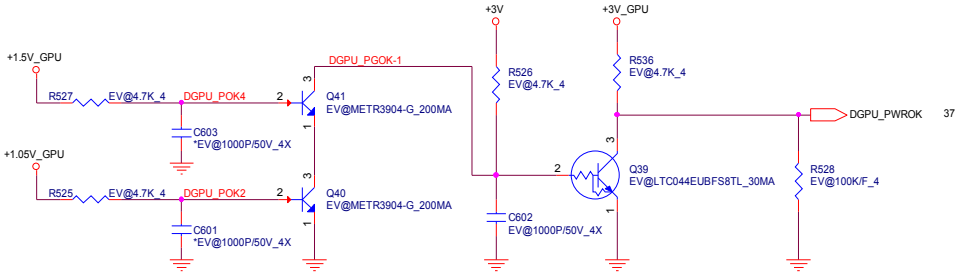




## Power down sequence

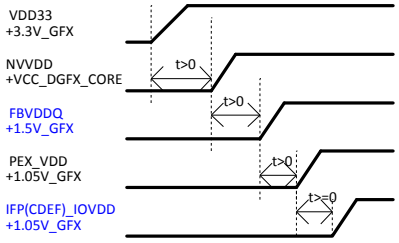
for meet Power down sequence for +3V_GFX




## Power up sequence




Quanta Computer Inc.

PROJECT : MTC_MTCD

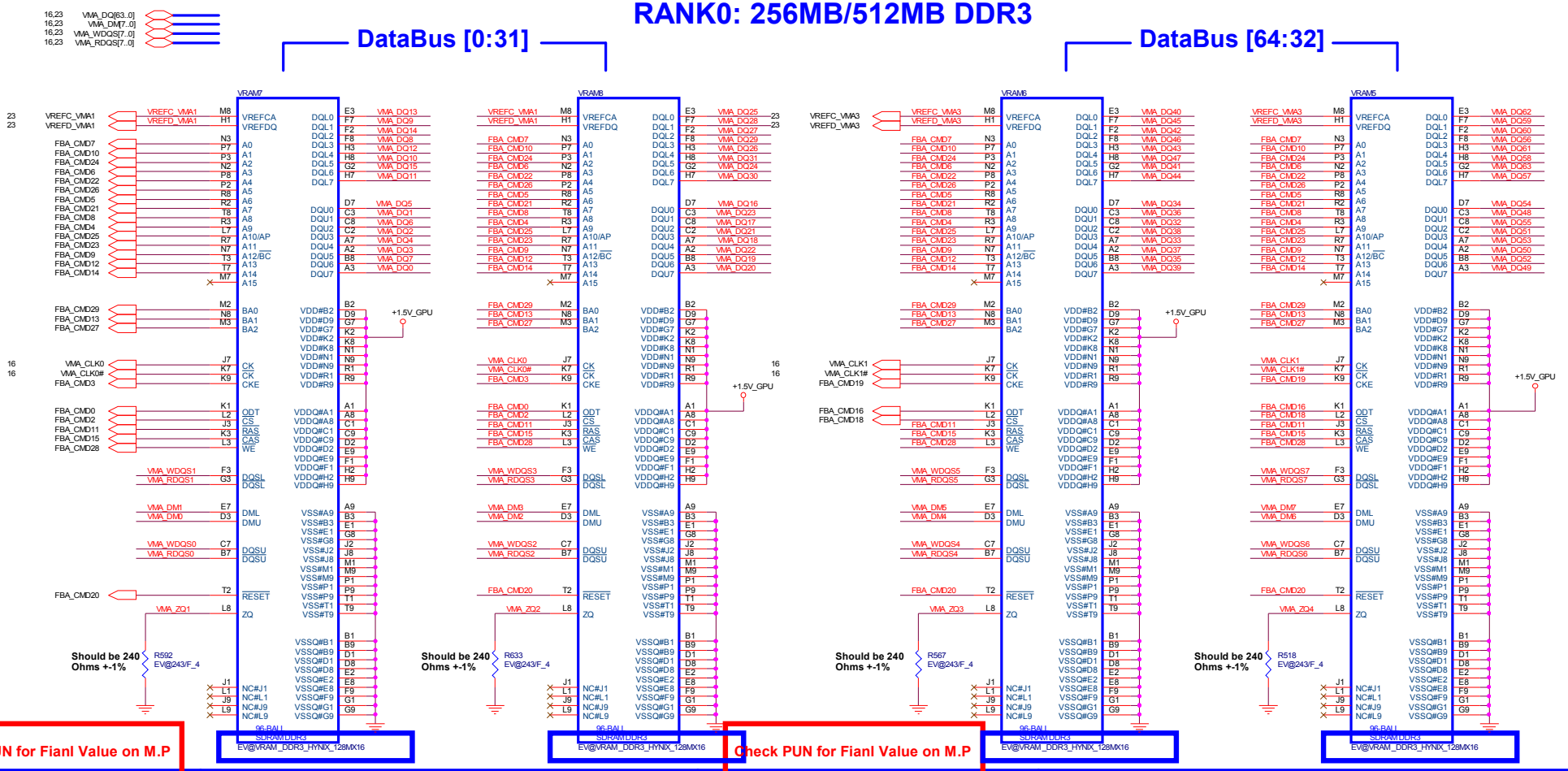
| Size | Document Number | Rev |
|---|---|---|
| | N14x (Power/GND) | A1A |

Date: Friday, December 28, 2012 Sheet 21 of 49

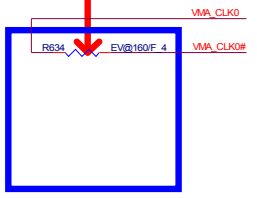
# RANK0: 256MB/512MB DDR3

## DataBus [0:31]

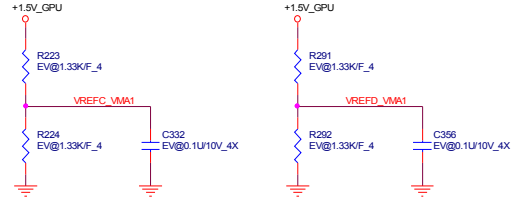
## DataBus [64:32]



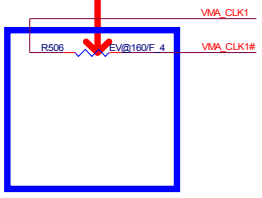

## CLK-A0 Termination



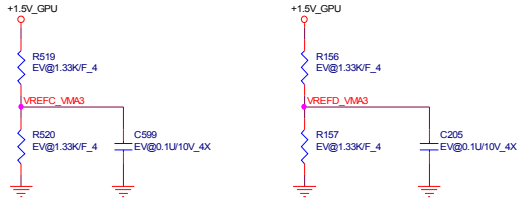

## MEM Reference Voltage (Low)



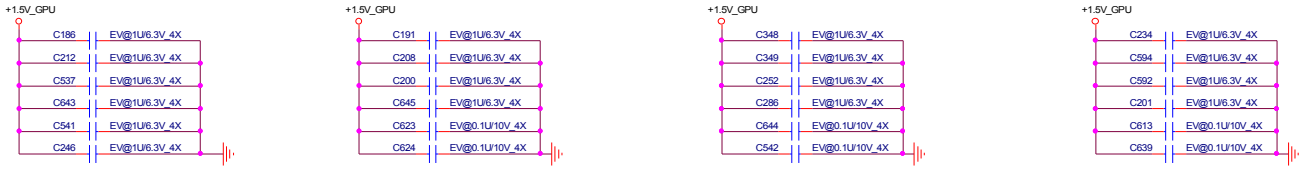

## CLK-A1 Termination




## MEM Reference Voltage (High Bus)




## VRAM De-Coupling




Quanta Computer Inc.

PROJECT : MTC_MTCD

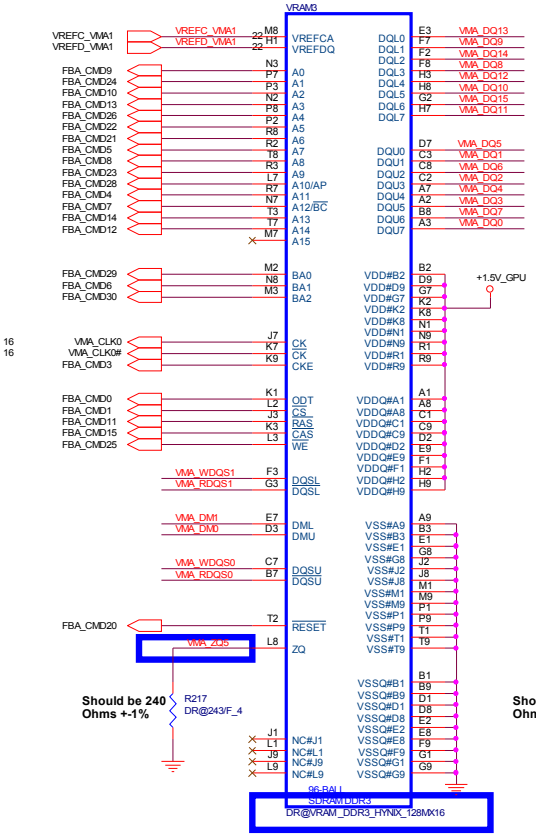
| Size | Document Number | Rev |
|---|---|---|
| | N14x (DDR/Rank0) | A1A |

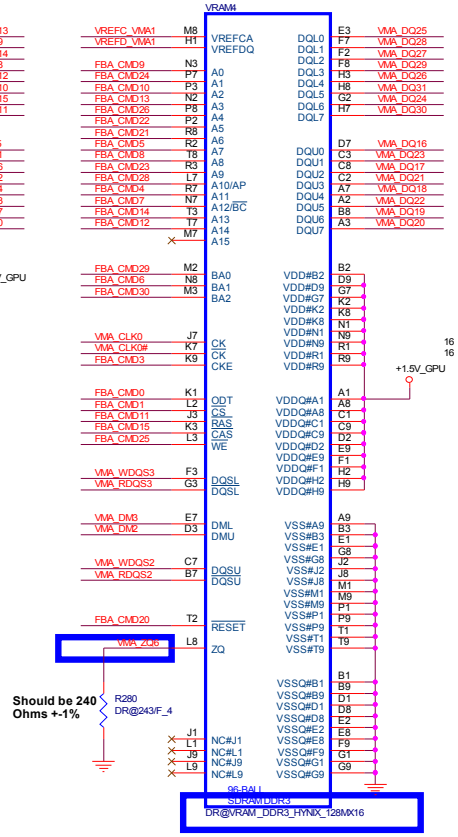
Date: Friday, December 28, 2012 Sheet 22 of 49

# RANK1: 256MB/512MB DDR3

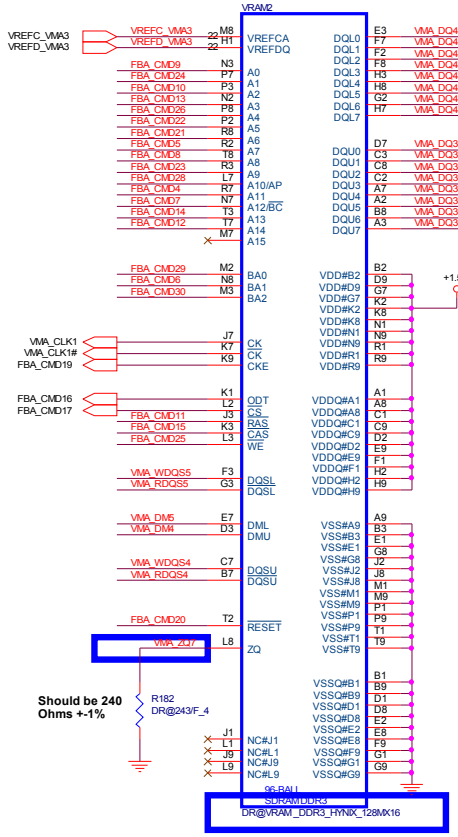
16,22 VMA_DQ[63..0]
16,22 VMA_DM[7..0]
16,22 VMA_WDQS[7..0]
16,22 VMA_RDQS[7..0]

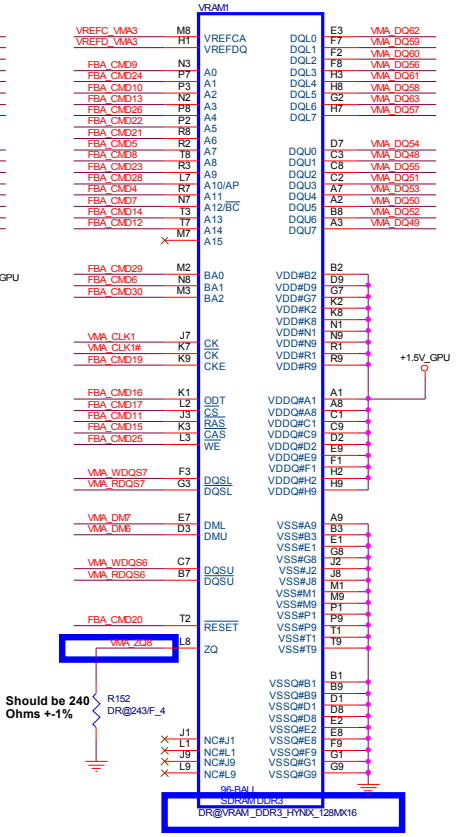
## DataBus [0:31]



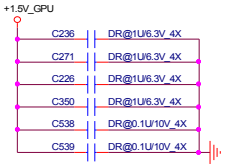



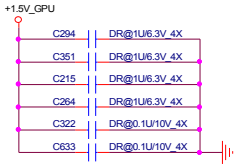

## DataBus [64:32]

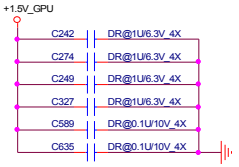


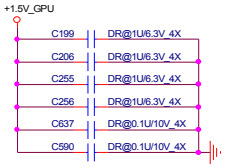




## VRAM De-Coupling



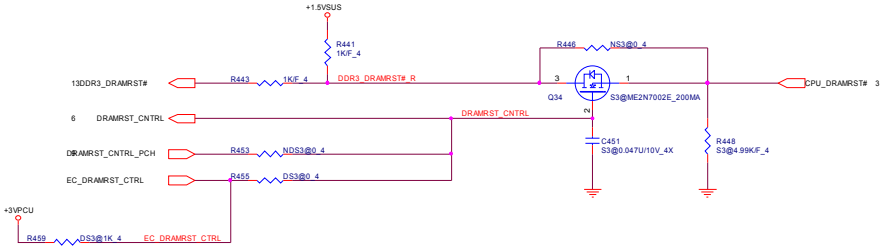




Quanta Computer Inc.
PROJECT : MTC_MTCD

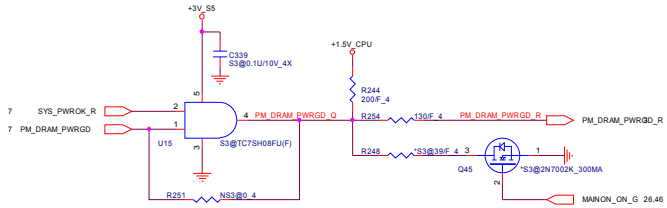
| Size | Document Number | Rev |
|---|---|---|
| | N14x (DDR/Rank1) | A1A |

Date: Friday, December 28, 2012 Sheet 23 of 49

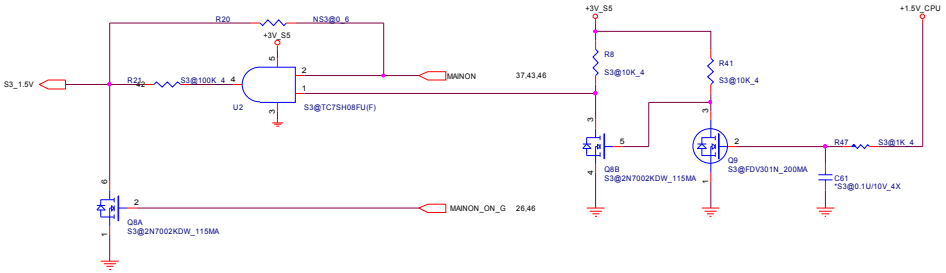
## S3 power Reduction (SM_DRAMRST#) S3P/NS3P/CPU



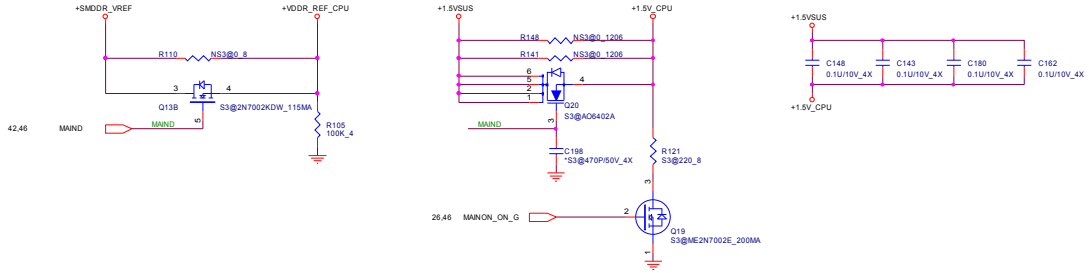

## S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU



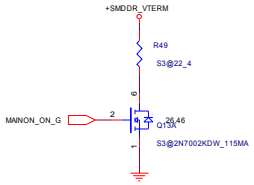

## For S3 power Reduction Sequence S3P/NS3P/CPU




## S3 power Reduction (CPU Power) S3P/NS3P/CPU




## For S3 power Reduction VTT discharge S3P/NS3P/CPU



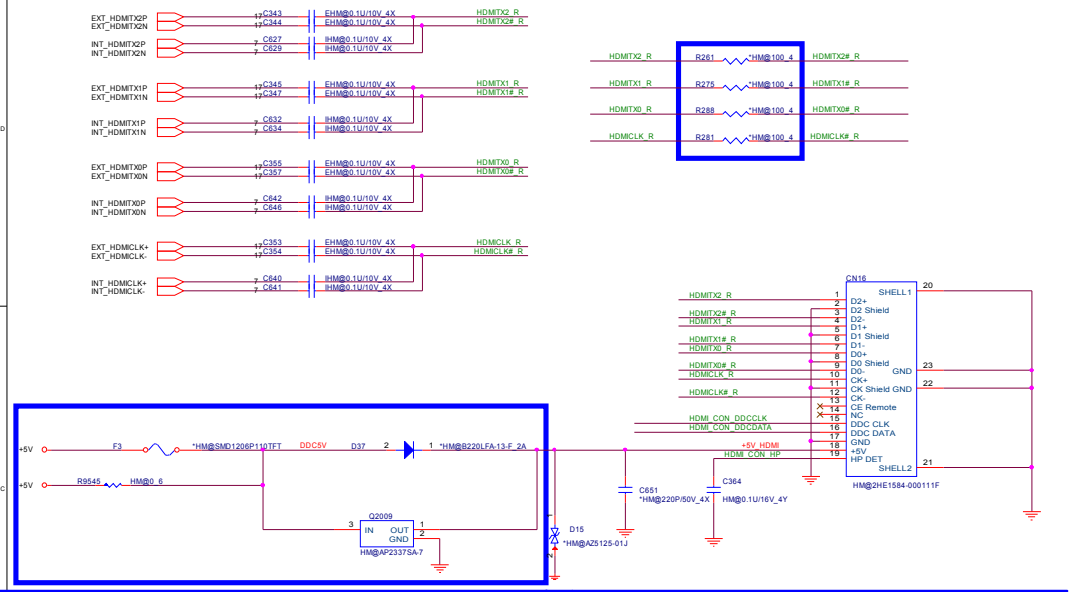

Quanta Computer Inc.

PROJECT : MTC MTCD

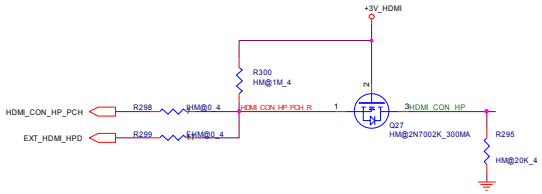
| Size | Document Number | Rev |
|---|---|---|
| | S3 power Reduction | A1A |

Date: Friday, December 28, 2012 Sheet 26 of 49

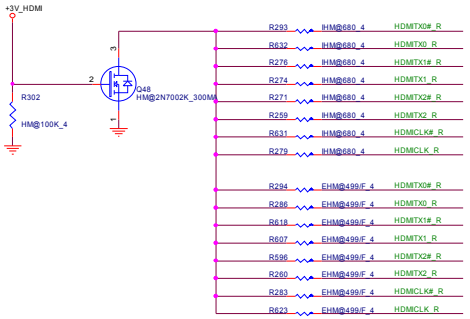
## HDMI Conn HDM/HMU/HMV



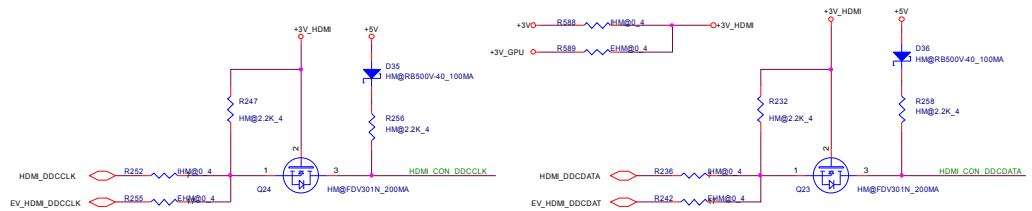

## HDMI-HPD HDM/HMU/HMV




## HDMI LEVEL SHIFT HDM/HMU/HMV

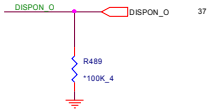



## HDMI-SMBus HDM/HMU/HMV

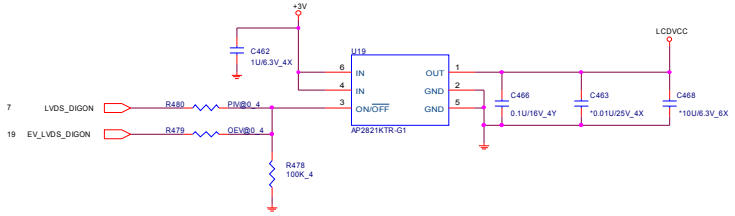



Quanta Computer Inc.
PROJECT : MTC_MTCD
Size | Document Number: HDMI CONN | Rev: A1A
Date: Friday, December 28, 2012 Sheet 27 of 49

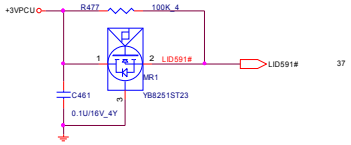
## Panel backlight control LDS



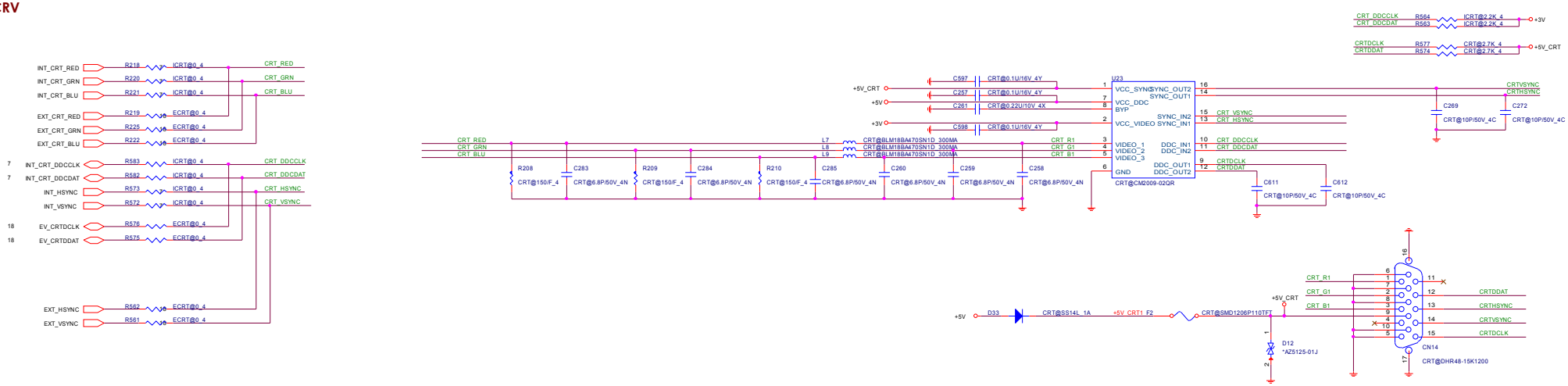

## LCD POWER SWITCH LDS/LDU/LDV




## HALL Sensor HSR

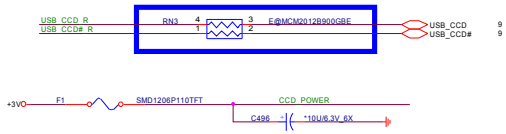



## CRT CRT/CRU/CRV




## LCD Panel Module <LDS>


## CCD CCD



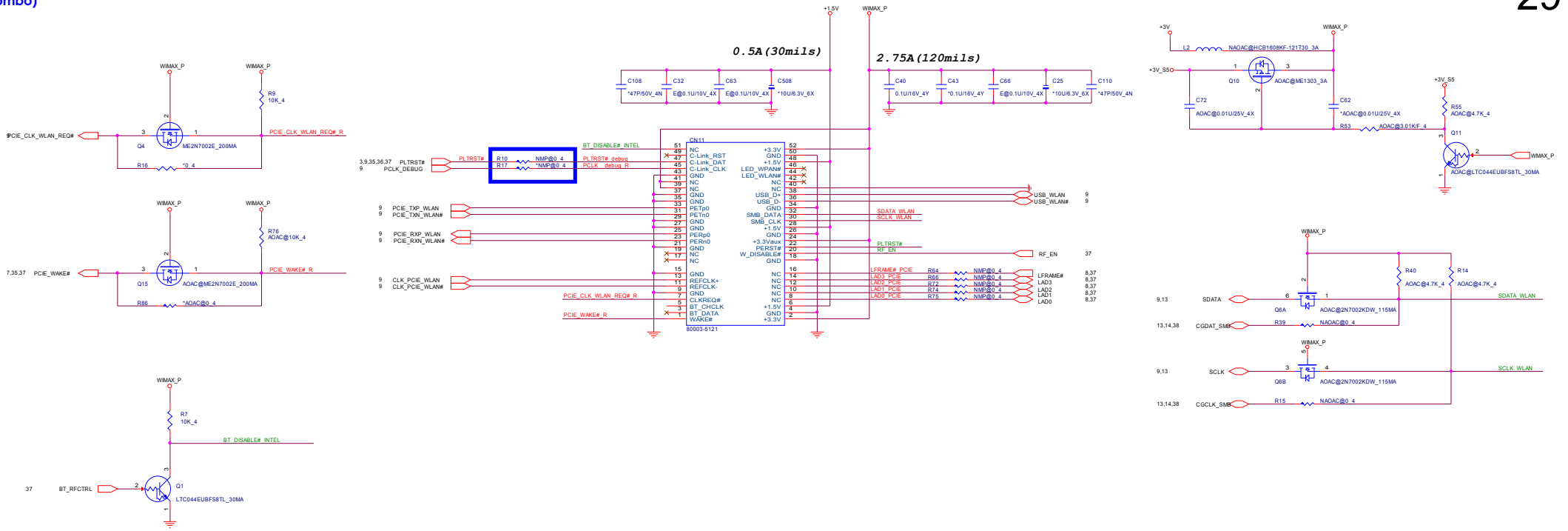

Quanta Computer Inc.
PROJECT : MTC_MTCD
Size | Document Number: LCD/LED Panel/CCD | Rev: A1A
Date: Friday, December 28, 2012 | Sheet 28 of 49

# MINI Card Slot#1(WiFi / Wimax / Combo)

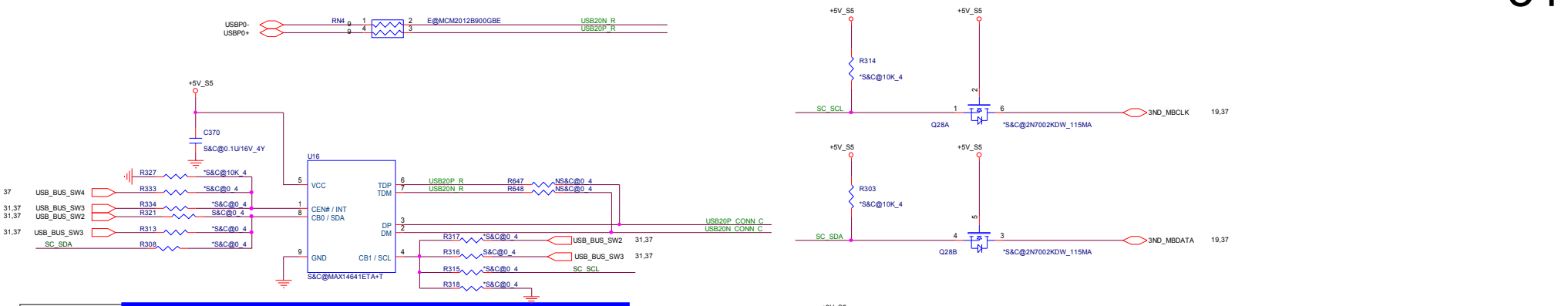
**MNW/DEG**

[AOAC]





# USB CONNECT RIGHT(UR) <U3B/USB>




| | R333 | R334 | R316 | R318 | R327 | R321 | R313 | R308 | R315 |
|---|---|---|---|---|---|---|---|---|---|
| 14566 | | V | | V | | | | | |
| 14600 | | | V | | | V | | | |
| 14617(with CB2) | V | | V | | | | | | |
| 14617(no CB2) | | | V | | V | | | | |
| 14641/14642/14644 | | | V | | | V | | | |
| 14640 | | | | | | | | V | V |

**2013 Chief River/Brazos**

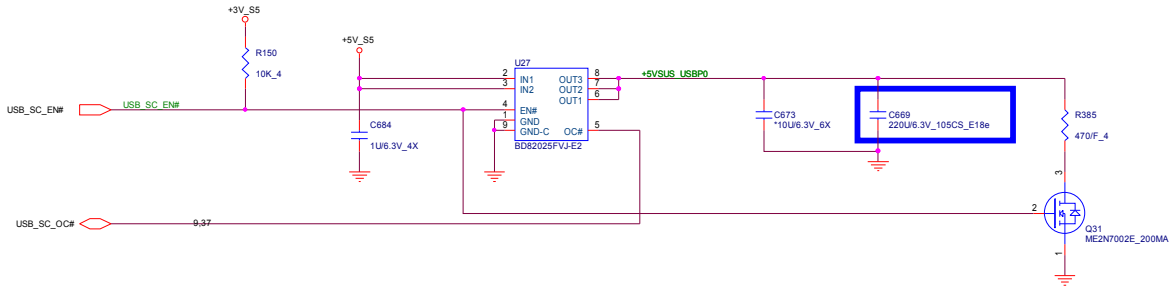
| SW2 | SW3 | 14600 | |
|---|---|---|---|
| CB0 | CB1 | Status | |
| 0 | 0 | Auto mode | Charger , AM |
| 0 | 1 | Force dedicated charger mode | Charger , FM |
| 1 | 0 | Pass-Through(USB) mode | USB , PM |
| 1 | 1 | pass-through(USB) with CDP Emulation | USB , CM |

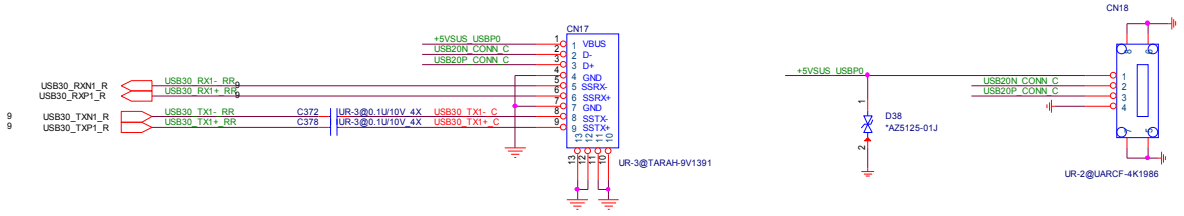
**2013 Shark bay / Kabini**

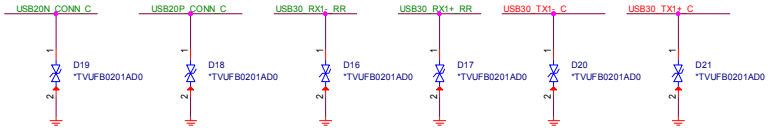
| SW3 | SW2 | 14641 | |
|---|---|---|---|
| CB1 | CB0 | Status | |
| 0 | 0 | 2A Auto mode for Apple device | Charger , AM2 |
| **1** | **0** | Force 1A for Apple device | Charger , AP1 |
| **0** | **1** | Pass-Through(USB) mode | USB , PM |
| 1 | 1 | pass-through(USB) with CDP Emulation | USB , CM |

| SW3 | SW2 | 14644 | |
|---|---|---|---|
| CB1 | CB0 | Status | |
| 0 | 0 | 2A Auto mode for Apple device | Charger , AM2 |
| **1** | **0** | Force dedicated charger mode | Charger , FM |
| **0** | **1** | Pass-Through(USB) mode | USB , PM |
| 1 | 1 | pass-through(USB) with CDP Emulation | USB , CM |

| SW3 | SW2 | 14642 | |
|---|---|---|---|
| CB1 | CB0 | Status | |
| X | 0 | 2A Auto mode for Apple device | Charger , AM2 |
| **0** | **1** | Pass-Through(USB) mode | USB , PM |
| 1 | 1 | pass-through(USB) with CDP Emulation | USB , CM |




Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | USB3 Redriver/S&C/USB2 | A1A |

Date: Friday, December 28, 2012 Sheet 31 of 49

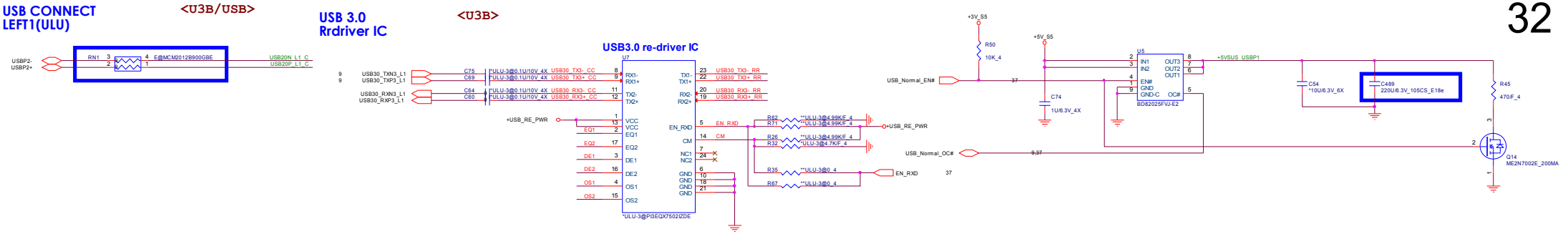
## USB CONNECT LEFT1(ULU)

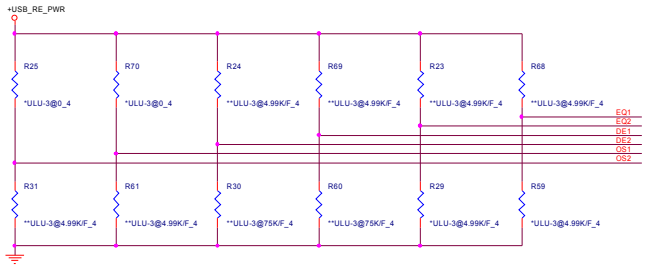
<U3B/USB>

## USB 3.0 Rrdriver IC

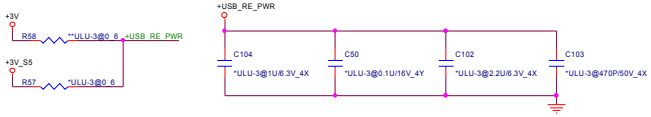
<U3B>

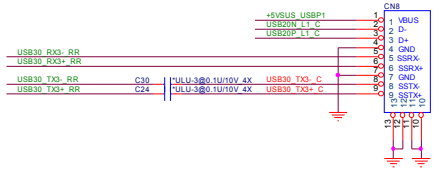
### USB3.0 re-driver IC

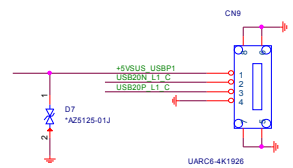


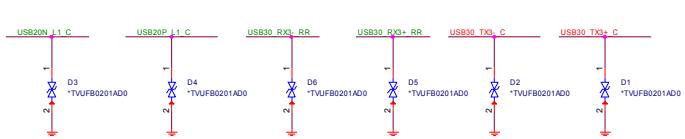




| Control pins setting | | | |
|---|---|---|---|
| **EN_RXD** | **Device function** | **CM** | **Device function** |
| 1(default) | Normal Operation | 0(default) | Normal Operation |
| 0 | Sleep Mode | 1 | Compliance Test Mode |



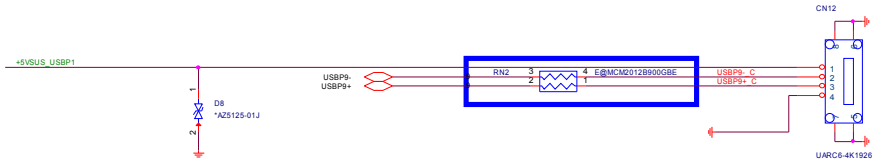



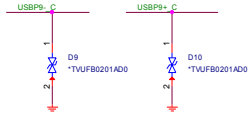




## USB CONNECT LEFT2(ULD)

ULD




Quanta Computer Inc.

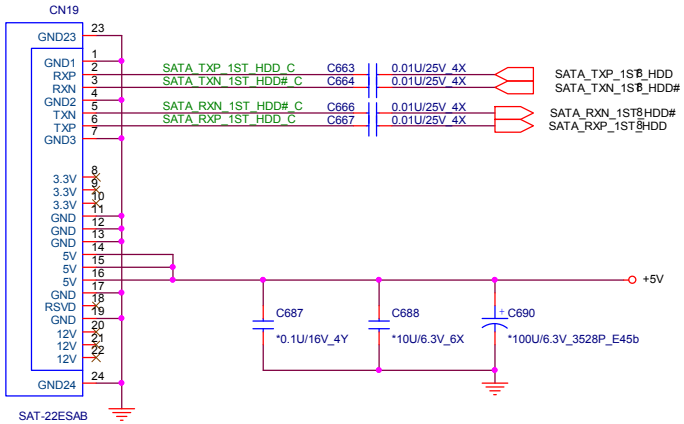
PROJECT : MTC MTCD

| Size | Document Number | Rev |
|---|---|---|
| | USB3 Redriver/USB2_Left | A1A |

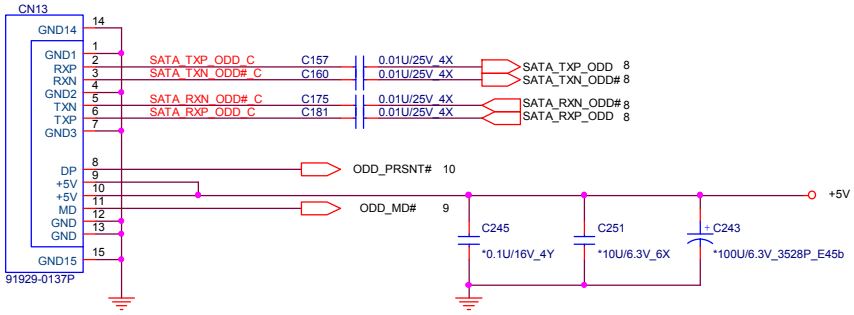
Date: Friday, December 28, 2012 Sheet 32 of 49

# SATA HDD

## HDD




# SATA ODD <ODD>



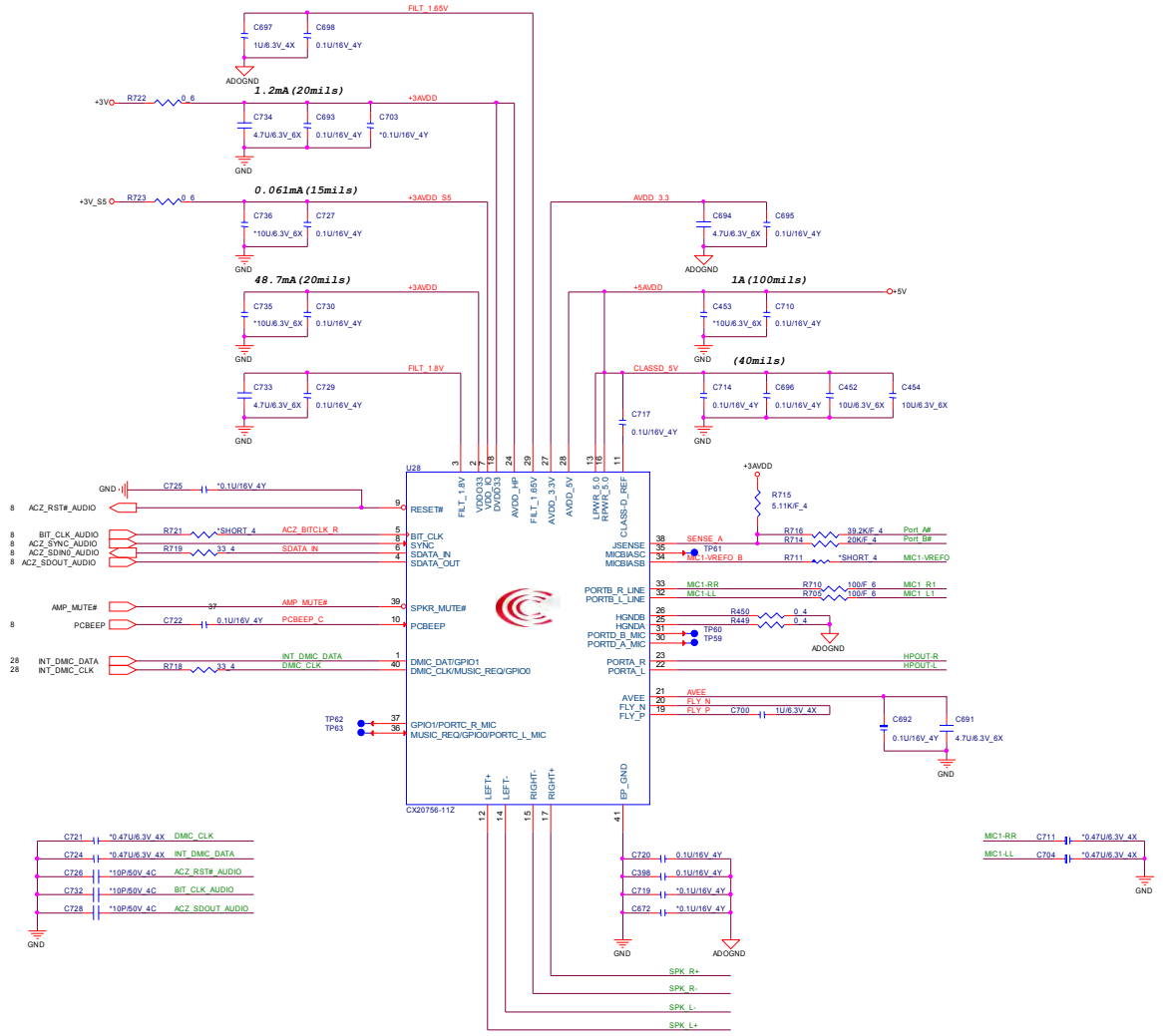

Quanta Computer Inc.

PROJECT : MTC_MTCD

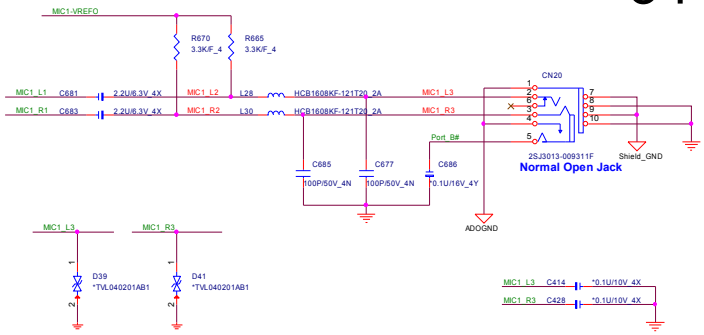
| Size | Document Number | Rev |
|---|---|---|
| | HDD/ODD | A1A |

Date: Friday, December 28, 2012 Sheet 33 of 49

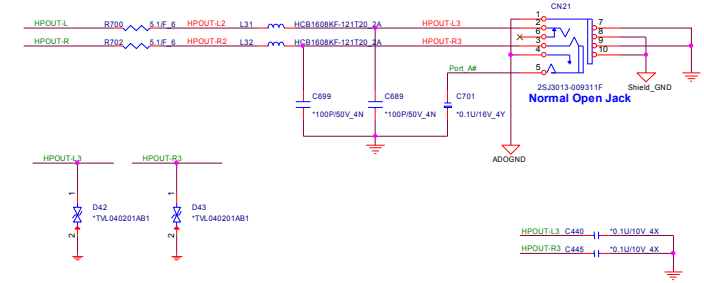
# Codec (CX20756-11Z) <ADO>



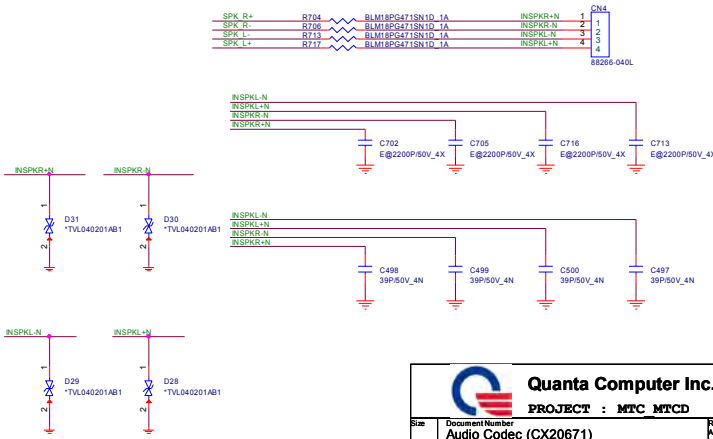

## External MIC <ADO>




## Headphone <ADO>




## Internal Speaker <ADO>




Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | Audio Codec (CX20671) | A1A |

Date: Friday, December 28, 2012 Sheet 34 of 49

# Atheros Lan <LAN/LN1.LNG>

| | |
|---|---|
| | L1,C42,C49,C39 |
| Switch mode | Mount |
| LDO mode | NC |

| | |
|---|---|
| | L17 |
| Switch mode | Mount |
| LDO mode | NC |

0.163A(20mils)

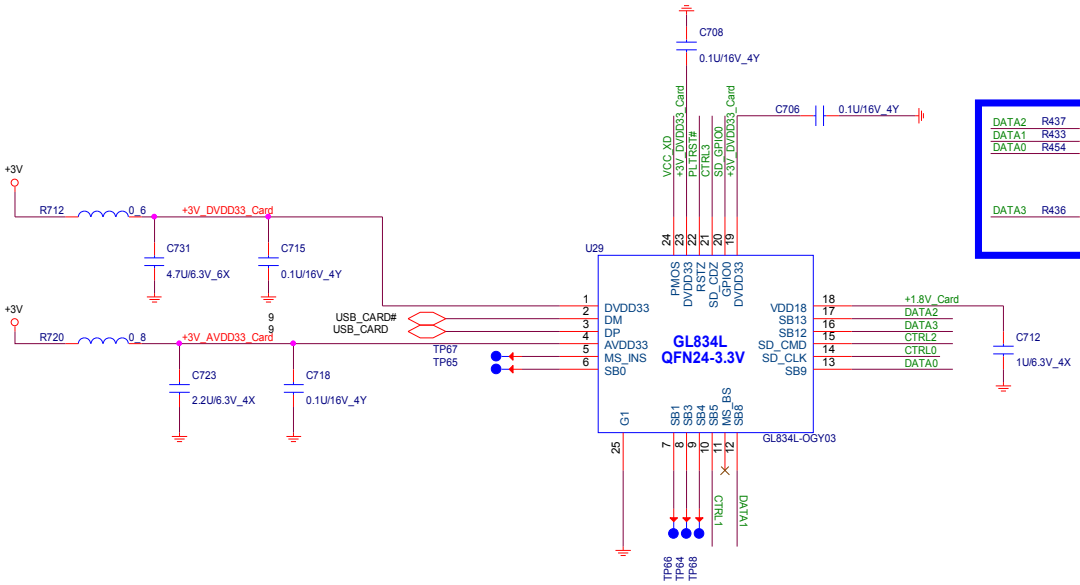
Atheros AR8161/8162

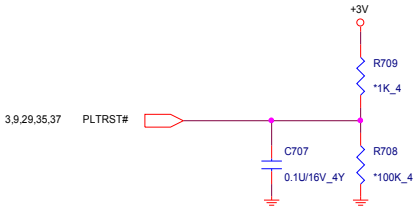
## TRANSFORMER <LAN/LN1.LNG>

## RJ45 <LAN>

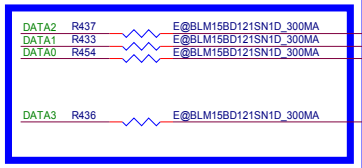
Quanta Computer Inc.
PROJECT : BLG
Size: N87 | Document Number: Atheros Lan | Rev: A1A
Date: Friday, December 28, 2012 | Sheet 35 of 49

# Card Reader (GL834L) <MMC>



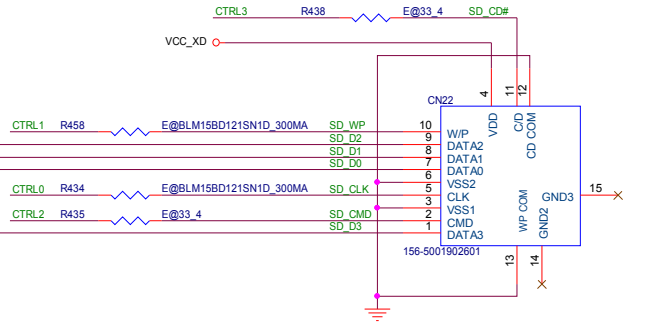


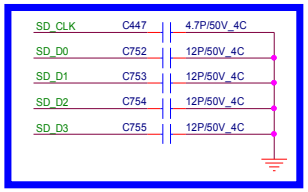


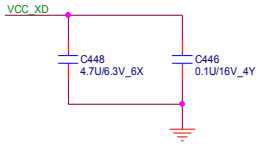

## 2 IN 1 Card Reader(SD & MMC) <MMC>

36

### EMI



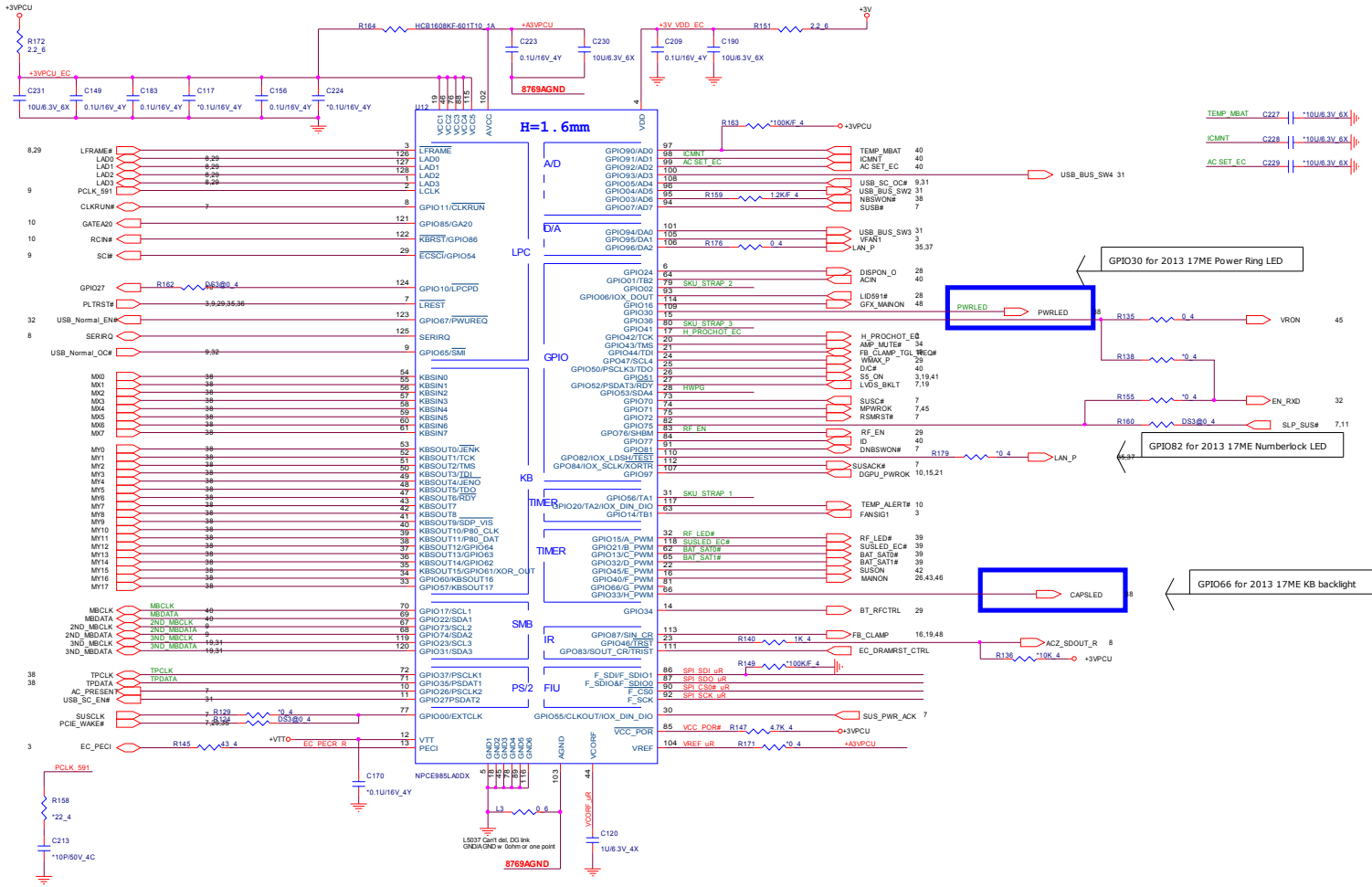

Quanta Computer Inc.

PROJECT : MTC_MTCD

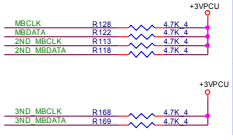
| Size | Document Number | Rev |
|---|---|---|
| | Card Reader(AU6437) | A1A |

Date: Friday, December 28, 2012 Sheet 36 of 49

## EC<KBC>



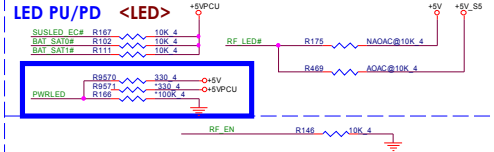

## SM BUS PU/Address <KBC>



| SMBUS | Devices | Address |
|---|---|---|
| 1 | Battery(A) | |
| 2 | PCH(S5) | |
| | G-sensor(S0) | |
| | CPU Thermal(A) | 98H |
| | IDROM(A) | |
| 3 | VGA Thermal(A or S0) | 98H |
| | CEC(A) | |
| | MMB(A) | |

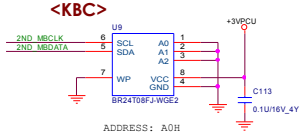
## TP <KBC>

## LED PU/PD <LED>



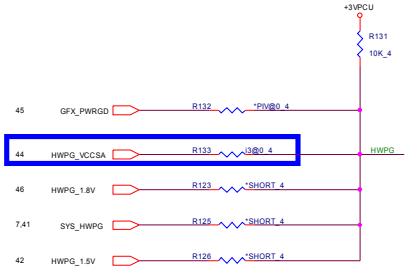
## INTERNAL KEYBOARD STRIP SET <KBC>

## ID EEPROM <KBC>

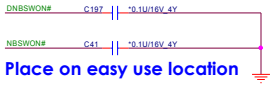



## SPI FLASH <KBC>

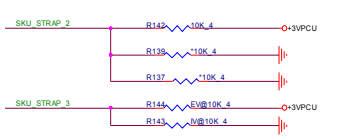
## HWPG circuit <KBC>



## Power Button <KBC>



Place on easy use location



| MS Strap | SKU_STRAP_1 | SKU_STRAP_2 | SKU_STRAP_3 |
|---|---|---|---|
| 13" UMA | 0 | 0 | 0 |
| 13" DIS | 0 | 0 | 1 |
| 14" Capetown UMA | 0 | 1 | 0 |
| 14" Capetown DIS | 0 | 1 | 1 |
| 17" Aswan UMA | 1 | 0 | 0 |
| 17" Aswan DIS | 1 | 0 | 1 |

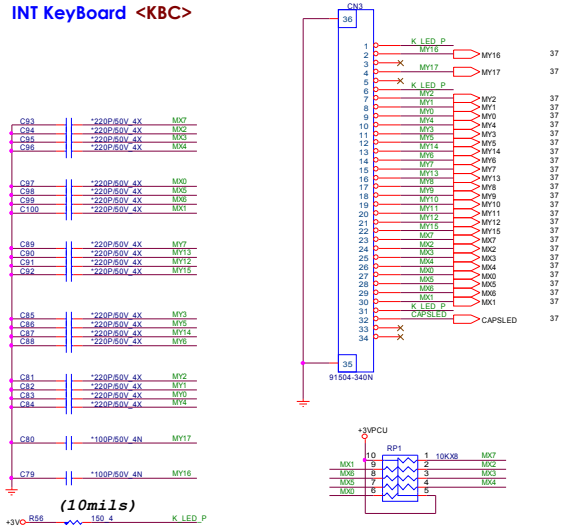
Capetown@/Aswan@ EV@ / IV@

Quanta Computer Inc.
PROJECT : MTC_MTCD

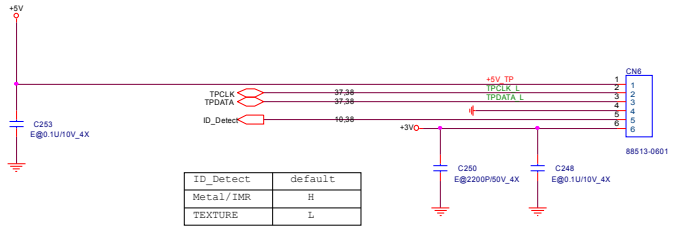
| Size | Document Number | Rev |
|---|---|---|
| | EC-NPCE885L | A1A |

Date: Friday, December 28, 2012 Sheet 37 of 49

## INT KeyBoard <KBC>

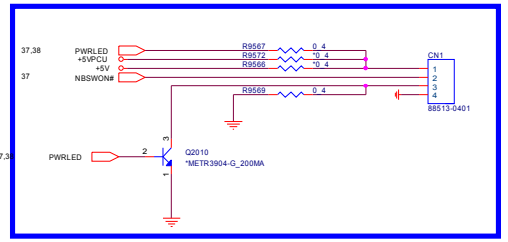



## TP board <TPD>

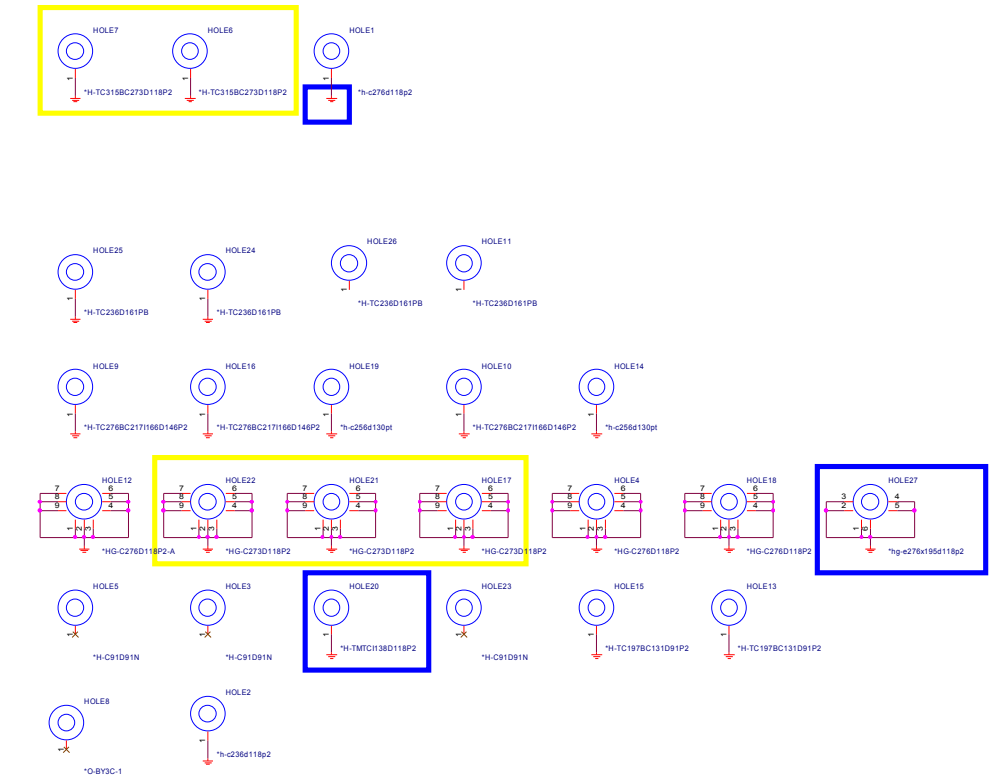



| ID_Detect | default |
|---|---|
| Metal/IMR | H |
| TEXTURE | L |

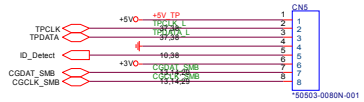
## Power board w LED <PSW>




## HOLE




## TP board <TPD>




Quanta Computer Inc.

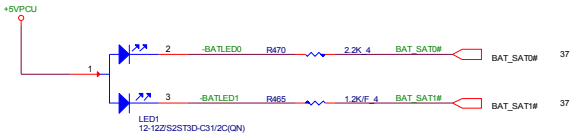
PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | KB/TP&TP/PB/FL/LEB/MMB/B-CAS | A1A |

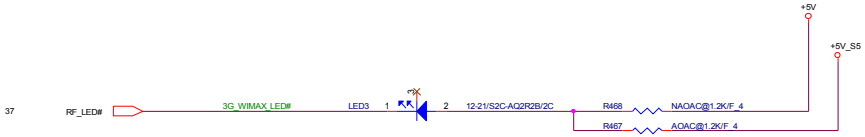
Date: Friday, December 28, 2012 Sheet 38 of 49

## LED LED

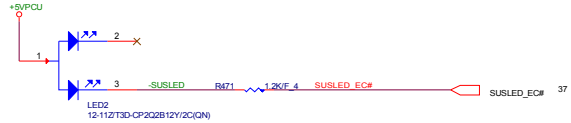
BATERRY



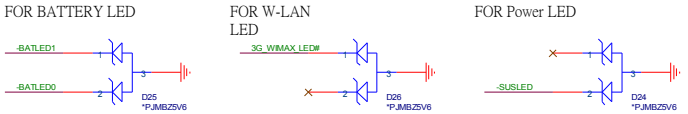

## RF LED LED



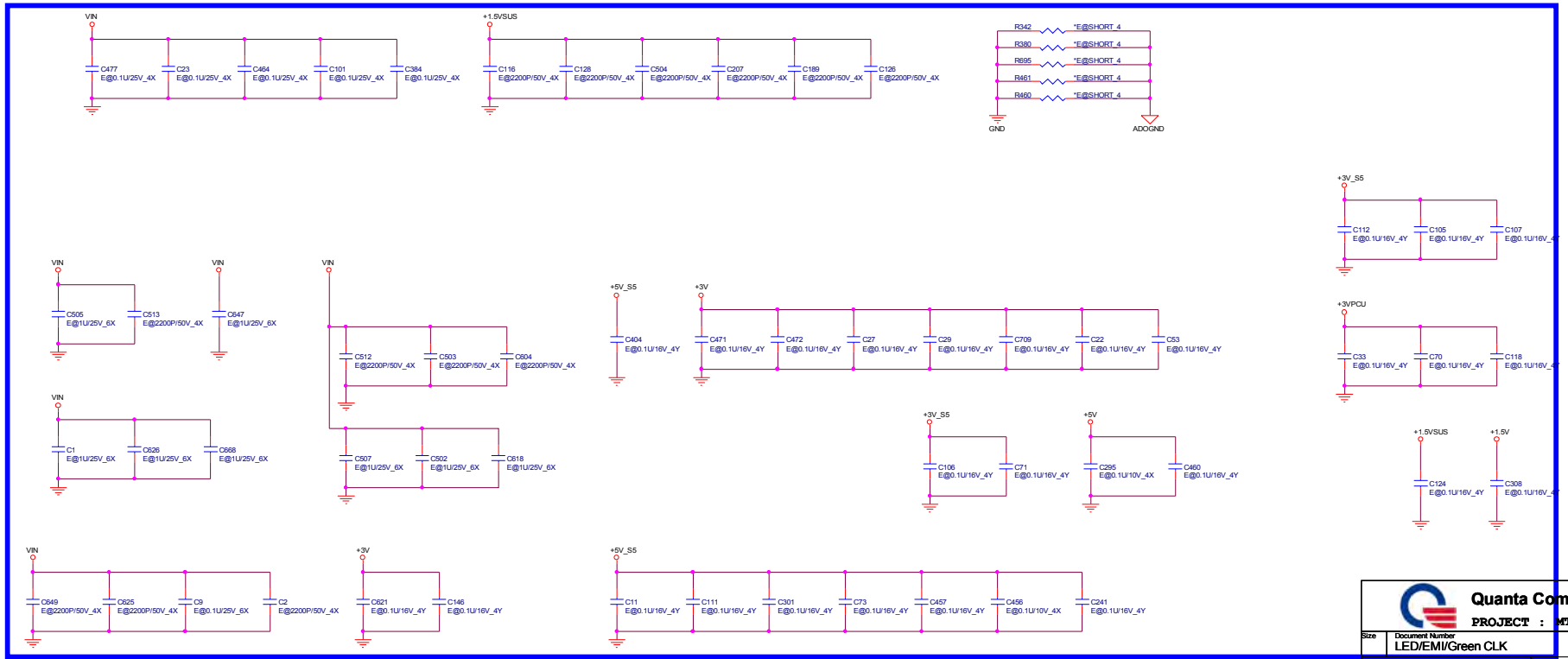

## POWER LED




## ESD Protect LED




## EMI EMI

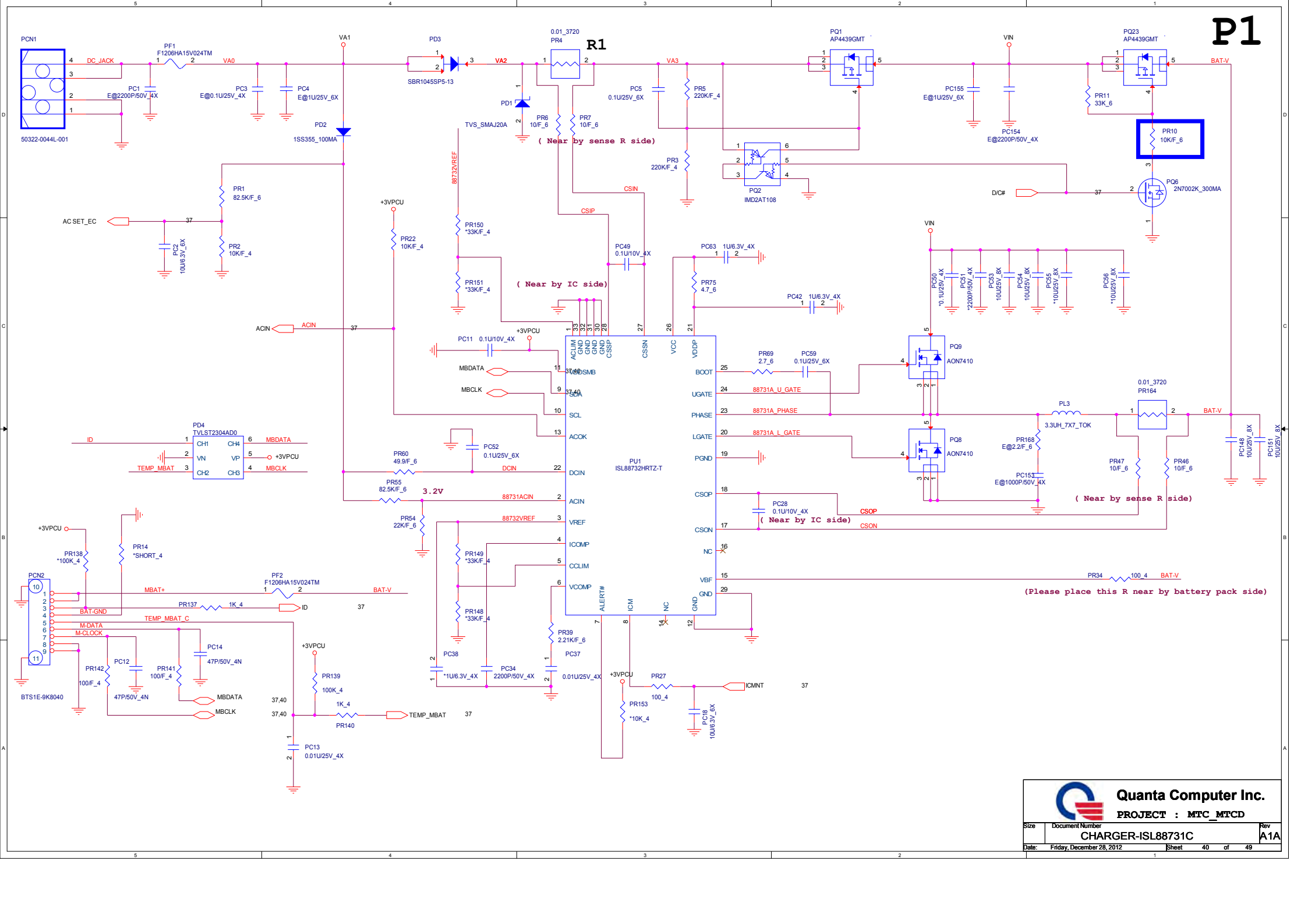


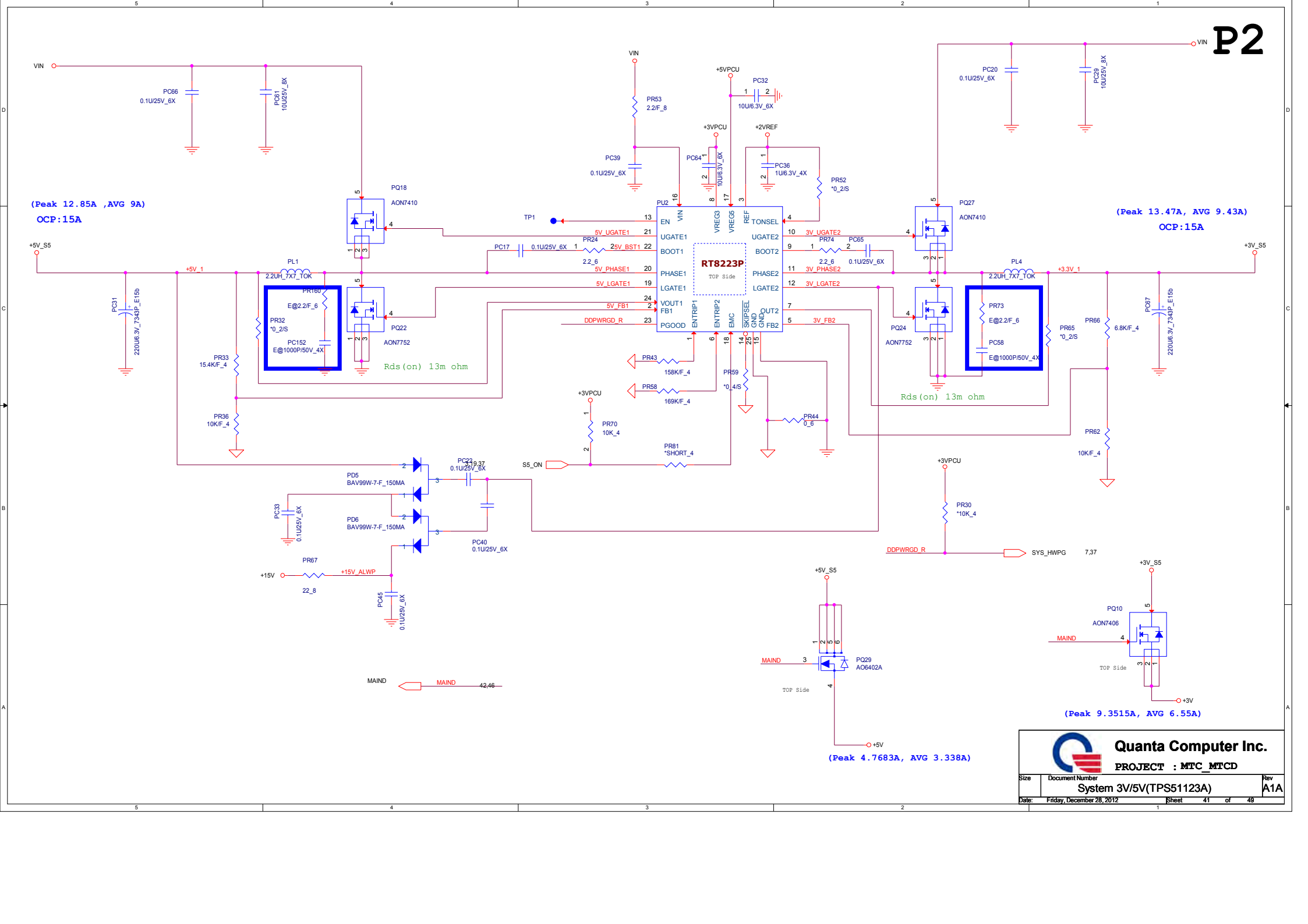

Quanta Computer Inc.

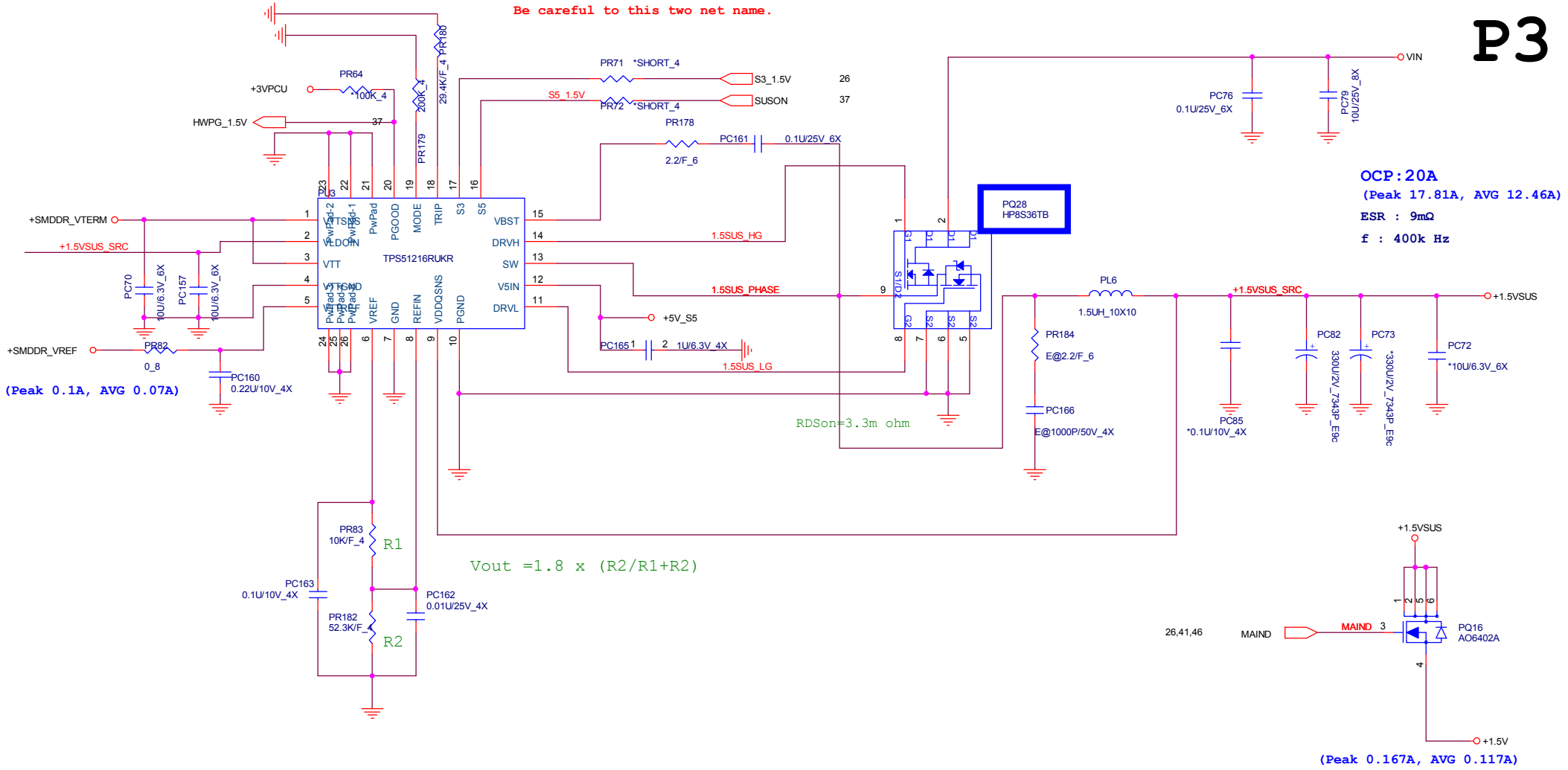
PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | LED/EMI/Green CLK | A1A |

Date: Friday, December 28, 2012 Sheet 39 of 49


P1
R1
PCN1
50322-0044L-001
DC_JACK
PF1
F1206HA15V024TM
VA0
VA1
PD3
SBR1045SP5-13
VA2
0.01_3720
PR4
VA3
PQ1
AP4439GMT
VIN
PQ23
AP4439GMT
BAT-V
PC1
E@2200P/50V_4X
PC3
E@0.1U/25V_4X
PC4
E@1U/25V_6X
PD2
1SS355_100MA
PD1
TVS_SMAJ20A
PR6
10/F_6
PR7
10/F_6
( Near by sense R side)
PC5
0.1U/25V_6X
PR5
220K/F_4
PR3
220K/F_4
PQ2
IMD2AT108
PC155
E@1U/25V_6X
PC154
E@2200P/50V_4X
PR11
33K_6
PR10
10K/F_6
PQ6
2N7002K_300MA
D/C#
PR1
82.5K/F_6
PR2
10K/F_4
AC SET_EC
PC2
10U/6.3V_6X
+3VPCU
PR22
10K/F_4
88732VREF
PR150
*33K/F_4
PR151
*33K/F_4
CSIN
CSIP
PC49
0.1U/10V_4X
PC63
1U/6.3V_4X
PR75
4.7_6
PC42
1U/6.3V_4X
( Near by IC side)
ACIN
PC11
0.1U/10V_4X
MBDATA
MBCLK
PU1
ISL88732HRTZ-T
ACLIM
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
SMBSDA
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
CCLIM
VCOMP
ALERT#
ICM
NC
GND
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR69
2.7_6
PC59
0.1U/25V_6X
88731A_U_GATE
88731A_PHASE
88731A_L_GATE
PQ9
AON7410
PQ8
AON7410
PL3
3.3UH_7X7_TOK
PR168
E@2.2/F_6
PC153
E@1000P/50V_4X
PR47
10/F_6
PR46
10/F_6
PC148
10U/25V_8X
PC151
10U/25V_8X
PC50
*0.1U/25V_4X
PC51
*2200P/50V_4X
PC53
10U/25V_8X
PC54
10U/25V_8X
PC55
*10U/25V_8X
PC56
*10U/25V_8X
PC52
0.1U/25V_6X
PR60
49.9/F_6
PR55
82.5K/F_6
3.2V
88731ACIN
PR54
22K/F_6
PC28
0.1U/10V_4X
( Near by IC side)
( Near by sense R side)
PR34
100_4
(Please place this R near by battery pack side)
PD4
TVLST2304AD0
ID
TEMP_MBAT
MBDATA
+3VPCU
MBCLK
PR149
*33K/F_4
PR148
*33K/F_4
PR39
2.21K/F_6
PC38
*1U/6.3V_4X
PC34
2200P/50V_4X
PC37
0.01U/25V_4X
PR27
100_4
PR153
*10K_4
ICMNT
PC18
10U/6.3V_6X
PCN2
BTS1E-9K8040
PR138
*100K_4
PR14
*SHORT_4
MBAT+
BAT-GND
PF2
F1206HA15V024TM
PR137
1K_4
TEMP_MBAT_C
M-DATA
M-CLOCK
PR142
100/F_4
PC12
47P/50V_4N
PR141
100/F_4
PC14
47P/50V_4N
PR139
100K_4
1K_4
PR140
PC13
0.01U/25V_4X
Quanta Computer Inc.
PROJECT : MTC_MTCD
Size
Document Number
CHARGER-ISL88731C
Rev
A1A
Date: Friday, December 28, 2012
Sheet 40 of 49


P2
VIN
PC66 0.1U/25V_6X
PC81 10U/25V_8X
PC20 0.1U/25V_6X
PC29 10U/25V_8X
PR53 2.2/F_8
PC39 0.1U/25V_6X
+5VPCU
PC32 10U/6.3V_6X
+3VPCU
PC64 10U/6.3V_6X
+2VREF
PC36 1U/6.3V_4X
PR52 *0_2/S
PU2
RT8223P
TOP Side
EN
VIN
UGATE1
BOOT1
PHASE1
LGATE1
VOUT1
FB1
PGOOD
VREG3
VREG5
REF
TONSEL
UGATE2
BOOT2
PHASE2
LGATE2
OUT2
FB2
ENTRIP1
ENTRIP2
EMC
SKIPSEL
GND
TP1
5V_UGATE1
5V_BST1
5V_PHASE1
5V_LGATE1
5V_FB1
DDPWRGD_R
3V_UGATE2
3V_PHASE2
3V_LGATE2
3V_FB2
PR24 2.2_6
PC17 0.1U/25V_6X
PR74 2.2_6
PC65 0.1U/25V_6X
PR43 158K/F_4
PR58 169K/F_4
PR59 *0_4/S
PR44 0_6
PR70 10K_4
PR81 *SHORT_4
S5_ON
PQ18 AON7410
PQ22 AON7752
PQ27 AON7410
PQ24 AON7752
(Peak 12.85A ,AVG 9A)
OCP:15A
(Peak 13.47A, AVG 9.43A)
OCP:15A
+5V_S5
+5V_1
PL1 2.2UH_7X7_TOK
PR160 E@2.2/F_6
PR32 *0_2/S
PC152 E@1000P/50V_4X
PC31 220U/6.3V_7343P_E15b
PR33 15.4K/F_4
PR36 10K/F_4
Rds(on) 13m ohm
+3V_S5
+3.3V_1
PL4 2.2UH_7X7_TOK
PR73 E@2.2/F_6
PC58 E@1000P/50V_4X
PR65 *0_2/S
PR66 6.8K/F_4
PC67 220U/6.3V_7343P_E15b
PR62 10K/F_4
Rds(on) 13m ohm
PC22 0.1U/25V_8X
PD5 BAV99W-7-F_150MA
PD6 BAV99W-7-F_150MA
PC33 0.1U/25V_6X
PC40 0.1U/25V_6X
PR67 22_8
+15V
+15V_ALWP
PC45 0.1U/25V_6X
PR30 *10K_4
DDPWRGD_R
SYS_HWPG 7,37
MAIND
MAIND 42,46
PQ29 AO6402A
+5V
(Peak 4.7683A, AVG 3.338A)
PQ10 AON7406
+3V
(Peak 9.3515A, AVG 6.55A)
Quanta Computer Inc.
PROJECT : MTC_MTCD
Size
Document Number
System 3V/5V(TPS51123A)
Rev
A1A
Date: Friday, December 28, 2012
Sheet 41 of 49

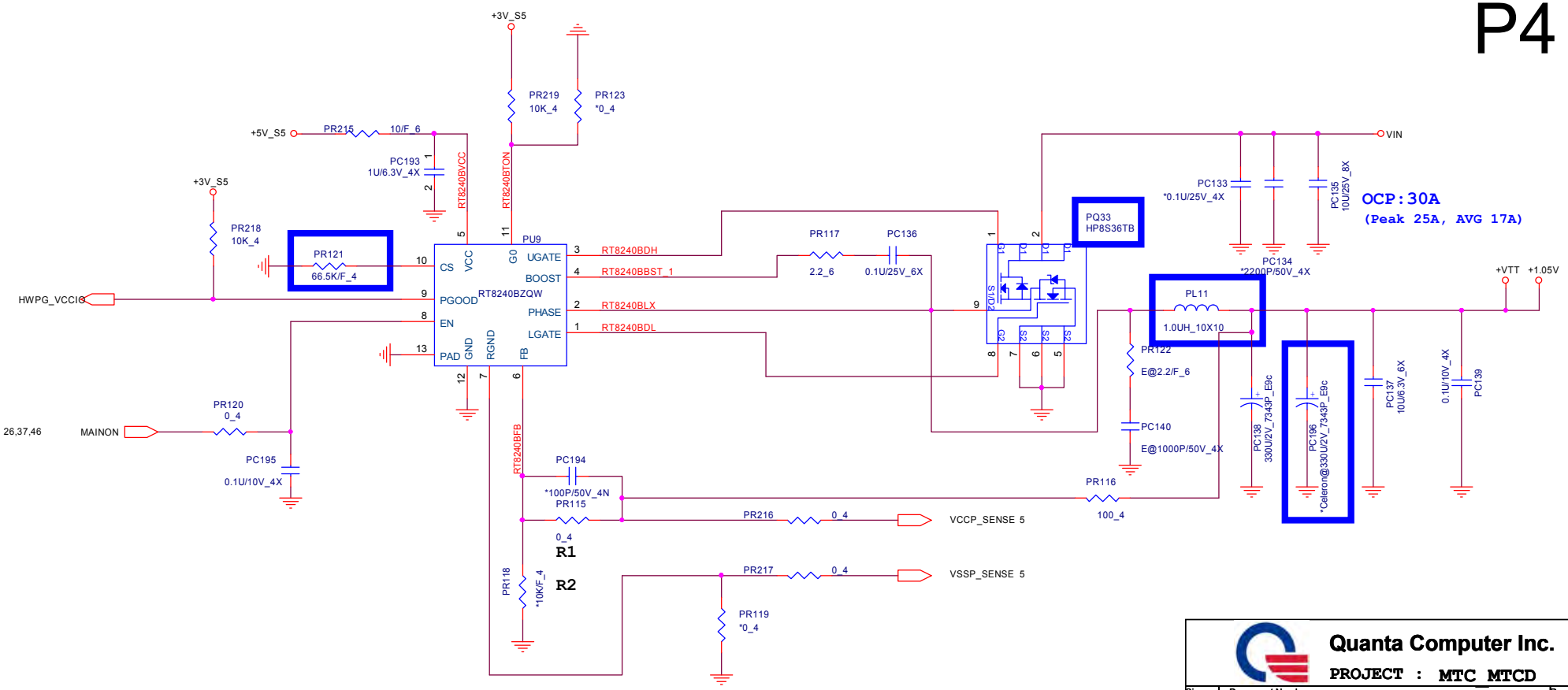


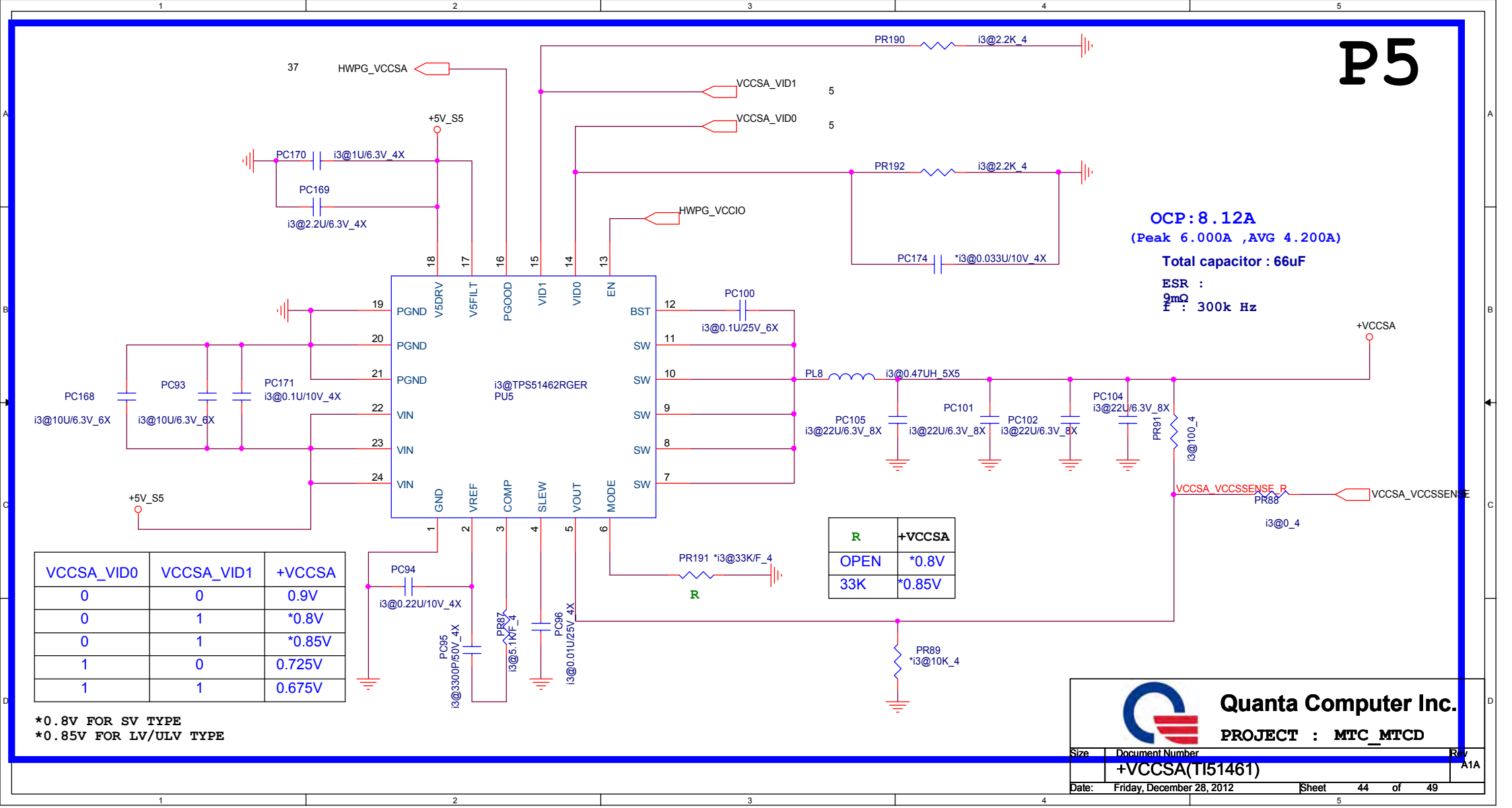

Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | DDR1.5V | A1A |

Date: Friday, December 28, 2012 Sheet 42 of 49


P4
+3V_S5
PR219
10K_4
PR123
*0_4
+5V_S5
PR215
10/F_6
PC193
1U/6.3V_4X
RT8240BVCC
RT8240BTON
+3V_S5
PR218
10K_4
PR121
66.5K/F_4
HWPG_VCCIO
PU9
RT8240BZQW
CS
VCC
G0
UGATE
BOOST
PGOOD
PHASE
EN
LGATE
PAD
GND
RGND
FB
RT8240BDH
RT8240BBST_1
RT8240BLX
RT8240BDL
PR117
2.2_6
PC136
0.1U/25V_6X
PQ33
HP8S36TB
VIN
PC133
*0.1U/25V_4X
PC135
10U/25V_8X
PC134
*2200P/50V_4X
OCP:30A
(Peak 25A, AVG 17A)
+VTT
+1.05V
PL11
1.0UH_10X10
PR122
E@2.2/F_6
PC140
E@1000P/50V_4X
PC138
330U/2V_7343P_E9c
PC196
*Celeron@330U/2V_7343P_E9c
PC137
10U/6.3V_6X
0.1U/10V_4X
PC139
PR120
0_4
26,37,46
MAINON
PC195
0.1U/10V_4X
RT8240BFB
PC194
*100P/50V_4N
PR115
0_4
R1
PR118
*10K/F_4
R2
PR216
0_4
VCCP_SENSE 5
PR217
0_4
VSSP_SENSE 5
PR119
*0_4
PR116
100_4
VOUT=(1+R1/R2)*0.5
Quanta Computer Inc.
PROJECT : MTC_MTCD
Size
Document Number
+VCCIO(RT8240BGQW)
Rev
A1A
Date: Friday, December 28, 2012
Sheet 43 of 49



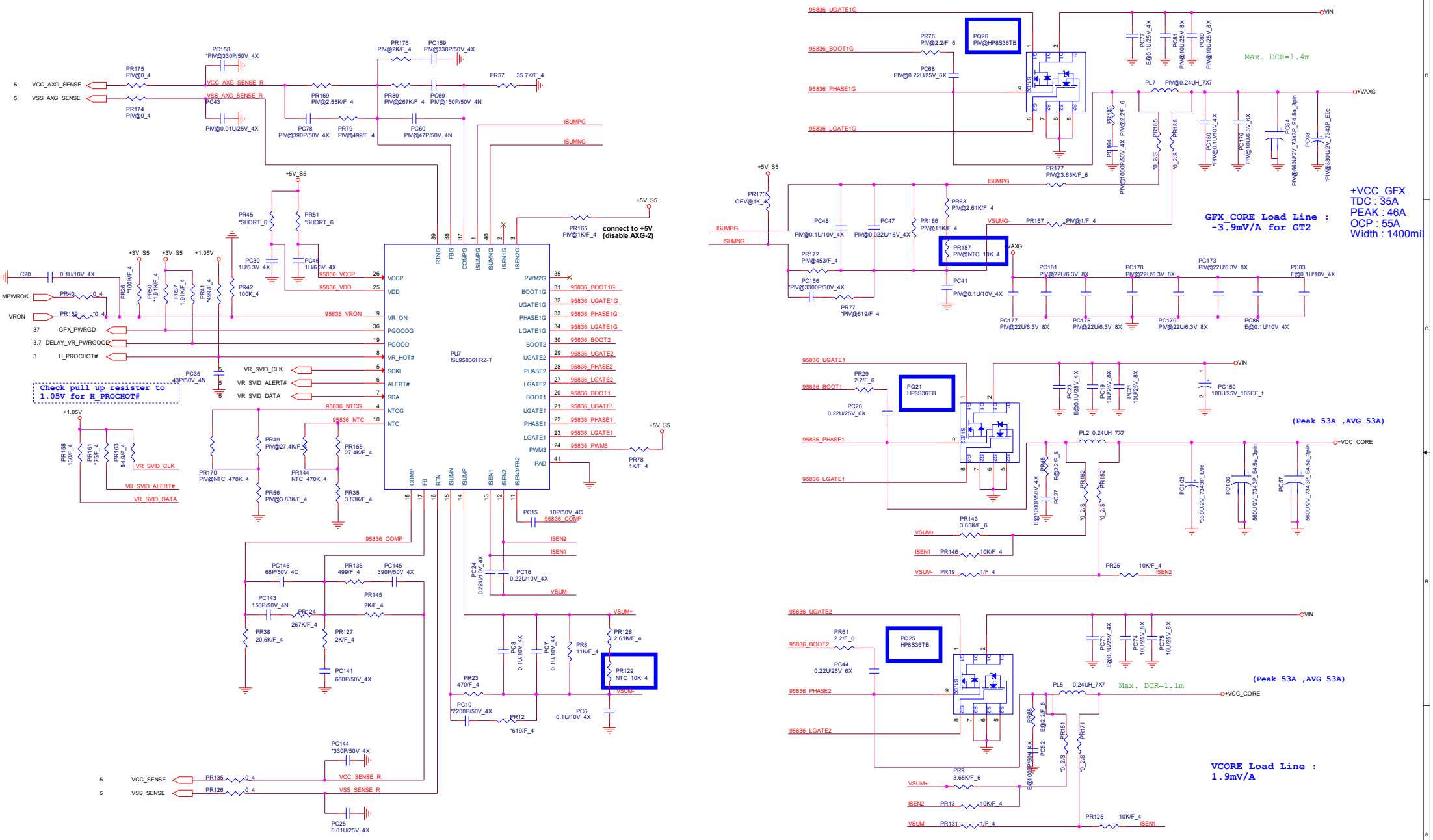

| R | +VCCSA |
|---|---|
| OPEN | *0.8V |
| 33K | *0.85V |

| VCCSA_VID0 | VCCSA_VID1 | +VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | *0.8V |
| 0 | 1 | *0.85V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

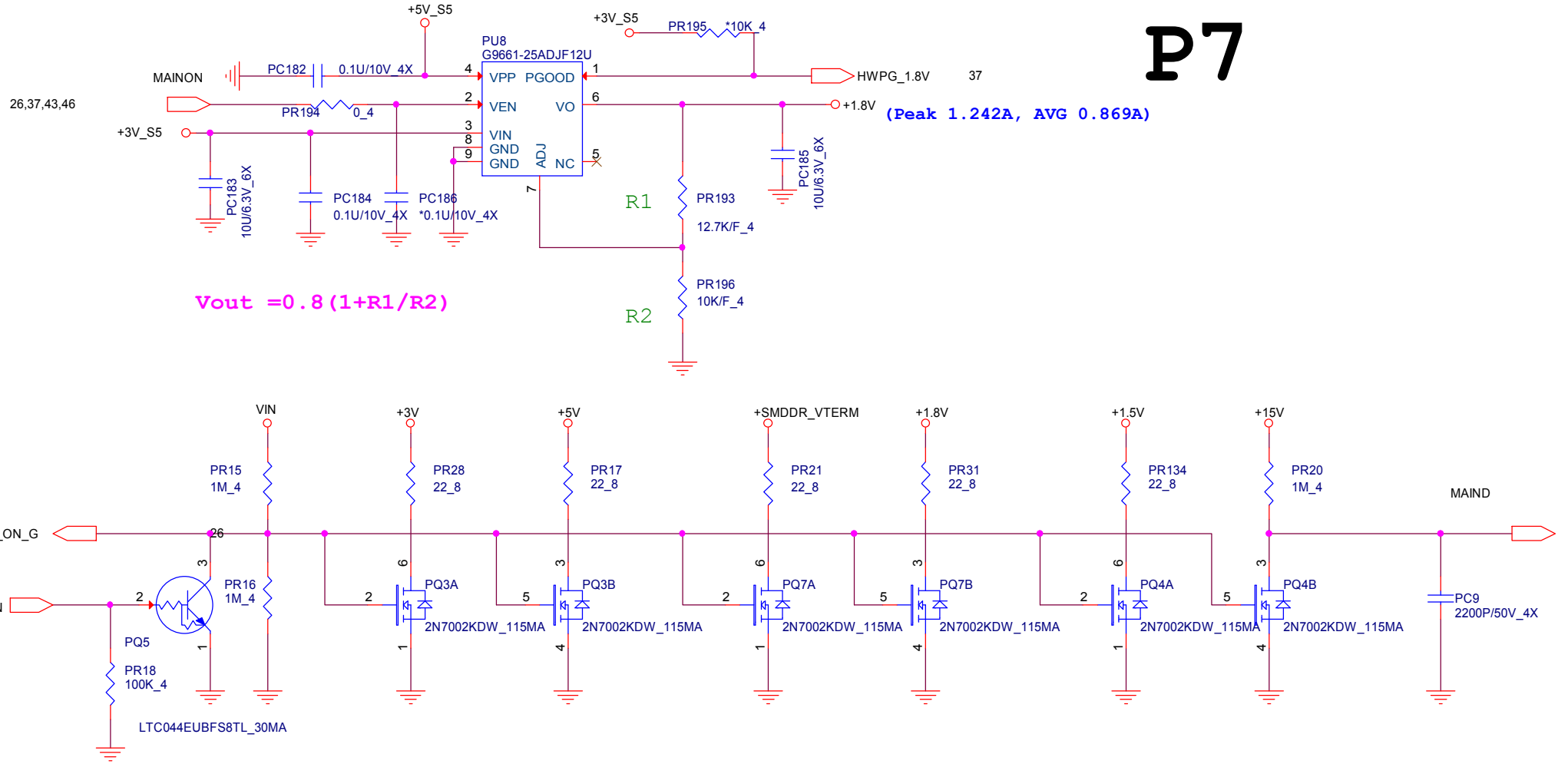
*0.8V FOR SV TYPE
*0.85V FOR LV/ULV TYPE

Quanta Computer Inc.
PROJECT : MTC_MTCD

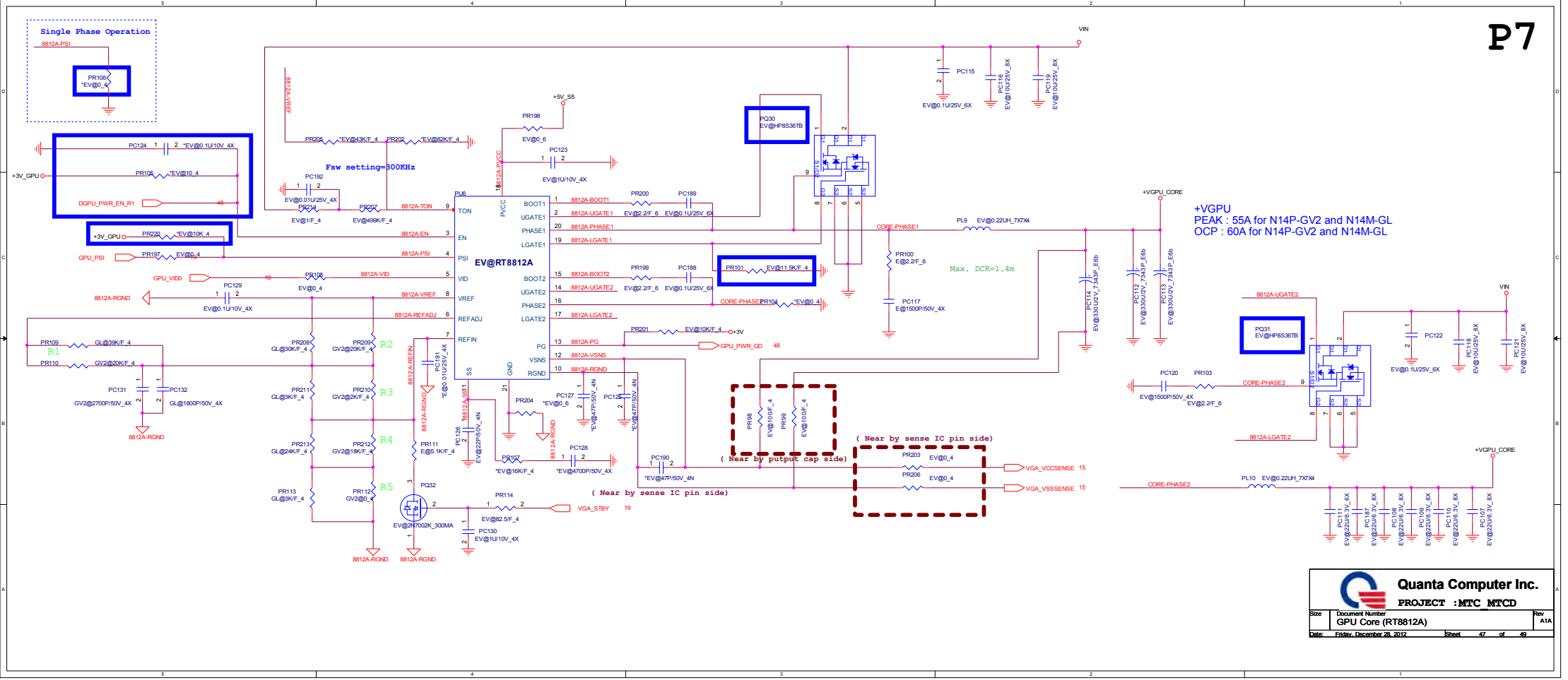
| Size | Document Number | Rev |
|---|---|---|
| | +VCCSA(TI51461) | A1A |
| Date: Friday, December 28, 2012 | Sheet 44 of 49 | |


PU7
ISL95836HRZ-T
Check pull up resister to 1.05V for H_PROCHOT#
connect to +5V (disable AXG-2)
+VCC_GFX
TDC : 35A
PEAK : 46A
OCP : 55A
Width : 1400mil
GFX_CORE Load Line : -3.9mV/A for GT2
Max. DCR=1.4m
(Peak 53A ,AVG 53A)
Max. DCR=1.1m
VCORE Load Line : 1.9mV/A
Quanta Computer Inc.
PROJECT : MTC_MTCD
+VCC_CORE+VGFX (ISL95836) 35W
Rev A1A
Friday, December 28, 2012
Sheet 45 of 49

# P7

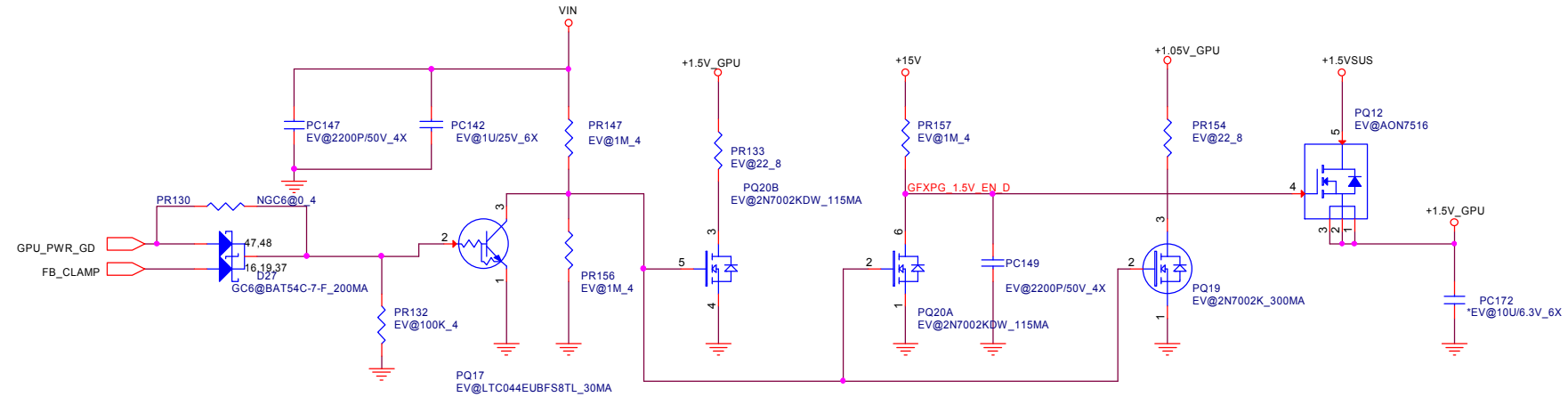


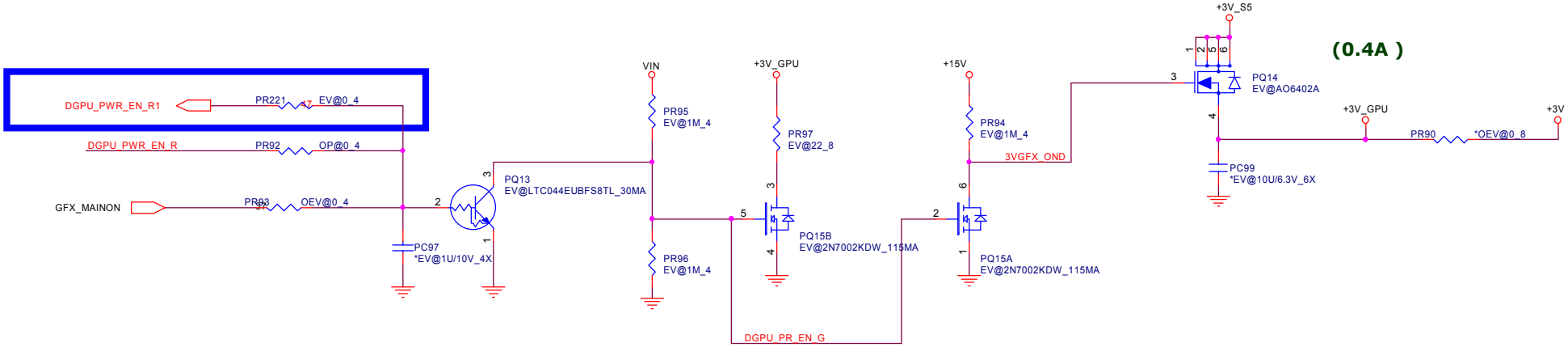

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT :MTC_MTCD | | |
| Size | Document Number: +1.8V/Discharge | Rev: A1A |
| Date: Friday, December 28, 2012 | Sheet 46 of 49 | |

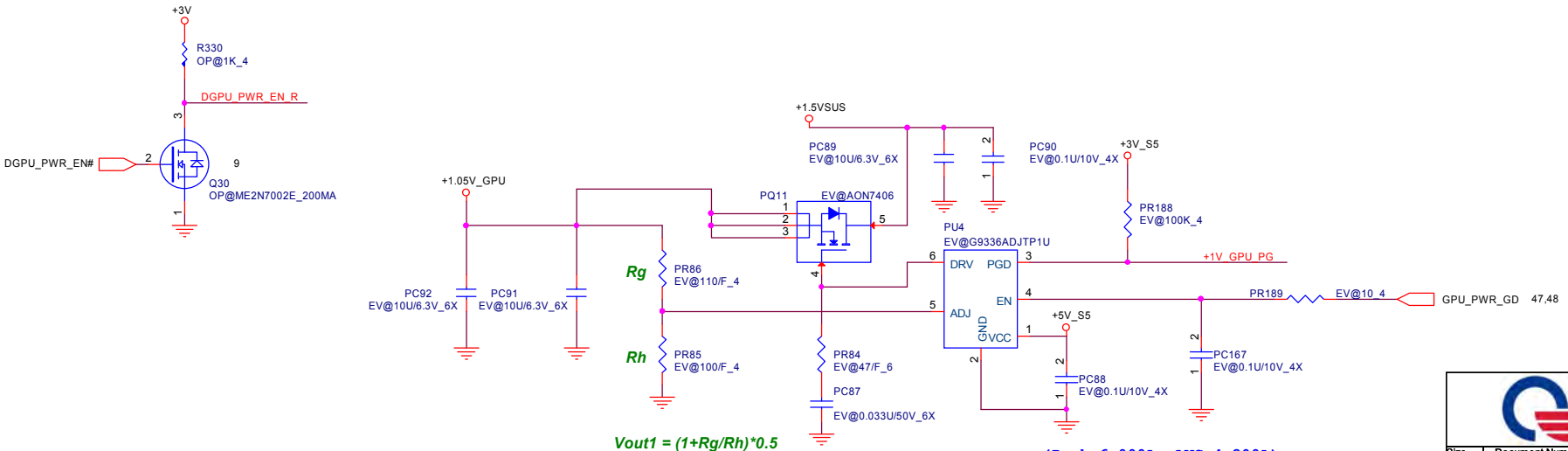



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

P9




Quanta Computer Inc.

PROJECT : MTC_MTCD

| Size | Document Number | Rev |
|---|---|---|
| | +VGACORE | A1A |
| Date: Friday, December 28, 2012 | Sheet 48 of 49 | |

# CHANGE LIST

| Model | REV | |
|---|---|---|
| MTC/MTCD | A1A | Schematic Release |
| | B2A | Page 47: Reverse PR106 and 8812A-PSI reverse 10K_4 PU to +3V_GPU |
| | | Page 35: Add LAN Surge protection and CN7 pin9 connect to GND |
| | | Page 22: Change VRAM Footprint to follow BY3 VRAM |
| | | Page 23: Change VRAM Footprint to follow BY3 VRAM |
| | | Page 38: Add MOS to support LED EC pin change from low-active to high-active |
| | | Page 27: Reverse R261,R275,R288,R281 for HDMI EA fail |
| | | Page 43: Reverse PC196 and change PL11 footprint for support Celeron CPU and change PR121 value to 66.5K/F_4 |
| | | Page 5: Add R9559/R9560 for support Celeron CPU |
| | | Page 44: Change VCCSA schematic value to add i3@ for option i357 / Celeron CPU |
| | | Page 38: Change HOLE1 to connect to GND |
| | | Page 22: Del R635,R636,C648,C532,R501,R502 and change R634/R506 value to 160/F_4 for NV suggestion |
| | | Page 23: Change VMA_ZQ1~4 netname to VMA_ZQ5~8 for layout |
| | | Page 37: Change R166 Value to 100K_4 PD |

MODEL: MTC/MTD

| PAGE | FROM | To |
|---|---|---|
| 1 | 1A | |
| 2 | 1A | |
| 3 | 1A | |
| 4 | 1A | |
| 5 | 1A | |
| 6 | 1A | |
| 7 | 1A | |
| 8 | 1A | |
| 9 | 1A | |
| 10 | 1A | |
| 11 | 1A | |
| 12 | 1A | |
| 13 | 1A | |
| 14 | 1A | |
| 15 | 1A | |
| 16 | 1A | |
| 17 | 1A | |
| 18 | 1A | |
| 19 | 1A | |
| 20 | 1A | |
| 21 | 1A | |
| 22 | 1A | |
| 23 | 1A | |
| 24 | 1A | |
| 25 | 1A | |
| 26 | 1A | |
| 27 | 1A | |
| 28 | 1A | |
| 29 | 1A | |
| 30 | 1A | |

**DOC NO. 204**

| | | | | | |
|---|---|---|---|---|---|
| PROJECT MODEL : | BY3E,BY4E | APPROVED BY: | | DATE: | |
| PART NUMBER: | | DRAWING BY: | | REVISON: | |

Quanta Computer Inc.

PROJECT : MTC_MTCD

Size | Document Number: Change list | Rev: 1A

Date: Friday, December 28, 2012 | Sheet 49 of 49