MODEL NAME : DAM00
DAM01

PCB NO : LA-F541P

BOM P/N :

Dell/Compal Confidential

Schematic Document

Berlinetta MLK CFL-H (Coffee Lake-H)

2018-01-10

Rev: DVT2.0

@ : Nopop Component
NDS3@ : Nopop Component
XDP@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
TPM@ : TPM funct i on
EMC@ : Pop of EMI parts
Q1VRAMS@ : Samsung GDDR5 for Q1-GPU
Q1VRAMM@ : Micron GDDR5 for Q1-GPU
G0VRAMS@ : Samsung GDDR5 for G0-GPU
G0VRAMM@ : Micron GDDR5 for G0-GPU
G0VRAMH@ : Hynix GDDR5 for G0-GPU
BreakDown@ : for measure power consumpt i on
Q1@ : GPU N18PQ1
G0@ : GPU N17PG0
UMA@ / DIS@ : UMA/DIS
CSMB@ :XPS
BC@ :Perision
SPAD@ : Nopop Component 0 Ohm Short-PAD for NPI test require
eSPI@ :eSPI
G1@ : GPU N17PG1
Q3@ : GPU N18PQ3

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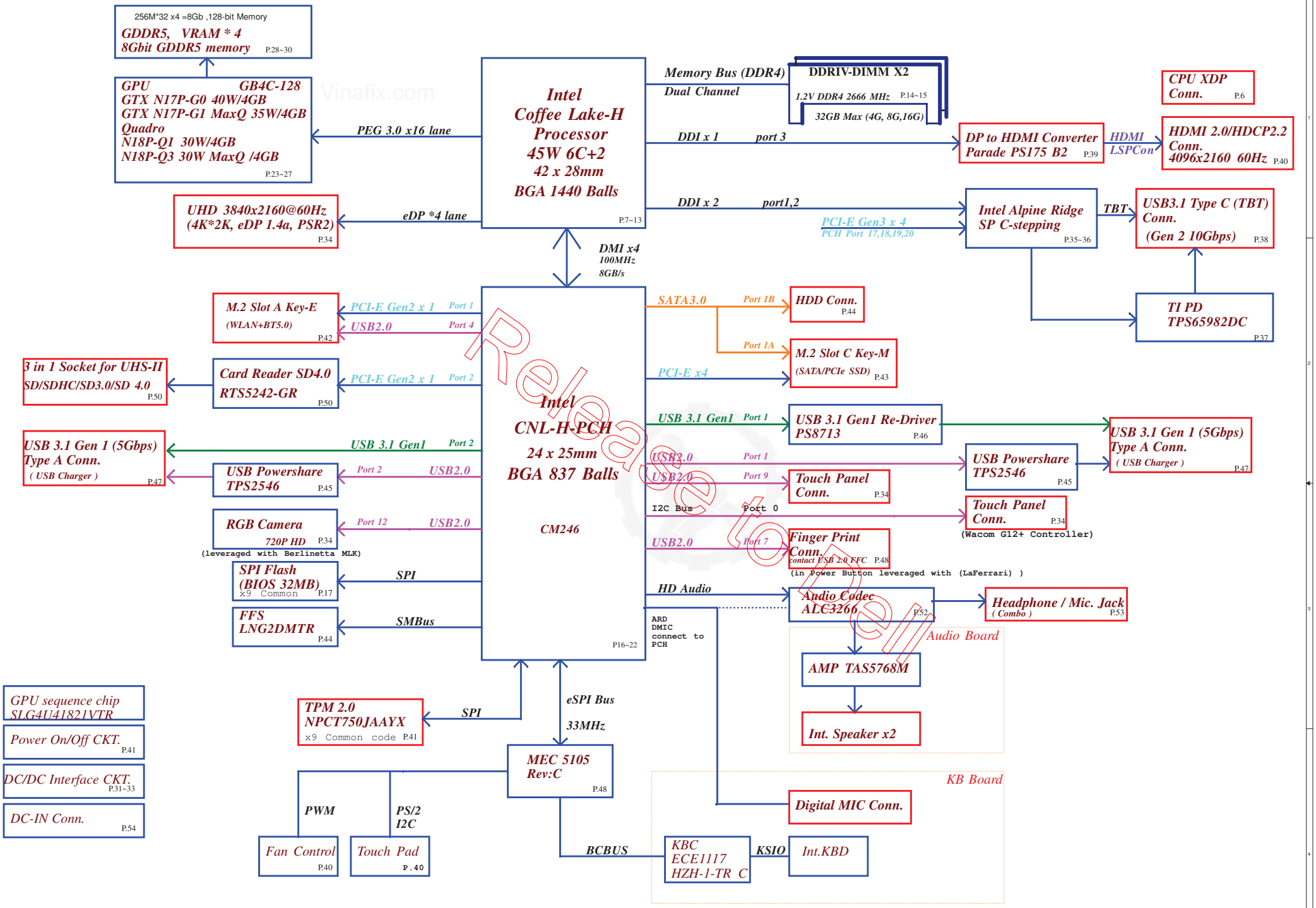
Title: P01-Cover Page

Size	Document Number	Rev
	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 Sheet 1 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P02-Block Diagram

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

Date: Friday, March 23, 2018 Sheet 2 of 76

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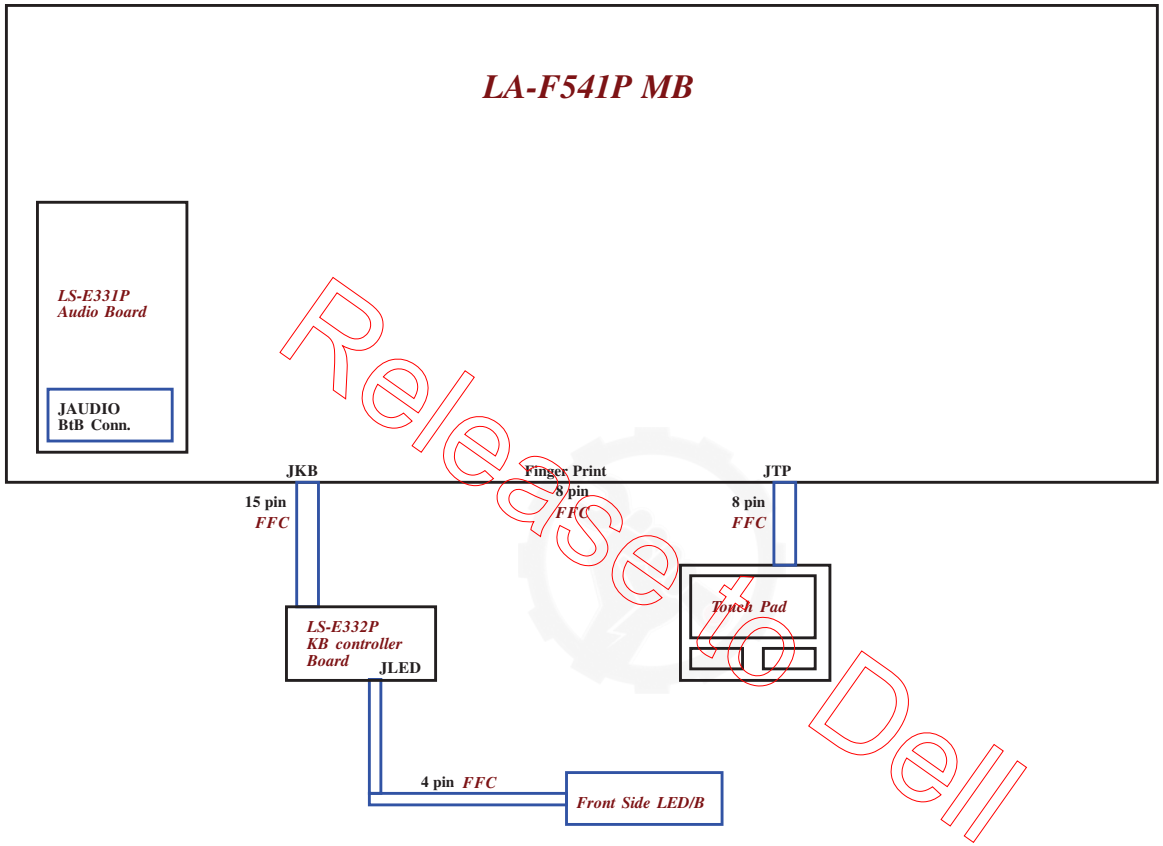
Project Code : DAM00 / DAM01
File Name :



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Title: **P03-Daughter/B block diagram**

Size	Document Number	Rev
		0.1(X00)

Date: Friday, March 23, 2018 Sheet 3 of 76

Board ID	Resistor
X00	240K
X01	130K
X02	
X03	
A00	

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	Touch Screen
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION
Lane 1	NGFF-1 WLAN + BT
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	CARD READER
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	None
Lane 16	None
Lane 17	Alpine Ridge
Lane 18	
Lane 19	
Lane 20	

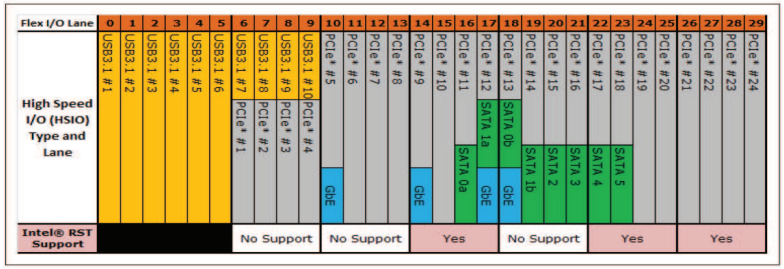
USB3.0	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	N/A
1A	SSD
0B	N/A
1B	N/A
2	HDD
3	N/A
4	N/A
5	N/A

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT



The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 Intel® Optane™ Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: P04-Notes List

Size | Document Number: LA-F541P | Rev: 0.1(X00)

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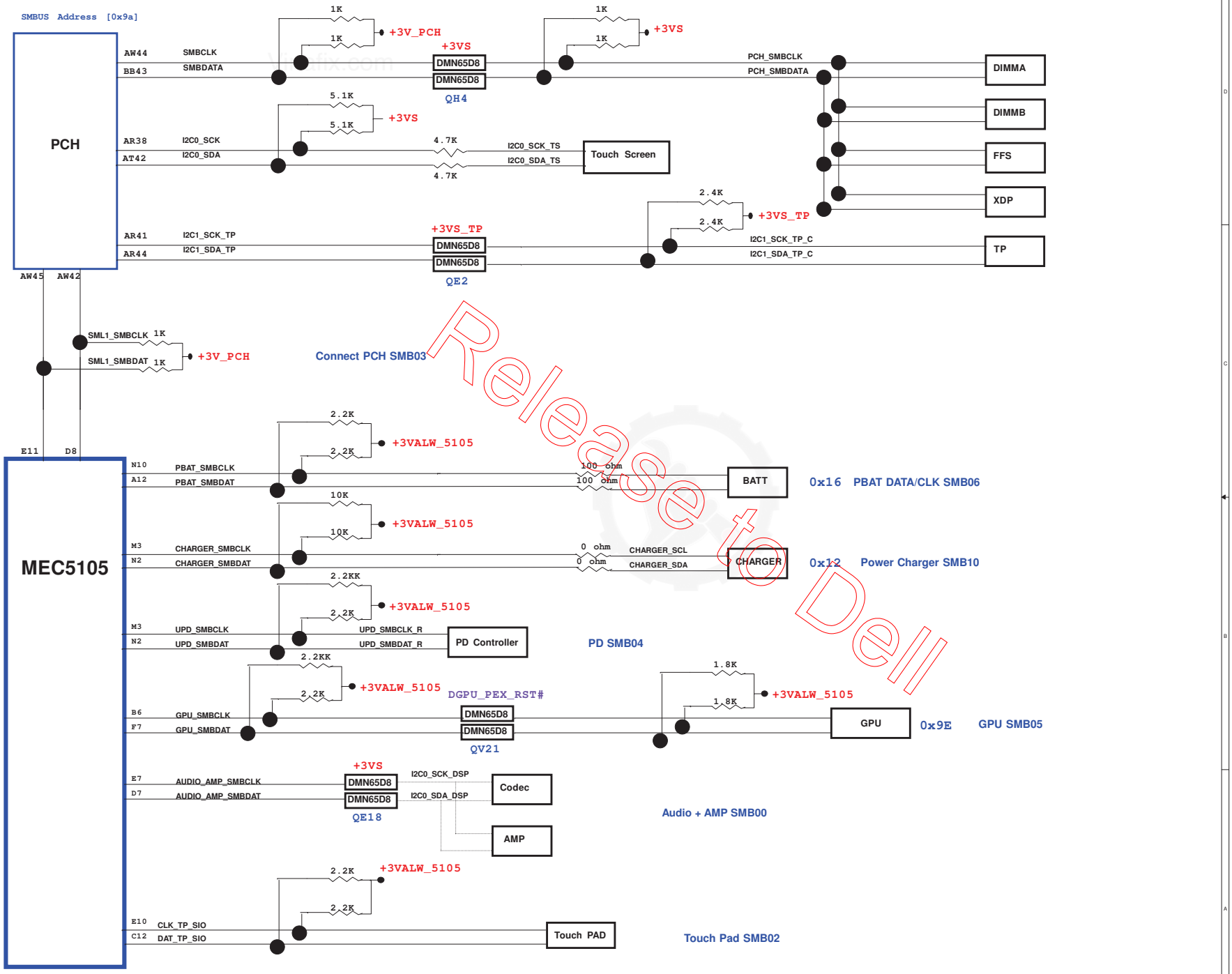

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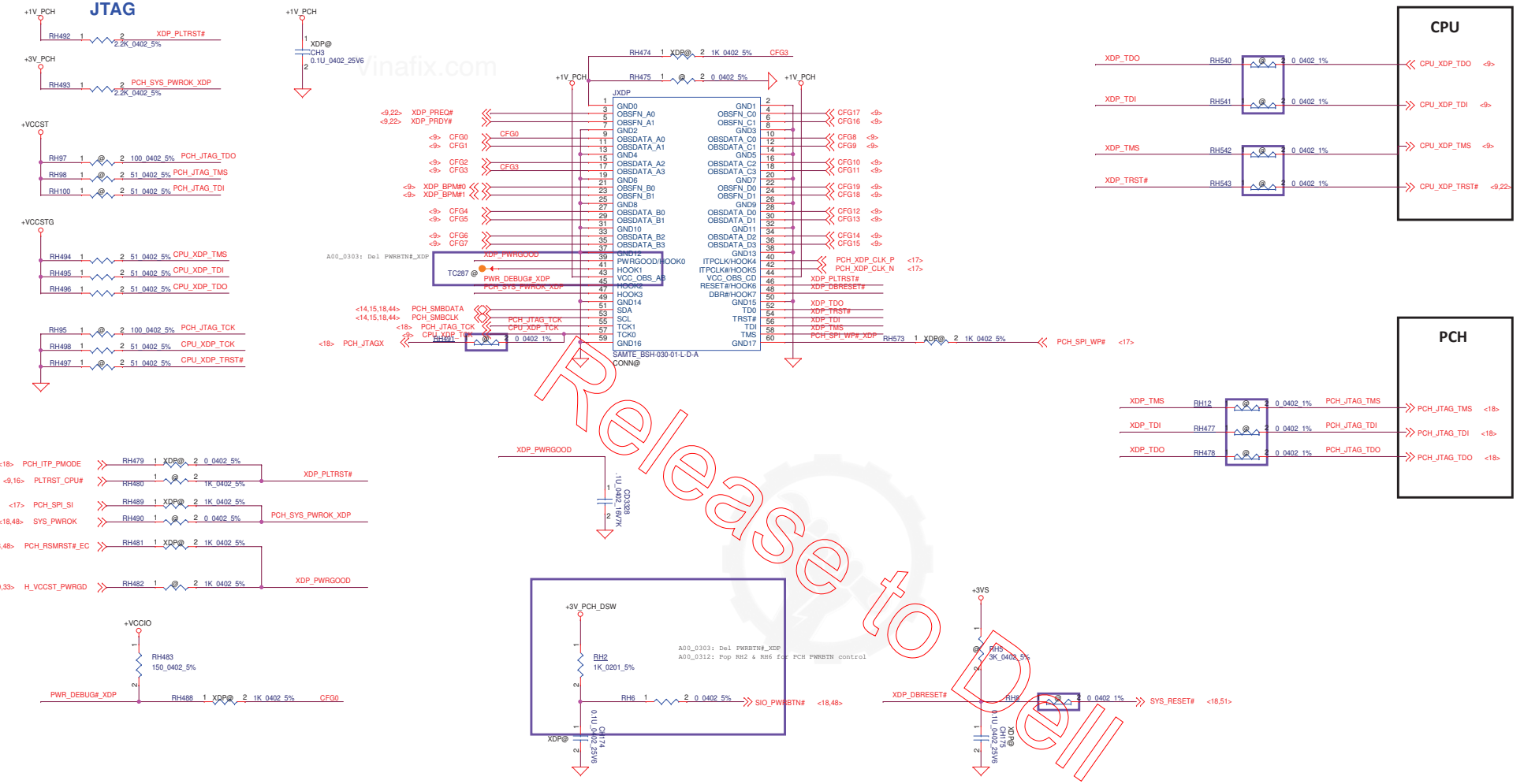
Title: P05-SMBus block diagram

Size	Document Number	Rev
Custom		0.1(X00)

Date: Friday, March 23, 2018 Sheet 5 of 76



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Compal Electronics, Inc.

Title: **P06-XDP CONN**

Size	Document Number	Rev
		0.1(X00)

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Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P07-CPU(1/7) DMI,PEG,DDI,EDP**

Size	Document Number	Rev
C		0.1(000)

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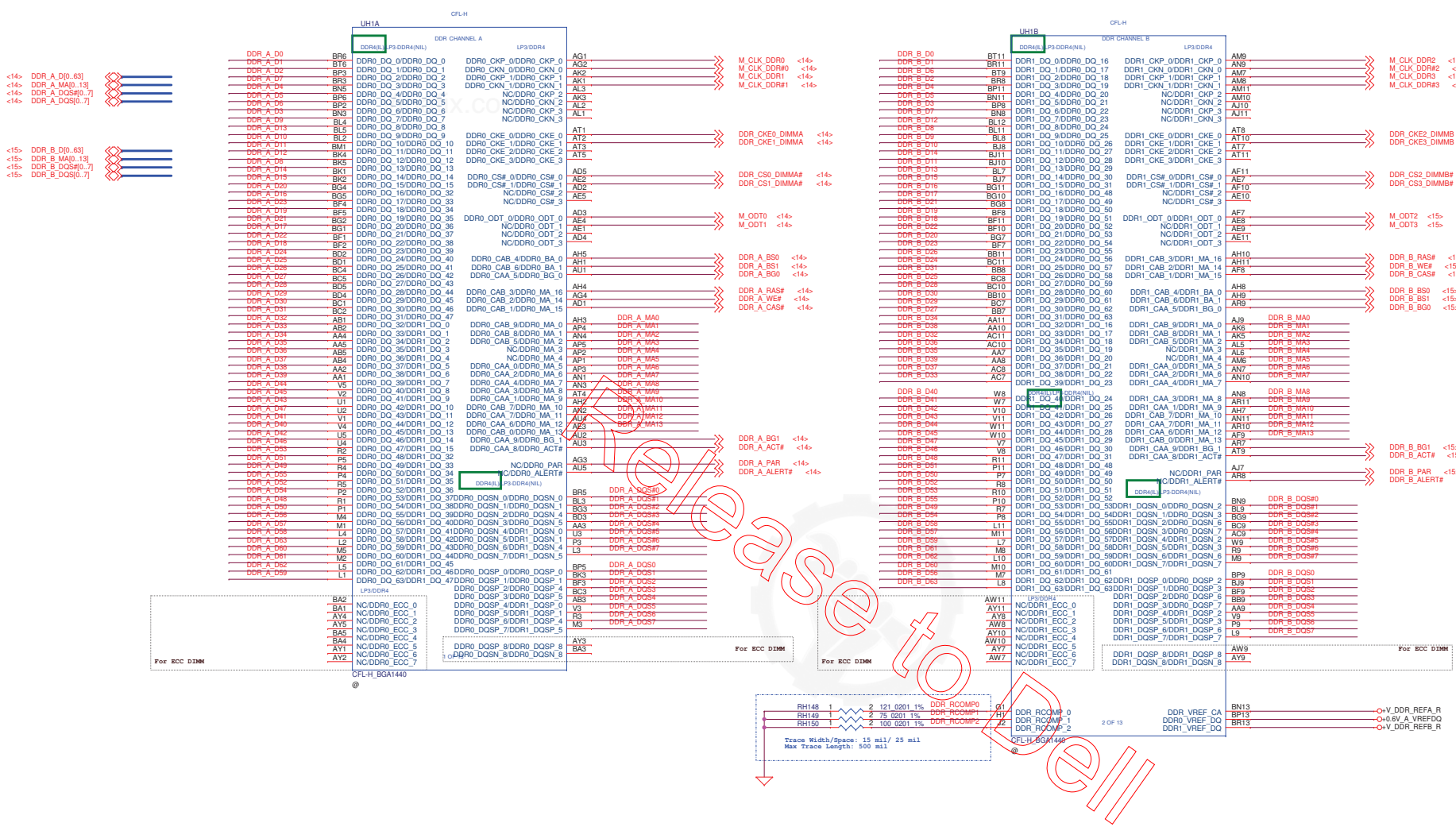
Interleave



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Title: **P08-CPU(2/7) DDR4**

Size	Document Number	Rev
C		0.1(X00)

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CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	★11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

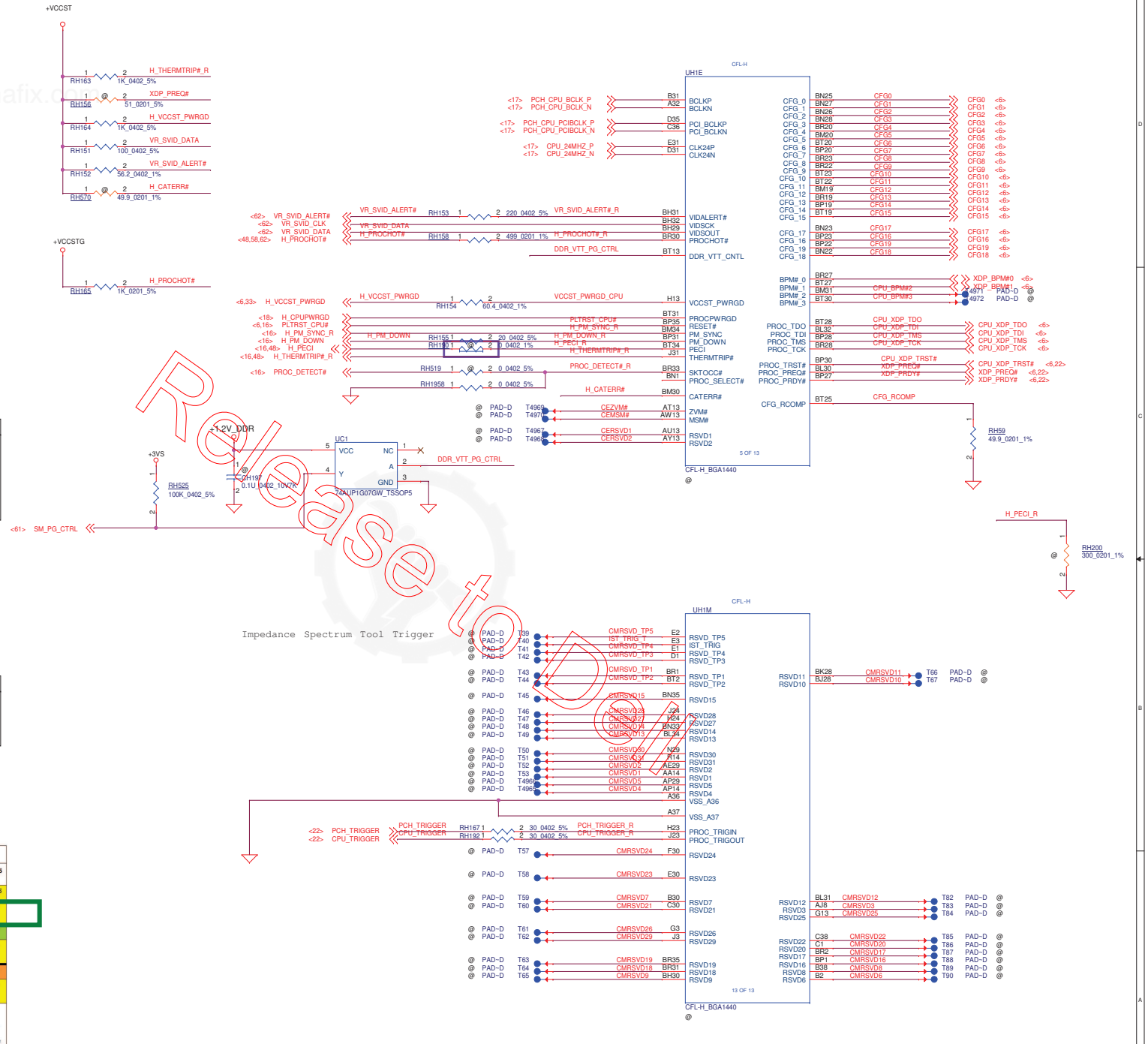
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lanes device should use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
4. for reversal lanes, for example:
   When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
5. For Basin Falls platform use 1x8+2x4 Bifurcation



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Title: P09-CPU(3/7) RSVD,CFG,XDP

Size	Document Number	Rev
C		0.1(X00)

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Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Title: *P10-CPU(4/7) PWR,VCore,RSVD*

Size	Document Number	Rev
Custom		0.1(X00)

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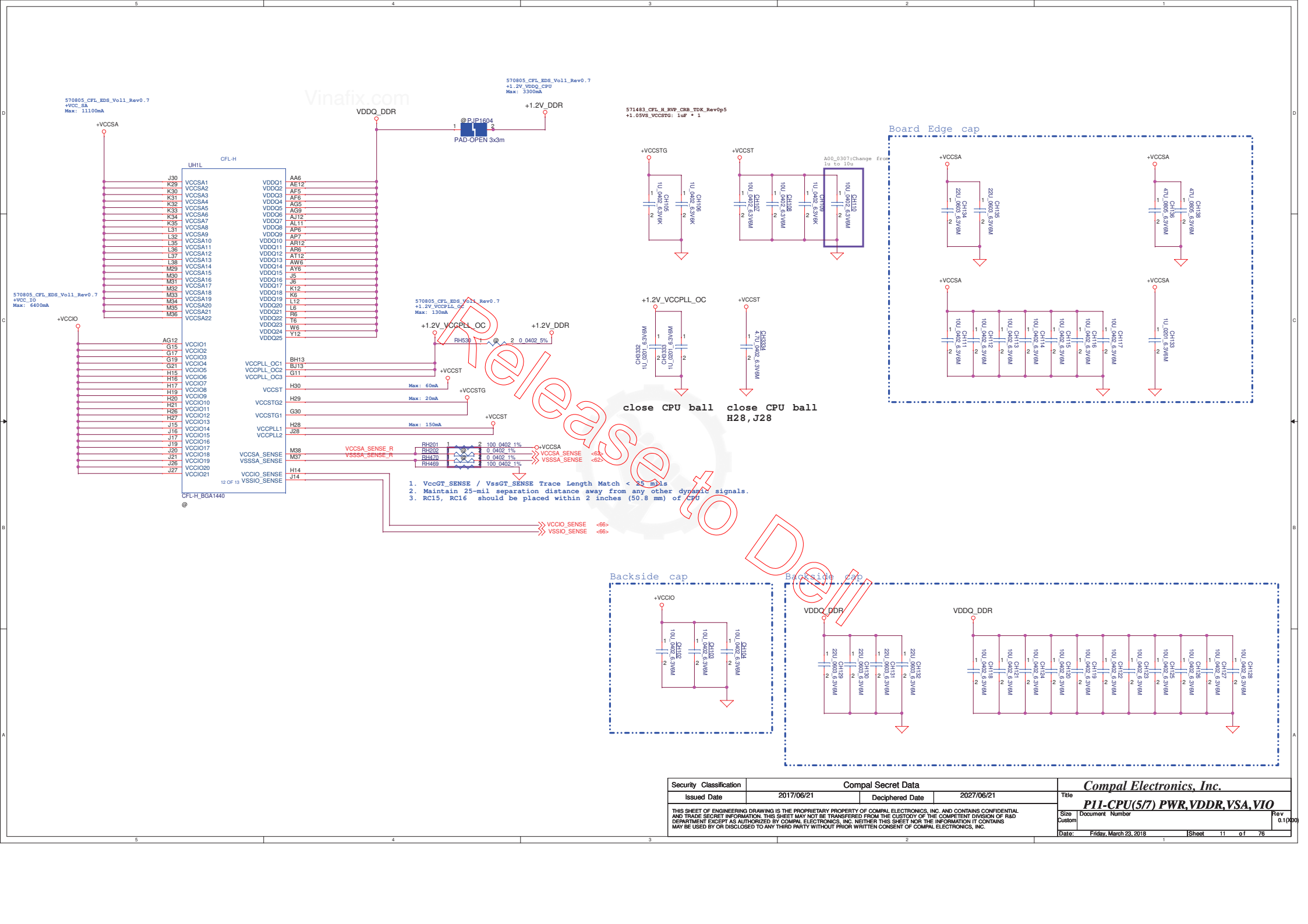

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P11-CPU(5/7) PWR,VDDR,VSA,VIO

Size	Document Number	Rev
Custom		0.1(X00)

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GT
55000mA(Hexa Core GT2)

+VCCGT

+VCCGT

CFL-H

UH1K

AT14	VCCGT1	VCCGT80	BD35
AT31	VCCGT2	VCCGT81	BD36
AT32	VCCGT3	VCCGT82	BE31
AT33	VCCGT4	VCCGT83	BE32
AT34	VCCGT5	VCCGT84	BE33
AT35	VCCGT6	VCCGT85	BE34
AT36	VCCGT7	VCCGT86	BE35
AT37	VCCGT8	VCCGT87	BE36
AT38	VCCGT9	VCCGT88	BE37
AU14	VCCGT10	VCCGT89	BE38
AU29	VCCGT11	VCCGT90	BF13
AU30	VCCGT12	VCCGT91	BF14
AU31	VCCGT13	VCCGT92	BF29
AU32	VCCGT14	VCCGT93	BF30
AU35	VCCGT15	VCCGT94	BF31
AU36	VCCGT16	VCCGT95	BF32
AU37	VCCGT17	VCCGT96	BF35
AU38	VCCGT18	VCCGT97	BF36
AV29	VCCGT19	VCCGT98	BF37
AV30	VCCGT20	VCCGT99	BF38
AV31	VCCGT21	VCCGT100	BG29
AV32	VCCGT22	VCCGT101	BG30
AV33	VCCGT23	VCCGT102	BG31
AV34	VCCGT24	VCCGT103	BG32
AV35	VCCGT25	VCCGT104	BG33
AV36	VCCGT26	VCCGT105	BG34
AW14	VCCGT27	VCCGT106	BG35
AW31	VCCGT28	VCCGT107	BG36
AW32	VCCGT29	VCCGT108	BH33
AW33	VCCGT30	VCCGT109	BH34
AW34	VCCGT31	VCCGT110	BH35
AW35	VCCGT32	VCCGT111	BH36
AW36	VCCGT33	VCCGT112	BH37
AW37	VCCGT34	VCCGT113	BH38
AW38	VCCGT35	VCCGT114	BJ16
AY29	VCCGT36	VCCGT115	BJ17
AY30	VCCGT37	VCCGT116	BJ19
AY31	VCCGT38	VCCGT117	BJ20
AY32	VCCGT39	VCCGT118	BJ21
AY35	VCCGT40	VCCGT119	BJ23
AY36	VCCGT41	VCCGT120	BJ24
AY37	VCCGT42	VCCGT121	BJ26
AY38	VCCGT43	VCCGT122	BJ27
BA13	VCCGT44	VCCGT123	BJ37
BA14	VCCGT45	VCCGT124	BJ38
BA29	VCCGT46	VCCGT125	BK16
BA30	VCCGT47	VCCGT126	BK17
BA31	VCCGT48	VCCGT127	BK19
BA32	VCCGT49	VCCGT128	BK20
BA33	VCCGT50	VCCGT129	BK21
BA34	VCCGT51	VCCGT130	BK23
BA35	VCCGT52	VCCGT131	BK24
BA36	VCCGT53	VCCGT132	BK26
BB13	VCCGT54	VCCGT133	BK27
BB14	VCCGT55	VCCGT134	BL15
BB31	VCCGT56	VCCGT135	BL16
BB32	VCCGT57	VCCGT136	BL17
BB33	VCCGT58	VCCGT137	BL23
BB34	VCCGT59	VCCGT138	BL24
BB35	VCCGT60	VCCGT139	BL25
BB36	VCCGT61	VCCGT140	BL26
BB37	VCCGT62	VCCGT141	BL27
BB38	VCCGT63	VCCGT142	BL28
BC29	VCCGT64	VCCGT143	BL36
BC30	VCCGT65	VCCGT144	BL37
BC31	VCCGT66	VCCGT145	BM15
BC32	VCCGT67	VCCGT146	BM16
BC35	VCCGT68	VCCGT147	BM17
BC36	VCCGT69	VCCGT148	BM36
BC37	VCCGT70	VCCGT149	BM37
BC38	VCCGT71	VCCGT150	BN15
BD13	VCCGT72	VCCGT151	BN16
BD14	VCCGT73	VCCGT152	BN17
BD29	VCCGT74	VCCGT153	BN36
BD30	VCCGT75	VCCGT154	BN37
BD31	VCCGT76	VCCGT155	BN38
BD32	VCCGT77	VCCGT156	BP15
BD33	VCCGT78	VCCGT157	BP16
BD34	VCCGT79	VCCGT158	BP17
BP37	VCCGT159	VCCGT164	BR37
BP38	VCCGT160	VCCGT165	BT15
BR15	VCCGT161	VCCGT166	BT16
BR16	VCCGT162	VCCGT167	BT17
BR17	VCCGT163	VCCGT168	BT37

11 OF 11

AH37	VSSGT_SENSE	VSSGT_SENSE_R	RH204 0_0402_1%
AH38	VCCGT_SENSE	VCCGT_SENSE_R	RH471 0_0402_1%

CFL-H_BGA1440

@

+VCCGT

RH203
100_0402_1%

RH472
100_0402_1%

VSSGT_SENSE <62>
VCCGT_SENSE <62>

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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Title: P12-CPU(6/7) PWR,VGT

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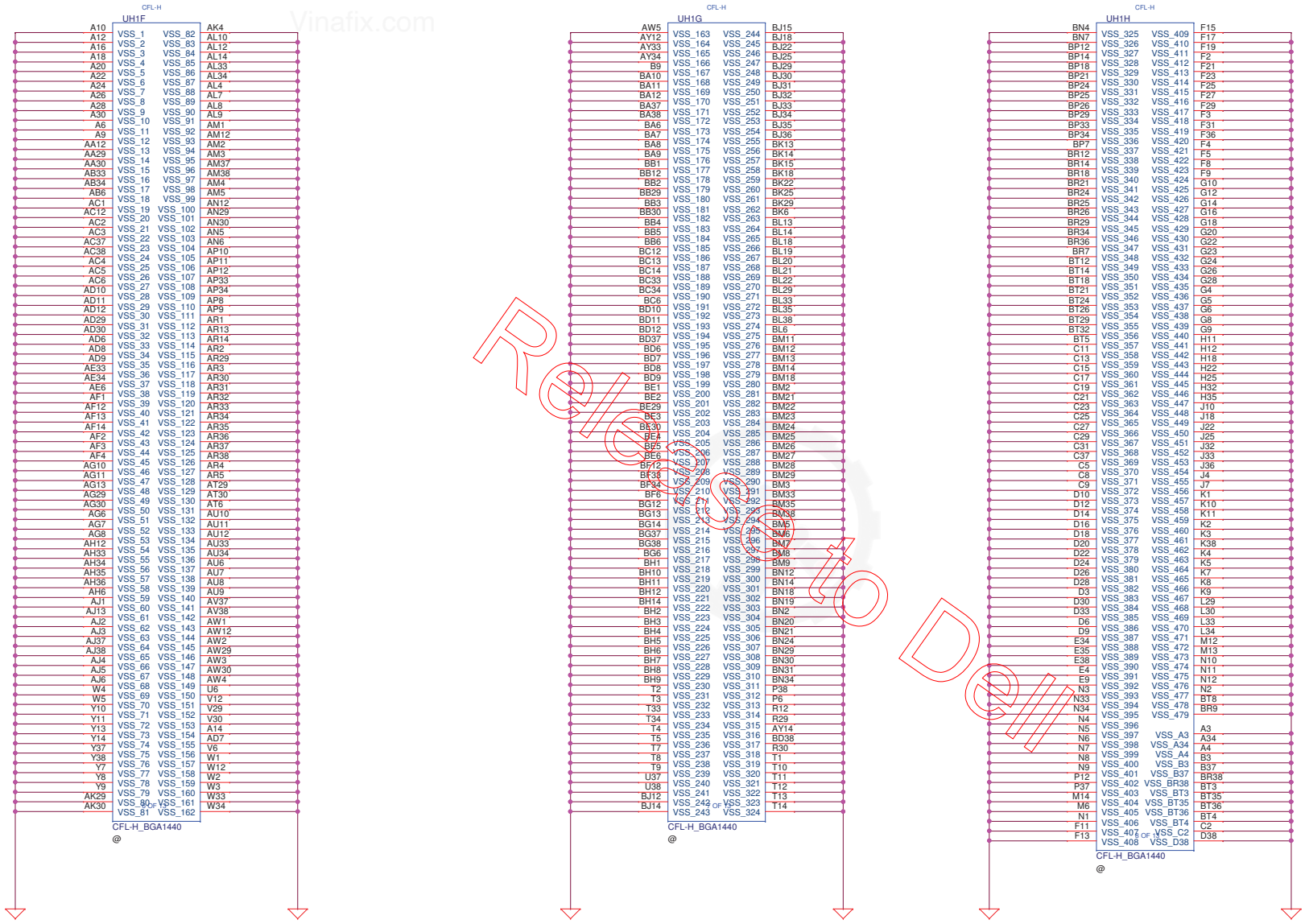

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Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P13-CPU(7/7) VSS

Size	Document Number	Rev
Custom		0.1(X00)

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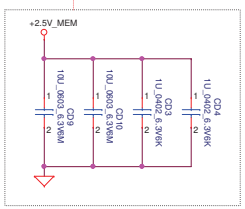
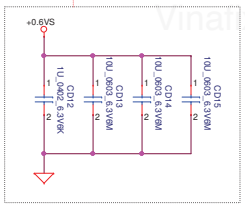
Layout Note:
Place near JDIMM1.257,259

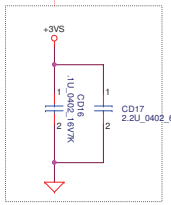
Layout Note:
Place near JDIMM1.258

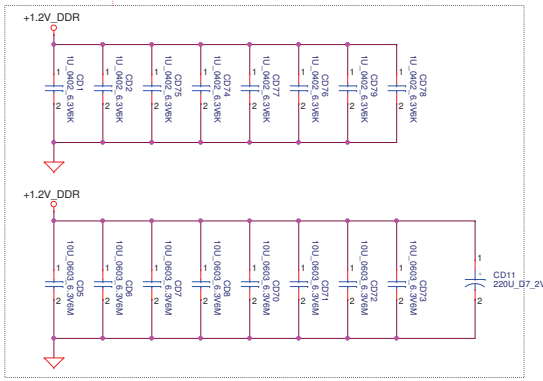
Layout Note:
Place near JDIMM1.255

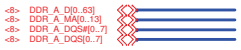
Layout Note:
Place near JDIMM1

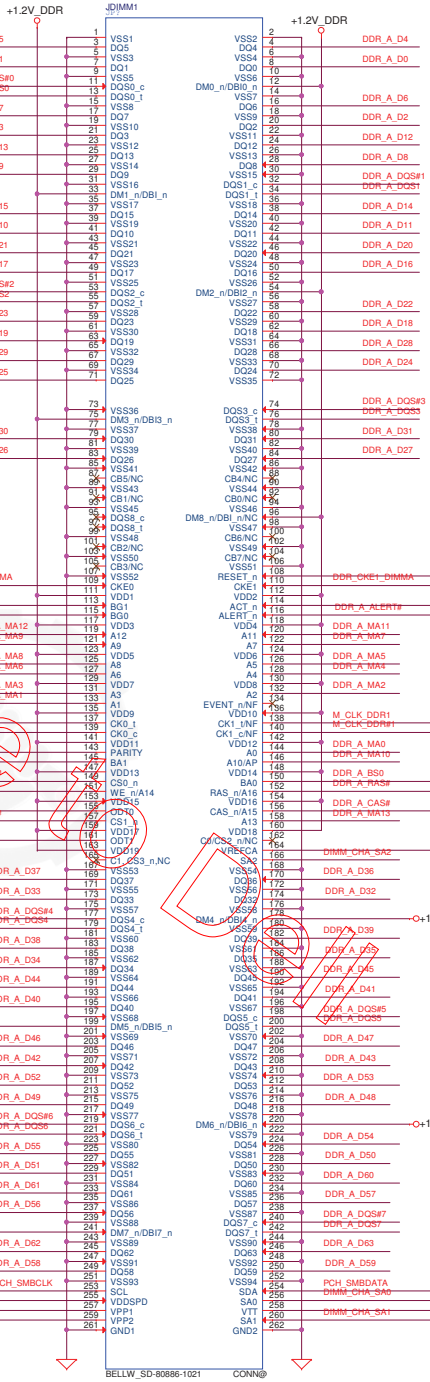


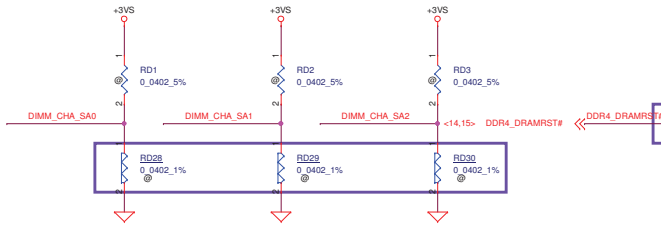


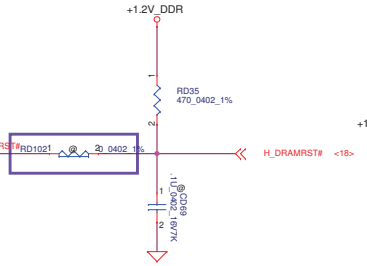




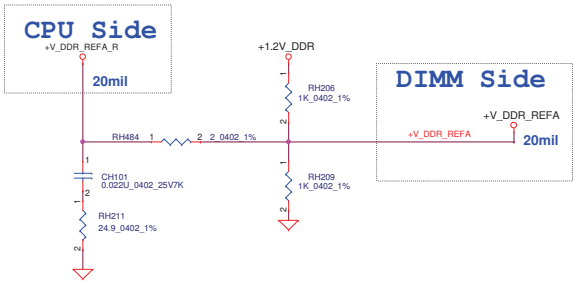








VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



All VREF traces should have 10 mil trace width

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Title: P14-DDR4 DIMMA

Size	Document Number	Rev
	LA-F541P	0.1(000)

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Layout Note:
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Layout Note:
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Layout Note:
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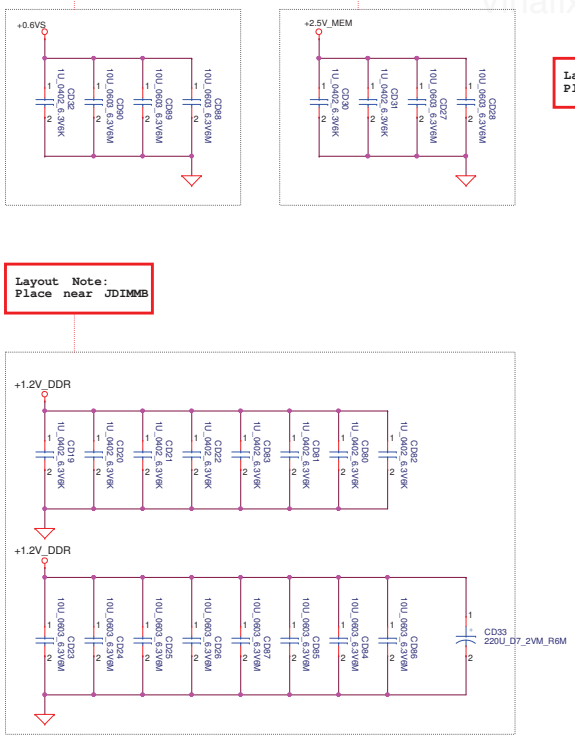
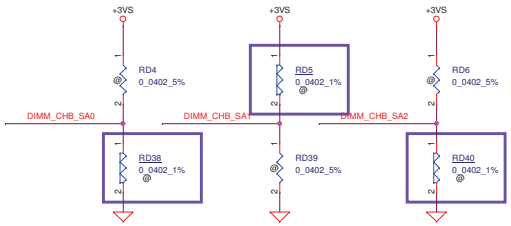
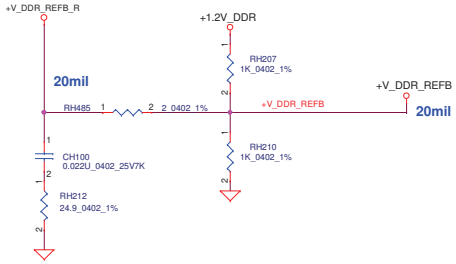
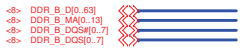
Layout Note:
Place near JDIMMB

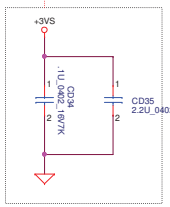


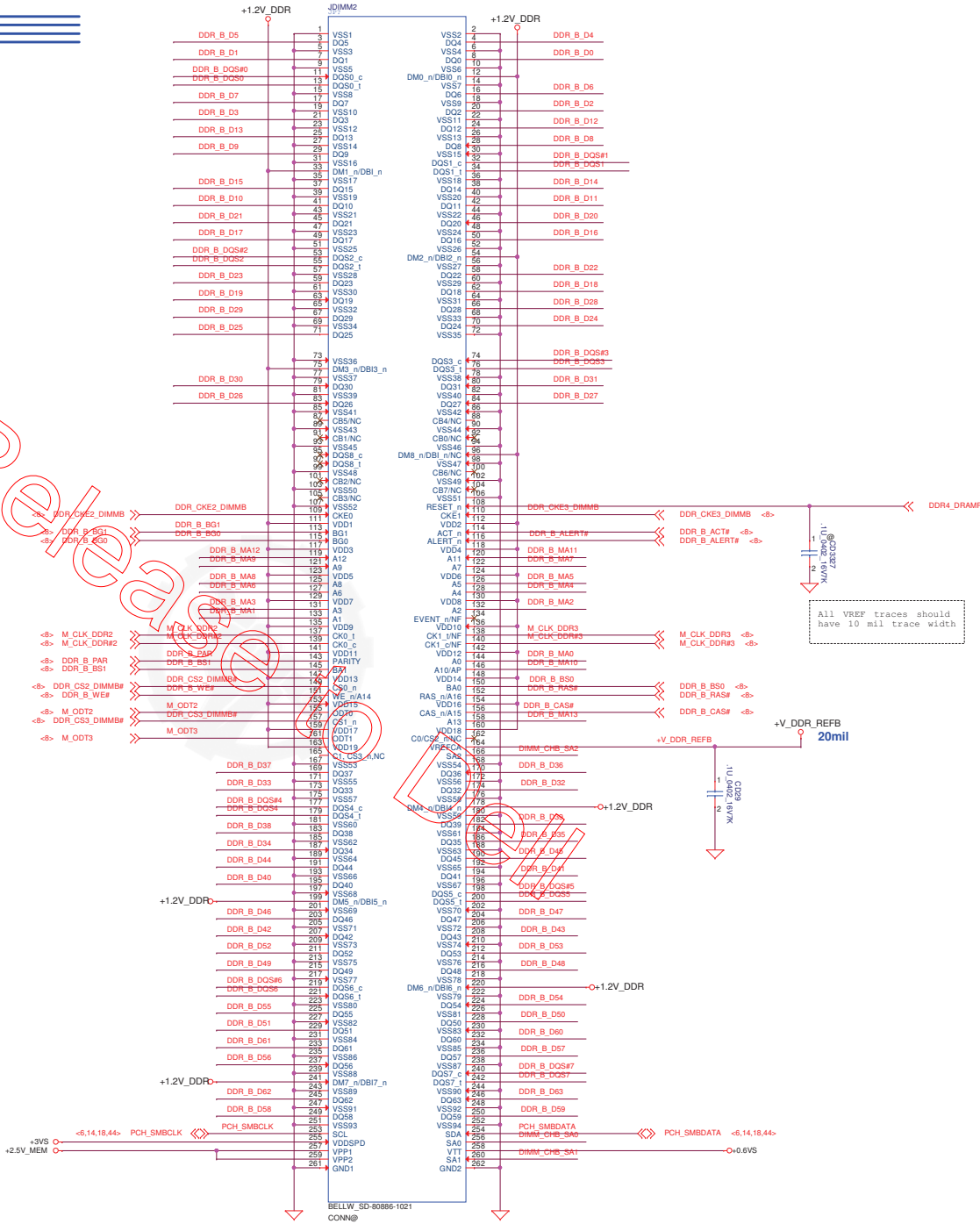


VREF traces should be at least 20 mils wide with 20 mils spacing to other signals









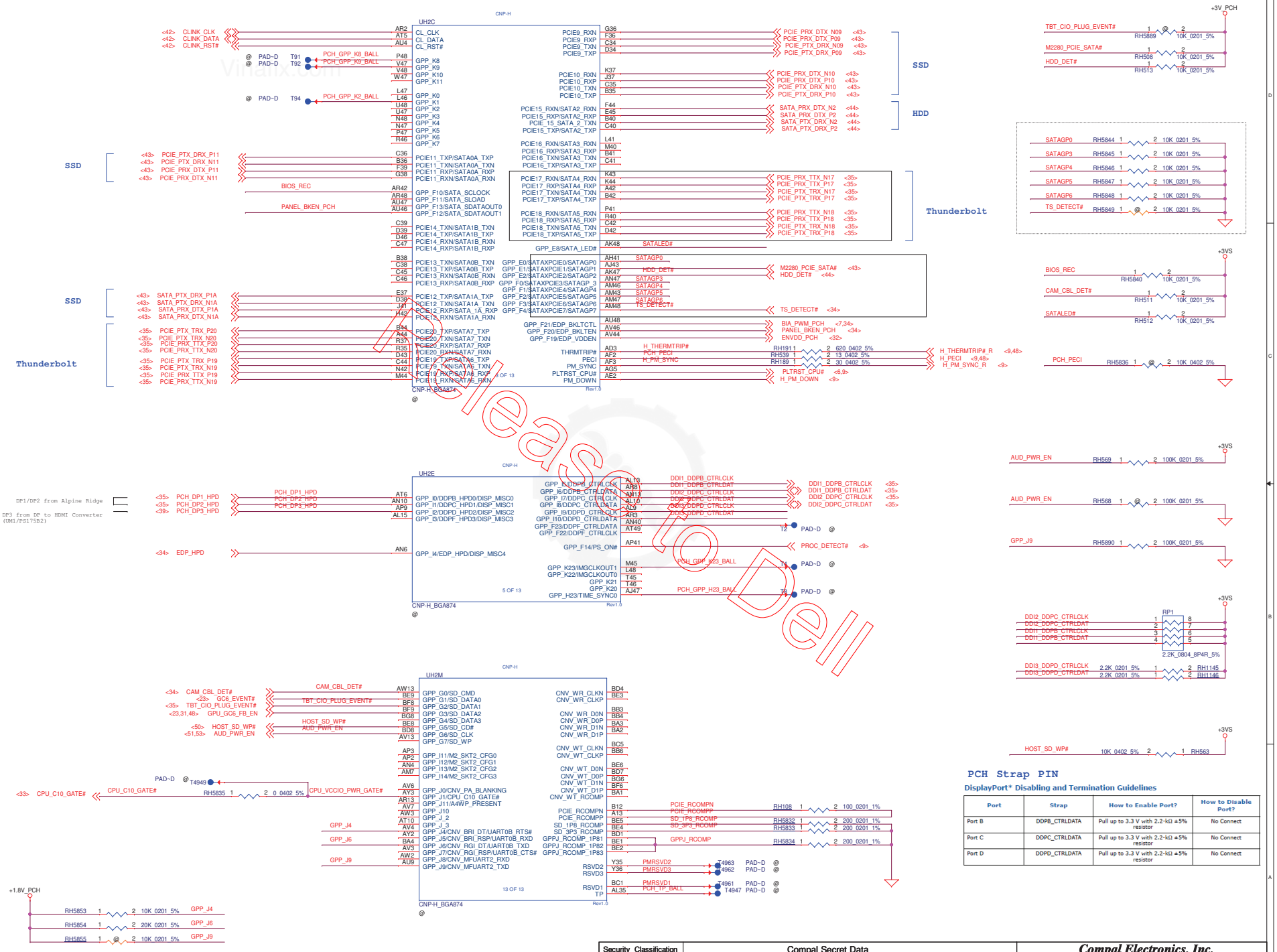
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P15-DDR4 DIMMB

Size	Document Number	Rev
	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 15 of 76


UH2C
CNP-H
CNP-H_BGA874
Rev1.0
SSD
HDD
Thunderbolt
UH2E
UH2M
13 OF 13
PCH Strap PIN
DisplayPort* Disabling and Termination Guidelines
Port | Strap | How to Enable Port? | How to Disable Port?
Port B | DDPB_CTRLDATA | Pull up to 3.3 V with 2.2-kΩ ±5% resistor | No Connect
Port C | DDPC_CTRLDATA | Pull up to 3.3 V with 2.2-kΩ ±5% resistor | No Connect
Port D | DDPD_CTRLDATA | Pull up to 3.3 V with 2.2-kΩ ±5% resistor | No Connect
Security Classification
Compal Secret Data
Issued Date
2017/06/21
Deciphered Date
2027/06/21
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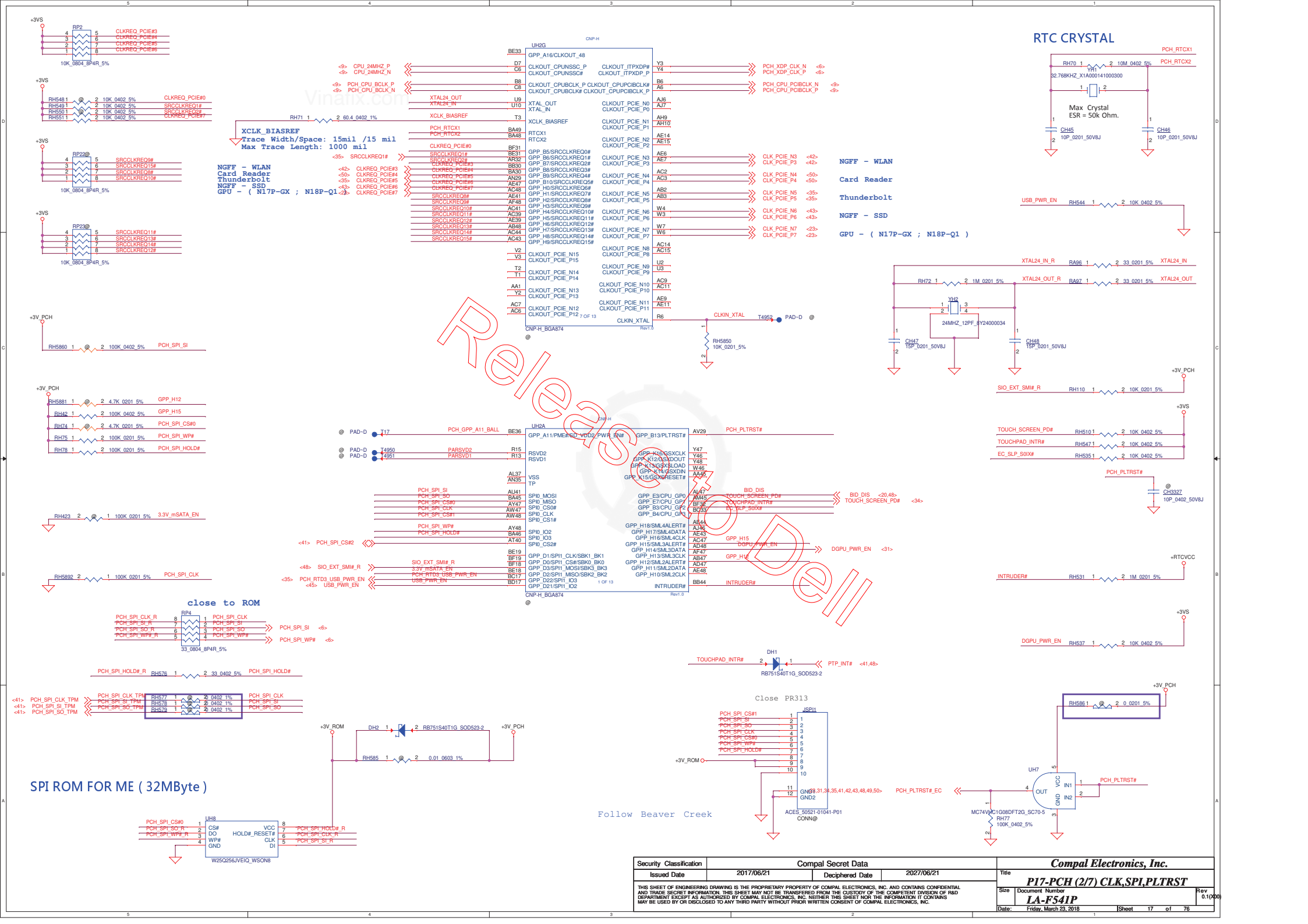
Compal Electronics, Inc.
Title
P16-PCH (1/7) SATA,DDC,PCIE,CNV
Size
Document Number
LA-F541P
Rev
0.1(000)
Date: Friday, March 23, 2018
Sheet 16 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

Title: P17-PCH (2/7) CLK,SPI,PLTRST

Size	Document Number	Rev
	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 17 of 76

HDA_SDO / I2S0_TXD

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
1=Disable ME Protect (ME can be updated) 0=Enable ME Protect (ME cannot be updated)

RP15 33_0804_8P4R_5%

HDA_SDIN0 EMI@ CD3324 2P_0201_25V8B

HDA_SDOUT EMI@ CD3325 2P_0201_25V8B

+RTCVCC

PCH_SRTCRST# RH83 20K 0201 5%

CH52 1U_0402_6.3V6K

PCH_RTCRST# RH84 20K 0201 5%

close to BOT

CH53 1U_0402_6.3V6K CLRP1 SHORT PADS

+3V_PCH

MEM_SMBCLK RH458 1K 0201 5%

MEM_SMBDATA RH459 1K 0201 5%

SML1_SMBCLK RH460 1K 0201 5%

SML1_SMBDAT RH461 1K 0201 5%

SML0_SMBCLK RH501 1K 0201 1%

SML0_SMBDAT RH502 1K 0201 1%

KB_DET# RH557 10K 0402 5%

+3VS

PCH_SMBCLK RH463 1K 0201 5%

PCH_SMBDATA RH462 1K 0201 5%

DGPU_PWROK RH516 10K 0201 5%

SYS_PWROK RH91 100K 0201 5%

PCH_RSMRST#_R RH5841 10K 0201 5%

PCH_DPWROK_R RH401 100K 0201 5%

SIO_SLP_A# RH1152 100K 0201 5%

SIO_SLP_S3# RZ1150 100K 0201 5%

SIO_SLP_S4# RZ1151 100K 0201 5%

<52> HDA_SDIN0_AUDIO RH96 0 0201 5%

HDA_BITCLK HDA_SDIN0 HDA_SDOUT HDA_SYNC HDA_RST#

Close to PCH

<7> AUD_AZA_CPU_SDO RH146 30 0201 1% AUD_AZA_CPU_SDO_R

<7> AUD_AZA_CPU_SDI_R RH147 30 0201 1% AUD_AZA_CPU_SDI_R

<7> AUD_AZA_CPU_SCLK AUD_AZA_CPU_SCLK_R

@ PAD-D T121 PCH_GPP_D7_BALL

<51> PCH_DMIC_DAT_R RA102 33 0402 5% PCH_DMIC_DAT

<51> PCH_DMIC_CLK_R RA103 33 0402 5% PCH_DMIC_CLK

<23,71> DGPU_PWROK

<51> KB_DET#

<51> PCH_RTCRST# PCH_RTCRST# PCH_SRTCRST#

<6,48> PCH_RSMRST#_EC RH133 0 0402 1% PCH_RSMRST#_R

RH5859 0 0402 5%

RH309 1 0 0402 5% PCH_PWROK

<48> PCH_DPWROK_EC PCH_DPWROK_R

PCH_SMB_ALERT#

MEM_SMBCLK

MEM_SMBDATA

SML0ALERT#

SML0_SMBCLK

SML0_SMBDATA

SML1ALERT#

<48> SML1_SMBCLK SML1_SMBCLK

<48> SML1_SMBDAT SML1_SMBDAT

UH2D CNP-H

BD11	HDA_BCLK/I2S0_SCLK	GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#	BF36
BE11	HDA_SDI/I2S0_RXD	GPP_A8/CLKRUN#	AV32 CLKRUN#
BF12	HDA_SDO/I2S0_TXD	GPD11/LANPHYPC	BF41 PM_LANPHY_ENABLE
BG13	HDA_SYNC/I2S0_SFRM	GPD9/SLP_WLAN#	BD42 SIO_SLP_WLAN#
BE10	HDA_RST#/I2S1_SCLK	DRAM_RESET#	BB46
BF10	HDA_SDI/I2S1_RXD	GPP_B2/VRALERT#	BE32 VRALERT#
BE12	I2S1_TXD/SNDW2_DATA	GPP_B1/GSPI1_CS#/TIME_SYNC1	BF33
BD12	I2S1_SFRM/SNDW2_CLK	GPP_B0/GSPI0_CS1#	BE29 TS_I2C_RST#
AM2	HDACPU_SDO	GPP_K17/ADR_COMPLETE	R47
AN3	HDACPU_SDI	GPP_B11/I2S_MCLK	AP29 I2C2_IRQ_TS
AM3	HDACPU_SCLK	SYS_PWROK	AU3 SYS_PWROK
AV18	GPP_D8/I2S2_SCLK	WAKE#	BB47 PCH_PCIE_WAKE#
AW18	GPP_D7/I2S2_RXD	GPD6/SLP_A#	BE40 SIO_SLP_A#
BA17	GPP_D6/I2S2_TXD/MODEM_CLKREQ	SLP_LAN#	BF40 PCH_SLP_LAN#
BE16	GPP_D5/I2S2_SFRM/CNV_RF_RESET#	GPP_B12/SLP_S0#	BC28
BF15	GPP_D20/DMIC_DATA0/SNDW4_DATA	GPD4/SLP_S3#	BF42
BD16	GPP_D19/DMIC_CLK0/SNDW4_CLK	GPD5/SLP_S4#	BE42 SIO_SLP_S4#
AV16	GPP_D18/DMIC_DATA1/SNDW3_DATA	GPD10/SLP_S5#	BC42
AW15	GPP_D17/DMIC_CLK1/SNDW3_CLK	GPD8/SUSCLK	BE45 SUSCLK <42,43>
BE47	RTCRST#	GPD0/BATLOW#	BF44 PCH_BATLOW#
BD46	SRTCRST#	GPP_A15/SUSACK#	BE35 SUSACK#
AY42	PCH_PWROK	GPP_A13/SUSWARN#/SUSPWRDNACK	BC37 ME_SUS_PWR_ACK_R
AW41	DSW_PWROK	GPD2/LAN_WAKE#	BG44 LAN_WAKE#
BE25	GPP_C2/SMBALERT#	GPD1/ACPRESENT	BG42 AC_PRESENT
BE26	GPP_C0/SMBCLK	SLP_SUS#	BD39
BF26	GPP_C1/SMBDATA	GPD3/PWRBTN#	BE46
BF24	GPP_C5/SML0ALERT#	SYS_RESET#	AU2 SYS_RESET#
BF25	GPP_C3/SML0CLK	GPP_B14/SPKR	AW29 SPKR
BE24	GPP_C4/SML0DATA	CPUPWRGD	AE3
BD33	GPP_B23/SML1ALERT#/PCHHOT#	ITP_PMODE	AL3 PCH_ITP_PMODE
BF27	GPP_C6/SML1CLK	PCH_JTAGX	AH4 PCH_JTAGX
BE27	GPP_C7/SML1DATA	PCH_JTAG_TMS	AJ4 PCH_JTAG_TMS
		PCH_JTAG_TDO	AH3 PCH_JTAG_TDO
		PCH_JTAG_TDI	AH2 PCH_JTAG_TDI
		PCH_JTAG_TCK	AJ3 PCH_JTAG_TCK

1 OF 12

CNP-H_BGA874 @ Rev1.0

+3VS_TS

I2C2_IRQ_TS RH5891 100K 0201 5%

+3V_PCH_DSW

PM_LANPHY_ENABLE RH5842 10K 0402 5%

PCH_PCIE_WAKE# RH453 1K 0402 5%

PCH_BATLOW# RH515 8.2K 0402 5%

AC_PRESENT RH533 8.2K 0402 5%

LAN_WAKE# RH545 10K 0201 5%

VRALERT# 4.7K 0402 5% RH5837

+3V_PCH

ME_SUS_PWR_ACK RH506 1M 0402 5%

SYS_RESET# RH571 8.2K 0402 5%

+3VS

CLKRUN# RH85 8.2K 0402 5%

+3V_PCH

SPKR 4.7K 0402 5% RH82

Top Swap Override (internal PD)	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

A00_0322:for BIOS setting, change BOM structure

<48> +3V_PCH

PCH_SMB_ALERT# 4.7K 0402 5% RH505

TLS CONFIDENTIALITY	
HIGH	vPRO
LOW(DEFAULT)	non-vPRO

+3V_PCH

SML0ALERT# 4.7K 0402 5% RH503

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

+3V_PCH

SML1ALERT# 150K 0402 5% RH504

PCHHOT# (IntelR DCI-OOB)	
HIGH	Enable
LOW(DEFAULT)	Disable

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

+3V_PCH RH536 1K_0201_5% +3V_PCH_ME_SW SW4 SSAL120100_3P

HDA_SDOUT 1K 0201 5% RH454 ME_EN

0_0201_5% RH487

<48> ME_FWP

A00_0313: Remove debug part

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default posit i on)

+3VS

PCH to DDR, XDP, FFS

QH4A DMN65D8LDW-7_SOT363-6

MEM_SMBCLK PCH_SMBCLK PCH_SMBCLK <6,14,15,44>

MEM_SMBDATA PCH_SMBDATA PCH_SMBDATA <6,14,15,44>

QH4B DMN65D8LDW-7_SOT363-6

<62> IMVP_VR_PG

<48> RUNPWROK

+3VS UH14 MC74VHC1G08DFT2G_SC70-5 PCH_PWROK RH529 100K_0201_5%

Reserve for EMI

EMC@ CH50 8.2P 0201_50V8B HDA_BITCLK

@ CH51 10P_0201_25V8 HDA_SDOUT

Reserve for RF please close to UH1

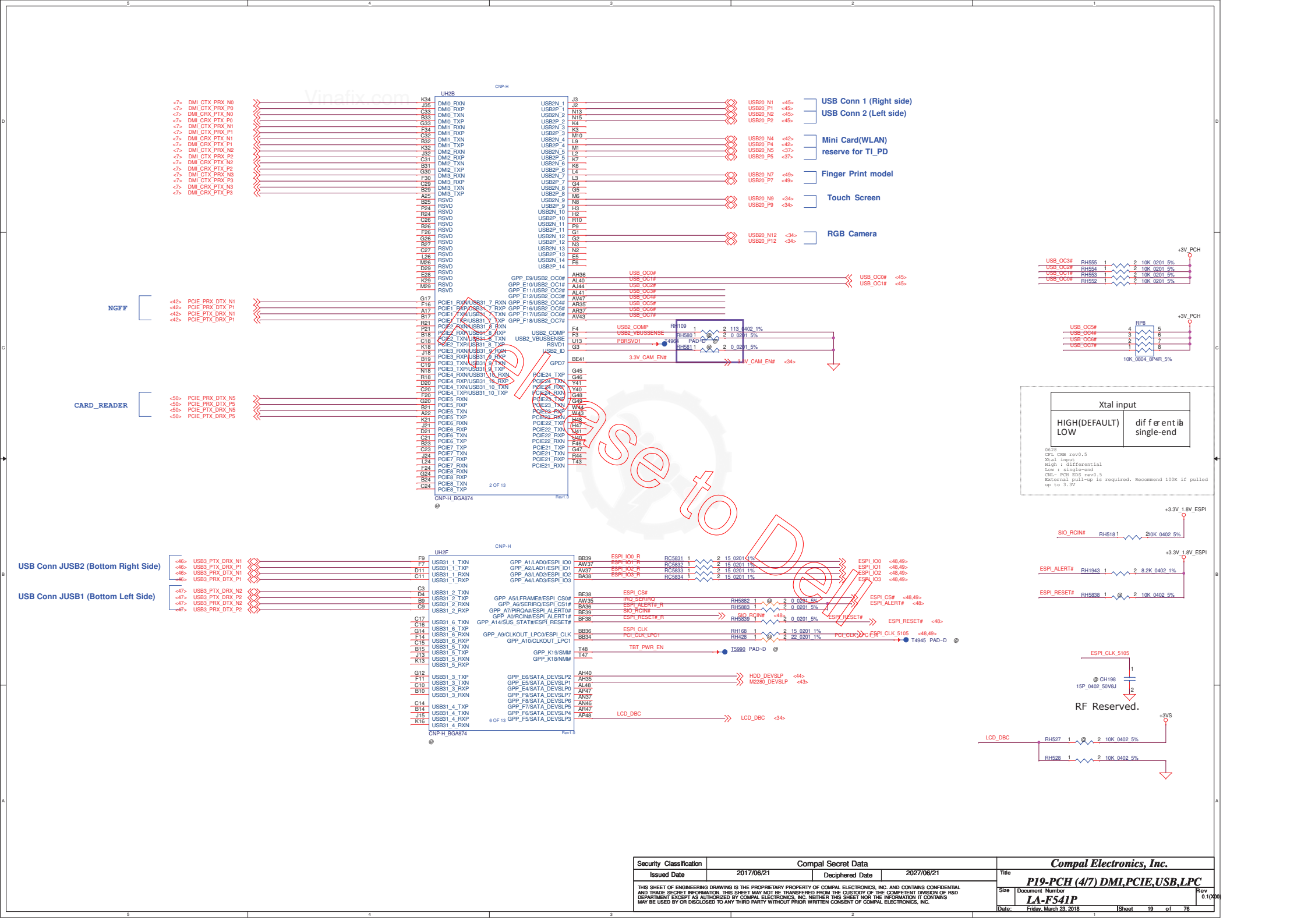
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P18-PCH (3/7) PM,HDA,SMB,JTAG

Size: | Document Number: LA-F541P | Rev: 0.1(000)

Date: Friday, March 23, 2018 | Sheet 18 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

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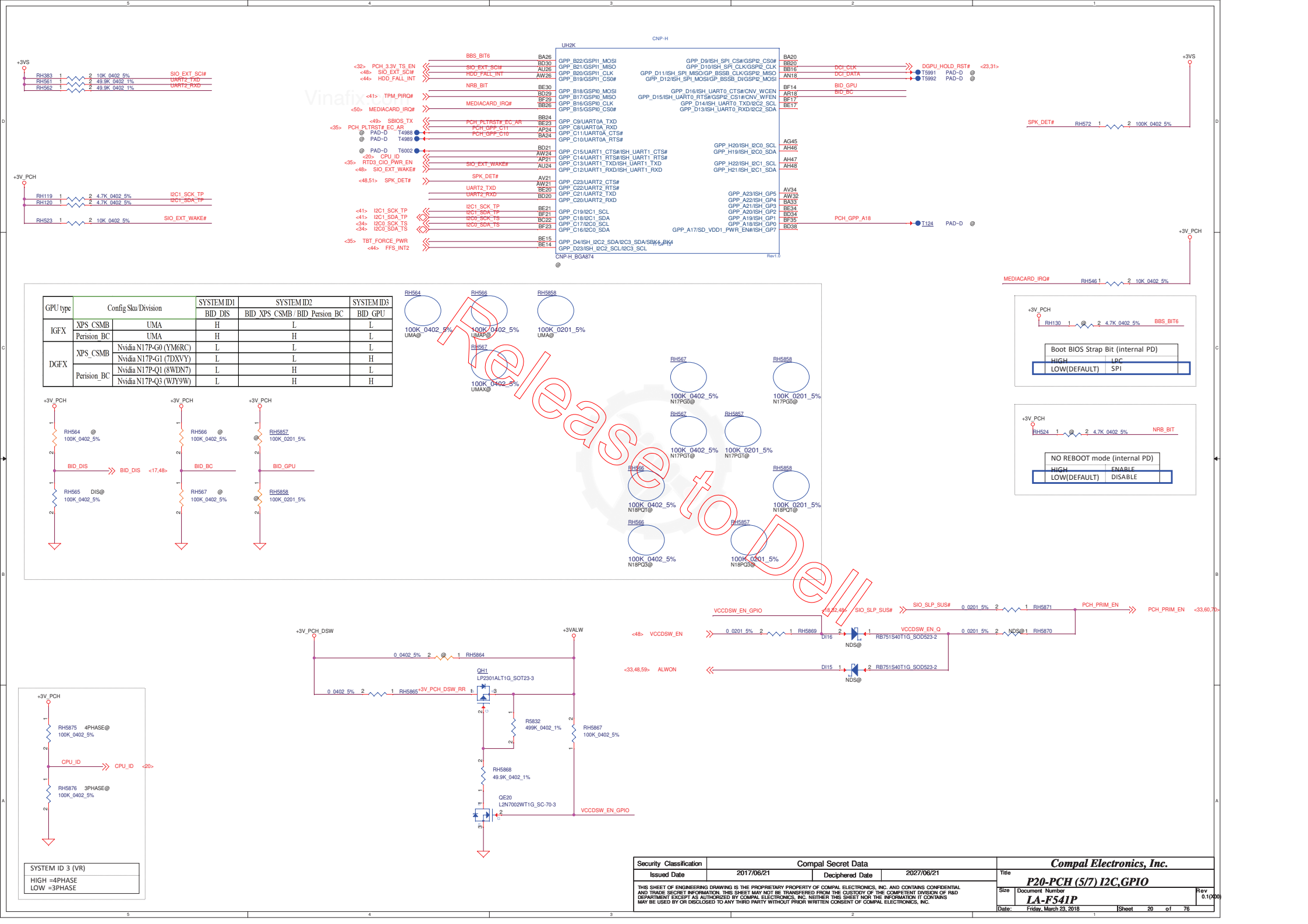
Compal Electronics, Inc.

Title: **P19-PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

Date: Friday, March 23, 2018 | Sheet 19 of 76



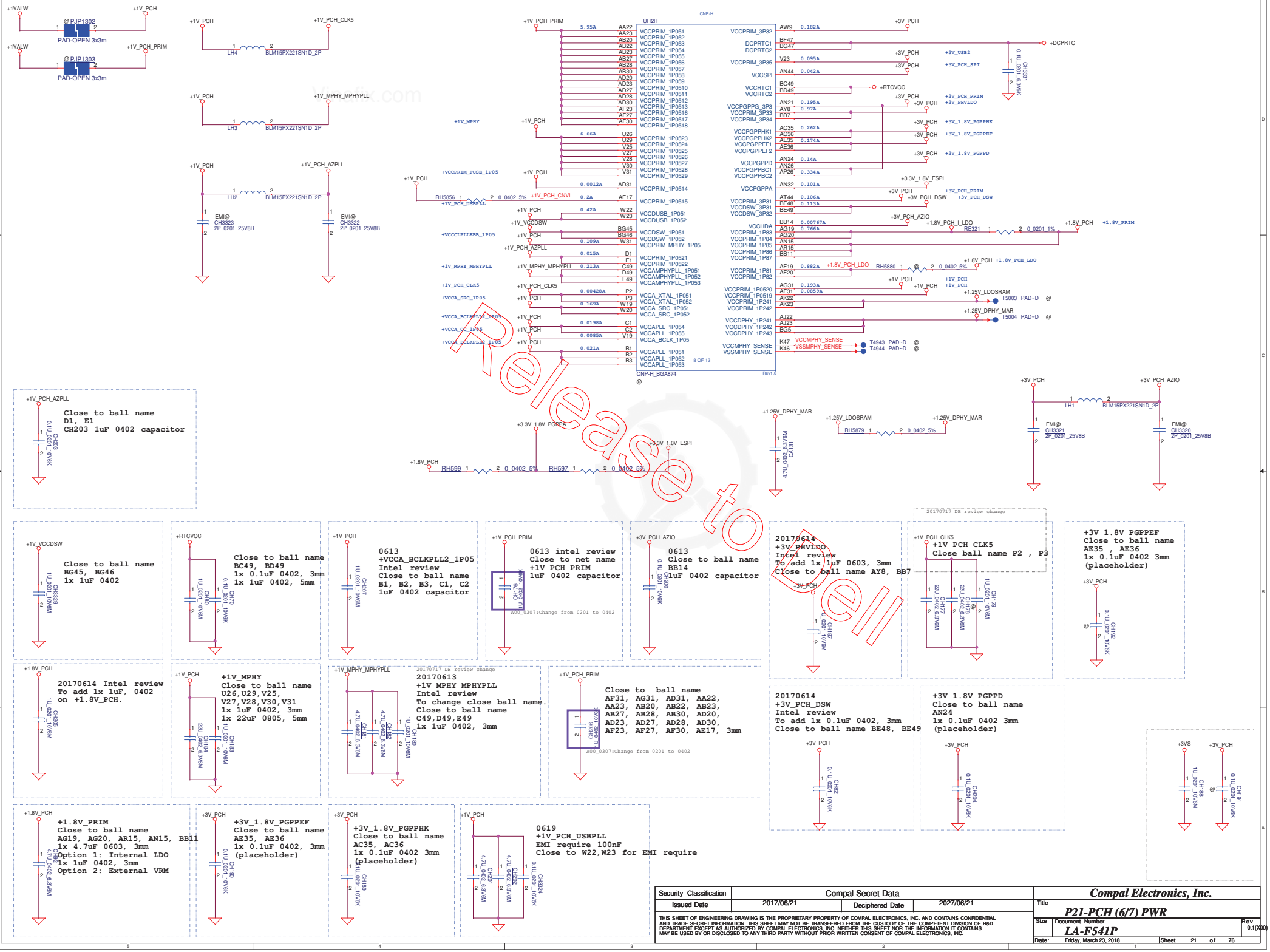
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P20-PCH (5/7) I2C,GPIO**

Size	Document Number	Rev
	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 20 of 76



+1V_PCH_AZPLL

Close to ball name
D1, E1
CH203 1uF 0402 capacitor

+1V_VCCDSW

Close to ball name
BG45, BG46
1x 1uF 0402

+RTCVCC

Close to ball name
BC49, BD49
1x 0.1uF 0402, 3mm
1x 1uF 0402, 5mm

+1V_PCH

0613
+VCCA_BCLKPLL2_1P05
Intel review
Close to ball name
B1, B2, B3, C1, C2
1uF 0402 capacitor

+1V_PCH_PRIM

0613 intel review
Close to net name
+1V_PCH_PRIM
1uF 0402 capacitor

A00_0307:Change from 0201 to 0402

+3V_PCH_AZIO

0613
Close to ball name
BB14
1uF 0402 capacitor

20170614
+3V_PHVLDO
Intel review
To add 1x 1uF 0603, 3mm
Close to ball name AY8, BB7

20170717 DB review change

+1V_PCH_CLK5

+1V_PCH_CLK5
Close ball name P2 , P3

+3V_1.8V_PGPPEF

Close to ball name
AE35 , AE36
1x 0.1uF 0402 3mm
(placeholder)

+1.8V_PCH

20170614 Intel review
To add 1x 1uF, 0402
on +1.8V_PCH.

+1V_PCH

+1V_MPHY
Close to ball name
U26,U29,V25,
V27,V28,V30,V31
1x 1uF 0402, 3mm
1x 22uF 0805, 5mm

+1V_MPHY_MPHYPLL

20170717 DB review change

20170613
+1V_MPHY_MPHYPLL
Intel review
To change close ball name.
Close to ball name
C49,D49,E49
1x 1uF 0402, 3mm

+1V_PCH_PRIM

Close to ball name
AF31, AG31, AD31, AA22,
AA23, AB20, AB22, AB23,
AB27, AB28, AB30, AD20,
AD23, AD27, AD28, AD30,
AF23, AF27, AF30, AE17, 3mm

A00_0307:Change from 0201 to 0402

20170614
+3V_PCH_DSW
Intel review
To add 1x 0.1uF 0402, 3mm
Close to ball name BE48, BE49

+3V_1.8V_PGPPD

Close to ball name
AN24
1x 0.1uF 0402 3mm
(placeholder)

+3VS

+1.8V_PRIM

Close to ball name
AG19, AG20, AR15, AN15, BB11
1x 4.7uF 0603, 3mm
Option 1: Internal LDO
1x 1uF 0402, 3mm
Option 2: External VRM

+3V_1.8V_PGPPEF

Close to ball name
AE35, AE36
1x 0.1uF 0402, 3mm
(placeholder)

+3V_1.8V_PGPPHK

Close to ball name
AC35, AC36
1x 0.1uF 0402 3mm
(placeholder)

+1V_PCH

0619
+1V_PCH_USBPLL
EMI require 100nF
Close to W22,W23 for EMI require

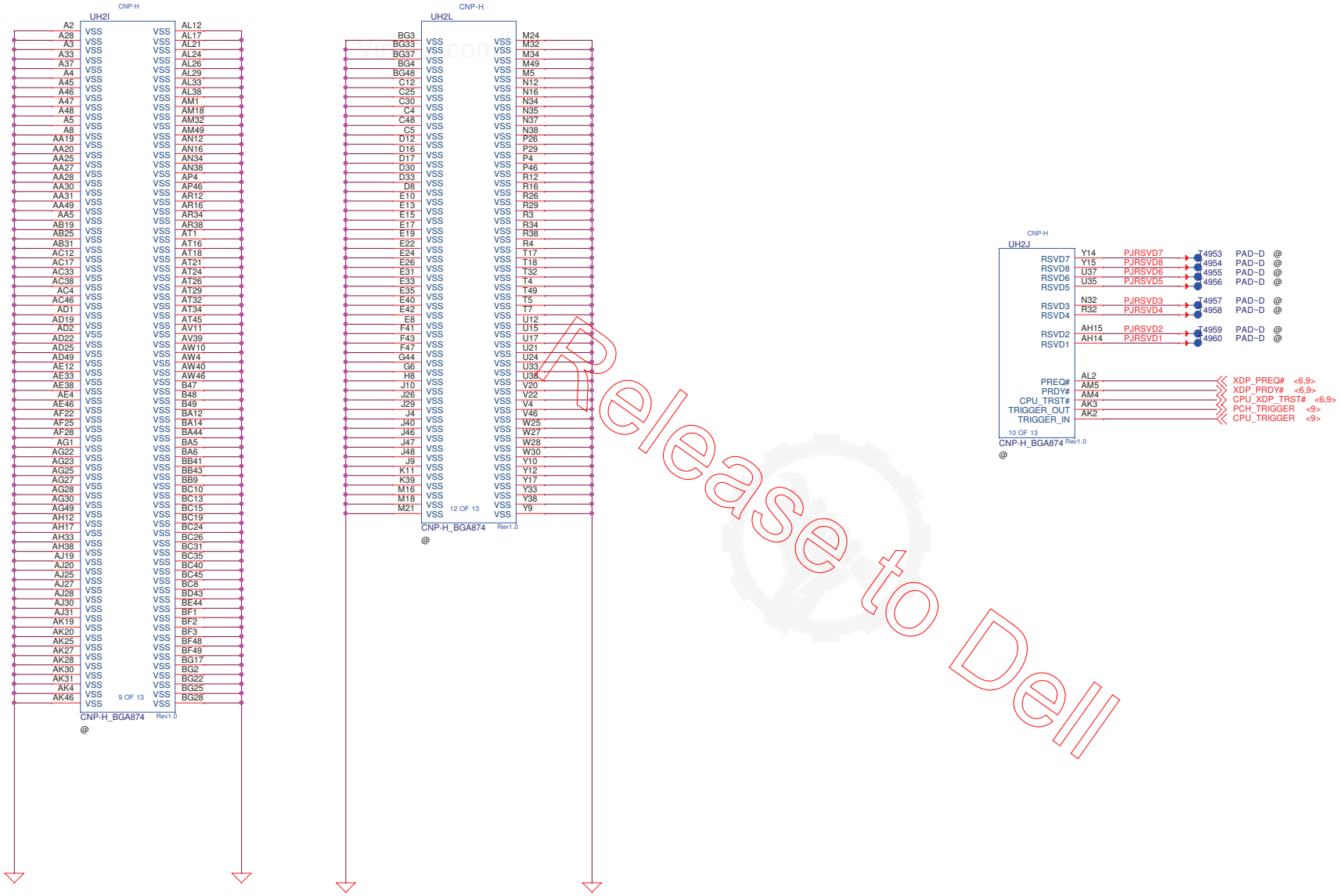
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P21-PCH (6/7) PWR**

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

Date: Friday, March 23, 2018 | Sheet 21 of 76



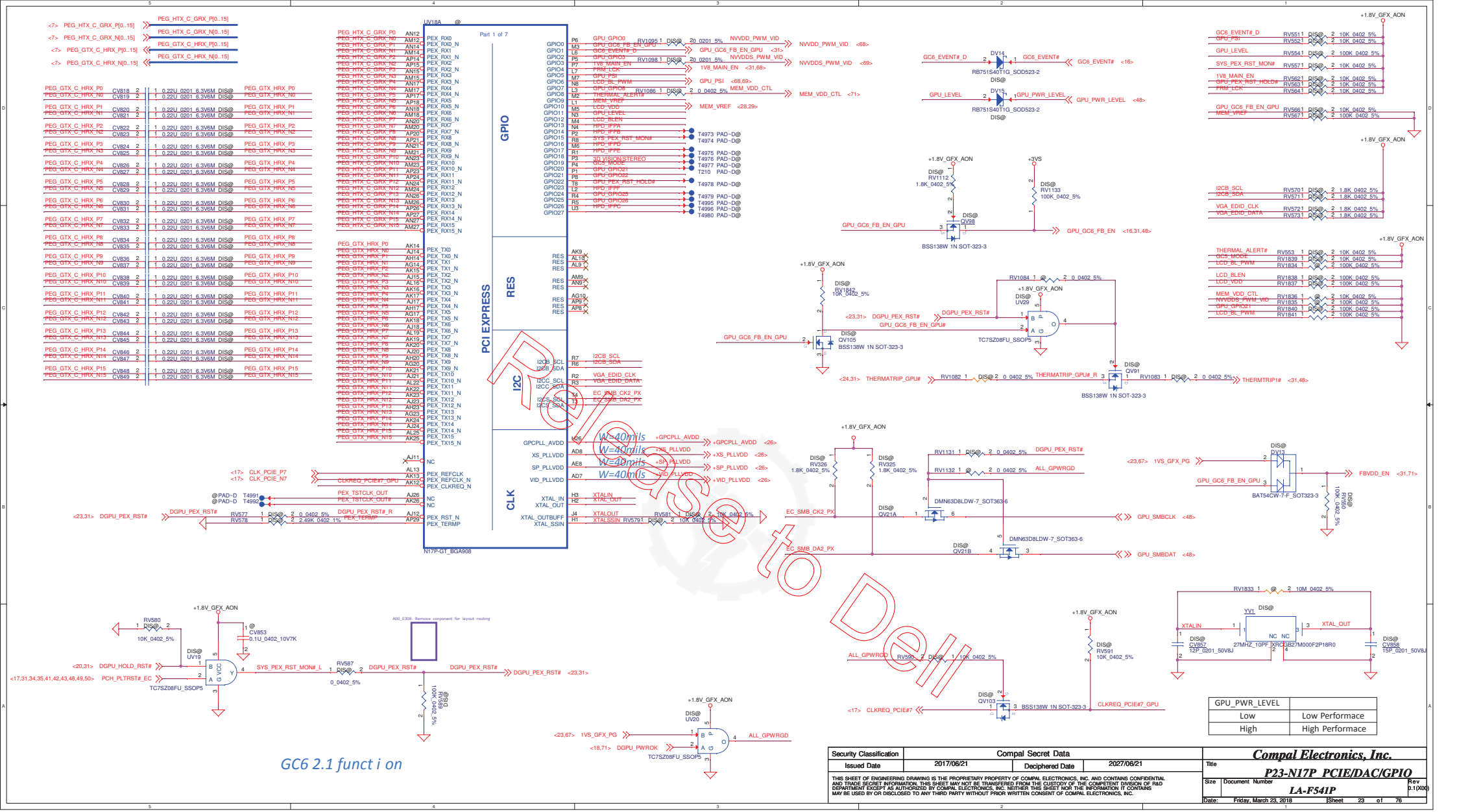
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P22-PCH (7/7) VSS**

Size: | Document Number: **LA-F541P** | Rev: 0.1(X00)

Date: Friday, March 23, 2018 | Sheet 22 of 76


PEG_HTX_C_GRX_P[0..15]
PEG_HTX_C_GRX_N[0..15]
PEG_GTX_C_HRX_P[0..15]
PEG_GTX_C_HRX_N[0..15]
UV18A
Part 1 of 7
PCI EXPRESS
GPIO
RES
I2C
CLK
N17P-GT_BGA908
GPU_GPIO0
GPU_GC6_FB_EN_GPU
GC6_EVENT#_D
GPU_PSI
LCD_BLEN
LCD_VDD
LCD_BL_PWM
HPD_IFPA
HPD_IFPB
SYS_PEX_RST_MON#
HPD_IFPC
3D_VISION/STEREO
GC6_MODE
GPU_GPIO21
GPU_PEX_RST_HOLD#
GPU_GPIO25
GPU_GPIO26
HPD_IFPG
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA
XTALIN
XTAL_OUT
XTALSSIN
NVVDD_PWM_VID
NVVDDS_PWM_VID
1V8_MAIN_EN
GPU_PSI
LCD_BL_PWM
FRM_LCK
MEM_VDD_CTL
MEM_VREF
LCD_VDD
LCD_BLEN
GPU_LEVEL
GPU_GC6_FB_EN_GPU
GPU_PWR_LEVEL
GC6_EVENT#
THERMAL_ALERT#
GC5_MODE
THERMTRIP1#
THERMATRIP_GPU#
VGA_EDID_CLK
VGA_EDID_DATA
EC_SMB_CK2_PX
EC_SMB_DA2_PX
GPU_SMBCLK
GPU_SMBDAT
DGPU_PEX_RST#
DGPU_HOLD_RST#
PCH_PLTRST#_EC
SYS_PEX_RST_MON#_L
CLK_PCIE_P7
CLK_PCIE_N7
CLKREQ_PCIE#7_GPU
1VS_GFX_PG
FBVDD_EN
DGPU_PWROK
ALL_GPWRGD
+1.8V_GFX_AON
+3VS
+GPCPLL_AVDD
+XS_PLLVDD
+SP_PLLVDD
+VID_PLLVDD
W=40mils
RB751S40T1G_SOD523-2
BSS138W 1N SOT-323-3
TC7SZ08FU_SSOP5
BAT54CW-7-F_SOT323-3
DMN63D8LDW-7_SOT363-6
27MHZ_10PF_XRCGB27M000F2P18R0
Title
P23-N17P PCIE/DAC/GPIO
Size
Document Number
LA-F541P
Rev
0.1(XXX)
Date: Friday, March 23, 2018
Sheet 23 of 76
Security Classification
Compal Secret Data
Issued Date
2017/06/21
Deciphered Date
2027/06/21
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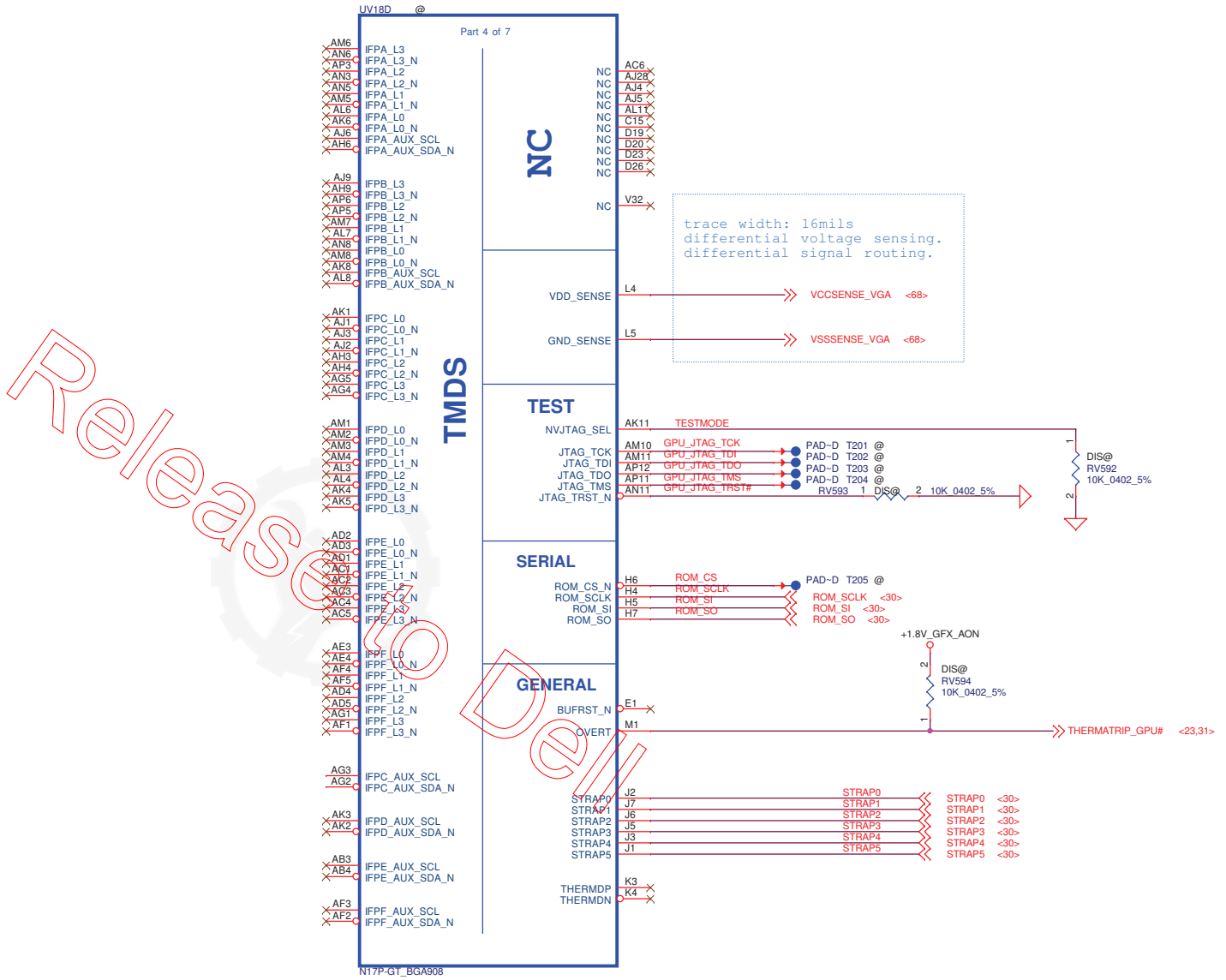
GPU_PWR_LEVEL
Low
Low Performace
High
High Performace
GC6 2.1 funct i on
Refer to Del



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Compal Electronics, Inc.

Title: **P24-N17P_eDP/HDMI/mDP**

Size	Document Number	Rev
	LA-F541P	0.1(X00)

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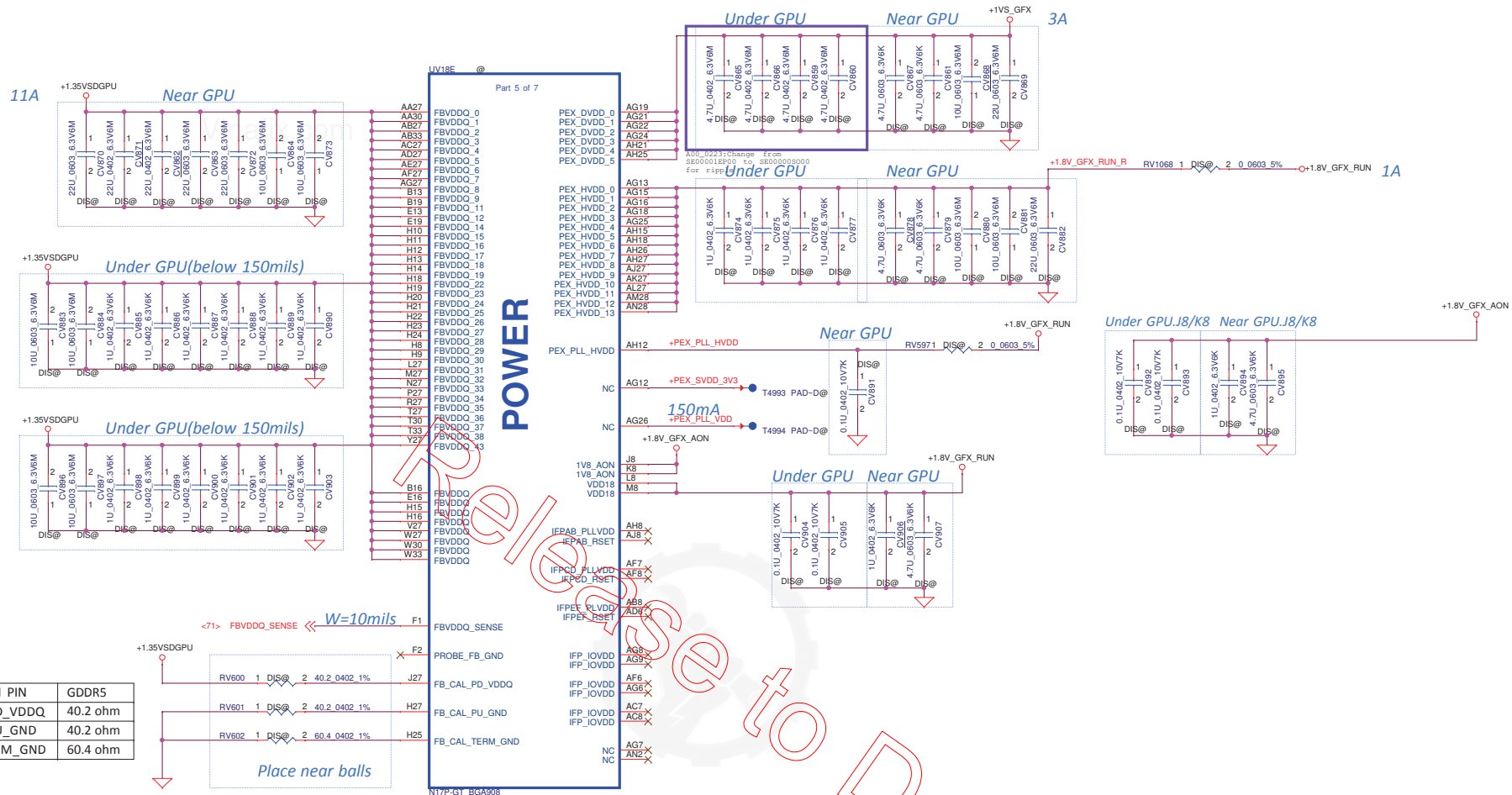
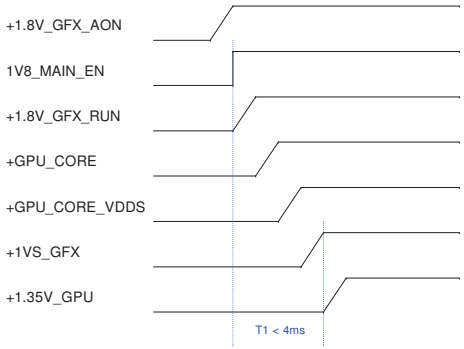


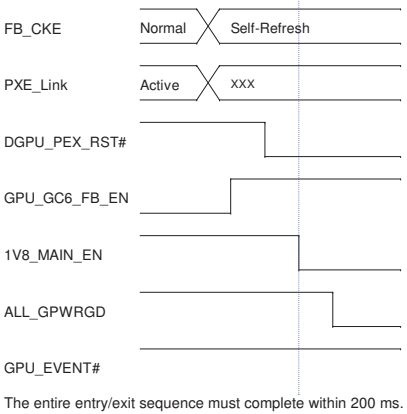
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

GPU Power Up Sequence



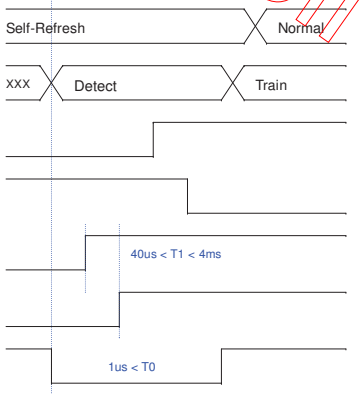
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

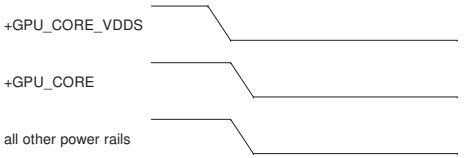


The entire entry/exit sequence must complete within 200 ms.

GPU GC6 Exit Sequence



GPU Power Down Sequence



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Compal Electronics, Inc.	
Title	P25-N17P_Power
Size	Document Number: LA-F541P
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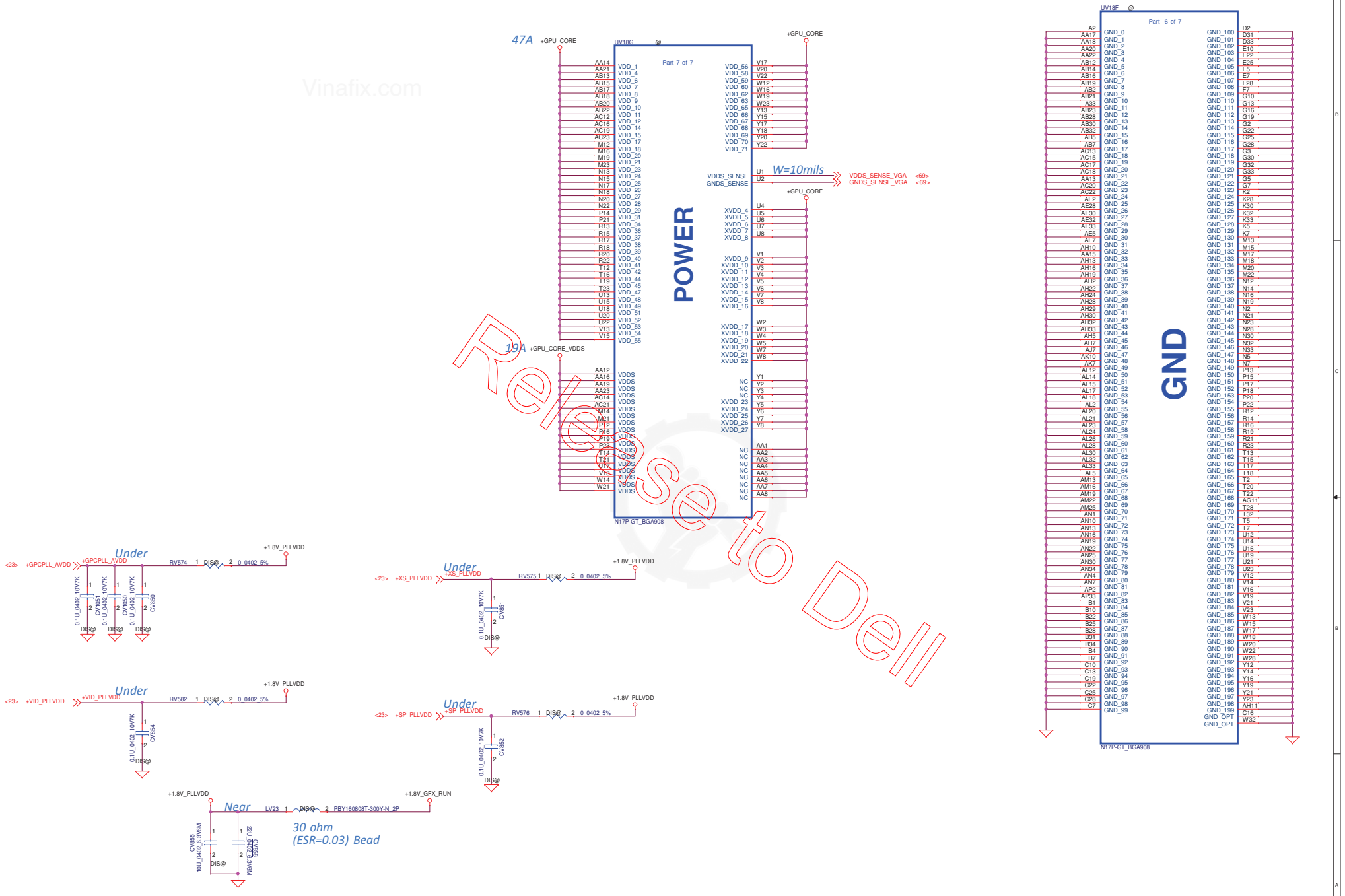

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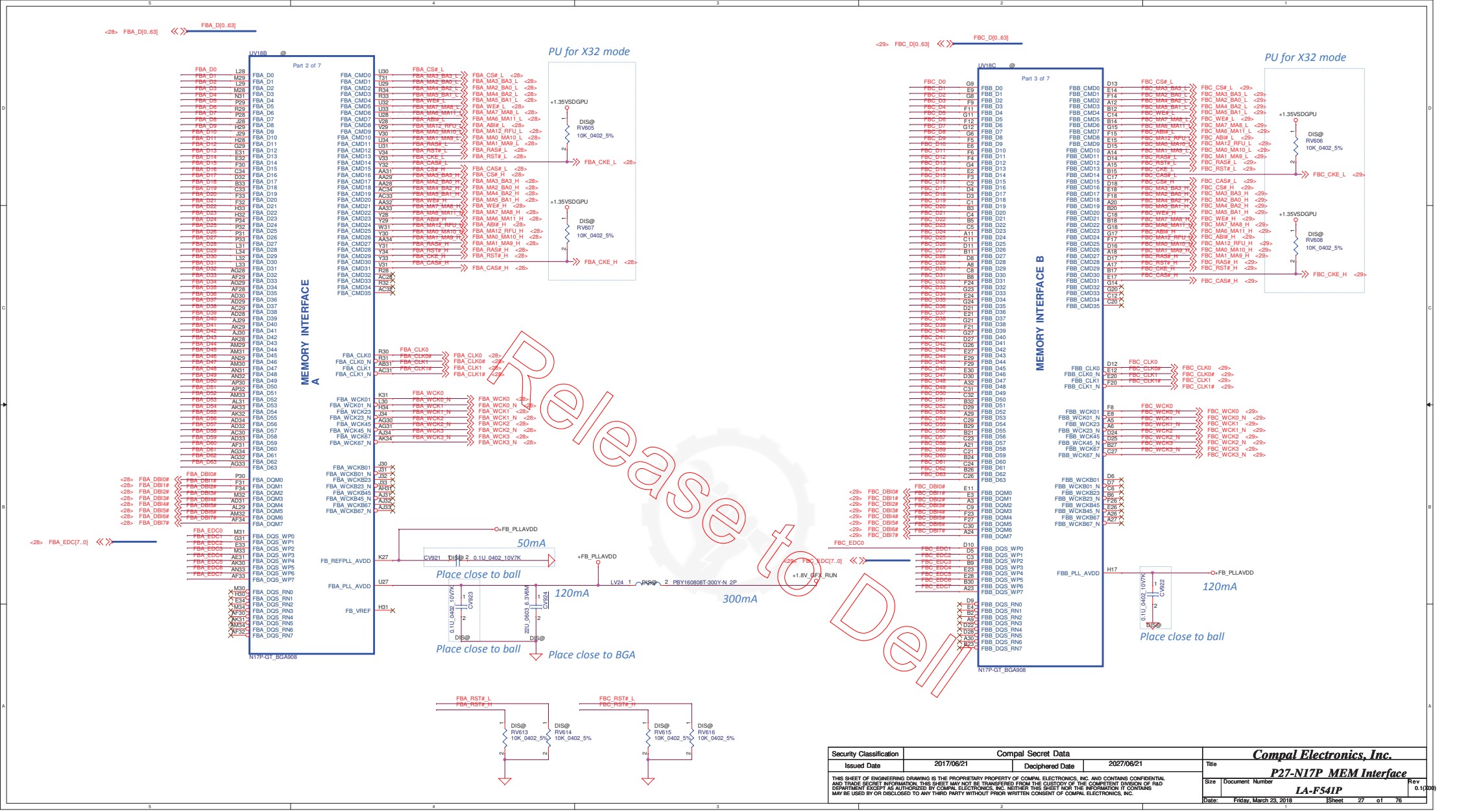
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title	P26-N17P_VGA CORE/GND		
Size	Document Number	LA-F541P	Rev 0.1(000)
Date: Friday, March 23, 2018	Sheet 26 of 76		



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Compal Electronics, Inc.

Title: **P27-N17P MEM Interface**

Size: | Document Number: **LA-F541P** | Rev: 0.1(X00)

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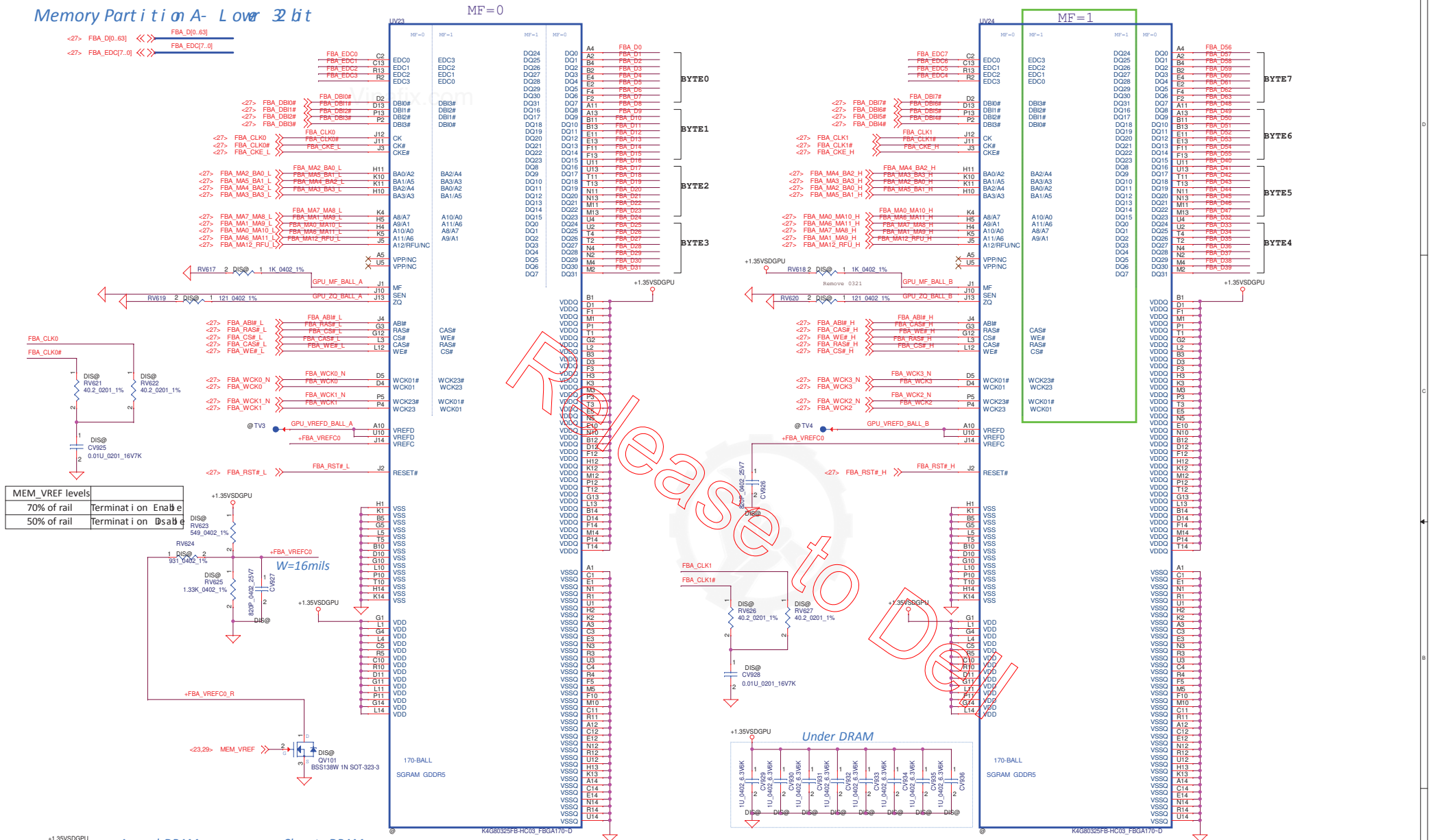
Memory Partition A- Lower 32bit

MF=0

MF=1



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Compal Electronics, Inc.

Title: **P28-N17P_GDDR5_A**

Size	Document Number	Rev
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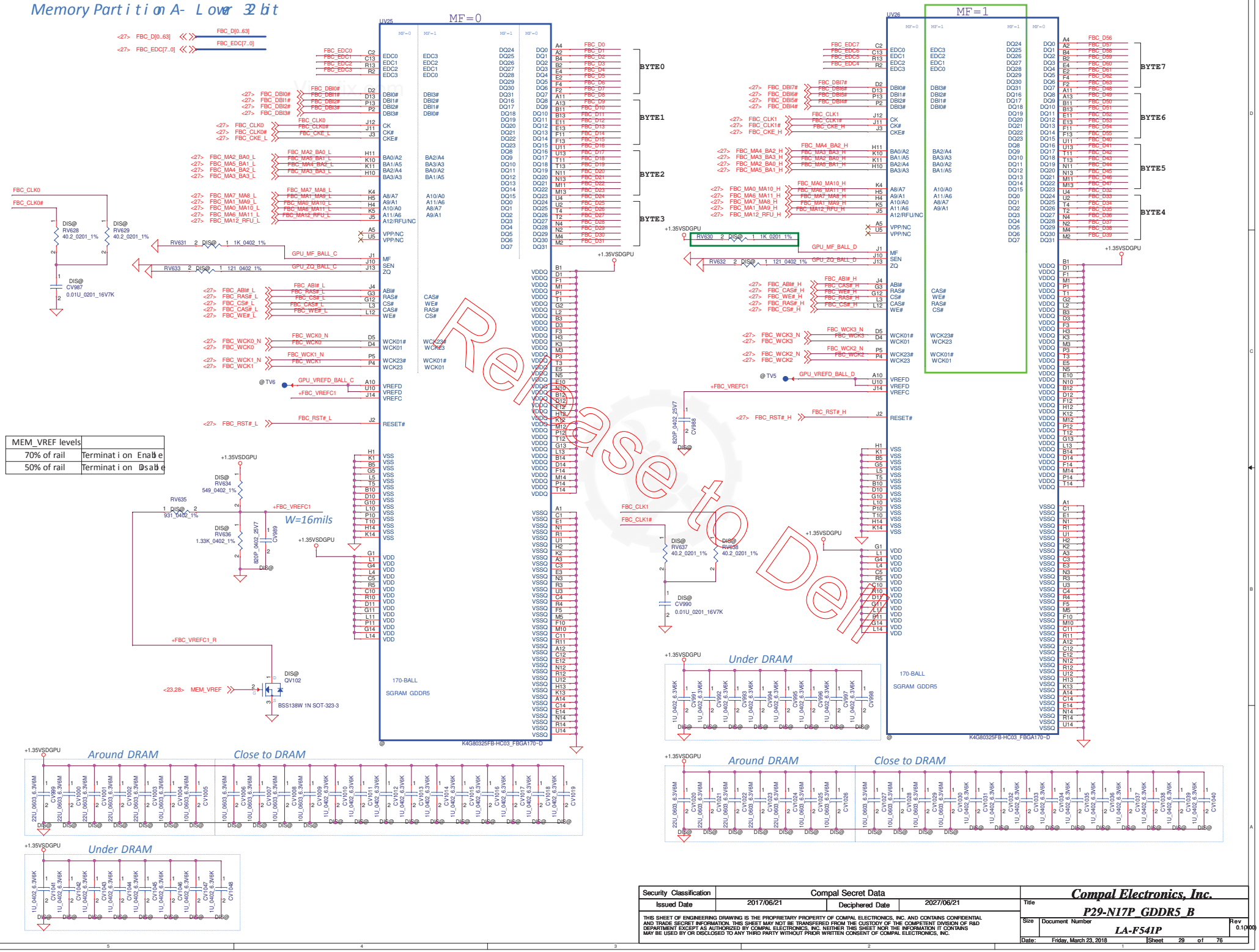
Memory Partition A- Lower 32bit



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Compal Electronics, Inc.

Title: P29-N17P_GDDR5_B

Size: | Document Number: LA-F541P | Rev: 0.1(000)

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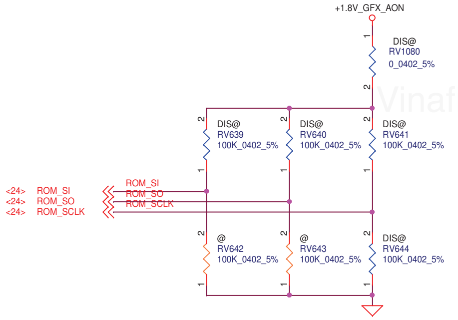
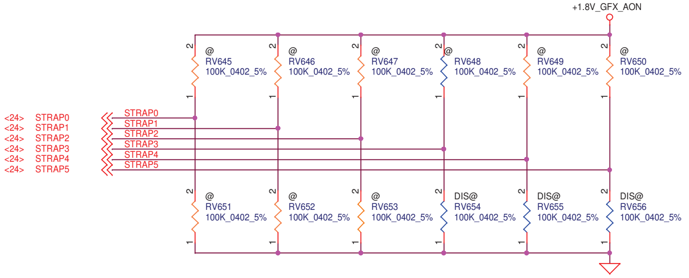




SMB_ALT_ADDR	State
Low	Single GPU
High	Dual GPU

DEVID_SEL	State
Low	Original Device ID
High	Re-brand Device ID

PCIE_CFG	State
Low	Normal signal swing
High	Reduce the signal amplitude

VGA_DEVICE	State
Low	3D Device
High	VGA Device

Table 5.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 3. N17P-G0/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V²	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver³
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver³
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver³

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

Berlinetta MLK			
Straps	(N17P-Q1)	(N17P-G0)	
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL.	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0) , DEVIE_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0) , VGA_DEVICE(0)
STRAP5	Unused	"L"	

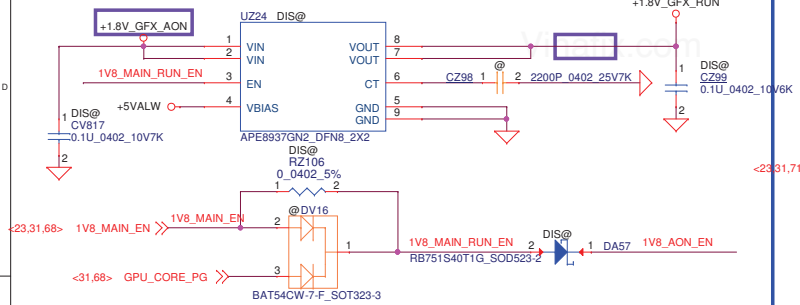
Table 4. N17P-Q1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

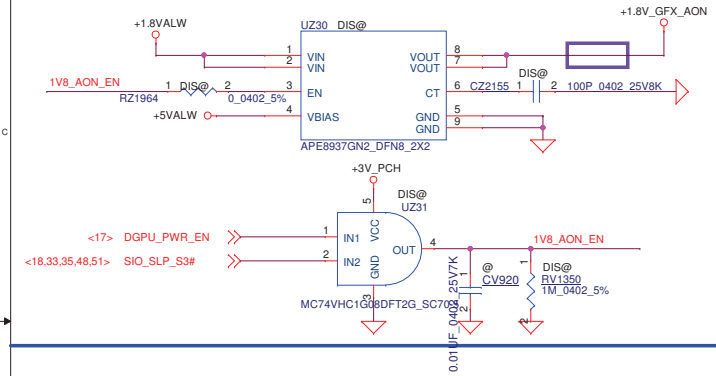
Notes:

1. For N17P-Q1, the maximum allowable memory case temperature is 85 °C.

+1.8V_3.3V_GFX_RUN

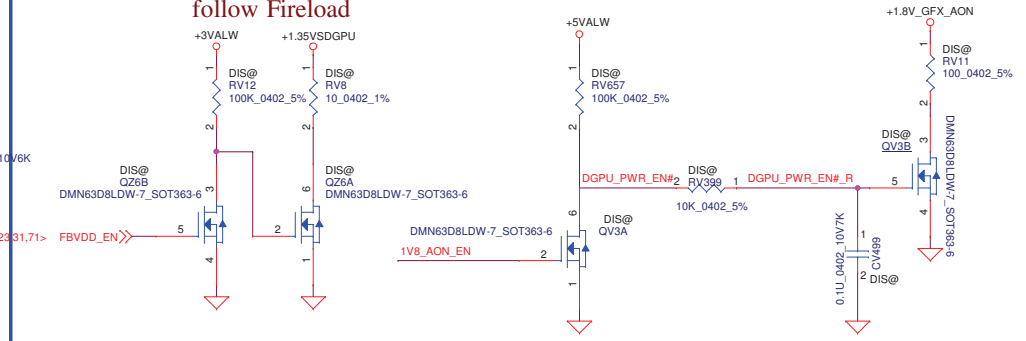


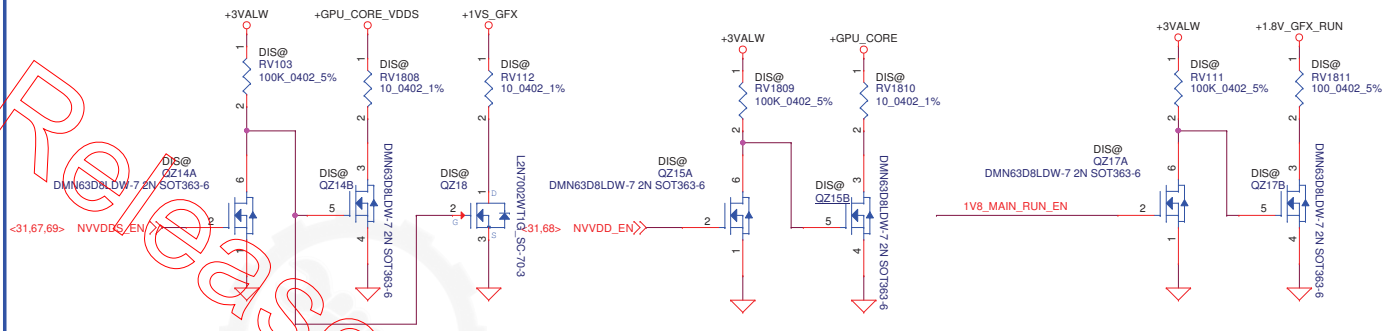
+1.8VALW to +1.8V_3.3V_GFX_AON



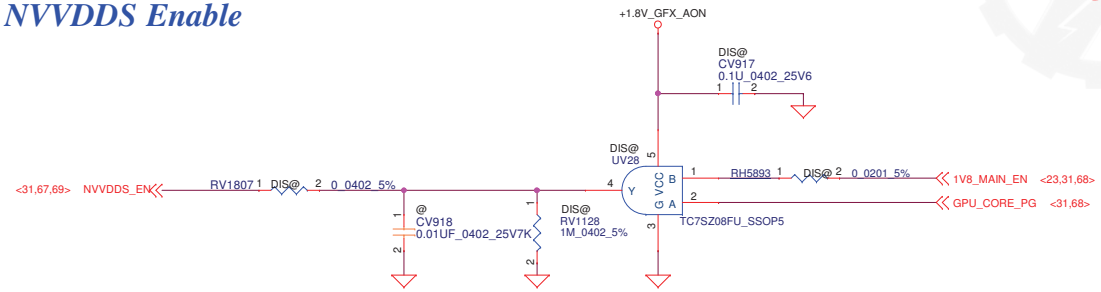
Discharge

follow Fireload

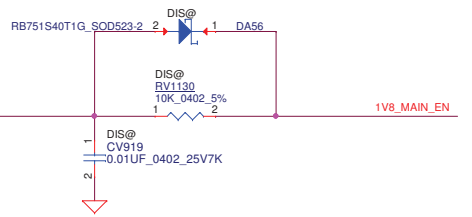


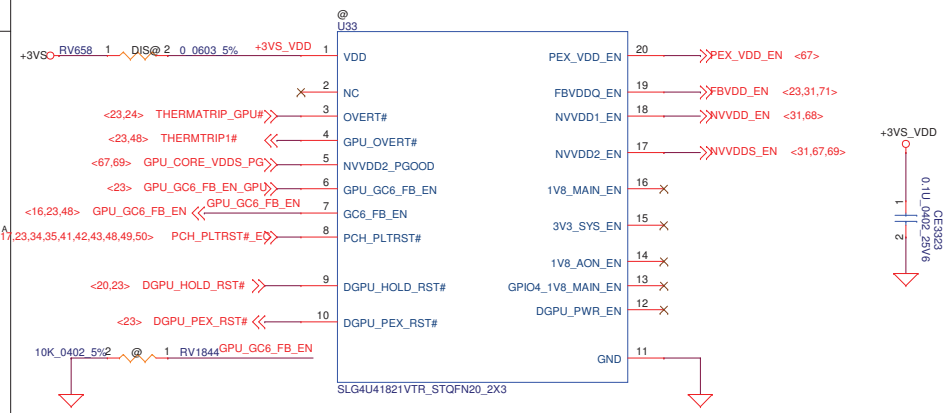


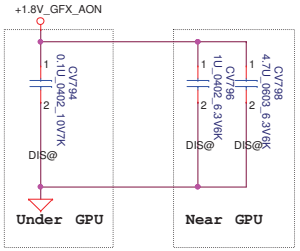
NVVDDS Enable



NVVDD Enable







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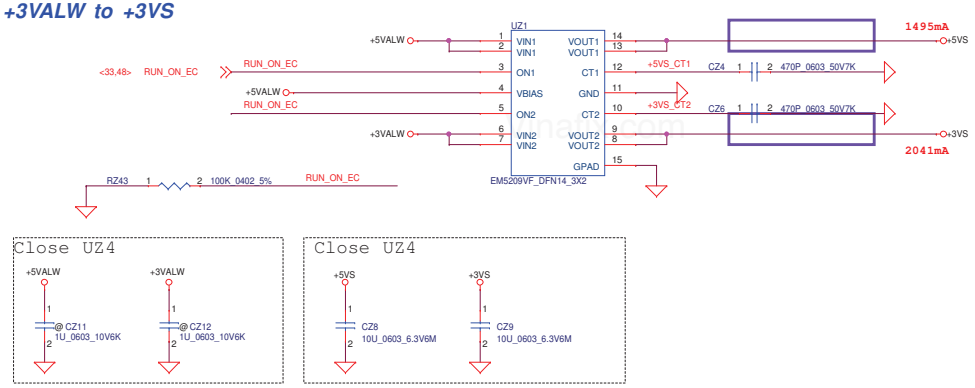
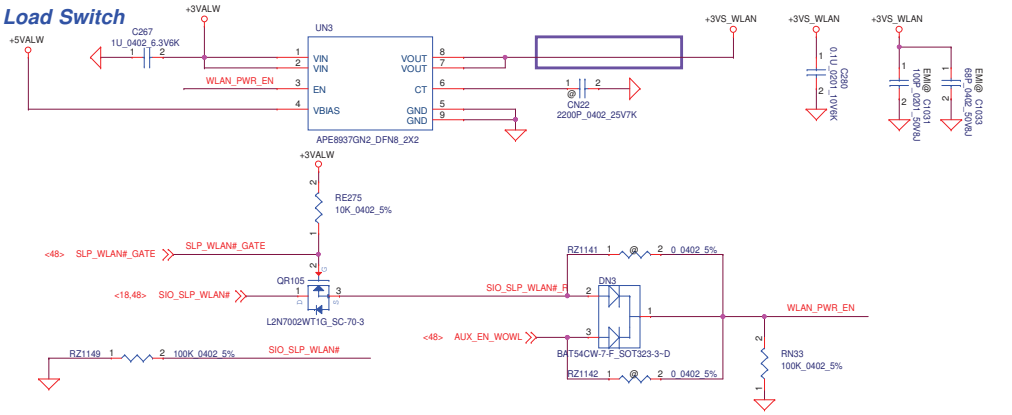
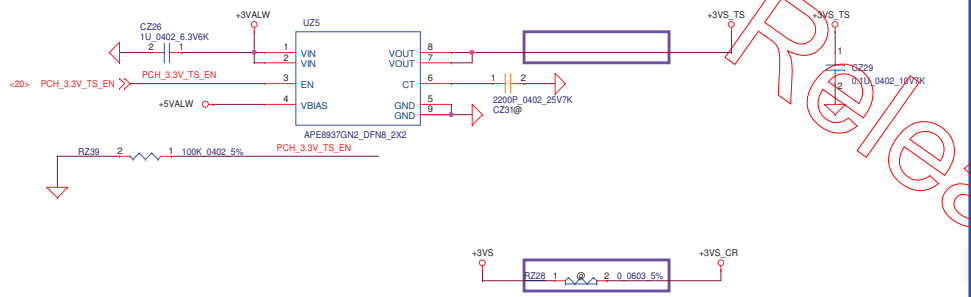
+5VALW to +5VS
+3VALW to +3VS



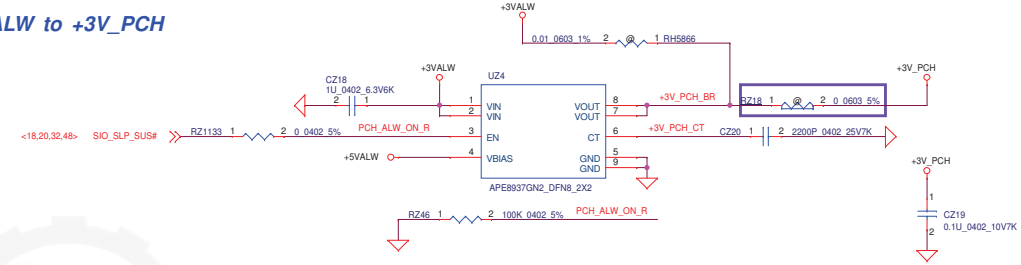
WLAN Load Switch



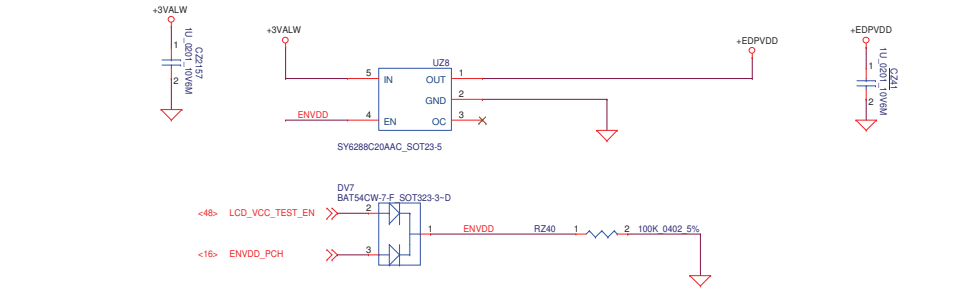
Touch Screen Load Switch & Card Reader



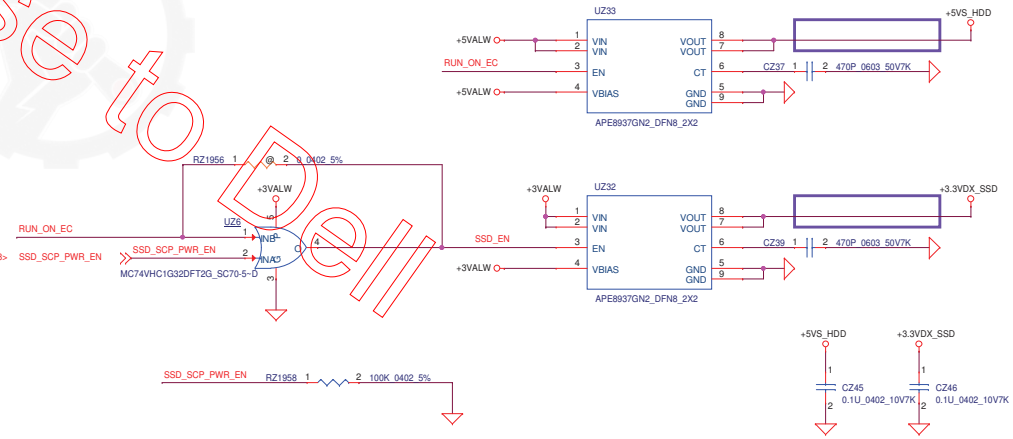
+3VALW to +3V_PCH



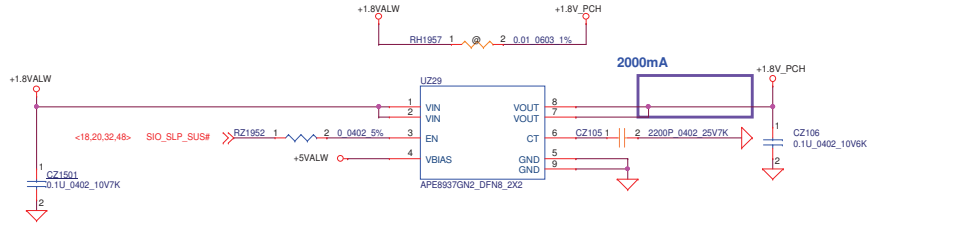
eDP & Camera Load Switch



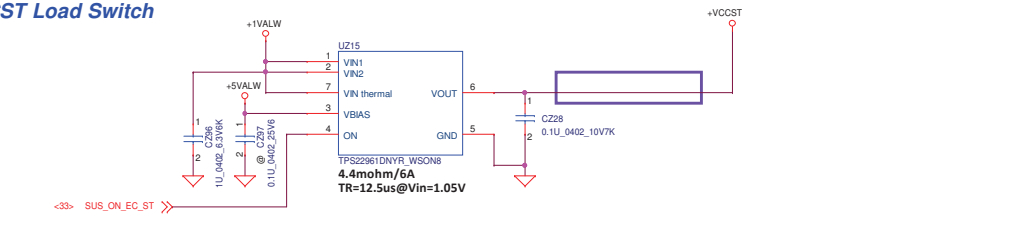
HDD, SSD Load Switch



+1.8VALW to +1.8V_PCH



+VCCST Load Switch



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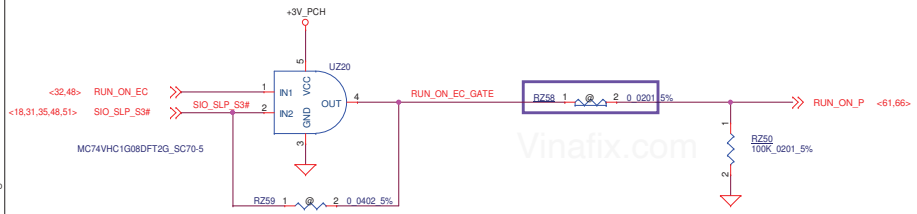
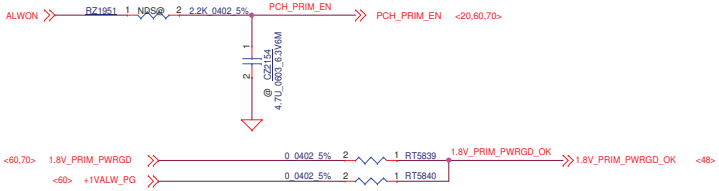
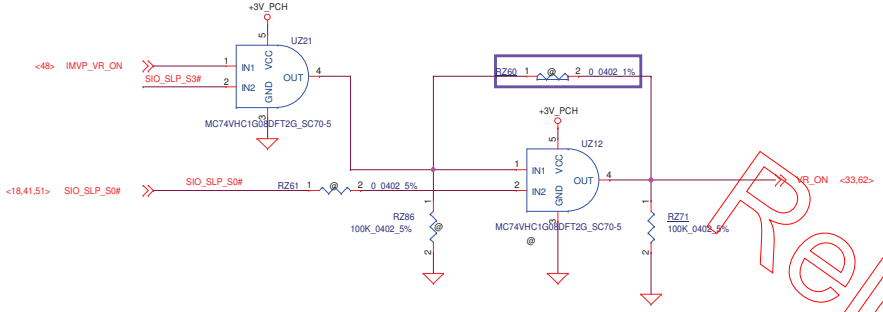
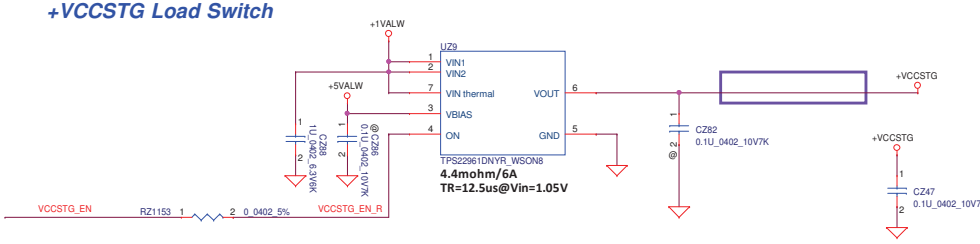
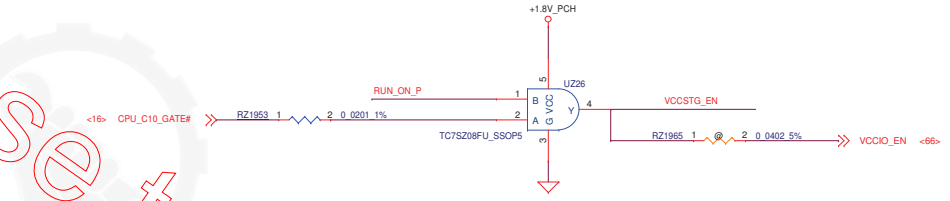


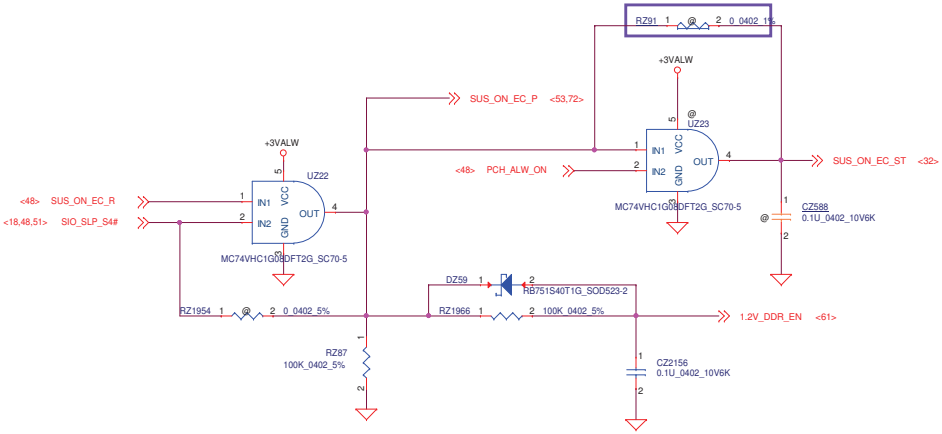




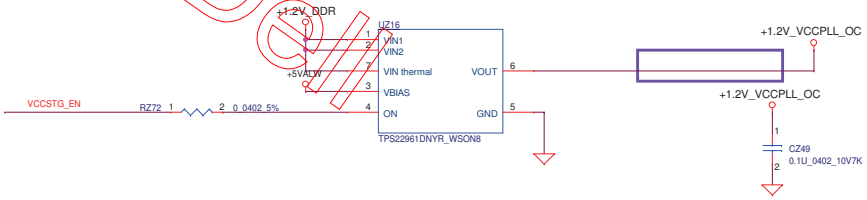
+VCCSTG Load Switch

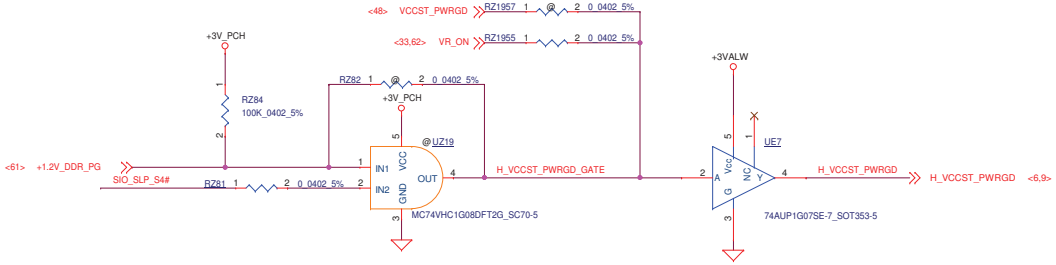






+VCCPLL_OC Load Switch





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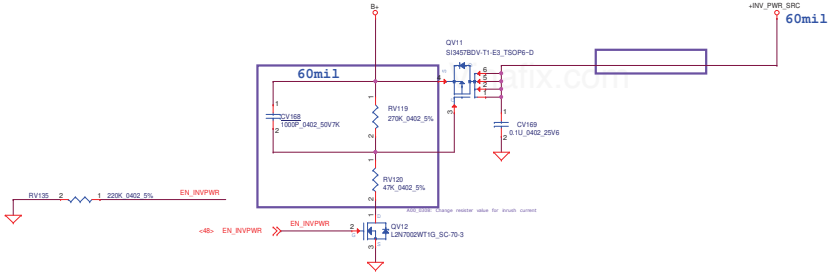
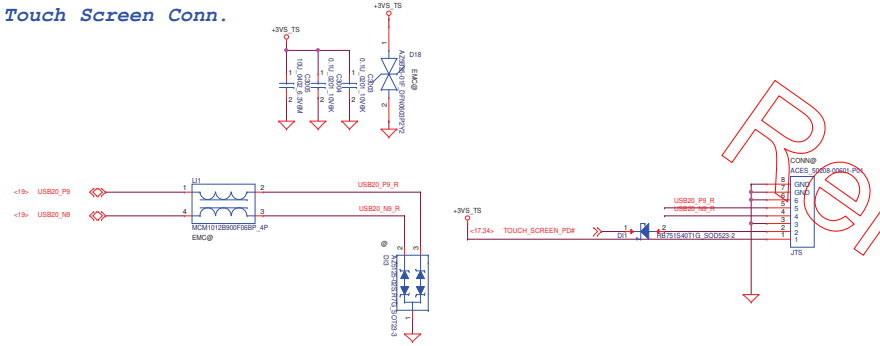
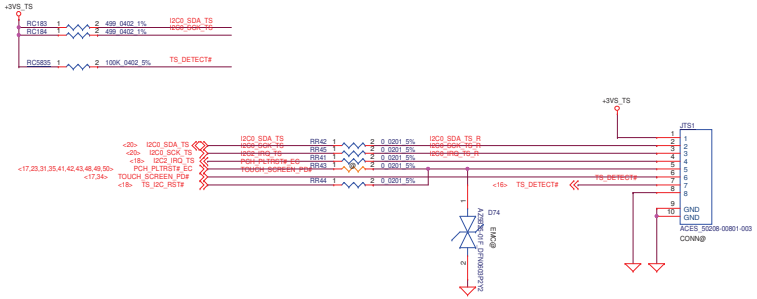
LCD backlight PWR CTRL

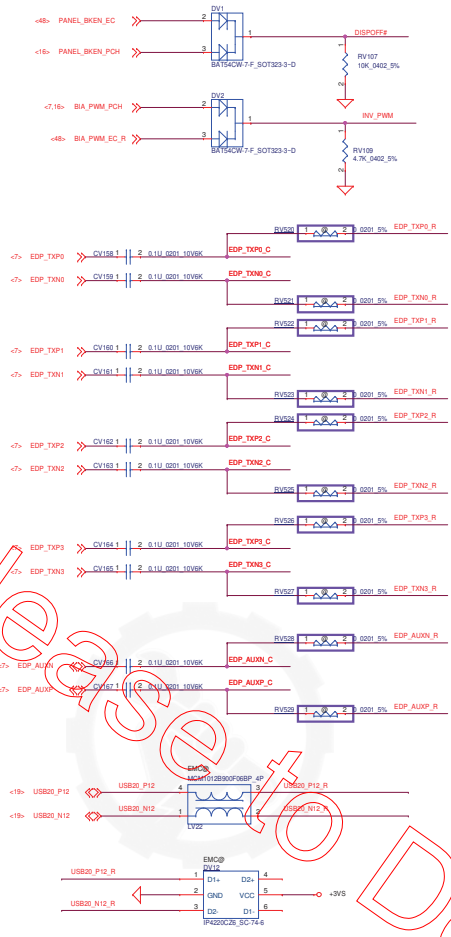


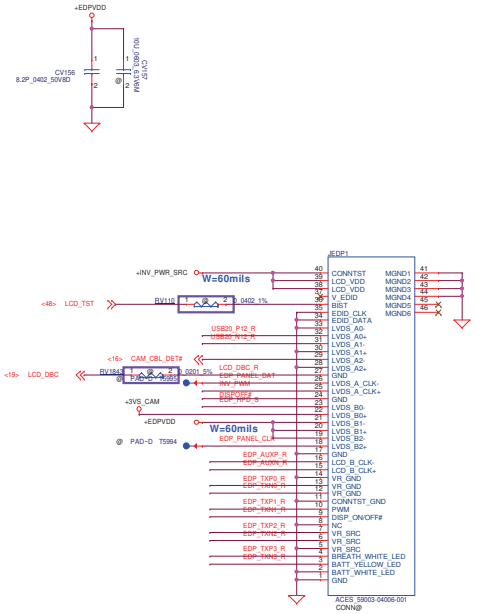
Touch Screen Conn.

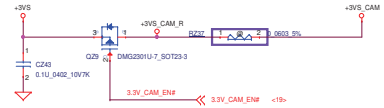


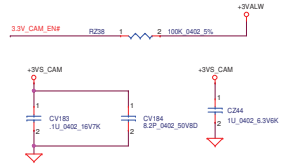


eDP & CCD(RGB) Conn.









Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/06/21	Deciphered Date 2027/06/21	Title: P34-eDP/CCD/TS
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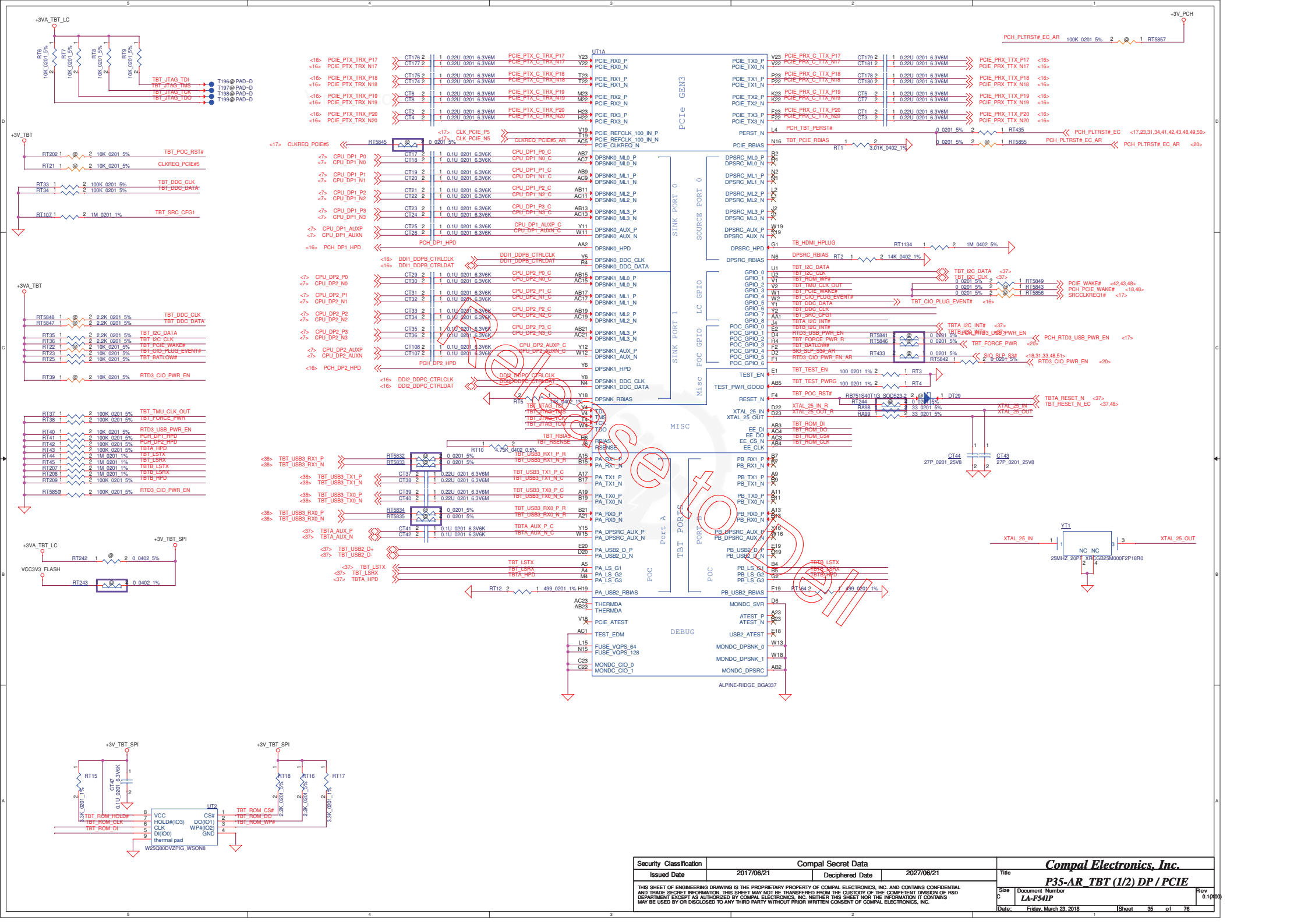
			Date: Friday, March 23, 2018; Sheet 34 of 76



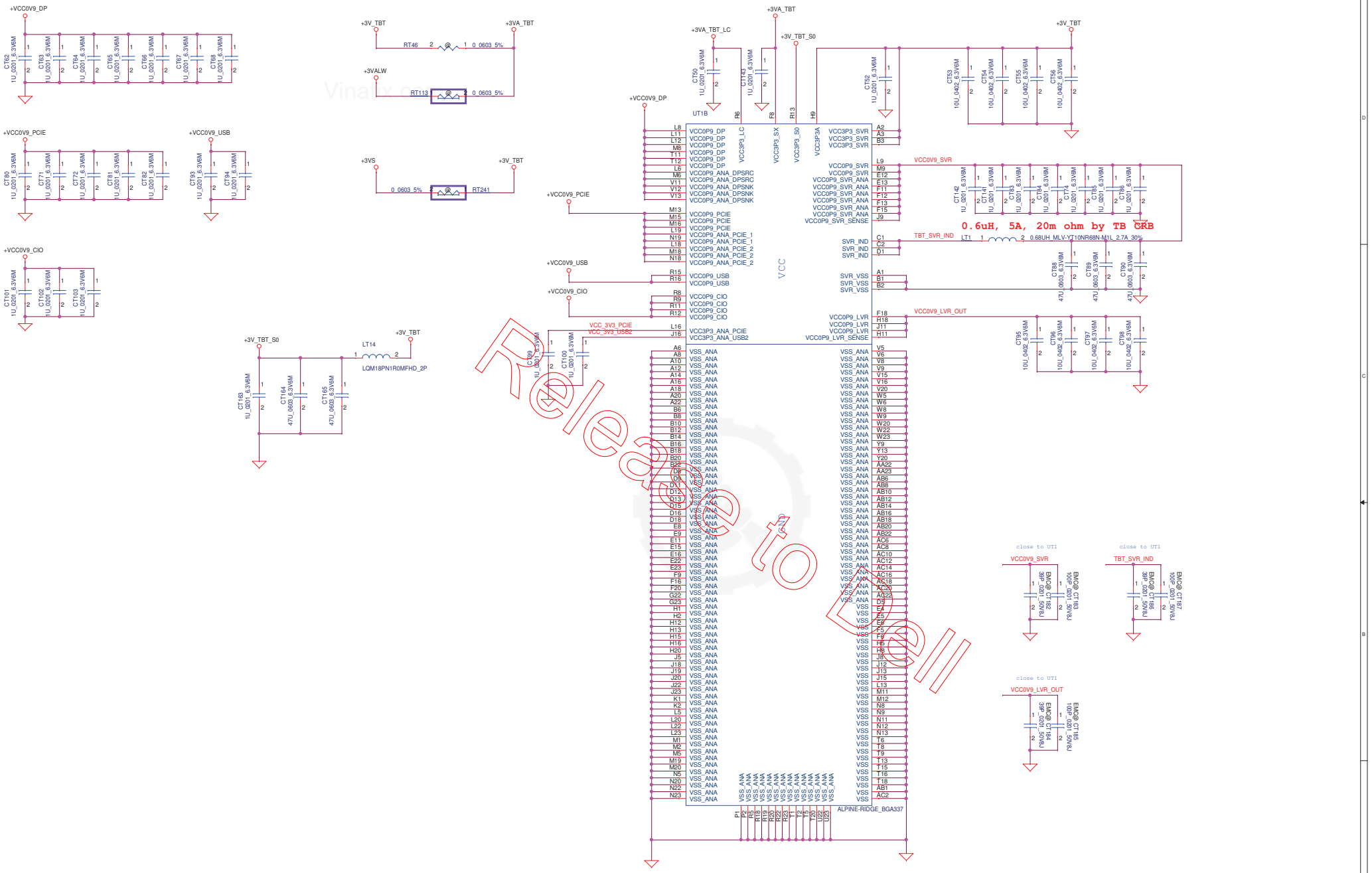
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P35-AR_TBT (1/2) DP / PCIE**

Size	Document Number	Rev
C	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 35 of 76



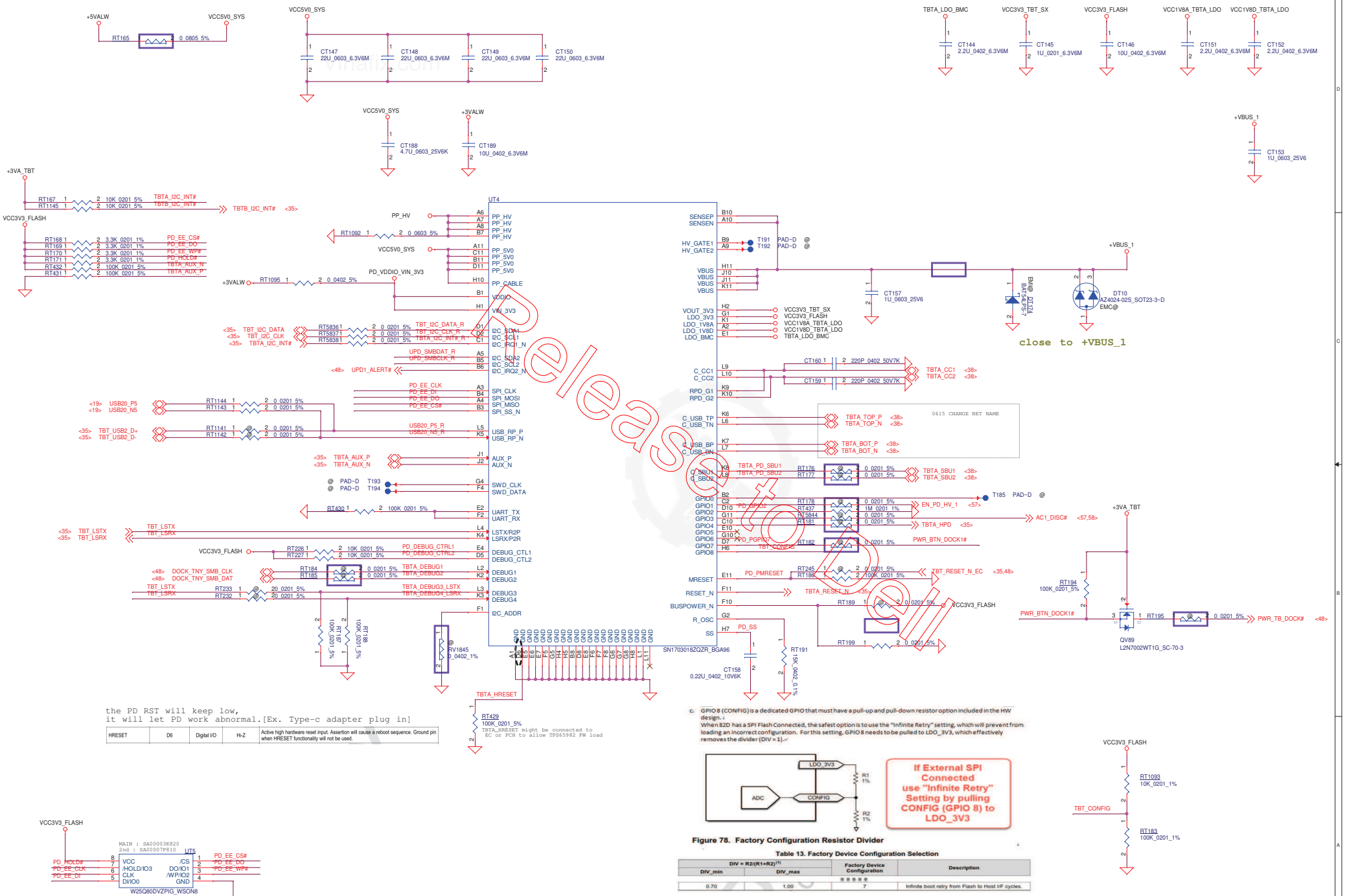
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P36-AR_TBT (2/2) PWR / VSS**

Size	Document Number	Rev
C	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 36 of 76



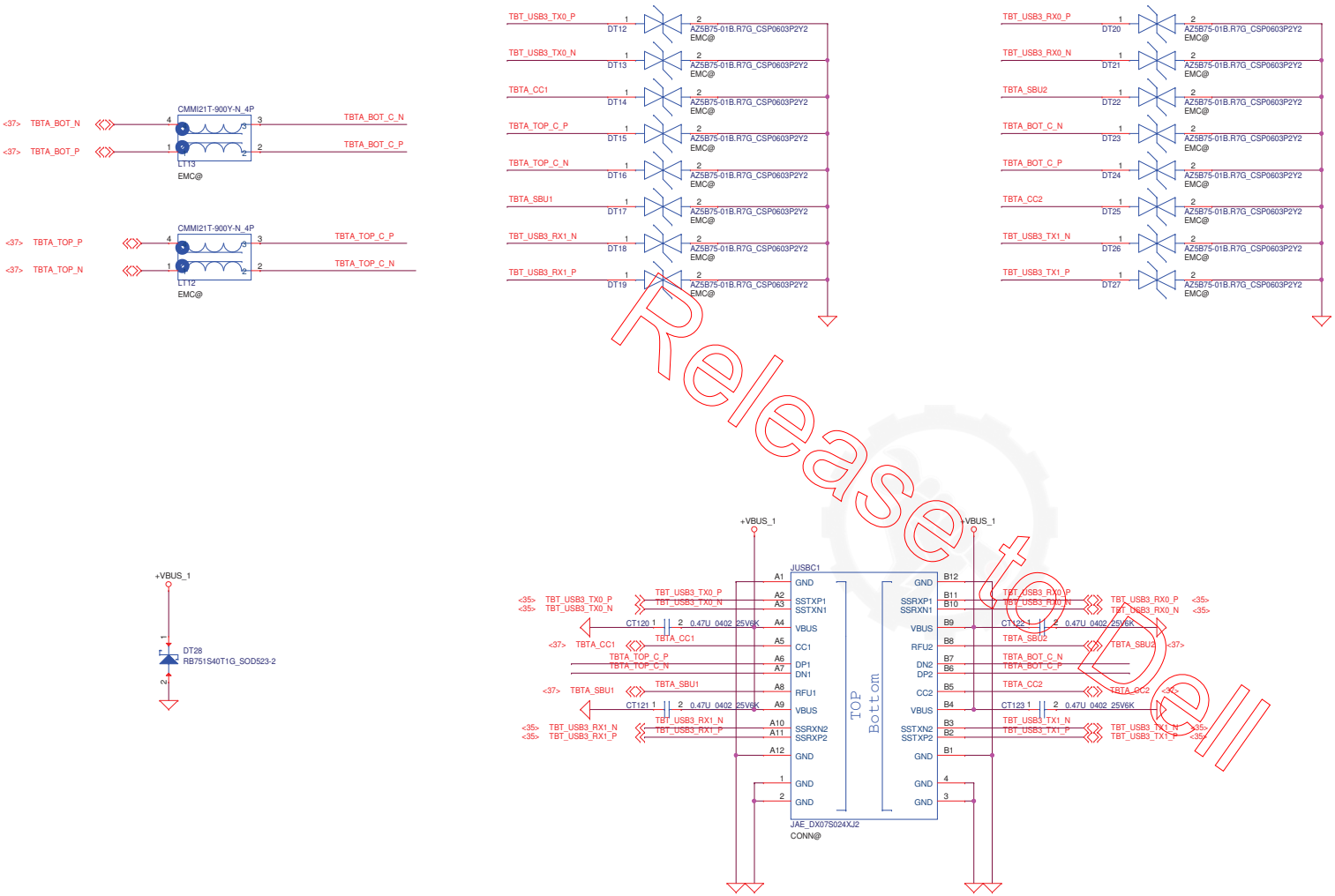
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P37-PD CONTROLLER**

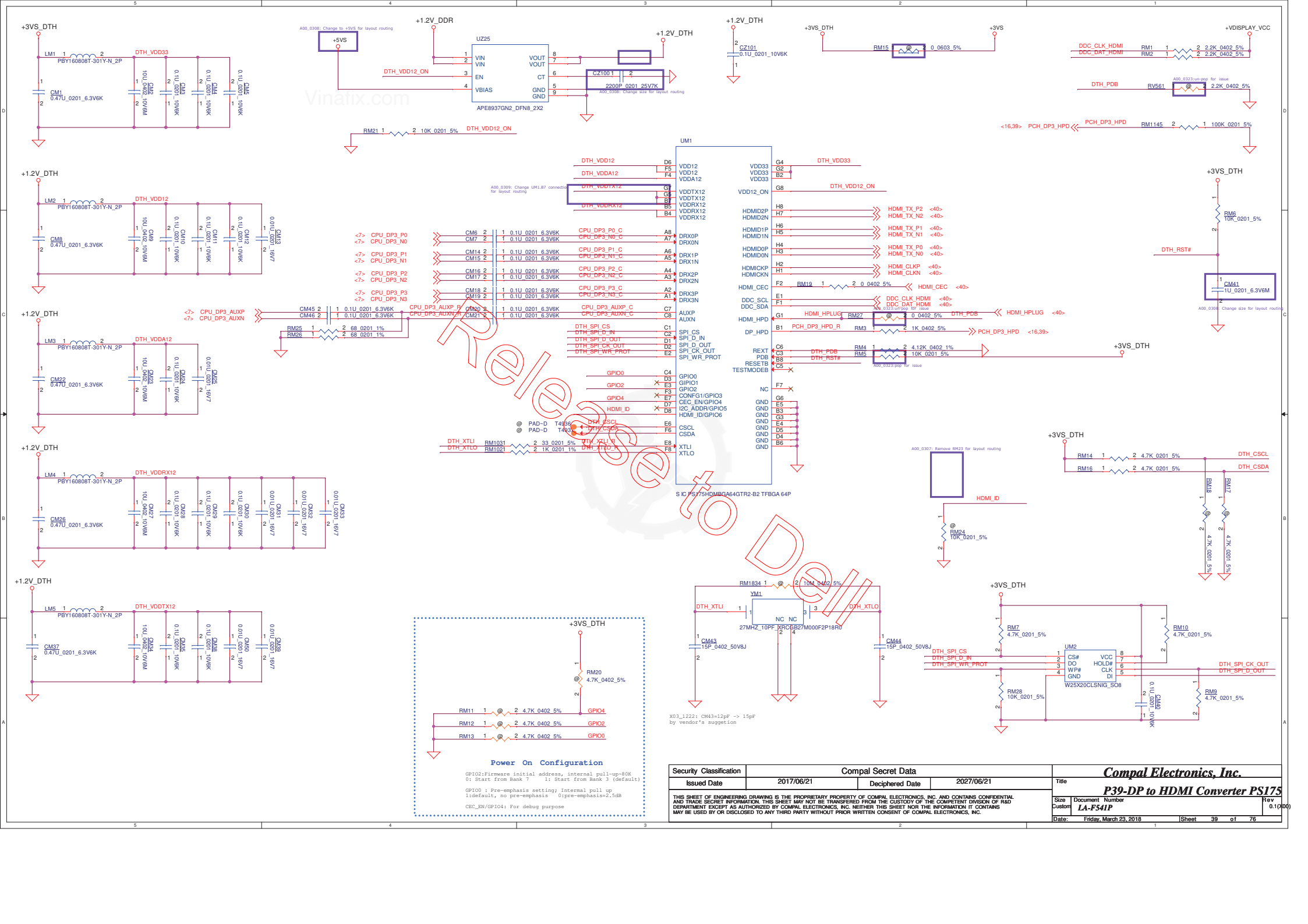
Size	Document Number	Rev
	LA-F541P	0.1(X00)

Date: Friday, March 23, 2018 | Sheet 37 of 76



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title: P38-PD USB TYPE-C CONN.			
Size: C	Document Number: LA-F541P		Rev: 0.1(000)
Date: Wednesday, March 28, 2018	Sheet 38 of 76		



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

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Compal Electronics, Inc.

Title: **P39-DP to HDMI Converter PS175**

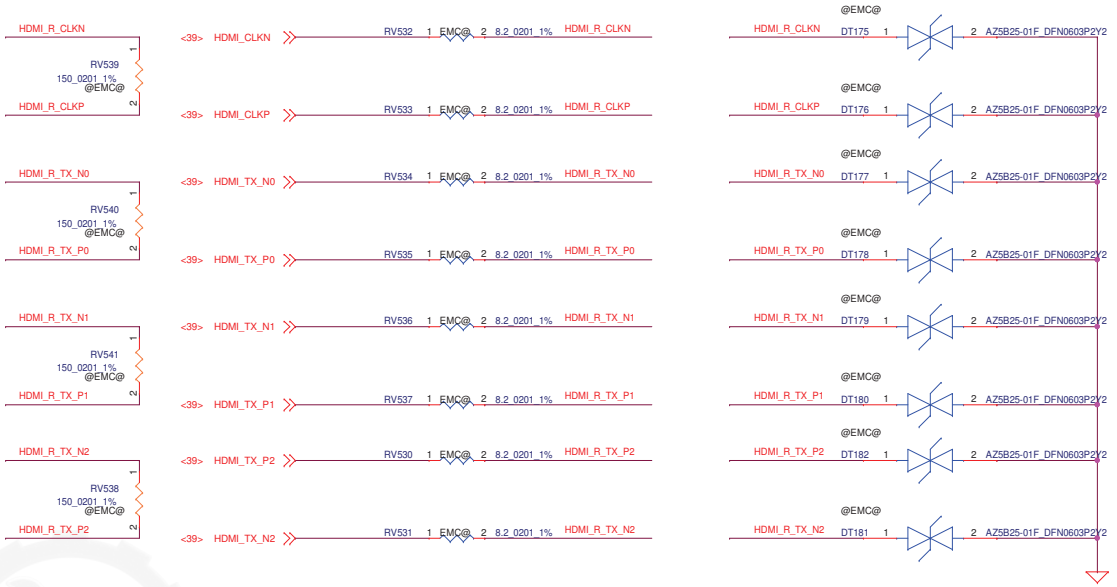
Size	Document Number	Rev
Custom	LA-F541P	0.1(X00)

Date: Friday, March 23, 2018 Sheet 39 of 76

HDMI change to CPU to PS185 to CONN

Place between ESD and CM-Choke

Place close to JHDMI1



HDMI DDC

HDMI conn

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

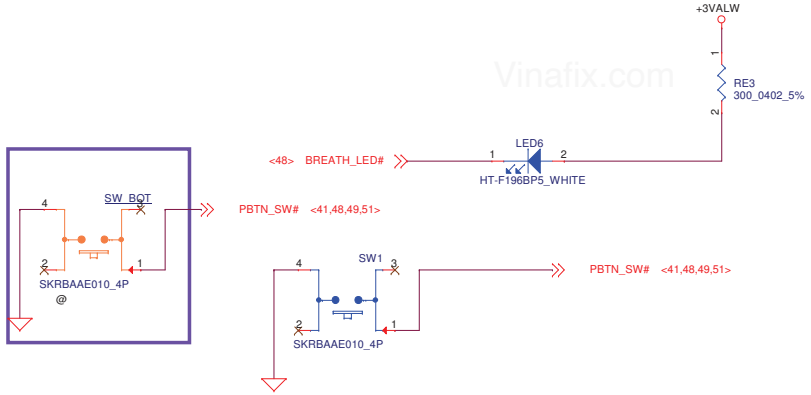
Compal Electronics, Inc.

Title: **P40-HDMI Connector**

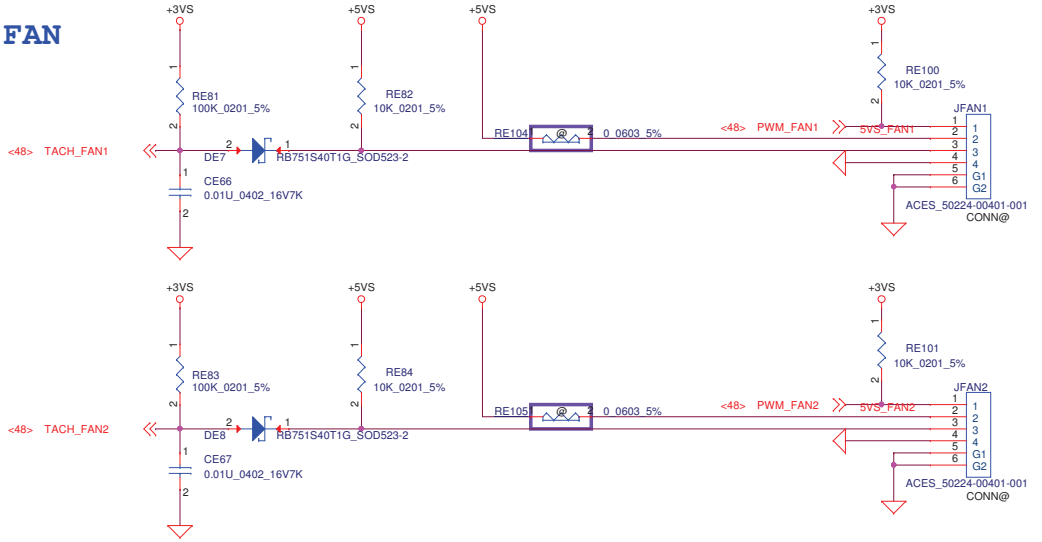
Size	Document Number	Rev
Custom	LA-F541P	0.1(X00)

Date: Friday, March 23, 2018 Sheet 40 of 76

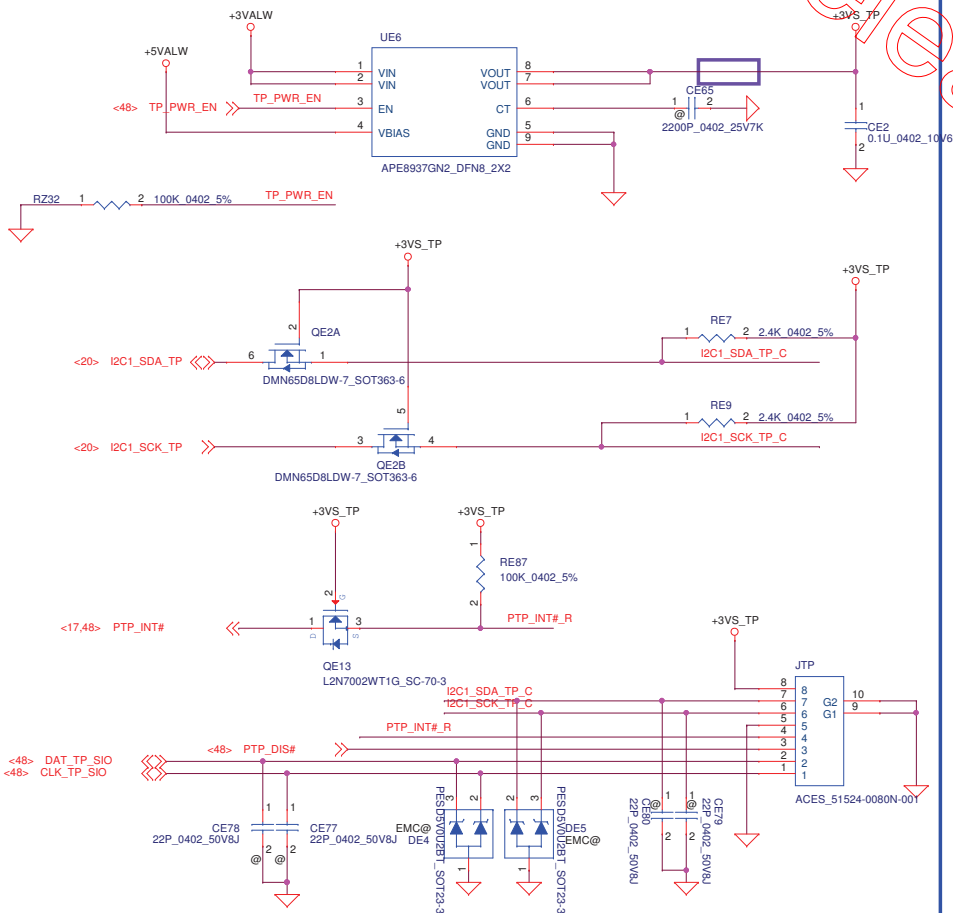
Power Button and LED



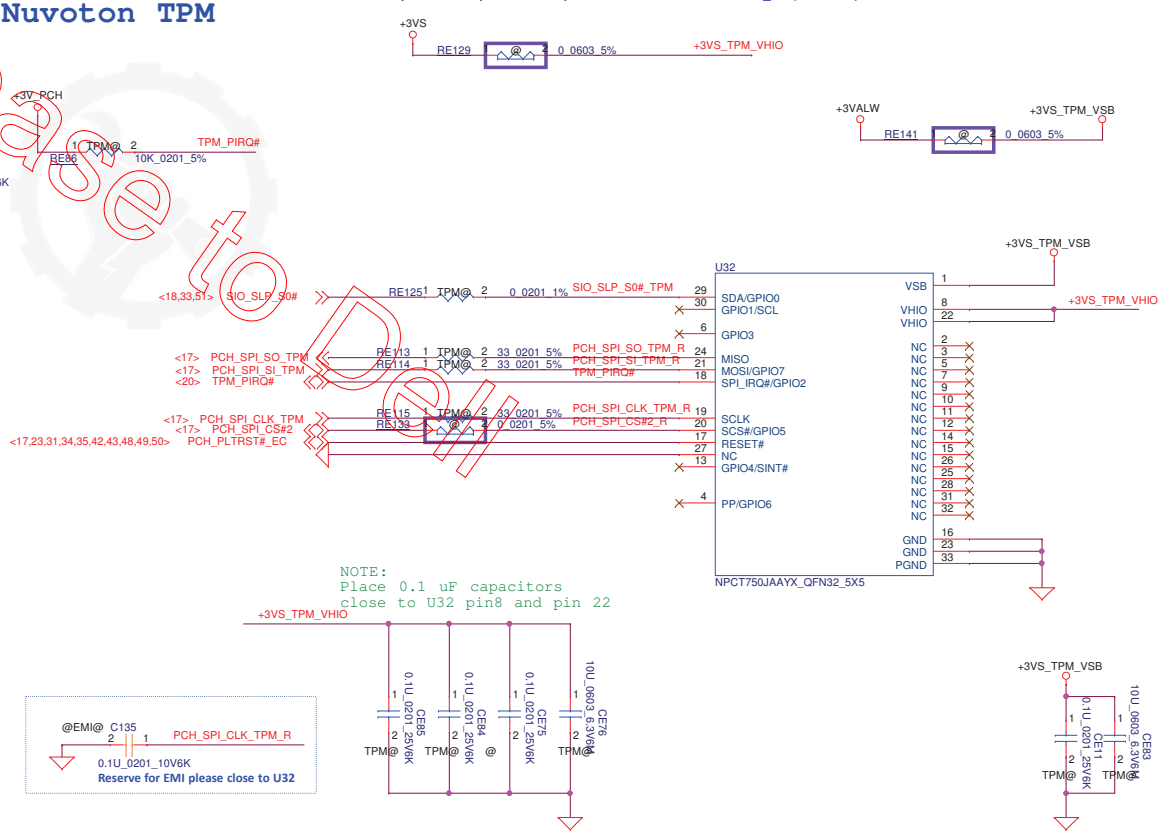
PWM FAN



Touch pad



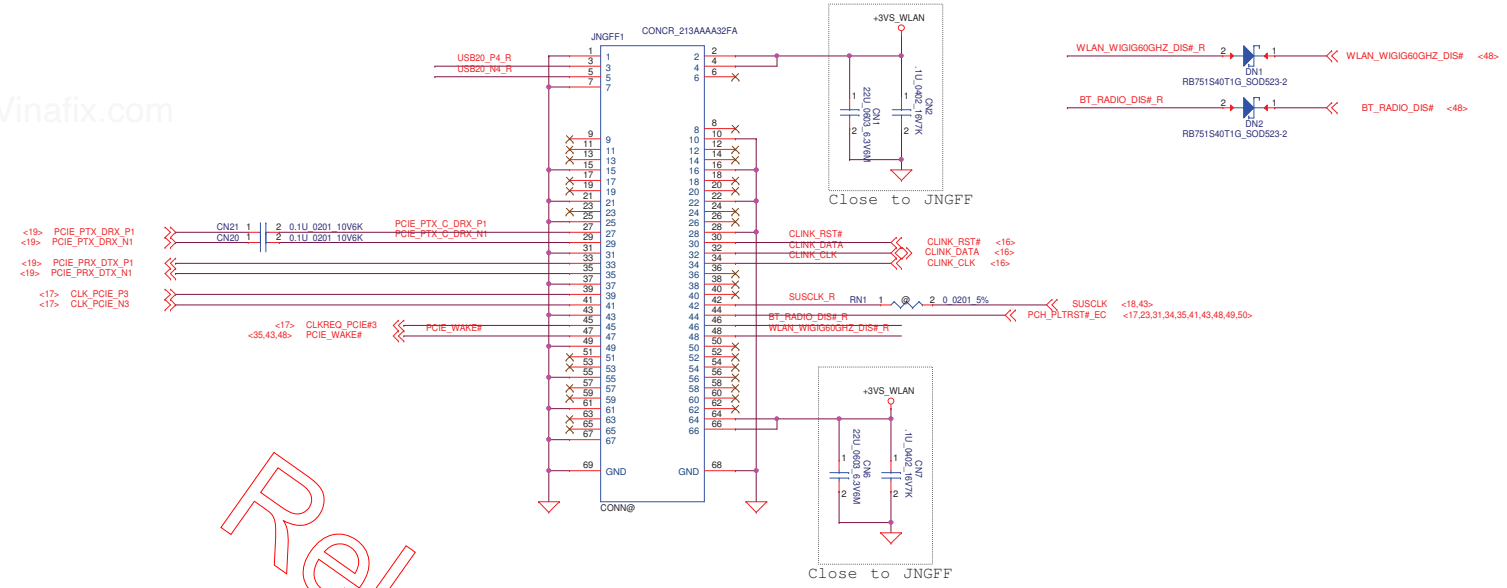
Nuvoton TPM



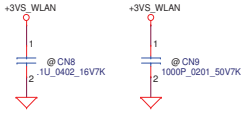
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

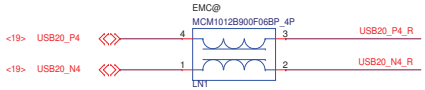
Compal Electronics, Inc.			
Title	P41-FAN/TP/TPM/SW		
Size: Custom	Document Number: LA-F541P		Rev: 0.1(X00)
Date: Friday, March 23, 2018	Sheet 41 of 76		

M.2 Slot-A Key-A (WLAN + BT)



Reserve for EMI





Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

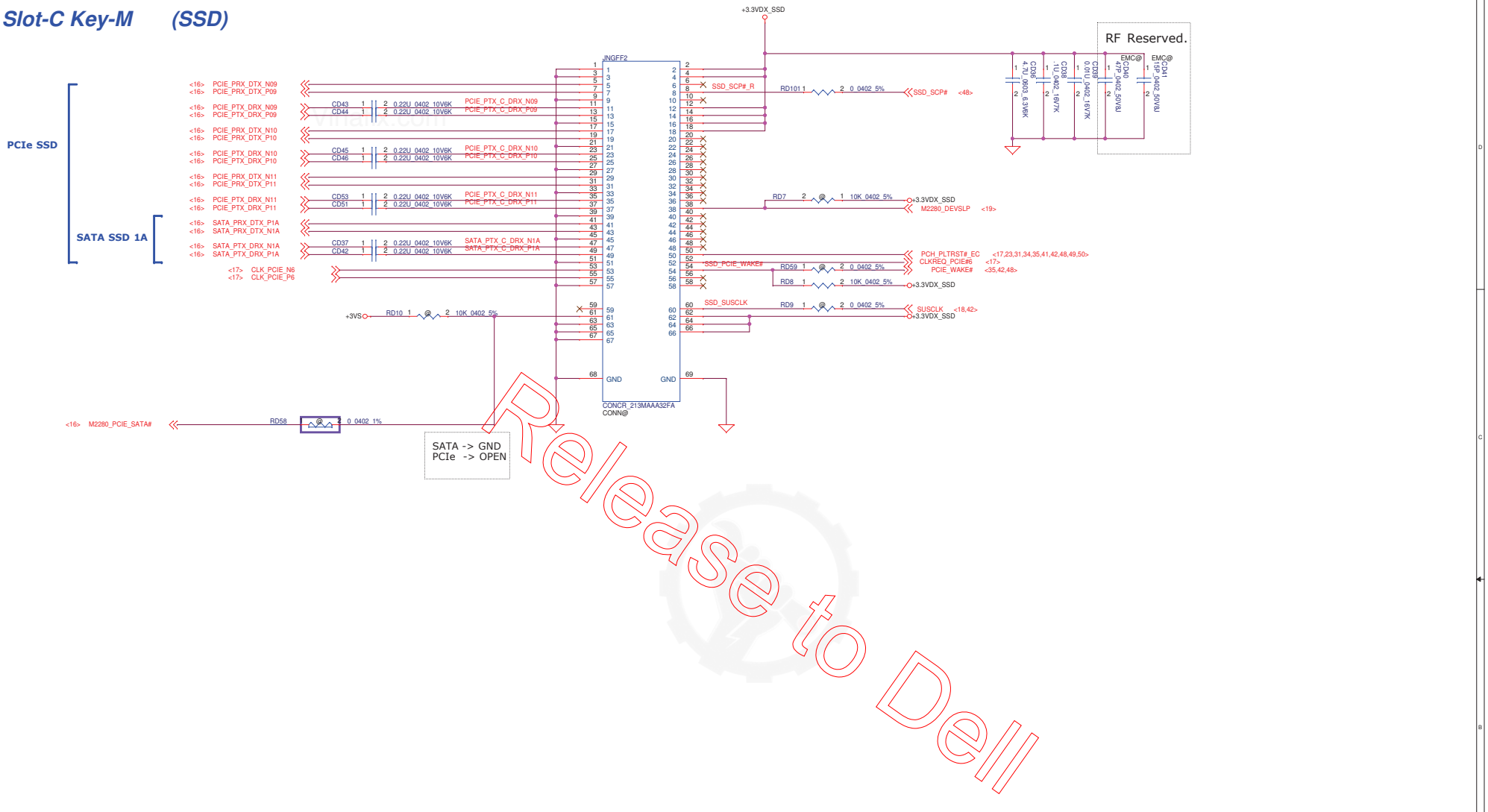
Compal Electronics, Inc.

Title: P42-NGFF-WLAN/BT

Size	Document Number	Rev
C	LA-F541P	0.1(000)

Date: Friday, March 23, 2018 | Sheet 42 of 76

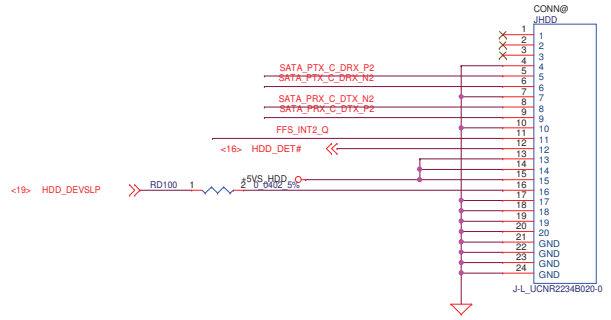
M.2 Slot-C Key-M (SSD)



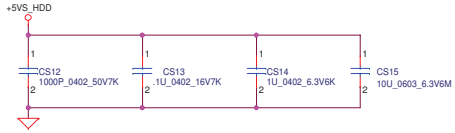
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

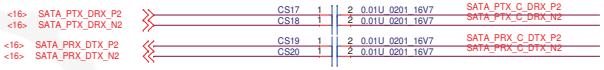
Compal Electronics, Inc.		
Title: P43-NGFF-SSD		
Size: C	Document Number: LA-F541P	Rev: 0.1(000)
Date: Friday, March 23, 2018	Sheet 43 of 76	

HDD CONN



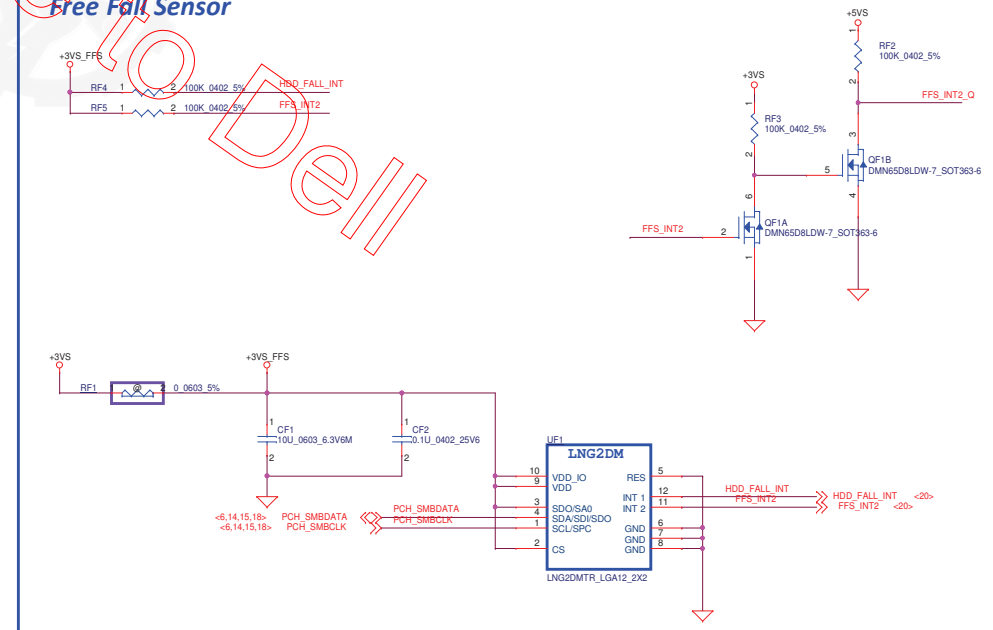
Place near HDD CONN (JHDD1)





BYPASS Circuit

Free Fall Sensor



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P44-HDD / FFS**

Size	Document Number	Rev
C	LA-F541P	0.1(X00)

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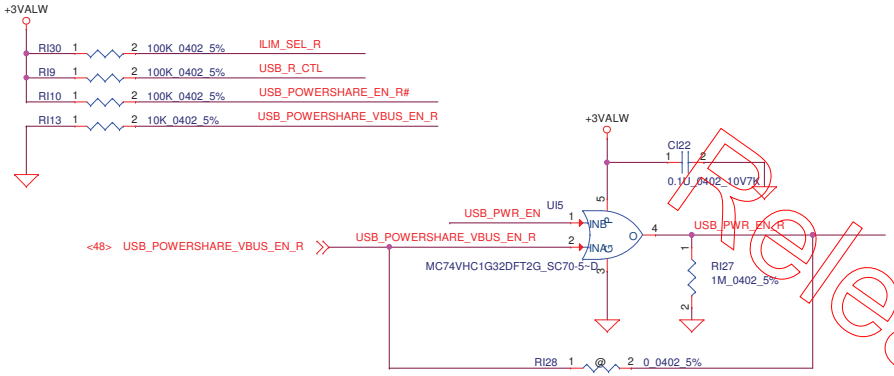
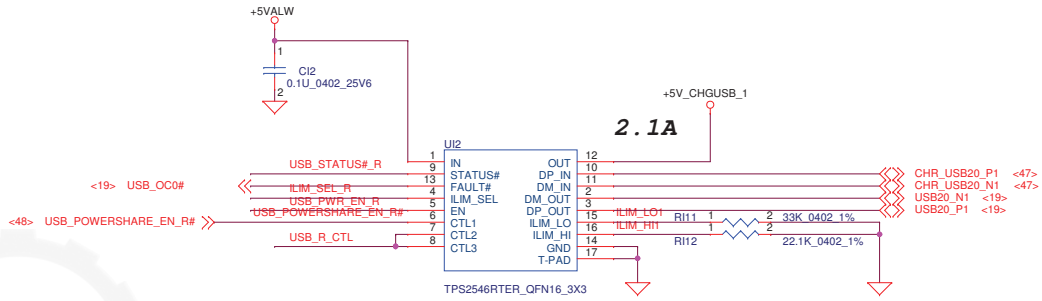
USB Powershare

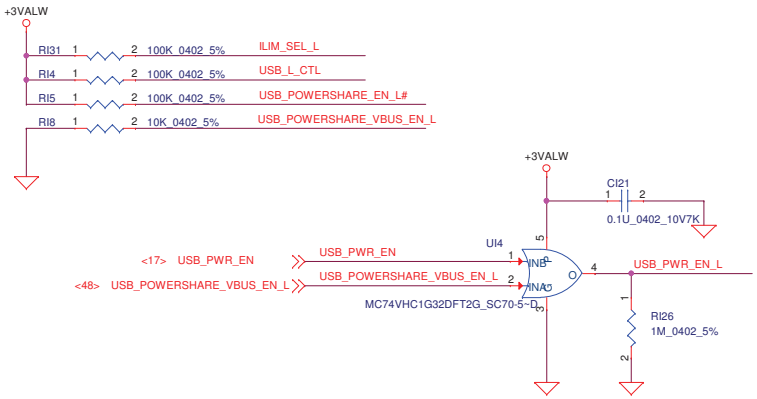
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

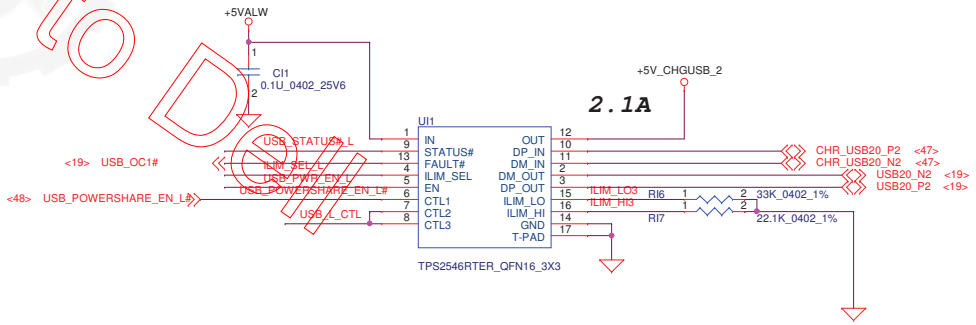


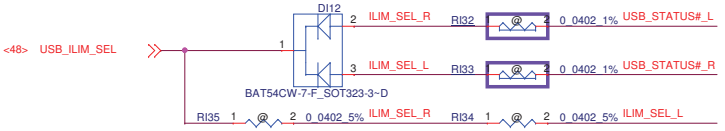
USB3.1 / USB2.0 Port1 (Right Side)





USB3.1 / USB2.0 Port2 (Left Side)





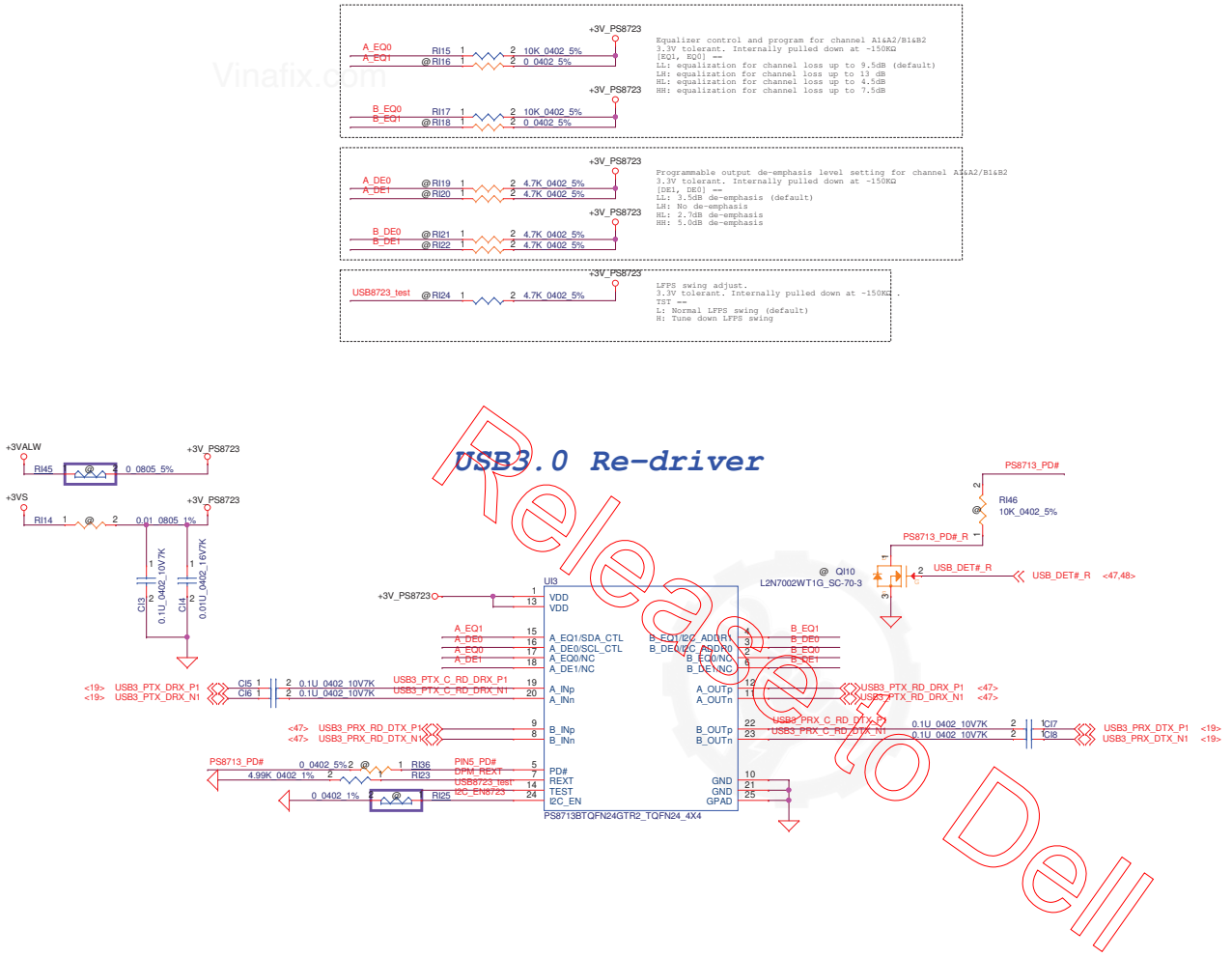
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P45-USB Powershare

Size | Document Number: LA-F541P | Rev: 0.1(X00)

Date: Friday, March 23, 2018 | Sheet 45 of 76



USB3.0 Re-driver

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

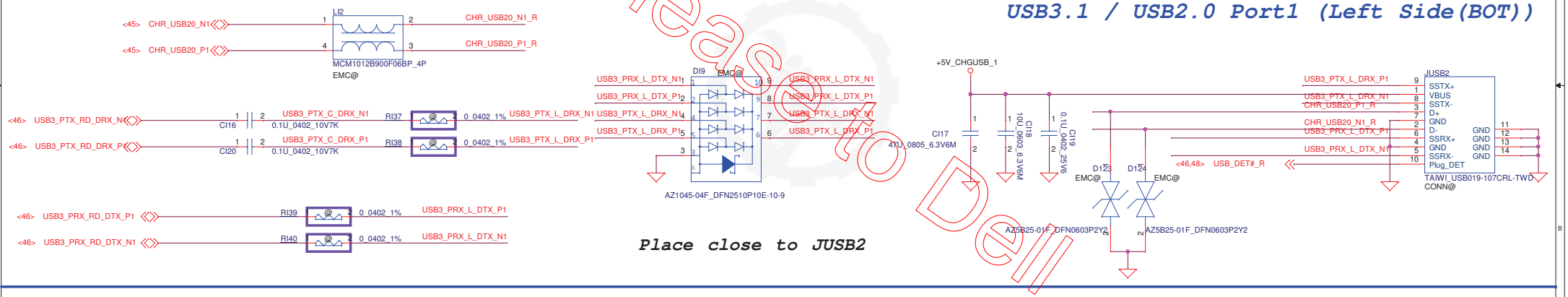
Compal Electronics, Inc.

Title: P46-USB3.1 retimer

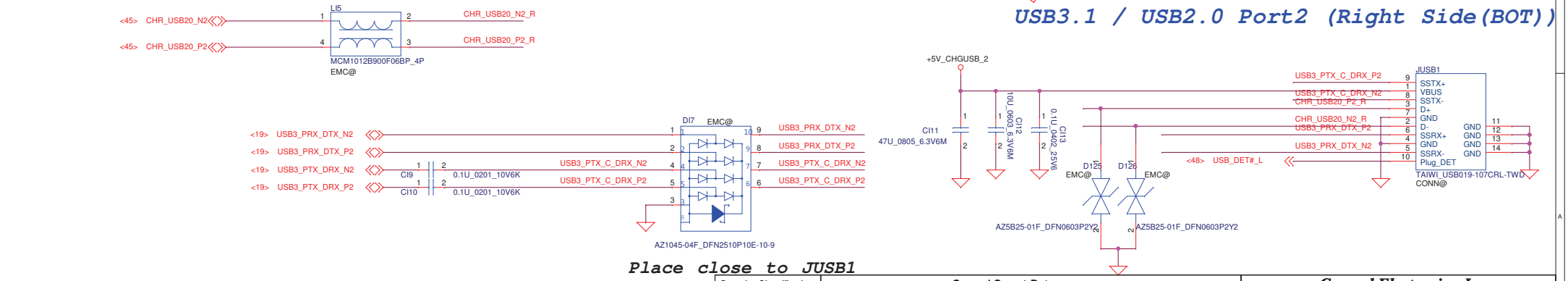
Size	Document Number	Rev
Custom		0.1(100)

Date: Friday, March 23, 2018 Sheet 46 of 76

USB3.1 / USB2.0 Port1 (Left Side(BOT))



USB3.1 / USB2.0 Port2 (Right Side(BOT))



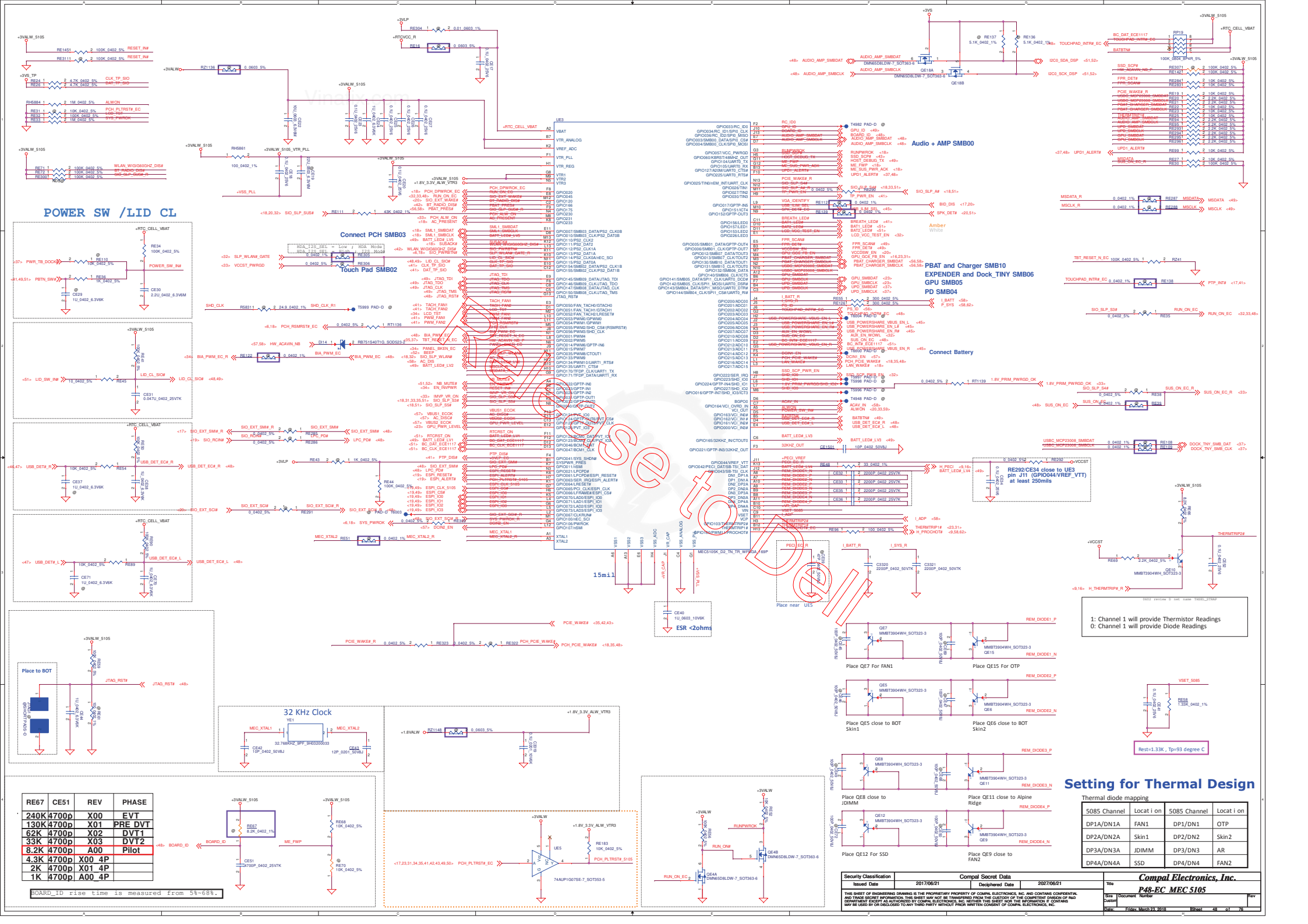
Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P47-USB3.1/USB2.0 conn

Size | Document Number: LA-F541P | Rev: 0.1(X00)

Date: Friday, March 23, 2018 | Sheet 47 of 76



RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	Pilot
4.3K	4700p	X00_4P	
2K	4700p	X01_4P	
1K	4700p	A00_4P	

5085 Channel	Locat i on	5085 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDIMM	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

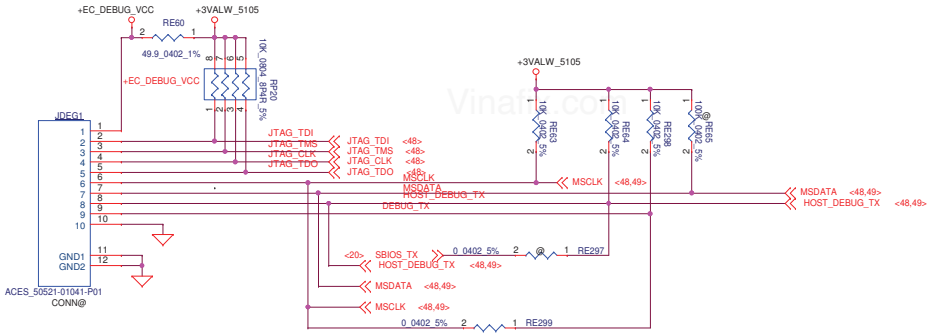
Compal Electronics, Inc.

Title: P48-EC MEC 5105

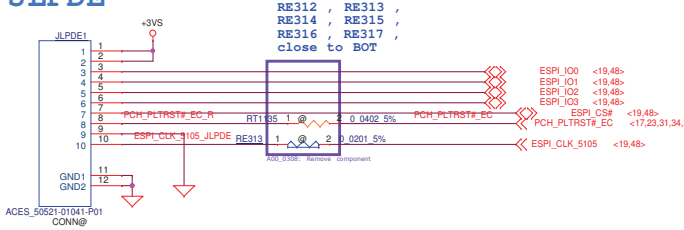
Size: Custom | Document Number | Rev

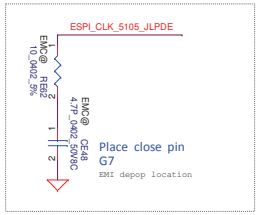
Date: Friday, March 23, 2018 | Sheet 48 of 78

JDEG

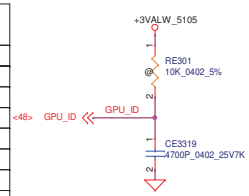


JLPDE

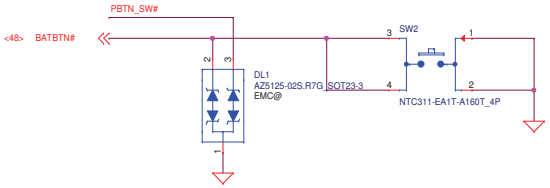




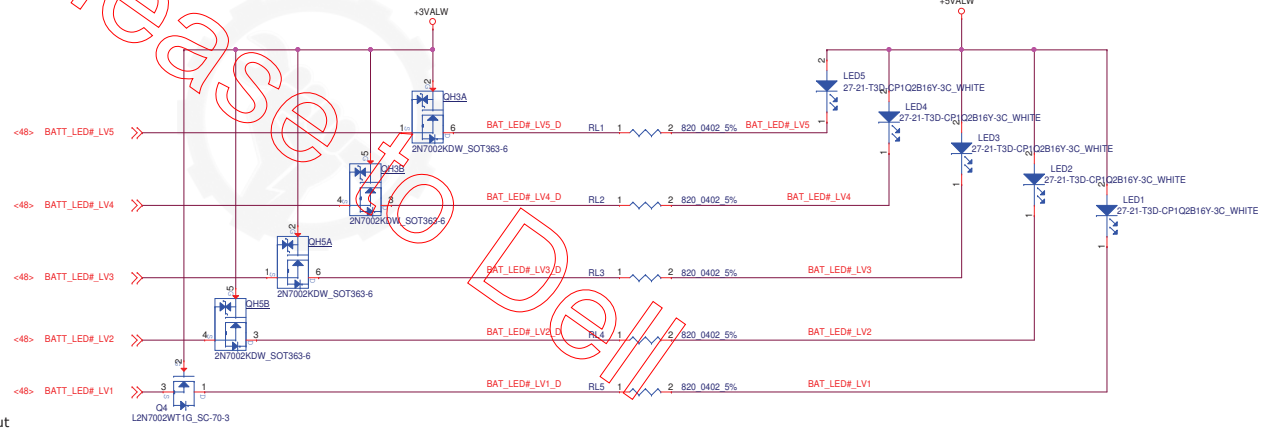
RE301	CE3319	REV
240K	4700p	i3 CPU/UMA
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	



BATT LED Power Button

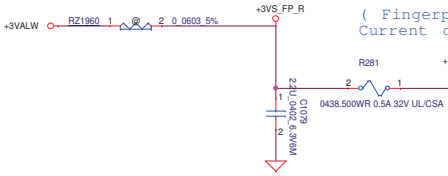


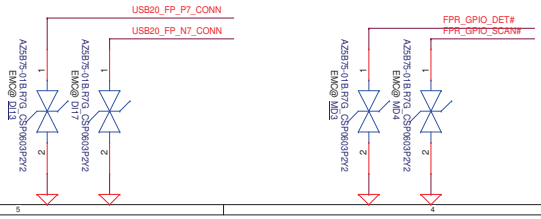
Bat t ery Gauge LED

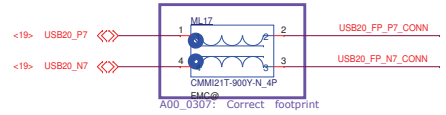


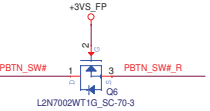
EC GPIO set to OD output

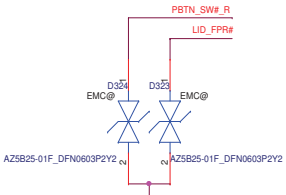
Finger Print circuit

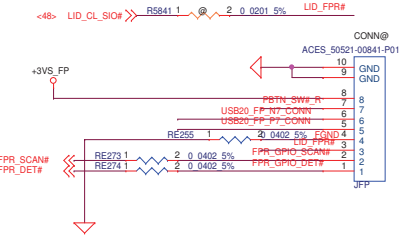












Fingerprint Reader CONN

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P49-BAT LED/BUZZER/FP

Size	Document Number	Rev
C	LA-F541P	0.1(X00)

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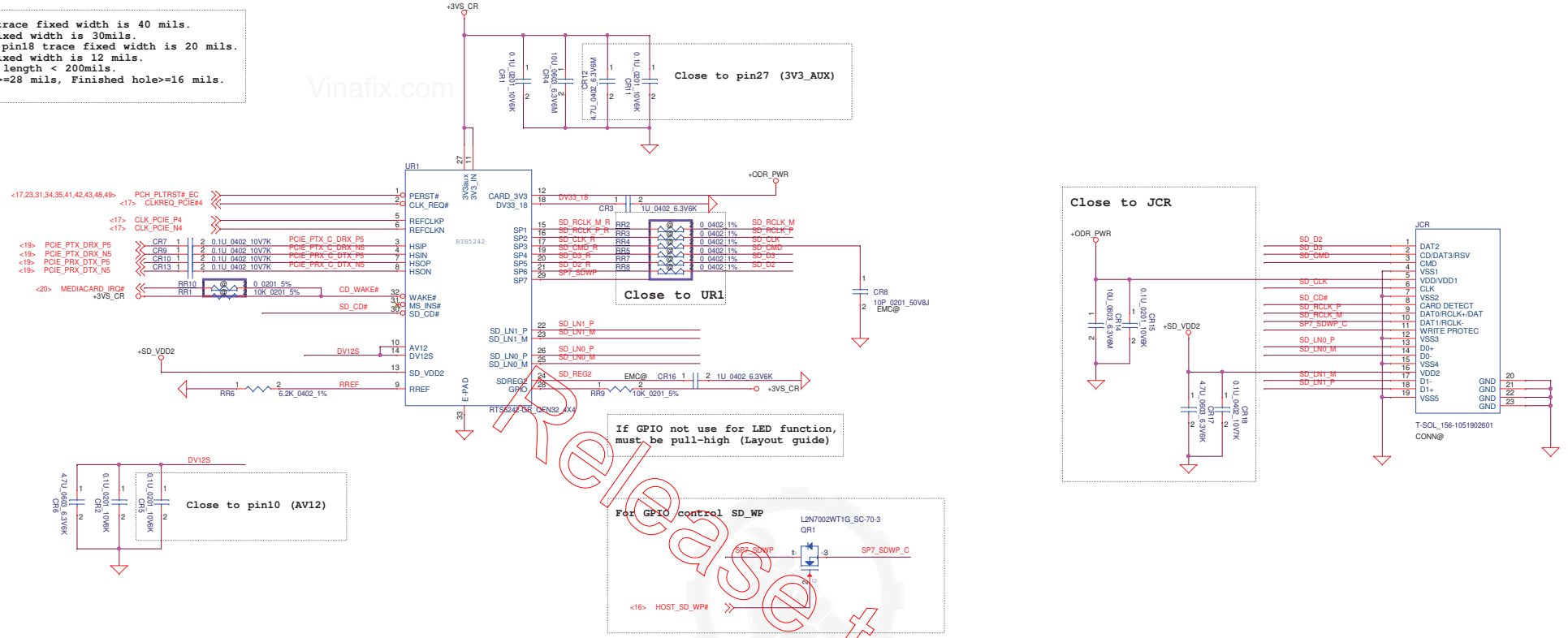
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P50-Card Reader**

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		0.1(X00)

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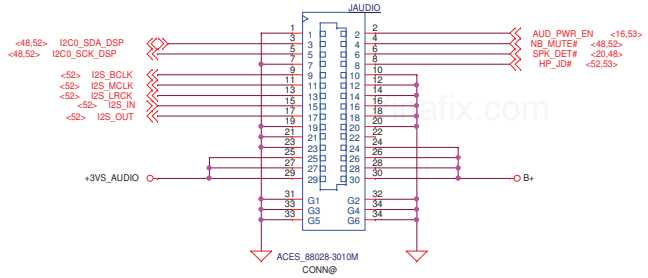
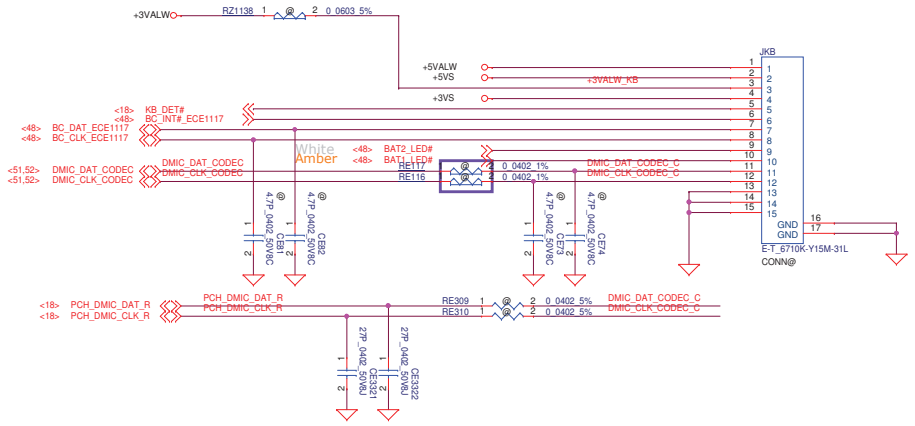
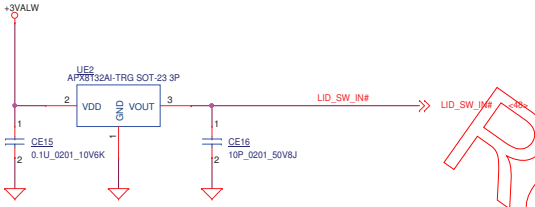
AUDIO Board Conn.



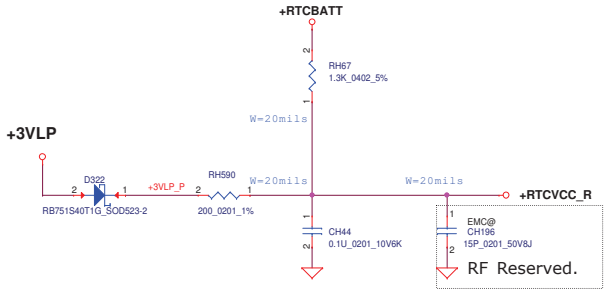
Keyboard Controller board + DMIC

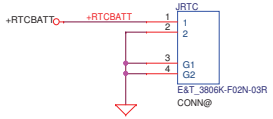


Lid Switch

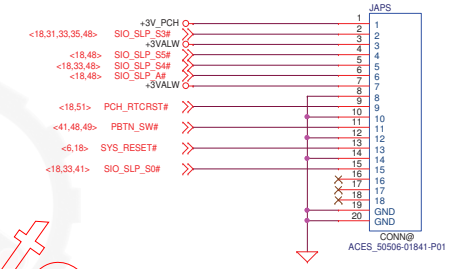


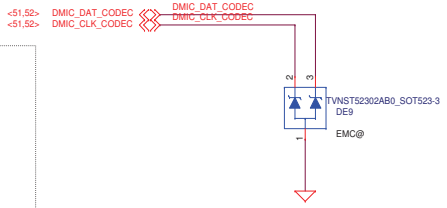
RTC Battery With Charge Function



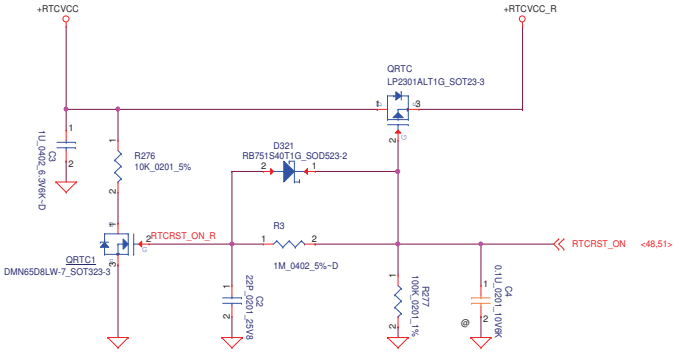


APS CONN

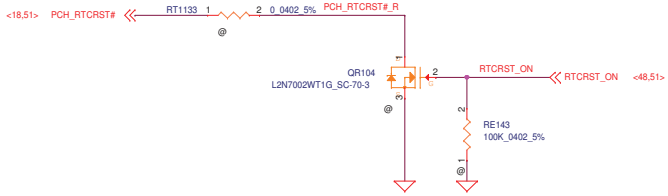




Default: OD EC drives GPIOs to LOW to turn off power to VCCRTC.



follow Intel Keep old RTC



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P51-CONN/Lid/RTC**

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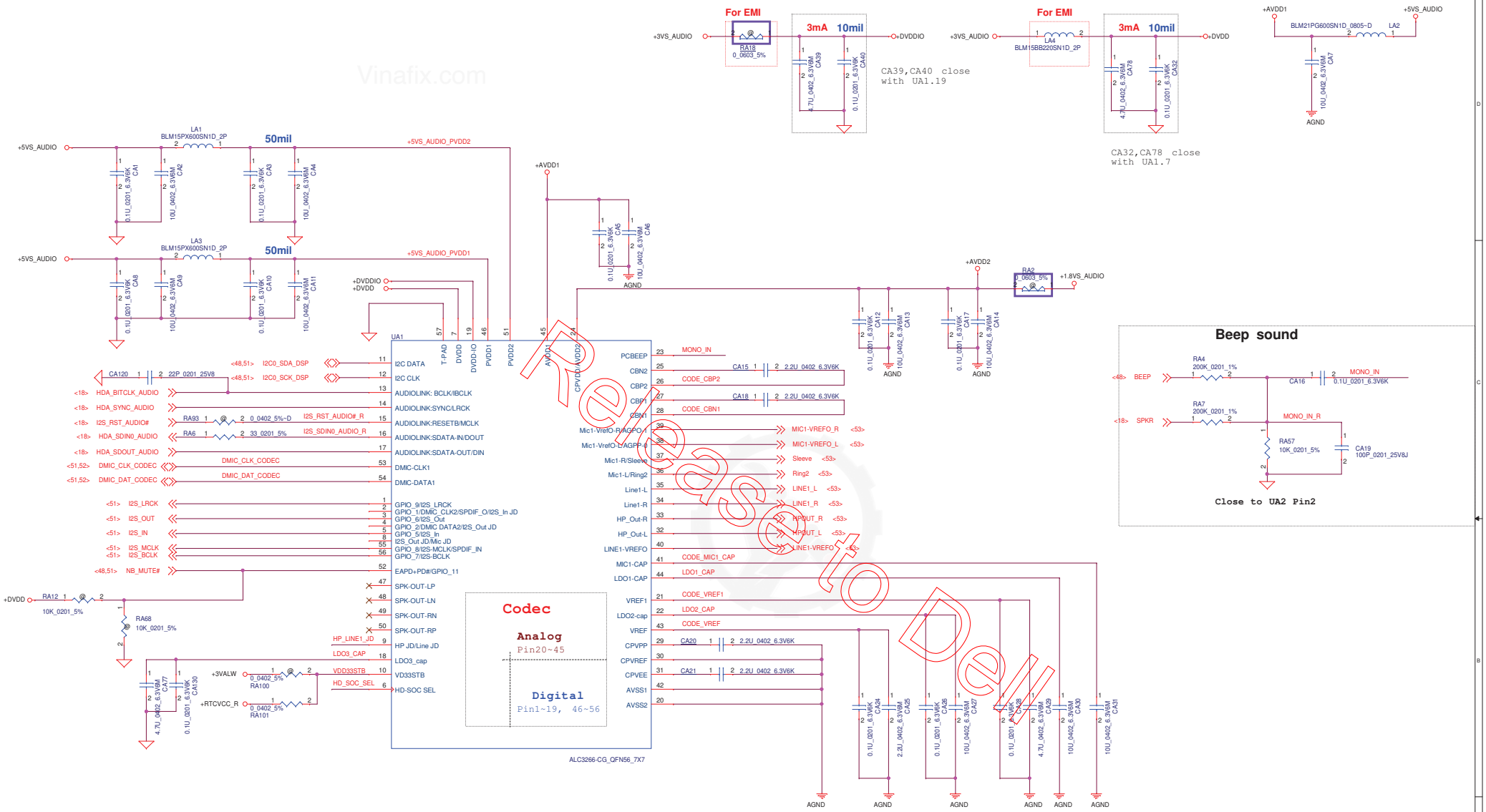
HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

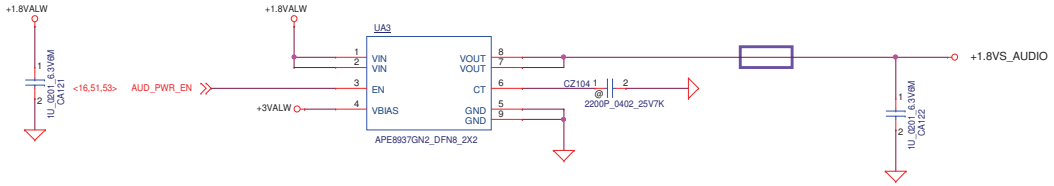
Compal Electronics, Inc.

Title: P52-ALC3266

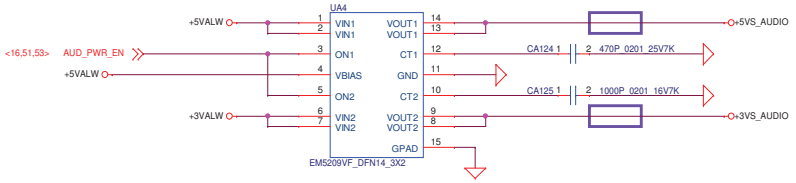
Size | Document Number: LA-F541P | Rev: 0.1(X00)

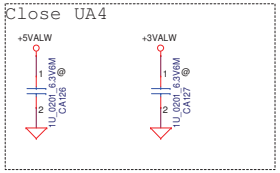
Date: Friday, March 23, 2018 | Sheet 52 of 76

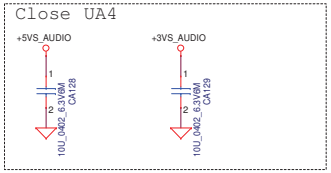
+1.8VALW To +1.8VS_AUDIO



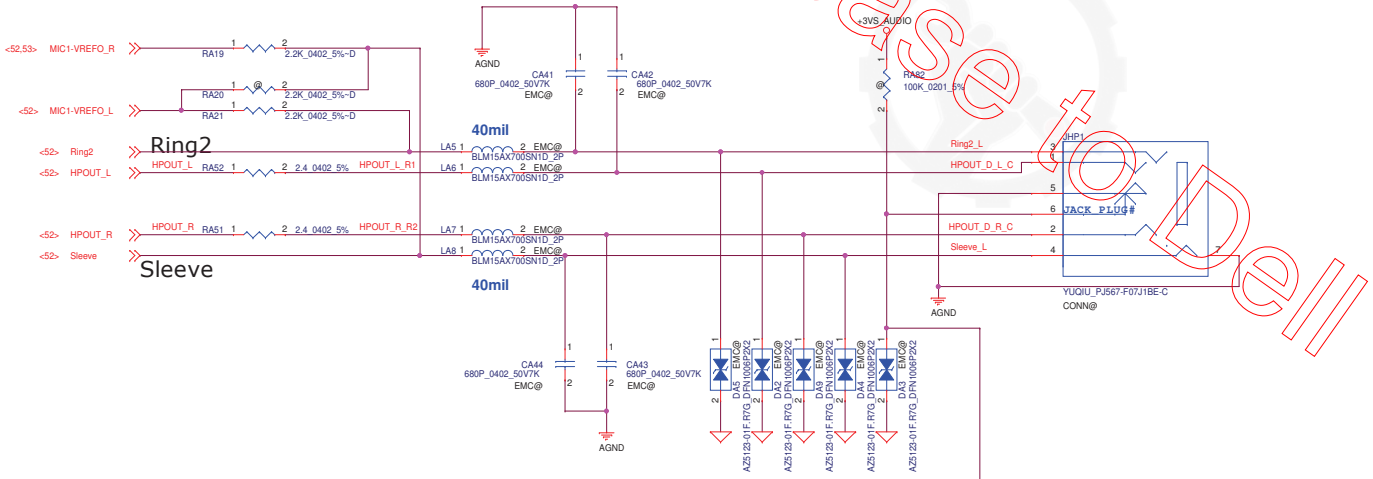
+5VALW and +3VALW To +5VS_AUDIO and +3VS_AUDIO



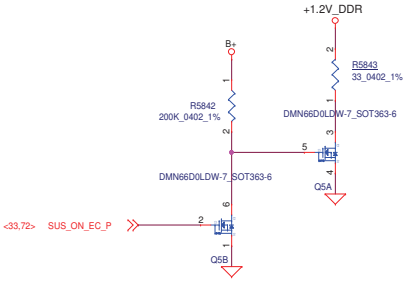




Universal Audio Jack



1.2V DDR dischager



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

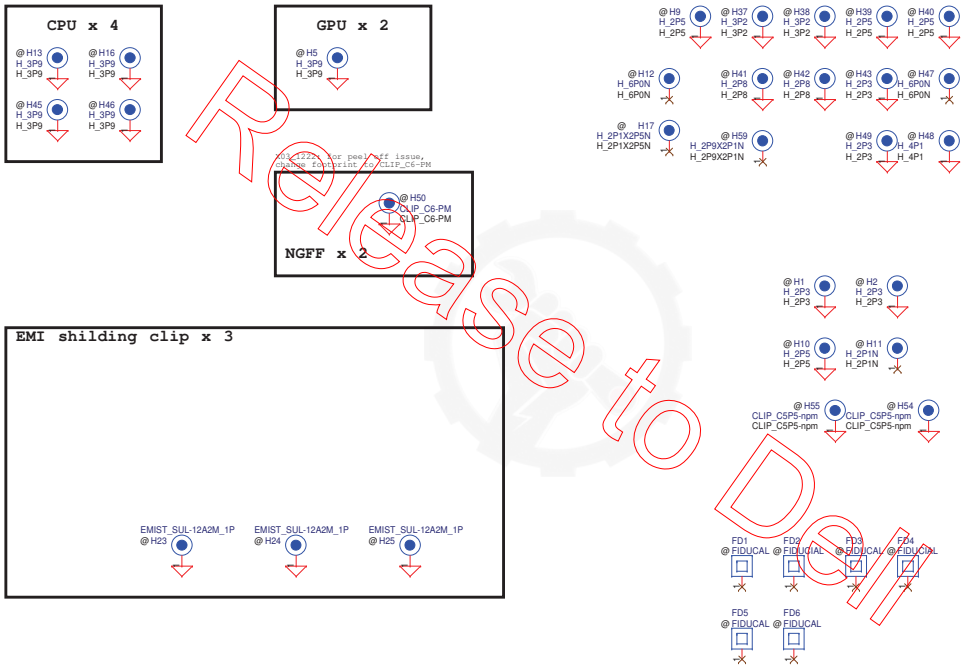
Compal Electronics, Inc.

Title: P53-Audio_Jack

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

Date: Friday, March 23, 2018 | Sheet 53 of 76

Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: **P54-Screws**

Size	Document Number	Rev
		0.1(X00)

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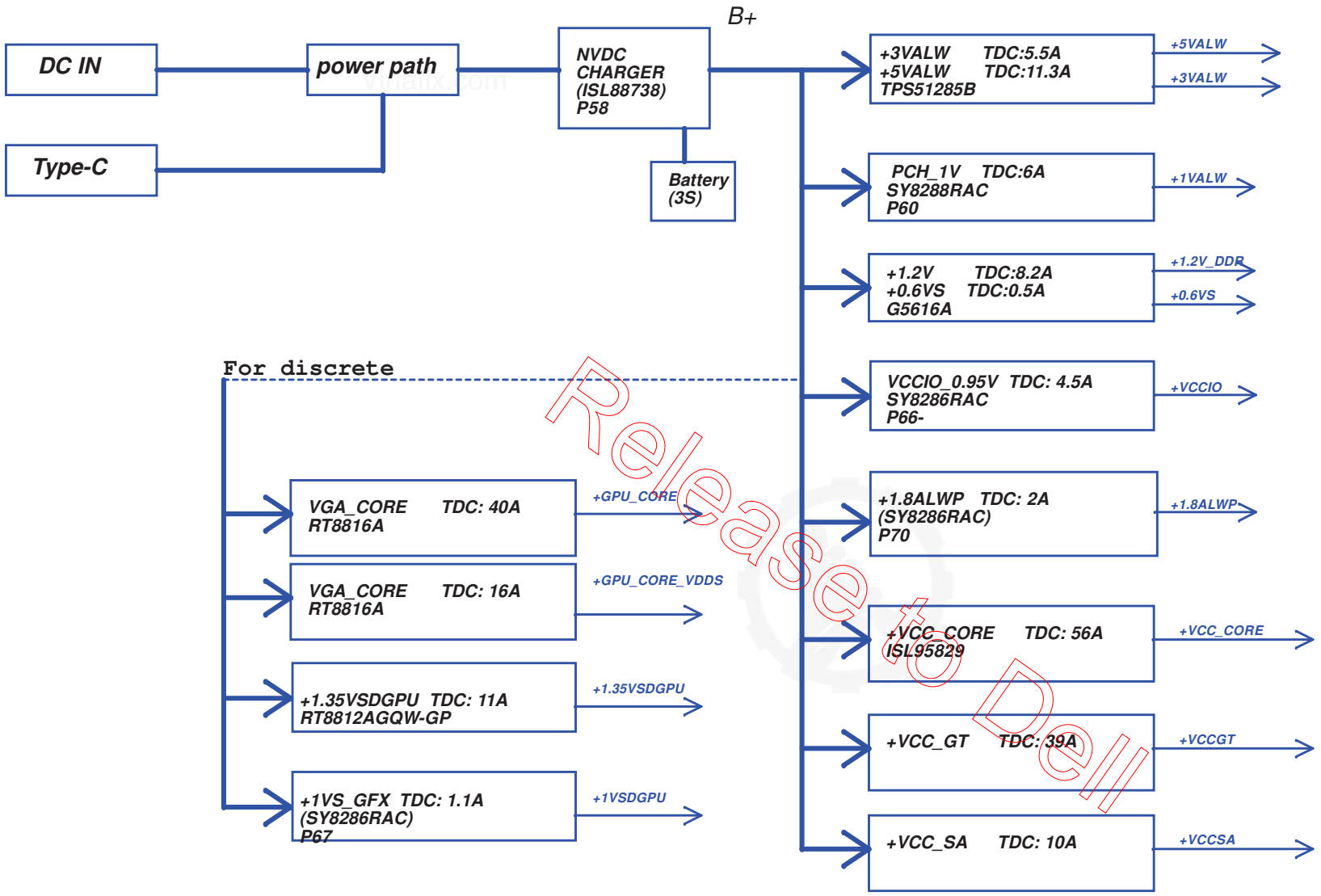
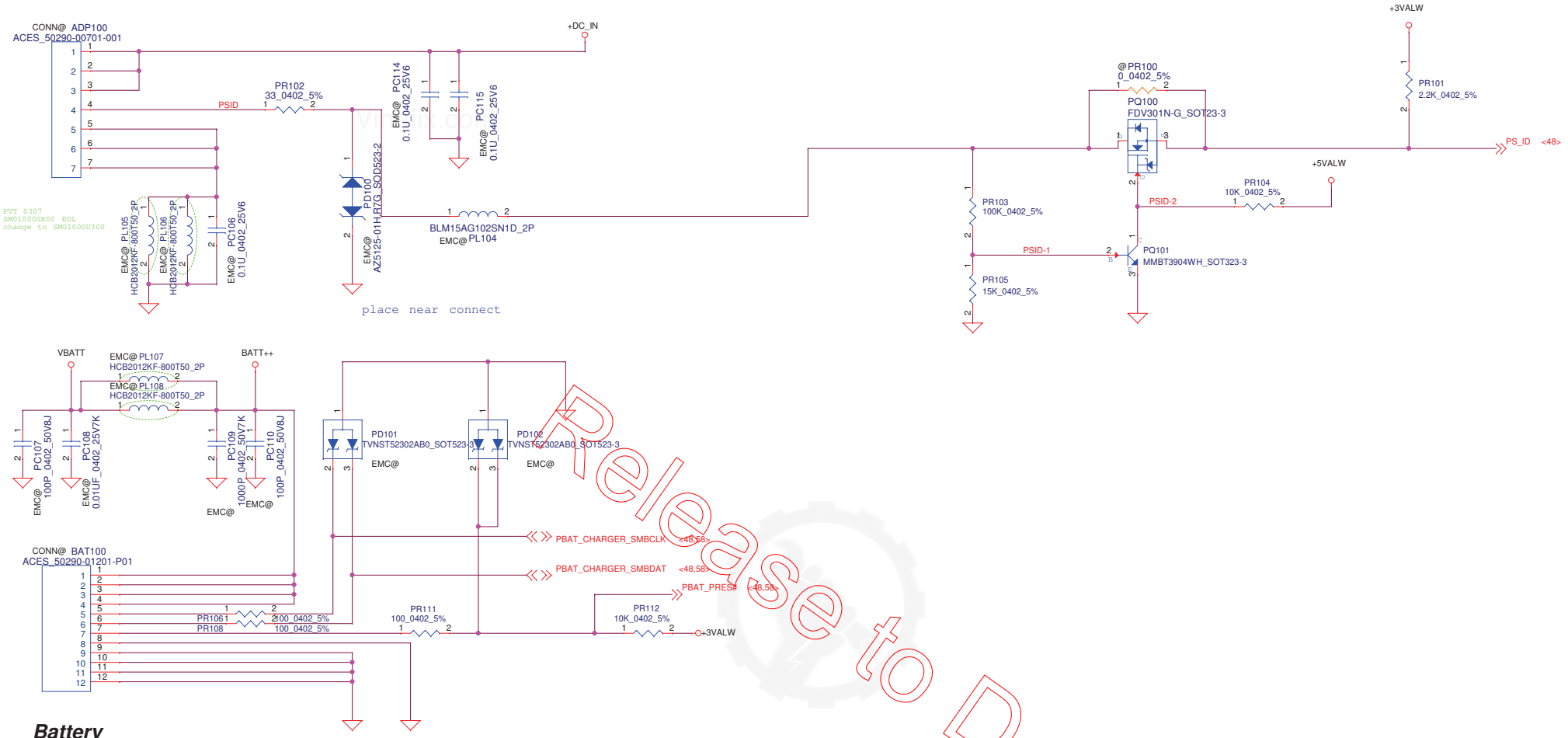


@ : Nopop Component
@DIS@ : Nopop Component
DIS@: POP for discrete GPU SKU

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.			
Title	P55-Power Block Diagram		
Size	Document Number		Rev 0.1(X00)
Date: Friday, March 23, 2018		Sheet 55 of 74	



Battery
(3S2P) 97W
(3S1P) 56W

JIMBTY battery connector

SMART
Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Smart Adapter circuit (39.1)

Compal Electronics, Inc.
Title: P56-PWR_DCIN / BATT CONN / OTP
Size: Document Number: LA-F541P
Rev: 0.1(X00)
Date: Friday, March 23, 2018
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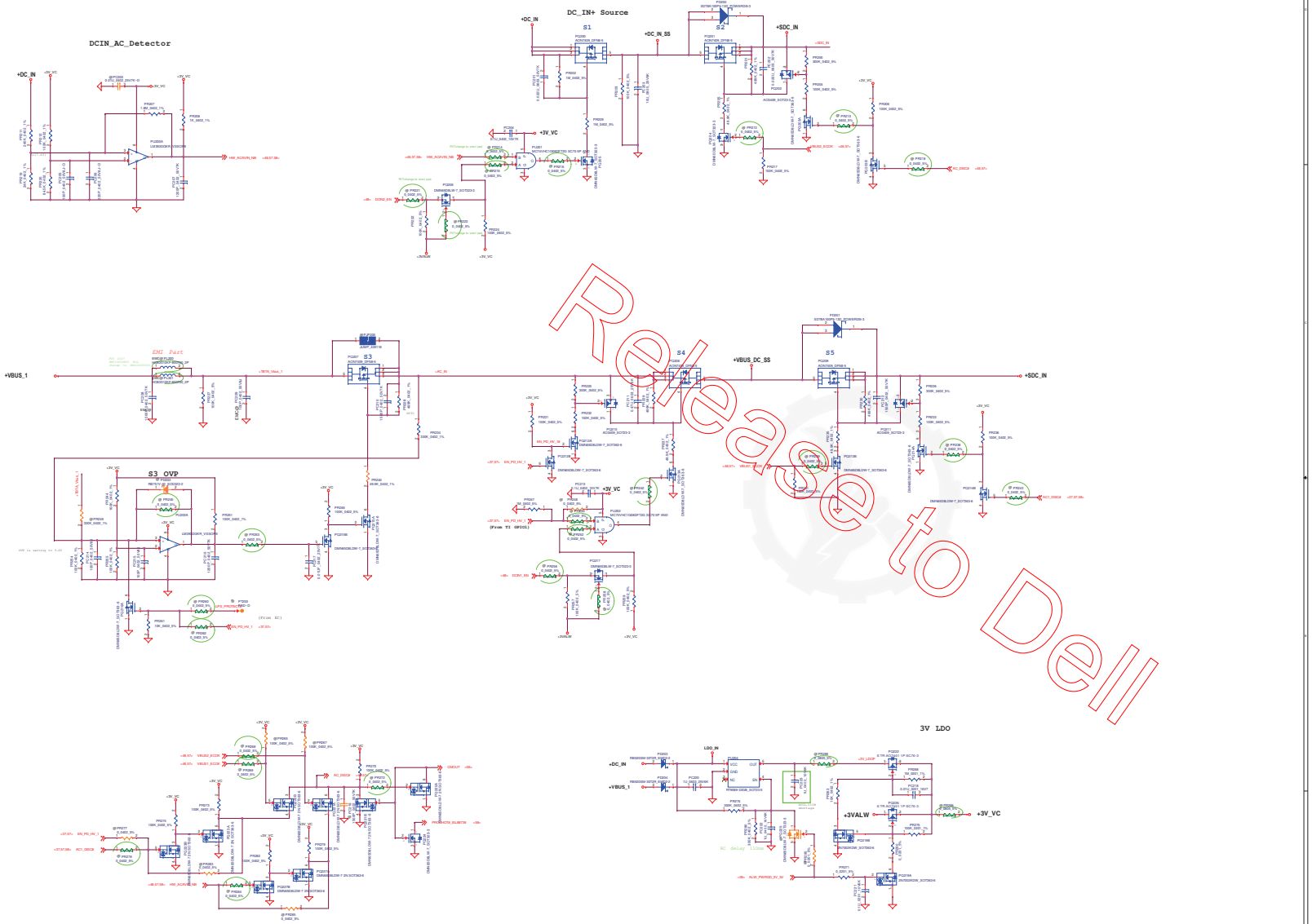

Title	P57-PWR_Switch
Size	Document Number
Custom	P57/P
Date	Friday, March 08, 2019
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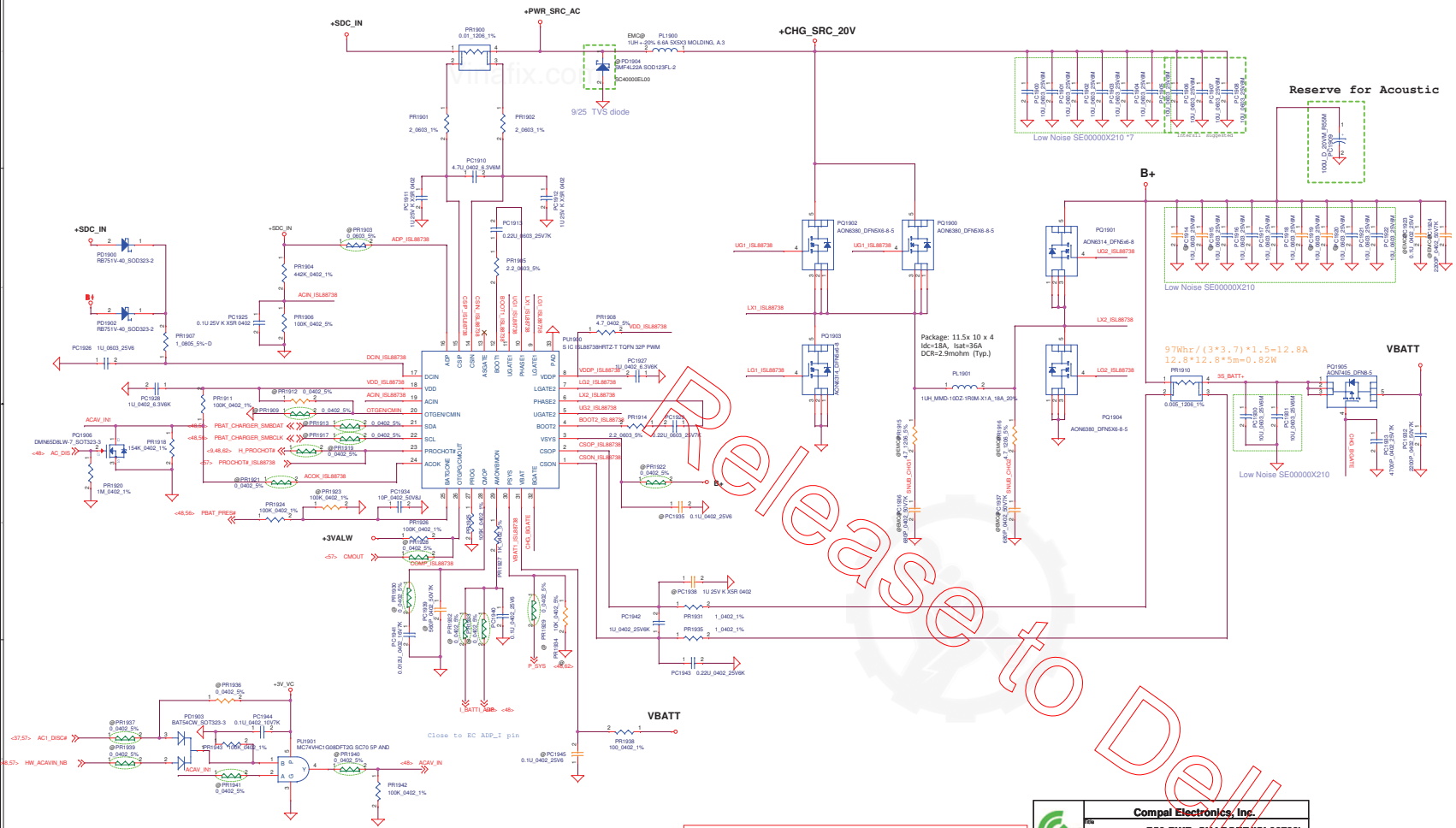

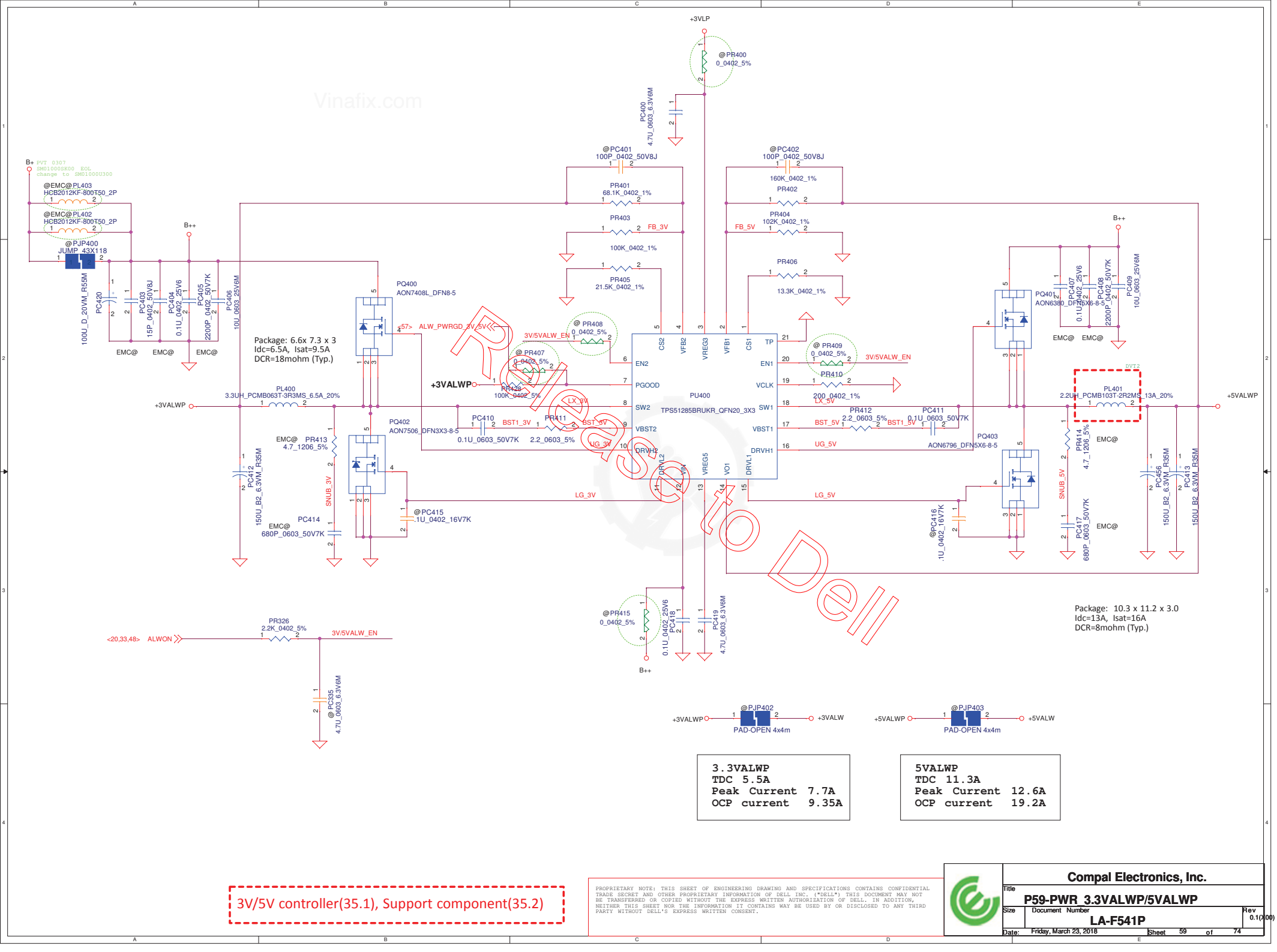
+3VLP
@PR400 0_0402_5%
PC400 4.7U_0603_6.3V6M
@PC401 100P_0402_50V8J
@PC402 100P_0402_50V8J
PR401 68.1K_0402_1%
PR402 160K_0402_1%
PR403 100K_0402_1%
PR404 102K_0402_1%
PR405 21.5K_0402_1%
PR406 13.3K_0402_1%
B+
PVT 0307
SM01000SK00 EOL
change to SM01000U300
@EMC@PL403 HCB2012KF-800T50_2P
@EMC@PL402 HCB2012KF-800T50_2P
@PJP400 JUMP_43X118
B++
PC420 100U_D_20VM_R55M
PC403 15P_0402_50V8J
PC404 0.1U_0402_25V6
PC405 2200P_0402_50V7K
PC406 10U_0603_25V6M
EMC@
Package: 6.6x 7.3 x 3
Idc=6.5A, Isat=9.5A
DCR=18mohm (Typ.)
PQ400 AON7408L_DFN8-5
<57> ALW_PWRGD_3V_5V
3V/5VALW_EN
@ PR408 0_0402_5%
@ PR407 0_0402_5%
PR429 100K_0402_5%
+3VALWP
PU400 TPS51285BRUKR_QFN20_3X3
CS2 VFB2 VREG3 VFB1 CS1
EN2 PGOOD SW2 VBST2 DRVH2 DRVL2 VIN VREG5 VO1 DRVL1 VBST1 DRVH1 SW1 VCLK EN1 TP
@ PR409 0_0402_5%
PR410 200_0402_1%
PL400 3.3UH_PCMB063T-3R3MS_6.5A_20%
PC410 0.1U_0603_50V7K
PR411 2.2_0603_5%
PC411 0.1U_0603_50V7K
PR412 2.2_0603_5%
PQ402 AON7506_DFN3X3-8-5
PQ403 AON6796_DFN5X6-8-5
PR413 4.7_1206_5%
PC412 150U_B2_6.3VM_R35M
PC414 680P_0603_50V7K
@PC415 .1U_0402_16V7K
@PC416 .1U_0402_16V7K
LX_5V
BST_5V
BST1_5V
UG_5V
LG_5V
SNUB_5V
PQ401 AON6380_DFN5X6-8-5
PC407 0.1U_0402_25V6
PC408 2200P_0402_50V7K
PC409 10U_0603_25V6M
PL401 2.2UH_PCMB103T-2R2MS_13A_20%
PR414 4.7_1206_5%
PC417 680P_0603_50V7K
PC456 150U_B2_6.3VM_R35M
PC413 150U_B2_6.3VM_R35M
+5VALWP
DVT2
Package: 10.3 x 11.2 x 3.0
Idc=13A, Isat=16A
DCR=8mohm (Typ.)
PR326 2.2K_0402_5%
<20,33,48> ALWON
@ PC335 4.7U_0603_6.3V6M
@PR415 0_0402_5%
PC418 0.1U_0402_25V6
PC419 4.7U_0603_6.3V6M
@PJP402 PAD-OPEN 4x4m
+3VALWP
+3VALW
@PJP403 PAD-OPEN 4x4m
+5VALWP
+5VALW
3.3VALWP
TDC 5.5A
Peak Current 7.7A
OCP current 9.35A
5VALWP
TDC 11.3A
Peak Current 12.6A
OCP current 19.2A
3V/5V controller(35.1), Support component(35.2)
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
P59-PWR_3.3VALWP/5VALWP
Size
Document Number
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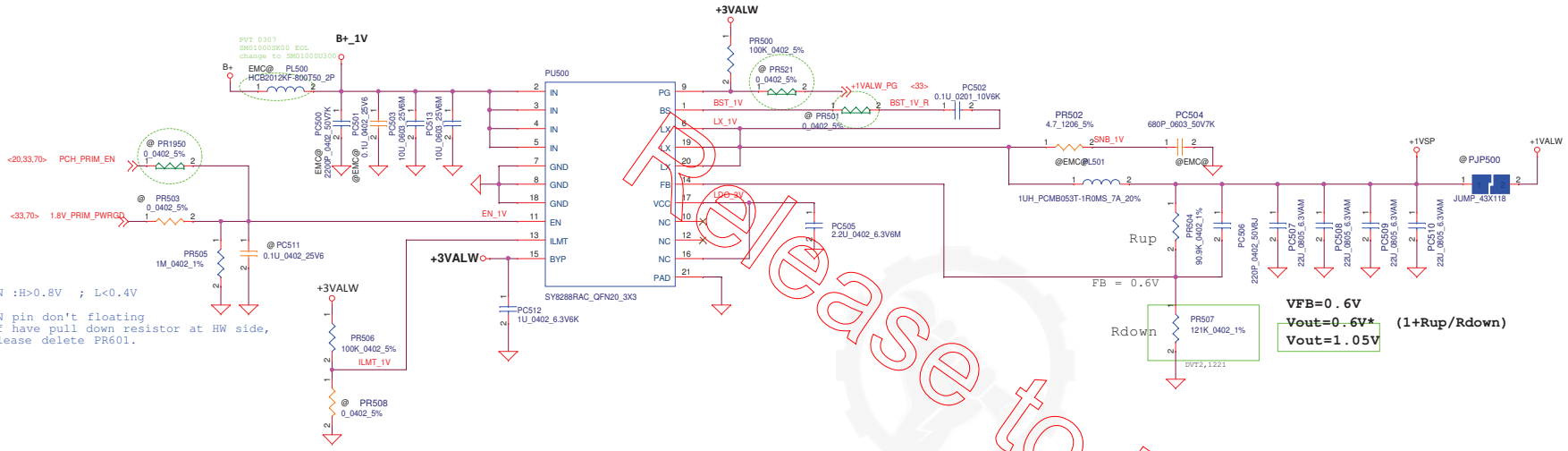
+1VSP
TDC 6A
Peak Current 8.2A
OCP current 12A(fix)



VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.05V

EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side, please delete PR601.

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

PWR.Plane.Regulator(35.25), Support component(35.26)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P60-PWR_PCH_1V(SY8288RAC)

Size	Document Number	Rev
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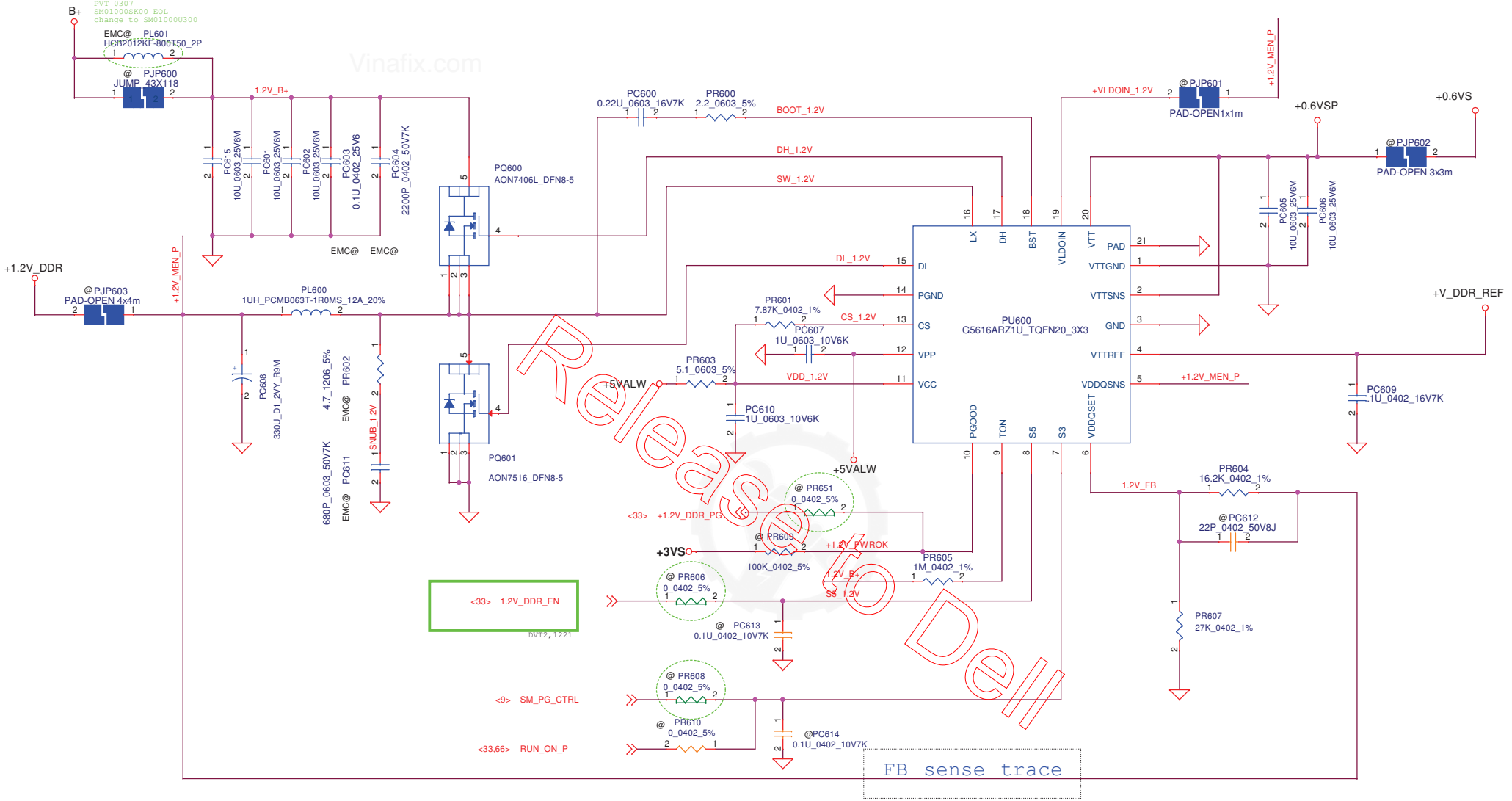

1.2Volt +/- 5%
TDC 8.2A
Peak Current 15.4A
OCP current

0.6Volt +/- 5%
TDC 0.5A
Peak Current 0.7A
OCP Current 0.85A

DDR controller(35.3), Support component(35.4)

Compal Electronics, Inc.

Title: P61-PWR_+1.2V_MEN/+0.6V_DDR

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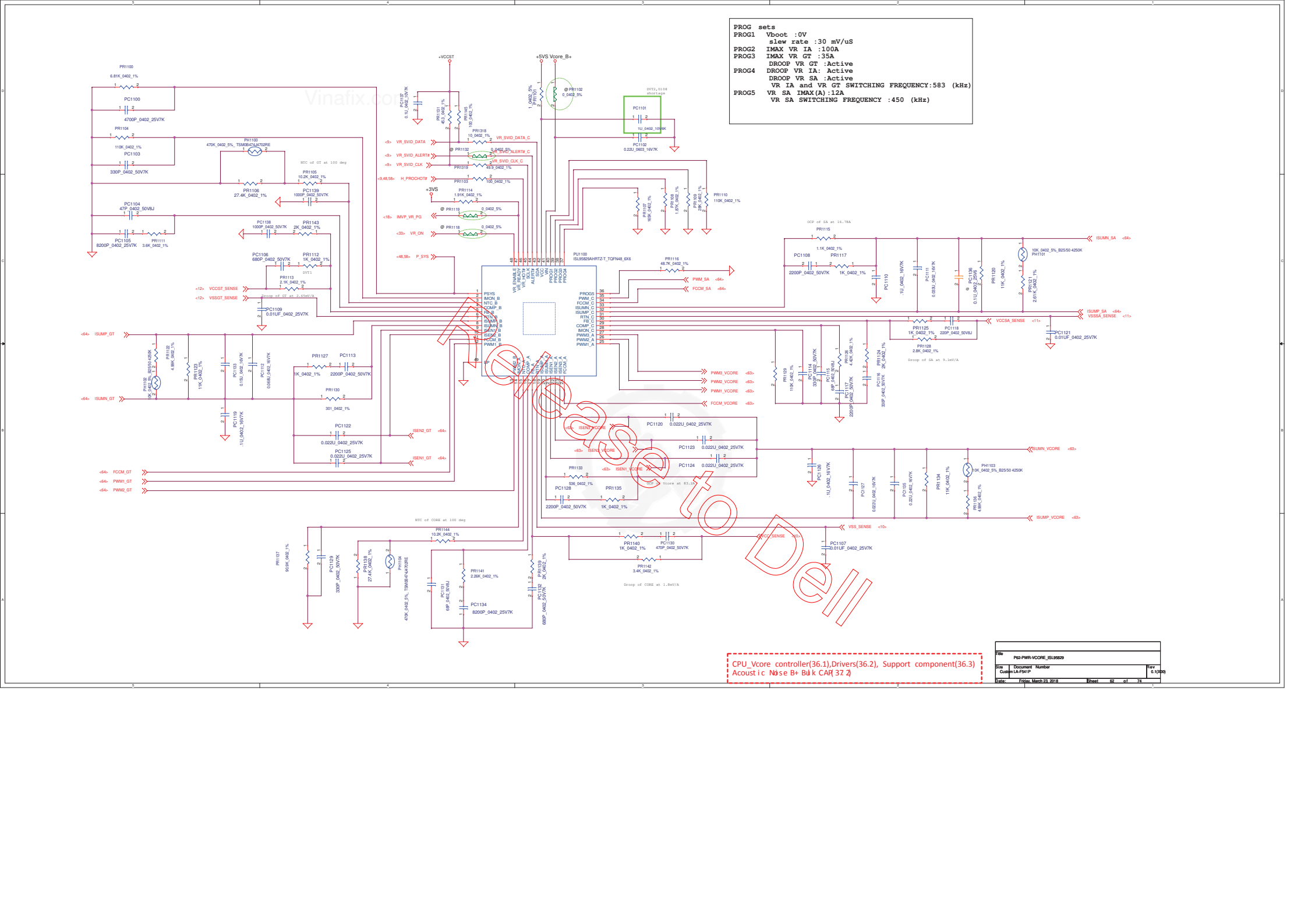
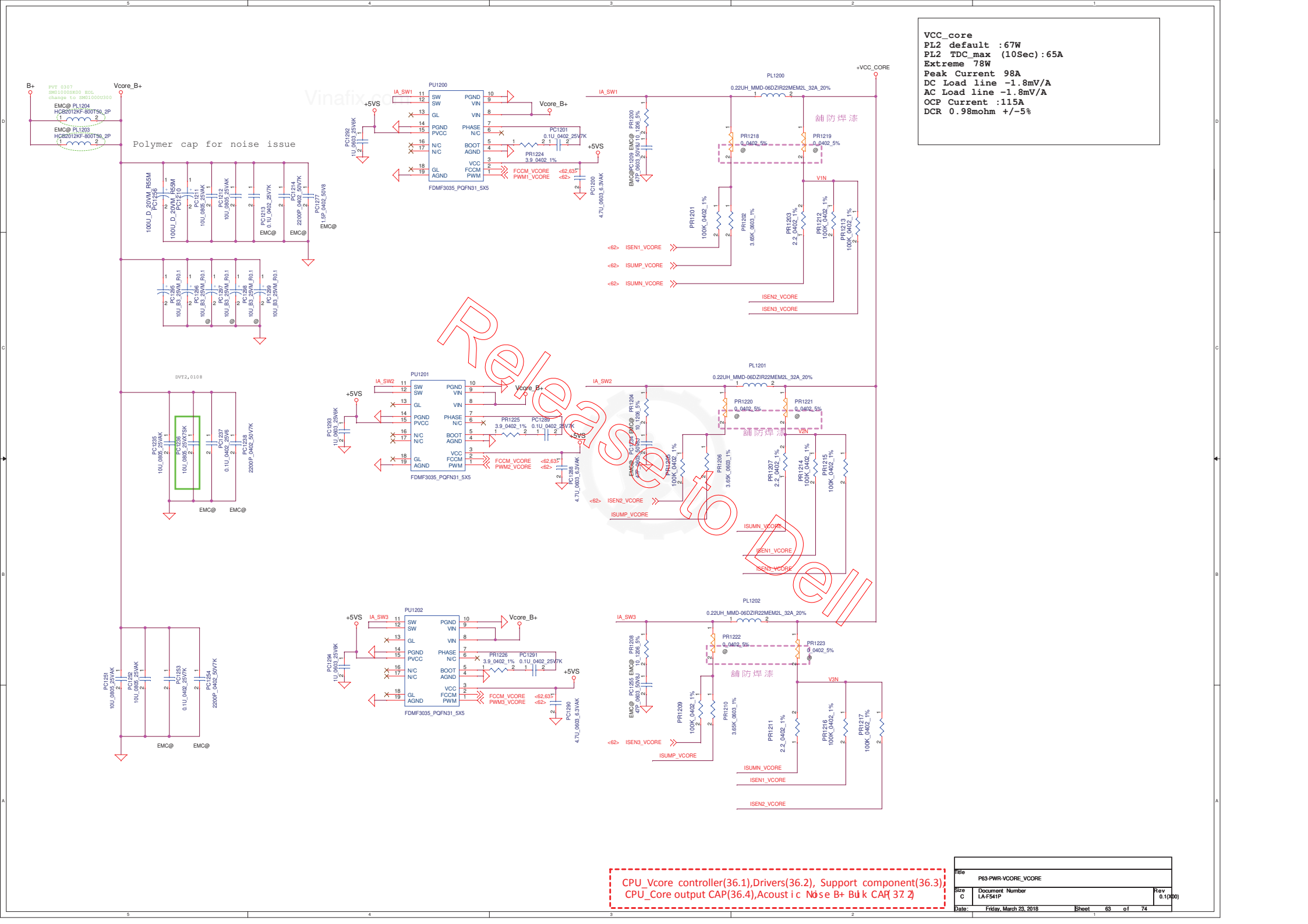
Date: Friday, March 23, 2018 | Sheet 61 of 74


PROG sets
PROG1 Vboot :0V
slew rate :30 mV/uS
PROG2 IMAX VR IA :10DA
PROG3 IMAX VR GT :35A
DROOP VR GT :Active
PROG4 DROOP VR IA: Active
DROOP VR SA :Active
VR IA and VR GT SWITCHING FREQUENCY:583 (kHz)
PROG5 VR SA IMAX(A):12A
VR SA SWITCHING FREQUENCY :450 (kHz)
+VCCST
+5VS Vcore_B+
+3VS
PU1100 ISL95829AHRTZ-T_TQFN48_6X6
NTC of GT at 100 deg
NTC of CORE at 100 deg
OCP of SA at 16.78A
OCP of Vcore at 83.2A
Droop of GT at 2.65mV/A
Droop of SA at 9.1mV/A
Droop of CORE at 1.8mV/A
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)
Title
P62-PWR-VCORE_ISL95829
Size Document Number Rev
Custom LA-F541P 0.1(X00)
Date: Friday, March 23, 2018 Sheet 62 of 74


VCC_core
PL2 default :67W
PL2 TDC_max (10Sec):65A
Extreme 78W
Peak Current 98A
DC Load line -1.8mV/A
AC Load line -1.8mV/A
OCP Current :115A
DCR 0.98mohm +/-5%
Polymer cap for noise issue
PU1200
PU1201
PU1202
FDMF3035_PQFN31_5X5
PL1200
PL1201
PL1202
0.22UH_MMD-06DZIR22MEM2L_32A_20%
+VCC_CORE
Vcore_B+
+5VS
B+
IA_SW1
IA_SW2
IA_SW3
FCCM_VCORE
PWM1_VCORE
PWM2_VCORE
PWM3_VCORE
ISEN1_VCORE
ISEN2_VCORE
ISEN3_VCORE
ISUMP_VCORE
ISUMN_VCORE
V1N
V2N
V3N
舖防焊漆
EMC@
DVT2,0108
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)
Title
P63-PWR-VCORE_VCORE
Size C
Document Number LA-F541P
Rev 0.1(X00)
Date: Friday, March 23, 2018
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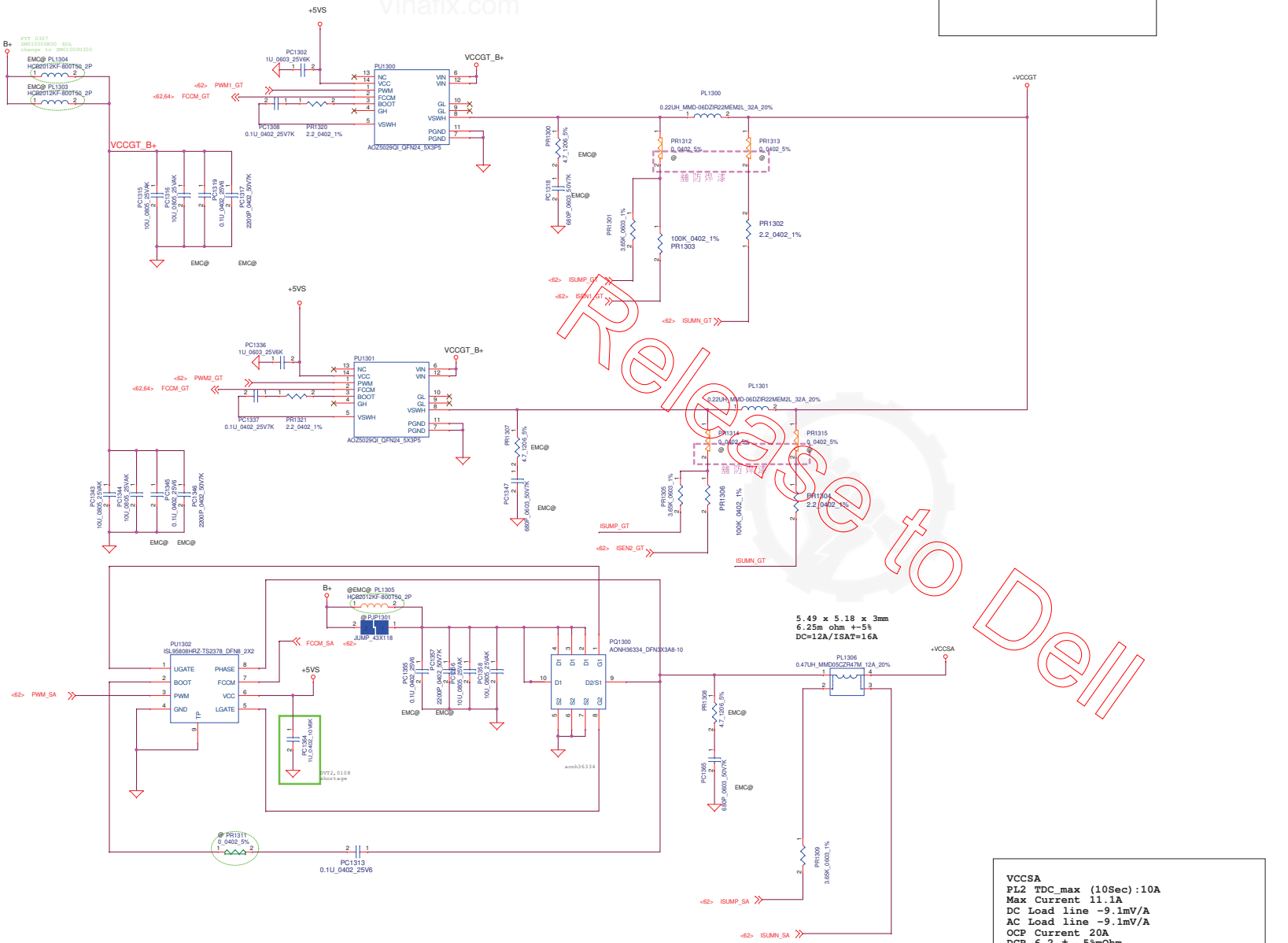
VCCGT
PL2 TDC_max (10Sec):25A
Max Current 32A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 48A
DCR 0.98mohm +/-5%
VCCSA
PL2 TDC_max (10Sec):10A
Max Current 11.1A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 6.2 ± 5%mOhm
5.49 x 5.18 x 3mm
6.25m ohm +-5%
DC=12A/ISAT=16A
Release to Dell
Vinafix.com
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)
P64-PWR_VCORE_VGT,VSA
Custom LA-F541P
Friday, March 23, 2018
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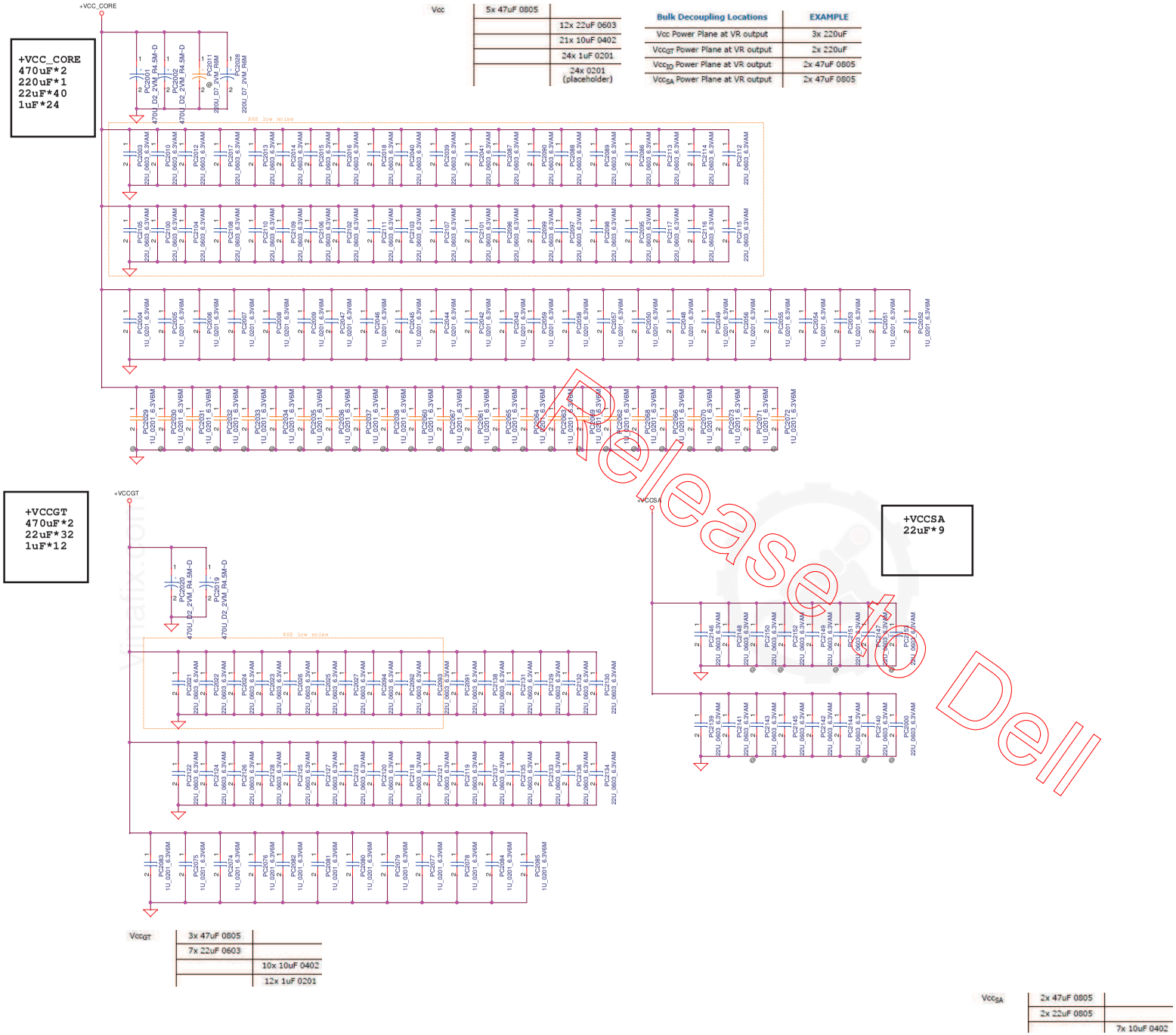

Security Classification	Compal Secret Data	
Issued Date	2017/06/21	Deciphered Date 2027/06/21

Compal Electronics, Inc.

Title: **P65-PWR_PROCESSOR_DECOUPING**

Size	Document Number	Rev
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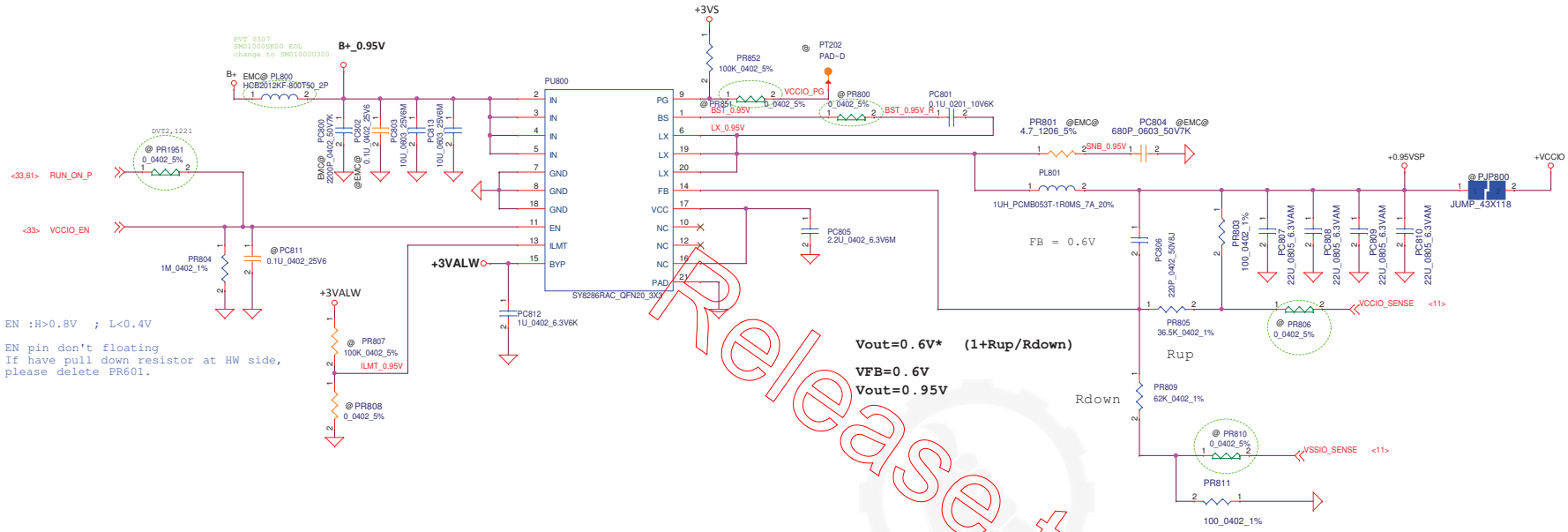
Date: Friday, March 23, 2018 | Sheet 65 of 74

+0.95V
TDC 4.5A
Peak Current 6.5A
OCP current 9A(fix)



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

Vout=0.6V* (1+Rup/Rdown)

VFB=0.6V
Vout=0.95V

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P66-PWR_VCCIO_0.95V(SY8286RAC)

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

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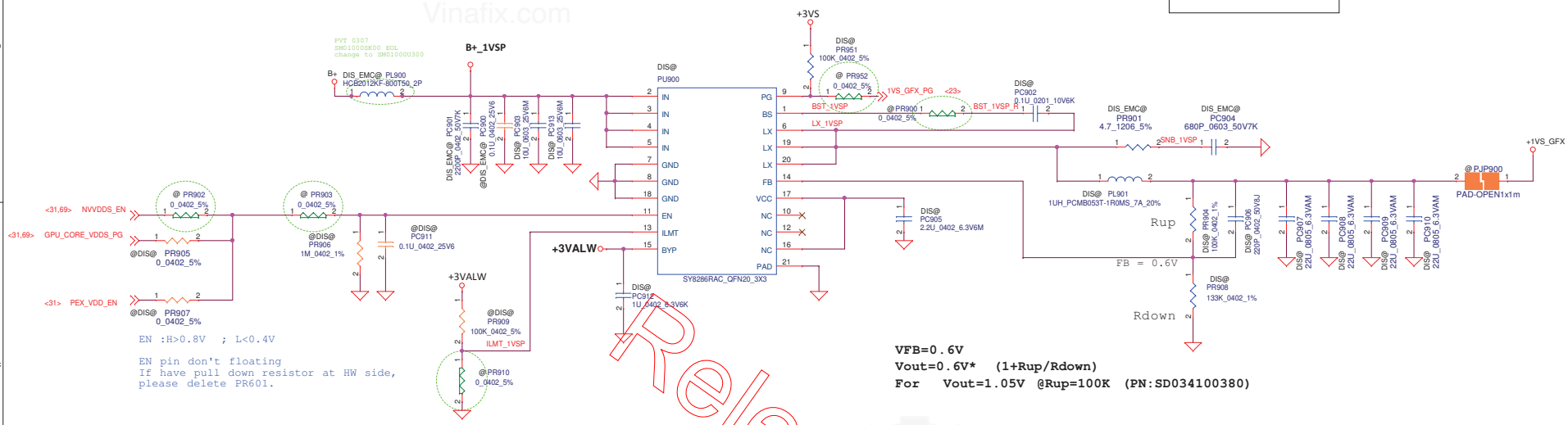
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

+1.0VSP/1.05VSP
TDC 1.1A
Peak Current 1.1A
OCP current 6A(fix)



The current limit is set to 6A, 8A or 12A when this pin
is pull low, floating or pull high

GPU other power_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P67-PWR_+1.05VSDGPU(SY8286RAC)

Size	Document Number	Rev
	LA-F541P	0.1(XXX)

Date: Friday, March 23, 2018 Sheet 67 of 74

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

GPU_CORE (0.95V)
TDC 41A
Peak Current 94A
OCP current 100A
DCR 0.98mohm +/- 5%

	MIN	MAX
H/S Rds(on)	3.7mohm	4.5mohm
L/S Rds(on)	1.5mohm	1.9mohm

Vmax=1.3V
Vmin=0.3V
Vboot=0.8V

Enable 1.2V
Disable 0.55V

Fsw=370KHz

RT8816AGQW_WQFN20_3X3

+GPU_CORE (place under GPU)

+GPU_CORE (place near GPU)

Under:
4.7U_0603_6.3VAK *16
1U_0402_6.3VAK *10

Near:
10U_0805_6.3V6M*7
22U_0805_6.3V6M *7
4.7U_0805_6.3V6K *6
330u*3

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.
Title: P68-PWR-+GPU_CORE
Size: Document Number: LA-F541P
Rev: 0.1(X00)
Date: Friday, March 23, 2018
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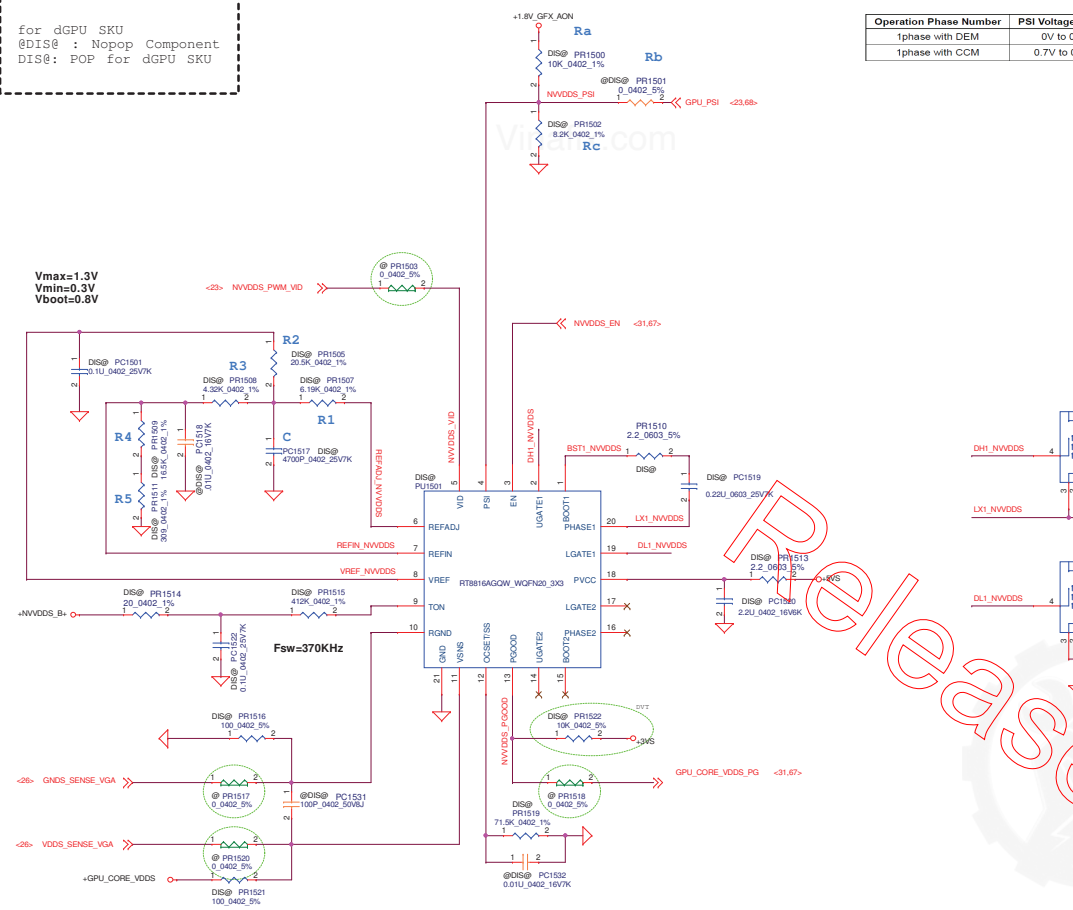
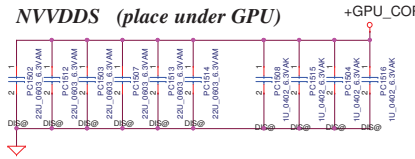
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

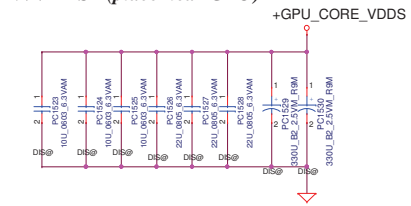
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

+GPU_CORE_VDDS
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%

	MIN	MAX
H/S Rds(on)	3.7mohm	4.5mohm
L/S Rds(on)	1.5mohm	1.9mohm







Under:
4.7U_0603_6.3VAK *6
1U_0402_6.3VAK *4

Near:
10U_0603_6.3V6M *3
22U_0805_6.3V6M *3
330u*2

VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

Compal Electronics, Inc.
Title: P69-PWR-+GPU_CORE_VDDS
Size: Document Number: LA-F541P
Rev: 0.1(X00)
Date: Friday, March 23, 2018
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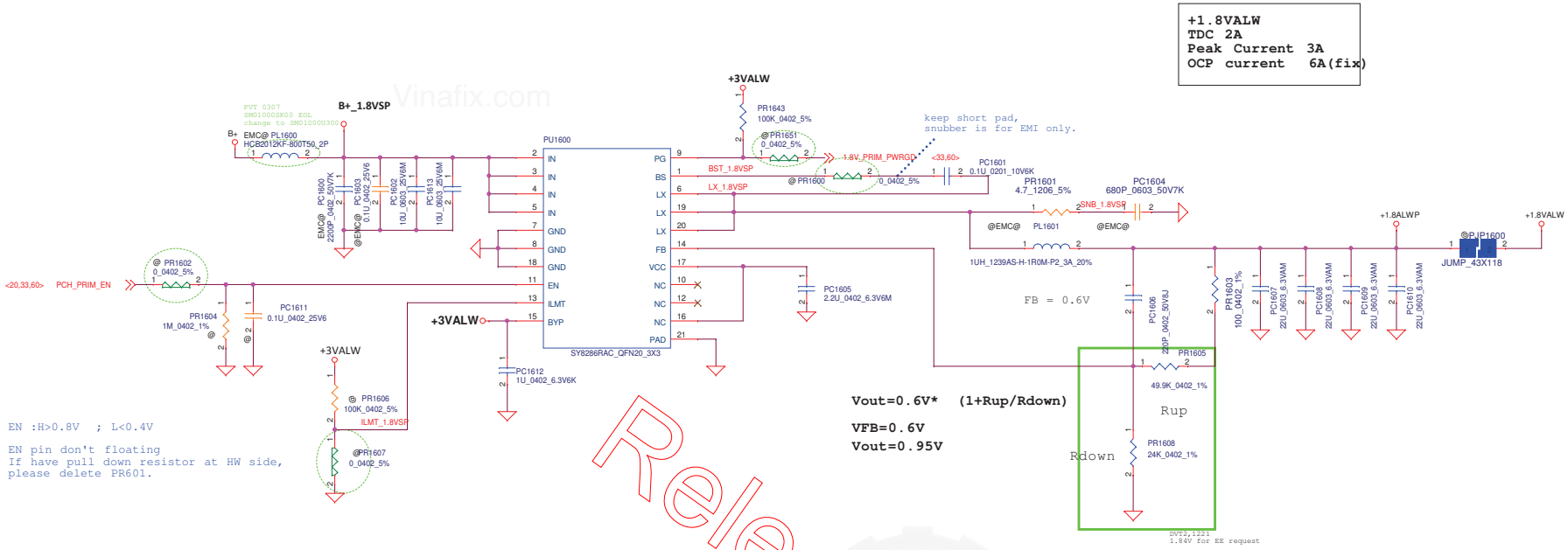


Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

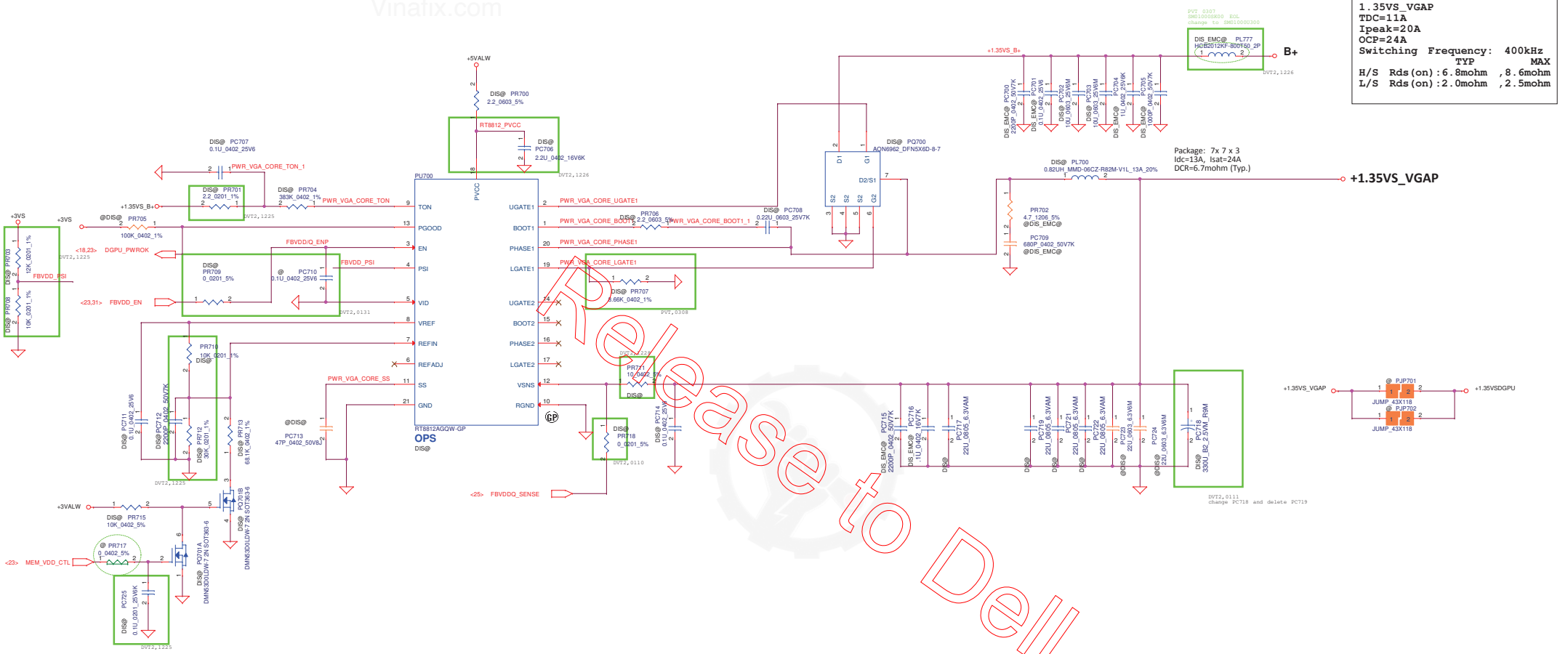
Title: P70-PWR_+1.8ALWP(SY8286RAC)

Size	Document Number	Rev
C		0.1(000)

Date: Friday, March 23, 2018 Sheet 70 of 74

for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU

1.35VS_VGAP
TDC=11A
Ipeak=20A
OCP=24A
Switching Frequency: 400kHz
TYP MAX
H/S Rds(on):6.8mohm ,8.6mohm
L/S Rds(on):2.0mohm ,2.5mohm



MEM_VDD_CTL	VOUT
L	1.35V
H	1.5V/1.55V

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

Compal Electronics, Inc.

Title: PWR +1.35VRAM

Size: | Document Number: LA-E994P | Rev: 0.1(100)

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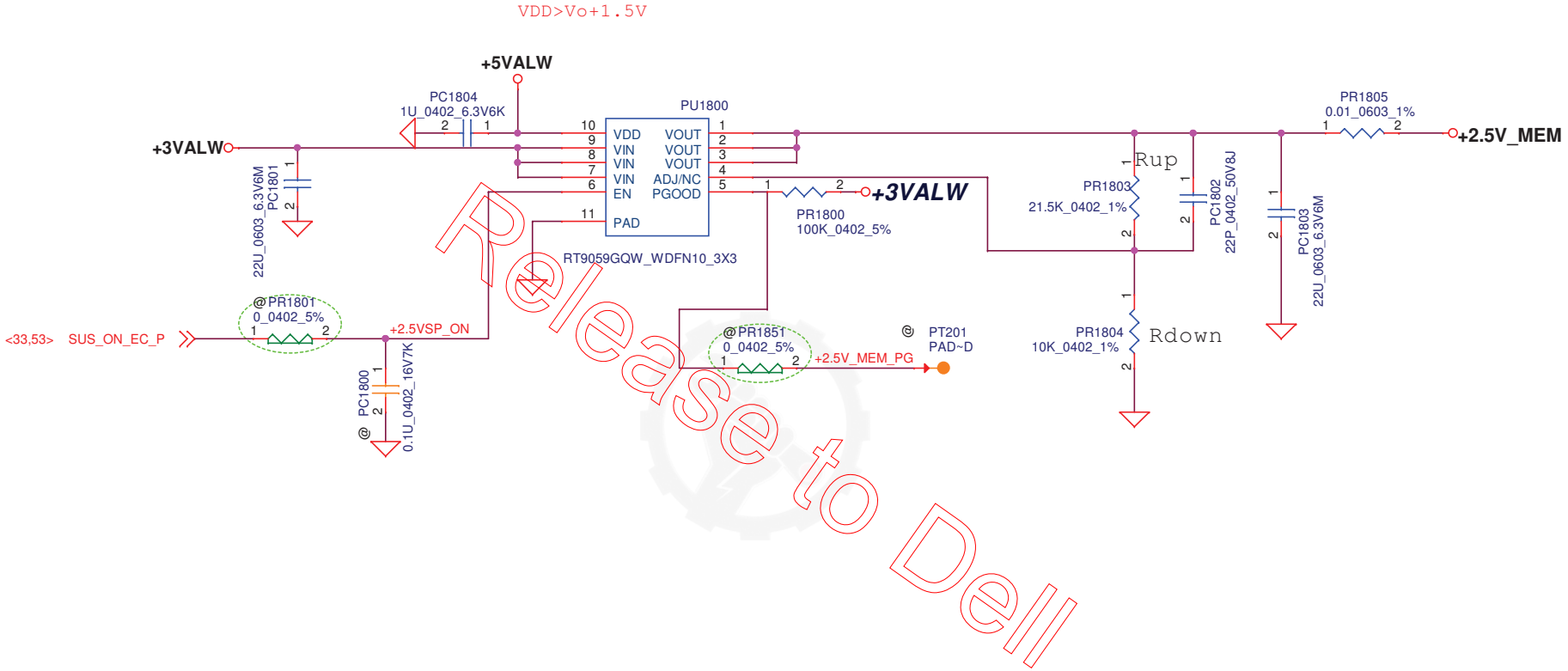
2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.86A
Peak Current 1A
OCP Current 1.46A



Security Classification	Compal Secret Data		
Issued Date	2017/06/21	Deciphered Date	2027/06/21

Compal Electronics, Inc.

Title: P72-PWR +2.5V_MEM(RT9059GSP)

Size	Document Number	Rev
	LA-F541P	0.1(X00)

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Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	NA	2014/12/12	EE	NA	NA	X01
2				EE			X01
3				EE			X01
4				EE			X01
5				EE			X01
6				EE			X01
7				EE			X01
8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
12				EE			X01
13				EE			X01
14				EE			X01
15				EE			X01
16				EE			X01
17				EE			X01
18				EE			X01
19				EE			X01
20				EE			X01
21				EE			X01
22				EE			X01
23				EE			X01
24				EE			X01
25				EE			X01
26				EE			
27				EE			
28				EE			
29				EE			
30				EE			
31				EE			
32				EE			
33				EE			
34				EE			
35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

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Title: P74-EE - NOTE2

Size | Document Number: LA-F541P | Rev: 0.1(X00)

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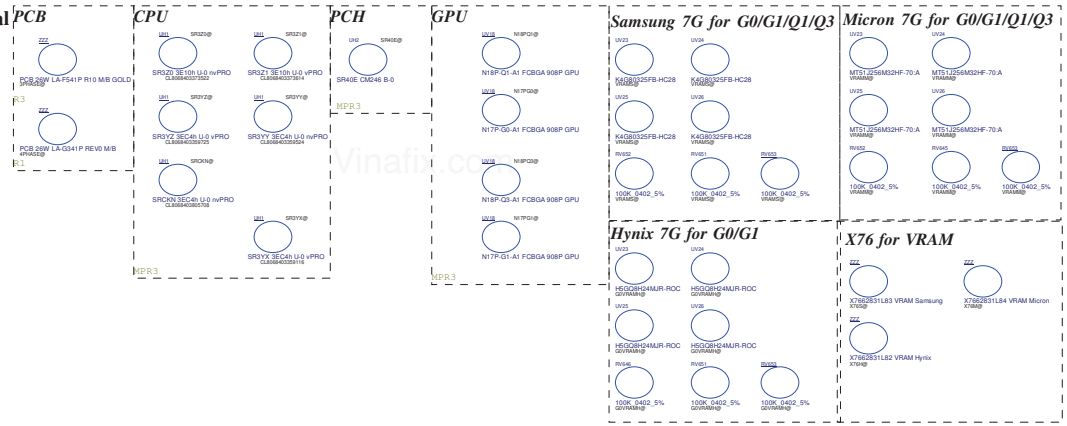
Project Code :
File Name :



RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	

RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	PVT
4.3K	4700p	X00_4P	i9 EVT
2K	4700p	X01_4P	i9 DVT
1K	4700p	A00_4P	i9 PVT

TLS CONFIDENTIALITY

HIGH(4.7k)	vPRO
LOW(DEFAULT)(100K) BIOS 20k internal pull-down	non-vPRO

DRAM Option	DRAM Config Option (MEM_CONFIG0 MEM_CONFIG1 MEM_CONFIG2 MEM_CONFIG3 MEM_CONFIG4)	DRAM SDP / DDP Option	R_COMP	X76
SDP MICRON 8G/2400				X7674531L07
SDP HYNIX 8G/2400				X7674531L09
SDP SAMSUNG 8G/2400				X7674531L08
DDP MICRON 16G/2400				X7674531L10
DDP HYNIX 16G/2400				X7674531L15
DDP SAMSUNG 16G/2400				X7674531L11

Security Classification	Compal Secret Data		
Issued Date	2017/04/07	Deciphered Date	2018/12/31

Compal Electronics, Inc.			
Title: BOM Option			
Size:	Document Number: LA-F211P		Rev: 0.6MM
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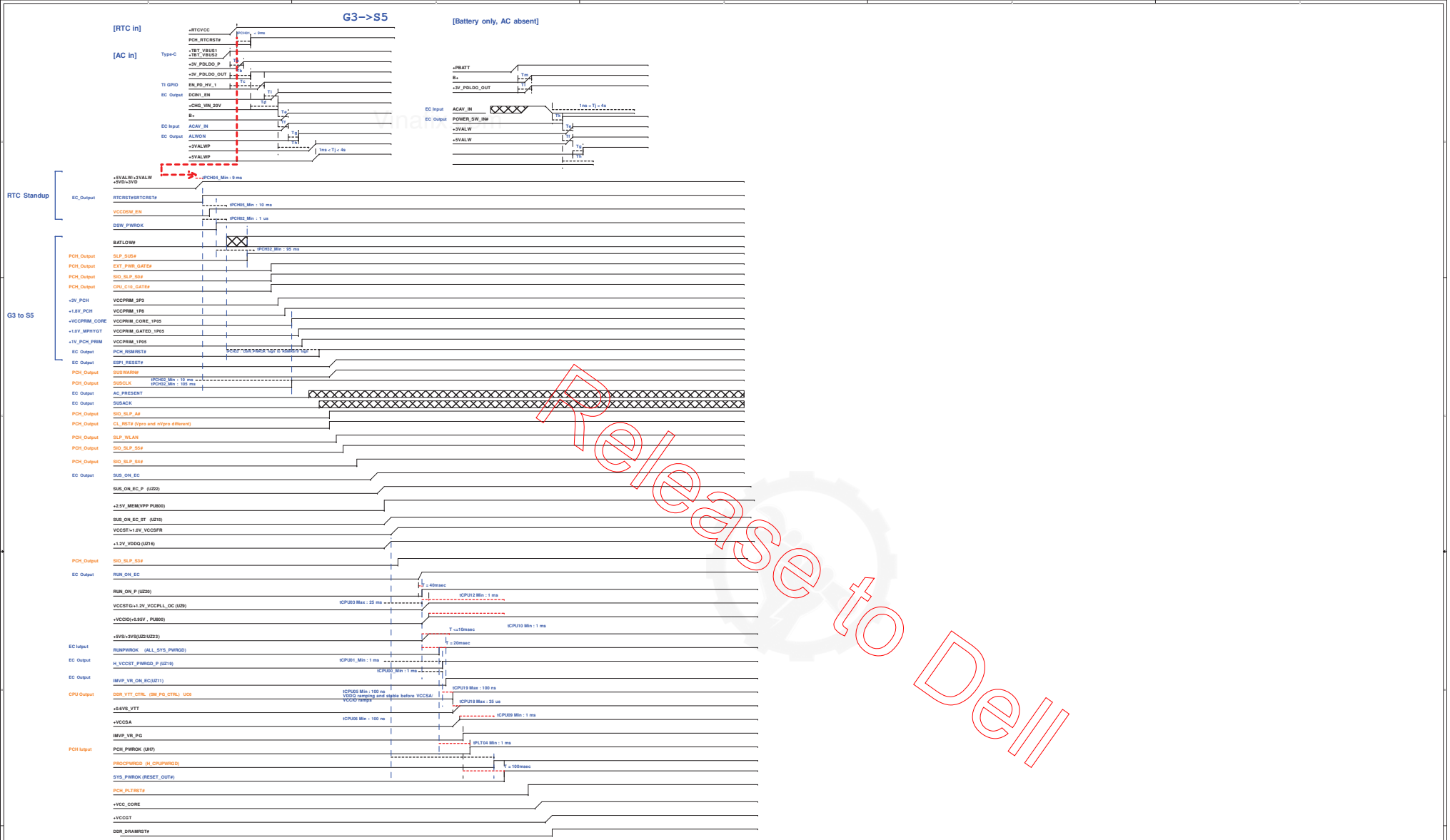

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Issued Date	2017/04/07	Deciphered Date	2018/12/31	Title: Power Up Sequence
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			Date: Friday, March 29, 2019	Sheet 19 of 36