Asus GL552VW Block Diagram

Skylake Platform

Nvidia N16P-GX — Page 70~79
VRAM (128x32/256x32) GDDR5 2GB/4GB

PEG x16

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Quad & Dual Core
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DDIC → HDMI — Page 48

DMI x4

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Keyboard — Page 31

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SATA

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Option
1 : HDD
2 : SATA SSD + HDD
3 : PCIE SSD + HDD
4 : SATA SSD
5 : PCIE SSD
(PCIE/SATA SSD colay)

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CX20752
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Load Switch — Page 88
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ASUSTeK COMPUTER INC. NB1

Title : Block Diagram
Engineer: Mario_Jhu

Size	Project Name	Rev
C	GL552VW	2.0

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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	PCI_PME#			
GPP_A12	GPI	GPO	PCH_GPP_A12			
GPP_A13	SUSWANRN#	Native	ME_SusPwrDnAck		PU 10K	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPO	GPP_A16			
GPP_A17	GPI	GPO	PCH_GPP_A17			
GPP_A18	GPI	GPO	PCH_GPP_A18			
GPP_A19	GPI	GPO	PCH_GPP_A19			
GPP_A20	GPI	GPO	PCH_GPP_A20			
GPP_A21	GPI	GPO	PCH_GPP_A21			
GPP_A22	GPI	GPO	PCH_GPP_A22			
GPP_A23	GPI	GPO	PCH_GPP_A23			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPO	GPO	(N.C)			
GPP_B2	GPI	GPO	(N.C)			
GPP_B3	GPI	GPO	(N.C)			
GPP_B4	GPI	GPO	(N.C)			
GPP_B5	GPI	Native	CLK_PEGA_REQ0#_X1		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLKREQ3_WLAN#_X1		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLKREQ4_GLAN#_X1		PU 10K	+3VSUS
GPP_B10	GPI	Native	CLKREQ5_USB31#_X1		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPO	GSPI0_CS#			
GPP_B16	GPI	GPO	GSPI0_CLK			
GPP_B17	GPI	GPO	GSPI0_MISO			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/NV_GPU_EVENT#		PU 10K(@)	+3VS
GPP_B21	GPI	GPI	PCH_GPPB21/NV_GC6_FB_EN		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	PCH_GPPC2			
GPP_C3	SMLOCLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SMLODATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		+3VSUS
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	PCH_GPPC8			
GPP_C9	GPI	GPO	PCH_GPPC9			
GPP_C10	GPI	GPO	PCH_GPPC10			
GPP_C11	GPI	GPO	PCH_GPPC11			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	Strap	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	AOAC_WLANLED		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	PCH_GPPC17		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 4.7K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 4.7K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK			
GPP_C21	GPI	GPO	PCH_GPPC21/GPO_RST#		PD 10K	
GPP_C22	GPI	GPO	PCH_GPPC22/DGPU_PWR_EN#		PU 10K	+3VS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPO	CIO_PLUG_EVENT			
GPP_D1	GPI	GPO	GPIO_3_FORCE_PWR			
GPP_D2	GPI	GPI	EXT_SMI#		PU 10K	+3VS
GPP_D3	GPI	GPI	EXT_SCI#		PU 10K	+3VS
GPP_D4	GPI	GPO	(N.C)			
GPP_D5	GPI	GPO	(N.C)			
GPP_D6	GPI	GPO	(N.C)			
GPP_D7	GPI	GPO	WLAN_ON#		PD 100K(@)	
GPP_D8	GPI	GPO	(N.C)			
GPP_D9	GPI	Strap	PCB_ID0		PD 10K	
GPP_D10	GPI	Strap	PCB_ID1		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID		PD 10K	
GPP_D12	GPI	Strap	TOUCH_PANEL_ID		PD 10K	
GPP_D13	GPI	GPO	PCH_GPP_D13		PD 10K(@)	+3VSUS
GPP_D14	GPI	GPO	PCH_GPP_D14/WLAN_LED			
GPP_D15	GPI	GPO	PCH_GPP_D15/WLAN_BT_LED			
GPP_D16	GPI	GPO	(N.C)			
GPP_D17	GPI	GPO	(N.C)			
GPP_D18	GPI	GPO	(N.C)			
GPP_D19	GPI	GPO	(N.C)			
GPP_D20	GPI	GPO	(N.C)			
GPP_D21	GPI	GPO	LED_Record			
GPP_D22	GPI	GPO	(N.C)			
GPP_D23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	Native	DIRECT_ESATA_DETECT#		PU 10K	+3VS
GPP_E1	GPI	Native	SATA_ODD_PRSNT#		PU 10K	+3VS
GPP_E2	GPI	Native	M2ATA_MPCIE_DET#		PU 10K	+3VS
GPP_E3	GPI	GPI	USB31_SMI#		PU 10K	+3V
GPP_E4	GPI	Native	SATA0_HDD_DEVSLP		PU 10K(@)	+3VS
GPP_E5	GPI	Native	NGFF1_DEVSLP		PU 10K(@)	+3VS
GPP_E6	GPI	GPO	(N.C)			
GPP_E7	GPI	GPO	(N.C)			
GPP_E8	GPI	Native	SATA_LED#		PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPO	(N.C)			
GPP_F1	GPI	GPO	(N.C)			
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	(N.C)			
GPP_F4	GPI	GPO	(N.C)			
GPP_F5	GPI	GPO	NGFF3_DEVSLP		PU 10K(@)	+3VS
GPP_F6	GPI	GPO	NGFF2_DEVSLP		PU 10K(@)	+3VS
GPP_F7	GPI	GPO	(N.C)			
GPP_F8	GPI	GPO	(N.C)			
GPP_F9	GPI	GPO	(N.C)			
GPP_F10	GPI	GPO	(N.C)			
GPP_F11	GPI	GPO	(N.C)			
GPP_F12	GPI	GPO	(N.C)			
GPP_F13	GPI	GPO	(N.C)			
GPP_F14	GPI	GPO	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1		PD 100K	
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1			
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1		PD 10K	
GPP_F22	GPI	GPO	(N.C)			
GPP_F23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPO	(N.C)			
GPP_G1	GPI	GPO	SATA_ODD_PWRGT		PU 10K	+3VS
GPP_G2	GPI	GPI	SATA_ODD_DA#			
GPP_G3	GPI	GPO	(N.C)			
GPP_G4	GPI	GPO	(N.C)			
GPP_G5	GPI	GPO	(N.C)			
GPP_G6	GPI	GPO	(N.C)			
GPP_G7	GPI	GPO	(N.C)			
GPP_G8	FAN_PWM_0	GPO	(N.C)			
GPP_G9	FAN_PWM_1	GPO	(N.C)			
GPP_G10	FAN_PWM_2	GPO	(N.C)			
GPP_G11	FAN_PWM_3	GPO	(N.C)			
GPP_G12	GPI	GPO	(N.C)			
GPP_G13	GPI	GPO	(N.C)			
GPP_G14	GPI	GPO	(N.C)			
GPP_G15	GPI	GPO	(N.C)			
GPP_G16	GPI	GPO	(N.C)			
GPP_G17	GPI	GPO	(N.C)			
GPP_G18	GPI	GPO	PCH_GPP_G18			
GPP_G19	GPI	GPO	PCH_GPP_G19			
GPP_G20	GPI	GPO	(N.C)			
GPP_G21	GPI	GPO	(N.C)			
GPP_G22	GPI	GPO	(N.C)			
GPP_G23	GPI	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#_X1		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLK_REQ7#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLK_REQ8#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	CLK_REQ10#		PU 10K	+3VSUS
GPP_H5	GPI	Native	CLK_REQ11#		PU 10K	+3VSUS
GPP_H6	GPI	Native	CLK_REQ12#		PU 10K	+3VSUS
GPP_H7	GPI	Native	CLK_REQ13#		PU 10K	+3VSUS
GPP_H8	GPI	Native	CLK_REQ14#		PU 10K	+3VSUS
GPP_H9	GPI	Native	CLK_REQ15#		PU 10K	+3VSUS
GPP_H10	GPI	GPO	(N.C)			
GPP_H11	GPI	GPO	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPO	(N.C)			
GPP_H14	GPI	GPO	(N.C)			
GPP_H15	GPI	GPO	(N.C)			
GPP_H16	GPI	GPO	(N.C)			
GPP_H17	GPI	GPO	(N.C)			
GPP_H18	GPI	GPO	(N.C)			
GPP_H19	GPI	GPO	(N.C)			
GPP_H20	GPI	GPO	(N.C)			
GPP_H21	GPI	GPO	(N.C)			
GPP_H22	GPI	GPO	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	GPO	DDI1_DP_HPD0			
GPP_I1	GPI	Native	DDI2_HDMI_HPD1		PD 10K	
GPP_I2	GPI	GPO	DDI3_TBT_HPD2			
GPP_I3	GPI	GPO	DDIE_VGA_HPD3			
GPP_I4	GPI	Native	EDP_HPD		PD 100K	
GPP_I5	GPI	GPO	DDPB_SCL_PCH		PU 2.2K	+3VS
GPP_I6	GPO	GPO	DDPB_SDA_PCH	PD	PU 2.2K	+3VS
GPP_I7	GPI	Native	DDPC_SCL_PCH		PU 2.2K	+3VS
GPP_I8	GPO	Native	DDPC_SDA_PCH	PD	PU 2.2K	+3VS
GPP_I9	GPI	GPO	DDPD_SCL_PCH		PU 2.2K(@)	+3VS
GPP_I10	GPO	GPO	DDPD_SDA_PCH	PD	PU 2.2K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	PCH_GPD2#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	GPO	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	GPO	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	GPO	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	GPO	SLP_S5#			
GPD11	LANPHYPC	Native	LAN_PWREN		PU 10K	+3VA_DSW

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON		
GPB5	O	GPO	A20GATE	PU 10K (@)	+3VS
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTB#	PU 10K	+3V
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	+3VA_EC
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT		
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	EC_GPD7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	LAN_WAKE#	PU 10K (@)	+3VA_EC
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH	PD 10K (@)	
GPG4	GPI		EC_SI/EC_SI_PCH	PD 10K (@)	
GPG5	GPI		EC_SO/EC_SO_PCH	PD 10K (@)	
GPG6	O	GPO	USB30_5VBOS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K&PD 93.1K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+5V
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	FL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	EC_GPJ6/ID#	PU 10K	+3V
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

Device Identification

CPU Thermal Sensor		
1st	06G023123010	NCT7717U
2nd		

Memory Thermal Sensor		
1st	06G023040020	
2nd		

Design IP Source:

GL552VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
SO-DIMM A(0)	A0h	
SO-DIMM B(0)	A4h	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
VGA Thermal Sensor	96h	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	
CC logic IC	3Ah	

Device Identification

CPU Thermal Sensor		
1st	06G023123010	NCT7717U
2nd		

GL552VW PCIE & USB Function define
Skylake HM170

HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01	USB3.0 IO colay USB3.1	
03	USB3#03 / SSIC#02	USB3.0 IO colay USB3.1	
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06		
07	USB3#07 / PCIE#01		
08	USB3#08 / PCIE#02		
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN & CardReader	SRC4
11	PCIE#05 / GBE	USB 3.1	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	1st HDD	
20	PCIE#14 / SATA#1	ODD	
21	PCIE#15 / SATA#2	SATA SSD	
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

USB 2.0	Function
USB2_01	USB3.0 IO
USB2_02	USB3.0 IO colay USB3.1
USB2_03	
USB2_04	Camera
USB2_05	USB3.0 IO
USB2_06	USB2.0 IO
USB2_07	
USB2_08	
USB2_09	BT/WLAN
USB2_10	
USB2_11	
USB2_12	

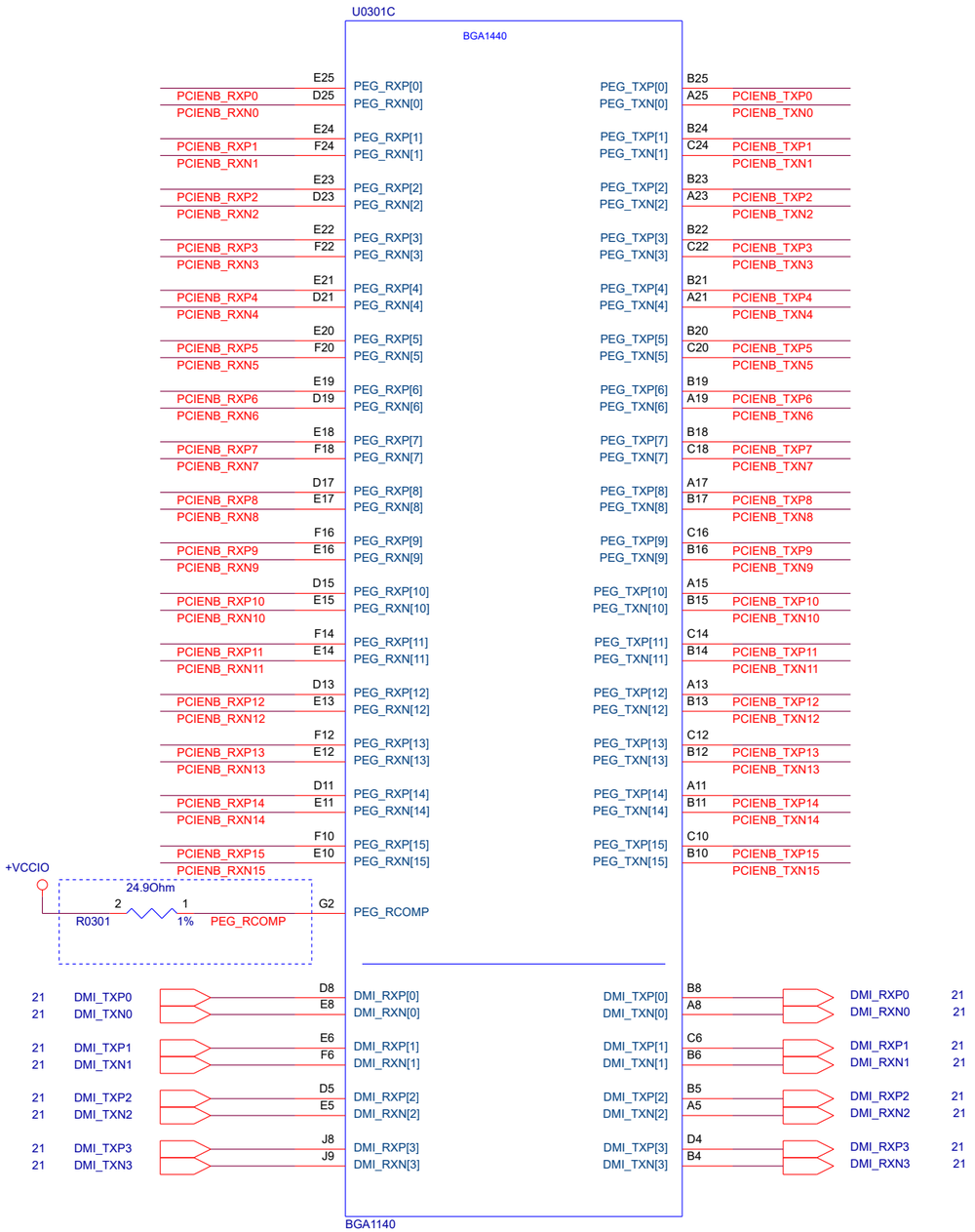
COMPRESSED IMAGE

COMPRESSED IMAGE

SKL PCH-H HM170 HSIO					
1	USB3 #1 (OTG)				
2	USB3 #2	SSIC #1			
3	USB3 #3	SSIC #2			
4	USB3 #4				
5	USB3 #5				
6	USB3 #6				
7	USB3 #7	PCIE #1	x 2	x 4	NA
8	USB3 #8	PCIE #2			
9	PCIE #3		x 2		
10	PCIE #4	GbE			
11	PCIE #5	GbE	x 2	x 4	NA
12	PCIE #6				
13	PCIE #7		x 2		
14	PCIE #8				
15	PCIE #9	SATA #0 GbE	x 2	x 4	Intel IRST PCIE Storage Device #1
16	PCIE #10	SATA #1			
17	PCIE #11		x 2		
18	PCIE #12	GbE			
19	PCIE #13	SATA #0* GbE	x 2	x 4	Intel IRST PCIE Storage Device #2
20	PCIE #14	SATA #1*			
21	PCIE #15	SATA #2	x 2		
22	PCIE #16	SATA #3			
23			NA	NA	NA
24					
25			NA		
26					

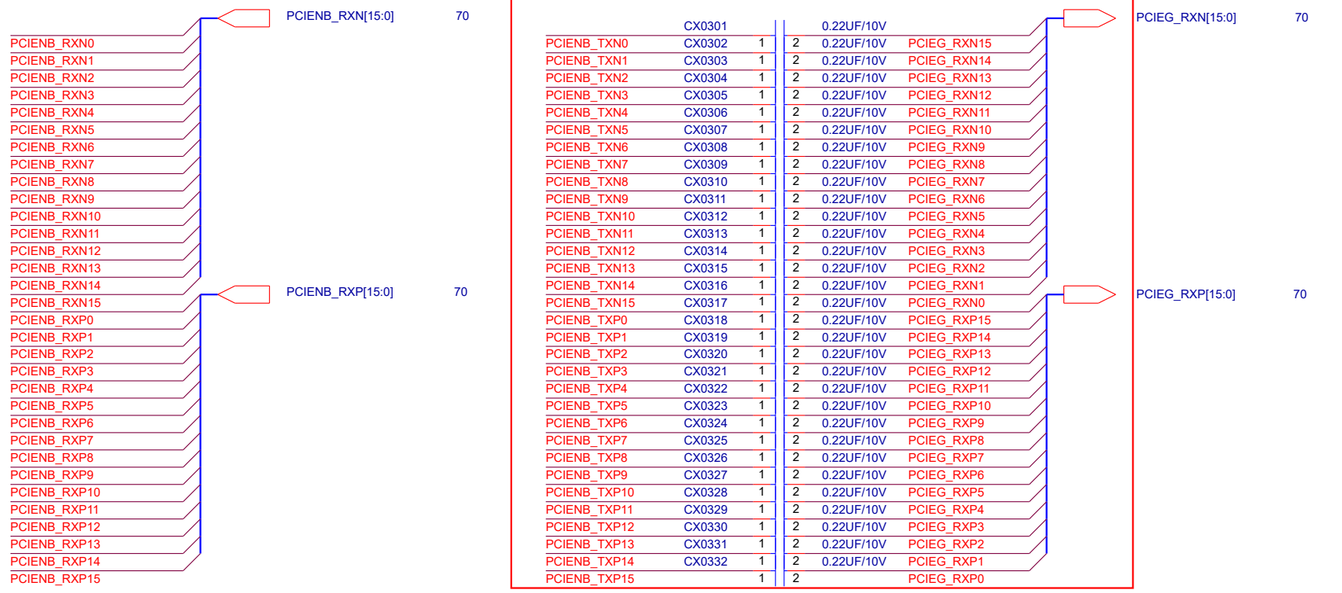
ASUS	Project Name: GL552VW		Rev: 2.0
Title : System Setting			
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet: 2 of 103		

PCIEG

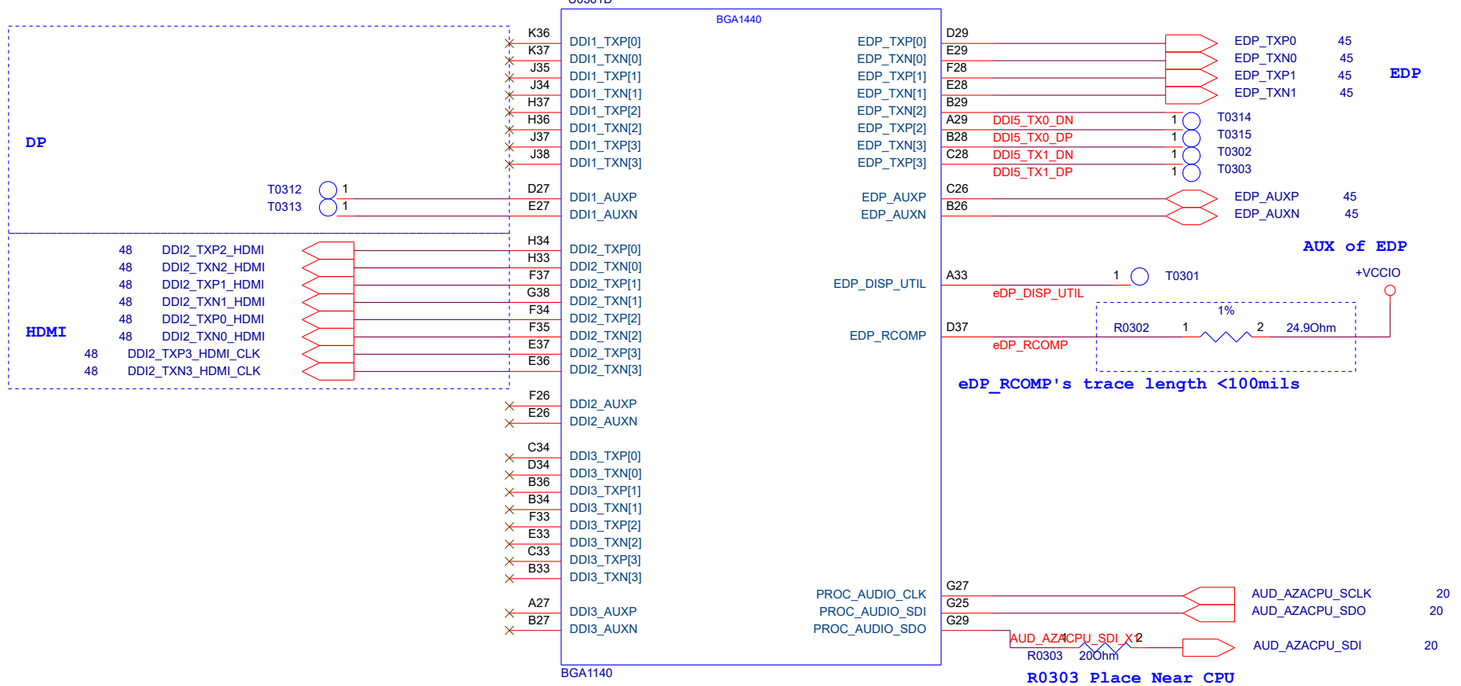


R0301 close to CPU
PEG_COMP trace length <400mils

Main Board



Display



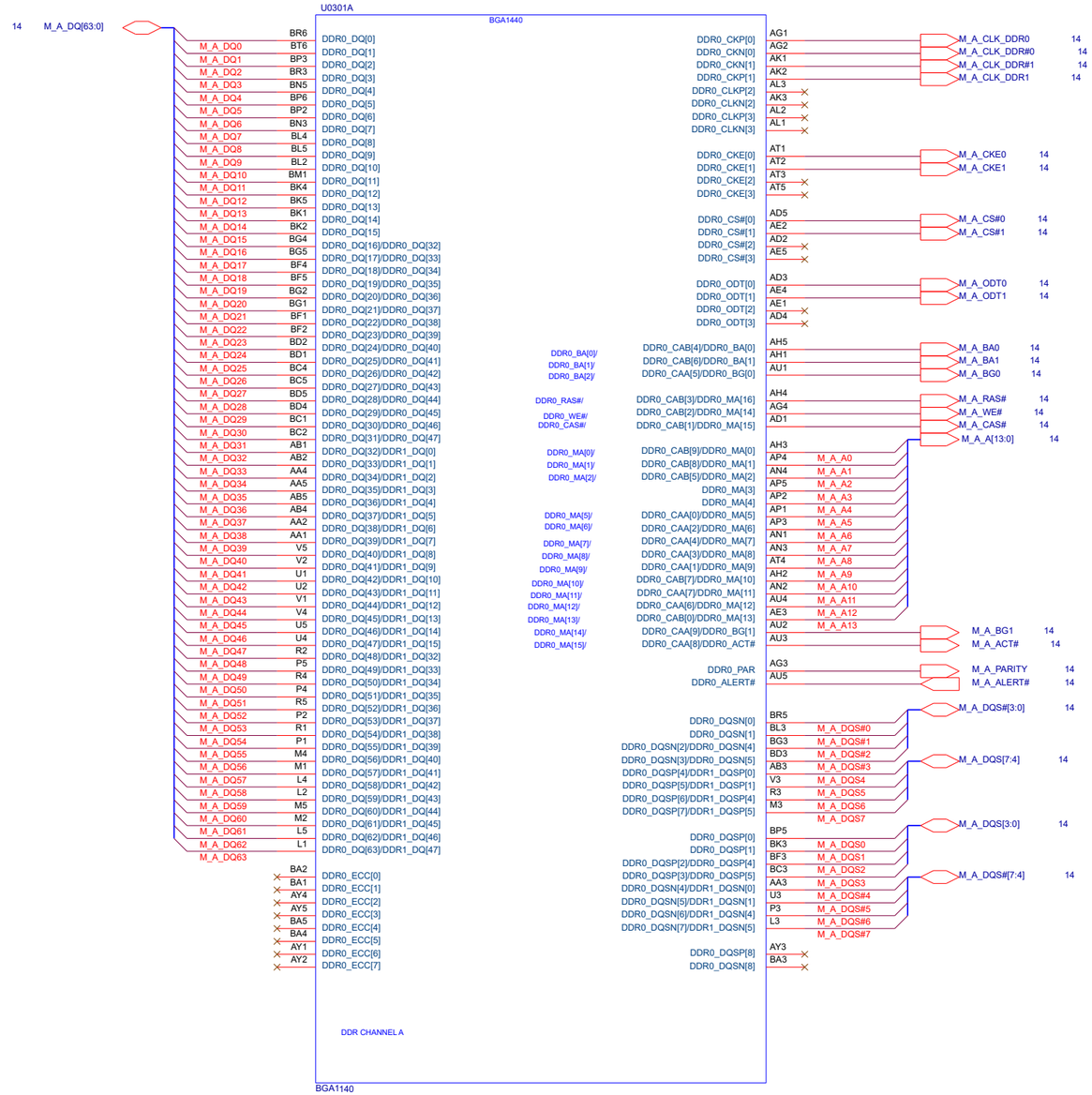
eDP_RCOMP's trace length <100mils

R0303 Place Near CPU

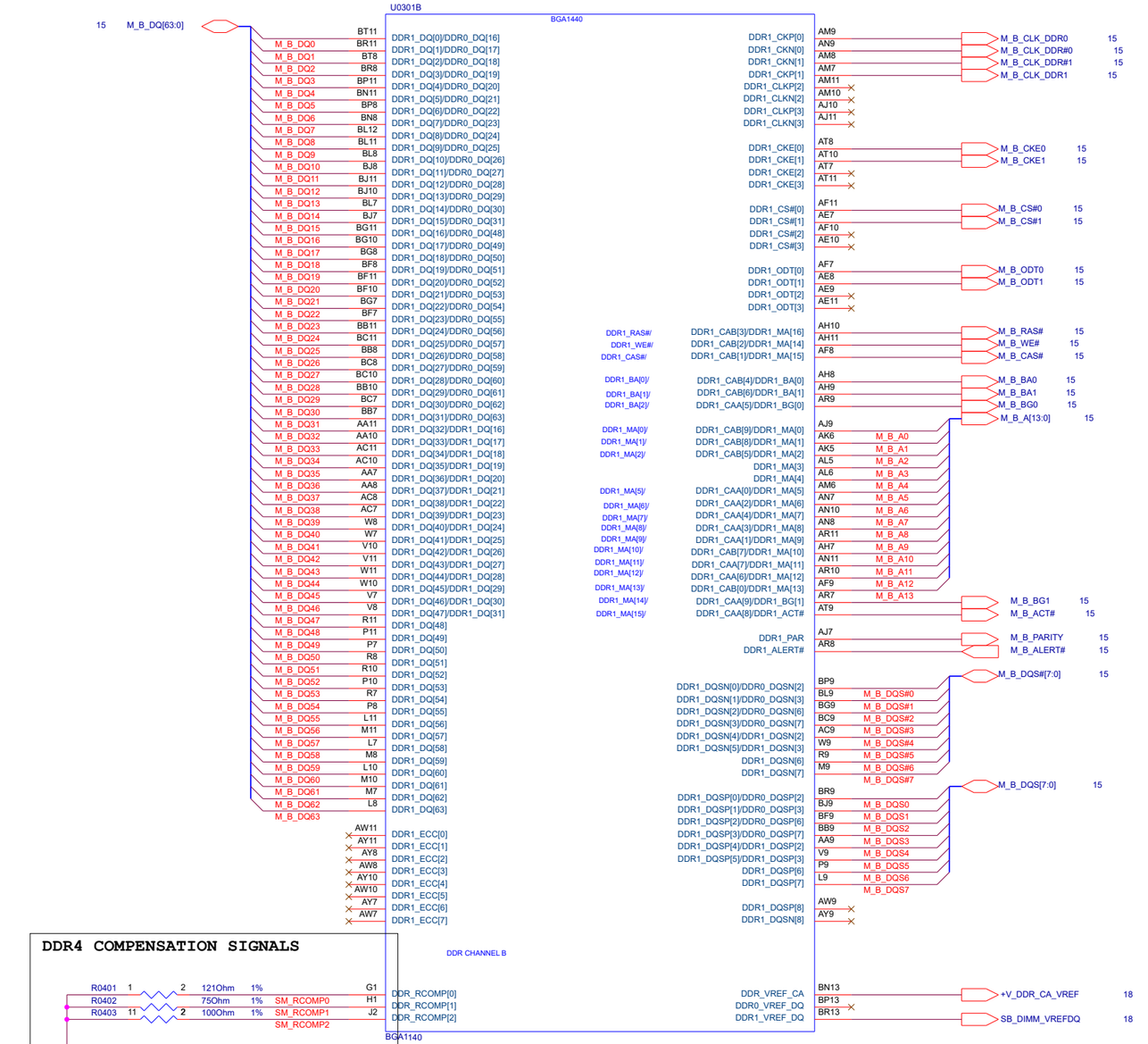
Intel CPU	ASUS P/N	規格
Quad Core (QS)	01001-01150500	I7-6700HQ 2.8G/8M QJJR 45W BGA
Dual Core (QS)	01001-01150400	I5-6300HQ 2.3G/6M QJJQ 45W BGA

Project Name: GL552VW		Rev: 2.0
Title : CPU_DMI,PEG,FDI,eDP,DDI		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 3 of 103	

Memory Channel A



Memory Channel B



DDR4 COMPENSATION SIGNALS

Main Board

Project Name: GL552VW		Rev: 2.0
Title : CPU_DDR4		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 4 of 103	

Main Board

U0301F

BGA1440

Y38	VSS445	VSS370	K1
Y37	VSS444	VSS367	J36
Y14	VSS443	VSS366	J33
Y13	VSS442	VSS365	J32
Y11	VSS441	VSS364	J25
Y10	VSS440	VSS363	J22
Y9	VSS448	VSS362	J18
Y8	VSS447	VSS361	J10
Y7	VSS446	VSS369	J7
W34	VSS437	VSS368	J4
W33	VSS436	VSS360	H35
W12	VSS433	VSS359	H32
W5	VSS439	VSS358	H25
W4	VSS438	VSS357	H22
W3	VSS435	VSS356	H18
W2	VSS434	VSS355	H12
W1	VSS432	VSS354	H11
V30	VSS430	VSS348	G28
V29	VSS429	VSS347	G26
V12	VSS428	VSS346	G24
V6	VSS431	VSS345	G23
U38	VSS426	VSS344	G22
U37	VSS425	VSS343	G20
U6	VSS427	VSS342	G18
T34	VSS419	VSS341	G16
T33	VSS418	VSS340	G14
T14	VSS415	VSS339	G12
T13	VSS414	VSS338	G10
T12	VSS413	VSS353	G9
T11	VSS412	VSS352	G8
T10	VSS411	VSS351	G6
T9	VSS424	VSS350	G5
T8	VSS423	VSS349	G4
T7	VSS422	VSS333	F36
T5	VSS421	VSS332	F31
T4	VSS420	VSS330	F29
T3	VSS417	VSS329	F27
T2	VSS416	VSS328	F25
T1	VSS410	VSS327	F23
R30	VSS409	VSS326	F21
R29	VSS408	VSS324	F19
R12	VSS407	VSS323	F17
P38	VSS405	VSS322	F15
P37	VSS404	VSS321	F13
P12	VSS403	VSS320	F11
P6	VSS406	VSS337	F9
N34	VSS396	VSS336	F8
N33	VSS395	VSS335	F5
N12	VSS392	VSS334	F4
N11	VSS391	VSS331	F3
N10	VSS390	VSS325	F2
N9	VSS402	VSS317	E38
N8	VSS401	VSS316	E35
N7	VSS400	VSS315	E34
N6	VSS399	VSS319	E9
N5	VSS398	VSS318	E4
N4	VSS397	VSS312	D33
N3	VSS394	VSS311	D30
N2	VSS393	VSS309	D28
N1	VSS389	VSS308	D26
M14	VSS387	VSS307	D24
M13	VSS386	VSS306	D22
M12	VSS385	VSS305	D20
M6	VSS388	VSS304	D18
L34	VSS384	VSS303	D16
L33	VSS383	VSS302	D14
L30	VSS382	VSS301	D12
L29	VSS381	VSS300	D10
K38	VSS375	VSS314	D9
K11	VSS372	VSS313	D6
K10	VSS371	VSS310	D3
K9	VSS380	VSS296	C37
K8	VSS379	VSS295	C31
K7	VSS378	VSS294	C29
K5	VSS377	VSS293	C27
K4	VSS376		
K3	VSS374	NCTFVSS12	D38
K2	VSS373		

BGA1140

GND GND

U0301L

BGA1440

C17	VSS288	VSS292	C25
C13	VSS286	VSS291	C23
C9	VSS299	VSS290	C21
BT32	VSS282	VSS289	C19
BT26	VSS281	VSS287	C15
BT24	VSS280	VSS285	C11
BT21	VSS279	VSS298	C8
BT18	VSS278	VSS297	C5
BT14	VSS277	VSS232	BM29
BT12	VSS276	VSS228	BM25
BT9	VSS284	VSS224	BM18
BT5	VSS283	VSS221	BM11
BR36	VSS274	VSS239	BM8
BR34	VSS273	VSS238	BM7
BR29	VSS272	VSS236	BM5
BR26	VSS271	VSS233	BM3
BR24	VSS270	VSS219	BL38
BR21	VSS269	VSS218	BL35
BR18	VSS268	VSS216	BL13
BR14	VSS267	VSS220	BL6
BR12	VSS266	VSS213	BK25
BR7	VSS275	VSS212	BK22
BP34	VSS264	VSS208	BK13
BP33	VSS263	VSS215	BK6
BP29	VSS262	VSS205	BJ30
BP26	VSS261	VSS204	BJ29
BP24	VSS260	VSS200	BJ15
BP21	VSS259	VSS199	BJ12
BP18	VSS258	VSS188	BH11
BP14	VSS257	VSS187	BH10
BP12	VSS256	VSS196	BH7
BP7	VSS265	VSS195	BH6
BN34	VSS252	VSS192	BH3
BN31	VSS251	VSS191	BH2
BN30	VSS250	VSS183	BG37
BN29	VSS249	VSS182	BG14
BN24	VSS248	VSS185	BG6
BN21	VSS247	VSS178	BF34
BN20	VSS246	VSS179	BF6
BN19	VSS244	VSS172	BE30
BN18	VSS243	VSS174	BE5
BN14	VSS242	VSS173	BE4
BN12	VSS241	VSS171	BE3
BN9	VSS255	VSS169	BE2
BN7	VSS254	VSS168	BE1
BN4	VSS253	VSS163	BD38
BN2	VSS245	VSS162	BD37
BM38	VSS235	VSS161	BD12
BM35	VSS234	VSS160	BD11
BM28	VSS231	VSS159	BD10
BM27	VSS230	VSS166	BD8
BM26	VSS229	VSS165	BD7
BM23	VSS227	VSS164	BD6
BM21	VSS226	VSS156	BC33
BM13	VSS223	VSS155	BC14
BM12	VSS222	VSS154	BC13
BM9	VSS240	VSS158	BC6
BM6	VSS237	VSS149	BB30
BM2	VSS225	VSS147	BB29
BL29	VSS217	VSS152	BB6
BK29	VSS214	VSS151	BB5
BK15	VSS210		
BK14	VSS209		
BJ32	VSS207		
BJ31	VSS206		
BJ25	VSS203		
BJ22	VSS202		
BH14	VSS190		
BH12	VSS189	NCTFVSS11	C2
BH9	VSS198	NCTFVSS9	BT36
BH8	VSS197	NCTFVSS8	BT35
BH5	VSS194	NCTFVSS10	BT4
BH4	VSS193	NCTFVSS7	BT3
BH1	VSS186	NCTFVSS6	BR38
BG38	VSS184		
BG13	VSS181		
BG12	VSS180		
BF33	VSS177		
BF12	VSS176		
BE29	VSS170		
BE6	VSS175		
BD9	VSS167		
BC34	VSS157		
BC12	VSS153		
BB12	VSS145		

BGA1140

GND GND

U0301M

BGA1440

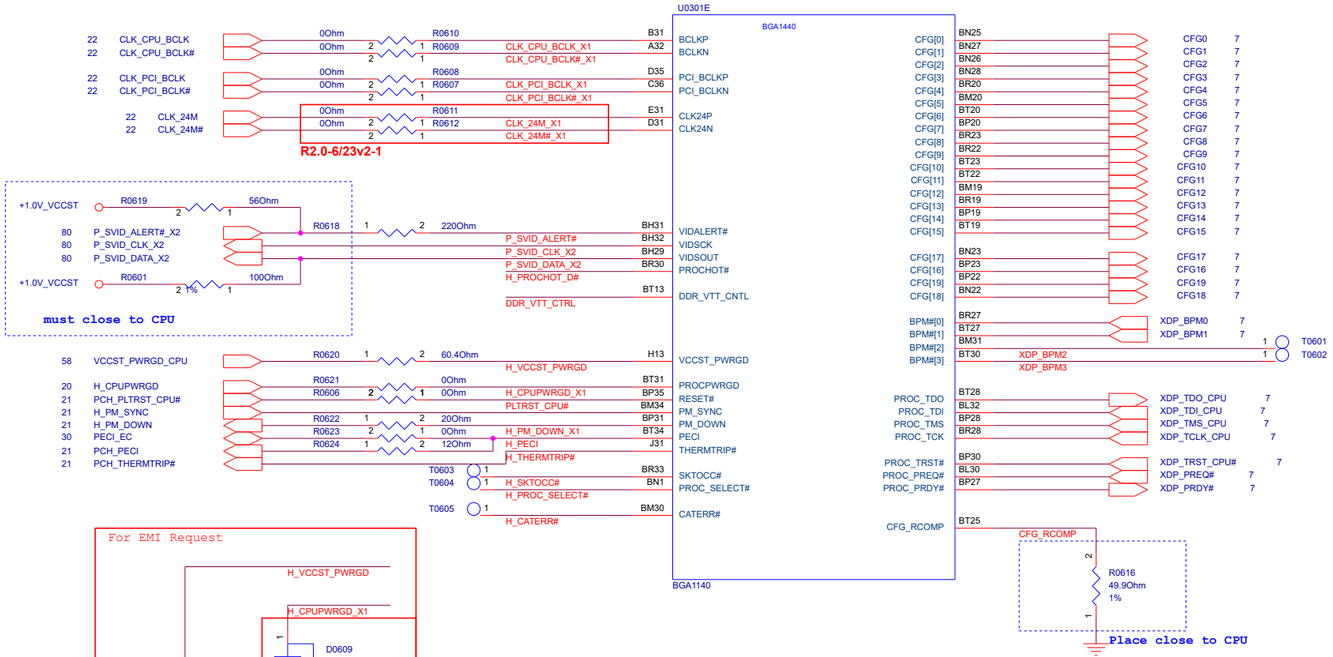
BB4	VSS150	VSS68	AK30
BB3	VSS148	VSS67	AK29
BB2	VSS146	VSS69	AK4
BB1	VSS144	VSS63	AJ38
BA38	VSS139	VSS62	AJ37
BA37	VSS138	VSS66	AJ6
BA12	VSS137	VSS65	AJ5
BA11	VSS136	VSS64	AJ4
BA10	VSS135	VSS61	AJ3
BA9	VSS143	VSS60	AJ2
BA8	VSS142	VSS59	AJ1
BA7	VSS141	VSS57	AH34
BA6	VSS140	VSS56	AH33
B9	VSS134	VSS55	AH12
AY34	VSS133	VSS58	AH6
AY33	VSS132	VSS51	AG30
AY14	VSS131	VSS50	AG29
AY12	VSS130	VSS49	AG11
AW30	VSS127	VSS48	AG10
AW29	VSS125	VSS54	AG8
AW12	VSS123	VSS53	AG7
AW5	VSS129	VSS52	AG6
AW4	VSS128	VSS44	AF14
AW3	VSS126	VSS43	AF13
AW2	VSS124	VSS42	AF12
AW1	VSS122	VSS47	AF4
AV38	VSS121	VSS46	AF3
AV37	VSS120	VSS45	AF2
AU34	VSS115	VSS41	AF1
AU33	VSS114	VSS39	AE34
AU12	VSS113	VSS38	AE33
AU11	VSS112	VSS40	AE6
AU10	VSS111	VSS33	AD30
AU9	VSS119	VSS32	AD29
AU8	VSS118	VSS31	AD12
AU7	VSS117	VSS30	AD11
AU6	VSS116	VSS29	AD10
AT30	VSS109	VSS37	AD9
AT29	VSS108	VSS36	AD8
AT6	VSS110	VSS35	AD7
AR38	VSS105	VSS34	AD6
AR37	VSS104	VSS25	AC38
AR14	VSS101	VSS24	AC37
AR13	VSS100	VSS21	AC12
AR5	VSS107	VSS28	AC6
AR4	VSS106	VSS27	AC5
AR3	VSS103	VSS26	AC4
AR2	VSS102	VSS23	AC3
AR1	VSS99	VSS22	AC2
AP34	VSS96	VSS20	AC1
AP33	VSS95	VSS18	AB34
AP12	VSS94	VSS17	AB33
AP11	VSS93	VSS19	AB6
AP10	VSS92	VSS16	AA30
AP9	VSS98	VSS15	AA29
AP8	VSS97	VSS14	AA12
AN30	VSS89	VSS11	A30
AN29	VSS88	VSS10	A28
AN12	VSS87	VSS9	A26
AN6	VSS91	VSS8	A24
AN5	VSS90	VSS7	A22
AM38	VSS84	VSS6	A20
AM37	VSS83	VSS5	A18
AM12	VSS80	VSS4	A16
AM5	VSS86	VSS3	A14
AM4	VSS85	VSS2	A12
AM3	VSS82	VSS1	A10
AM2	VSS81	VSS13	A9
AM1	VSS79	VSS12	A6
AL34	VSS74		
AL33	VSS73		
AL14	VSS72	NCTFVSS5	B37
AL12	VSS71	NCTFVSS4	B3
AL10	VSS70	NCTFVSS2	A34
AL9	VSS78	NCTFVSS3	A4
AL8	VSS77	NCTFVSS1	A3
AL7	VSS76		
AL4	VSS75		

BGA1140

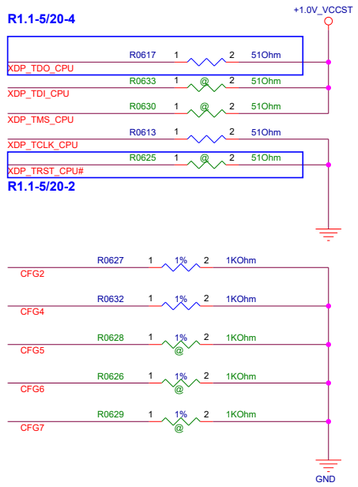
GND GND

Project Name	GL552VW		Rev 2.0
Title :	CPU_CFG,RSVD,GND		
Size B	Dept.: ASUSTeK COMPUTER INC. (BU)	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 5	of 103	

CFG



CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

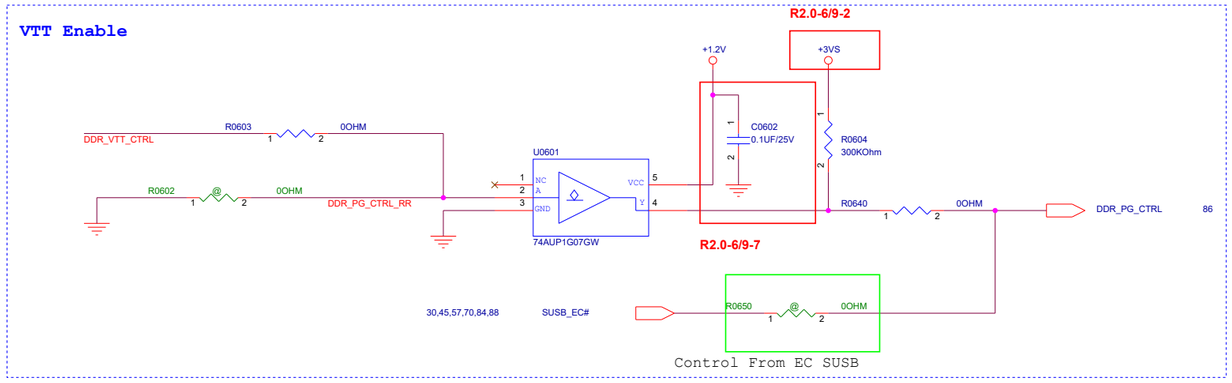
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

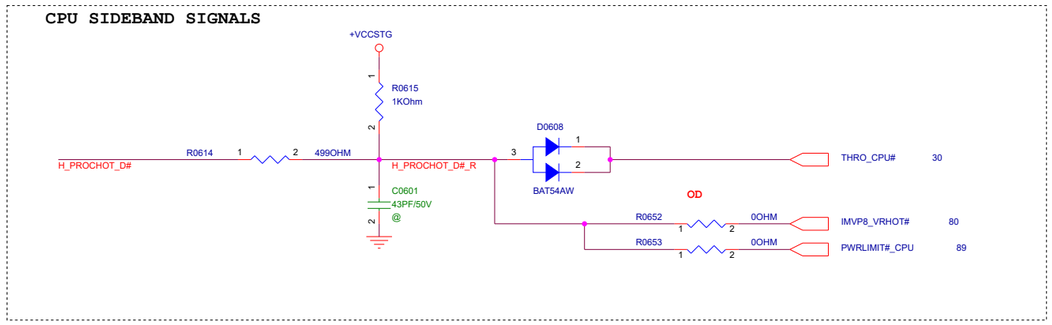
CFG[19:8] : Reserved Configuration Lanes

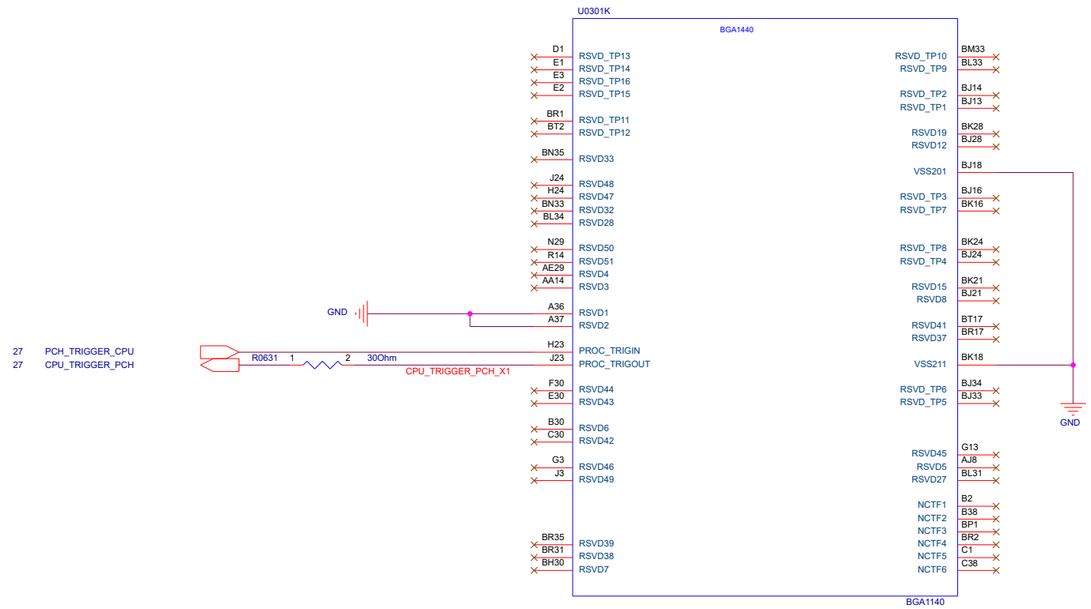
Reserved Configuration Lanes

Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 2014I209

DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120







ASUS	Project Name: GL552VW		Rev: 2.0
Title : NB_****			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 6 of 103		

CPU XDP connector

Main Board

R1.1-4/13-1

27 XDP_PREQ#_PCH
6 XDP_PREQ#
6 XDP_PRDY#
27 XDP_PRDY#_PCH

R0733 2 1 0Ohm
R0732 2 1 0Ohm

R1.1-5/8-1

R0734 1 2 1KOhm CFG3 /CPU_XDP
R0735 0Ohm 2 /CPU_XDP@

R1.1-5/12-10

J0701

6 CFG0
6 CFG1
6 CFG2
6 CFG3
6 XDP_BPM0
6 XDP_BPM1
6 CFG4
6 CFG5
6 CFG6
6 CFG7
20,28,30,33 PM_RSMRST#

CFG17 6
CFG16 6
CFG8 6
CFG9 6
CFG10 6
CFG11 6
CFG19 6
CFG18 6
CFG12 6
CFG13 6
CFG14 6
CFG15 6

R1.1-5/8-1

+3VSUS
R0736 1 2 2.2KOhm /CPU_XDP PM_PWRBTN#_XDP_X1
30,31,32 PWR_SW# R0708 2 1 0Ohm /CPU_XDP@
20,30 PM_PWRBTN# R0709 2 1 0Ohm /CPU_XDP@ PM_PWRBTN#_XDP

+1.0VSUS
C0701 0.1UF/16V /CPU_XDP@

R1.1-5/20-2

R0704 2 1 0Ohm PM_PWRBTN#_XDP /CPU_XDP@ PM_RSMRST#
R0703 2 1 0Ohm CFG0 /CPU_XDP@ FIVR_EN_R
SPI0_MOSI_SYS_PWROK_XDP

14,15,28 SMB_DAT_S
14,15,28 SMB_CLK_S
20 PCH_JTAG_TCK
6 XDP_TCLK_CPU
20 PCH_JTAGX

R0713 2 1 0Ohm /CPU_XDP XDP_TCLK1
R0717 2 1 0Ohm /CPU_XDP

NP_NC1
NP_NC2

BtoB_CON_60P
/CPU_XDP@

CLK_ITP_BCLK_PCH_X1
CLK_ITP_BCLK_PCH#_X1
ITP_PMODE_XDP_RST_R_N
XDP_DBRESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_PIN60
R0710 2 1 1KOhm /CPU_XDP
R0720 0Ohm /CPU_XDP@

CLK_ITP_BCLK_PCH#_X1 /CPU_XDP 0Ohm 3 RN0701B CLK_ITP_BCLK_PCH# 22
CLK_ITP_BCLK_PCH_X1 /CPU_XDP 0Ohm 4 RN0701A CLK_ITP_BCLK_PCH 22

+1.0VSUS
C0702 0.1UF/16V /CPU_XDP@

HDIO2_SPI 24,28

R1.1-5/8-1

R1.1-5/20-2 & 3

R0777 1 2 0OHM /CPU_XDP@ PM_SYSRST#_PCH 20
C0707 0.1UF/16V /CPU_XDP@

R1.1-5/8-1

+VCCIO
R0774 150Ohm /CPU_XDP
FIVR_EN_R

+3VSUS
R0772 1.5KOhm /CPU_XDP
24,28 SPI_SI_SPI R0731 2 1 1KOhm /CPU_XDP
R0775 2 1 0Ohm /CPU_XDP@ PM_SYSPWROK 20,30
SPI0_MOSI_SYS_PWROK_XDP
C0706 0.1UF/16V /CPU_XDP@

+1.0VSUS
R0773 1.5KOhm /CPU_XDP
R0776 2 1 0Ohm /CPU_XDP ITP_PMODE_XDP_RST_R_N
20 ITP_PMODE
R0702 1 2 1KOhm /CPU_XDP@ BUF_PLT_RST# 24,30,33,40,46,53,70

+3VS
R0719 10KOhm 5% /CPU_XDP@
+3VS
C0705 0.1UF/16V /CPU_XDP@

U0701
74CBTLV3126DS
06004-00220000
/CPU_XDP

1	NC1	VCC	16
2	1OE	4OE	15
3	1A	4A	14
4	1B	4B	13
5	2OE	3OE	12
6	2A	3A	11
7	2B	3B	10
8	GND	NC2	9

20,30,58,80 ALL_SYSTEM_PWRGD
20 PCH_JTAG_TDO
6 XDP_TDO_CPU
20 PCH_JTAG_TDI
6 XDP_TDI_CPU

/CPU_XDP@
R0721 2 1 0Ohm
R0715 2 1 0Ohm
R0711 2 /CPU_XDP 1 0Ohm /CPU_XDP
R0716 2 1 0Ohm
R0714 2 /CPU_XDP 1 0Ohm /CPU_XDP

XDP_TDO_CPU
XDP_TDO_CPU
XDP_TDI_CPU
XDP_TDI_CPU
XDP_TDO
XDP_TDI

R0723 2 1 0Ohm
R0718 2 /CPU_XDP 1 0Ohm /CPU_XDP XDP_TRST_CPU#
R0712 2 1 0Ohm
R0722 2 /CPU_XDP 1 0Ohm /CPU_XDP XDP_TMS_CPU

XDP_TRST#
XDP_TRST_CPU#
XDP_TMS
XDP_TMS_CPU

PCH_TRST# 27
XDP_TRST_CPU# 6
PCH_JTAG_TMS 20
XDP_TMS_CPU 6

Boundary Scan TP (CPU)

R1.1-5/11-10

XDP_TMS_CPU	T0705	XDP_TDO_CPU	T0704
XDP_TRST_CPU#	T0706	XDP_PREQ#	T0701
XDP_TDI_CPU	T0707	XDP_PRDY#	T0702
XDP_TCLK_CPU	T0708	CFG3	T0703

Boundary Scan TP (PCH)

24 HDIO2_PCH		HDIO2_PCH	T0712
20 PM_RSMRST#_X1		PM_RSMRST#_X1	T0709
		PCH_JTAG_TCK	T0715
		PCH_JTAG_TDI	T0716
PCH_JTAG_TDO	T0713		
PCH_JTAG_TMS	T0714		
PM_SYSRST#_PCH	T0710		
ITP_PMODE	T0711		

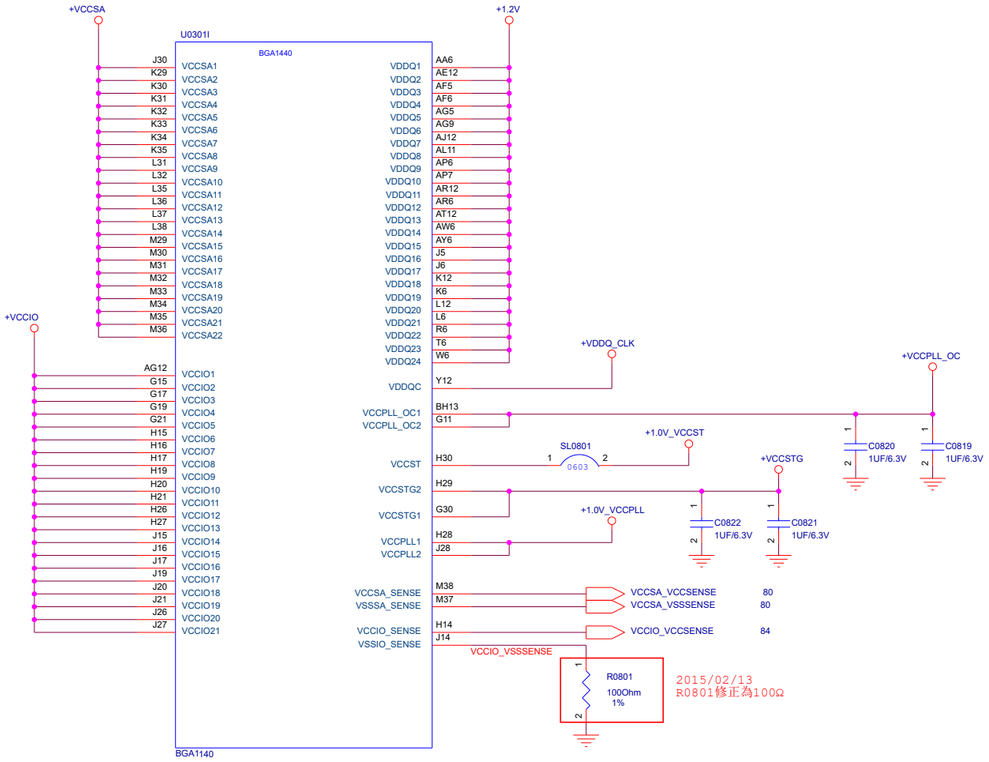
BOM

ASUSTeK COMPUTER INC. NB1

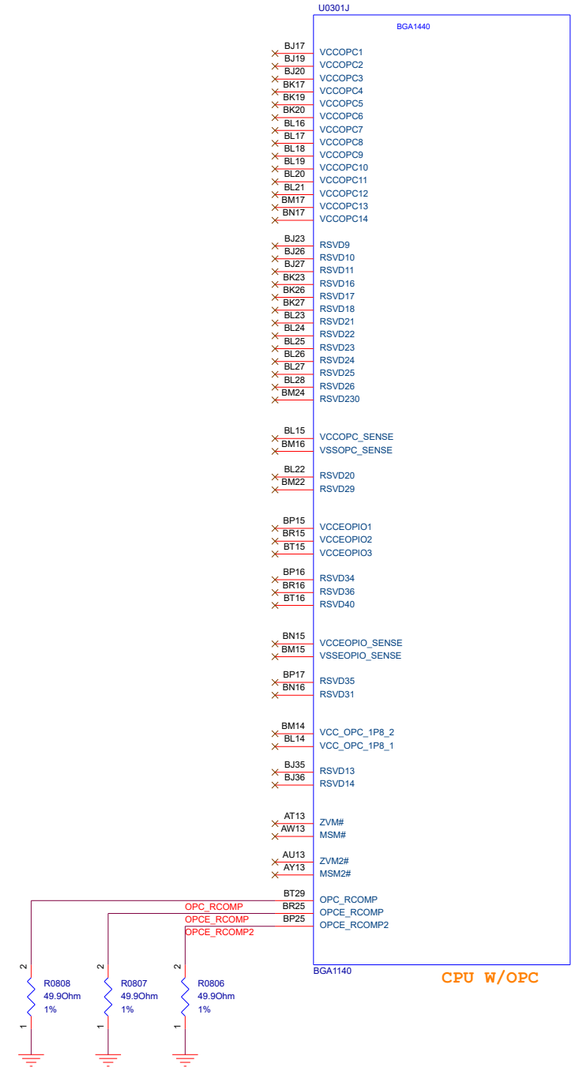
Title : CPU_XDP
Engineer: Mario_Jhu

Size	Project Name	Rev
B	GL552VW	2.0

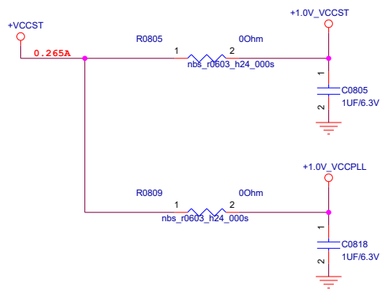
Date: Tuesday, June 23, 2015 Sheet 7 of 103



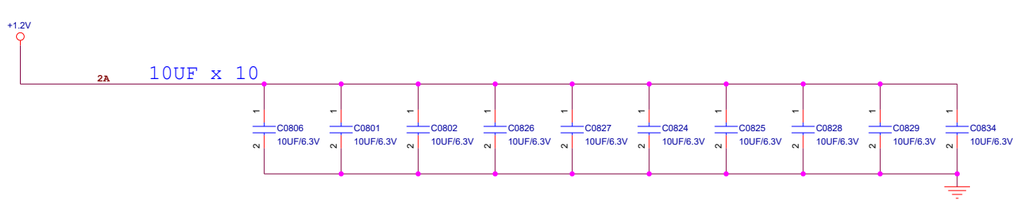
OPC Power Rails



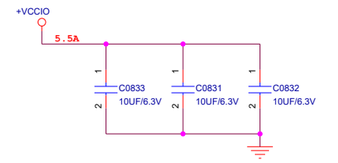
+1.0V_VCCST/+1.0V_VCCPLL DECAPS Place Back Side (TOP)



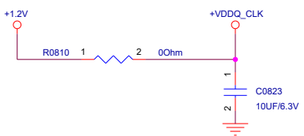
+VDDQ DECAPS Place Back Side (TOP)



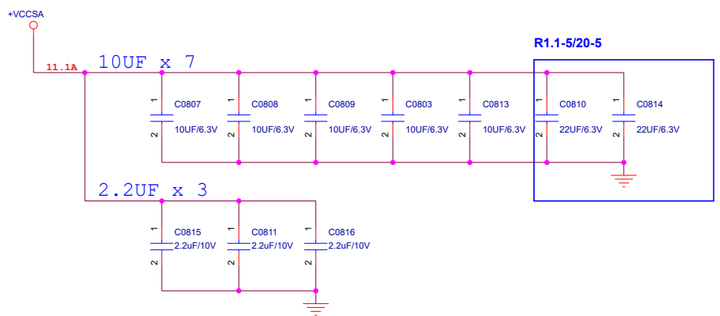
+VCCIO DECAPS Place Back Side (TOP)

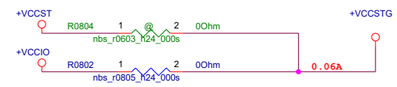


+VDDQ_CLK DECAPS Place Back Side (TOP)



+VCCSA DECAPS Place Back Side (TOP)





Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)

ASUS	Project Name: GL552VW	Rev: 2.0
Title : CPU_PWR		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 8 of 103	

Main Board

For W/GT3/GT4 CPU

+VCCGT

U0301N — BGA1440

AJ29	VCCGT1	VCCGTX1	AF29
AJ30	VCCGT2	VCCGTX2	AF30
AJ31	VCCGT3	VCCGTX3	AF31
AJ32	VCCGT4	VCCGTX4	AF32
AJ33	VCCGT5	VCCGTX5	AF33
AJ34	VCCGT6	VCCGTX6	AF34
AJ35	VCCGT7	VCCGTX7	AG13
AJ36	VCCGT8	VCCGTX8	AG14
AK31	VCCGT9	VCCGTX9	AG31
AK32	VCCGT10	VCCGTX10	AG32
AK33	VCCGT11	VCCGTX11	AG33
AK34	VCCGT12	VCCGTX12	AG34
AK35	VCCGT13	VCCGTX13	AG35
AK36	VCCGT14	VCCGTX14	AG36
AK37	VCCGT15	VCCGTX15	AH13
AK38	VCCGT16	VCCGTX16	AH14
AL13	VCCGT17	VCCGTX17	AH29
AL29	VCCGT18	VCCGTX18	AH30
AL30	VCCGT19	VCCGTX19	AH31
AL31	VCCGT20	VCCGTX20	AH32
AL32	VCCGT21	VCCGTX21	AJ13
AL35	VCCGT22	VCCGTX22	AJ14
AL36	VCCGT23		
AL37	VCCGT24		
AL38	VCCGT25		
AM13	VCCGT26		
AM14	VCCGT27		
AM29	VCCGT28		
AM30	VCCGT29		
AM31	VCCGT30		
AM32	VCCGT31		
AM33	VCCGT32		
AM34	VCCGT33		
AM35	VCCGT34		
AM36	VCCGT35		
AN13	VCCGT36		
AN14	VCCGT37		
AN31	VCCGT38		
AN32	VCCGT39		
AN33	VCCGT40		
AN34	VCCGT41		
AN35	VCCGT42		
AN36	VCCGT43		
AN37	VCCGT44		
AN38	VCCGT45		
AP13	VCCGT46		
AP14	VCCGT47		
AP29	VCCGT48		
AP30	VCCGT49		
AP31	VCCGT50		
AP32	VCCGT51		
AP35	VCCGT52		
AP36	VCCGT53		
AP37	VCCGT54		
AP38	VCCGT55		
AR29	VCCGT56		
AR30	VCCGT57		
AR31	VCCGT58		
AR32	VCCGT59		
AR33	VCCGT60		
AR34	VCCGT61		
AR35	VCCGT62		
AR36	VCCGT63		
AT14	VCCGT64		
AT31	VCCGT65		
AT32	VCCGT66		
AT33	VCCGT67		
AT34	VCCGT68		
AT35	VCCGT69		
AT36	VCCGT70		
AT37	VCCGT71		
AT38	VCCGT72		
AU14	VCCGT73		
AU29	VCCGT74		
AU30	VCCGT75		
AU31	VCCGT76		
AU32	VCCGT77		
AU35	VCCGT78		
AU36	VCCGT79		
AU37	VCCGT80		
AU38	VCCGT81		

BGA1140

VCCGT_SENSE	AH38	VCCGT_VCCSENSE 80
VSSGTX_SENSE	AH35	
VSSGT_SENSE	AH37	VCCGT_VSSSENSE 80
VCCGTX_SENSE	AH36	

+VCCGT

+VCCGT

U0301H — BGA1440

BG34	VCCGT168	VCCGT82	AV29
BG35	VCCGT169	VCCGT83	AV30
BG36	VCCGT170	VCCGT84	AV31
BH33	VCCGT171	VCCGT85	AV32
BH34	VCCGT172	VCCGT86	AV33
BH35	VCCGT173	VCCGT87	AV34
BH36	VCCGT174	VCCGT88	AV35
BH37	VCCGT175	VCCGT89	AV36
BH38	VCCGT176	VCCGT90	AW14
BJ37	VCCGT177	VCCGT91	AW31
BJ38	VCCGT178	VCCGT92	AW32
BL36	VCCGT179	VCCGT93	AW33
BL37	VCCGT180	VCCGT94	AW34
BM36	VCCGT181	VCCGT95	AW35
BM37	VCCGT182	VCCGT96	AW36
BN36	VCCGT183	VCCGT97	AW37
BN37	VCCGT184	VCCGT98	AW38
BN38	VCCGT185	VCCGT99	AY29
BP37	VCCGT186	VCCGT100	AY30
BP38	VCCGT187	VCCGT101	AY31
BR37	VCCGT188	VCCGT102	AY32
BT37	VCCGT189	VCCGT103	AY35
BE38	VCCGT152	VCCGT104	AY36
BF13	VCCGT153	VCCGT105	AY37
BF14	VCCGT154	VCCGT106	AY38
BF29	VCCGT155	VCCGT107	BA13
BF30	VCCGT156	VCCGT108	BA14
BF31	VCCGT157	VCCGT109	BA29
BF32	VCCGT158	VCCGT110	BA30
BF35	VCCGT159	VCCGT111	BA31
BF36	VCCGT160	VCCGT112	BA32
BF37	VCCGT161	VCCGT113	BA33
BF38	VCCGT162	VCCGT114	BA34
BG29	VCCGT163	VCCGT115	BA35
BG30	VCCGT164	VCCGT116	BA36
BG31	VCCGT165	VCCGT117	BB13
BG32	VCCGT166	VCCGT118	BB14
BG33	VCCGT167	VCCGT119	BB31
BC36	VCCGT132	VCCGT120	BB32
BC37	VCCGT133	VCCGT121	BB33
BC38	VCCGT134	VCCGT122	BB34
BD13	VCCGT135	VCCGT123	BB35
BD14	VCCGT136	VCCGT124	BB36
BD29	VCCGT137	VCCGT125	BB37
BD30	VCCGT138	VCCGT126	BB38
BD31	VCCGT139	VCCGT127	BC29
BD32	VCCGT140	VCCGT128	BC30
BD33	VCCGT141	VCCGT129	BC31
BD34	VCCGT142	VCCGT130	BC32
BD35	VCCGT143	VCCGT131	BC35
BD36	VCCGT144	VCCGT147	BE33
BE31	VCCGT145	VCCGT148	BE34
BE32	VCCGT146	VCCGT149	BE35
BE37	VCCGT151	VCCGT150	BE36

BGA1140

+VCCCORE

+VCCCORE

U0301G — BGA1440

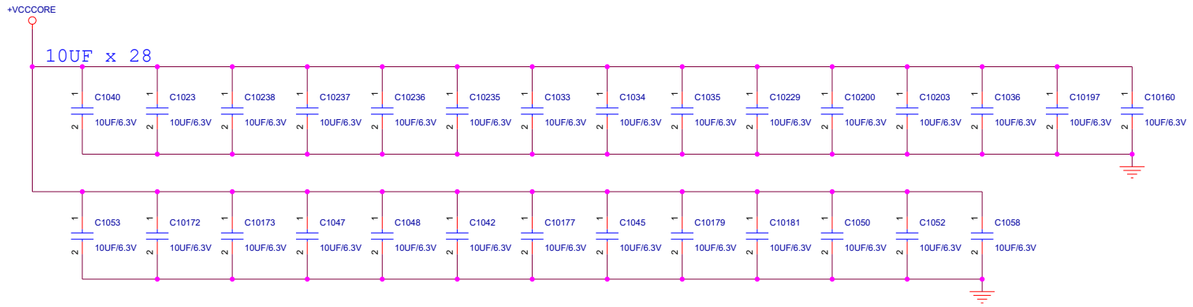
AA13	VCC1	VCC102	V32
AA31	VCC2	VCC103	V33
AA32	VCC3	VCC104	V34
AA33	VCC4	VCC105	V35
AA34	VCC5	VCC106	V36
AA35	VCC6	VCC107	V37
AA36	VCC7	VCC108	V38
AA37	VCC8	VCC109	W13
AA38	VCC9	VCC110	W14
AB29	VCC10	VCC111	W29
AB30	VCC11	VCC112	W30
AB31	VCC12	VCC113	W31
AB32	VCC13	VCC114	W32
AB35	VCC14	VCC115	W35
AB36	VCC15	VCC116	W36
AB37	VCC16	VCC117	W37
AB38	VCC17	VCC118	W38
AC13	VCC18	VCC119	Y29
AC14	VCC19	VCC120	Y30
AC29	VCC20	VCC121	Y31
AC30	VCC21	VCC122	Y32
AC31	VCC22	VCC123	Y33
AC32	VCC23	VCC124	Y34
AC33	VCC24	VCC125	Y35
AC34	VCC25	VCC126	Y36
AC35	VCC26	VCC54	L14
AC36	VCC27	VCC66	P29
AD13	VCC28	VCC67	P30
AD14	VCC29	VCC68	P31
AD31	VCC30	VCC69	P32
AD32	VCC31	VCC70	P33
AD33	VCC32	VCC71	P34
AD34	VCC33	VCC72	P35
AD35	VCC34	VCC73	P36
AD36	VCC35	VCC74	R13
AD37	VCC36	VCC75	R31
AD38	VCC37	VCC76	R32
AE13	VCC38	VCC77	R33
AE14	VCC39	VCC78	R34
AE30	VCC40	VCC79	R35
AE31	VCC41	VCC80	R36
AE32	VCC42	VCC81	R37
AE35	VCC43	VCC82	R38
AE36	VCC44	VCC83	T29
AE37	VCC45	VCC84	T30
AE38	VCC46	VCC85	T31
AF35	VCC47	VCC86	T32
AF36	VCC48	VCC87	T35
AF37	VCC49	VCC88	T36
AF38	VCC50	VCC89	T37
K13	VCC51	VCC90	T38
K14	VCC52	VCC91	U29
L13	VCC53	VCC92	U30
N13	VCC55	VCC93	U31
N14	VCC56	VCC94	U32
N30	VCC57	VCC95	U33
N31	VCC58	VCC96	U34
N32	VCC59	VCC97	U35
N35	VCC60	VCC98	U36
N36	VCC61	VCC99	V13
N37	VCC62	VCC100	V14
N38	VCC63	VCC101	V31
P13	VCC64	VCC65	P14

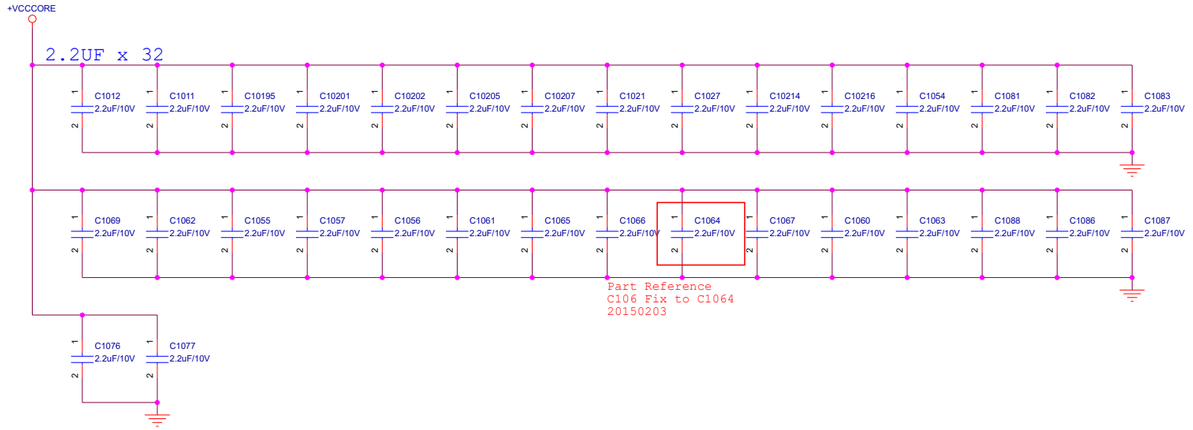
BGA1140

VCC_SENSE	AG37	VCCCORE_VCCSENSE 80
VSS_SENSE	AG38	VCCCORE_VSSSENSE 80

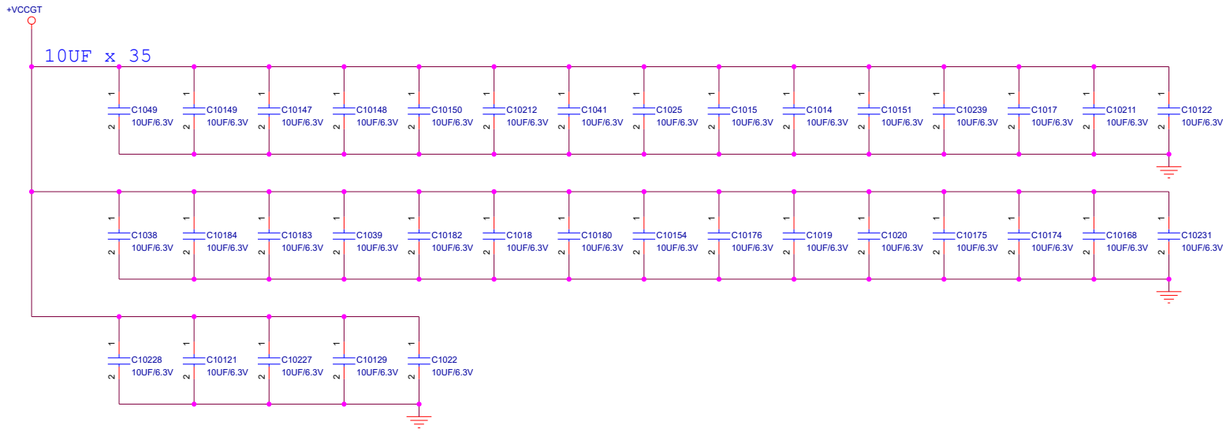
Project Name: GL552VW			Rev: 2.0
Title : NB_****			
Size: B	Dept.: ASUSTeK COMPUTER INC. (BU9)	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 9 of 103		

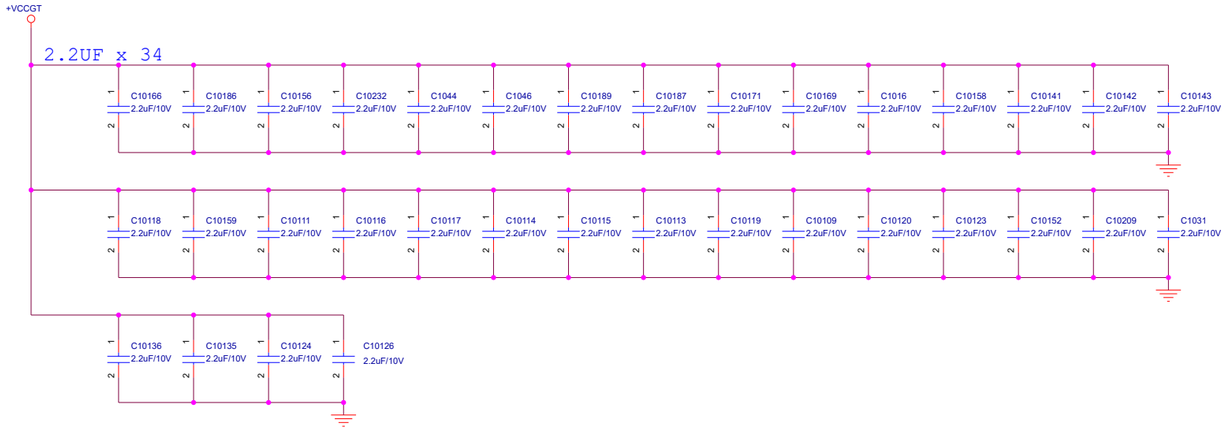
+VCCORE DECAPS Place Back Side (TOP)





+VCCGT DECAPS Place Back Side (TOP)

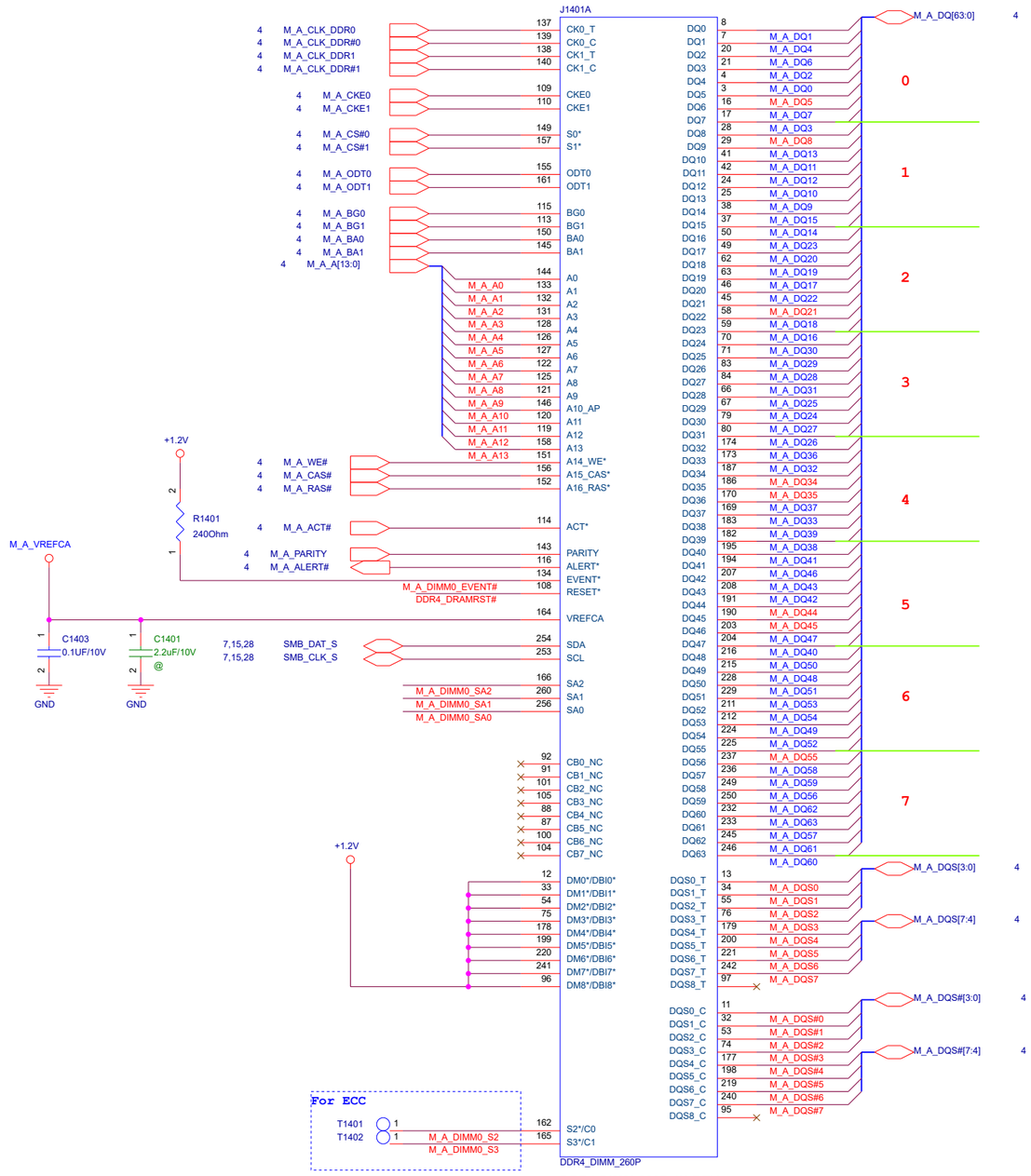




ASUS	Project Name: GL552VW	Rev: 2.0
Title : 010_CPU_POWER_CAP		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 10 of 103	

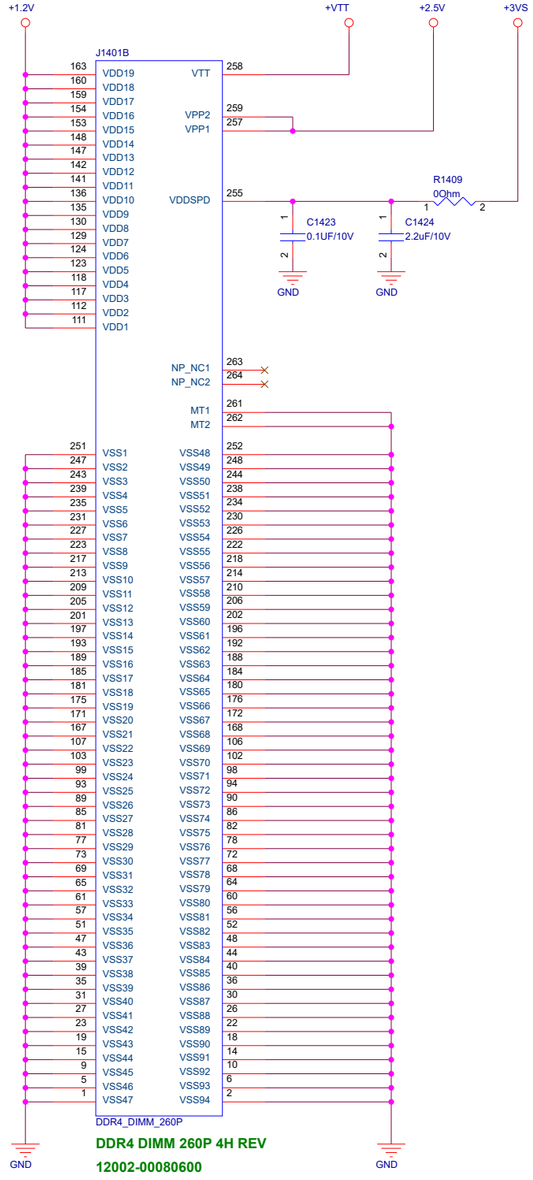
SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

12002-00080600
DDR4 DIMM 260P 4H REV



DDR4 DIMM 260P 4H REV

12002-00080600



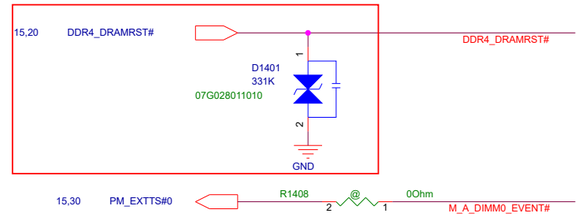
DDR4 DIMM 260P 4H REV

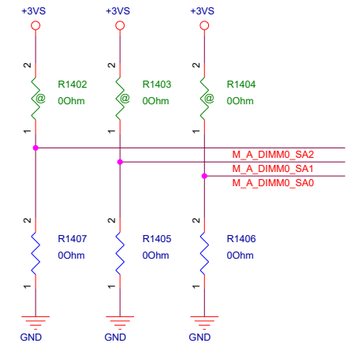
12002-00080600

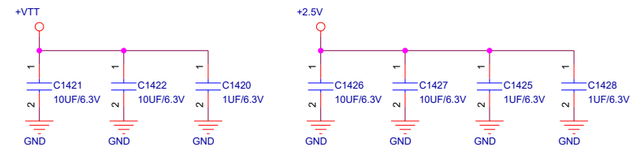
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

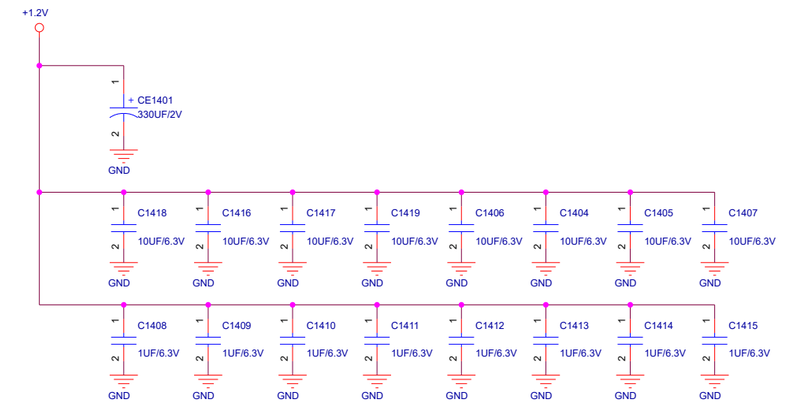
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

R2.0-6/17-1





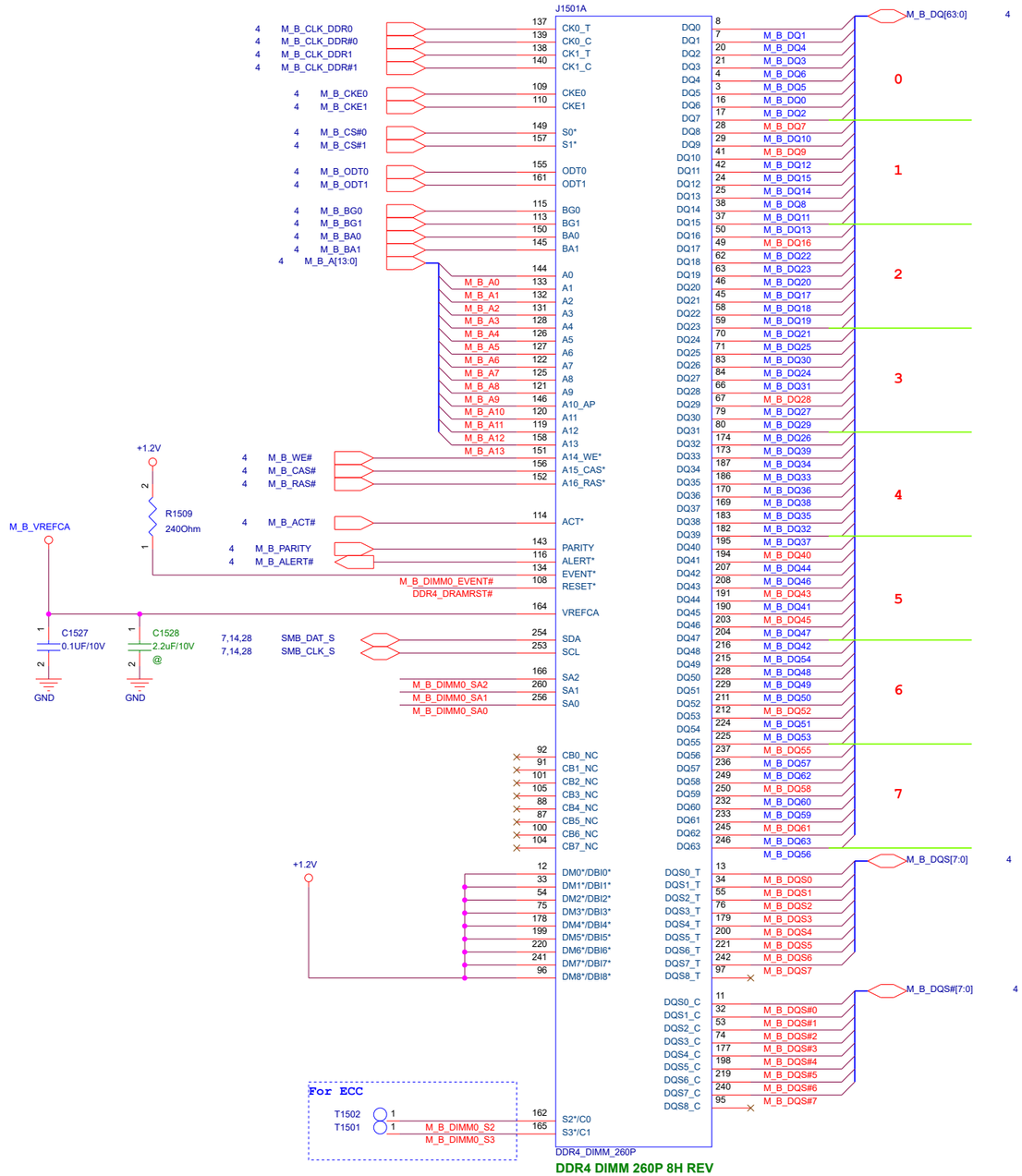


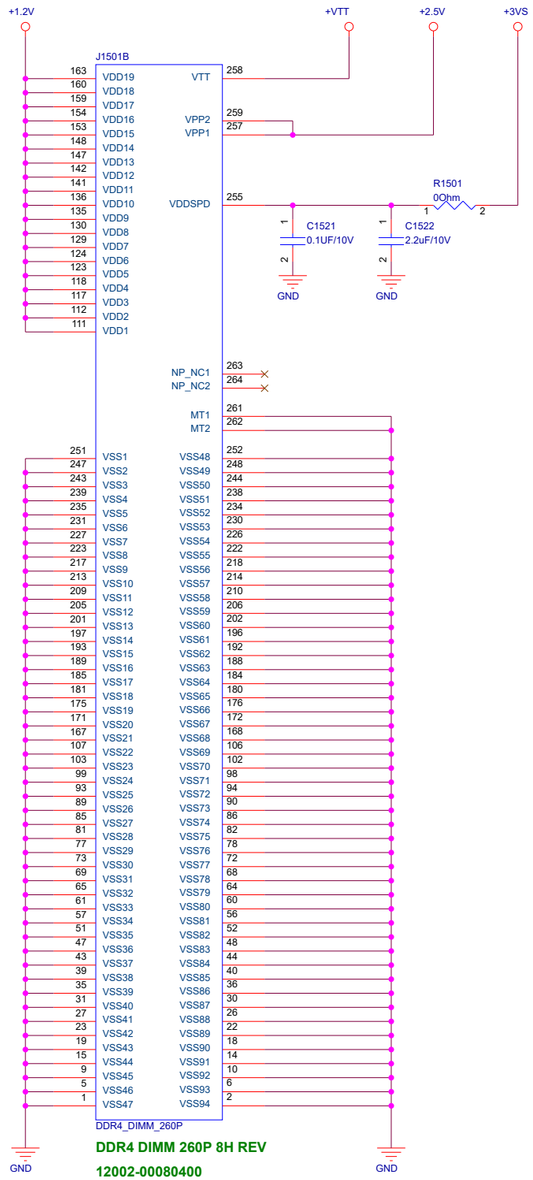


ASUS	Project Name: GL552VW	Rev: 2.0
Title : DIM_DDR4 SO-DIMM A1		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. (BU9)	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 14 of 103	

SODIMM CHB-DIMM0
TOP H8.0mm REV (J1501)

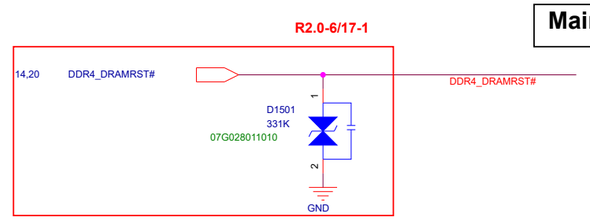
12002-00080400
DDR4 DIMM 260P 8H REV

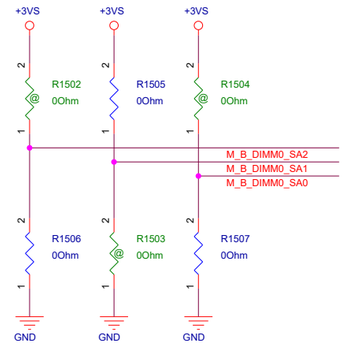


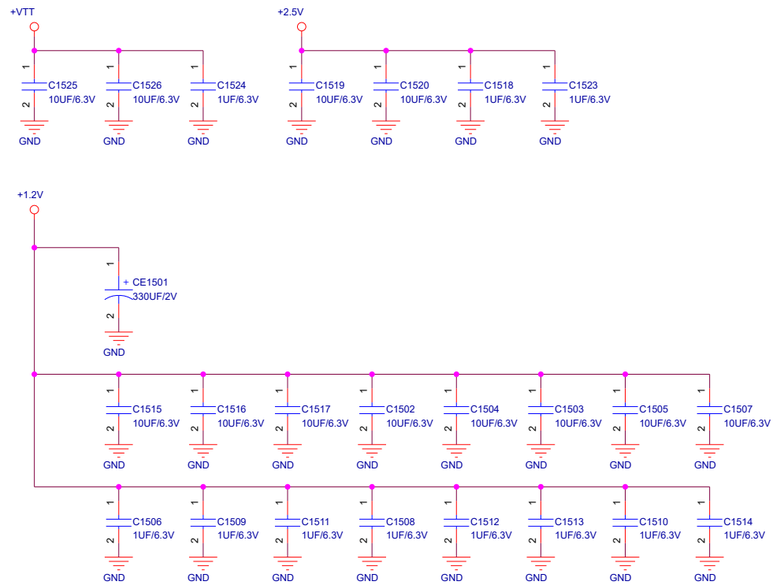


SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

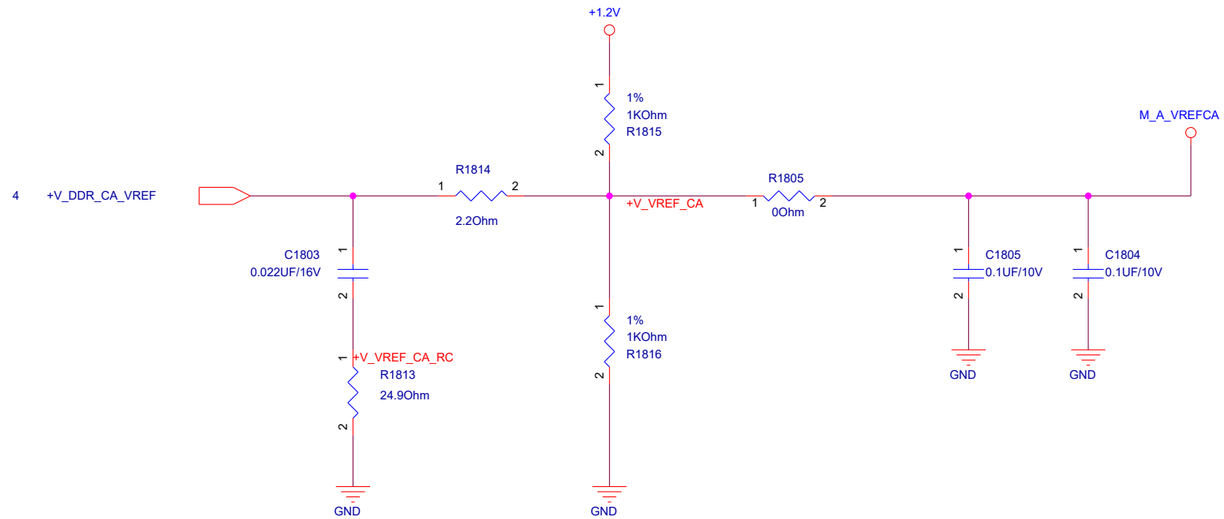




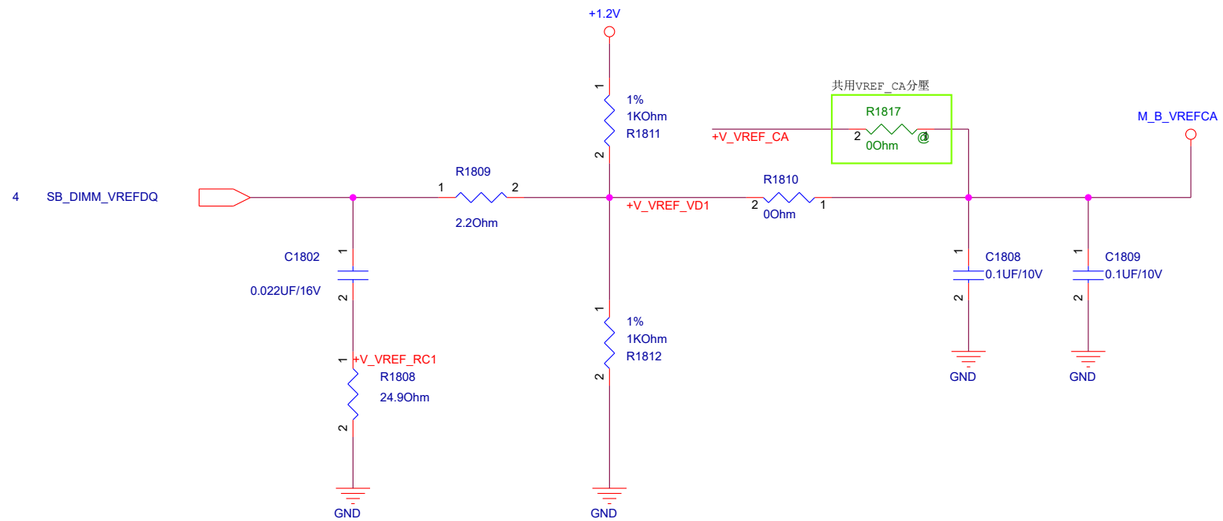


ASUS	Project Name: GL552VW	Rev: 2.0
Title :	DIM_DDR4 SO-DIMM B1	
Size: Custom	Dept.: ASUSTeK COMPUTER INC. (BU9)	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 15 of 103	

SO-DIMM0 Vref



SO-DIMM1 Vref



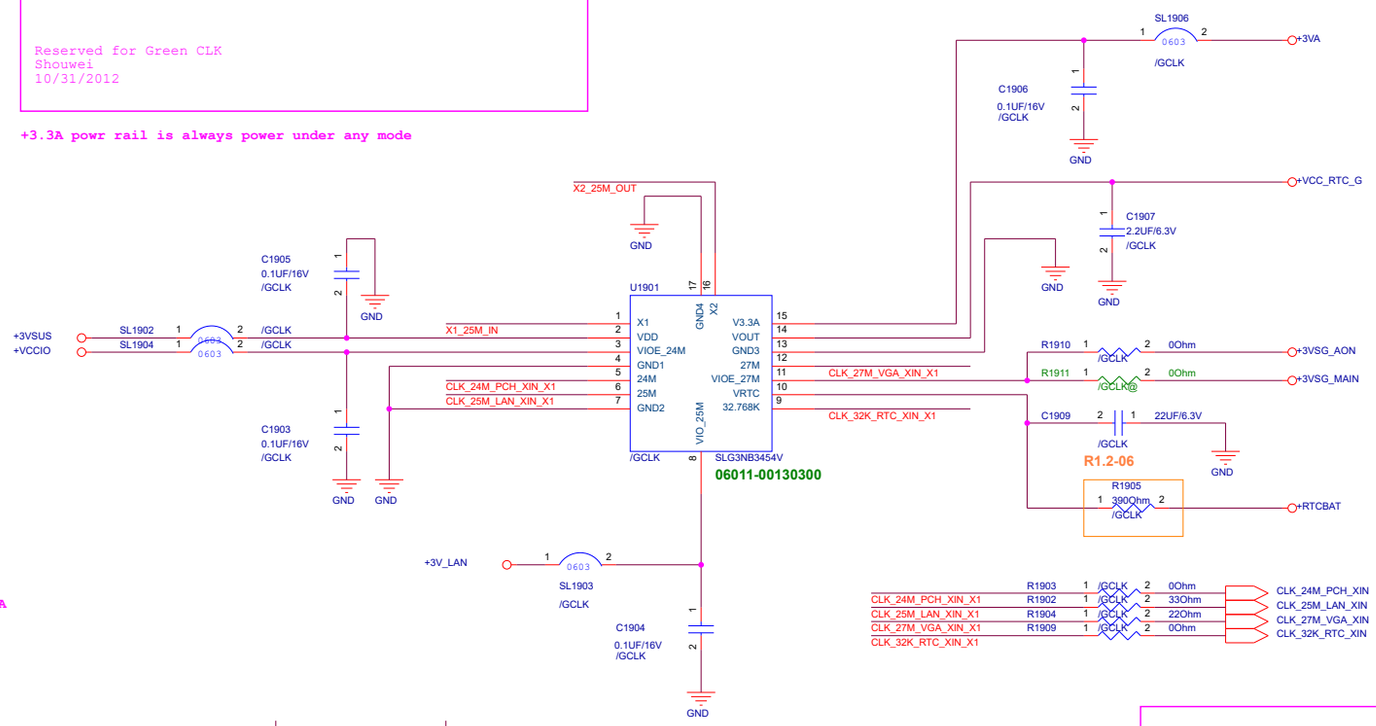
Project Name: GL552VW		Rev: 2.0
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 18 of 103	

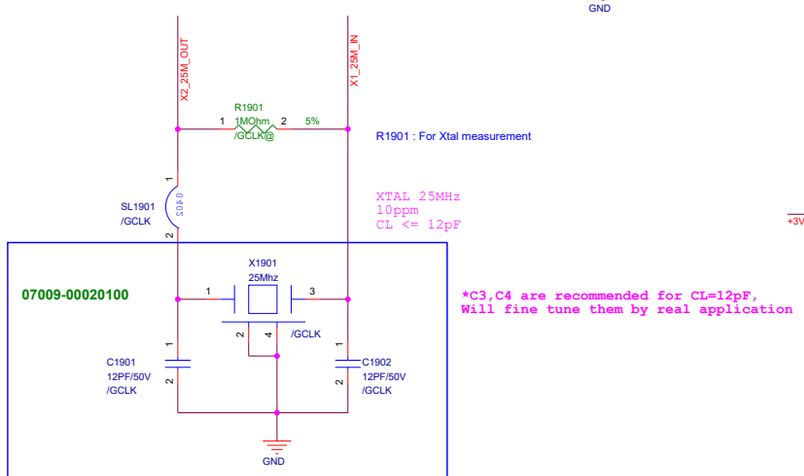
Silego Green CLK

Reserved for Green CLK
Shouwei
10/31/2012

+3.3A powr rail is always power under any mode

VDD must supply same power rail or prior to VDDIO_25M_A
& VDDIO_25M_B for Wake function
VDDIO_25M_A MUST supply
same power rail as LAN_3.3V
VDDIO_25M_B MUST supply
same power rail as PCH of XTALIN_25M

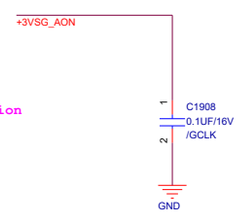


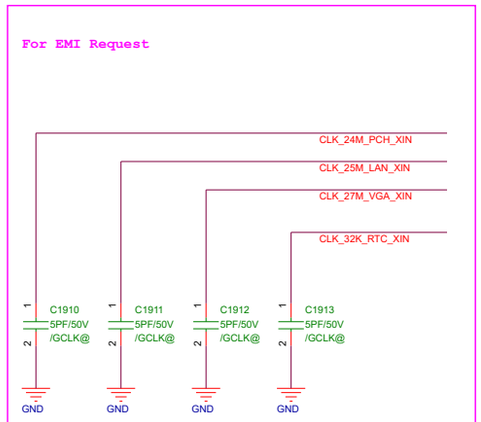


R1.1-4/13-5

X1901: 25MHZ +/-20ppm/10pF (3225)
1st: P/N:07009-00020700 HOSONIC/E3FB25.0000F10E22
2nd: P/N:07009-00020800 TXC/7V25000036
3rd: P/N:07009-00020100 EPSON/FA-238G

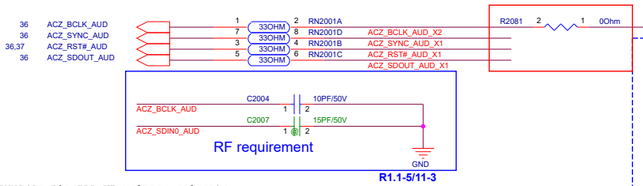
R1.1-4/13-5



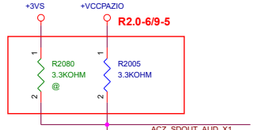


ASUSTeK COMPUTER INC. NB1	Title : Green CLK Gen	
	Engineer: Mario_Jhu	
Size: C	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 19 of 103	

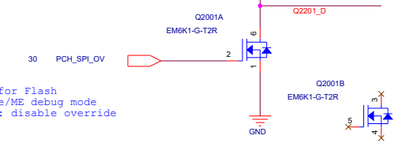
HD Audio



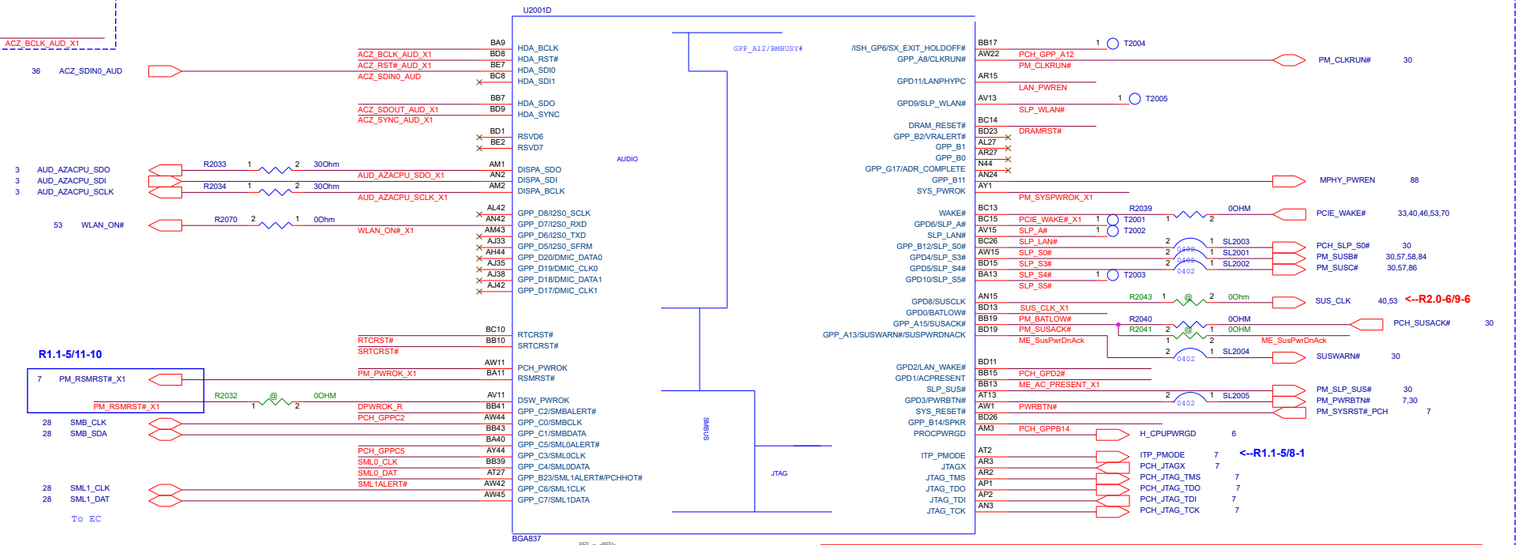
HDA_SYNC(On-Die PLL VR voltage select):
Rising edge of RSMRST# pin
High:1.5V, Low:1.8V (default)



ACZ_SDOUT:
(1)PCH:
Internal PD 20k ohm,
VIL=0.35V,VIH=0.65~3.3V
(2)ALC269:
VIL<0.35*3.3V,VIH>0.65*3.3V



ACZ_SDOUT is a signal used for Flash
Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

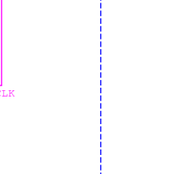


Power failure solution (S0-->G3,S5-->G3):

Intel PCH	ASUS P/N	規格
QS sample	02001-00590000	INTEL QFN48 SKYLAKE D1 QJHT

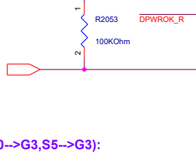
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RTCBAT	+RTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST	
	+1.2V			
	+3VAO	+3VA	+3VA_EC	
	+3VA_DSW	+3VSUS	+3VSUS_PCH	+VCCPAZIO
		+3VS		

eSPI or LPC



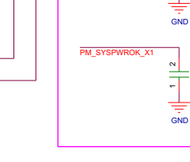
PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

TLS Confidentiality



PCH_GPPC2: weak internal pull down	
PU	Enable
PD	Disable (default)

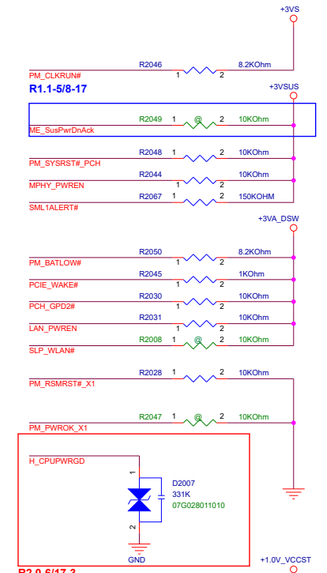
Top Swap Override



PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

SMBUS

30 LAN_WAKE#



CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

RTC battery

R2.0-6/22-2

USE RTC Battery:
P/N: 0B001-00030000 CELL COIN 3V/35mAH KTS/BCR1220H2.8AM1KB
P/N: 0B100-00040100 BATT-LI CR1220 3V/38mAH JHT/CR1220-M1

Power failure solution (S0-->G3,S5-->G3):

For EMI

R2.0-6/17-1

ASUS	Project Name: GL552VW		Rev: 2.0
Title :	PCH-CPT(1)SATA,IHDA,RTC,JTAG		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 20 of 103		

Main Board

Main Board

PCIE Setting

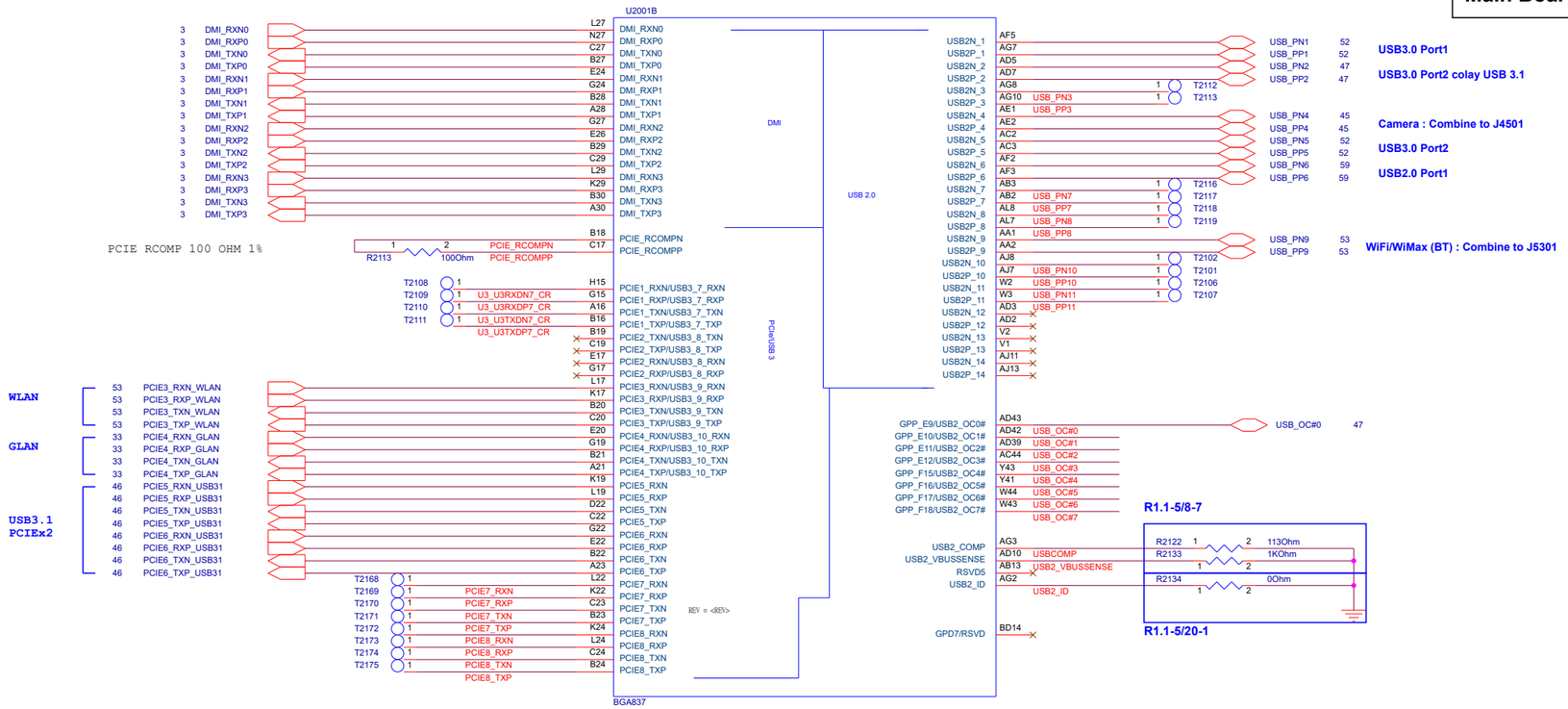
GL552VW PCIE Function define
Skylake HM170

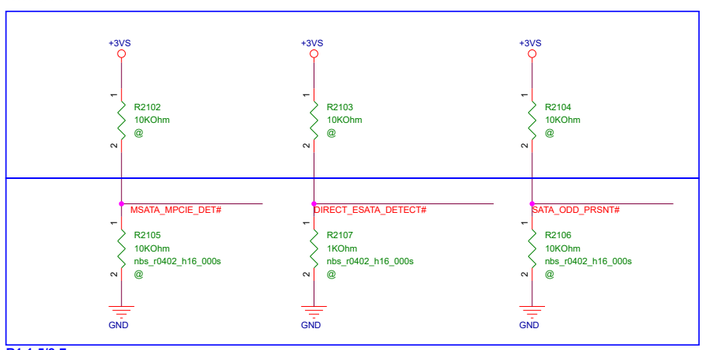
HSIO	HSIO Capabilities	Function	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3_IO	
02	USB3#02 / SSIC#01	USB3.0 IO colay USB3.1	
03	USB3#03 / SSIC#02	USB3.0 IO colay USB3.1	
04	USB3#04		
05	USB3#05	USB3_IO	
06	USB3#06		
07	USB3#07 / PCIE#01		
08	USB3#08 / PCIE#02		
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	GLAN & CardReader	SRC4
11	PCIE#05 / GBE	USB 3.1	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	PCIE*4 SSD	SRC6
16	PCIE#10 / SATA#1		
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE	1st HDD	
20	PCIE#14 / SATA#1	ODD	
21	PCIE#15 / SATA#2	SATA SSD	
22	PCIE#16 / SATA#3		
23			
24			
25			
26			

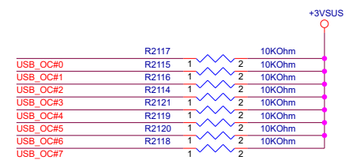
USB Setting

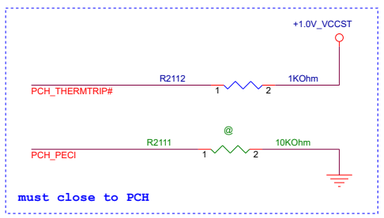
GL552VW USB Function define
Skylake HM170

USB 2.0	Function	USB 3.0	Function
USB2_01	USB3.0 IO	USB3_01	USB3.0 IO
USB2_02	USB3.0 IO colay USB3.1	USB3_02	USB3.0 IO colay USB3.1
USB2_03		USB3_03	USB3.0 IO colay USB3.1
USB2_04	Camera	USB3_04	
USB2_05	USB3.0 IO	USB3_05	USB3.0 IO
USB2_06	USB2.0 IO	USB3_06	
USB2_07		USB3_07	
USB2_08		USB3_08	
USB2_09	BT/WLAN		
USB2_10			
USB2_11			
USB2_12			



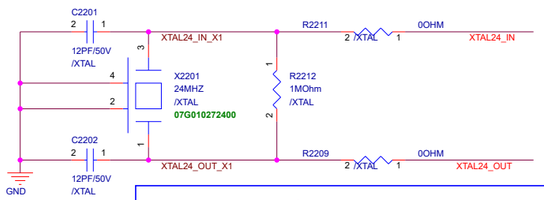






Project Name: GL552VW		Rev: 2.0
Title : PCH-CPT(2)_PCIE,CLK,USB		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 21 of 103	

XTAL 24MHz

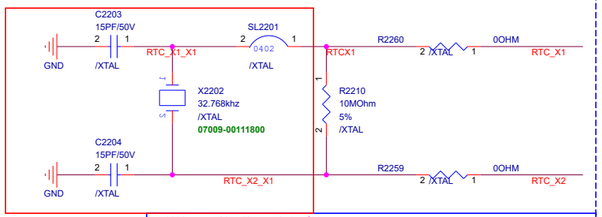


X2201_XTAL 24MHZ 3*2.5 10PF/30PPM
1st Source: P/N:07G010272400 TXC/7V24000007/24.000MHZ
2nd Source: P/N:07009-00061100 HOSONIC/E3FB24.0000F10E33
3rd Source: P/N:07009-00061000 HELE/HSX321G/X3G024000FA1H

R1.1-4/13-5

RTC CRYSTAL 32.768KHz

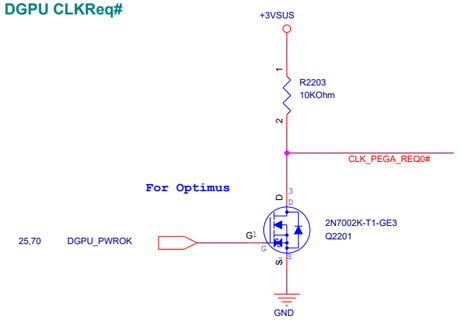
R2.0-6/9-7



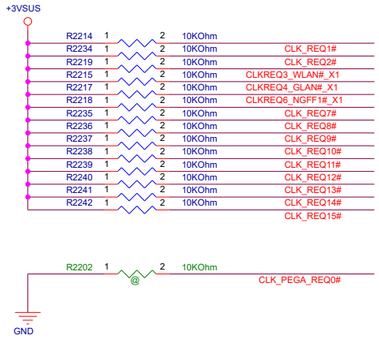
X2202_XTAL 32.768KHZ 12.5PF/20PPM
1st Source: P/N:07009-00111800 SIWARD/XTL721-M99-113 3.2*1.5
2nd Source: P/N:07009-00112000 EPSON/X1A000141000300 3.2*1.5
3rd Source: P/N:07009-00112500 TXC/9H03200052 SMD 3.2*1.5

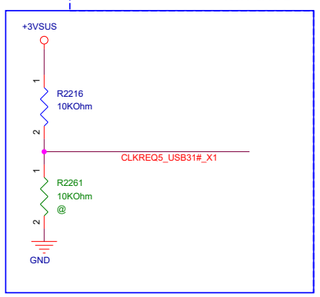
R1.1-4/13-5

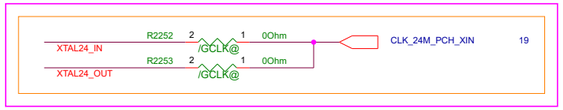
DGPU CLKReq#



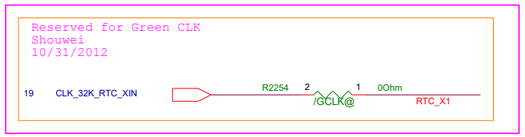
PCH CLKREQ Setting:







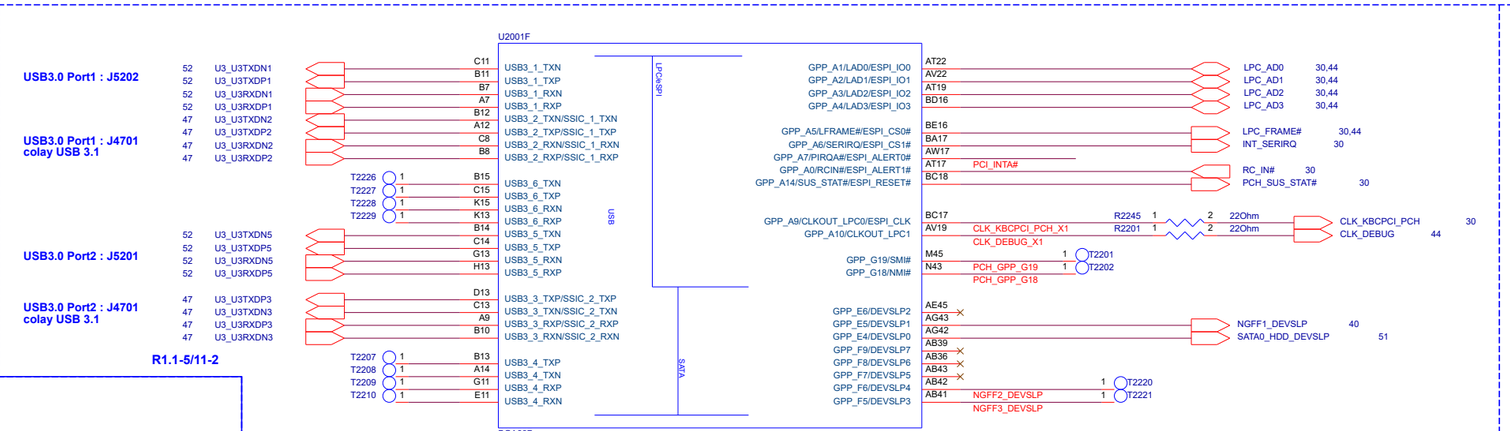
R1.0-2/9-4



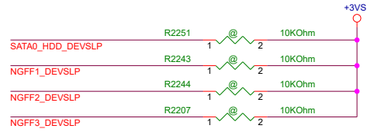
R1.0-2/9-4

R2.0-6/23v2-1

REV = <REV>



REV = <REV>



ASUS	Project Name: GL552VW		Rev: 2.0
Title :	PCH-CPT(3)_FDI,DMI,SYS PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 22 of 103		

HPD0 to WIGIG

HPD1 to HDMI

HPD2 to DP

HPD3 to VGA

HPD4 to EDP Panel

DDPD Strap Setting Update :
0 = Port D is not detected (Default)
1 = Port D is detected
20150309

+3VS

DDPC_SDA_PCH — 1 — 2.2KOHM — 2 — RN2302A
DDPC_SCL_PCH — 4 — 2.2KOHM — 3 — RN2302B

DDPB_SCL_PCH — 1 — 2.2KOHM — 2 — RN2303A
DDPB_SDA_PCH — 3 — 2.2KOHM — 4 — RN2303B

DDPD_SCL_PCH — 2.2kOHM 1 @ 2 — R2302
DDPD_SDA_PCH — 2.2kOHM 1 2 — R2301

U2001E

SPT-H_PCH

DP

HDMI

48 DDI2_HDMI_PD1

TBT DP

VGA

EDP

45 EDP_HPD

T2301 1 — DDI1_DP_HPD0 — AW4 — GPP_I0/DDPB_HPD0
T2308 1 — AY2 — GPP_I1/DDPC_HPD1
T2310 1 — DDI3_TBT_HPD2 — AV4 — GPP_I2/DDPD_HPD2
DDIE_VGA_HPD3 — BA4 — GPP_I3/DDPE_HPD3

BD7 — GPP_I4/EDP_HPD

GPP_I7/DDPC_CTRLCLK — BB3
GPP_I8/DDPC_CTRLDATA — BD6 — DDPC_SCL_PCH
GPP_I5/DDPB_CTRLCLK — BA5 — DDPC_SDA_PCH
GPP_I6/DDPB_CTRLDATA — BC4 — DDPB_SCL_PCH — 1 — T2307
GPP_I9/DDPD_CTRLCLK — BE5 — DDPB_SDA_PCH — 1 — T2306
GPP_I10/DDPD_CTRLDATA — BE6 — DDPD_SCL_PCH — 1 — T2302
DDPD_SDA_PCH — 1 — T2303

DDPC_SCL_PCH
DDPC_SDA_PCH

48 48 HDMI

GPP_F14 — Y44
GPP_F23 — V44
GPP_F22 — W39
GPP_G23 — L43
GPP_G22 — L44
GPP_G21 — U35
GPP_G20 — R35
GPP_H23 — BD36

WLAN_WAKE_CTRL_CRB — 1 — T2309

<PART_SYM_NUM>

BGA837

REV = <REV>

ASUS	Project Name: GL552VW	Rev: 2.0
Title : PCH-CPT(4)_eDP,PCI,DP		
Size: A	Dept.: ASUSTeK COMPUTER INC. NBG	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 23 of 103	

Main Board

U2001A — SPT-H_PCH — BGA837

T2401 1 — PCI_PME# — BD17 GPP_A11/PME#

AG15 RSVD1
AG14 RSVD2
AF17 RSVD3
AE17 RSVD4

T2402 1 — AR19 TP2
T2403 1 — PCH_TP2 — AN17 TP1
PCH_TP1

7,28 SPI_SI_SPI — 15Ohm 1 2 R2401 — BB29 SPI0_MOSI
28 SPI_SO_SPI — 15Ohm 1 2 R2402 — SPI_SI — BE30 SPI0_MISO
28 SPI_CS#0_SPI — 0Ohm R2403 — SPI_SO — BD31 SPI0_CS0#
28 SPI_CLK_SPI — 15Ohm 11 2 R2404 — SPI_CS#0 — BC31 SPI0_CLK
T2404 1 — SPI_CLK — AW31 SPI0_CS1#
SB_SPICS1#

7 HDIO2_PCH
7,28 HDIO2_SPI — 15Ohm 1 2 R2405 — BC29 SPI0_IO2
28 HDIO3_SPI — 15Ohm 1 2 R2406 — BD30 SPI0_IO3
T2405 1 — HDIO3 — AT31 SPI0_CS2#

R1.1-5/11-10

T2408 1 — SB_SPICS2# — AN36 GPP_D1
T2406 1 — GPIO_3_FORCE_PWR — AL39 GPP_D0
CIO_PLUG_EVENT — AN41 GPP_D3

30 EXT_SCI# — EXT_SCI# — AN38 GPP_D2
30 EXT_SMI# — EXT_SMI# — AH43 GPP_D22
T2407 1 — AG44 GPP_D21
LED_Record

GPP_B13/PLTRST# — BB27 — PLT_RST#

GPP_G16/GSXCLK — P43
GPP_G12/GSXDOUT — R39
GPP_G13/GSXSLOAD — R36
GPP_G14/GSXDIN — R42
GPP_G15/GSXSRESET# — R41

GPP_E3/CPU_GP0 — AF41 — USB31_SMI# — 46
GPP_E7/CPU_GP1 — AE44
GPP_B3/CPU_GP2 — BC23
GPP_B4/CPU_GP3 — BD24

GPP_H18/SML4ALERT# — BC36
GPP_H17/SML4DATA — BE34
GPP_H16/SML4CLK — BD39
GPP_H15/SML3ALERT# — BB36
GPP_H14/SML3DATA — BA35
GPP_H13/SML3CLK — BC35
GPP_H12/SML2ALERT# — BD35
GPP_H11/SML2DATA — AW35
GPP_H10/SML2CLK — BD34
INTRUDER# — BE11 — SM_INTRUDER#

R1.1-5/8-12

T2409 1 — +3VA_RTC
R2407 1 1MOhm 2

+3VS

R2411 1 2 10KOhm — EXT_SCI#
R2410 1 2 10KOhm — EXT_SMI#

For USB3.1 Legacy support

+3V — R2412 @ 10KOhm — USB31_SMI#

R1.1-5/12-6

U2401 — 74LVC1G08GW — REV = <REV>

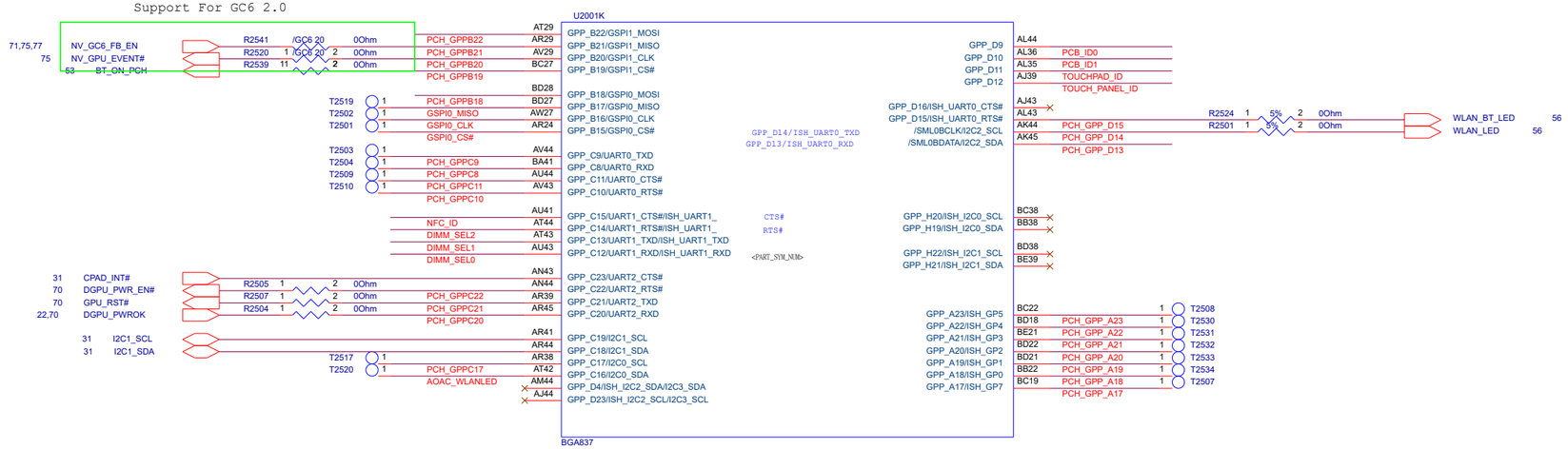
+3V
1 INB
2 INA
3 GND
5 VCC
4 OUTY

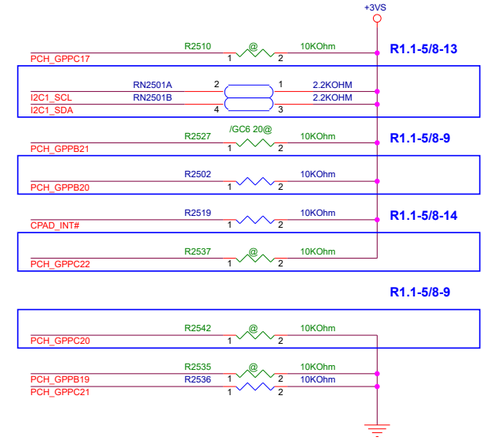
PLT_RST# — BUF_PLT_RST# — 7,30,33,40,46,53,70

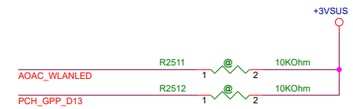
GND
R2408 100KOhm
R2409 1 @ 2 0Ohm
PLT_RST# — 32
GND

Project Name: GL552VW		Rev: 2.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 24 of 103	

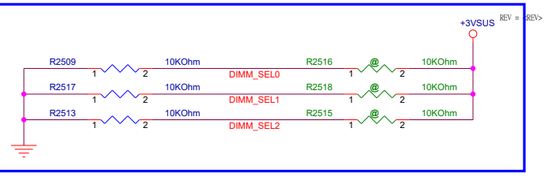
Support For GC6 2.0







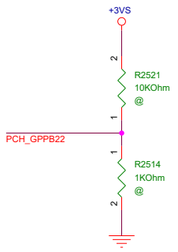
Onboard Memory PCB-ID:
GPA_18 => DIMM_SEL0
GPA_19 => DIMM_SEL1
GPA_20 => DIMM_SEL2



	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)	
DIMM_SEL0				
DIMM_SEL1				
DIMM_SEL2				

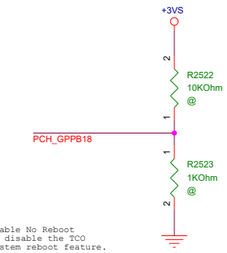
	HYNIX (4Gb) 03006-00011600 DDR3L 1600 512M*8 1.35V HYNIX/H5TC4G83AFR-PBA	ELPIDA (4Gb)	Micron(4Gb) 03006-00011400 DDR3L 1600 512M*8 1.35V MICRON/MT41K512M8RH-125:E	
DIMM_SEL0	L		L	
DIMM_SEL1	L		L	
DIMM_SEL2	H		L	

Boot BIOS Strap Bit BBS



PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

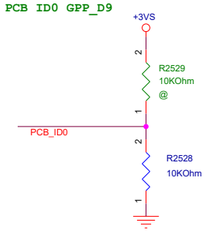
No Reboot



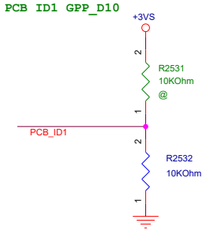
NOTE: Enable No Reboot
PCH will disable the TCO
Timer system reboot feature.
This function is useful when running ITP/XDP.

PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

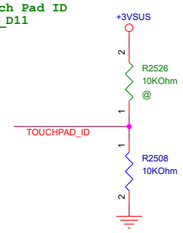
PCB ID0 GPP_D9



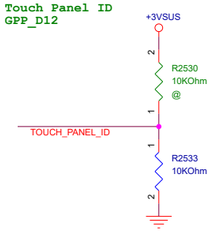
PCB ID1 GPP_D10



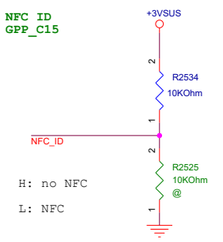
Touch Pad ID
GPP_D11



Touch Panel ID
GPP_D12



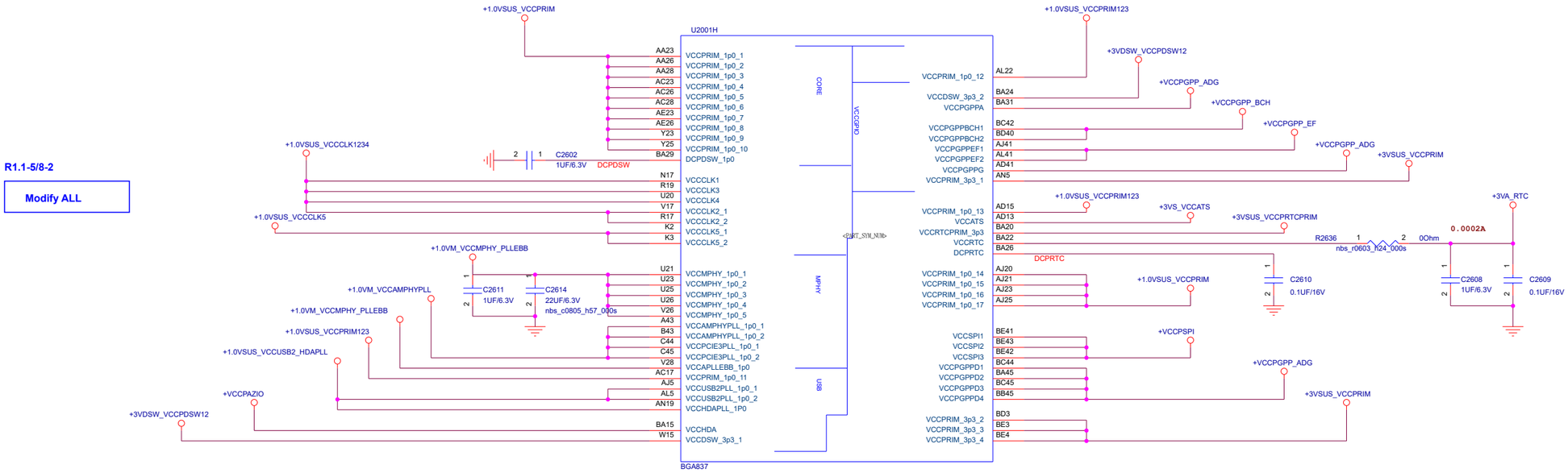
NFC ID
GPP_C15

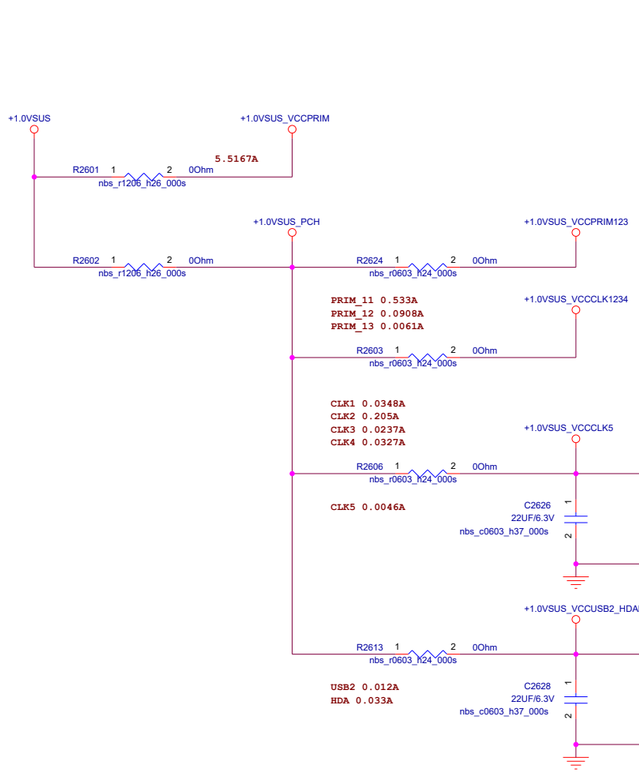


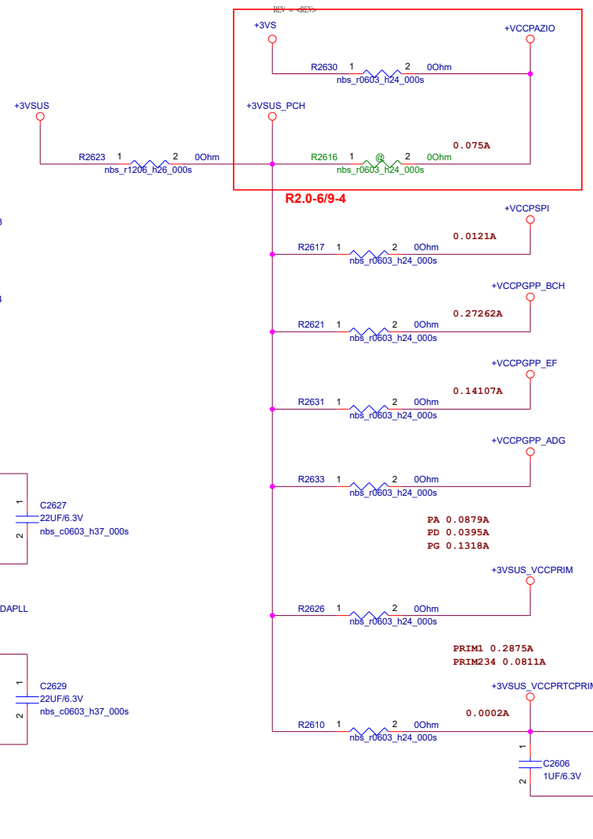
Project Name: GL552VW		Rev: 2.0
Title : PCH-CPT(6)_GPIO,MISC		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 25 of 103	

R1.1-5/8-2

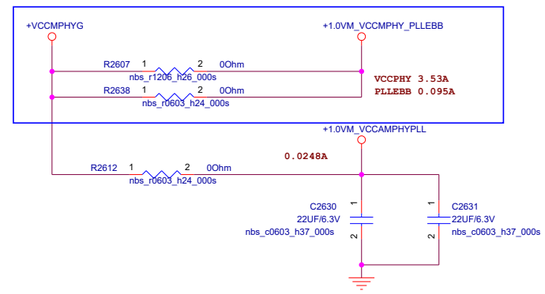
Modify ALL

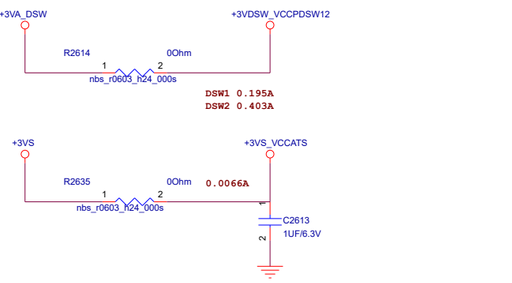






R1.1-5/11-5





ASUS	Project Name: GL552VW		Rev: 2.0
Title : PCH-CPT(7)_POWER,GND			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015		Sheet 26 of 103	

U2001I

SPT-H_PCH

AC18	VSS1	VSS75	AR5		
AN4	VSS2	VSS76	AR7		
AN10	VSS3	VSS77	U15		
BE14	VSS4	VSS78	AL4		
BE18	VSS5	VSS79	AE29		
BE23	VSS6	VSS80	AE4		
BE28	VSS7	VSS81	AE42		
BE32	VSS8	VSS82	AF18		
BE37	VSS9	VSS83	AF20		
BE40	VSS10	VSS84	AF21		
BE9	VSS11	VSS85	AF23		
C10	VSS12	VSS86	AF25		
C2	VSS13	VSS87	AF26		
C28	VSS14	VSS88	AF28		
C37	VSS15	VSS89	AF29		
J7	VSS16	VSS90	AG11		
K10	VSS17	VSS91	AG13		
K27	VSS18	VSS92	AG31		
K33	VSS19	VSS93	AG32		
K36	VSS20	VSS94	AG33		
K4	VSS21	VSS95	AG38		
K42	VSS22	VSS96	AG4		
K43	VSS23	VSS97	AH1		
L12	VSS24	VSS98	AH17		
L13	VSS25	VSS99	AH18		
L15	VSS26	VSS100	AH20		
L4	VSS27	VSS101	AH21		
L41	VSS28	VSS102	AH23		
L8	VSS29	VSS103	AH25		
M35	VSS30	VSS104	AH26		
M42	VSS31	VSS105	AH28		
N10	VSS32	VSS106	AH29		
N15	VSS33	VSS107	AH45		
N19	VSS34	VSS108	AJ10		
N22	VSS35	VSS109	AJ14		
N24	VSS36	VSS110	AJ15		
N35	VSS37	VSS111	AJ17		
N36	VSS38	VSS112	AJ18		
N4	VSS39	VSS113	AJ26		
N41	VSS40	VSS114	AJ28		
N5	VSS41	VSS115	AJ29		
P17	VSS42	VSS116	AJ31		
P19	VSS43	VSS117	AJ32		
P22	VSS44	VSS118	AJ36		
P45	VSS45	VSS119	AK4		
R10	VSS46	VSS120	AK42		
R14	VSS47	VSS121	AU7		
R22	VSS48	VSS122	AV17		
R29	VSS49	VSS123	AV24		
R33	VSS50	VSS124	AV27		
R38	VSS51	VSS125	AV31		
R5	VSS52	VSS126	AV33		
T1	VSS53	VSS127	AV6		
T2	VSS54	VSS128	AW13		
T4	VSS55	VSS129	AW19		
Y18	VSS56	VSS130	AW29		
Y20	VSS57	VSS131	AW37		
Y21	VSS58	VSS132	AW9		
Y26	VSS59	VSS133	AY38		
Y28	VSS60	VSS134	AY45		
Y29	VSS61	VSS135	B25		
A18	VSS62	VSS136	B3		
A25	VSS63	VSS137	B37		
A32	VSS64	VSS138	B40		
A37	VSS65	VSS139	B6		
AA17	VSS66	VSS140	BA1		
AA18	VSS67	VSS141	BB11		
AA20	VSS68	VSS142	BB16		
AA21	VSS69	VSS143	BB21		
AA25	VSS70	VSS144	BB25		
AA29	VSS71	VSS145	BB30		
AA4	VSS72	VSS146	BB34		
AA42	VSS73	VSS147	BC2		
AB10	VSS74	VSS148	BD43		

REV = <REV>

BGA837 <PART_SYM_NUM>

GND GND

U2001L

C42	VSS165	VSS233	AB11
D10	VSS166	VSS234	AB7
D12	VSS167	VSS235	AB14
D15	VSS168	VSS236	AB31
D16	VSS169	VSS237	AB32
D17	VSS170	VSS238	AB38
D19	VSS171	VSS239	AB4
D21	VSS172	VSS240	AB5
D24	VSS173	VSS241	AC1
D25	VSS174	VSS242	AC20
D27	VSS175	VSS243	AC21
D29	VSS176	VSS244	AC25
D30	VSS177	VSS245	AC29
D31	VSS178	VSS246	AC45
D33	VSS179	VSS247	AB8
D35	VSS180	VSS248	AD11
D36	VSS181	VSS249	AD14
E13	VSS182	VSS250	AB15
E15	VSS183	VSS251	AD32
E31	VSS184	VSS252	AD33
E33	VSS185	VSS253	AD36
F44	VSS186	VSS254	AD4
F8	VSS187	VSS255	AD8
G42	VSS188	VSS256	AE18
G9	VSS189	VSS257	AE20
H17	VSS190	VSS258	AE21
H19	VSS191	VSS259	AE25
H22	VSS192	VSS260	AE28
H24	VSS193	VSS261	AL10
H27	VSS194	VSS262	AL11
H29	VSS195	VSS263	AL13
H3	VSS196	VSS264	AL17
H35	VSS197	VSS265	AL19
J10	VSS198	VSS266	AL24
J11	VSS199	VSS267	AL29
J3	VSS200	VSS268	AL32
J39	VSS201	VSS269	AL33
J5	VSS202	VSS270	AL38
T42	VSS203	VSS271	AM15
U10	VSS204	VSS272	AM17
U11	VSS205	VSS273	AM19
U14	VSS206	VSS274	AM22
U17	VSS207	VSS275	AM24
U18	VSS208	VSS276	AM27
U28	VSS209	VSS277	AM29
U29	VSS210	VSS278	AM45
U31	VSS211	VSS279	AN11
U32	VSS212	VSS280	AN22
U33	VSS213	VSS281	AN27
U38	VSS214	VSS282	AN31
U4	VSS215	VSS283	AN39
U8	VSS216	VSS284	AN7
V18	VSS217	VSS285	AN8
V20	VSS218	VSS286	AP11
V21	VSS219	VSS287	AP4
V23	VSS220	VSS288	AR33
V25	VSS221	VSS289	AR34
V29	VSS222	VSS290	AR42
V3	VSS223	VSS291	AR9
V45	VSS224	VSS292	AT10
W14	VSS225	VSS293	AT15
W31	VSS226	VSS294	AT36
W32	VSS227	VSS295	AT9
W33	VSS228	VSS296	AU1
W38	VSS229	VSS297	AU35
W4	VSS230	VSS298	AU36
W8	VSS231	VSS299	AU39
Y17	VSS232	VSS300	AU45
		VSS301	C4

REV = <REV>

BGA837 <PART_SYM_NUM>

GND GND

U2001J

BD2	VSS149	RSVD10	AR22
BD45	VSS150	RSVD11	W13
BD44	VSS151	RSVD12	U13
BE44	VSS152	RSVD13	P31
D45	VSS153	RSVD14	N31
A42	VSS154		
B45	VSS155	RSVD15	P27
B44	VSS156	RSVD16	R27
A4	VSS157	RSVD17	N29
A3	VSS158	RSVD18	P29
B2	VSS159	RSVD19	AN29
A2	VSS160	RSVD20	R24
B1	VSS161	RSVD21	P24
BB1	VSS162	PREQ#	AT3
BC1	VSS163	PRDY#	AT4
A44	VSS164	CPU_TRST#	AY5
C1	RSVD8	PCH_TRIGOUT	AL2
D1	RSVD9	PCH_TRIGIN	AK1

BGA837

GND

R2701 1 2 30Ohm

PCH_TRIGGER_CPU_X1

R1.1-4/13-1

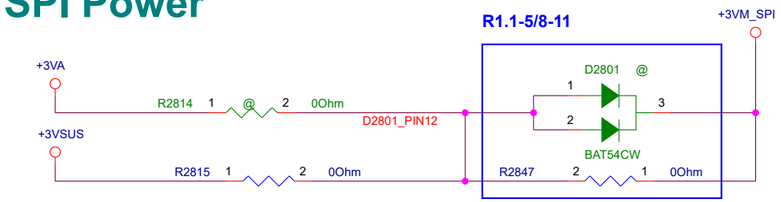
XDP_PREQ#_PCH		7
XDP_PRDY#_PCH		7
PCH_TRST#	7	
PCH_TRIGGER_CPU		6
CPU_TRIGGER_PCH		6

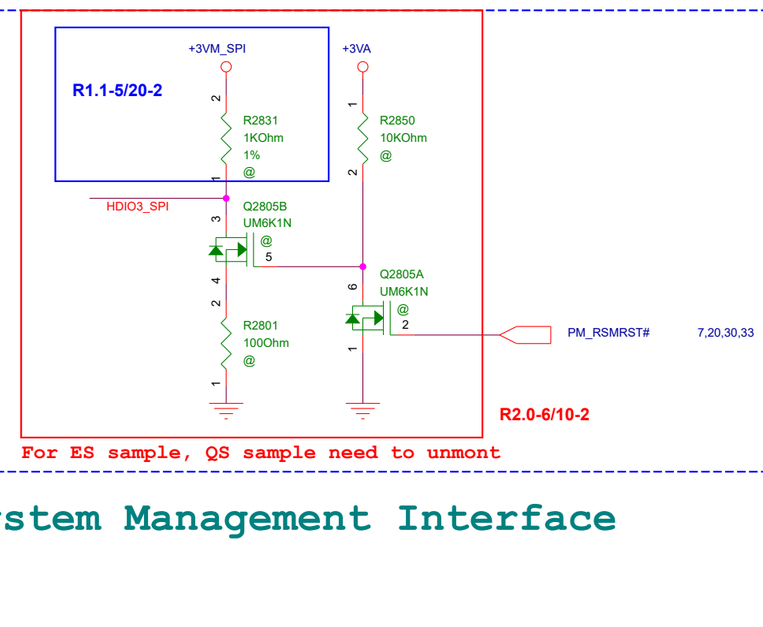
REV = <REV>

Project Name	GL552VW	Rev	2.0
Title :	PCH-CPT(8)_POWER,GND		
Size	B	Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Mario_Jhu		
Date:	Tuesday, June 23, 2015	Sheet	27 of 103

Main Board

SPI Power





For ES sample, QS sample need to unmont

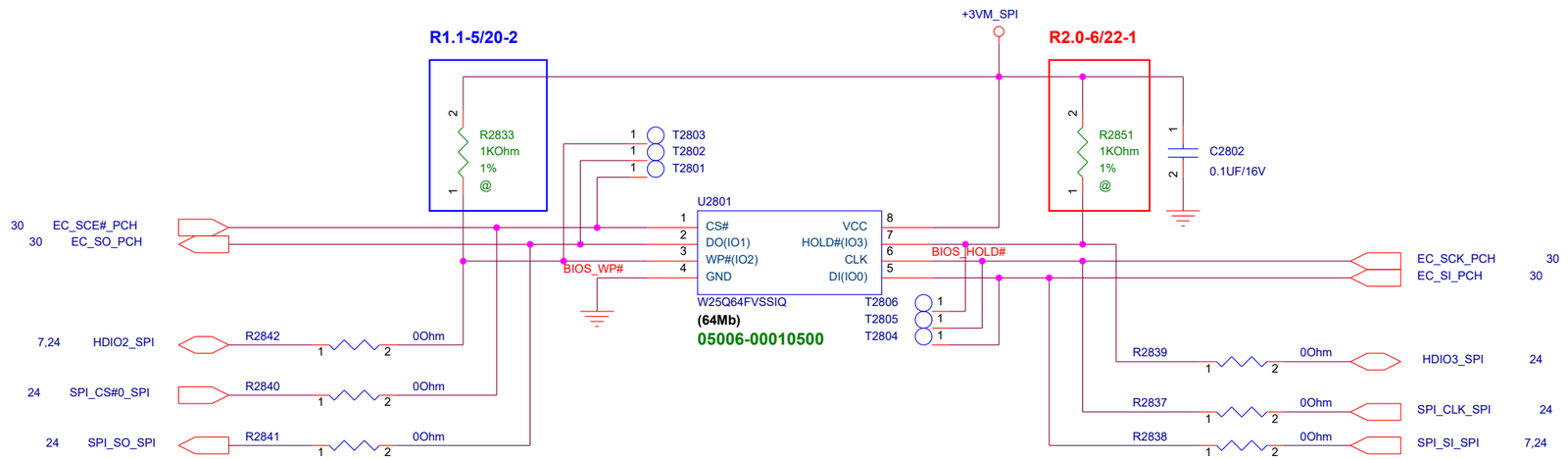
1st SPI ROM

R1.1-4/13-5

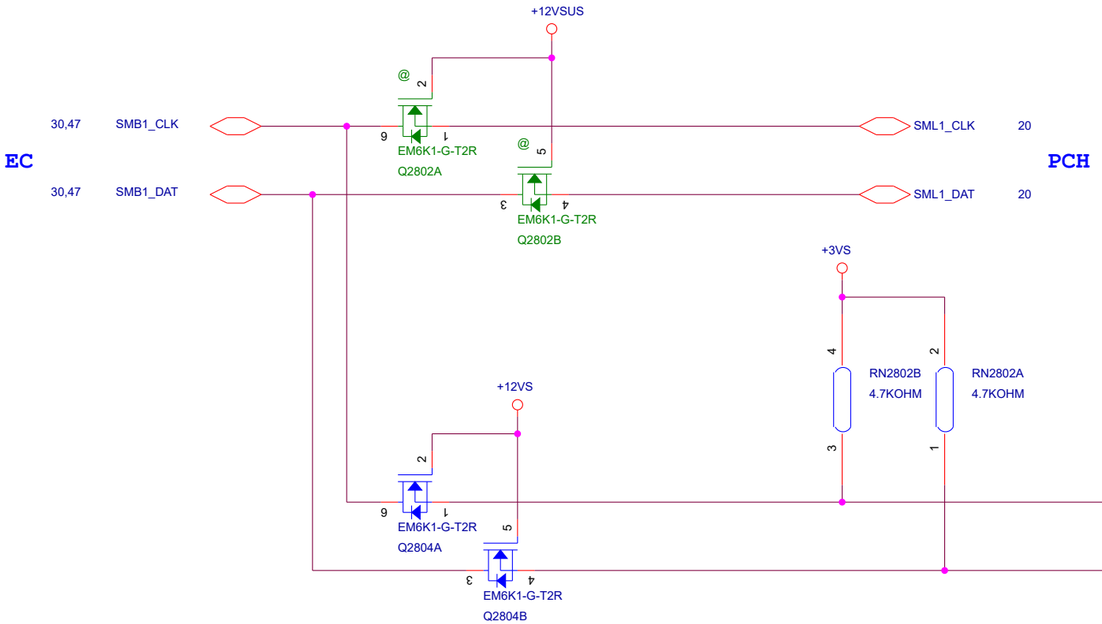
U2801_FLASH WINBOND W25Q64FVSSIQ

1st Source: P/N:05006-00010500 FLASH WINBOND W25Q64FVSSIQ

2nd Source: P/N:05006-00011600 FLASH MXIC MX25L6473EM2I-10G



System Management Interface



SMBus Interface

ASUS	Project Name: GL552VW		Rev: 2.0
Title : PCH-SPI ROM,OTH			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015		Sheet 28 of 103	

EC 8995

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

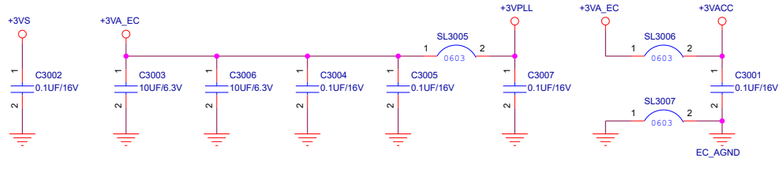
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

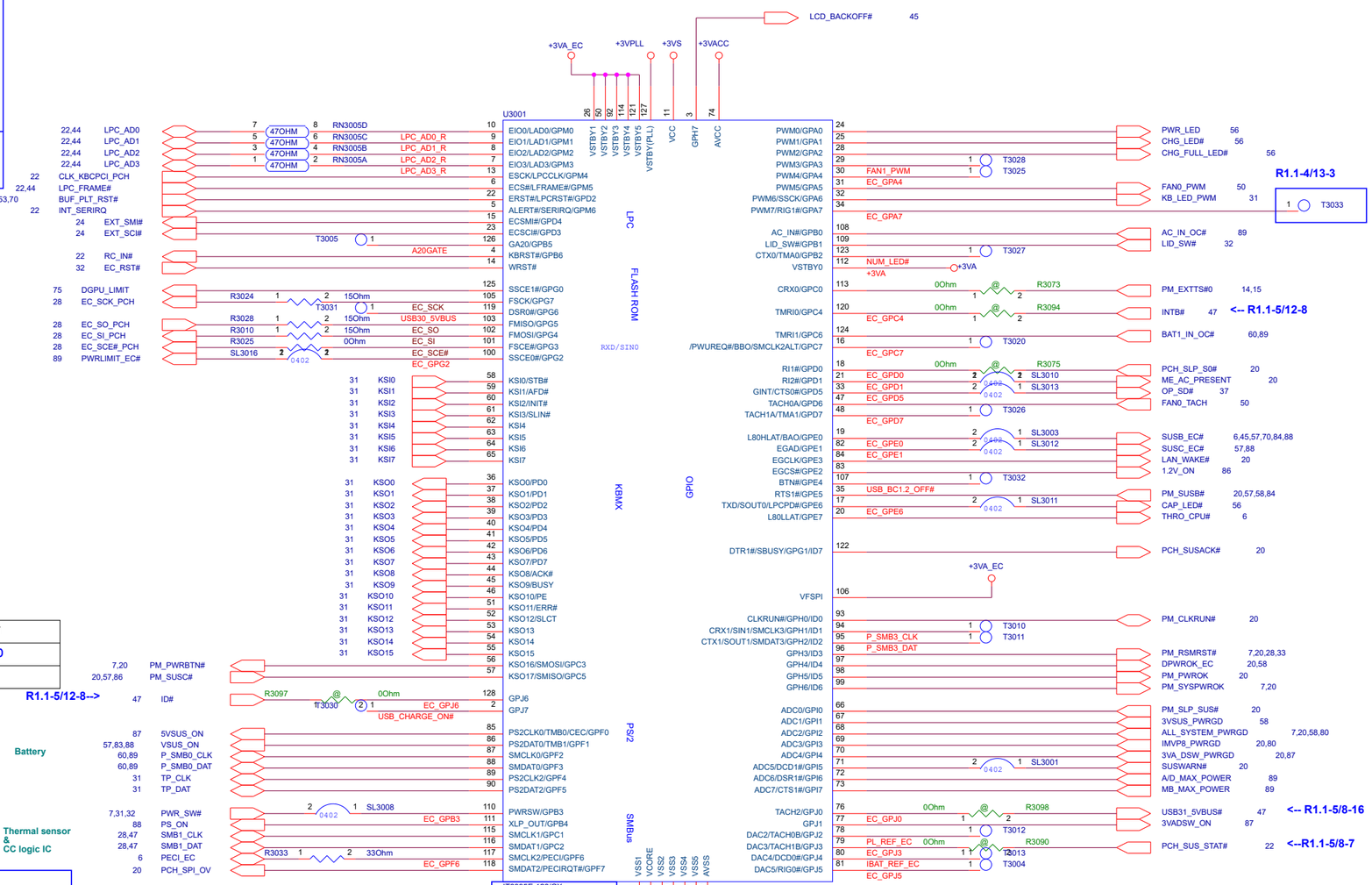
EC Require

ITE Version	ASUS P/N
IT8995E-128/CX	06037-00050500

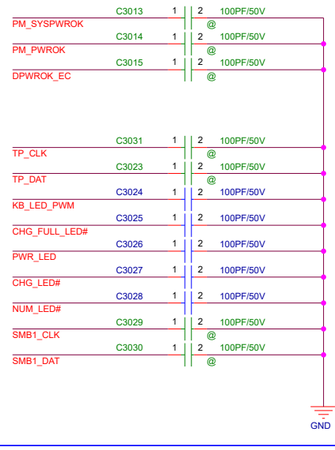
R1.1-5/12-8-->

Power

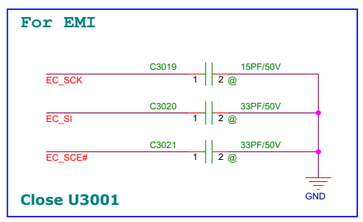




For EMI



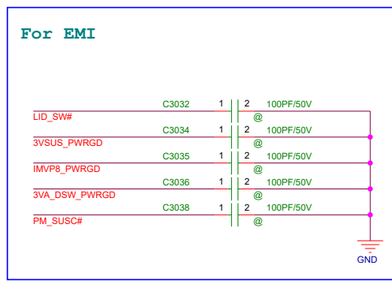
For EMI

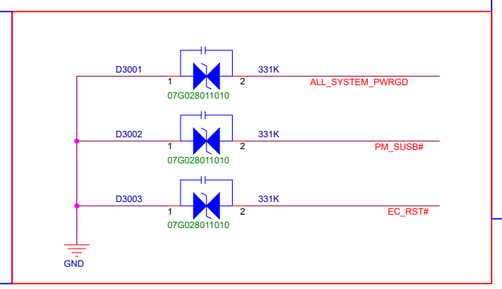


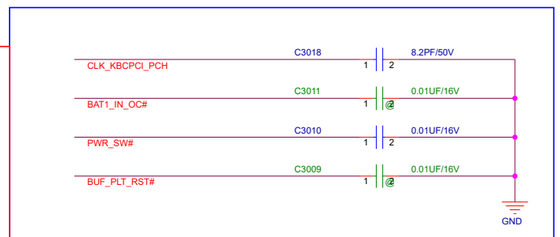
Close U3001

R2.0-6/17-3

For EMI

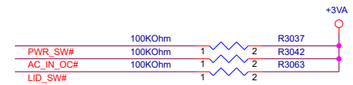


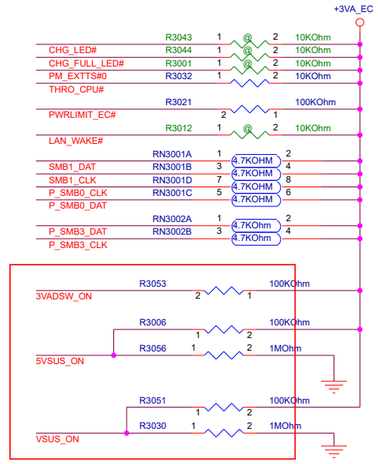


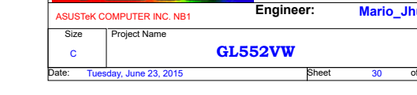


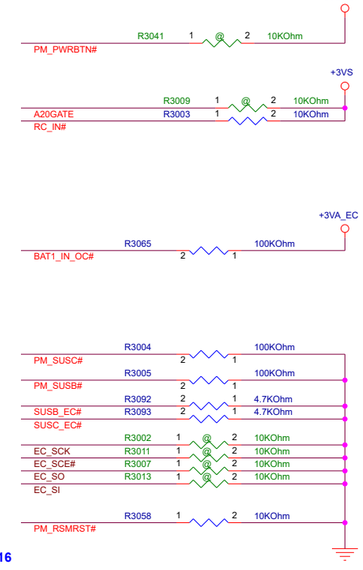
R2.0-6/17-3

PU/PD



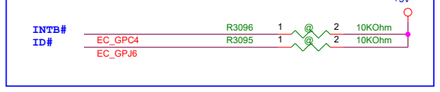






R1.1-5/8-16

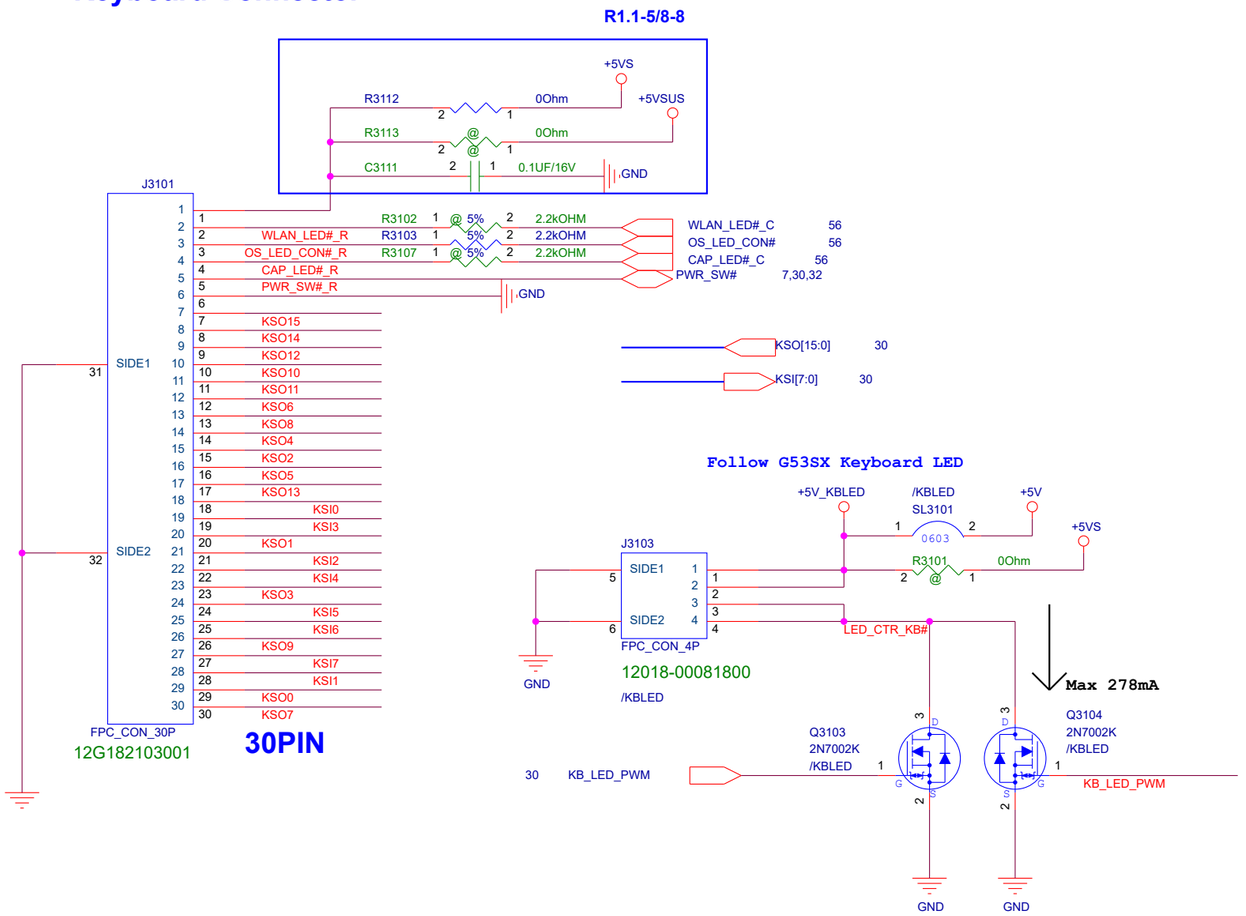
To CC logic at p. 47

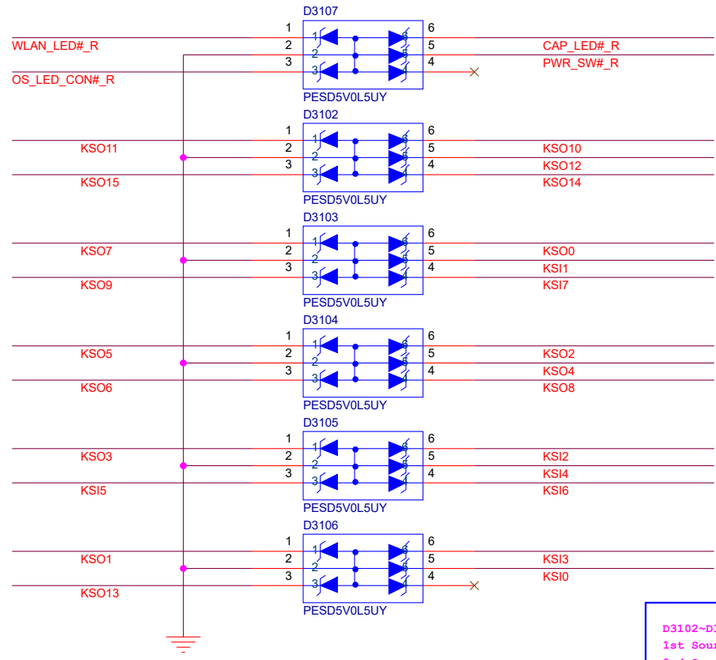


BOM

Title :	CR_KBC_IT8521
ASUSTeK COMPUTER INC. NB1	Engineer: Mario_Jhu
Size: C	Project Name: GL552VW
Rev: 2.0	
Date: Tuesday, June 23, 2015	Sheet 30 of 103

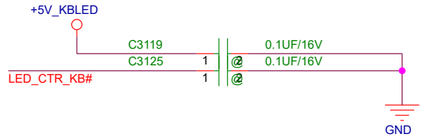
Keyboard Connector



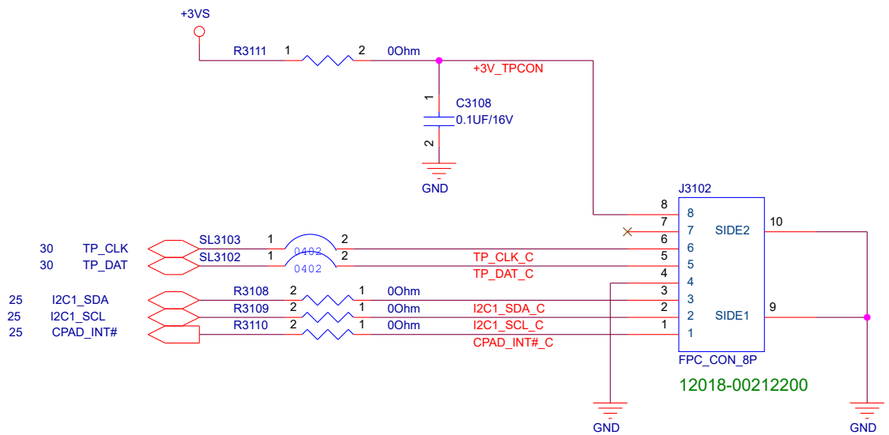


R1.1-4/13-5

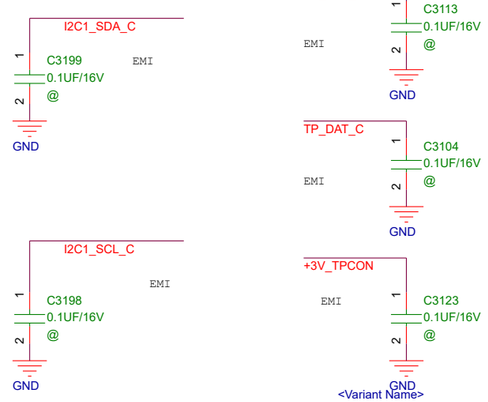
D3102~D317 ESD PROTECTION AZ2115-05C
1st Source: P/N:07G028162010 NXP SOT363
2nd Source: P/N:07G028127010 AMAZING SC70-6L



Click touch Pad Connector



Reserved for EMI

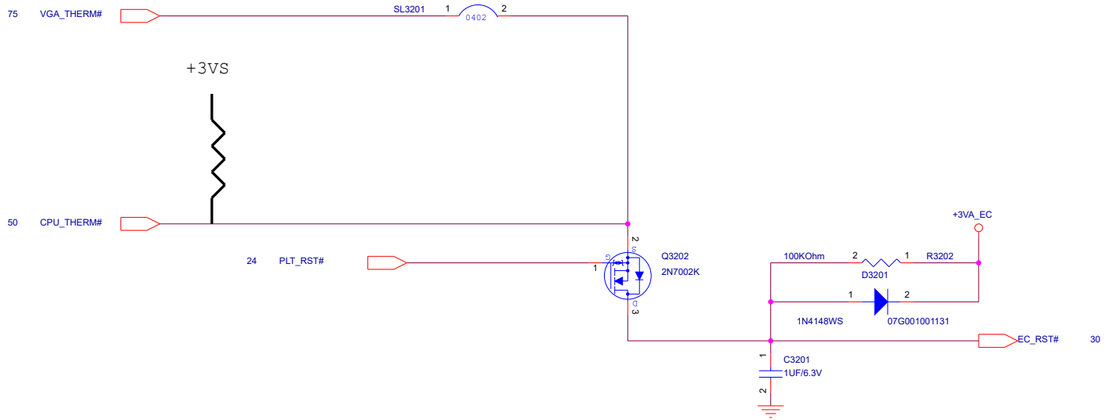


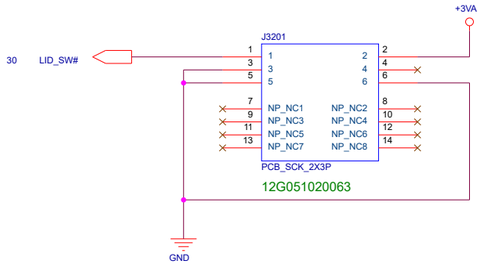
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : KBC_KB & TP	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 31 of 103	

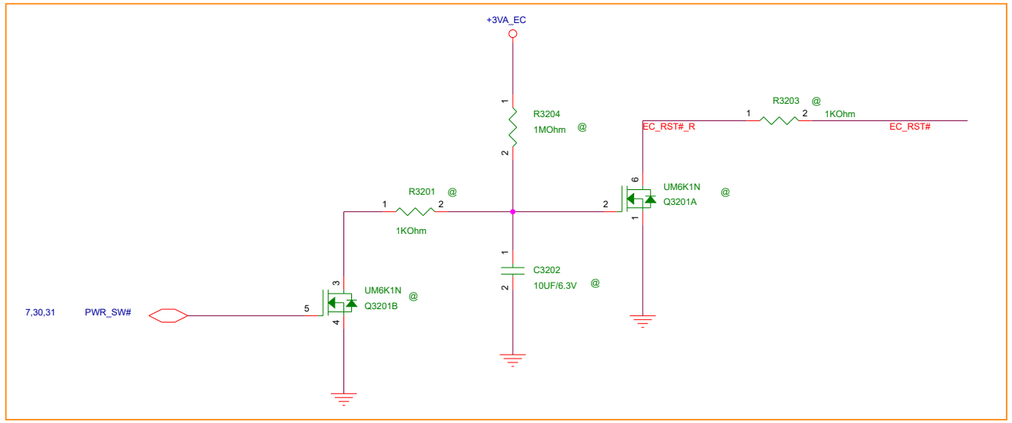
Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5006.



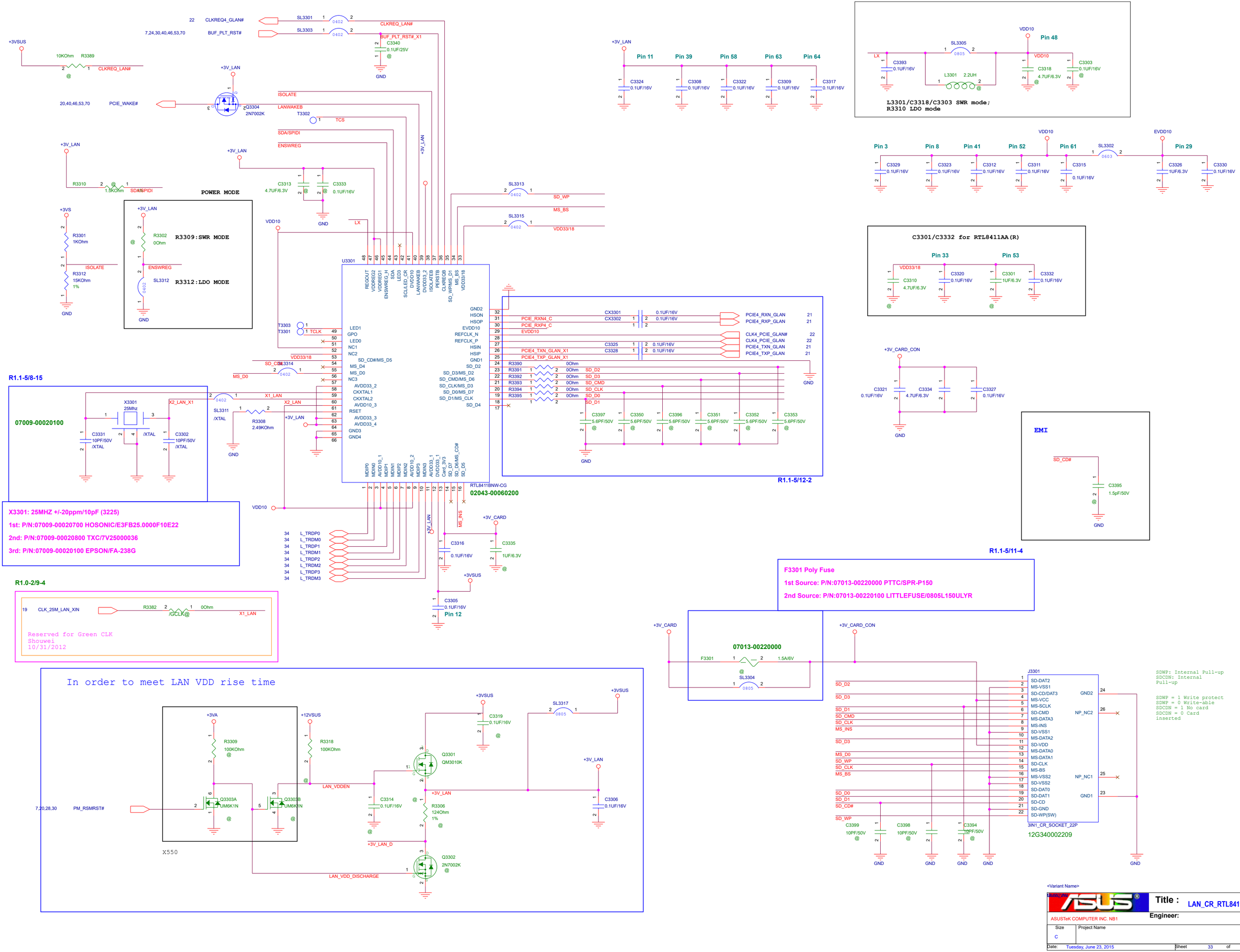


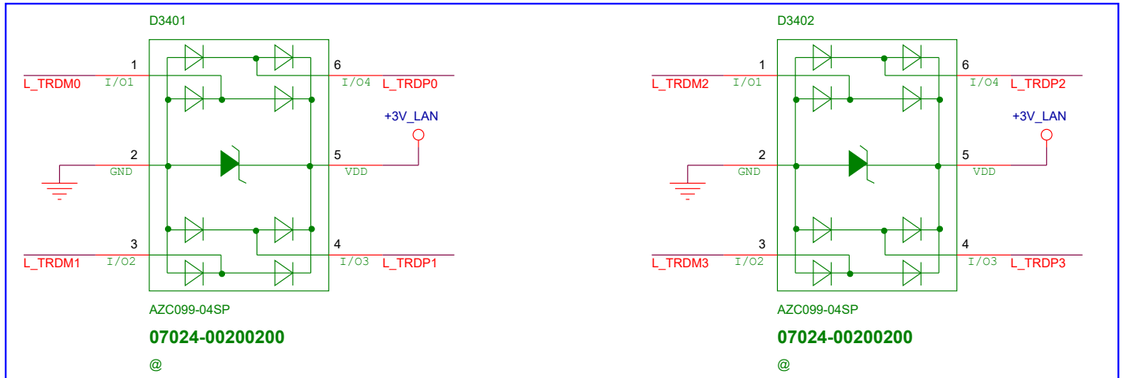
For battery embedded case (press pwr_sw 10sec, then reset ec) (need to modify)



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : RST_Reset Circuit	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 32 of 103	


22 CLKREQ4_GLAN#
SL3301 0402 CLKREQ_LAN#
7,24,30,40,46,53,70 BUF_PLT_RST#
SL3303 0402 BUF_PLT_RST#_X1
C3340 0.1UF/25V
+3VSUS
10KOhm R3389
CLKREQ_LAN#
+3V_LAN
20,40,46,53,70 PCIE_WAKE#
Q3304 2N7002K
ISOLATE
LANWAKEB
T3302 TCS
SDA/SPIDI
ENSWREG
+3V_LAN
R3310 1.5KOhm SDA/SPIDI
POWER MODE
C3313 4.7UF/6.3V
C3333 0.1UF/16V
GND
SL3313 0402 SD_WP
MS_BS
SL3315 0402 VDD33/18
+3VS
R3301 1KOhm
ISOLATE
R3312 15KOhm 1%
R3302 0Ohm
R3309:SWR MODE
ENSWREG
SL3312 0402
R3312:LDO MODE
VDD10
LX
U3301
RECOUT VDDREG2 VDDREG1 ENSWREG_H SDA LED3 SCLLED_CR DVDD10 LANWAKEB DVDD33_2 ISOLATEB PERSTB CLKREQB SD_WPMS_D1 MS_SIS VDD33/6
T3303 T3301 TCLK
LED1 GPO LED0 NC1 NC2 SD_CD#/MS_D5 MS_D4 MS_D0 NC3 AVDD33_2 CKXTAL1 CKXTAL2 AVDD10_3 RSET AVDD33_3 AVDD33_4 GND3 GND4
SD_CD#
SL3314 0402
MS_D0
VDD33/18
GND2 HSON HSOP EVDD10 REFCLK_N REFCLK_P HSIN HSIP GND1 SD_D2 SD_D3/MS_D2 SD_CMD/MS_D6 SD_CLK/MS_D3 SD_D0/MS_D7 SD_D1/MS_CLK SD_D4
MDIP0 MDIN0 AVDD10_1 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10_2 MDIP3 MDIN3 AVDD33_1 DVDD33_1 Card_3V3 SD_D7 SD_D6/MS_CD# SD_D5
RTL8411BNW-CG
02043-00060200
MS_INS
+3V_CARD
C3316 0.1UF/16V
C3335 1UF/6.3V
+3VSUS
C3305 0.1UF/16V
Pin 12
34 L_TRDP0
34 L_TRDM0
34 L_TRDP1
34 L_TRDM1
34 L_TRDP2
34 L_TRDM2
34 L_TRDP3
34 L_TRDM3
R1.1-5/8-15
07009-00020100
X3301 25Mhz
C3331 10PF/50V /XTAL
C3302 10PF/50V /XTAL
X2_LAN_X1
SL3311 /XTAL
X1_LAN
R3308 2.49KOhm
X2_LAN
+3V_LAN
GND
X3301: 25MHZ +/-20ppm/10pF (3225)
1st: P/N:07009-00020700 HOSONIC/E3FB25.0000F10E22
2nd: P/N:07009-00020800 TXC/7V25000036
3rd: P/N:07009-00020100 EPSON/FA-238G
R1.0-2/9-4
19 CLK_25M_LAN_XIN
R3382 /GCLK@ 0Ohm X1_LAN
Reserved for Green CLK
Shouwei
10/31/2012
R1.1-5/12-2
CX3301 CX3302 0.1UF/16V
PCIE_RXN4_C PCIE_RXP4_C
PCIE4_RXN_GLAN PCIE4_RXP_GLAN
EVDD10
C3325 C3328 0.1UF/16V
PCIE4_TXN_GLAN_X1 PCIE4_TXP_GLAN_X1
CLK4_PCIE_GLAN# CLK4_PCIE_GLAN
PCIE4_TXN_GLAN PCIE4_TXP_GLAN
R3390 R3391 R3392 R3393 R3394 R3395 0Ohm
SD_D2 SD_D3 SD_CMD SD_CLK SD_D0 SD_D1
C3397 C3350 C3396 C3351 C3352 C3353 5.6PF/50V
+3V_LAN
Pin 11 Pin 39 Pin 58 Pin 63 Pin 64
C3324 C3308 C3322 C3309 C3317 0.1UF/16V
L3301/C3318/C3303 SWR mode;
R3310 LDO mode
SL3305 0805
LX C3393 0.1UF/16V
L3301 2.2UH
VDD10 Pin 48
C3318 4.7UF/6.3V
C3303 0.1UF/16V
Pin 3 Pin 8 Pin 41 Pin 52 Pin 61
C3329 C3323 C3312 C3311 C3315 0.1UF/16V
SL3302 0603
EVDD10 Pin 29
C3326 1UF/6.3V
C3330 0.1UF/16V
C3301/C3332 for RTL8411AA(R)
Pin 33 Pin 53
VDD33/18
C3310 4.7UF/6.3V
C3320 C3301 C3332 0.1UF/16V
1UF/6.3V
+3V_CARD_CON
C3321 C3334 C3327 0.1UF/16V
4.7UF/6.3V
EMI
SD_CD#
C3395 1.5pF/50V
R1.1-5/11-4
F3301 Poly Fuse
1st Source: P/N:07013-00220000 PTTC/SPR-P150
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR
+3V_CARD
07013-00220000
F3301 1.5A/6V
SL3304 0805
+3V_CARD_CON
J3301
SD_D2 SD_D3 SD_D1 SD_CMD SD_CLK MS_INS SD_D3 MS_D0 SD_WP SD_CLK MS_BS SD_D0 SD_D1 SD_CD# SD_WP
SD-DAT2 MS-VSS1 SD-CD/DAT3 MS-VCC MS-SCLK SD-CMD MS-DATA3 MS-INS SD-VSS1 MS-DATA2 SD-VDD MS-DATA0 MS-DATA1 SD-CLK MS-BS MS-VSS2 SD-VSS2 SD-DAT0 SD-DAT1 SD-CD SD-GND SD-WP(SW)
GND2 NP_NC2 NP_NC1 GND1
C3399 C3398 C3394 10PF/50V
3IN1_CR_SOCKET_22P
12G340002209
SDWP: Internal Pull-up
SDCDN: Internal Pull-up
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted
In order to meet LAN VDD rise time
+3VA +12VSUS +3VSUS
R3309 100KOhm
R3318 100KOhm
Q3303A UM6K1N
Q3303B UM6K1N
7,20,28,30 PM_RSMRST#
LAN_VDDEN
C3319 0.1UF/16V
SL3317 0805
Q3301 QM3010K
C3314 0.1UF/16V
R3306 124Ohm 1%
C3306 0.1UF/16V
+3V_LAN_D
Q3302 2N7002K
LAN_VDD_DISCHARGE
X550

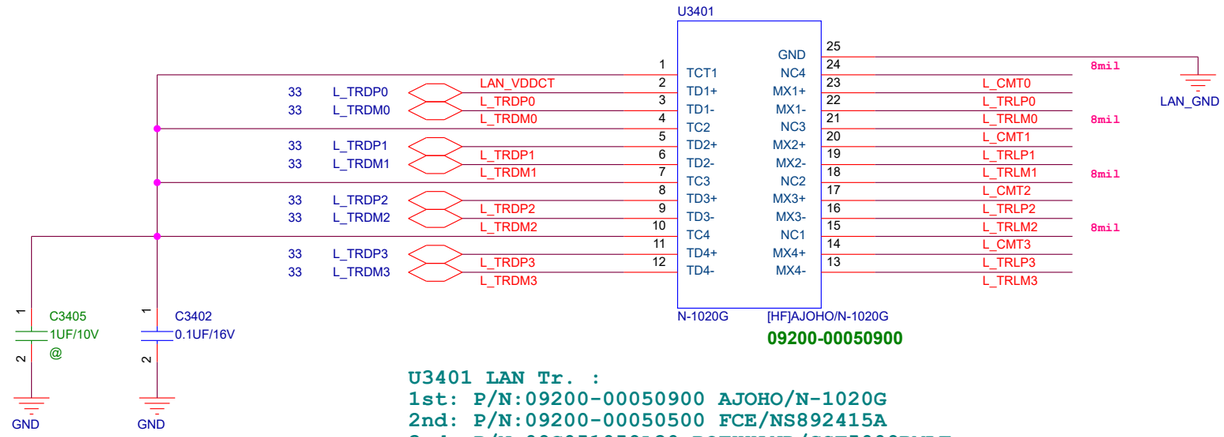


R1.1-4/13-5

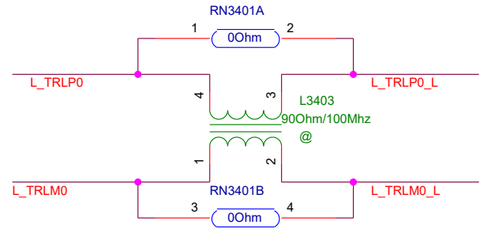
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

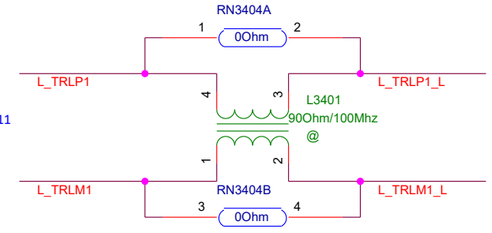


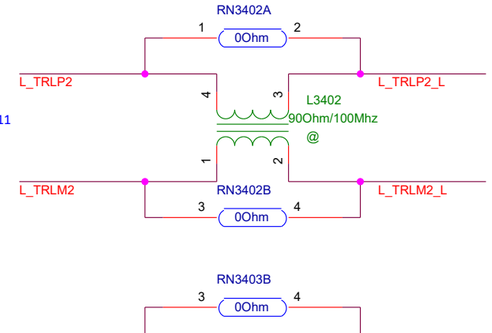
U3401 LAN Tr. :
1st: P/N:09200-00050900 AJOHO/N-1020G
2nd: P/N:09200-00050500 FCE/NS892415A
3rd: P/N:09G051059A20 BOTHHAND/GST5009BMLF



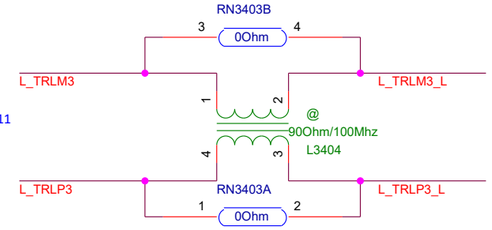
R1.0-5

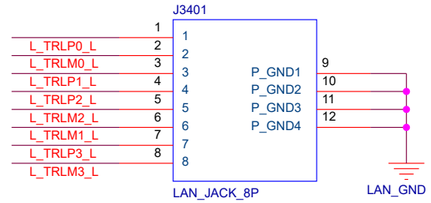
SWAP_20140211





SWAP_20140211

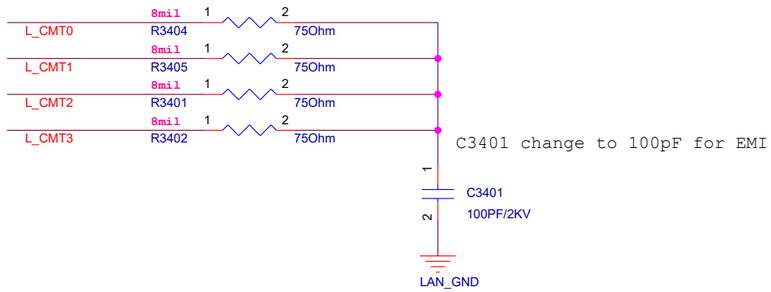


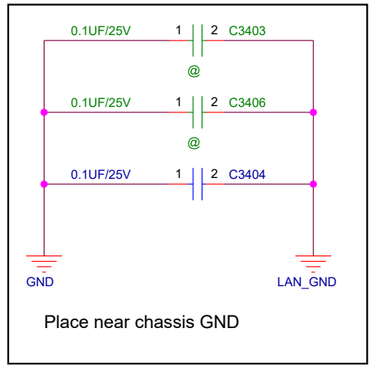


Change GND TO LAN_GND FOR EMI

Test Point_LAN Tr.

拿掉ATE測點, 改由layout主動加





<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : LAN RJ45		
	Engineer: Mario_Jhu		
Size: B	Project Name: GL552VW		Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 34 of 103		

Pin_27 is 3.3V output form internal LDO

C3616 place clode Pin18

R2.0-6/9-4

R1.1-5/11-3

R1.1-5/11-3

R1.1:EE change Part
C3601, C3604, C3612, C3615

GND_AUDIO

GND

R0.14. Item 2.
Add snubber networks for class-d outputs,

ANALOG

For EMI

R1.1. Item 4. Change 0 ohm resistor for analog and digital ground. If EMI test ok, 0 ohm resistor can be replaced by short land for your project.

DETECTION

CLASSD_MONO_EN
Mount R3612 support class-D mono mode(Left speaker)

PORTC_MONO_EN
1.mount R3603 for A-MIC mono support(PORTC_L).
2.Support D-MIC unmount R3603

R0.14. Item 1.
Delete R3610 20k ohm that don't use this Resistor to detect universal jack.

HGNDA/HGNDB 走線70 mil

Headphone:Port A
External MIC:Port B
Internal MIC:Port C
Headset:Port A + port D

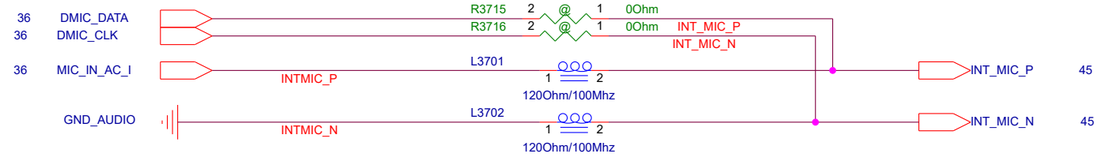
TO EXTERNAL MIC(Port B)

TO INTERNAL MIC(Port C)

R0.14. Item 3.
Chang C3618~3622 1uF/Y5V to 2.2uF/X5R for MIC THD+N dynamic test.

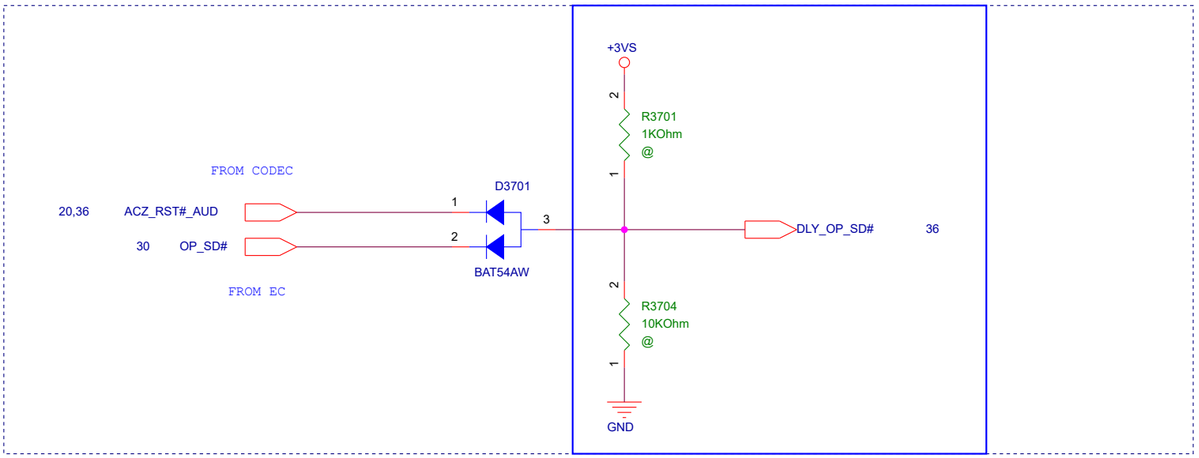
Title :	AUDIO_CX20752_R1.3
Engineer:	Mario_Jhu
ASUSTeK COMPUTER INC. NB1	
Size: C	Project Name: GL552VW
Rev: 2.0	
Date: Tuesday, June 23, 2015	Sheet 36 of 103

INTERNAL MICROPHONE



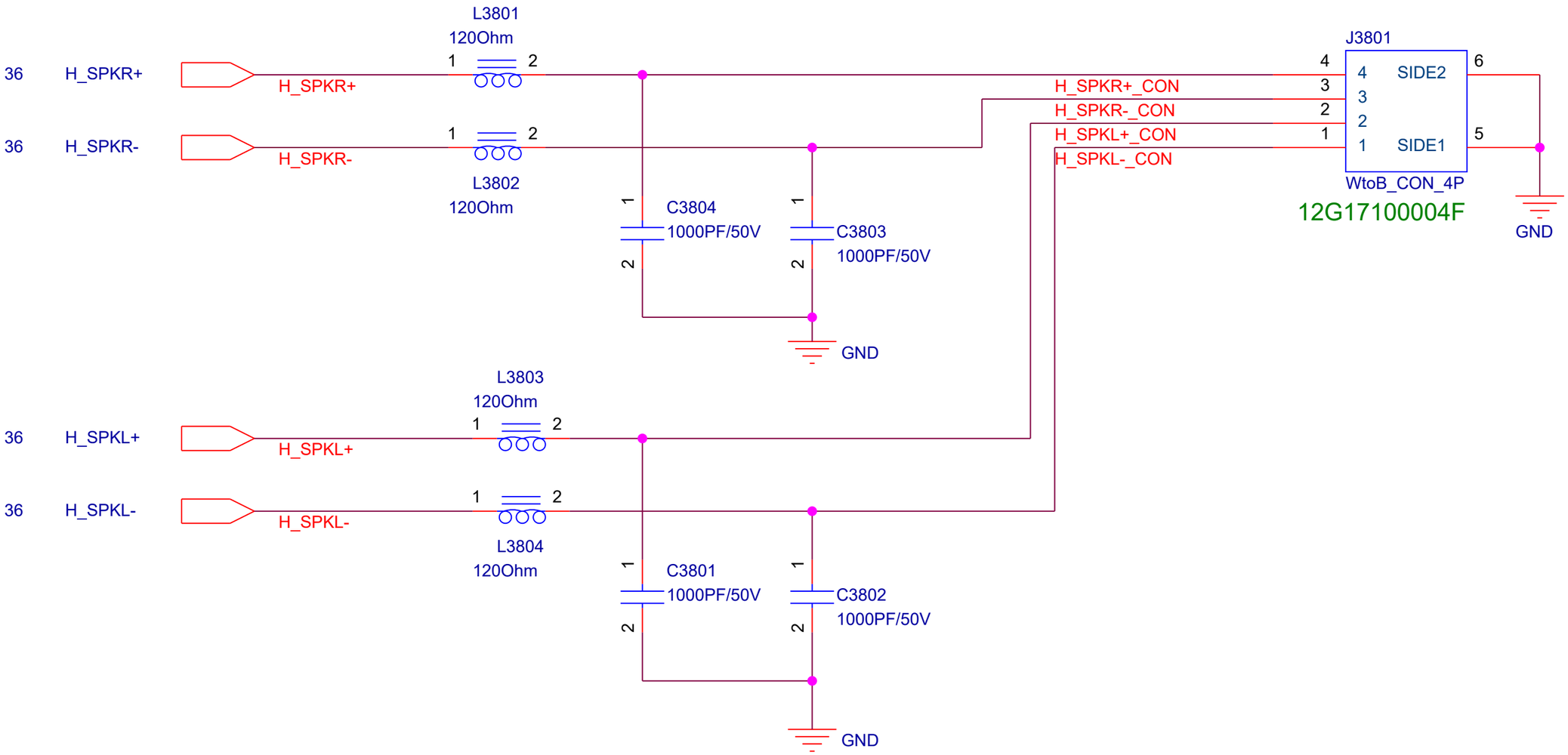
MUTE CONTROL

R1.1-5/12-9



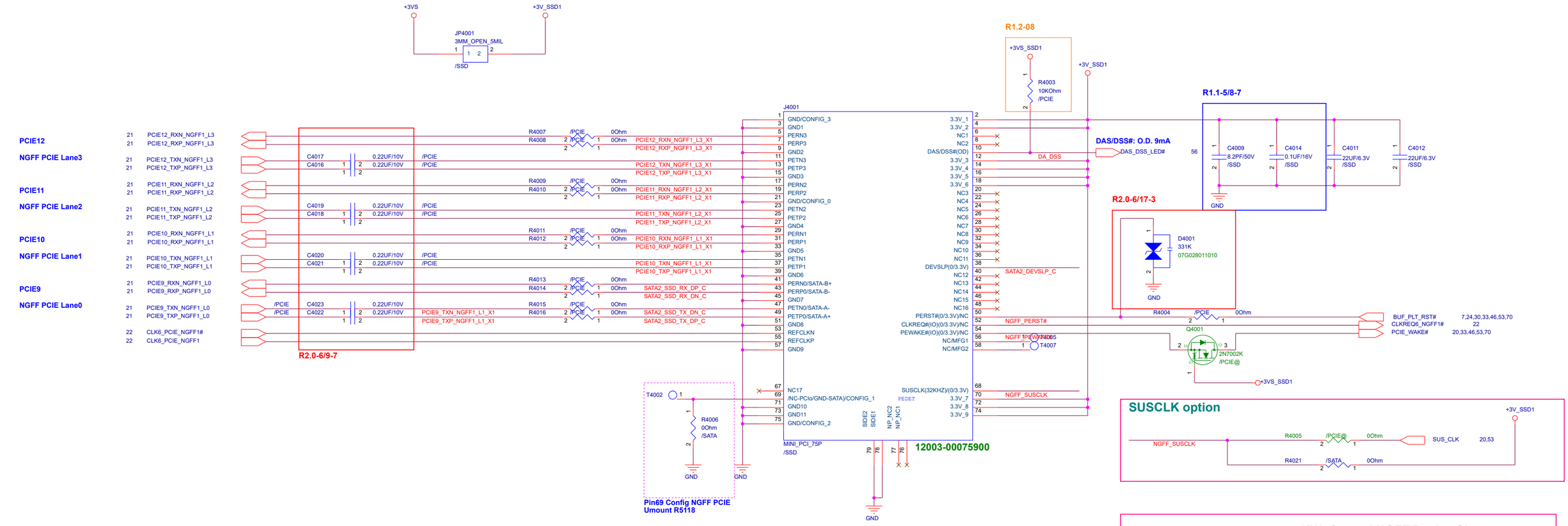
ASUSTeK COMPUTER INC. NB1	Title : AUD-AMP		
	Engineer: Mario_Jhu		
Size: B	Project Name: GL552VW		Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 37 of 103		

Mount C3801~C3804 and change SL to
L3801~L3804 in ER 20141121



ASUSTeK COMPUTER INC. NB1	Title : AUD-MIC-IN__R1.4	
	Engineer: Mario_Jhu	
Size: A	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 38 of 103	

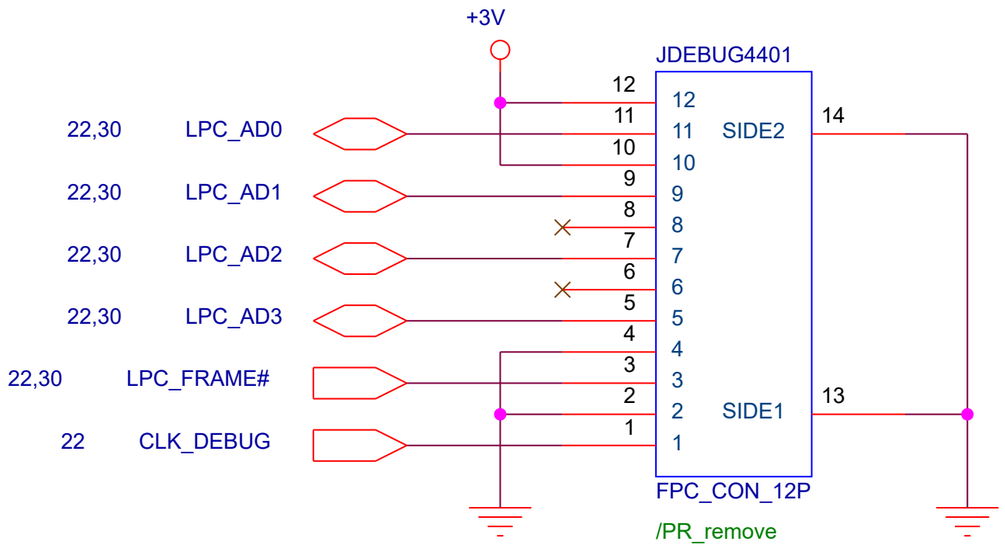
NGFF_SSD



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : MiniCard_SSD	
	Engineer: Mario_Jhu	
Size: C	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 40 of 103	

LPC Debug Port



12018-00102900

R1.1-4/13-5

JDEBUG4401 Connector (NPI USE)

1st Source: P/N:12018-00102900 ENTERY/6705K-Y12N-20L

2nd Source: P/N:12018-00103000 ACES/51578-01201-002

R1.1-4/13-5

JDEBUG4401 Connector (MP USE)

1st Source: P/N:12018-00102400 P-TWO/196479-12041-3

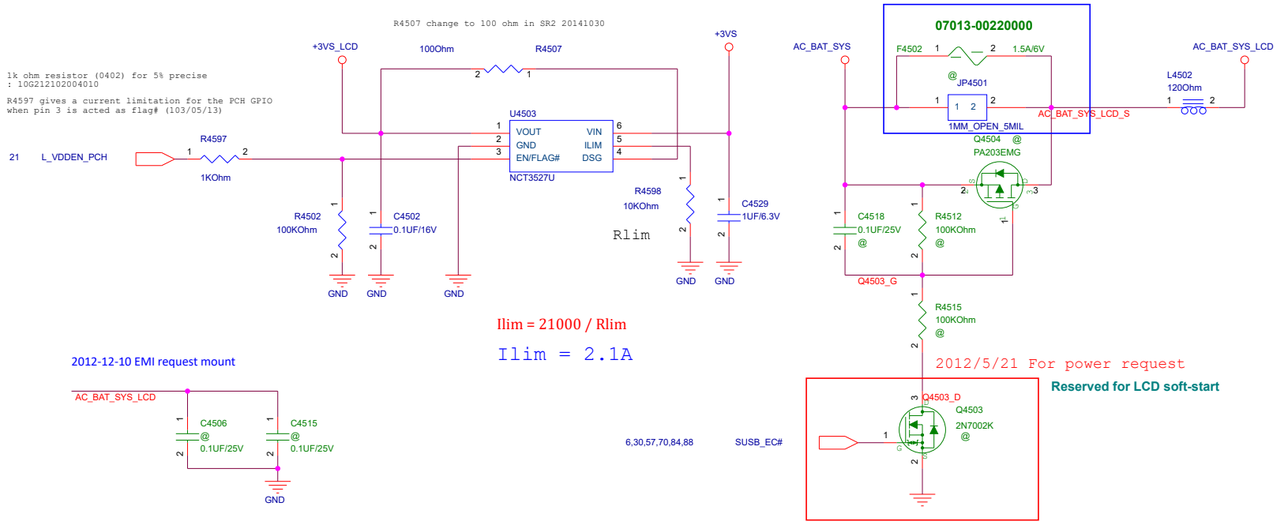
2nd Source: P/N:12018-00102100 ENTERY/6705K-Y12N-00L

3rd Source: P/N:12018-00102300 ACES/51578-01201-001

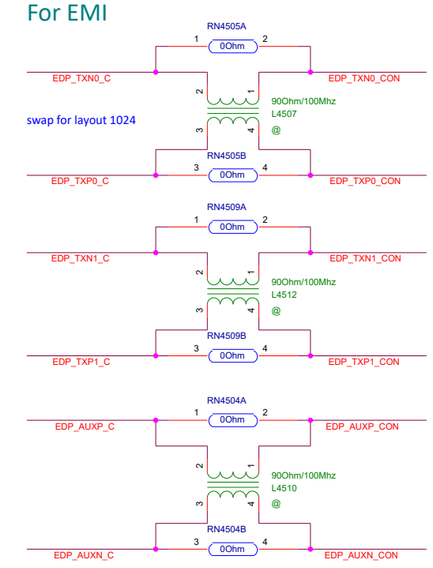
<Variant Name>

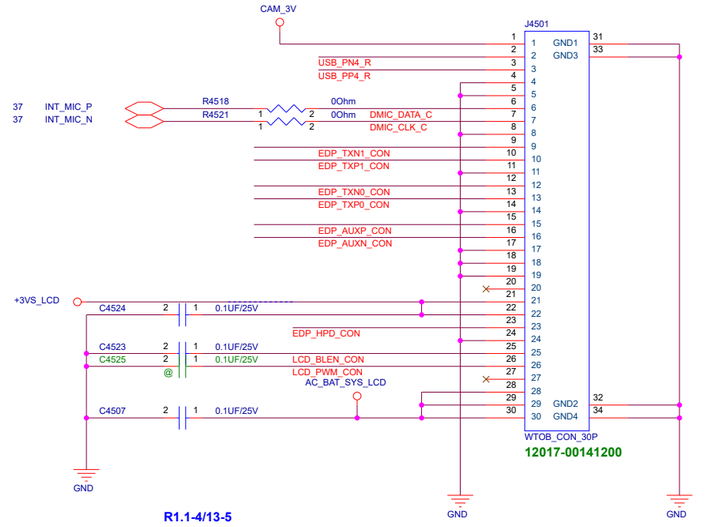
ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC	
	Engineer: Mario_Jhu	
Size: A	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 44 of 103	

LCD Power switch



For EMI





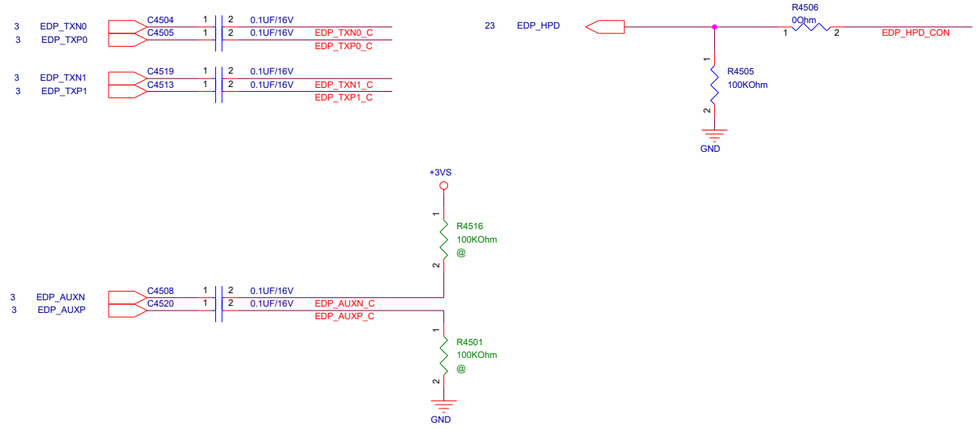
R1.1-4/13-5

J4501 WtoB CON 30P 0.5MM 1.0H RA SMT

1st Source: P/N:12017-00141200 STARCONN/300E30-0010RA-G3

2nd Source: P/N:12017-00141100 ACES/51473-0300M-001

eDP from CPU



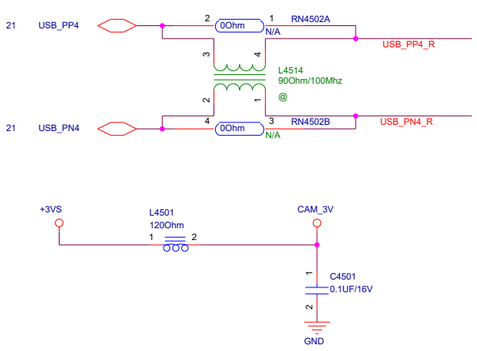
R1.1-5/11-4

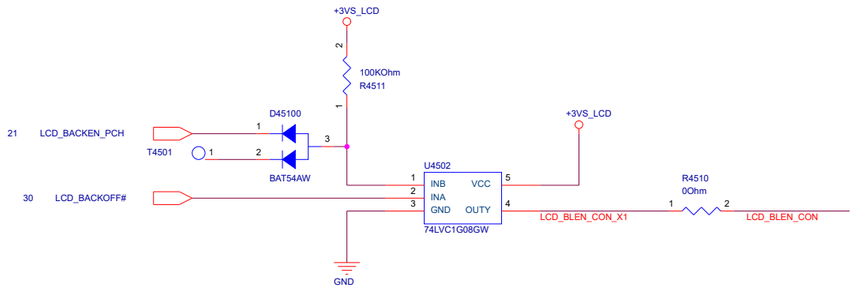
F4502 Poly Fuse

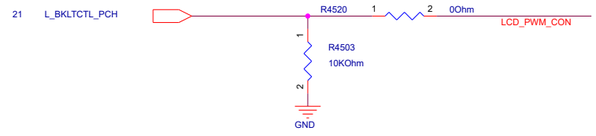
1st Source: P/N:07013-00220000 PTTC/SPR-P150

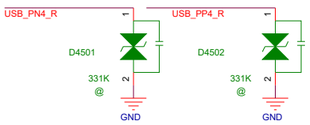
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR

Camera module

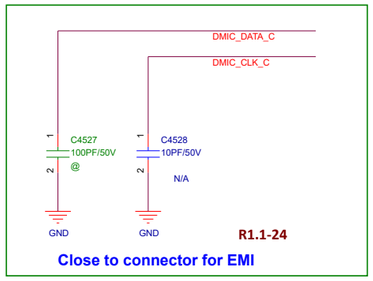






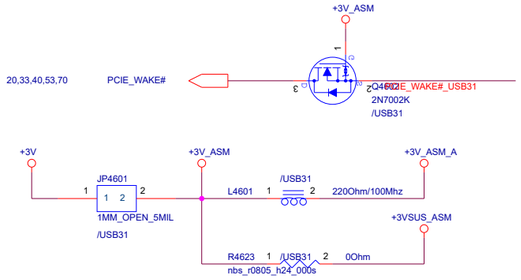


R1.2-8 R1.2-9

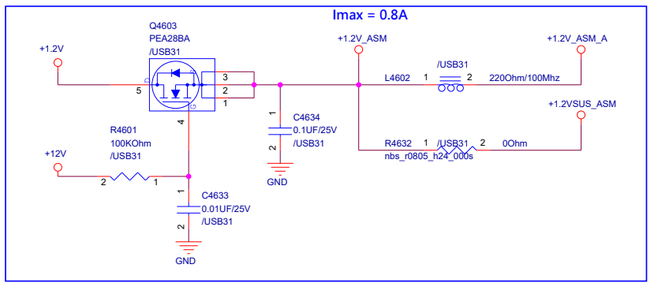


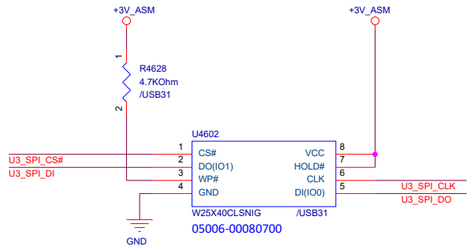
<variant_name>

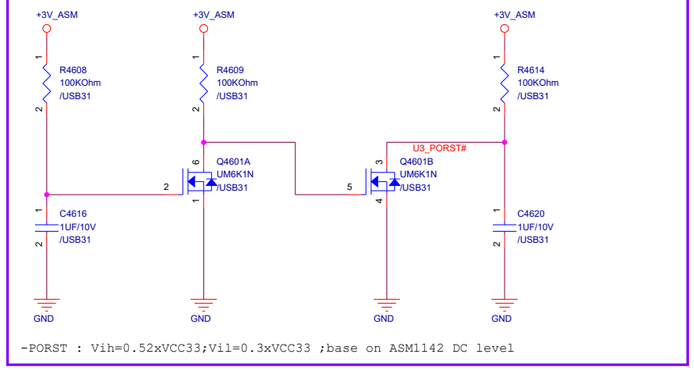
ASUSTeK COMPUTER INC. NB1	Title : CRT_eDP	
	Engineer: Mario_Jhu	
Size: C	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 45 of 103	



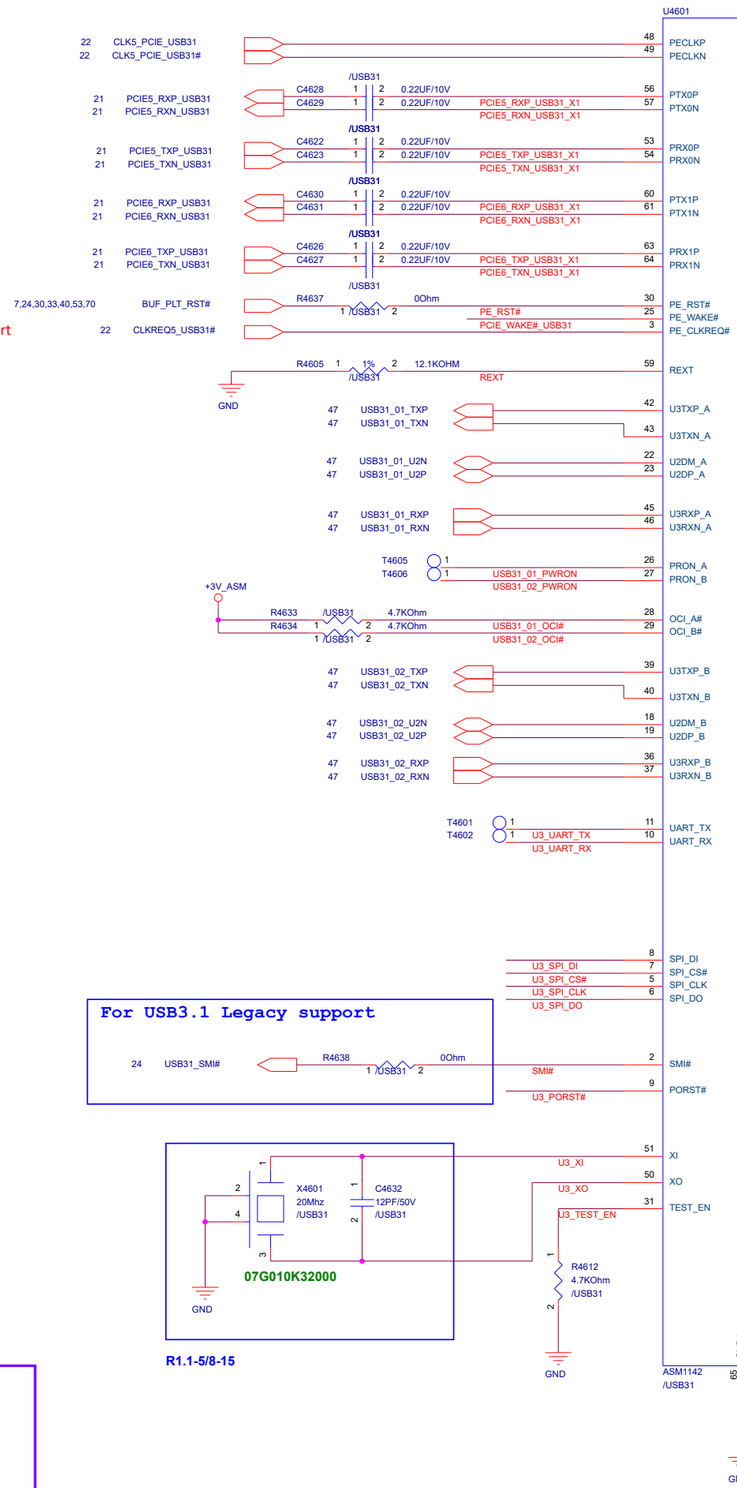
R1.1-5/12-3

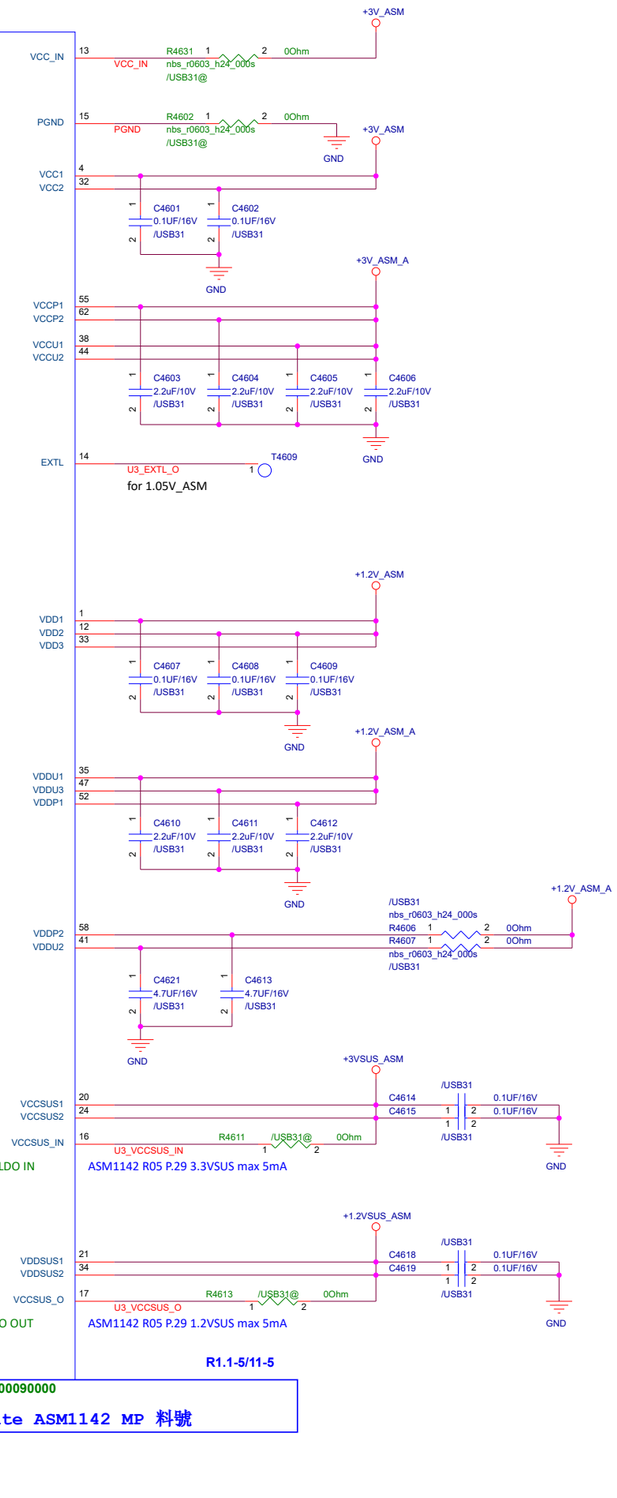






CLKREQ 目前ASM1142不support，在PCH做PD





R1.1-5/11-5

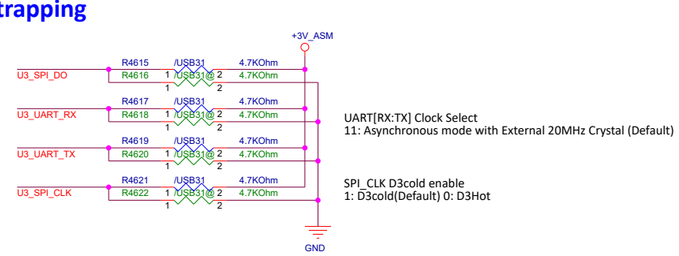
For USB3.1 Legacy support

R1.1-5/8-15

06050-00090000

Update ASM1142 MP 料號

H/W Strapping



UART[RX:TX] Clock Select
11: Asynchronous mode with External 20MHz Crystal (Default)

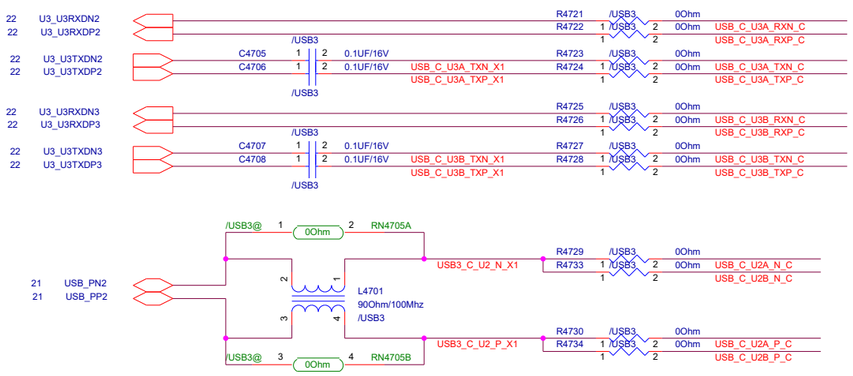
SPI_CLK D3cold enable
1: D3cold(Default) 0: D3Hot

X4602 ASM 確認用料

07G010K32000	XTAL 20MHZ SMD 16PF/10PPM//SIWARD/XTL571100-G47-085	Siward	希華
07G010242000	XTAL 20MHZ 3.2*2.5 16PF/10PPM//TXC/7M20000061	TXC	台灣晶技
07009-00080800	XTAL 20MHZ SMD 16PF/10PPM SKCTECH/FSK3M200000M161	SKC	鑫谷

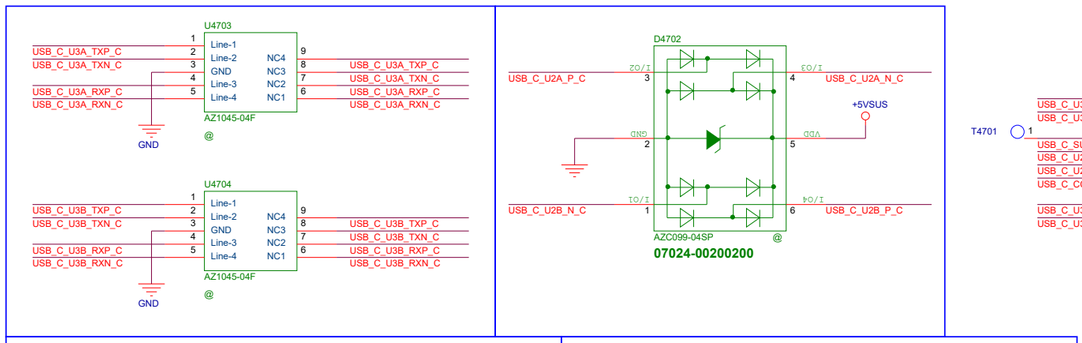
Project Name: GL552VW		Rev: 2.0
Title : USB 3.1 ASM1142		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 46 of 103	

PCH USB3.0



Type C Con. & USB3.0 EMI protect

R1.1-5/12-4



U4703 & U4704 ESD PROTECTION

1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

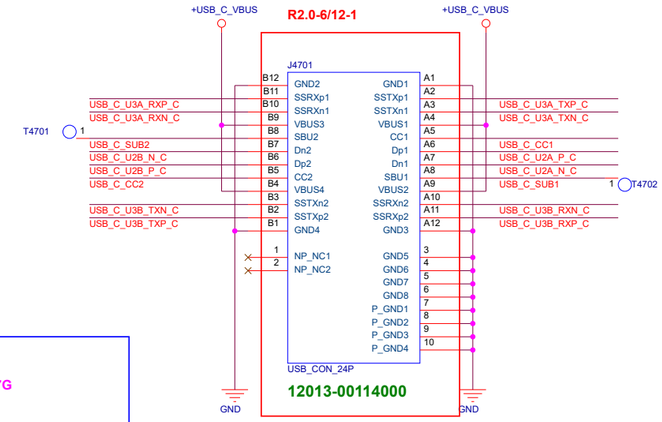
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

D4702 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

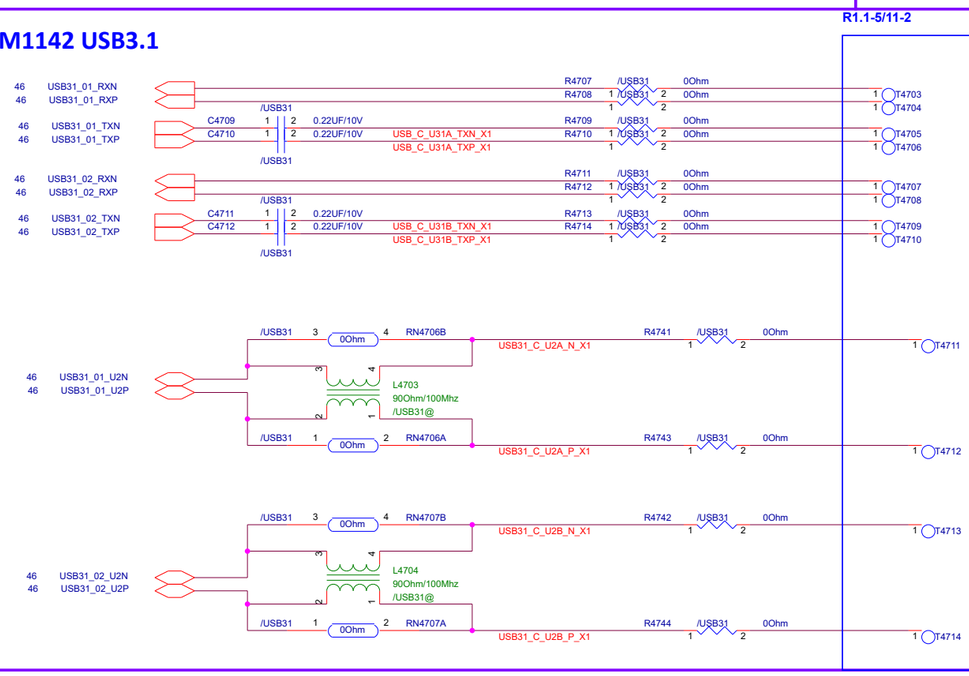
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

R2.0-6/12-1



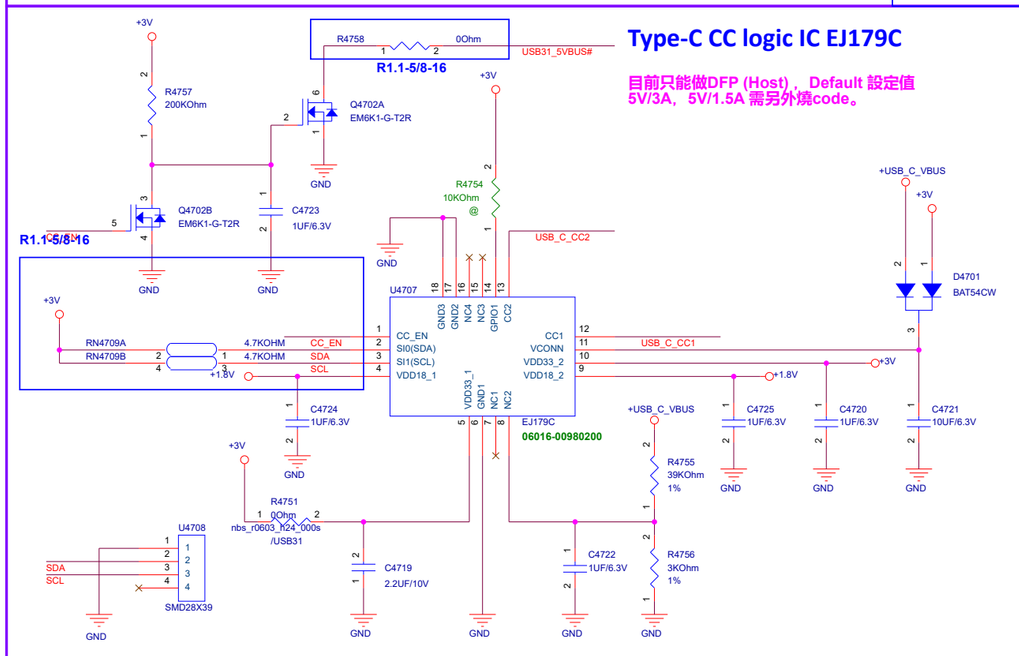
ASM1142 USB3.1

R1.1-5/11-2



Type-C CC logic IC EJ179C

目前只能做DFP (Host)，Default 設定值
5V/3A，5V/1.5A 需另外燒code。

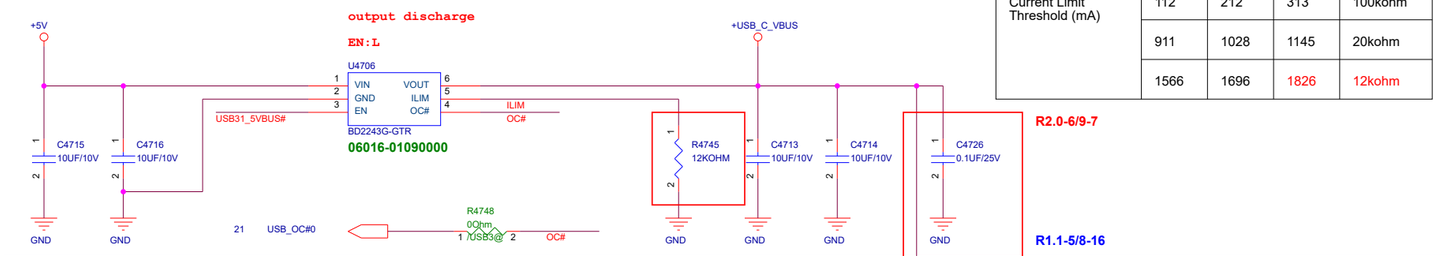


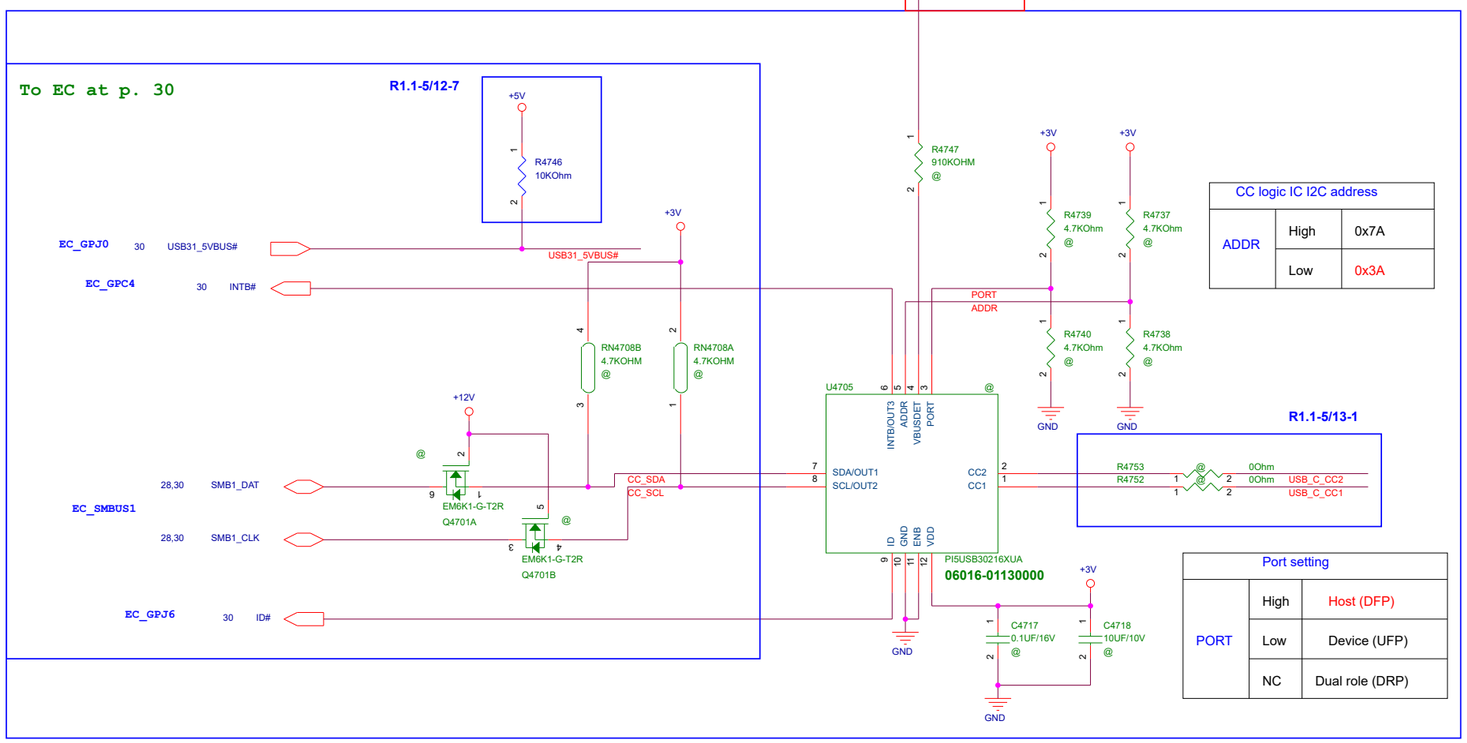
Type-C CC logic IC PI5USB30216 & VBUS POWER Switch

Current Limit Threshold (mA)	Min	Typ	Max	R4745
	112	212	313	100kohm
	911	1028	1145	20kohm
	1566	1696	1826	12kohm

R2.0-6/9-7

R1.1-5/8-16





CC logic IC I2C address		
ADDR	High	0x7A
	Low	0x3A

Port setting		
PORT	High	Host (DFP)
	Low	Device (UFP)
	NC	Dual role (DRP)

<Variant Name>

ASUS	Project Name: GL552VW	Rev: 2.0
Title : USB 3.1 MB Type-C		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 47 of 103	

CPU DDIC

3 DDI2_TXN3_HDMI_CLK
3 DDI2_TXP3_HDMI_CLK
C4808 0.1UF/16V
C4804 1 2 0.1UF/16V HDMI_CLK-
1 2 HDMI_CLK+

3 DDI2_TXP1_HDMI
3 DDI2_TXN1_HDMI
C4812 0.1UF/16V
C4807 1 2 0.1UF/16V HDMI_TX1+
1 2 HDMI_TX1-

3 DDI2_TXN0_HDMI
3 DDI2_TXP0_HDMI
C4803 0.1UF/16V
C4806 1 2 0.1UF/16V HDMI_TX0-
1 2 HDMI_TX0+

3 DDI2_TXP2_HDMI
3 DDI2_TXN2_HDMI
C4801 0.1UF/16V
C4802 1 2 0.1UF/16V HDMI_TX2+
1 2 HDMI_TX2-

+3VS
Q4803
2N7002K
R4805 1 1% 2 470Ohm HDMI_CLK-
R4824 1 1% 2 470Ohm HDMI_CLK+
R4808 1 1% 2 470Ohm HDMI_TX0-
R4811 1 1% 2 470Ohm HDMI_TX0+
R4813 1 1% 2 470Ohm HDMI_TX1-
R4815 1 1% 2 470Ohm HDMI_TX1+
R4817 1 1% 2 470Ohm HDMI_TX2-
R4821 1 1% 2 470Ohm HDMI_TX2+
GND

R1.0-2

R4809 2 1 0Ohm HDMI_CLK+ HDMI_CLKP_CON
SWAP_20140211
LX4802 90Ohm/100Mhz @
R4812 2 1 0Ohm HDMI_CLK- HDMI_CLKN_CON

R4816 2 1 0Ohm HDMI_TX0- HDMI_TXN0_CON
SWAP_20140210
@ 90Ohm/100Mhz LX4803
R4819 2 1 0Ohm HDMI_TX0+ HDMI_TXP0_CON

R4825 2 1 0Ohm HDMI_TX1- HDMI_TXN1_CON
SWAP_20140211
LX4804 90Ohm/100Mhz @
R4801 2 1 0Ohm HDMI_TX1+ HDMI_TXP1_CON

R4803 2 1 0Ohm HDMI_TX2- HDMI_TXN2_CON
@ 90Ohm/100Mhz LX4801
R4806 2 1 0Ohm HDMI_TX2+ HDMI_TXP2_CON

R1.1-17

U4802
HDMI_TXP2_CON 1 Line-1 NC4 9
HDMI_TXN2_CON 2 Line-2 NC3 8 HDMI_TXP2_CON
HDMI_TXP1_CON 3 GND NC2 7 HDMI_TXN2_CON
HDMI_TXN1_CON 4 Line-3 NC1 6 HDMI_TXP1_CON
5 Line-4 5 HDMI_TXN1_CON
AZ1045-04F @
GND

U4801
HDMI_CLKN_CON 1 Line-1 9
HDMI_CLKP_CON 2 Line-2 NC4 8 HDMI_CLKN_CON
HDMI_TXN0_CON 3 GND NC3 7 HDMI_CLKP_CON
HDMI_TXP0_CON 4 Line-3 NC2 6 HDMI_TXN0_CON
5 Line-4 NC1 HDMI_TXP0_CON
AZ1045-04F @
GND

U4801 & U4802 ESD PROTECTION

1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

R1.1-4/13-5

+5VS_HDMI
RN4801A 2.2KOHM
RN4801B 2.2KOHM
+3VS
Q4804A UM6K31N
Q4804B UM6K31N
23 DDPC_SCL_PCH
23 DDPC_SDA_PCH
HDMI_SCL_CON1_R
HDMI_SDA_CON1_R
HDMI_SCL_CON
HDMI_SDA_CON
C4810 22PF/25V @
C4805 22PF/25V @

+3VS
Q4802 PMBS3904
R4822 150KOHM
HDMI_HPD1
HDMI_HPD_CON
C4811 0.1UF/10V @
23 DDI2_HDMI_HPD1
DDI2_HDMI_HPD1
R4826 10KOhm
GND

+12VS
R4820 100KOhm
+5VS
Q4801 AP2304GN
+5VS_F
F4801 0.75A/6V
07013-00100000
+5VS_HDMI_1
SL4814 0603
+5VS_HDMI
C4809 0.1UF/16V
JP4801 1MM_OPEN_5MIL @

F4801
Main: 07013-00100000
2nd : 07013-00060200

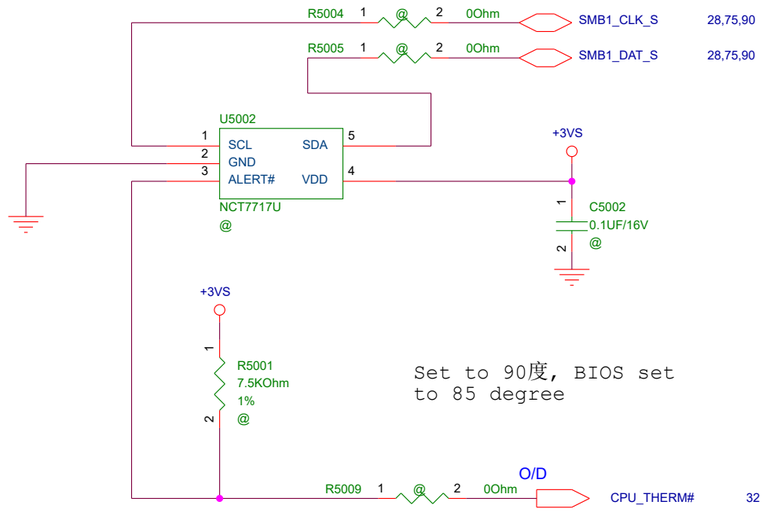
J4801
HDMI_TXP2_CON 1
HDMI_TXN2_CON 3
HDMI_TXP1_CON 4
HDMI_TXN1_CON 6
HDMI_TXP0_CON 7
HDMI_TXN0_CON 9
HDMI_CLKP_CON 10
HDMI_CLKN_CON 12
HDMI_SCL_CON 15
HDMI_SDA_CON 16
+5VS_HDMI 18
HDMI_HPD_CON 19
P_GND2 21
P_GND4 23
P_GND3 22
P_GND1 20
HDMI_CON_19P
12022-00047400

12/21/11
For HDMI Design IP R1.4
Del D4801
Add Q4803 07G005047212
F4801=>07G014075310
L4802=>09G013120802

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : HDMI	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 48 of 103	

CPU Thermal Sensor

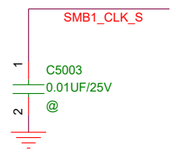


Set to 90度, BIOS set to 85 degree

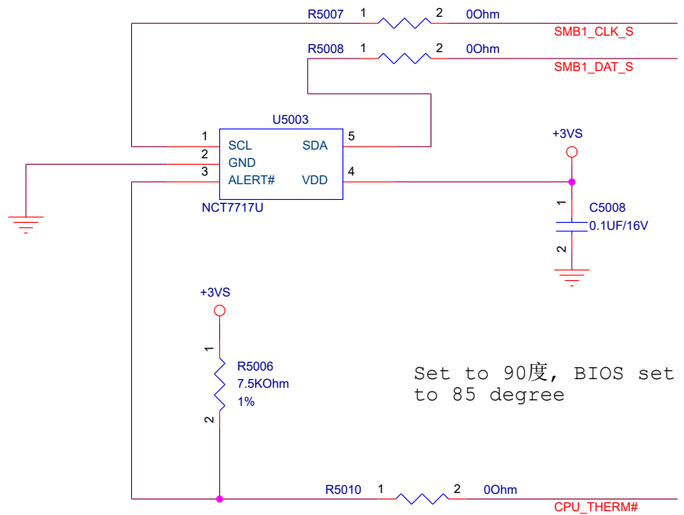
SMBUS address=10010000 (90)

Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for powr noise



SSD Thermal Sensor Test

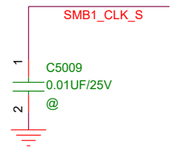


Set to 90度, BIOS set to 85 degree

SMBUS address=10010000 (90)

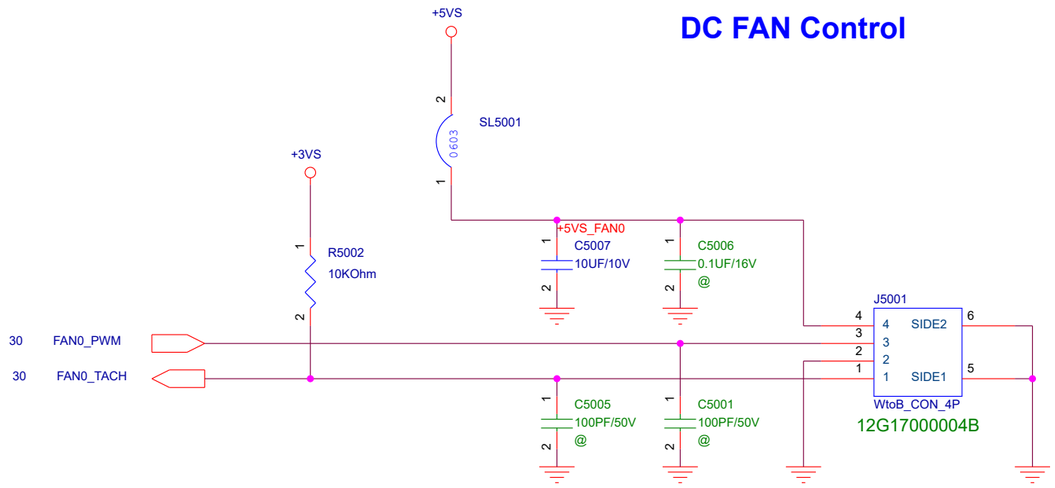
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for powr noise



R2.0-6/23-1

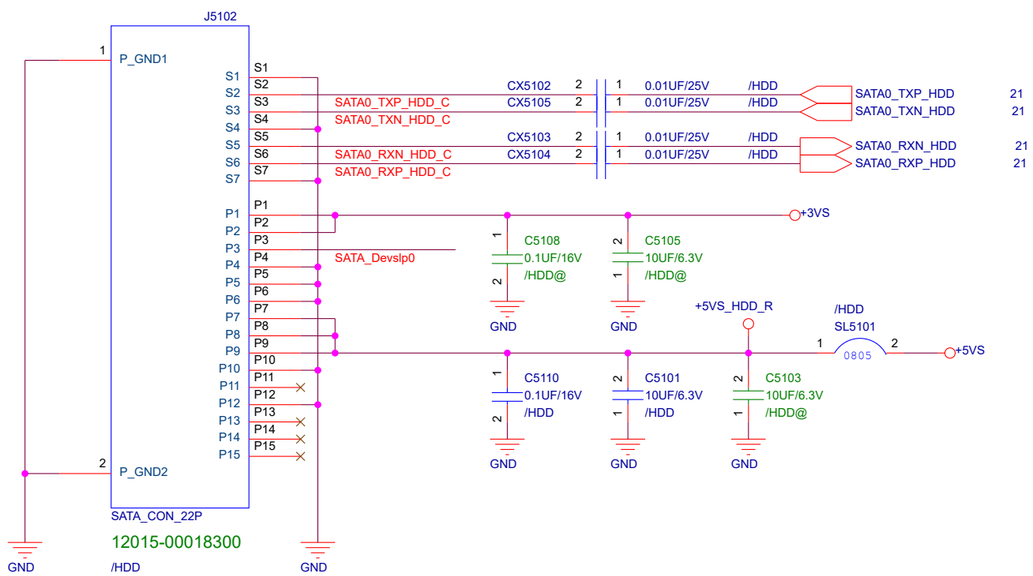
DC FAN Control



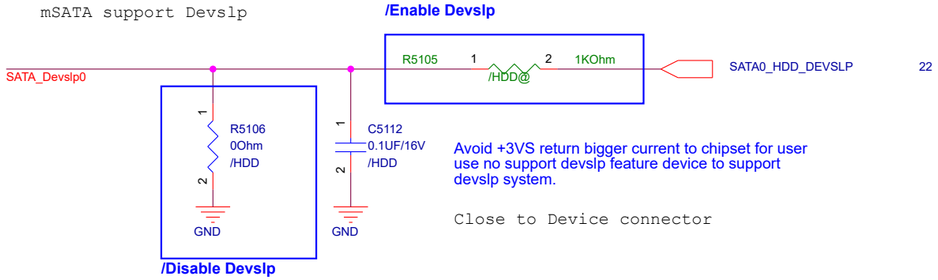
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : FAN_Thermal Sensor & Fan	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 50 of 103	

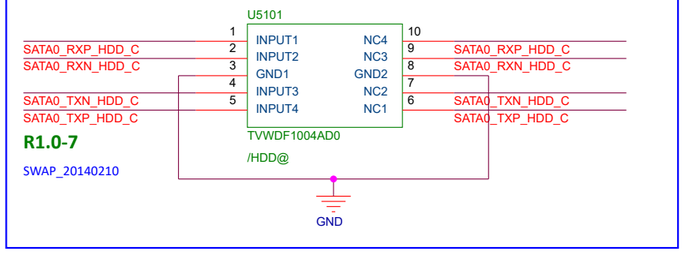
HDD



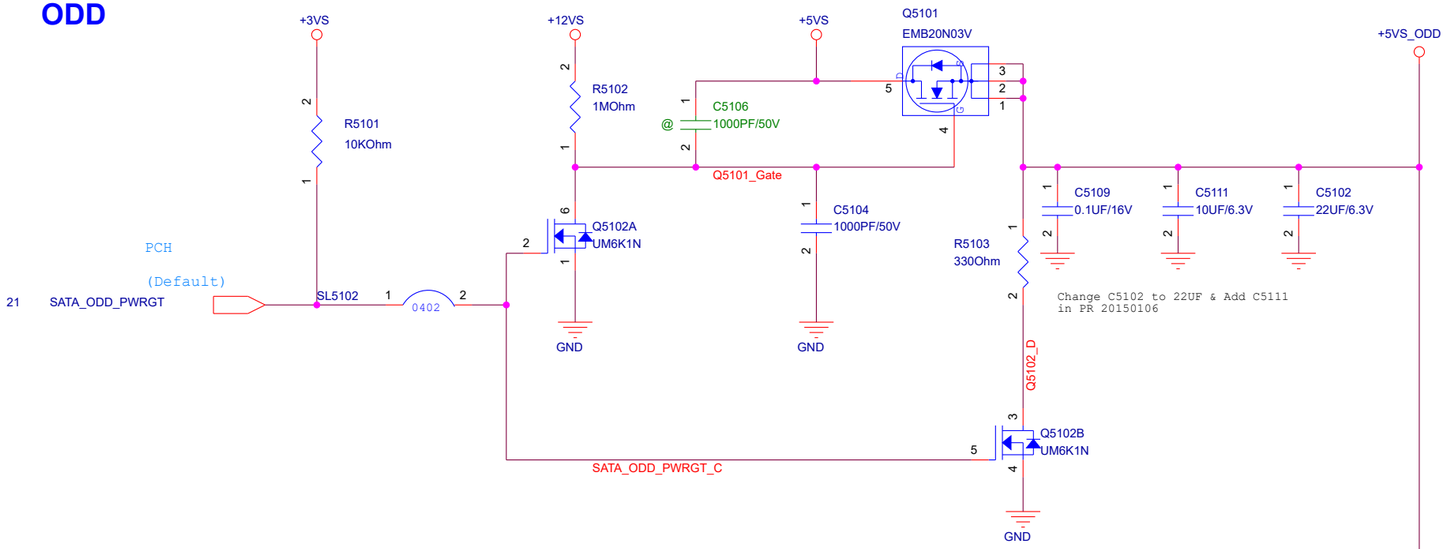
HW_Control SATA Device Sleep

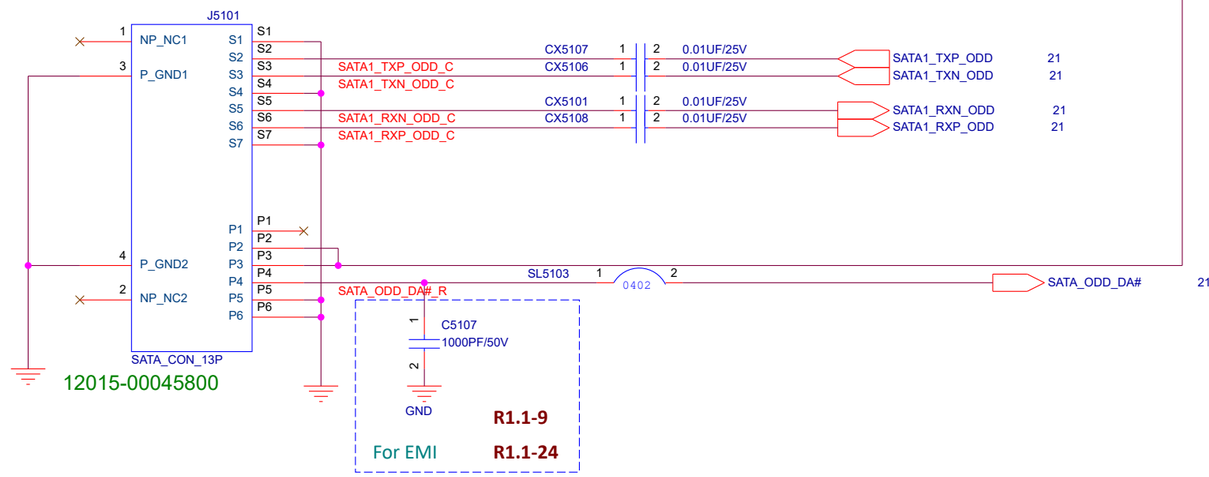


For EMI



ODD



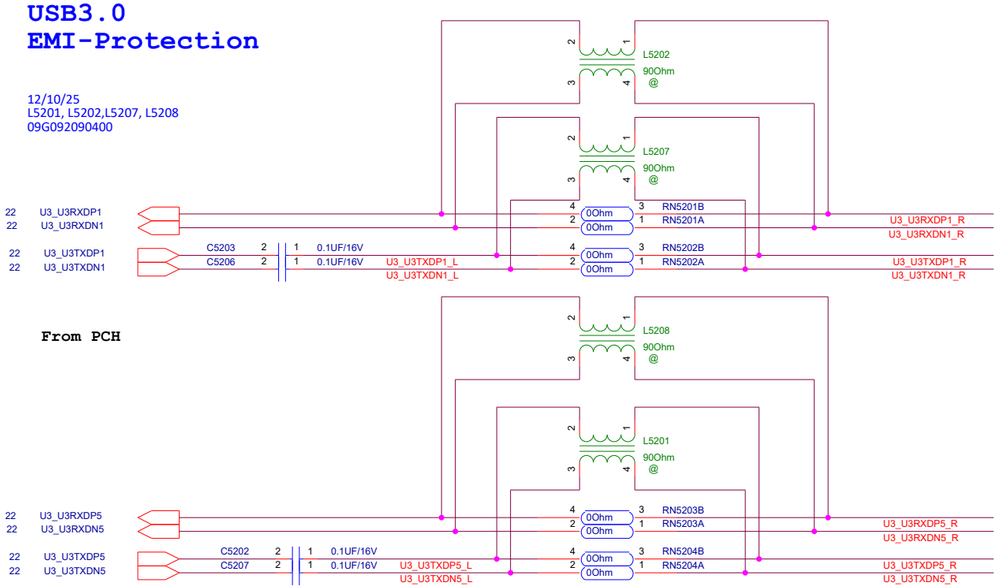


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : HDD & ODD CON	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 51 of 103	

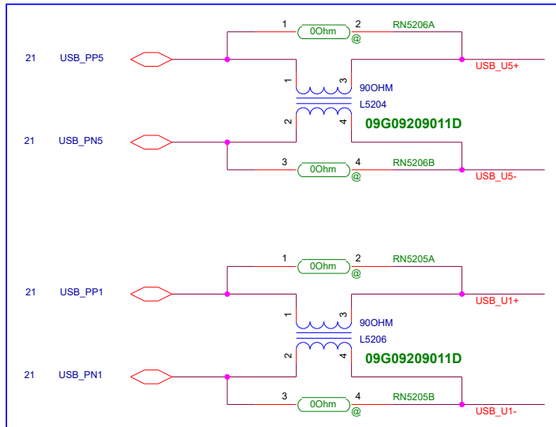
USB3.0 EMI-Protection

12/10/25
L5201, L5202,L5207, L5208
09G092090400



USB2.0 EMI-Protection

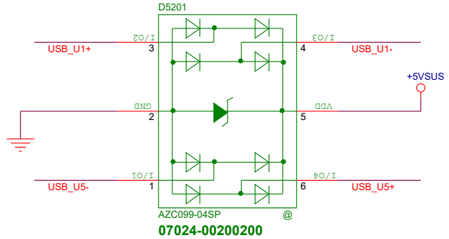
R1.1-4/13-5



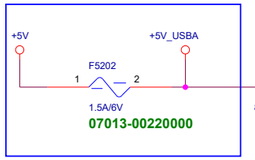
L5204 & L5206 C.M. CHOKE(0805)90 OHM/330mA
1st Source: P/N:09G09209011D INPAQ/MCM2012D900FBE
2nd Source: P/N:09G092090300 TAI-TECH/WCM2012F2SF-900T04
3rd Source: P/N:09G092090110 MURATA/DLW21SN900SQ2L
4th Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S
5th Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L

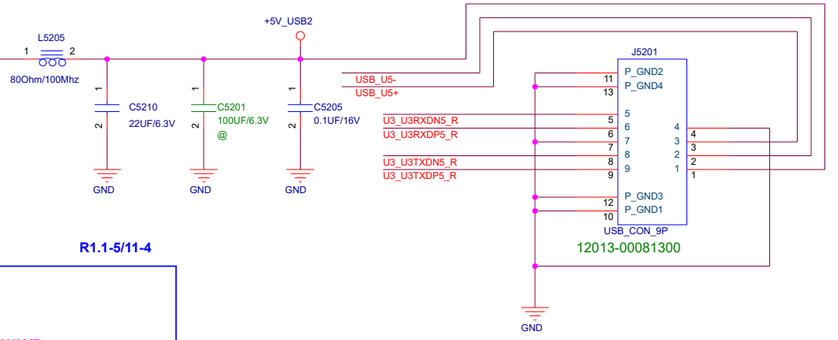
R1.1-4/13-5

D5201 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D



R1.1-5/11-4

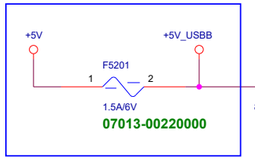


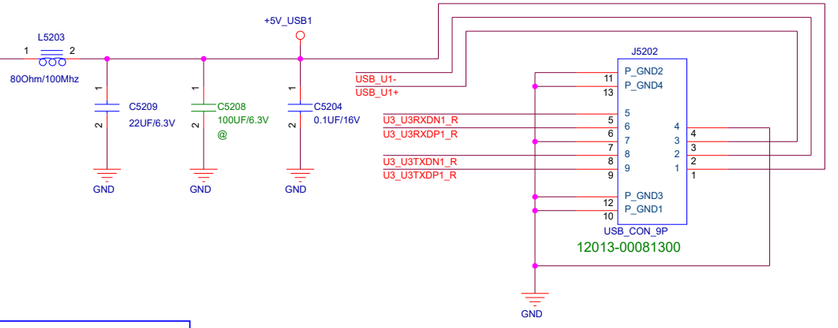


R1.1-5/11-4

F5201, F5202 Poly Fuse
1st Source: P/N:07013-00220000 PTTC/SPR-P150
2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR

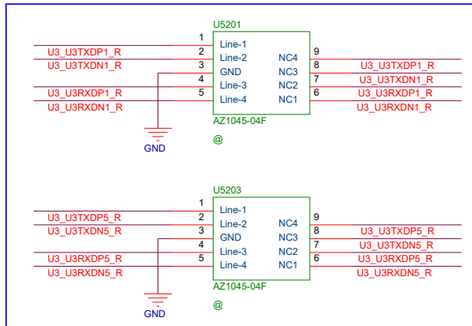
R1.1-5/11-4





USB3.0/USB 2.0 ESD-Protection

R1.1-4/13-5



U5201 & U5203 ESD PROTECTION
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

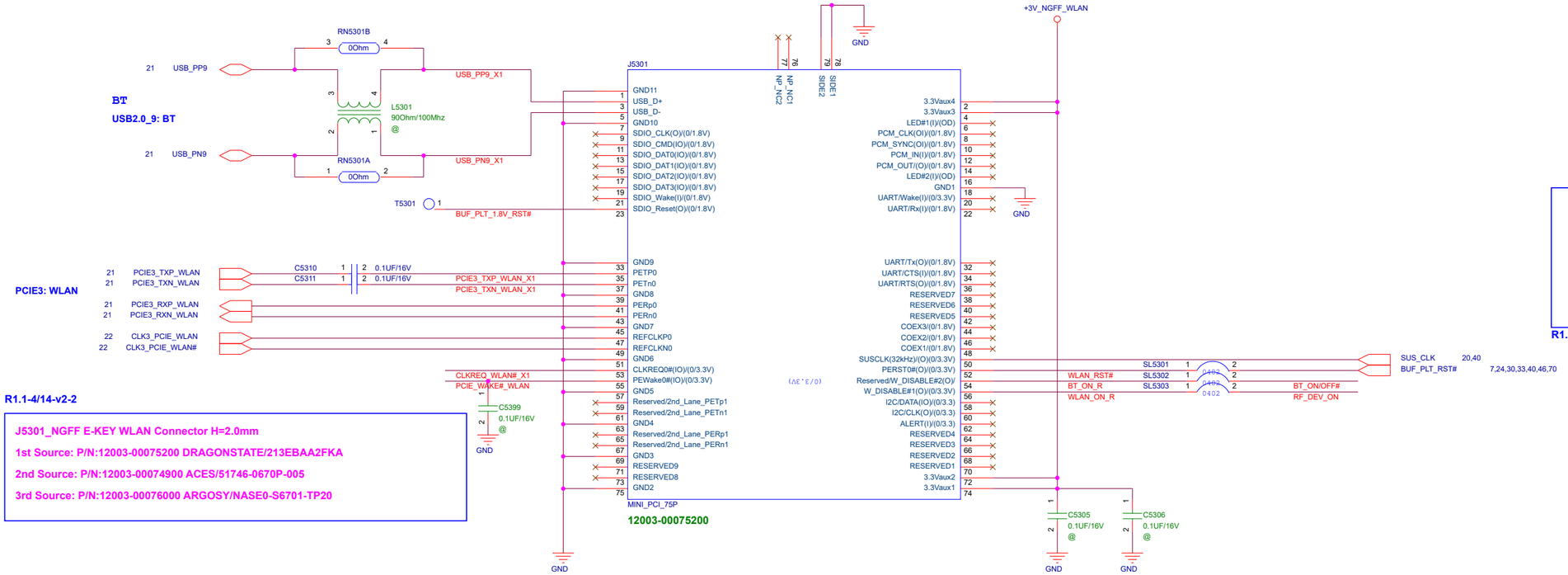
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : USB Port	
	Engineer: Mario_Jhu	
Size: Custom	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 52 of 103	

R1.1-02

NGFF M.2 TYPE_E-KEY WIFI

Main Board



R1.1-4/14-v2-2

J5301_NGFF E-KEY WLAN Connector H=2.0mm

1st Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FKA

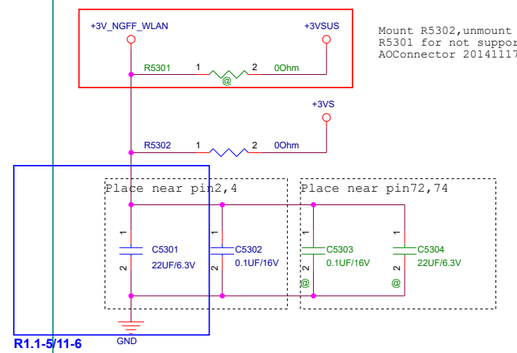
2nd Source: P/N:12003-00074900 ACES/51746-0670P-005

3rd Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)

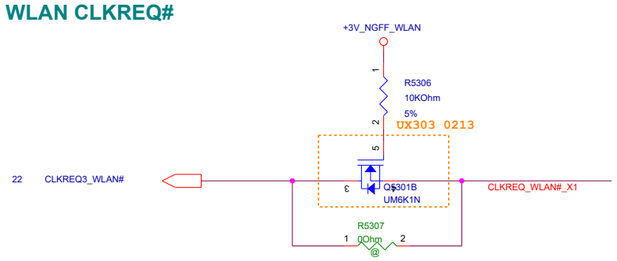
WLAN PWR to +3VSUS



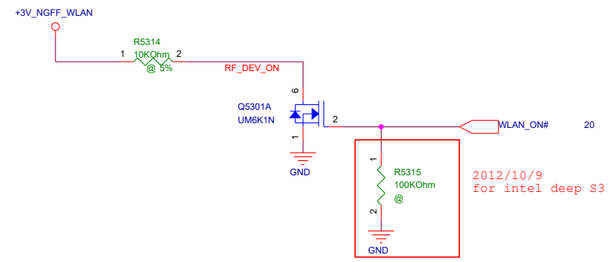
R1.1-5/11-6

74	3.3Vaux	GND	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GND	69
66	RESERVED	Reserved/2nd Lane PERn1	67
64	GPIO0 NFC Reset# (MGPIO7)(O)(0/3.3V)	Reserved/2nd Lane PERp1	65
62	NFC I2C IRQ (MGPIO5)(I)(0/3.3)	GND	63
60	NFC I2C SM CLK (O)(0/3.3)	Reserved/2nd Lane PETn1	61
58	NFC I2C SM DATA (IO)(0/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (?)(0/1.8V)	REFCLKN0	49
46	COEX2(?)(0/1.8V)	REFCLKP0	47
44	COEX3(?)(0/1.8V)	GND	45
42	CLink CLK	PERn0	43
40	CLink DATA	PERp0	41
38	CLink RESET (O)(0/3.3V)	GND	39
36	UART CTS (O)(0/1.8V)	PETn0	37
34	UART RTS (I)(0/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I)(0/1.8V)	SDIO Reset(O)(0/1.8V)	23
20	UART Wake (I)(0/3.3V)	SDIO Wake(I)(0/1.8V)	21
18	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (I)(0/1.8V)	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (O)(0/1.8V)	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (OI)(0/1.8V)	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (OI)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3Vaux	USB_D-	5
2	3.3Vaux	USB_D+	3
		GND	1

WLAN CLKREQ#

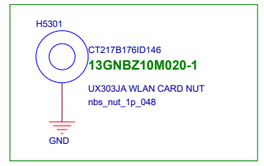


WLAN & BT ON

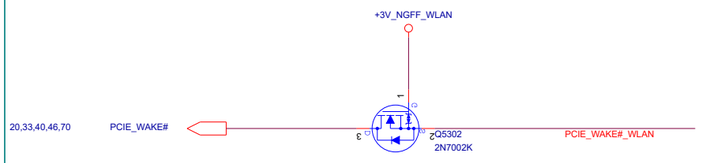


WLAN NUT

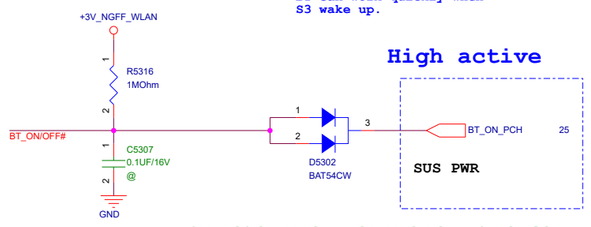
R1.0-29



WLAN_Wake# Control

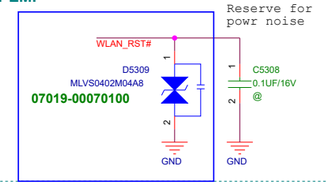


To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

For EMI



R1.1-4/13-5

D5309_VARISTOR 5V 100PF (0402)

1st Source: P/N:07019-00070100 INPAQ/MLVS0402M04A8/SMD

2nd Source: P/N:07G028011010 INPAQ

3rd Source: P/N:07G022005Q11 INPAQ/VPORT0402101MV05

4th Source: P/N:07G022005830 THINKING/TVM0G5R5M261R

5th Source: P/N:07G022005N30 TKS/TVM0G5R5M101R001

R1.1-4/13-5

<Variant Name>

ASUSTeK COMPUTER INC. NB1

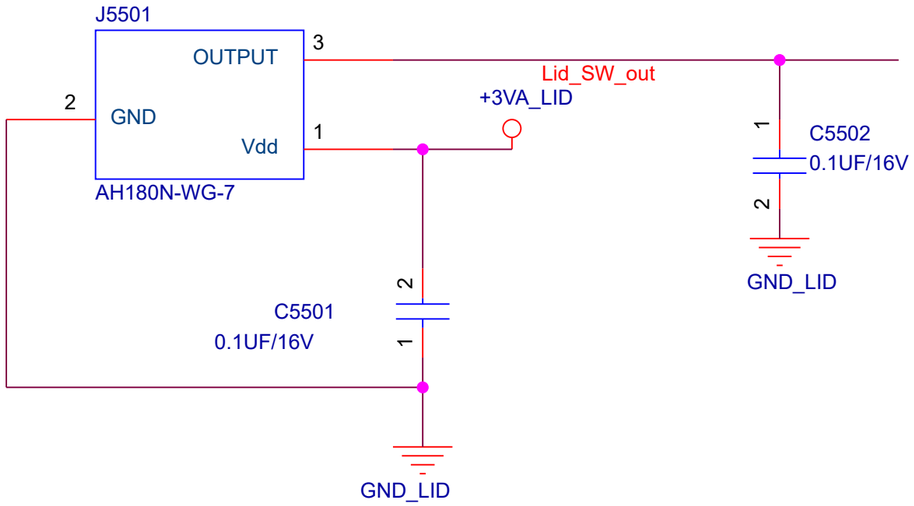
Title : WiFi/WiMax

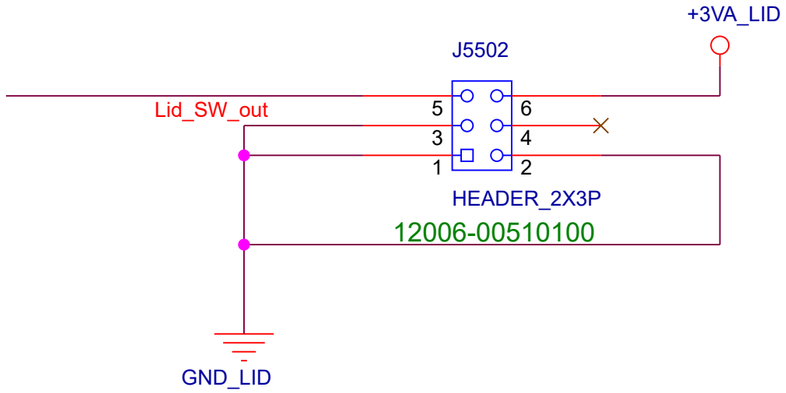
Engineer: Mario_Jhu

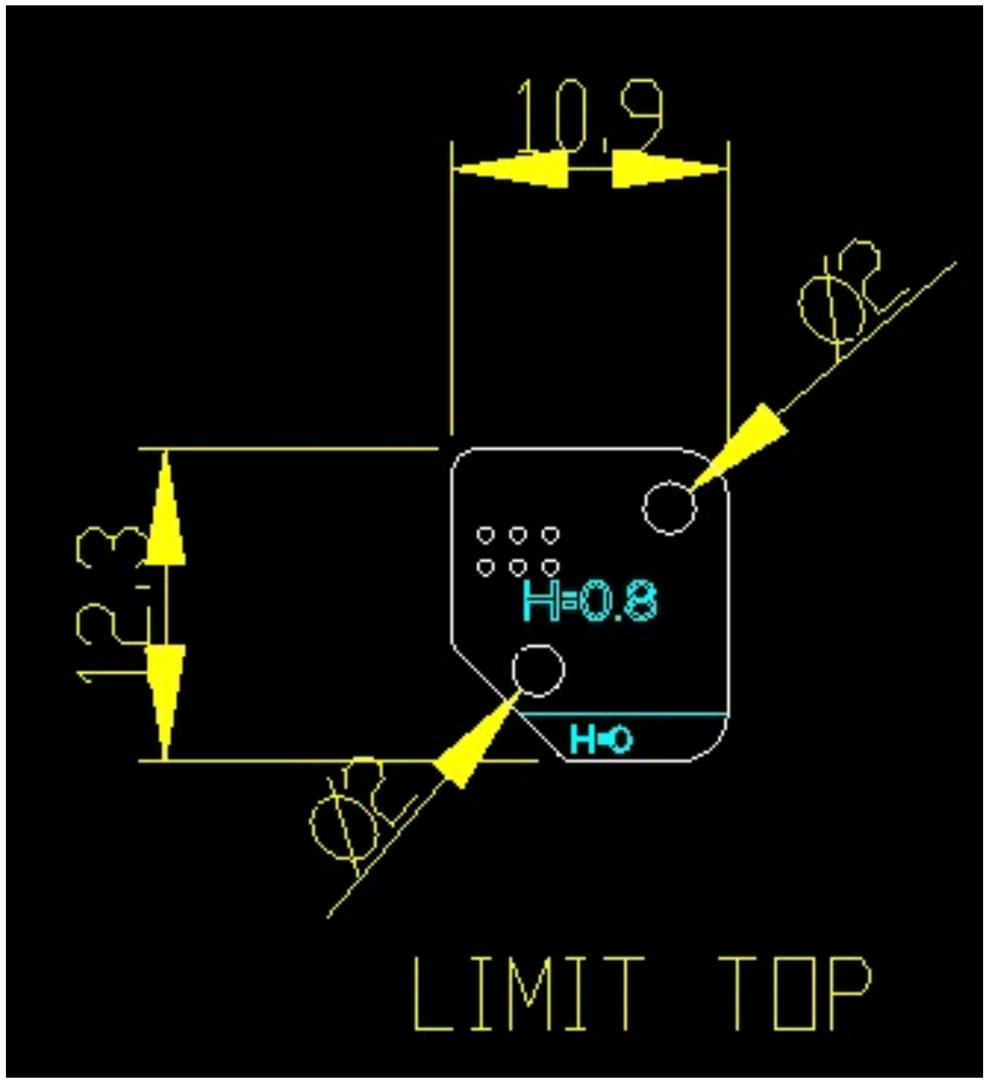
Size	Project Name	Rev
C	GL552VW	2.0

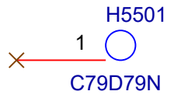
Date: Tuesday, June 23, 2015 Sheet 53 of 103

LID Switch





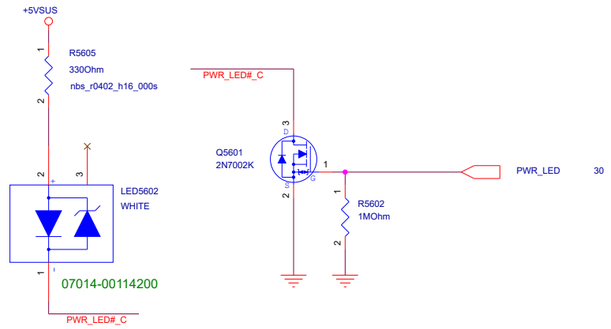




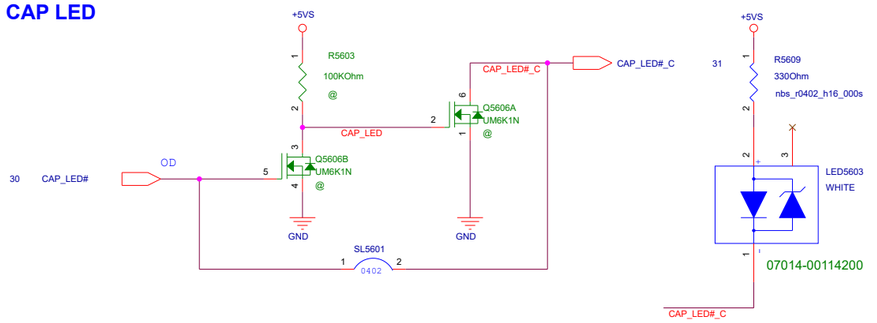
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : Lid_SW_BD		
	Engineer: Mario_Jhu		
Size: A	Project Name: GL552VW		Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 55 of 103		

POWER LED

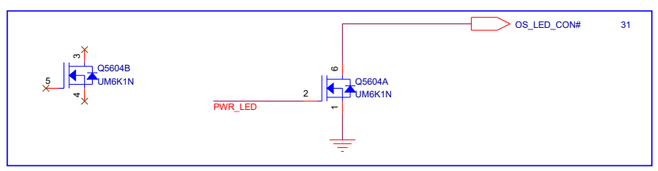


CAP LED

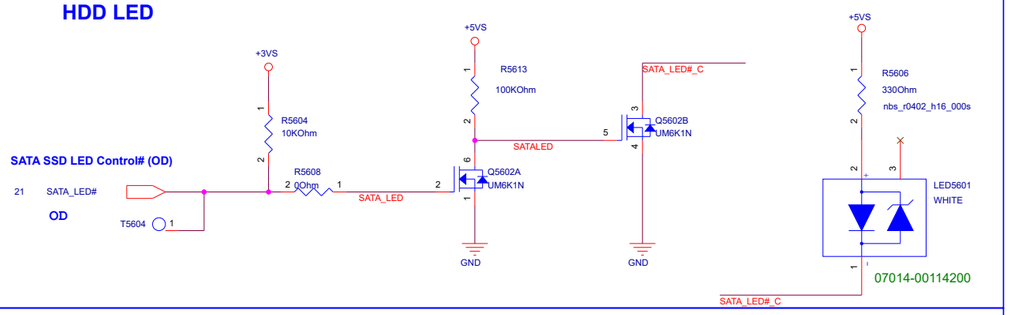


OS_LED#

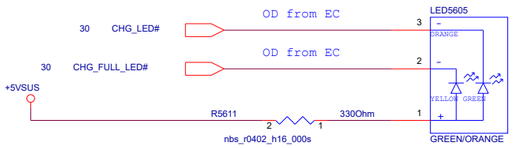
R1.1-5/8-8



HDD LED



Charger LED

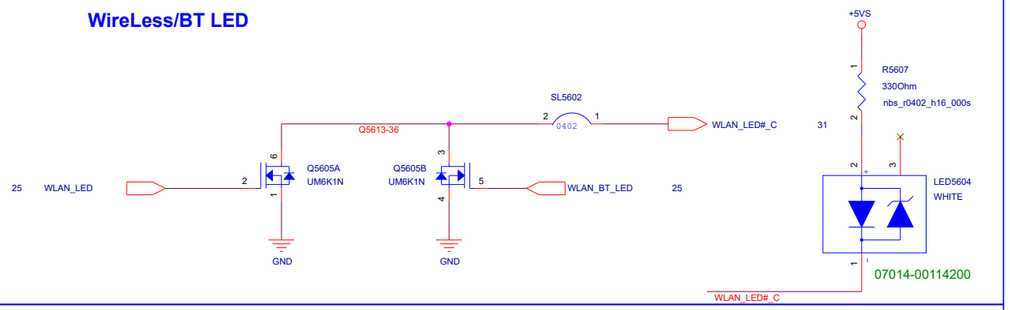


LED5605_ORANGE LIGHT Charge LED

1st Source: P/N:07G015701358 12-22/S2G6C-C30/2C

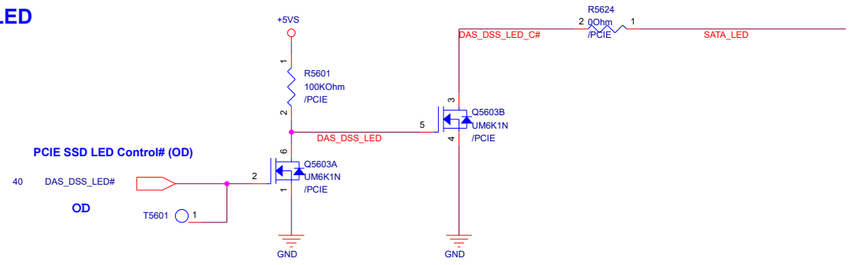
2nd Source: P/N:07014-00140000 LTST-S326KGKFKT-PE

WireLess/BT LED



		The default use of this pin is GPIO49.
SATALED#	OD O	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.
		SGPIO Reference Clock: The SATA controller uses rising edges of

SSD LED



R2.0-6/12v3-1

+5VS
R5703
330Ohm
+5VS_DISCHRG
Q5701B
EM6K1-G-T2R
GND

+3VS
R5704
330Ohm
+3VS_DISCHRG
Q5702A
EM6K1-G-T2R
GND

+VTT
R5708
330Ohm
+VTT_DISCHRG
Q5702B
EM6K1-G-T2R
GND

+3VA
R5701
100KOhm
Q5701A
EM6K1-G-T2R
GND

6,30,45,70,84,88 SUSB_EC#
SUSB_EC
T5701

+12VS
D5701
BAT54CW
@
R5735
0Ohm
@
C5701
0.01UF/25V
@
GND
R5732
1KOhm
@
nbs_r0603_h24_000s
+12VS_DISCHRG
Q5713A
UM6K31N
@
GND

nbs_r0603
1Sec -> 1/10W
10mSec -> 1/2W
10uSec -> 1W

+3VA
R5709
100KOhm
@
Q5712A
UM6K31N
@
GND

+3VSUS
R5716
124Ohm
@
Q5712B
UM6K31N
@
GND

30,83,88 VSUS_ON

+12V & +12VS 需斷開+12VSUS
load switch 後才能放電

+VCCSA
R5717
330Ohm
+VCCSA_DISCHRG
Q5703A
UM6K31N
GND

+VCCIO
R5707
330Ohm
+VCCIO_DISCHRG
Q5703B
UM6K31N
GND

+VCCGT
R5705
330Ohm
+VCCGT_DISCHRG
Q5704A
UM6K31N
GND

+VCCCORE
R5713
330Ohm
+VCCCORE_DISCHRG
Q5704B
UM6K31N
GND

+VCCIO
R5720
330Ohm
@
+VCCIO_DISCHRG
Q5713B
UM6K31N
@
GND

+3VA
R5718
100KOhm
Q5707A
EM6K1-G-T2R
GND

20,30,58,84 PM_SUSB#
PM_SUSB
T5702

+1.2V
R5712
330Ohm
+1.2V_DISCHRG
Q5706B
UM6K31N
GND

+3VA
R5719
100KOhm
PM_SUSC_DISCHRG
Q5707B
EM6K1-G-T2R
GND

20,30,86 PM_SUSC#

R2.0-6/12v3-1

+5V
R5710
330Ohm
+5V_DISCHRG
Q5705B
EM6K1-G-T2R
GND

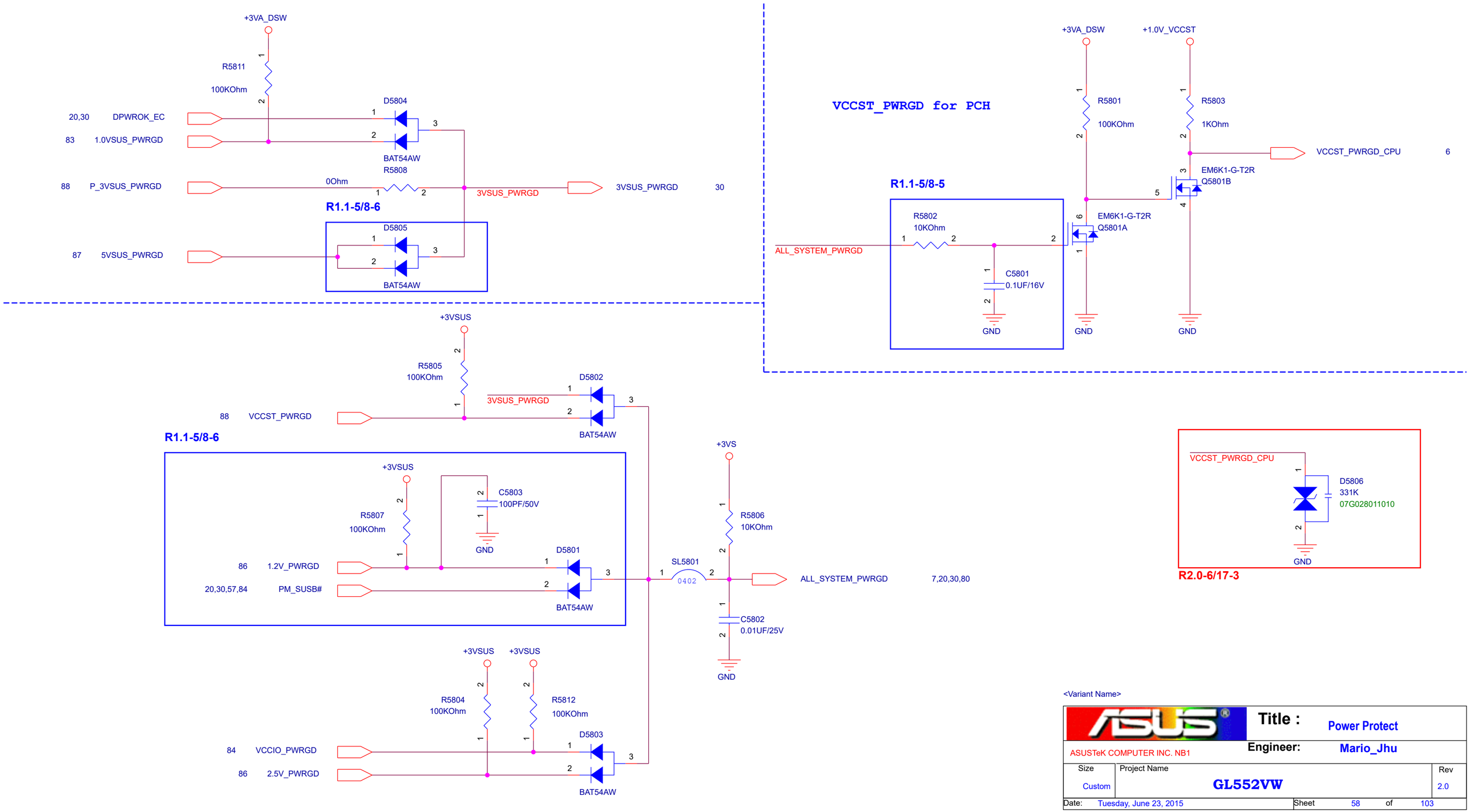
+3V
R5711
330Ohm
+3V_DISCHRG
Q5706A
UM6K31N
GND

+3VA
R5702
100KOhm
Q5705A
EM6K1-G-T2R
GND

30,88 SUSC_EC#
SUSC_EC_DISCHRG

+12V
D5702
BAT54CW
@
R5736
0Ohm
@
C5703
0.01UF/25V
@
R5730
1KOhm
@
nbs_r0603_h24_000s
+12V_DISCHRG
Q5714A
UM6K31N
@
Q5714B
UM6K31N
@

Project Name: GL552VW		Rev: 2.0
Title : DSG Discharge		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 57 of 103	



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : Power Protect	
	Engineer: Mario_Jhu	
Size: Custom	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 58 of 103	

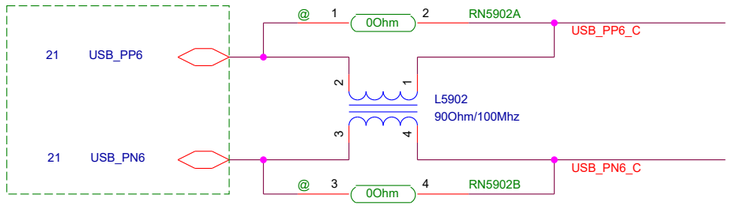
To I/O Board

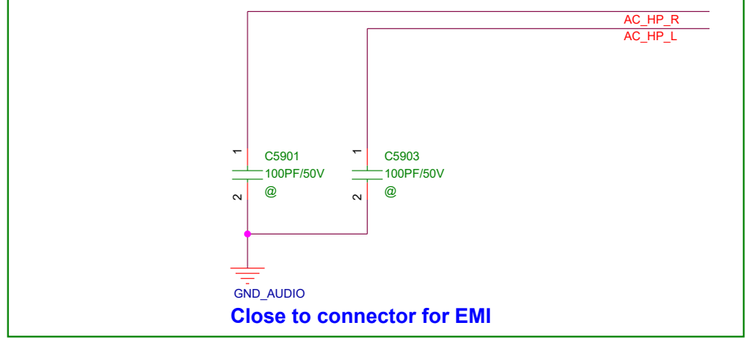
R1.1-5/11-3

L5902 Choke

1st Source: P/N:09G092090100 MURATA/DLW21HN900SQ2L <G>

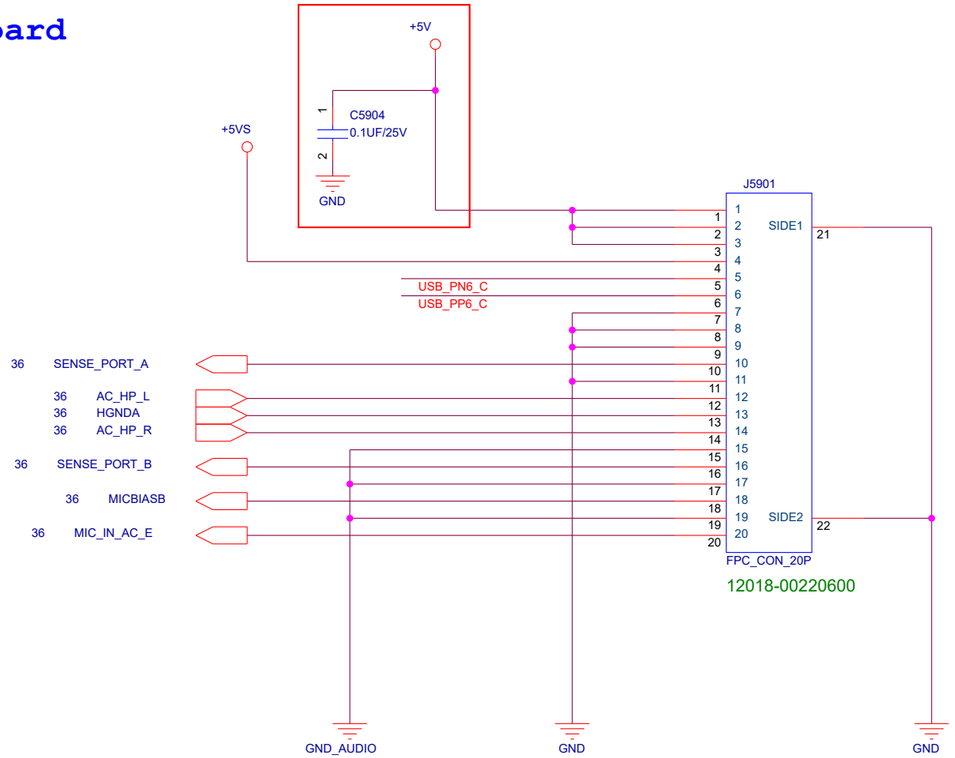
2nd Source: P/N:09G092090107 CHILISIN/CMM21T-900M-S <G>

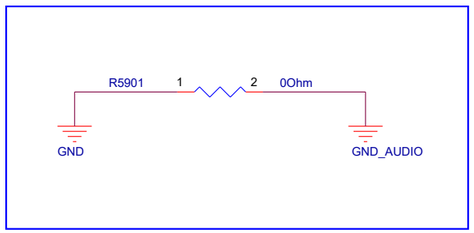




Close to connector for EMI

R2.0-6/9-7



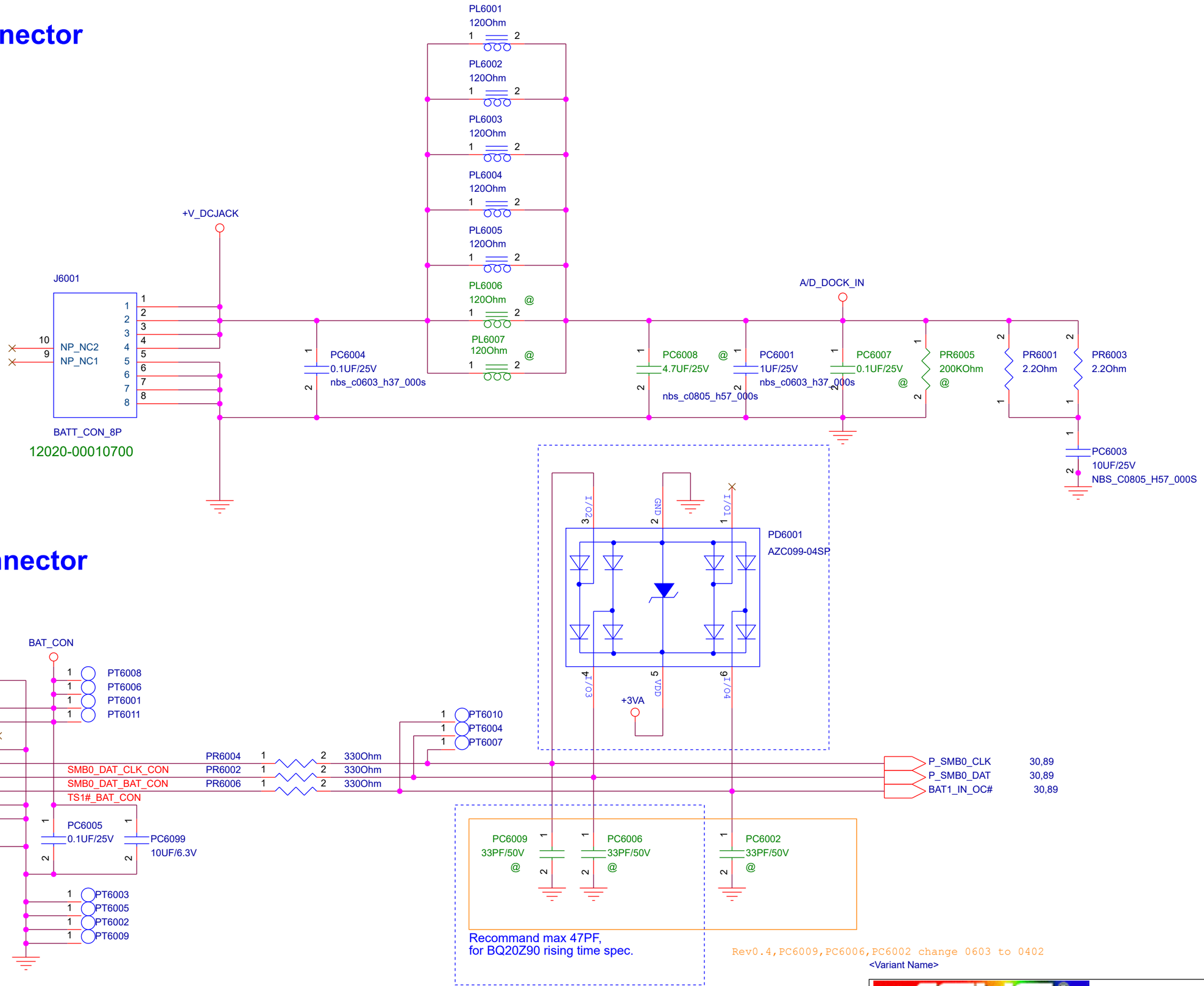


R1.1-5/11-3

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : MB_to_I/O_CONN.	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 59 of 103	

DC-IN Connector

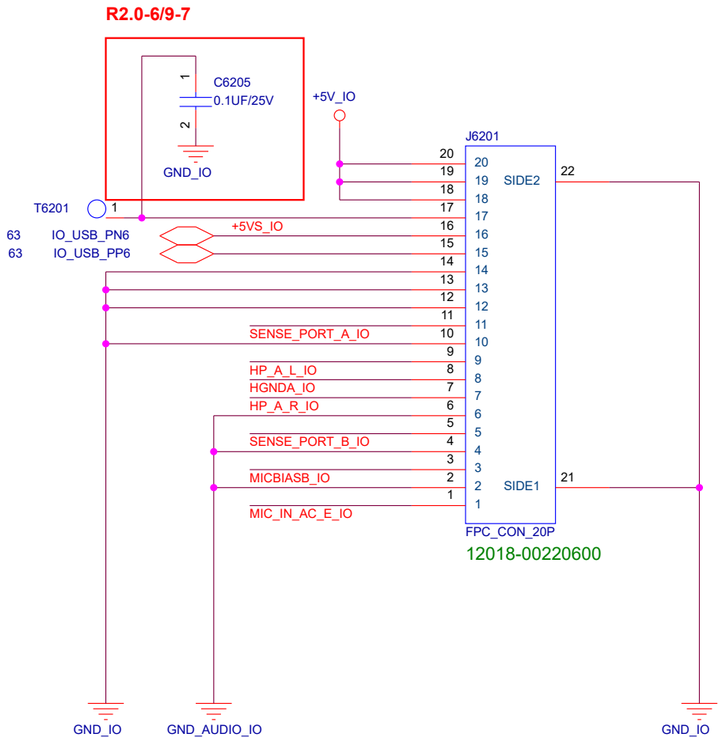


Battery Connector

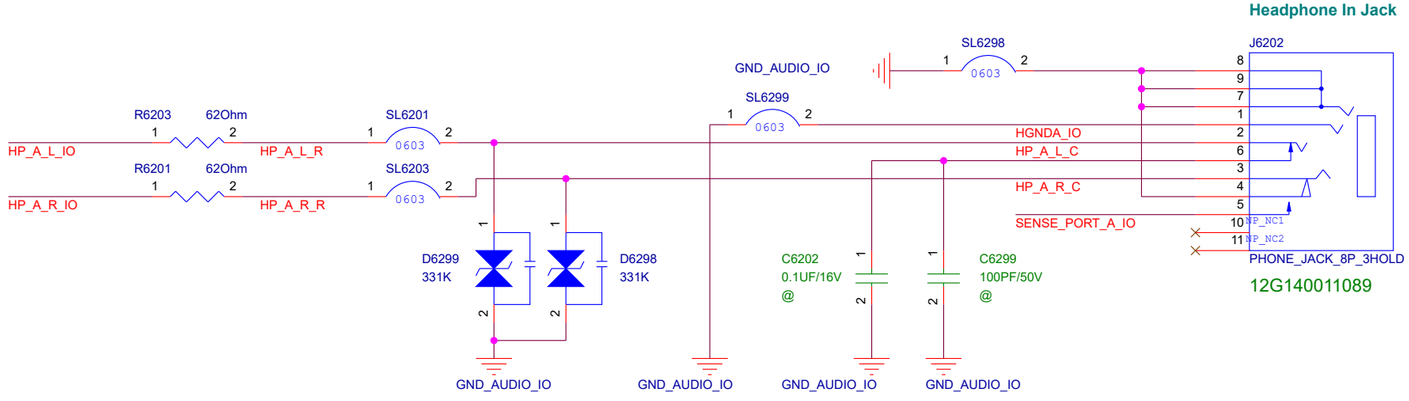
081111 -> 090604:
1. Change PD6001 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer: Edison		
Size: Custom	Project Name: GL552VW		Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 60 of 103		

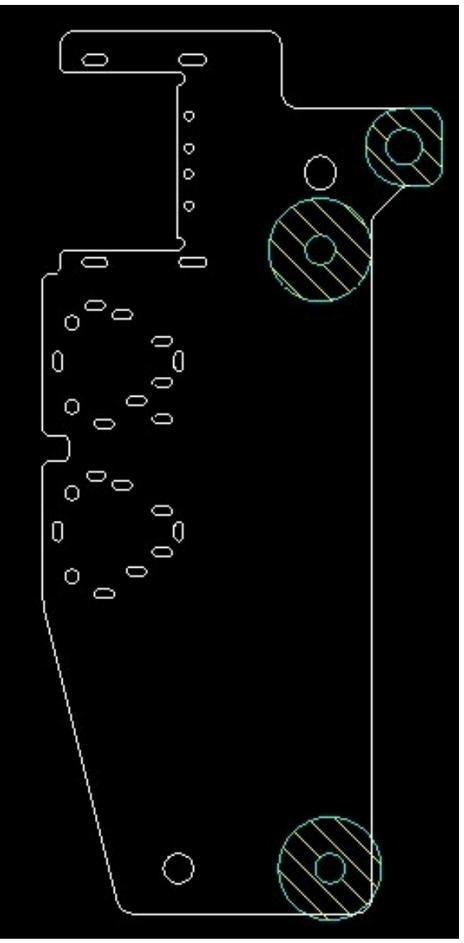
HP JACK for Dual JACK Solution

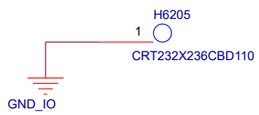


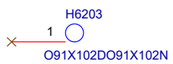
Change to 07g005000313 in SR2 20141027

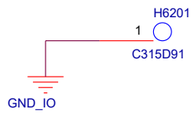


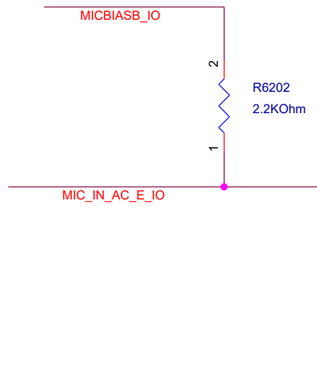
EXTERNAL MICROPHONE

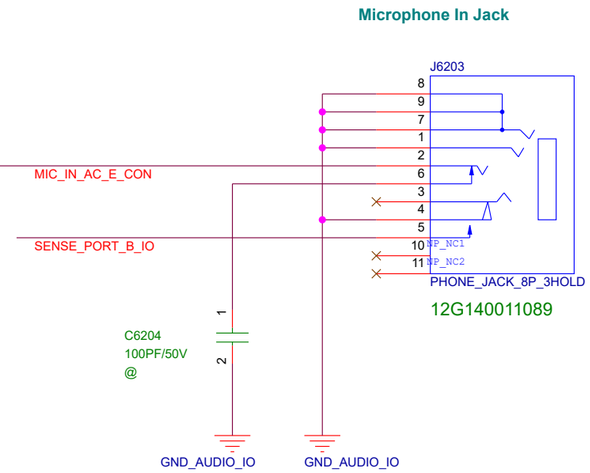


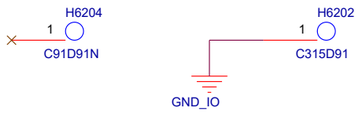


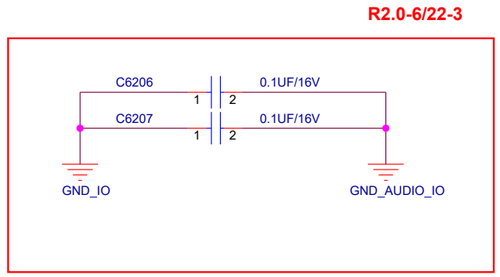












<Variant Name>

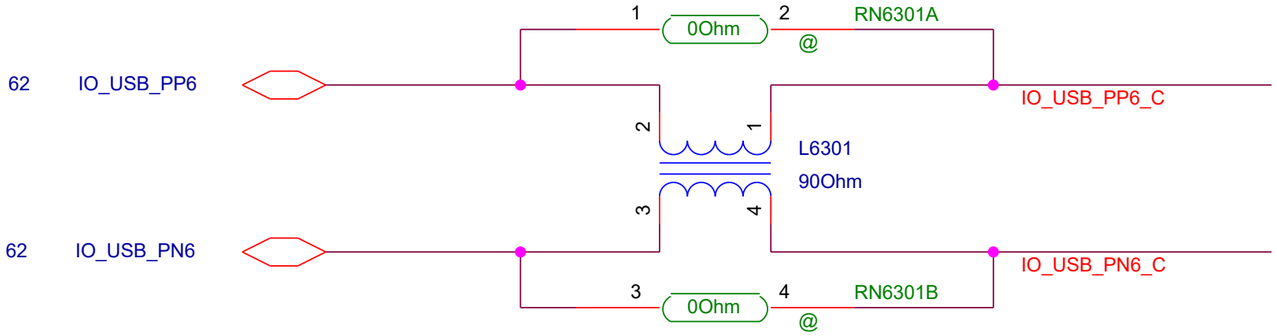
ASUSTeK COMPUTER INC. NB1

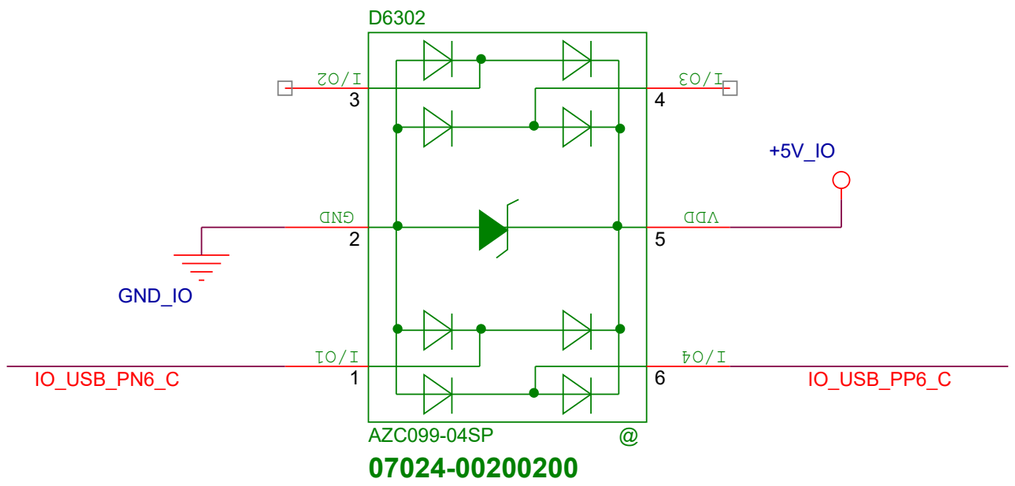
Title : I/O board(1)_MIC/HP

Engineer: Mario_Jhu

Size	Project Name	Rev
Custom	GL552VW	2.0

Date: Tuesday, June 23, 2015 Sheet 62 of 103





USB2.0_Port 3

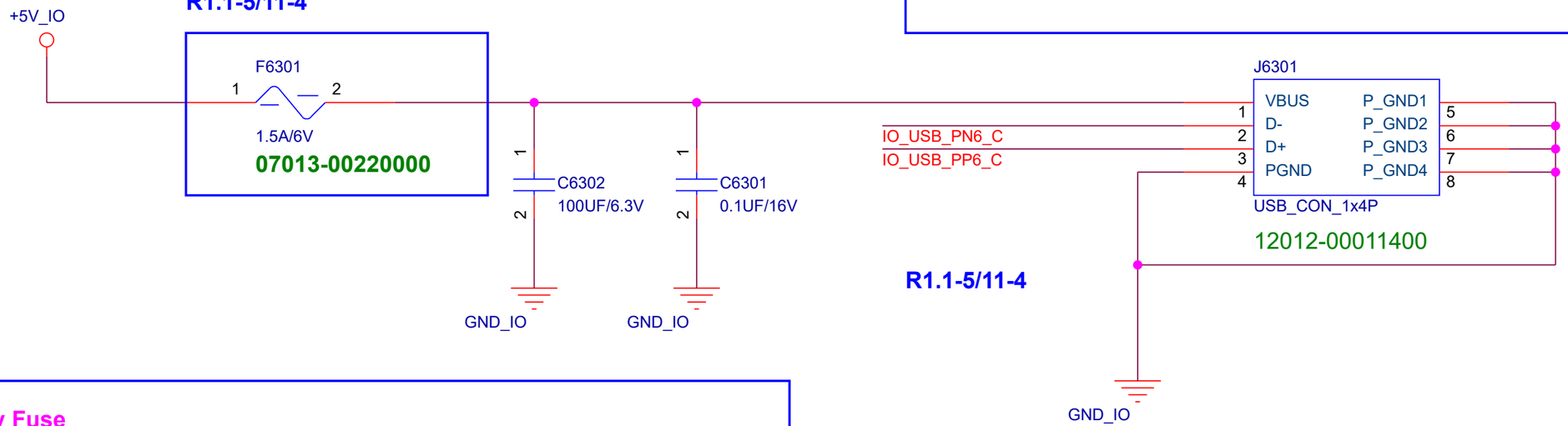
R1.1-4/13-5

D6302 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

R1.1-5/11-4



R1.1-5/11-4

F6301 Poly Fuse

1st Source: P/N:07013-00220000 PTTC/SPR-P150

2nd Source: P/N:07013-00220100 LITTLEFUSE/0805L150ULYR

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : I/O board(2)_USB	
	Engineer: Mario_Jhu	
Size: A	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 63 of 103	

EMI GASKET

H6530 LPG-R-3-2.5-3 GND
H6531 LPG-R-3-2.5-3 GND
H6532 LPG-R-3-2.5-3 GND
H6538 GASKET_1P GND
H6534 LPG-R-3-2.5-3 GND
H6535 LPG-R-3-2.5-3 GND
H6536 LPG-R-3-2.5-3 @ GND

Bracket change to Nut in SR2 20141031

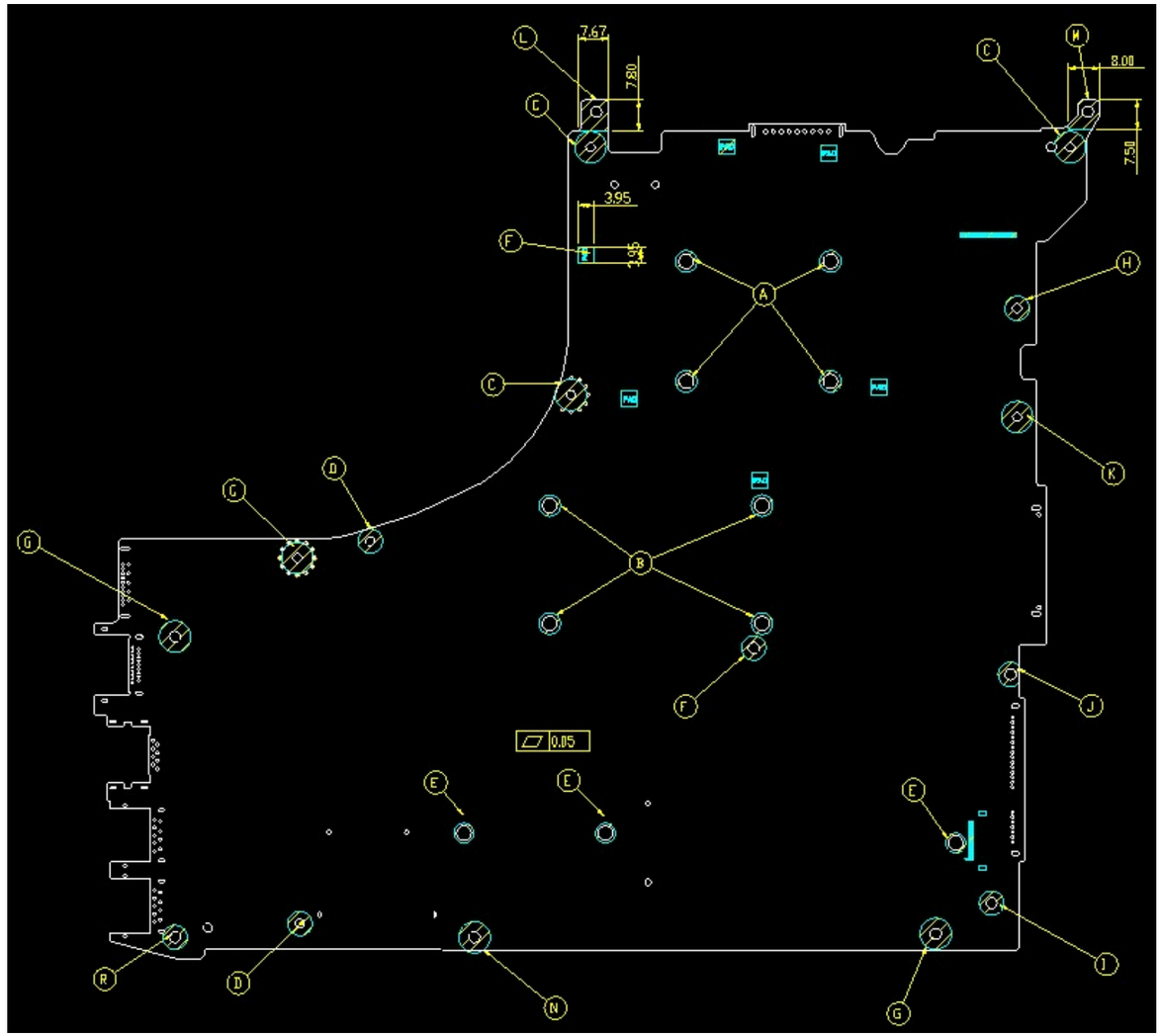
H6533 GASKET_1P GND
H6537 GASKET_1P GND

H6533 & H6537 Change to H=3.5mm Gasket in PR

SSD

H6547 CT217CB140D110 13020-02260200 nbs_smdpad_1p_062 GND
H6548 CT217CB140D110 13020-02260200 nbs_smdpad_1p_062 GND

R2.0-6/12-2



A - dGPU

H6501 CT236CB176D146 13020-02260000 GND
H6502 CT236CB176D146 13020-02260000 GND
H6503 CT236CB176D146 13020-02260000 GND
H6504 CT236CB176D146 13020-02260000 GND

B - CPU

H6506 CT236CB176D146 13020-02260100 GND
H6508 CT236CB176D146 13020-02260100 GND
H6505 CT236CB176D146 13020-02260100 GND
H6507 CT236CB176D146 13020-02260100 GND

R1.1-5/11-9

C

H6509 HOLE_13PTH
P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_GND7 P_GND8 P_GND9 P_GND10 P_GND11 P_GND12 P_GND13
GND
H6511 C315D91 GND

H6513 9D_D91_D28
P_GND1 P_GND2 P_GND3 P_GND4 P_GND5 P_GND6 P_GND7 P_GND8 P_GND9
GND

C1

C2

H6529 2D_D91_DO98X87N
GND NP_NC
GND

D

H6515 C244D91 GND
H6516 C244D91 GND

R1.1-5/12-13

E - PCH

H6517 CT217B176D146 13G021052050 GND
H6518 CT217B176D146 13G021052050 GND

H6519 CT217CB176D146 13GNER10S040-1 GND_AUDIO

G

H6520 C315D110 GND
H6512 C315D110 GND

H

H6523 CT244CB315D91 GND

F

H6541 CT244CB315D110 GND

I

H6524 CT244B413X402D110 GND

J

H6525 CRT215X244RBD110 GND

N

H6510 CT315CB236D110 GND

R

H6527 C87D87N
H6521 CT244CB236D110 GND

L

H6539 CRT302X307CBD110 GND

K

H6526 CT315RB407X787D91 GND

M

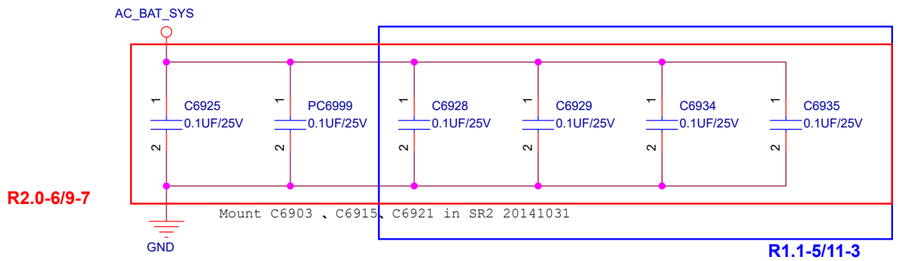
H6540 CRT315X295CBD110 GND

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title :	ME_NUT
	Engineer:	Mario_Jhu
Size: Custom	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 65 of 103	

2014-02-12 Add EMI solution
(6042.00 6728.00)、(1947.00 3850.00)、
(1757.00 1852.00)、(6369.00 -299.00)

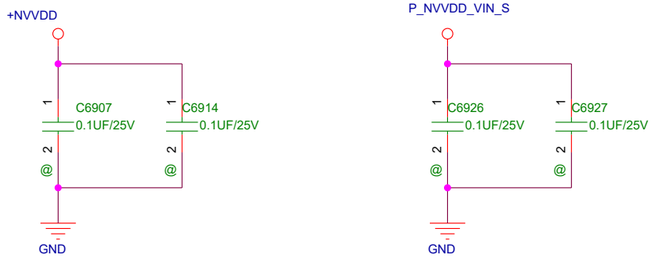
R1.0-16



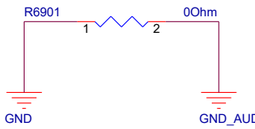
R2.0-6/9-7

R1.1-5/11-3

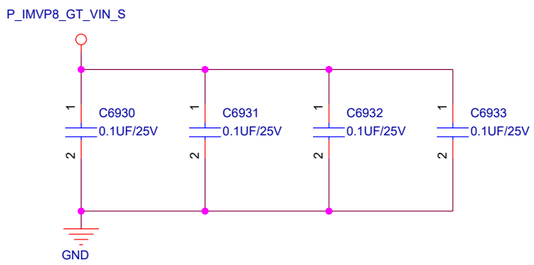
(6490.00 4706.00)、(7437.00 3852.00)



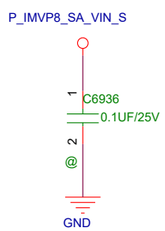
(8004.00 585.00)



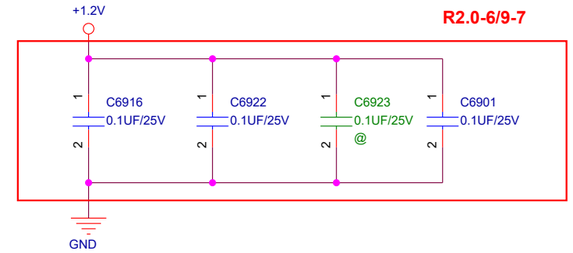
R2.0-6/9-7



R1.1-5/11-3



2014-04-03 Add EMI solution
(3678, 2622)、(4011, 2594)、(4975, 2580)、(5169, 2585)

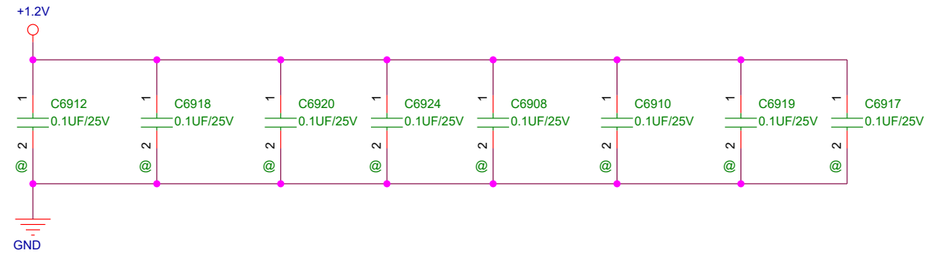


R2.0-6/9-7

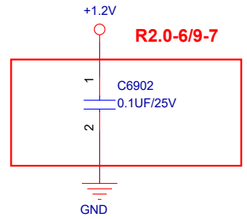
R1.1-15

R1.1-24

2014-04-03 Add EMI solution
Top
(3541,2591)、(3339,2115)、(3807,2452)、(4030,2118)、
(3367,1670)、(3583,1965)、(3819,1953)、(4013,1650)



Bot (3809, 2558)



R2.0-6/9-7

R1.1-22

R1.1-24

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : OTH_EMI	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 69 of 103	

PCI EXPRESS

3 PCIENB_RXN[15:0]
3 PCIENB_RXP[15:0]

3 PCIEG_RXN[15:0]
3 PCIEG_RXP[15:0]

R2.0-6/9-7

PCIENB_RXN0	0.22UF/10V	2 1	CX7032		
PCIENB_RXP0	0.22UF/10V	2 1	CX7001		PCIEG_TXN15
					PCIEG_TXP15
PCIENB_RXN1	0.22UF/10V	2 1	CX7015		
PCIENB_RXP1	0.22UF/10V	2 1	CX7014		PCIEG_TXN14
					PCIEG_TXP14
PCIENB_RXN2	0.22UF/10V	2 1	CX7027		
PCIENB_RXP2	0.22UF/10V	2 1	CX7019		PCIEG_TXN13
					PCIEG_TXP13
PCIENB_RXN3	0.22UF/10V	2 1	CX7003		
PCIENB_RXP3	0.22UF/10V	2 1	CX7024		PCIEG_TXN12
					PCIEG_TXP12
PCIENB_RXN4	0.22UF/10V	2 1	CX7018		
PCIENB_RXP4	0.22UF/10V	2 1	CX7025		PCIEG_TXN11
					PCIEG_TXP11
PCIENB_RXN5	0.22UF/10V	2 1	CX7031		
PCIENB_RXP5	0.22UF/10V	2 1	CX7008		PCIEG_TXN10
					PCIEG_TXP10
PCIENB_RXN6	0.22UF/10V	2 1	CX7010		
PCIENB_RXP6	0.22UF/10V	2 1	CX7002		PCIEG_TXN9
					PCIEG_TXP9
PCIENB_RXN7	0.22UF/10V	2 1	CX7026		
PCIENB_RXP7	0.22UF/10V	2 1	CX7022		PCIEG_TXN8
					PCIEG_TXP8
PCIENB_RXN8	0.22UF/10V	2 1	CX7017		
PCIENB_RXP8	0.22UF/10V	2 1	CX7013		PCIEG_TXN7
					PCIEG_TXP7
PCIENB_RXN9	0.22UF/10V	2 1	CX7016		
PCIENB_RXP9	0.22UF/10V	2 1	CX7021		PCIEG_TXN6
					PCIEG_TXP6
PCIENB_RXN10	0.22UF/10V	2 1	CX7004		PCIEG_TXN5
PCIENB_RXP10	0.22UF/10V	2 1	CX7006		PCIEG_TXP5
PCIENB_RXN11	0.22UF/10V	2 1	CX7011		PCIEG_TXN4
PCIENB_RXP11	0.22UF/10V	2 1	CX7023		PCIEG_TXP4
PCIENB_RXN12	0.22UF/10V	2 1	CX7005		PCIEG_TXN3
PCIENB_RXP12	0.22UF/10V	2 1	CX7030		PCIEG_TXP3
PCIENB_RXN13	0.22UF/10V	2 1	CX7028		PCIEG_TXN2
PCIENB_RXP13	0.22UF/10V	2 1	CX7009		PCIEG_TXP2
PCIENB_RXN14	0.22UF/10V	2 1	CX7007		PCIEG_TXN1
PCIENB_RXP14	0.22UF/10V	2 1	CX7012		PCIEG_TXP1
PCIENB_RXN15	0.22UF/10V	2 1	CX7029		PCIEG_TXN0
PCIENB_RXP15	0.22UF/10V	2 1	CX7020		PCIEG_TXP0

20,33,40,46,53 PCIE_WAKE# — R7023 @ 0Ohm

NV review 20140918

+3VSG_AON — R7014 10KOhm

22 CLK_PEGA_REQ0# — R7005 @ 0Ohm — CLK_PEGA_REQ0#_VGA

22 CLK0_PCIE_PEG_VGA
22 CLK0_PCIE_PEG#_VGA

U7001A
1/18 PCI_EXPRESS
GM107/GM108 GK107/GK208 GF117: NC

NC1	AJ11		
DGPU_RST#	AJ12	PEX_RST_N	
CLK_PEGA_REQ0#_VGA	AK12	PEX_CLKREQ_N	
	AL13	PEX_REFCLK	
	AK13	PEX_REFCLK_N	
PCIEG_TXP0	AK14	PEX_TX0	
PCIEG_TXN0	AJ14	PEX_TX0_N	
PCIEG_RXP0	AN12	PEX_RX0	
PCIEG_RXN0	AM12	PEX_RX0_N	
PCIEG_TXP1	AH14	PEX_TX1	
PCIEG_TXN1	AG14	PEX_TX1_N	
PCIEG_RXP1	AN14	PEX_RX1	
PCIEG_RXN1	AM14	PEX_RX1_N	
PCIEG_TXP2	AK15	PEX_TX2	
PCIEG_TXN2	AJ15	PEX_TX2_N	
PCIEG_RXP2	AP14	PEX_RX2	
PCIEG_RXN2	AP15	PEX_RX2_N	
PCIEG_TXP3	AL16	PEX_TX3	
PCIEG_TXN3	AK16	PEX_TX3_N	
PCIEG_RXP3	AN15	PEX_RX3	
PCIEG_RXN3	AM15	PEX_RX3_N	
PCIEG_TXP4	AK17	PEX_TX4	
PCIEG_TXN4	AJ17	PEX_TX4_N	
PCIEG_RXP4	AN17	PEX_RX4	
PCIEG_RXN4	AM17	PEX_RX4_N	
PCIEG_TXP5	AH17	PEX_TX5	
PCIEG_TXN5	AG17	PEX_TX5_N	
PCIEG_RXP5	AP17	PEX_RX5	
PCIEG_RXN5	AP18	PEX_RX5_N	
PCIEG_TXP6	AK18	PEX_TX6	
PCIEG_TXN6	AJ18	PEX_TX6_N	
PCIEG_RXP6	AN18	PEX_RX6	
PCIEG_RXN6	AM18	PEX_RX6_N	
PCIEG_TXP7	AL19	PEX_TX7	
PCIEG_TXN7	AK19	PEX_TX7_N	
PCIEG_RXP7	AN20	PEX_RX7	
PCIEG_RXN7	AM20	PEX_RX7_N	
PCIEG_TXP8	AK20	PEX_TX8	
PCIEG_TXN8	AJ20	PEX_TX8_N	
PCIEG_RXP8	AP20	PEX_RX8	
PCIEG_RXN8	AP21	PEX_RX8_N	
PCIEG_TXP9	AH20	PEX_TX9	
PCIEG_TXN9	AG20	PEX_TX9_N	
PCIEG_RXP9	AN21	PEX_RX9	
PCIEG_RXN9	AM21	PEX_RX9_N	
PCIEG_TXP10	AK21	PEX_TX10	
PCIEG_TXN10	AJ21	PEX_TX10_N	
PCIEG_RXP10	AN23	PEX_RX10	
PCIEG_RXN10	AM23	PEX_RX10_N	
PCIEG_TXP11	AL22	PEX_TX11	
PCIEG_TXN11	AK22	PEX_TX11_N	
PCIEG_RXP11	AP23	PEX_RX11	
PCIEG_RXN11	AP24	PEX_RX11_N	
PCIEG_TXP12	AK23	PEX_TX12	
PCIEG_TXN12	AJ23	PEX_TX12_N	
PCIEG_RXP12	AN24	PEX_RX12	
PCIEG_RXN12	AM24	PEX_RX12_N	
PCIEG_TXP13	AH23	PEX_TX13	
PCIEG_TXN13	AG23	PEX_TX13_N	
PCIEG_RXP13	AN26	PEX_RX13	
PCIEG_RXN13	AM26	PEX_RX13_N	
PCIEG_TXP14	AK24	PEX_TX14	
PCIEG_TXN14	AJ24	PEX_TX14_N	
PCIEG_RXP14	AP26	PEX_RX14	
PCIEG_RXN14	AP27	PEX_RX14_N	
PCIEG_TXP15	AL25	PEX_TX15	
PCIEG_TXN15	AK25	PEX_TX15_N	
PCIEG_RXP15	AN27	PEX_RX15	
PCIEG_RXN15	AM27	PEX_RX15_N	

PEX LANES 8 TO 15 NC FOR GK208/GF117
PEX LANES 4 TO 15 NC FOR GM108

N16P-GX-A2
02004-00450100
C.S N16P-GX-A2 FCBGA908

[HF]NVIDIA GB4B-128 GM107-770-A2
NVIDIA GB4B-128 GM107-770-A2

1. P/N:02004-00450100 (PS) C.S N16P-GX-A2 FCBGA908

PLACE under BGA — near BGA — PLACE between BGA and POWER SUPPLY

PEXIOVDD1 AG19
PEXIOVDD2 AG21
PEXIOVDD3 AG22
PEXIOVDD4 AG24
PEXIOVDD5 AH21
PEXIOVDD6 AH25

C7007 1UF/6.3V — C7002 1UF/6.3V — C7015 4.7UF/6.3V — C7005 10UF/6.3V — C7012 10UF/6.3V — C7001 22UF/6.3V nbs_c0603_h37_000s — C7014 22UF/6.3V nbs_c0603_h37_000s

+PEX_VDD — GND

PEXIOVDDQ1 AG13
PEXIOVDDQ2 AG15
PEXIOVDDQ3 AG16
PEXIOVDDQ4 AG18
PEXIOVDDQ5 AG25
PEXIOVDDQ6 AH15
PEXIOVDDQ7 AH18
PEXIOVDDQ8 AH26
PEXIOVDDQ9 AH27
PEXIOVDDQ10 AJ27
PEXIOVDDQ11 AK27
PEXIOVDDQ12 AL27
PEXIOVDDQ13 AM28
PEXIOVDDQ14 AN28

C7011 1UF/6.3V — C7018 1UF/6.3V — C7022 4.7UF/6.3V — C7020 10UF/6.3V — C7016 10UF/6.3V — C7009 22UF/6.3V nbs_c0603_h37_000s — C7004 22UF/6.3V nbs_c0603_h37_000s

+PEX_VDD — GND

near BGA

R2.0-6/9-7

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12

C7013 0.1UF/16V — C7021 4.7UF/6.3V — C7017 4.7UF/6.3V — PEX_SSVDD_3V3 — SL7005 0402 — +3VSG_AON — GND

VDD_SENSE L4 — NVVDD_VCCSENSE 91
GND_SENSE L5 — NVDD_GND_SENSE — SL7001 0603 — NVVDD_VSSSENSE 91

R7004 0Ohm @ — GND

3V3AUX_NC P8

PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT_N AK26
PEX_TSTCLK_OUT
PEX_TSTCLK_OUTN

R7009 @ 200Ohm

PLACE near BALL — near BGA

PEX_PLLVDD AG26

+PEX_PLLVDD — C7008 0.1UF/16V — C7010 1UF/6.3V — GND
C7006 4.7UF/6.3V — GND
SL7006 0805 — +PEX_VDD Max:120mA — C7019 1UF/6.3V — GND

TESTMODE AK11 — R7015 10KOhm — GPU_TESTMODE

PEX_TERMP AP29 — R7019 1% 2.49KOhm — PEX_TERMP — GND

Control Signal from PCH

+3VSG_AON — R7021 10KOhm

GPIO17

22,25 DGPU_PWROK

R1.1-5/8/18

D7002 1N4148WS 07G001001131 — +3VSG_AON
R7003 2.2KOHM — +3VSG_AON
C7003 1UF/6.3V — GND

77,91 PS_PGOOD_NV_FB — D7001 BAT54CW

93 +FBVDDQ_PWRGD — R7025 @ 0Ohm
92 +PEXVDD_PWRGD — R7024 0Ohm

R1.1-5/13-2

	R7003	C7003
/GC6 10	1 Kohm	0.022uF/25V
/GC6 20	2.2 Kohm	1uF/6.3V

C7099 100PF/50V @ — GND

7,24,30,33,40,46,53 BUF_PLT_RST#

25 GPU_RST# — SL7007 0402 — GPU_RST#_R

GPIO50

U7002 74LVC1G08GW (INB, INA, GND, VCC, OUTY) — +3VSG_AON
R7018 100KOhm

SL7002 0402 /GC6 20 — SYS_PEX_RST_MON# — SYS_PEX_RST_MON# 75
C7098 100PF/50V @

GC6_2.0

C7097 0.1UF/16V @ EMI — GND

GC6_2.0

75 GPU_PEX_RST_HOLD#

U7004 74LVC1G08GW (INB, INA, GND, VCC, OUTY) — +3VSG_AON
SYS_PEX_RST_MON# — DGPU_RST# — DGPU_RST# 75
R7006 10KOhm /GC6 20 — GND

6,30,45,57,84,88 SUSB_EC#

SL7003 0402 — SUSB#_PWR_R

U7003 74LVC1G08GW (INB, INA, GND, VCC, OUTY) — +3VSUS — GPU_PWR_EN 77

+3VS — R7010 10KOhm — GND

GPU_PWRON — R7013 @ 0Ohm

GPIO54

25 DGPU_PWR_EN#

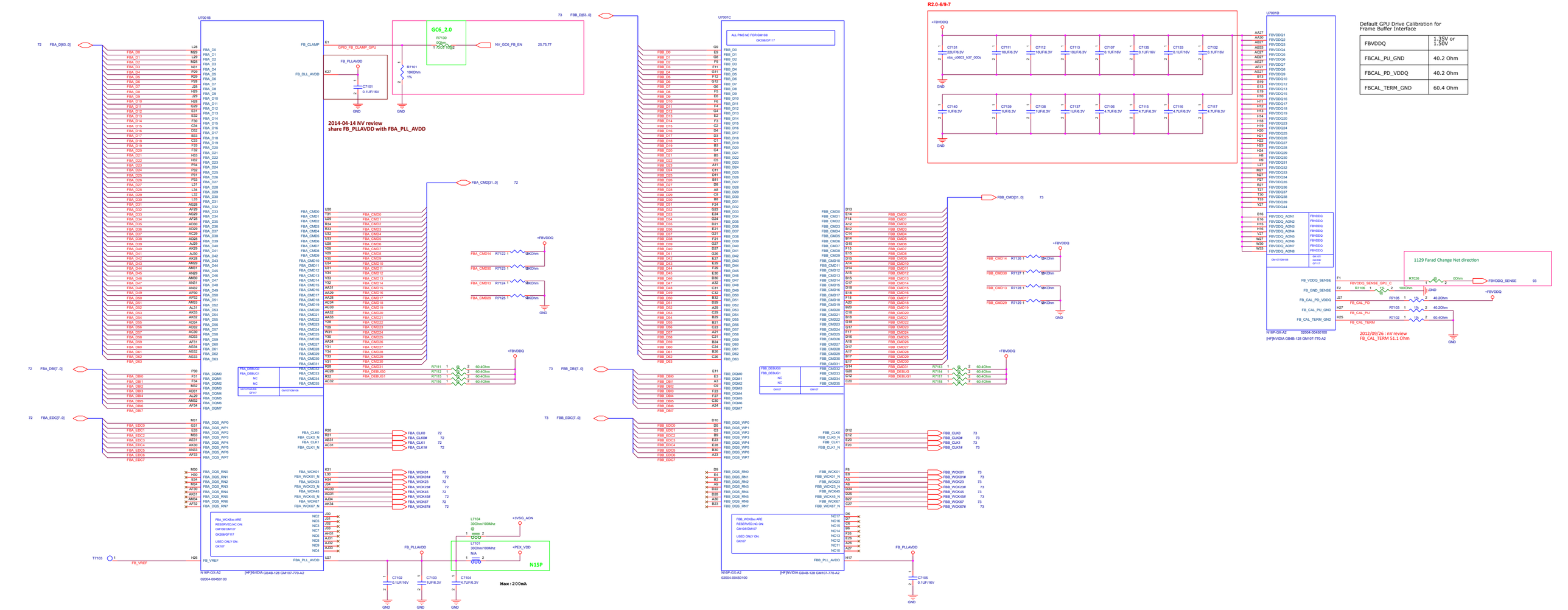
Q7001 2N7002K — R7016 1KOhm — GND — R7022 100KOhm — GND

<Variant Name>

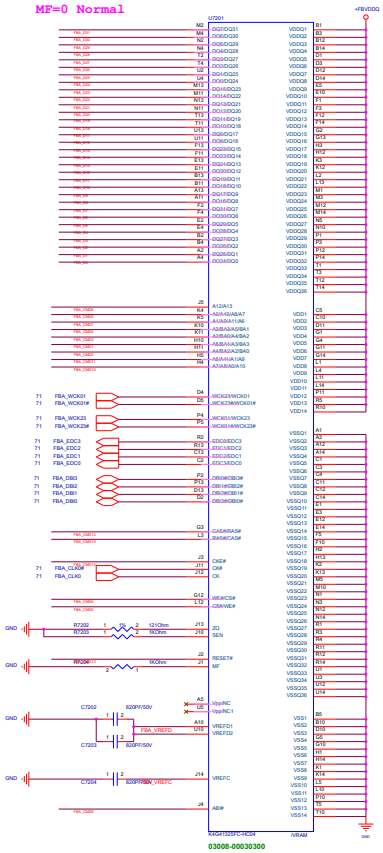
ASUSTeK COMPUTER INC. NB1	Title :	GPU_PCI-EXPRESS(1)	
	Engineer:	Mario_Jhu	
Size: Custom	Project Name: GL552VW		Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 70 of 103		

GPU MEMORY INTERFACE: PARTITION A

GPU MEMORY INTERFACE: PARTITION B



MF=0 Normal



FBA Partition Memory (1 of 2)

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

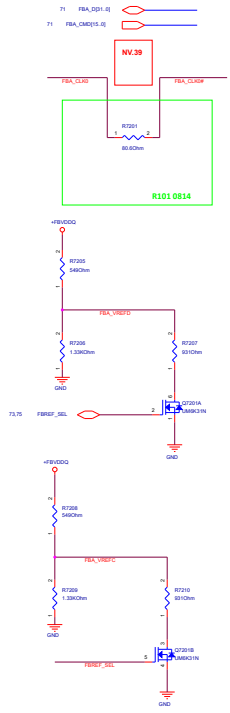
USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)

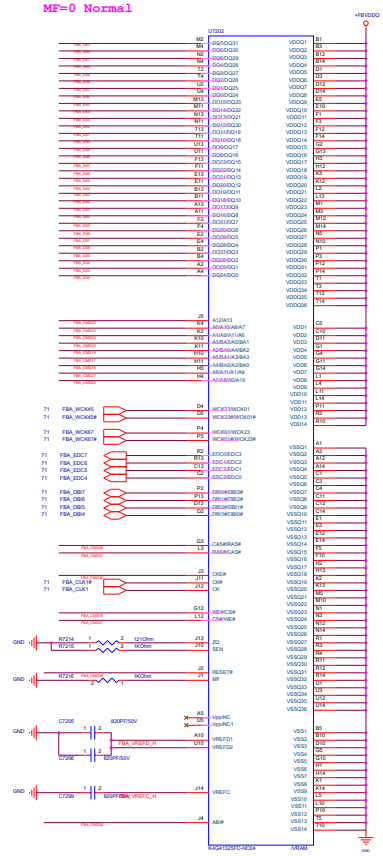
2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

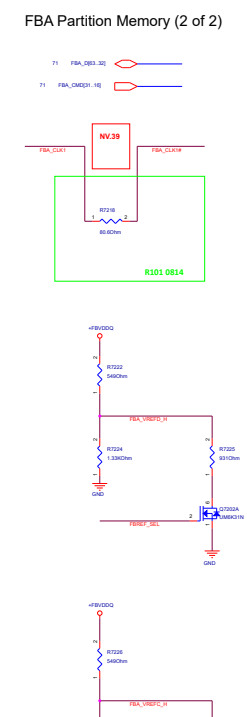
	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm



MF=0 Normal



FBA Partition Memory (2 of 2)



MF=0 Normal

FBB Partition Memory (1 of 2)

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)

2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

	PR9310
+1.35V	8.06Kohm
+1.5V	10Kohm

03008-00030300

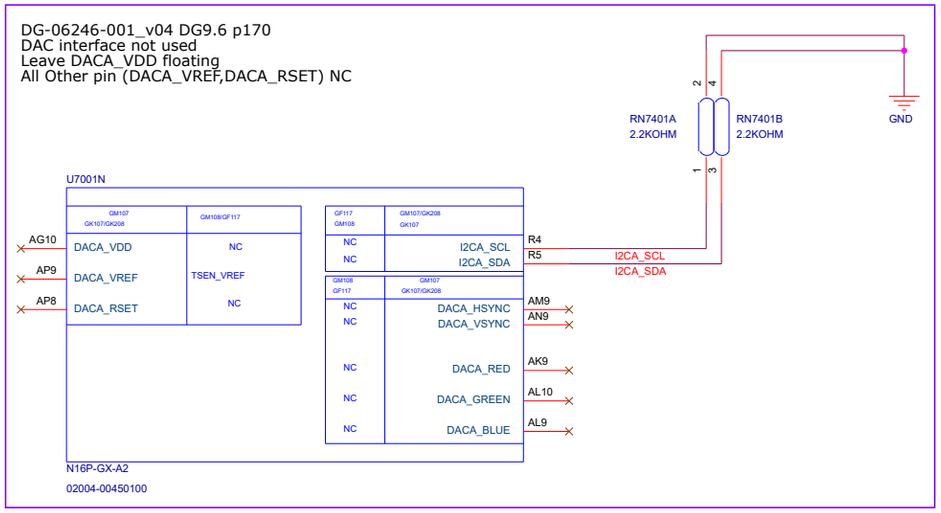
MF=0 Normal

FBB Partition Memory (2 of 2)

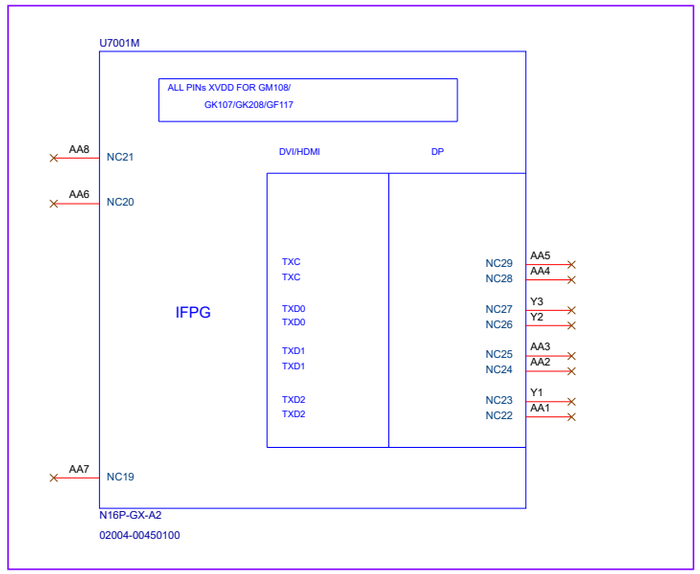
03008-00030300

DG-06246-001_v02 DG10.2.1 p168
Unused I2C should be soft grounded or
PU 3.3V via 2.2kOhm

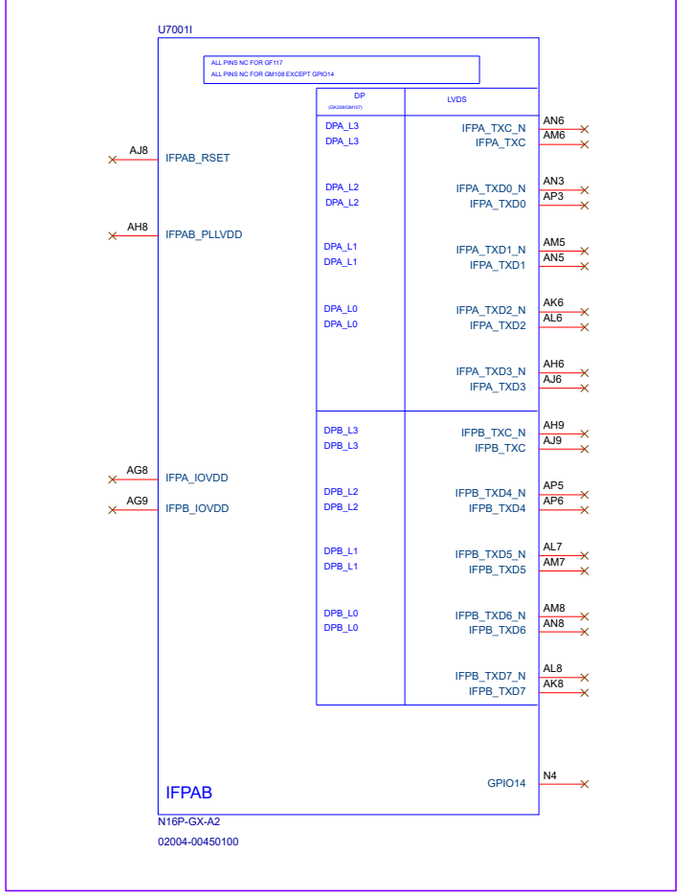
CRT DAC_A



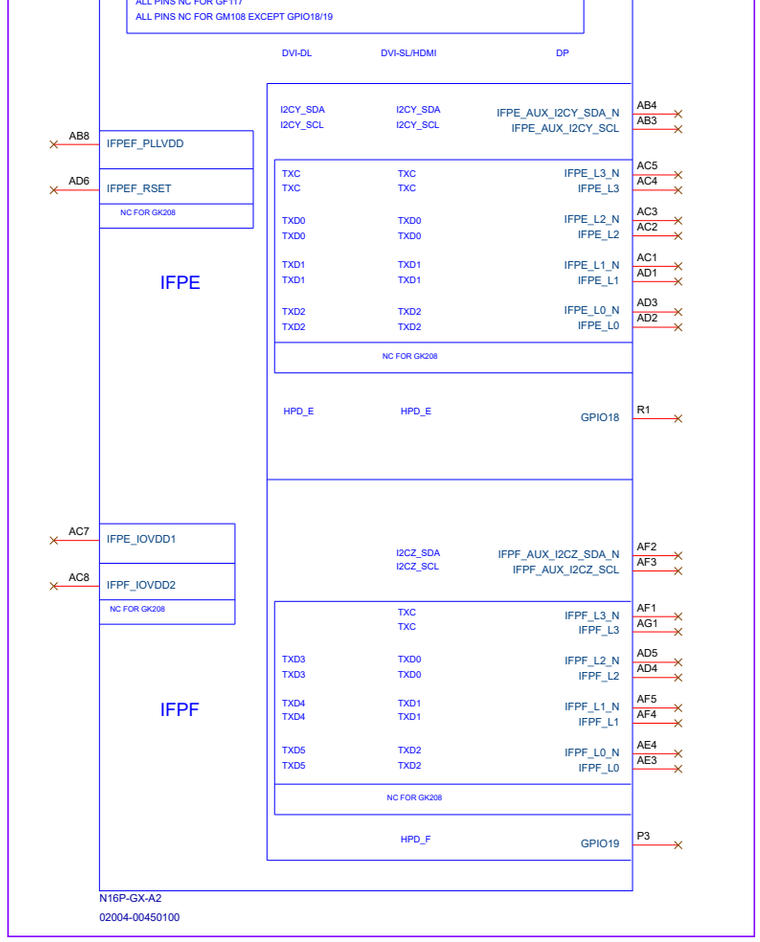
LVDS IFPG



LVDS IFPA/B



LVDS IFPE/F



<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : VGA_CRT/LVDS(5)

Engineer: Mario_Jhu

Size	Project Name	Rev
C	GL552VW	2.0

Date: Tuesday, June 23, 2015 Sheet 74 of 103

DG-07158-001_v05_secured Table 12-2.

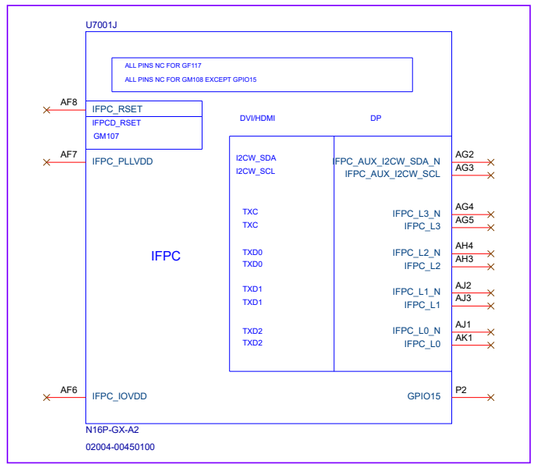
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	OUT	Low	GC6_FBEN
1	OUT	High/Low	MEM_VDD_CTL
2	OUT	Low	LCD_BL_PWM
3	OUT	Low	LCD_VCC
4	OUT	Low	LCD_BLEN
5	OUT	High	3V3_MAIN_EN
6	IN	High	GPU_EVENT#
7	OUT	Low	3DVision
8	IN	High	SYS_PEX_RST_MON#
9	I/O	High	THERM_ALERT
10	OUT	Low	MEM_VREF_CTL
11	OUT		PWM_VID
12	IN	High	PWR_LEVEL
13	OUT	High	PSI
14	IN	Fig. 12-1	HPD_IFPAB
15	IN	Fig. 12-1	HPD_IFPC
16	IN	High	FRAME_LOCK#
17	IN	Fig. 12-1	HPF_IFPD
18	IN	Fig. 12-1	HPD_IFPE
19	IN	Fig. 12-1	HPD_IFPFB
20			Reserved
21	OUT	High	GPU_PEX_RST_HOLD#
OVERT	I/O	High	OVERT

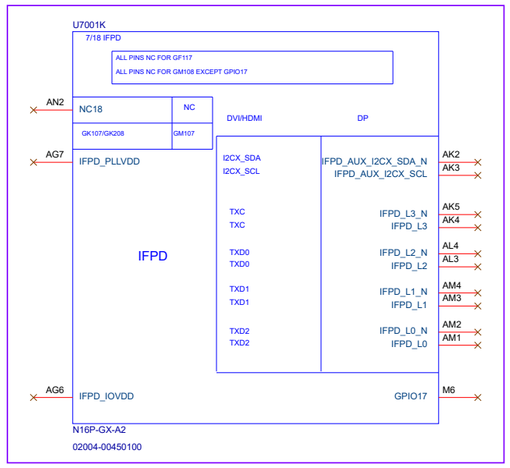
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

DG-06246-001_v02 p157 DG8.6
IPF not used
IFPxy_IOCDD/IFPxy_PLLVDD 10K PD
Other pin NC

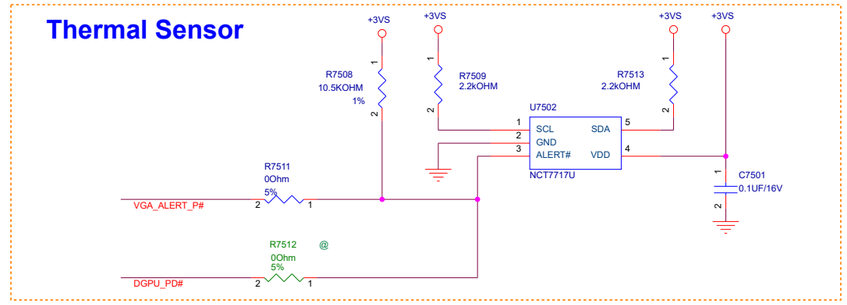
DP(link C)



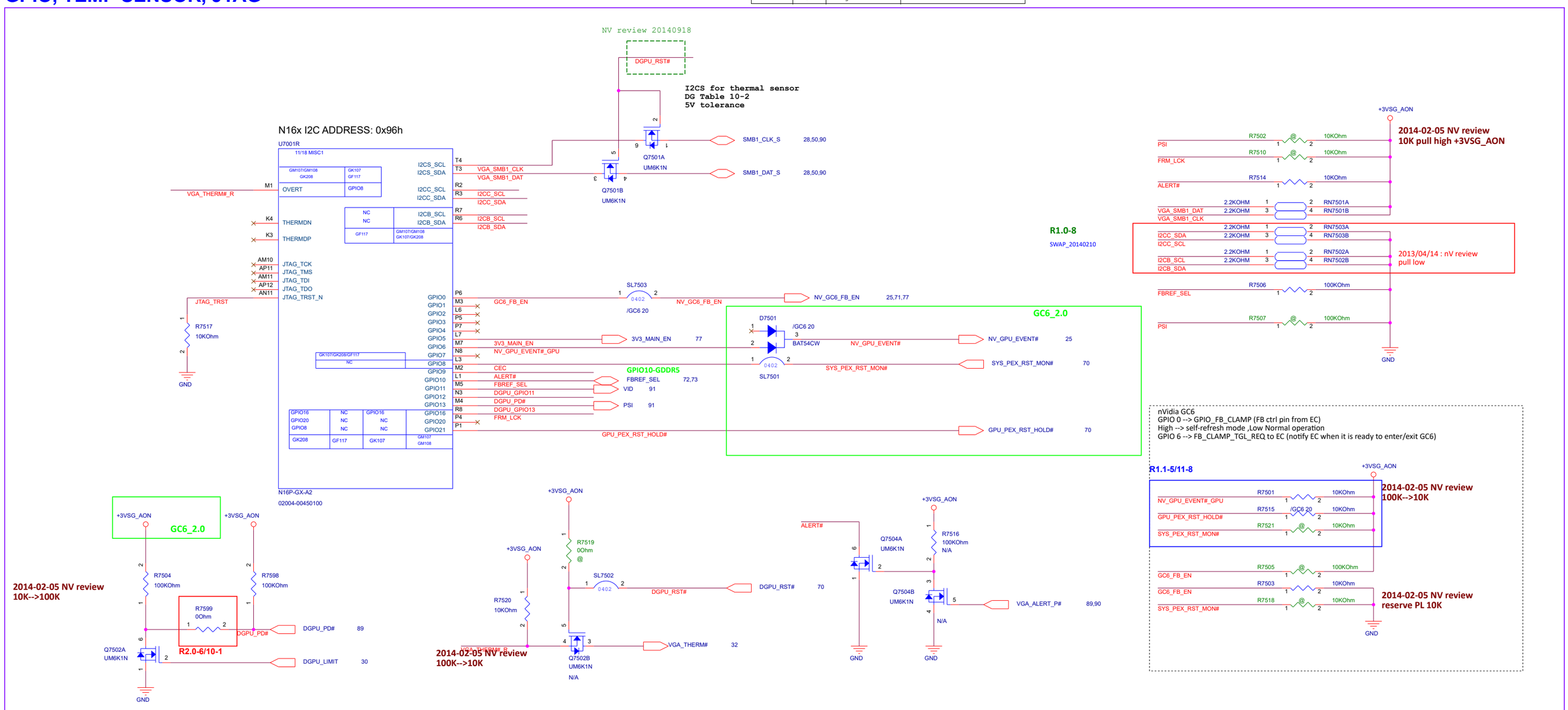
DVI(link D)



Thermal Sensor



GPIO, TEMP SENSOR, JTAG



<Variant Name>

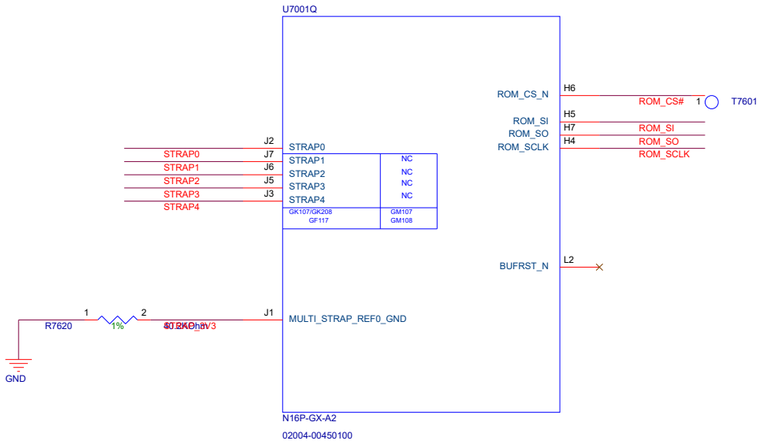
ASUSTeK COMPUTER INC. NB1

Title : VGA_GPIO/DVI/DP(6)

Engineer: Mario_Jhu

Size	Project Name	Rev
Custom	GL552VW	2.0

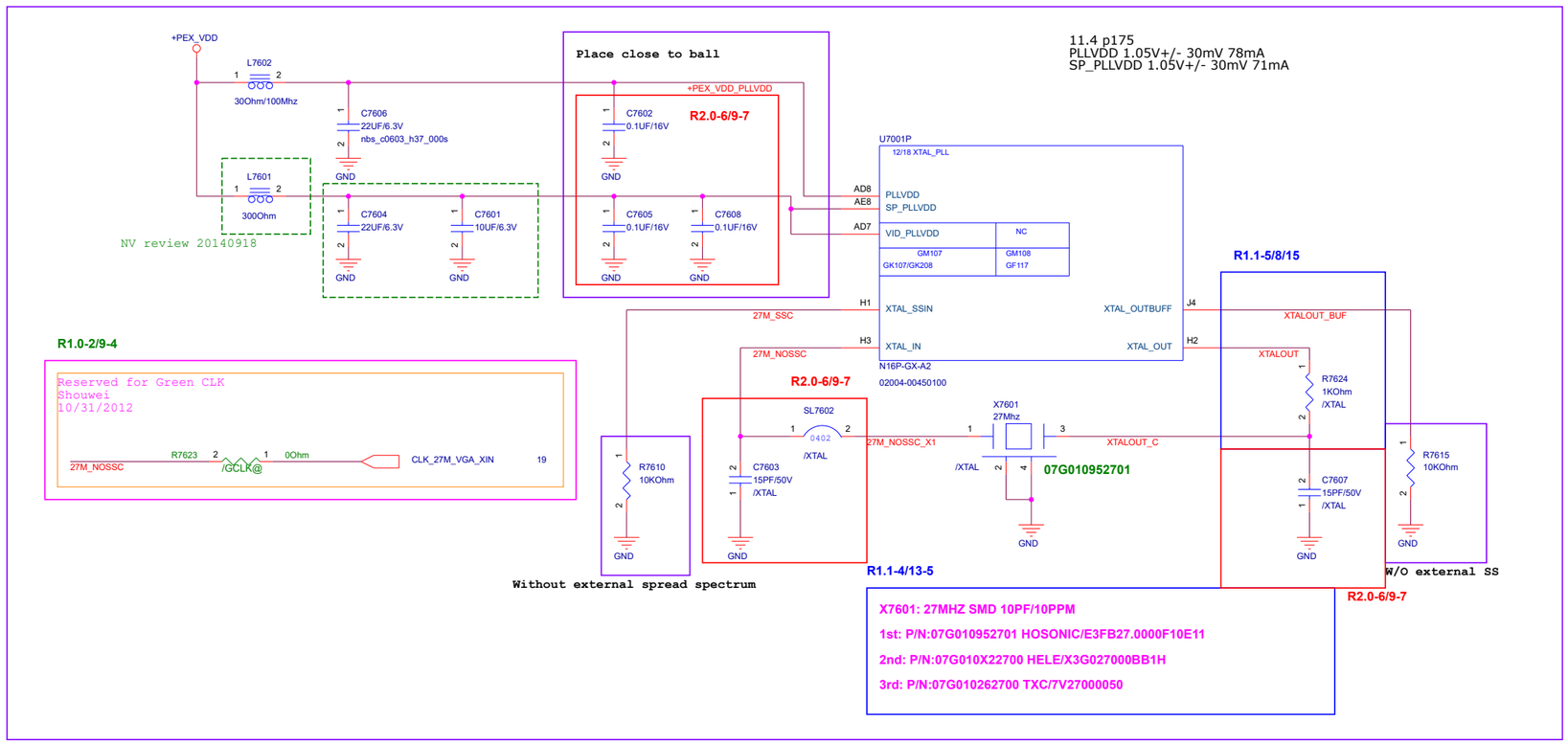
Date: Tuesday, June 23, 2015 Sheet 75 of 103



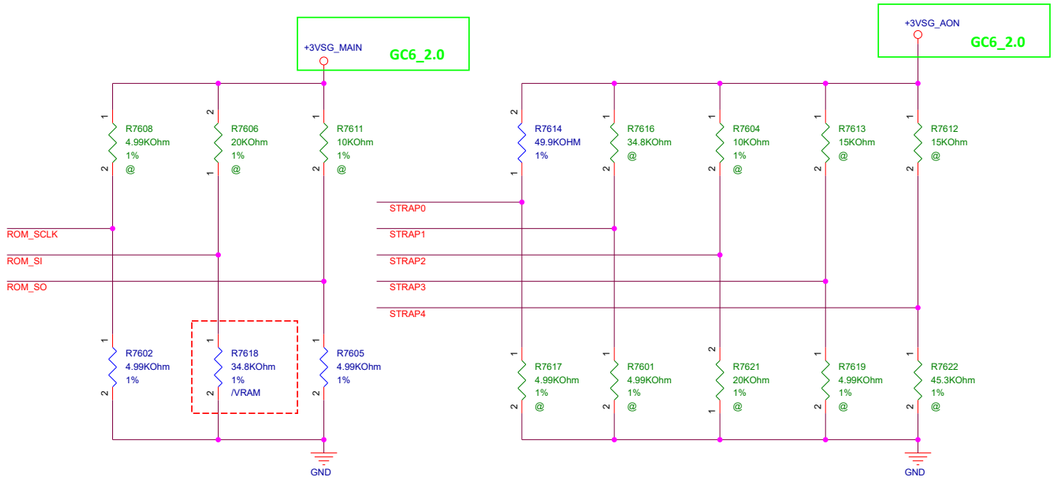
DG-06246-001_v02 DG15.2 p192
Multi_Strap_Ref0_GND 40.2k 1% to GND

DG-06246-001_v02 DG8.4.2.2 p145
N14x GPUs do not support CEC.
Leave the CEC pin as NC

XTAL



STRAPPING OPTIONS for N16P



Change R7618 VRAM Vendor

USE GDDR5 VRAM 128Mb x 32 (512MB)

Hynix strap 0x6 HYNIX/H5GC4H24AJR-T2C - 34.8Kohm +1.35V

Micron strap 0x4 Micron/EDW4032BABG-60-F - 24.9Kohm +1.35V

Samsung strap 0x3 Samsung/K4G41325FC-HC04 - 20Kohm +1.5V non-RVL

DG-07158-001_v05_secured p.197
Table 15-3. GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print fot pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print fot pull-up to 3V3_AON and pull-down to GND. Do not Stuff.			

Table 15-2.

	PU	PD
4.99Kohm	**1000**	**0000**
10.0Kohm	**1001**	**0001**
15.0Kohm	**1010**	**0010**
20.0Kohm	**1011**	**0011**
24.9Kohm	**1100**	**0100**
30.1Kohm	**1101**	**0101**
34.8Kohm	**1110**	**0110**
45.3Kohm	**1111**	**0111**

	PR9310
+1.35V	**8.06Kohm**
+1.5V	**10Kohm**

<Variant Name>

ASUSTeK COMPUTER INC. NB1

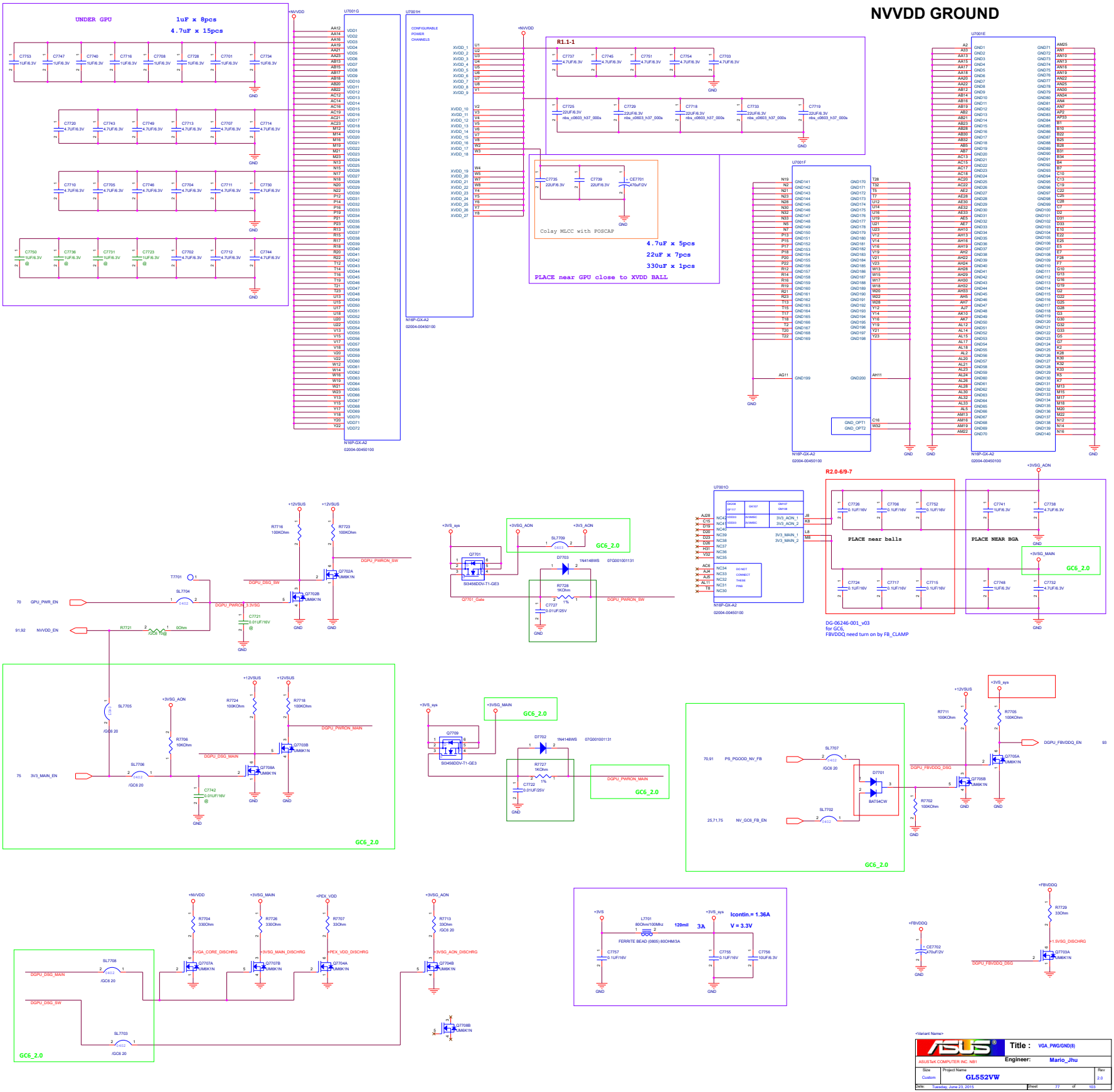
Title : VGA_XTAL/STRAPPING(7)

Engineer: Mario_Jhu

Size	Project Name	Rev
C	GL552VW	2.0

Date: Tuesday, June 23, 2015 Sheet 76 of 103

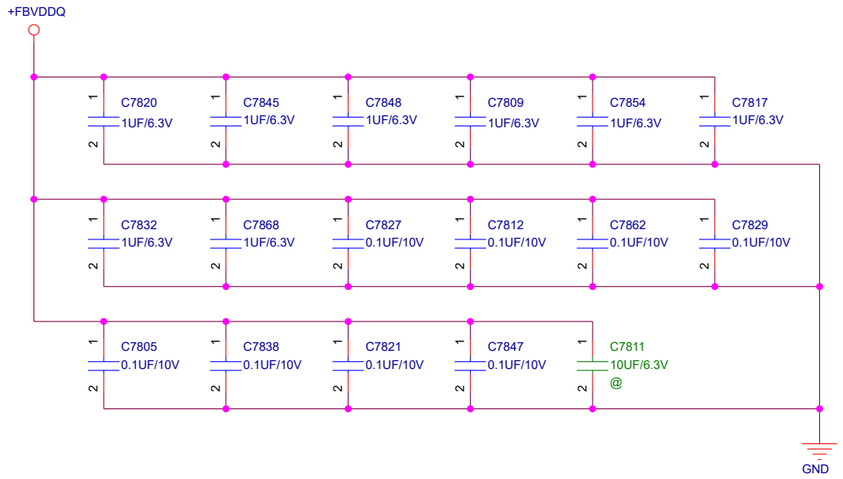
NVVDD POWER AND DECOUPLING



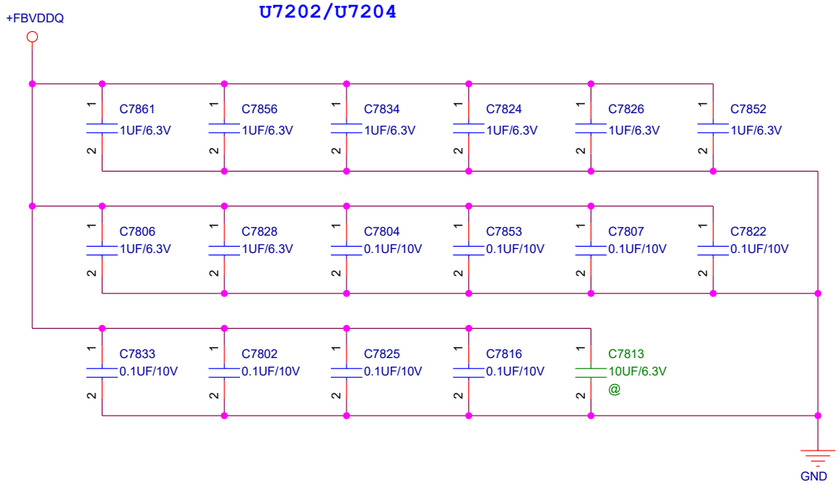
Location is close to DRAM for clamshell mode

0.1uF X8
1uF X 8

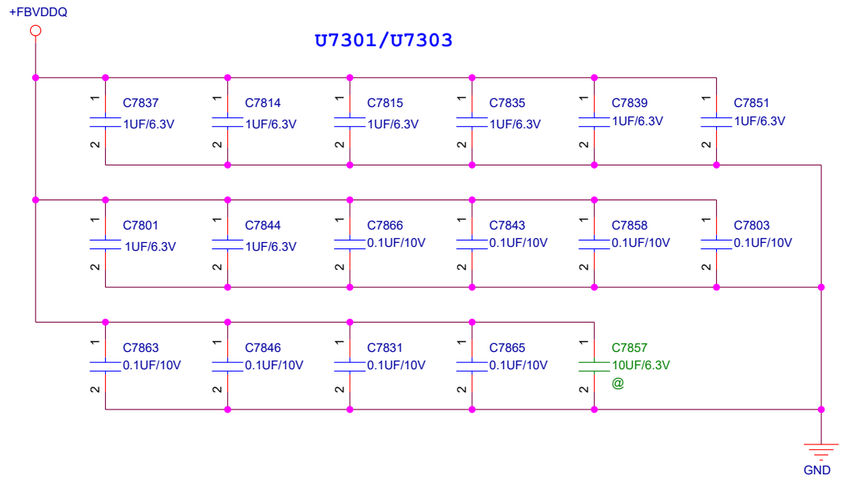
U7201/U7203



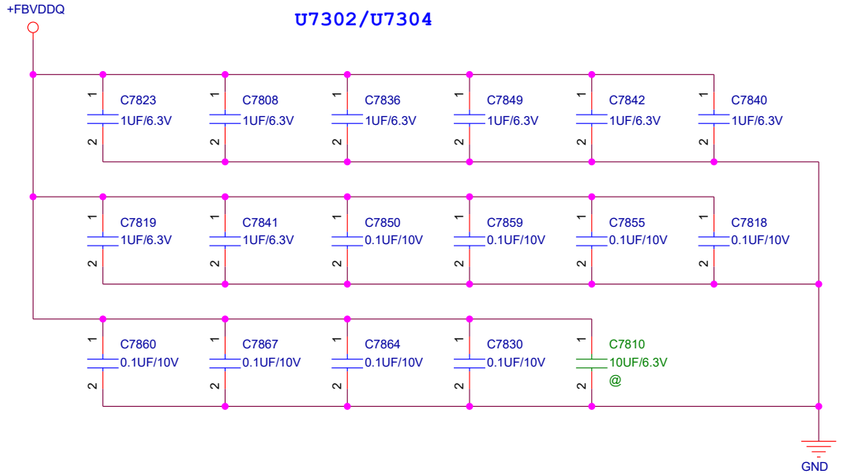
U7202/U7204



U7301/U7303



U7302/U7304



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : VRAM CAP	
	Engineer: Mario_Jhu	
Size: B	Project Name: GL552VW	Rev: 2.0
Date: Tuesday, June 23, 2015	Sheet 78 of 103	

Skylake IMVP8 Power [For CPU]

PTR8006請放靠近PL8105,
附近不可有其他組電感

PJ8009、PJ8008請放靠近CPU Socket下方MLCC上,
PR8047、PR8049、PSL8010、PR8048請放靠近CPU端

PJ8004、PJ8005請放靠近CPU Socket下方MLCC上,
PR8007、PSL8001、PSL8002、PR8008請放靠近CPU端

PJ8006、PJ8007請放靠近CPU Socket下方MLCC上,
PR8038、PSL8003、PSL8004、PR8039請放靠近CPU端

PTR8004請放靠近PL8100,
附近不可有其他組電感

PTR8005請放靠近PL8103,
附近不可有其他組電感

SA
ICCMAX=11A

SA
LL=9.1mohm

VCORE
OCP=120A

VCORE
LL=1.8mohm

GT
LL=2.65mohm

VCORE
ICCMAX=68A

GT
ICCMAX=55A

SA
Fsw=600KHz

CORE&GT
Fsw=500KHz

VCORE Thermal Sense

PTR8002 close to PQ8102

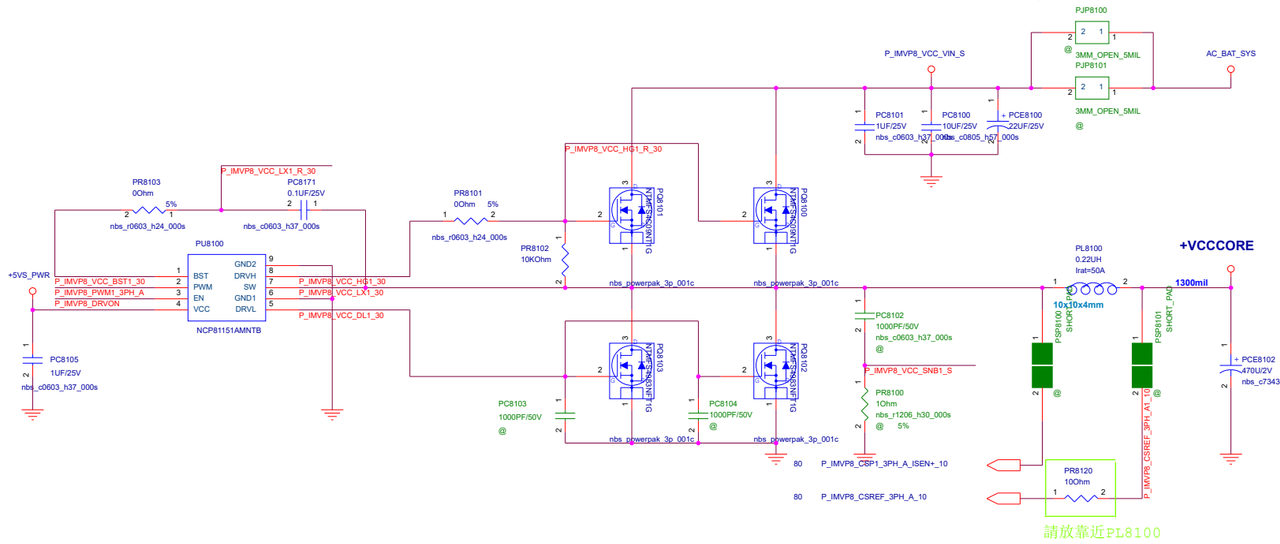
GT Thermal Sense

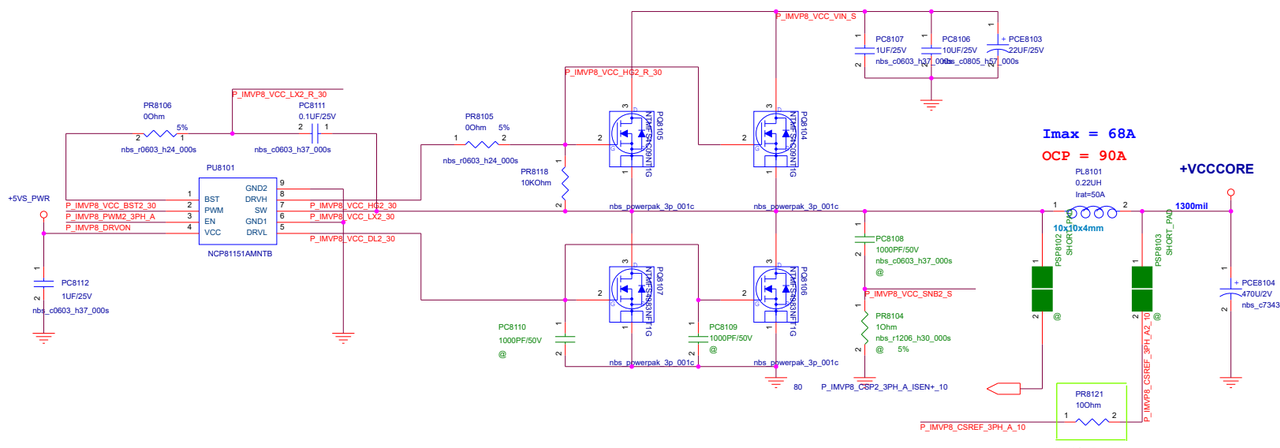
PTR8002 close to PQ8114

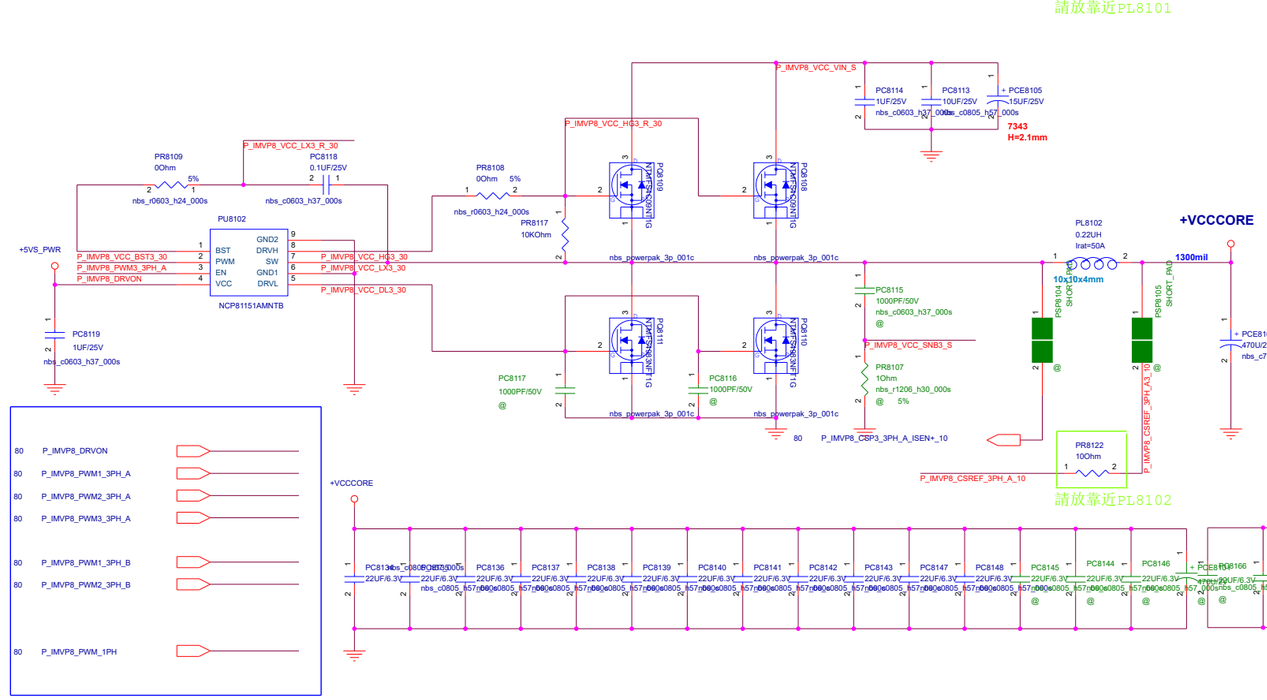
<variant_name>

ASUS	Project Name: Skylake-H		Rev: 2.0
Title : PW_SKYLAKE (1)			
Size: D	Dept.: NB Power team	Engineer: Edison	
Date: Tuesday, June 23, 2015	Sheet 80 of 103		

Skylake IMVP8 Power [For CPU]







80 P_IMVP8_DRVON
80 P_IMVP8_PWM1_3PH_A
80 P_IMVP8_PWM2_3PH_A
80 P_IMVP8_PWM3_3PH_A
80 P_IMVP8_PWM1_3PH_B
80 P_IMVP8_PWM2_3PH_B
80 P_IMVP8_PWM_1PH

+VCCCORE

PC8134 PC8135 PC8136 PC8137 PC8138 PC8139 PC8140 PC8141 PC8142 PC8143 PC8147 PC8148 PC8145 PC8144 PC8146 + PCE8107 PC8166 PC8165 PC8164 PC8163 PC8162

+VCCGT

PC8152 PC8153 PC8154 PC8155 PC8156 PC8157 PC8158 PC8159 PC8160 PC8161 + PCE8111 + PCE8114 PC8179 PC8180 PC8181 PC8182 PC8183 PC8184

22UF/6.3V nbs_c0805_h57_000s @

+VCCSA

<Variant Name>

ASUS	Project Name: Skylake-H		Rev: 2.0
Title : PW_SKYLAKE (2)			
Size: A2	Dept.: NB Power team	Engineer: Edison	
Date: Tuesday, June 23, 2015		Sheet 81 of 103	

Main Board

+1.0VSUS [For PCH]

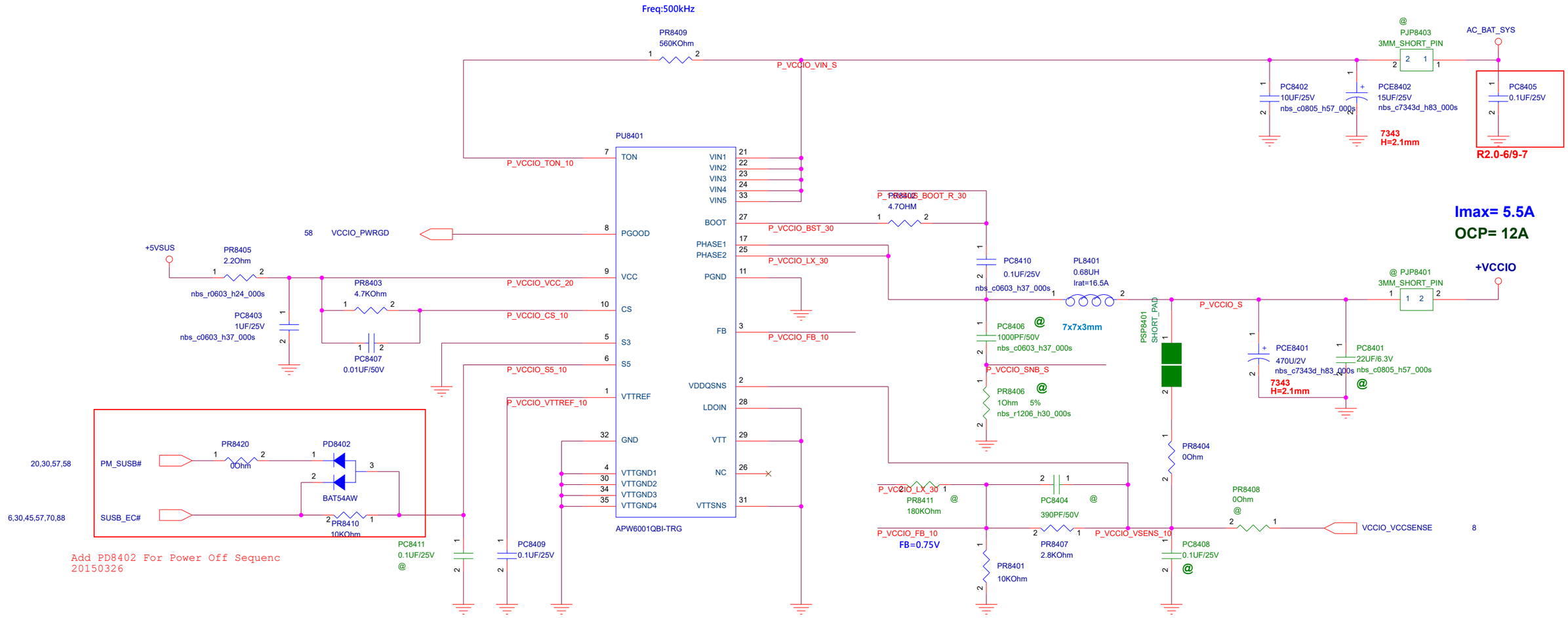
PR8304 620KOhm
P_1.0VSUS_VIN_S
PC8306 0.1UF/25V
P_1.0VSUS_VSENS_10
P_1.0VSUS_VTTREF_10
GND
PU8301 RT8248AGQW
VDDQ VTTREF GND1 VTTSNS VTTGND
GND4 GND3 GND2 VTT VLDOIN BOOT UGATE PHASE
FB S3 S5 TON PGOOD
VID VDD CS PGND LGATE
PD8301 BAT54CW
PR8307 0Ohm
30,57,88 VSUS_ON
58 1.0VSUS_PWRGD
PC8309 0.1UF/25V
P_1.0VSUS_FB_10
P_1.0VSUS_EN_10
P_1.0VSUS_TON_10
P_1.0VSUS_BST_30
P_1.0VSUS_HG_30
P_1.0VSUS_LX_30
PR8303 0Ohm 5% nbs_r0603_h24_000s
P_1.0VSUS_BST_R_30
PC8312 0.1UF/25V nbs_c0603_h37_000s
PR8305 0Ohm nbs_r0603_h24_000s 5%
P_1.0VSUS_DHR_30
PR8309 10KOhm
PQ8301 NTMFS4C08NT1G nba_powerpak_3p_001c
PQ8302 NTMFS4C06NT1G nba_powerpak_3p_001c
PC8307 2200PF/50V
PC8304 0.1UF/25V
PC8303 1UF/25V nbs_c0603_h37_000s @
PCE8301 15UF/25V nbs_c7343d_h83_000s 7343 H=2.1mm
PJP8301 3MM_SHORT_PIN @
AC_BAT_SYS
PC8308 0.1UF/25V @
Imax= 8A
OCP= 16A
PL8301 0.68UH Irat=16.5A 7x7x3mm
PJP8302 3MM_SHORT_PIN @
PJP8303 3MM_SHORT_PIN @
+1.0VSUS
480mil
P_1.0VSUS_VO_S
PC8305 1000PF/50V nbs_c0603_h37_000s @
P_1.0VSUS_SNB_S
PR8302 1Ohm 5% nbs_r1206_h30_000s @
PSP8301 SHORT_PAD @
PC8301 22UF/6.3V nbs_c0805_h57_000s
PCE8302 470U/2V nbs_c7343d_h83_000s 7343 H=2.1mm
+5VSUS
PR8311 5% 2.2Ohm nbs_r0603_h24_000s
PR8312 2.2Ohm nbs_r0603_h24_000s 5%
P_1.0VSUS_VID_10
P_1.0VSUS_VDD_30
P_1.0VSUS_CS_10
P_1.0VSUS_LG_30
PR8314 5% 0Ohm nbs_r0603_h24_000s
PC8310 1UF/25V nbs_c0603_h37_000s
PR8306 91KOhm
PC8311 820PF/50V @
VFB=0.75V
PR8313 3.65KOHM
P_1.0VSUS_FB_10
P_1.0VSUS_VSENS_10
PSL8300 0402 @
P_1.0VSUS_LOSENS_10
PR8310 10KOhm
PC8302 0.1UF/25V
R2.0-6/9-7

+1.0VSUS Discharge for OFF sequence

+3VA
PR8316 100KOhm @
+1.0VSUS
PR8315 33Ohm @
EM6K1-G-T2R PQ8303B @
EM6K1-G-T2R PQ8303A @
VSUS_ON
P_1.0VSUS_DISCHG_10

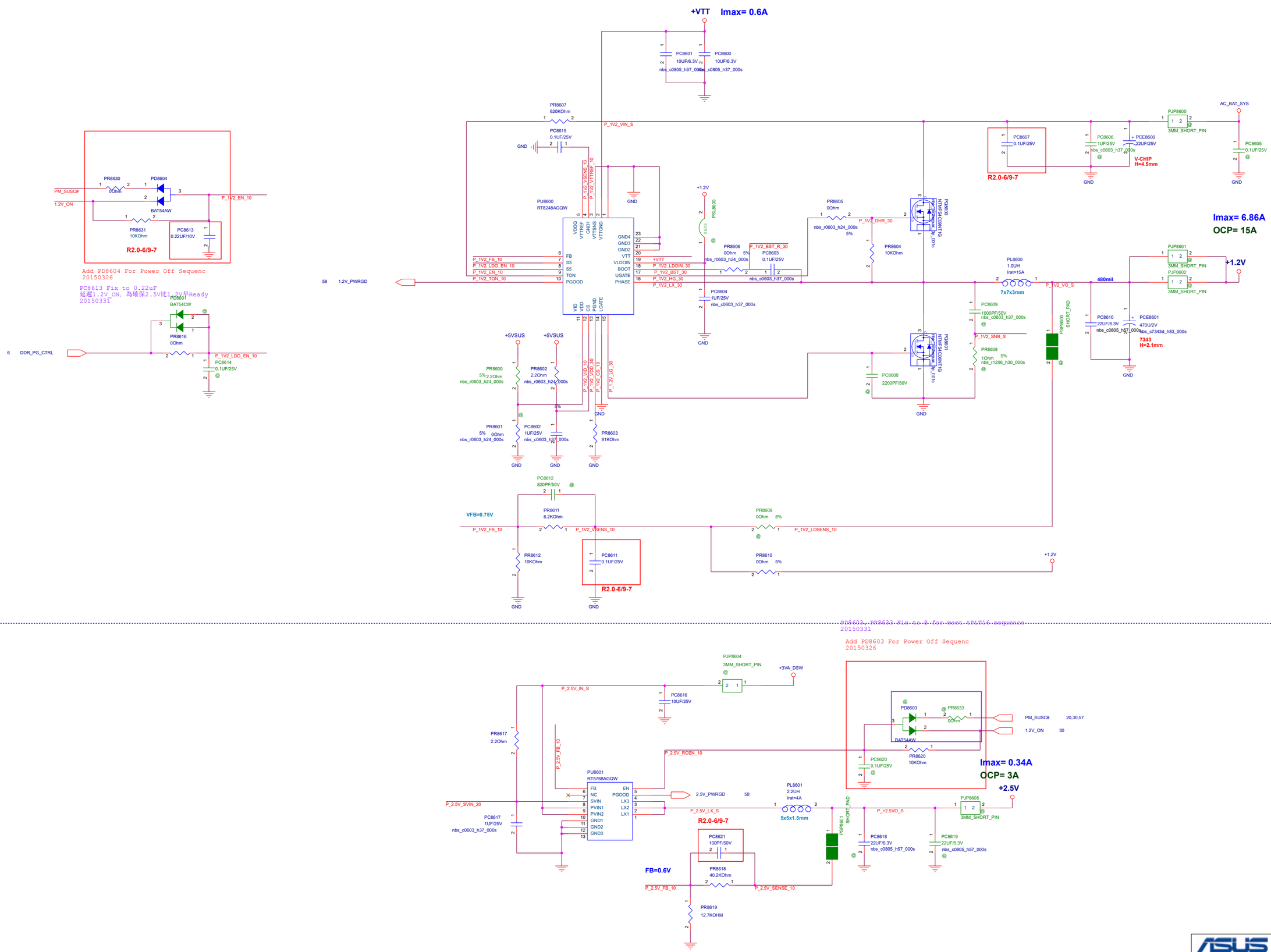
Project Name: GL552VW			Rev: 2.0
Title: PW_+1.0VSUS			
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: Edison	
Date: Tuesday, June 23, 2015	Sheet 83 of 103		

+VCCIO [For CPU]



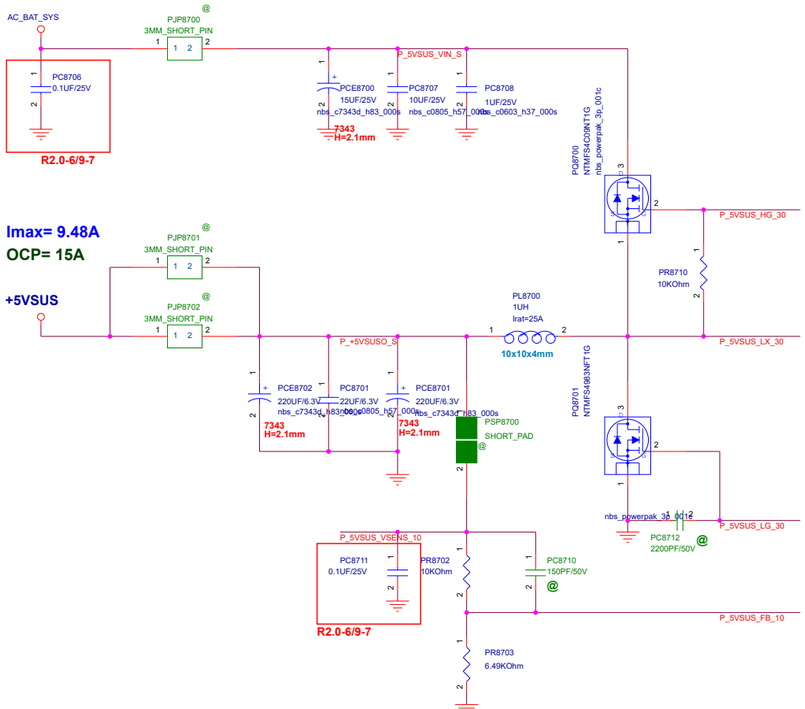
ASUS	Project Name: GL552VW		Rev: 2.0
Title : PW_+VCCIO			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Tuesday, June 23, 2015	Sheet 84 of 103		

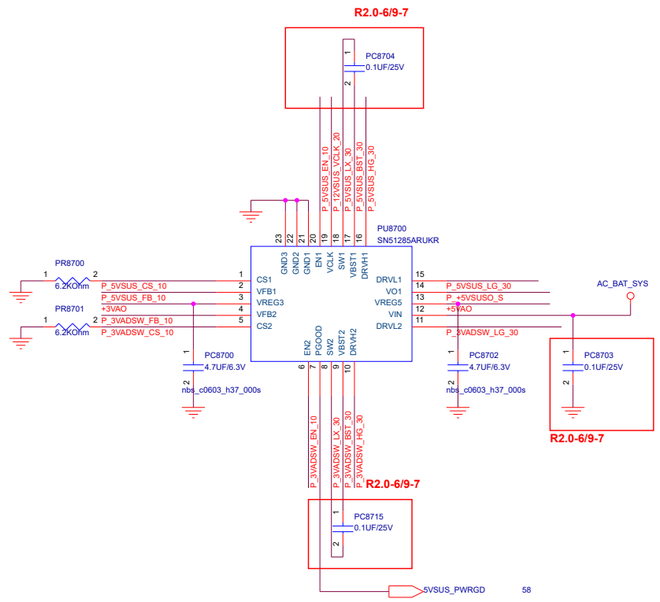
+1.2V / VTT / 2.5V[For Memory]

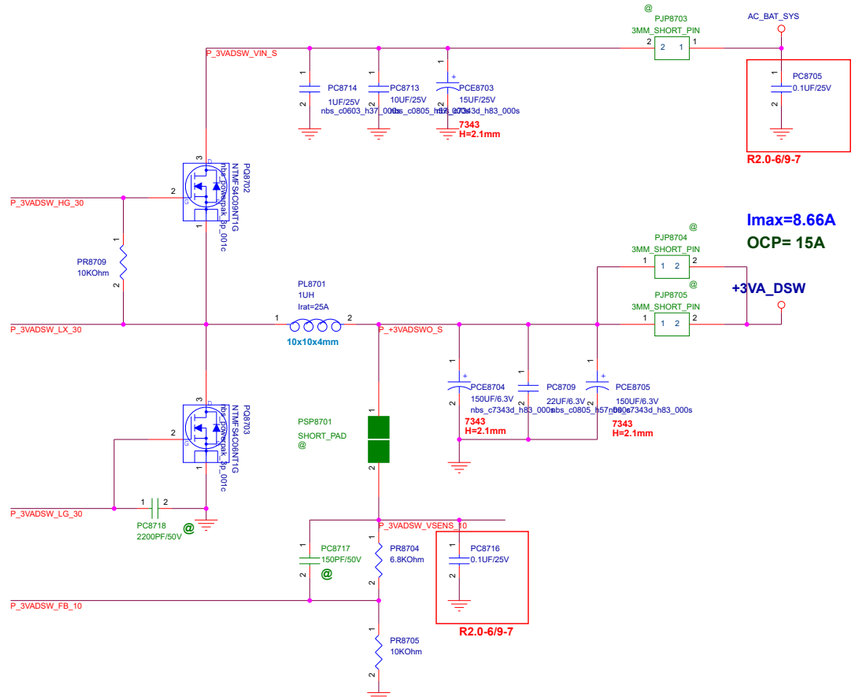


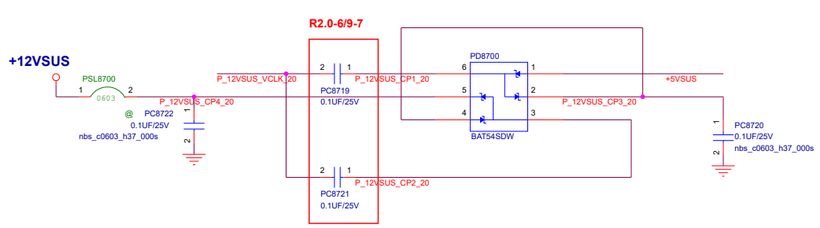
ASUS	Project Name: GL552VW		Rev: 2.0
Title : PW_+1.2V/+VTT/+2.5V			
Size: A2	Dept.: ASUSTeK COMPUTER INC.	Engineer: Edison	
Date: Tuesday, June 23, 2015		Sheet 86 of 103	

+3VA_DSW / +5VSUS [System Power]

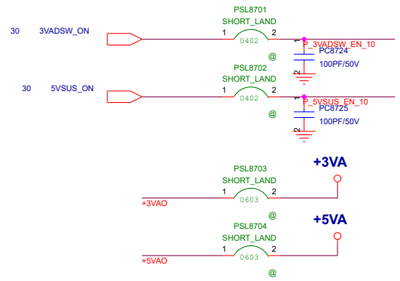


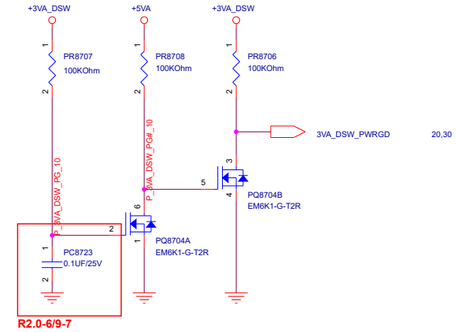






請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



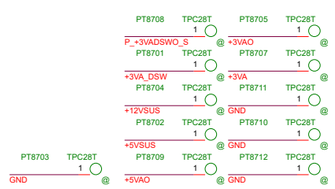


Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0



<variant_name>

ASUS	Project Name: Skylake-H	Rev: 2.0
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Edison
Date: Tuesday, June 23, 2015	Sheet 87 of 103	

Load Switch

Main Board

+3VA_EC

Imax = 0.2A

+3VA → PR8820 0Ohm (30 PS_ON) / PR8819 0Ohm (30,57,83 VSUS_ON) → PU8802 SN1409049DPUR (VIN1_1, VIN1_2, ON1, VBIAS, ON2, VIN2_1, VIN2_2; GND4, GND3, GND2, VOUT1_2, VOUT1_1, CT1, GND1, CT2, VOUT2_2, VOUT2_1)

PC8816 0.1UF/25V

PSL8801 0603 @

PC8801 470PF/50V

PC8817 0.1UF/25V

P_LS_3VA_EC_ON_10 / P_LS_3VSUS_ON_10 / P_LS_3VA_EC_CT_10 / P_LS_3VSUS_CT_10 / +3VA_ECO

R2.0-6/9-7

+3VSUS

Imax = 3.25A

+3V

Imax = 0.5A

PQ8800 PEA28BA

PC8805 0.1UF/25V

P_LS_3V_RC_10 / PC8820 0.01UF/25V / PR8816 100KOhm

R2.0-6/9-7

+3VS

Imax = 3.98A

PQ8801 NTMFS4C06NT1G

PC8828 0.1UF/25V

R2.0-6/9-7

P_LS_3VS_RC_10 / PC8827 0.01UF/25V / PR8804 100KOhm

PR8809 100KOhm (+3VSUS)

PR8813 100KOhm (+3VA_DSW)

PR8802 100KOhm (+3VSUS)

P_LS_3VSUS_PG_10 / P_LS_3VSUS_PG#_10

PC8819 0.1UF/25V

PQ8802A EM6K1-G-T2R

PQ8802B EM6K1-G-T2R

58 P_3VSUS_PWRGD

R2.0-6/9-7

+5V

Imax = 4.78A

PQ8803 NTMFS4C06NT1G

PC8813 0.1UF/25V

P_LS_5V_RC_10 / PC8814 0.01UF/25V / PR8814 10KOhm

R2.0-6/9-7

+5VS_PWR

Imax = 4.66A

PQ8804 PEA28BA

PSL8803 0603 @

PC8823 0.1UF/25V

P_LS_5VS_RC_10 / PC8822 0.01UF/25V / PR8823 10KOhm

R2.0-6/9-7

PSL8803請放置PQ8804旁

R1.1-4/13-5 必上件

+1.0VSUS

Imax = 3.65A

PJP8801 3MM_SHORT_RN

PQ8805 PEA28BA @

PC8803 0.1UF/25V

P_LS_VCCMPHYG_RC_10 / PC8807 0.01UF/25V @ / PR8803 100KOhm @ / P_MPHY_PWREN_10

R2.0-6/9-7

+VCCST

Imax = 0.265A

PQ8806 PEA28BA

PC8808 0.1UF/25V

P_LS_VCCST_RC_10 / PC8809 1UF/25V

PR8806 100KOhm (+12V) / PR8808 100KOhm @ (+12VS)

R2.0-6/9-7

PR8801 1KOhm / PR8815 100KOhm

PQ8810 PMBS3904

PC8806 4.7UF/6.3V

PC8802 0.1UF/25V @

P_LS_VCCST_PG_10

PQ8807A EM6K1-G-T2R

PQ8807B EM6K1-G-T2R

VCCST_PWRGD

+VCCPLL_OC

Imax = 0.26A

P_+VCCPLL_OC_EN_R_10 / SUSC_EC# / SUSB_EC#

PR8807 0Ohm / PR8805 0Ohm @

PD8802 BAT54CW

PR8826 100KOhm

PC8810 0.01UF/25V

P_+VCCPLL_OC_EN_10

PR8817 10Ohm +1.2V

PC8837 1UF/6.3V

PU8801 APL3527GHAI-TRG (VDD, VIN, EN, VOUT, SS, GND)

P_VCCPLL_OC_SS_10

PC8825 0.1UF/25V @

PC8804 0.1UF/25V

R2.0-6/9-7

+12V

PQ8812 PUMD12

20mil / 20mil

P_LS_12V_EN_10

PR8812 1MOhm

30,57 SUSC_EC#

+12VS

PQ8813 PUMD12 @

20mil / 20mil

P_LS_MPHY_EN_10 / P_MPHY_PWREN_10

PR8824 1MOhm @

20 MPHY_PWREN

PQ8814 PUMD12

20mil / 20mil

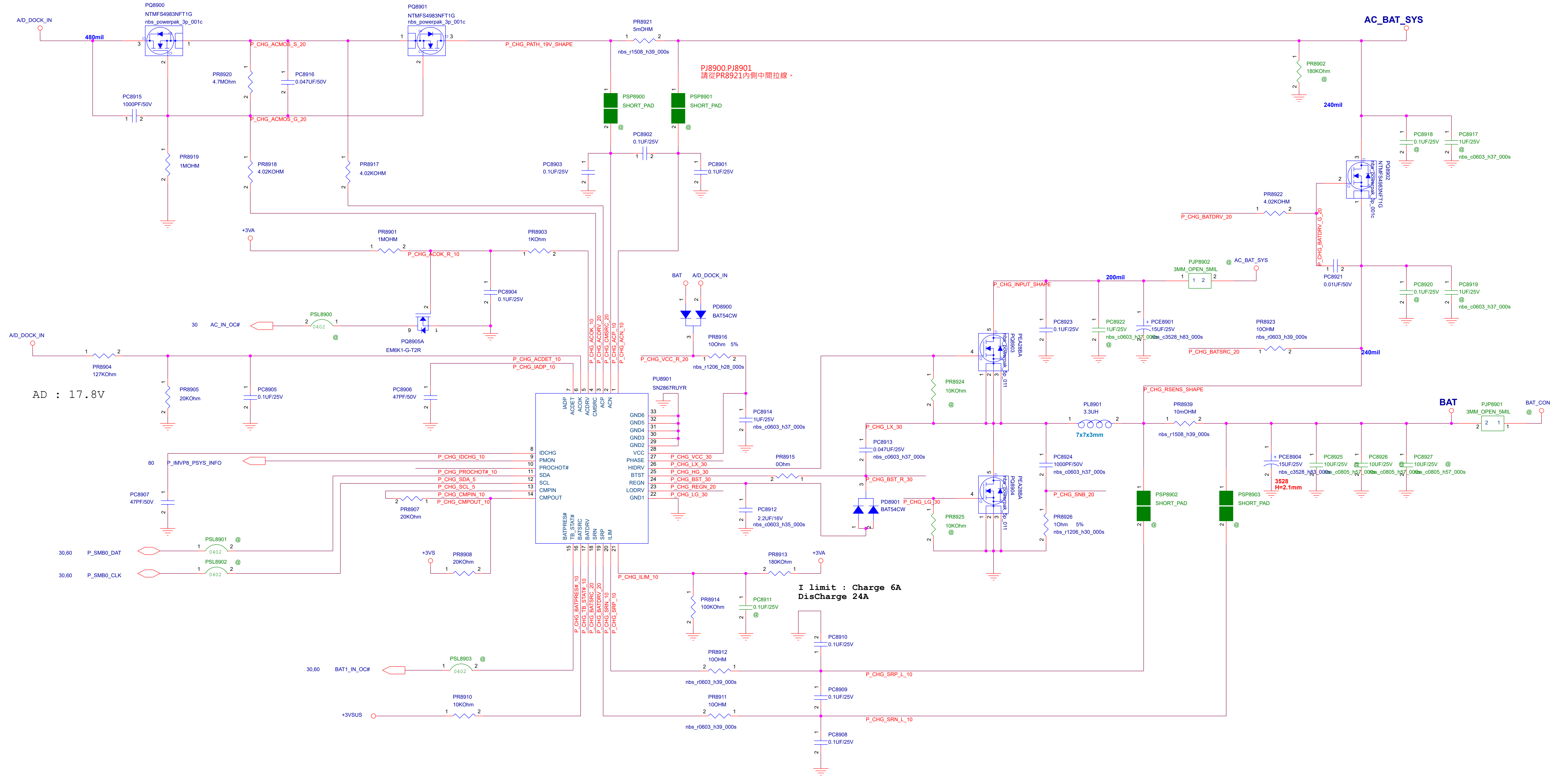
P_LS_12VS_EN_10

PR8810 1MOhm

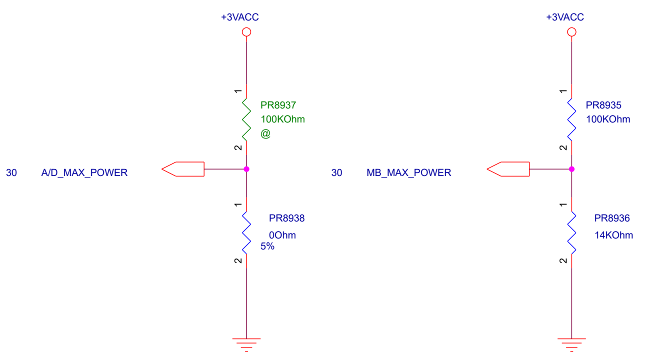
6,30,45,57,70,84 SUSB_EC#

Project Name: GL552VW			Rev: 2.0
Title: PW_LOAD SWITCH			
Size: A3	Dept.: ASUSTeK COMPUTER INC. (ESC)	Engineer: Edison	
Date: Tuesday, June 23, 2015		Sheet 88 of 103	

	<=40W	<=120W	>=120W
PR8921	25m	10m	5m
	EPC	NB	G

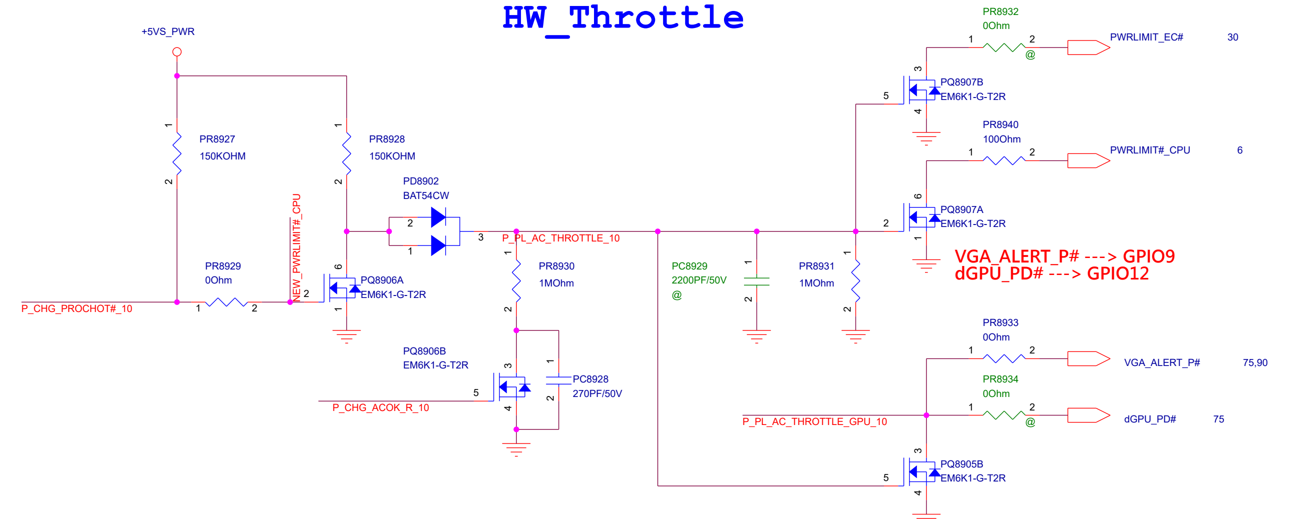


Adaptor select



Adaptor select			
		N Series	G Series
PR8936		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	300W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle



Project Name: GL552VW
Rev: 2.0
Title : PW_CHARGER
Size: A2
Dept.: ASUSTeK COMPUTER INC.
Engineer: Edison
Date: Tuesday, June 23, 2015
Sheet 89 of 102

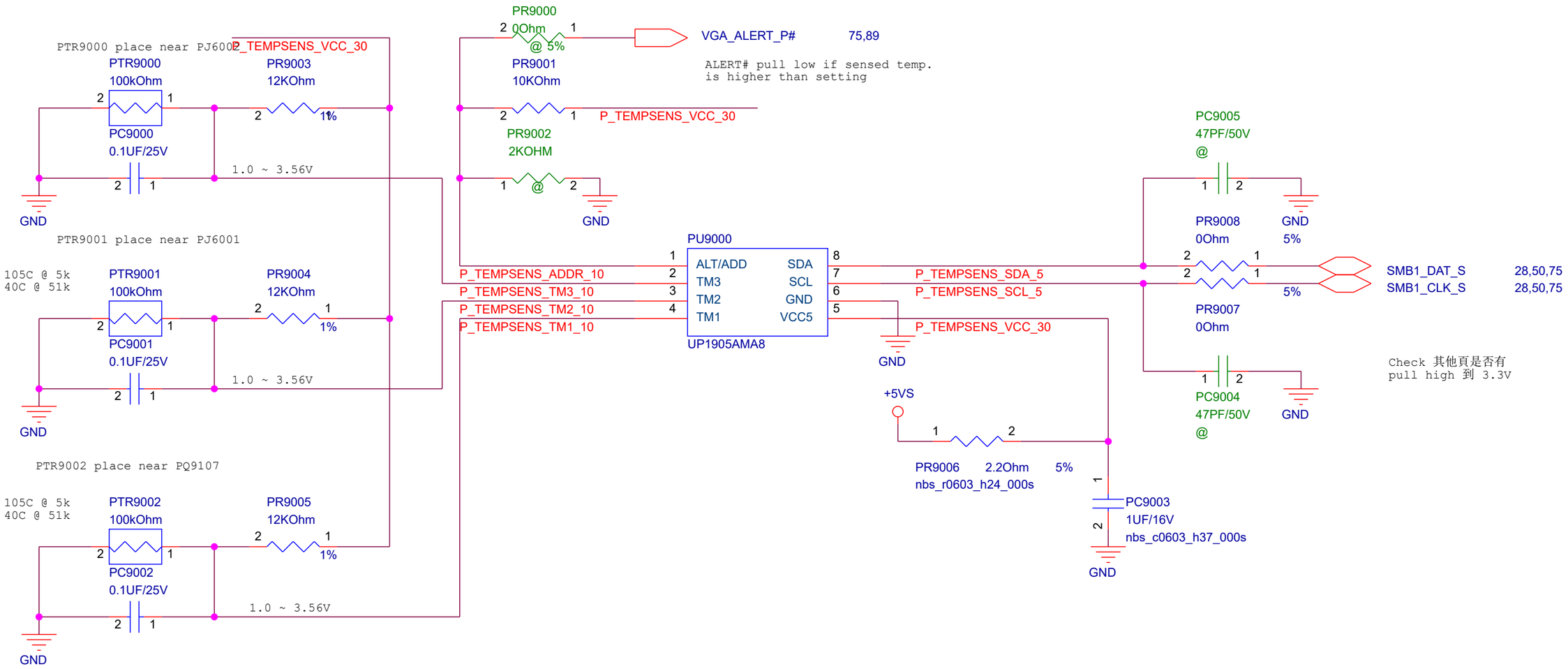
Main Board

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9404	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9405	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



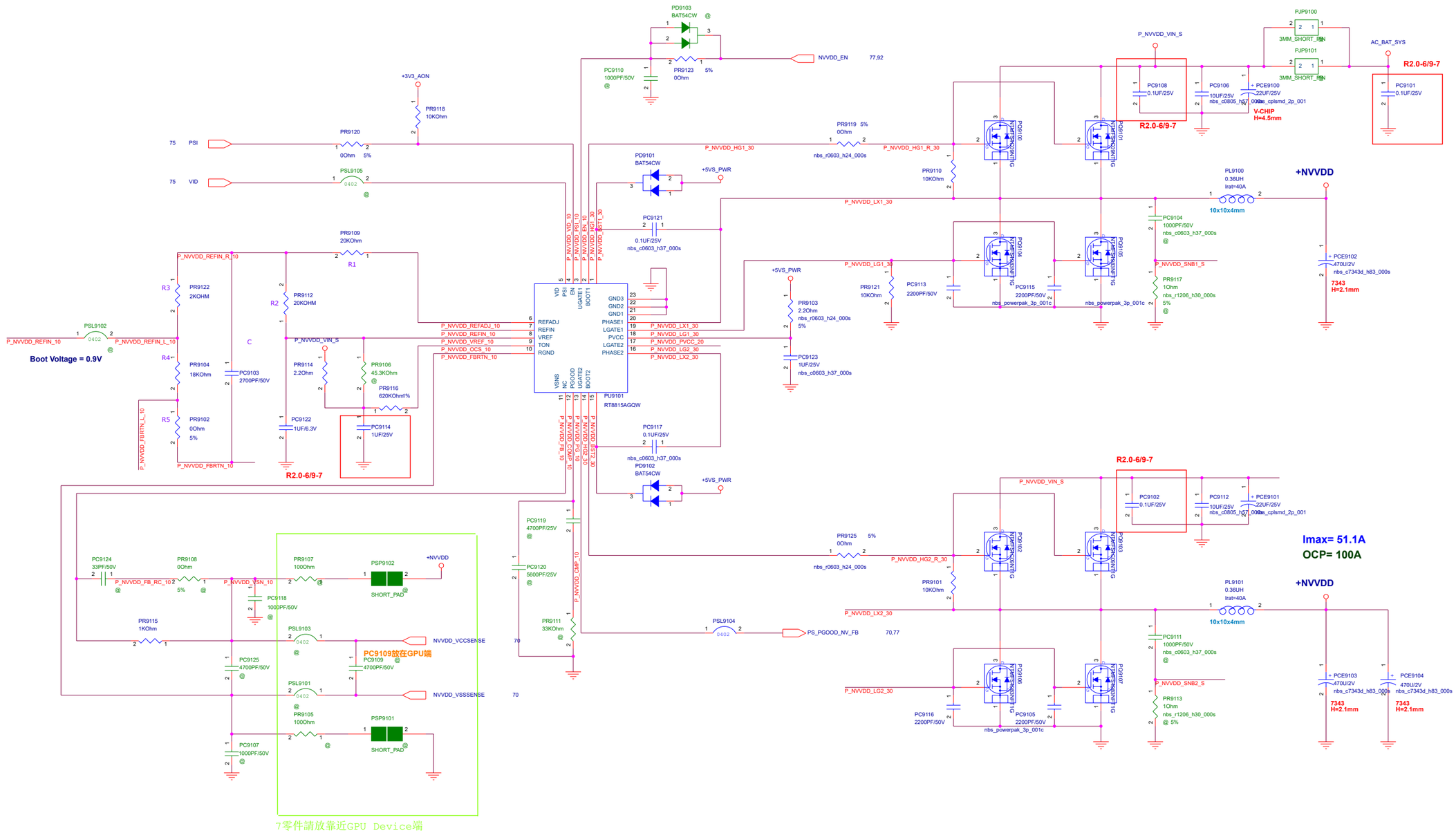
Project Name: GL552VW		Rev: 2.0
Title : PW_PROTECTION		
Size: A4	Dept.: ASUSTeK COMPUTER INC. MB	Engineer: Edison
Date: Tuesday, June 23, 2015	Sheet 90	of 103

+NVVDD [For DGPU]

PWM-VID Spec

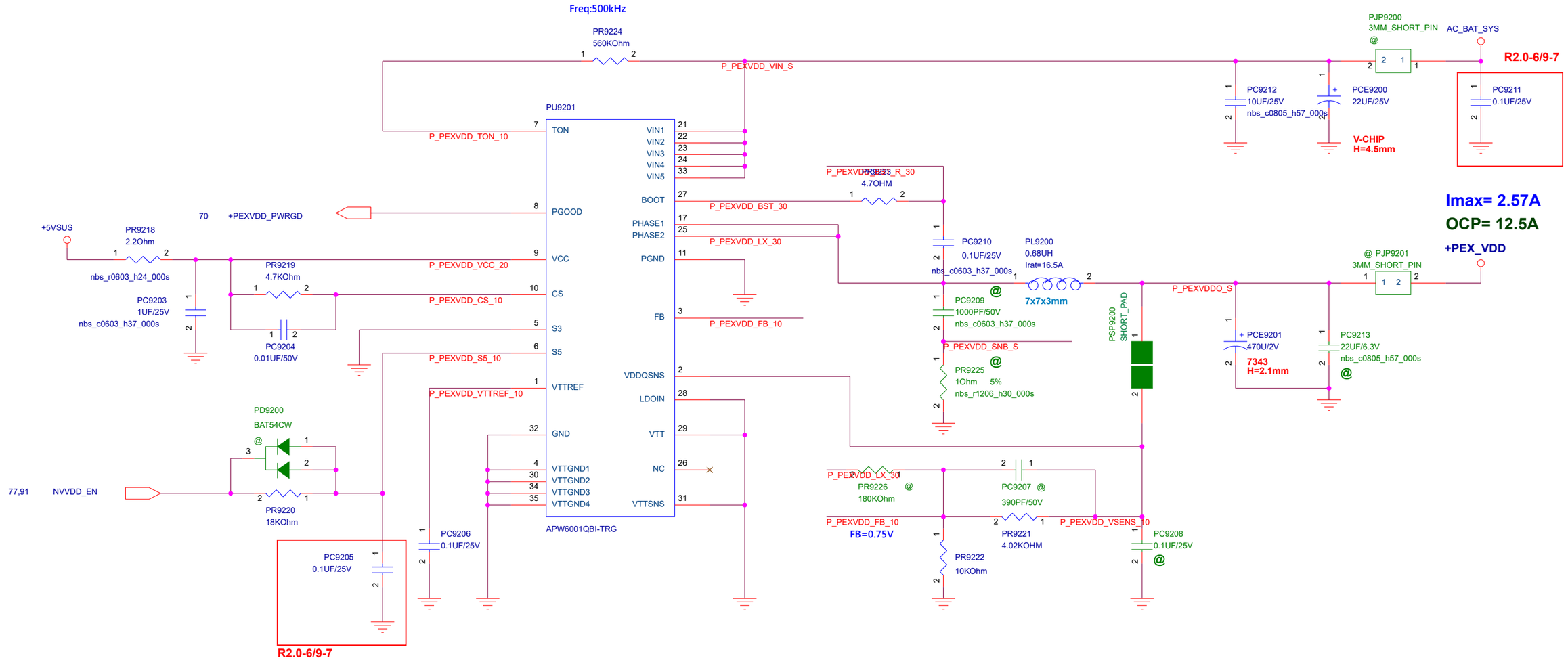
	Config A	Config B
R1 (kohm)	39	20
R2 (kohm)	39	20
R3 (kohm)	1.5	2
R4 (kohm)	30	18
R5 (kohm)	1.5	0
C (nF)	1.5	2.7

Boot Voltage = 0.9V



Project Name: GL552VW			Rev: 2.0
Title : PW_+NVVDD			
Size: A2	Dept.: ASUSTeK COMPUTER INC.	Engineer: Edison	
Date: Tuesday, June 23, 2015		Sheet 91 of 103	

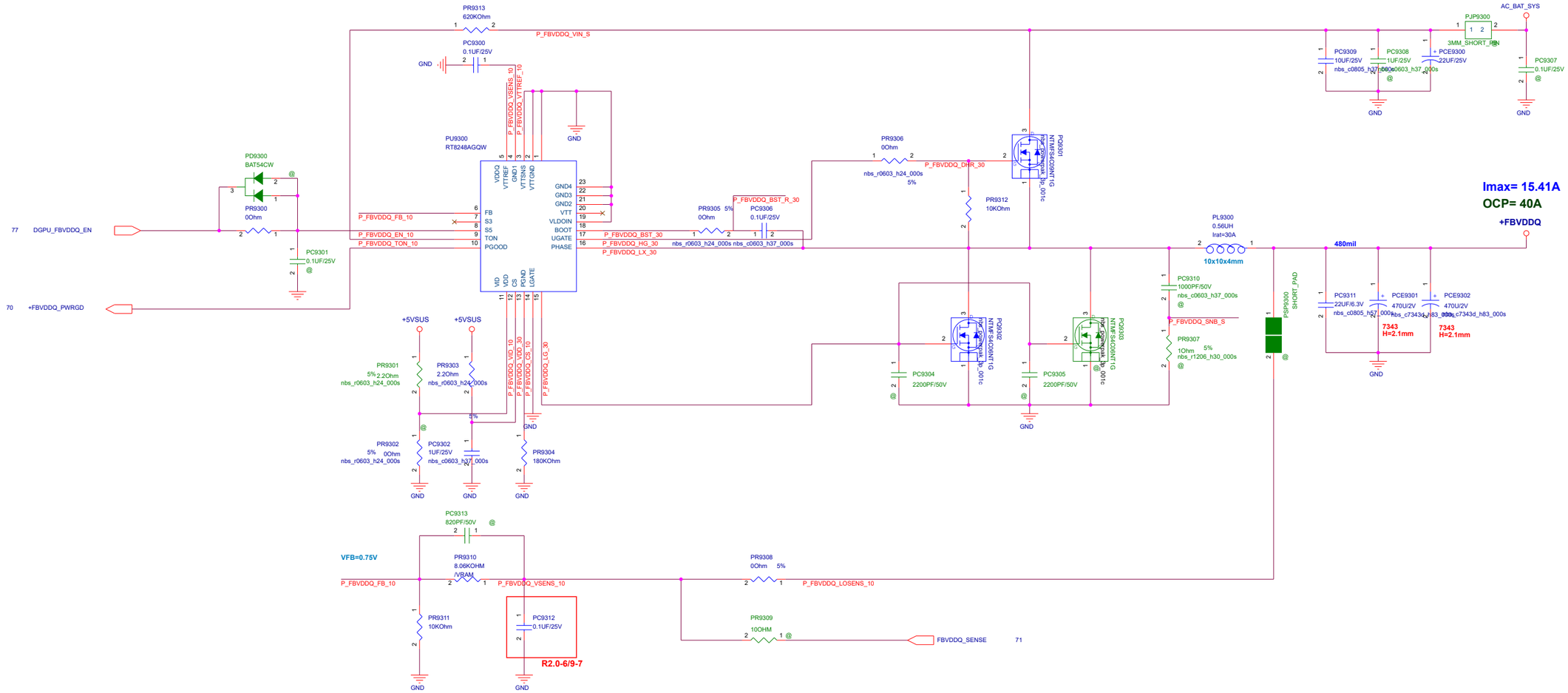
+PEX_VDD [For DGPU]



PR9221	UP1740Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

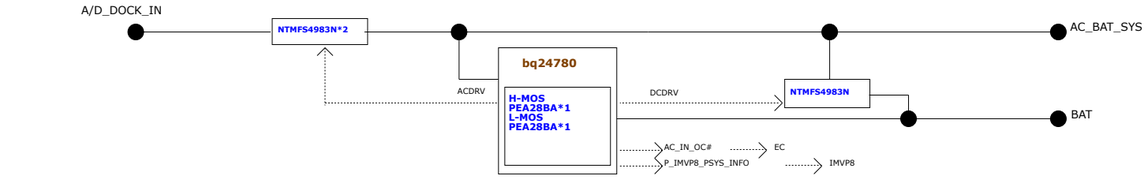
Project Name: GL552VW			Rev: 2.0
Title : PW_PEX_VDD			
Size: A3	Dept.: NB Power team	Engineer: Edison	
Date: Tuesday, June 23, 2015	Sheet 92 of 103		

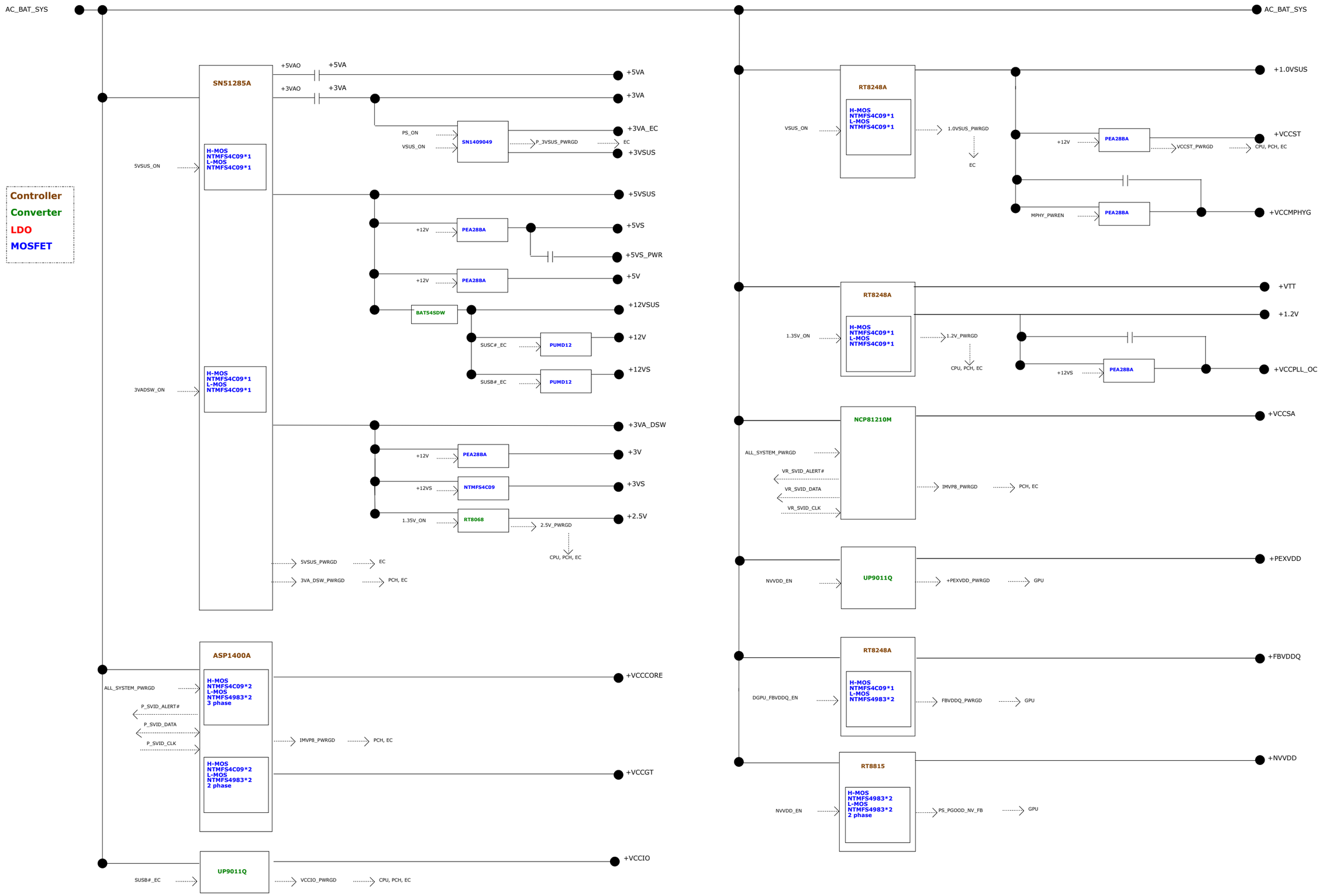
+FBVDDQ [For VRAM]



PR9310	RT8248_Vout
8.06kohm	1.35V
10.5kohm	1.5V

ASUS	Project Name: GL552VW		Rev: 2.0
Title :			
Size: A2	Dept.: ASUSTeK COMPUTER INC.	Engineer: Edison	
Date: Tuesday, June 23, 2015		Sheet 93 of 103	





<variant_name>

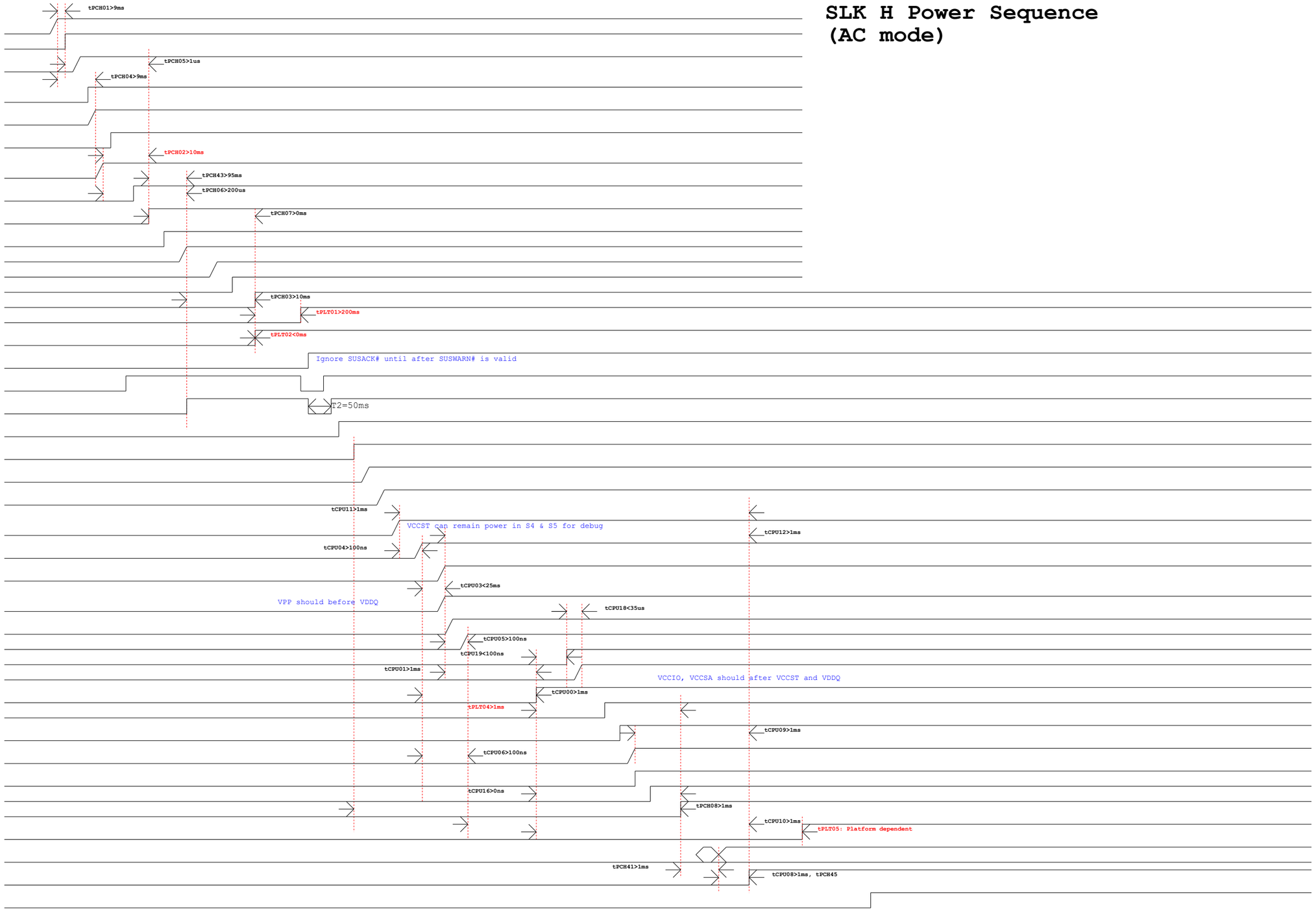
ASUS	Project Name: GL552VW		Rev: 2.0
Title : PW_FLOW CHART			
Size: A1	Dept.: ASUSTeK COMPUTER INC.	Engineer: Edison	
Date: Tuesday, June 23, 2015	Sheet 99 of 103		

AC-IN Mode

SLK H Power Sequence (AC mode)

Power
Signal

+RTCBAT
RTCRST#
(1) +3VA/+5VA
(2) PS_ON
(3) +3VA_EC
(4) +EC_RST#
(5) +3VA_DSW
(6) 3VA_DSW_PWRGD
(7) DPWROK_EC
(8) PM_SLP_SUS#
(9) +3VSUS/+1.0VSUS
(10) +12VSUS/+5VSUS
(11) 3VSUS_PERGD
(12) PM_RSMRST#
(13) SUSWARN#
(14) ME_AC_PRESENT
(15) PCH_SUSACK#
(16) PWR_SW#
(17) PM_PWRBTN#
(18) PM_SUSC#
(19) PM_SUSB#
(20) +12V/+5V/+3V/+VCCST
(21) +12VS/+5VS/+5VS_PWR/+3VS/+VCCPLL_OC
+1.0V_VCCST,VCCPLL
+VCCSTG
+VCCPLL_OC
(22) +1.2V
(23) +2.5V
+VCCIO
DDR_VTT_CTRL
+VTT
(24) ALL_SYSTEM_PWRGD
(25) P_IMVP8_EN_10
(26) P_IMVP8_DRVON
+VCCCORE/+VCCGT/+VCCSA
(27) IMVP8_PWRGD
(28) VCCST_PWRGD_CPU
(29) PM_PWROK
(30) PM_SYSPWROK
CLK_PCH_BCLK
(31) H_CPUPWRGD
(32) PCH_PLTRST_CPU#



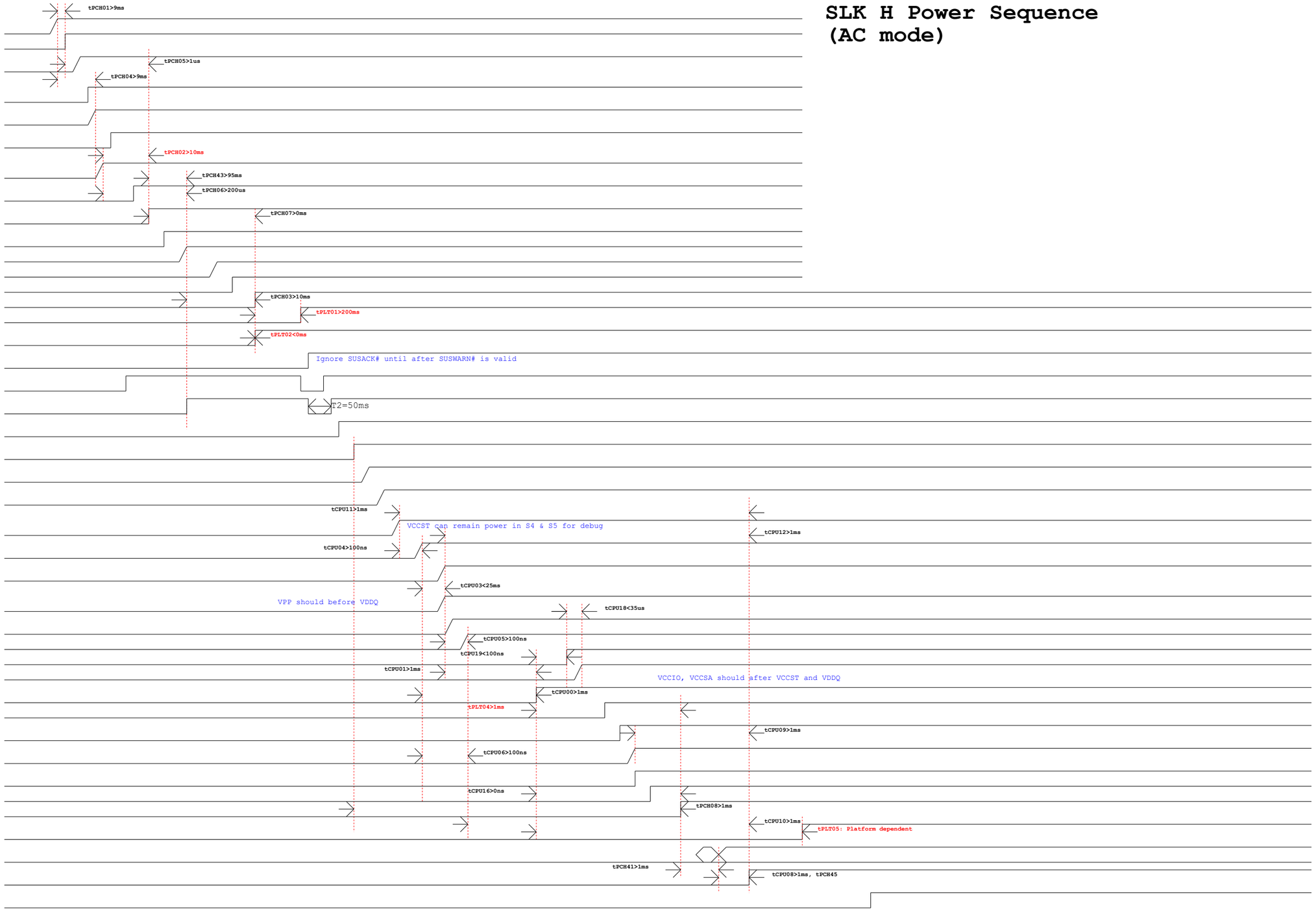
Project Name: GL552VW		Rev: 2.0
Title : AC Power On Timing		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 100 of 103	

AC-IN Mode

SLK H Power Sequence (AC mode)

Power
Signal

+RTCBAT
RTCRST#
(1) +3VA/+5VA
(2) PS_ON
(3) +3VA_EC
(4) +EC_RST#
(5) +3VA_DSW
(6) 3VA_DSW_PWRGD
(7) DPWROK_EC
(8) PM_SLP_SUS#
(9) +3VSUS/+1.0VSUS
(10) +12VSUS/+5VSUS
(11) 3VSUS_PERGD
(12) PM_RSMRST#
(13) SUSWARN#
(14) ME_AC_PRESENT
(15) PCH_SUSACK#
(16) PWR_SW#
(17) PM_PWRBTN#
(18) PM_SUSC#
(19) PM_SUSB#
(20) +12V/+5V/+3V/+VCCST
(21) +12VS/+5VS/+5VS_PWR/+3VS/+VCCPLL_OC
+1.0V_VCCST,VCCPLL
+VCCSTG
+VCCPLL_OC
(22) +1.2V
(23) +2.5V
+VCCIO
DDR_VTT_CTRL
+VTT
(24) ALL_SYSTEM_PWRGD
(25) P_IMVP8_EN_10
(26) P_IMVP8_DRVON
+VCCCORE/+VCCGT/+VCCSA
(27) IMVP8_PWRGD
(28) VCCST_PWRGD_CPU
(29) PM_PWROK
(30) PM_SYSPWROK
CLK_PCH_BCLK
(31) H_CPUPWRGD
(32) PCH_PLTRST_CPU#

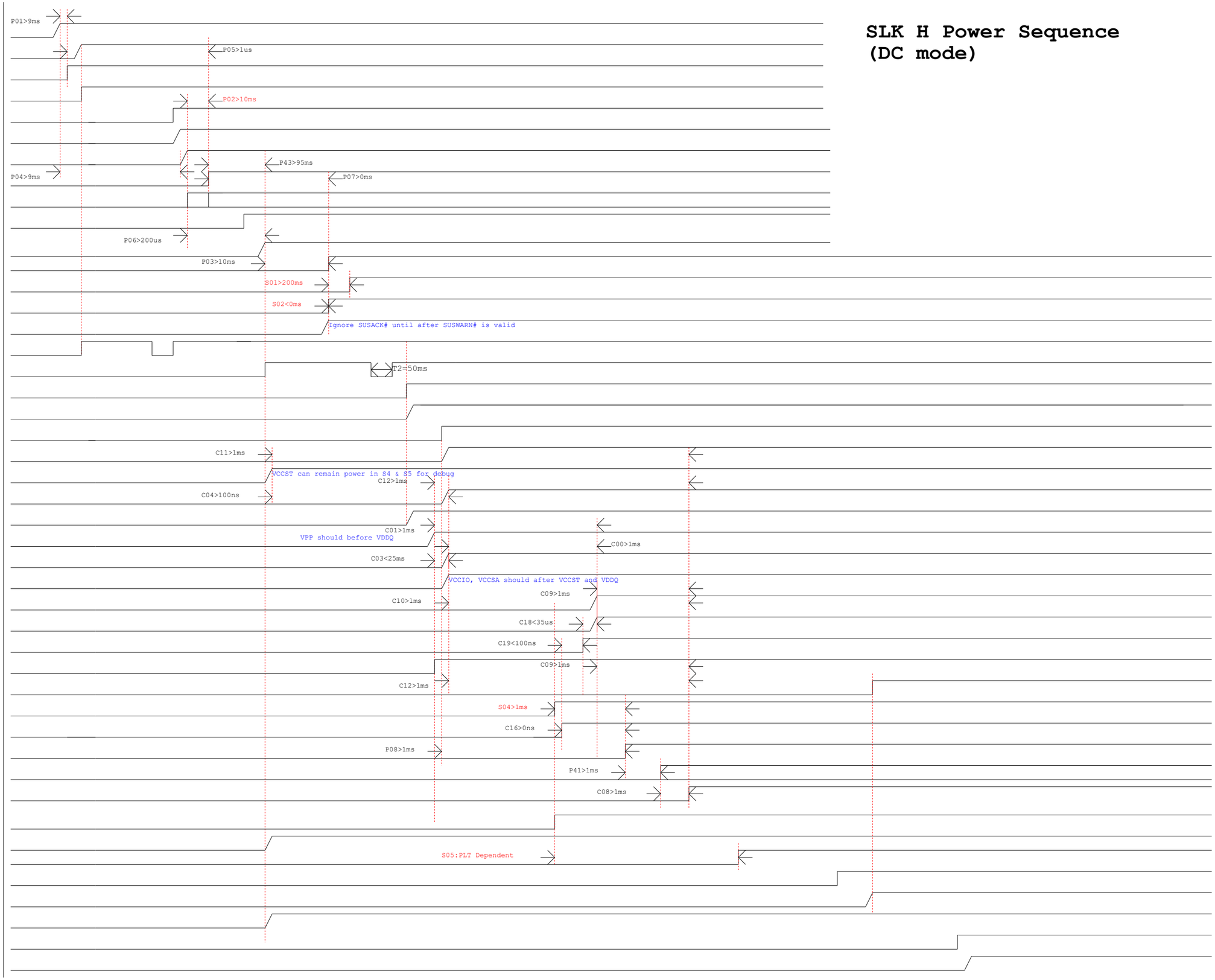


Project Name: GL552VW		Rev: 2.0
Title : AC Power On Timing		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu
Date: Tuesday, June 23, 2015	Sheet 100 of 103	

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



SLK H Power Sequence (DC mode)

ASUS	Project Name: GL552VW		Rev: 2.0
Title : POWER-ON SEQUENCE			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Mario_Jhu	
Date: Tuesday, June 23, 2015	Sheet 101 of 103		

Rev	Date	Description
2.0 Red	06/09/2015	1. Update Power schematic, 詳見GL552VW_PSR_DSN檔修改事項 20150609 2. 修改DDR_VTT_CTRL power plane to +3VS for 黑電issue at p. 6 3. 修改Power Thermal sensor power protection at p. 28 4. change HDA power plane to +3VS power with Intel confirm at p. 26 5. change R2080 & R2005 to 3.3KOHM pull-high follow VC at p. 20 6. Change net name SUS_CLK# to SUS_CLK_X1 at p. 20 7. fix Samsung 禁用料 at p. 3, 6, 22, 40, 47, 59, 62, 69, 70, 71, 76, 77, 83, 84, 86, 87, 88, 91, 92, 93 8. add Intel QS sample ASUS P/N at p. 3 & 20
	06/10/2015	1. mont R7599 for Power request at p. 75 2. unmont SPI IO3 circuit for Intel QS Sample at p. 28 3. Update Power schematic, 詳見GL552VW_PSR_DSN檔修改事項 20150610
	06/12/2015	1. change [ARGOSY] Type-C Connector to Pin 長 1.1mm at p.47 2. change SSD NUT at p. 65
	06/12/2015 v2	1. PU8801由POWER SW. UP9020BFB6-00(06016-01110000)上件 改為POWER SW. APL3527GHAI-TRG(06016-00160300)上件 2. PC8837由MLCC 1UF/16V(0603)X7R 10%(11G233110511030)上件 改為MLCC 4.7UF/16V (0603) X5R 10%(11204-0003F000)上件
	06/12/2015 v3	1. add DSG circuit for +12V & +12VS follow VC at p. 57
	06/17/2015	1. DRAMRST# issue, change C2008, C1402 & C1501 for EMI & VC at p. 14, 15 & 20. 2. 預留 CLK_24M 0 ohm EMI at p. 22 3. Add Varister for EMI request at p. 6, 20, 30, 40, 58
	06/18/2015	1. PR8056由RES 20K OHM 1/16W (0402) 1%(10G212200214030)上件改為 RES 40.2K OHM 1/16W (0402) 1%(10G212402214010)上件 2. Update GPIO Table at p. 2
	06/22/2015	1. 預留SPI_IO3 PU電阻 R2851 for Intel at p. 28 2. change RTC to small at p. 20 3. change 0 Ohm to 0.1uF for EA Audio test at p. 62 4. PR8817由RES 2.2 OHM 1/10W(0603)5%(10G2132R2003010)上件改為 RES 10 OHM 1/16W (0402) 1%(10G21210R014030)上件 5. PC8837由MLCC 4.7UF/16V (0603) X5R 10%(11204-0003F000)上件 改為MLCC 1UF/6.3V (0402) X5R 10%(11G232210515070)上件
	06/23/2015	1. SSD Thermal Sensor 上件, CPU Thermal Sensor 不上件 at p. 50 2. 預留0 Ohm for EMI BCLK at p. 20 3. change 0 Ohm to 5.1 Ohm for EMI request at p. 6
	06/23/2015 v2	1. change 5.1 Ohm to PCH for EMI request at p. 6 & 22 2. PCE8402 CAP PL 15UF/25V 7343 SMD(11020-00275100)由不上件改上件 3. PCE9200 CAP PL 22UF/25V 4.6*6.3 20%(11032-0008F000) 由不上件改上件

Rev	Date	Description

Rev	Date	Description

Rev	Date	Description

ASUSTeK COMPUTER INC. NB1

Title : Revision History

Engineer: Mario_Jhu

Size	Project Name	Rev
D	GL552VW	2.0

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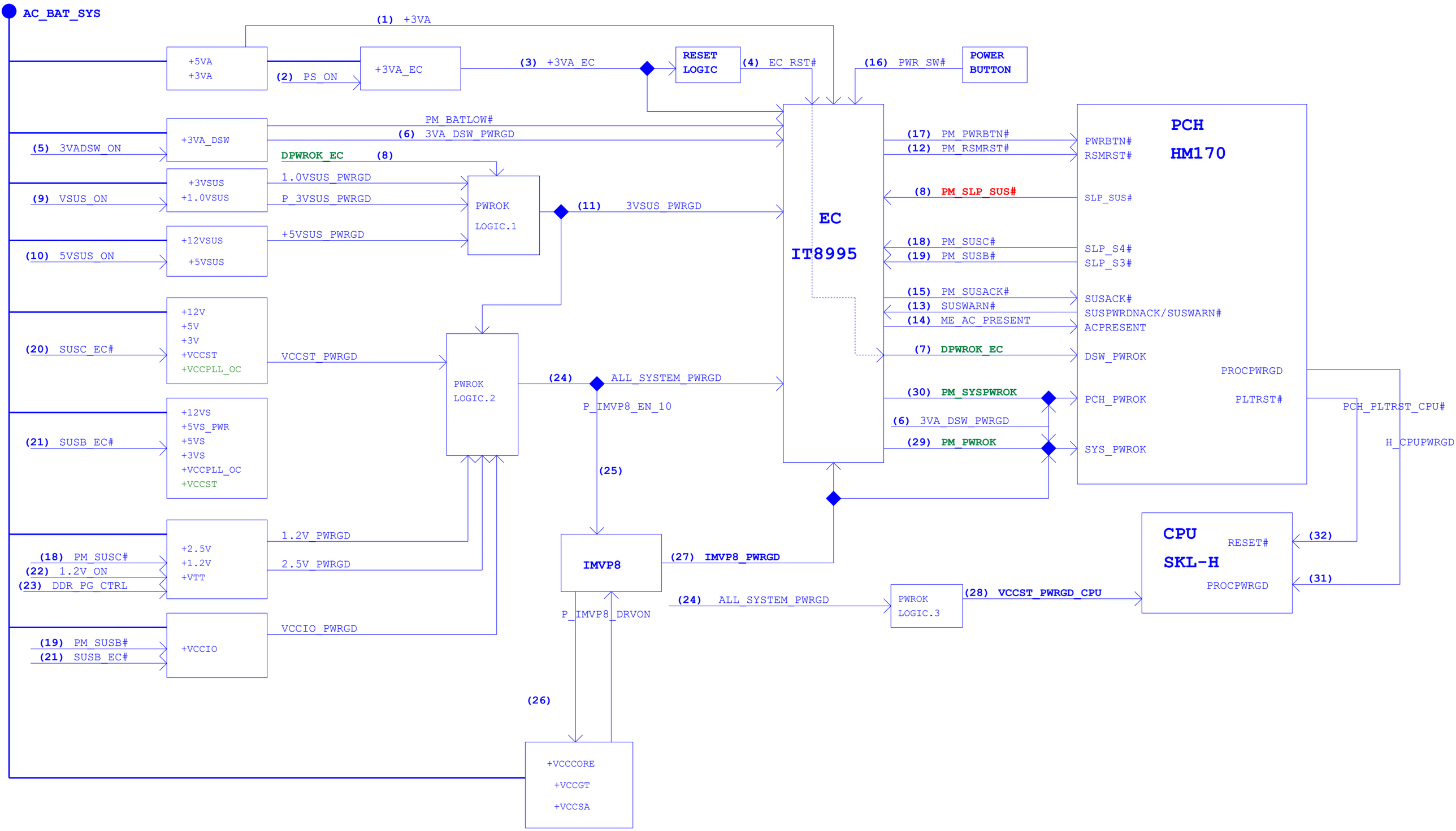
+RTCBAT->3.3V
RTCCLK->on
RTC_RST->High

AC-IN Mode

AC_IN_OC->Low

GL552VW Power On Sequence Diagram Rev.1.0



ASUSTeK COMPUTER INC. NB1	Title : POWER SEQUENCE		
	Engineer: Mario_Jhu		
Size: C	Project Name: GL552VW		Rev: 2.0
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