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IH11V-MHS H110MLC D4 VER 7.0

CPU:

Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:

SPT-H PCH

Main Memory:

Dual Channel/DDR-4*2(Max 16GB)1867/2133

Onboard Device:

Super I/O:IT8613E
LAN:Realtek 8111H
HD Codec:ALC887

Power solution:

CPU Voltage Regulators:3phase by RT3606 high 1 Low 1 OV by RT3606
DDR Voltage Regulators:1Phase by UP1514 high 1 Low 1 OV by IT8613E

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT *2

REAR IO:

PS/2 PORT
DVI Port
VGA Port
USB3.0 PORT *2
Gb RJ-45 +2 layer USB3.0 Ports
Audio Jackets (3 PORT)

Front I/O:

SATA3 *6
USB 2.0 Header * 2 Serial header
USB 3.0 Header * 1 Front Audio Header
CPU FAN *1
System FAN *1

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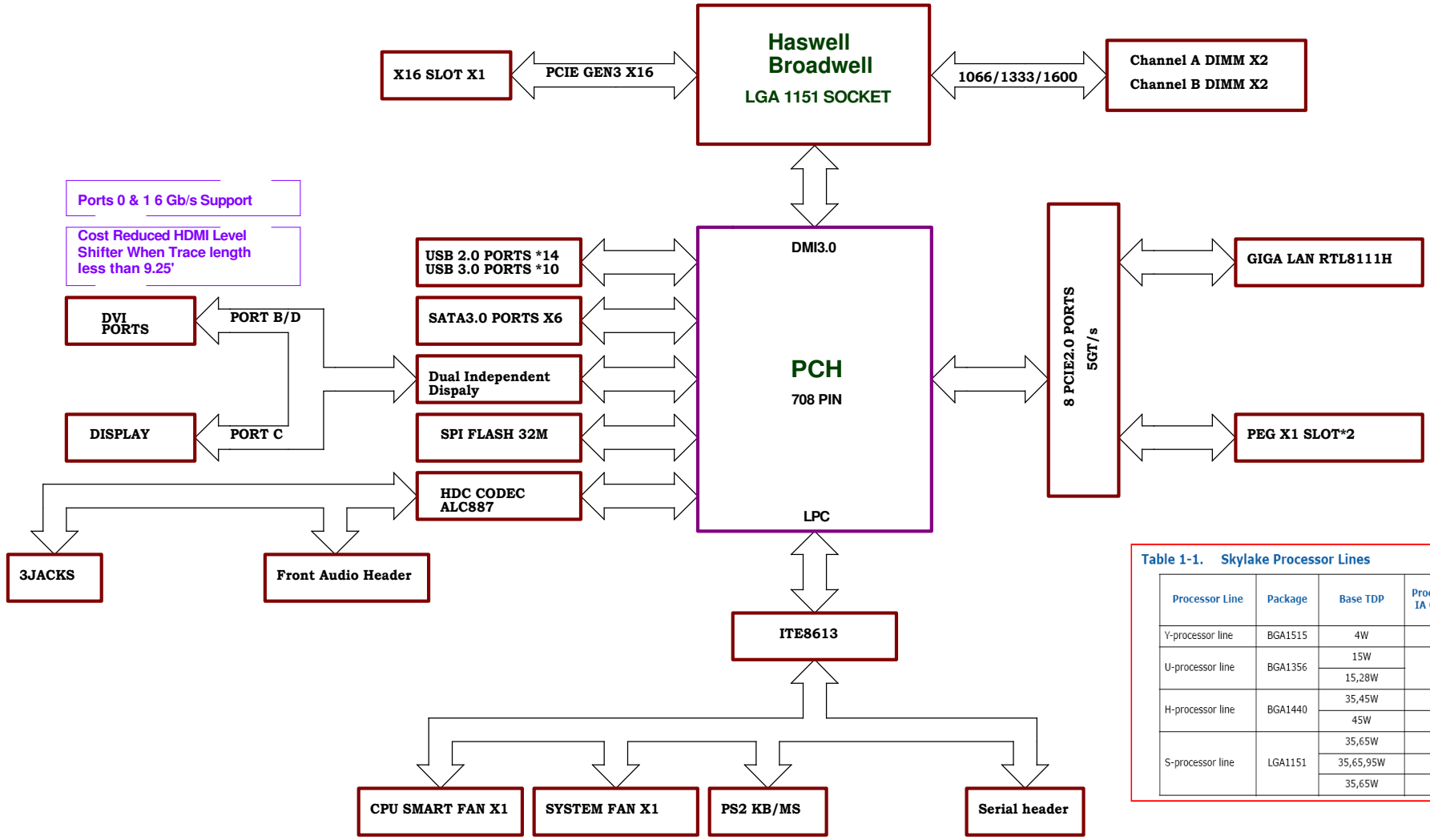

Table 1-1. Skylake Processor Lines

Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2		1-Chip
		15,28W		GT3	64 MB	
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	

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Title: BLOCK DIAGRAM

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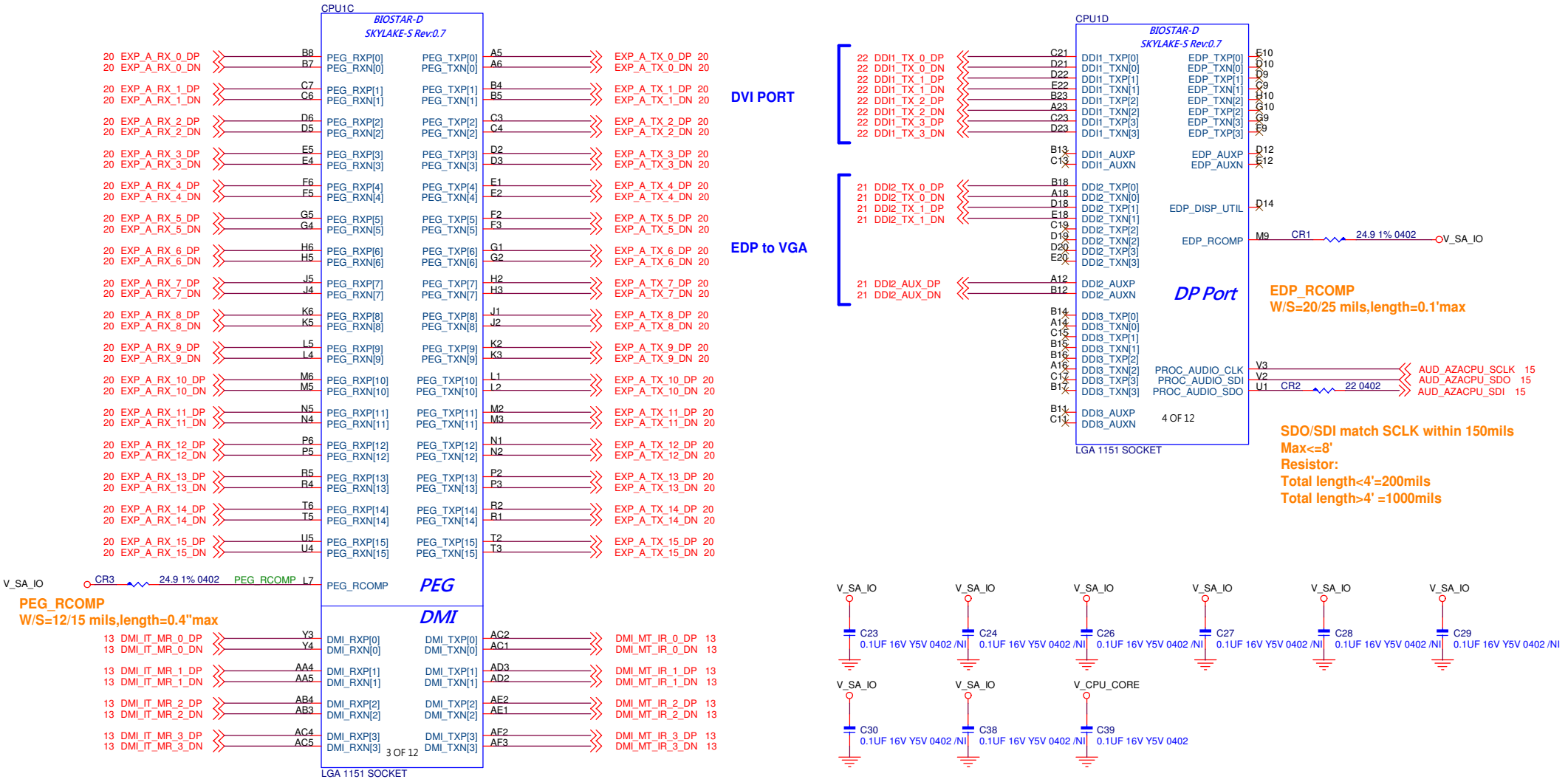

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Title	CPU PCIEX16/DMI/FDI	
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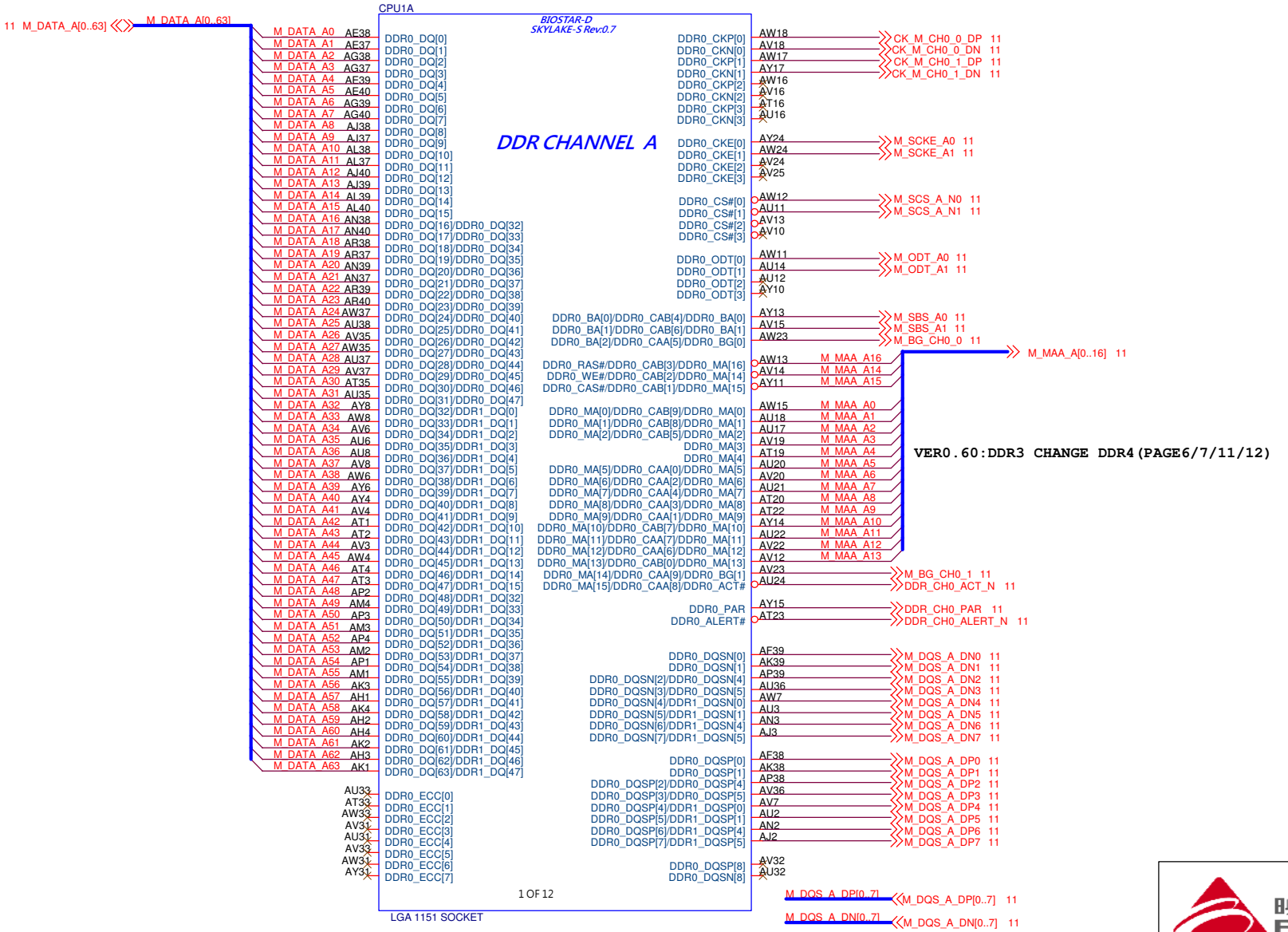

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Title	CPU DDR3 CHANNEL A	
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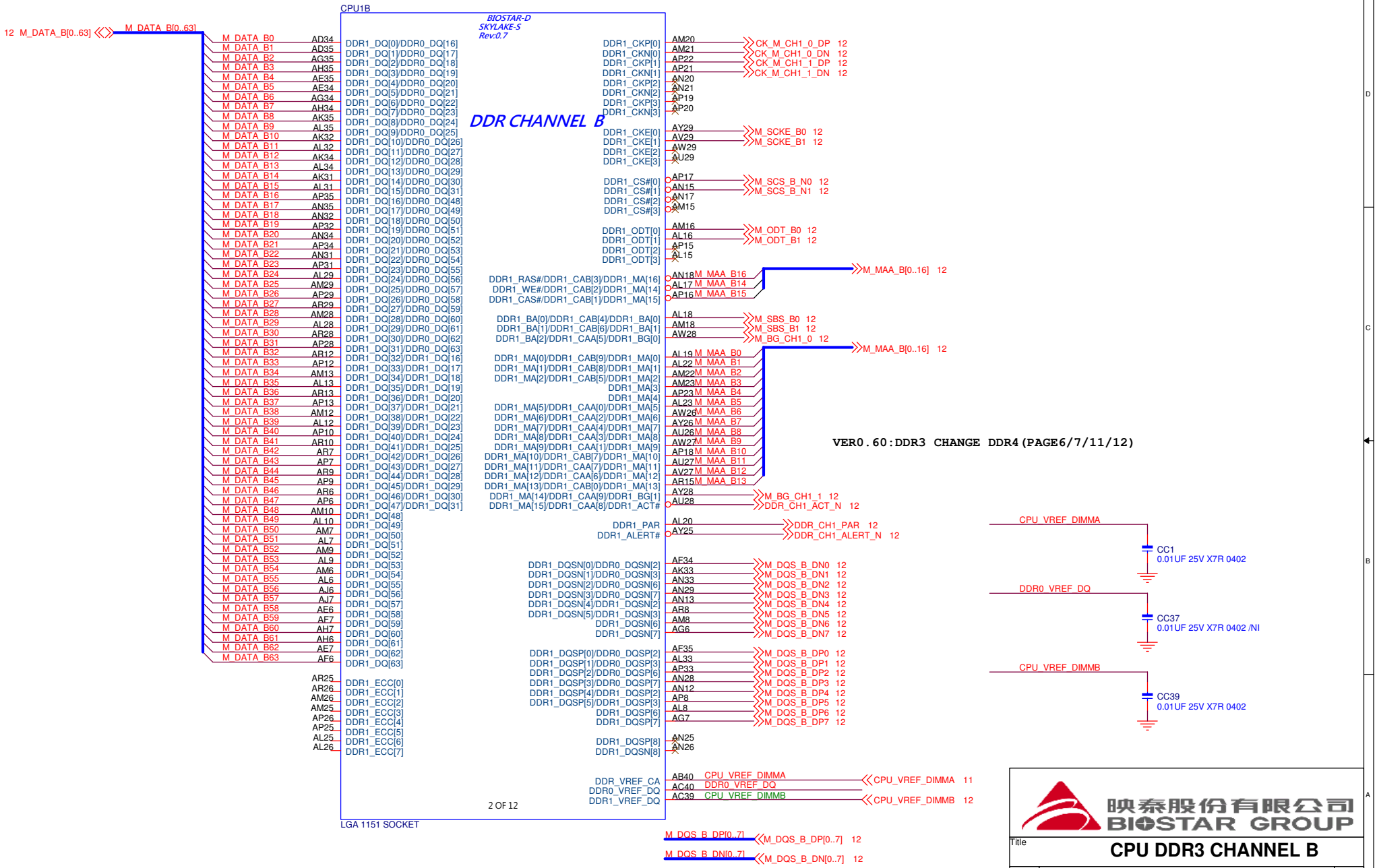
CPU1B
BIOSTAR-D
SKYLAKE-S
Rev:0.7
DDR CHANNEL B
12 M_DATA_B[0..63]
M_DATA_B[0..63]
DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]
2 OF 12
LGA 1151 SOCKET
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
CK_M_CH1_0_DP 12
CK_M_CH1_0_DN 12
CK_M_CH1_1_DP 12
CK_M_CH1_1_DN 12
DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]
M_SCKE_B0 12
M_SCKE_B1 12
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
M_SCS_B_N0 12
M_SCS_B_N1 12
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
M_ODT_B0 12
M_ODT_B1 12
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]
M_MAA_B16
M_MAA_B14
M_MAA_B15
M_MAA_B[0..16] 12
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]
M_SBS_B0 12
M_SBS_B1 12
M_BG_CH1_0 12
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
M_MAA_B0
M_MAA_B1
M_MAA_B2
M_MAA_B3
M_MAA_B4
M_MAA_B5
M_MAA_B6
M_MAA_B7
M_MAA_B8
M_MAA_B9
M_MAA_B10
M_MAA_B11
M_MAA_B12
M_MAA_B13
M_MAA_B[0..16] 12
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#
M_BG_CH1_1 12
DDR_CH1_ACT_N 12
DDR1_PAR
DDR1_ALERT#
DDR_CH1_PAR 12
DDR_CH1_ALERT_N 12
DDR1_DQSN[0]/DDR0_DQSN[2]
DDR1_DQSN[1]/DDR0_DQSN[3]
DDR1_DQSN[2]/DDR0_DQSN[6]
DDR1_DQSN[3]/DDR0_DQSN[7]
DDR1_DQSN[4]/DDR1_DQSN[2]
DDR1_DQSN[5]/DDR1_DQSN[3]
DDR1_DQSN[6]
DDR1_DQSN[7]
M_DQS_B_DN0 12
M_DQS_B_DN1 12
M_DQS_B_DN2 12
M_DQS_B_DN3 12
M_DQS_B_DN4 12
M_DQS_B_DN5 12
M_DQS_B_DN6 12
M_DQS_B_DN7 12
DDR1_DQSP[0]/DDR0_DQSP[2]
DDR1_DQSP[1]/DDR0_DQSP[3]
DDR1_DQSP[2]/DDR0_DQSP[6]
DDR1_DQSP[3]/DDR0_DQSP[7]
DDR1_DQSP[4]/DDR1_DQSP[2]
DDR1_DQSP[5]/DDR1_DQSP[3]
DDR1_DQSP[6]
DDR1_DQSP[7]
M_DQS_B_DP0 12
M_DQS_B_DP1 12
M_DQS_B_DP2 12
M_DQS_B_DP3 12
M_DQS_B_DP4 12
M_DQS_B_DP5 12
M_DQS_B_DP6 12
M_DQS_B_DP7 12
DDR1_DQSP[8]
DDR1_DQSN[8]
DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ
CPU_VREF_DIMMA
DDR0_VREF_DQ
CPU_VREF_DIMMB
CPU_VREF_DIMMA 11
CPU_VREF_DIMMB 12
M_DQS_B_DP[0..7]
M_DQS_B_DN[0..7]
M_DQS_B_DP[0..7] 12
M_DQS_B_DN[0..7] 12
VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)
CPU_VREF_DIMMA
CC1
0.01UF 25V X7R 0402
DDR0_VREF_DQ
CC37
0.01UF 25V X7R 0402 /NI
CPU_VREF_DIMMB
CC39
0.01UF 25V X7R 0402
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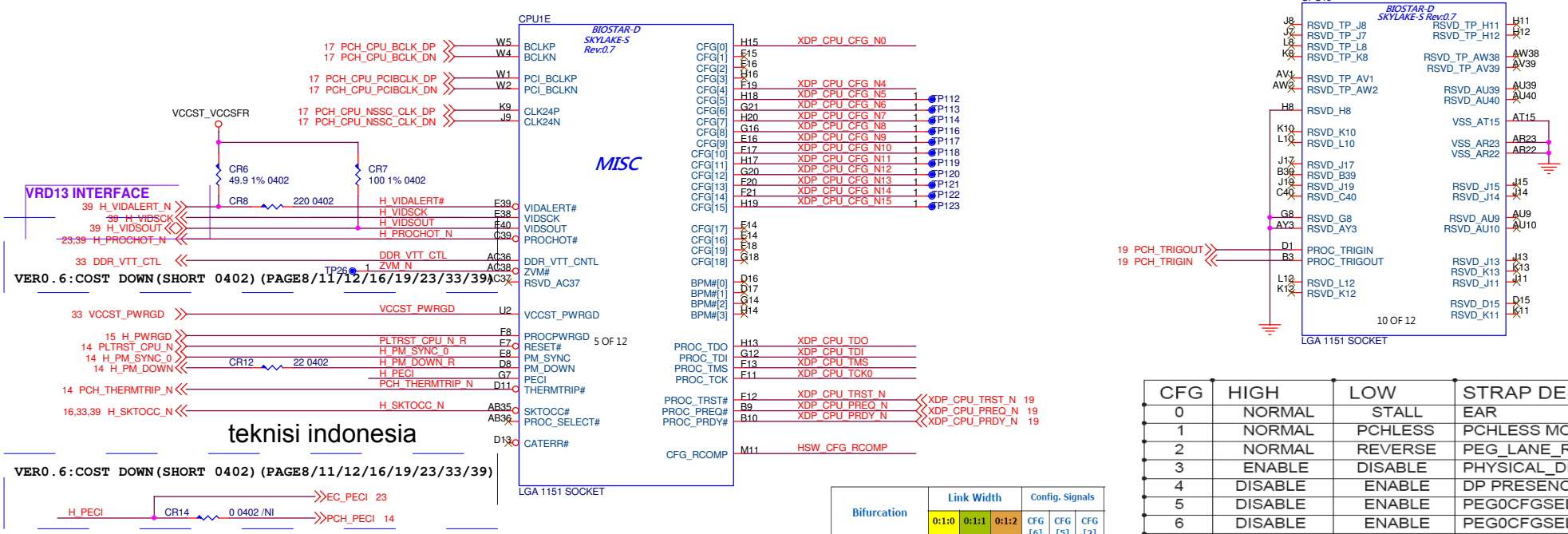

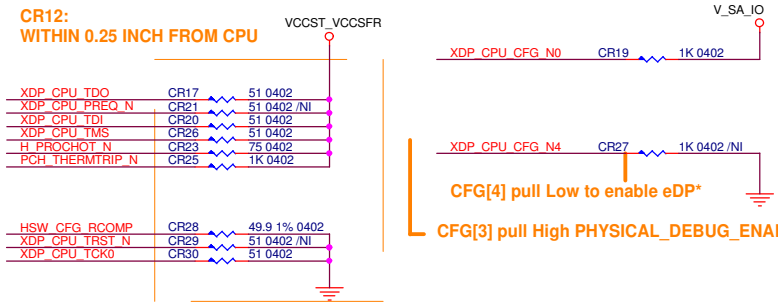

Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 **Reversed**	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 **Reversed**	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0

CFG[19:0]

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
Intel recommends placing test points on the board for CFG pins.

- **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted;
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]:** Reserved configuration lane.
- **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]:** PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.

CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		
ALL PINS HAVE INTERNAL PULL-UPS			

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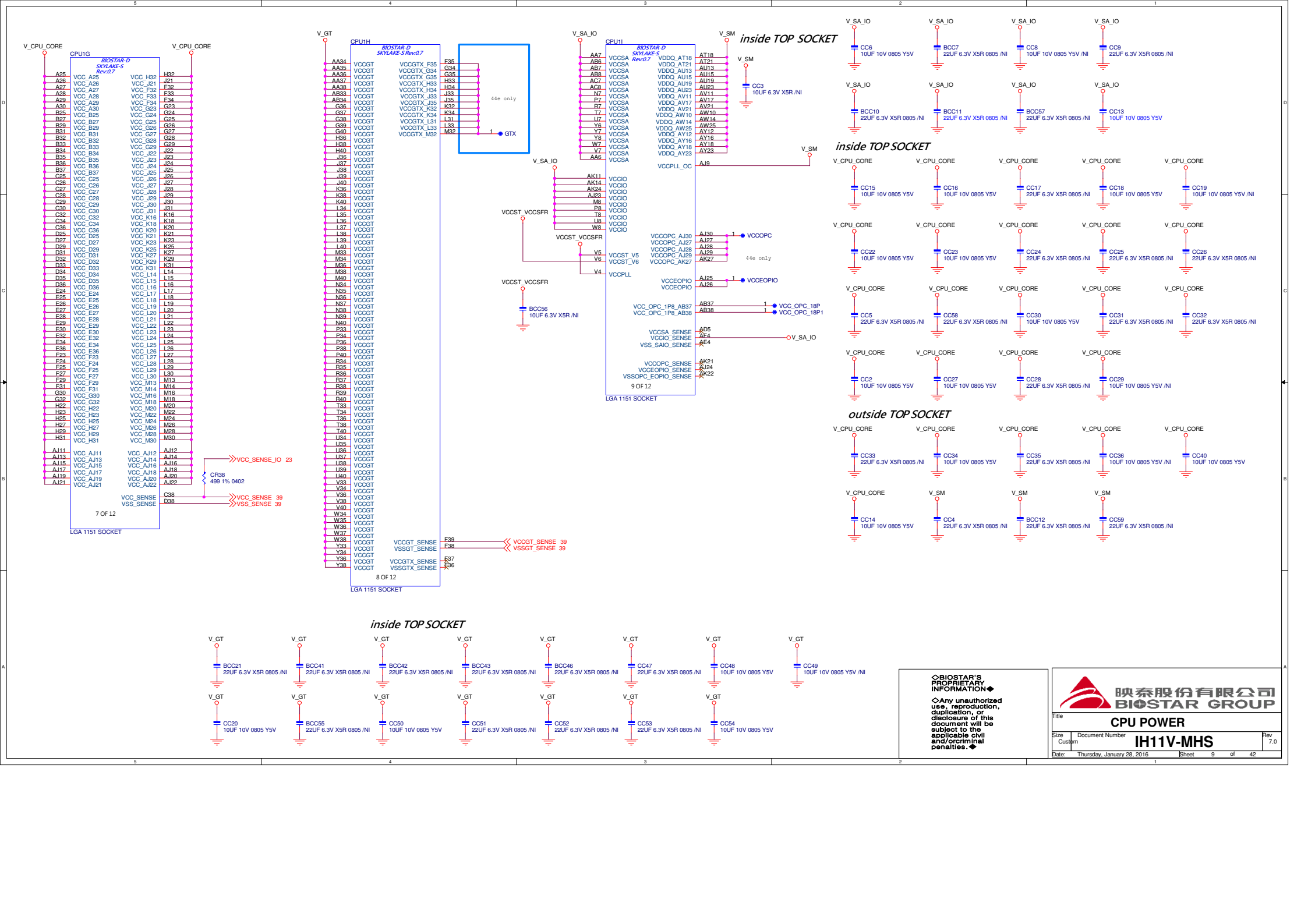
V_CPU_CORE
CPU1G
BIOSTAR-D SKYLAKE-S Rev:0.7
7 OF 12
LGA 1151 SOCKET
VCC_SENSE_IO 23
CR38 499 1% 0402
VCC_SENSE 39
VSS_SENSE 39
V_GT
CPU1H
8 OF 12
44e only
GTX
VCCGT_SENSE 39
VSSGT_SENSE 39
V_SA_IO
V_SM
CPU1I
9 OF 12
CC3 10UF 6.3V X5R /NI
VCCPLL_OC
VCCIO
VCCST_VCCSFR
BCC56 10UF 6.3V X5R /NI
VCCOPC
VCCEOPIO
VCC_OPC_18P
VCC_OPC_18P1
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
inside TOP SOCKET
CC6 10UF 10V 0805 Y5V
BCC7 22UF 6.3V X5R 0805 /NI
CC8 10UF 10V 0805 Y5V /NI
CC9 22UF 6.3V X5R 0805 /NI
BCC10 22UF 6.3V X5R 0805 /NI
BCC11 22UF 6.3V X5R 0805 /NI
BCC57 22UF 6.3V X5R 0805 /NI
CC13 10UF 10V 0805 Y5V
CC15 10UF 10V 0805 Y5V
CC16 10UF 10V 0805 Y5V
CC17 22UF 6.3V X5R 0805 /NI
CC18 10UF 10V 0805 Y5V
CC19 10UF 10V 0805 Y5V /NI
CC22 10UF 10V 0805 Y5V
CC23 10UF 10V 0805 Y5V
CC24 22UF 6.3V X5R 0805 /NI
CC25 22UF 6.3V X5R 0805 /NI
CC26 22UF 6.3V X5R 0805 /NI
CC5 22UF 6.3V X5R 0805 /NI
CC58 22UF 6.3V X5R 0805 /NI
CC30 10UF 10V 0805 Y5V
CC31 22UF 6.3V X5R 0805 /NI
CC32 22UF 6.3V X5R 0805 /NI
CC2 10UF 10V 0805 Y5V
CC27 10UF 10V 0805 Y5V
CC28 22UF 6.3V X5R 0805 /NI
CC29 10UF 10V 0805 Y5V /NI
outside TOP SOCKET
CC33 22UF 6.3V X5R 0805 /NI
CC34 10UF 10V 0805 Y5V
CC35 22UF 6.3V X5R 0805 /NI
CC36 10UF 10V 0805 Y5V /NI
CC40 10UF 10V 0805 Y5V
CC14 10UF 10V 0805 Y5V
CC4 22UF 6.3V X5R 0805 /NI
BCC12 22UF 6.3V X5R 0805 /NI
CC59 22UF 6.3V X5R 0805 /NI
inside TOP SOCKET
BCC21 22UF 6.3V X5R 0805 /NI
BCC41 22UF 6.3V X5R 0805 /NI
BCC42 22UF 6.3V X5R 0805 /NI
BCC43 22UF 6.3V X5R 0805 /NI
BCC46 22UF 6.3V X5R 0805 /NI
CC47 22UF 6.3V X5R 0805 /NI
CC48 10UF 10V 0805 Y5V
CC49 10UF 10V 0805 Y5V /NI
CC20 10UF 10V 0805 Y5V
BCC55 22UF 6.3V X5R 0805 /NI
CC50 10UF 10V 0805 Y5V
CC51 22UF 6.3V X5R 0805 /NI
CC52 22UF 6.3V X5R 0805 /NI
CC53 22UF 6.3V X5R 0805 /NI
CC54 10UF 10V 0805 Y5V
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CPU POWER
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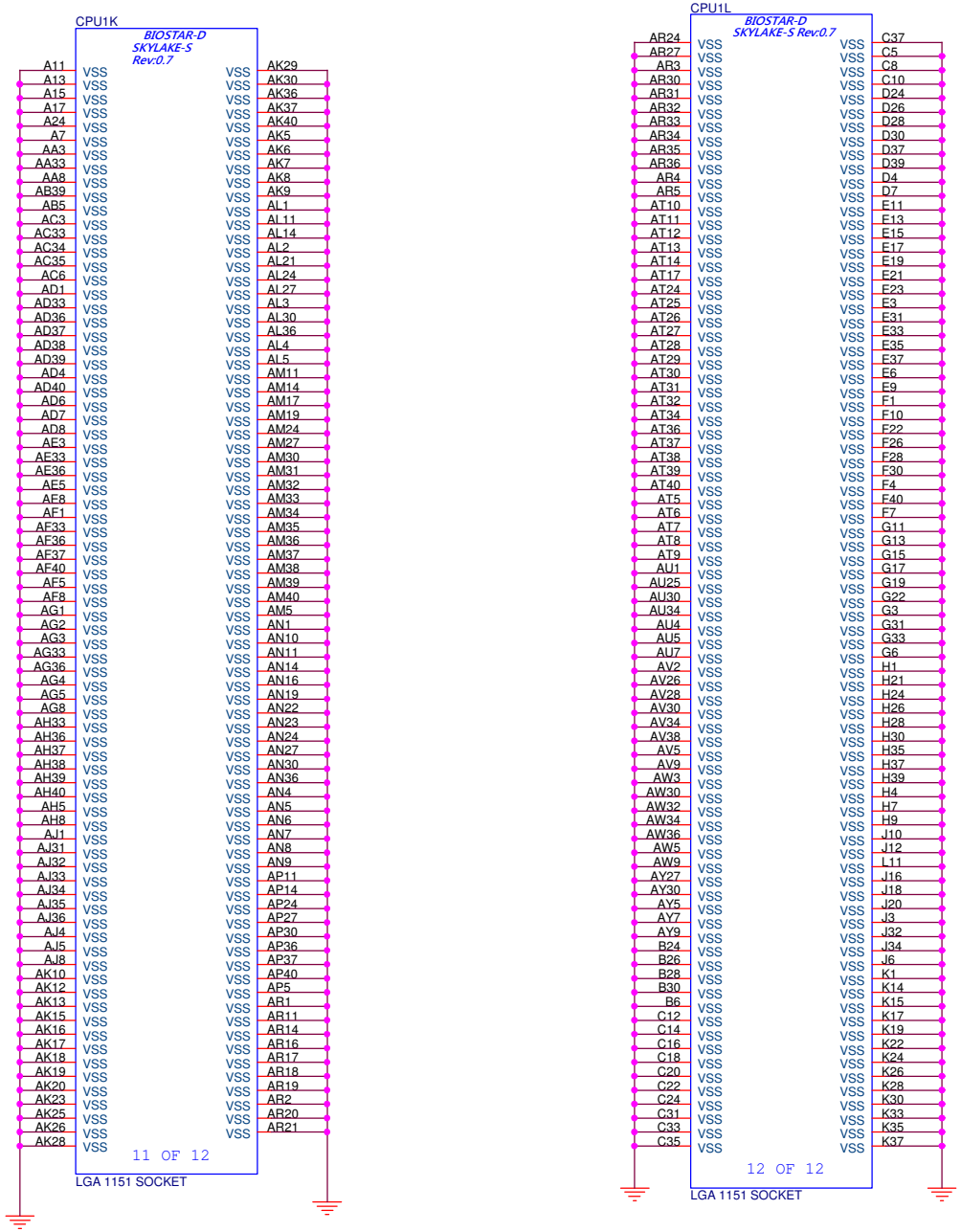

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Title: CPU GND

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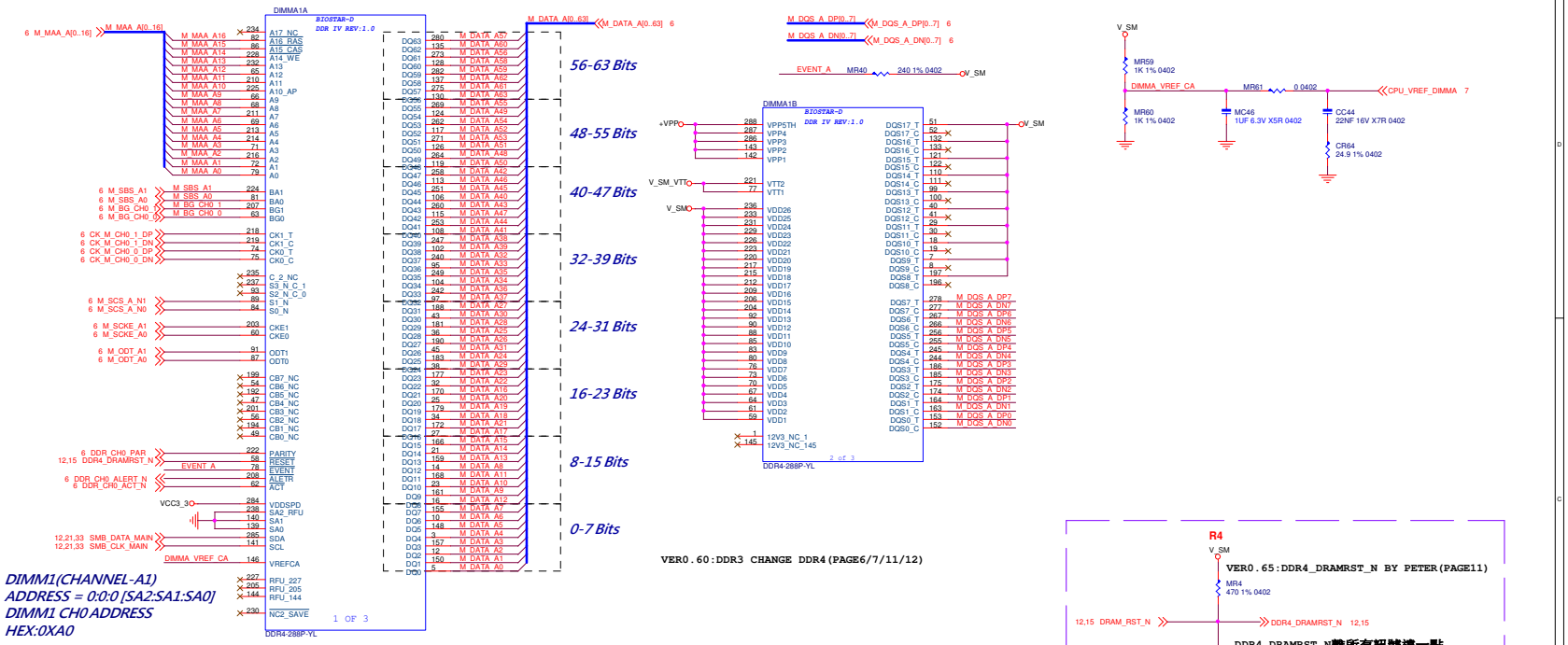

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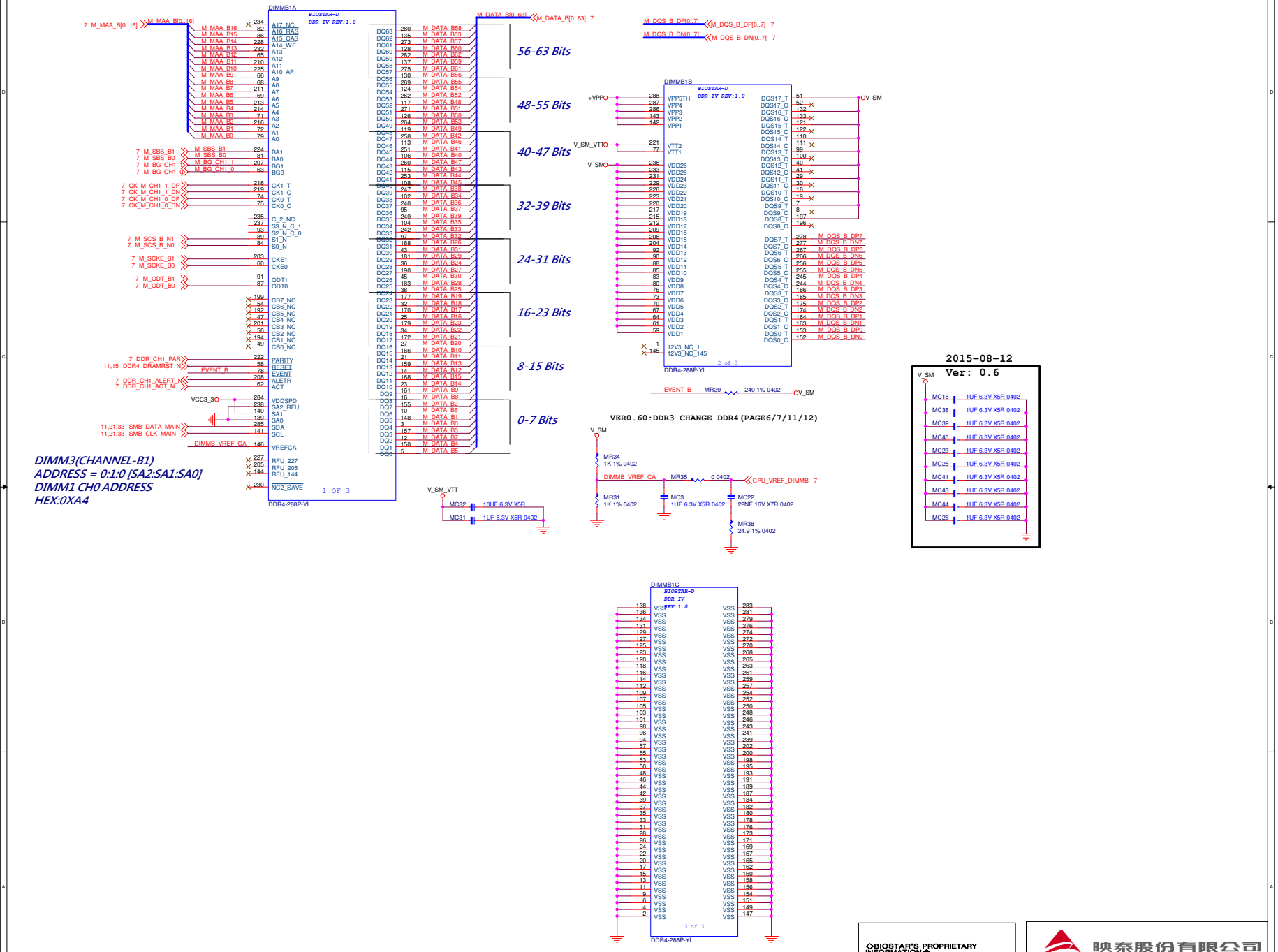

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Title: DDR3L DIMMB1

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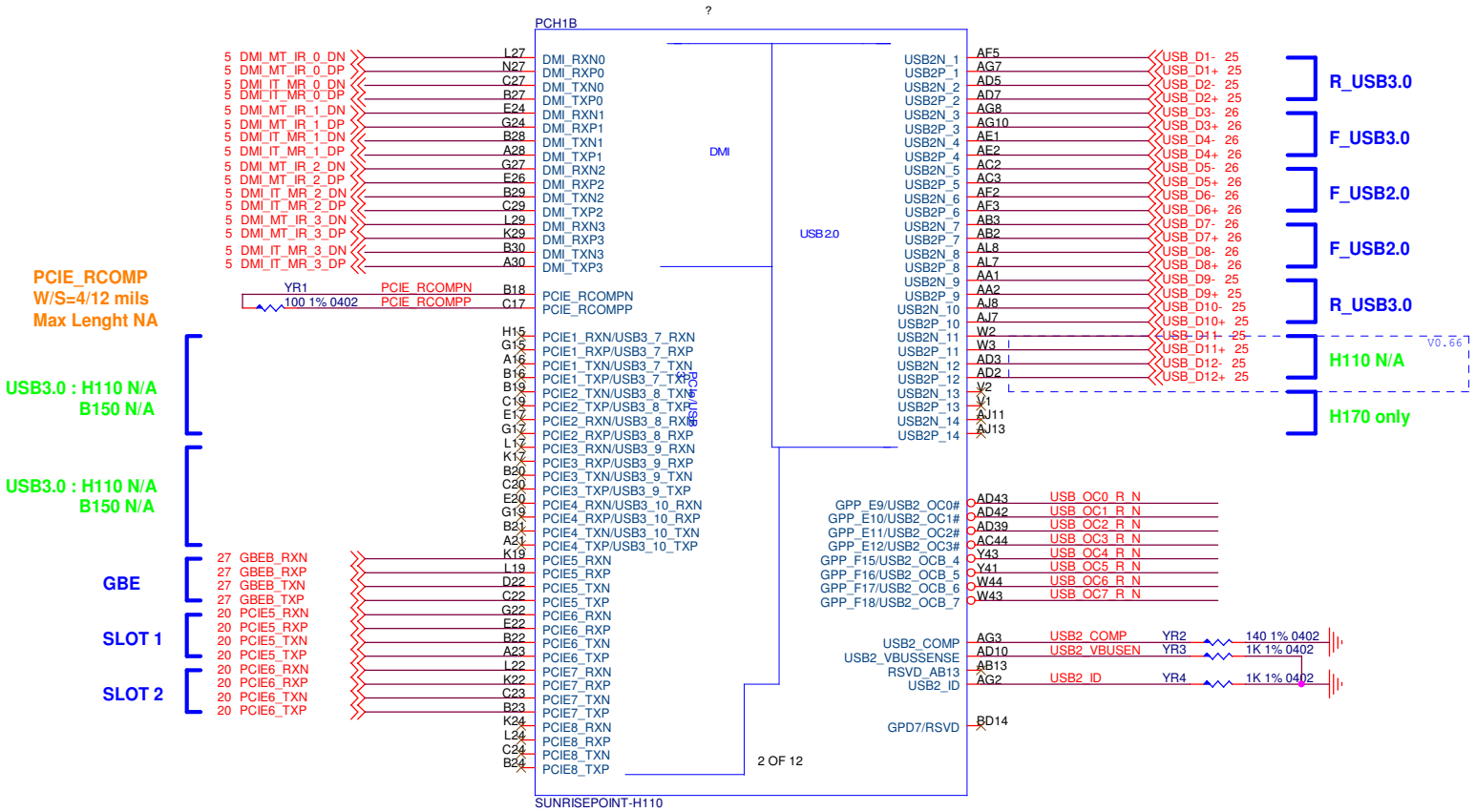
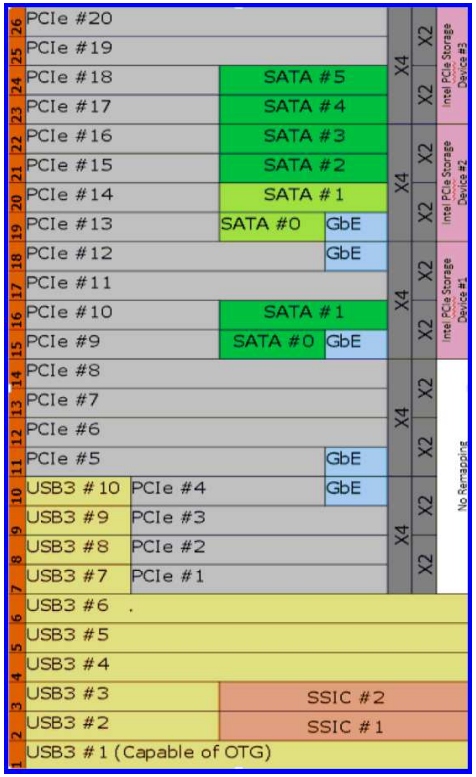
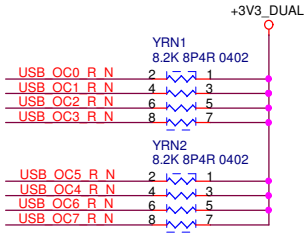
PCH PART: Y+Reference







映泰股份有限公司
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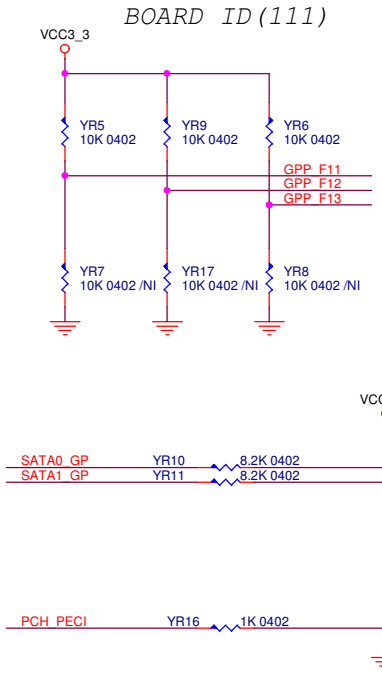
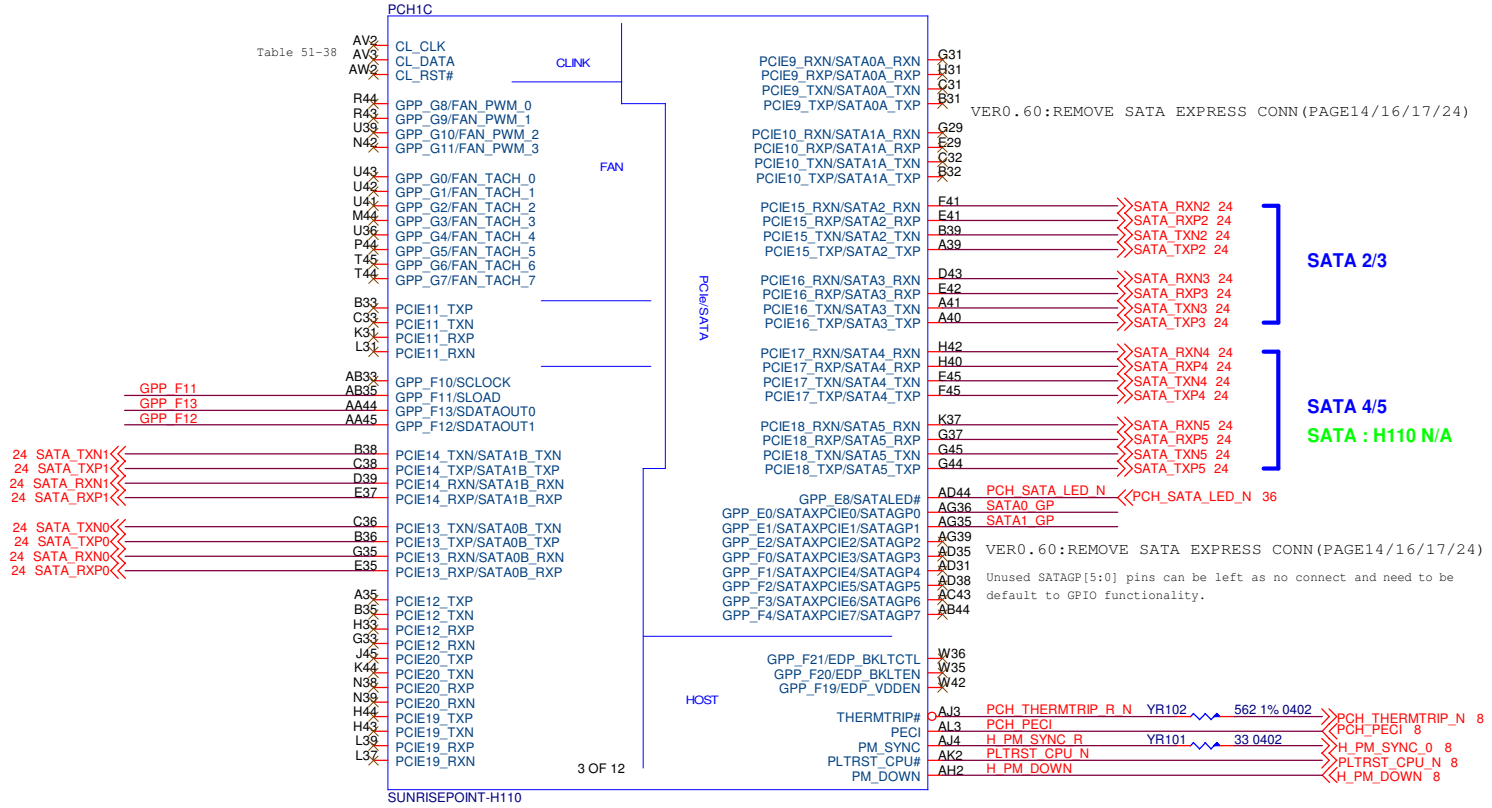
Title	PCH DMI/PCIE/USB	
Size B	Document Number IH11V-MHS	Rev 7.0
Date: Thursday, January 28, 2016	Sheet 13 of 42	

PCH PART: Y+Reference

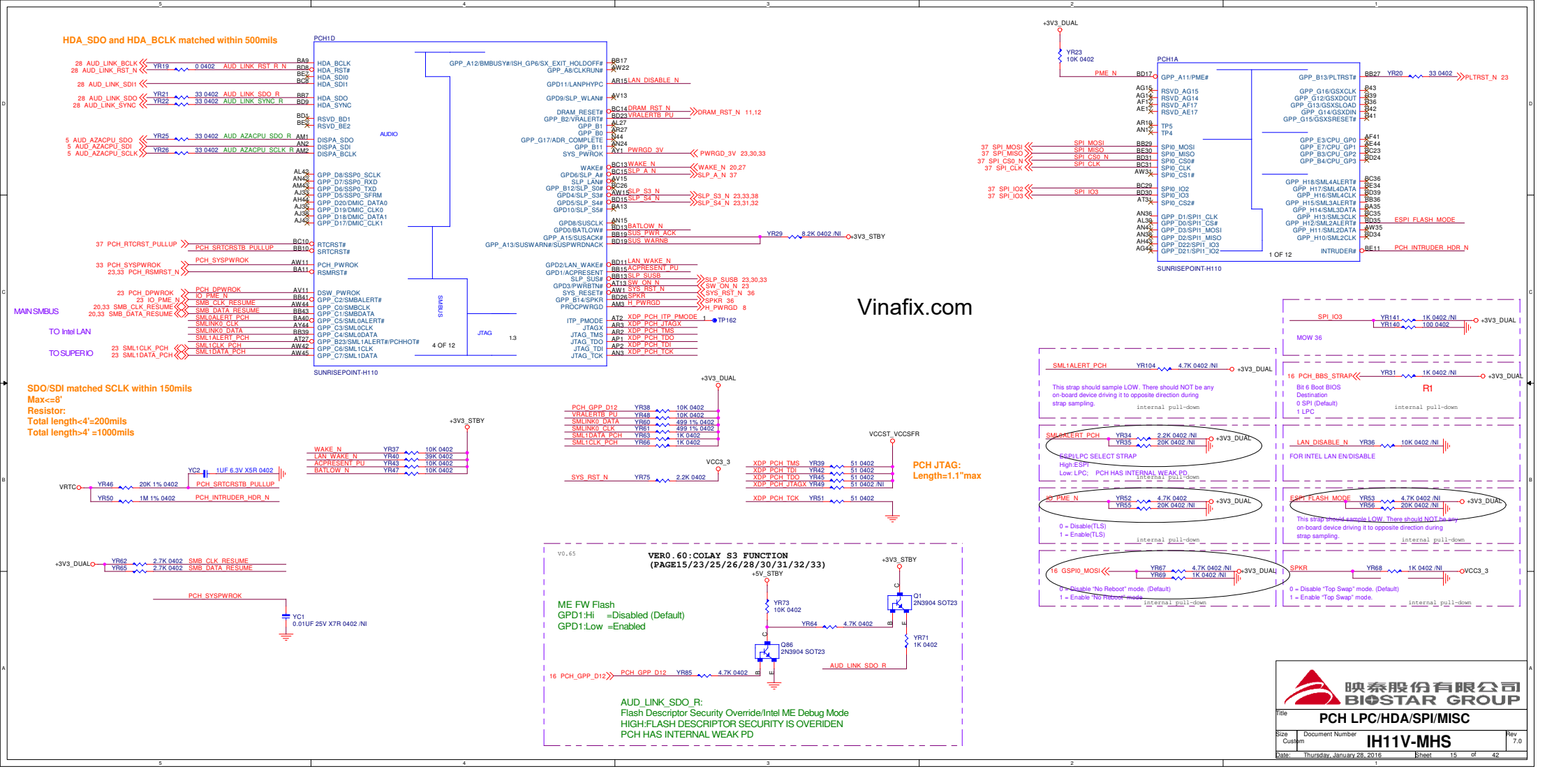




GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

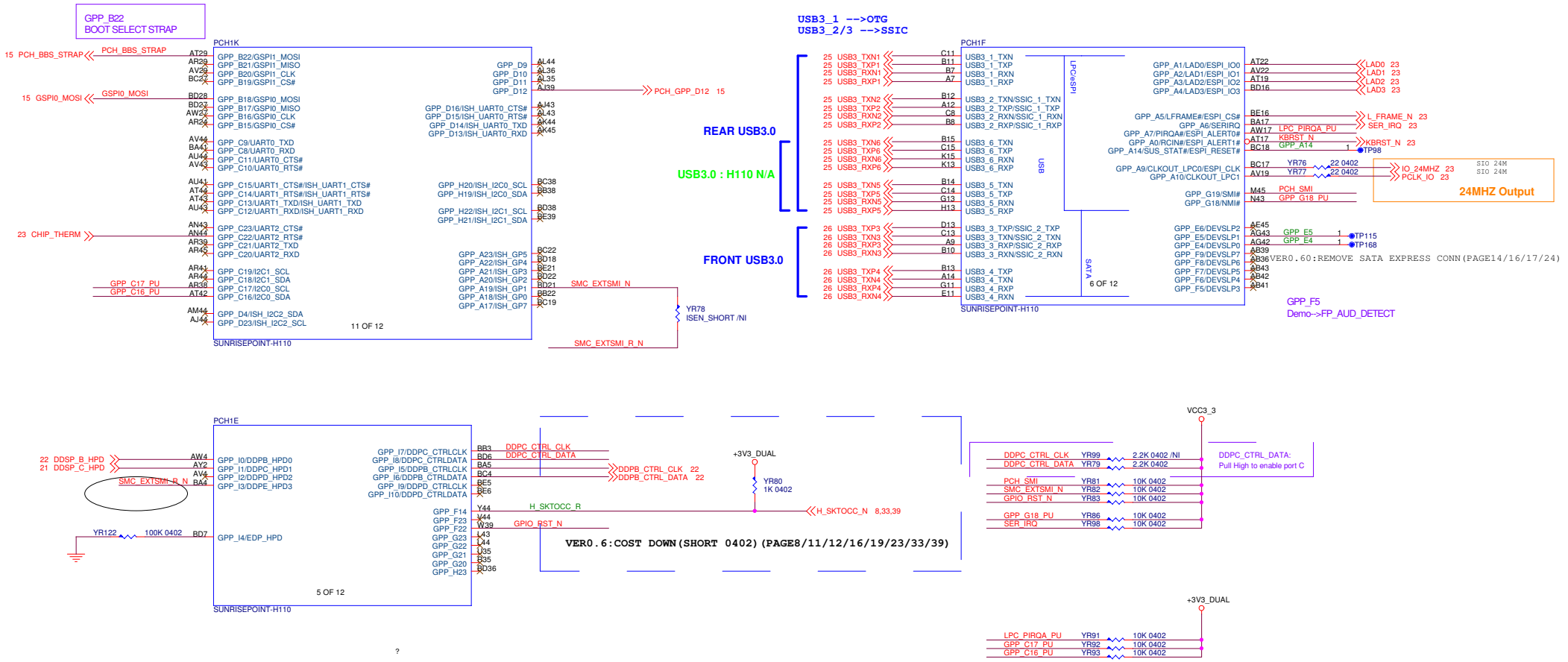
映泰股份有限公司 BIOSTAR GROUP

Title	PCH CLINK/SATA/CPU HOST	
Size B	Document Number IH11V-MHS	Rev 7.0
Date: Thursday, January 28, 2016	Sheet 14 of 42	



Title	PCH LPC/HDA/SPI/MISC
Size	Custom
Document Number	IH11V-MHS
Rev	7.0
Date:	Thursday, January 28, 2016
Sheet	15 of 42

PCH PART: Y+Reference



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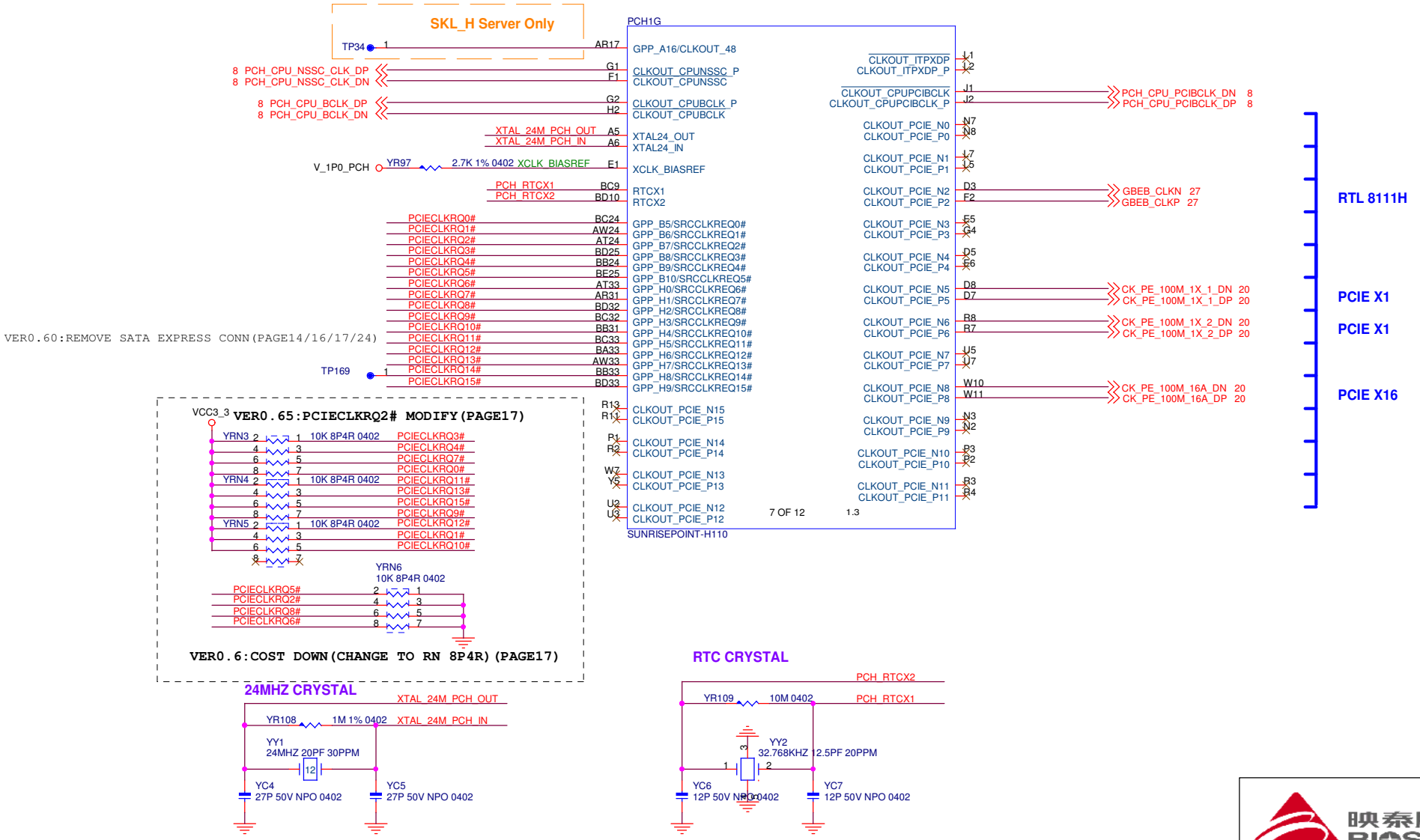
Title	PCH LPC/DP/USB3/UART	
Size: Custom	Document Number: IH11V-MHS	Rev: 7.0
Date: Thursday, January 28, 2016	Sheet 16 of 42	



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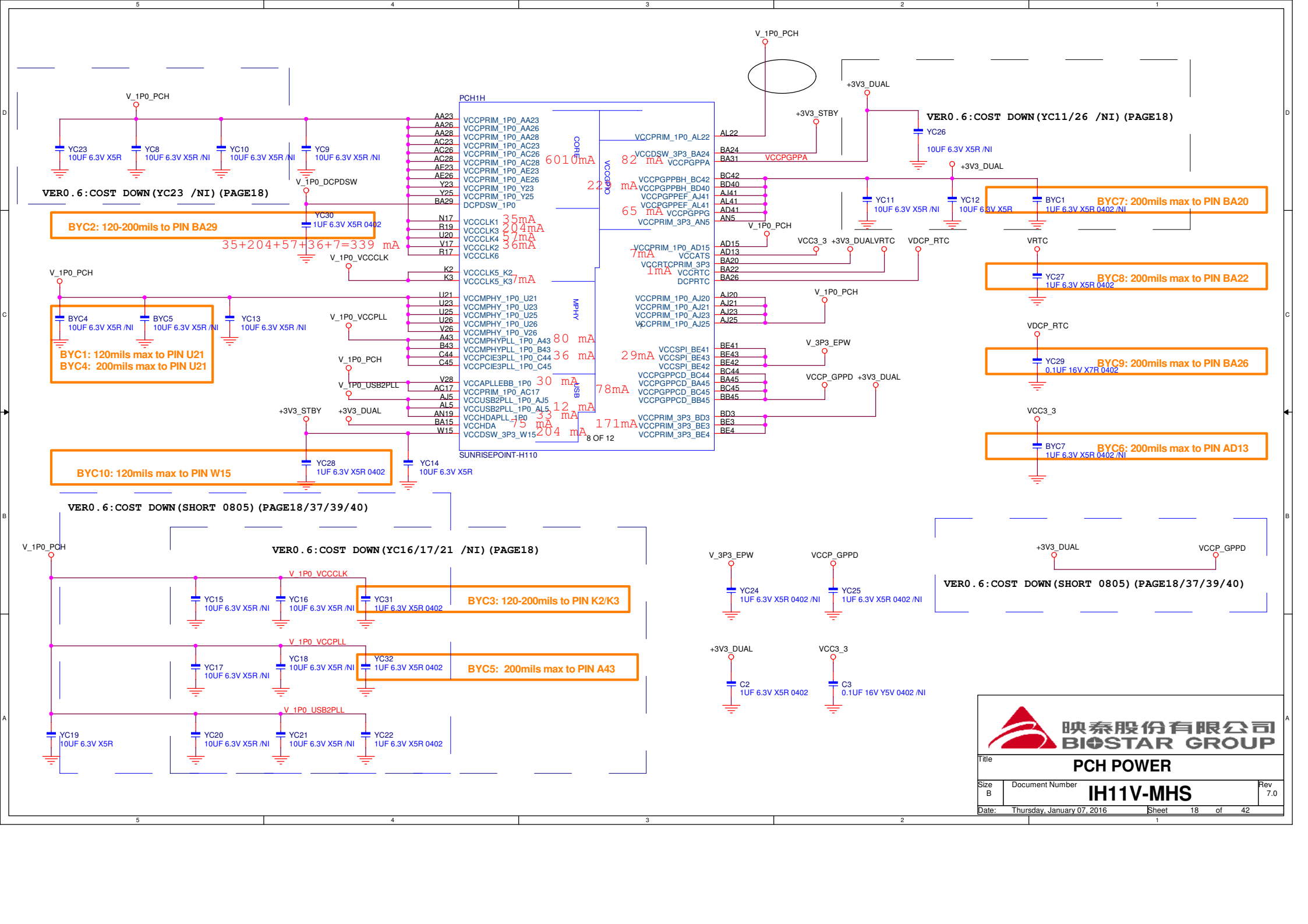
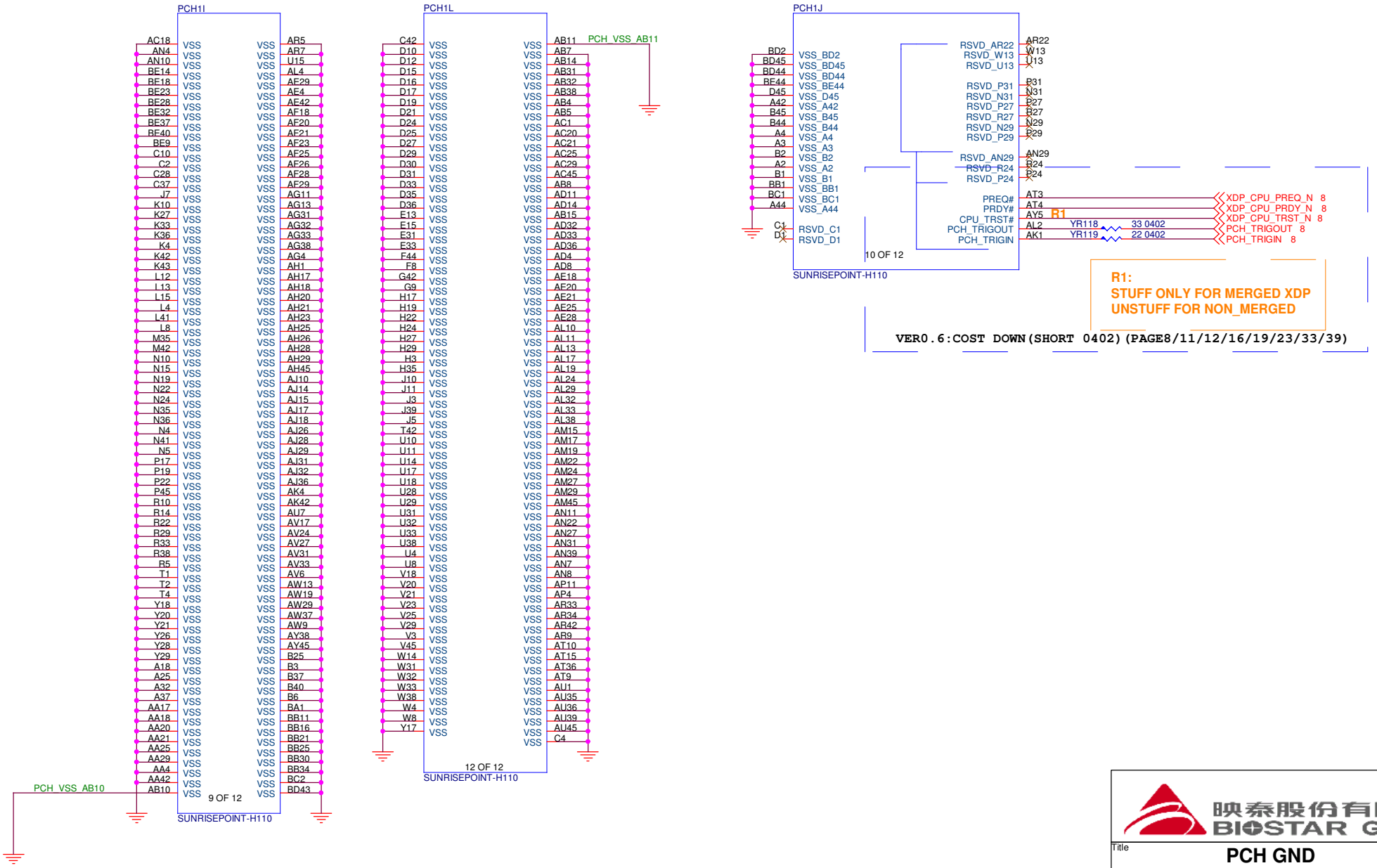
Title	PCH CLOCK BUFFER	
Size B	Document Number IH11V-MHS	Rev 7.0
Date: Thursday, January 28, 2016	Sheet 17 of 42	


V_1P0_PCH
YC23 10UF 6.3V X5R
YC8 10UF 6.3V X5R /NI
YC10 10UF 6.3V X5R /NI
YC9 10UF 6.3V X5R /NI
VER0.6:COST DOWN(YC23 /NI)(PAGE18)
V_1P0_DCPDSW
YC30 1UF 6.3V X5R 0402
BYC2: 120-200mils to PIN BA29
35+204+57+36+7=339 mA
V_1P0_VCCCLK
V_1P0_PCH
BYC4 10UF 6.3V X5R /NI
BYC5 10UF 6.3V X5R /NI
YC13 10UF 6.3V X5R /NI
BYC1: 120mils max to PIN U21
BYC4: 200mils max to PIN U21
V_1P0_VCCPLL
V_1P0_PCH
V_1P0_USB2PLL
+3V3_STBY
+3V3_DUAL
YC28 1UF 6.3V X5R 0402
YC14 10UF 6.3V X5R
BYC10: 120mils max to PIN W15
PCH1H
AA23 VCCPRIM_1P0_AA23
AA26 VCCPRIM_1P0_AA26
AA28 VCCPRIM_1P0_AA28
AC23 VCCPRIM_1P0_AC23
AC26 VCCPRIM_1P0_AC26
AC28 VCCPRIM_1P0_AC28
AE23 VCCPRIM_1P0_AE23
AE26 VCCPRIM_1P0_AE26
Y23 VCCPRIM_1P0_Y23
Y25 VCCPRIM_1P0_Y25
BA29 DCPDSW_1P0
N17 VCCCLK1
R19 VCCCLK3
U20 VCCCLK4
V17 VCCCLK2
R17 VCCCLK6
K2 VCCCLK5_K2
K3 VCCCLK5_K3
U21 VCCMPHY_1P0_U21
U23 VCCMPHY_1P0_U23
U25 VCCMPHY_1P0_U25
U26 VCCMPHY_1P0_U26
V26 VCCMPHY_1P0_V26
A43 VCCMPHYPLL_1P0_A43
B43 VCCMPHYPLL_1P0_B43
C44 VCCPCIE3PLL_1P0_C44
C45 VCCPCIE3PLL_1P0_C45
V28 VCCAPLLEBB_1P0
AC17 VCCPRIM_1P0_AC17
AJ5 VCCUSB2PLL_1P0_AJ5
AL5 VCCUSB2PLL_1P0_AL5
AN19 VCCHDAPLL_1P0
BA15 VCCHDA
W15 VCCDSW_3P3_W15
CORE
6010mA
VCCGPPC
VCCPRIM_1P0_AL22
AL22
BA24 VCCDSW_3P3_BA24
BA31 VCCPGPPA
82 mA
22 mA
65 mA
VCCPGPPBH_BC42
VCCPGPPBH_BD40
VCCPGPPEF_AJ41
VCCPGPPEF_AL41
VCCPGPPG
VCCPRIM_3P3_AN5
BC42
BD40
AJ41
AL41
AD41
AN5
MPHY
35mA
204mA
57mA
36mA
7mA
80 mA
36 mA
30 mA
12 mA
33 mA
75 mA
204 mA
8 OF 12
VCCPRIM_1P0_AD15
VCCATS
VCCRTCPRIM_3P3
VCCRTC
DCPRTC
AD15
AD13
BA20
BA22
BA26
7mA
1mA
VCCPRIM_1P0_AJ20
VCCPRIM_1P0_AJ21
VCCPRIM_1P0_AJ23
VCCPRIM_1P0_AJ25
AJ20
AJ21
AJ23
AJ25
VCCSPI_BE41
VCCSPI_BE43
VCCSPI_BE42
BE41
BE43
BE42
29mA
USB
78mA
VCCPGPPCD_BC44
VCCPGPPCD_BA45
VCCPGPPCD_BC45
VCCPGPPCD_BB45
BC44
BA45
BC45
BB45
VCCPRIM_3P3_BD3
VCCPRIM_3P3_BE3
VCCPRIM_3P3_BE4
BD3
BE3
BE4
171mA
SUNRISEPOINT-H110
+3V3_DUAL
+3V3_STBY
VCCPGPPA
YC26 10UF 6.3V X5R /NI
VER0.6:COST DOWN(YC11/26 /NI)(PAGE18)
YC11 10UF 6.3V X5R /NI
YC12 10UF 6.3V X5R
BYC1 1UF 6.3V X5R 0402 /NI
BYC7: 200mils max to PIN BA20
VCC3_3
+3V3_DUALVRTC
VDCP_RTC
VRTC
YC27 1UF 6.3V X5R 0402
BYC8: 200mils max to PIN BA22
V_3P3_EPW
VCCP_GPPD
YC29 0.1UF 16V X7R 0402
BYC9: 200mils max to PIN BA26
BYC7 1UF 6.3V X5R 0402 /NI
BYC6: 200mils max to PIN AD13
VER0.6:COST DOWN(SHORT 0805)(PAGE18/37/39/40)
VER0.6:COST DOWN(YC16/17/21 /NI)(PAGE18)
V_1P0_VCCCLK
YC15 10UF 6.3V X5R /NI
YC16 10UF 6.3V X5R /NI
YC31 1UF 6.3V X5R 0402
BYC3: 120-200mils to PIN K2/K3
V_1P0_VCCPLL
YC17 10UF 6.3V X5R /NI
YC18 10UF 6.3V X5R /NI
YC32 1UF 6.3V X5R 0402
BYC5: 200mils max to PIN A43
V_1P0_USB2PLL
YC19 10UF 6.3V X5R
YC20 10UF 6.3V X5R /NI
YC21 10UF 6.3V X5R /NI
YC22 1UF 6.3V X5R 0402
V_3P3_EPW
YC24 1UF 6.3V X5R 0402 /NI
VCCP_GPPD
YC25 1UF 6.3V X5R 0402 /NI
+3V3_DUAL
C2 1UF 6.3V X5R 0402
VCC3_3
C3 0.1UF 16V Y5V 0402 /NI
+3V3_DUAL
VCCP_GPPD
VER0.6:COST DOWN(SHORT 0805)(PAGE18/37/39/40)
映泰股份有限公司
BIOSTAR GROUP
Title
PCH POWER
Size B
Document Number
IH11V-MHS
Rev 7.0
Date: Thursday, January 07, 2016
Sheet 18 of 42



映泰股份有限公司
BIOSTAR GROUP

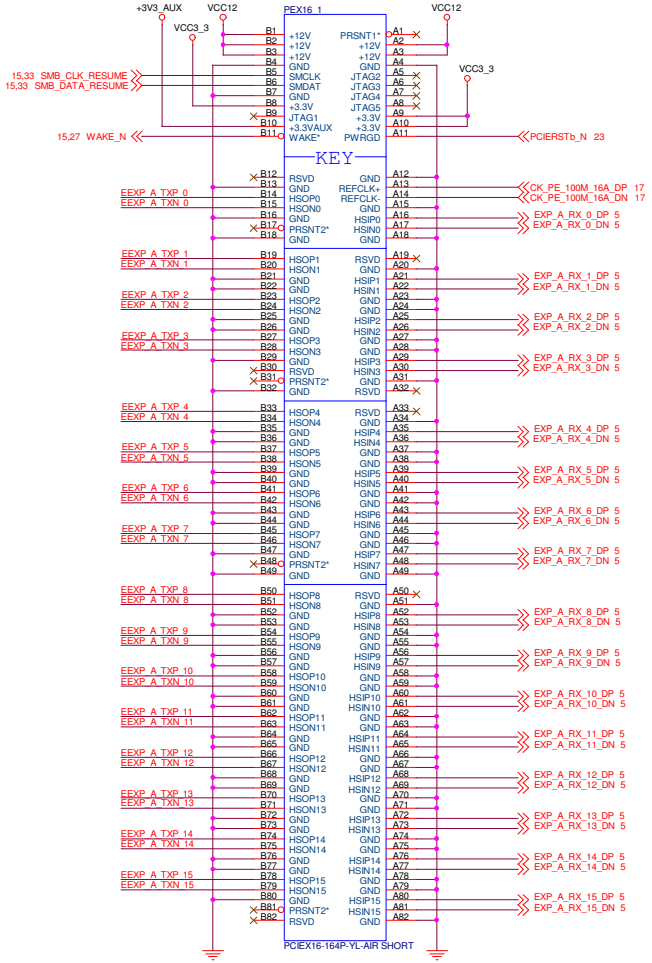
Title	PCH GND	
Size B	Document Number IH11V-MHS	Rev 7.0
Date: Thursday, January 28, 2016	Sheet 19 of 42	

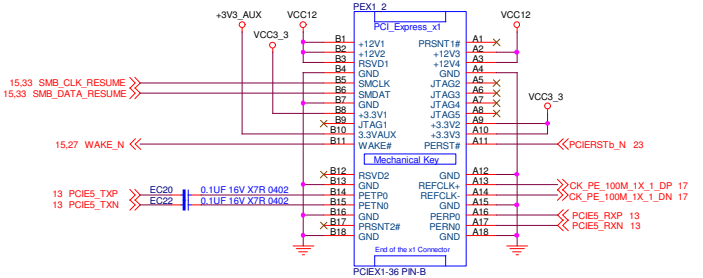
SLOT PART: E+Reference

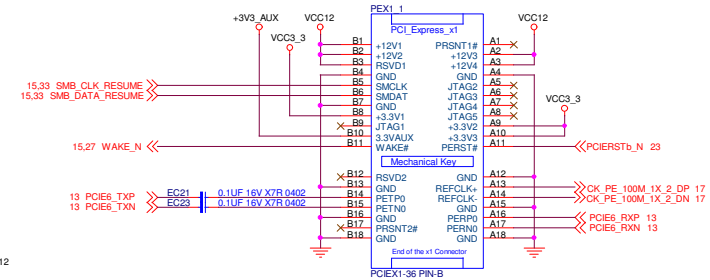
Value:180 nF - 265 nF

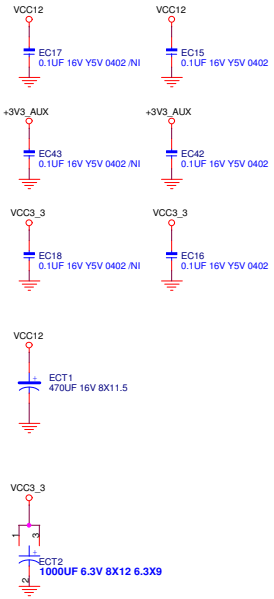
450 mils max to connector pin

5 EXP_A_TX_0_DP	EC1	0.22UF 10V X5R 0402	EEXP_A_TXP_0	
5 EXP_A_TX_0_DN	EC2	0.22UF 10V X5R 0402	EEXP_A_TXN_0	
5 EXP_A_TX_1_DP	EC3	0.22UF 10V X5R 0402	EEXP_A_TXP_1	
5 EXP_A_TX_1_DN	EC4	0.22UF 10V X5R 0402	EEXP_A_TXN_1	
5 EXP_A_TX_2_DP	EC5	0.22UF 10V X5R 0402	EEXP_A_TXP_2	
5 EXP_A_TX_2_DN	EC6	0.22UF 10V X5R 0402	EEXP_A_TXN_2	
5 EXP_A_TX_3_DP	EC7	0.22UF 10V X5R 0402	EEXP_A_TXP_3	
5 EXP_A_TX_3_DN	EC8	0.22UF 10V X5R 0402	EEXP_A_TXN_3	
5 EXP_A_TX_4_DP	EC9	0.22UF 10V X5R 0402	EEXP_A_TXP_4	
5 EXP_A_TX_4_DN	EC10	0.22UF 10V X5R 0402	EEXP_A_TXN_4	
5 EXP_A_TX_5_DP	EC11	0.22UF 10V X5R 0402	EEXP_A_TXP_5	
5 EXP_A_TX_5_DN	EC12	0.22UF 10V X5R 0402	EEXP_A_TXN_5	
5 EXP_A_TX_6_DP	EC13	0.22UF 10V X5R 0402	EEXP_A_TXP_6	
5 EXP_A_TX_6_DN	EC14	0.22UF 10V X5R 0402	EEXP_A_TXN_6	
5 EXP_A_TX_7_DP	EC19	0.22UF 10V X5R 0402	EEXP_A_TXP_7	
5 EXP_A_TX_7_DN	EC28	0.22UF 10V X5R 0402	EEXP_A_TXN_7	
5 EXP_A_TX_8_DP	EC49	0.22UF 10V X5R 0402	EEXP_A_TXP_8	
5 EXP_A_TX_8_DN	EC50	0.22UF 10V X5R 0402	EEXP_A_TXN_8	
5 EXP_A_TX_9_DP	EC30	0.22UF 10V X5R 0402	EEXP_A_TXP_9	
5 EXP_A_TX_9_DN	EC29	0.22UF 10V X5R 0402	EEXP_A_TXN_9	
5 EXP_A_TX_10_DP	EC33	0.22UF 10V X5R 0402	EEXP_A_TXP_10	
5 EXP_A_TX_10_DN	EC35	0.22UF 10V X5R 0402	EEXP_A_TXN_10	
5 EXP_A_TX_11_DP	EC32	0.22UF 10V X5R 0402	EEXP_A_TXP_11	
5 EXP_A_TX_11_DN	EC31	0.22UF 10V X5R 0402	EEXP_A_TXN_11	
5 EXP_A_TX_12_DP	EC37	0.22UF 10V X5R 0402	EEXP_A_TXP_12	
5 EXP_A_TX_12_DN	EC38	0.22UF 10V X5R 0402	EEXP_A_TXN_12	
5 EXP_A_TX_13_DP	EC36	0.22UF 10V X5R 0402	EEXP_A_TXP_13	
5 EXP_A_TX_13_DN	EC34	0.22UF 10V X5R 0402	EEXP_A_TXN_13	
5 EXP_A_TX_14_DP	EC39	0.22UF 10V X5R 0402	EEXP_A_TXP_14	
5 EXP_A_TX_14_DN	EC48	0.22UF 10V X5R 0402	EEXP_A_TXN_14	
5 EXP_A_TX_15_DP	EC40	0.22UF 10V X5R 0402	EEXP_A_TXP_15	
5 EXP_A_TX_15_DN	EC41	0.22UF 10V X5R 0402	EEXP_A_TXN_15	









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Title: PCIEX16 SLOT 1 & 2

Size: C | Document Number: IH11V-MHS | Rev: 7.0

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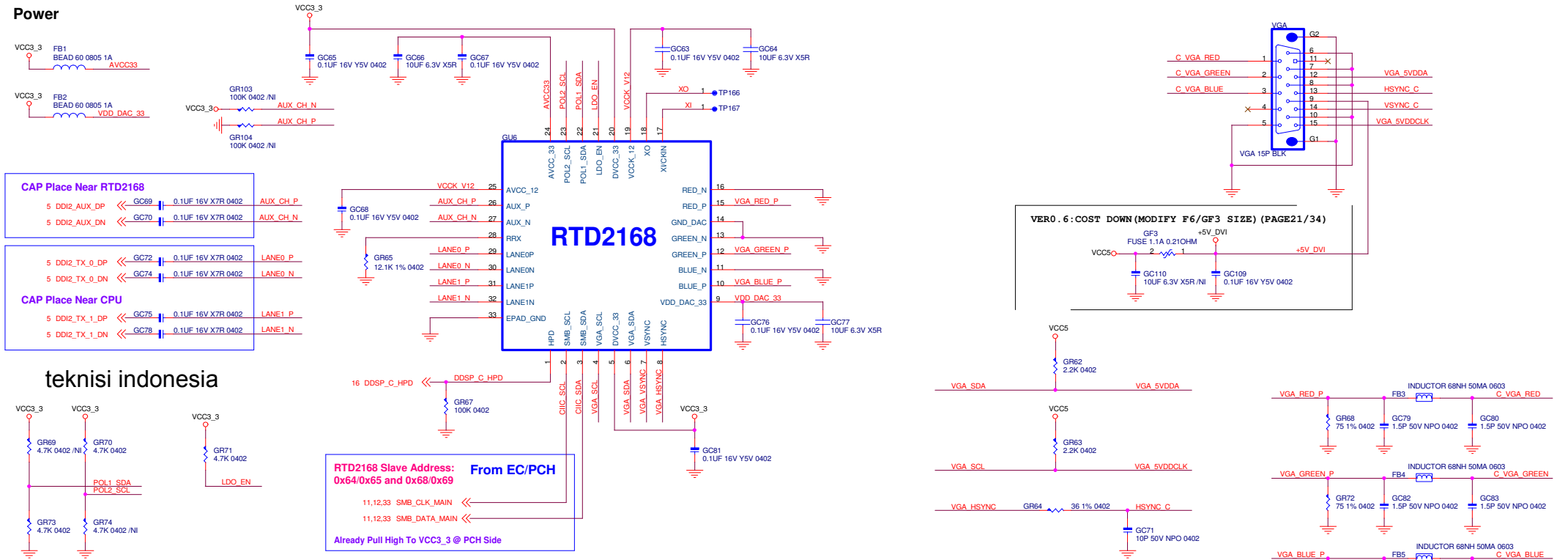

Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	**EEPROM MODE**

Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	**VCCK_V12 from Embedded LDO**

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW

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Title: **RTD2168 EDP to VGA**

Size: Custom | Document Number: **IH11V-MHS** | Rev: 7.0

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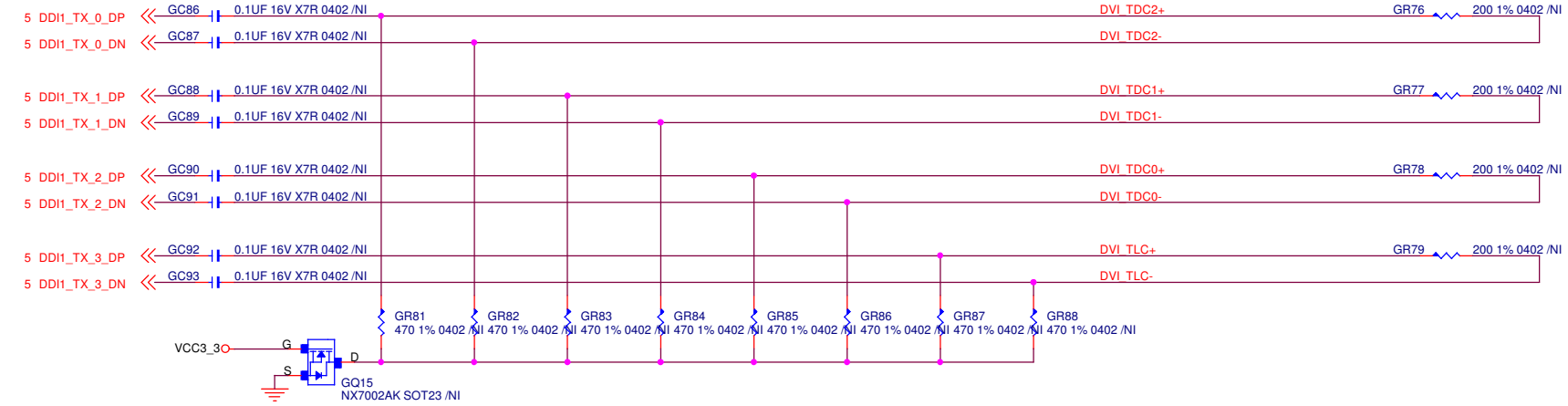

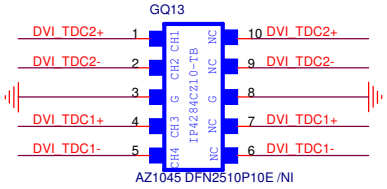

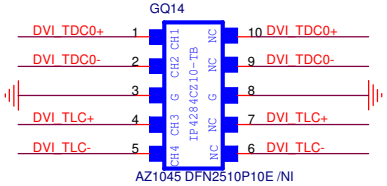

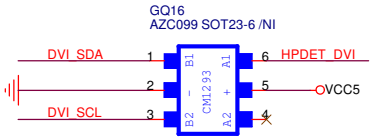

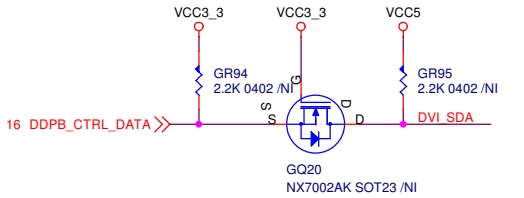

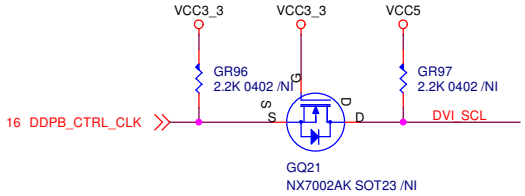

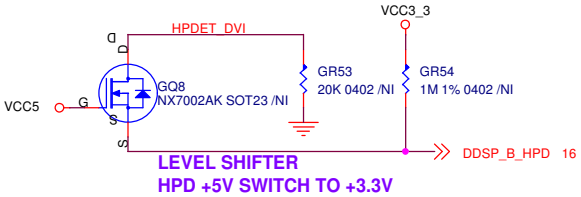

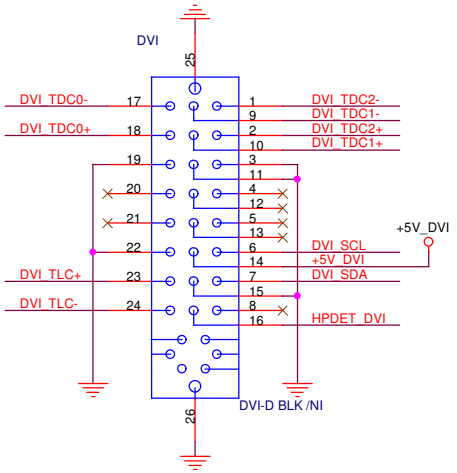

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Title: DVI-I CONNECTOR

Size: B | Document Number: IH11V-MHS | Rev: 7.0

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VER0.6:IO MODIFY BY KEVIN(PAGE23/27)

VER0.6:COST DOWN(SHORT 0402)(PAGE8/11/12/16/19/23/33/39)

IT8613E LQFP64

VER0.6:ATXPG MODIFY(PAGE23/36)
VER0.60:REMOVE Hi-Fi FUNCTION(PAGE28/29)

VER0.6:IO MODIFY BY KEVIN(PAGE23/27)

VER0.65:IO MODIFY BY PETER(PAGE23)

SUPERIO PULLS

VCC CAPS

MOS TEMPERATURE

SYSTEM TEMPERATURE

teknisi indonesia

64-LQFP

VER0.6:IO MODIFY BY KEVIN(PAGE23/27)

VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)

HARDWARE MONITOR

Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-24		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-56		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-58		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-60		0	Enable K8 Power Sequence

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)

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Title: SIO IT8613E

Size: Custom | Document Number: IH11V-MHS | Rev: 7.0

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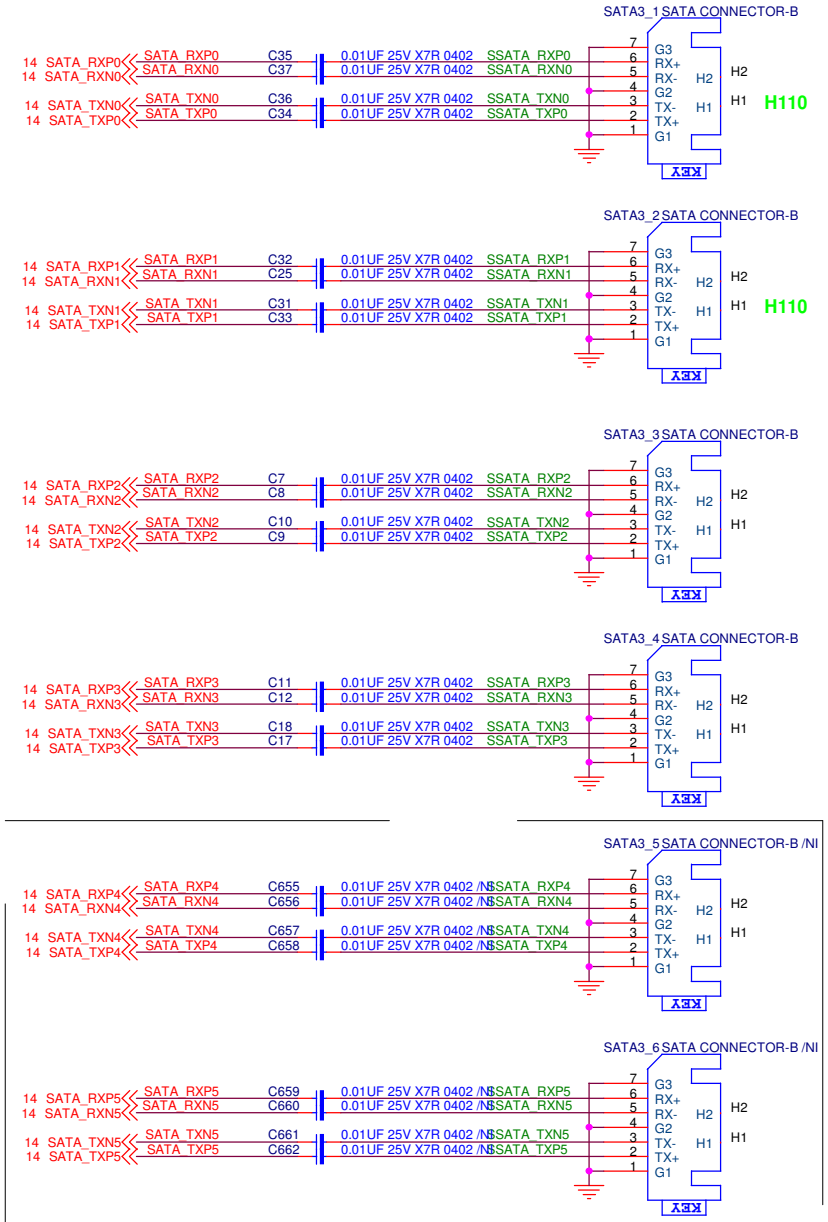

VER0.65:NEW ADD SATA CONN(PAGE14/24)

VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

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Title: SATA EXPRESS

Size	Document Number	Rev
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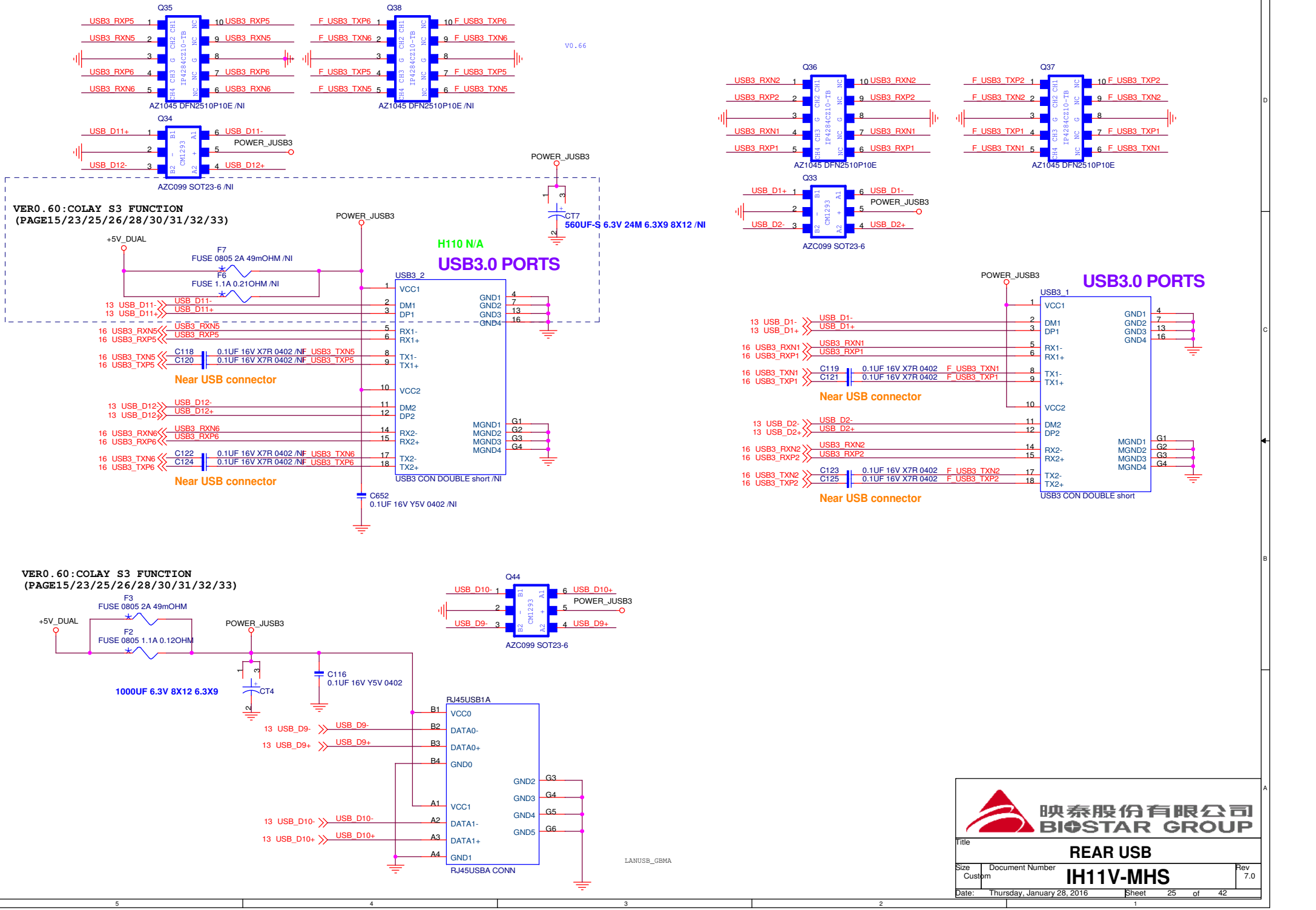
Q35
USB3_RXP5
USB3_RXN5
USB3_RXP6
USB3_RXN6
AZ1045 DFN2510P10E /NI
Q38
F_USB3_TXP6
F_USB3_TXN6
F_USB3_TXP5
F_USB3_TXN5
AZ1045 DFN2510P10E /NI
V0.66
Q34
USB_D11+
USB_D11-
POWER_JUSB3
USB_D12-
USB_D12+
AZC099 SOT23-6 /NI
Q36
USB3_RXN2
USB3_RXP2
USB3_RXN1
USB3_RXP1
AZ1045 DFN2510P10E
Q37
F_USB3_TXP2
F_USB3_TXN2
F_USB3_TXP1
F_USB3_TXN1
AZ1045 DFN2510P10E
Q33
USB_D1+
USB_D1-
POWER_JUSB3
USB_D2-
USB_D2+
AZC099 SOT23-6
VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)
POWER_JUSB3
CT7
560UF-S 6.3V 24M 6.3X9 8X12 /NI
+5V_DUAL
F7
FUSE 0805 2A 49mOHM /NI
F6
FUSE 1.1A 0.21OHM /NI
H110 N/A
USB3.0 PORTS
USB3_2
VCC1
DM1
DP1
RX1-
RX1+
VCC2
DM2
DP2
RX2-
RX2+
TX1-
TX1+
TX2-
TX2+
GND1
GND2
GND3
GND4
MGND1
MGND2
MGND3
MGND4
USB_D11-
USB_D11+
USB3_RXN5
USB3_RXP5
C118
C120
0.1UF 16V X7R 0402 /NI
USB3_TXN5
USB3_TXP5
Near USB connector
USB_D12-
USB_D12+
USB3_RXN6
USB3_RXP6
C122
C124
USB3_TXN6
USB3_TXP6
Near USB connector
USB3 CON DOUBLE short /NI
C652
0.1UF 16V Y5V 0402 /NI
POWER_JUSB3
USB3.0 PORTS
USB3_1
USB_D1-
USB_D1+
USB3_RXN1
USB3_RXP1
C119
C121
0.1UF 16V X7R 0402
F_USB3_TXN1
F_USB3_TXP1
Near USB connector
USB_D2-
USB_D2+
USB3_RXN2
USB3_RXP2
C123
C125
F_USB3_TXN2
F_USB3_TXP2
Near USB connector
USB3 CON DOUBLE short
VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)
F3
FUSE 0805 2A 49mOHM
+5V_DUAL
F2
FUSE 0805 1.1A 0.12OHM
POWER_JUSB3
1000UF 6.3V 8X12 6.3X9
CT4
C116
0.1UF 16V Y5V 0402
Q44
USB_D10-
USB_D10+
POWER_JUSB3
USB_D9-
USB_D9+
AZC099 SOT23-6
RJ45USB1A
VCC0
DATA0-
DATA0+
GND0
VCC1
DATA1-
DATA1+
GND1
GND2
GND3
GND4
GND5
RJ45USBA CONN
LANUSB_GBMA
映泰股份有限公司
BIOSTAR GROUP
Title
REAR USB
Size
Custom
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42

+5V_DUAL

F4
FUSE 0805 2A 49mOHM

F5
FUSE 0805 2A 49mOHM

CT5
1000UF 6.3V 8X12 6.3X9

VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)

POWER_JUSB1

VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

C126
0.1UF 16V Y5V 0402

F_USB1
13 USB_D7-
13 USB_D7+
USB_D7-
USB_D7+
USB_D8-
USB_D8+
USB_D8- 13
USB_D8+ 13
HEADER 2X5 N9 B-USB

POWER_JUSB1

F_USB2
13 USB_D5-
13 USB_D5+
USB_D5-
USB_D5+
USB_D6-
USB_D6+
USB_D6- 13
USB_D6+ 13
HEADER 2X5 N9 B-USB

Q40
USB_D6+
USB_D5+
USB_D6-
USB_D5-
POWER_JUSB1
CM1293
AZC099 SOT23-6

VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

Q39
USB_D7+
USB_D8-
USB_D7-
USB_D8+
POWER_JUSB1
CM1293
AZC099 SOT23-6

Q43
USB_D4-
USB_D3-
USB_D4+
USB_D3+
POWER_JUSB1
CM1293
AZC099 SOT23-6

VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

Q41
F_USB3_TXN3
F_USB3_TXP3
F_USB3_TXN4
F_USB3_TXP4
IP4284CZ10-TB
AZ1045 DFN2510P10E

Q42
USB3_RXN3
USB3_RXP3
USB3_RXN4
USB3_RXP4
IP4284CZ10-TB
AZ1045 DFN2510P10E

VER0.6:COST DOWN(POWER_JUSB1 COLAY POWER_JUSB2)(PAGE26)

VER0.6:COST DOWN(REMOVE CT6)(PAGE26)

POWER_JUSB1

C128
0.1UF 16V Y5V 0402

CT16
560UF-S 6.3V 24M 6.3X9 8X12 /NI

JFRONT_USB3_1
VBUS0
ID
VBUS1
SSRX1-
SSRX1+
SSRX2-
SSRX2+
SSTX1-
SSTX1+
SSTX2-
SSTX2+
D1-
D1+
D2-
D2+
GND_1
GND_0
GND_3
GND_4
BOX 2X10 N20-B USB3

16 USB3_RXN3
16 USB3_RXP3
USB3_RXN3
USB3_RXP3
USB3_RXN4
USB3_RXP4
USB3_RXN4 16
USB3_RXP4 16

C129
C131
0.1UF 16V X7R 0402
F_USB3_TXN3
F_USB3_TXP3
16 USB3_TXN3
16 USB3_TXP3
Near USB connector

C130
C132
0.1UF 16V X7R 0402
F_USB3_TXN4
F_USB3_TXP4
USB3_TXN4 16
USB3_TXP4 16
Near USB connector

13 USB_D3-
13 USB_D3+
USB_D3-
USB_D3+
USB_D4-
USB_D4+
USB_D4- 13
USB_D4+ 13

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Title: FRONT USB

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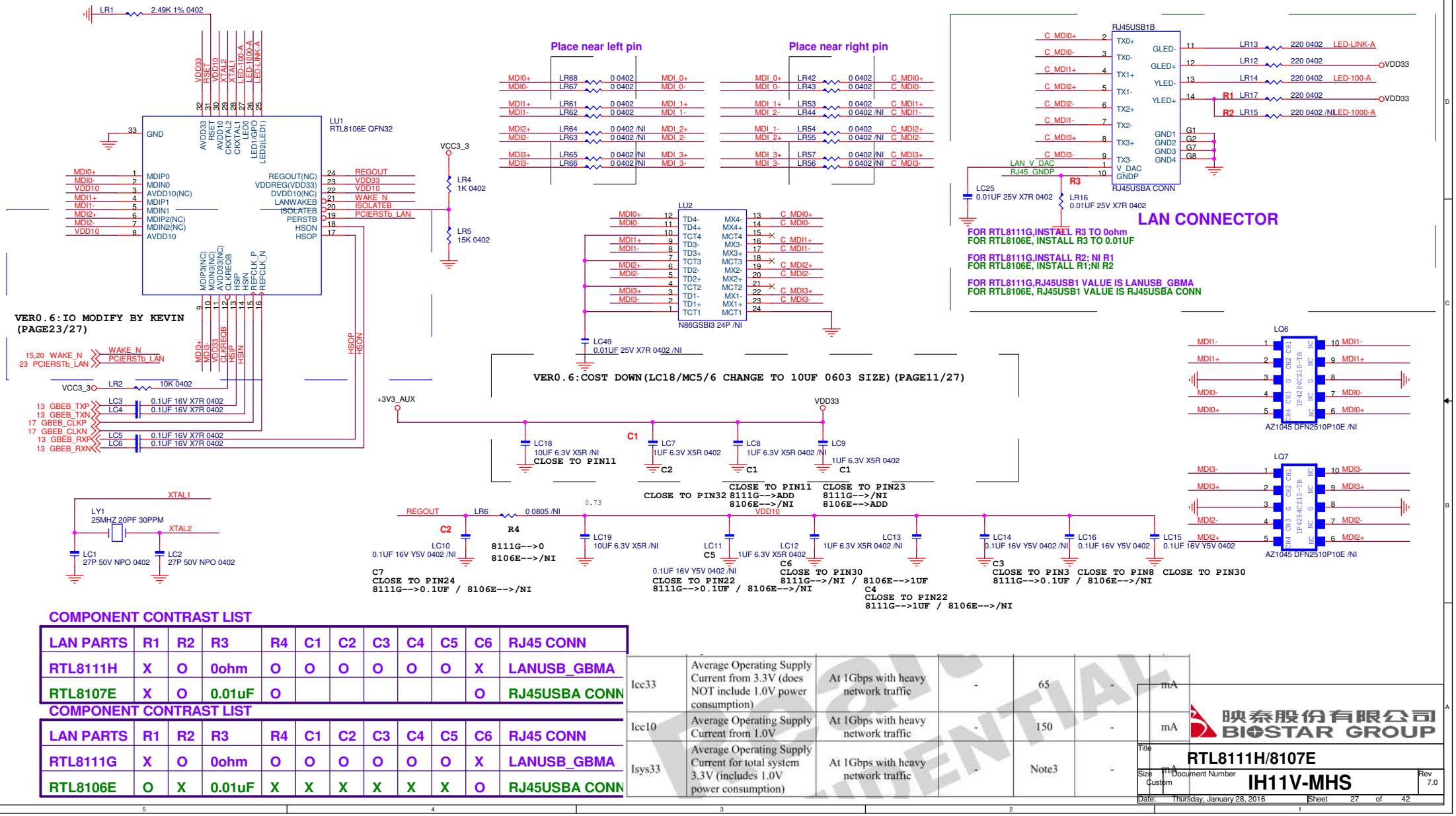

COMPONENT CONTRAST LIST

LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111H	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8107E	X	O	0.01uF	O						O	RJ45USBA CONN

COMPONENT CONTRAST LIST

LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111G	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8106E	O	X	0.01uF	X	X	X	X	X	X	O	RJ45USBA CONN

Icc33	Average Operating Supply Current from 3.3V (does NOT include 1.0V power consumption)	At 1Gbps with heavy network traffic	-	65	-	mA
Icc10	Average Operating Supply Current from 1.0V	At 1Gbps with heavy network traffic	-	150	-	mA
Isys33	Average Operating Supply Current for total system 3.3V (includes 1.0V power consumption)	At 1Gbps with heavy network traffic	-	Note3	-	mA

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Title: RTL8111H/8107E

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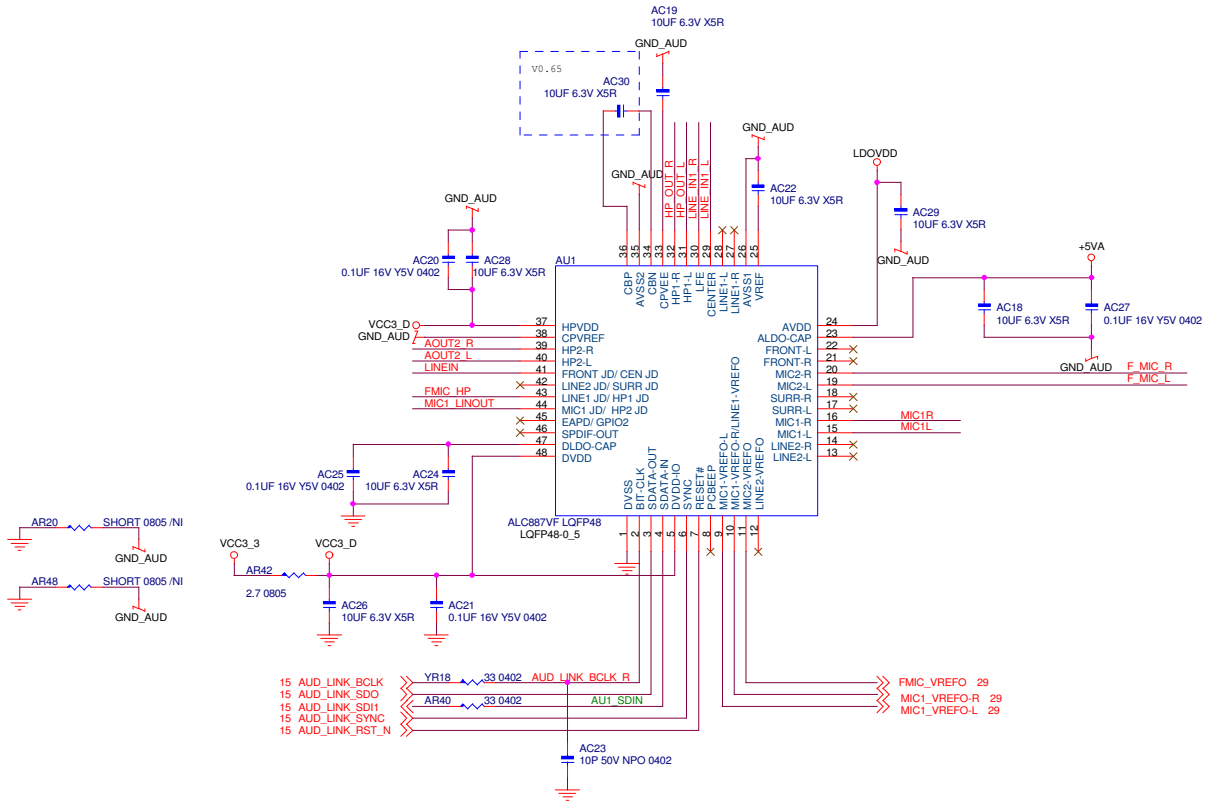

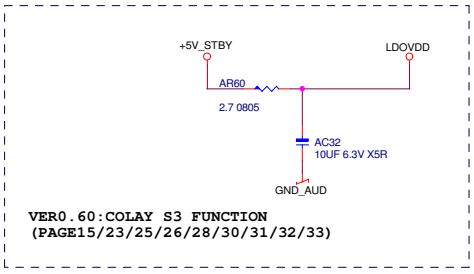

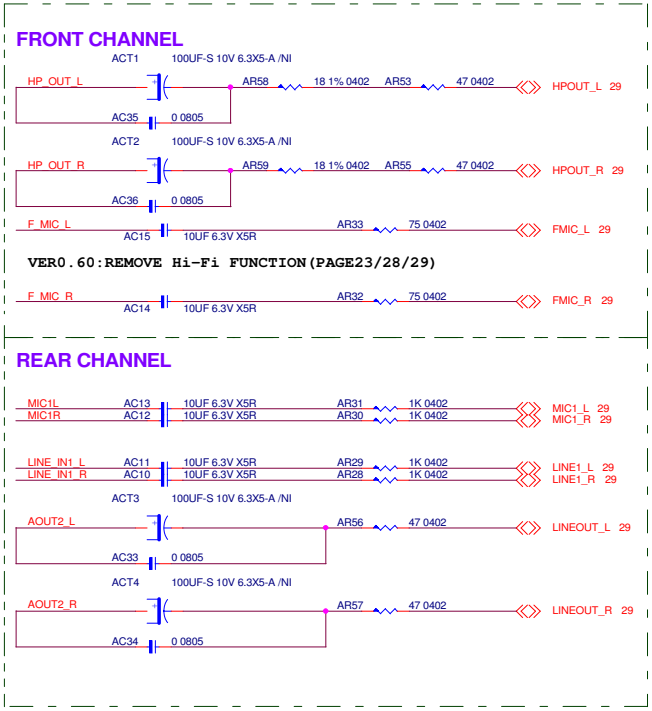

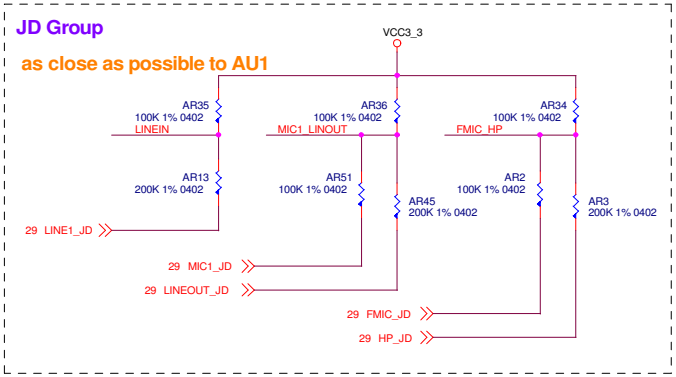

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Title: AUDIO CODEC ALC887

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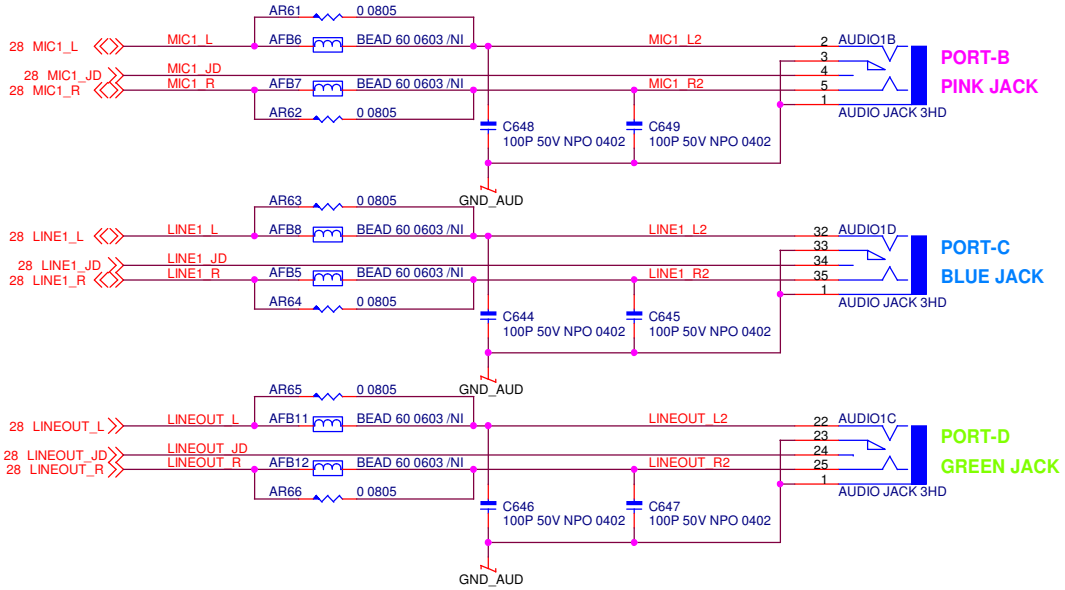
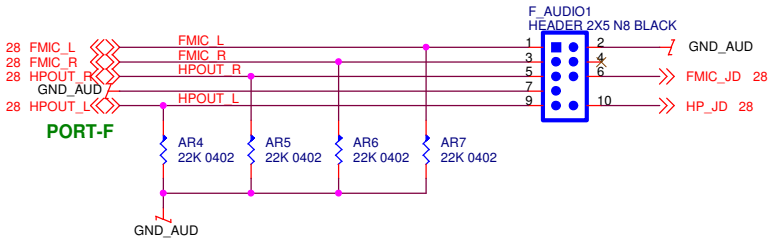
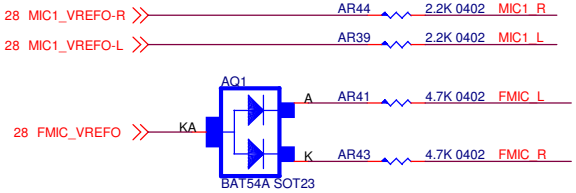


FRONT AUDIO HEADER

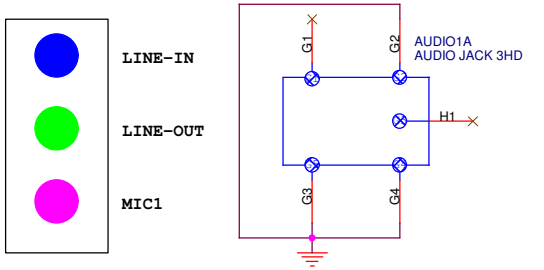


MIC VREF



SPDIF CONNECTOR

V0.66



AUDIO JACKS SHEEL

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Title	AUDIO CONNECTOR	
Size B	Document Number IH11V-MHS	Rev 7.0
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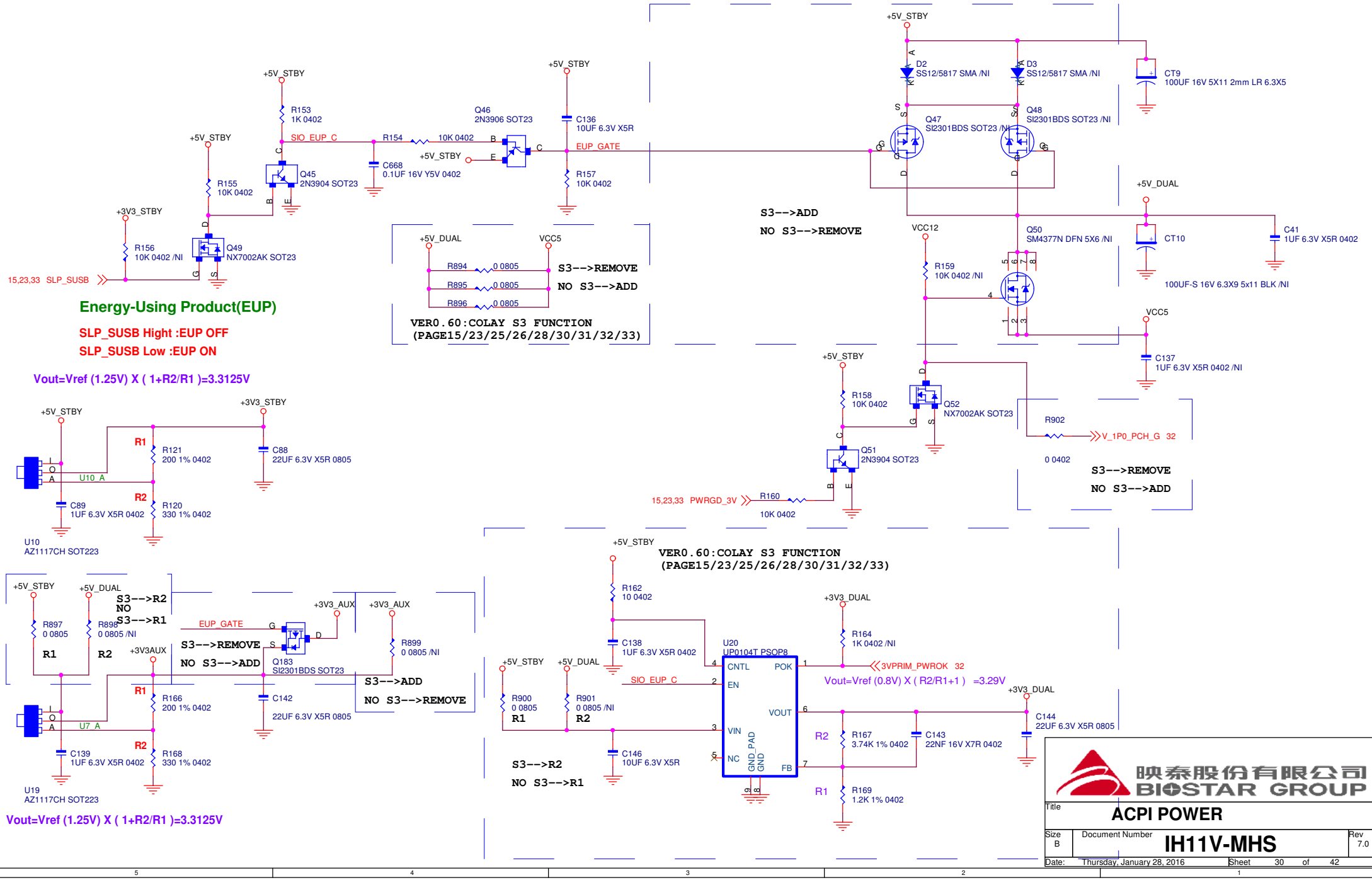

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Title	ACPI POWER	
Size B	Document Number IH11V-MHS	Rev 7.0
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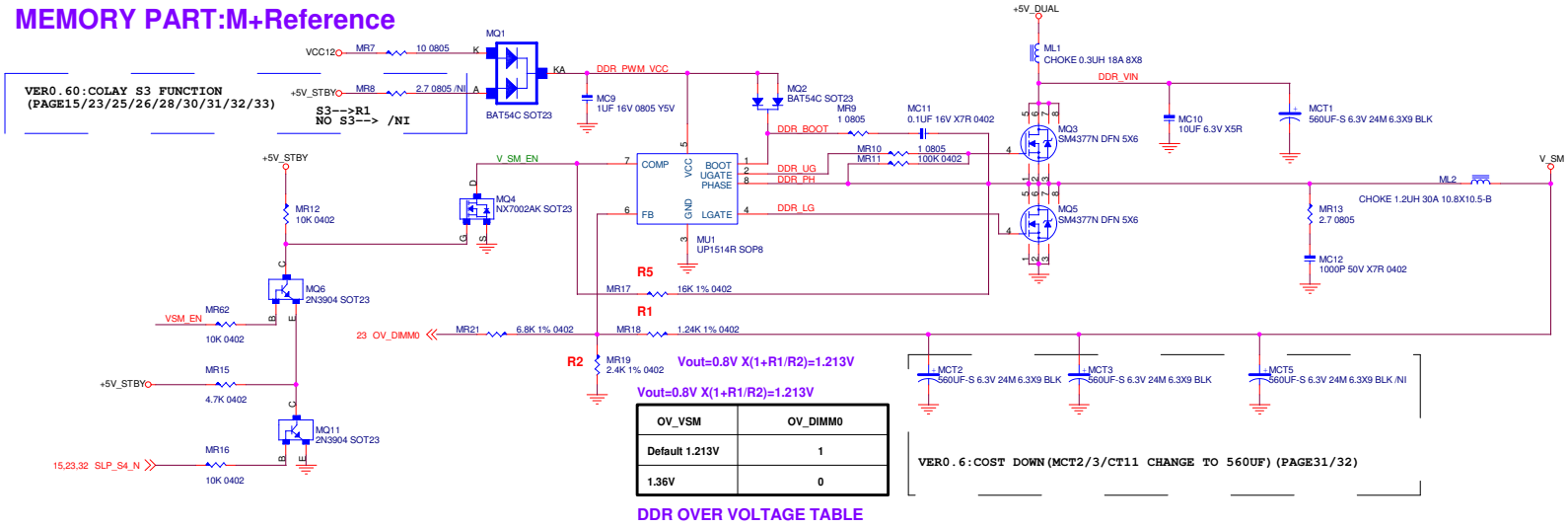
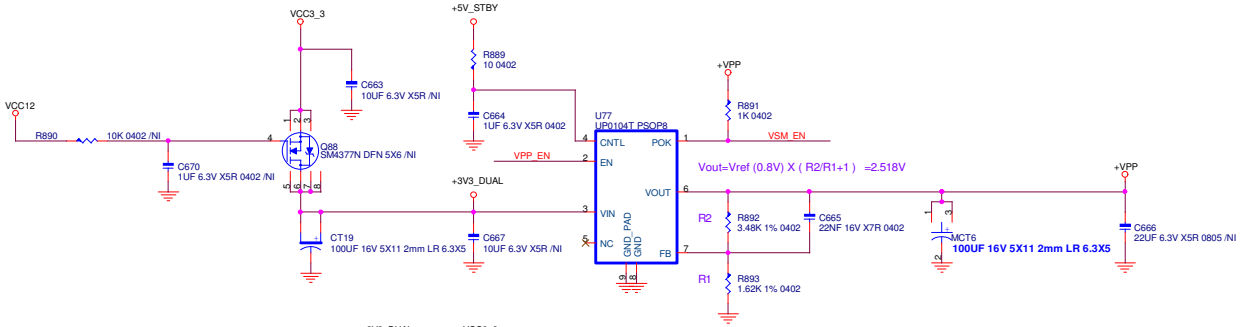
MEMORY PART:M+Reference

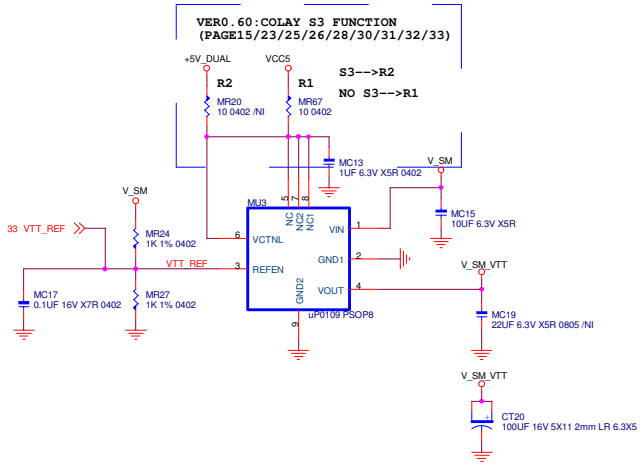


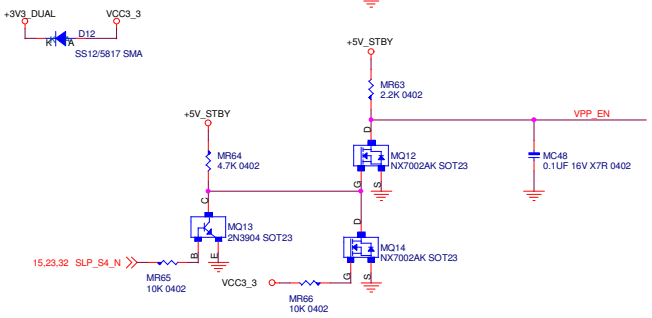
Vout=0.8V X(1+R1/R2)=1.213V

OV_VSM	OV_DIMM0
Default 1.213V	1
1.36V	0

DDR OVER VOLTAGE TABLE







映泰股份有限公司 BIOSTAR GROUP

Title: MEMORY DC-DC

Size: C | Document Number: IH11V-MHS | Rev: 7.0

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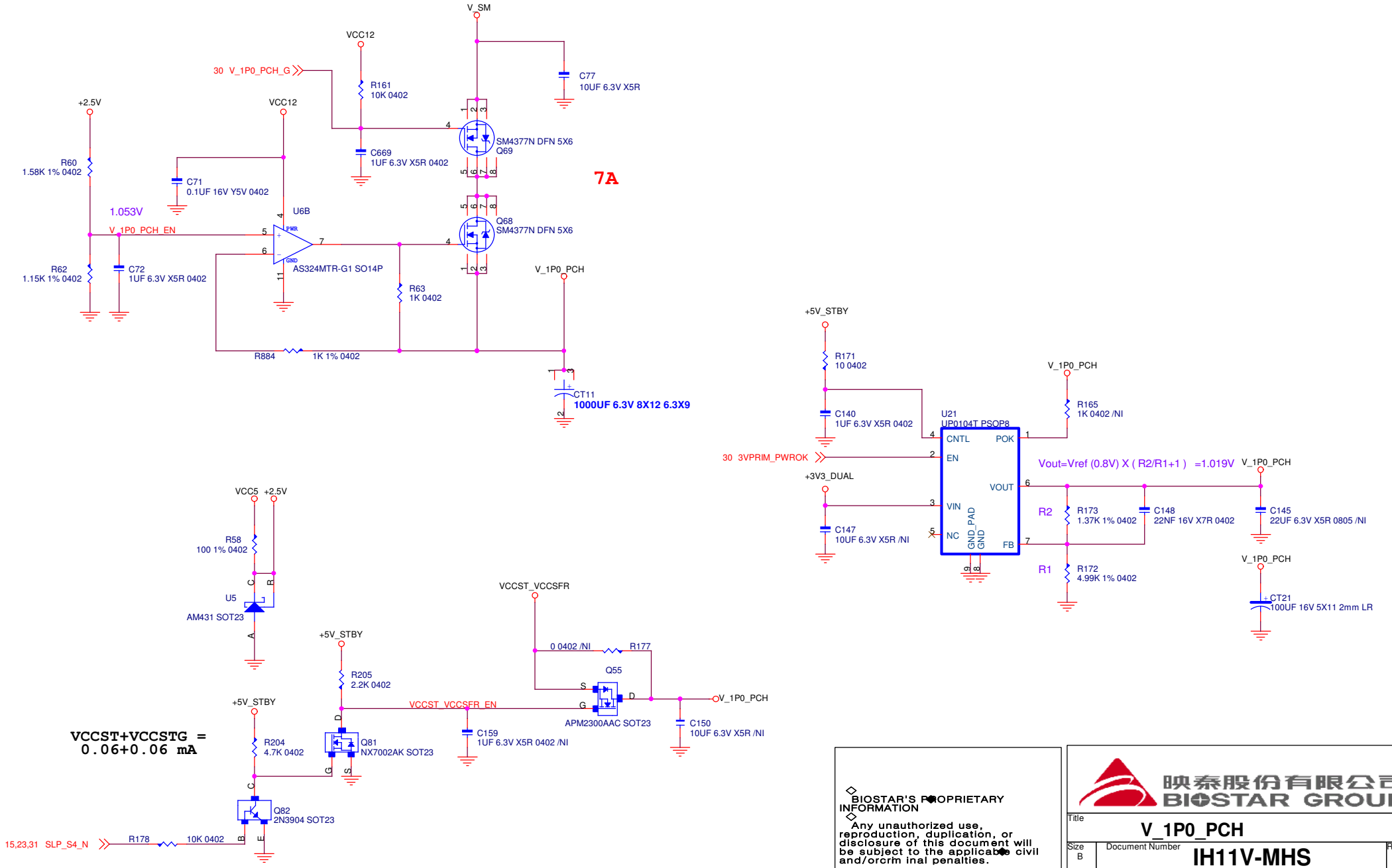

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Title	V_1P0_PCH	
Size B	Document Number IH11V-MHS	Rev 7.0
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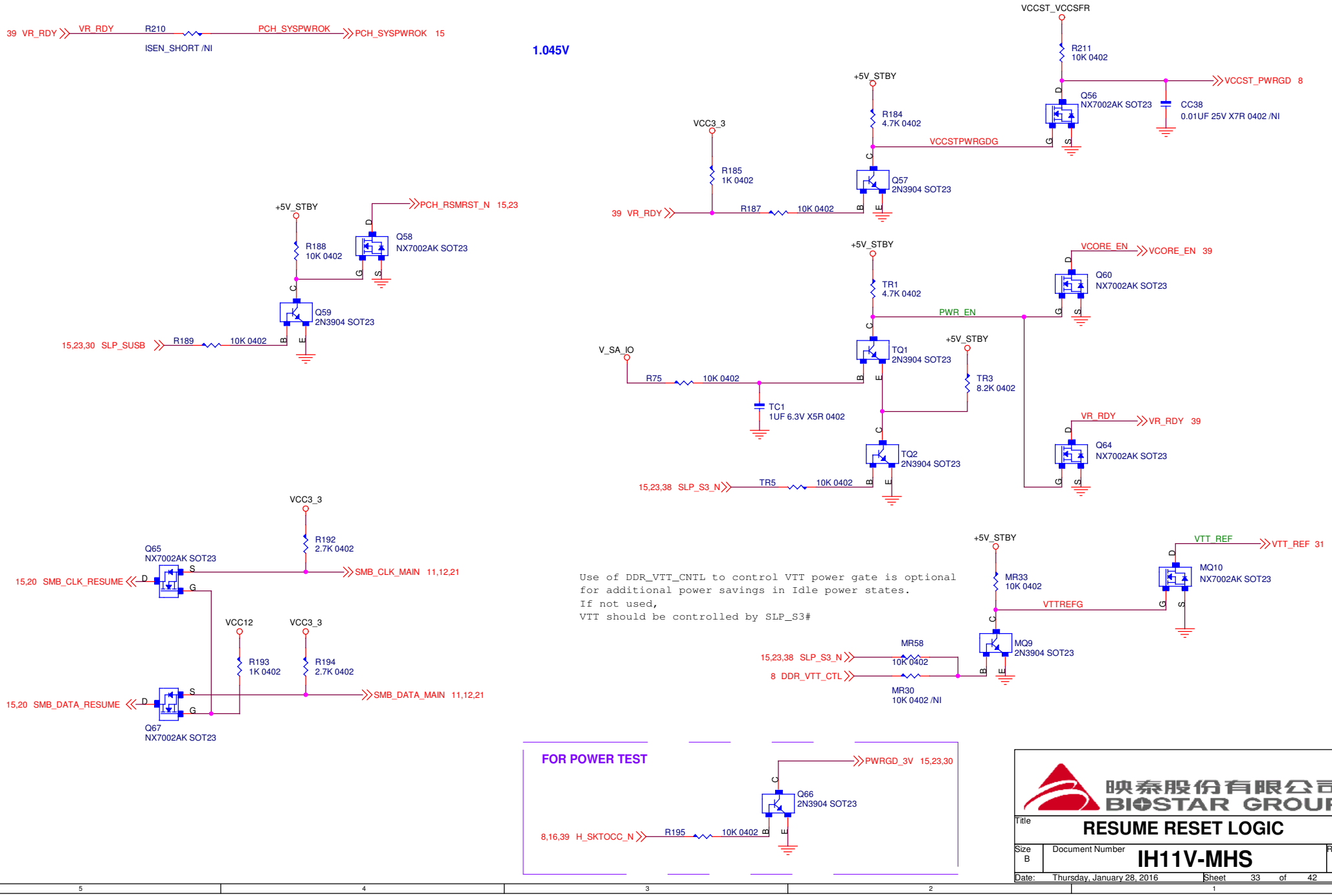
39 VR_RDY
VR_RDY
R210
ISEN_SHORT /NI
PCH_SYSPWROK
PCH_SYSPWROK 15
1.045V
VCCST_VCCSFR
R211
10K 0402
VCCST_PWRGD 8
+5V_STBY
R184
4.7K 0402
Q56
NX7002AK SOT23
CC38
0.01UF 25V X7R 0402 /NI
VCC3_3
VCCSTPWRGDG
R185
1K 0402
Q57
2N3904 SOT23
39 VR_RDY
R187
10K 0402
+5V_STBY
PCH_RSMRST_N 15,23
R188
10K 0402
Q58
NX7002AK SOT23
Q59
2N3904 SOT23
15,23,30 SLP_SUSB
R189
10K 0402
+5V_STBY
VCORE_EN
VCORE_EN 39
TR1
4.7K 0402
Q60
NX7002AK SOT23
PWR_EN
V_SA_IO
TQ1
2N3904 SOT23
+5V_STBY
R75
10K 0402
TR3
8.2K 0402
TC1
1UF 6.3V X5R 0402
VR_RDY
VR_RDY 39
Q64
NX7002AK SOT23
TQ2
2N3904 SOT23
15,23,38 SLP_S3_N
TR5
10K 0402
VCC3_3
R192
2.7K 0402
Q65
NX7002AK SOT23
15,20 SMB_CLK_RESUME
SMB_CLK_MAIN 11,12,21
VCC12
VCC3_3
R193
1K 0402
R194
2.7K 0402
15,20 SMB_DATA_RESUME
SMB_DATA_MAIN 11,12,21
Q67
NX7002AK SOT23
Use of DDR_VTT_CNTL to control VTT power gate is optional
for additional power savings in Idle power states.
If not used,
VTT should be controlled by SLP_S3#
+5V_STBY
MR33
10K 0402
VTT_REF
VTT_REF 31
MQ10
NX7002AK SOT23
VTTREFG
MQ9
2N3904 SOT23
MR58
10K 0402
15,23,38 SLP_S3_N
8 DDR_VTT_CTL
MR30
10K 0402 /NI
FOR POWER TEST
PWRGD_3V 15,23,30
Q66
2N3904 SOT23
8,16,39 H_SKTOCC_N
R195
10K 0402
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BIOSTAR GROUP
Title
RESUME RESET LOGIC
Size
B
Document Number
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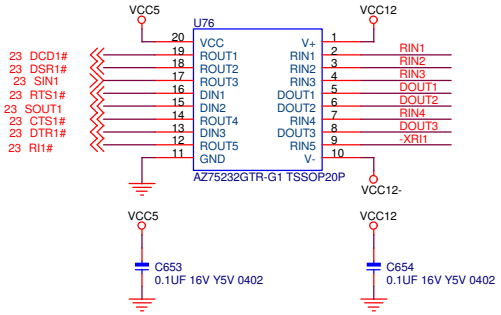
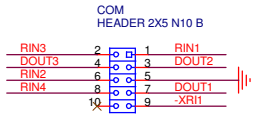
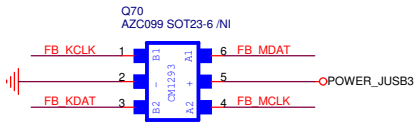




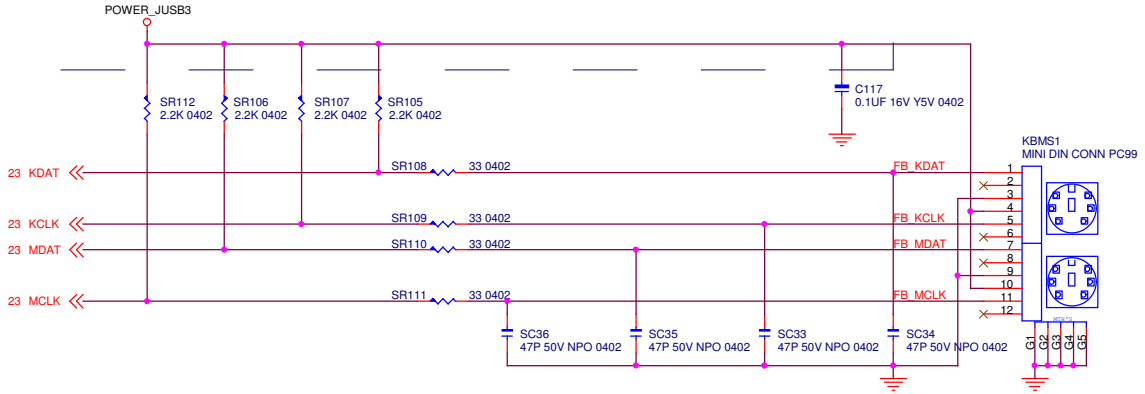
COM PORT

WAKE ON RING

KEYBOARD & MOUSE



VER0.6:COST DOWN(POWER_JUSB4/POWER_JUSB5 COLAY)(PAGE25/34)



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Title	COM1 / PS2 CONN	
Size: Custom	Document Number: IH11V-MHS	Rev: 7.0
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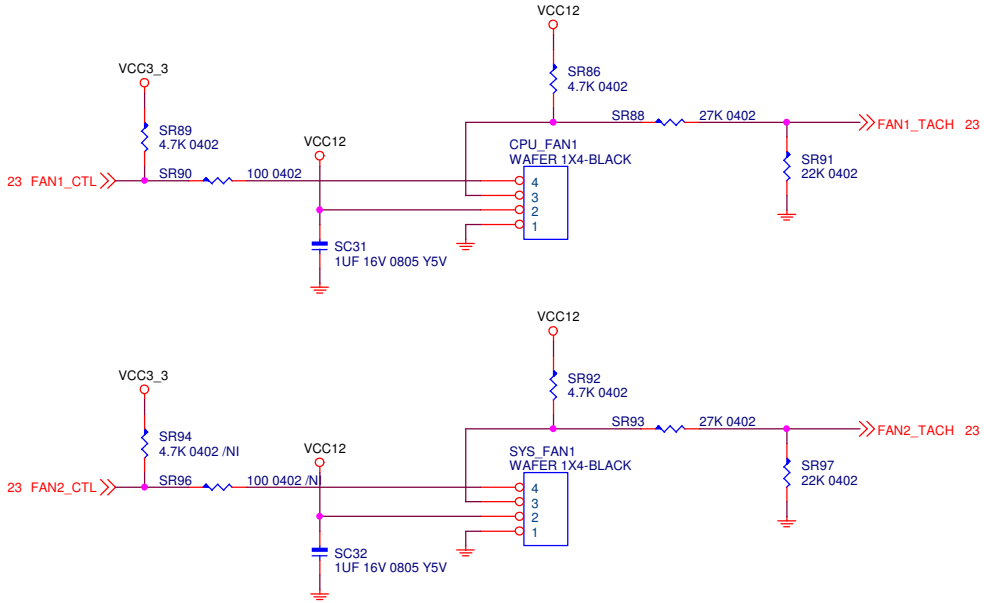

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Title: FAN & PS2

Size	Document Number	Rev
B	IH11V-MHS	7.0

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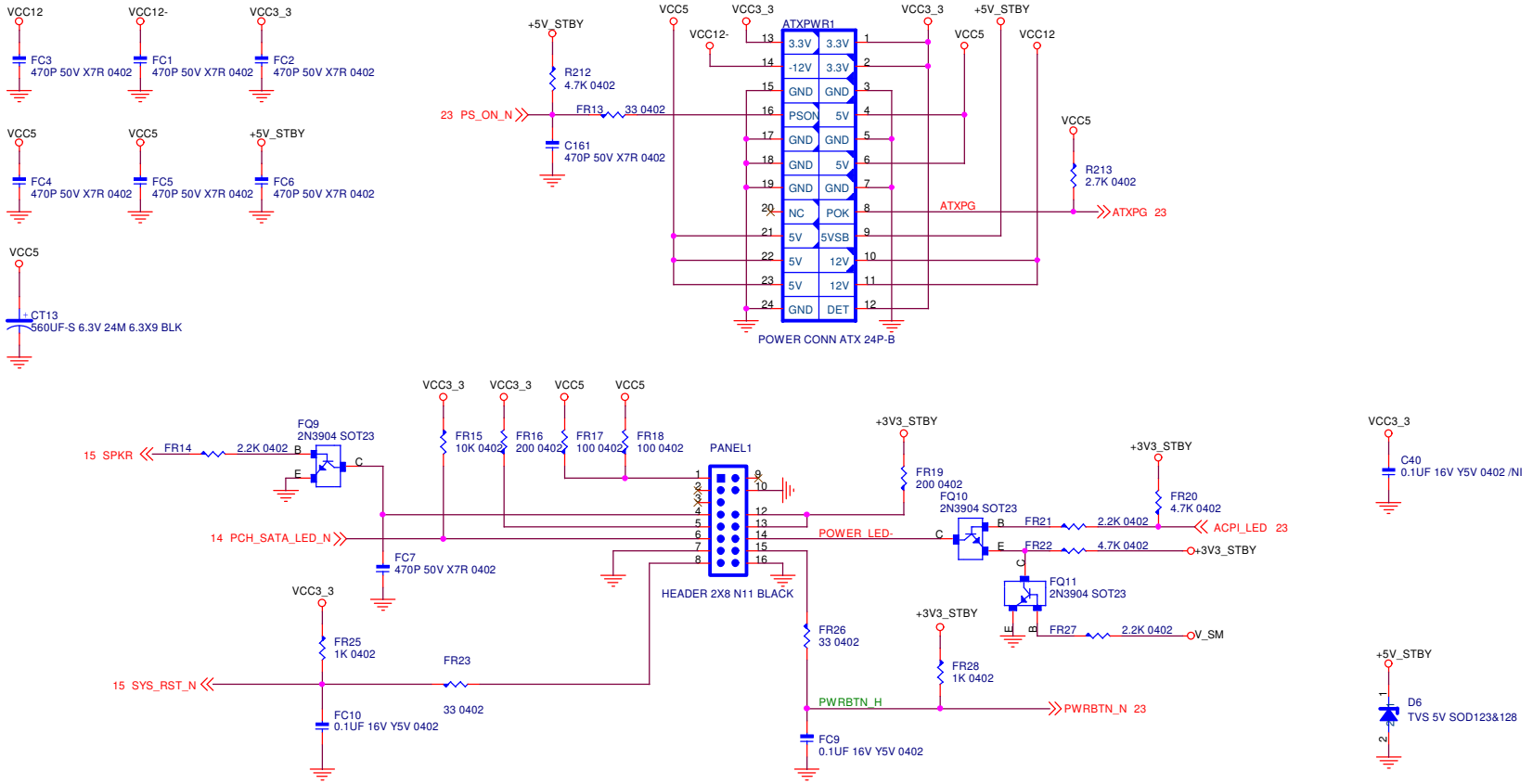
FP PART: F+Reference



映泰股份有限公司
BIOSTAR GROUP

Title: 24PIN CONN & FP

Size	Document Number	Rev
Custom	IH11V-MHS	7.0

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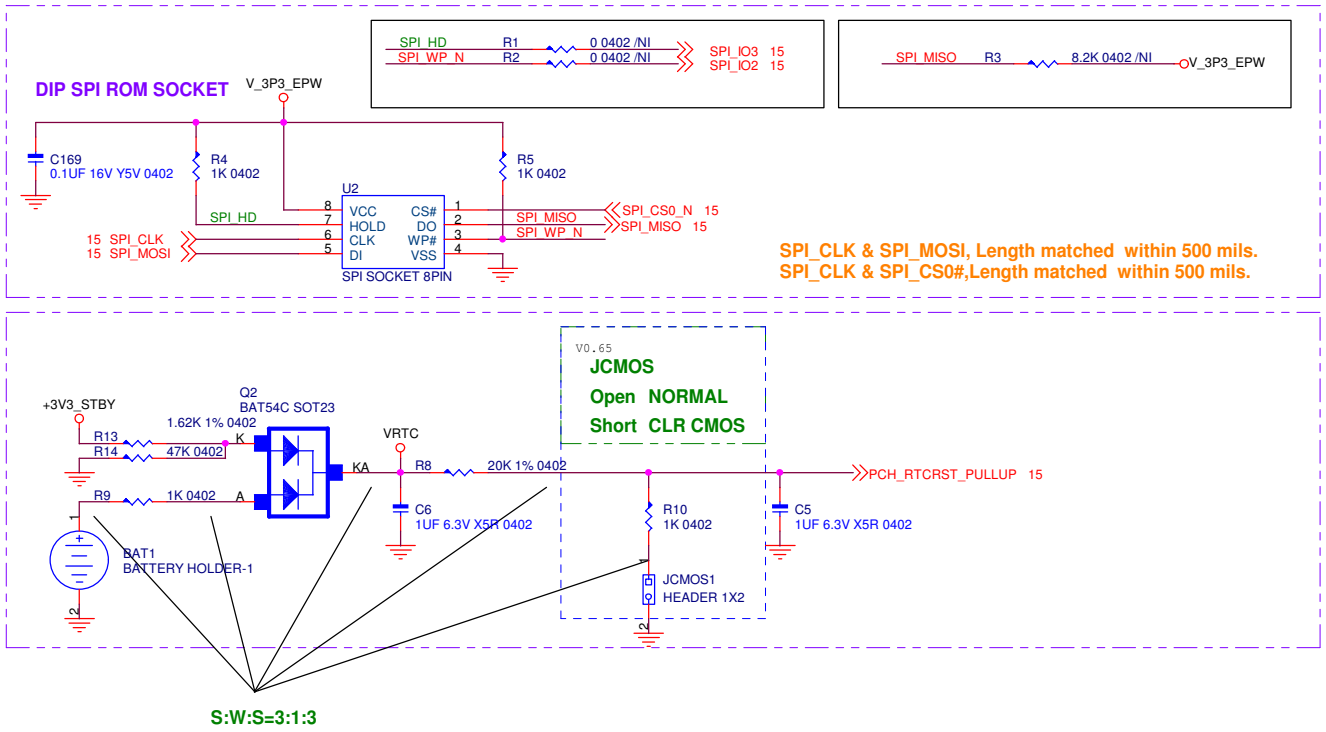

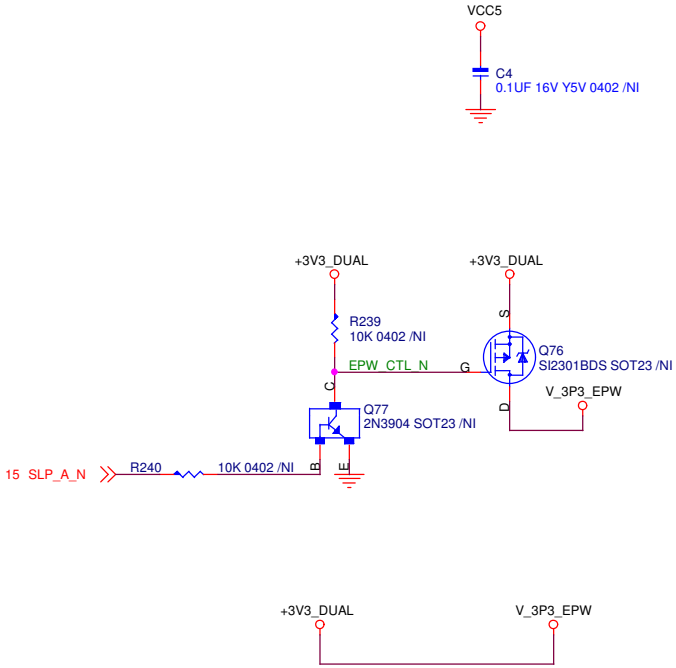

映泰股份有限公司
BIOSTAR GROUP

Title	SPI ROM/RTC CRYSTAL/BAT	
Size B	Document Number IH11V-MHS	Rev 7.0
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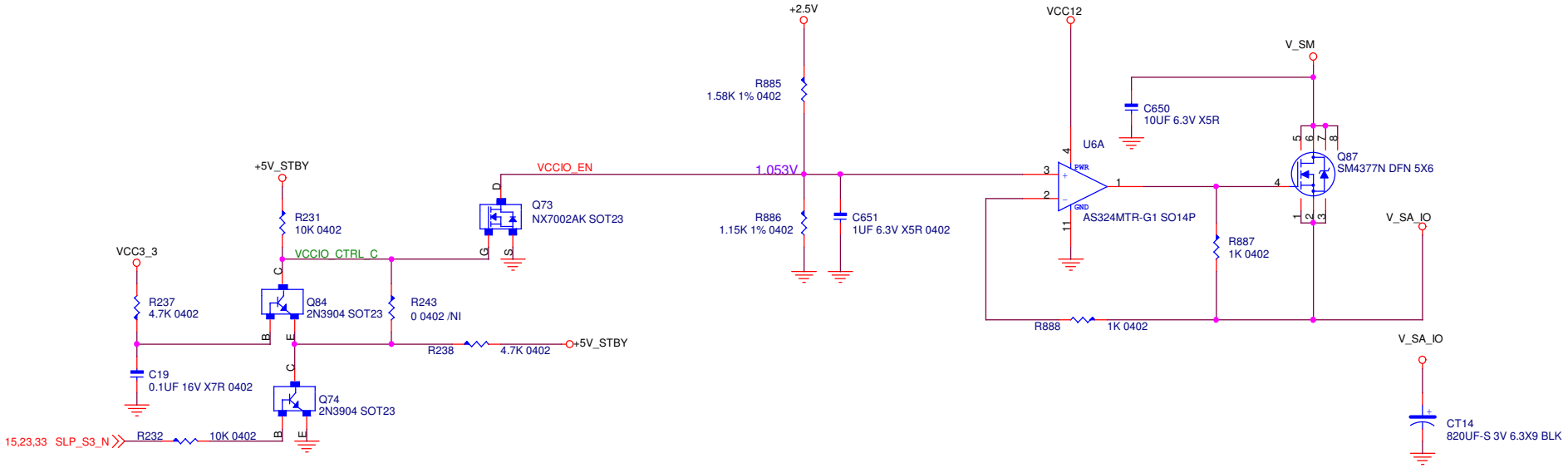

映泰股份有限公司
BIOSTAR GROUP

Title: VCCIO/VCCSA DC-DC

Size: B | Document Number: IH11V-MHS | Rev: 7.0

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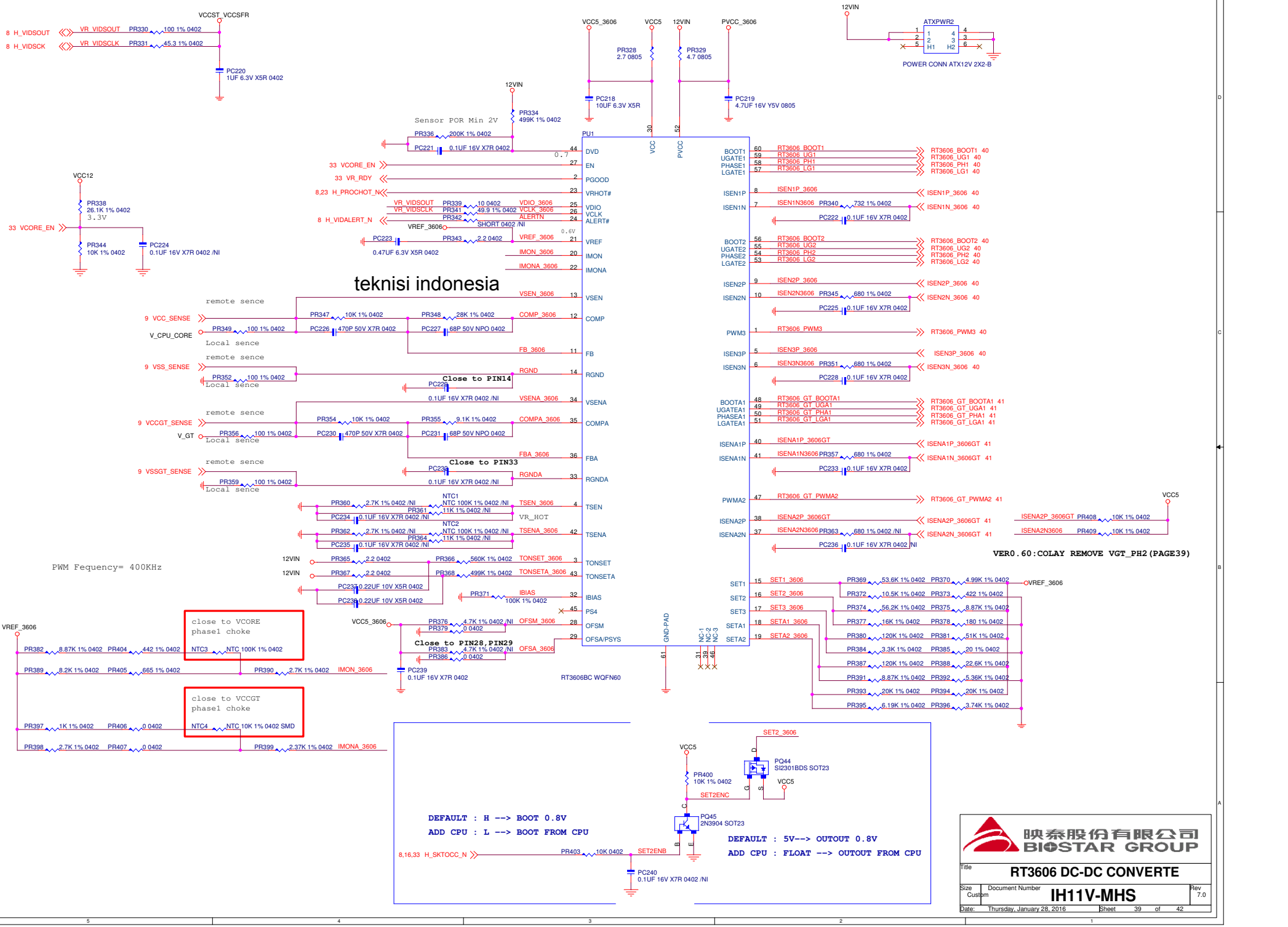
teknisi indonesia
RT3606BC WQFN60
PU1
PWM Fequency= 400KHz
VER0.60:COLAY REMOVE VGT_PH2(PAGE39)
DEFAULT : H --> BOOT 0.8V
ADD CPU : L --> BOOT FROM CPU
DEFAULT : 5V--> OUTOUT 0.8V
ADD CPU : FLOAT --> OUTOUT FROM CPU
close to VCORE phase1 choke
close to VCCGT phase1 choke
Close to PIN14
Close to PIN33
Close to PIN28,PIN29
Sensor POR Min 2V
remote sence
Local sence
POWER CONN ATX12V 2X2-B
映泰股份有限公司
BIOSTAR GROUP
RT3606 DC-DC CONVERTE
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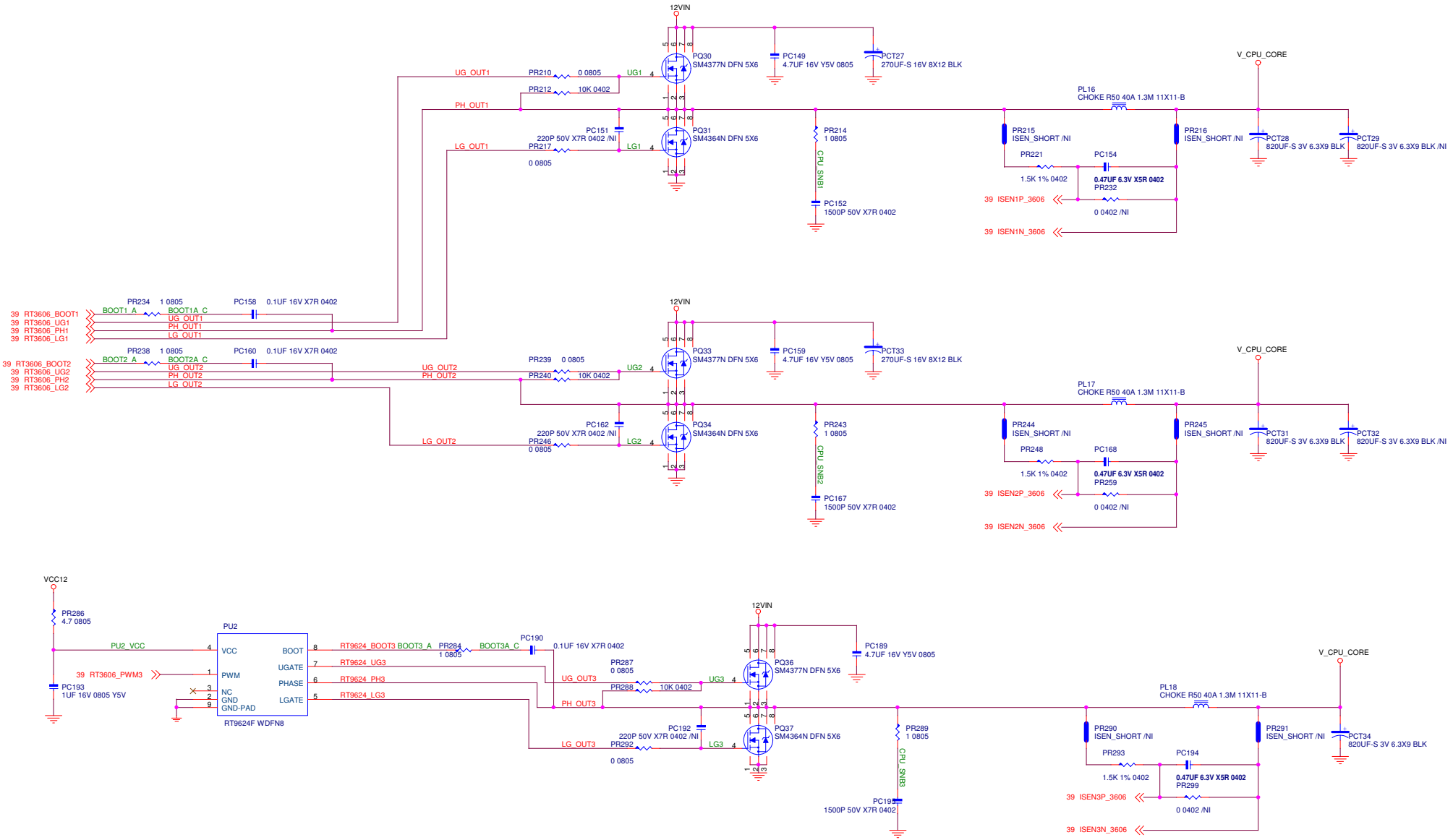

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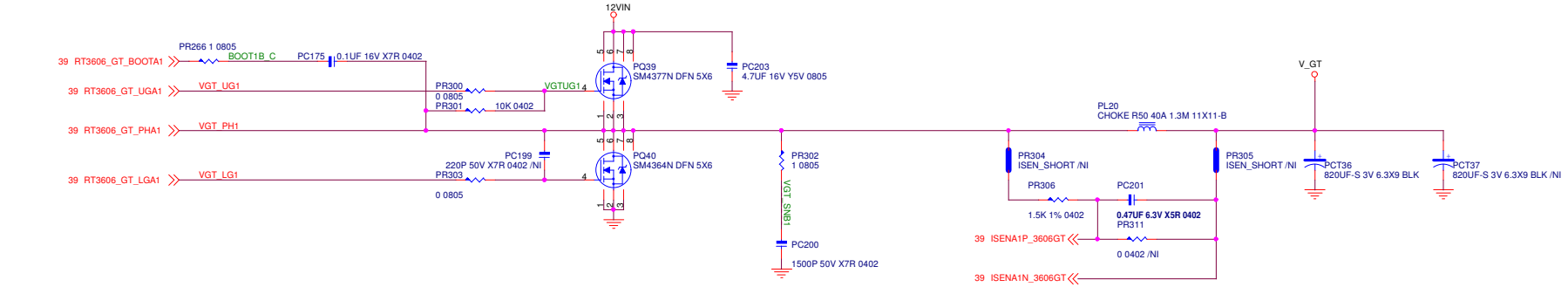
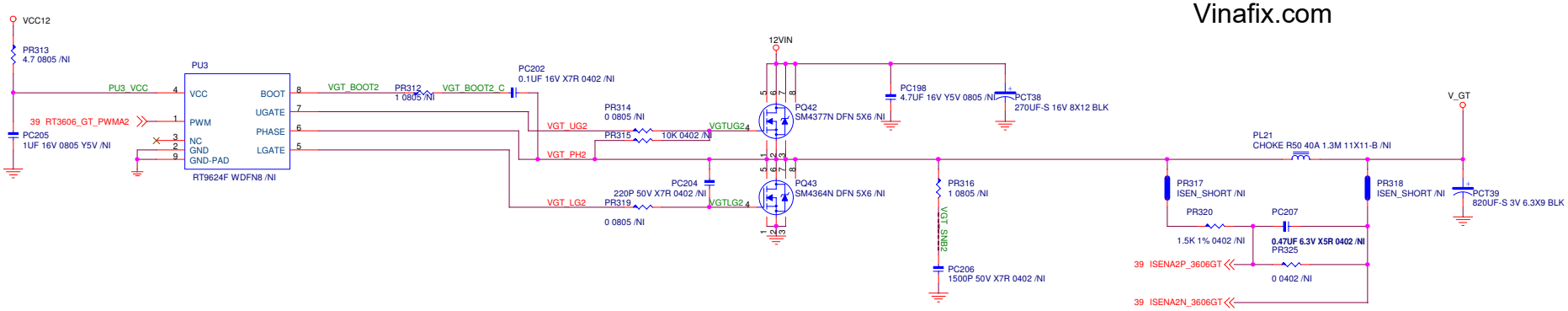
Skylake S-line 42 95W RT3606_VGT





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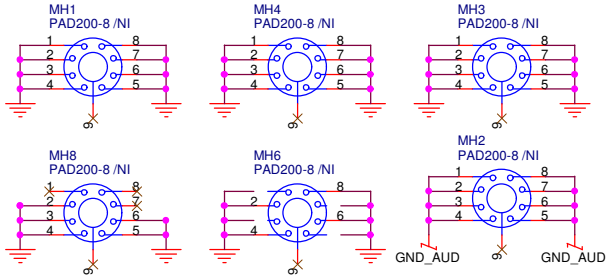

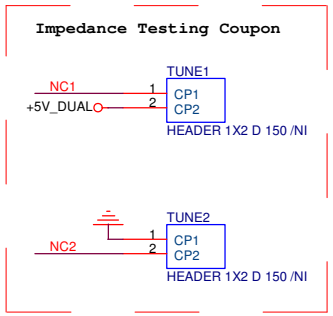

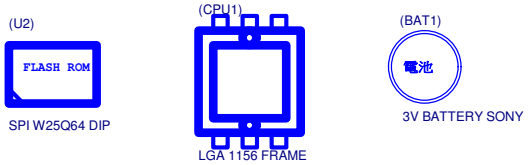

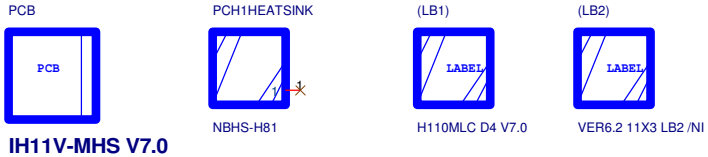

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