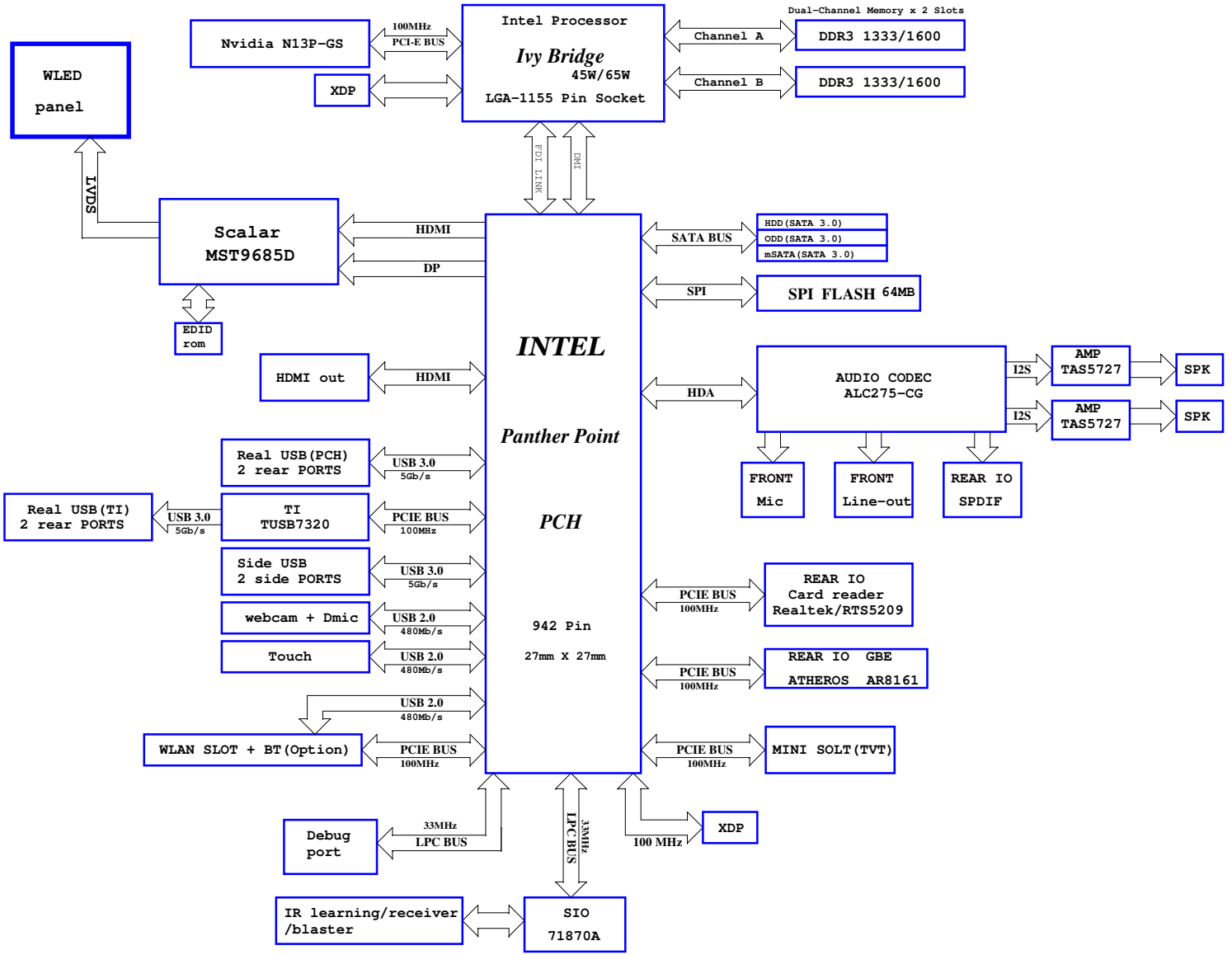
Princeville



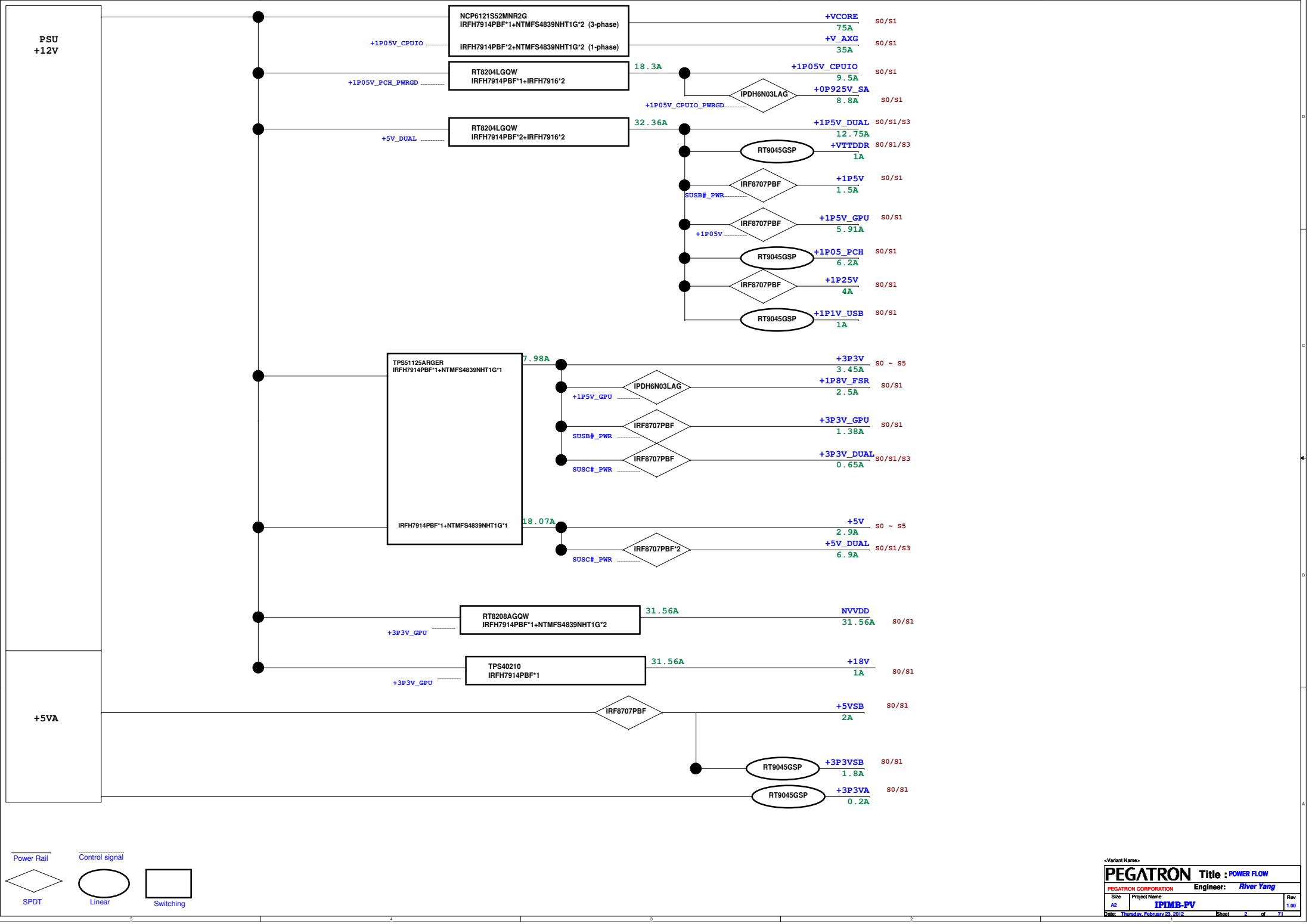
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 1 of 71



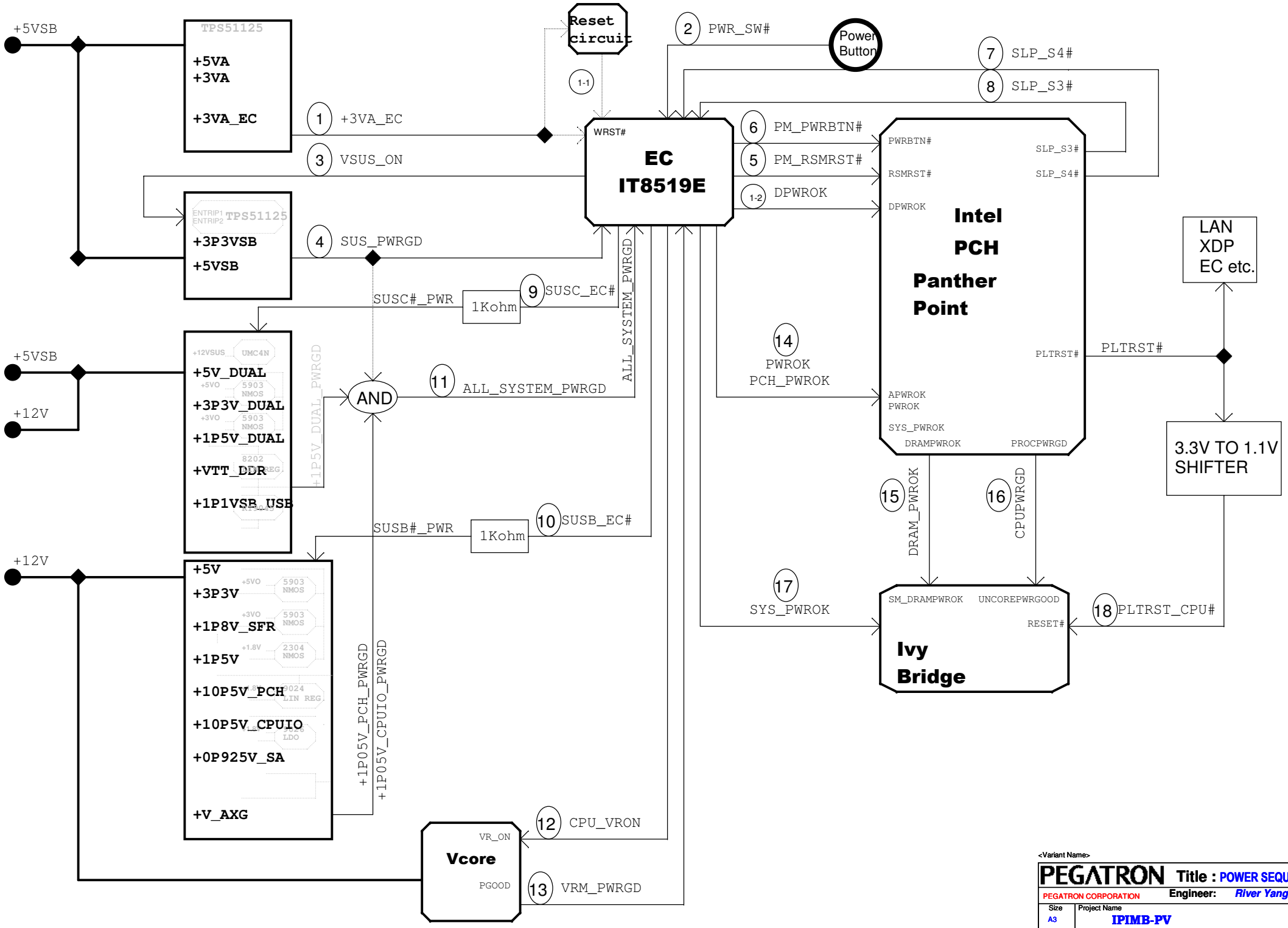
<Variant Name>

PEGATRON Title : POWER FLOW

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 2 of 71



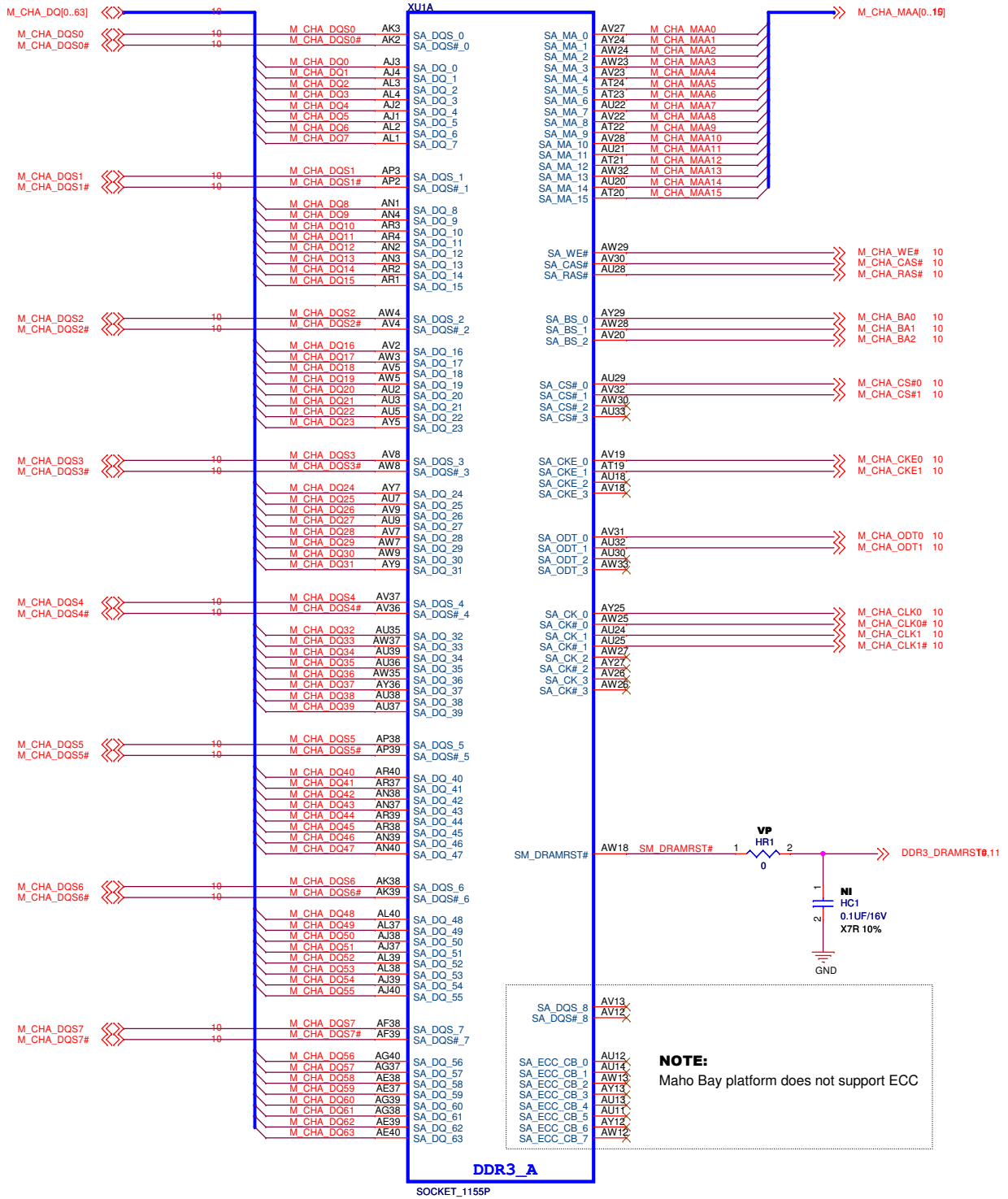
<Variant Name>

PEGATRON Title : POWER SEQUENCE

PEGATRON CORPORATION Engineer: River Yang

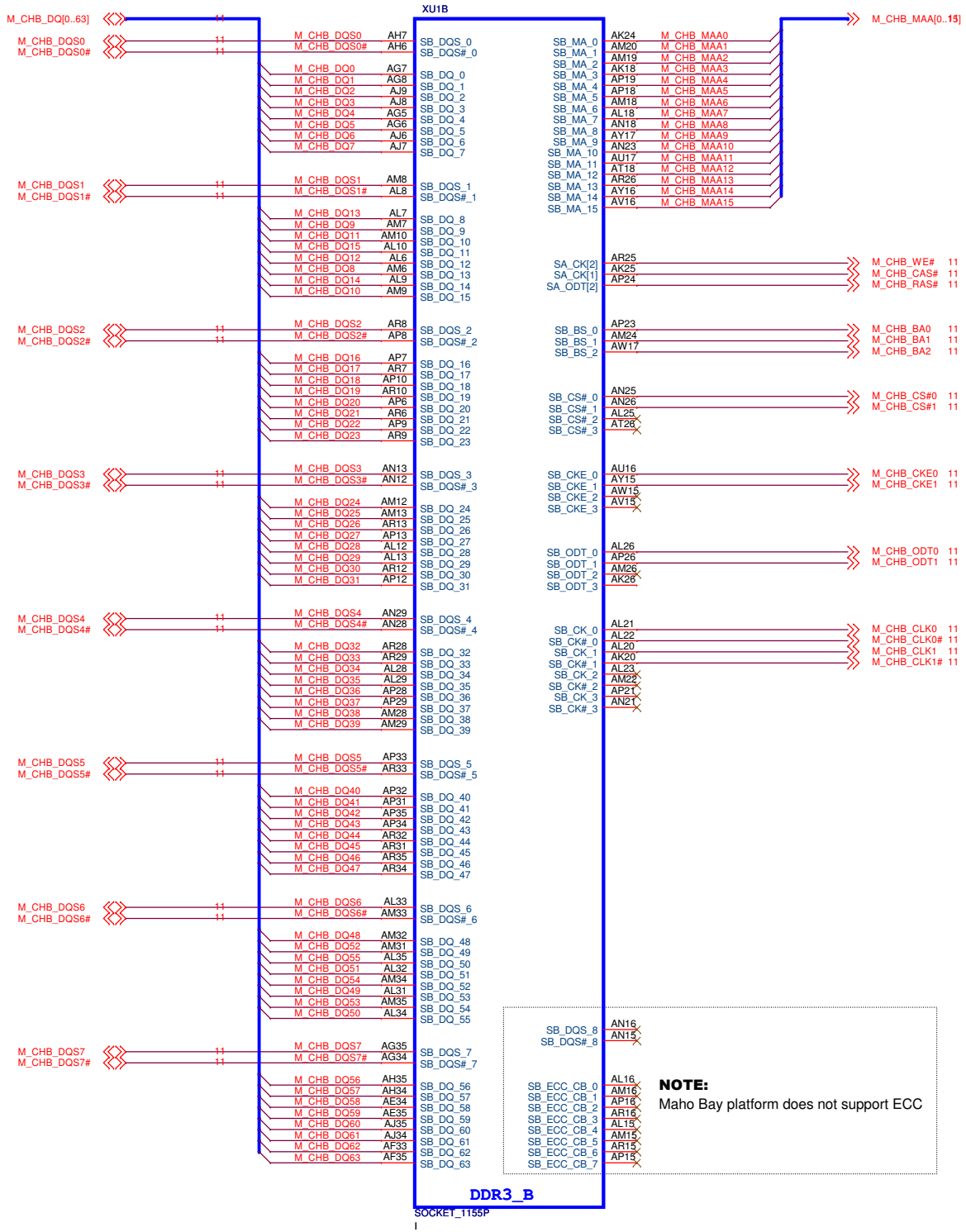
Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 3 of 71



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	DDR3_A 1-6
PEGATRON CORPORATION	Engineer:	River Yang
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 4 of 71	



PEGATRON DT-MB RESTRICTED SECRET

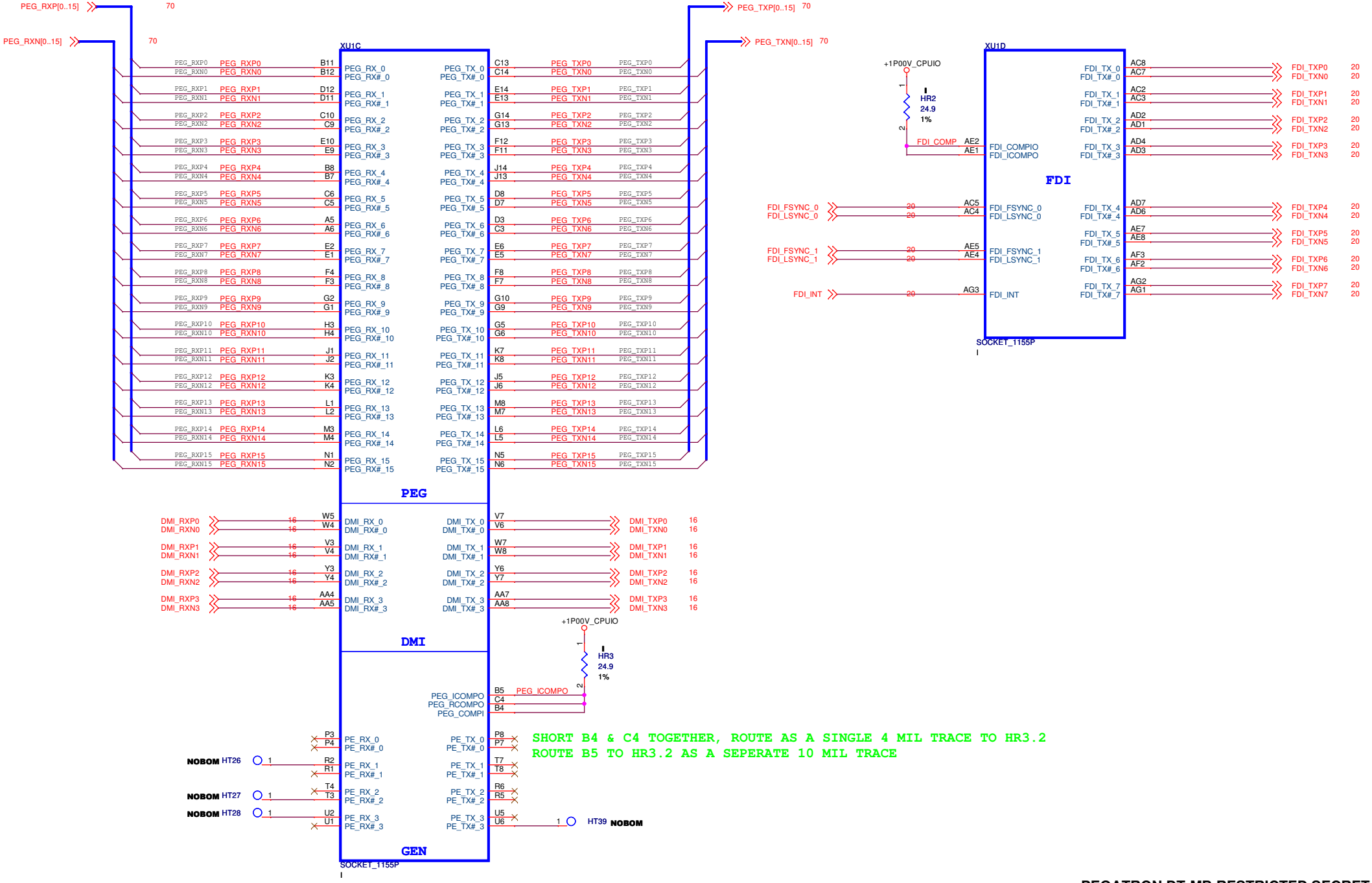
PEGATRON CORPORATION

Title : DDR3_B 2-6

Engineer: River Yang

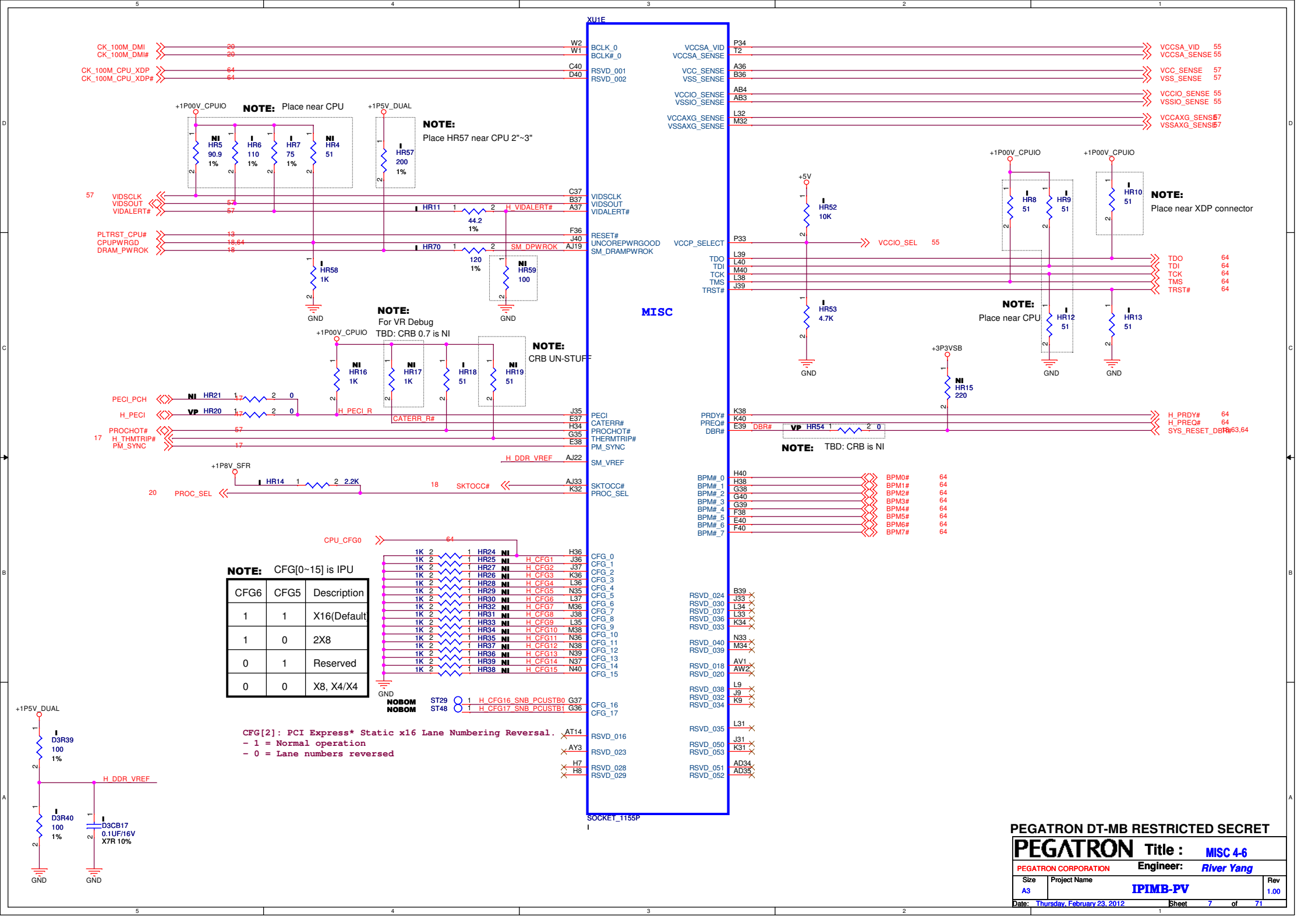
Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 5 of 71

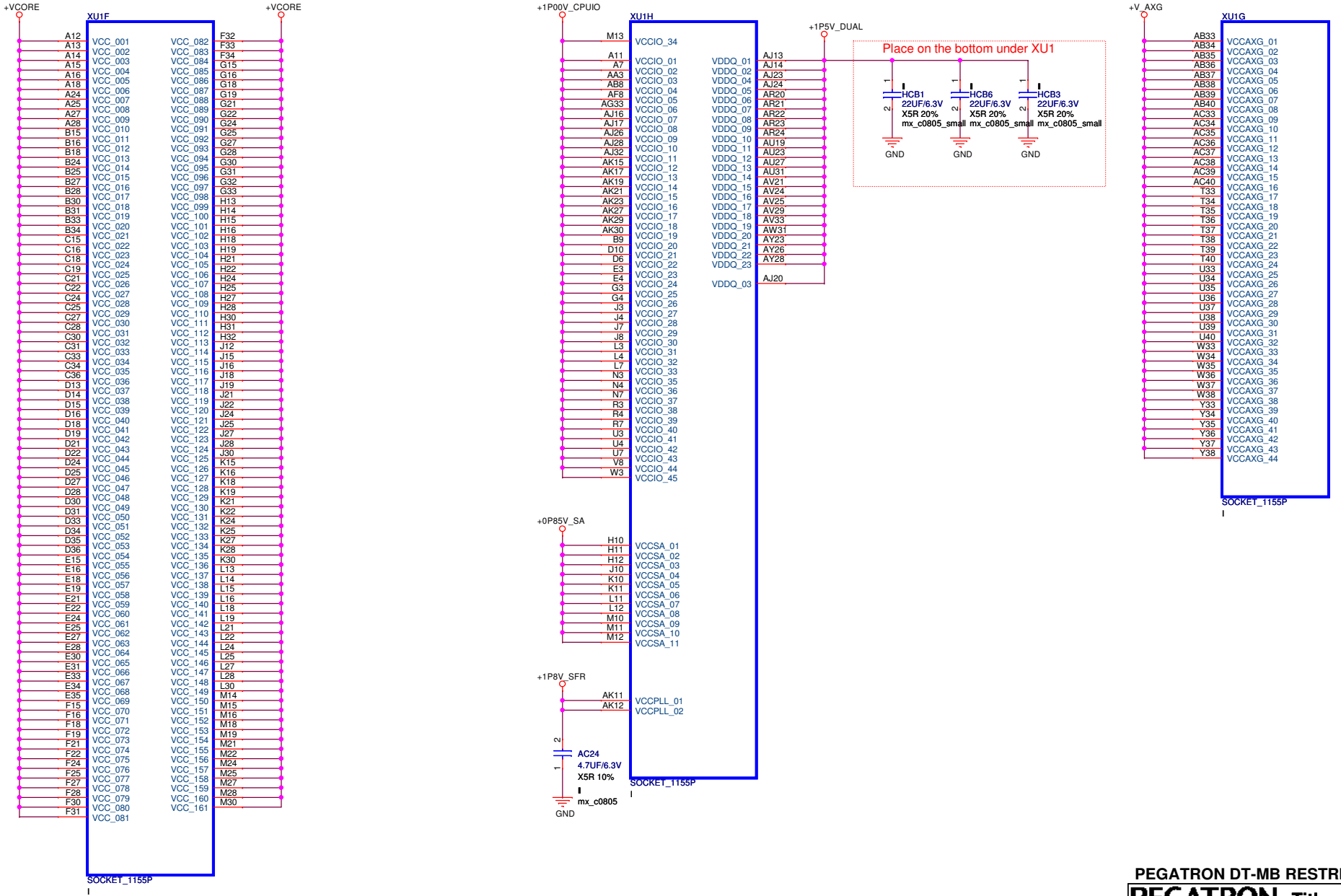


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	PCIE/DMI/FDI 3-6
PEGATRON CORPORATION	Engineer:	River Yang
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 6 of 71	



CFG6	CFG5	Description
1	1	X16(Default
1	0	2X8
0	1	Reserved
0	0	X8, X4/X4



PEGATRON DT-MB RESTRICTED SECRET

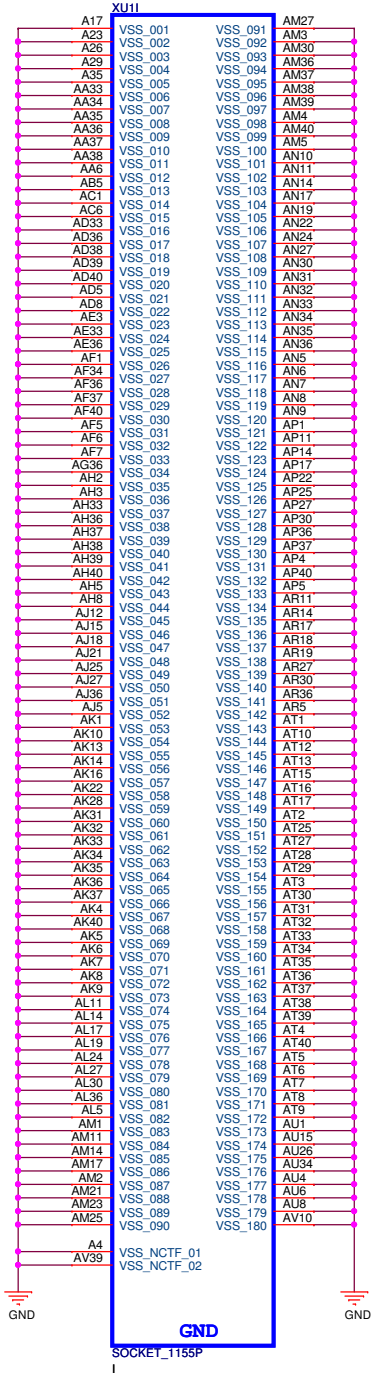
PEGATRON CORPORATION

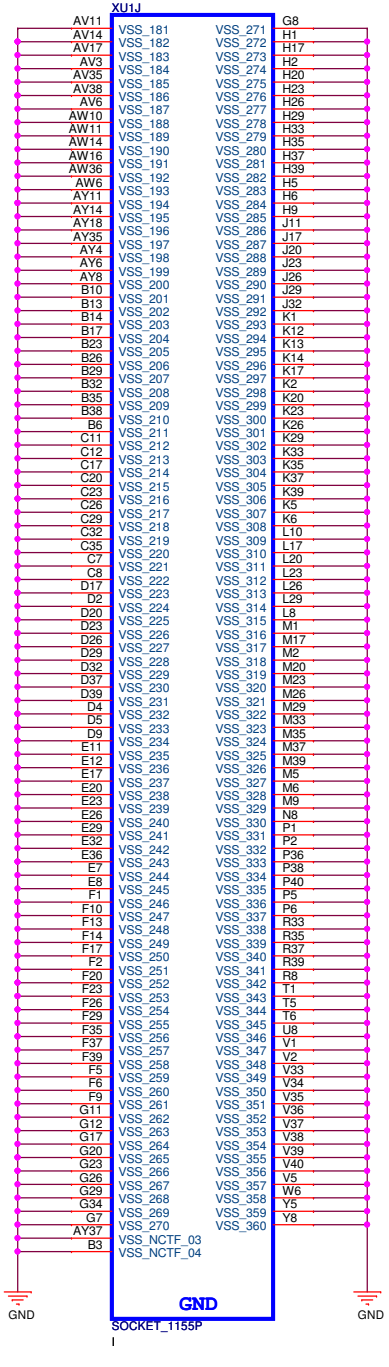
Title : VCC 5 - 6

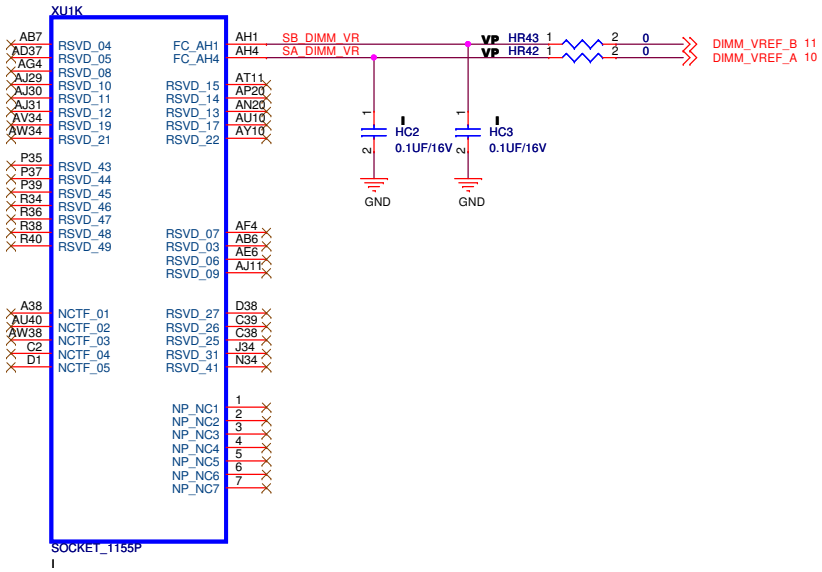
Engineer: River Yang

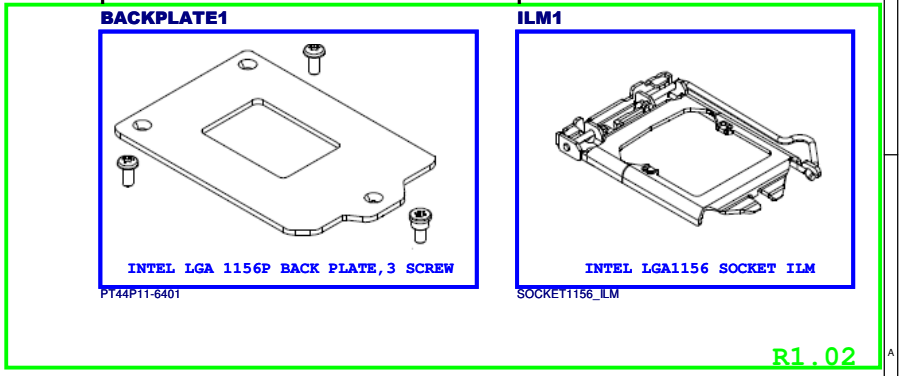
Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 8 of 82









PEGATRON DT-MB RESTRICTED SECRET

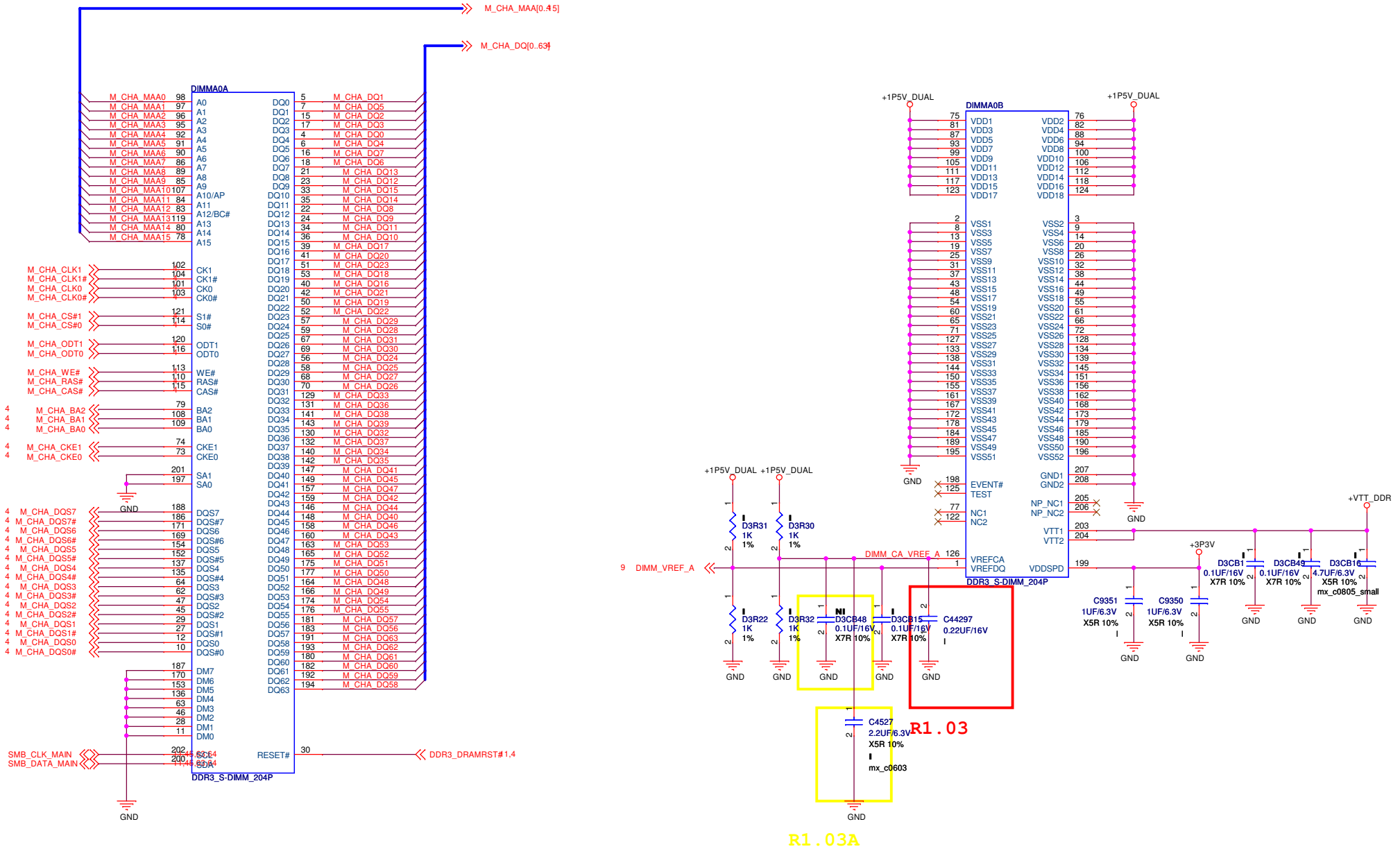
PEGATRON Title : VSS 6 - 6

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

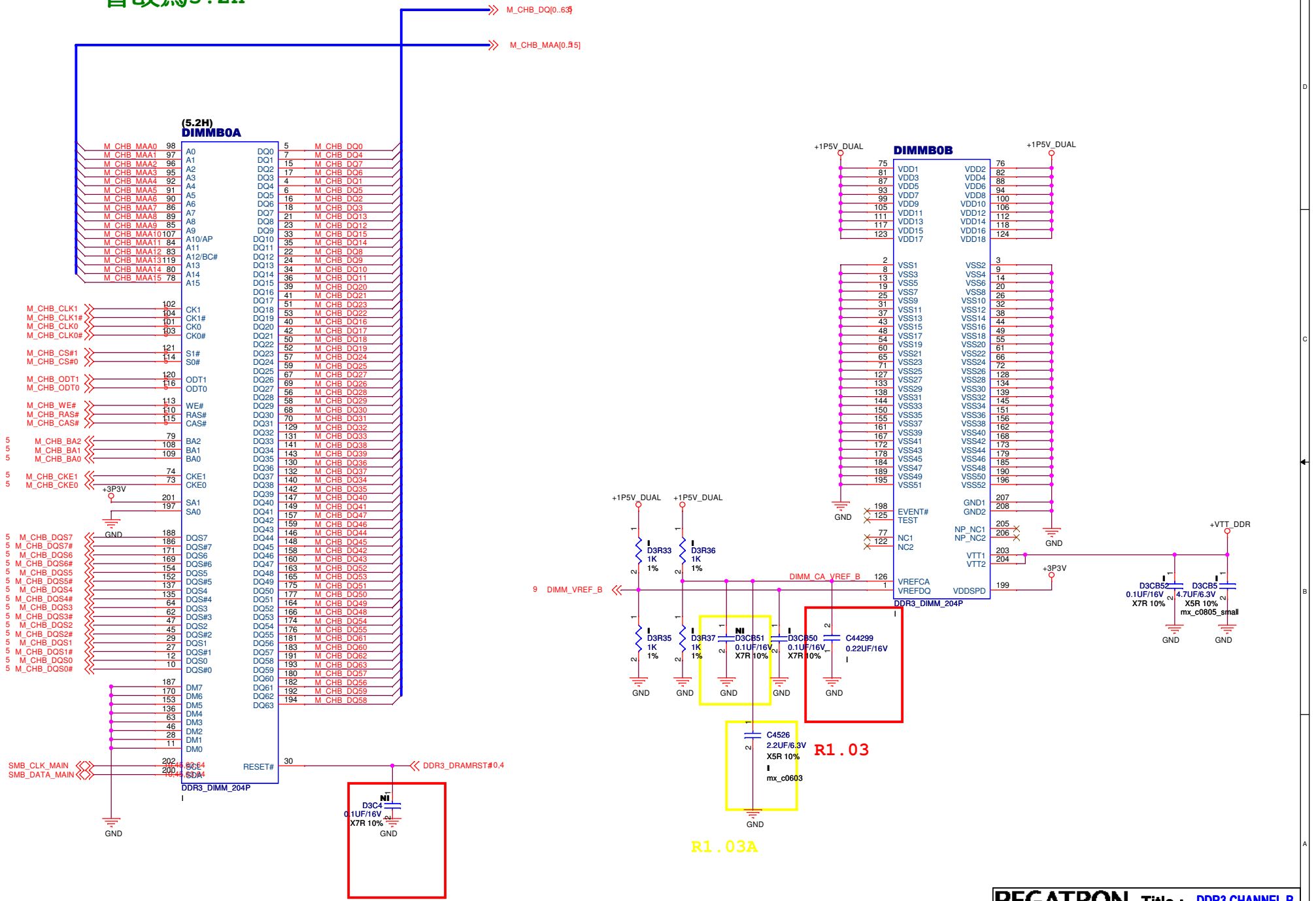
Date: Thursday, February 23, 2012 Sheet 9 of 71

改爲9.2H

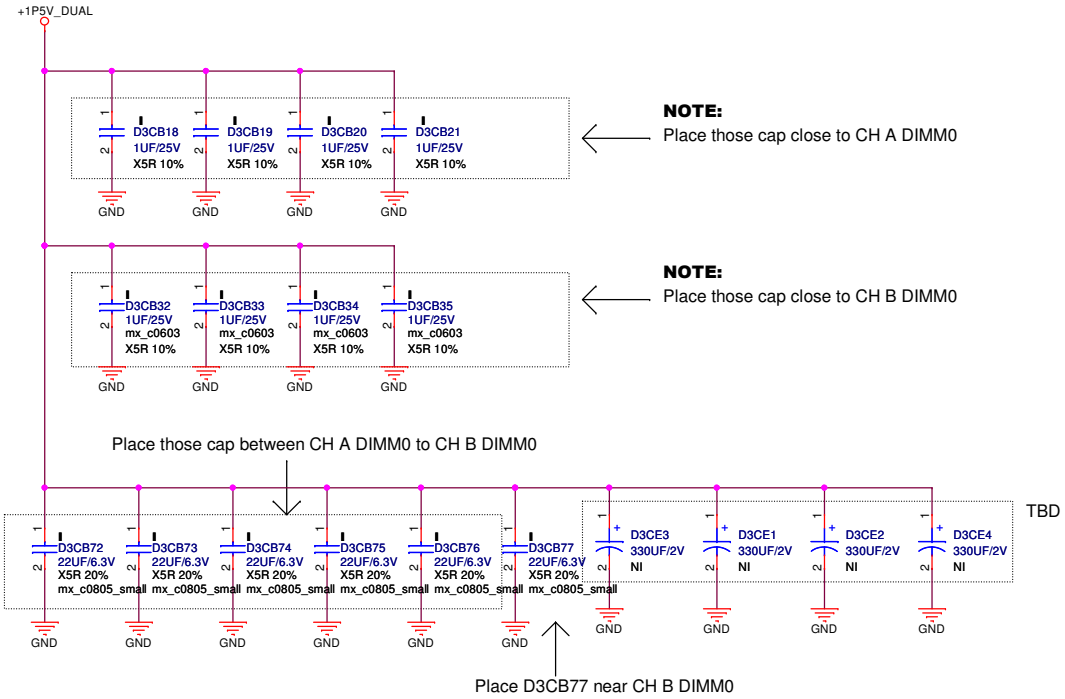


PEGATRON	Title :	DDR3 CHANNEL A	
PEGATRON CORPORATION	Engineer:	River Yang	
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 10 of 71		

皆改爲5.2H

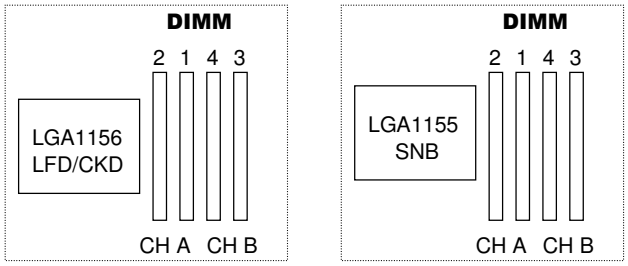


PEGATRON	Title :	DDR3 CHANNEL B	
PEGATRON CORPORATION	Engineer:	River Yang	
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 11 of 71		



NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

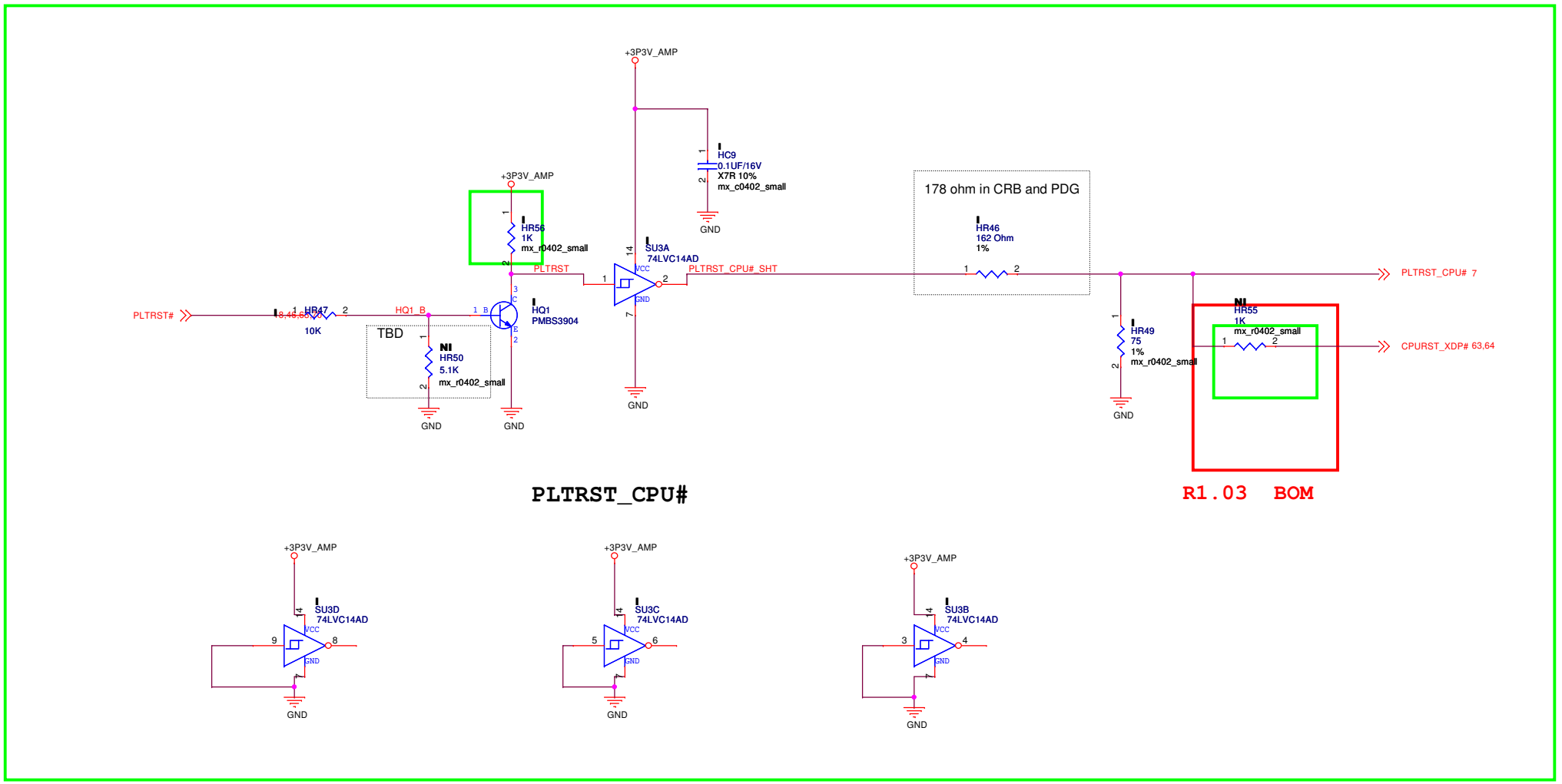
PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 12 of 71

PLTRST_CPU#

R1.02



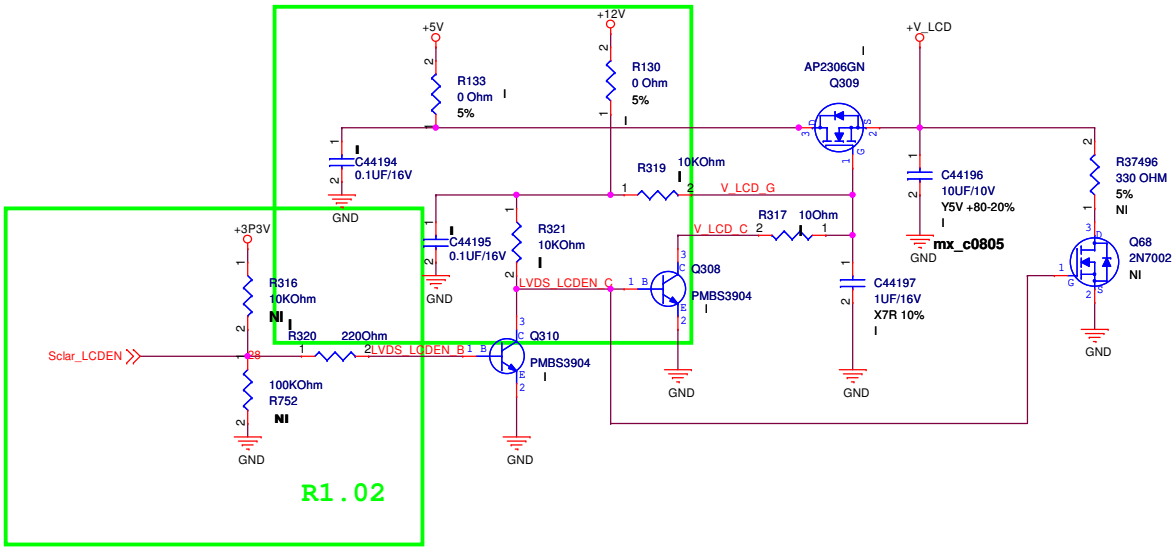
PEGATRON DT-MB RESTRICTED SECRET

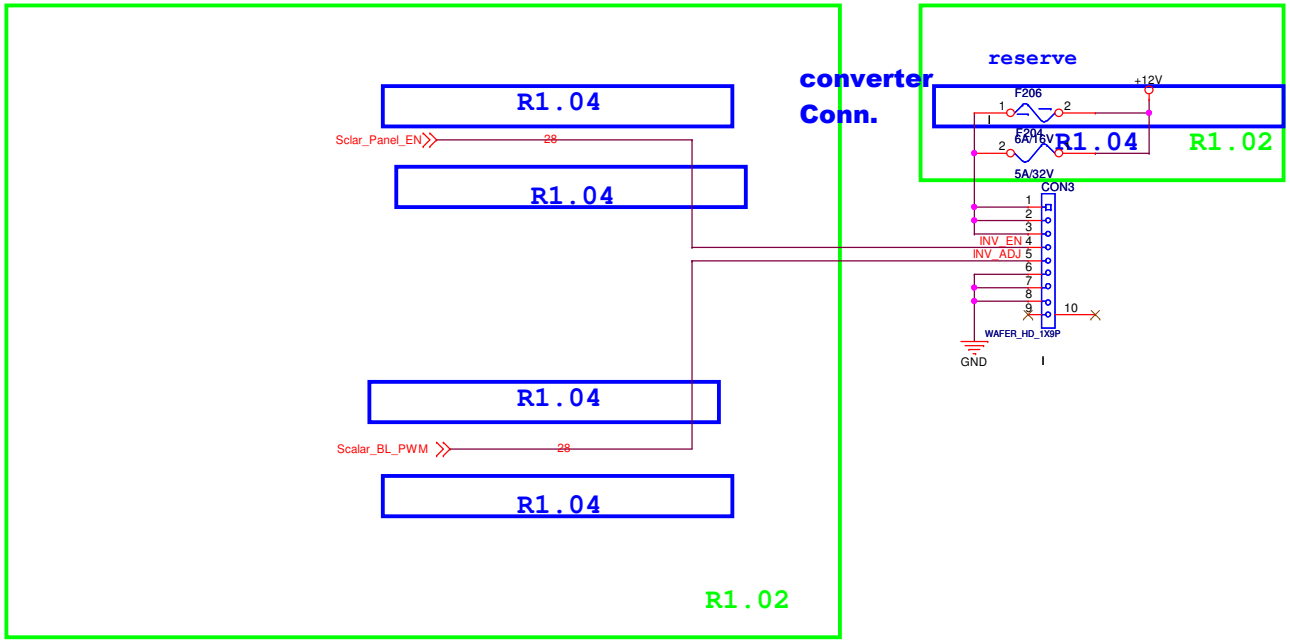
PEGATRON Title : PLTRST_CPU#&SMbus

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 13 of 71





PEGATRON Title : Converter Controllor

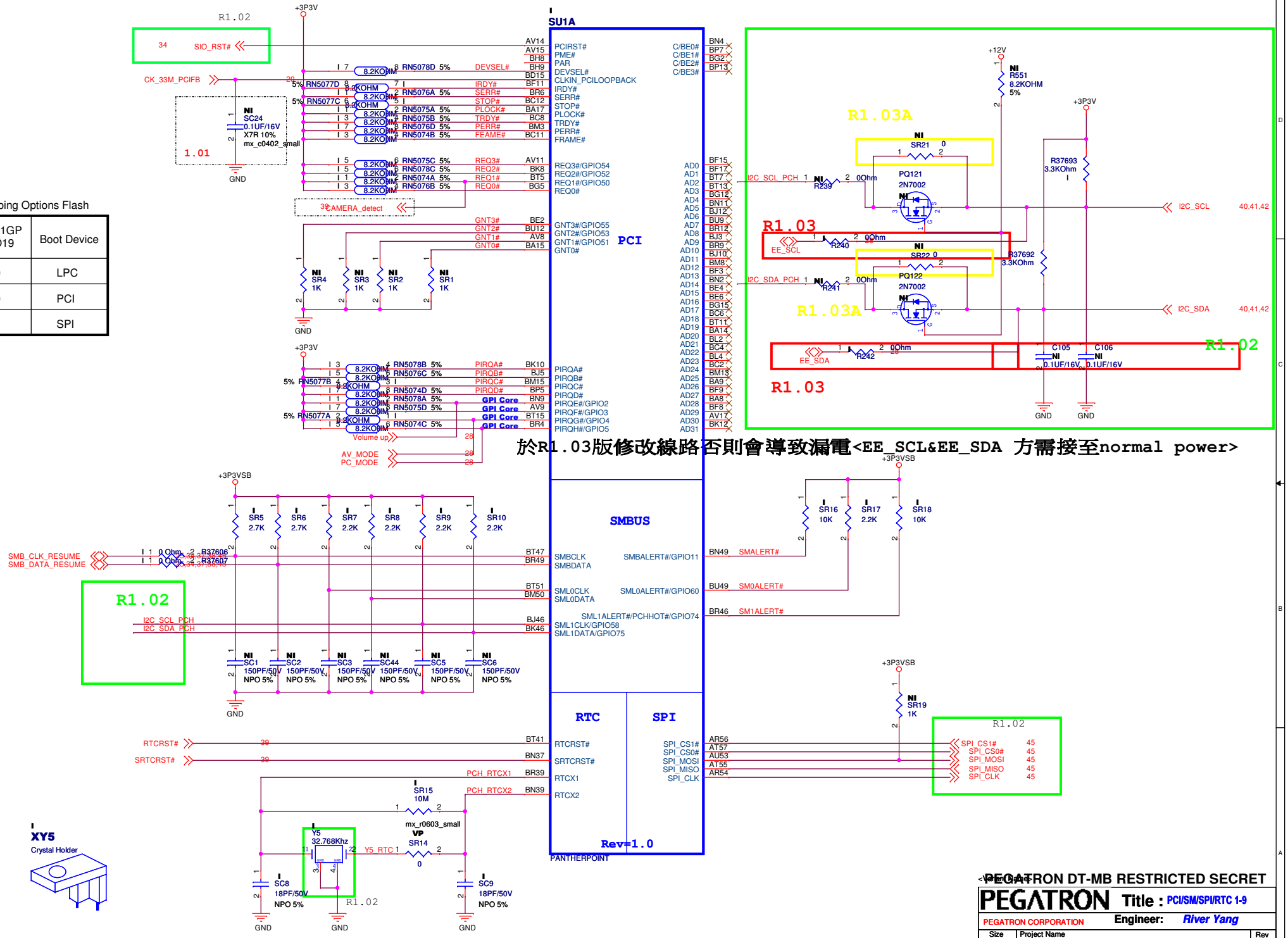
Pegatron Corp. Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 14 of 71

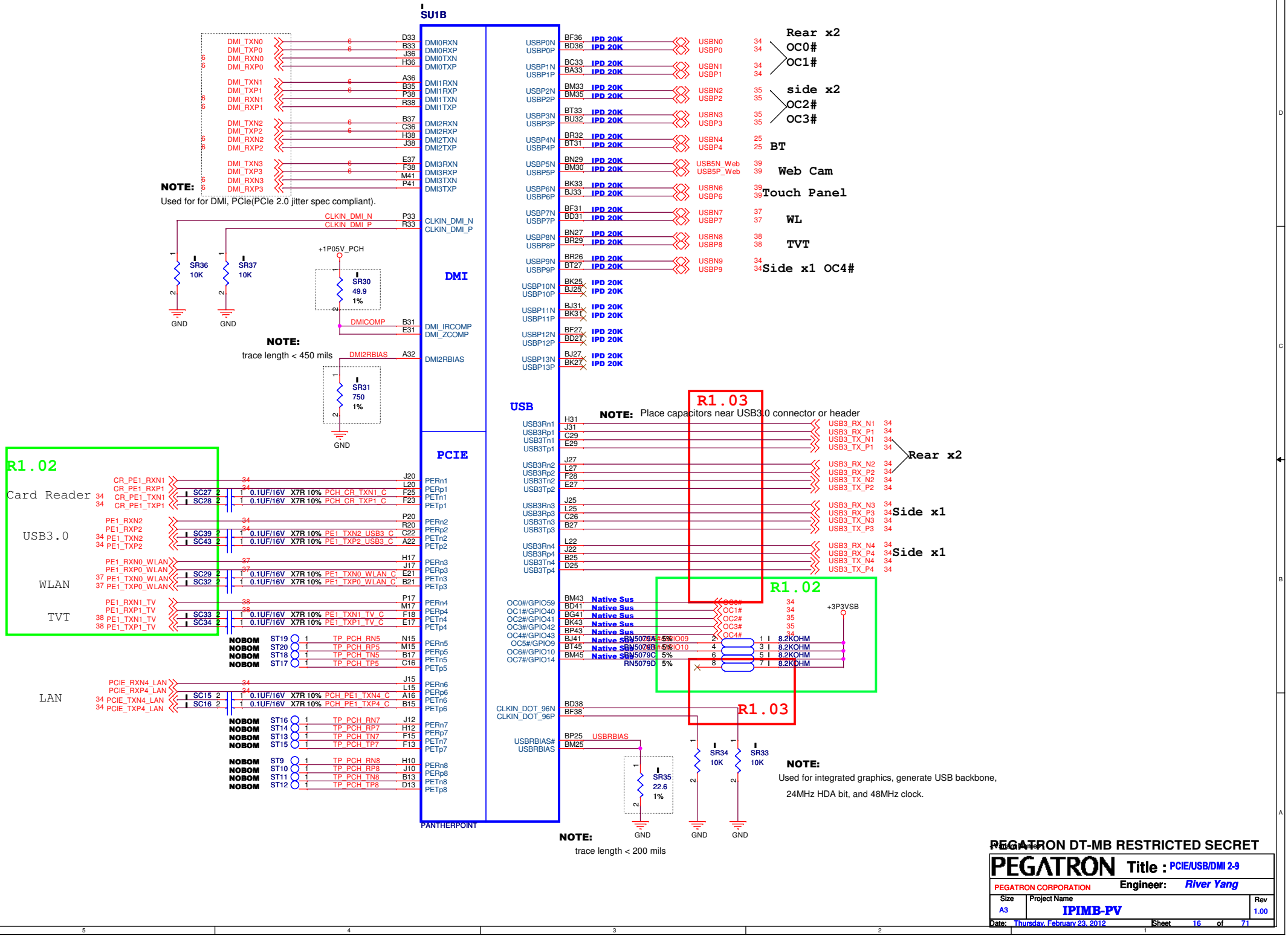
NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI



於R1.03版修改線路否則會導致漏電<EE_SCL&EE_SDA 方需接至normal power>

PEGATRON	Title : PCI/SM/SPI/RTC 1-9		
PEGATRON CORPORATION	Engineer: River Yang		
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 15 of 82		


SU1B
DMI
PCIE
USB
PANTHERPOINT
DMI_TXN0
DMI_TXP0
DMI_RXN0
DMI_RXP0
DMI_TXN1
DMI_TXP1
DMI_RXN1
DMI_RXP1
DMI_TXN2
DMI_TXP2
DMI_RXN2
DMI_RXP2
DMI_TXN3
DMI_TXP3
DMI_RXN3
DMI_RXP3
NOTE:
Used for for DMI, PCIe(PCIe 2.0 jitter spec compliant).
CLKIN_DMI_N
CLKIN_DMI_P
+1P05V_PCH
SR36 10K
SR37 10K
SR30 49.9 1%
GND
DMICOMP
DMI_IRCOMP
DMI_ZCOMP
NOTE:
trace length < 450 mils
DMI2RBIAS
SR31 750 1%
R1.02
Card Reader
USB3.0
WLAN
TVT
LAN
CR_PE1_RXN1
CR_PE1_RXP1
CR_PE1_TXN1
CR_PE1_TXP1
SC27 0.1UF/16V X7R 10% PCH_CR_TXN1_C
SC28 0.1UF/16V X7R 10% PCH_CR_TXP1_C
PE1_RXN2
PE1_RXP2
PE1_TXN2
PE1_TXP2
SC39 0.1UF/16V X7R 10% PE1_TXN2_USB3_C
SC43 0.1UF/16V X7R 10% PE1_TXP2_USB3_C
PE1_RXN0_WLAN
PE1_RXP0_WLAN
PE1_TXN0_WLAN
PE1_TXP0_WLAN
SC29 0.1UF/16V X7R 10% PE1_TXN0_WLAN_C
SC32 0.1UF/16V X7R 10% PE1_TXP0_WLAN_C
PE1_RXN1_TV
PE1_RXP1_TV
PE1_TXN1_TV
PE1_TXP1_TV
SC33 0.1UF/16V X7R 10% PE1_TXN1_TV_C
SC34 0.1UF/16V X7R 10% PE1_TXP1_TV_C
NOBOM ST19 TP_PCH_RN5
NOBOM ST20 TP_PCH_RP5
NOBOM ST18 TP_PCH_TN5
NOBOM ST17 TP_PCH_TP5
PCIE_RXN4_LAN
PCIE_RXP4_LAN
PCIE_TXN4_LAN
PCIE_TXP4_LAN
SC15 0.1UF/16V X7R 10% PCH_PE1_TXN4_C
SC16 0.1UF/16V X7R 10% PCH_PE1_TXP4_C
NOBOM ST16 TP_PCH_RN7
NOBOM ST14 TP_PCH_RP7
NOBOM ST13 TP_PCH_TN7
NOBOM ST15 TP_PCH_TP7
NOBOM ST9 TP_PCH_RN8
NOBOM ST10 TP_PCH_RP8
NOBOM ST11 TP_PCH_TN8
NOBOM ST12 TP_PCH_TP8
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
IPD 20K
USBN0
USBP0
USBN1
USBP1
USBN2
USBP2
USBN3
USBP3
USBN4
USBP4
USB5N_Web
USB5P_Web
USBN6
USBP6
USBN7
USBP7
USBN8
USBP8
USBN9
USBP9
Rear x2
OC0#
OC1#
side x2
OC2#
OC3#
BT
Web Cam
Touch Panel
WL
TVT
Side x1 OC4#
R1.03
NOTE: Place capacitors near USB3.0 connector or header
USB3Rn1
USB3Rp1
USB3Tn1
USB3Tp1
USB3Rn2
USB3Rp2
USB3Tn2
USB3Tp2
USB3Rn3
USB3Rp3
USB3Tn3
USB3Tp3
USB3Rn4
USB3Rp4
USB3Tn4
USB3Tp4
USB3_RX_N1
USB3_RX_P1
USB3_TX_N1
USB3_TX_P1
USB3_RX_N2
USB3_RX_P2
USB3_TX_N2
USB3_TX_P2
USB3_RX_N3
USB3_RX_P3
USB3_TX_N3
USB3_TX_P3
USB3_RX_N4
USB3_RX_P4
USB3_TX_N4
USB3_TX_P4
Rear x2
Side x1
Side x1
R1.02
+3P3VSB
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO9
OC6#/GPIO10
OC7#/GPIO14
Native Sus
RN5079A 5% 8.2KOHM
RN5079B 5% 8.2KOHM
RN5079C 5% 8.2KOHM
RN5079D 5% 8.2KOHM
CLKIN_DOT_96N
CLKIN_DOT_96P
R1.03
USBRBIAS#
USBRBIAS
SR35 22.6 1%
SR34 10K
SR33 10K
NOTE:
Used for integrated graphics, generate USB backbone,
24MHz HDA bit, and 48MHz clock.
NOTE:
trace length < 200 mils
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCIE/USB/DMI 2-9
PEGATRON CORPORATION
Engineer: River Yang
Size A3
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
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NOTE:

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

SU1C

PANTHERPOINT

CLINK
FAN
GPIO
HOST

IPU 32/ IPD 100
IPU 32/ IPD 100
CL_CLK1
CL_DATA1
CL_RST1#
APWROK
PCH_PWROK
PCH_MEPWROK

PWM0
PWM1
PWM2
PWM3
NOBOM ST28 TP_PCH_PWM0
NOBOM ST25 TP_PCH_PWM1
NOBOM ST26 TP_PCH_PWM2
NOBOM ST27 TP_PCH_PWM3

TACH0/GPIO17
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
TACH4/GPIO68
TACH5/GPIO69
TACH6/GPIO70
TACH7/GPIO71
SATA5GP/GPIO49/THERM_ALERT#
SST
GPIO1

SCLOCK/GPIO22
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48

CLKIN_SATA_N
CLKIN_SATA_P
NC_1

SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP

SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
SATA4GP/GPIO16

SATAICOMPI
SATAICOMPO
SATA3COMPI
SATA3RCOMPO
SATALED#
TP16
SATA3RBIAS

A20GATE
INIT3_3V#
RCIN#
SERIRQ
THRMTRIP#
PECI
PMSYNCH

HDD SATA 3.0
mSATA SATA 3.0
ODD

EDS 1.0 SATA2GP/SATA3GP should not be pulled high when strap is sampled.

NOTE: trace length < 450 mils

NOTE: trace length < 200 mils

NOTE: trace length < 450 mils

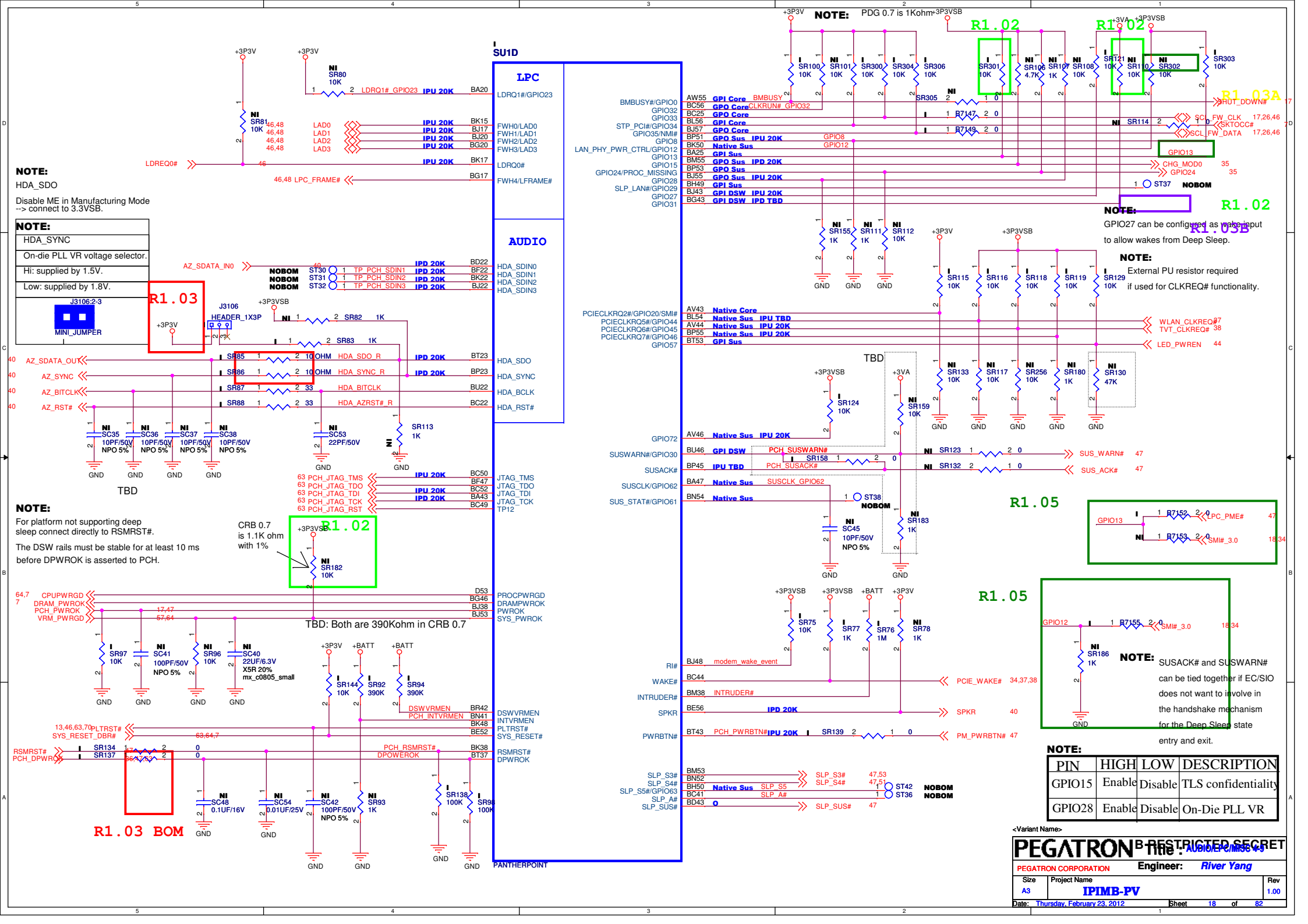
R1.02
R1.05
R1.03C
R1.03A
1.01

ODD eject
Volume down
TOUCH_Det
D8868 TVL040201AB0 NI
C34 0.1UF/16V X7R 10% NI
SC30 100PF/50V NPO 5% NI
SC31 220PF/50V X7R 10% NI

SCL_FW_DATA
SCL_FW_CLK
BRD_ID1
CHASSIS_ID1
CLPWD#
HD_LED#
SHUT_DOWN#
H_THMTRIP#
GPU_TRIP#

SR309 2.2KOHM 1% NI
SR310 2.2KOHM 1% I
HR40 340 OHM
HR22 340 OHM
SR70 750 1% mx_r0402_small
SR74 1K mx_r0402_small
HC8 680PF/50V X7R 10% mx_c0402_small
O2C23 0.1UF/16V mx_c0402_small
SR66 37.4 1%
SR67 49.9 1%
Q9360 PMBS3904
Q9361 PMBS3904

PEGATRON Title : SATA/HOST/FAN 3-9
PEGATRON CORPORATION Engineer: River Yang
Size A3 | Project Name IPIMB-PV | Rev 1.00
Date: Thursday, February 23, 2012 | Sheet 17 of 71


SU1D
LPC
AUDIO
PANTHERPOINT
NOTE:
HDA_SDO
Disable ME in Manufacturing Mode
--> connect to 3.3VSB.
NOTE:
HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.
J3106:2-3
MINI_JUMPER
R1.03
J3106
HEADER_1X3P
TBD
NOTE:
For platform not supporting deep sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.
CRB 0.7 is 1.1K ohm with 1%
R1.02
TBD: Both are 390Kohm in CRB 0.7
R1.03 BOM
NOTE:
PDG 0.7 is 1Kohm
R1.02
R1.03A
R1.03B
NOTE:
GPIO27 can be configured as wake input to allow wakes from Deep Sleep.
NOTE:
External PU resistor required if used for CLKREQ# functionality.
R1.05
NOTE:
SUSACK# and SUSWARN# can be tied together if EC/SIO does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
NOTE:
PIN | HIGH | LOW | DESCRIPTION
GPIO15 | Enable | Disable | TLS confidentiality
GPIO28 | Enable | Disable | On-Die PLL VR
PEGATRON
PEGATRON CORPORATION
Engineer: River Yang
Size A3
Project Name IPIMB-PV
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Date: Thursday, February 23, 2012
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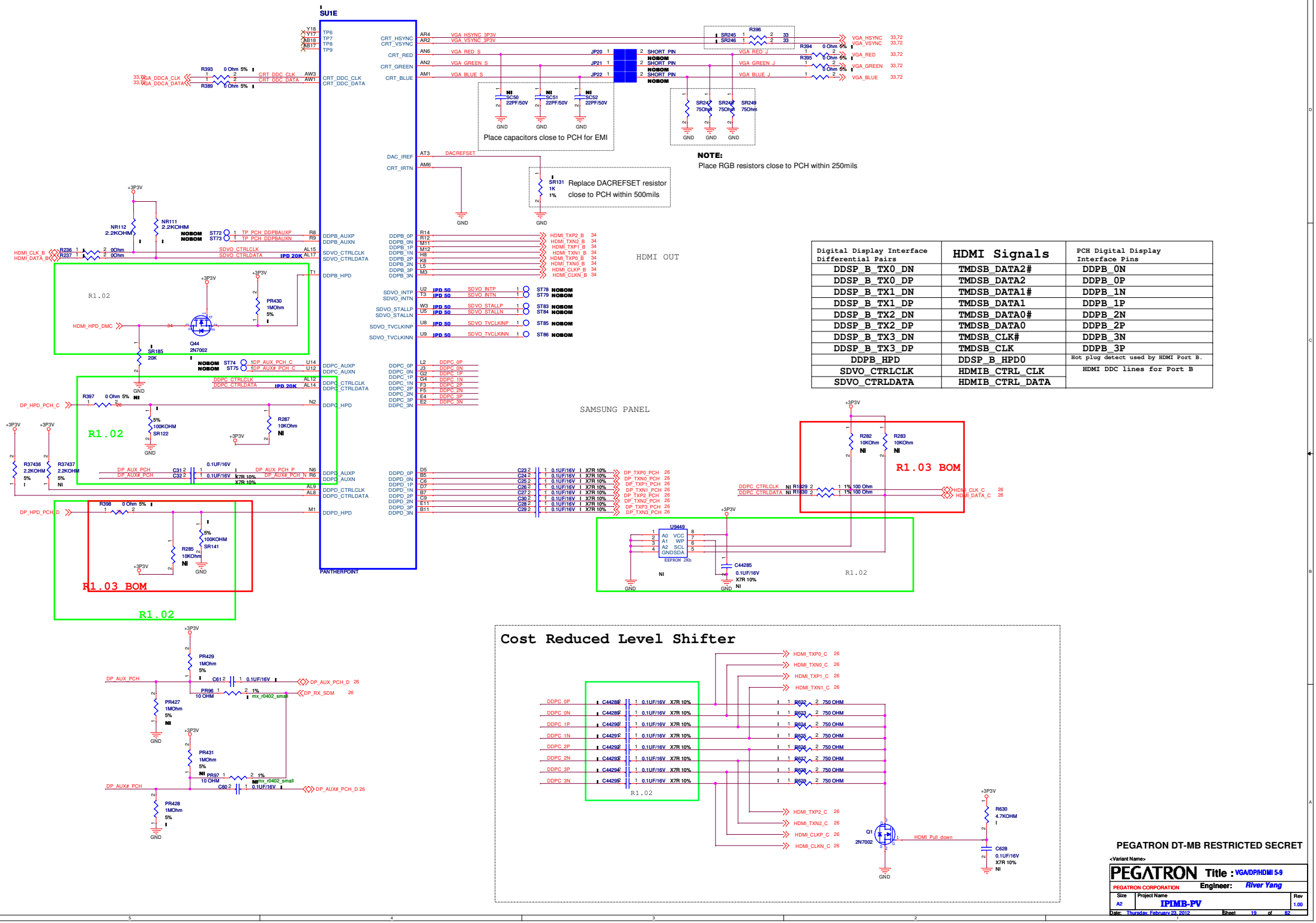

Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIB_CTRL_DATA	

Cost Reduced Level Shifter

PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

PEGATRON Title : VGA/DP/HDMI 5-9

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.00

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SU1F

FDI

FDI_TXN0 FDI_TXP0 FDI_TXN1 FDI_TXP1 FDI_TXN2 FDI_TXP2 FDI_TXN3 FDI_TXP3 FDI_TXN4 FDI_TXP4 FDI_TXN5 FDI_TXP5 FDI_TXN6 FDI_TXP6 FDI_TXN7 FDI_TXP7 (6)

C42 B43 F45 F43 H41 J41 C46 D47 B45 A46 B47 C49 J43 H43 M43 P43

FDI_RXN0 FDI_RXP0 FDI_RXN1 FDI_RXP1 FDI_RXN2 FDI_RXP2 FDI_RXN3 FDI_RXP3 FDI_RXN4 FDI_RXP4 FDI_RXN5 FDI_RXP5 FDI_RXN6 FDI_RXP6 FDI_RXN7 FDI_RXP7

FDI_FSYNC0 B51 → FDI_FSYNC_0 6
FDI_LSYNC0 E49 → FDI_LSYNC_0 6

FDI_FSYNC1 C52 → FDI_FSYNC_1 6
FDI_LSYNC1 D51 → FDI_LSYNC_1 6

FDI_INT H46 → FDI_INT 6

RSD

PROC_SEL → HR23 2 1 4.7K → DF_TVS IPD 20K

Place HR23 close to NVRAM connector
and minimize this stub to <100 mils
with PCH and NVRAM connector

M48 R47 Y41 M50 M49 U43 J57 → Reserved_001 DF_TVS Reserved_002 Reserved_003 Reserved_004 Reserved_005 Reserved_006

G56 AB46 K49 K50 → Reserved_007 Reserved_008 Reserved_009 Reserved_010

Y44 L53 → Reserved_011 Reserved_012

Reserved_013 AB50
Reserved_014 Y50
Reserved_015 AB49
Reserved_016 AB44
Reserved_017 U49
Reserved_018 R44
Reserved_019 U50
Reserved_020 U46
Reserved_021 U44
Reserved_022 H50
Reserved_023 K46
Reserved_024 L56
Reserved_025 J55
Reserved_026 F53
Reserved_027 H52
Reserved_028 E52

Reserved_029 R50 TP_NV_RCOMP 1 ST1 NOBOM

CLOCK

+1P05V_PCH
SR136 90.9 1%
XCLK_RCOMP AL2 → XCLK_RCOMP

CLKOUT_ITPXDP_N R52 CLKOUT_ITPXDP# VP SR147 → CK_100M_CPUX#
CLKOUT_ITPXDP_P N52 CLKOUT_ITPXDP VP SR148 → CK_100M_CPUX

CLKOUT_DMI_N P31 CLKOUT_DMI# VP SR229 → CK_100M_DMI# 7
CLKOUT_DMI_P R31 CLKOUT_DMI VP SR230 → CK_100M_DMI 7

CLKOUT_DP_N N56 TP_CLKOUT_DP# CLKOUT_BCLK1# ST40 NOBOM
CLKOUT_DP_P M55 TP_CLKOUT_DP# CLKOUT_BCLK1 ST41 NOBOM

CLKOUT_PCIE7N AE2
CLKOUT_PCIE7P AF1

PCH_CLKIN_BCLK_GND0# W53
PCH_CLKIN_BCLK_GND0 V52 → CLKIN_GND0_N CLKIN_GND0_P

PCH_CLKIN_DMI2_GND1# R27
PCH_CLKIN_DMI2_GND1 P27 → CLKIN_GND1_N CLKIN_GND1_P

REFCLK14IN AN8 → REFCLK14IN

SR125 10K SR126 10K SR127 10K SR128 10K SR157 10K
GND

CLKOUT_PCIE6N AB3 CLKOUT_PCIE6# SR153 → CLK_100M_MINI#
CLKOUT_PCIE6P AA2 CLKOUT_PCIE6 SR154 → CLK_100M_MINI

CLKOUT_PCIE5N AF3 CLKOUT_PCIE5# VP SR233 → CLK_100M_MINI#
CLKOUT_PCIE5P AG2 CLKOUT_PCIE5 VP SR234 → CLK_100M_MINI

CLKOUT_PCIE4N Y9 TP_CLKOUT_PCIE4# VP SR241 → CK_100M_PCHX#
CLKOUT_PCIE4P Y8 TP_CLKOUT_PCIE4 VP SR242 → CK_100M_PCHX

CLKOUT_PCIE3N AB9
CLKOUT_PCIE3P AB8

CLKOUT_PCIE2N AB12 CLKOUT_PCIE2# VP SR235 → CK_100M_LAN#
CLKOUT_PCIE2P AB14 CLKOUT_PCIE2 VP SR236 → CK_100M_LAN

CLKOUT_PCIE1N AA5 CLKOUT_PCIE1# VP SR237 → CK_100M_USB3#
CLKOUT_PCIE1P W5 CLKOUT_PCIE1 VP SR238 → CK_100M_USB3

CLKOUT_PCIE0N AE6 CLKOUT_PCIE0# VP SR243 → CK_100M_CR#
CLKOUT_PCIE0P AC6 CLKOUT_PCIE0 VP SR244 → CK_100M_CR

CLKOUT_PEG_A_N AG8 CLKOUT_PEG_A# VP SR239 → CLK_PEGA#
CLKOUT_PEG_A_P AG9 CLKOUT_PEG_A VP SR240 → CLK_PEGA

CLKOUT_PEG_B_N AE12 TP_CLKOUT_PEG_B# ST54 NOBOM
CLKOUT_PEG_B_P AE11 TP_CLKOUT_PEG_B ST55 NOBOM

XTAL_25M_PCH_IN AJ3 → XTAL25_IN
XTAL_25M_PCH_OUT AJ5 → XTAL25_OUT

SR140 1MOHM 1%
Y12 25Mhz
SR142 0
SC55 27PF/50V NPO 5%
SC56 27PF/50V NPO 5%
R1.02
GND

CLKOUT_PCI0 AT11 IPD 20K PCH_CLKOUT_PCI0 SR251 22 OHM → CK_33M_SIO 46
CLKOUT_PCI1 AN14 IPD 20K PCH_CLKOUT_PCI1 SR262 22 OHM → CLK_DBGPCI 48
CLKOUT_PCI2 AT12 IPD 20K SR277 22 OHM → CK_33M_PCIFB 15
CLKOUT_PCI3 AT17 IPD 20K
CLKOUT_PCI4 AT14 IPD 20K

CLKOUTFLEX0/GPIO64 AT9 IPD 20K CLKOUTFLEX0_GPIO64 ST143 NOBOM
CLKOUTFLEX1/GPIO65 BA5 IPD 20K TP_CLKOUTFLEX1_GPIO65 SR264 22 OHM → SIO_48M
CLKOUTFLEX2/GPIO66 AW5 IPD 20K
CLKOUTFLEX3/GPIO67 BA2 IPD 20K

NI SR265 22 OHM → CK_27M_GPU 71
R1.02

NI SC46 150PF/50V NPO 5%
NI SC47 150PF/50V NPO 5%
GND

PANTHERPOINT

NOTE:

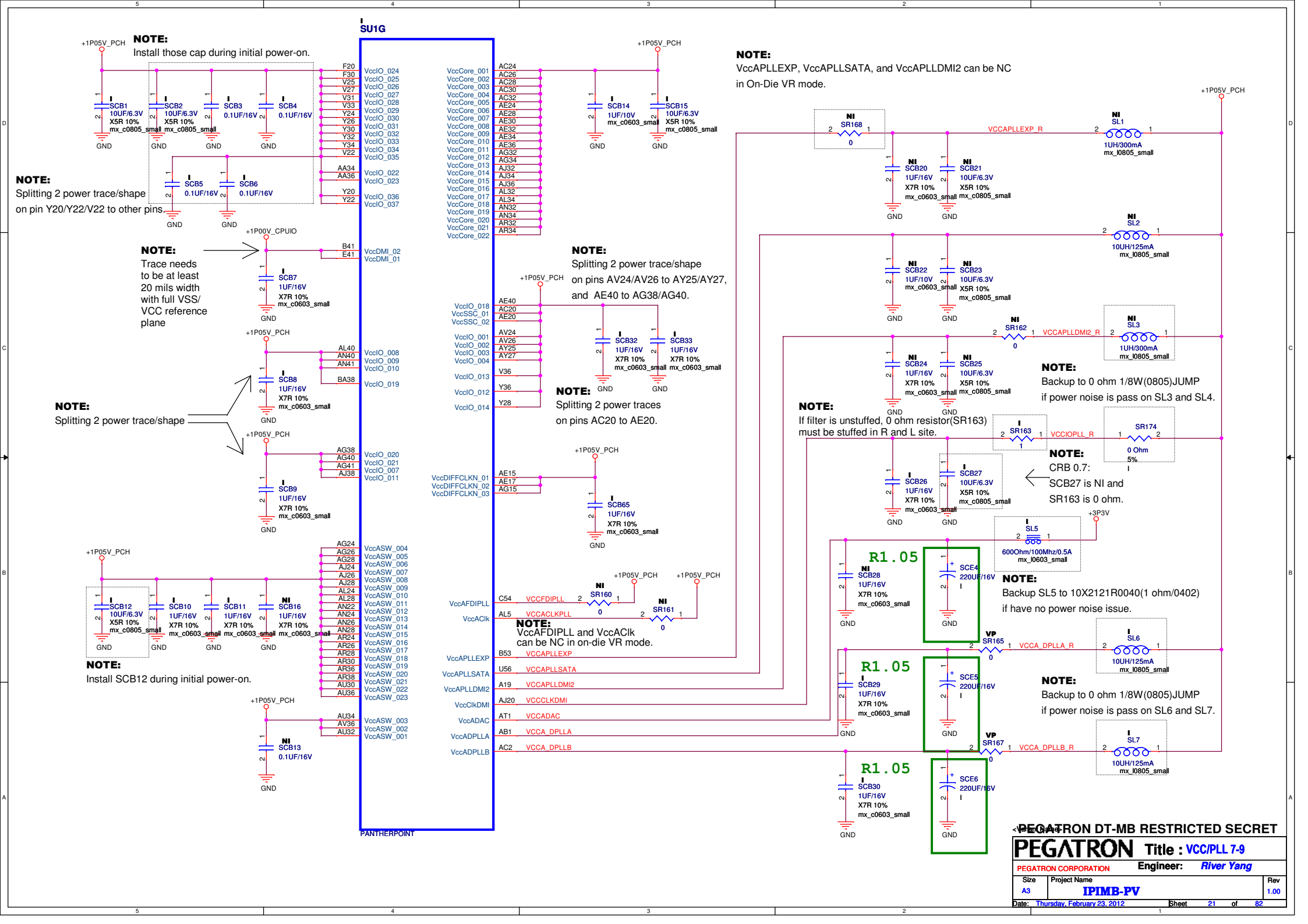
1.Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2.Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2
if more than 2 PCI clocks + PCI loopback are routed.
3.With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
a. 27MHz(SSC/non-SSC) b.14.31818MHz c.24/48 d.25MHz

PEGATRON DT-MB RESTRICTED SECRET
<Variant Name>

PEGATRON Title : CLK/NVRAM/FDI 6-9
PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 20 of 71

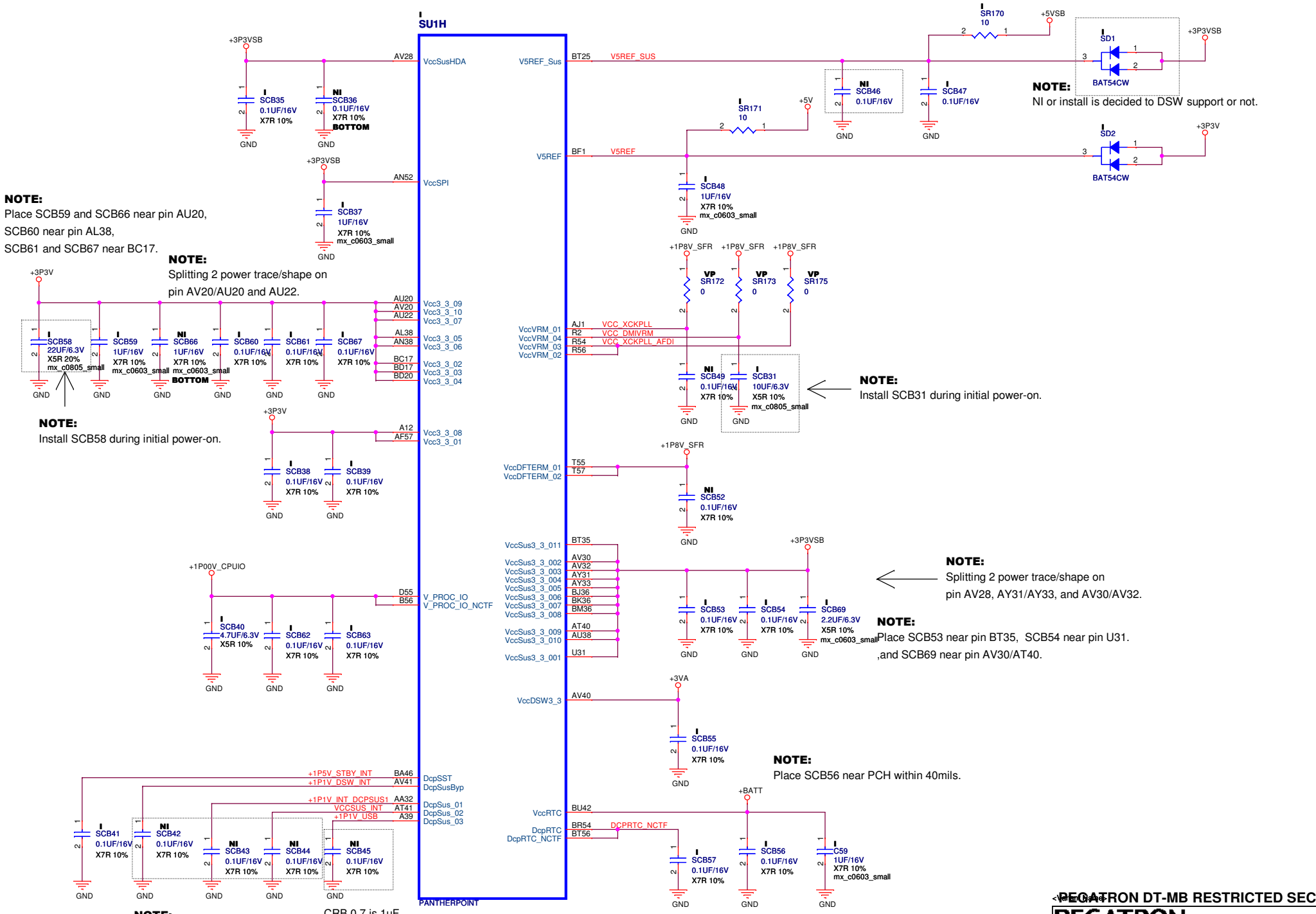


PEGATRON Title : VCC/PLL 7-9

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 21 of 82

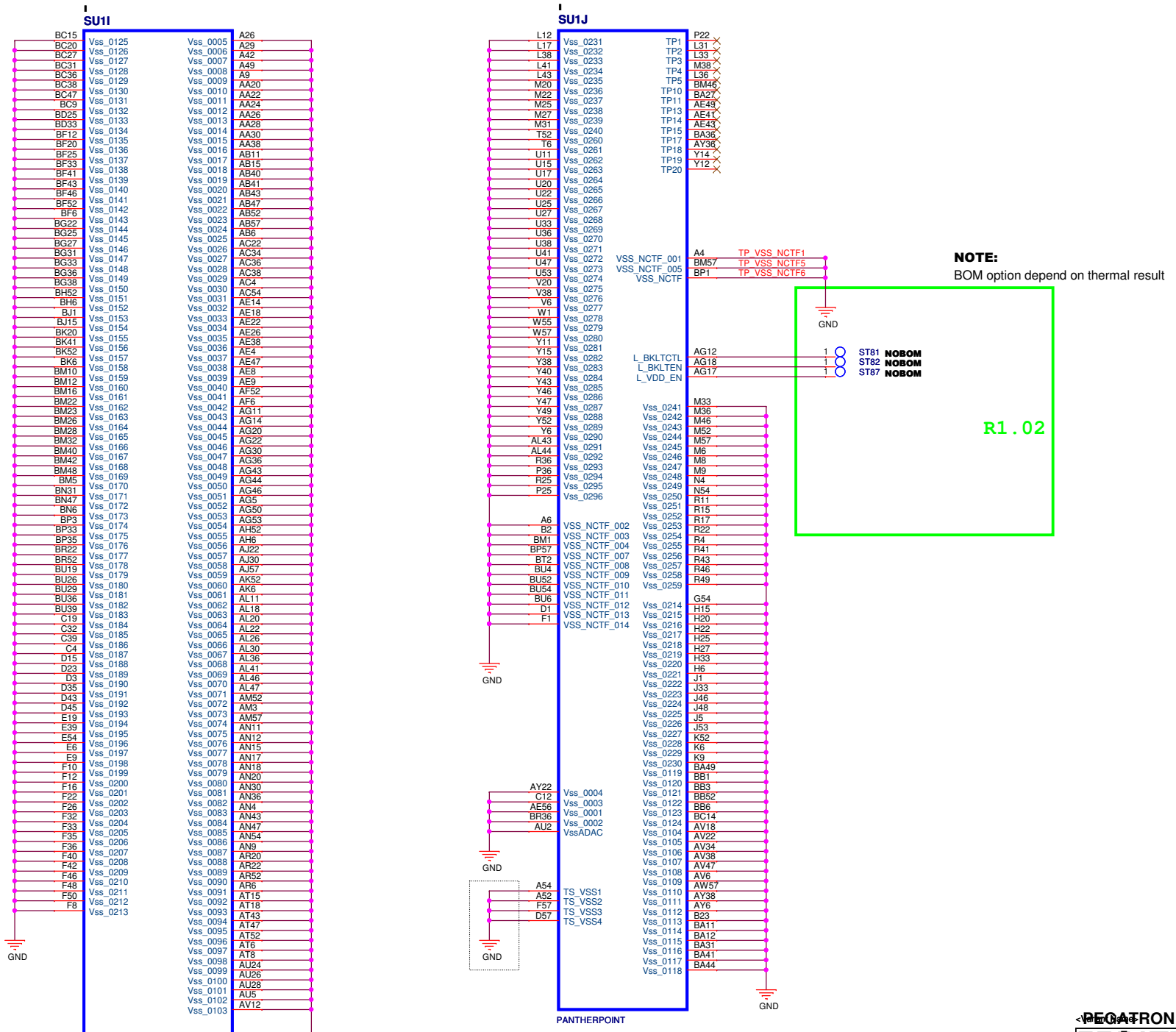


PEGATRON Title : VCCSUS 8-9

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 22 of 82



PEGATRON Title : VSS 9-9

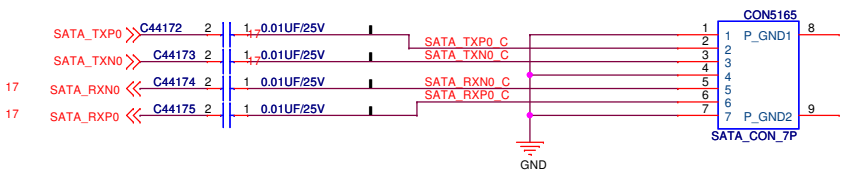
PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

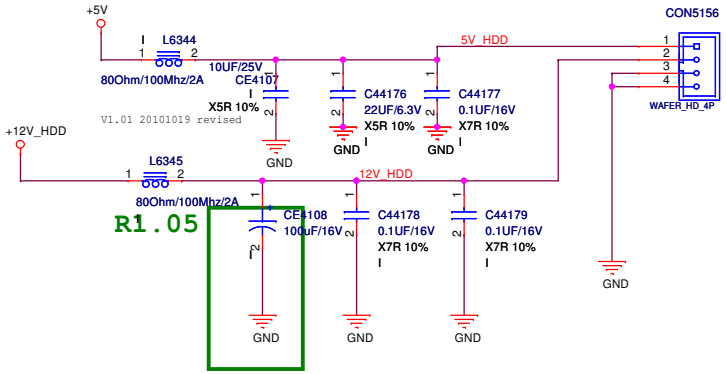
Date: Thursday, February 23, 2012 Sheet 23 of 71

SATA POWER CONN.

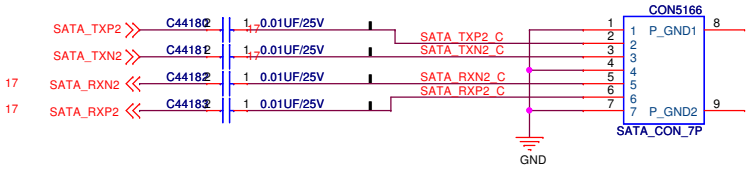
SATA HDD CON



SATA CONTROLLER #1
(MASTER)
COLOR = DARK BLUE

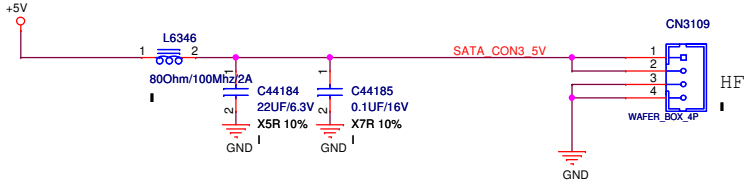


SATA ODD CON



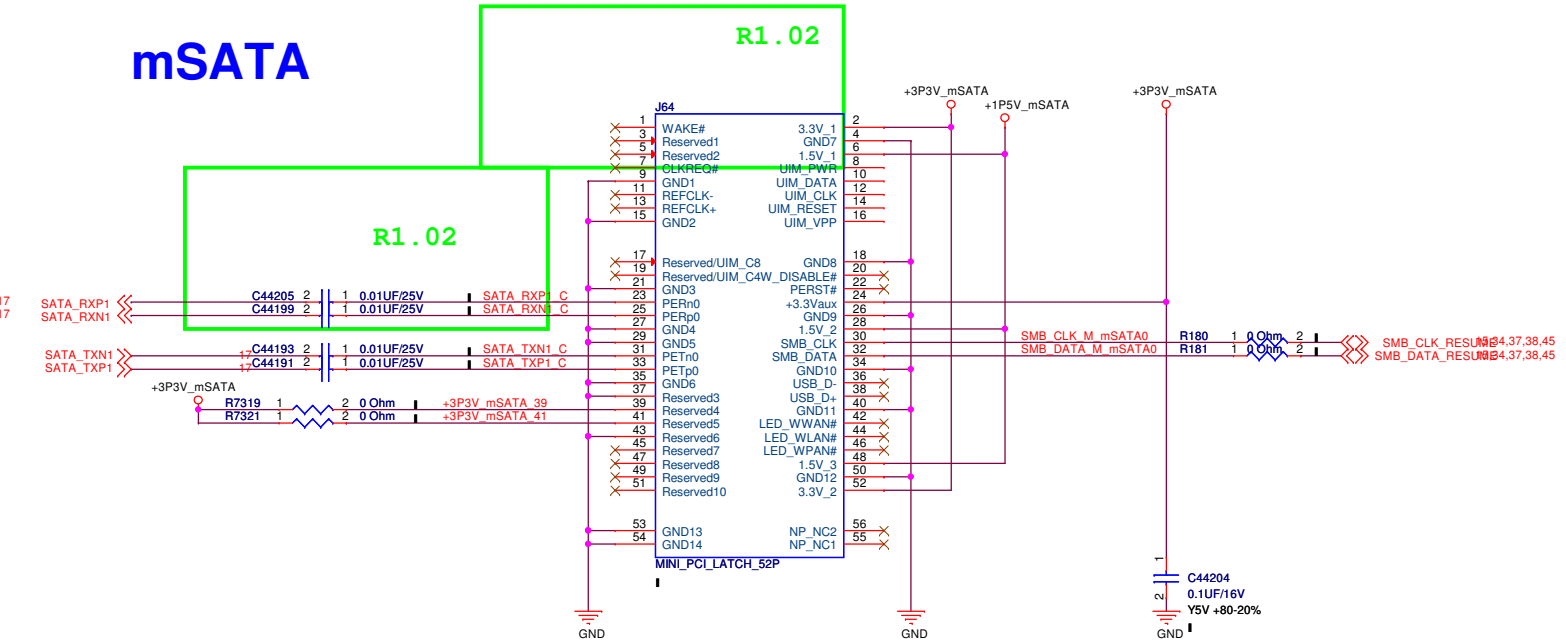
SATA CONTROLLER #2
(SLAVE)
COLOR = WHITE

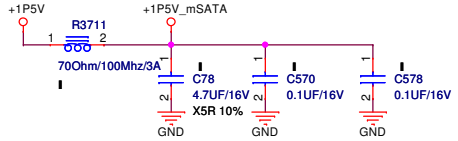
ODD POWER CONN.

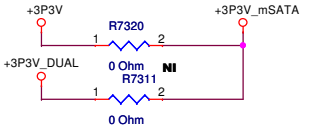


PEGATRON	Title : SATA	
PEGATRON CORPORATION	Engineer: River Yang	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 24 of 71	

mSATA

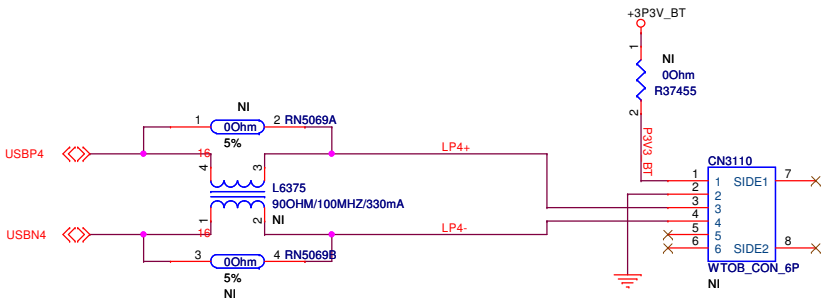


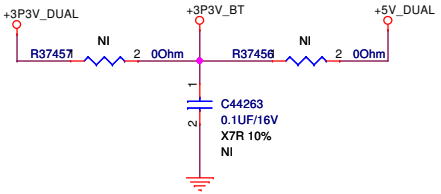


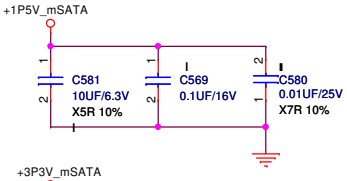


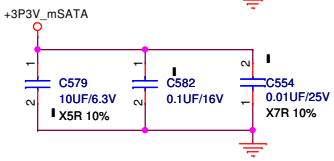
Internal I/O

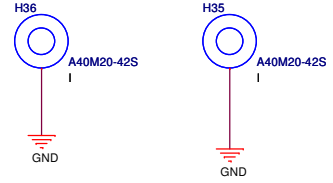
BLUE TOOTH



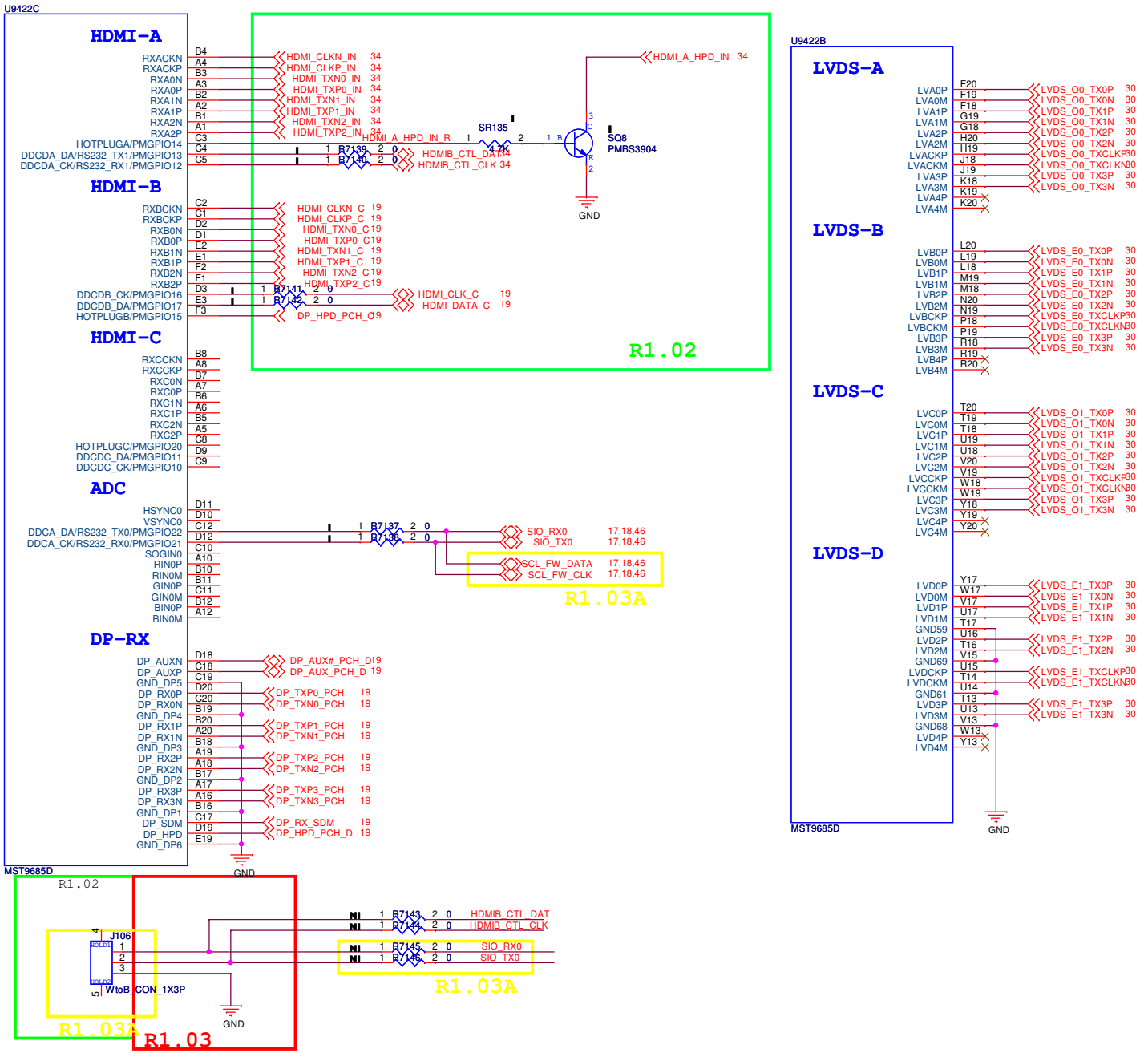






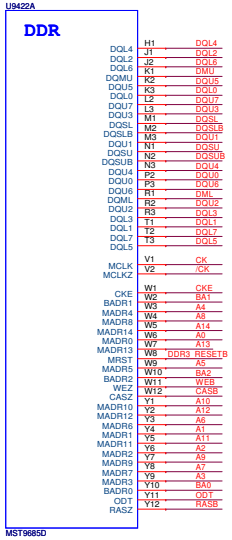


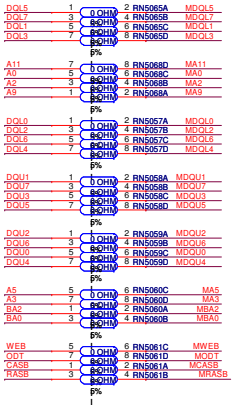
PEGATRON	Title : Mini CARD(mSATA)& BT	
R&D 2	Engineer: River Yang	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 25 of 71	

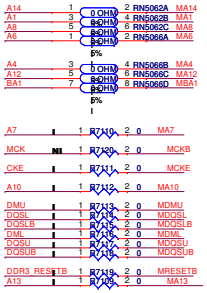


PEGATRON	Title :	HDMI to LVDS-1
PEGATRON CORPORATION	Engineer:	River Yang
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 26 of 71	

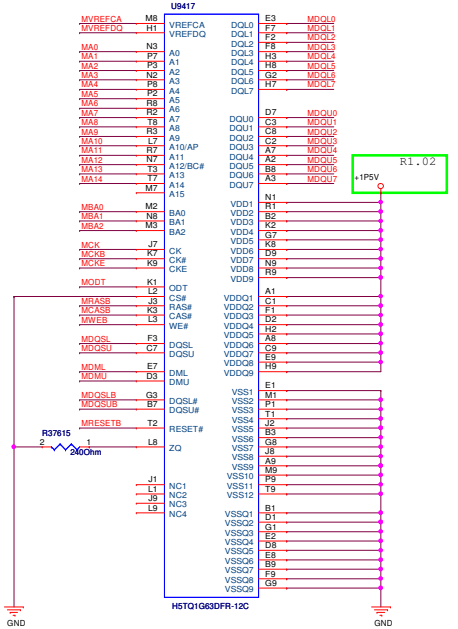
MST9685D DDR

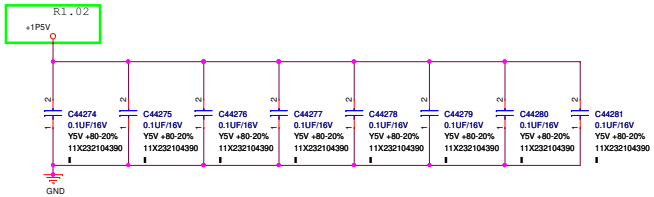


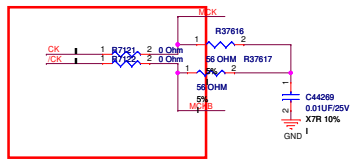




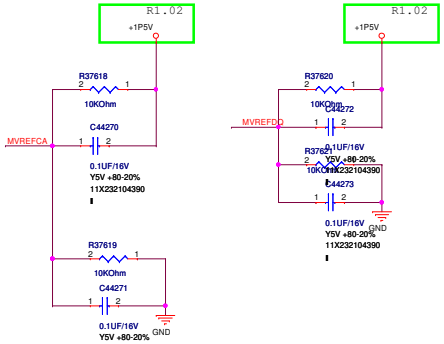
DDR3



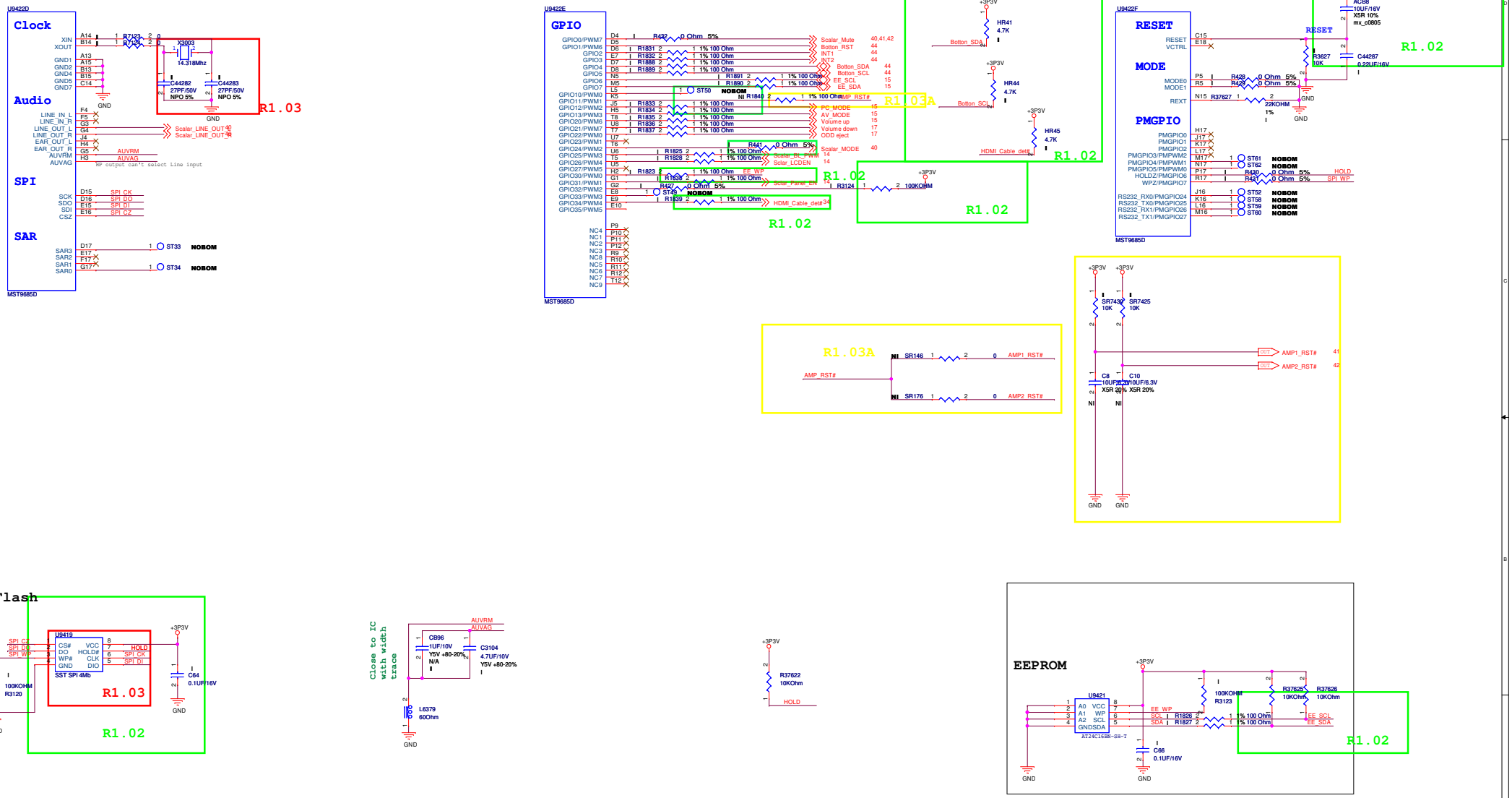




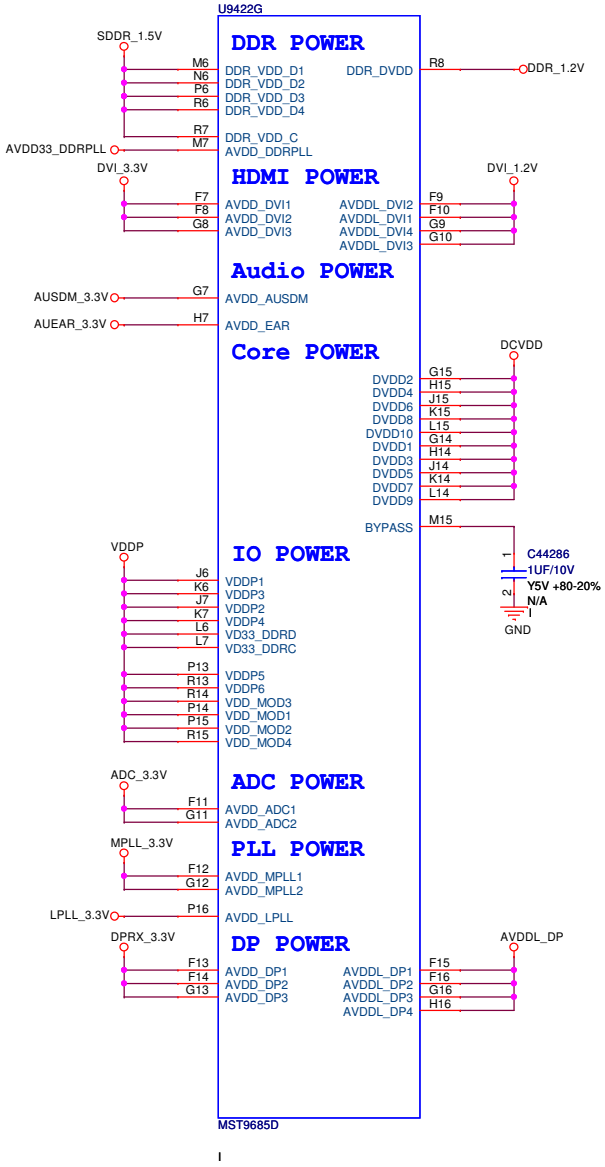
R1.03 EMI BOM ?? 沒導入

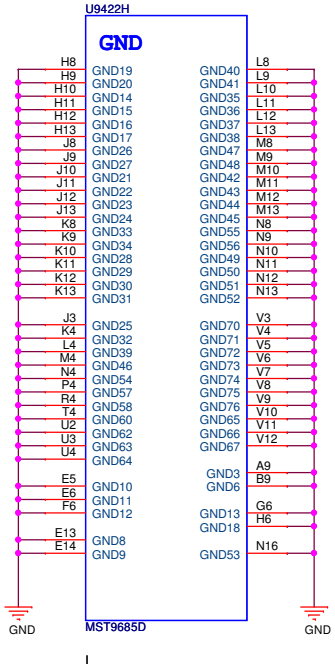


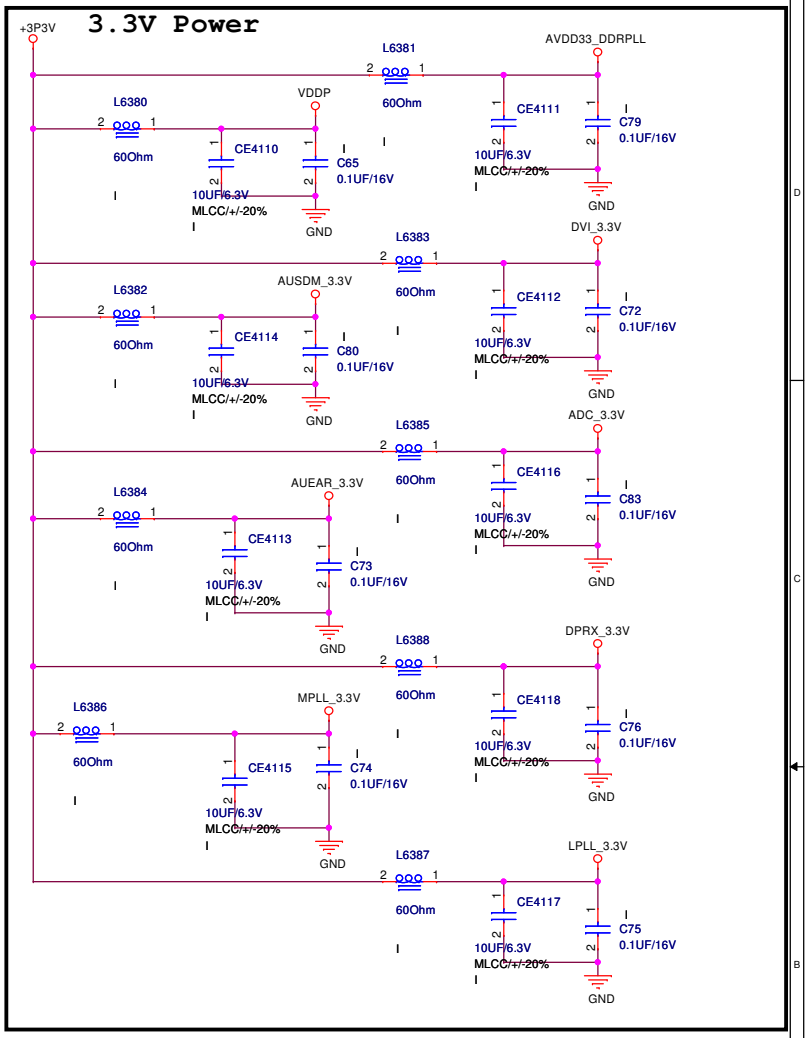
PEGATRON	Title :	HDMI to LVDS-2	
PEGATRON CORPORATION	Engineer:	River Yang	
Size: A2	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet	27 of 52	

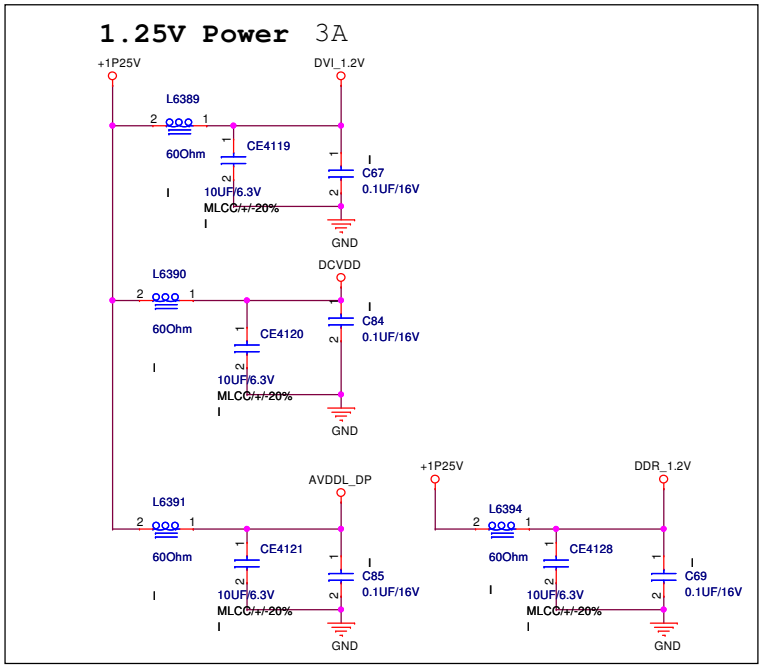


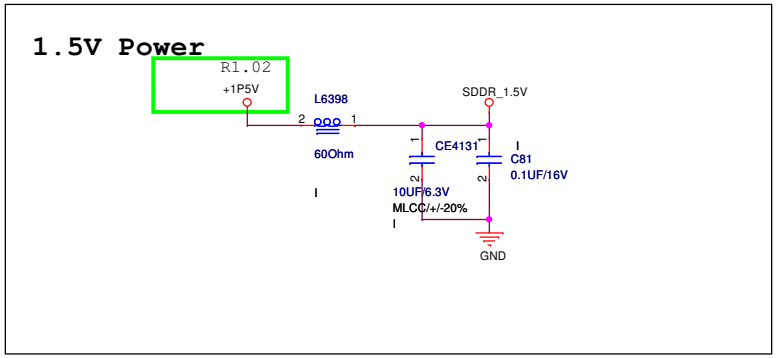
PEGATRON	Title :	HDMI to LVDS-3
PEGATRON CORPORATION	Engineer:	River Yang
Size: A2	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 28 of 52	









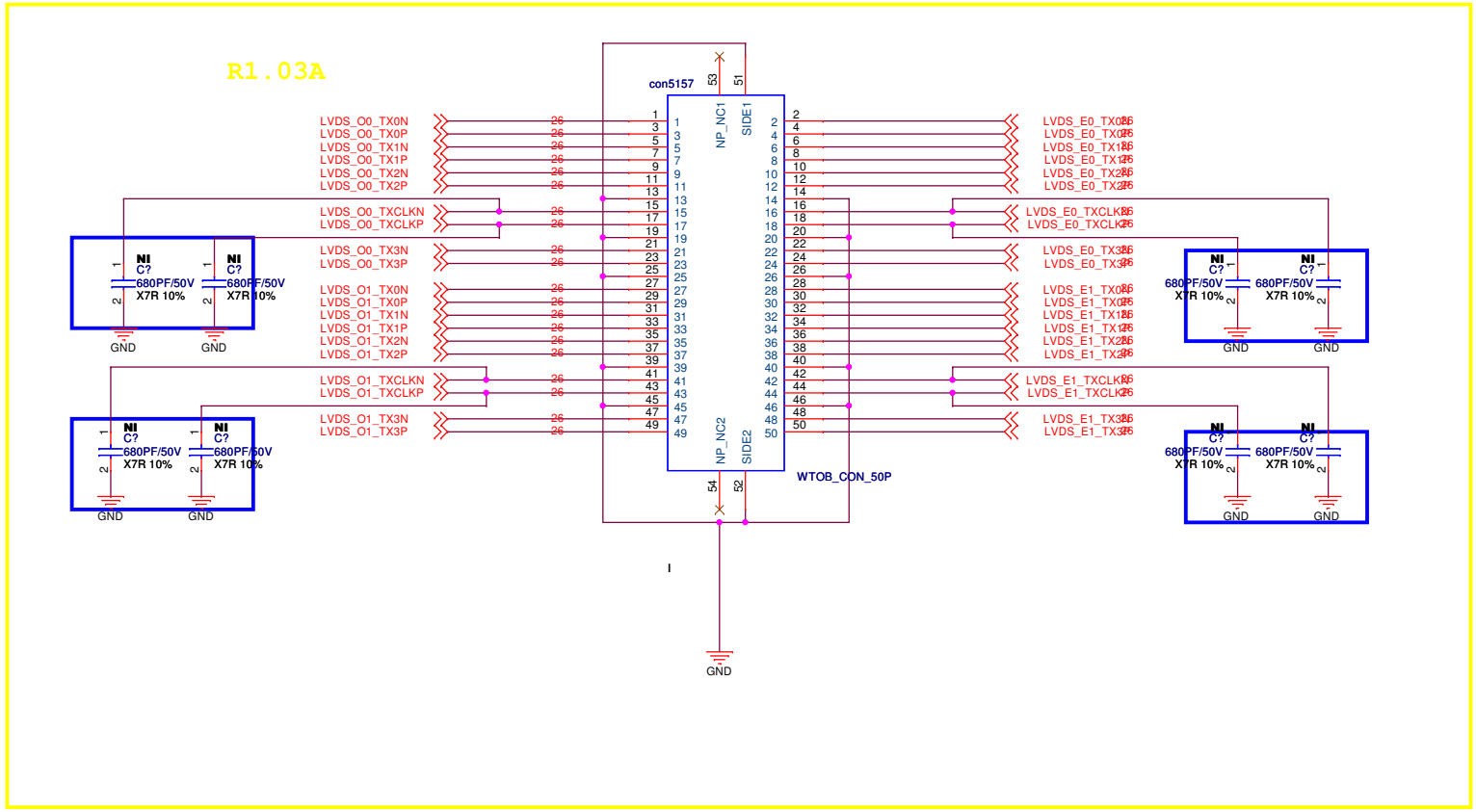


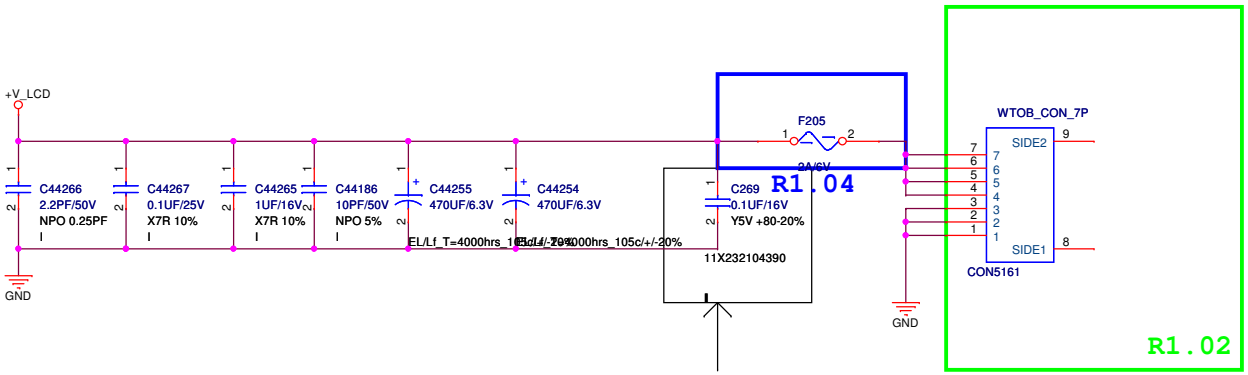
PEGATRON Title : HDMI to LVDS-4

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 29 of 71





NOTE:
Place those cap close to CON5161

<Variant Name>

PEGATRON Title : LVDS connector

<OrgName> Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 30 of 71

<Variant Name>

PEGATRON Title : MHL

<OrgName> Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 31 of 71

D C B A

D C B A

5 4 3 2 1

<Variant Name>

PEGATRON Title : HPD DET

R&D 2 Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

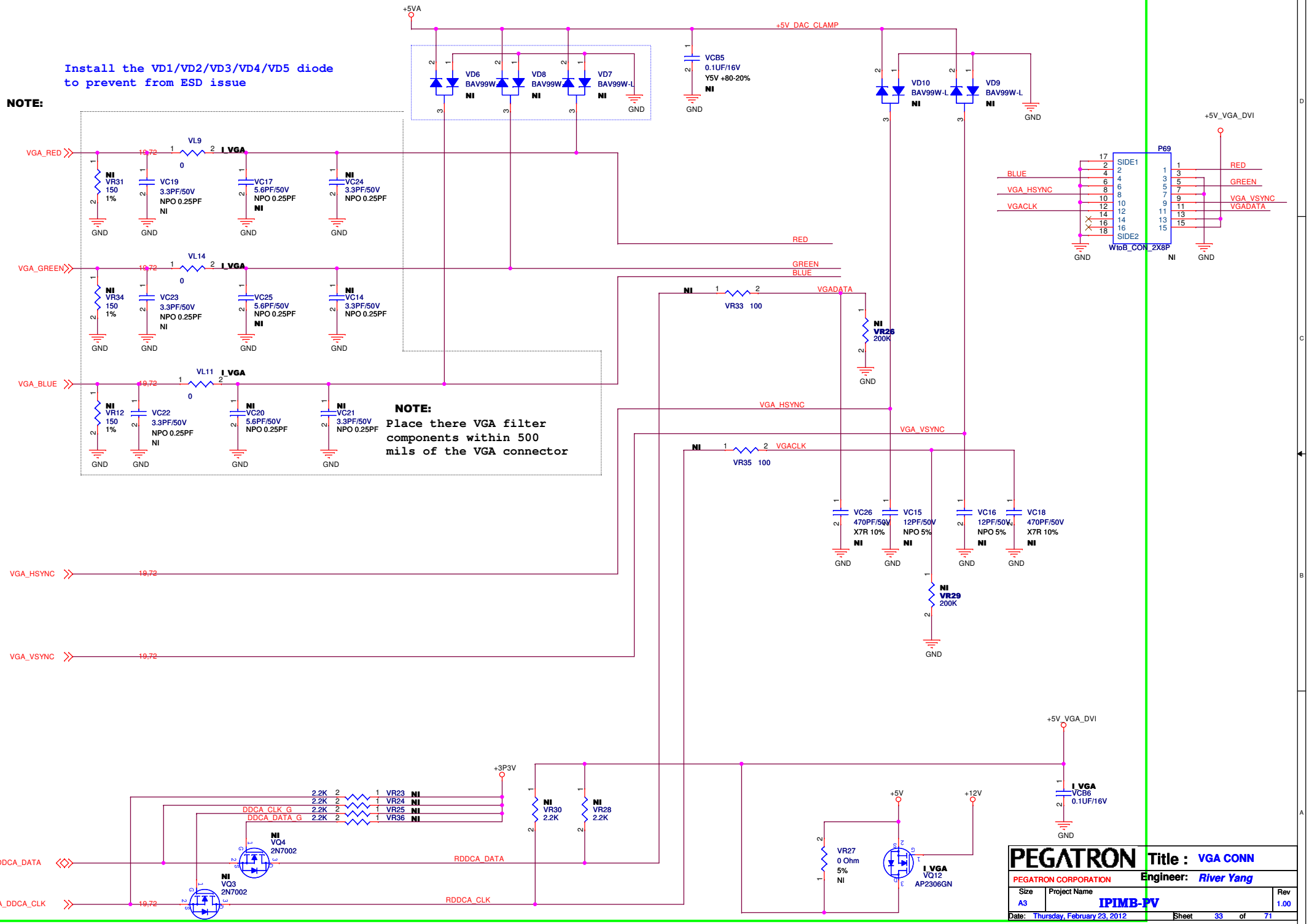
Date: Thursday, February 23, 2012 Sheet 32 of 71

R1.02

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

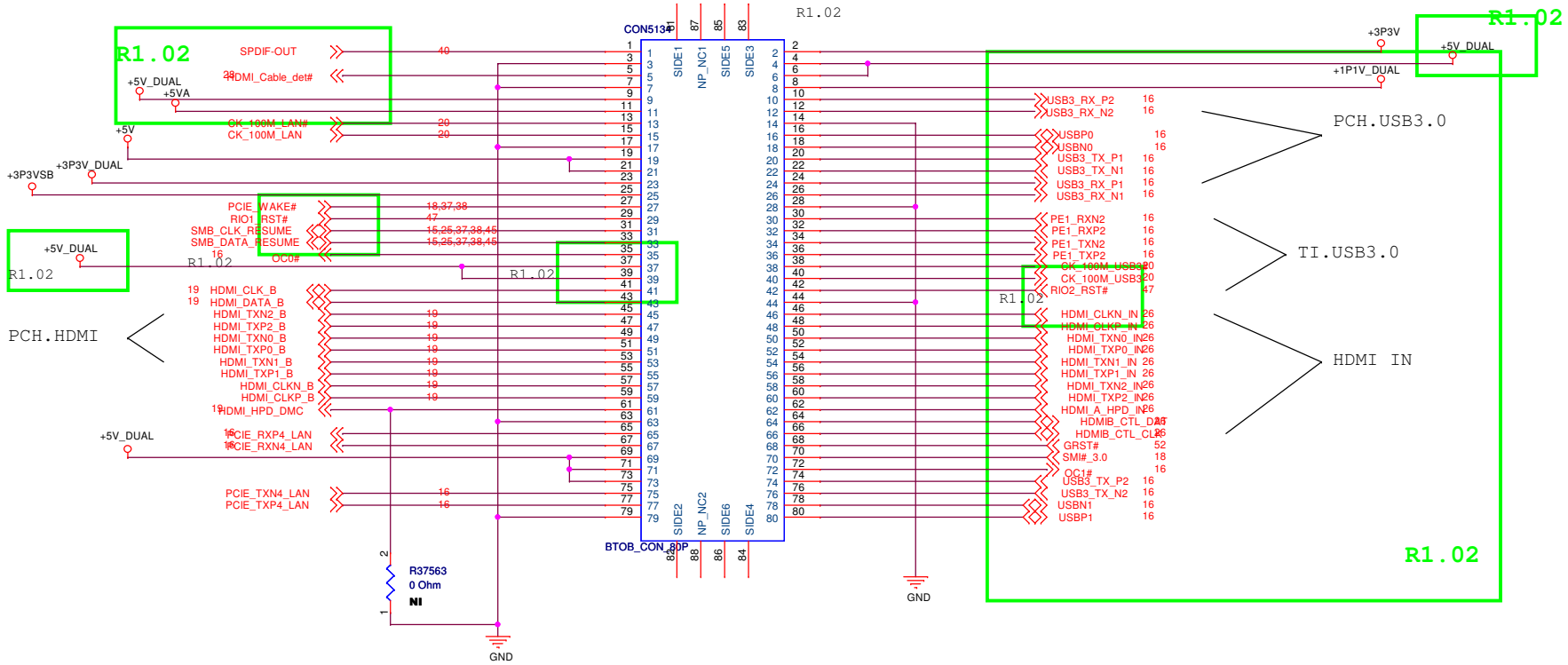
NOTE:

NOTE:
Place there VGA filter components within 500 mils of the VGA connector

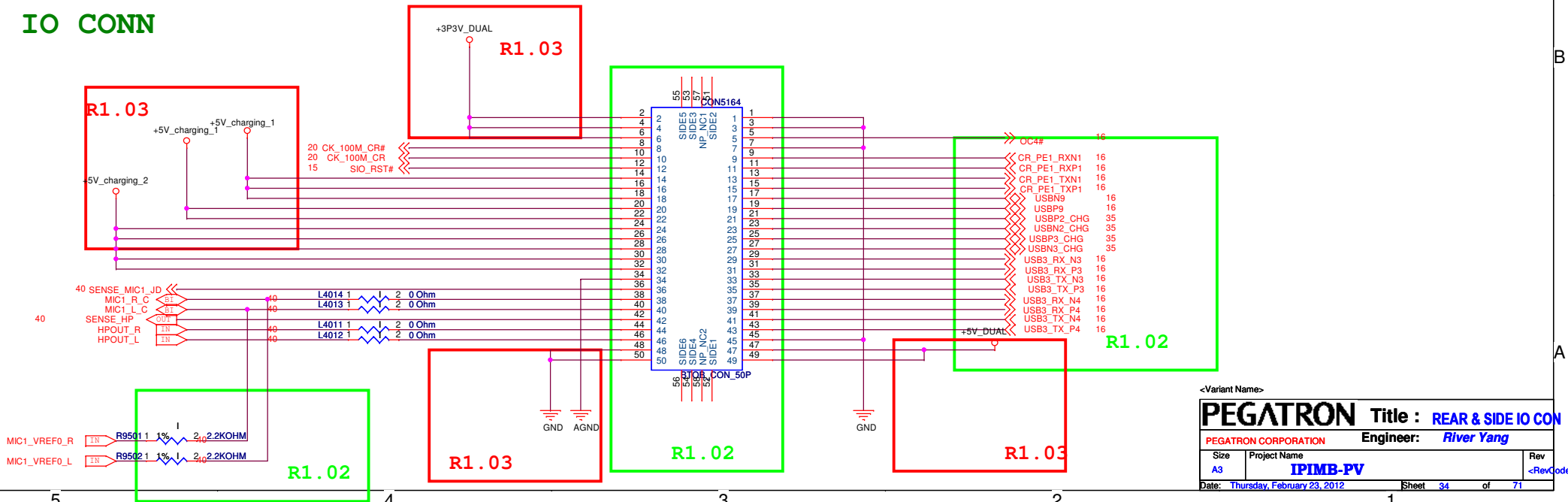


PEGATRON	Title :	VGA CONN
PEGATRON CORPORATION	Engineer:	River Yang
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 33 of 71	

REAR IO CONN



SIDE IO CONN



<Variant Name>

PEGATRON Title : REAR & SIDE IO CON

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	<RevCode>

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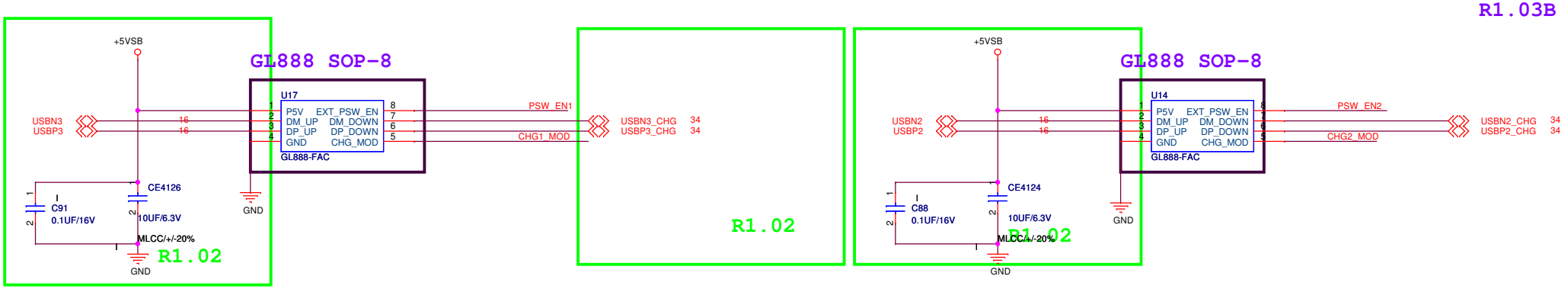
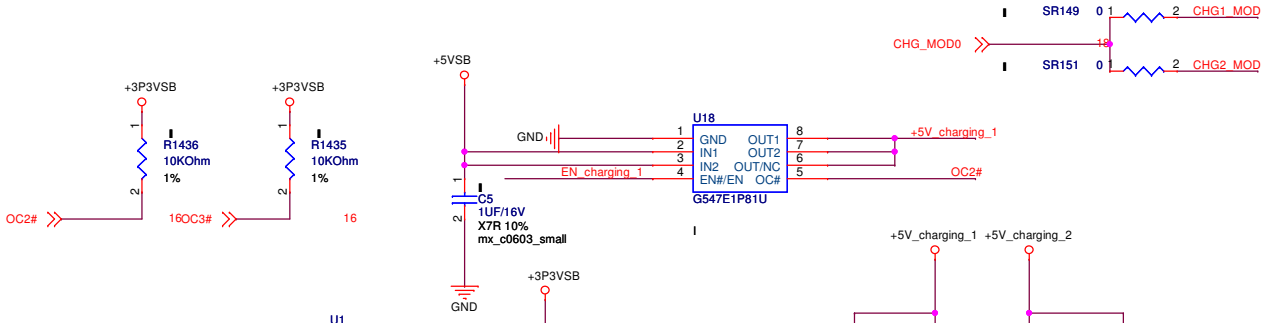
R1.03B

GL888 SOP-8





Controlled Status		Power Switch
Option1	0	Disable
PSW_EN1	1	Enable

Controlled Status		Power Switch
Option1	0	Disable
PSW_EN2	1	Enable

		CHG_MOD0	Charge Mode
		0	CDP mode
		1	Auto mode (DCP and Apple 2A)

<Variant Name>

PEGATRON Title : USB Charging Controller-1

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

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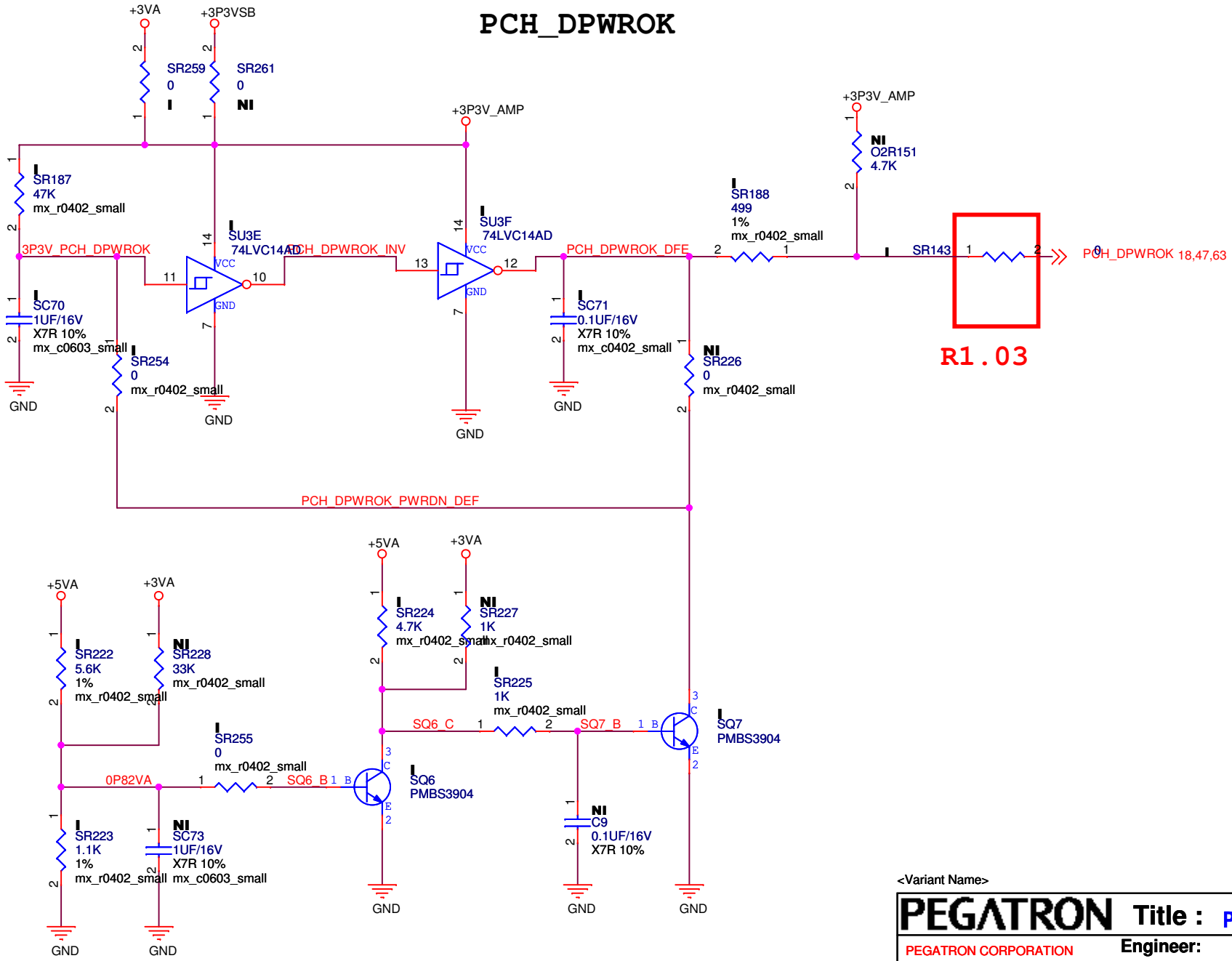


<Variant Name>

PEGATRON

Title : PCH_DPWROK

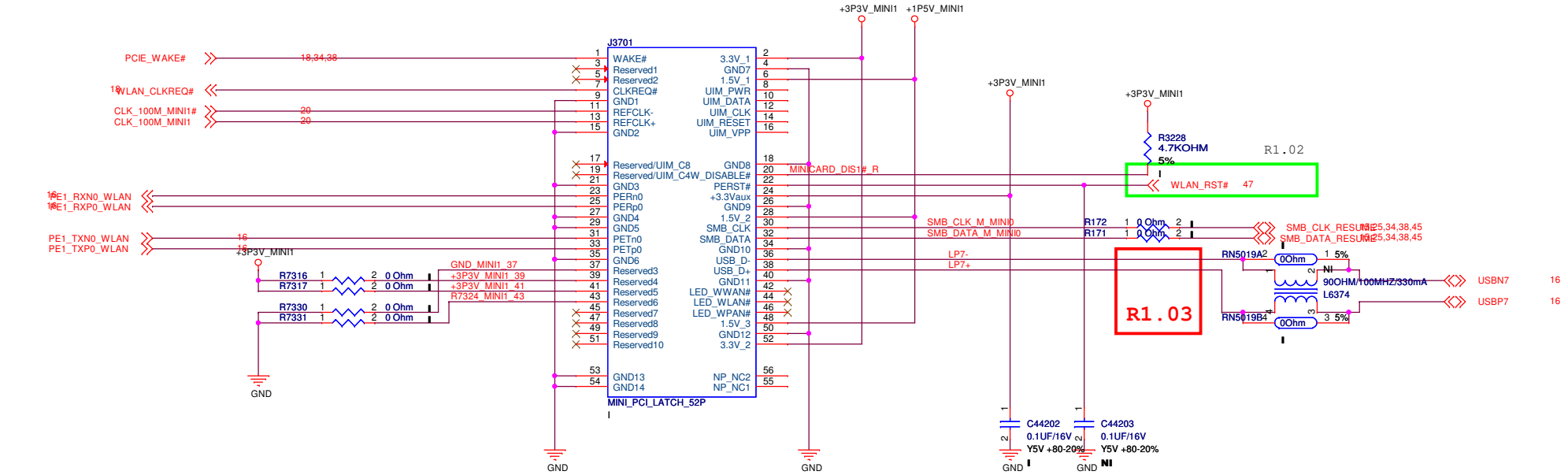
PEGATRON CORPORATION

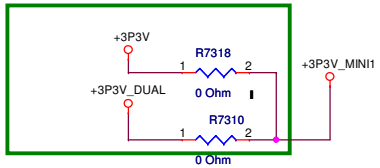
Engineer: River Yang

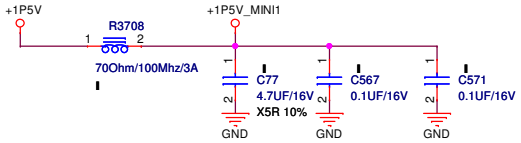
Size	Project Name	Rev
A4	IPIMB-PV	<RevC

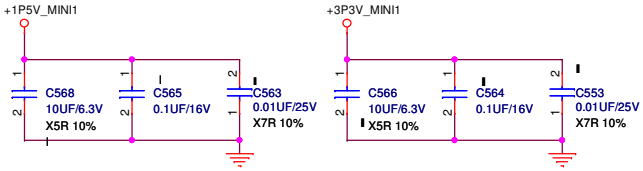
Date: Thursday, February 23, 2012 Sheet 36 of 71

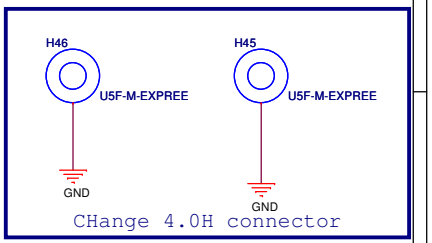
Mini Card(WL)





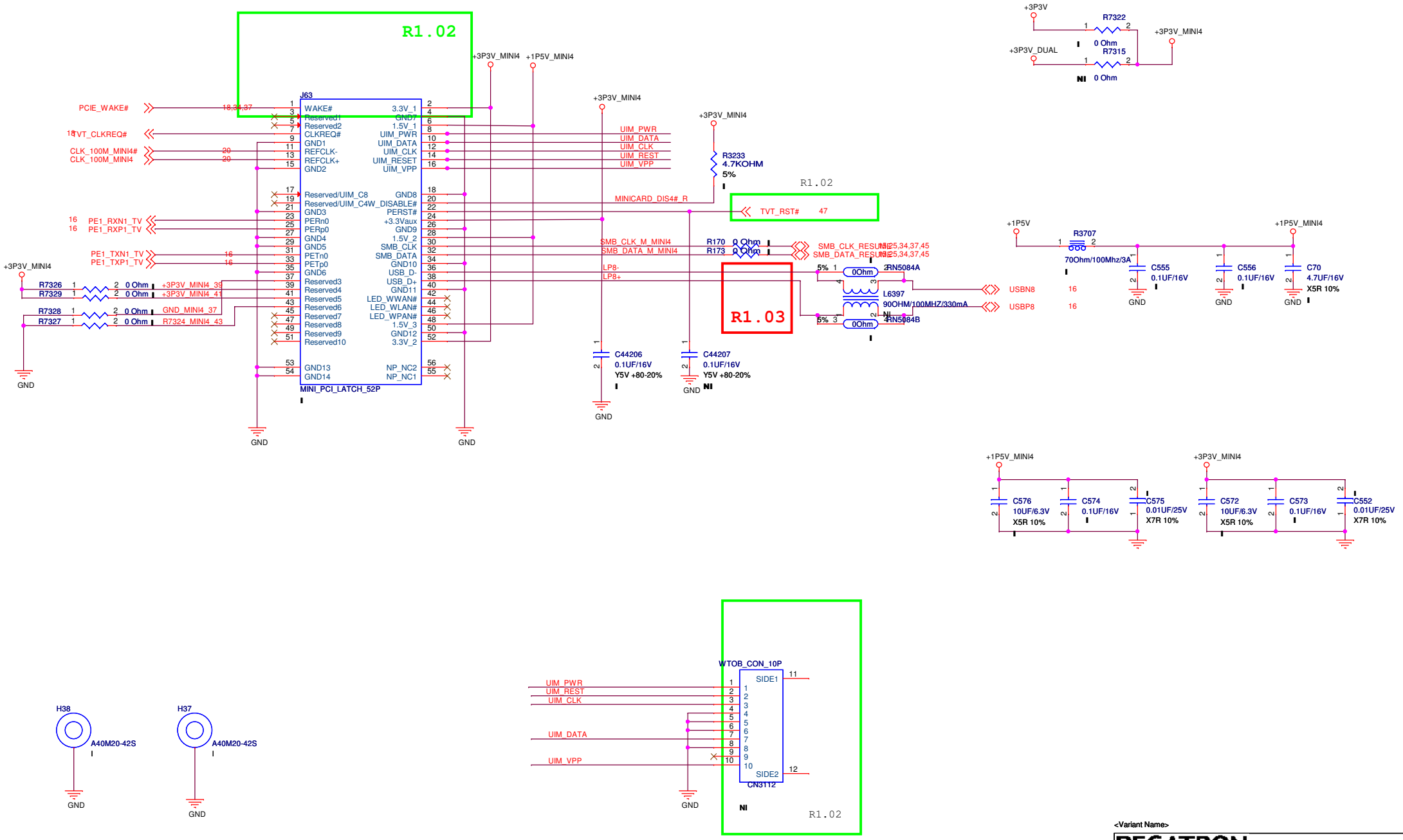






PEGATRON	Title :	Mini Card(WL)
PEGATRON CORPORATION	Engineer:	River Yang
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 37 of 71	

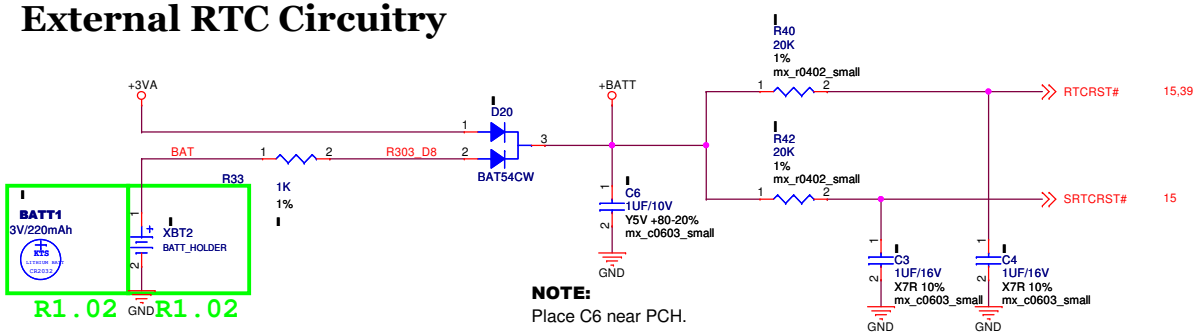
Mini Card(TVT)



<Variant Name>

PEGATRON	Title : Mini Card(TVT)	
PEGATRON CORPORATION	Engineer: River Yang	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 38 of 71	

External RTC Circuitry

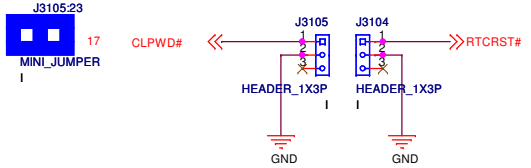


NOTE:
Place C6 near PCH.

Battery Socket

CLR PASSWORD CIRCUIT

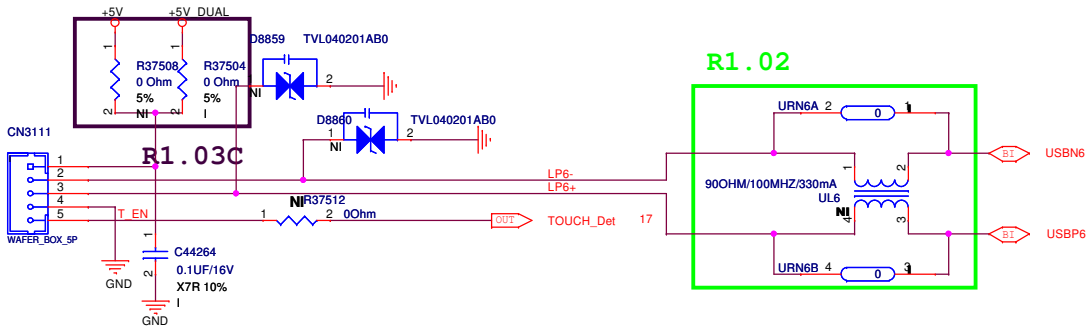
	PASSWORD
1-2	CLEAR
2-3	Default



CLR CMOS CIRCUIT

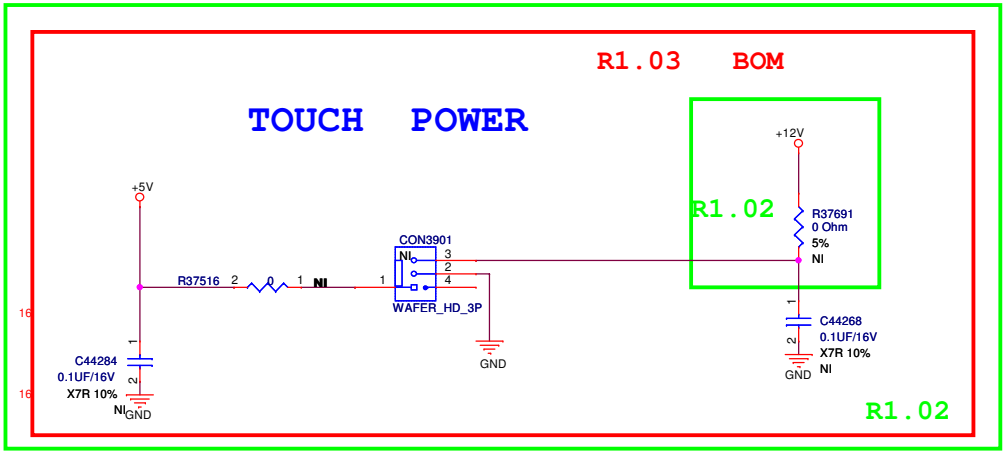
	CMOS RTC
1-2	CLEAR
2-3	Default

TOUCH

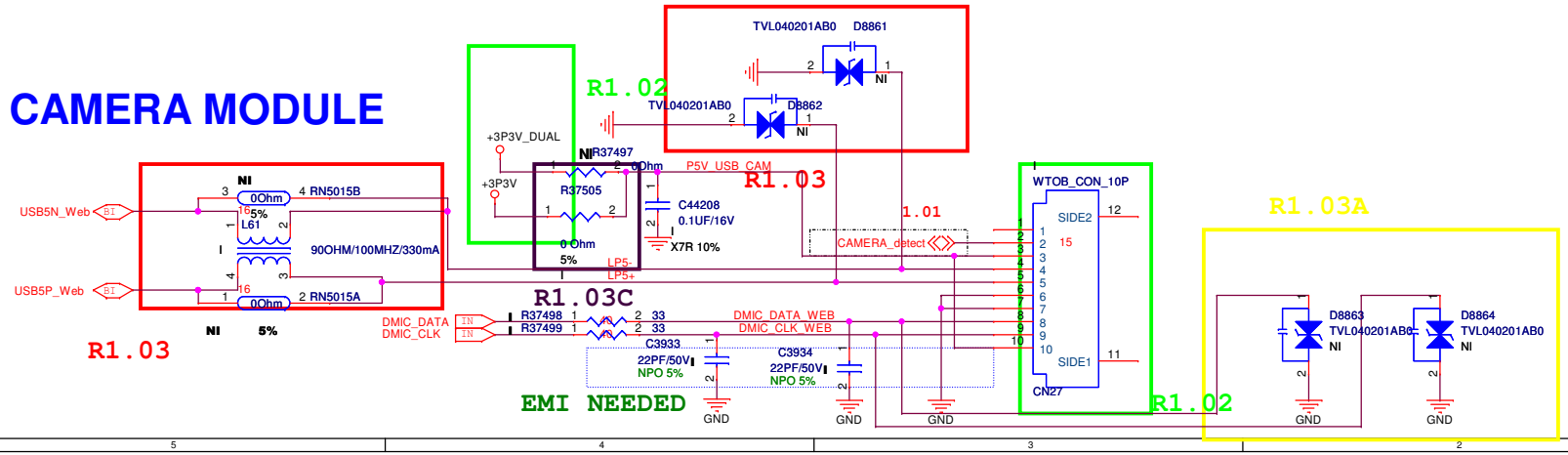


TOUCH POWER

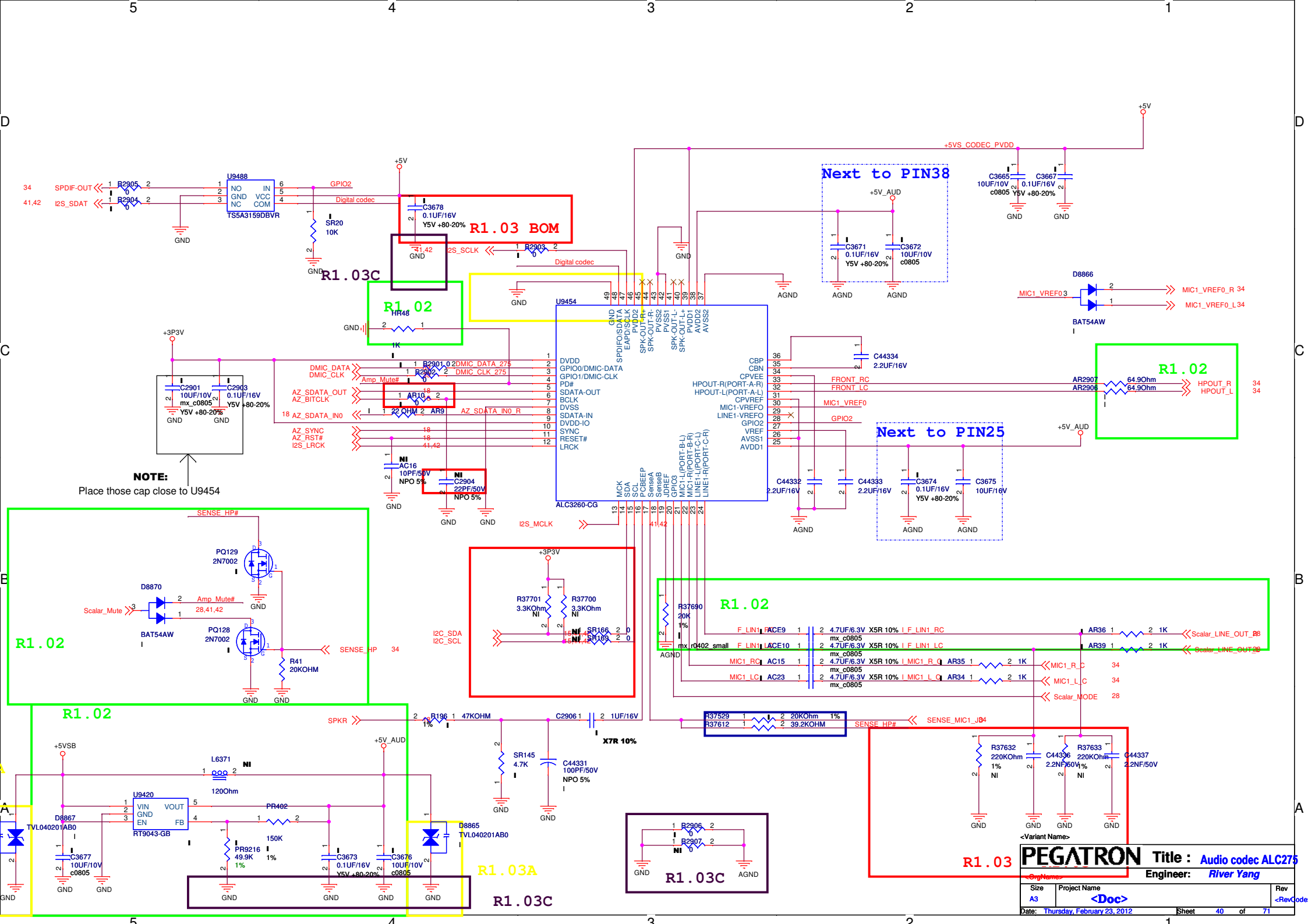
R1.03 BOM

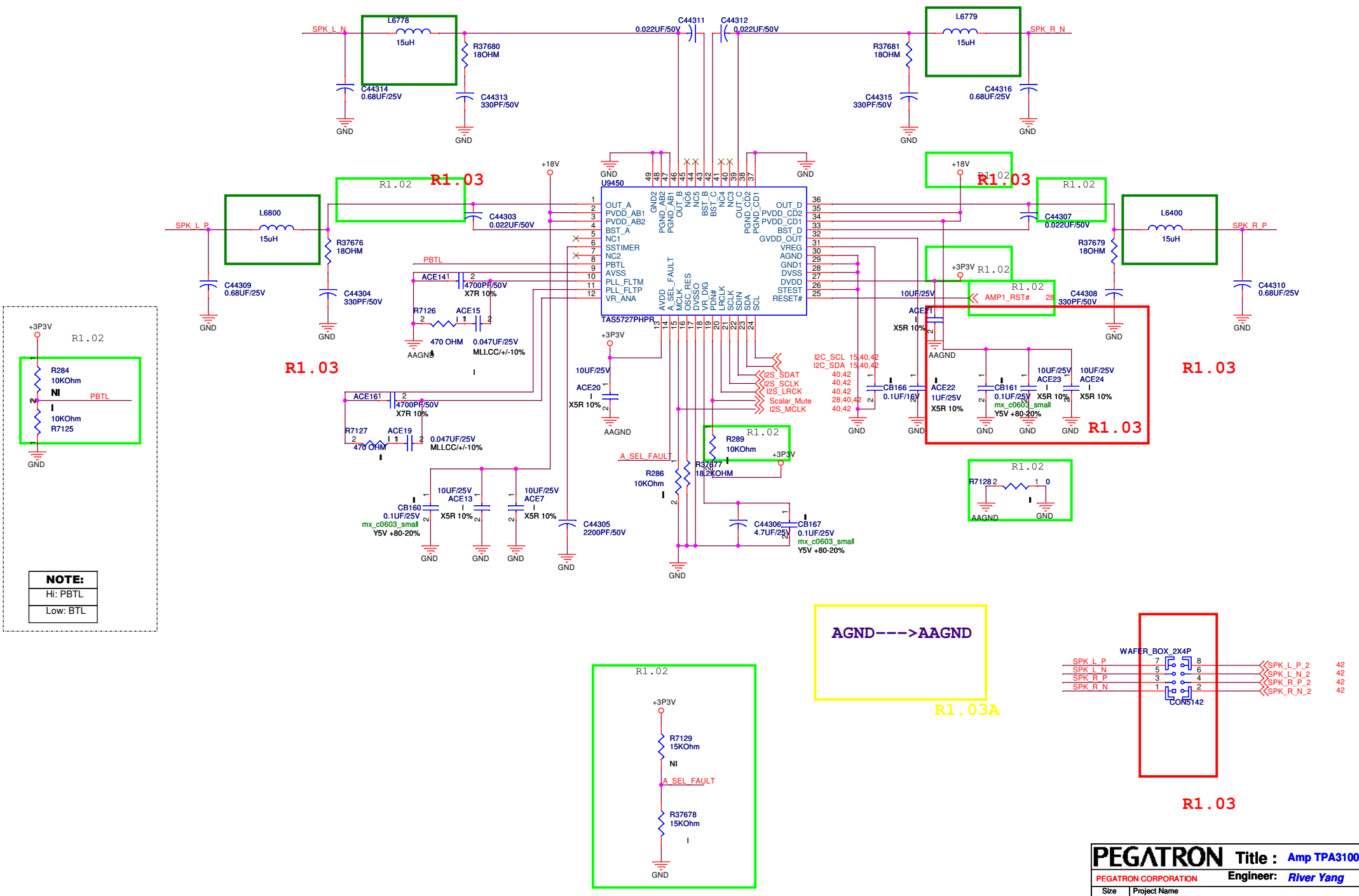


CAMERA MODULE



PEGATRON	Title :	RTC&CAM&TOUCH	
PEGATRON CORPORATION	Engineer:	River Yang	
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 39 of 71		


NOTE:
Place those cap close to U9454
R1.03 BOM
R1.03C
R1.02
R1.03A
Next to PIN38
Next to PIN25
ALC3260-CG
U9454
U9488
TS5A3159DBVR
U9420
RT9043-GB
PEGATRON
Title : Audio codec ALC275
Engineer: River Yang
Project Name
<Doc>
Date: Thursday, February 23, 2012
Sheet 40 of 71



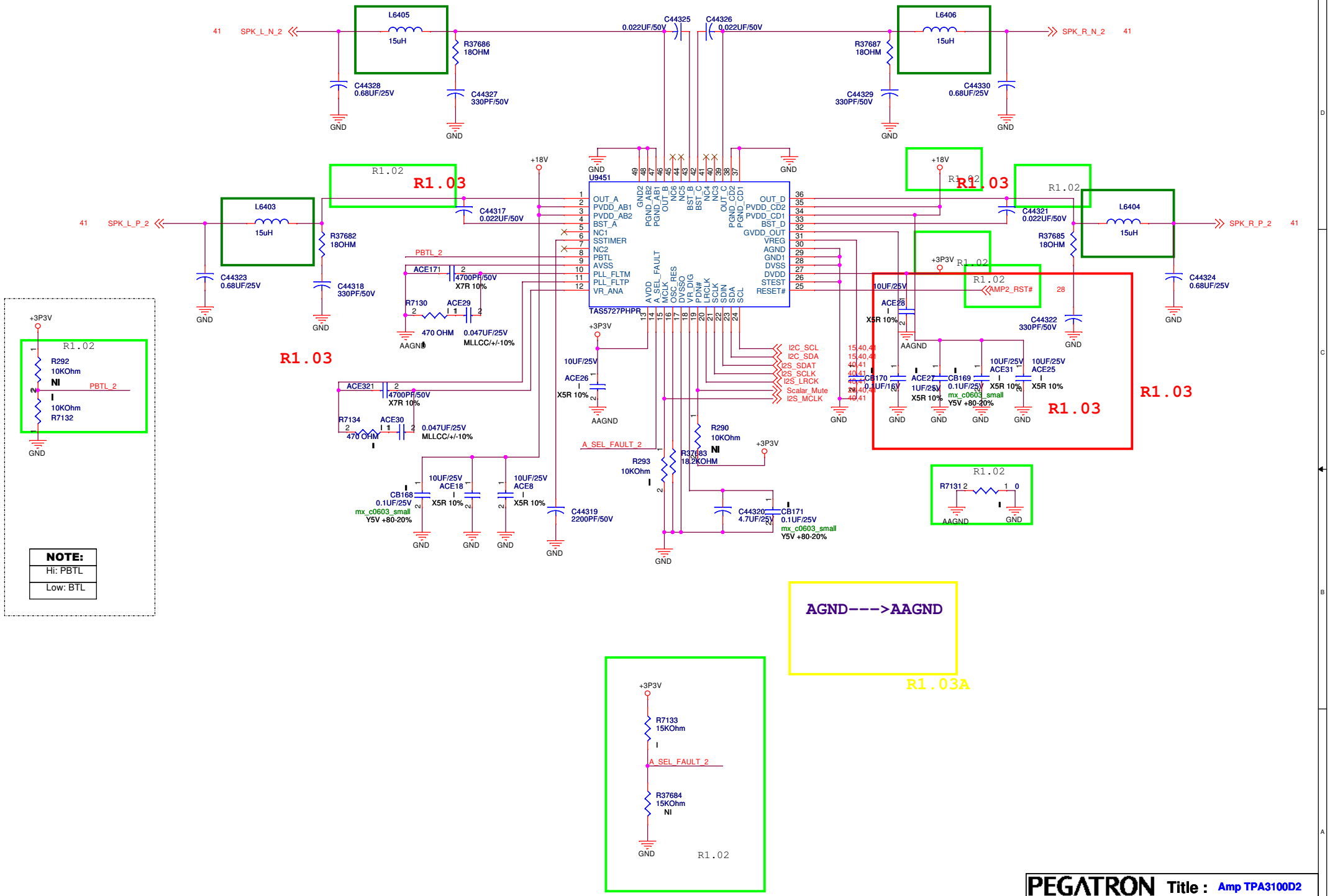
NOTE:

Hi: PBTL
Low: BTL

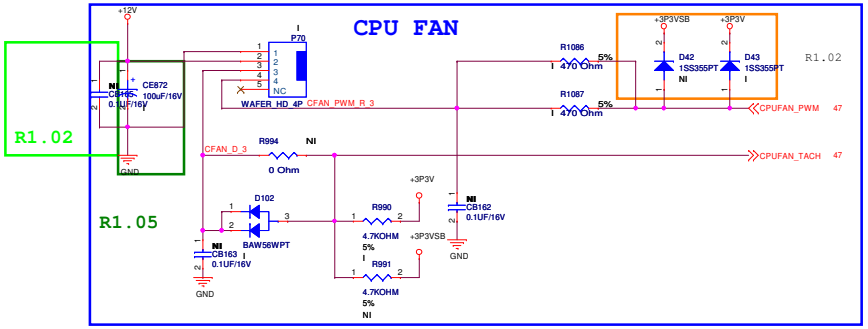
AGND--->AAGND

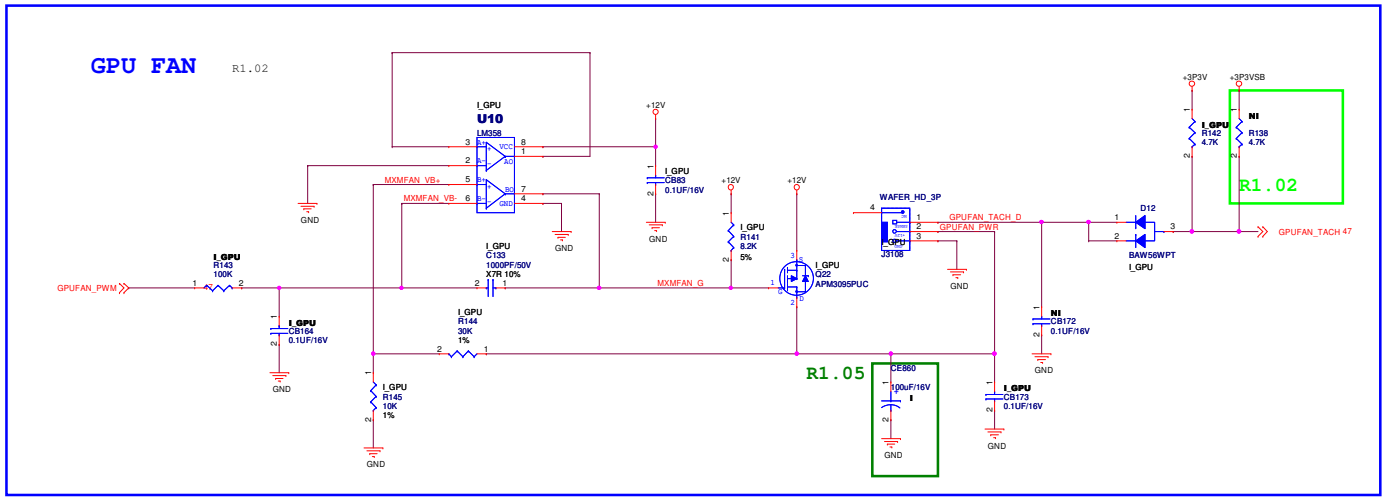
R1.03A

PEGATRON	Title :	Amp TPA3100D2	
PEGATRON CORPORATION	Engineer:	River Yang	
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 41 of 82		



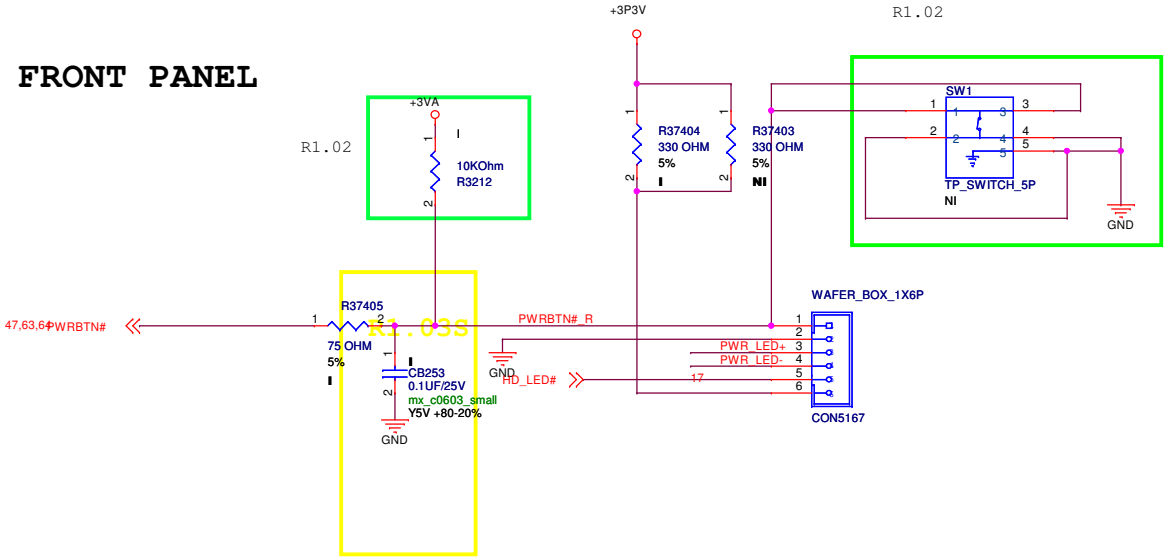
PEGATRON	Title : Amp TPA3100D2	
PEGATRON CORPORATION	Engineer: Jerry, Hsuan	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 42 of 82	

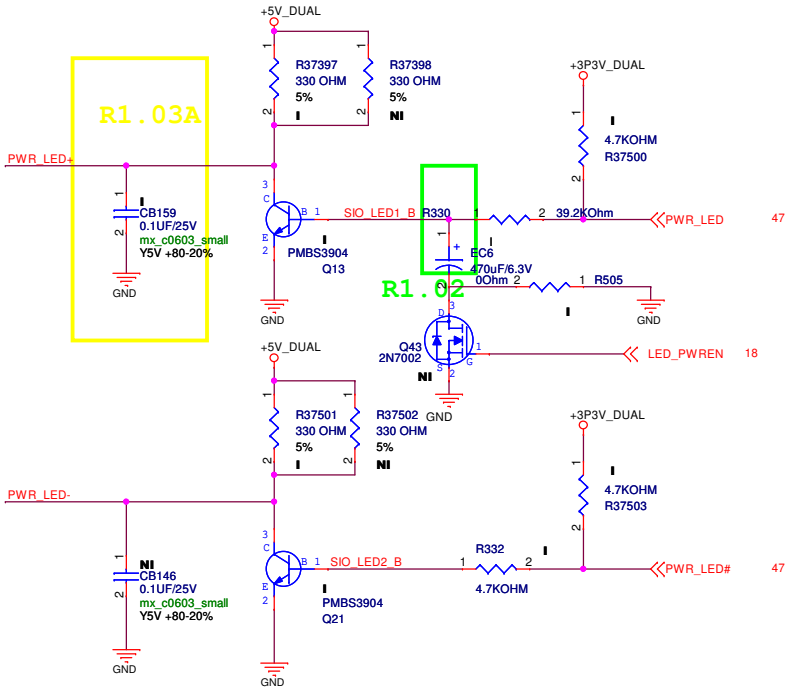




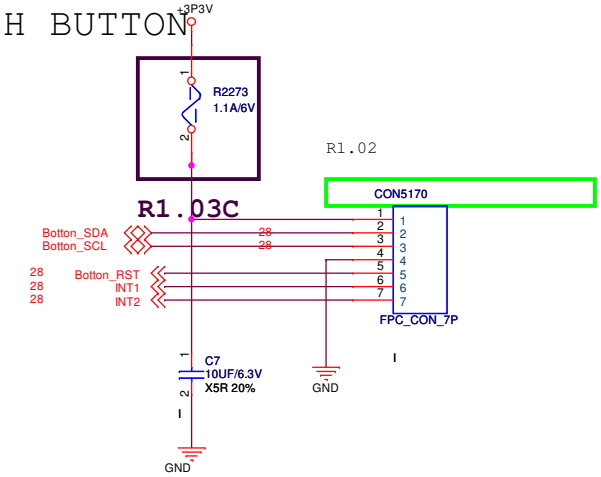
PEGATRON	Title : FAN	
PEGATRON CORPORATION	Engineer: River Yang	
Size: A2	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 43 of 71	

FRONT PANEL

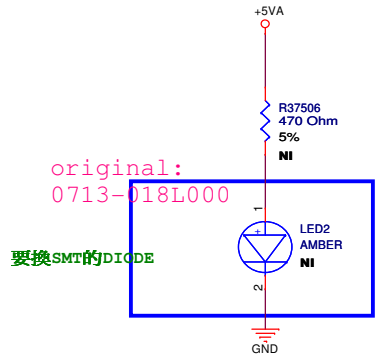




TOUCH BUTTON



Power supply LED



<Variant Name>

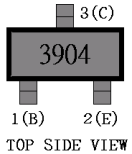
PEGATRON CORP.

Title : FRONT PANEL

Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 44 of 82

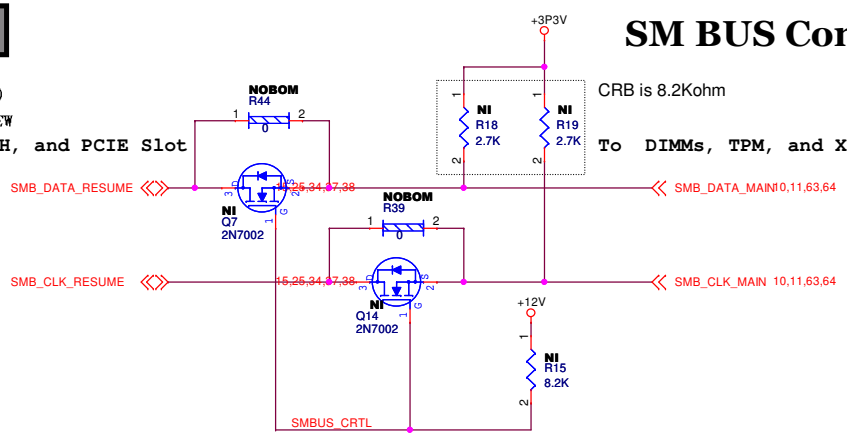


SM BUS Control

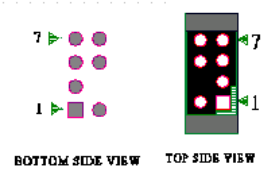
To PCH, and PCIE Slot

To DIMMs, TPM, and XDP Debug Port

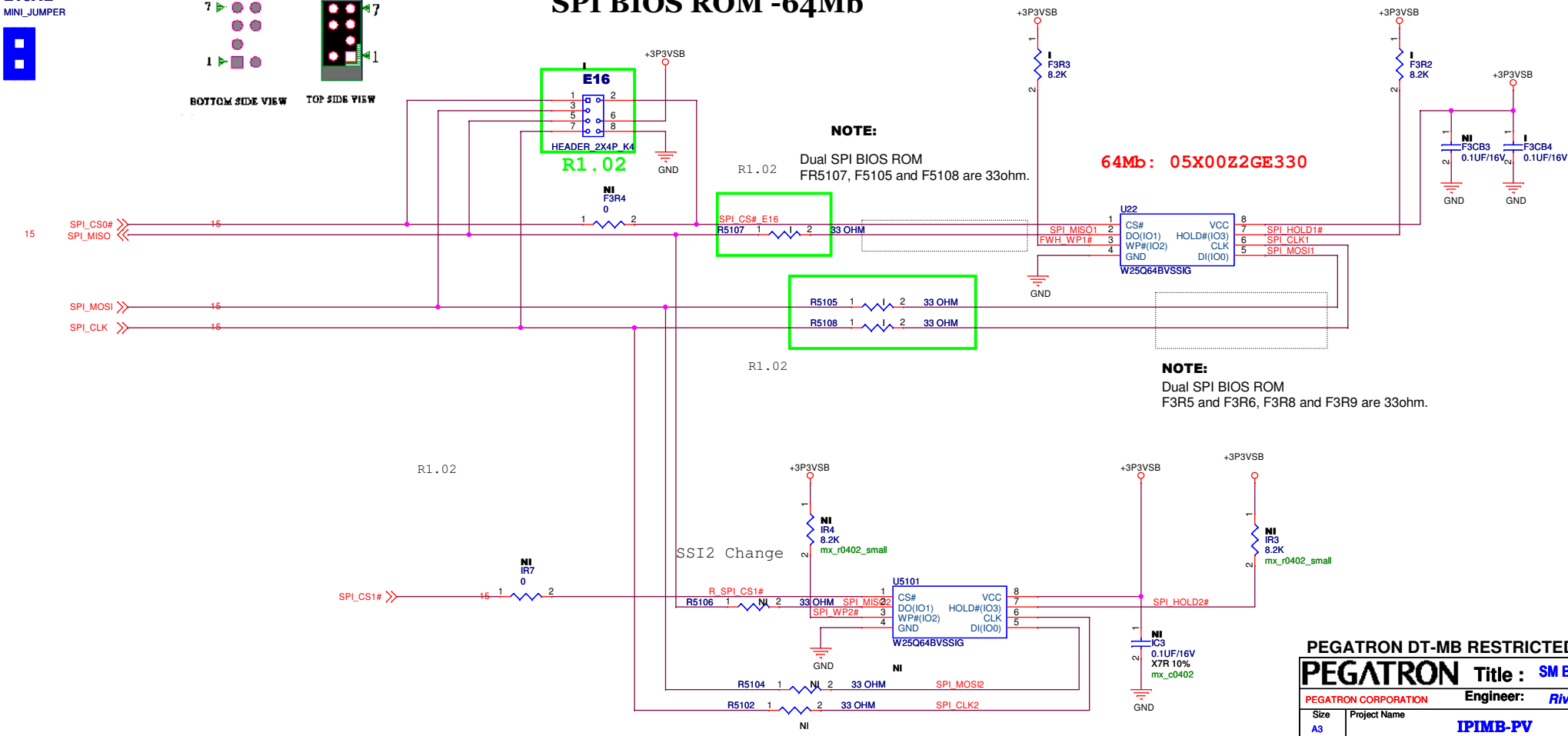
CRB is 8.2Kohm



I
E16:12
MINI_JUMPER



SPI BIOS ROM -64Mb



PEGATRON DT-MB RESTRICTED SECRET

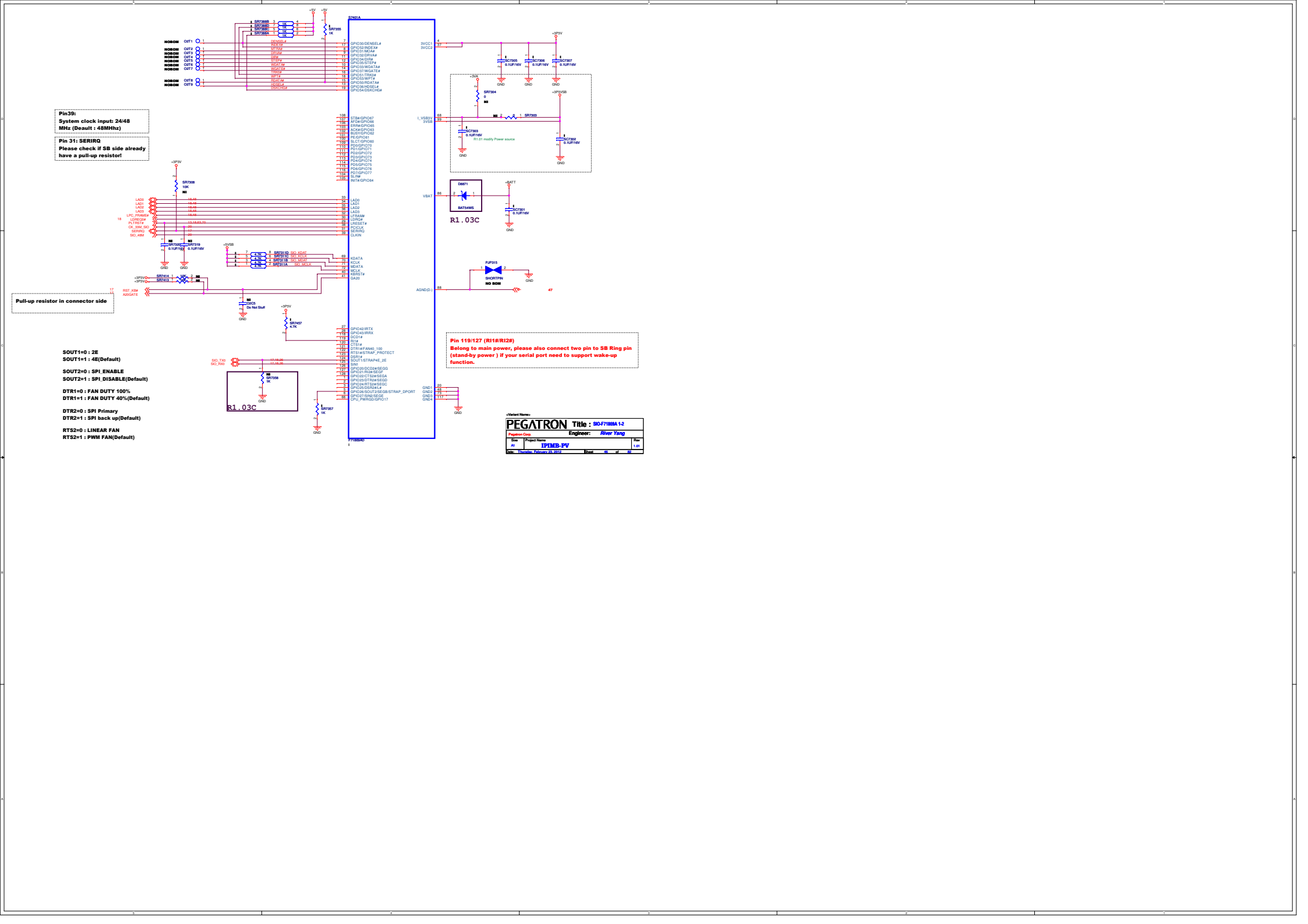
PEGATRON CORPORATION

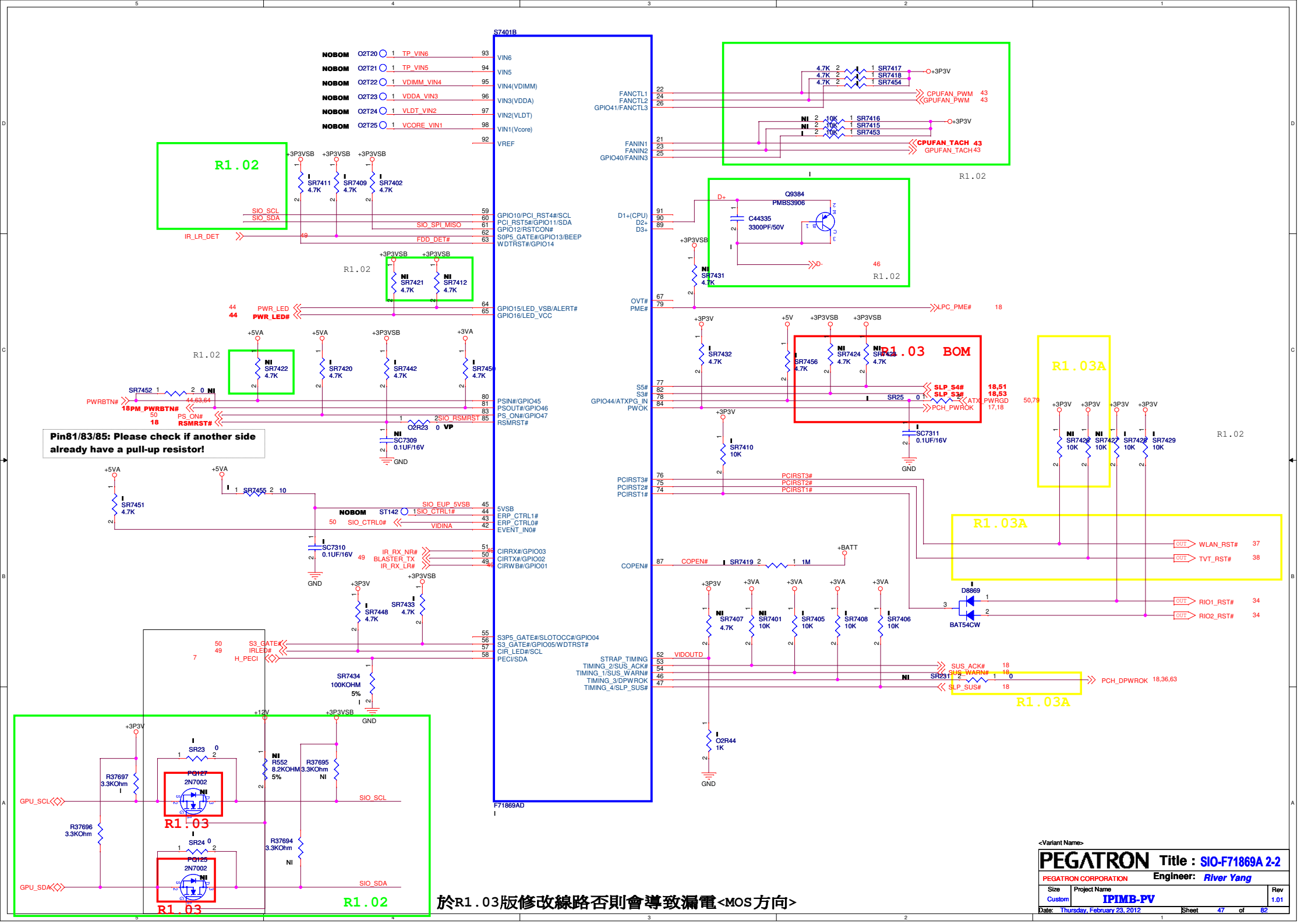
Title : SM BUS & SPI ROM

Engineer: River Yang

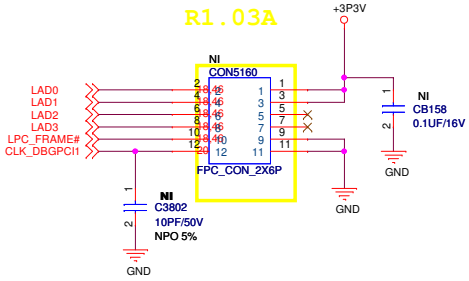
Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 45 of 71


Pin39:
System clock input: 24/48
MHz (Deault : 48MHhz)
Pin 31: SERIRQ
Please check if SB side already
have a pull-up resistor!
Pull-up resistor in connector side
SOUT1=0 : 2E
SOUT1=1 : 4E(Default)
SOUT2=0 : SPI_ENABLE
SOUT2=1 : SPI_DISABLE(Default)
DTR1=0 : FAN DUTY 100%
DTR1=1 : FAN DUTY 40%(Default)
DTR2=0 : SPI Primary
DTR2=1 : SPI back up(Default)
RTS2=0 : LINEAR FAN
RTS2=1 : PWM FAN(Default)
Pin 119/127 (R11#/RI2#)
Belong to main power, please also connect two pin to SB Ring pin
(stand-by power) if your serial port need to support wake-up
function.
R1.03C
R1.01 modify Power source
BAT54WS
SHORTPIN
NO BOM
PEGATRON
Title : SIO-F71889A 1-2
Engineer: River Yang
Pegatron Corp.
IPIMB-PV
Thursday, February 23, 2012


S7401B
F71869AD
R1.02
R1.03
R1.03A
R1.03 BOM
Pin81/83/85: Please check if another side already have a pull-up resistor!
於R1.03版修改線路否則會導致漏電<MOS方向>
PEGATRON
Title : SIO-F71869A 2-2
PEGATRON CORPORATION
Engineer: River Yang
Size: Custom
Project Name: IPIMB-PV
Rev: 1.01
Date: Thursday, February 23, 2012
Sheet 47 of 82

Debug Card CON



<Variant Name>

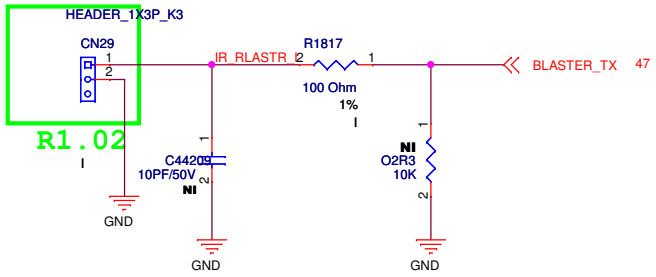
PEGATRON Title : LPC DEBUG

PEGATRON CORPORATION Engineer: River Yang

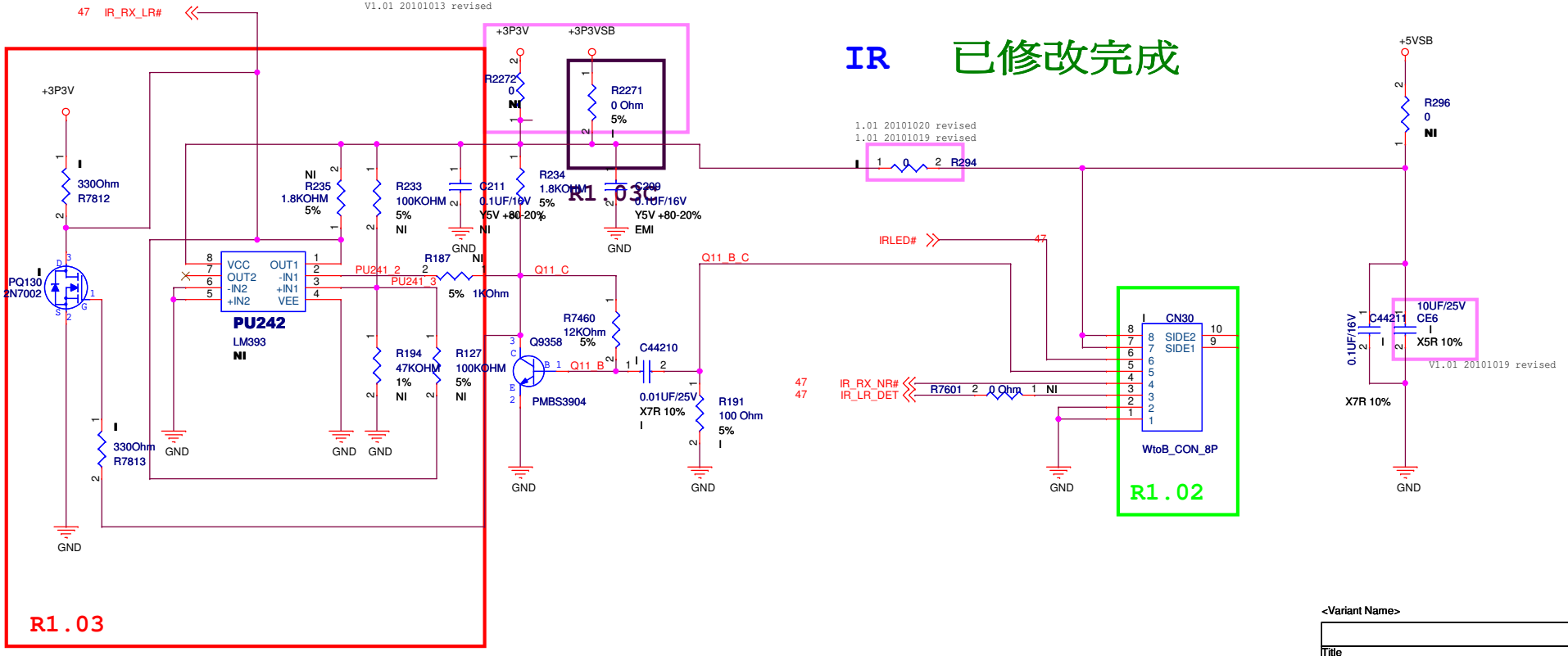
Size	Project Name	Rev
Custom	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 48 of 82

線條未改　　IR Blaster

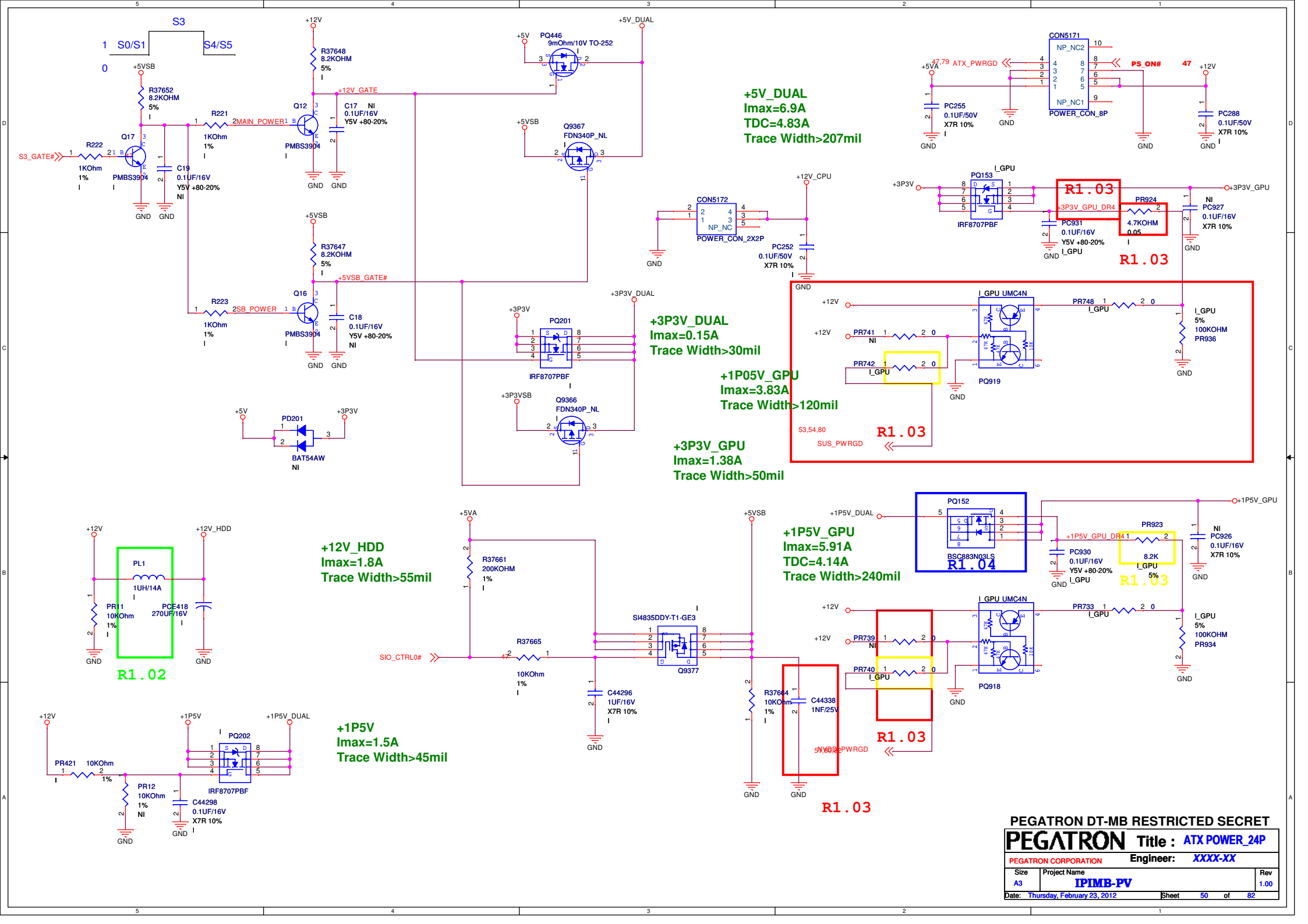


IR　已修改完成



<Variant Name>

Title	IR/IR BLASTER	
Size B	Document Number IPIMB-OP	Rev <RevCode>
Date: Thursday, February 23, 2012	Sheet 49 of 88	


S3
1 S0/S1 S4/S5
0
+5VSB
R37652
8.2KOHM
5%
R222
1KOhm
1%
PMBS3904
Q17
S3_GATE#
C19
0.1UF/16V
Y5V +80-20%
NI
GND
R221
1KOhm
1%
2MAIN_POWER1
Q12
+12V
R37648
8.2KOHM
5%
+12V_GATE
C17 NI
0.1UF/16V
Y5V +80-20%
+5V
PQ446
9mOhm/10V TO-252
+5V_DUAL
+5VSB
Q9367
FDN340P_NL
R37647
8.2KOHM
5%
+5VSB_GATE#
R223
1KOhm
1%
2SB_POWER
Q16
C18
0.1UF/16V
Y5V +80-20%
NI
+3P3V
PQ201
IRF8707PBF
+3P3V_DUAL
+3P3VSB
Q9366
FDN340P_NL
+5V
PD201
BAT54AW
NI
+3P3V
+5V_DUAL
Imax=6.9A
TDC=4.83A
Trace Width>207mil
+3P3V_DUAL
Imax=0.15A
Trace Width>30mil
+1P05V_GPU
Imax=3.83A
Trace Width>120mil
+3P3V_GPU
Imax=1.38A
Trace Width>50mil
+12V_HDD
Imax=1.8A
Trace Width>55mil
+1P5V
Imax=1.5A
Trace Width>45mil
+1P5V_GPU
Imax=5.91A
TDC=4.14A
Trace Width>240mil
CON5171
NP_NC2
NP_NC1
POWER_CON_8P
47.79 ATX_PWRGD
PS_ON#
47
PC255
0.1UF/50V
X7R 10%
PC288
0.1UF/50V
X7R 10%
CON5172
NP_NC
POWER_CON_2X2P
+12V_CPU
PC252
0.1UF/50V
X7R 10%
I_GPU
PQ153
IRF8707PBF
R1.03
+3P3V_GPU_DR4
PR924
4.7KOHM
0.05
PC931
0.1UF/16V
Y5V +80-20%
NI
PC927
0.1UF/16V
X7R 10%
I_GPU UMC4N
PQ919
PR748
PR741
NI
PR742
I_GPU
PR936
100KOHM
53,54,80
SUS_PWRGD
PL1
1UH/14A
PR11
10KOhm
1%
PCE418
270UF/16V
R1.02
R37661
200KOHM
1%
SIO_CTRL0#
R37665
10KOhm
1%
SI4835DDY-T1-GE3
Q9377
C44296
1UF/16V
X7R 10%
PQ152
BSC883N03LS
R1.04
+1P5V_GPU_DR4
PR923
8.2K
5%
PC930
0.1UF/16V
Y5V +80-20%
PC926
0.1UF/16V
X7R 10%
PR733
PR739
PR740
PQ918
PR934
R37664
10KOhm
1%
C44338
1NF/25V
SUS_PWRGD
PR421
10KOhm
1%
PQ202
IRF8707PBF
PR12
10KOhm
1%
NI
C44298
0.1UF/16V
X7R 10%
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : ATX POWER_24P
PEGATRON CORPORATION
Engineer: XXXX-XX
Size A3
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
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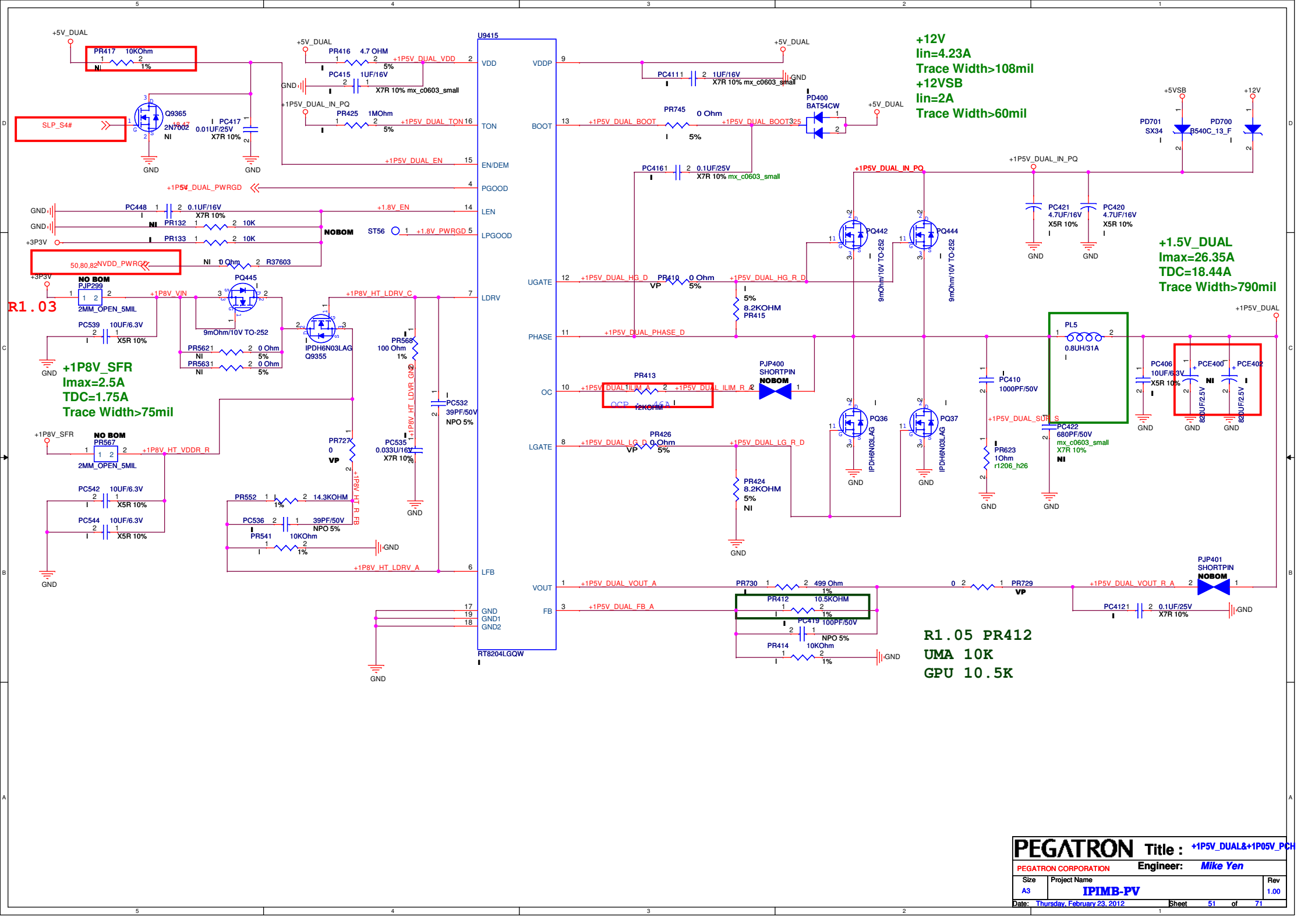
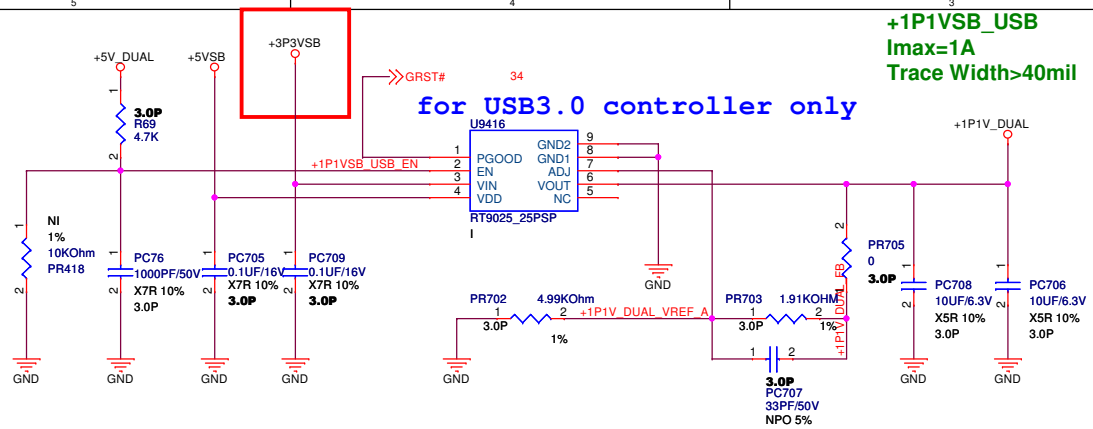
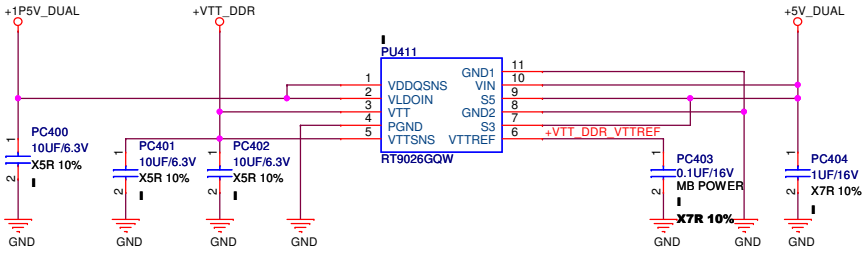
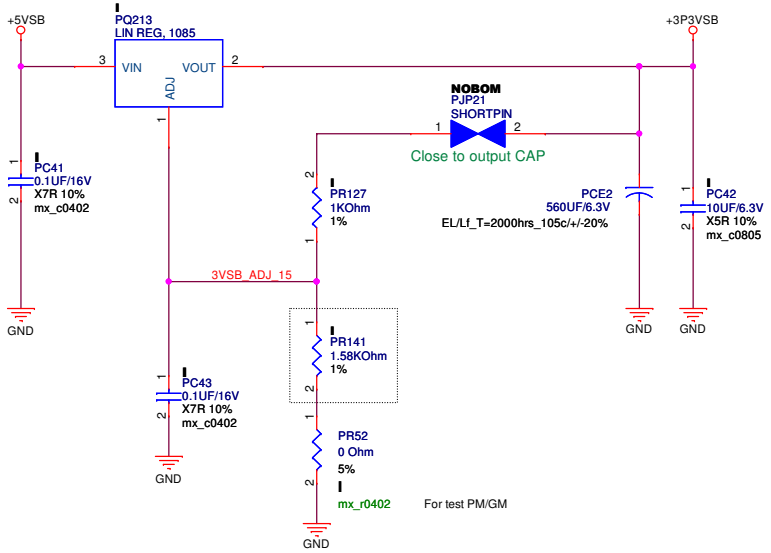
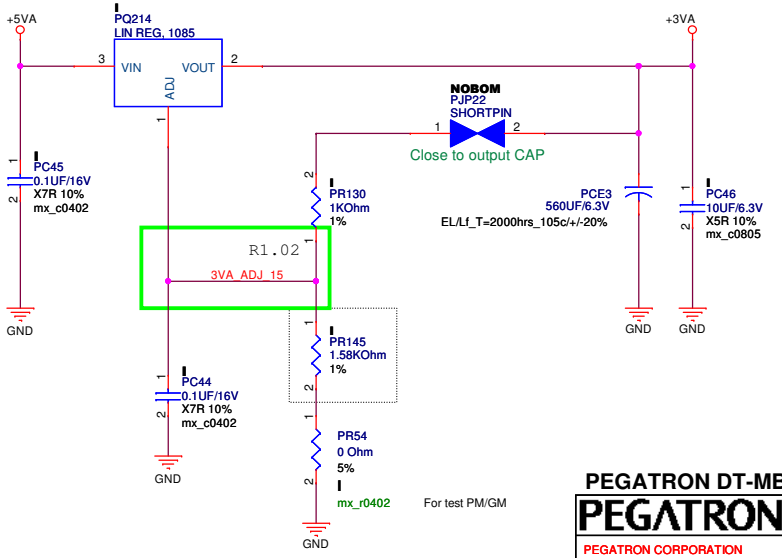

+12V
Iin=4.23A
Trace Width>108mil
+12VSB
Iin=2A
Trace Width>60mil
+1.5V_DUAL
Imax=26.35A
TDC=18.44A
Trace Width>790mil
+1P8V_SFR
Imax=2.5A
TDC=1.75A
Trace Width>75mil
R1.03
R1.05 PR412
UMA 10K
GPU 10.5K
U9415
RT8204LGQW
PEGATRON
Title : +1P5V_DUAL&+1P05V_PCH
PEGATRON CORPORATION
Engineer: Mike Yen
Size A3
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
Sheet 51 of 71







+3P3VSB
Imax=1.88A



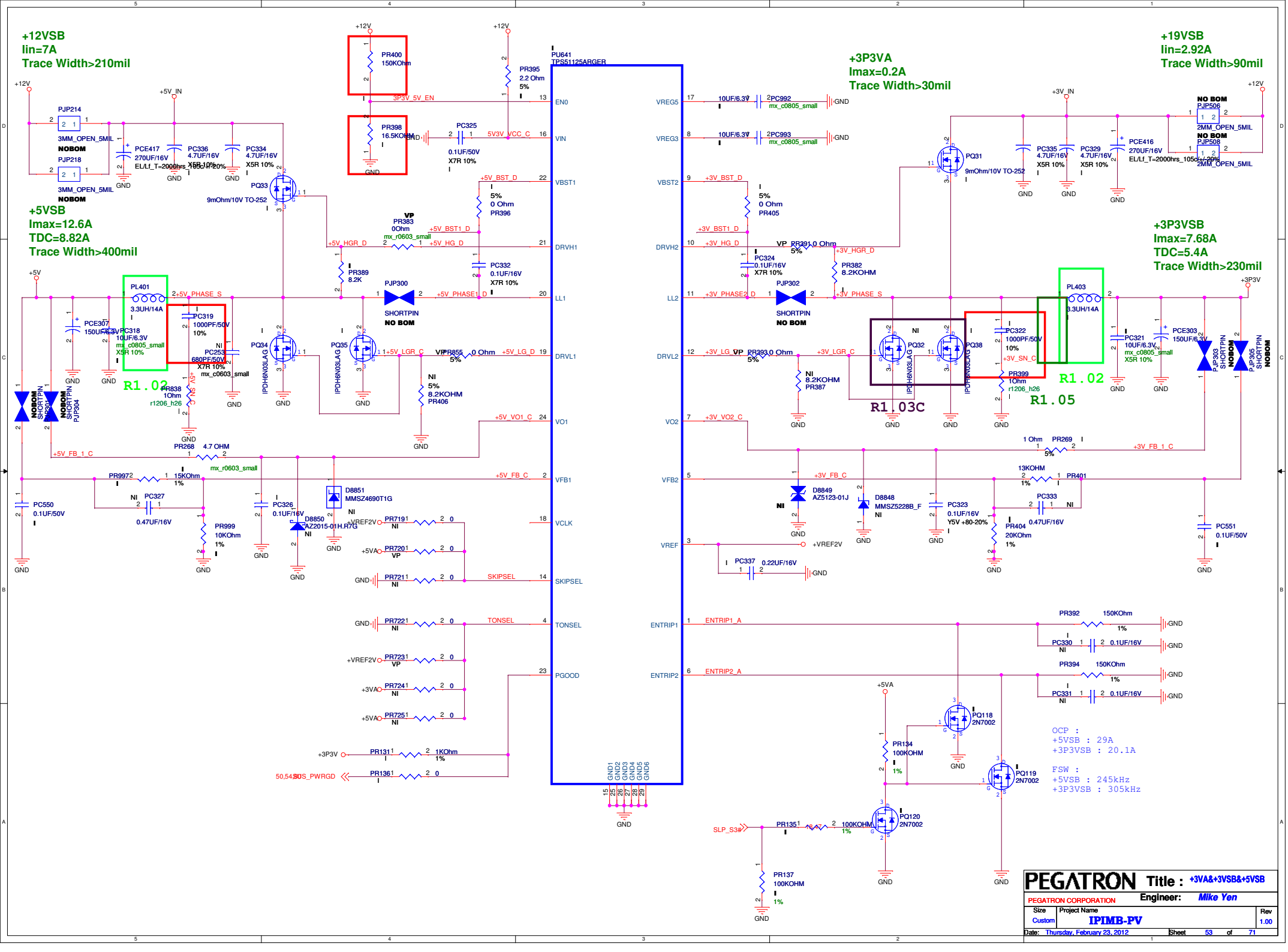
PEGATRON DT-MB RESTRICTED SECRET

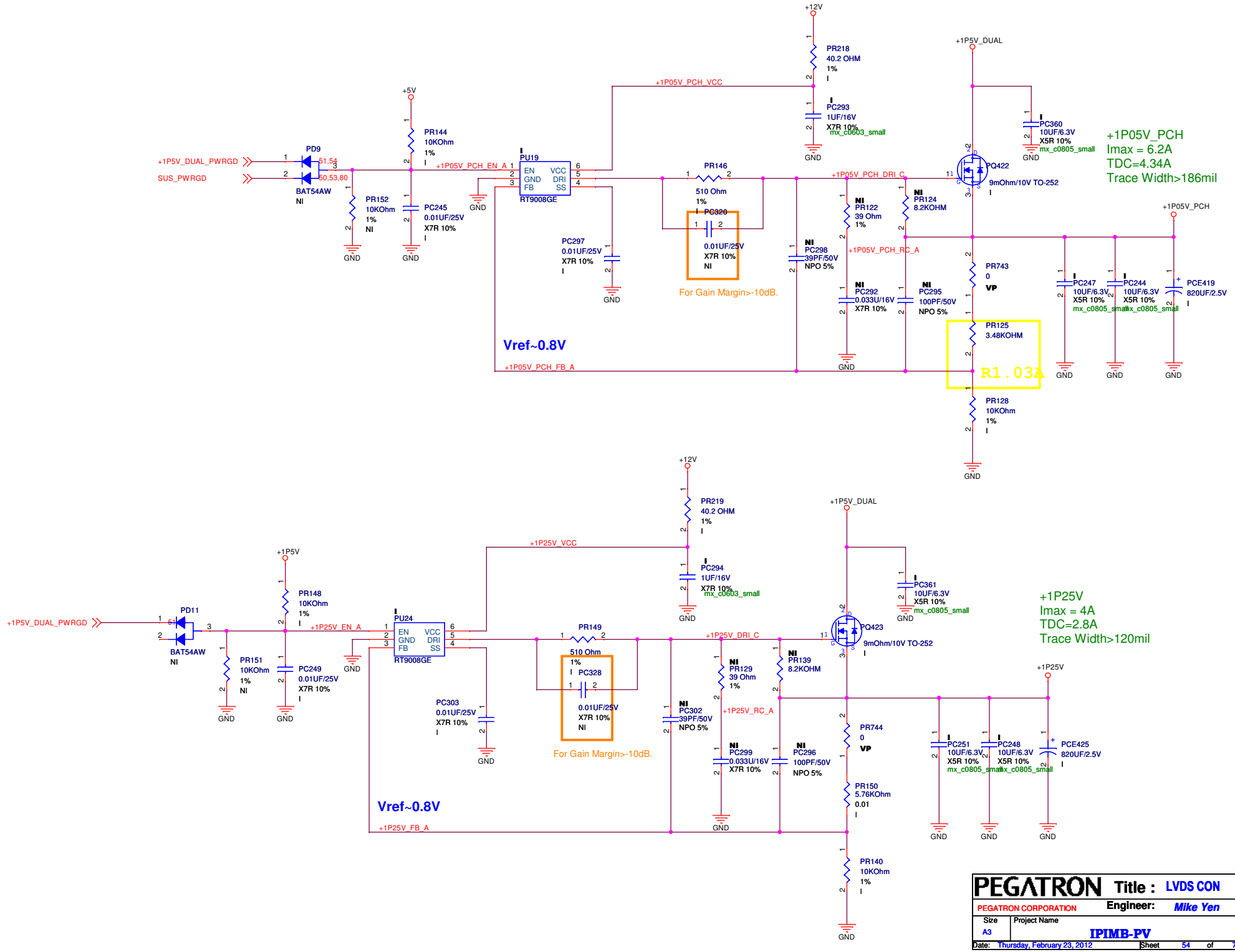
PEGATRON Title : N/A

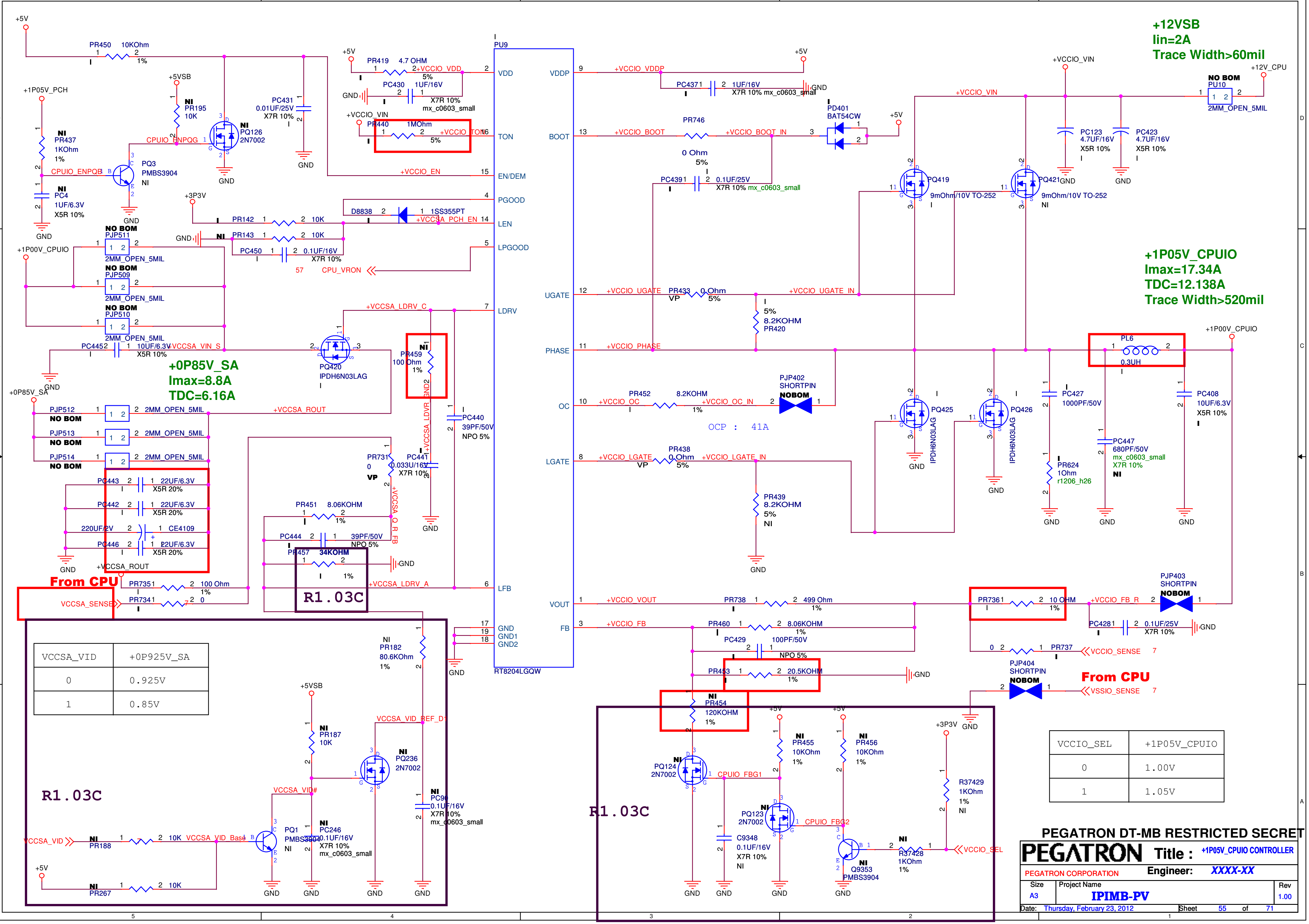
PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPIMB-PV	1.00

Date: Thursday, February 23, 2012 Sheet 52 of 82


+12VSB
Iin=7A
Trace Width>210mil
+5VSB
Imax=12.6A
TDC=8.82A
Trace Width>400mil
+3P3VA
Imax=0.2A
Trace Width>30mil
+19VSB
Iin=2.92A
Trace Width>90mil
+3P3VSB
Imax=7.68A
TDC=5.4A
Trace Width>230mil
PU641
TPS51125ARGER
EN0
VIN
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
VCLK
SKIPSEL
TONSEL
PGOOD
VREG5
VREG3
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
VREF
ENTRIP1
ENTRIP2
GND1
GND2
GND3
GND4
GND5
GND6
R1.02
R1.03C
R1.05
OCP :
+5VSB : 29A
+3P3VSB : 20.1A
FSW :
+5VSB : 245kHz
+3P3VSB : 305kHz
PEGATRON
Title : +3VA&+3VSB&+5VSB
PEGATRON CORPORATION
Engineer: Mike Yen
Size Custom
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
Sheet 53 of 71


+1P05V_PCH
Imax = 6.2A
TDC=4.34A
Trace Width>186mil
Vref~0.8V
For Gain Margin>-10dB.
R1.03A
+1P25V
Imax = 4A
TDC=2.8A
Trace Width>120mil
Vref~0.8V
For Gain Margin>-10dB.
PEGATRON
Title : LVDS CON
PEGATRON CORPORATION
Engineer: Mike Yen
Size A3
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
Sheet 54 of 71



VCCSA_VID	+0P925V_SA
0	0.925V
1	0.85V

VCCIO_SEL	+1P05V_CPUIO
0	1.00V
1	1.05V

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON

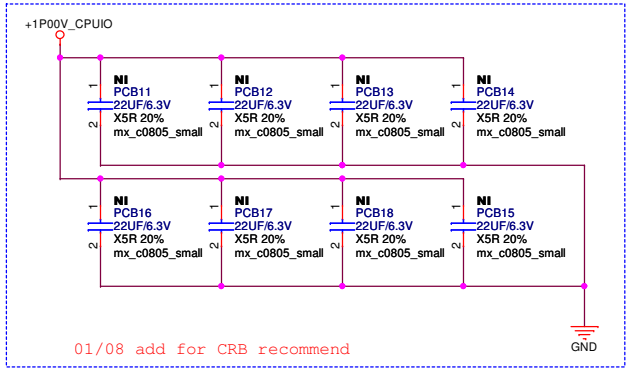
PEGATRON CORPORATION

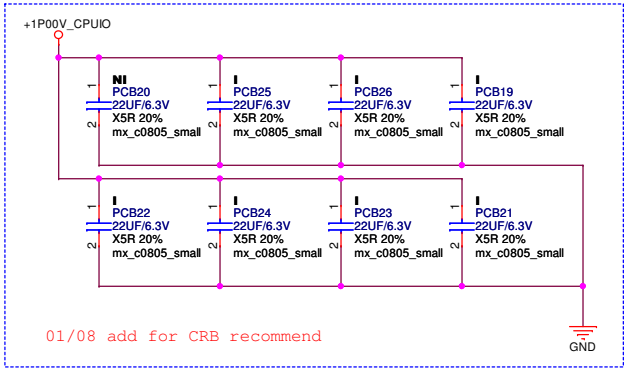
Title : +1P05V_CPUIO CONTROLLER

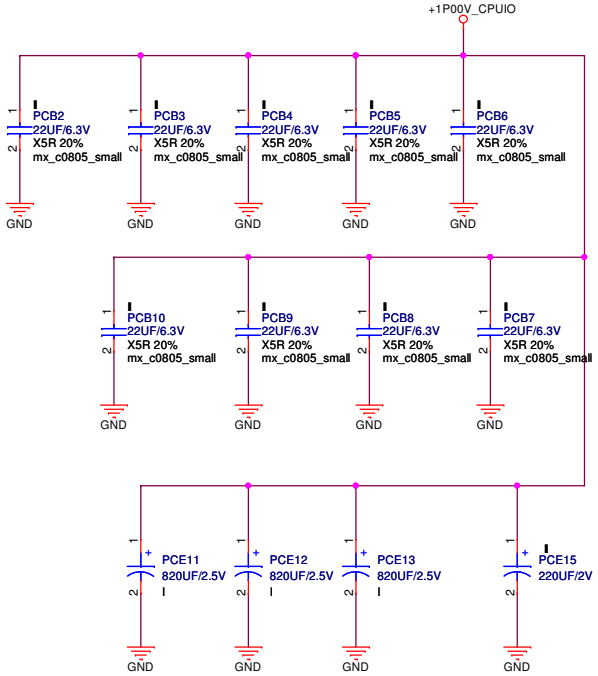
Engineer: XXXX-XX

Size A3 | Project Name IPIMB-PV | Rev 1.00

Date: Thursday, February 23, 2012 | Sheet 55 of 71







Place close to CPU bottom side

VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P05V_CPUIO CAP

PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPIMB-PV	1.00

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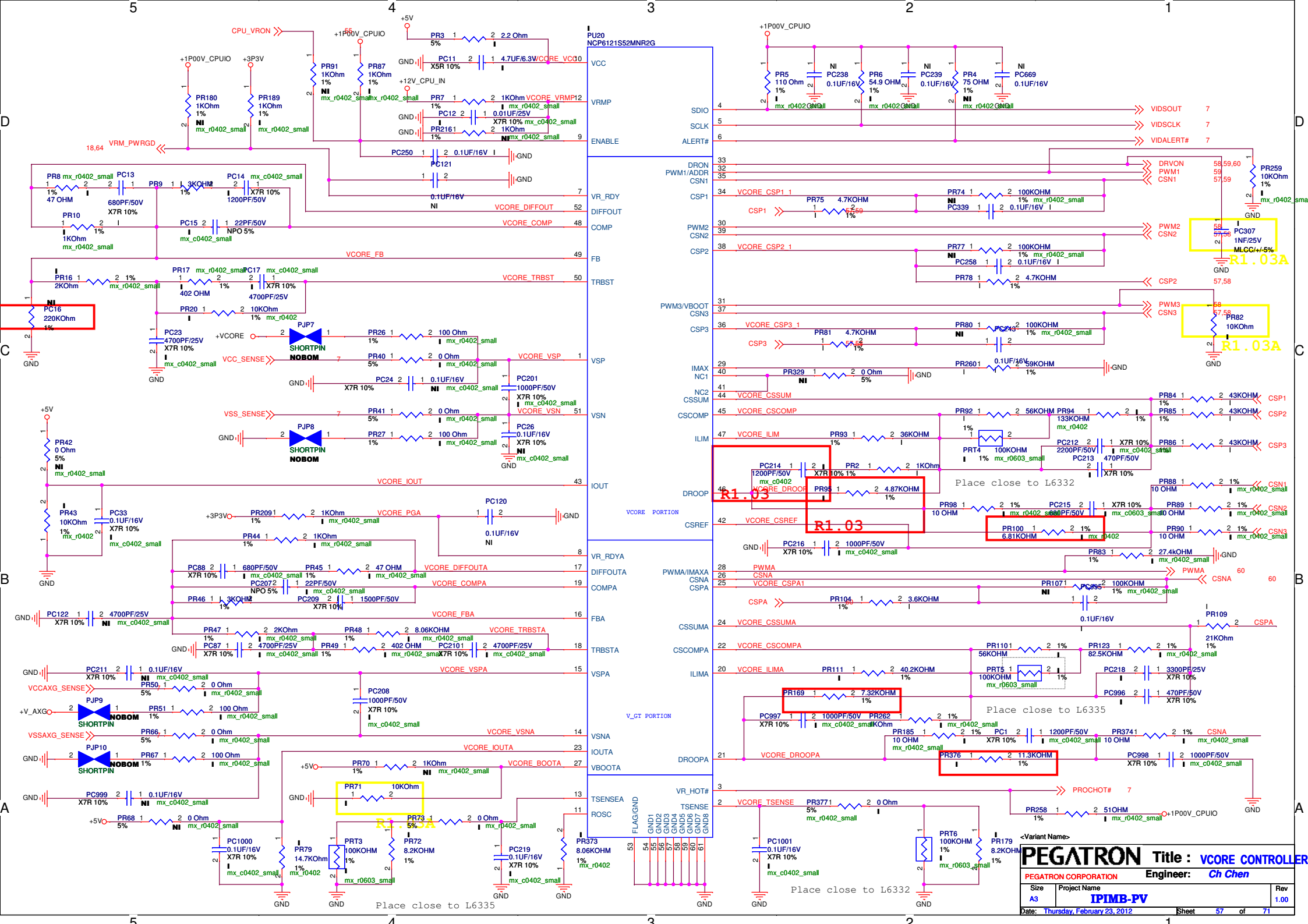
PU20
NCP6121S52MNR2G
VCC
VRMP
ENABLE
VR_RDY
DIFFOUT
COMP
FB
TRBST
VSP
VSN
IOUT
VR_RDYA
DIFFOUTA
COMPA
FBA
TRBSTA
VSPA
VSNA
IOUTA
VBOOTA
TSENSEA
ROSC
FLAG/GND
SDIO
SCLK
ALERT#
DRON
PWM1/ADDR
CSN1
CSP1
PWM2
CSN2
CSP2
PWM3/VBOOT
CSN3
CSP3
IMAX
NC1
NC2
CSSUM
CSCOMP
ILIM
DROOP
CSREF
PWMA/IMAXA
CSNA
CSPA
CSSUMA
CSCOMPA
ILIMA
DROOPA
VR_HOT#
TSENSE
VCORE PORTION
V_GT PORTION
Place close to L6335
Place close to L6332
R1.03
R1.03A
PEGATRON
Title : VCORE CONTROLLER
PEGATRON CORPORATION
Engineer: Ch Chen
Size A3
Project Name IPIMB-PV
Rev 1.00
Date: Thursday, February 23, 2012
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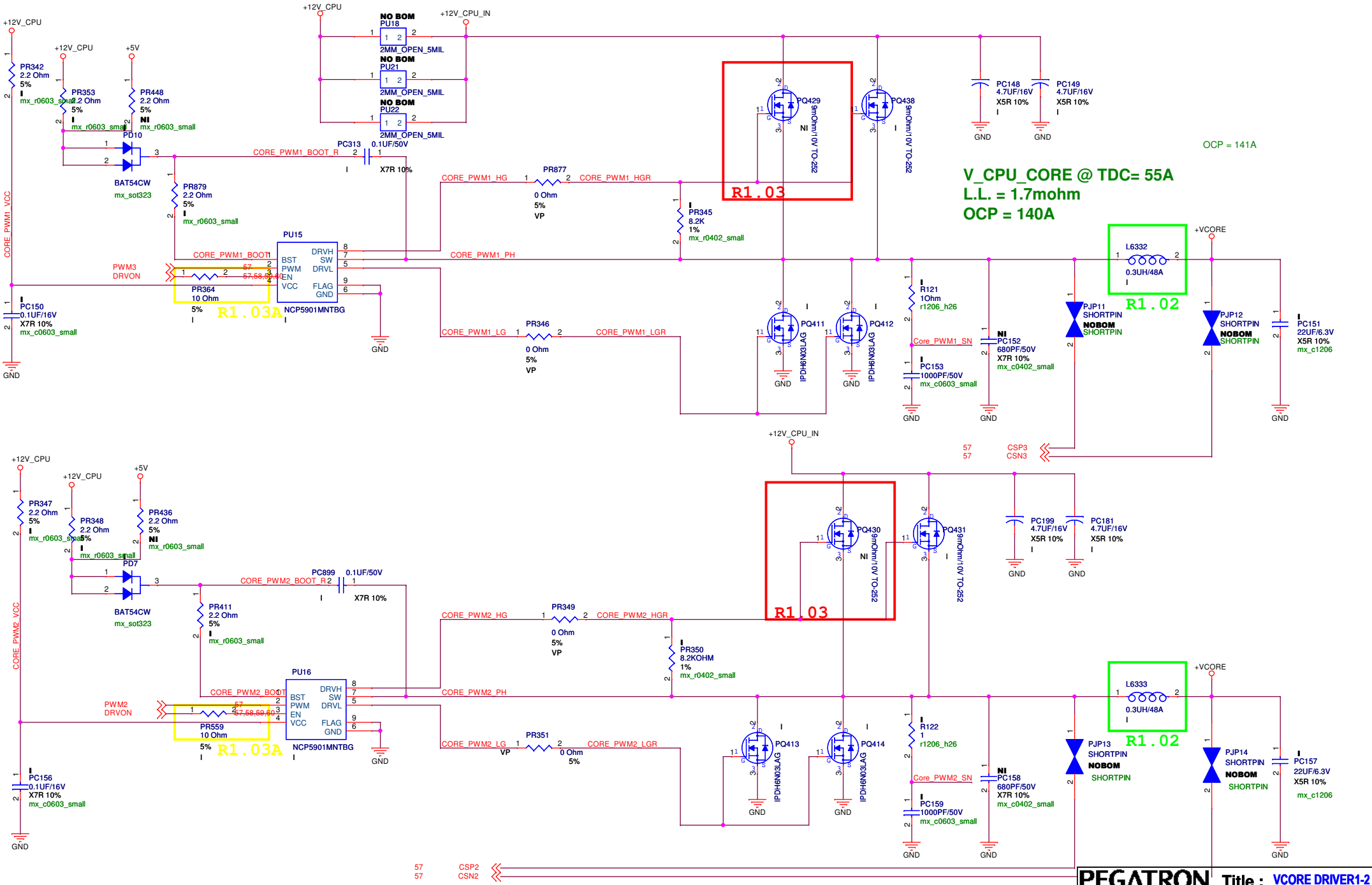

PEGATRON Title : VCORE DRIVER1-2

PEGATRON BT-MB RESTRICTED SECRET

Pegatron Corp. Engineer: xxxx-xx

Size	Project Name	Rev
A3	IPIMB-PV	1.00

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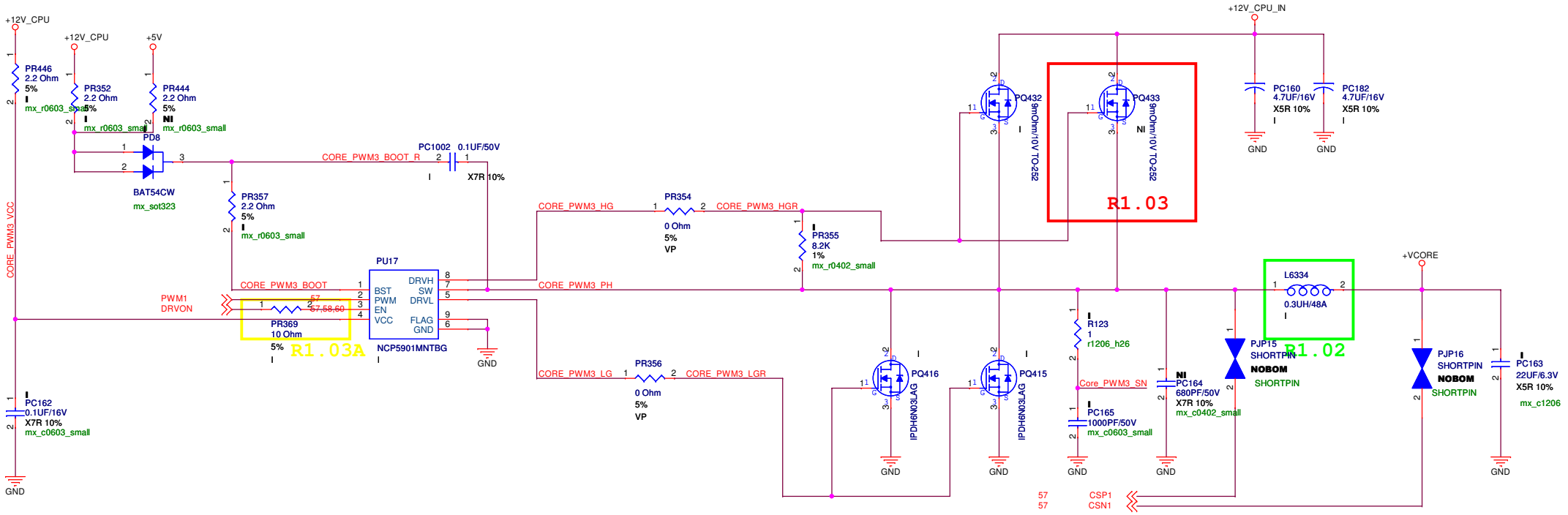
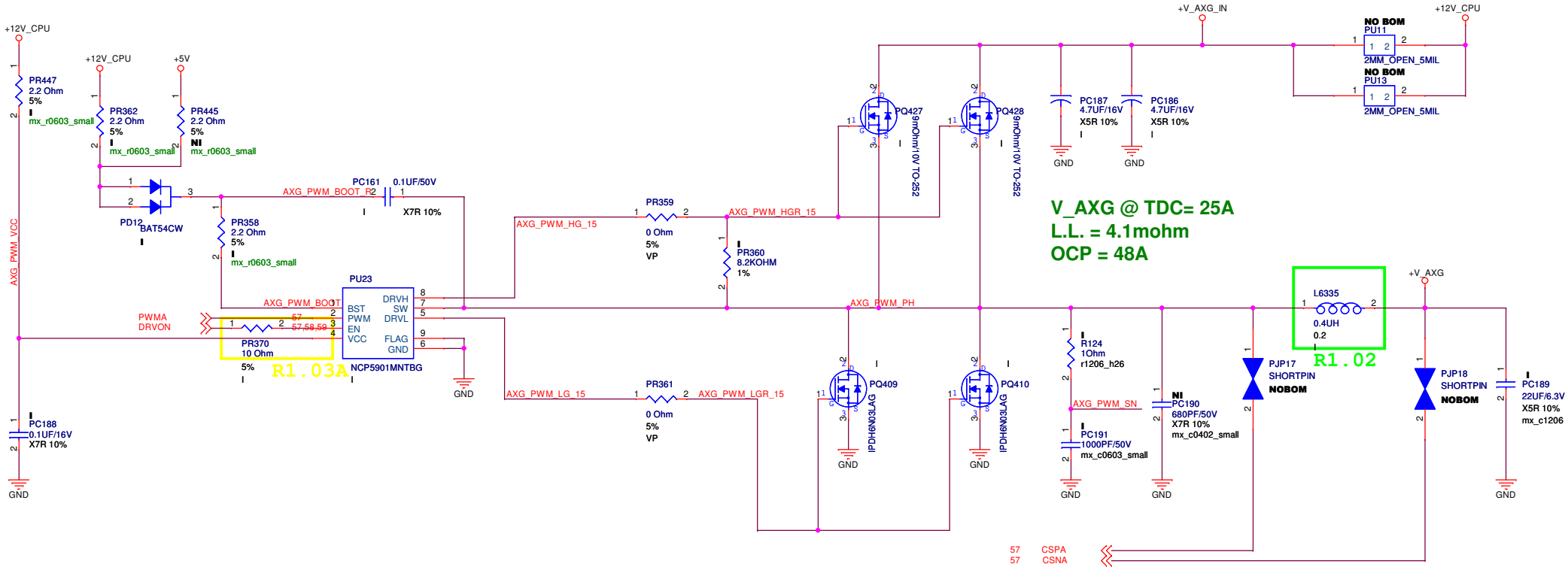


PEGATRON DT-MB RESTRICTED SECRET

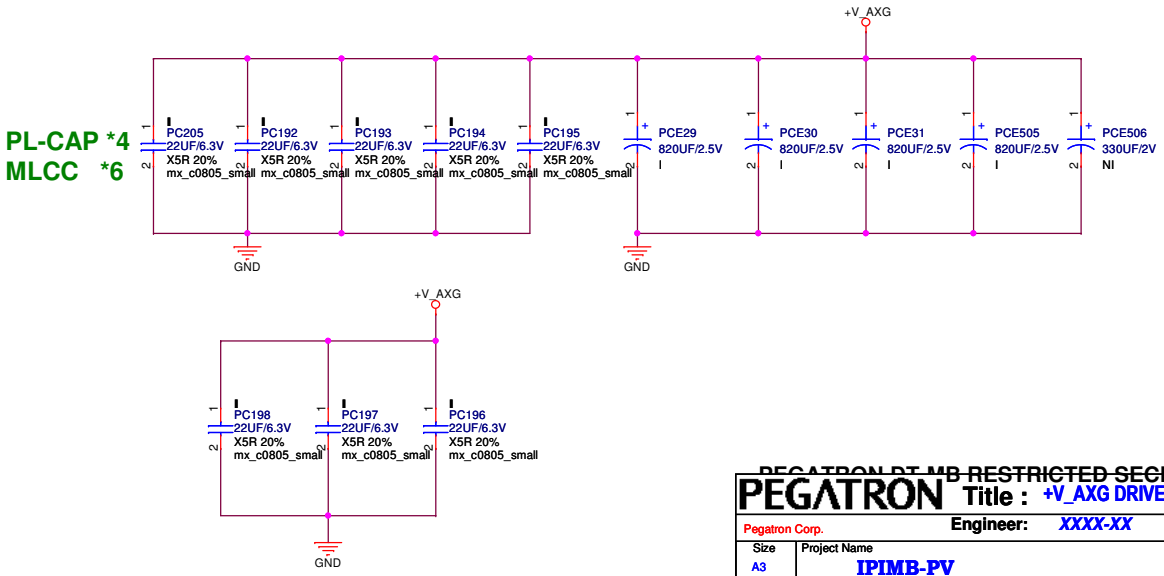
PEGATRON Pegatron Corp.	Title : VCORE DRIVER 2-2	
	Engineer: XXXX-XX	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 59 of 71	



Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1



PEGATRON DT MB RESTRICTED SECRET

PEGATRON Title : +V_AXG DRIVER

Pegatron Corp. Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPIMB-PV	1.00

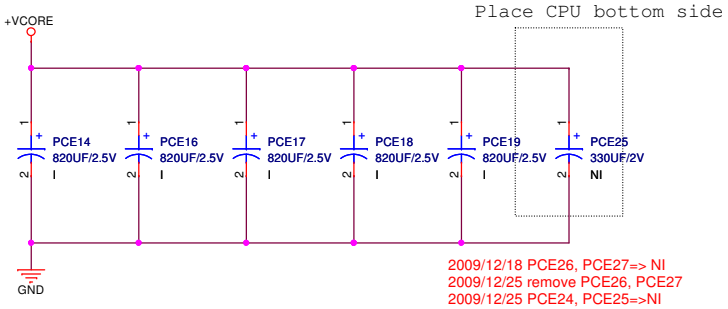
Date: Thursday, February 23, 2012 Sheet 60 of 71

Output CAP

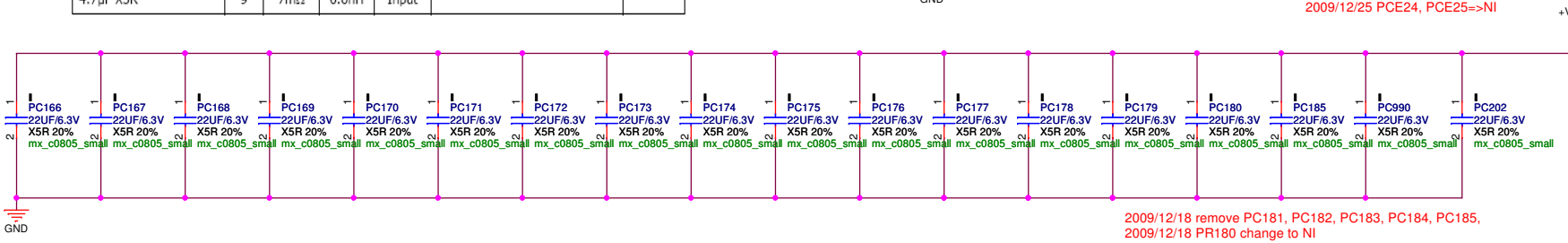
Table 30-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



2009/12/18 PCE26, PCE27=> NI
2009/12/25 remove PCE26, PCE27
2009/12/25 PCE24, PCE25=>NI



2009/12/18 remove PC181, PC182, PC183, PC184, PC185,
2009/12/18 PR180 change to NI
2009/12/21 PR180 change to I
2009/12/21 add PC185, PC199
2009/12/25 add PC200, PC201, PC202,
2009/01/09 remove PC200, PC201

PEGATRON	Title : +VCORE CAP		
PEGATRON CORPORATION	Engineer: TERRY		
Size: A3	Project Name: IPIMB-PV		Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 61 of 71		

PEGATRON

Title : +1P05V_ME

PEGATRON CORPORATION

Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPIMB-PV	1.00

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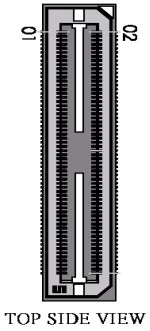
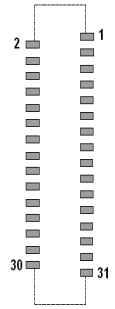
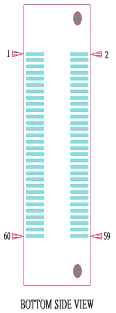
INTEL PCH XDP DEBUG PORT





HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



BOTTOM SIDE VIEW

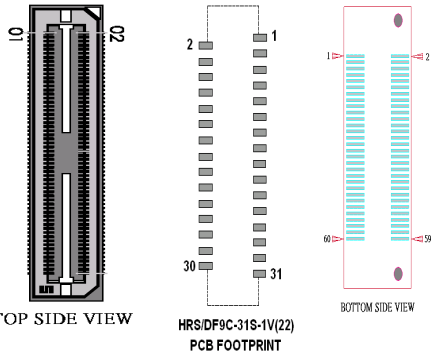
NOTE:
Place strap resistors of TDO near to XDP connector, and TDI and TMS near to CPU.

NOTE:
Place SR214 near to source in order to avoid stub.

R1.03

TBD

PEGATRON	Title : PCH XDP DEBUG	
PEGATRON CORPORATION	Engineer: River Yang	
Size: A3	Project Name: IPIMB-PV	Rev: 1.00
Date: Thursday, February 23, 2012	Sheet 63 of 82	



INTEL CPU XDP DEBUG PORT

NI
XDP1

+1P00V_CPUIO
PROTO HCB20 0.1UF/16V
GND

VCC_OBS_AB
VCC_OBS_CD

TCK1 TCK0 TDO TRSTn TDI TMS → TCK TDO TRST# TDI TMS (7)

+1P00V_CPUIO
NI HR61 1.5K
PROTO HR62
HOOK0 CPUXDP_HOOK0 → CPUPWRGD 18,7

+1P00V_CPUIO
NI HR63 1K
+3VA
NI HR65 1K
PROTO HR66 3.3K
PROTO HR64 1K
PROTO HR67 0

H_PREQ# H_PRDY# BPM0# BPM1# BPM2# BPM3# → OBSFN_A0 OBSFN_A1 OBSDATA_A0 OBSDATA_A1 OBSDATA_A2 OBSDATA_A3

BPM4# BPM5# BPM6# BPM7# → OBSFN_B0 OBSFN_B1 OBSDATA_B0 OBSDATA_B1 OBSDATA_B2 OBSDATA_B3

CK_100M_CPUXDP / CK_100M_CPUXDP# → PROTO HR68 HR69 → CPU_XDPCLK / CPU_XDPCLK# → PROTO HR72 HR73 → CPU_ITPCLK_HOOK4 / CPU_ITPCLK#_HOOK5 → ITPCLK/HOOK4 ITPCLK#/HOOK5

CR_100M_CPU_XDP / CR_100M_CPU_XDP# → NI HR74 HR75

HOOK1 HOOK2 HOOK3 HOOK6/RESET# HOOK7/DBR#
CPUXDP_HOOK1 CPUXDP_HOOK2 CPUXDP_HOOK3
PROTO HR66 PROTO HR64 PROTO HR67
→ PWRBTN# (44,47,63) CPU_CFG0 (7) VRM_PWRGD (18,57) CPURST_XDP# (13,63) SYS_RESET_DBR# (63,7)

SMB_DATA_MAIN (10,11,45,63) → SDA
SMB_CLK_MAIN (10,11,45,63) → SCL

OBSFN_C0 OBSFN_C1 OBSDATA_C0 OBSDATA_C1 OBSDATA_C2 OBSDATA_C3
OBSFN_D0 OBSFN_D1 OBSDATA_D0 OBSDATA_D1 OBSDATA_D2 OBSDATA_D3

GND1–GND18
NP_NC1 NP_NC2 NC
GND

BtoB_CON_60P

NOTE:
CRB is BTM

NOTE:
Please close to each other to reduse stub.

NOTE:
Place HR64 near HR24, reduce stub

R1.03

PEGATRON Title : CPU XDP DEBUG
PEGATRON CORPORATION Engineer: River Yang
Size A3 | Project Name IPIMB-PV | Rev 1.00
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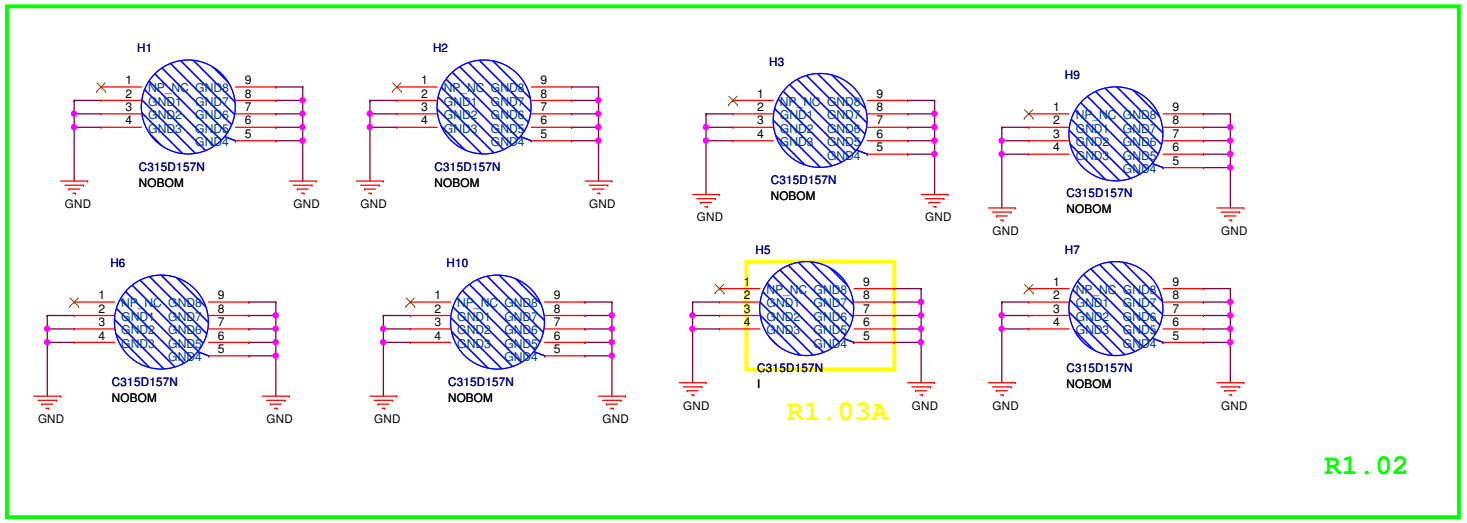
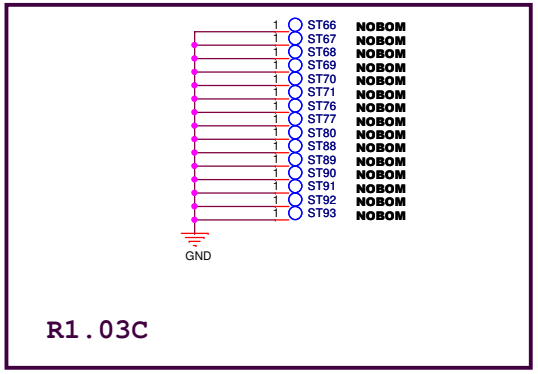
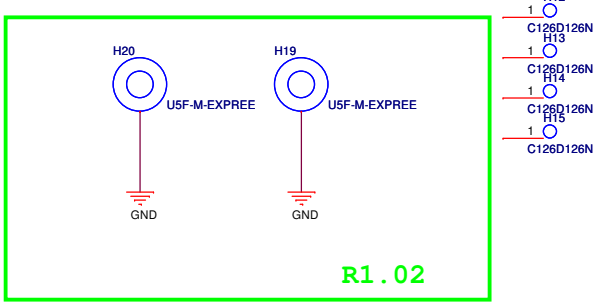
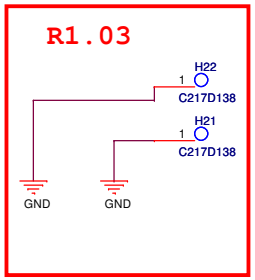


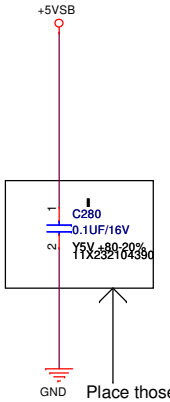




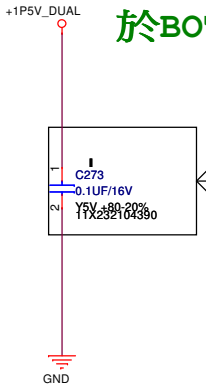


VESA mount hole

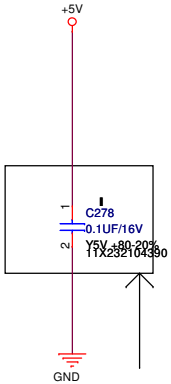
於BOTTOM LAYER 上



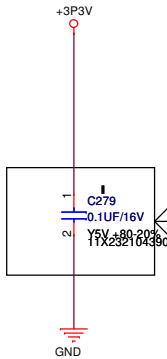
NOTE:
Place those cap close to CON5169



NOTE:
Place those cap close to U9415



NOTE:
Place those cap close to PU641



NOTE:
Place those cap close to PU641

<Variant Name>

PEGATRON Title : SCREW HOLE

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.00

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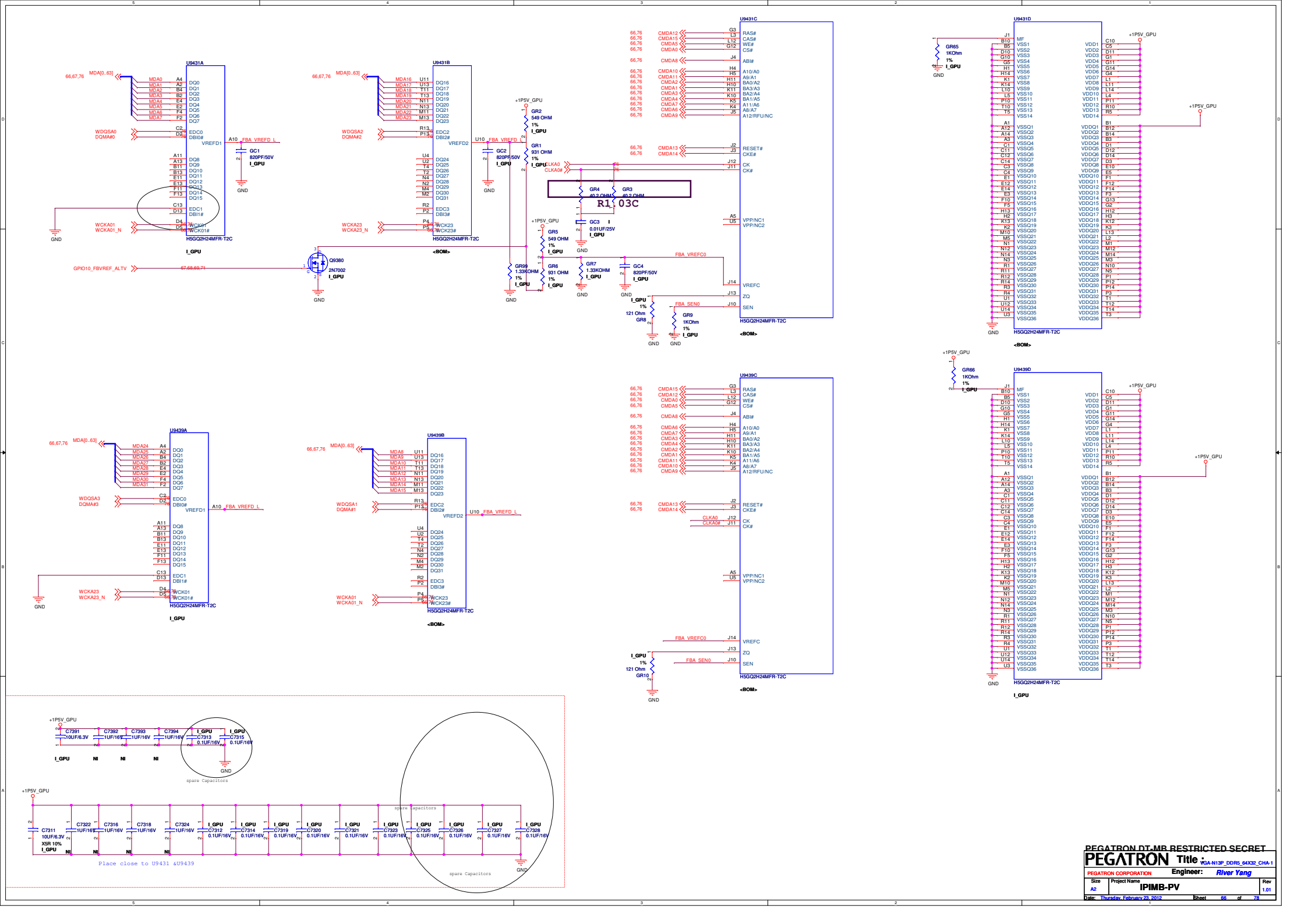

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON CORPORATION

Title : VGA-N13P_DDR5_64X32_CHA-1

Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

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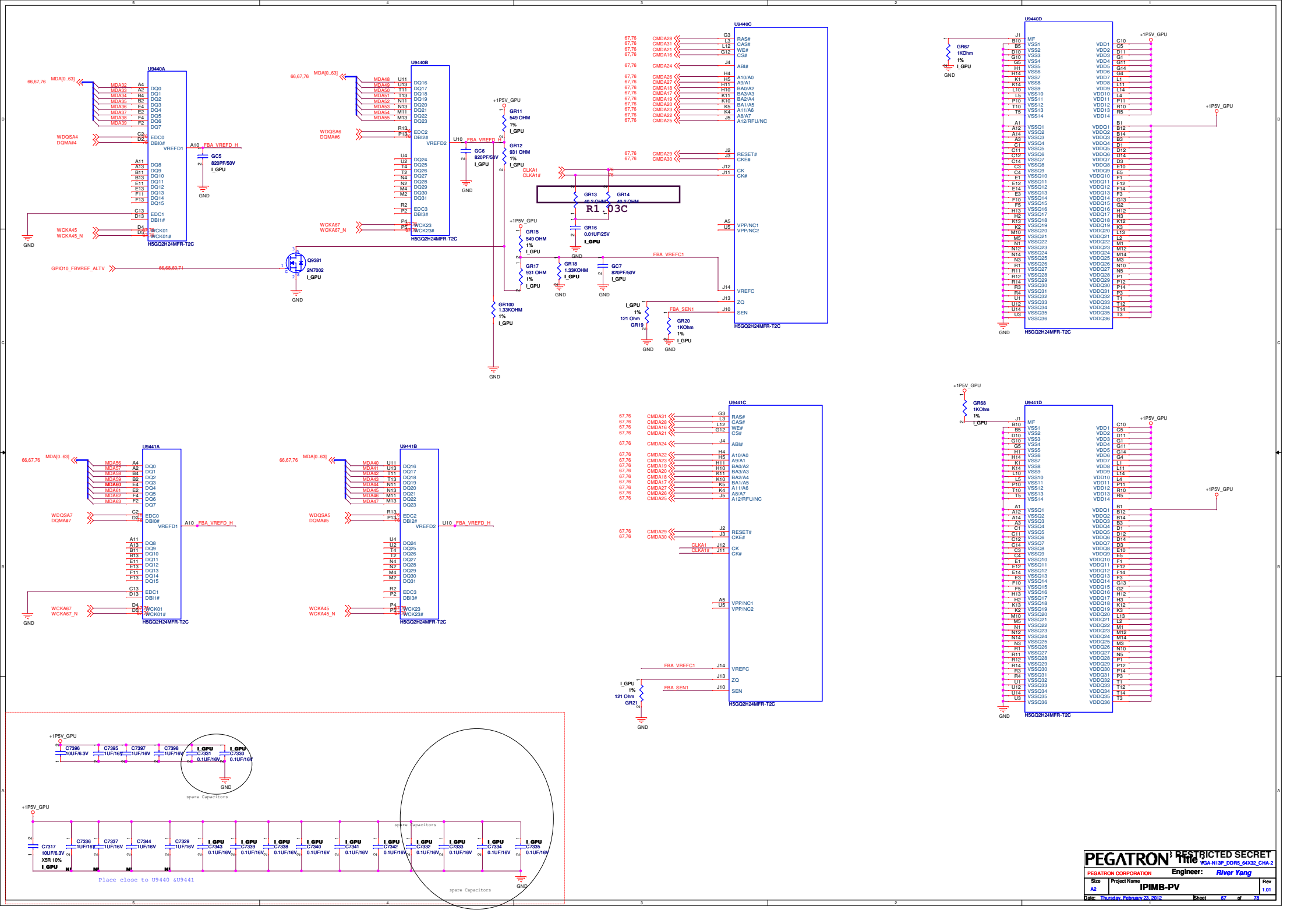


PEGATRON

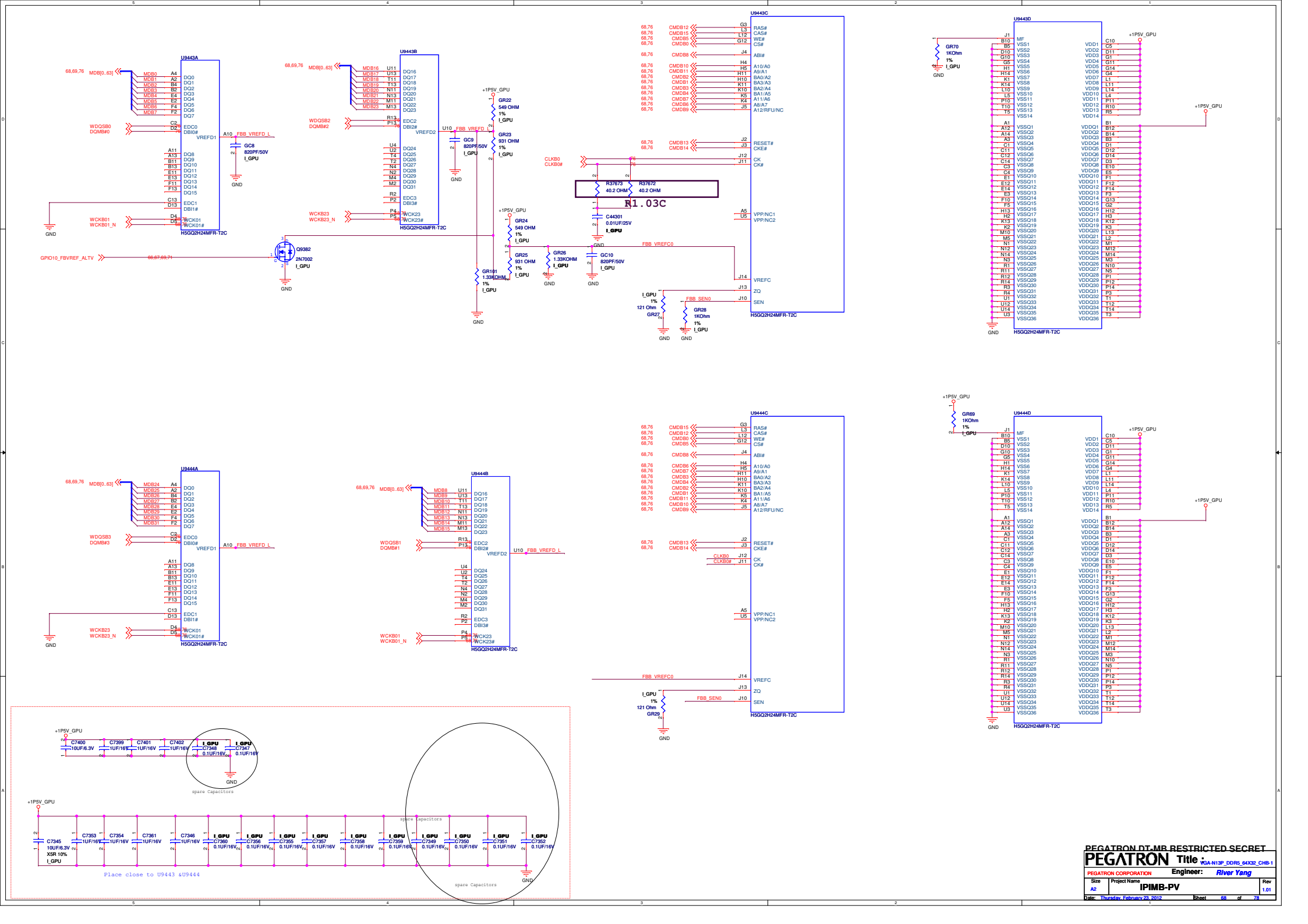
Title: VGA-N13P_DDR5_64X32_CHA-2

PEGATRON CORPORATION

Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

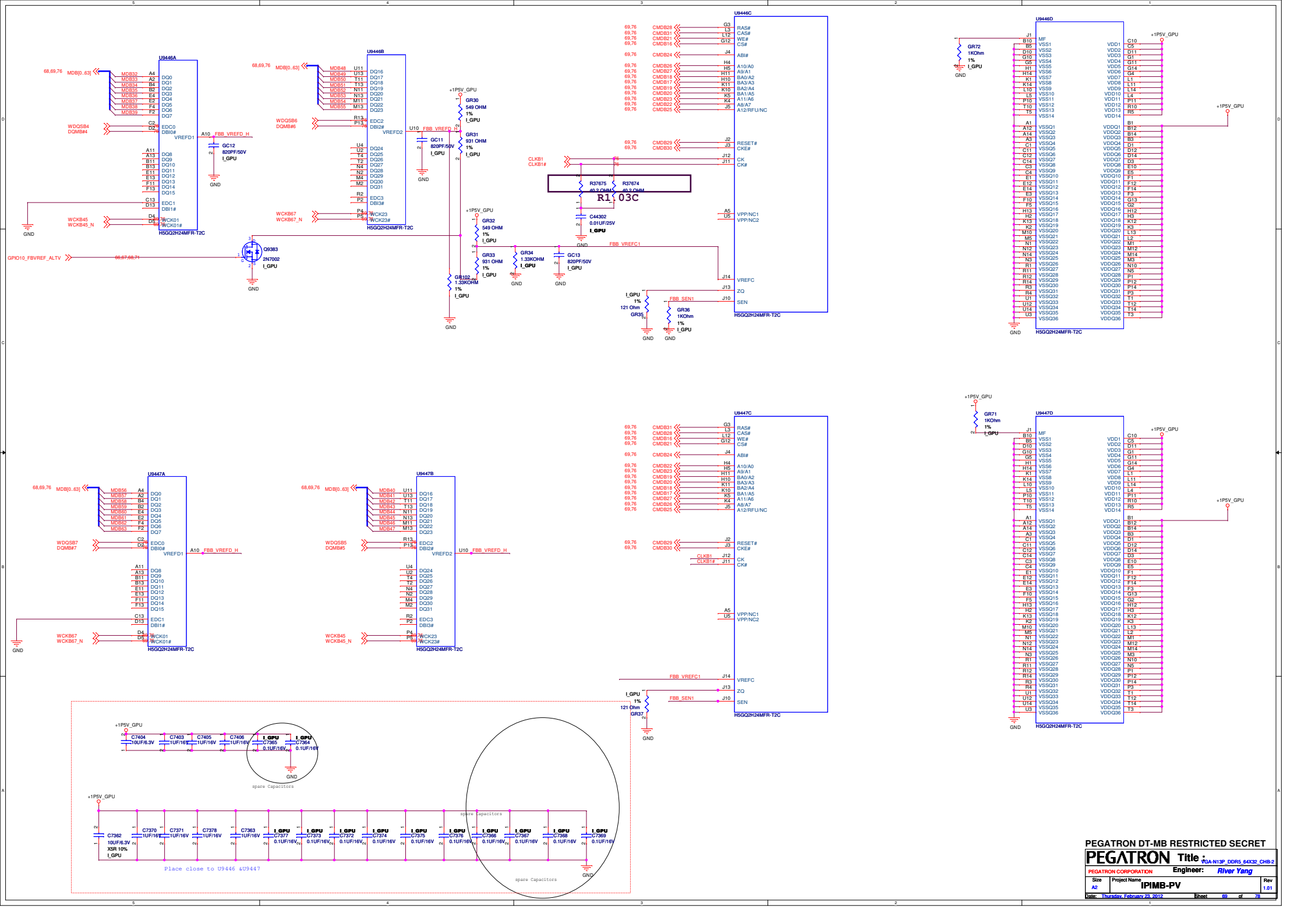
Date: Thursday, February 23, 2012 Sheet 67 of 78



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : YGA-N13P_DDR5_64X32_CHB-1

Date: Thursday, February 23, 2012



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON CORPORATION

Title * VGA-N13P_DDR5_64X32_CHB-2

Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

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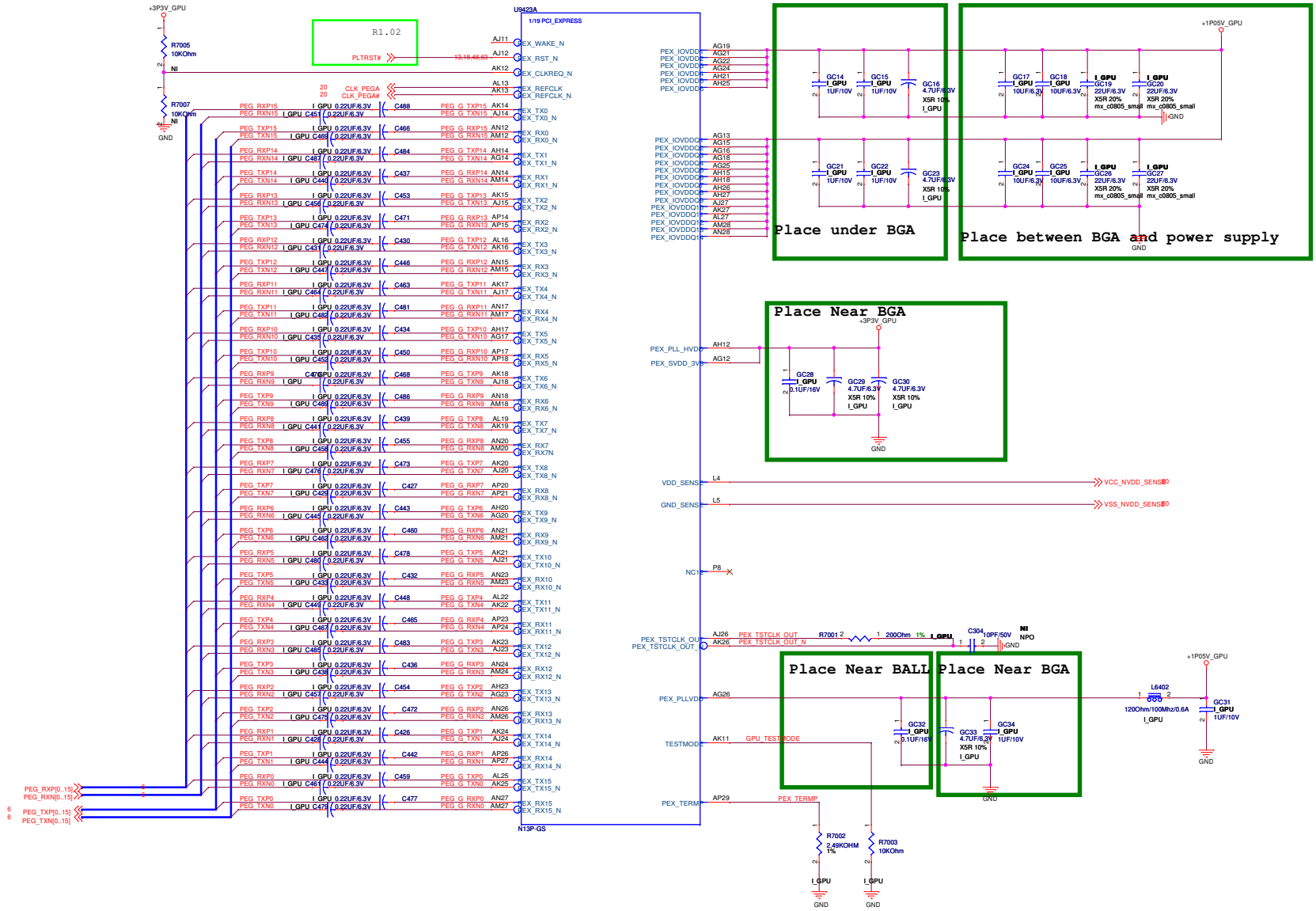
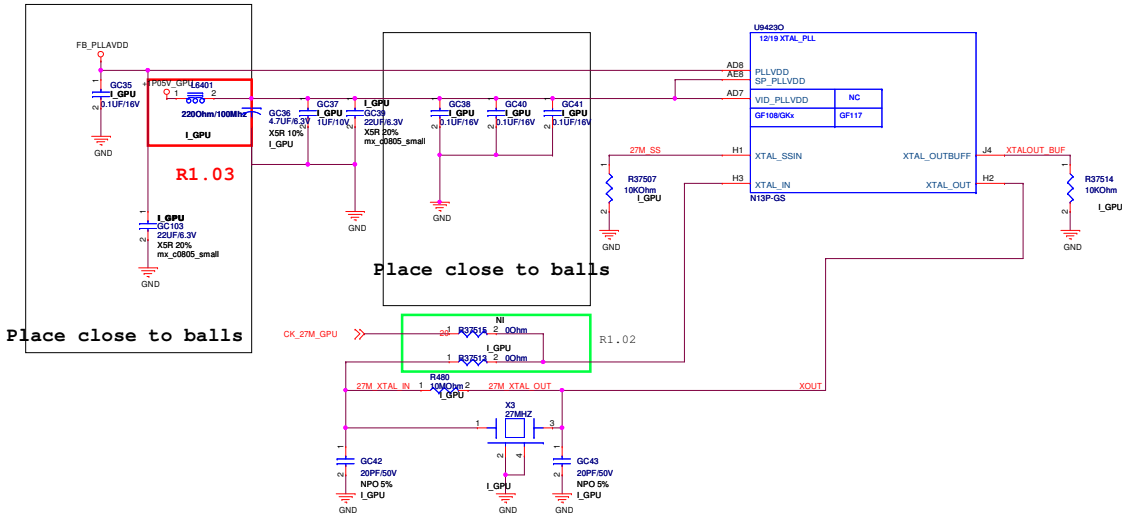
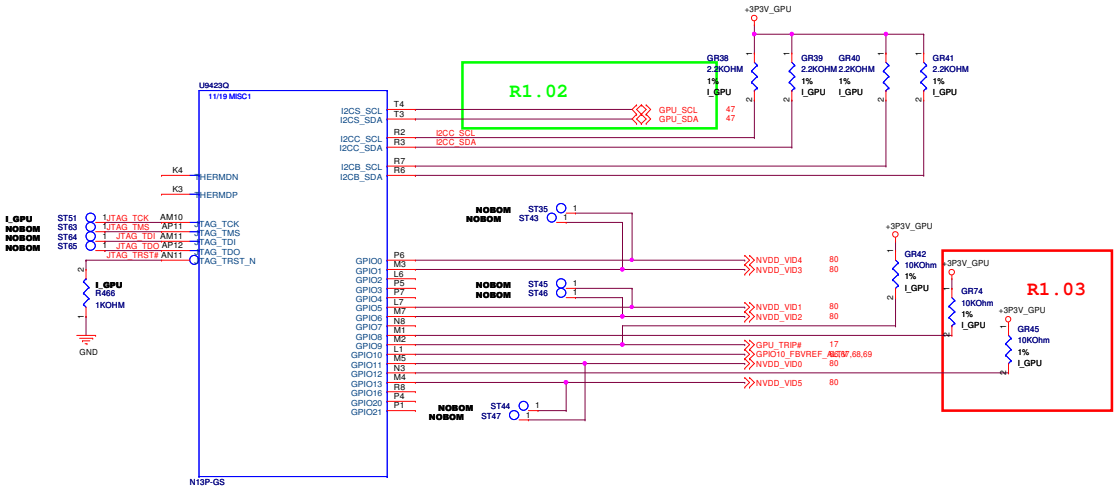


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	MXM.VGA_N13P_PCI-E
PEGATRON CORPORATION	Engineer:	River Yang
Size: A2	Project Name: IPIMB-PV	Rev: 1.01
Date: Thursday, February 23, 2012	Sheet 70 of 78	





GPIO	Function	GPIO	Function
GPIO 0	Debug Service Header/ALT Fan PWM		I2C PORT C
GPIO 1	NVVDD VID 2	EXPND 0	Level Shifter Error Correction
GPIO 2	LCD Brightness Control (BL PWM)	EXPND 1	Power Sequenser Margin*
GPIO 3	LCD Power Enable (PPEN)	EXPND 2	Power Sequenser MR*
GPIO 4	LCD Backlight Enable (BLEN)	EXPND 3	ALT Debug Service Header
GPIO 5	NVVDD VID 0		
GPIO 6	NVVDD VID 1		SMBUS
GPIO 7	3D STEREO		
GPIO 8	GPU Overtemp	EXPND 4	GPU_PS_EN
GPIO 9	GPU Thermal Alert	EXPND 5	Reserved
GPIO 10	FB Vref Control	EXPND 6	PEX_RST*
GPIO 11	FBVDD/Q VID	EXPND 7	Reserved
GPIO 12	PWR_Level AC Detect		
GPIO 13	PS1 & PS2 Vprgm Enable		
GPIO 14	HPD for IFP AB (not used)		
GPIO 15	HPD for IFP C (DP)		
GPIO 16	Fan PWM Control		
GPIO 17	HPD for IFP D (eDP)		
GPIO 18	HPD for IFP E (DP)		
GPIO 19	HPD for IFP F (DP)		
GPIO 20	<not used>		
GPIO 21	<not used>		

PEGATRON Title : 85XM VGA-N13P_Xtal/Thermal

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

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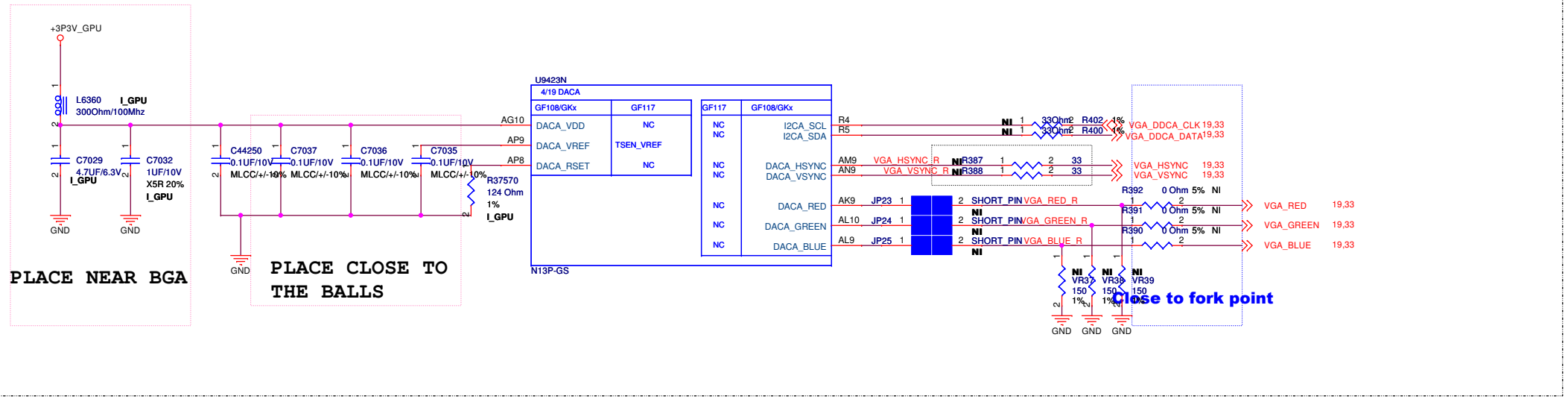
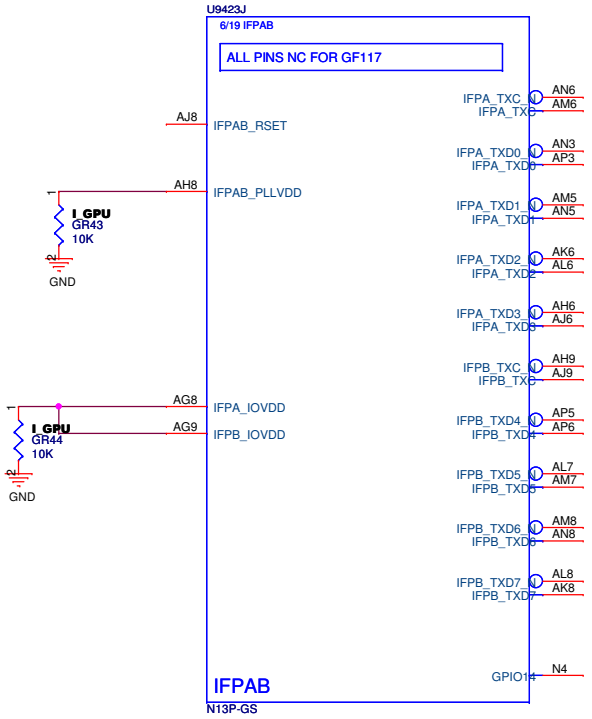




PEGATRON DT-MB RESTRICTED SECRET

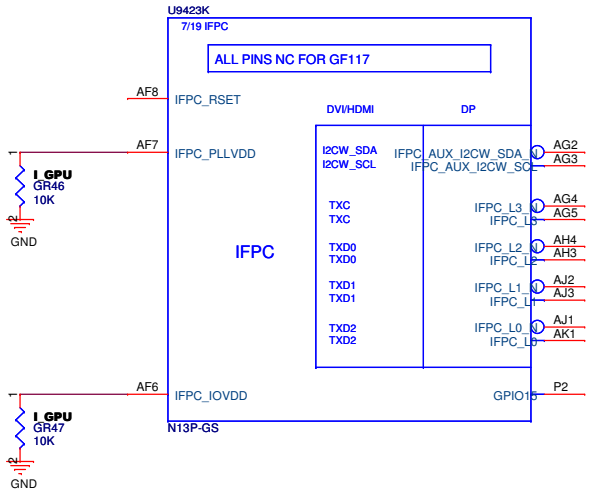
PEGATRON CORPORATION

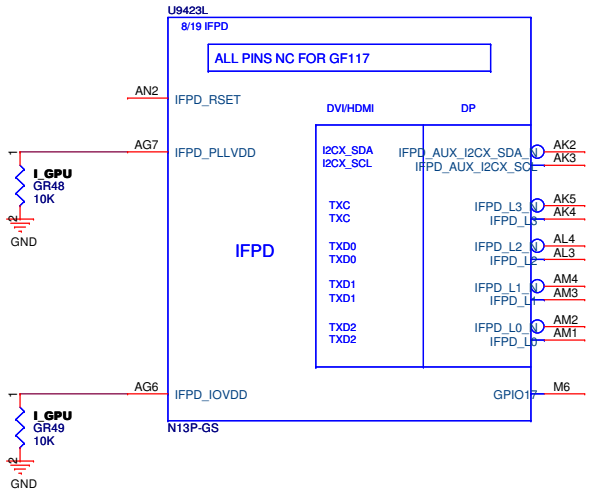
Title : MXM.VGA_N13P_PCI-E_LVDS_VGA

Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 72 of 78





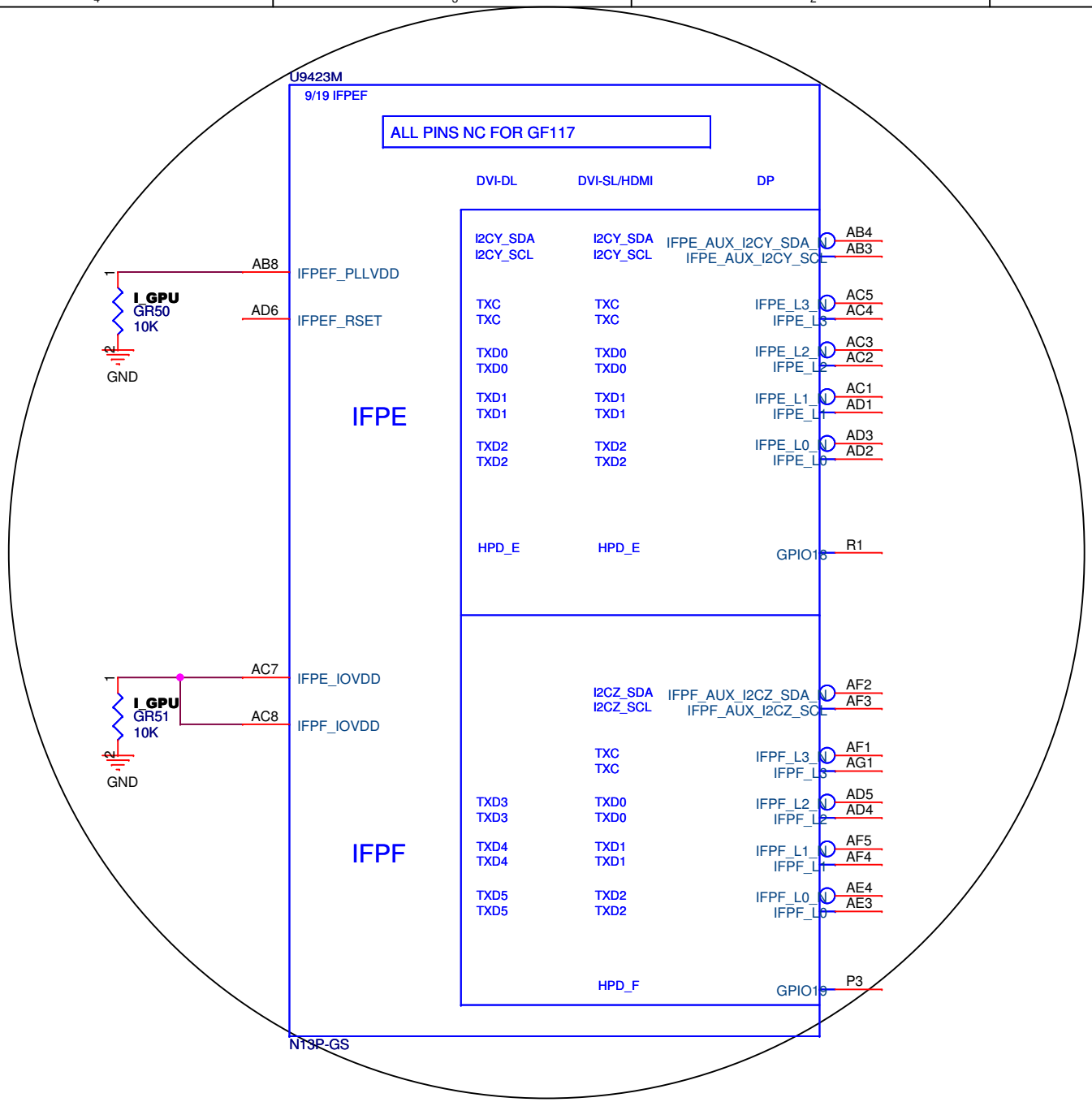
PEGATRON CORPORATION

Title : MXM.VGA_N13P_eDP-1

Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 73 of 78



PEGATRON

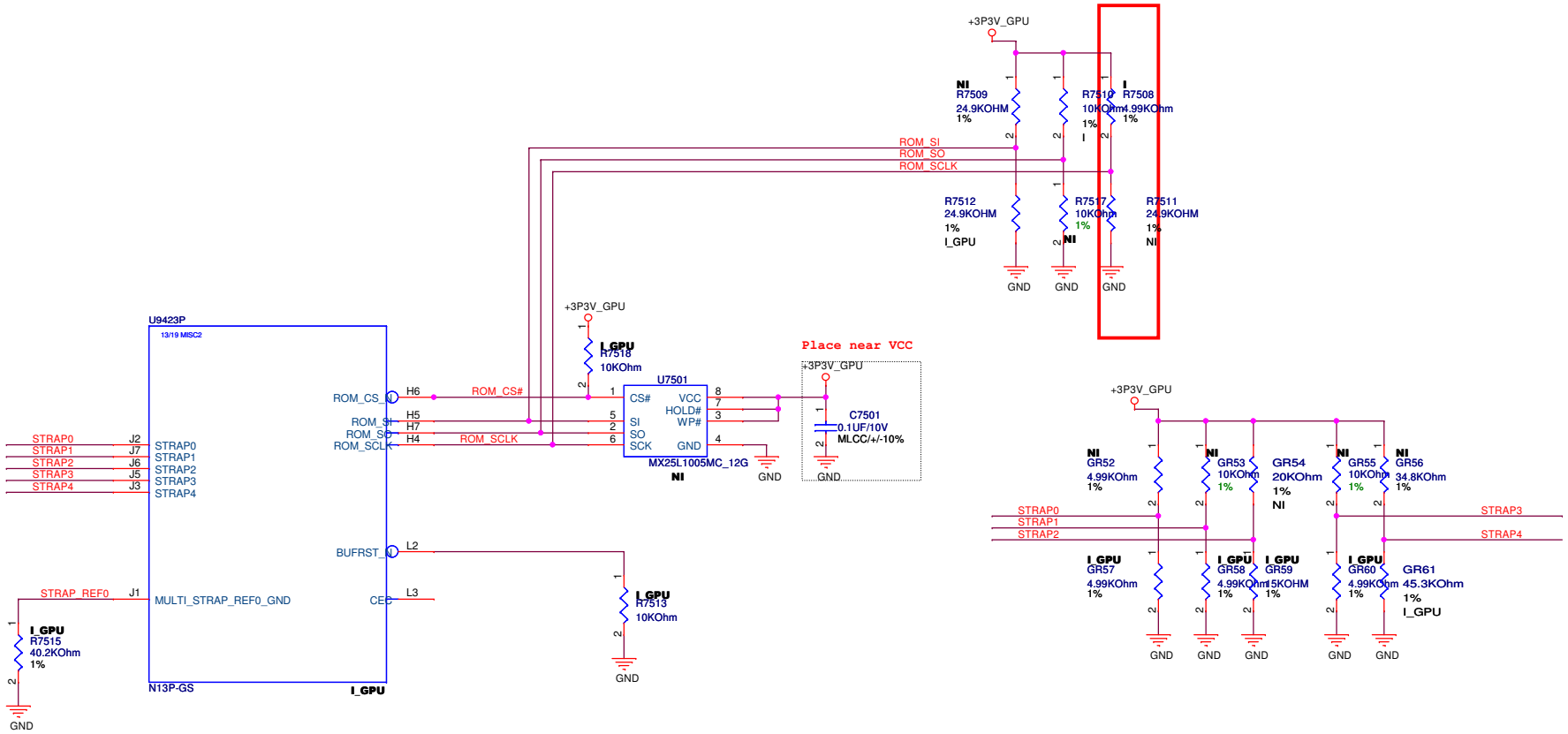
Title : MXM.VGA_N13P_eDP-2

PEGATRON CORPORATION

Engineer: River Yang

Size	Project Name	Rev
A4	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 74 of 78



ROM_SCLK *5k to 3.3V* **R1.03 BOM**

ROM_SI *25k to GND*

ROM_SO *10K to 3.3V*

STRAP0 *5k to GND*

STRAP1 *5k to GND*

STRAP2 *20K to 3.3V*

STRAP3 *5k to GND*

STRAP4 *45k to GND*

2G Hynix ROM_SI PD 25K 0315-00P0000

2G Samsumg ROM_SI PD 30K 0315-00V90DE

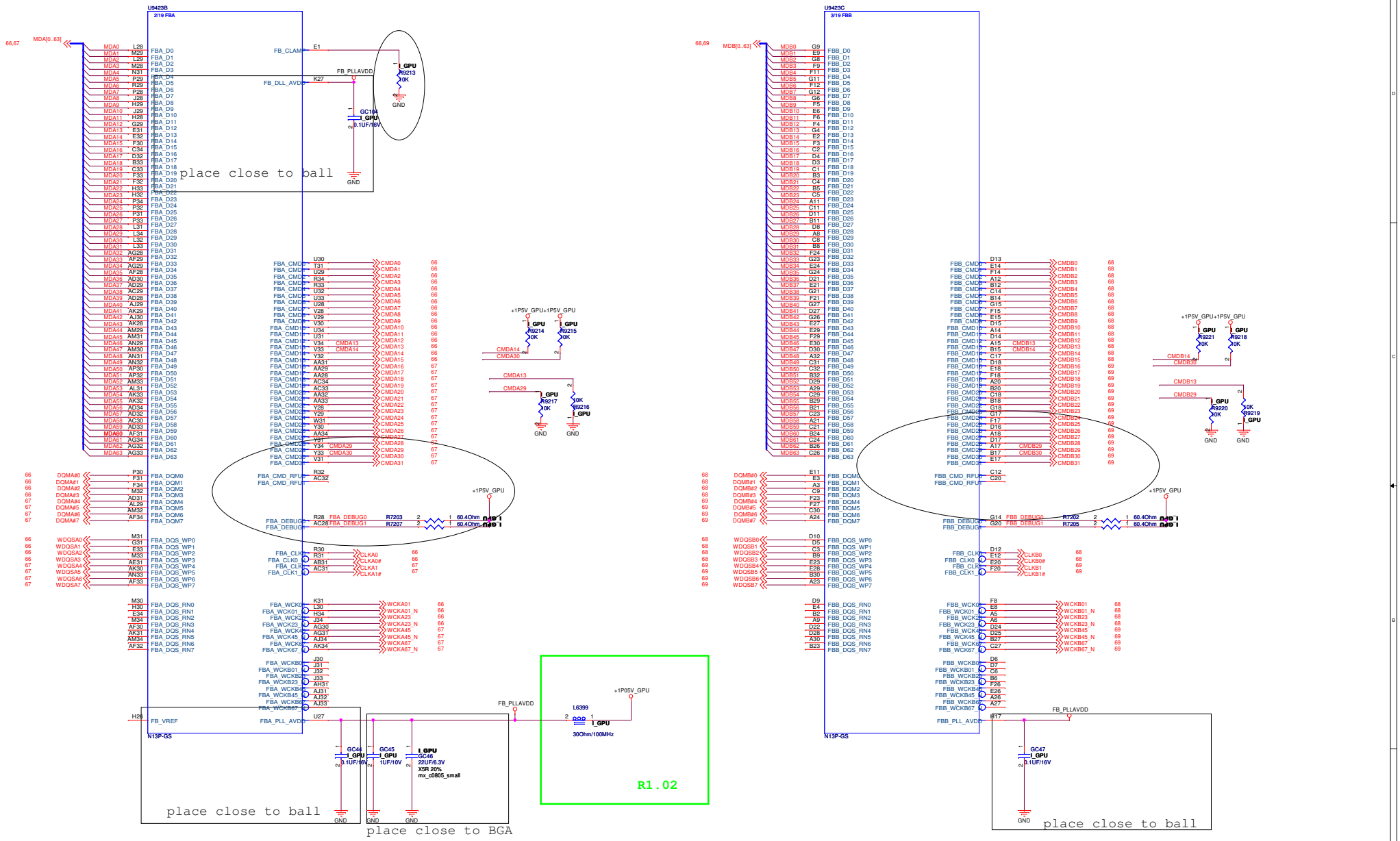
PEGATRON

Title : MXM.VGA_N13P_EEPROM

PEGATRON CORPORATION Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 75 of 82



PEGATRON CORPORATION

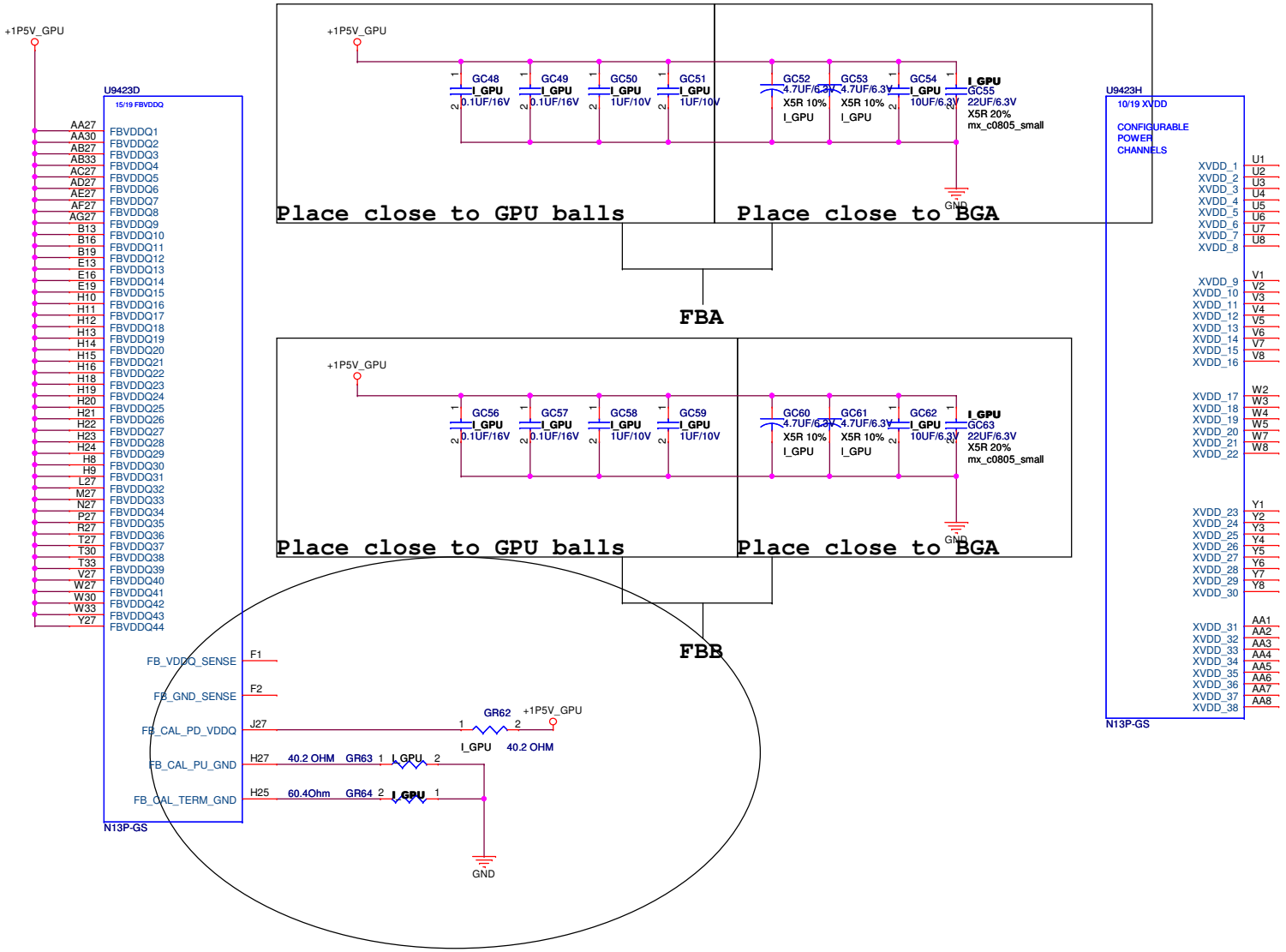
IB RESTRICTED SECRET

Title : MXM VGA_N13P_MEM Ctrl

Engineer: River Yang

Size	Project Name	Rev
A2	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 78 of 82



PEGATRON B-RESTRICTED SECRET

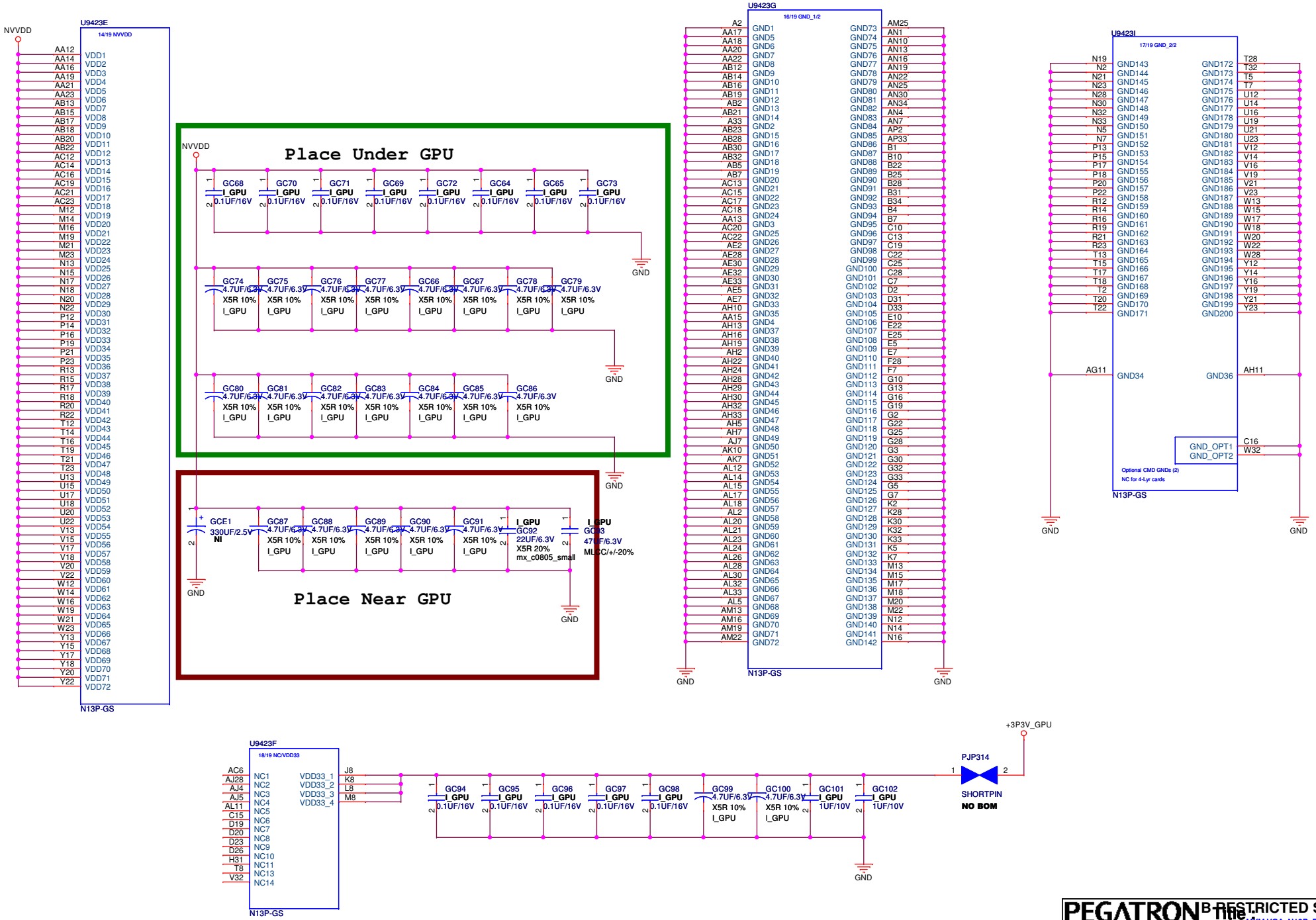
PEGATRON CORPORATION

Title : MXM.VGA_N13P_VDDQ_POWER

Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.01

Date: Thursday, February 23, 2012 Sheet 77 of 78



PEGATRON B-RESTRICTED SECRET

Title: MXM.VGA_N13P_POWER&GND

PEGATRON CORPORATION

Engineer: River Yang

Size	Project Name	Rev
A3	IPIMB-PV	1.01

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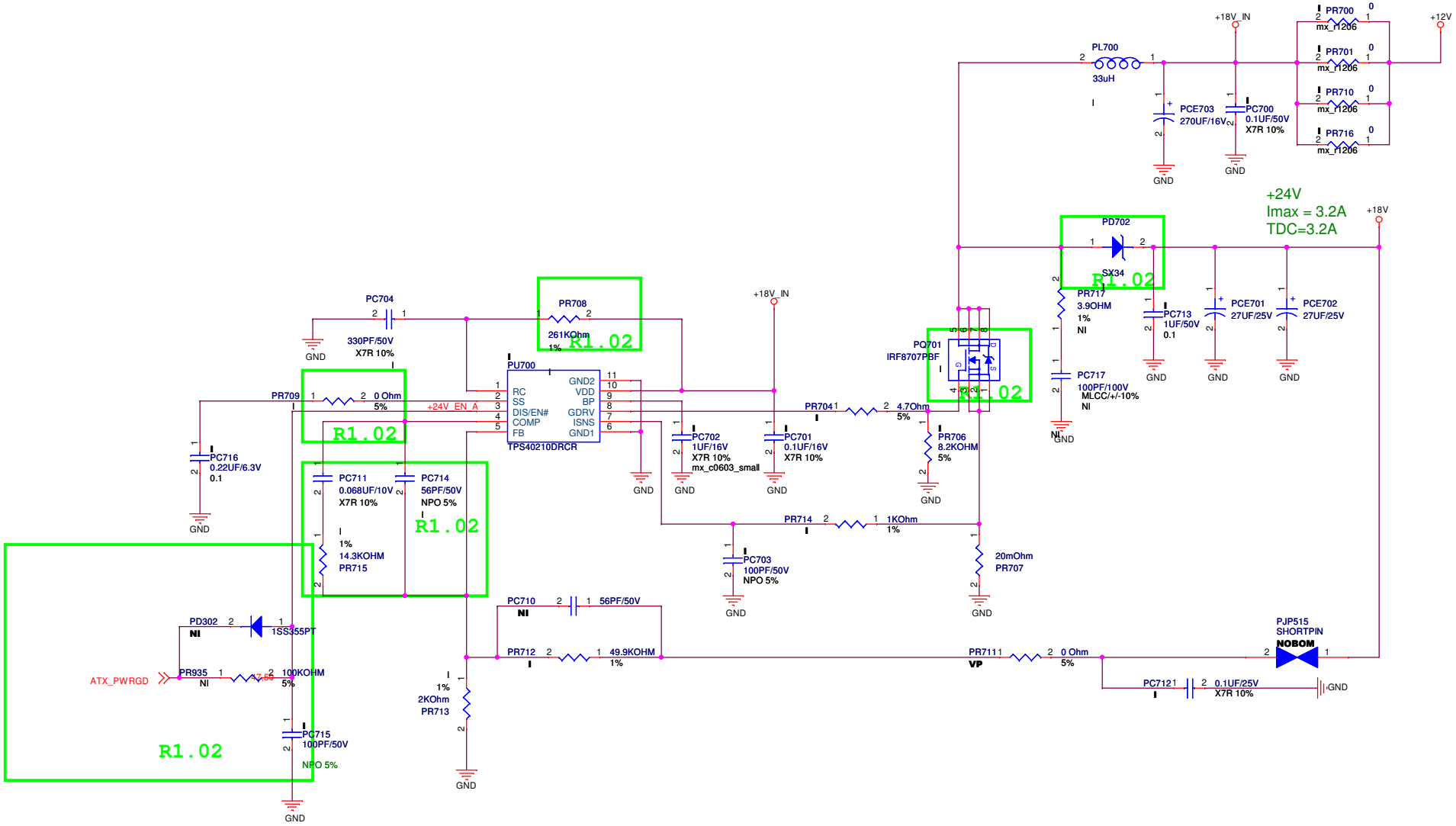

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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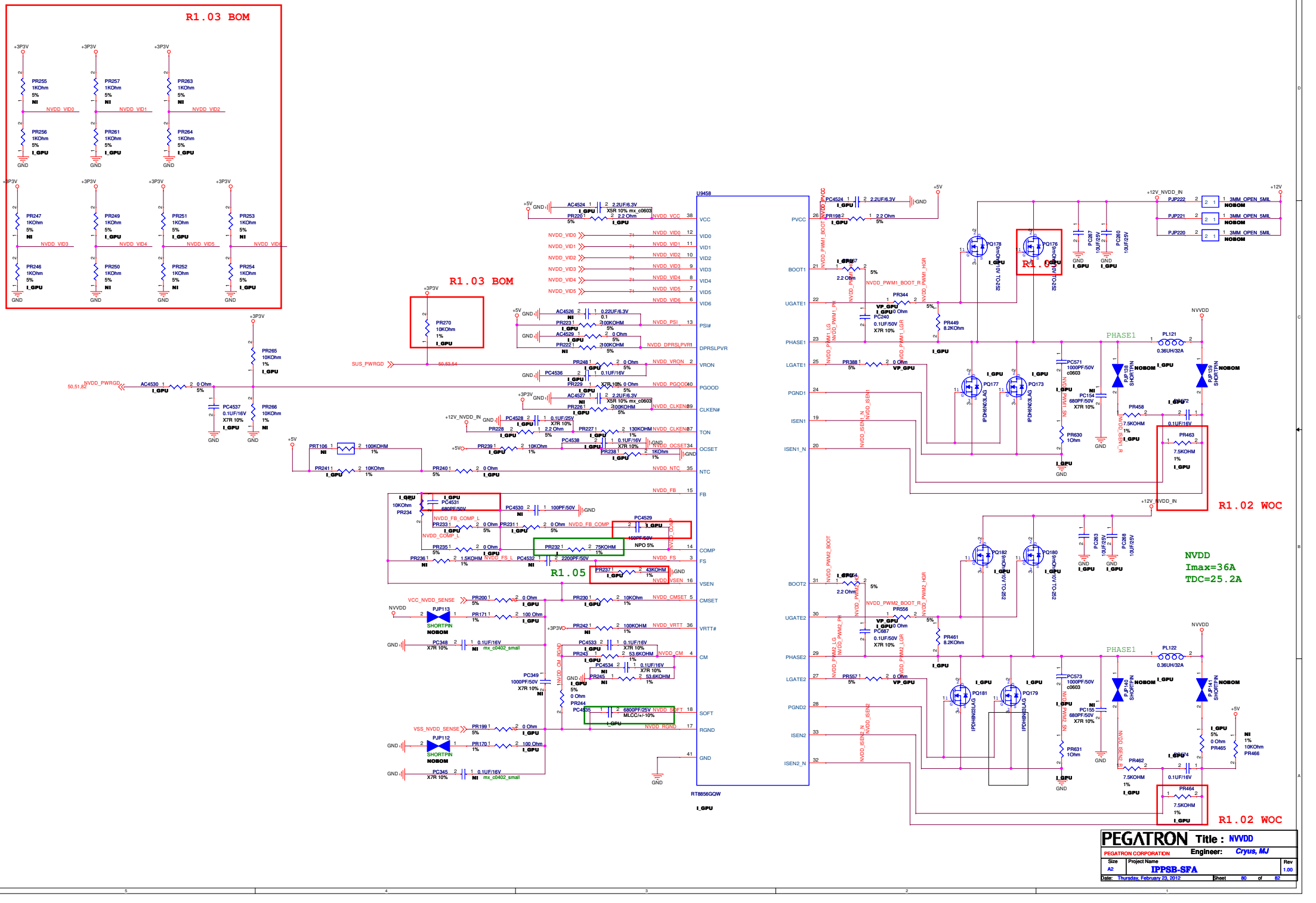
R1.03 BOM
R1.03 BOM
R1.05
R1.02 WOC
R1.02 WOC
NVDD
Imax=36A
TDC=25.2A
U9458
RT8856GQW
PEGATRON
Title : NVDD
PEGATRON CORPORATION
Engineer: Cryus, MJ
Size A2
Project Name IPPSB-SFA
Rev 1.00
Date: Thursday, February 23, 2012
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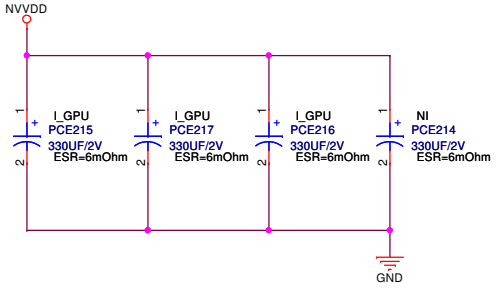
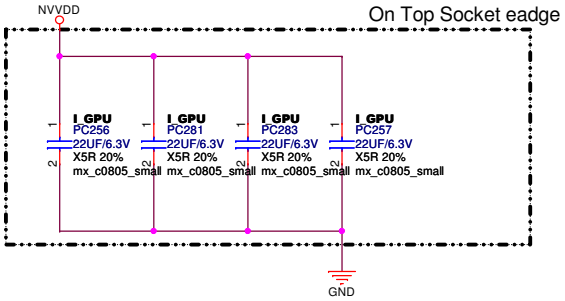
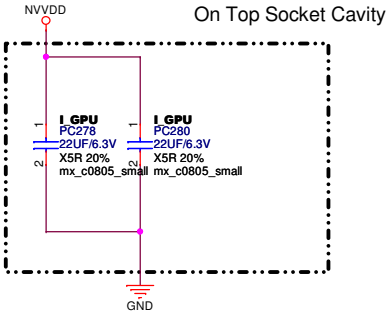
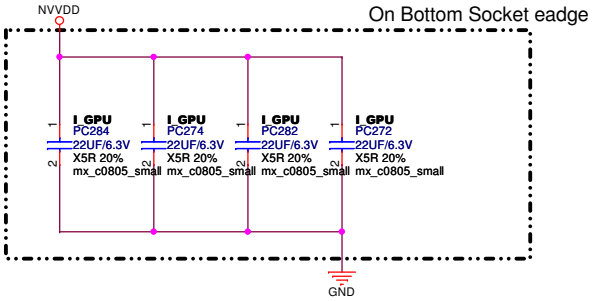
Output CAP

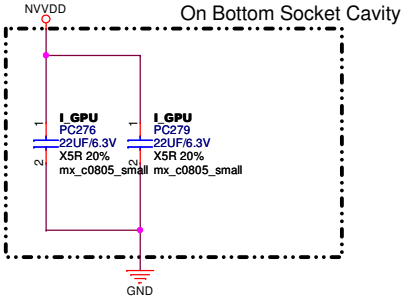
+V_AXG : 0 ~ 1.52 V











Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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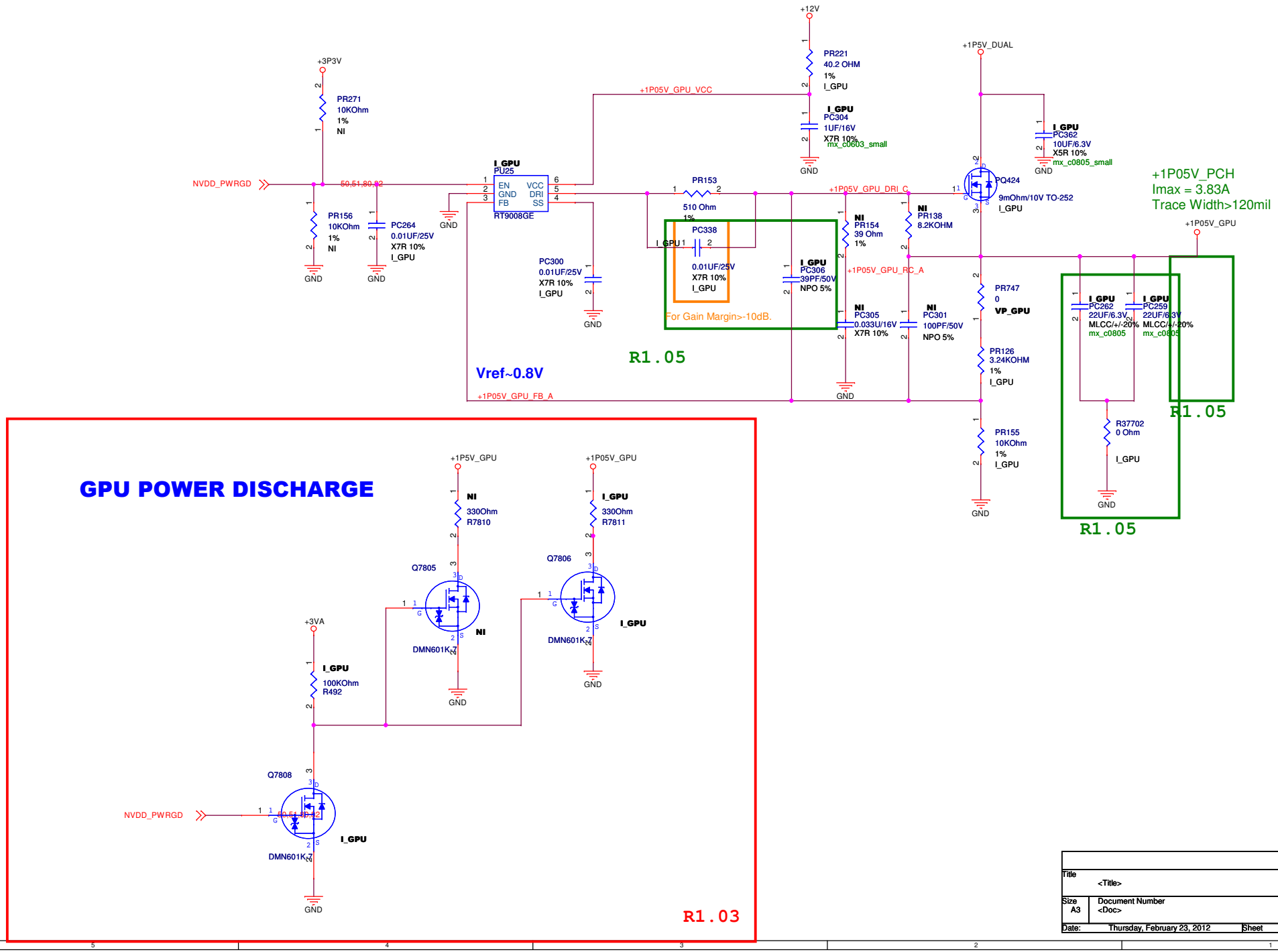

Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
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