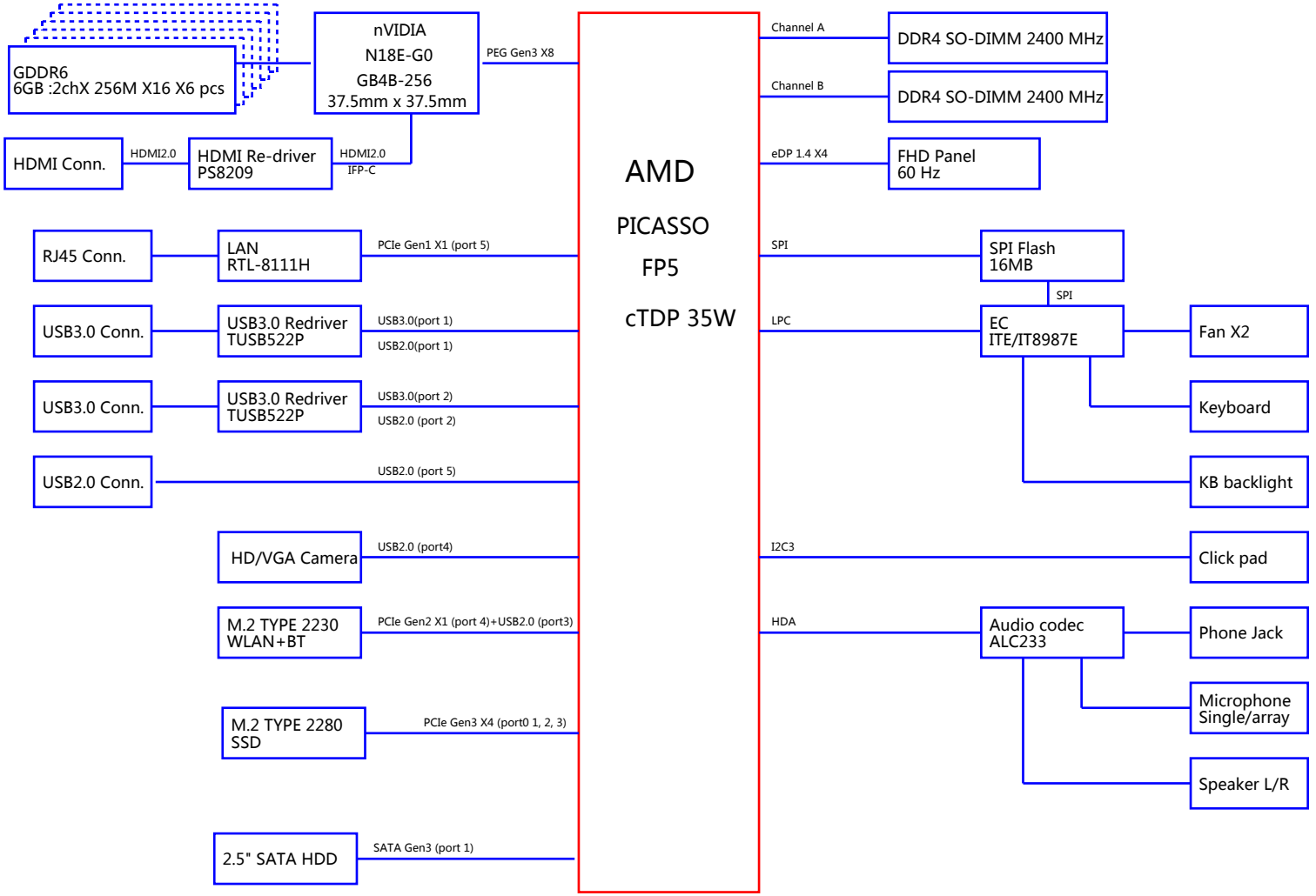
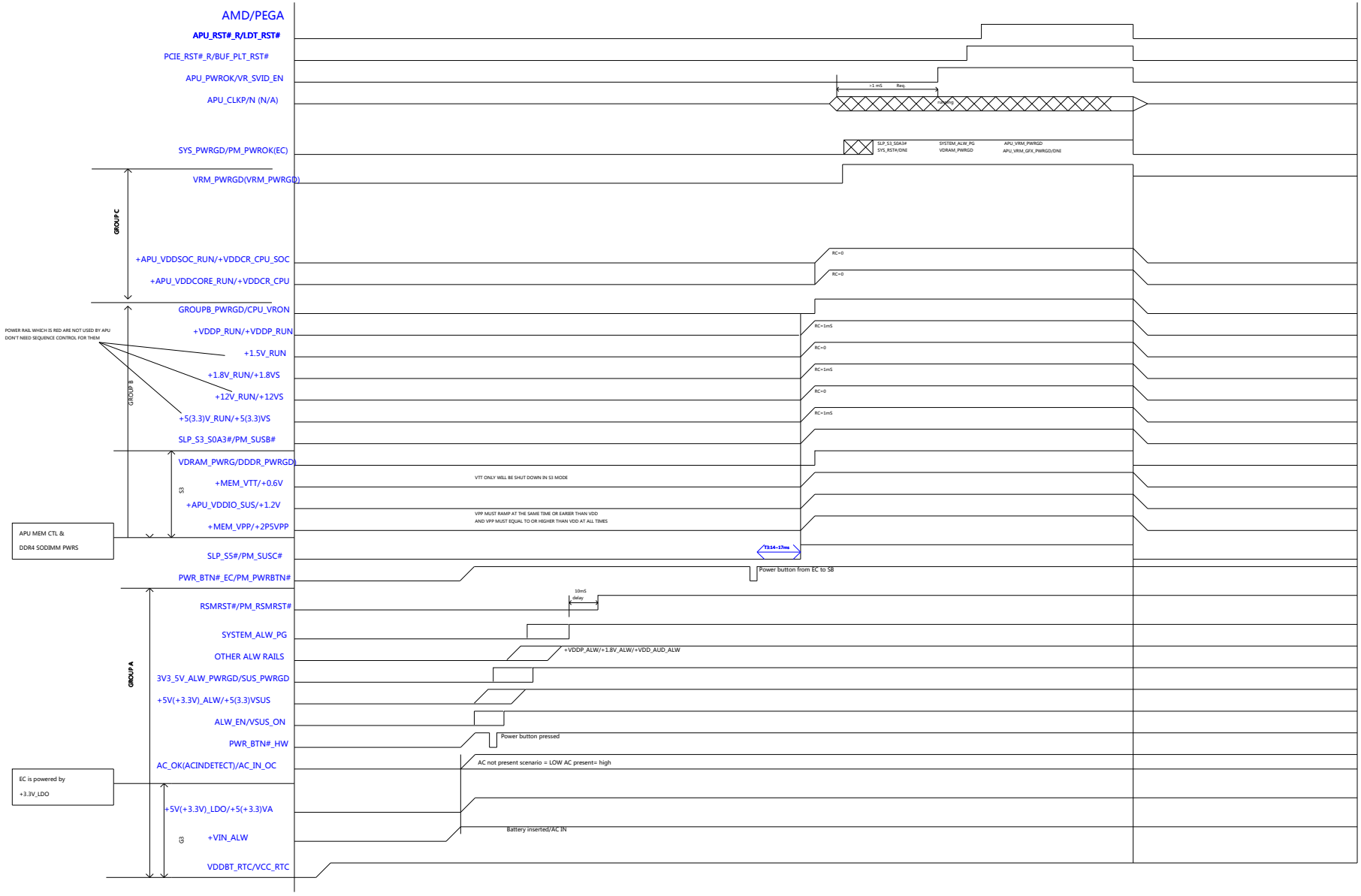
FX505DU Block Diagram



Power

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
RG1-HW3 RD

Title : Block Diagram
Engineer: Johnson Huang
Size: C | Project Name: FX505DU | Rev: 1.1
Date: Tuesday, March 12, 2019 | Sheet 1 of 99



PEGATRON PROPRIETARY AND CONFIDENTIAL

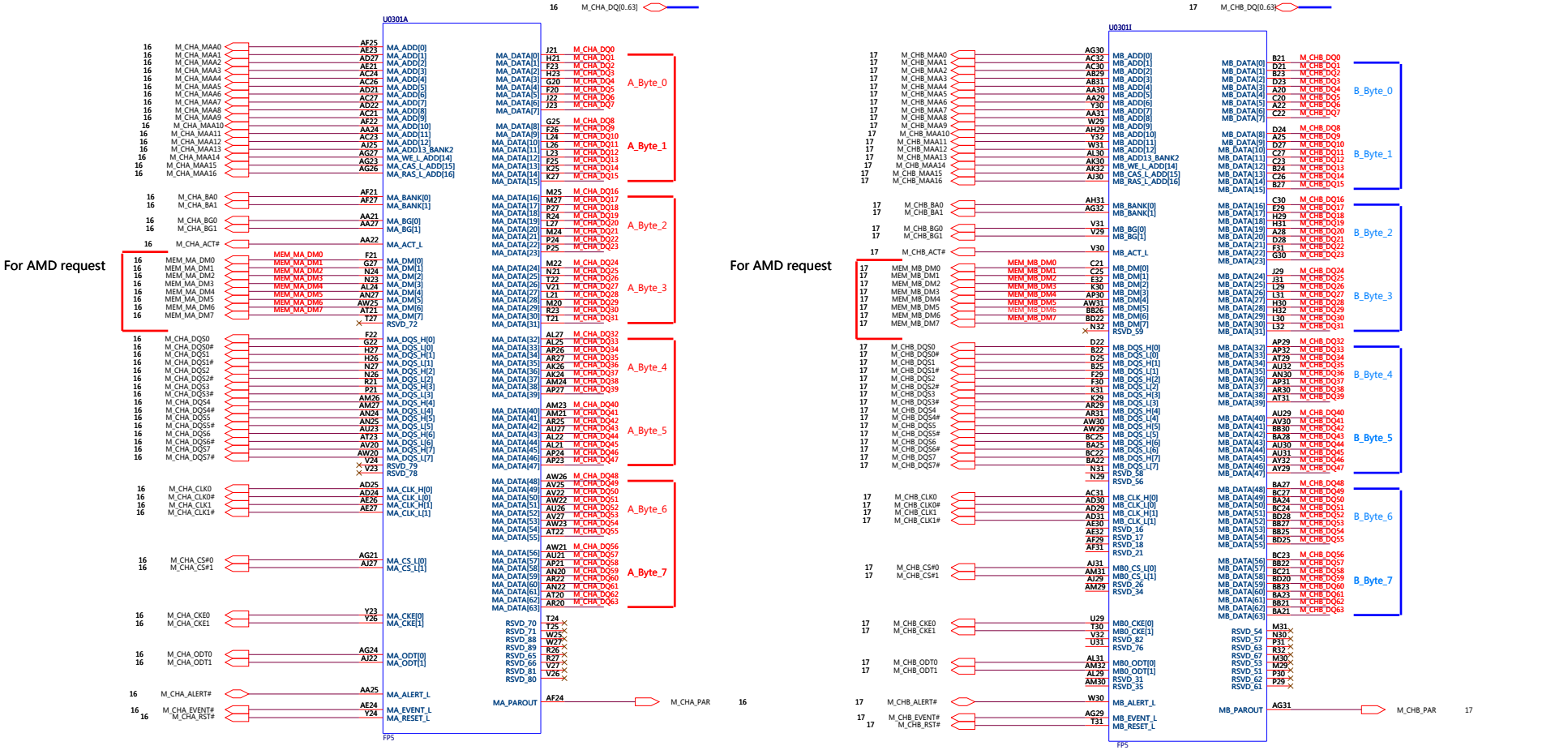
Title : Option

BG1-HW3 RD

Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

Date: Tuesday, March 12, 2019 Sheet 2 of 72



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

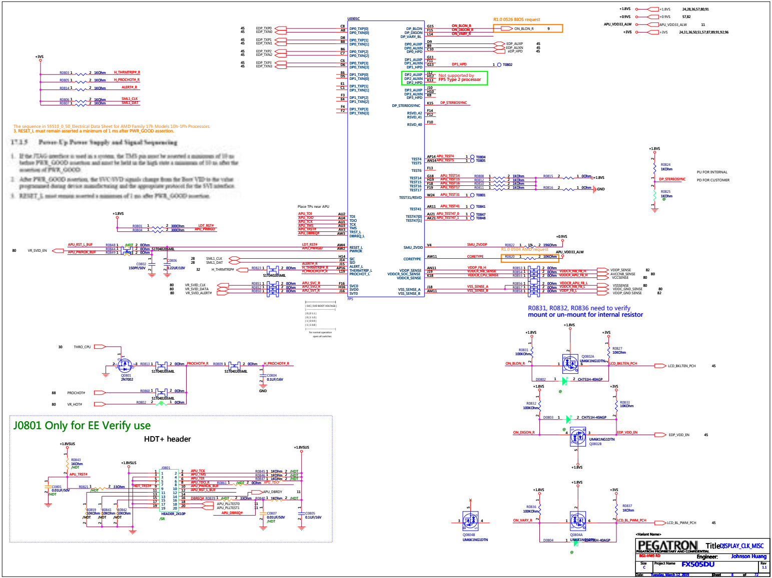
BG1-HW3 RD

Title : MEM & PCIE I_F

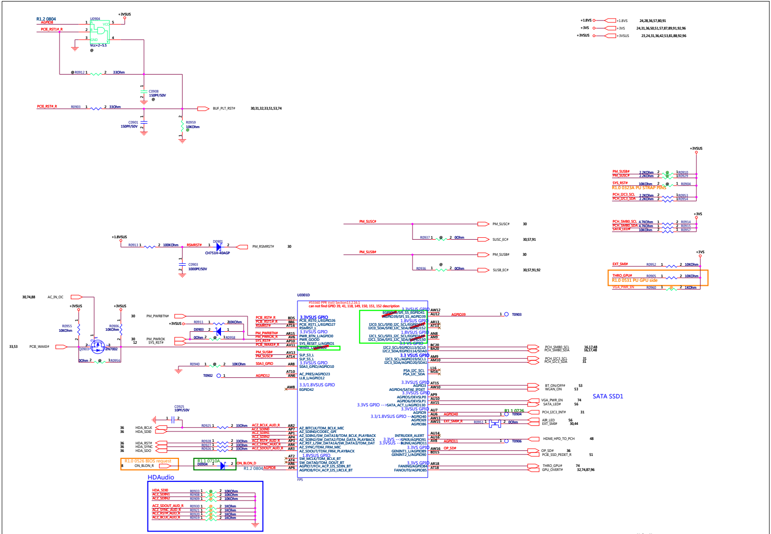
Engineer:

Size	Project Name	Rev
C		1.1

Date: Tuesday, March 12, 2019 Sheet 7 of 72



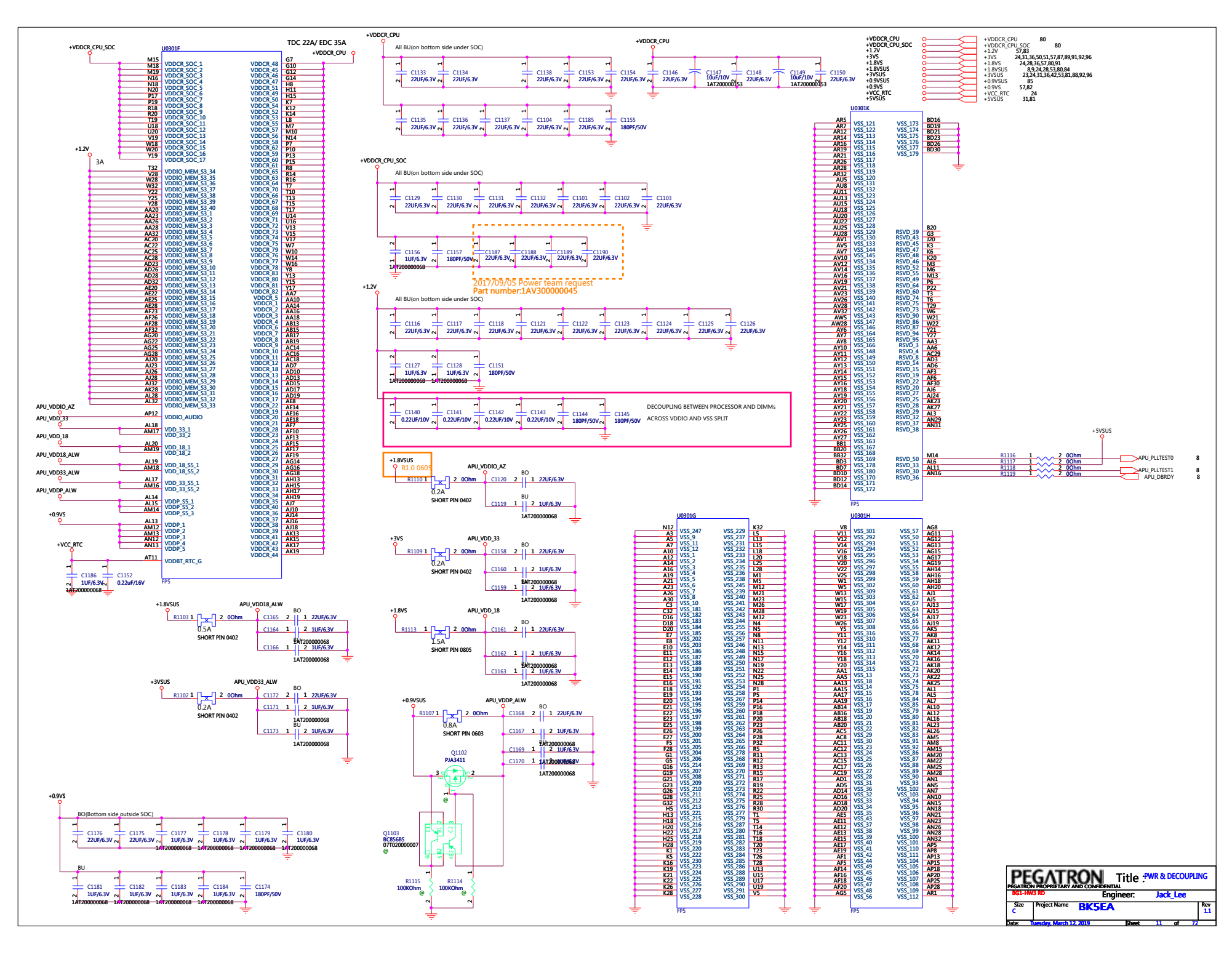
The sequence in 55510_0_50_Electrical Data Sheet for AMD Family 17h Models 10h-1Fh Processors.
3. RESET_L must remain asserted a minimum of 1 ms after PWR_GOOD assertion.
R1.0 0526 BIOS request
Not supported by FP5 Type 2 processor
R1.0 0504 AMD request
Place TPs near APU
PU FOR INTERNAL
PD FOR CUSTOMER
R0831, R0832, R0836 need to verify
mount or un-mount for internal resistor
J0801 Only for EE Verify use
HDT+ header
U0301C
FP5
HEADER_2X10P
Q0801 2N7002
Q0802A UM6K1NG1DTN
Q0802B UM6K1NG1DTN
Q0804A UM6K1NG1DTN
Q0804B UM6K1NG1DTN
D0802 CH751H-40AGP
D0803 CH751H-40AGP
D0804 CH751H-40AGP
LCD_BKLTEN_PCH
EDP_VDD_EN
LCD_BL_PWM_PCH
THRO_CPU
PROCHOT#
VR_HOT#
VR_SVID_EN
VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
SML1_CLK
SML1_DAT
H_THRMTRIP#
APU_VDD33_ALW
+1.8VS
+0.9VS
+3VS
+1.8VSUS
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Title DISPLAY_CLK_MISC
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 8 of 72



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

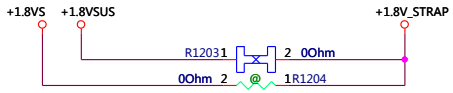
Title:	GEVENT_GPIO_SD_AZ
Engineer:	Johnson Huang
Size	C
Project Name	FX505DU
Rev	1.1
Date:	Tuesday, March 12, 2019
Sheet	9 of 72


TDC 22A/ EDC 35A
U0301F
U0301K
U0301G
U0301H
All BU(on bottom side under SOC)
2017/09/05 Power team request
Part number:1AV300000045
DECOUPLING BETWEEN PROCESSOR AND DIMMs
ACROSS VDDIO AND VSS SPLIT
SHORT PIN 0402
SHORT PIN 0805
SHORT PIN 0603
PJA3411
BC856BS
BO(Bottom side outside SOC)
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PWR & DECOUPLING
Engineer: Jack_Lee
Project Name BK5EA
Tuesday, March 12, 2019

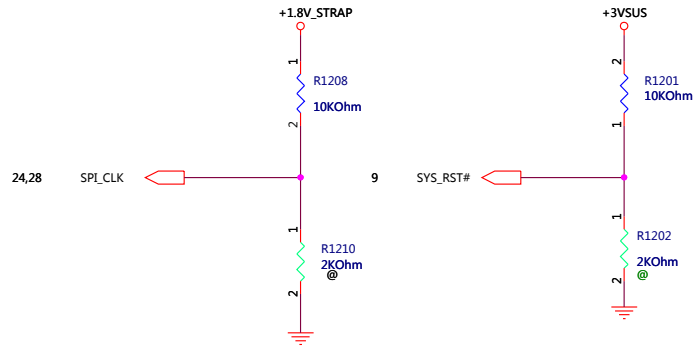
+1.8VSUS +1.8VSUS 8,9,24,28,53,80,84

+1.8VS +1.8VS 24,28,36,57,80,91

+3VSUS +3VSUS 23,24,31,36,42,53,81,88,92,96



STRAP PINS



STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

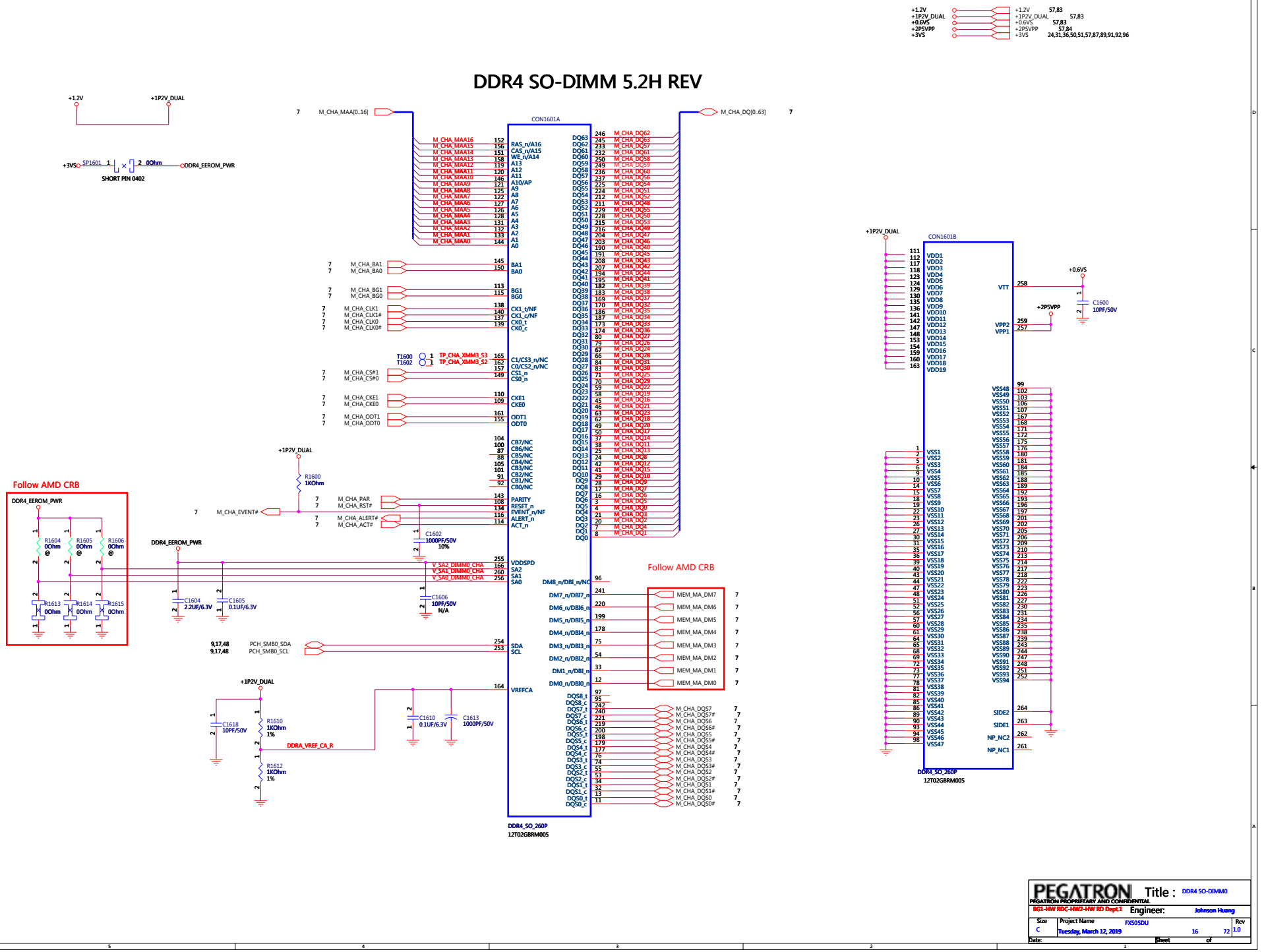
PEGATRON Title : STRAPS, SOCKET, HS

BG1-HW3 RD Engineer: Johnson Huang

Size B | Project Name FX505DU | Rev 1.1

Date: Tuesday, March 12, 2019 Sheet 12 of 72

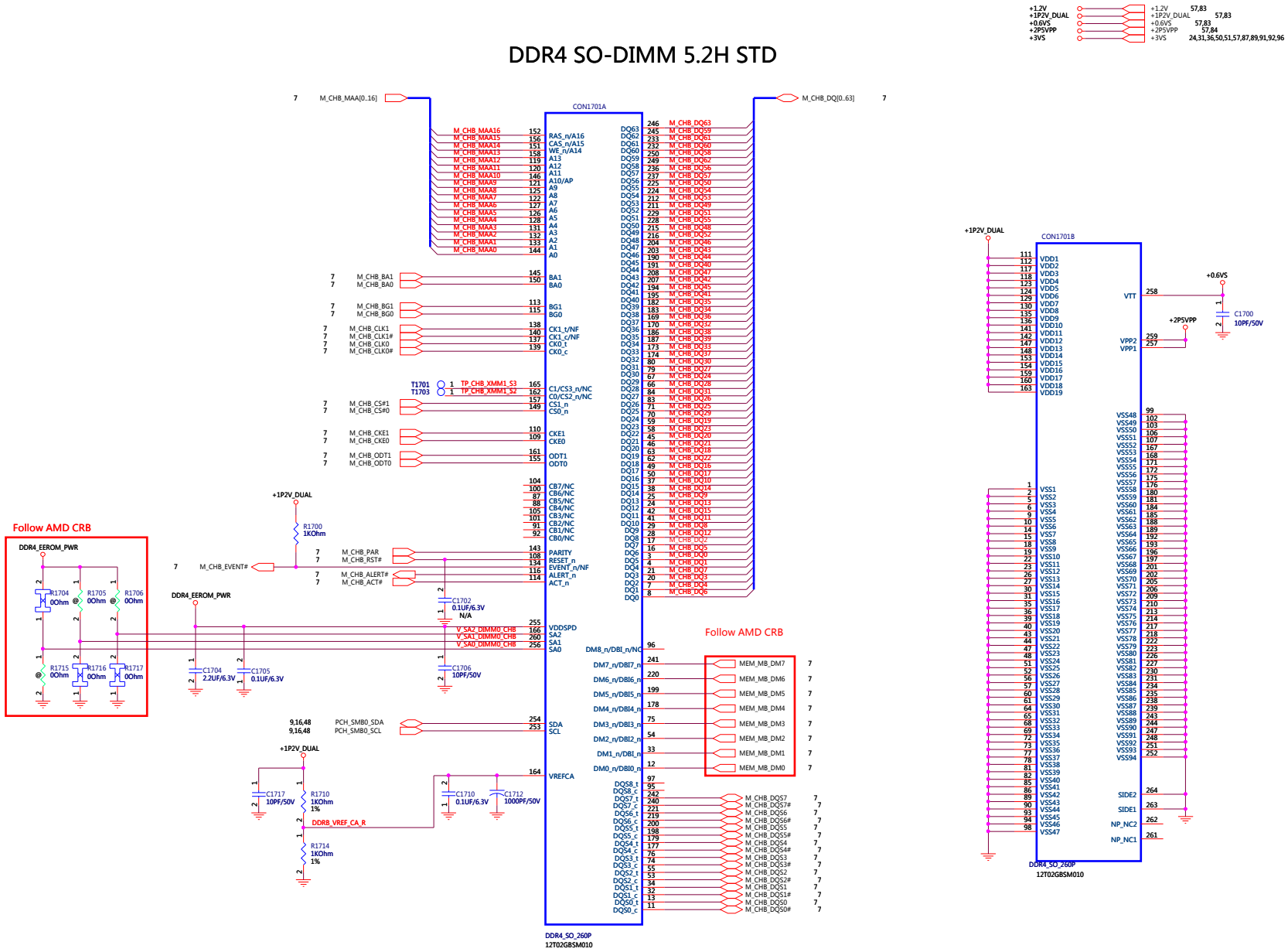
DDR4 SO-DIMM 5.2H REV



Title :	DDR4 SO-DIMM0	
Engineer:	Johnson Huang	
Project Name	FX505DU	Rev 1.0
Date:	Tuesday, March 12, 2019	Sheet 16 of 72

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1

DDR4 SO-DIMM 5.2H STD



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DDR4 SO-DIMM1

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 17 of 72

+1.2V
+1P2V_DUAL
+0.6VS
+2P5VPP
+3VS

+1.2V 57,83
+1P2V_DUAL 57,83
+0.6VS 57,83
+2P5VPP 57,84
+3VS 24,31,36,50,51,57,87,89,91,92,96

+1P2V_DUAL

NOTE:
Place those cap close to CH A DIMM

R1.1 modify
EMC

C1805 10UF/6.3V
C1806 10UF/6.3V
C1807 10UF/6.3V
C1800 2.2UF/6.3V
C1801 2.2UF/6.3V
C1802 2.2UF/6.3V
C1803 2.2UF/6.3V
C1804 2.2UF/6.3V
C1843 0.1UF/6.3V
C1846 0.1UF/6.3V
C1851 0.1UF/6.3V
C1848 10PF/50V
C1852 2.2UF/6.3V

C1822 1UF/6.3V 0201 X5R/+/-20%
C1858 1UF/6.3V 0201 X5R/+/-20%
C1823 1UF/6.3V 0201 X5R/+/-20%
C1859 1UF/6.3V 0201 X5R/+/-20%
C1824 1UF/6.3V 0201 X5R/+/-20%
C1860 10UF/6.3V
C1825 1UF/6.3V 0201 X5R/+/-20%
C1861 10UF/6.3V
C1826 1UF/6.3V 0201 X5R/+/-20%
C1862 1UF/6.3V 0201 X5R/+/-20%
C1827 1UF/6.3V 0201 X5R/+/-20%
C1863 10UF/6.3V
C1828 1UF/6.3V 0201 X5R/+/-20%
C1864 10UF/6.3V
C1829 1UF/6.3V 0201 X5R/+/-20%
C1865 1UF/6.3V 0201 X5R/+/-20%

R1.1 modify EMC
R1.1 modify EMC
R1.1 modify EMC
R1.1 modify EMC

FX505 RF reserve @20180131

+0.6VS

C1808 2.2UF/6.3V
C1809 2.2UF/6.3V
C1818 2.2UF/6.3V
C1854 10PF/50V
C1855 2.2UF/6.3V
C1819 2.2UF/6.3V
C1820 2.2UF/6.3V
C1821 2.2UF/6.3V

NOTE:
Place those cap close to CH B DIMM

R1.1 modify
EMC

C1815 10UF/6.3V
C1816 10UF/6.3V
C1817 10UF/6.3V
C1810 2.2UF/6.3V
C1811 2.2UF/6.3V
C1812 2.2UF/6.3V
C1813 2.2UF/6.3V
C1814 2.2UF/6.3V
C1844 0.1UF/6.3V
C1845 0.1UF/6.3V
C1850 0.1UF/6.3V
C1847 10PF/50V
C1853 10UF/6.3V

C1832 1UF/6.3V 0201 X5R/+/-20%
C1866 1UF/6.3V 0201 X5R/+/-20%
C1833 1UF/6.3V 0201 X5R/+/-20%
C1867 1UF/6.3V 0201 X5R/+/-20%
C1834 1UF/6.3V 0201 X5R/+/-20%
C1868 1UF/6.3V 0201 X5R/+/-20%
C1835 1UF/6.3V 0201 X5R/+/-20%
C1869 1UF/6.3V 0201 X5R/+/-20%
C1836 1UF/6.3V 0201 X5R/+/-20%
C1870 1UF/6.3V 0201 X5R/+/-20%
C1837 1UF/6.3V 0201 X5R/+/-20%
C1871 1UF/6.3V 0201 X5R/+/-20%
C1838 1UF/6.3V 0201 X5R/+/-20%
C1872 1UF/6.3V 0201 X5R/+/-20%
C1839 1UF/6.3V 0201 X5R/+/-20%
C1873 1UF/6.3V 0201 X5R/+/-20%

FX505 RF reserve @20180131

+2P5VPP

C1840 10UF/6.3V
C1842 1UF/6.3V 0201 X5R/+/-20%
C1875 1UF/6.3V 0201 X5R/+/-20%
C1856 10PF/50V
C1857 2.2UF/6.3V
C1841 10UF/6.3V
C1849 1UF/6.3V 0201 X5R/+/-20%
C1874 1UF/6.3V 0201 X5R/+/-20%

CE1800 330UF/2V @

CFL-H DDR4 SODIMM Decoupling

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x pF (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DDR, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DDR	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

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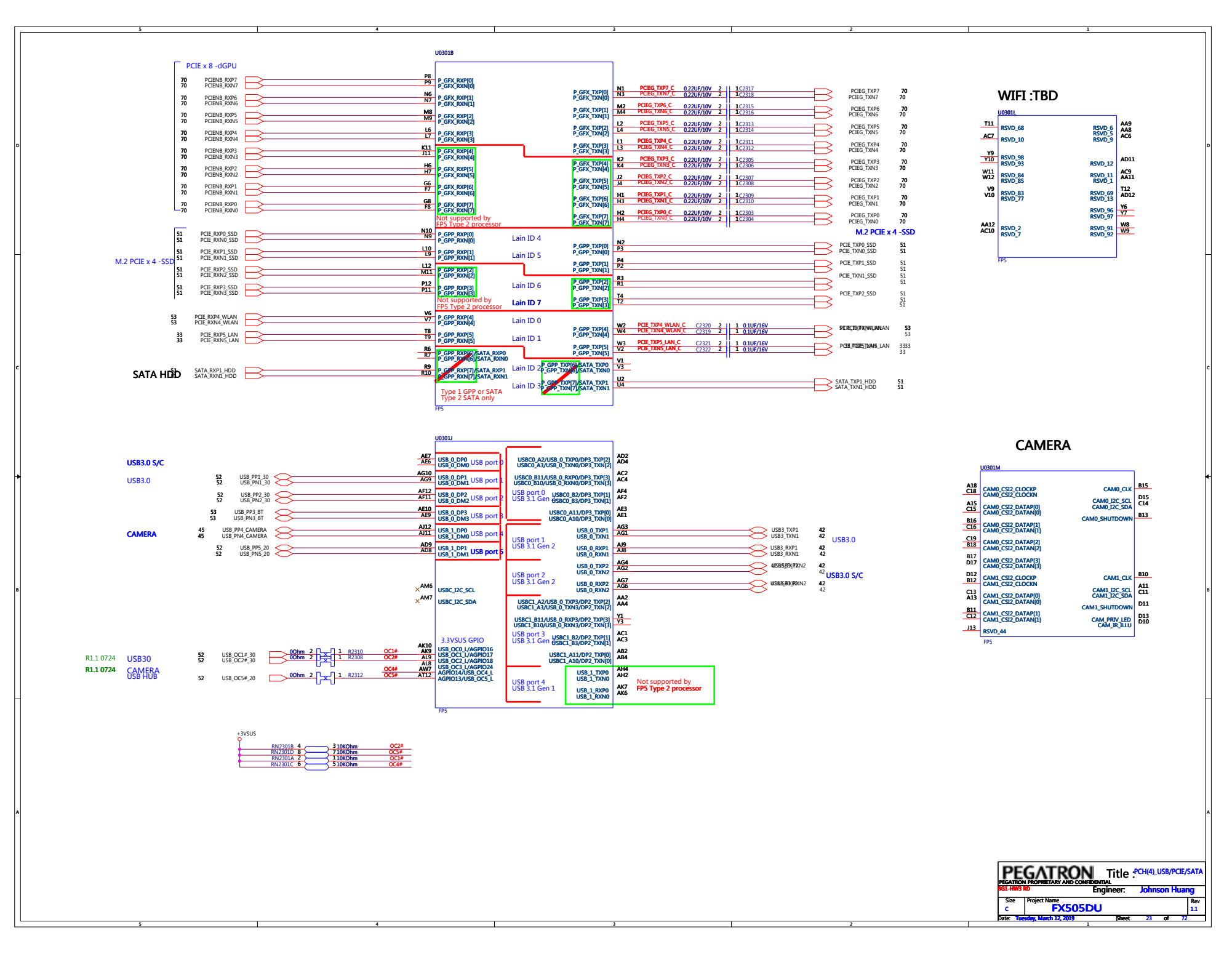
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4 Caps.
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.0
Date: Tuesday, March 12, 2019
Sheet 18 of 72



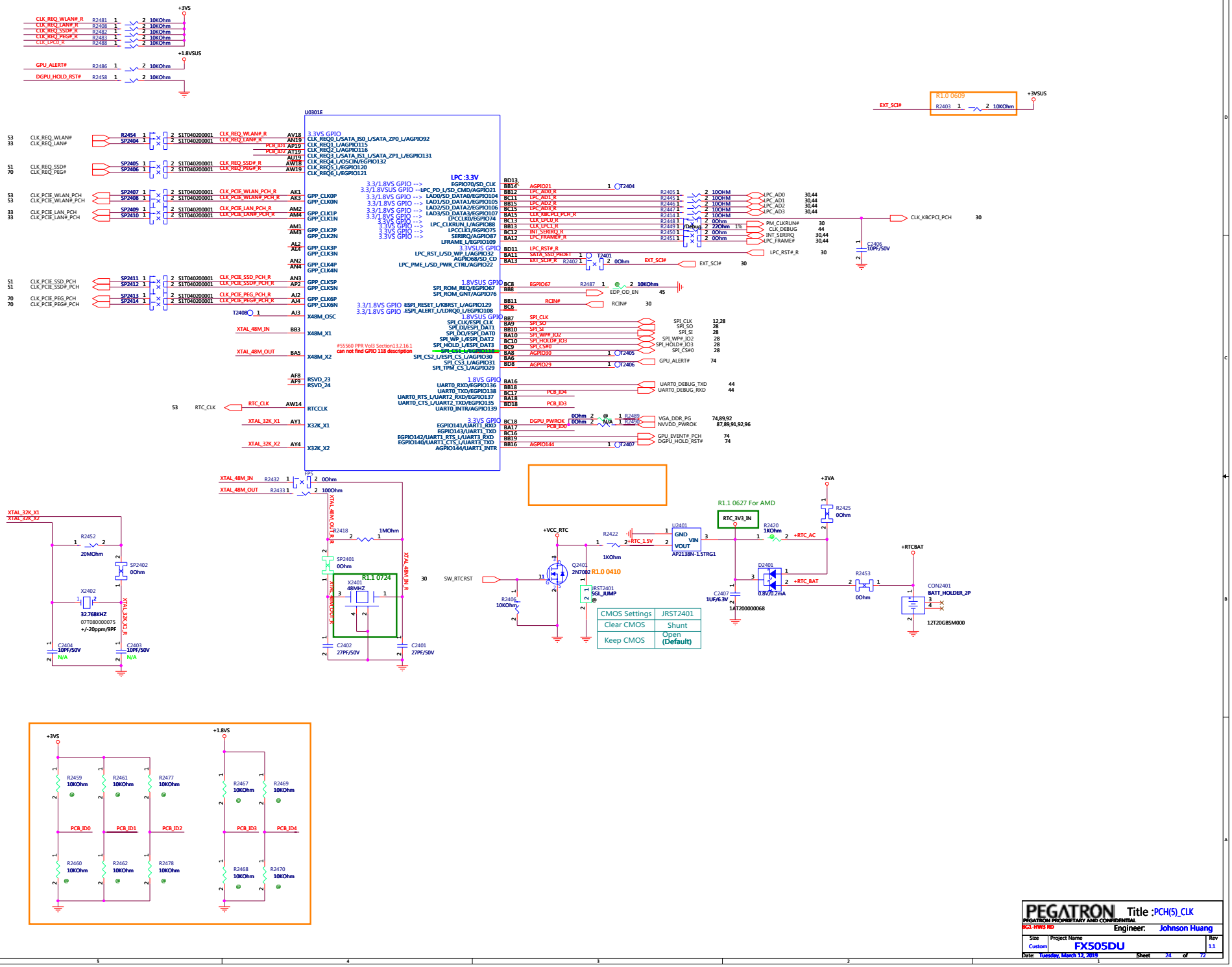
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

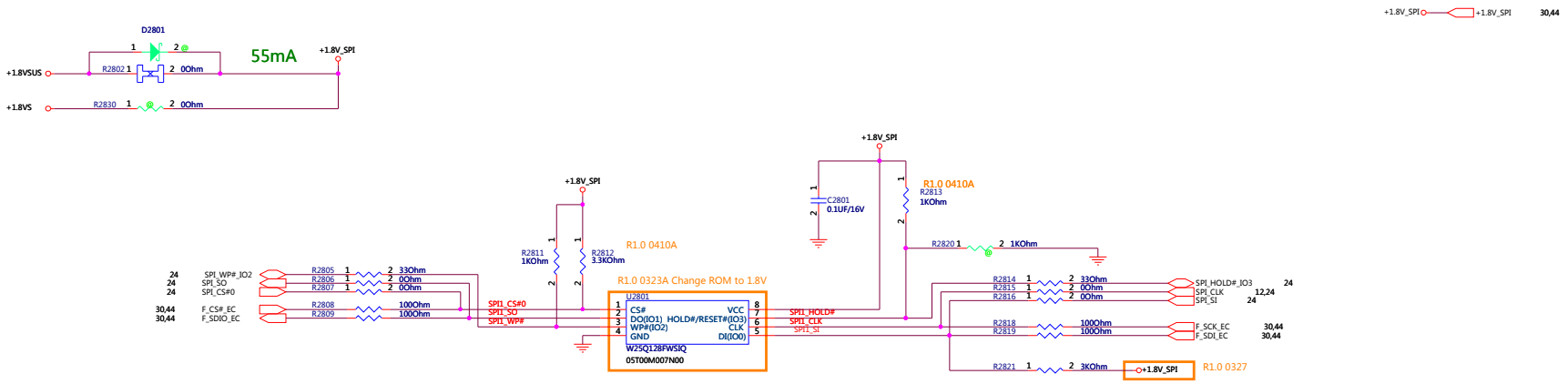
Title : PCH(4)_USB/PCIE/SATA

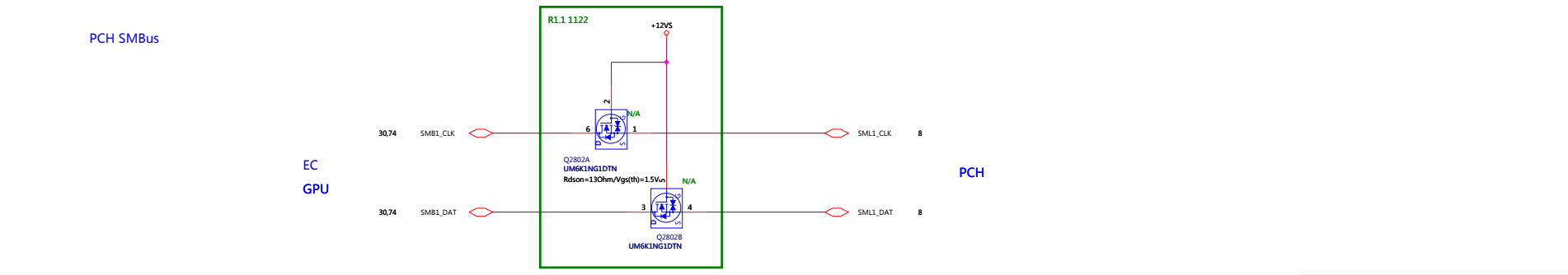
Engineer: Johnson Huang

Size	Project Name	Rev
C	FX505DU	1.1

Date: Tuesday, March 12, 2019 Sheet 23 of 72


+3VS
+1.8VSUS
CLK_REQ_WLAN#_R R2481 10KOhm
CLK_REQ_LAN#_R R2408 10KOhm
CLK_REQ_SSD#_R R2482 10KOhm
CLK_REQ_PEG#_R R2483 10KOhm
CLK_LPC0_R R2488 10KOhm
GPU_ALERT# R2486 10KOhm
DGPU_HOLD_RST# R2458 10KOhm
U0301E
3.3VS GPIO
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121
LPC :3.3V
EGPIO70/SD_CLK
LPC_PD_L/SD_CMD/AGPIO21
LAD0/SD_DATA0/EGPIO104
LAD1/SD_DATA1/EGPIO105
LAD2/SD_DATA2/EGPIO106
LAD3/SD_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
3.3VSUS GPIO
LPC_RST_L/SD_WP_L/AGPIO32
AGPIO68/SD_CD
LPC_PME_L/SD_PWR_CTRL/AGPIO22
1.8VSUS GPIO
SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/AGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108
SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DAT1
SPI_DO/ESPI_DAT0
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L/EGPIO118
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29
1.8VS GPIO
UART0_RXD/EGPIO136
UART0_TXD/EGPIO138
UART0_RTS_L/UART2_RXD/EGPIO137
UART0_CTS_L/UART2_TXD/EGPIO135
UART0_INTR/AGPIO139
3.3VS GPIO
EGPIO141/UART1_RXD
EGPIO143/UART1_TXD
EGPIO142/UART1_RTS_L/UART3_RXD
EGPIO140/UART1_CTS_L/UART3_TXD
AGPIO144/UART1_INTR
#55560 PPR Vol3 Section13.2.16.1
can not find GPIO 118 description
X48M_OSC
X48M_X1
X48M_X2
RSVD_23
RSVD_24
RTCCLK
X32K_X1
X32K_X2
CLK_REQ_WLAN# / CLK_REQ_LAN#
CLK_REQ_SSD# / CLK_REQ_PEG#
CLK_PCIE_WLAN_PCH / CLK_PCIE_WLAN#_PCH
CLK_PCIE_LAN_PCH / CLK_PCIE_LAN#_PCH
CLK_PCIE_SSD_PCH / CLK_PCIE_SSD#_PCH
CLK_PCIE_PEG_PCH / CLK_PCIE_PEG#_PCH
GPU_ALERT# 74
DGPU_HOLD_RST# 74
DGPU_PWROK 74,89,92
NVVDD_PWROK 87,89,91,92,96
VGA_DDR_PG 74,89,92
SW_RTCRST 30
EXT_SCI# 30
LPC_RST#_R 30
CLK_KBCPCI_PCH 30
EDP_OD_EN 45
RCIN# 30
SPI_CLK 12,28
SPI_SO 28
SPI_SI 28
SPI_WP# 28
SPI_HOLD# 28
SPI_CS#0 28
UART0_DEBUG_TXD 44
UART0_DEBUG_RXD 44
LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD2 30,44
LPC_AD3 30,44
PM_CLKRUN# 30
CLK_DEBUG 44
INT_SERIRQ 30,44
LPC_FRAME# 30,44
R1.0 0609
EXT_SCI# R2403 10KOhm +3VSUS
XTAL_48M_IN R2432 0Ohm
XTAL_48M_OUT R2433 100Ohm
XTAL_32K_X1 R2452 20MOhm
X2402 32.768KHZ 07T080000075 +/-20ppm/9PF
C2404 10PF/50V N/A
C2403 10PF/50V N/A
SP2402 0Ohm
SP2401 0Ohm
R1.1 0724
X2401 48MHZ
C2402 27PF/50V
C2401 27PF/50V
R2418 1MOhm
+VCC_RTC
Q2401 2N7002
R1.0 0410
R2422 1KOhm
+RTC_1.5V
U2401 AP2138N-1.5TRG1
R1.1 0627 For AMD
RTC_3V3_IN
R2420 1KOhm
+RTC_AC
+3VA
R2425 0Ohm
D2401 0.8V/0.2mA
+RTC_BAT
C2407 1UF/6.3V
1AT200000068
R2453 0Ohm
+RTCBAT
CON2401 BATT_HOLDER_2P
12T20GBSM000
JRST2401 SGI_JUMP
R2406 10KOhm
CMOS Settings | JRST2401
Clear CMOS | Shunt
Keep CMOS | Open (Default)
+3VS
+1.8VS
R2459 10KOhm
R2461 10KOhm
R2477 10KOhm
R2460 10KOhm
R2462 10KOhm
R2478 10KOhm
R2467 10KOhm
R2469 10KOhm
R2468 10KOhm
R2470 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
PCB_ID3
PCB_ID4
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :PCH(5)_CLK
BG1-HW3 R0
Engineer: Johnson Huang
Size Custom
Project Name FX505DU
Rev 1.1
Date: Tuesday, March 12, 2019
Sheet 24 of 72



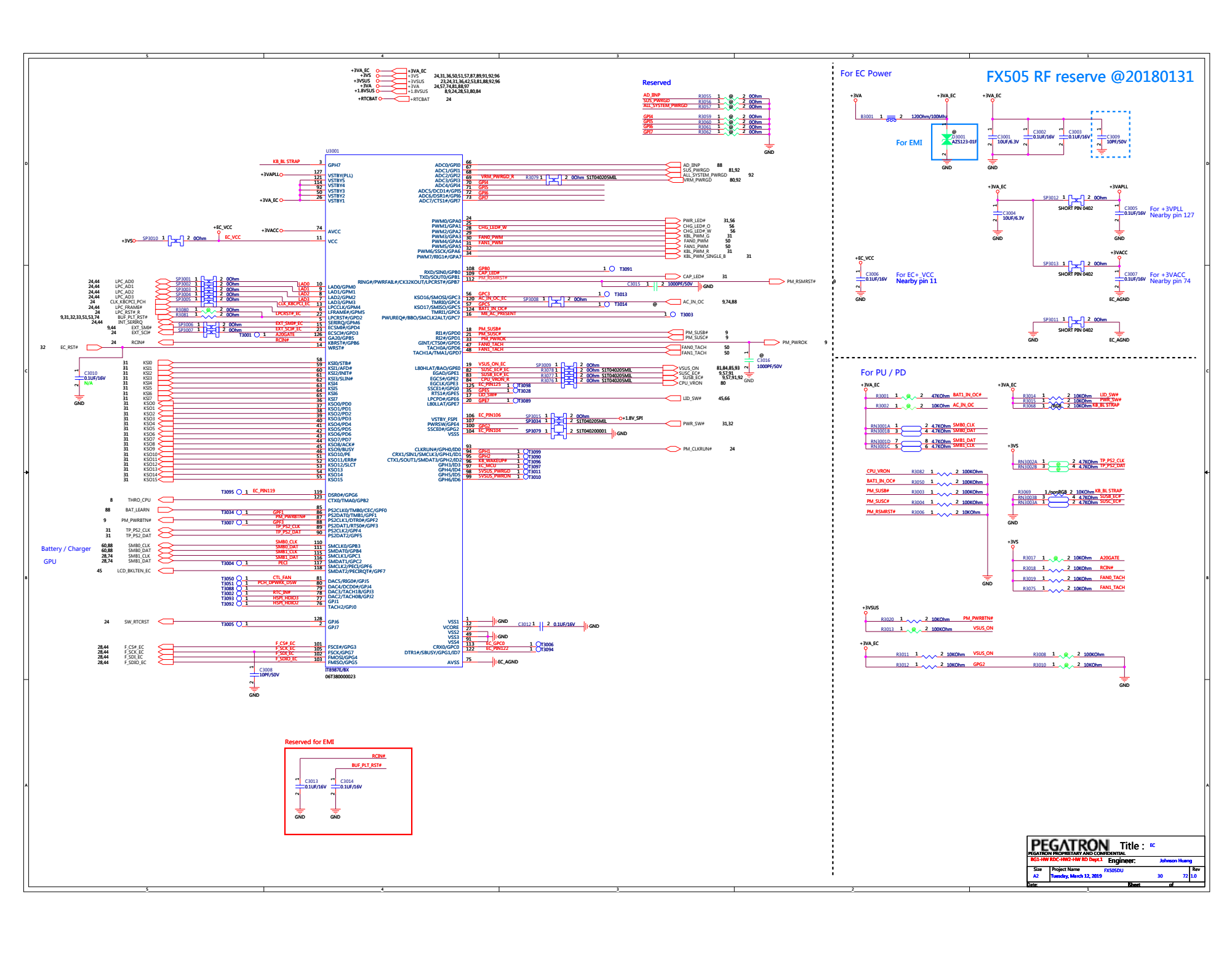


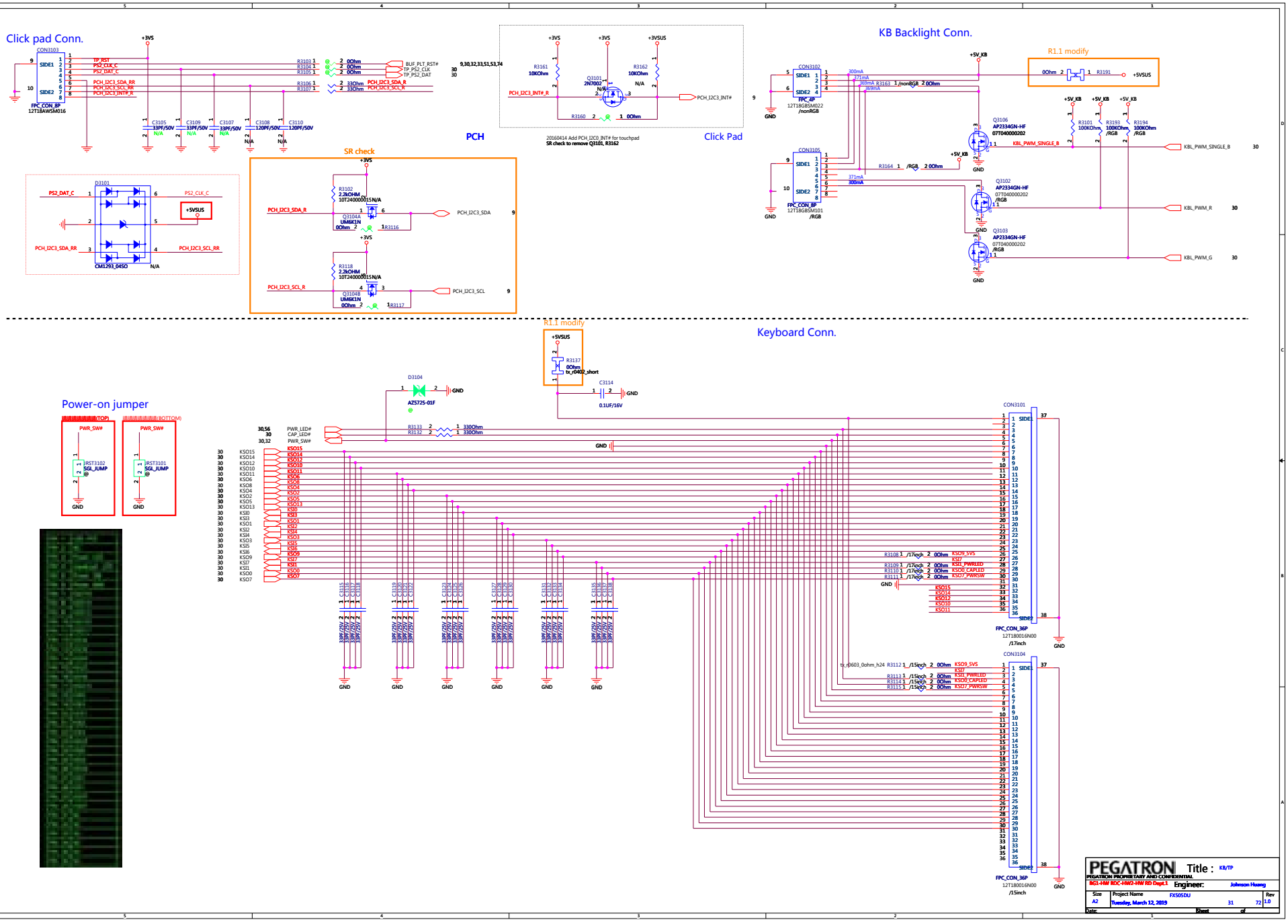
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
X51-HW3 RD

Title : PCH(9)_SPI_SMB
Engineer: Johnson Huang

Size	Project Name	Rev
Custom	FX505DU	1.1

Date: Tuesday, March 12, 2019 Sheet 28 of 72

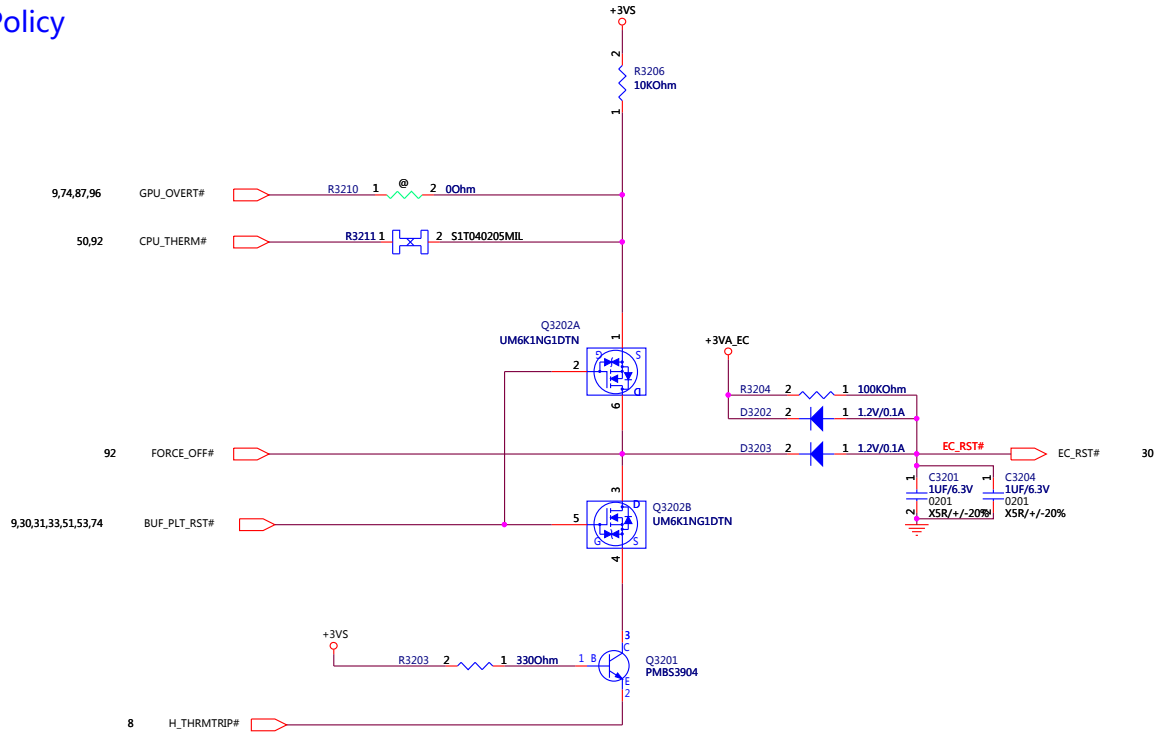

For EC Power
FX505 RF reserve @20180131
For EMI
For +3VPLL
Nearby pin 127
For EC+_VCC
Nearby pin 11
For +3VACC
Nearby pin 74
For PU / PD
Reserved
Reserved for EMI
Battery / Charger
GPU
U3001
IT8987E/BX
06T380000023
PEGATRON
Title : EC
PEGATRON PROPRIETARY AND CONFIDENTIAL
RC1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Project Name FX505DU
Tuesday, March 12, 2019
Rev 1.0


Click pad Conn.
PCH
Click Pad
SR check
KB Backlight Conn.
R1.1 modify
Power-on jumper
Keyboard Conn.
R1.1 modify
PEGATRON
Title : KB/TP
Engineer:
Johnson Huang
FX505DU
Tuesday, March 12, 2019

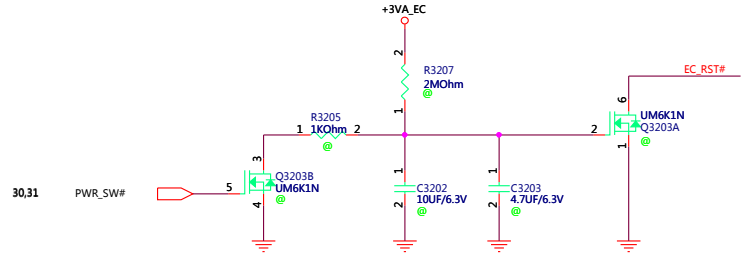
+3VA_EC +3VA_EC

+3VS +3VS 24,31,36,50,51,57,87,89,91,92,96

Thermal Policy



EC reset



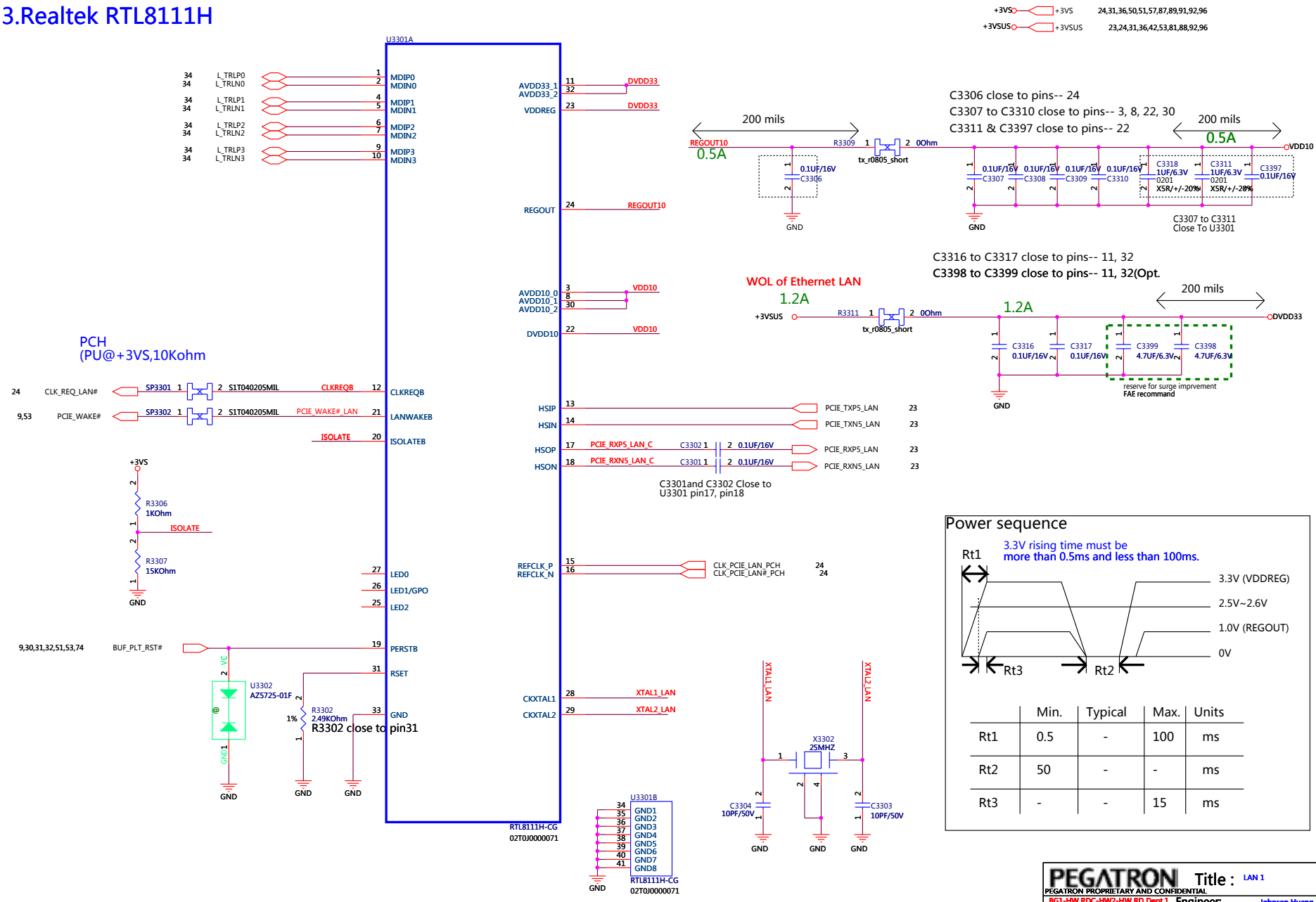
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 32 of 72	

33.Realtek RTL8111H

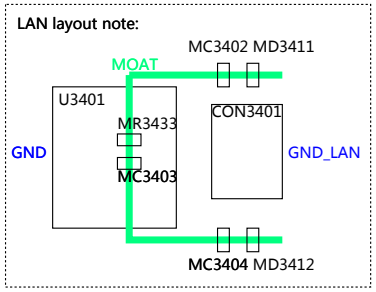


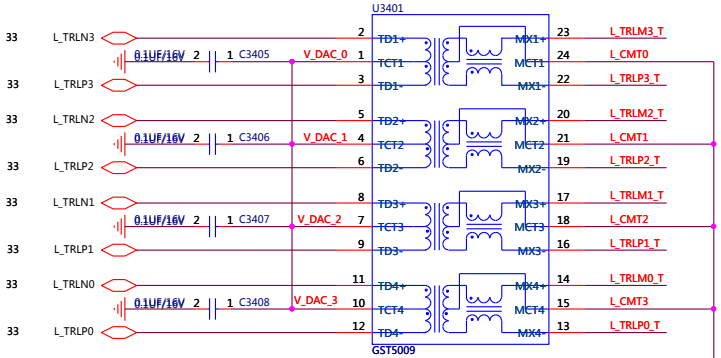
Power sequence

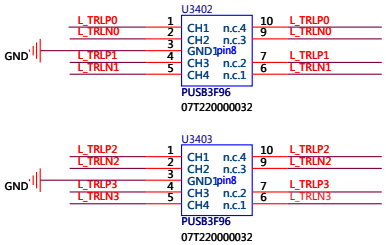
	Min.	Typical	Max.	Units
Rt1	0.5	-	100	ms
Rt2	50	-	-	ms
Rt3	-	-	15	ms

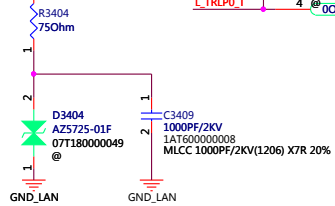
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : LAN 1
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size: A3
Project Name: FX505DU
Rev: 1.0
Date: Tuesday, March 12, 2019
Sheet 33 of 72

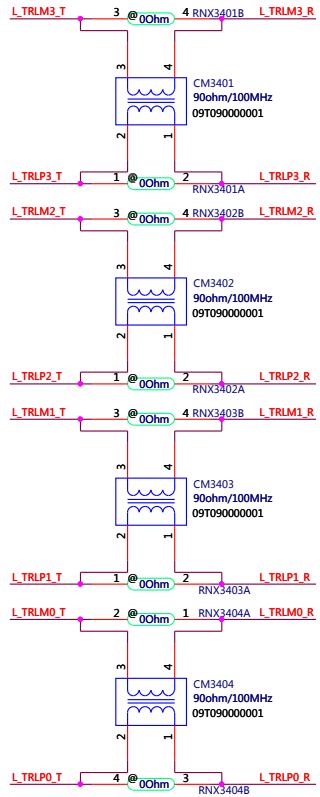
34.Transformer/RJ45

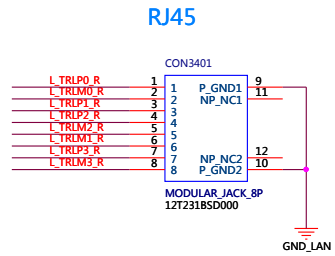


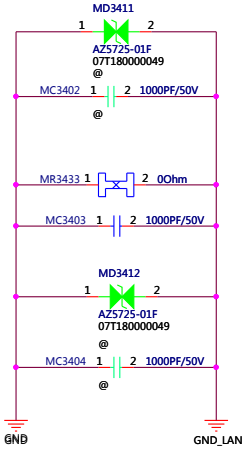












PEGATRON

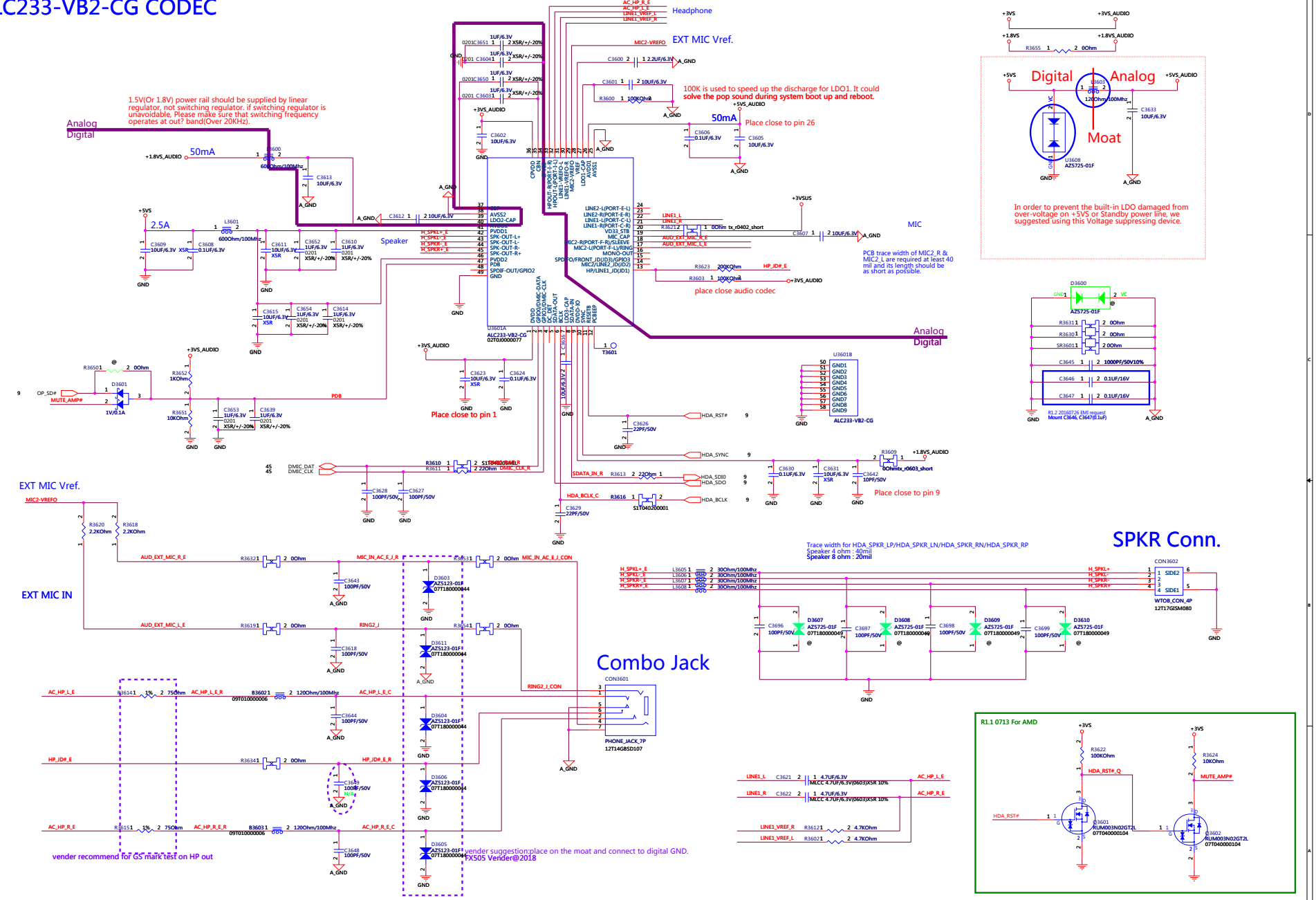
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LAN 2

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

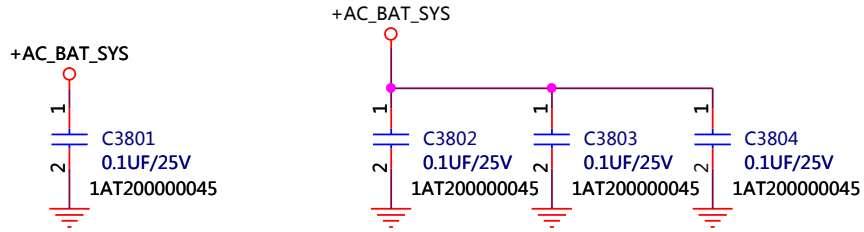
Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 34 of 72	

ALC233-VB2-CG CODEC



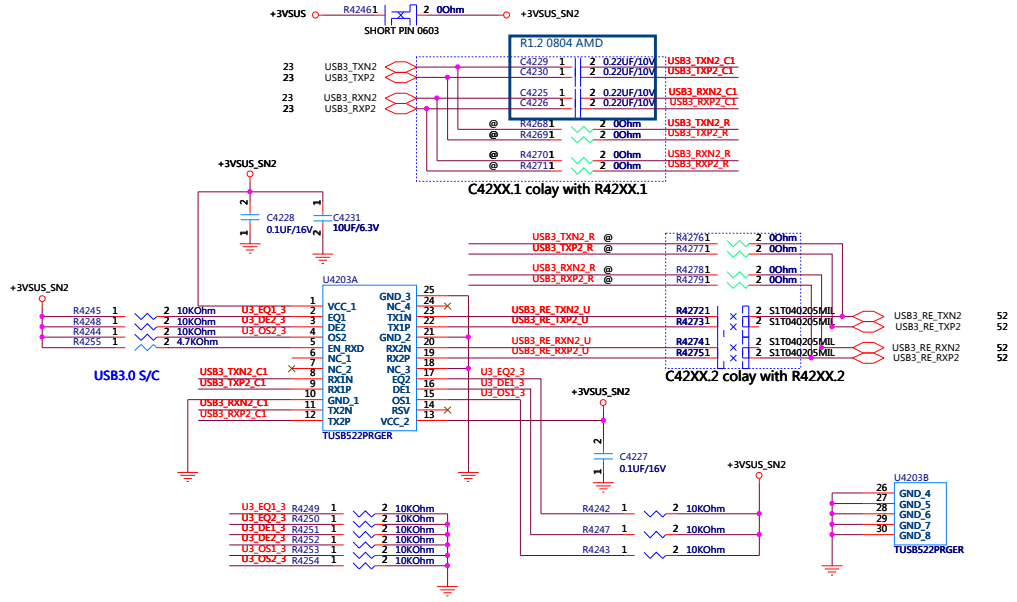
PEGATRON	Title :	AUDIO CODEC	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BST-HW RDC-MK2-HW RD Dept.	Engineer:	Johnson Huang	
Size	Project Name	FX505DU	Rev
Custom	Tuesday, March 12, 2019	36 72	1.0
Date:		Sheet of	

+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,84,88,97

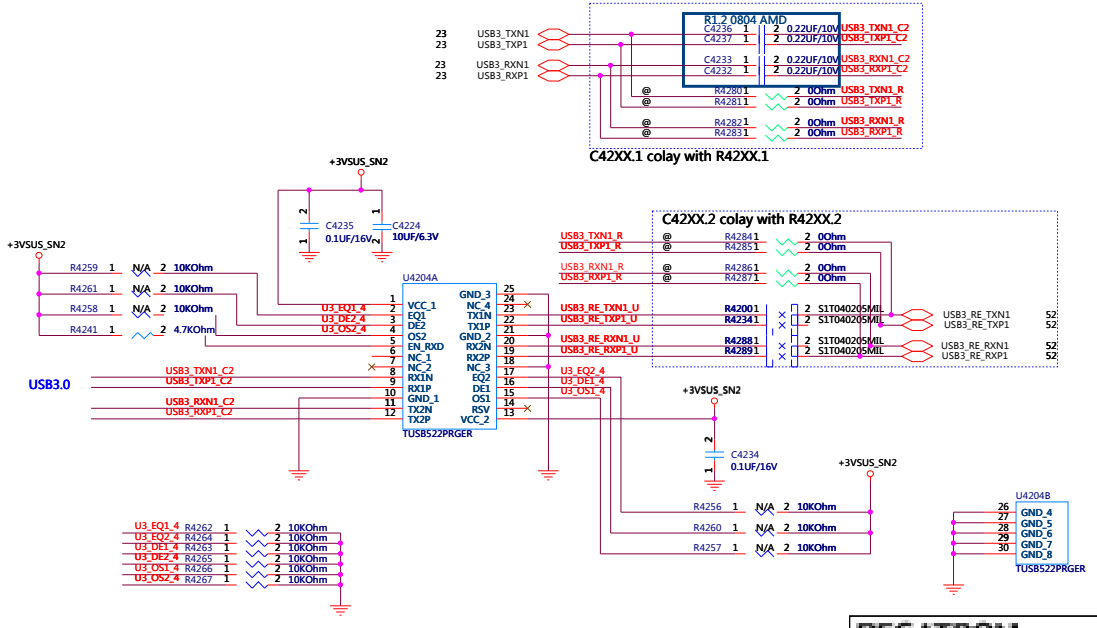


Title	<Title>	
Size A	Document Number FX505DU	Rev 1.1
Date: Tuesday, March 12, 2019	Sheet 38 of 72	

USB 3.0 PORT 0 S/C (Gen 1)



USB 3.0 PORT 1 (Gen 1)



PEGATRON Title : USB3 repeater

PEGATRON PROPRIETARY AND CONFIDENTIAL

BGT-HW3 RD

Engineer: Johnson Huang

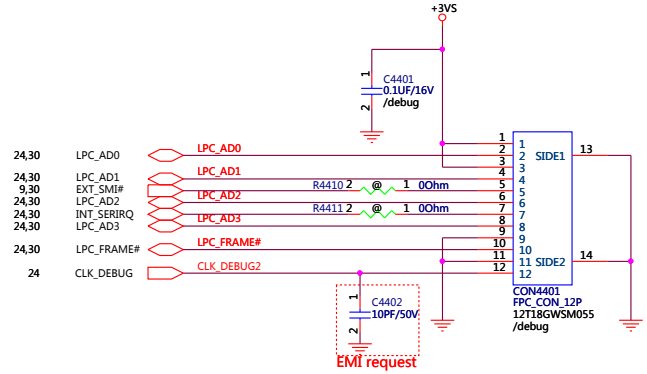
Size	Project Name	Rev
Custom	FX505DU	1.1

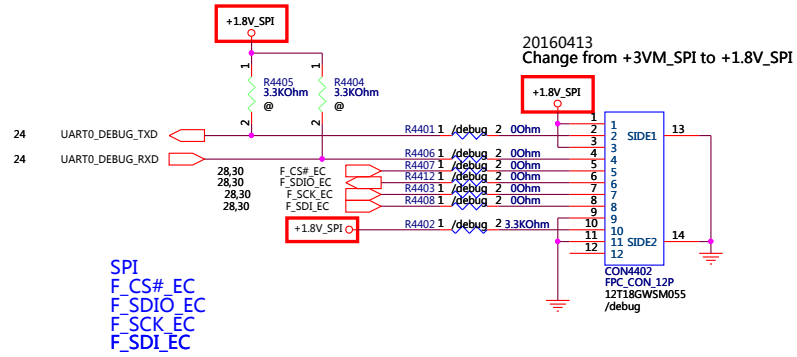
Date: Tuesday, March 12, 2019 Sheet 42 of 72

+3VS +3VS 24,31,36,50,51,57,87,89,91,92,96

+3VSUS +3VSUS 23,24,31,36,42,53,81,88,92,96

+3VM_SPI +3VM_SPI





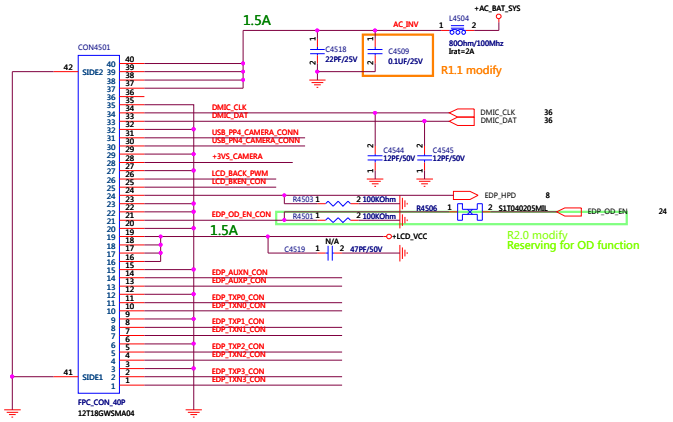
PEGATRON Title : DEBUG

PEGATRON PROPRIETARY AND CONFIDENTIAL

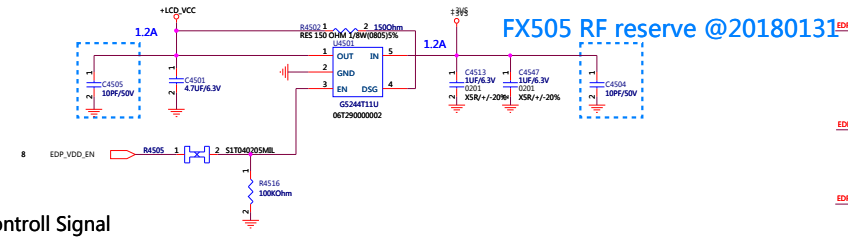
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 44 of 72	

eDP Conn.

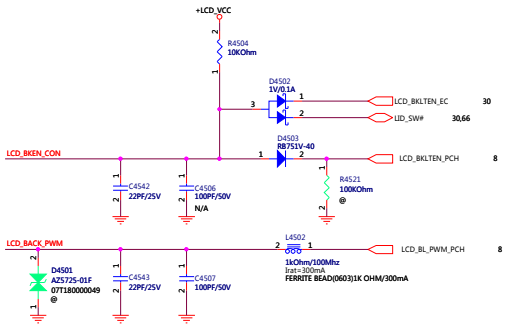


LCD VDDEN / +LED_VCC

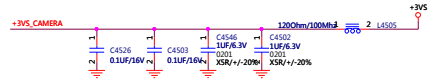


FX505 RF reserve @20180131

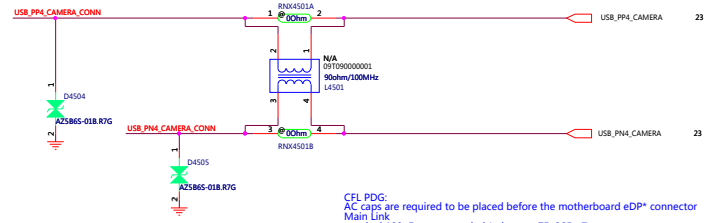
Controll Signal



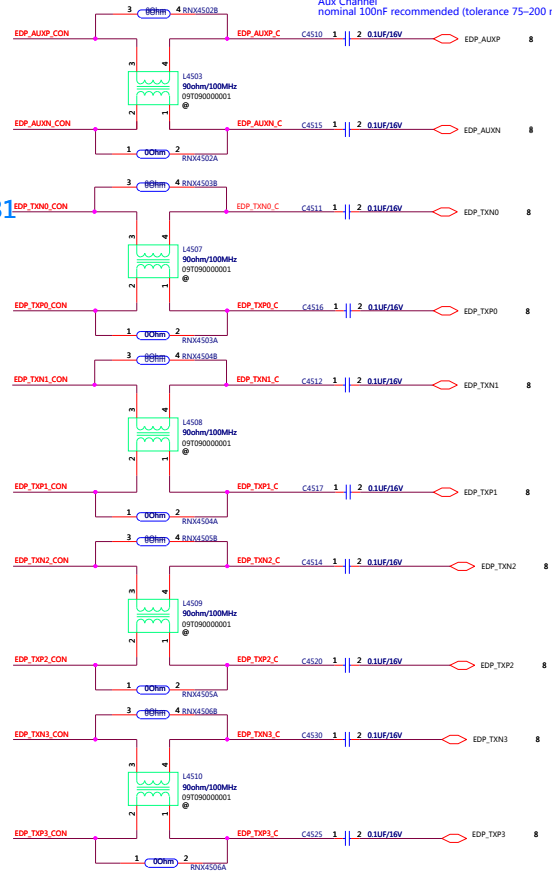
Camera Signal



CAMERA

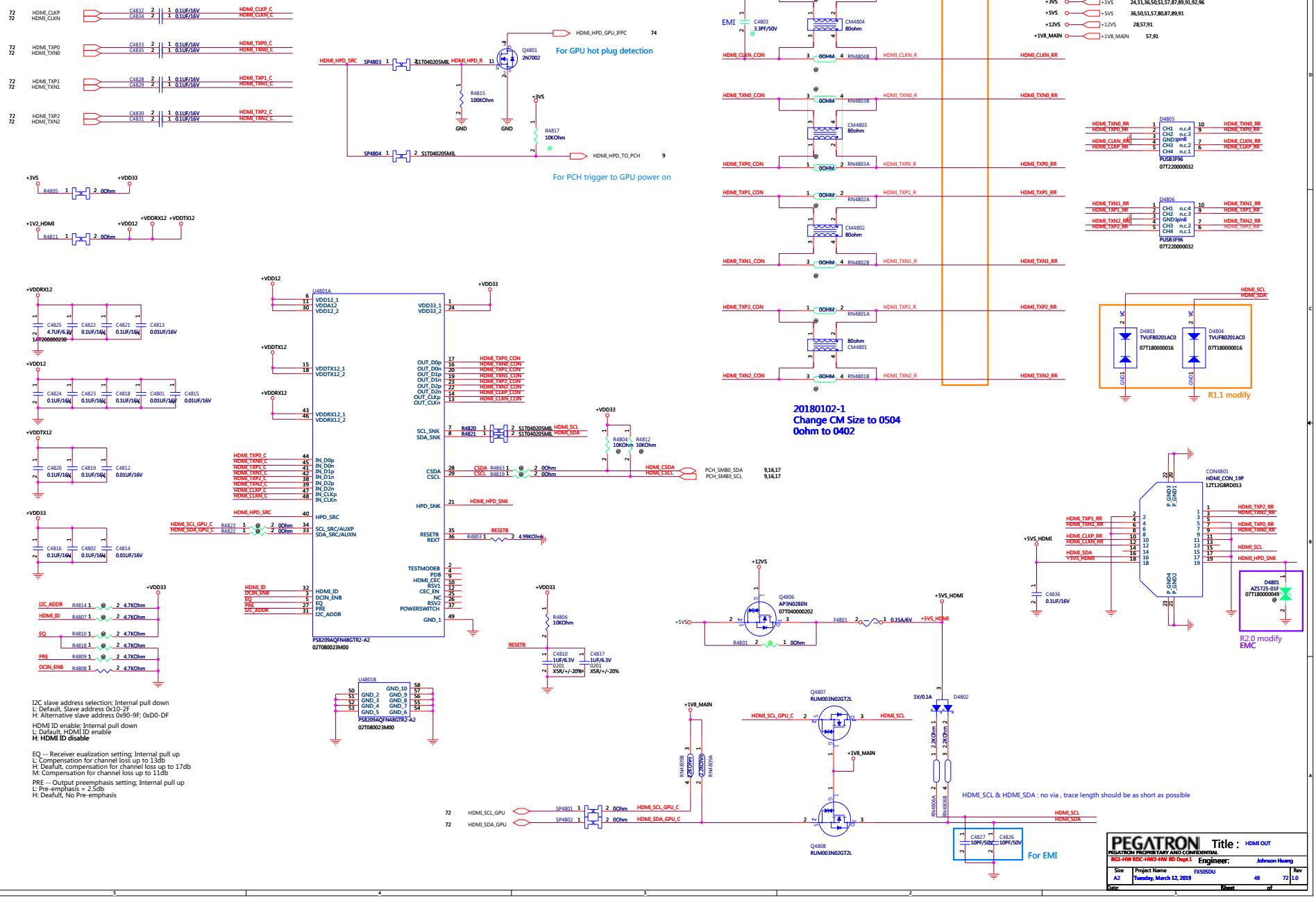


CFL PDG:
AC caps are required to be placed before the motherboard eDP* connector
Main Link
nominal 100nF recommended (tolerance 75~265 nF)
Aux Channel
nominal 100nF recommended (tolerance 75~200 nF)



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EDP/MIC
BG1-HW RDC-HW2-HW RD Dept.1
Engineer: Johnson Huang
Size: A2
Project Name: FX505DU
Rev: 1.0
Date: Tuesday, March 12, 2019
Sheet: 45 of 72

HDMI



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI OUT

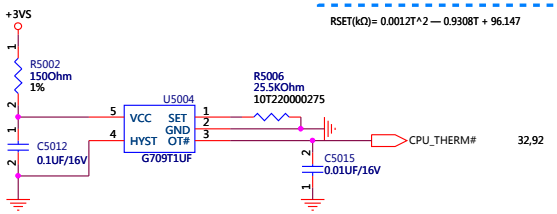
RCI-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
A2	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 48 of 72	

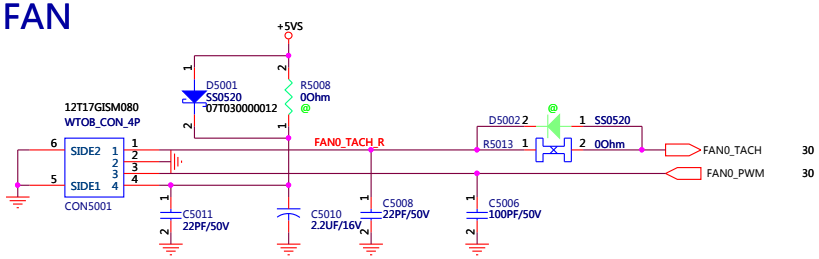
CPU Thermal Sensor

temperature set=85 C

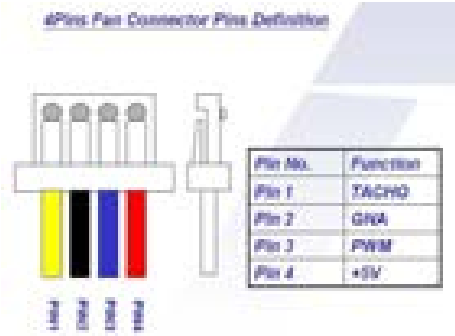
RSET(kΩ)= 0.0012T^2 — 0.9308T + 96.147



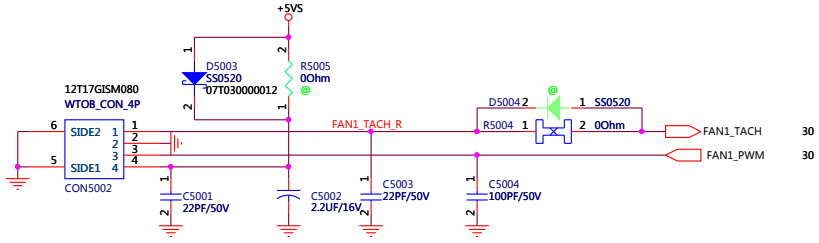
CPU FAN



EC(PU@+3VS,10Kohm



GPU FAN



EC(PU@+3VS,10Kohm

PEGATRON Title : FAN/THERMAL

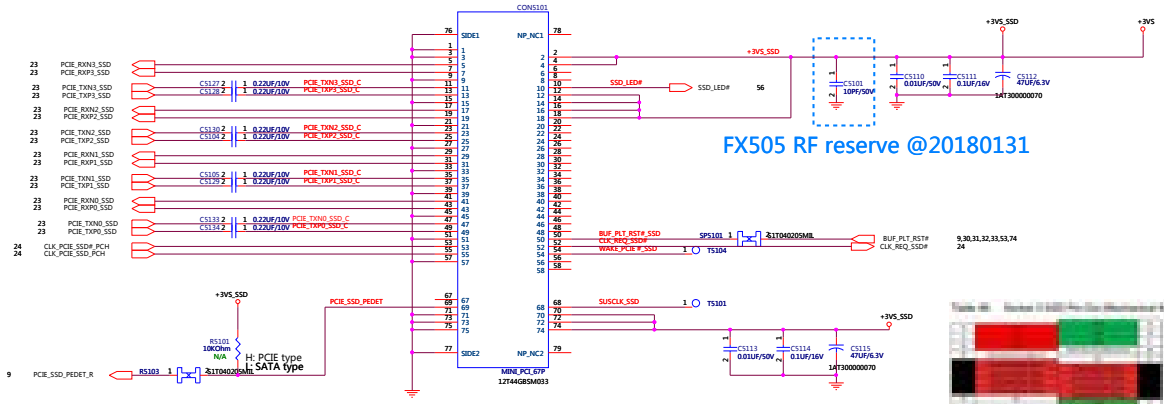
PEGATRON PROPRIETARY AND CONFIDENTIAL

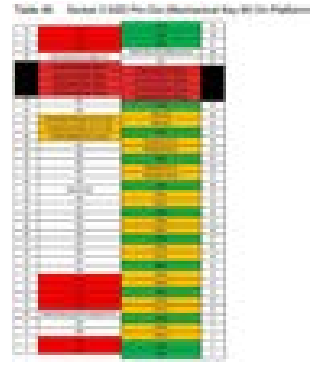
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name		Rev
A3	FX505DU		1.0
Date: Tuesday, March 12, 2019	Sheet 50	of 72	

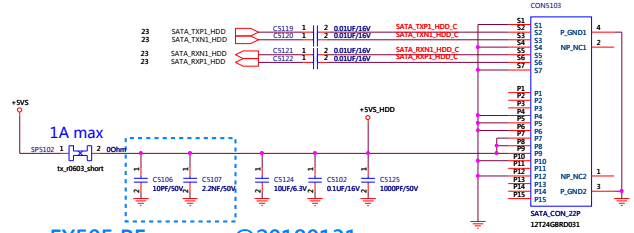
SSD/HDD

M.2 2280 KEY-M



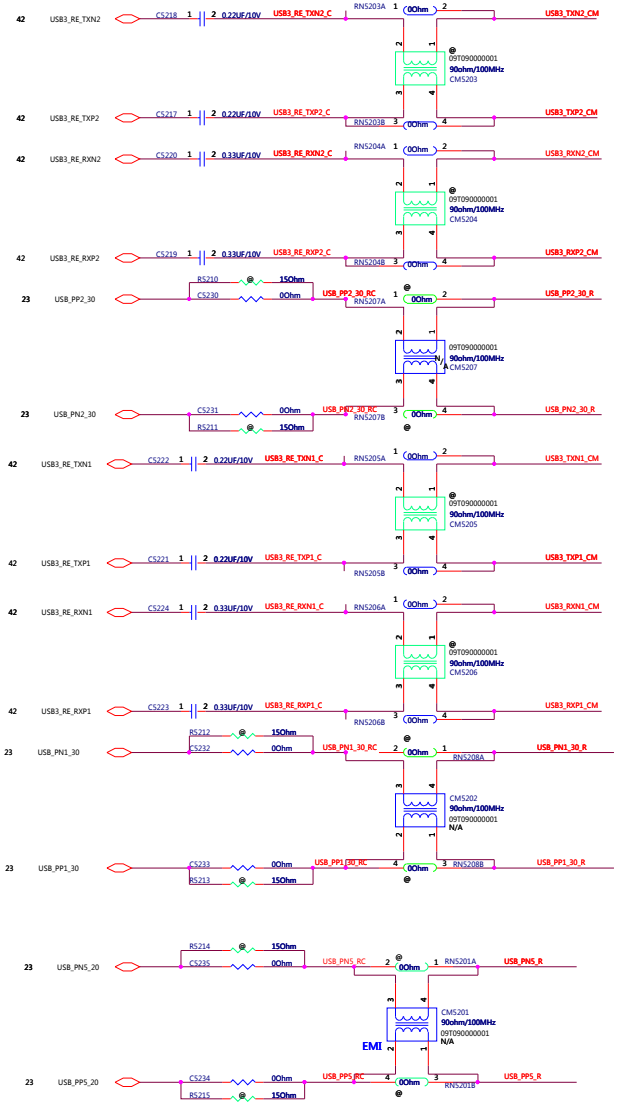


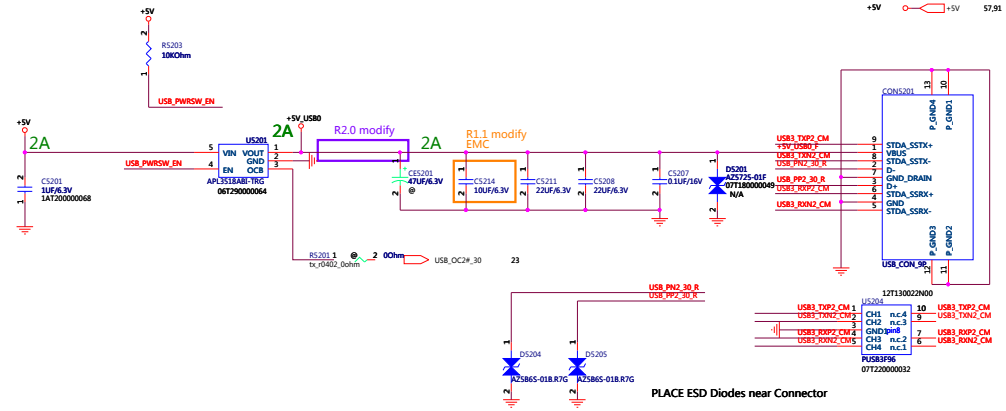
SATA Conn. 2.5"HDD

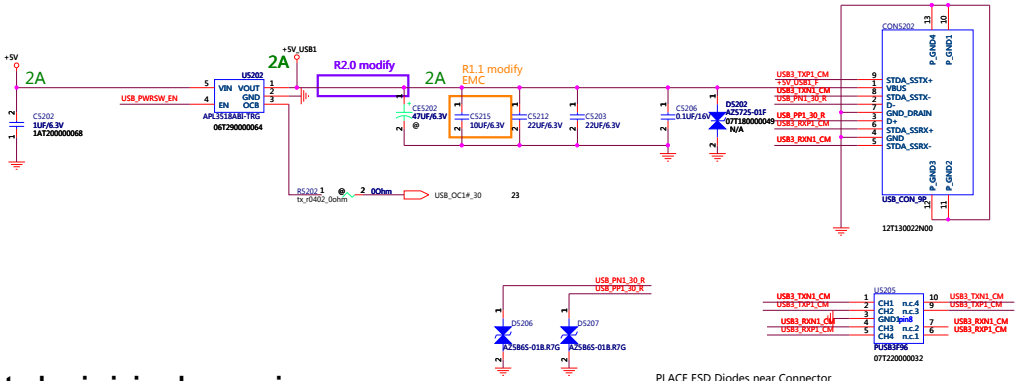


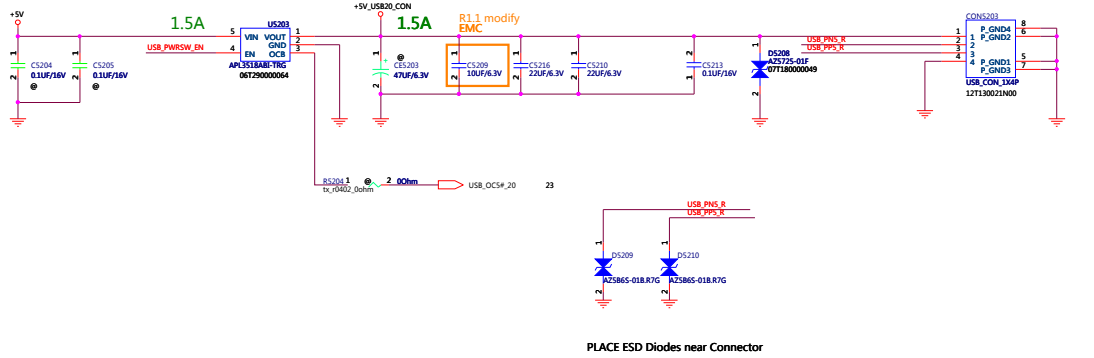
PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL		Title : SSD/HDD	
BU1-HW BDC-HMO-HW BD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: FX505DU	Rev: 1.0	
Date: Tuesday, March 12, 2019	Sheet: 51 of 72		

52.USB3.0









PEGATRON Title : USB JCAK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW MDC-HW2-HW RD Dept.1 Engineer: Johnson Hsiang

Size	Project Name	Rev
A2	FX505GE	1.0
Date: Tuesday, March 12, 2019	Sheet 52 of 72	

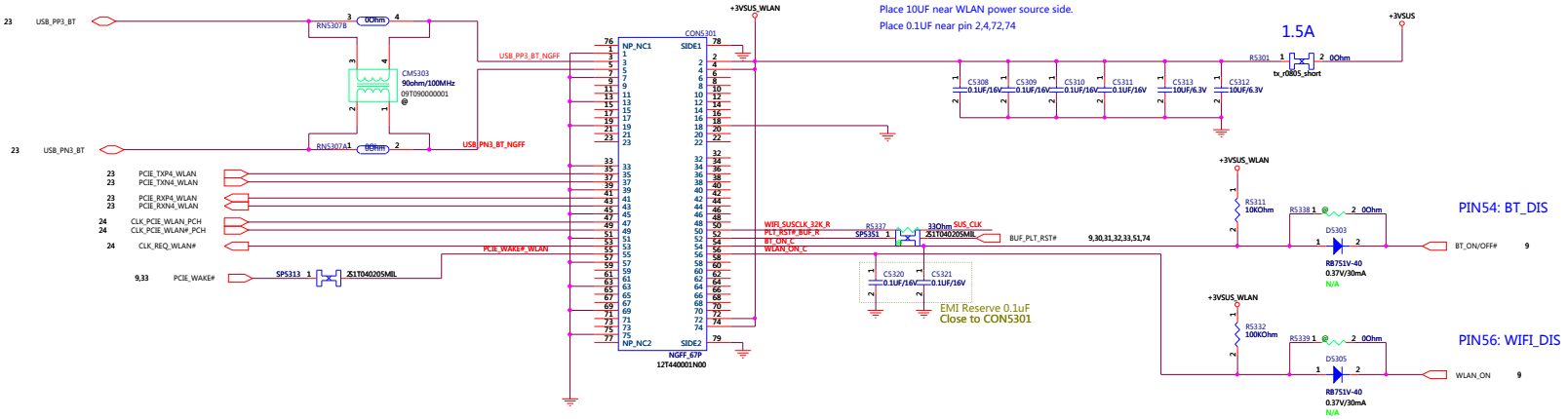
WLAN+BT

+3VSUS +3VSUS 9,11,12,23,24,30,31,33,36,42,74,81,88,92,96
+1.8VSUS +1.8VSUS 8,9,11,12,24,28,80,84

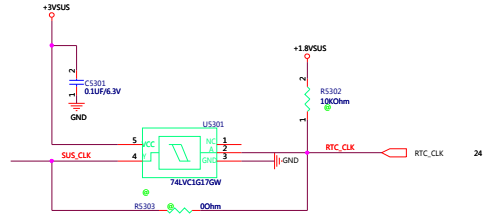
M.2 2230 KEY-E

WLAN bypass capactors:

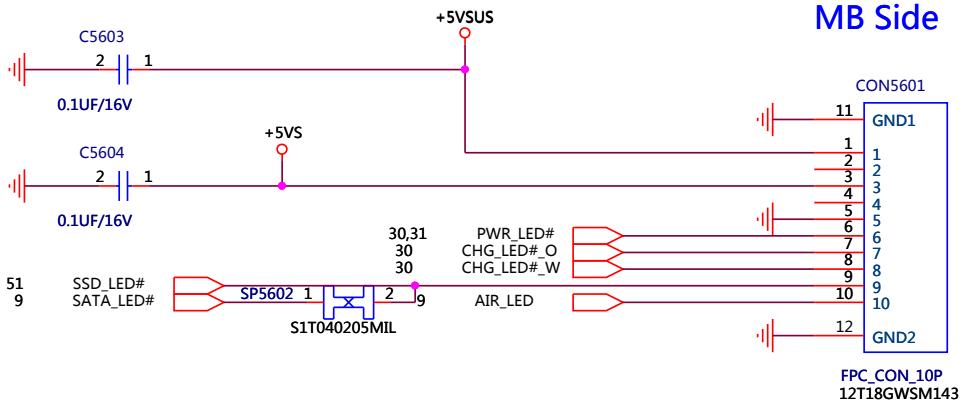
Place 10UF near WLAN power source side.
Place 0.1UF near pin 2,4,72,74



WLAN_SUS_CLK Update



PEGATRON Title : WLAN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW BDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A2 | Project Name EX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 53 of 72



+5VSUS	+5VSUS	31,81
+5VS	+5VS	36,50,51,57,80,87,89,91

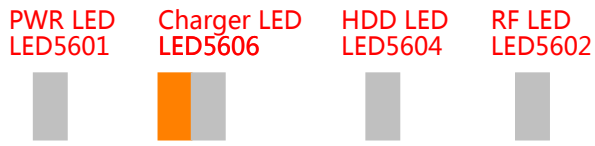
Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
High -> airplane mode ON -> LED ON
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION



HDD LED

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

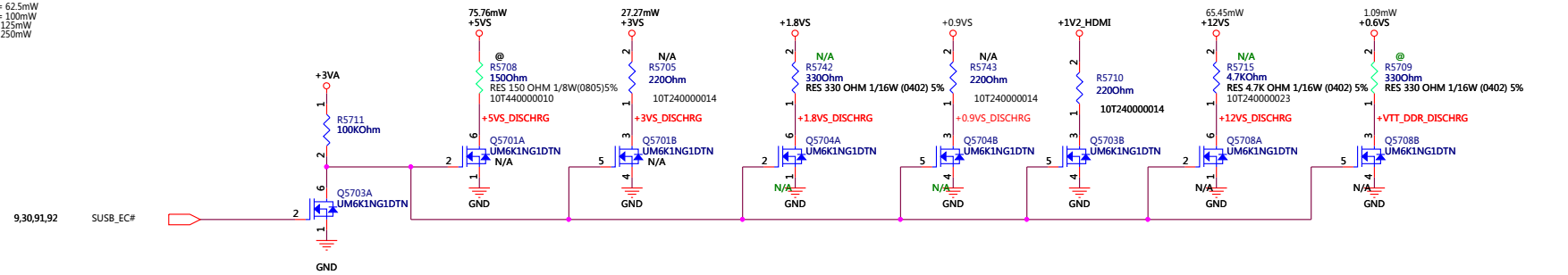
Title : LED

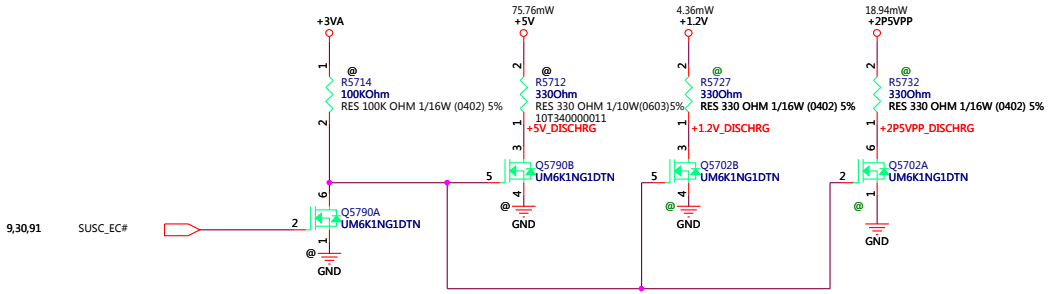
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang

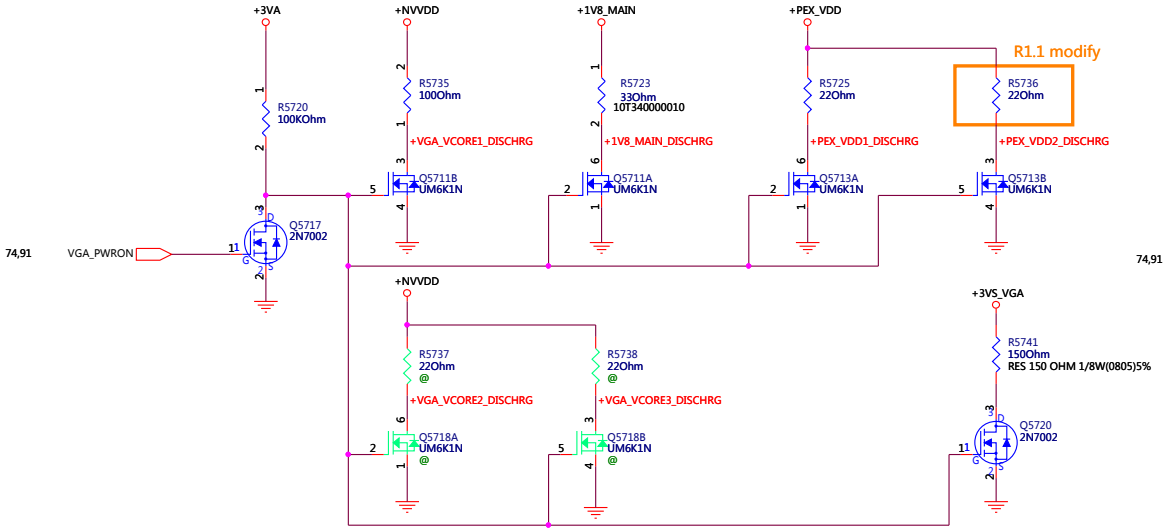
Size	Project Name	Rev
A4	FX505DU	1.0

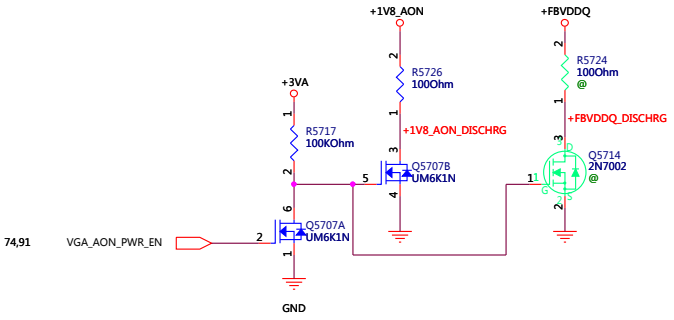
Date: Tuesday, March 12, 2019 Sheet 56 of 72

V^2/R
0402 = 1/16W = 62.5mW
0603 = 1/10W = 100mW
0805 = 1/8W = 125mW
1206 = 1/4W = 250mW







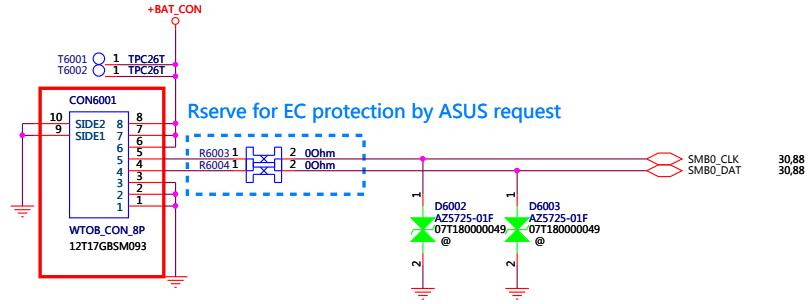


PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1

Title : DISCHARGE
Engineer: Johnson Huang

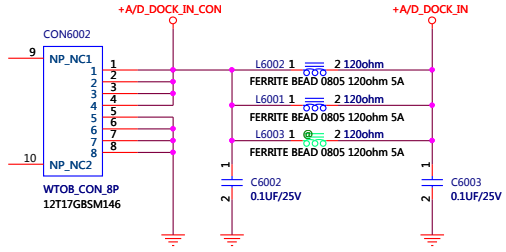
Size	Project Name	Rev
A3	FX505DU	1.0
Date: Tuesday, March 12, 2019	Sheet 57 of 72	

Battery Conn.



ABBA assign: 1217-01UG0AS(1217-017L000)，doesn't include 1217-01EG000 (the same pool)

AC in Conn.

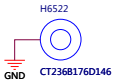


FX505DD/DT N17P/N18P Adaptor: 120W (6.32A)
FX505DU N18E-G0 Adaptor: 180W (9.23A)

PEGATRON Title : BAT/AC IN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size A3 | Project Name FX505DU | Rev 1.0
Date: Tuesday, March 12, 2019 | Sheet 60 of 99

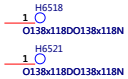
65.NUT,Screw hole,Tooling hole

M.2 SSD NUT:



Tooling hole

drill 3*3.5

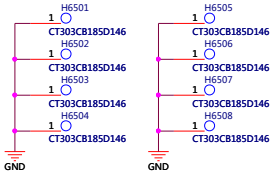


drill 1.7

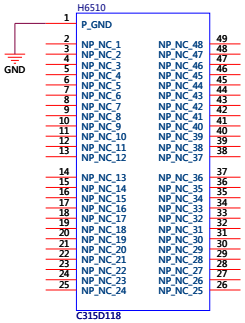
drill 2.2*1.7

Screw hole

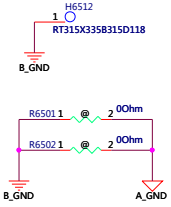
B group:
CPU GPU bracket hole



D group:

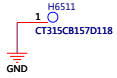


Near Audio Jack
TOP: square 8
BOT: phi 8 drill 3

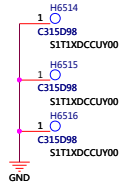


E:
TOP: phi 7 drill 6
BOT: phi 7 drill 6

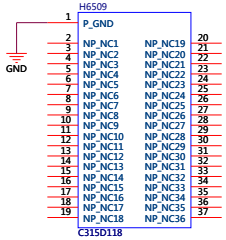
F:
TOP: phi 8 drill 3
BOT: phi 4 drill 3

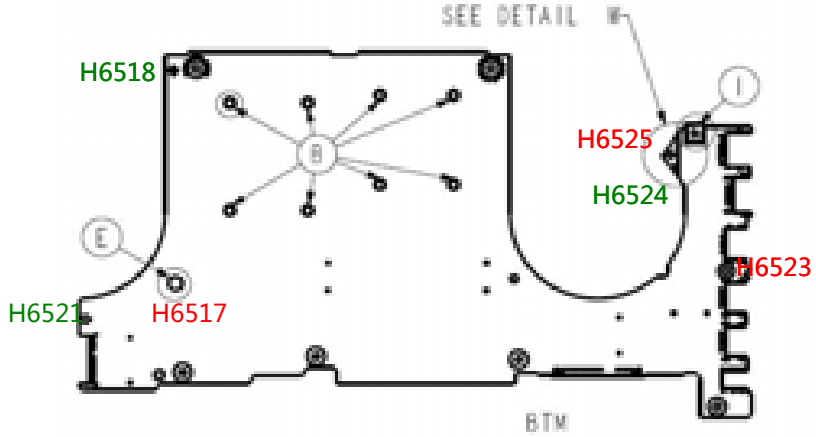


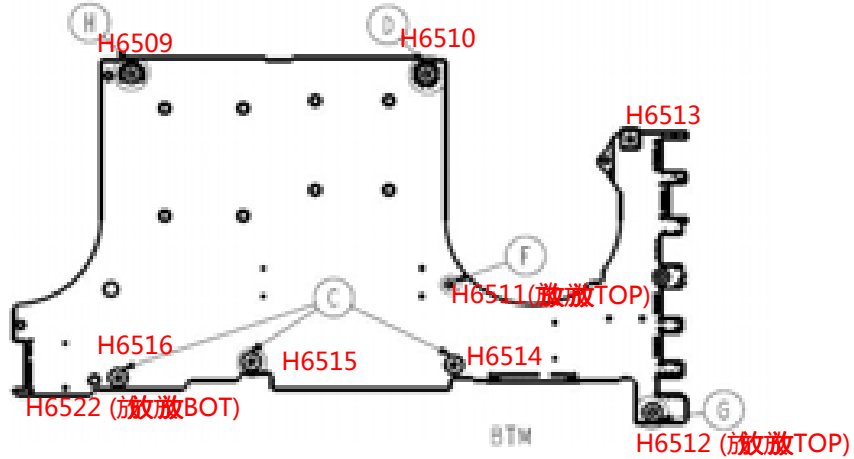
C group:
TOP: phi 8 drill 2.5
BOT: phi 8 drill 2.5



H group:

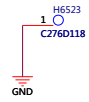






I group:
TOP: square8*8.5 drill 2.5
BOT: square8*8.5 drill 2.5

TOP: phi 7 drill 3
BOT: phi 7 drill 3

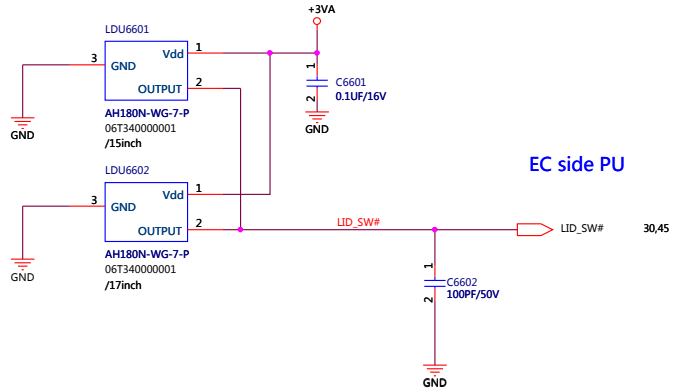


TOP: phi 3 drill 2.5
BOT: phi 3 drill 2.5

PEGATRON Title : NUT/HOLE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: Johnson Huang
Size: Custom | Project Name: FX505DU | Rev: 1.0
Date: Tuesday, March 12, 2019 | Sheet 65 of 72

+3VA +3VA 24,57,74,81,88,97

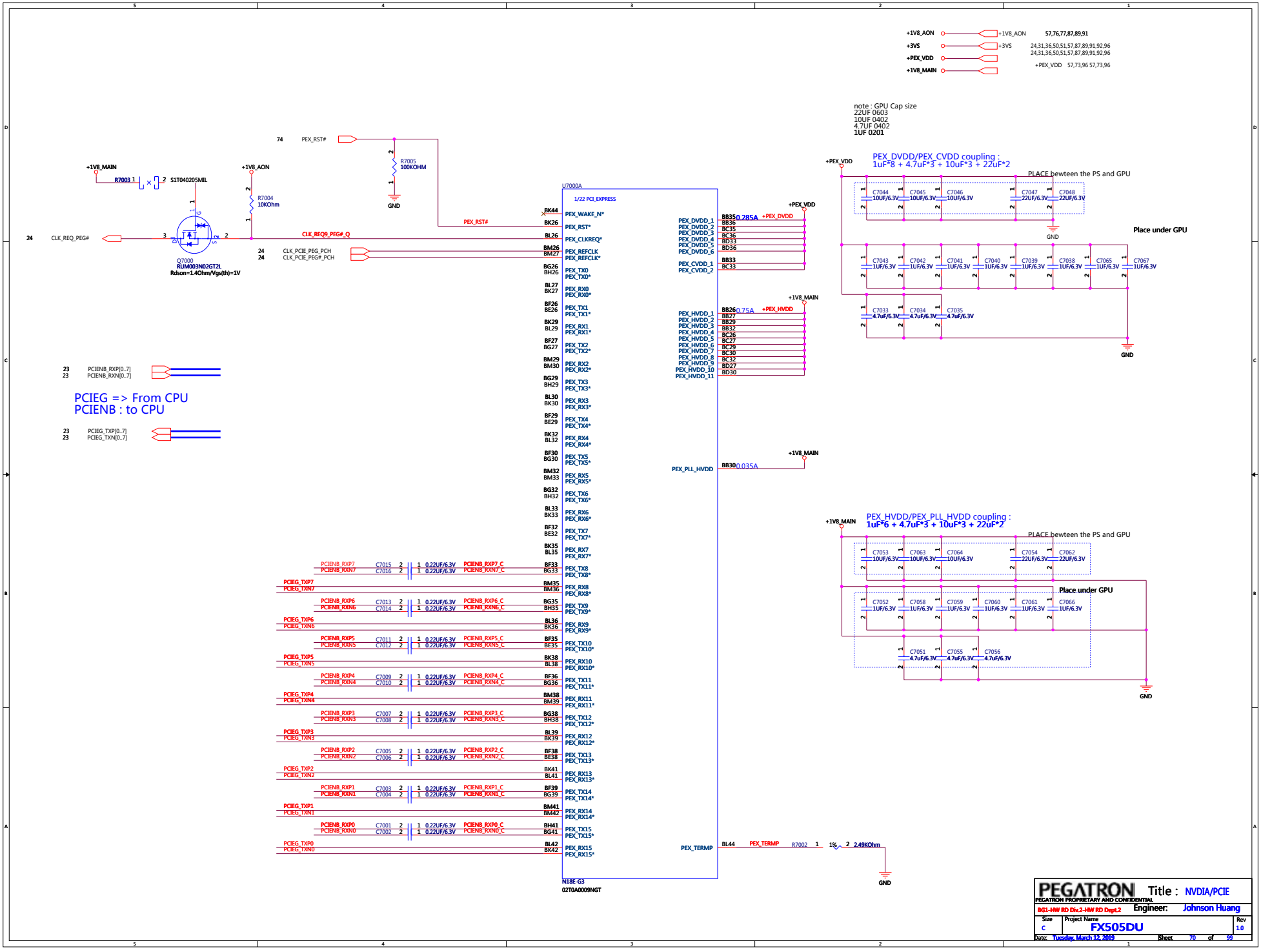
Hall sensor



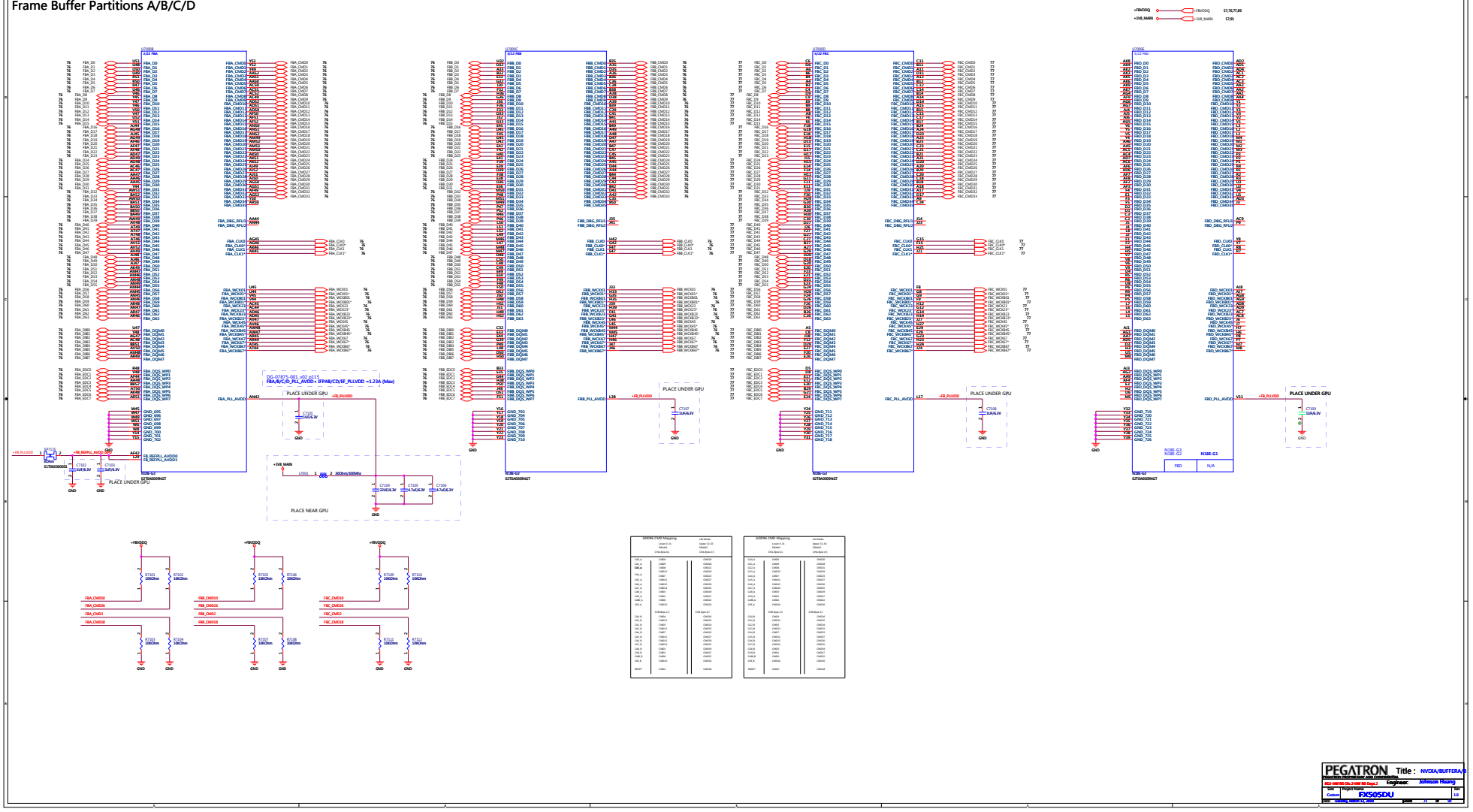
EC side PU

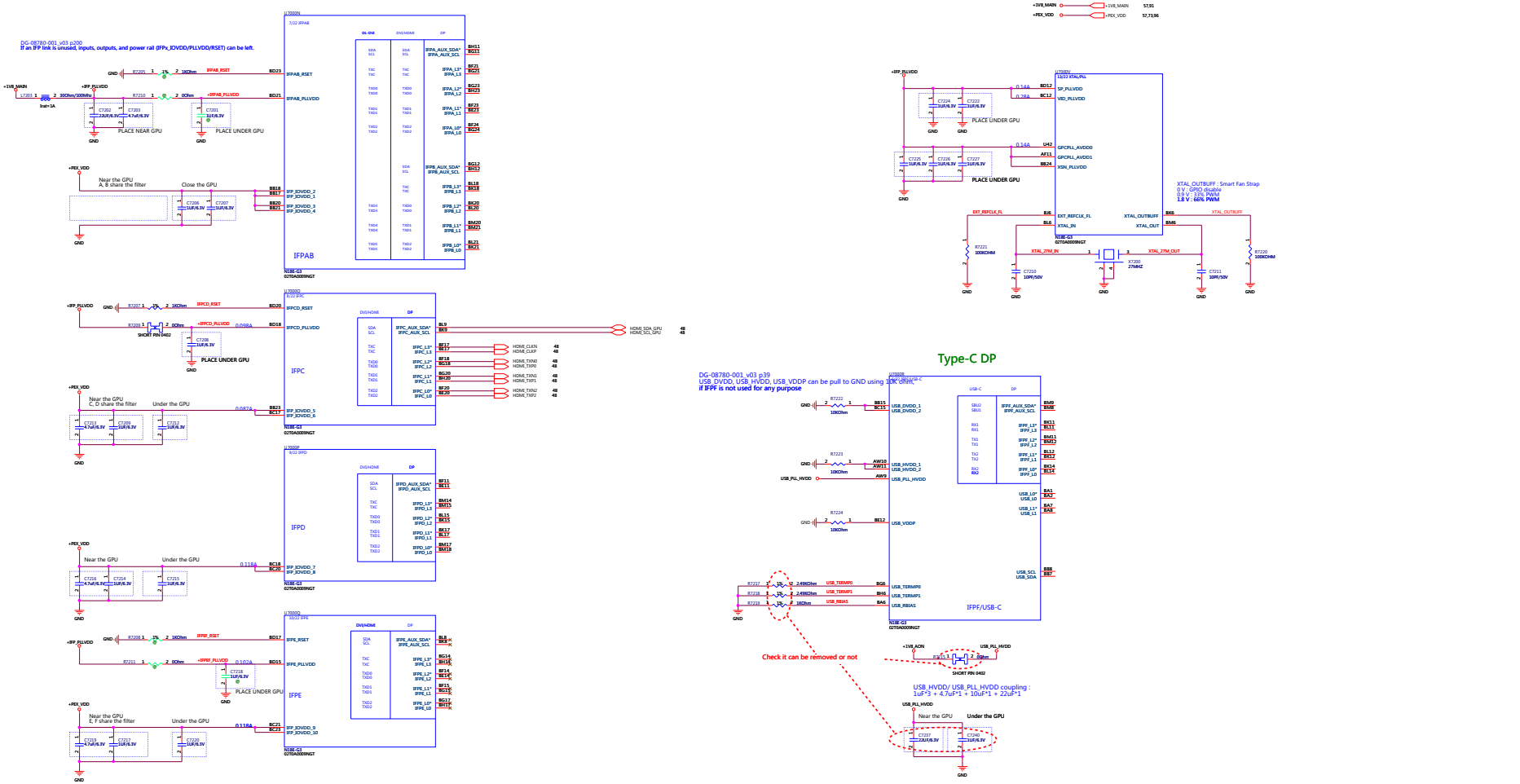
PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON	Title : TO DB	
BG1-HW RDC-HW2-HW RD Dept.1	Engineer: Johnson Huang	
Size: A3	Project Name: FX505DU	Rev: 1.0
Date: Tuesday, March 12, 2019	Sheet 66 of 72	


+1V8_AON
+3VS
+PEX_VDD
+1V8_MAIN
57,76,77,87,89,91
24,31,36,50,51,57,87,89,91,92,96
24,31,36,50,51,57,87,89,91,92,96
+PEX_VDD 57,73,96 57,73,96
note : GPU Cap size
22UF 0603
10UF 0402
4.7UF 0402
1UF 0201
74 PEX_RST#
+1V8_MAIN
R7003 1 2 S1T040205MIL
+1V8_AON
R7004 10KOhm
R7005 100KOHM
GND
24 CLK_REQ_PEG#
Q7000 RUM003N02GT2L
Rdson=1.4Ohm/Vgs(th)=1V
CLK_REQ9_PEG#_Q
24 CLK_REFCLK_PEG_PCH
24 CLK_REFCLK_PEG#_PCH
U7000A
1/22 PCI_EXPRESS
PEX_WAKE_N*
PEX_RST*
PEX_CLKREQ*
PEX_REFCLK
PEX_REFCLK*
PEX_TX0
PEX_TX0*
PEX_RX0
PEX_RX0*
PEX_TX1
PEX_TX1*
PEX_RX1
PEX_RX1*
PEX_TX2
PEX_TX2*
PEX_RX2
PEX_RX2*
PEX_TX3
PEX_TX3*
PEX_RX3
PEX_RX3*
PEX_TX4
PEX_TX4*
PEX_RX4
PEX_RX4*
PEX_TX5
PEX_TX5*
PEX_RX5
PEX_RX5*
PEX_TX6
PEX_TX6*
PEX_RX6
PEX_RX6*
PEX_TX7
PEX_TX7*
PEX_RX7
PEX_RX7*
PEX_TX8
PEX_TX8*
PEX_RX8
PEX_RX8*
PEX_TX9
PEX_TX9*
PEX_RX9
PEX_RX9*
PEX_TX10
PEX_TX10*
PEX_RX10
PEX_RX10*
PEX_TX11
PEX_TX11*
PEX_RX11
PEX_RX11*
PEX_TX12
PEX_TX12*
PEX_RX12
PEX_RX12*
PEX_TX13
PEX_TX13*
PEX_RX13
PEX_RX13*
PEX_TX14
PEX_TX14*
PEX_RX14
PEX_RX14*
PEX_TX15
PEX_TX15*
PEX_RX15
PEX_RX15*
N18E-G3
02T0A0009NGT
PEX_DVDD_1
PEX_DVDD_2
PEX_DVDD_3
PEX_DVDD_4
PEX_DVDD_5
PEX_DVDD_6
PEX_CVDD_1
PEX_CVDD_2
BB35 0.285A +PEX_DVDD
BB36
BC35
BC36
BD33
BD36
BB33
BC33
PEX_HVDD_1
PEX_HVDD_2
PEX_HVDD_3
PEX_HVDD_4
PEX_HVDD_5
PEX_HVDD_6
PEX_HVDD_7
PEX_HVDD_8
PEX_HVDD_9
PEX_HVDD_10
PEX_HVDD_11
BB26 0.75A +PEX_HVDD
BB27
BB29
BB32
BC26
BC27
BC29
BC30
BC32
BD27
BD30
PEX_PLL_HVDD
BB30 0.035A
PEX_TERMP
BL44 PEX_TERMP R7002 1 1% 2 2.49KOhm
GND
PEX_DVDD/PEX_CVDD coupling :
1uF*8 + 4.7uF*3 + 10uF*3 + 22uF*2
PLACE bewteen the PS and GPU
C7044 10UF/6.3V
C7045 10UF/6.3V
C7046 10UF/6.3V
C7047 22UF/6.3V
C7048 22UF/6.3V
Place under GPU
C7043 1UF/6.3V
C7042 1UF/6.3V
C7041 1UF/6.3V
C7040 1UF/6.3V
C7039 1UF/6.3V
C7038 1UF/6.3V
C7065 1UF/6.3V
C7067 1UF/6.3V
C7033 4.7uF/6.3V
C7034 4.7uF/6.3V
C7035 4.7uF/6.3V
PEX_HVDD/PEX_PLL_HVDD coupling :
1uF*6 + 4.7uF*3 + 10uF*3 + 22uF*2
C7053 10UF/6.3V
C7063 10UF/6.3V
C7064 10UF/6.3V
C7054 22UF/6.3V
C7062 22UF/6.3V
C7052 1UF/6.3V
C7058 1UF/6.3V
C7059 1UF/6.3V
C7060 1UF/6.3V
C7061 1UF/6.3V
C7066 1UF/6.3V
C7051 4.7uF/6.3V
C7055 4.7uF/6.3V
C7056 4.7uF/6.3V
23 PCIENB_RXP[0..7]
23 PCIENB_RXN[0..7]
PCIEG => From CPU
PCIENB : to CPU
23 PCIEG_TXP[0..7]
23 PCIEG_TXN[0..7]
PCIENB_RXP7 C7015 0.22UF/6.3V PCIENB_RXP7_C
PCIENB_RXN7 C7016 0.22UF/6.3V PCIENB_RXN7_C
PCIEG_TXP7
PCIEG_TXN7
PCIENB_RXP6 C7013 0.22UF/6.3V PCIENB_RXP6_C
PCIENB_RXN6 C7014 0.22UF/6.3V PCIENB_RXN6_C
PCIEG_TXP6
PCIEG_TXN6
PCIENB_RXP5 C7011 0.22UF/6.3V PCIENB_RXP5_C
PCIENB_RXN5 C7012 0.22UF/6.3V PCIENB_RXN5_C
PCIEG_TXP5
PCIEG_TXN5
PCIENB_RXP4 C7009 0.22UF/6.3V PCIENB_RXP4_C
PCIENB_RXN4 C7010 0.22UF/6.3V PCIENB_RXN4_C
PCIEG_TXP4
PCIEG_TXN4
PCIENB_RXP3 C7007 0.22UF/6.3V PCIENB_RXP3_C
PCIENB_RXN3 C7008 0.22UF/6.3V PCIENB_RXN3_C
PCIEG_TXP3
PCIEG_TXN3
PCIENB_RXP2 C7005 0.22UF/6.3V PCIENB_RXP2_C
PCIENB_RXN2 C7006 0.22UF/6.3V PCIENB_RXN2_C
PCIEG_TXP2
PCIEG_TXN2
PCIENB_RXP1 C7003 0.22UF/6.3V PCIENB_RXP1_C
PCIENB_RXN1 C7004 0.22UF/6.3V PCIENB_RXN1_C
PCIEG_TXP1
PCIEG_TXN1
PCIENB_RXP0 C7001 0.22UF/6.3V PCIENB_RXP0_C
PCIENB_RXN0 C7002 0.22UF/6.3V PCIENB_RXN0_C
PCIEG_TXP0
PCIEG_TXN0
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : NVDIA/PCIE
BG1-HW RD Div.2-HW RD Dept.2
Engineer: Johnson Huang
Size C
Project Name FX505DU
Rev 1.0
Date: Tuesday, March 12, 2019
Sheet 70 of 99

Frame Buffer Partitions A/B/C/D





PEGATRON CONFIDENTIAL

Title : NVDIA/DACA/XTAL

Engineer: Johnson Huang

Size	Project Name	Rev
10	FX505DU	1.0

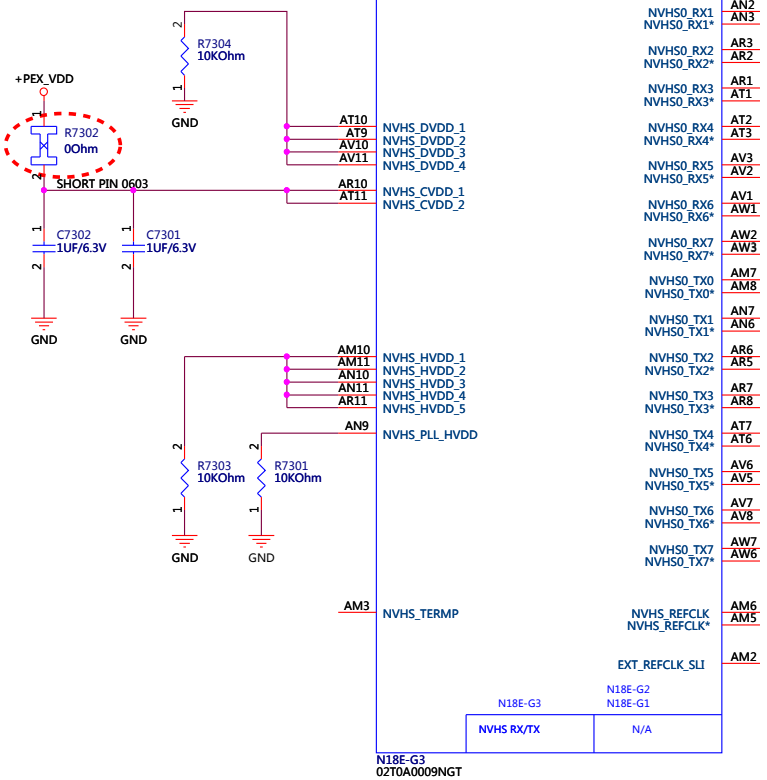
Date: Tuesday, March 12, 2019 Sheet 39 of 50

NVLINK

- N18E CPU does not support NVLink and SLI.
- Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, and NVHS_PLL_HVDD rails to GND with 10 K resistor
- Do not use any decoupling or filtering capacitor for NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, or NVHS_PLL_HVDD rails
- Leave NVHS_TERMP, EXT_REFCLK_SLI, NVHS_REFCLK, NVHS_TX, and NVHS_RX signals floating (NC).

DG-08780-001_v03 p38
NVHS_DVDD, NVHS_HVDD, NVHS_PLL_HVDD can be pull to GND using 10K ohm, if no application

Check it can be removed or not



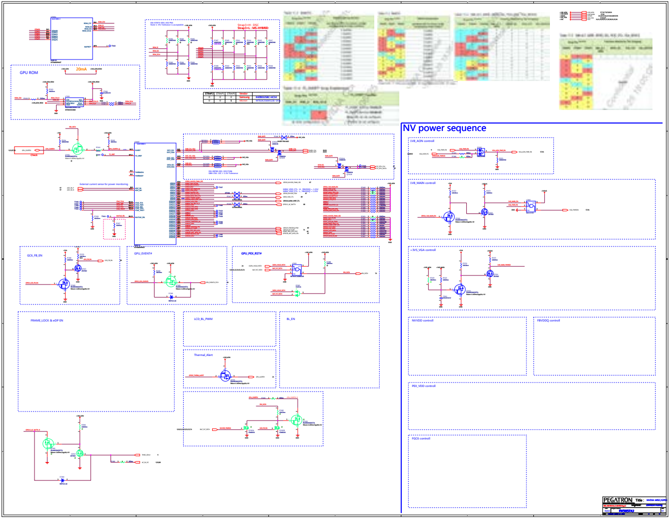
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

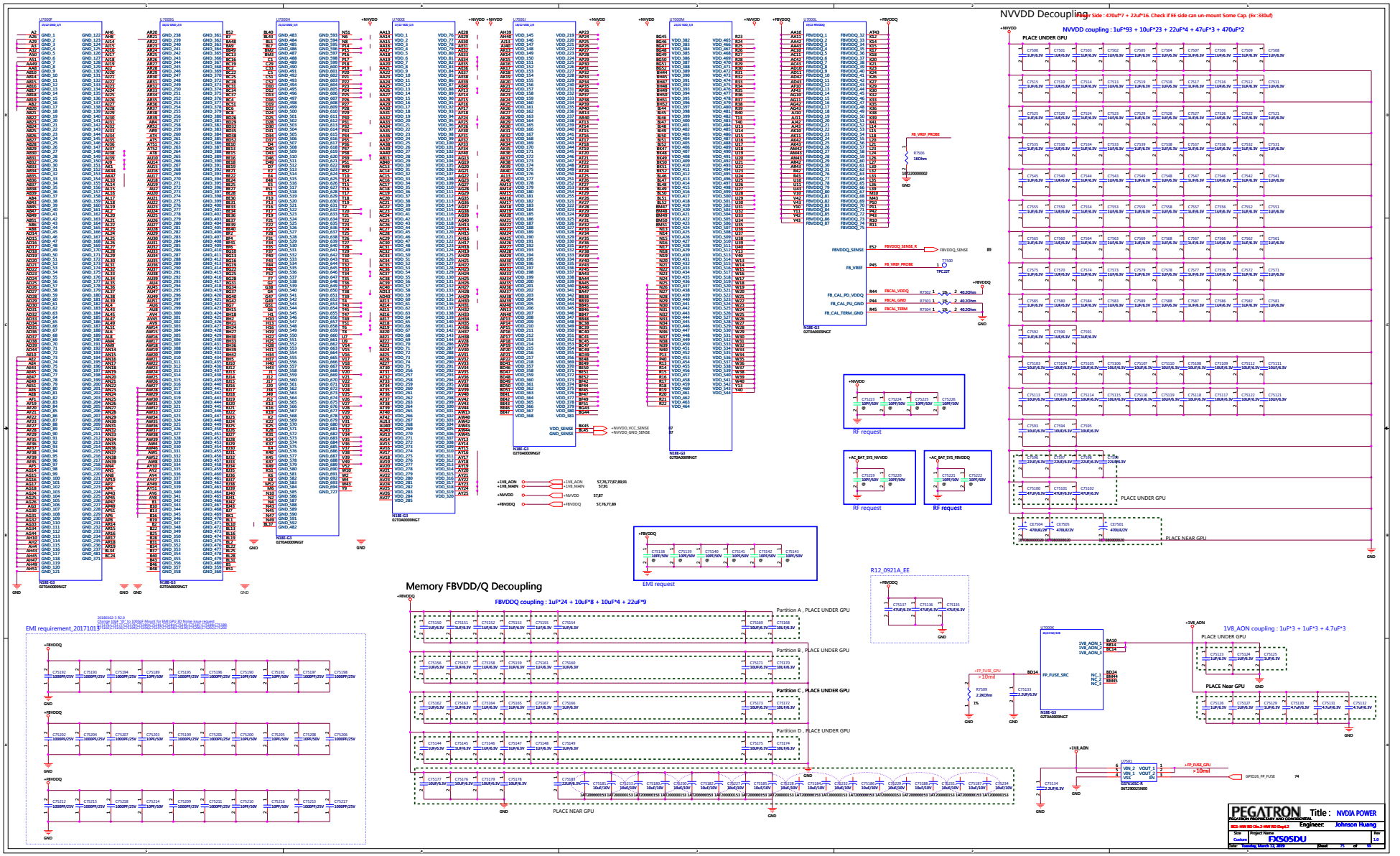
Title : NVDIA/Multi-use IO

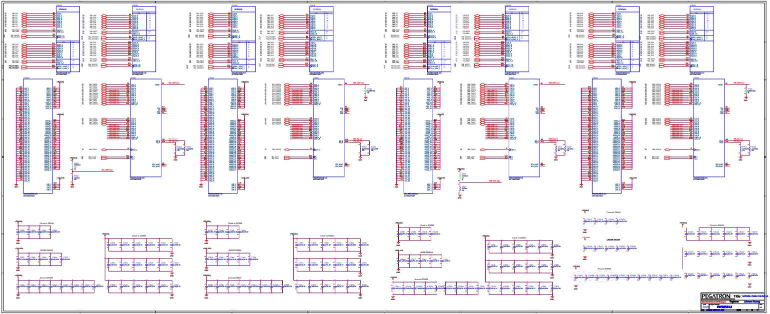
BG1-HW RD Div.2-HW RD Dept.2 Engineer: Johnson Huang

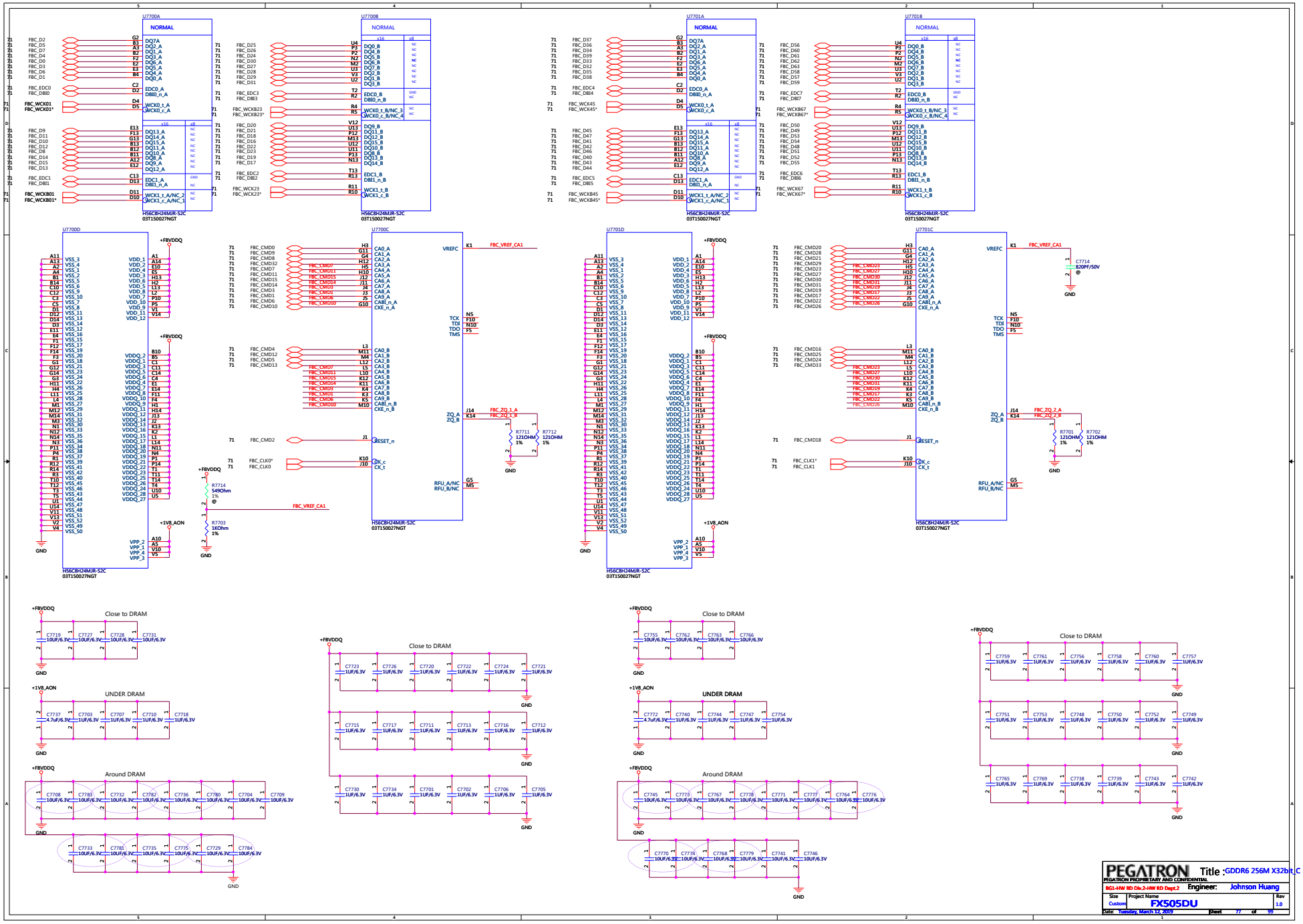
Size	Project Name	Rev
B	FX505DU	1.0

Date: Tuesday, March 12, 2019 Sheet 73 of 99


GPU ROM
20mA
Strap3=H : DSC
Strap3=L : MS-HYBRID
NV power sequence
1V8_AON controll
1V8_MAIN controll
+3VS_VGA controll
NVVDD controll
FBVDDQ controll
PEX_VDD controll
FGC6 controll
GC6_FB_EN
GPU_EVENT#
GPU_PEX_RST#
FRAME_LOCK & eDP EN
LCD_BL_PWM
BL_EN
Thermal_Alert
External current sense for power monitoring
Check
PEGATRON
Title :
NVDIA MISC/GPIO
Johnson Huang
PX585DU

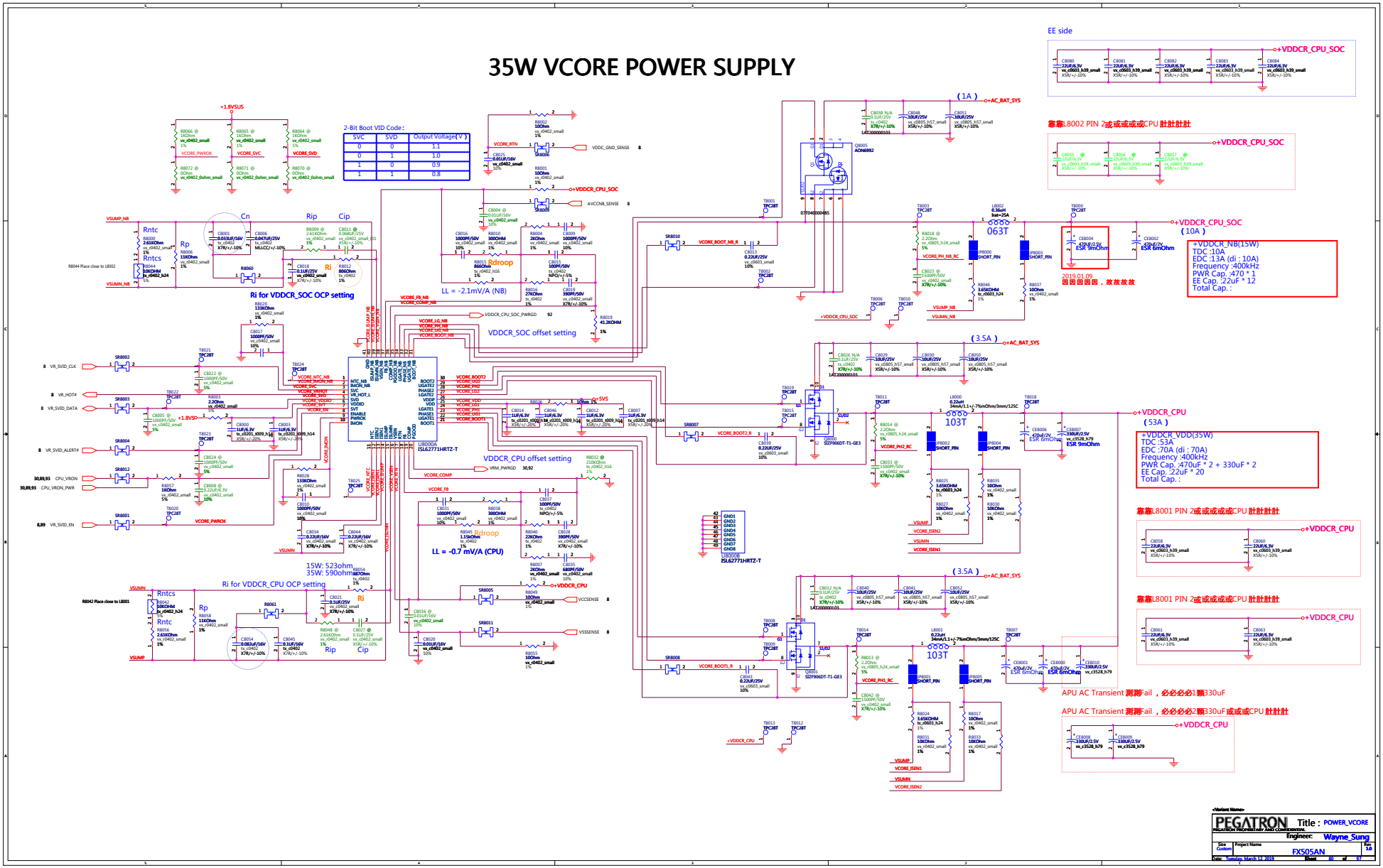

NVVDD Decoupling
NVVDD coupling : 1uF*93 + 10uF*23 + 22uF*4 + 47uF*3 + 470uF*2
PLACE UNDER GPU
PLACE NEAR GPU
RF request
EMI request
Memory FBVDD/Q Decoupling
FBVDDQ coupling : 1uF*24 + 10uF*8 + 10uF*4 + 22uF*9
Partition A , PLACE UNDER GPU
Partition B , PLACE UNDER GPU
Partition C , PLACE UNDER GPU
Partition D , PLACE UNDER GPU
1V8_AON coupling : 1uF*3 + 1uF*3 + 4.7uF*3
EMI requirement_20171011
R12_0921A_EE
PEGATRON
Title : NVDIA POWER
Engineer: Johnson Huang
Project Name: FX505DU
Size: Custom
Rev: 1.0
Date: Tuesday, March 13, 2018
Sheet 73 of 80


PEGATRON
Title : GDDR6 256M X32bit_A
Engineer: Johnson Huang
FX505DU

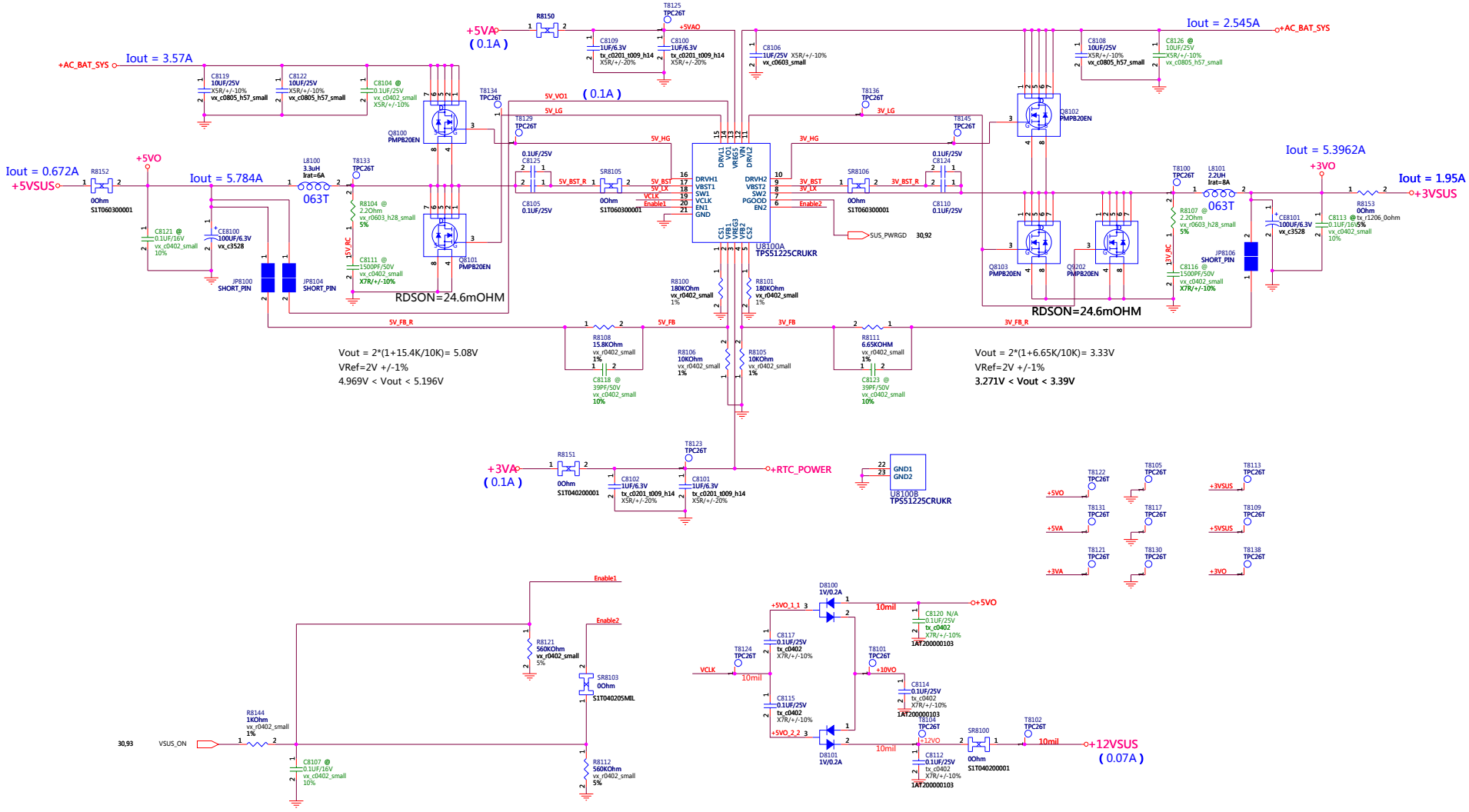


PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : GDDR6 256M X32bit_C		
BG1-HW BD Div-2-HW RD Dept.2	Engineer: Johnson Huang		
Size: Custom	Project Name: FX505DU	Rev: 1.0	
Date: Tuesday, March 12, 2019	Sheet 77 of 99		

35W VCORE POWER SUPPLY



5VO & 3VO POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

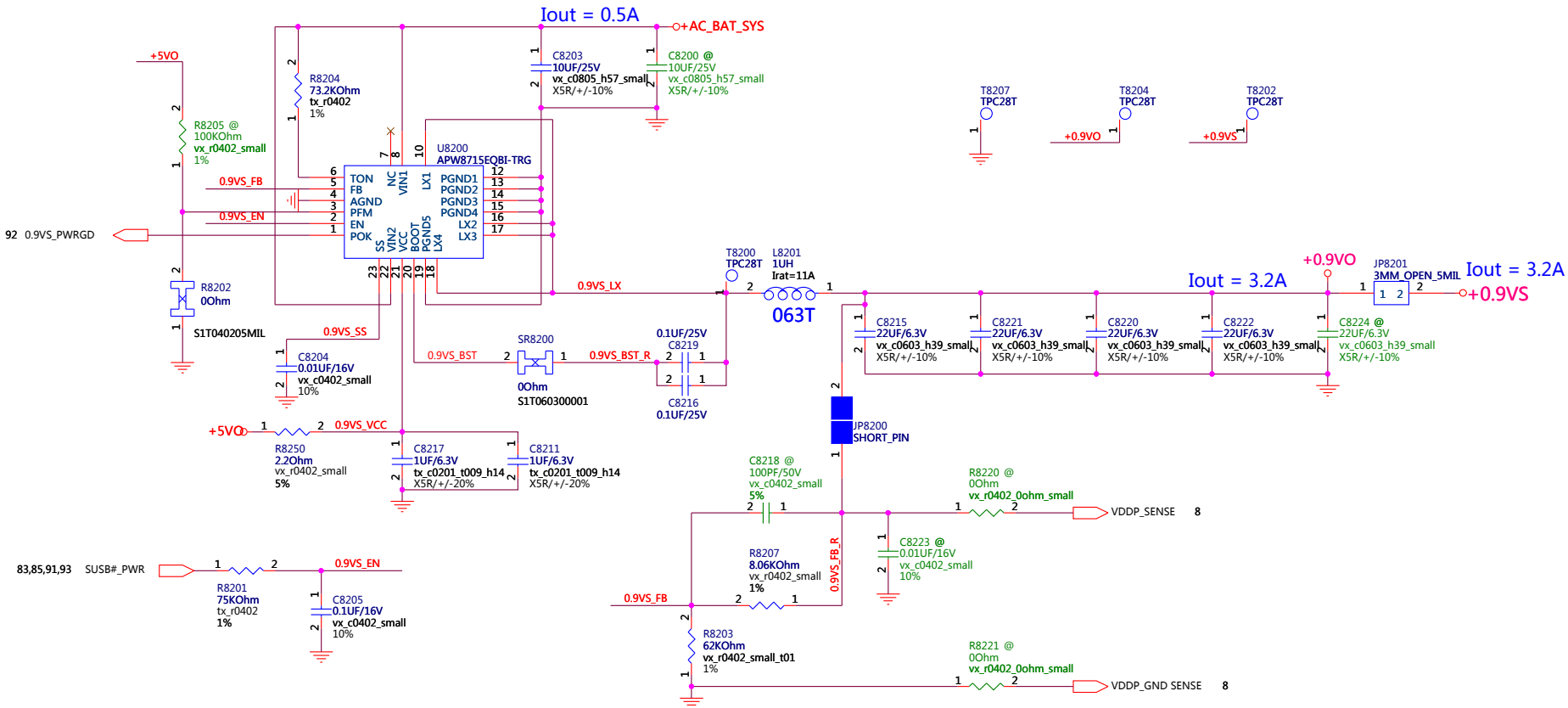
Title : POWER_SYSTEM

Engineer: Wayne_Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 81 of 97

0.9VS POWER SUPPLY



<Variant Name>

PEGATRON Title : +0.9VS

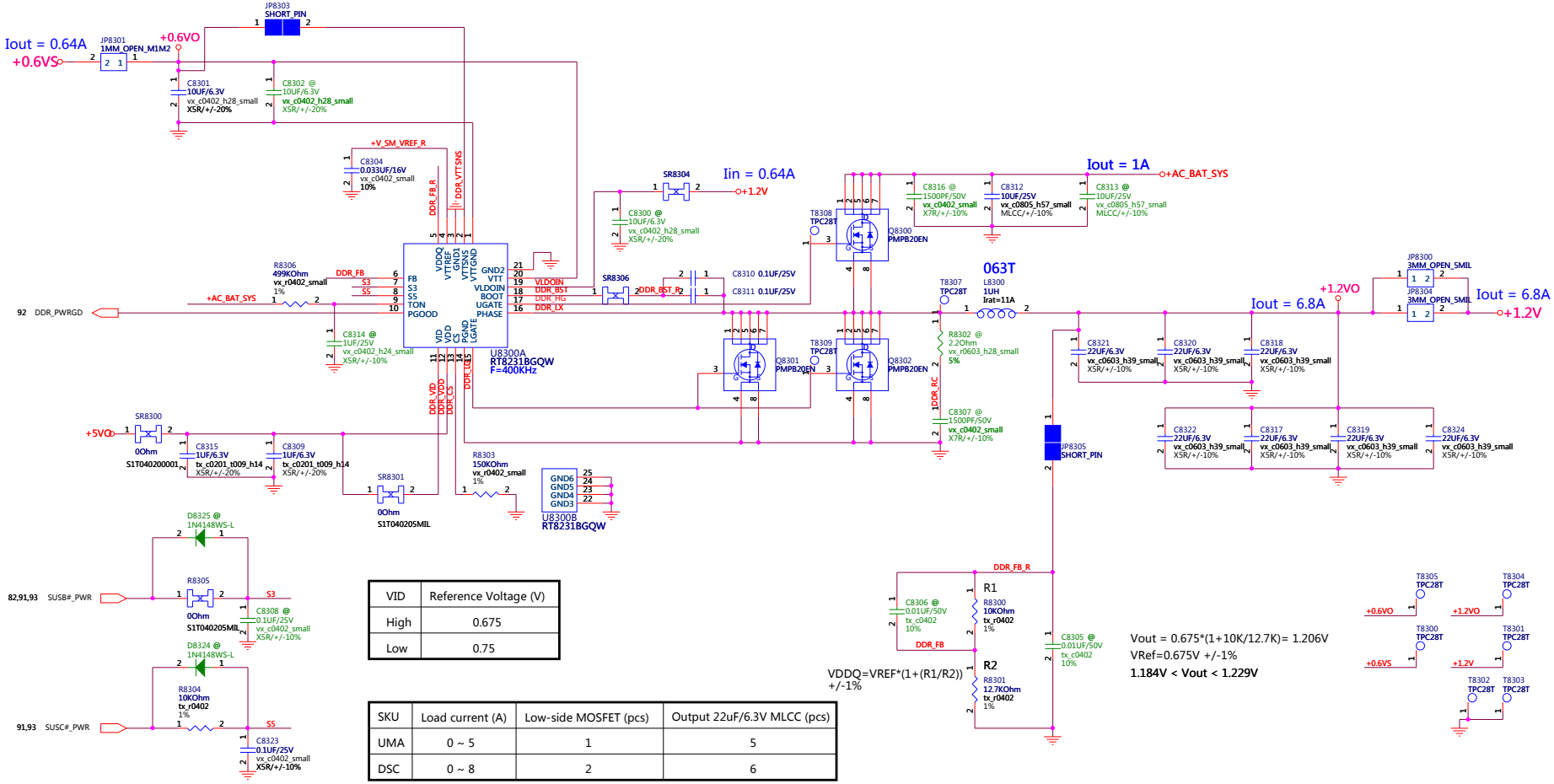
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Wayne_Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 82 of 97

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

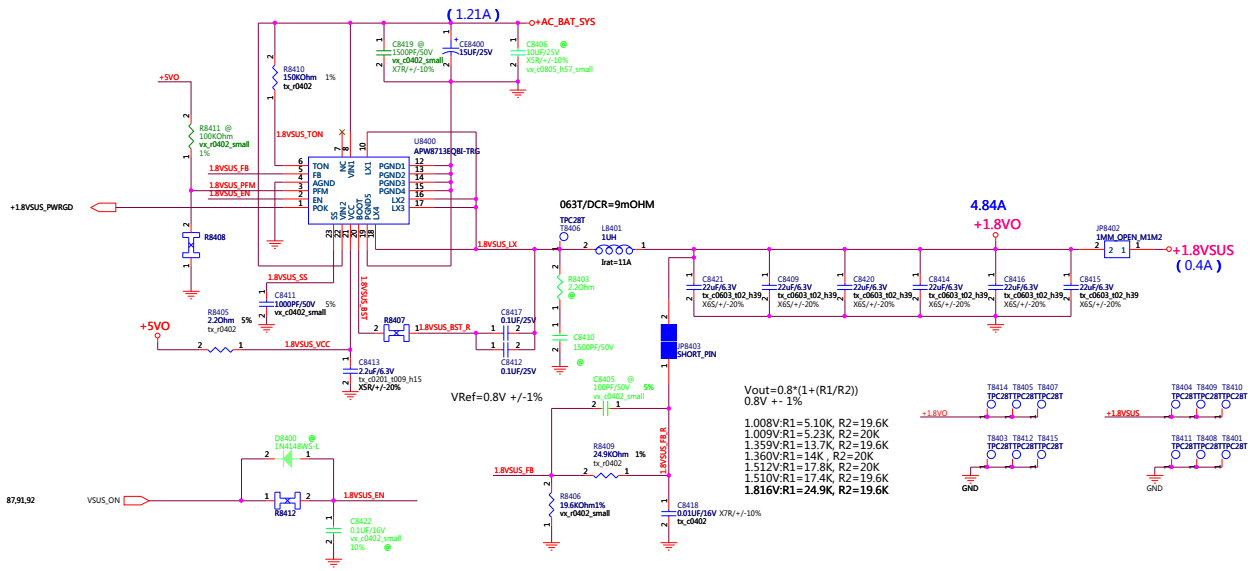
Title : POWER_DDR & VTT

Engineer: Wayne_Sung

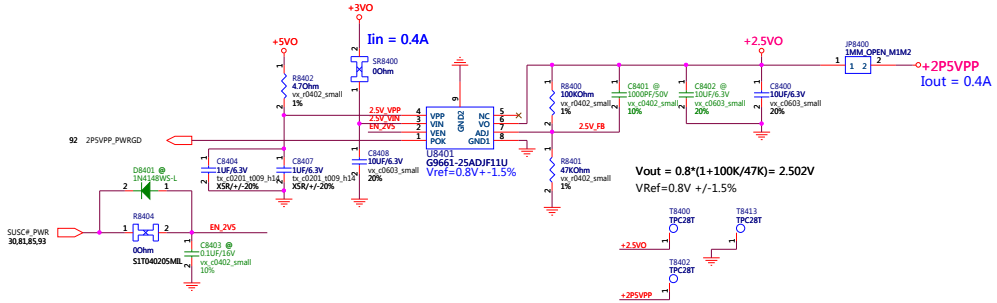
Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 83 of 97

1.8VSUS POWER SUPPLY

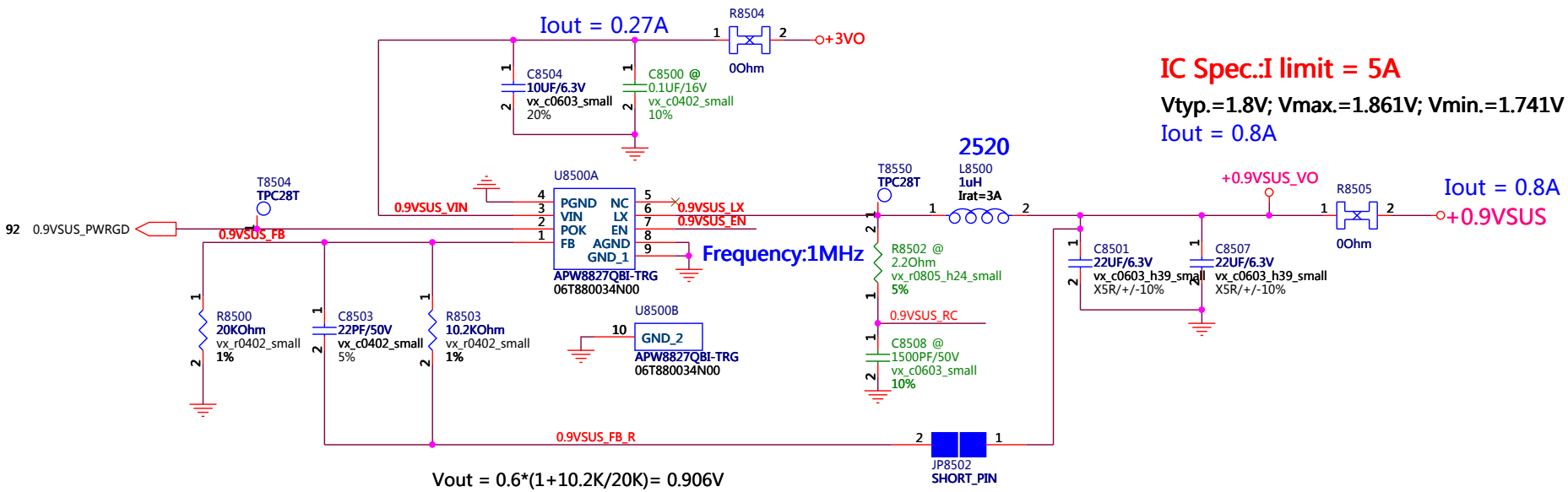


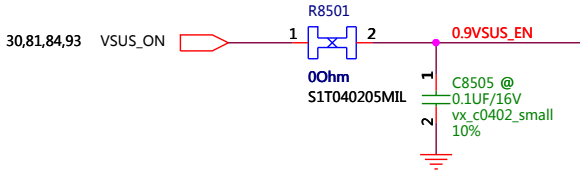
2.5VO POWER SUPPLY

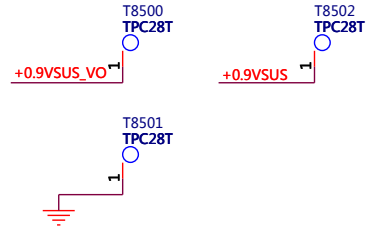


PEGATRON	Title :	POWER_+1.8VSUS_2.5V
Pegatron Corp.	Engineer:	Wayne Sung
Size: C	Project Name:	FX505AN
Rev: 1.0		
Date: Tuesday, March 12, 2019	Sheet 84 of 97	

0.9VSUS POWER SUPPLY







<Variant Name>

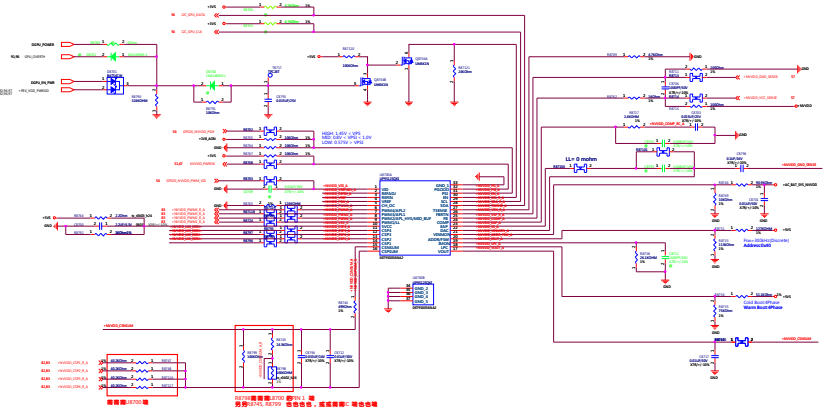
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_0.9VSUS

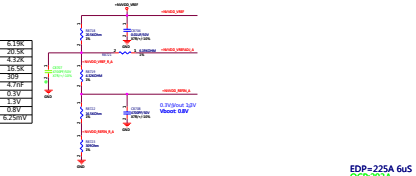
Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

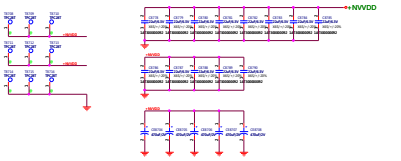
Date: Tuesday, March 12, 2019 Sheet 85 of 97

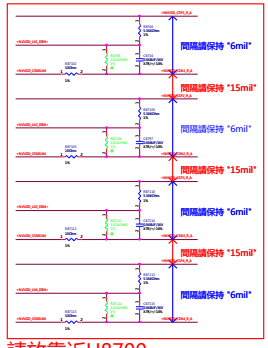


RB721	6.19K
RB718	20.5K
RB719	4.32K
RB722	16.5K
RB723	309
CB707	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV

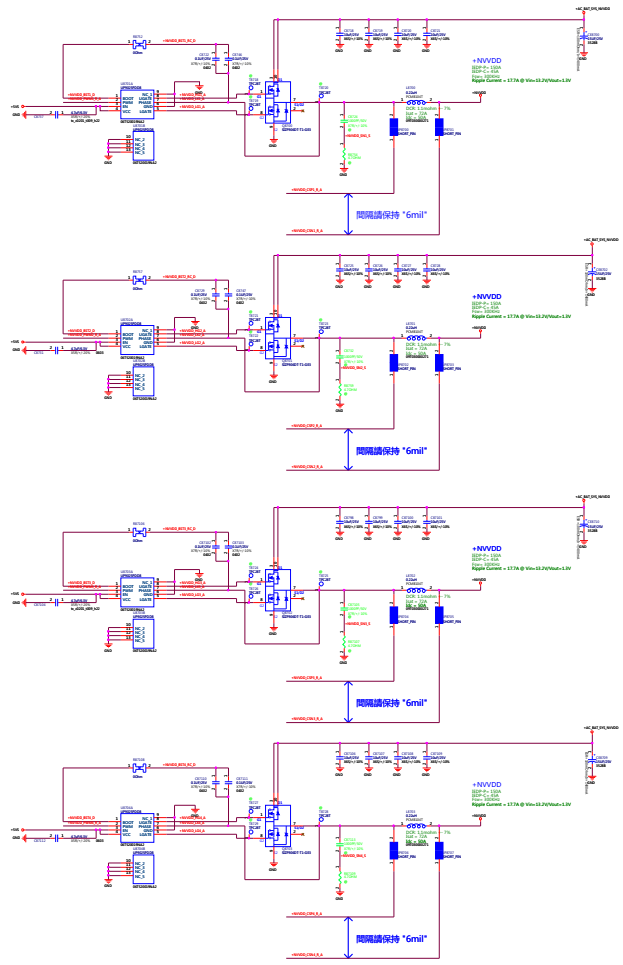


EDP=225A 6uS
OCP:293A
TDC=80A



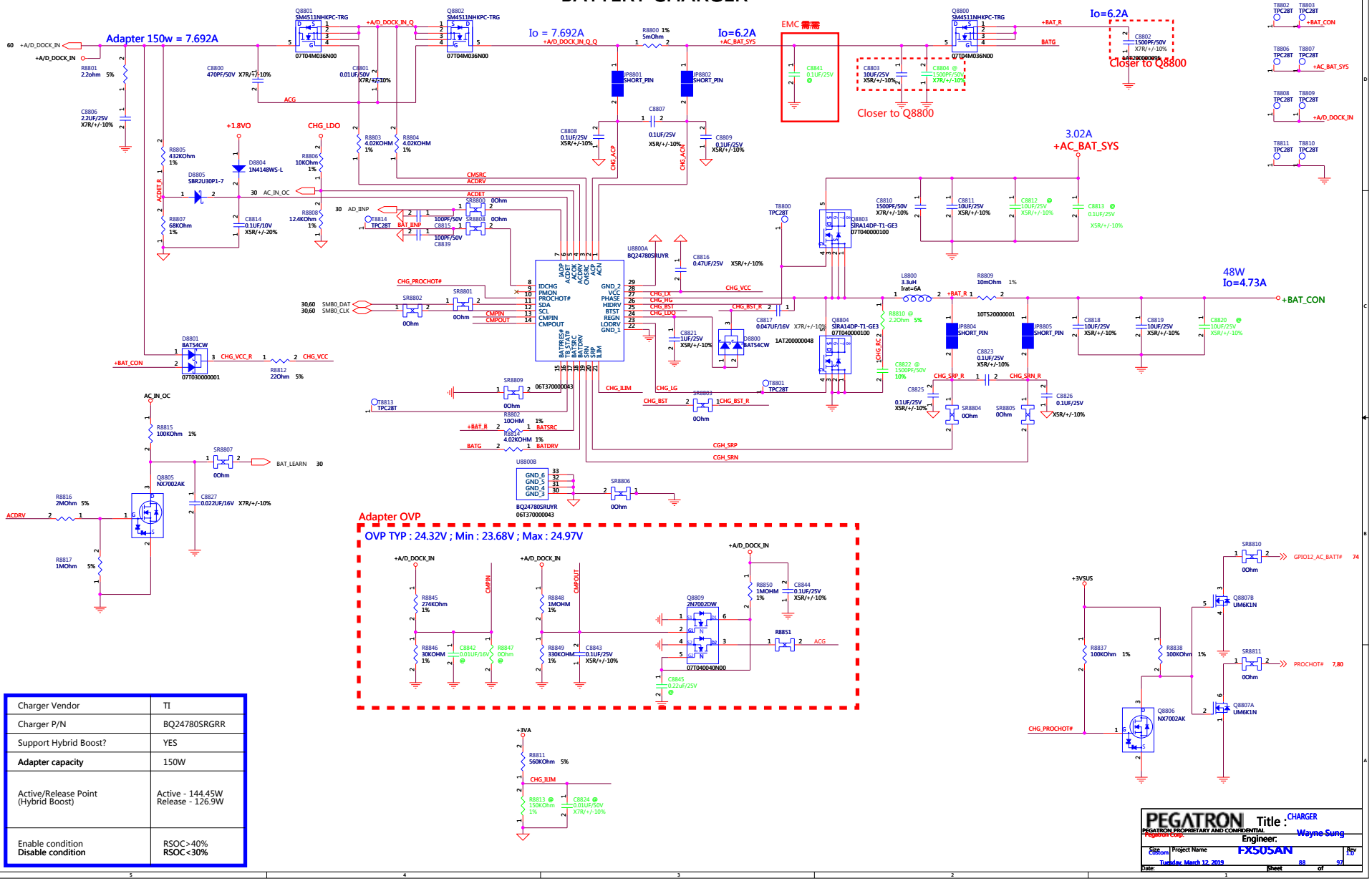


請放靠近U8700



PEGATRON Title : POWER_VGA
Engineer: Wayne_Song
FX505AN

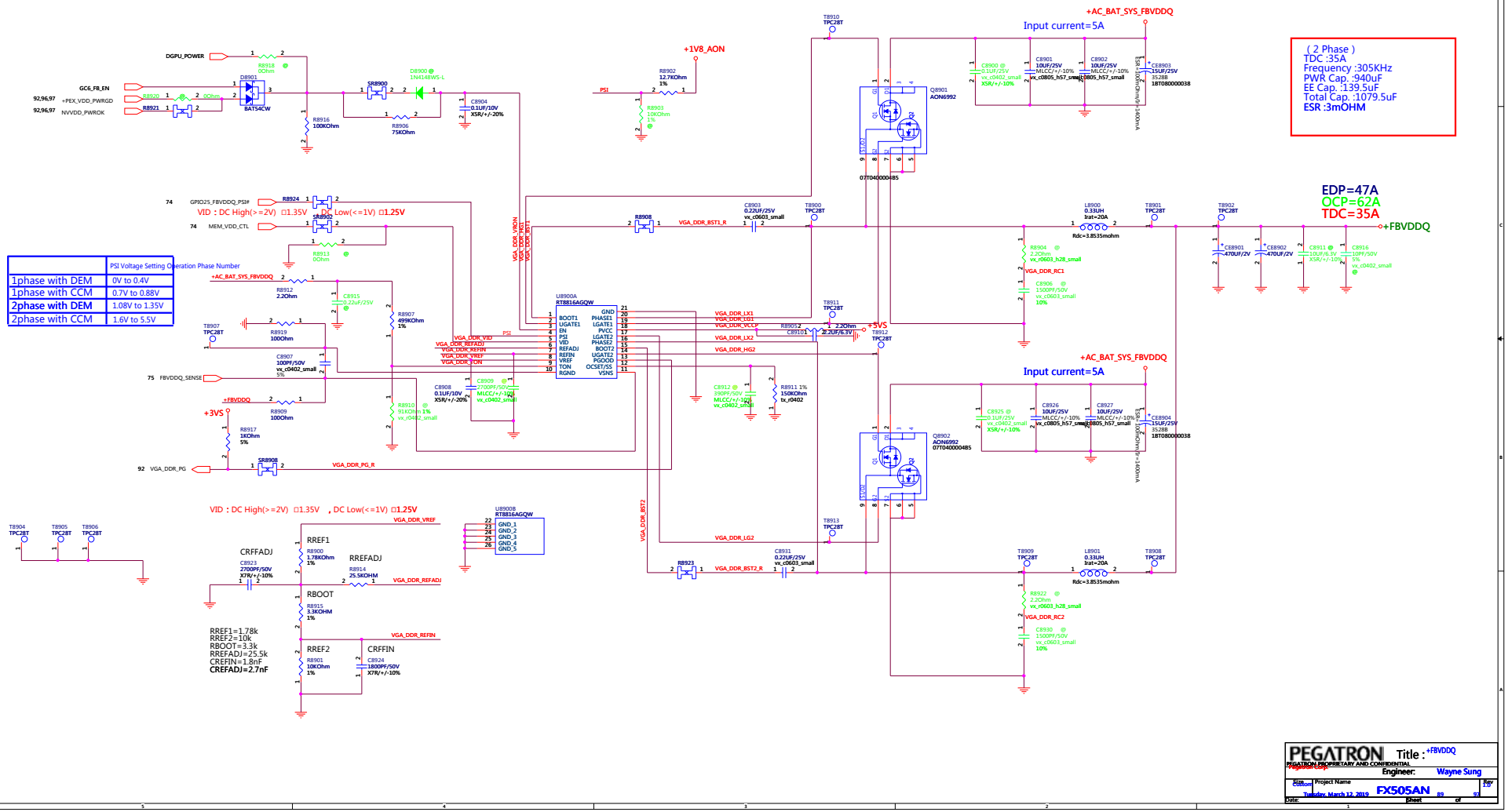
BATTERY CHARGER



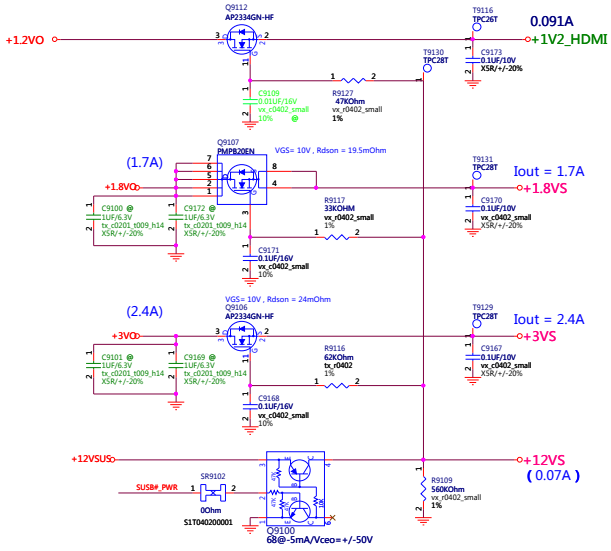
Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition **Disable condition**	RSOC>40% **RSOC<30%**

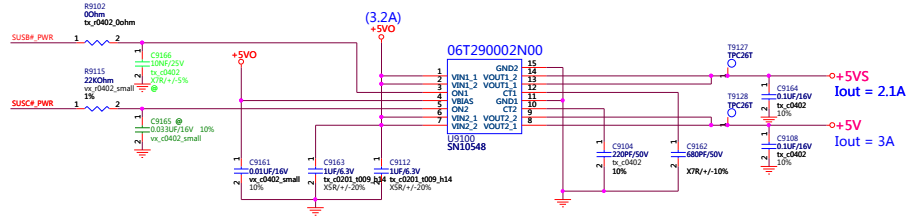
PEGATRON Title : CHARGER
PEGATRON CORP. PROPRIETARY AND CONFIDENTIAL
Engineer: Wayne Sung
Size: C | Project Name: FX505AN | Rev: 1.0
Date: Tuesday, March 12, 2019 | Sheet 88 of 97

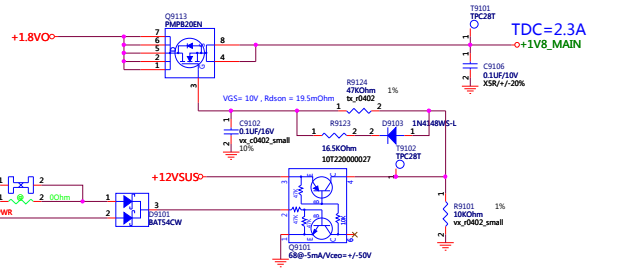
+FBVDDQ POWER SUPPLY



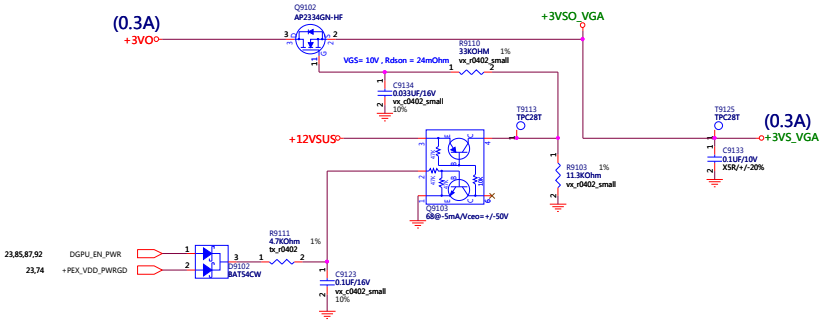
LOAD SWITCH

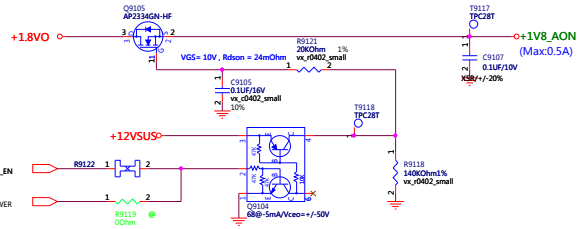




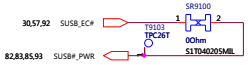


DSC_VGA_PWR POWER

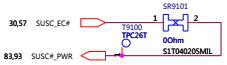




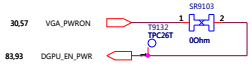
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

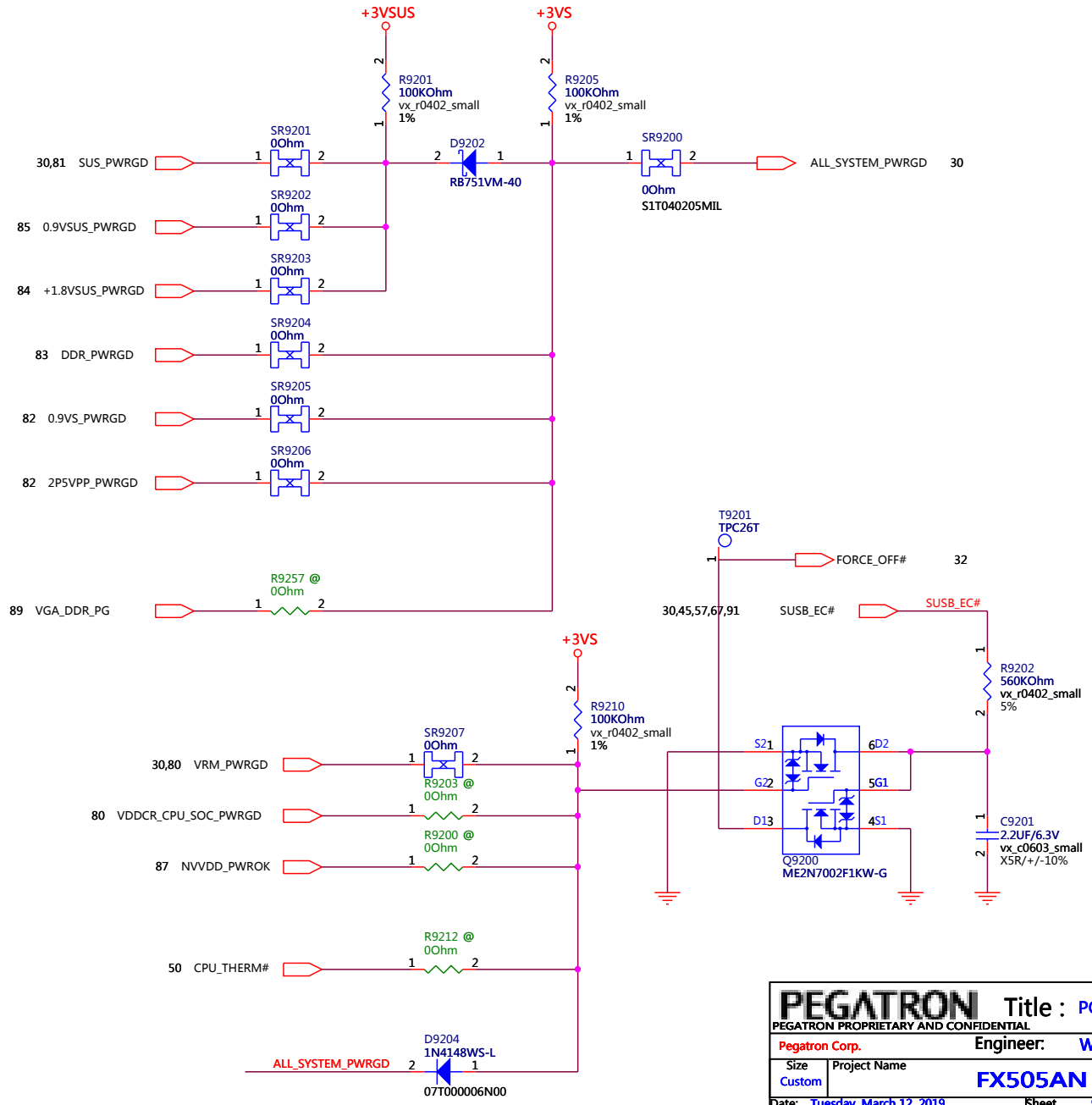
Title : POWER_LOAD SWITCH

Pegatron Corp. Engineer: Wayne Sung

Size	Project Name	Rev
A2	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 91 of 97

POWER GOOD DETECTER



PEGATRON Title : POWER_PROTECT

PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp. Engineer: Wayne Sung

Size	Project Name	Rev
Custom	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 92 of 97

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,88,89

+BAT_CON → +BAT_CON 60,88

+RTC_POWER → +RTC_POWER 81

+5VA → +5VA 56,66,81

+3VA → +3VA 11,28,30,56,57,60,66,81,88

+5VO → +5VO 81,83,85,89,91

+3VO → +3VO 81,84,85,89,91

+2.5VO → +2.5VO 83

+1.8VO → +1.8VO 84,85,91

+1.8VO_VGA → +1.8VO_VGA 83

+1.2VO → +1.2VO 83

+0.9VO → +0.9VO 83

+0.9VSUS_VO → +0.9VSUS_VO 83

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 52,66,81

+3VSUS → +3VSUS 8,9,11,12,28,30,31,36,51,81,92

+1.8VSUS → +1.8VSUS 9,11,28,80,84,89

+0.9VSUS → +0.9VSUS 83

+12VS → +12VS 28,31,48,91

+5VS → +5VS 30,31,36,48,50,51,56,57,61,80,91

+3VS → +3VS 8,9,10,11,12,16,17,28,30,31,36,37,40,45,48,50,51,53,56,57,61,62,64,66,91,92

+1.8VS → +1.8VS 8,9,11,28,31,44,48,57,80,89,91

+0.6VS → +0.6VS 16,17,57,83

+3V → +3V 31,44,57,64,66,91

+1.2V → +1.2V 7,11,16,17,57,83

+2P5VPP → +2P5VPP 83

+1.8VS_VGA → +1.8VS_VGA 83

+1.35VS_VGA → +1.35VS_VGA 83

+VDDCI_VGA → +VDDCI_VGA 11,80,89

+VDDC_VGA → +VDDC_VGA 11,80,89

+VDDCR_CPU_SOC → +VDDCR_CPU_SOC 11,80

+VDDCR_CPU → +VDDCR_CPU 11,80

FOR POWER TEST

+3VA

JP9300 SGL_JUMP (1 2) → T9300 TPC28T → CPU_VRON_PWR 30,80,89

JP9301 SGL_JUMP (1 2) → T9301 TPC28T → SUSB#_PWR 82,83,85,91

JP9302 SGL_JUMP (1 2) → T9302 TPC28T → SUSC#_PWR 83,91

JP9303 SGL_JUMP (1 2) → T9303 TPC28T → VSUS_ON 30,81,84,85

JP9304 SGL_JUMP (1 2) → T9304 TPC28T → DGPU_POWER 89

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

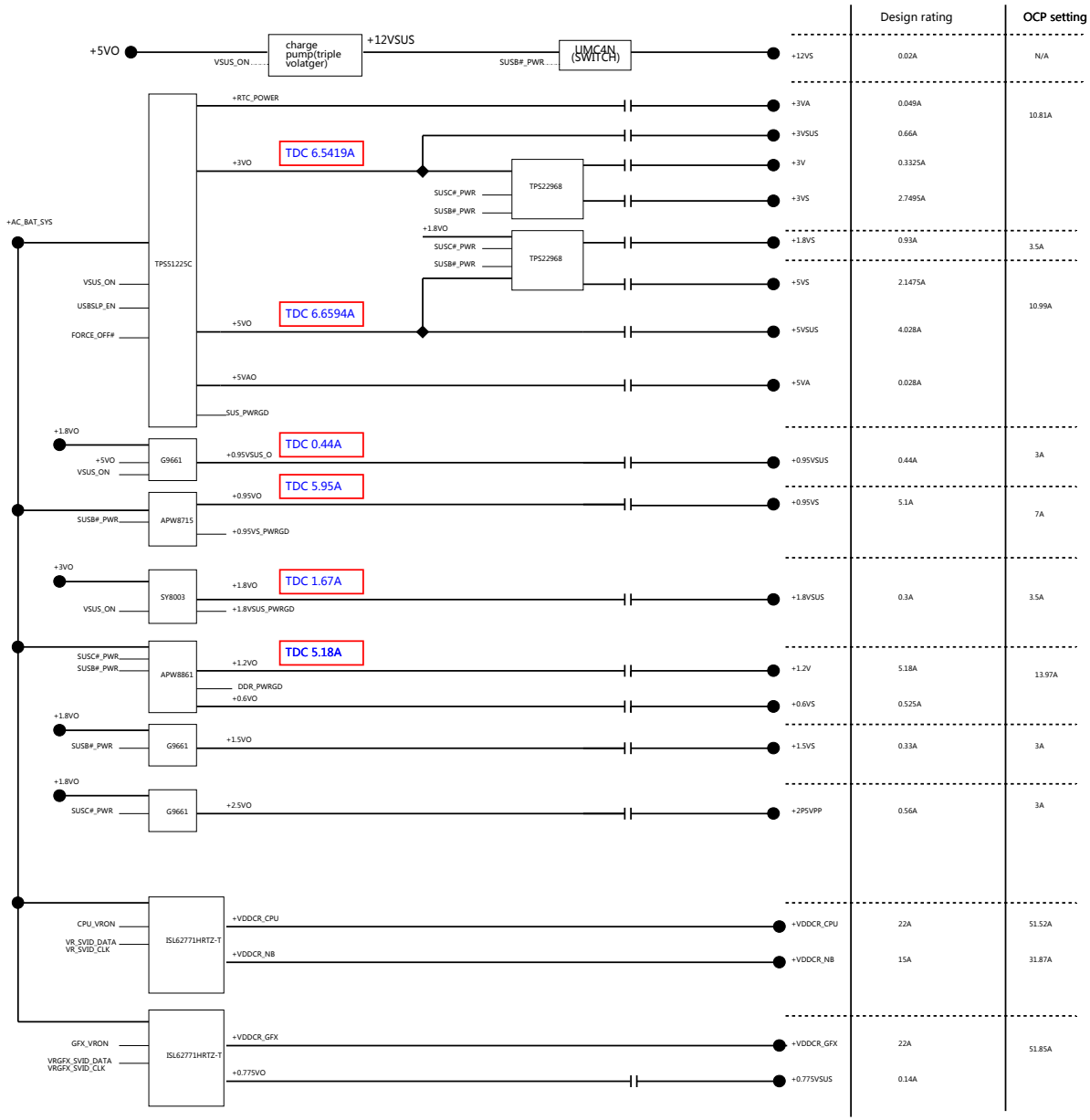
Title : POWER_SIGNAL

Pegatron Corp.

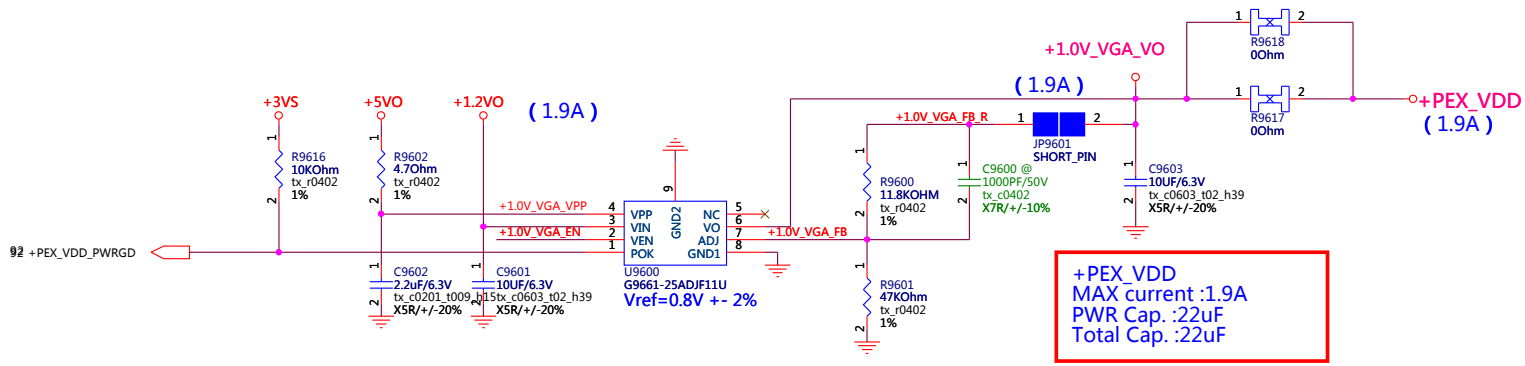
Engineer: Wayne Sung

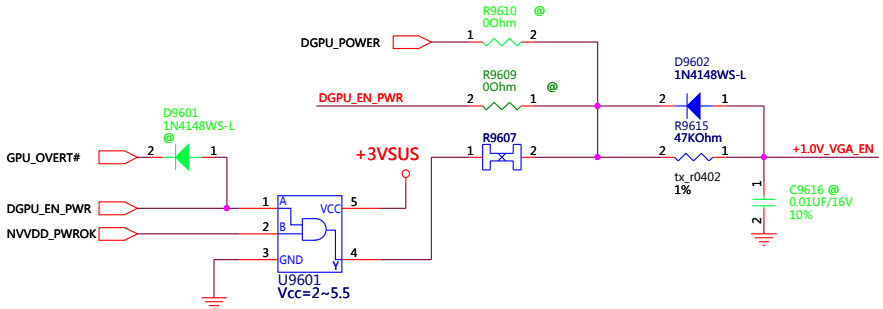
Size	Project Name	Rev
Custom	FX505AN	1.0

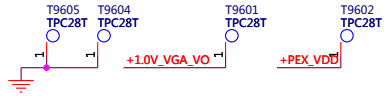
Date: Tuesday, March 12, 2019 Sheet 93 of 97


Design rating
OCP setting
+5VO
charge pump(triple volatger)
VSUS_ON
+12VSUS
SUSB#_PWR
LIMC4N (SWITCH)
+12VS
0.02A
N/A
+RTC_POWER
+3VA
0.049A
10.81A
+3VSUS
0.66A
TDC 6.5419A
+3VO
+3V
0.3325A
TPS22968
SUSC#_PWR
SUSB#_PWR
+3VS
2.7495A
+AC_BAT_SYS
+1.8VO
SUSC#_PWR
SUSB#_PWR
TPS22968
+1.8VS
0.93A
3.5A
TPS51225C
VSUS_ON
USBSLP_EN
FORCE_OFF#
+5VS
2.1475A
10.99A
TDC 6.6594A
+5VO
+5VSUS
4.028A
+5VAO
+5VA
0.028A
SUS_PWRGD
+1.8VO
TDC 0.44A
+0.95VSUS_O
+0.95VSUS
0.44A
3A
+5VO
VSUS_ON
G9661
TDC 5.95A
+0.95VO
+0.95VS
5.1A
7A
SUSB#_PWR
APW8715
+0.95VS_PWRGD
+3VO
TDC 1.67A
+1.8VO
+1.8VSUS
0.3A
3.5A
SY8003
VSUS_ON
+1.8VSUS_PWRGD
SUSC#_PWR
SUSB#_PWR
TDC 5.18A
+1.2VO
+1.2V
5.18A
13.97A
APW8861
DDR_PWRGD
+0.6VO
+0.6VS
0.525A
+1.8VO
SUSB#_PWR
G9661
+1.5VO
+1.5VS
0.33A
3A
+1.8VO
SUSC#_PWR
G9661
+2.5VO
+2P5VPP
0.56A
3A
CPU_VRON
VR_SVID_DATA
VR_SVID_CLK
ISL62771HRTZ-T
+VDDCR_CPU
+VDDCR_CPU
22A
51.52A
+VDDCR_NB
+VDDCR_NB
15A
31.87A
GFX_VRON
VRGFX_SVID_DATA
VRGFX_SVID_CLK
ISL62771HRTZ-T
+VDDCR_GFX
+VDDCR_GFX
22A
51.85A
+0.775VO
+0.775VSUS
0.14A
Title : POWER_SIGNAL
PEGATRON CONFIDENTIAL
Engineer: Wayne Sung
Pegatron Corp.
Size Custom
Project Name FX505AN
Rev 1.0
Date: Tuesday, March 12, 2019
Sheet 35 of 57

+PEX_VDD POWER SUPPLY







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +PEX_VDD

Engineer: Wayne Sung

Size	Project Name	Rev
B	FX505AN	1.0

Date: Tuesday, March 12, 2019 Sheet 96 of 97

14.78A
+AC_BAT_SYS

10.98A
+AC_BAT_SYS_FBVDDQ

10.98A
+AC_BAT_SYS_NVVDD

R9702 5mOHM 10TZ20112M00

R9715 5mOHM 10TZ20112M00

R9731 10Ohm @

R9704 10Ohm @

R9709 10Ohm @

R9703 10Ohm @

10UF/6.3V C9707 20% @

C9708 20% 10UF/6.3V @

IN-2

IN+2

IN-1

IN+1

+3VS_VGA

+3VA

R9750 0Ohm /UPI

R9749 0Ohm /ON

+3V_OVRM

	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	215 ohm	287 ohm
R9735	324K ohm	243K ohm

R953 R9729 75KOhm

R954 R9730 487Ohm C9705 1000PF/50V X7R/+/-5% C841

R952 R9733 75KOhm

R924 R9732 487Ohm C9706 1000PF/50V X7R/+/-5% C836

R9727 100Ohm

R9728 100Ohm

R977 R9726 215Ohm C9704 0.015UF/25V X7R/+/-10%

R9753 0Ohm /UPI

R9747 75KOhm /UPI

R9748 649Ohm /UPI C9722 1000PF/50V X7R/+/-5% /UPI

R9754 0Ohm /ON

R9745 0Ohm /ON

R9746 0Ohm /UPI

+3V_OVRM

UPI & ONSEMI colay

ENABLE

R9722 10KOhm +3V_OVRM

R9723 /UPI 10KOhm

Q9700 NX7002AK /ON

R9751 0Ohm /ON +3VS_VGA

R9752 100KOhm /ON

U9701A US5650QQKI

SH_IN_P1 BS_IN1 SH_IN_P2 BS_IN2 SH_O2 GND_FET_1 BS_IN3_4

GND_1 SH_O1 NC_4 BS_OK MUX_SEL ENABLE VCC MODE_SEL SKIP BS_REF BG_REF_OUT CM_REF_IN NC_3 DIFF_OUT_P DIFF_OUT_N NC_2 SH_O4

06T890006N00

2018/12/24 US5650QQKI

U9701B

GND_2 GND_3 GND_4 GND_5

US5650QQKI

06T890006N00

C9703 0.01UF/25V X7R/+/-10%

R923 R9725 215Ohm

R9721

R9744 10KOhm

R9740 1KOhm +3V_OVRM

R9738 R9739

ADC_IN_P 74

ADC_IN_N 74

N18E GPIO

GPIO28_ADC_MUX_SEL 74

R950

R9724 BS_OK

R9720 10KOhm +3V_OVRM

C9701 1UF/6.3V X5R/+/-20%

C9702 1UF/6.3V X5R/+/-20%

C9709 1nF/50V NPO/+/-5%

R9735 324KOHM

R9734 10KOhm

C9710 1nF/50V NPO/+/-5%

R9736 365KOhm

R9737 680KOhm

C9711 1nF/50V NPO/+/-5%

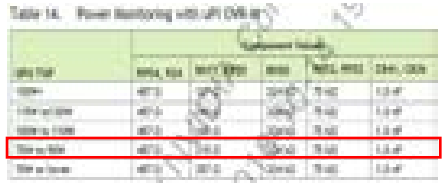
R9741

R9742

C9720 47PF/50V NPO/+/-5%

C9721 47PF/50V NPO/+/-5%

T9713 TPC28T



PEGATRON PROPRIETARY AND CONFIDENTIAL
Pegatron Corp.

Title : +NVVDS

Engineer: Wayne Sung

Size: C | Project Name: FX505AN | Rev: 1.0

Date: Tuesday, March 12, 2019 | Sheet 97 of 97

20181026D

C0853~C0858 are changed to 0402

20181028A

Reserving R0960
PCIE_TX[N:P][9:11]_SSD_C are changed to PCIE_TX[N:P][1:3]_SSD_C

20181031C

Add R7113-R7118
Remove CE7502
Add R3653, R3654

20181101A
Add R4403, R4408, R4412
memory swap
Delete test point on CON5103

20181101B
Add R2454
Add C5142, C5141
Add SATA/PCIE redriver on Page 51
Change R3653, R3654 to 0402

20181102
Add R5104
Change JRST2401 to jumper
Delete R2409

20181105
Change R3634, R3632, R3619 to TX
Change C5144, C5145 to 0.47uF
Add R5116, R5117
Remove SATA signals to SSD

20181105
D3101 swap

20181106
Remove SATA_DEVSLP

20181107
Remove H6527
Add L6003; Change the sequence of parts on smbus of battery

20181108
Modify for the circuit of GPU sense
HDMI and USB signals swap

20181109
Change C8106 from 0402 to 0603
Change PEXVDD JP to 0805 0ohm

20181112
RN7403 swap
Update power segment

20181113
Delete FBx_VREF_CA related circuit
Add Q3601, Q3602

20181114
Change D3611 to AGND

20181122
Change Q2802 to 12VS and be unmount

20181207
Change U5301 to 0603-001J000
Change R5723 to 33 ohm
Mounting R1107
Unmounting Q1102、Q1103、R1114、R1115
Change R0837 to 1Kohm
Add R2489, R2490, R0861
Rename FP_FUSE_GPU to +FP_FUSE_GPU

20181207
Unmount U5301, R5337

20181211
Update power schemtic 1211

20181217
Mount Q5704、Q5708、R5705、R5715、R5742
Change RTC_3V3_IN to +RTC_3V3_IN
Change 0ohm to short pad
Remove R7421

20181219
Remove D7405
Add R5205~R5210、C5225~C5230

20181224
Mount R5705, Q5701

20181226
Change INT of I2C of toucpad to level shifter

20181227
Change 0603 MLCC *1 to 0402 MLCC *2 for EMI/ME request
Change C0903 to 1000pF

20181228
Unmount R7455
Reserve C3015
Change C1147, C1149 to 10uF 0402; Remove C1139
Change R7215 to shortpad
Change R2425, R2453 to shortpad
Change R0914, R0915 to 4.7Kohm
Mount C3108, C3110

20190103
Change R7113-R7118 to T7101-T7106

20190104
Change R0860 to shortpad
Change R3623, R3102, R3118 to 5% component
Reserve C3016
Change C8731, C8737, C87104, C87112 to lower package

20190107
Delete T7101-T7106
Unmount Q7401
Change R2806, R2807, R2815, R2816 to 0 ohm; R2808, R2809, R2818, R2819 to 100 ohm

20190214
Mount Q2802
Mount R7414, unmount R7413

20190219
Change C2403, C2404 to 10pF
Change R2454 to shortpad

Title	<Title>	
Size B	Document Number FX505DU	Rev <RevCode>
Date: Tuesday, March 12, 2019	Sheet 100 of 1	