AMD AM4

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29	SIO HW Monitor / NCT7718W	59	PM - NB503 CHIP_SOC-1V		
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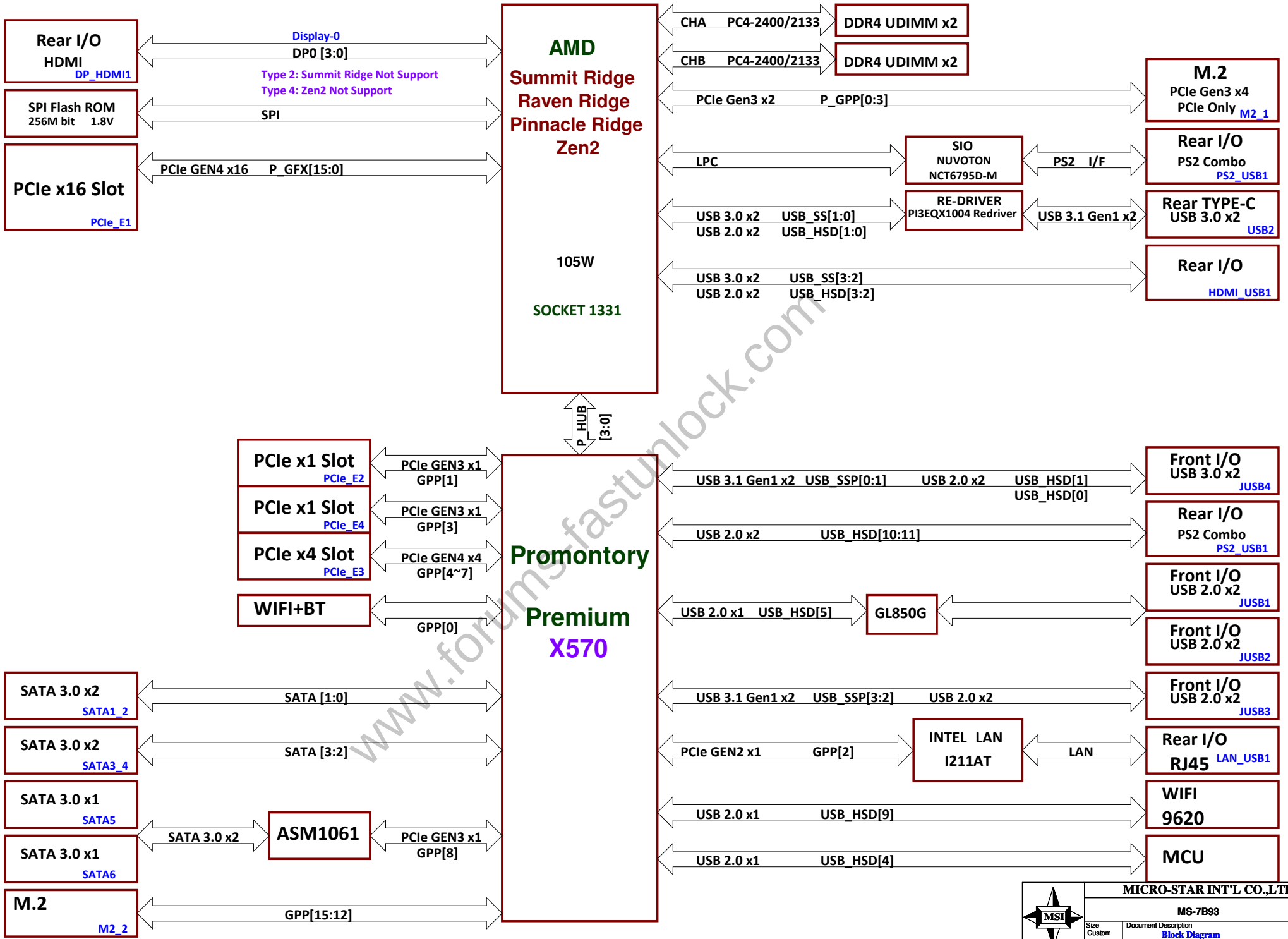

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Size	Document Description	Rev
Custom	Block Diagram	11

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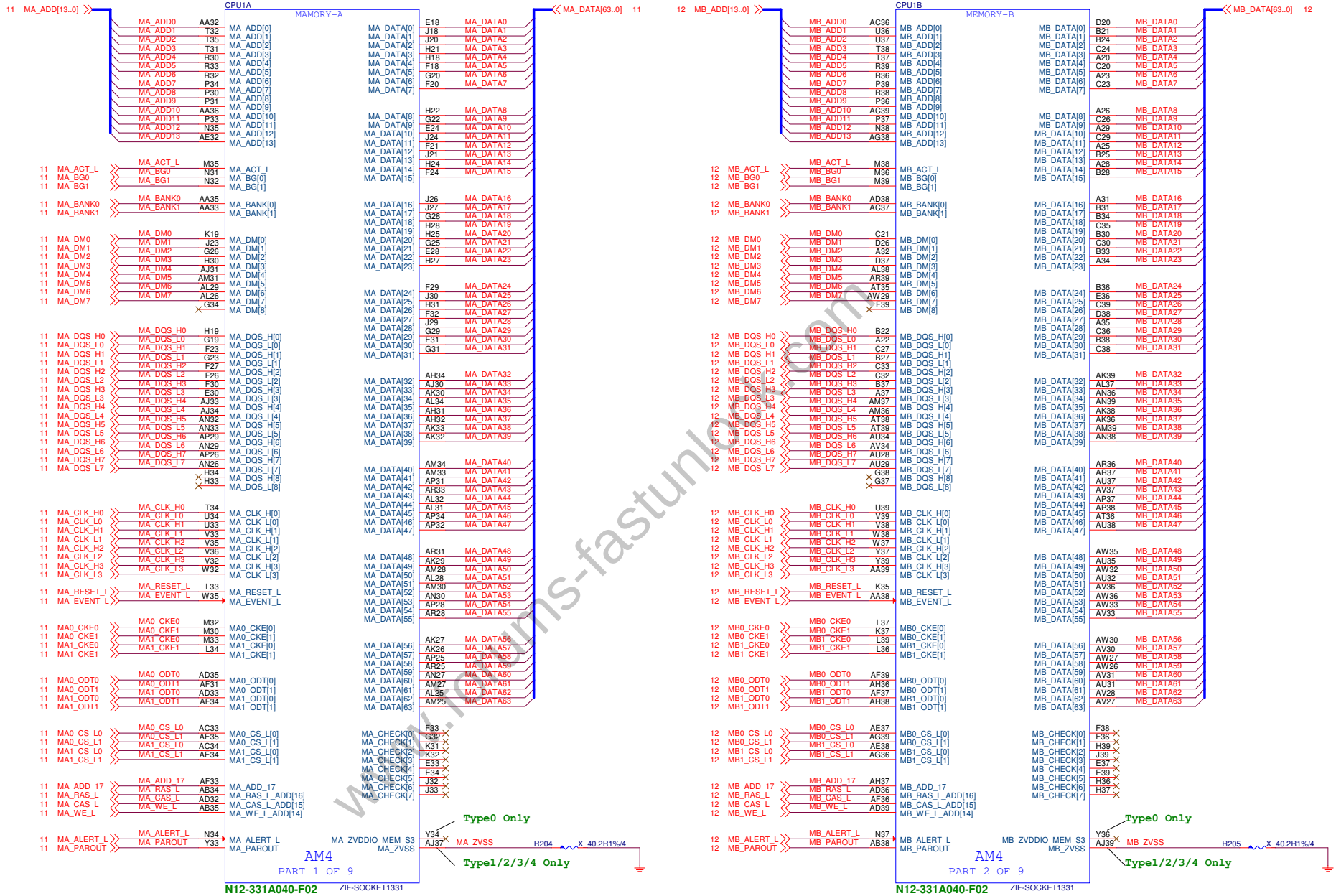
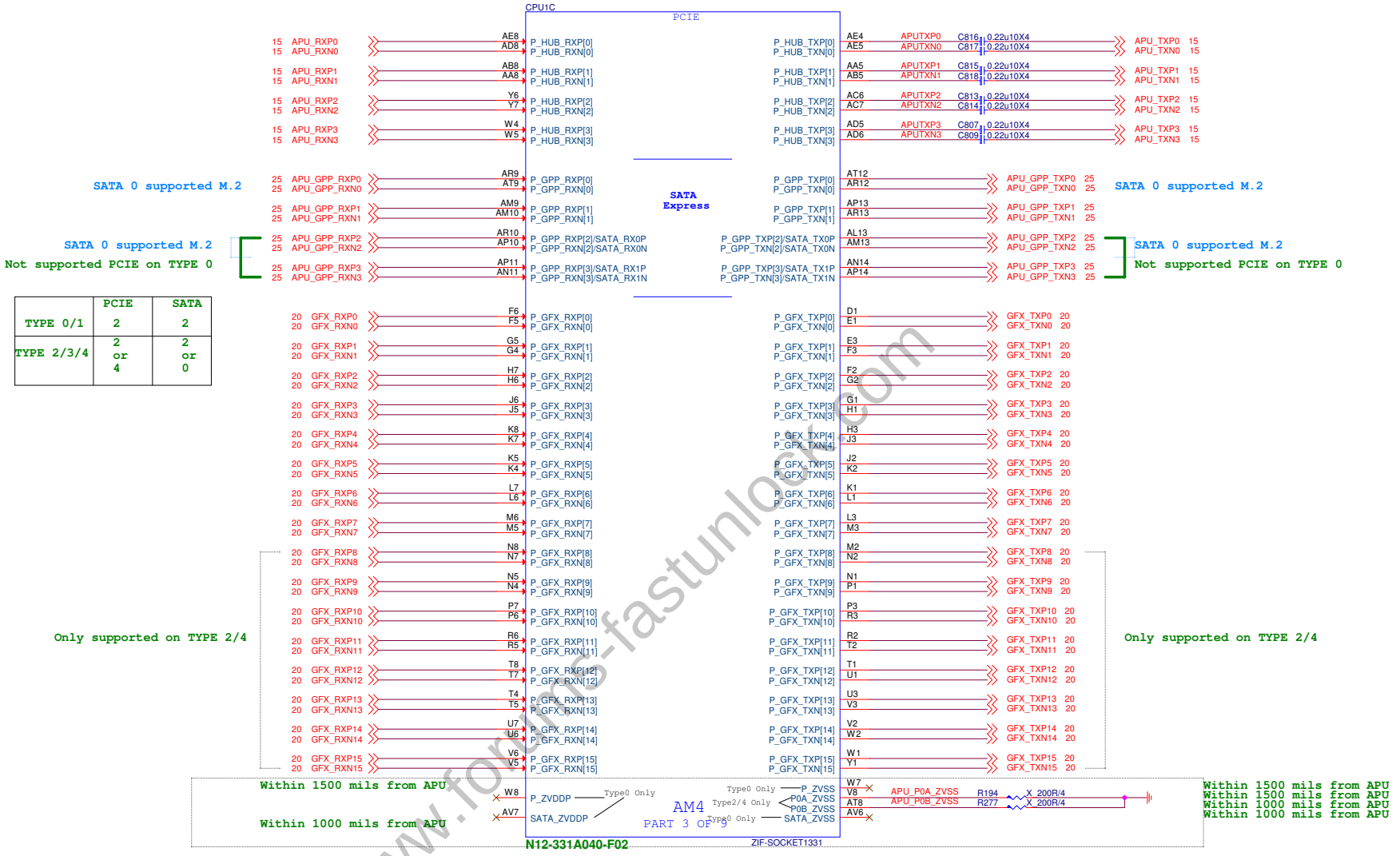


MICRO-STAR INT'L CO.,LTD	
MS-7B93	
Size: Custom	Document Description: AM4 DDR4 I/F
Rev: 11	
Date: Thursday, July 04, 2019	Sheet 3 of 75



	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: AM4 PCIE / SATAE
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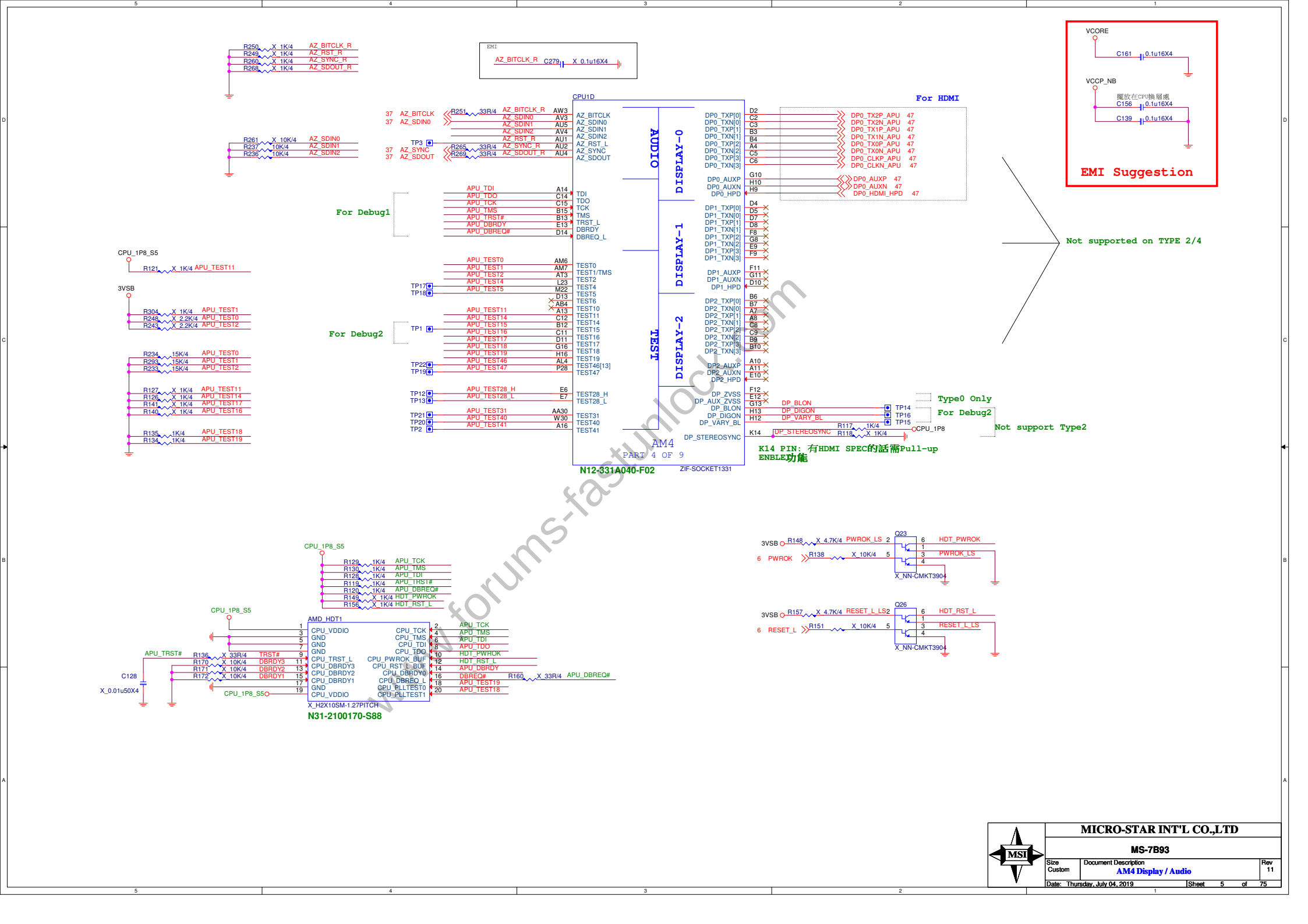
EMI Suggestion
VCORE
VCCP_NB
For HDMI
For Debug1
For Debug2
Not supported on TYPE 2/4
Type0 Only
For Debug2
Not support Type2
K14 PIN: 有HDMI SPEC的話需Pull-up
ENBLE功能
CPU1D
AUDIO
DISPLAY-0
DISPLAY-1
DISPLAY-2
TEST
AM4
PART 4 OF 9
N12-331A040-F02
ZIF-SOCKET1331
AMD_HDT1
N31-2100170-S88
X_H2X10SM-1.27PITCH
Q23
Q26
X_NN-CMKT3904
MICRO-STAR INT'L CO.,LTD
MS-7B93
AM4 Display / Audio
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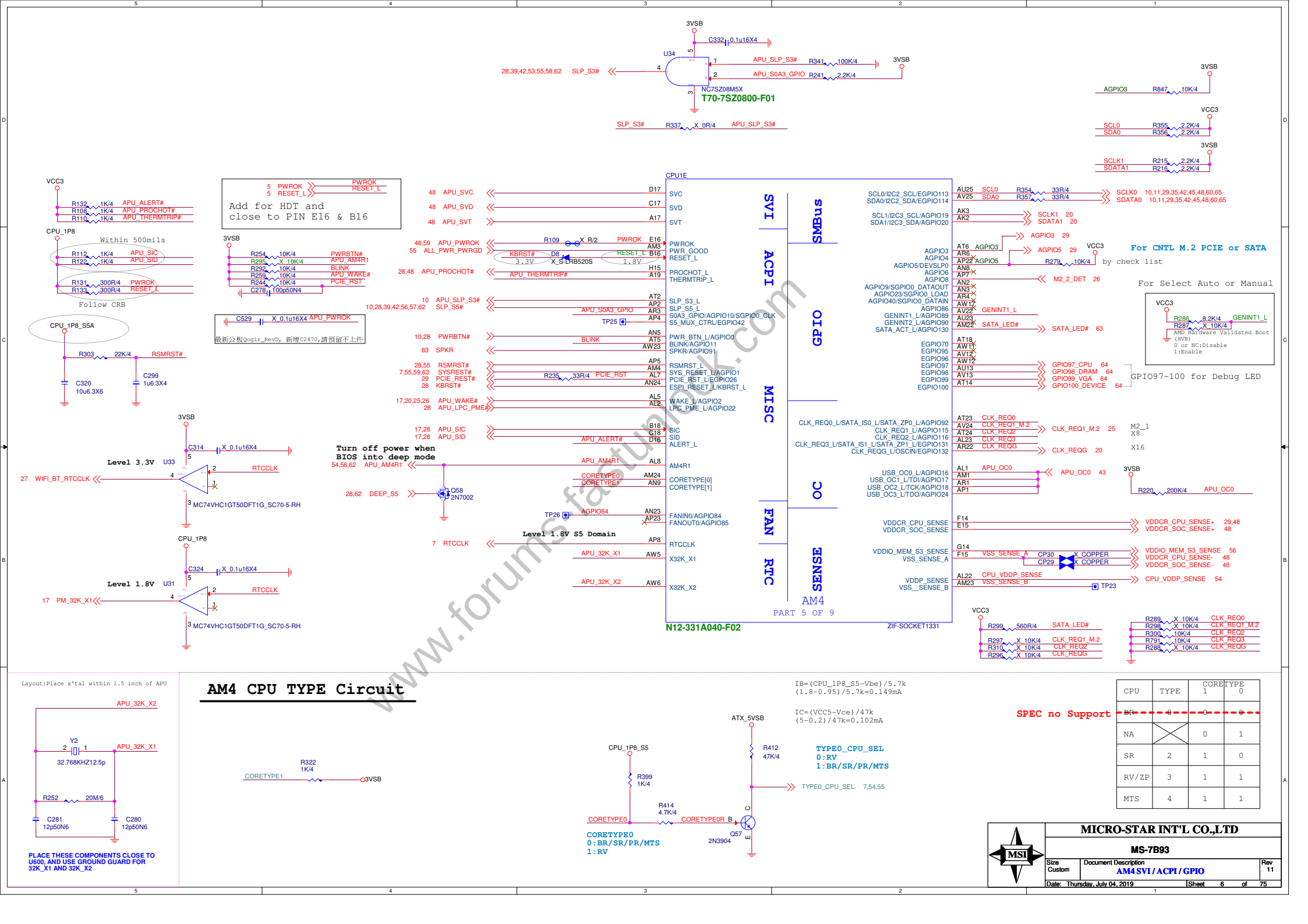
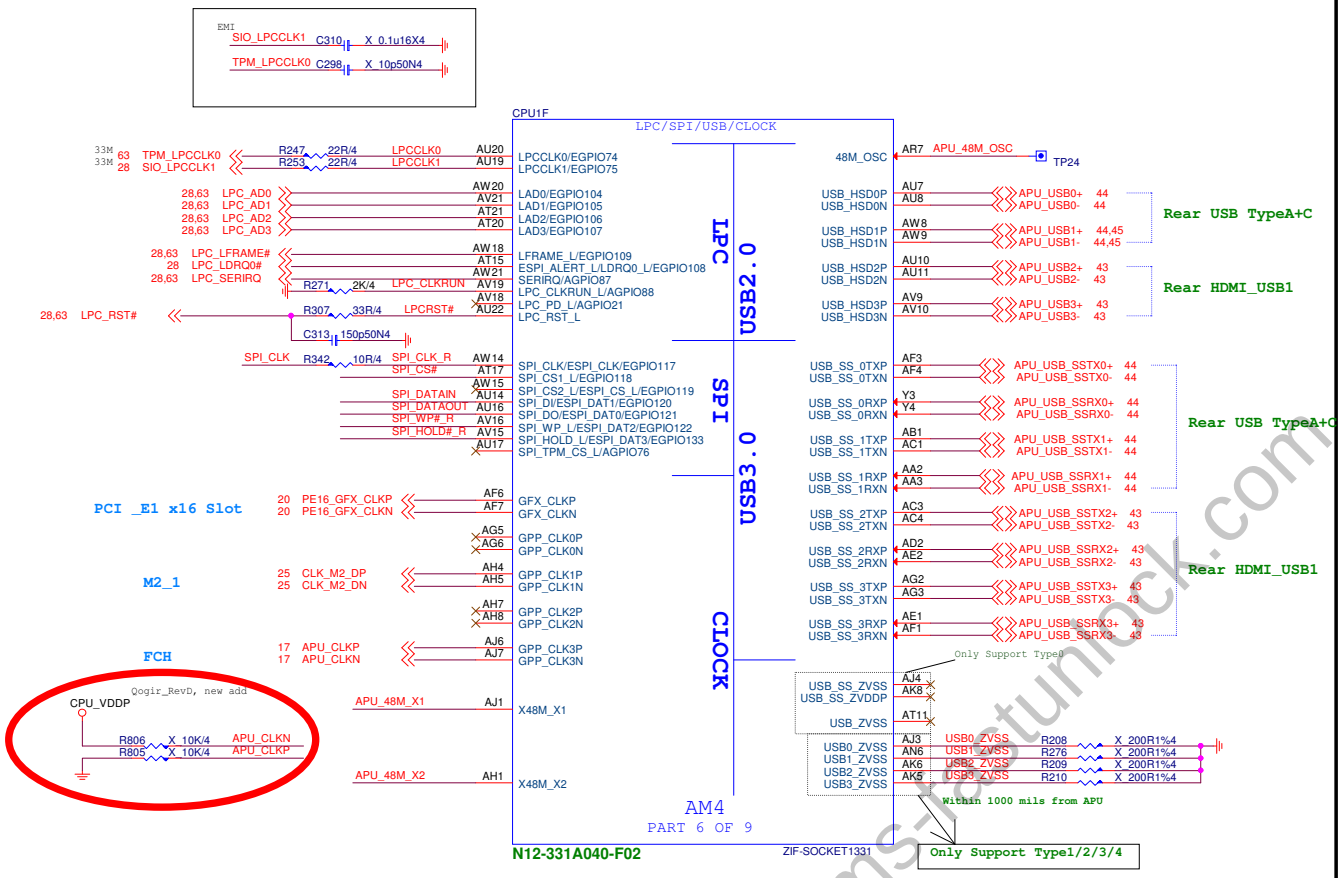


CPU	TYPE	CORETYPE 1	CORETYPE 0
~~BR~~	~~0~~	~~0~~	~~0~~
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	1



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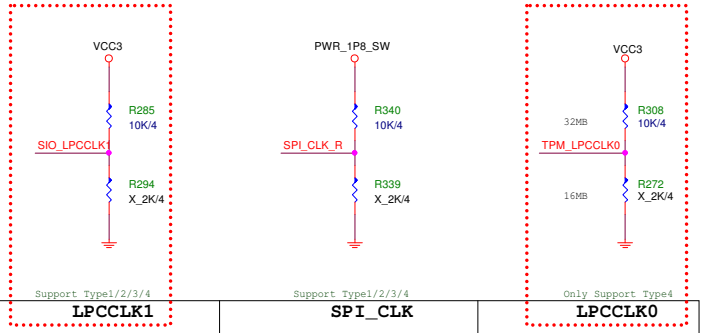
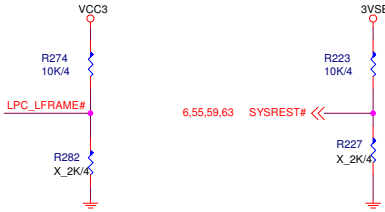
Strapping Options

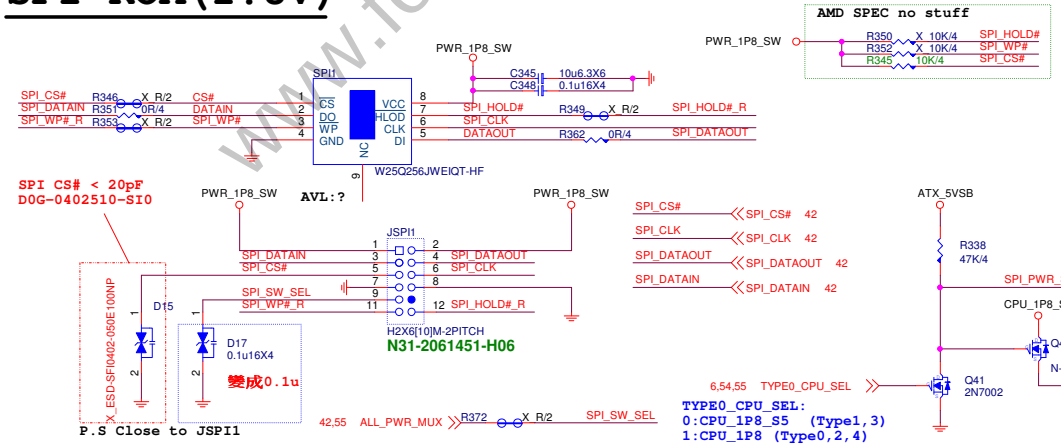


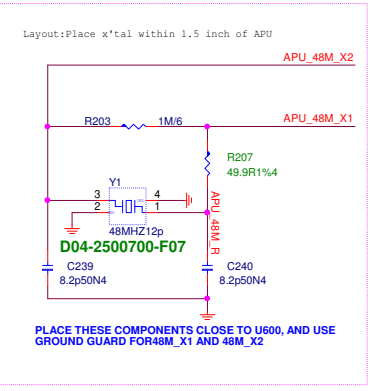
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image (Default)
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

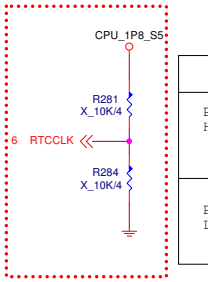


	AGPIO3	LFRAME	SYSREST#
	Only Support Type0	Support Type1/2/3/4	Support Type1/2/3/4
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)







	RTCCLK
	Only Support Type4
PULL HIGH	RTCCLK is input and is used as the bypass clock (Default)
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

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Size: Custom | Document Description: AM4 LPC / SPI / USB / CLK / STRAP | Rev: 11

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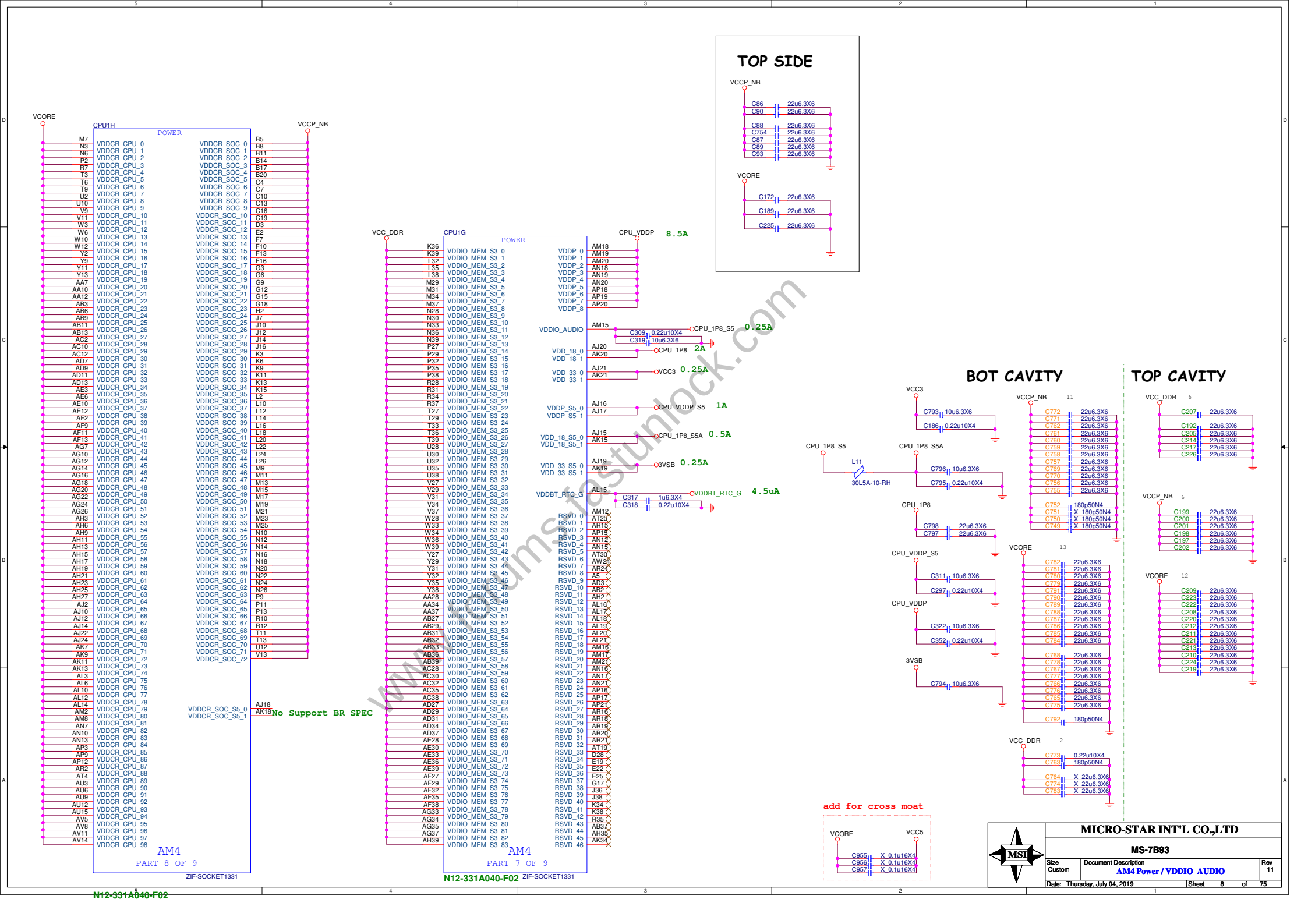

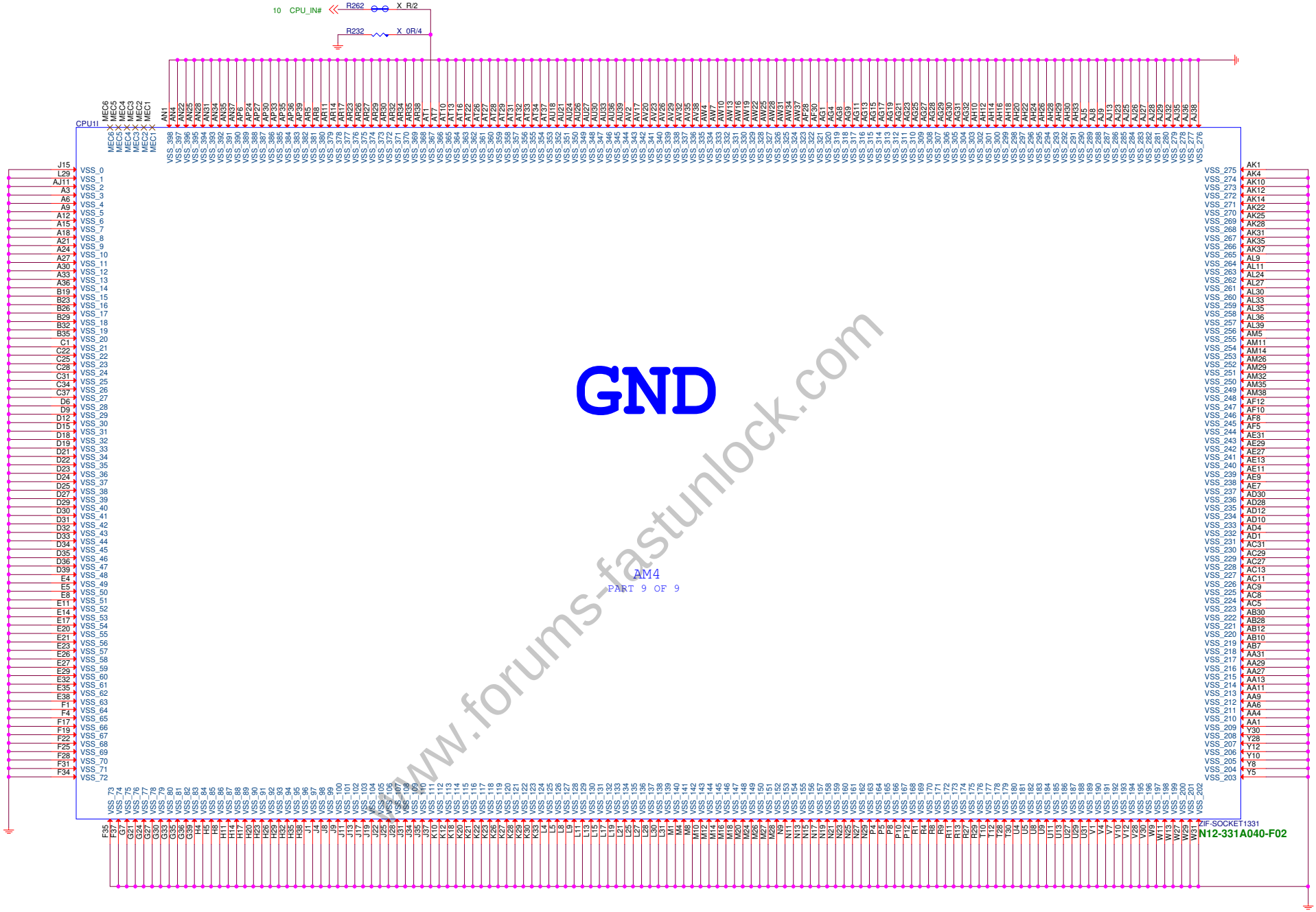

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Size: Custom	Document Description: AM4 GND
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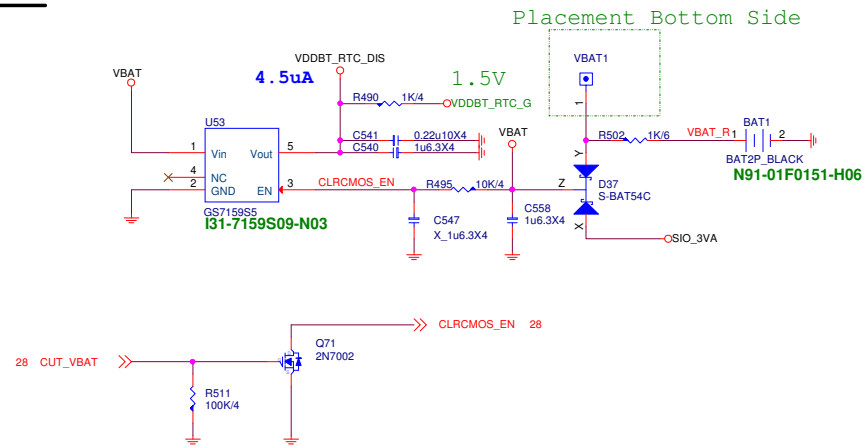
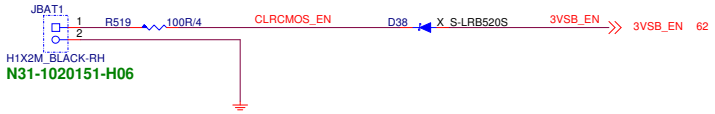
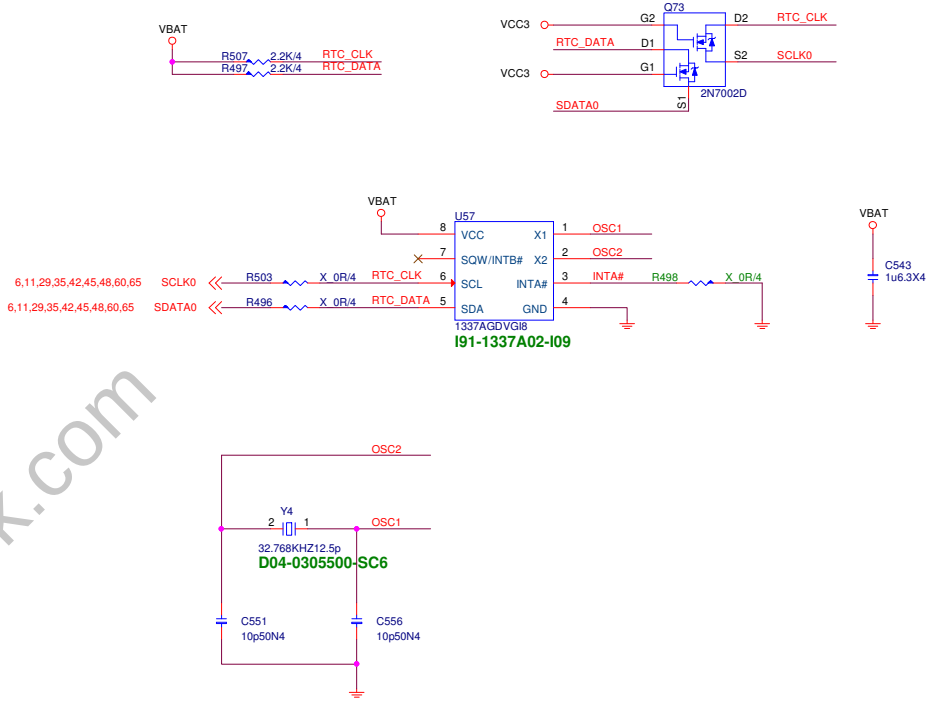
RTC & Clear CMOS Circuit

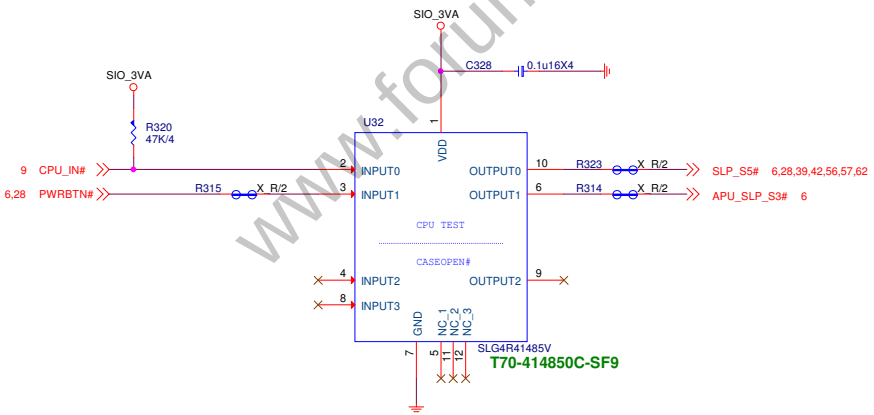


Clear CMOS button



RTC Backup





MICRO-STAR INT'L CO.,LTD

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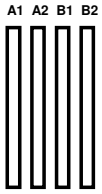

DIMMA1A

DIMMA2A

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

DDRIV-288P
N13-2880581-L06

AVL: N13-2880441-F02

DDRIV-288P
N13-2880581-L06

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7B93
Size	Custom
Document Description	DDR4 - DIMM CH-A
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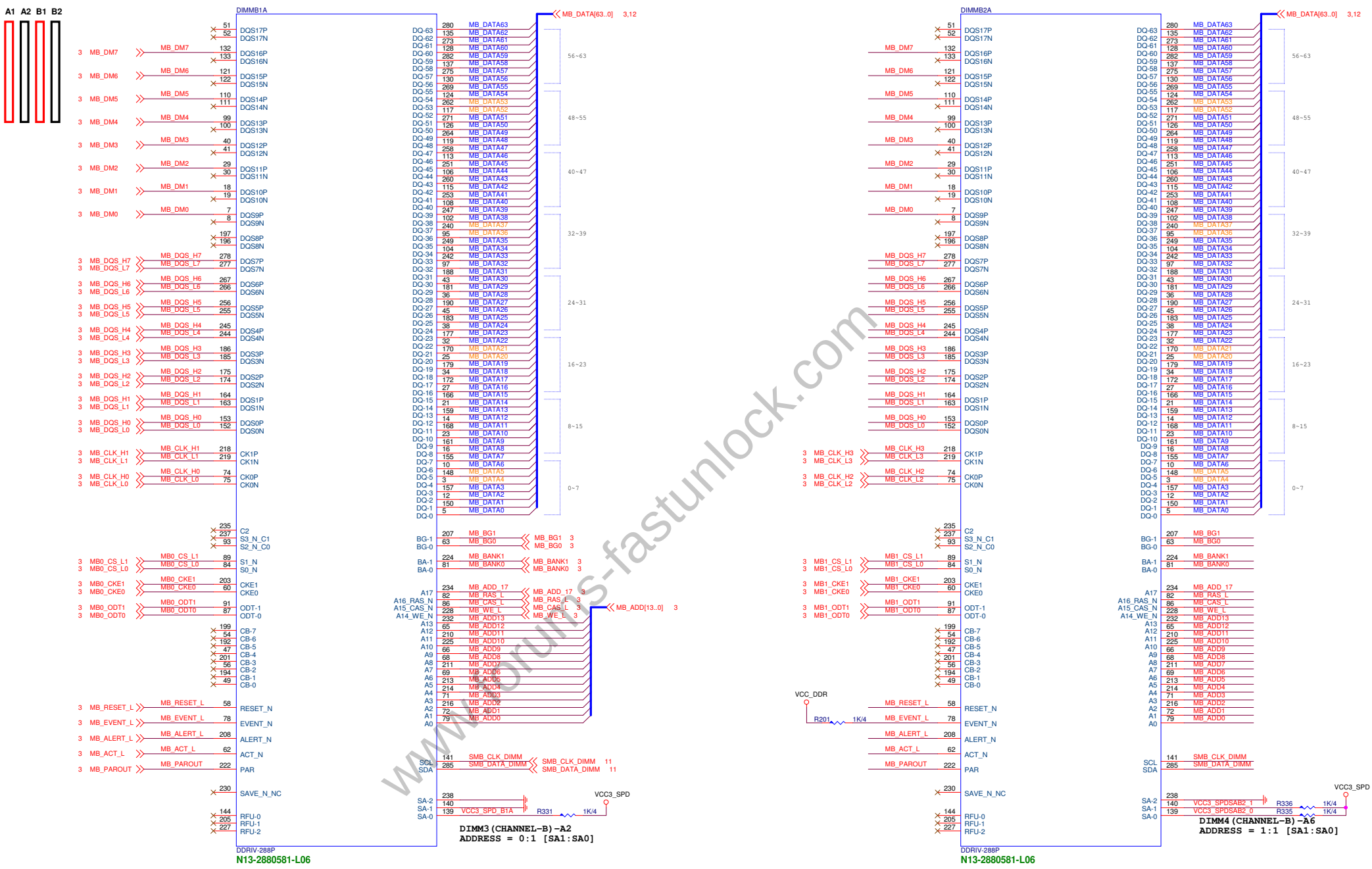

MICRO-STAR INT'L CO.,LTD	
MS-7B93	
Size: Custom	Document Description: DDR4 - DIMM CH-B
Rev: 11	
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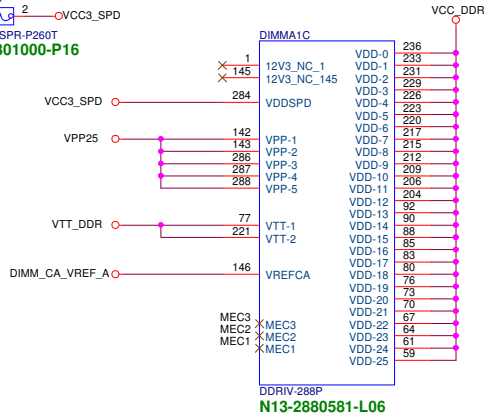
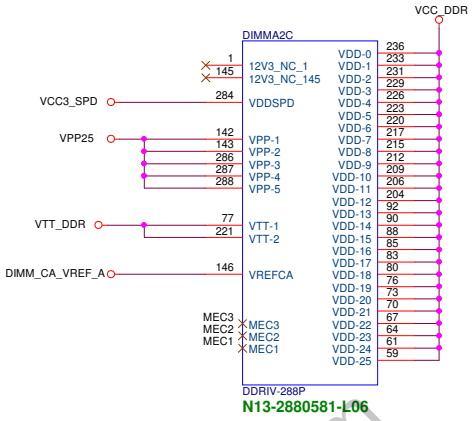
avl:D08-0301100-B07

F6
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC



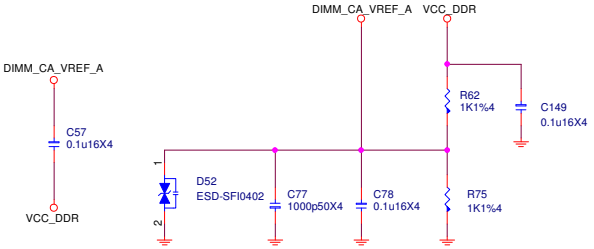
N13-2880581-L06

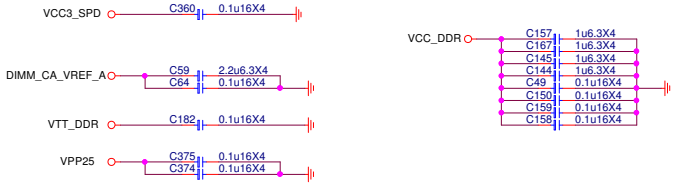


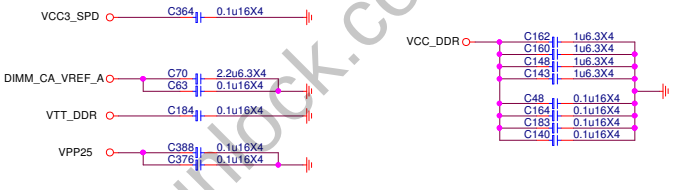
N13-2880581-L06

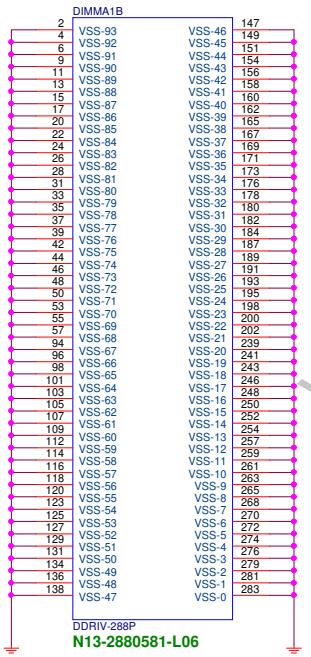
DDR VREF

(place resistors close to DIMMs)

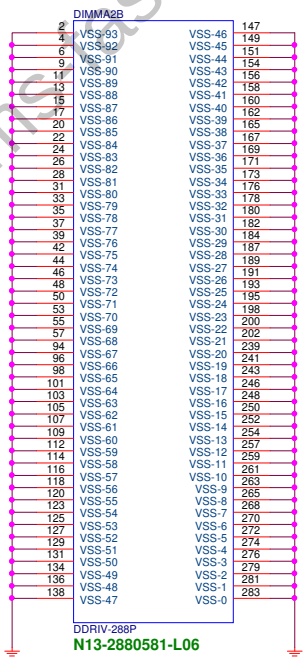








N13-2880581-L06



N13-2880581-L06

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Custom	DDR4 - POWER/GND-1	11

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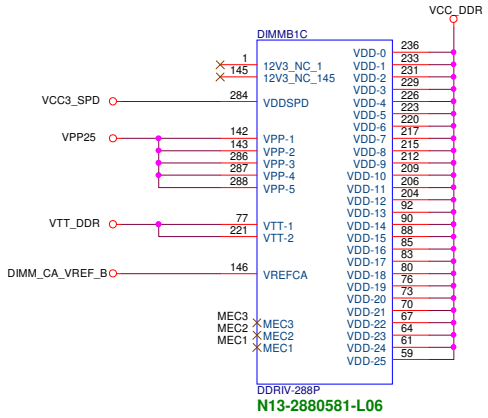
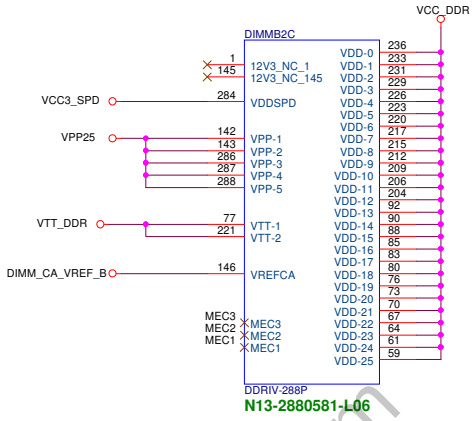
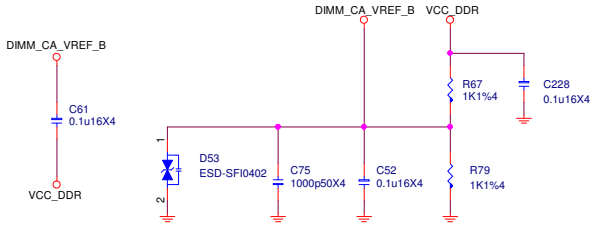




DDR VREF

(place resistors close to DIMMs)



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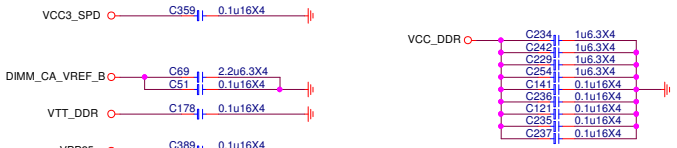

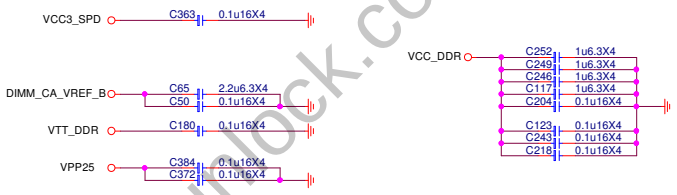

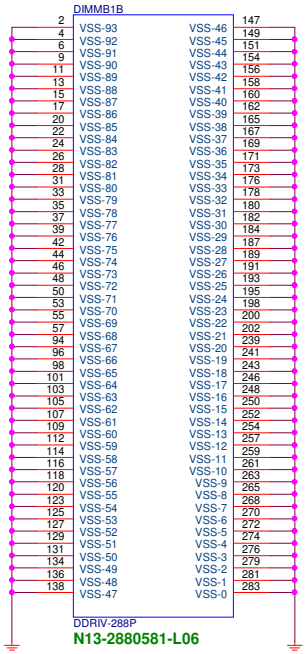

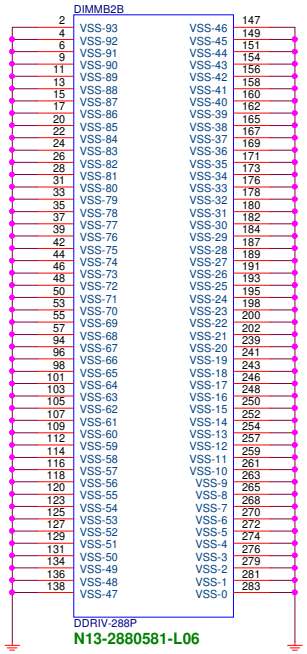

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MS-7B93

Size	Document Description	Rev
Custom	DDR4 - POWER/GND-2	11

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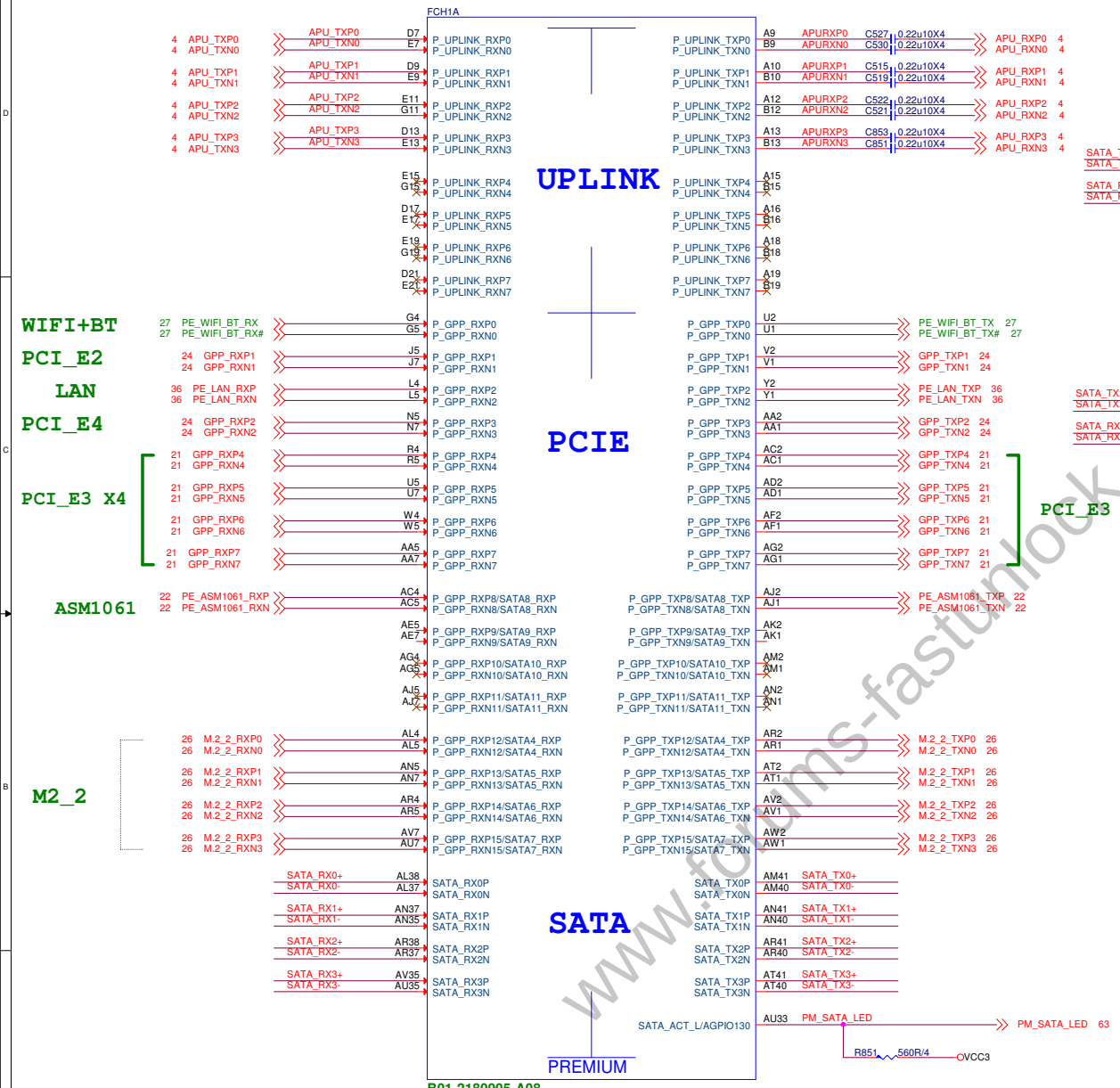
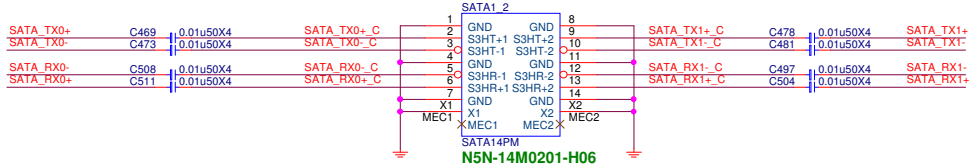


SATA Connector

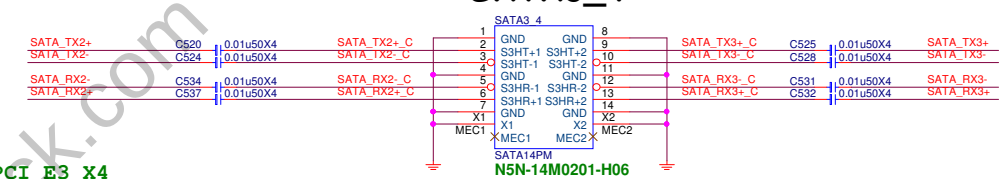
SATA1_2



N5N-14M0201-H06

AVL:N5N-14M0201-L06

SATA3_4

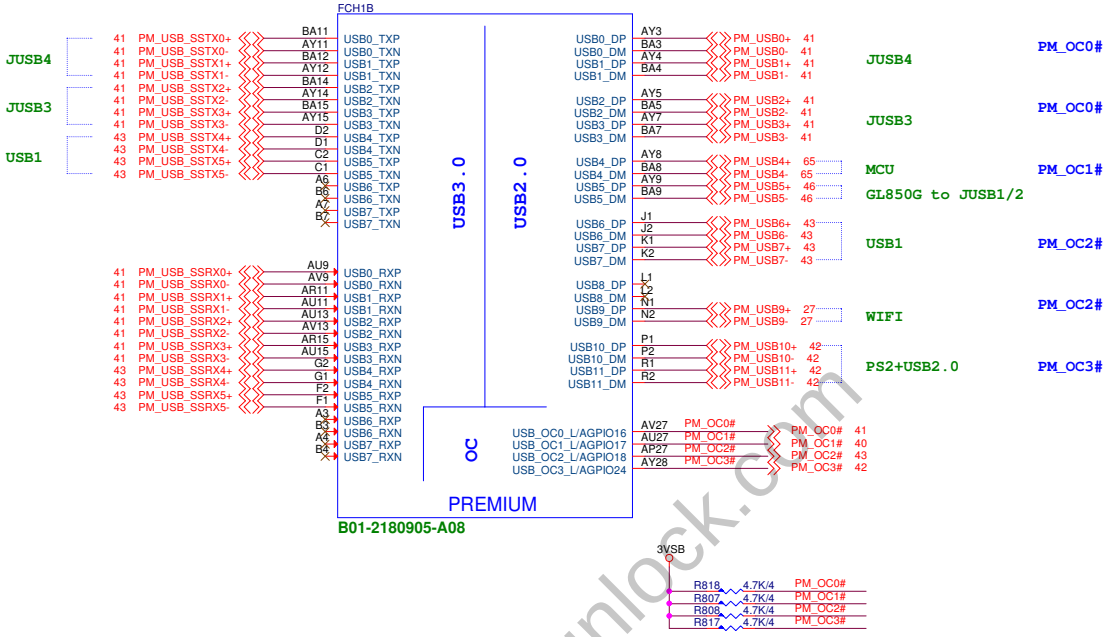


N5N-14M0201-H06

AVL:N5N-14M0201-L06

MICRO-STAR INT'L CO.,LTD		
MS-7B93		
Size: Custom	Document Description: Premium - PCIE/SATA	Rev: 11
Date: Thursday, July 04, 2019	Sheet 15 of 75	

HC0 will control USB[3:0]_RX/TX{P/N} and USB[5:0]_D{P/M}
HC1 will control USB[7:4]_RX/TX{P/N} and USB[11:6]_D{P/M}



B01-2180905-A08

HC0 will control USB[3:0]_RX/TX{P/N} and USB[5:0]_D{P/M}
HC1 will control USB[7:4]_RX/TX{P/N} and USB[11:6]_D{P/M}

1	2	3	4	5	6	7	8
PCIE	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE	PCIE
Intel WIFI (1T1R)	PCI_E2	PCI_E4	NA	PCI_E3			

M2_2支援PCIE/SATA mode

9	10	11	12	13	14	15	16	17	18	19	20
SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA	SATA
				SATAE/GEN4 PCIEx4				SATAE/GEN4 PCIEx4			
S1	S2	S3	S4	M2_2				LAN	ASM1061 (PCIe->SATA* 2)	NA	NA
									S5/S6		

21	22	23	24	25	26	27	28	29	30	31	32	31	32
U3.1	U3.1	U3.1	U3.1	U2	U2	U3.1	U3.1	U3.1	U3.1	U2	U2	NA	NA
Front U3 GEN1		Front U3 GEN1		MCU	USB hub ← 轉接 (GL85	Rear U3.1 GEN2 type A		NA	WIFI	Rear U2			

CPU	1	2	3	4	5	6	7	8
ZEN 2 Processor	SATA	SATA	Gen4 x2 PCIe		U3.1	U3.1	U3.1	U3.1
	Gen4 x4 PCIe NVME				U3.1	U3.1	U3.1	U3.1
Carbon AC	M2_1				Rear U3.1 GEN1 type A		Rear U3.1 GEN2 A+C	

M2_1支援PCIE mode

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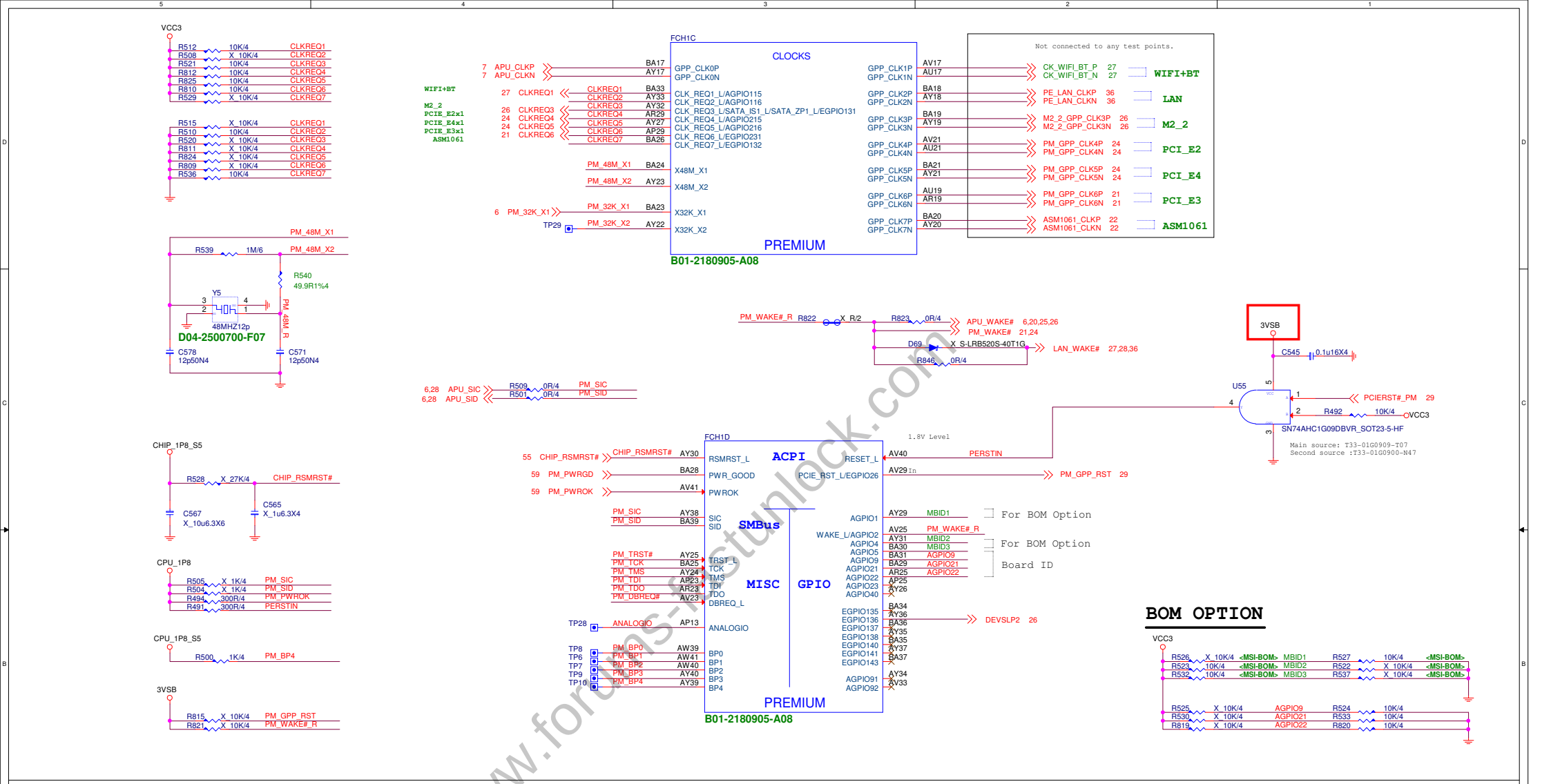
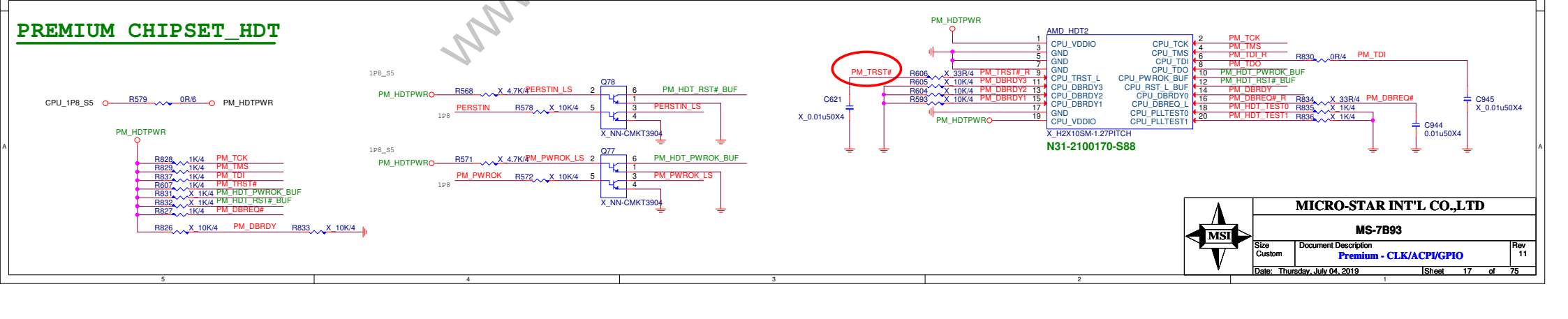


PREMIUM CHIPSET_HDT



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MS-7B93		
Size: Custom	Document Description: Premium - CLK/ACPI/GPIO	Rev: 11
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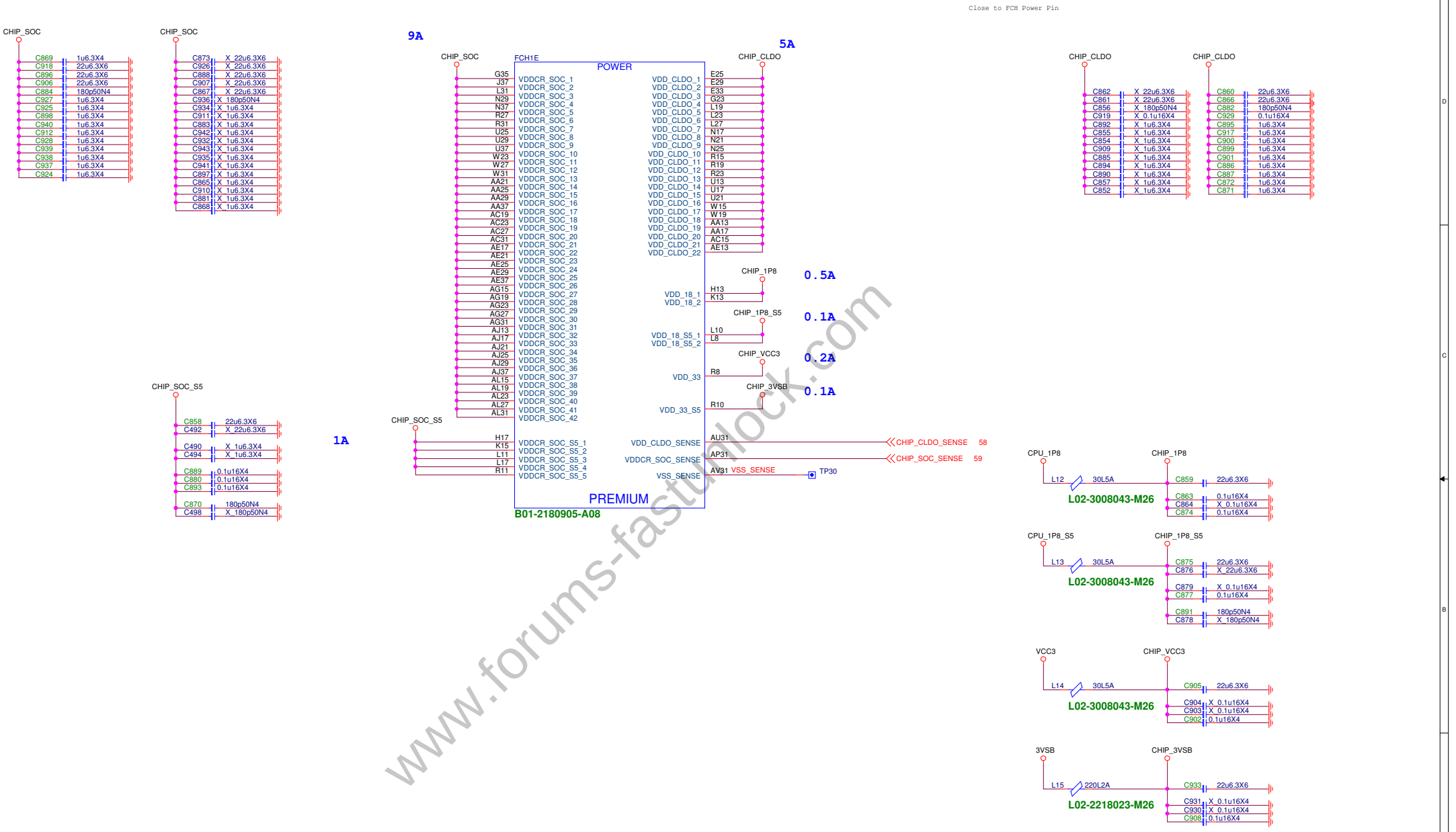

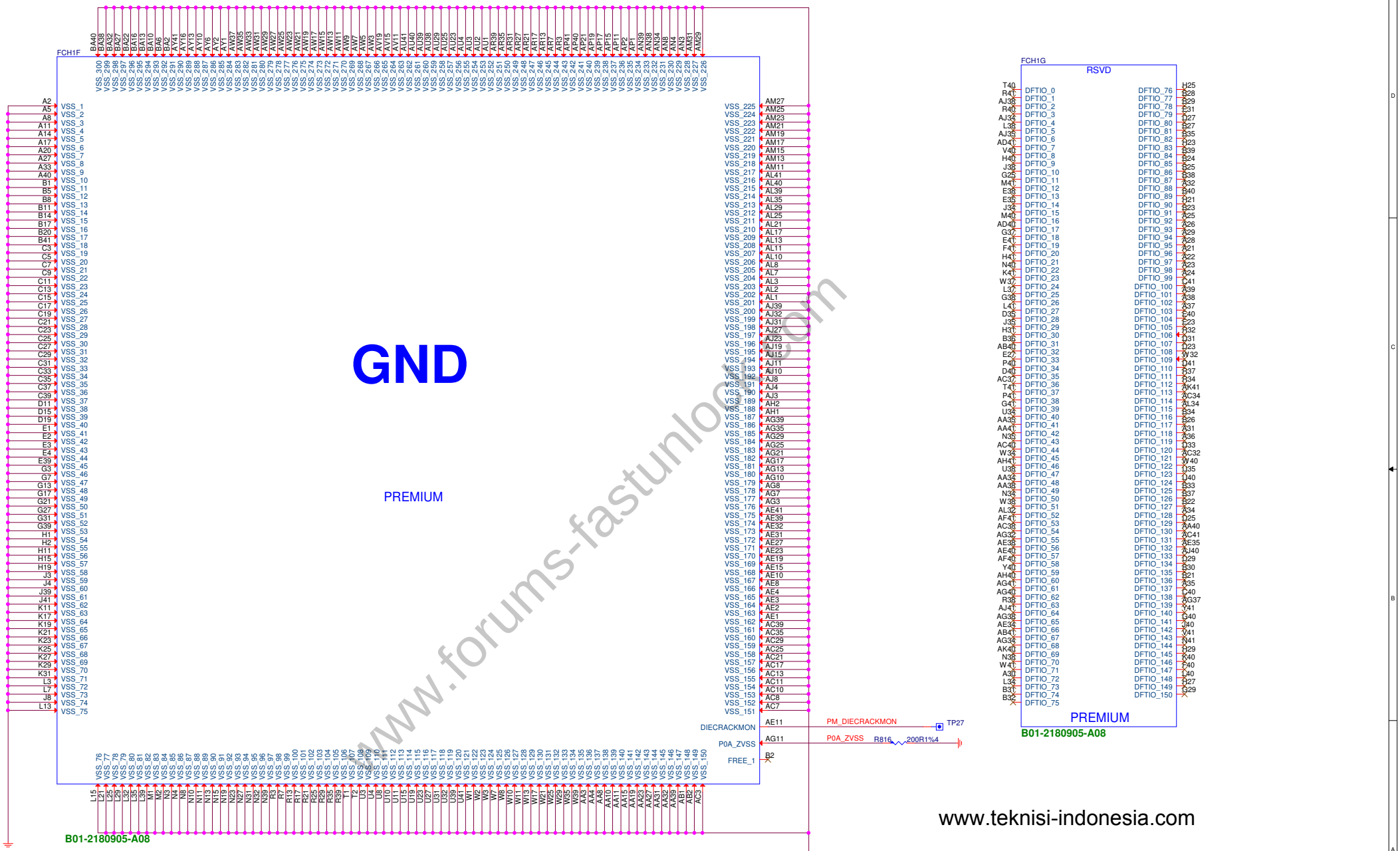

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MS-7B93		
Size: Custom	Document Description: Premium - GND	Rev: 11
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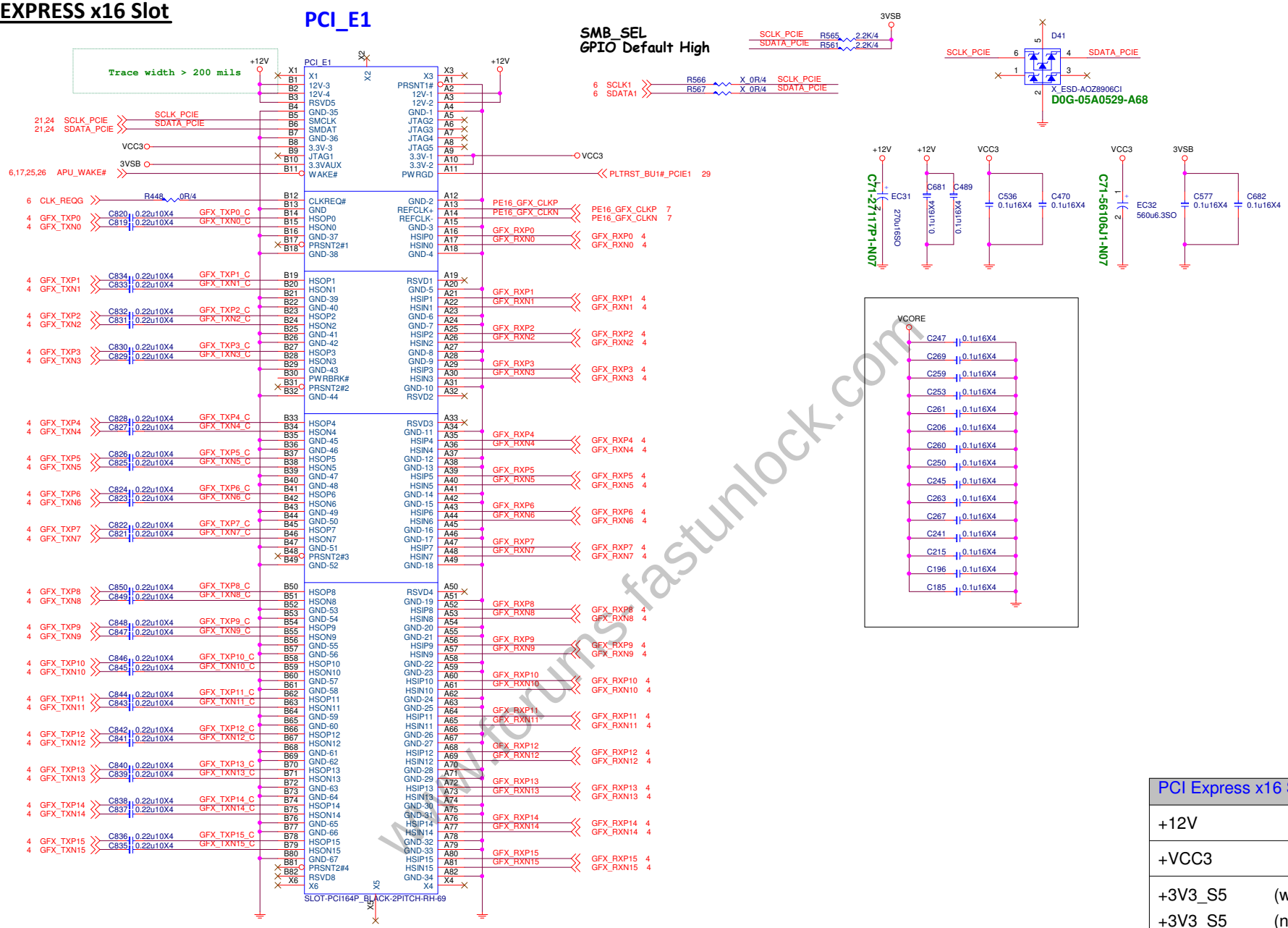
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Size: Custom	Document Description: PCI_E2 (X16)
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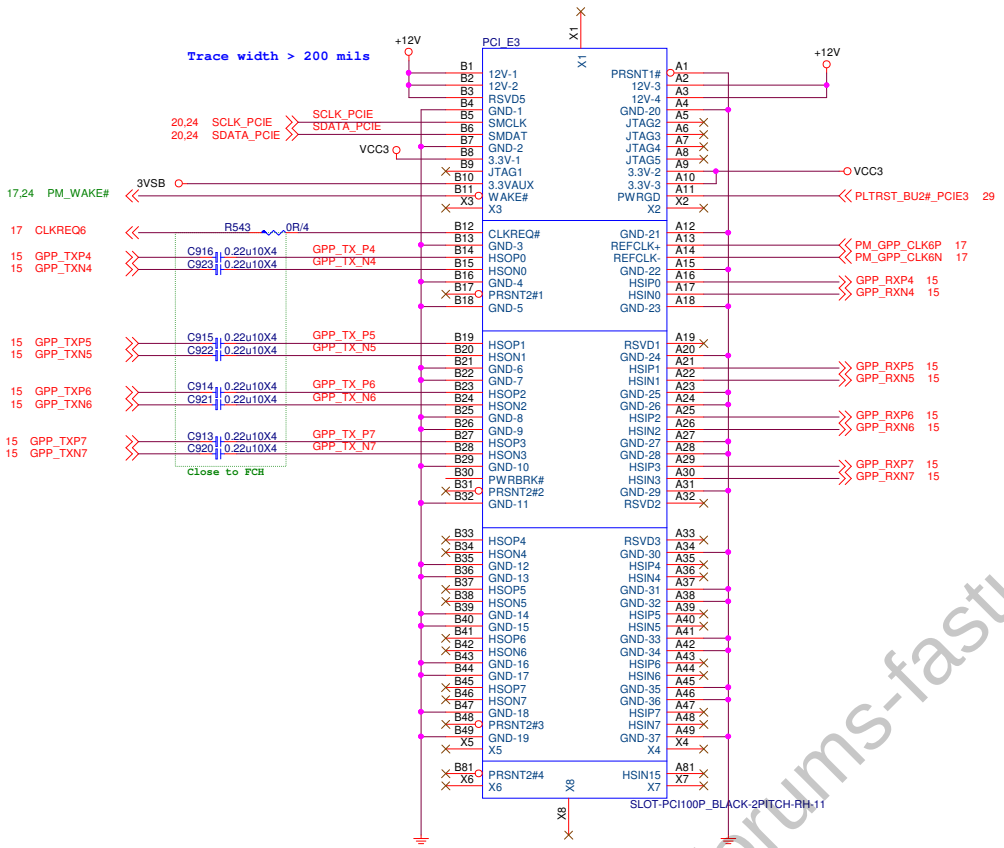
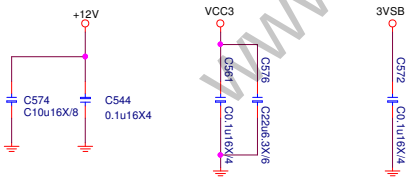
PCI_EXPRESS x4 SLOT

PCI_E3 X4





PCI Express x4 Slot		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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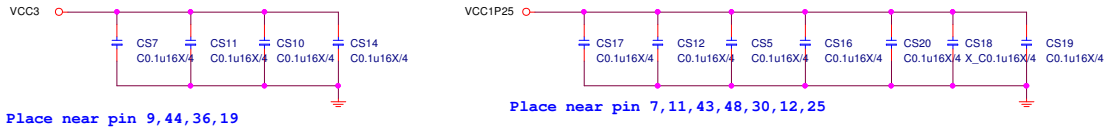
SATA Connector

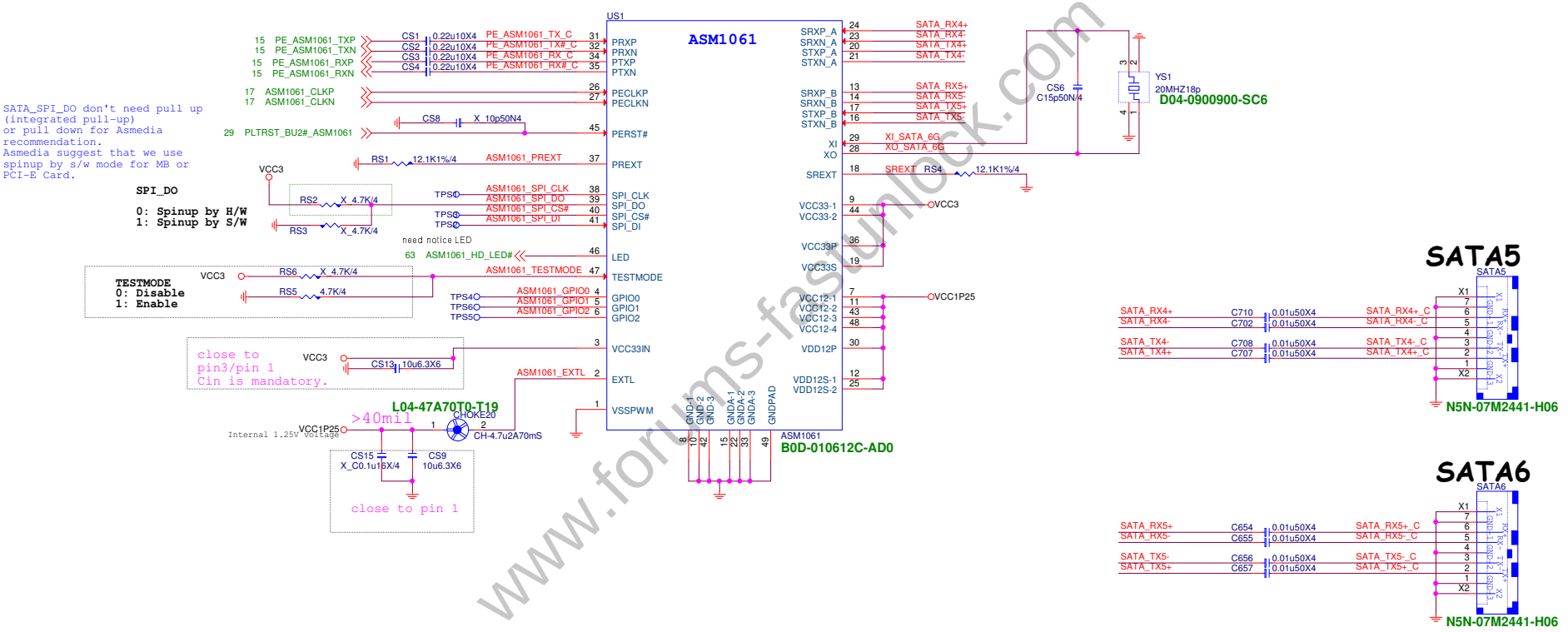
1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



ASM1061 SATA6G



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MS-7B93			
Size: Custom	Document Description: PCIE to SATA (ASM1061)		Rev: 11
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PCIE GEN4 MUX

For PCIE1 & PCIE3

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MS-7B93		
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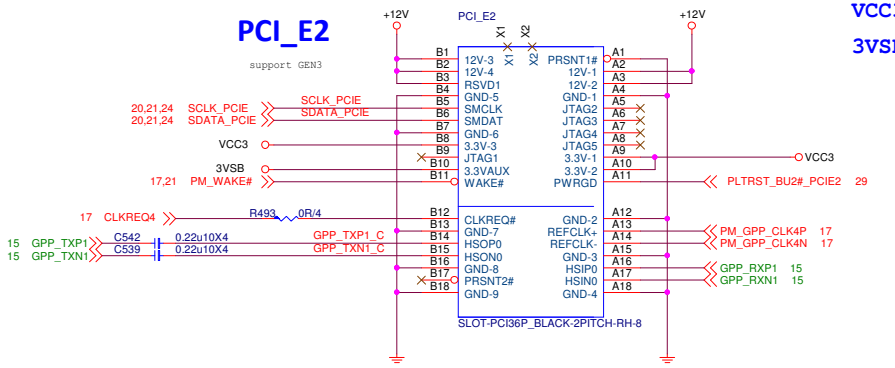
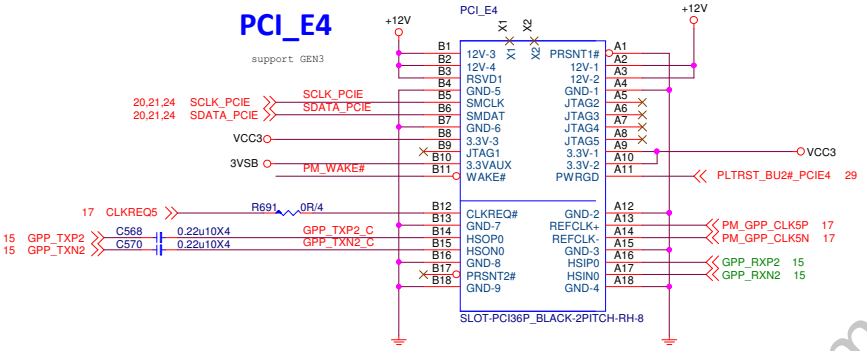
PCI EXPRESS X1 SLOT

12V - 0.5A

VCC3 - 3A

3VSBV - 375mA





PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 20mA

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MS-7B93

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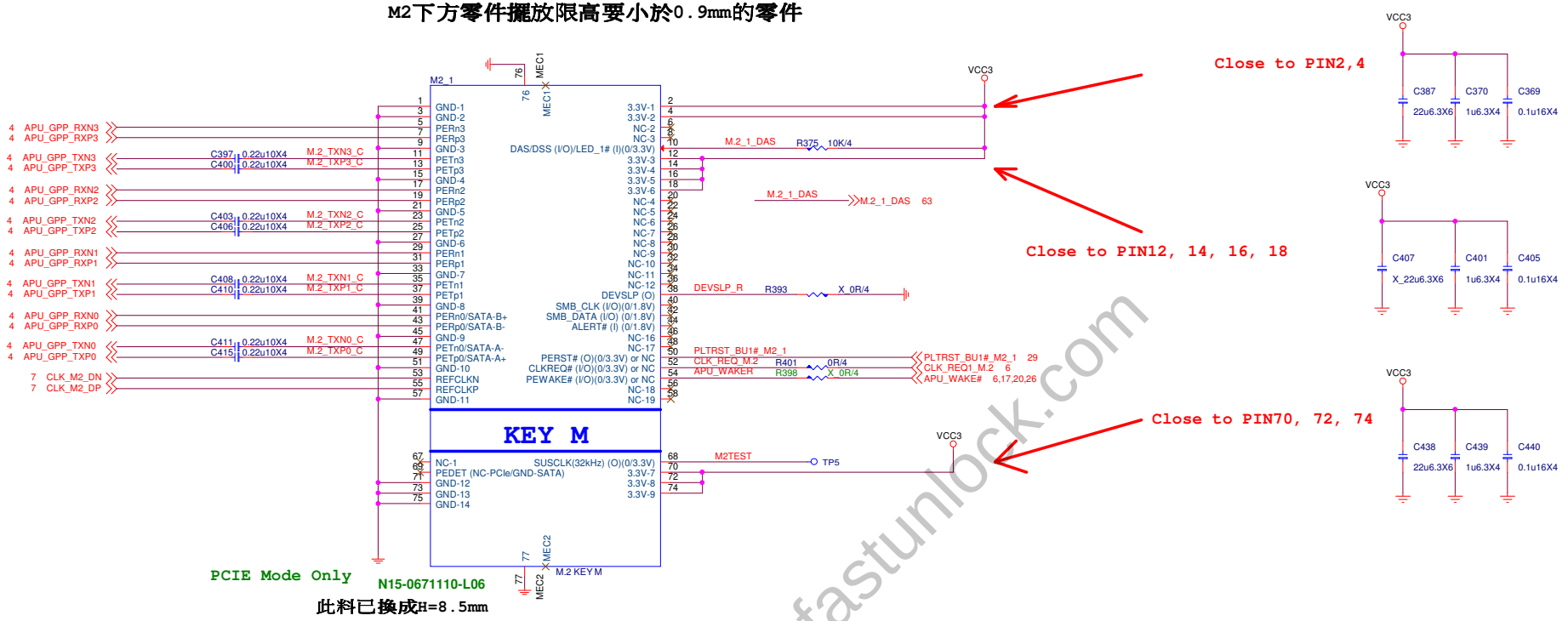
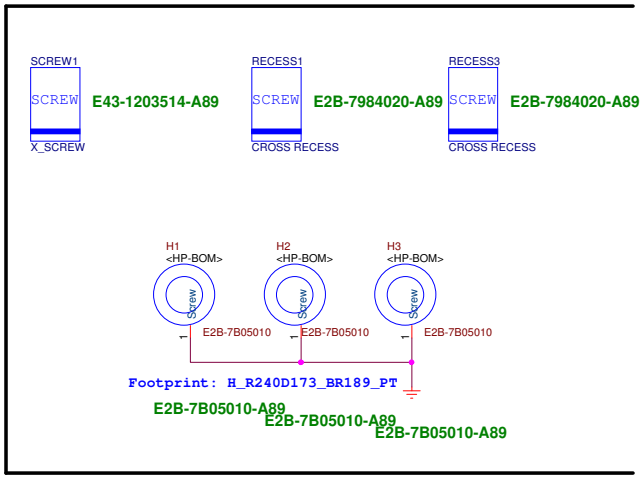
M.2_1 Connector

VCC3 4.25A
Max: 14W

M2下方零件擺放限高要小於0.9mm的零件





MICRO-STAR INT'L CO.,LTD

MS-7B93

Size: Custom | Document Description: M2_1 | Rev: 11

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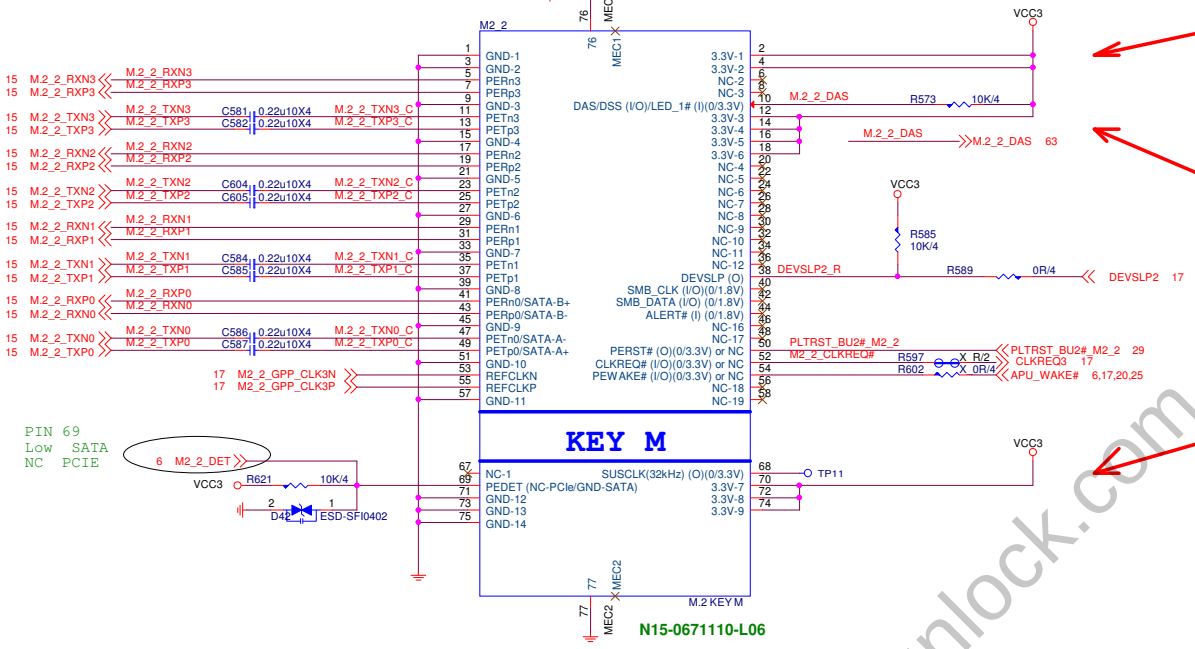
M.2_2 Connector

M2下方零件擺放限高要小於0.9mm的零件

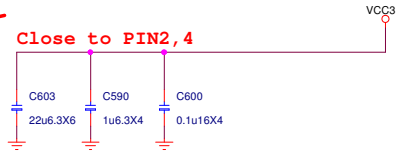
VCC3 4.25A
Max: 14W



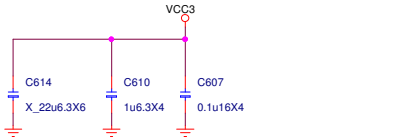
N15-0671110-L06

此料已換成H=8.5mm

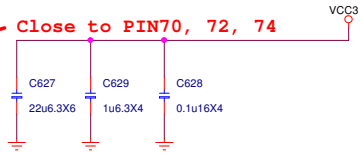
Close to PIN2,4

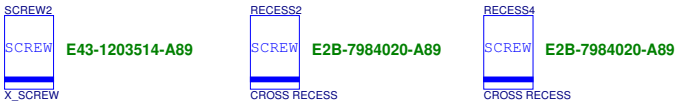


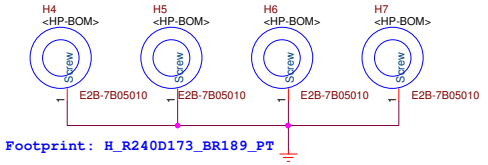
Close to PIN12, 14, 16, 18



Close to PIN70, 72, 74







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EMI

NEAR CONNECTOR

16 PM_USB9+ — PM_USB9+ — U25 — ESD-AOZ8906CI

16 PM_USB9- — PM_USB9-

3VSB — C133 — X_0.1u16X4

780mA

3VSB — C131 1u6.3X4 — C135 10u6.3X6 — C132 0.01u50X4

M2_WIFI1 — MEC2

1	GND-1	3.3V-1	2
PM_USB9+ 3	USB_D+	3.3V-2	4
PM_USB9- 5	USB_D-	LED1#	6
7	GND-11	PCM_CLK / I2S SCK	8
9	SDIO CLK	PCM_SYNC / I2S WS	10
11	SDIO CMD	PCM_IN / I2S SD_IN	12
13	SDIO DATA0	PCM_OUT / I2S SD_OUT	14
15	SDIO DATA1	LED2#	16
17	SDIO DATA2	GND-2	18
19	SDIO DATA3	UART WAKE#	20
21	SDIO WAKE#	UART RXD	22
23	SDIO RESET#		

KEY E

33	GND-10	UART TXD	32
15 PE_WIFI_BT_TX — 0.22u10X4 C173 — PE_WIFI_BT_TXC	35 PETp0	UART CTS	34
15 PE_WIFI_BT_TX# — 0.22u10X4 C175 — PE_WIFI_BT_TX#C	37 PETn0	UART RTS	36
39	GND-9	VENDOR DEFINED-1	38
15 PE_WIFI_BT_RX	41 PERp0	VENDOR DEFINED-2	40
15 PE_WIFI_BT_RX#	43 PERn0	VENDOR DEFINED-3	42
45	GND-8	COEX3	44
17 CK_WIFI_BT_P	47 REFCLKP0	COEX2	46
17 CK_WIFI_BT_N	49 REFCLKN0	COEX1	48
51	GND-7	SUSCLK	50 WIFI_BT_RTCCLK_R — R145 0R/4 — WIFI_BT_RTCCLK 6
17 CLKREQ1 — R177 X R/2 — CLKREQ1_R	53 CLKREQ0#	PERST0#	52 PLTRST_BU2#_M2_3 29
17,28,36 LAN_WAKE#	55 PEWAKE0#	W_DISABLE2#	54 BT_DISABLE_L# — R143 3.3KR/4 — 3VSB
57	GND-6	W_DISABLE1#	56 WIFI_DISABLE_L# — R142 3.3KR/4
59	RESERVED / PETp1	I2C DATA	58
61	RESERVED / PETn1	I2C CLK	60
63	GND-5	ALERT#	62
65	RESERVED / PERp1	RESERVED	64
67	RESERVED / PERn1	UIM_SWP / PERST1#	66
69	GND-4	UIM_POWER_SNK / CLKREQ1#	68
71	RESERVED / REFCLKP1	UIM_POWER_SRC/GPIO1 / PEWAKE1#	70
73	RESERVED / REFCLKN1	3.3V-3	72 — 3VSB
75	GND-3	3.3V-4	74 — C138 0.01u50X4 — C137 1u6.3X4 — C136 10u6.3X6

MEC1

SLOT-NGFFCARD67P_BLACK-HF-46

N15-0670610-L06

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.

ATX_5VSB — R146 47K/4 — 3VSB — R124 47K/4 — Q22 2N7002D — G2 D1 G1 S1 S2 D2 BT_DISABLE_L#

28 WIFI_BTDIS# — WIFI_BTDIS#

ATX_5VSB — R125 47K/4 — Q21 2N7002D — G2 D1 G1 S1 S2 D2 WIFI_DISABLE_L#

WIFI_BTDIS#

下蓋 COVER1 — VR Cover — X1 X2 — X_E21-4442021-RH

E21-4442021-C22

SCREW3 SCREW — 鎖WiFi Module螺絲

E43-1204046-P65

SCREW4 SCREW — 鎖WiFi Module螺絲

E43-1204046-P65

Wireless1 — INTEL-9620 — Wireless

604-4442-080

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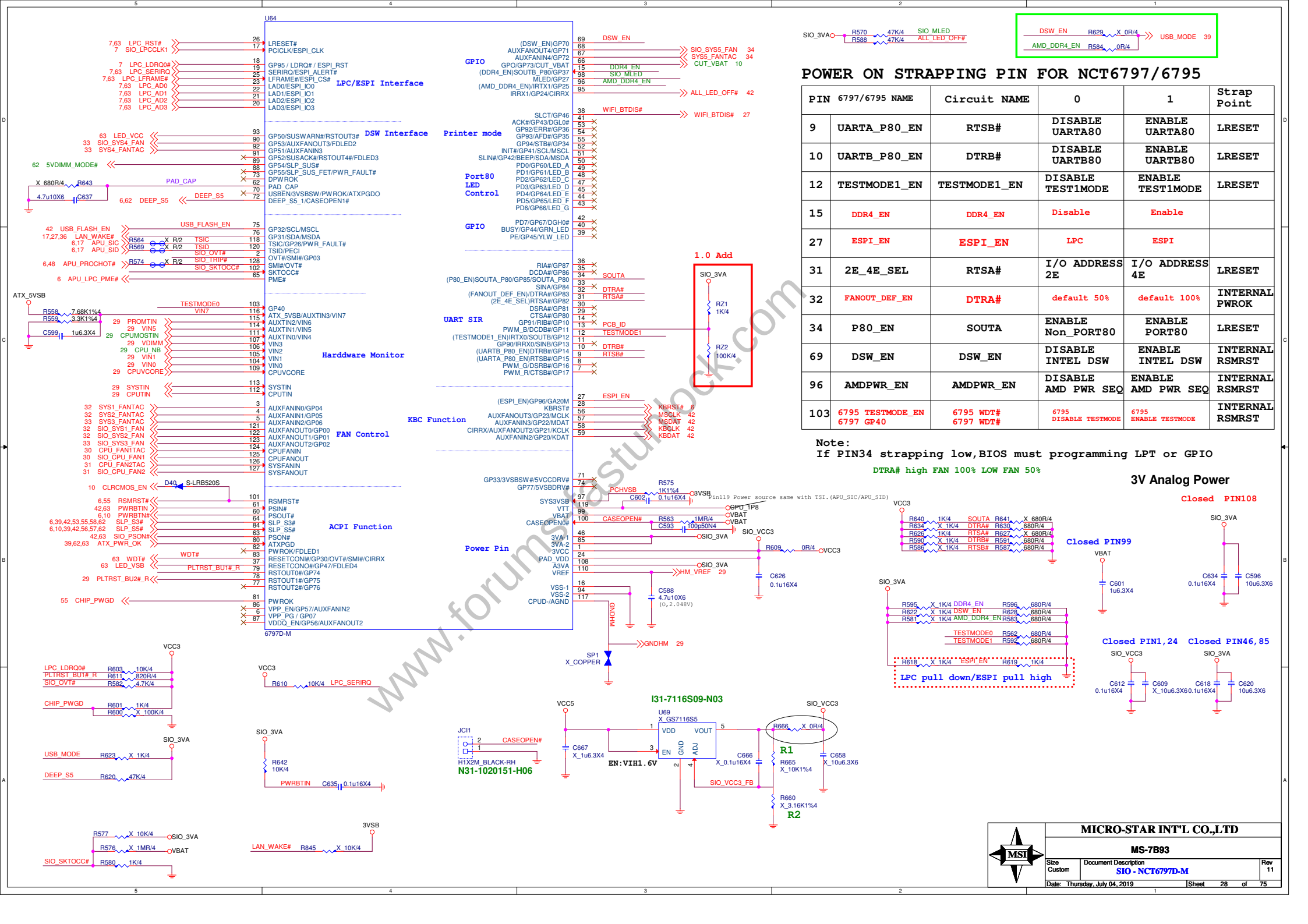

POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

DTRA# high FAN 100% LOW FAN 50%

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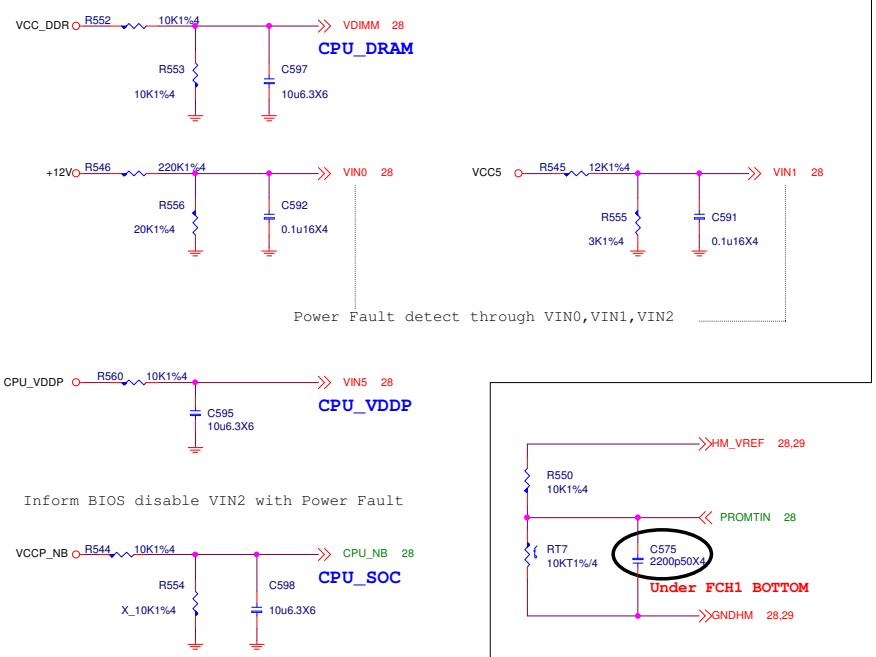
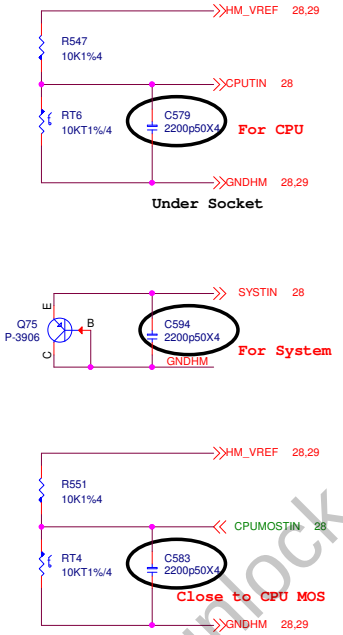
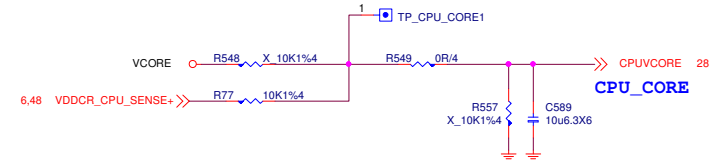
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

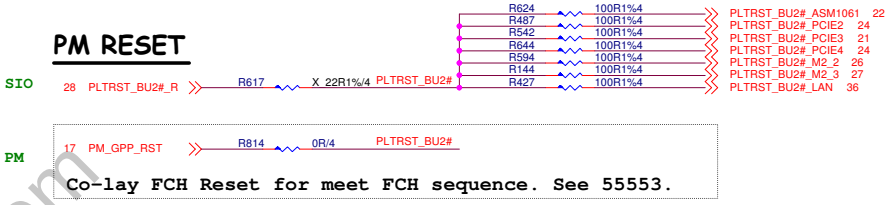


TEMP SENSOR

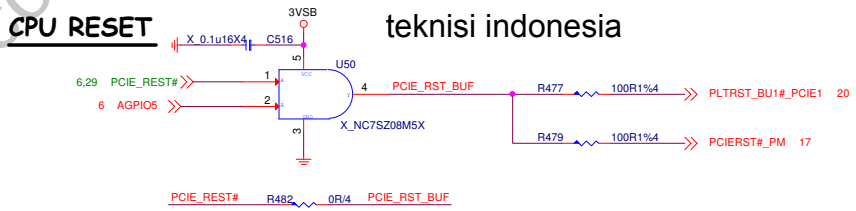


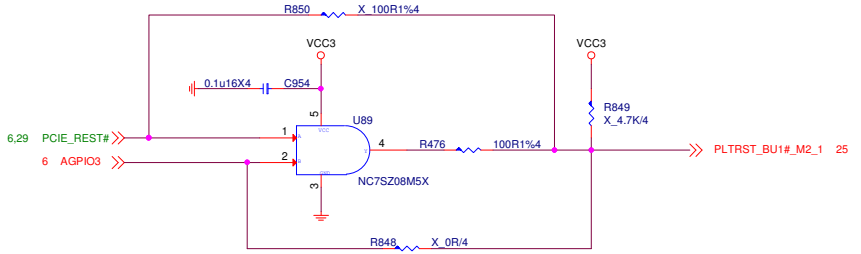


PM RESET

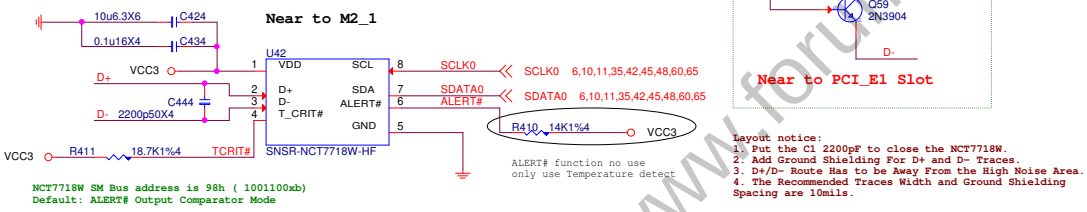


CPU RESET





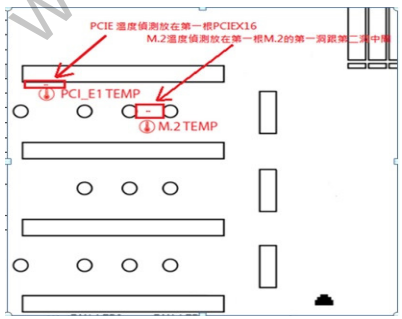
NCT7718W



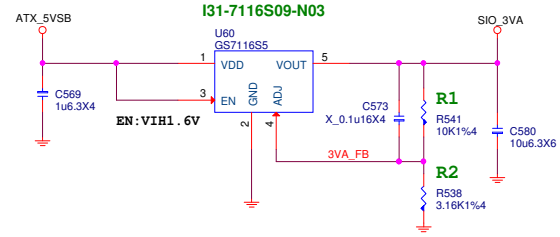
NCT7718W SM Bus address is 98h (1001100xb)
Default: ALERT# Output Comparator Mode

Layout notice:
1. Put the C1 2200pF to close the NCT7718W.
2. Add Ground Shielding For D+ and D- Traces.
3. D+/D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B93	
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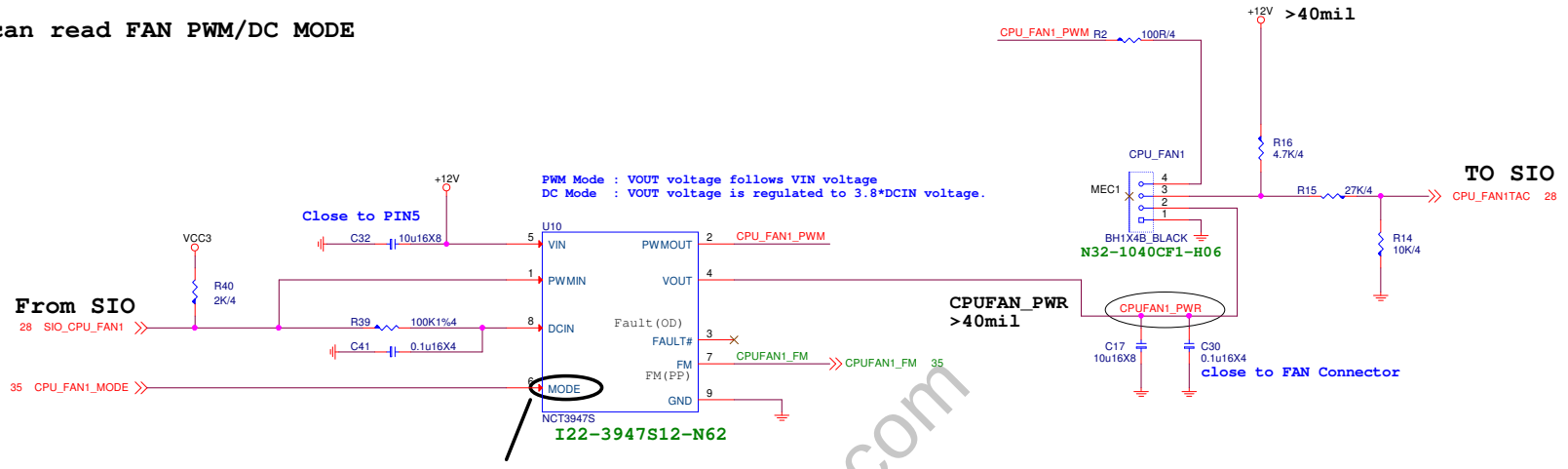
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD	
MS-7B93	
Size: Custom	Document Description: FAN TYPE-L CPUFAN1
Rev: 11	
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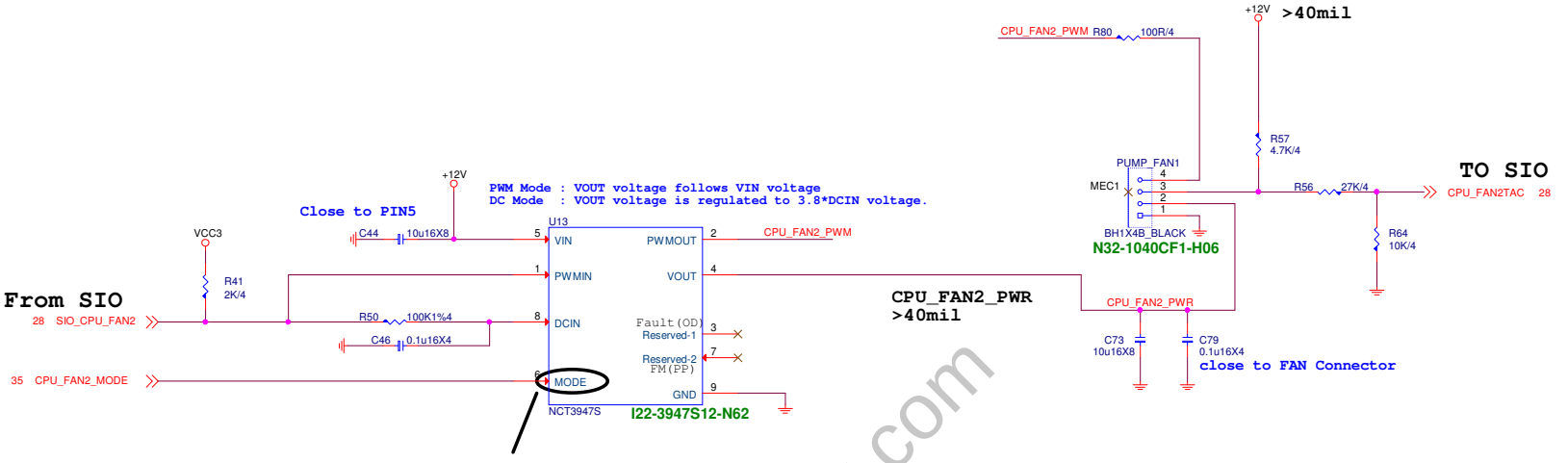
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD	
MS-7B93	
Size: Custom	Document Description: FAN TYPE-K PUMPFAN1
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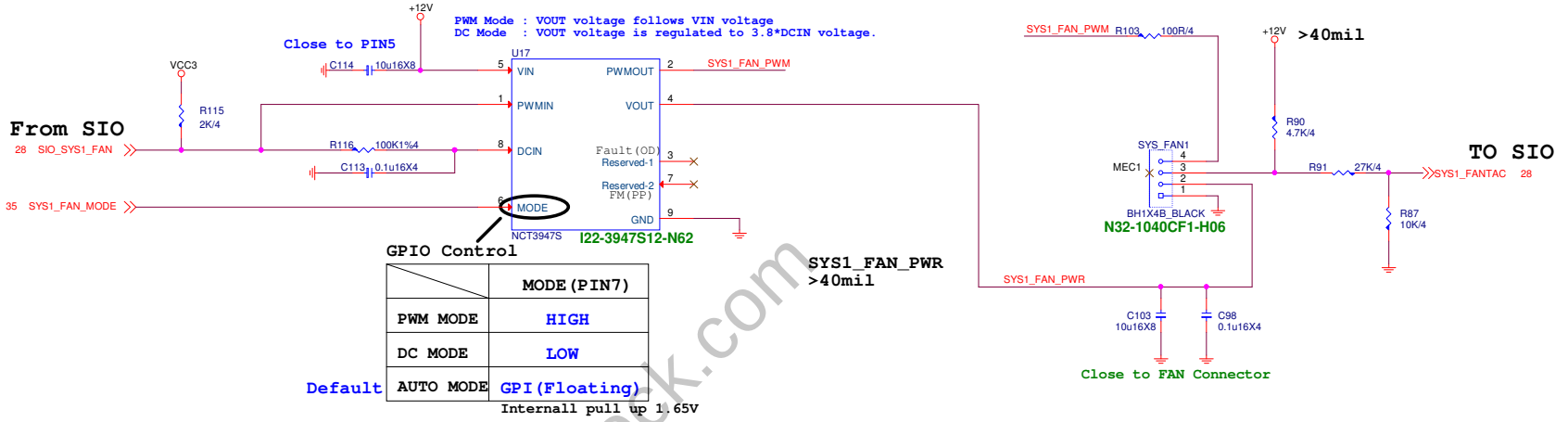
SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



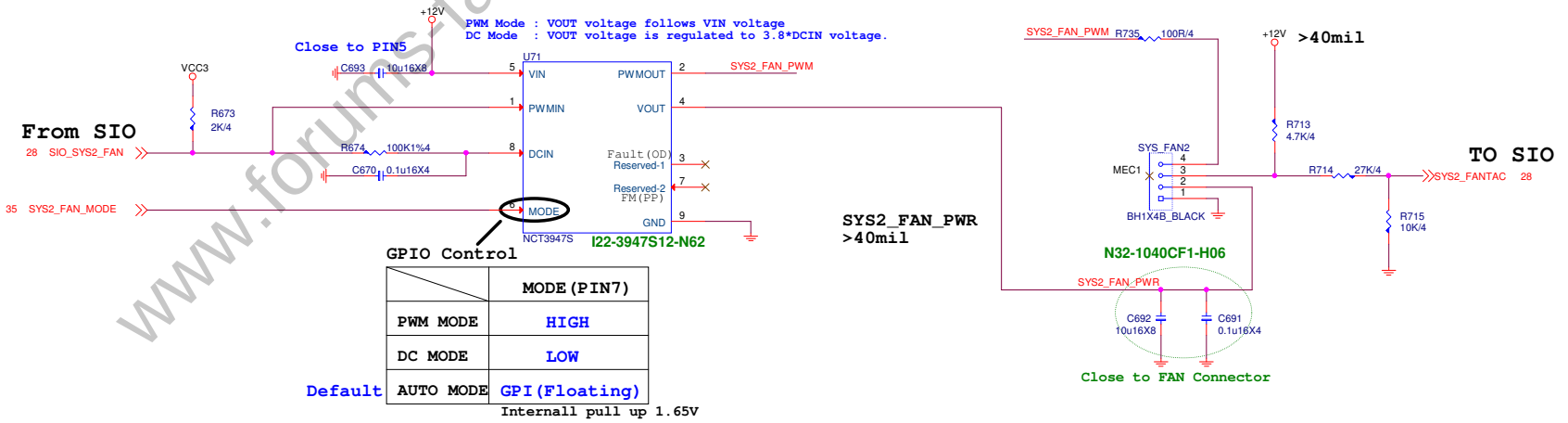
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD

MS-7B93

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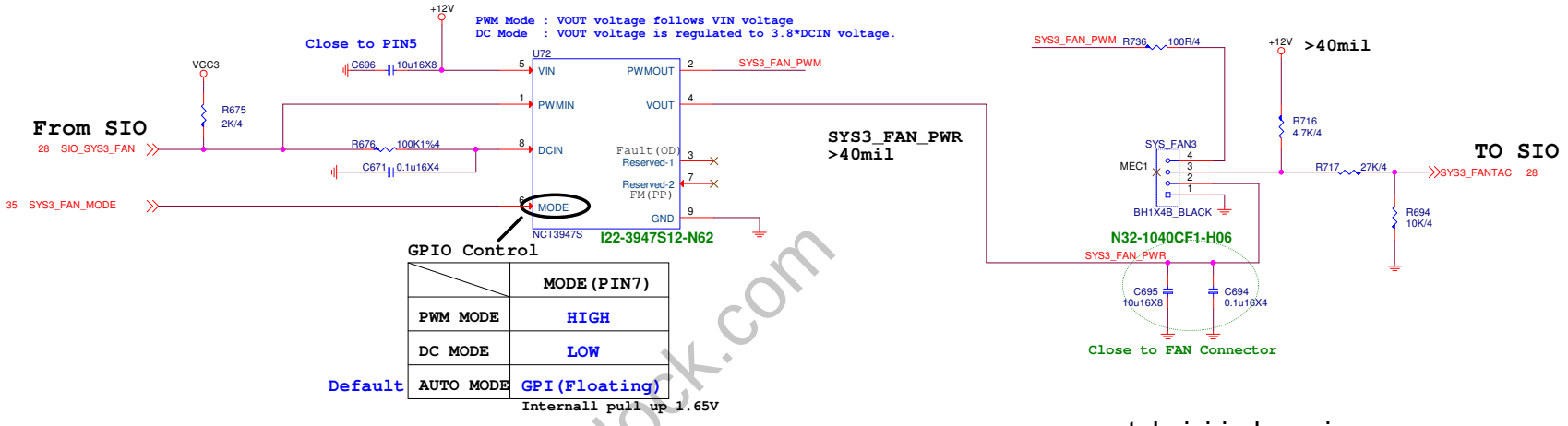
SYSFAN3 TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



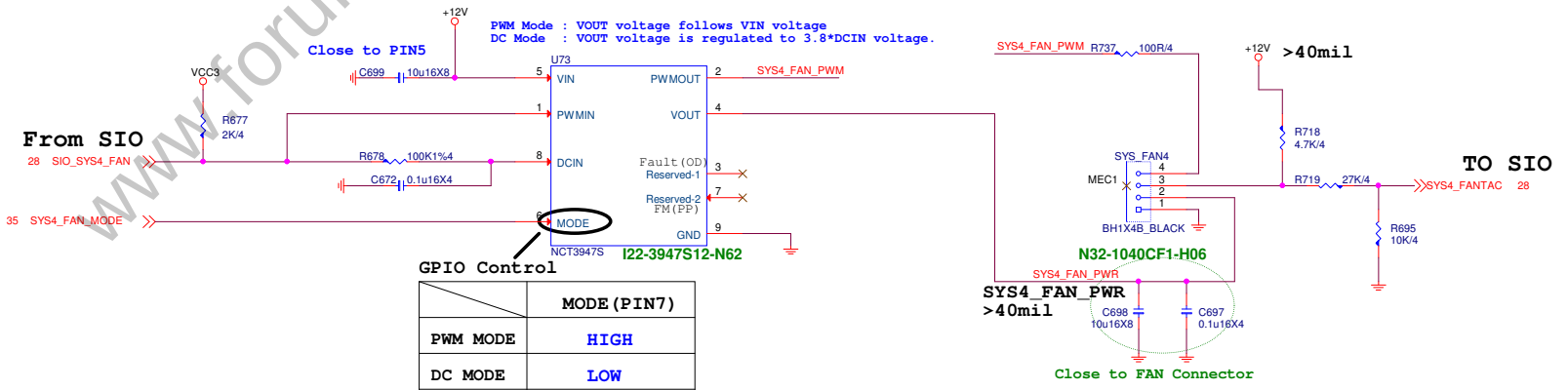
GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

SYSFAN4 TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

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Size: Custom	Document Description: FAN TYPE-K SYSFAN3/4
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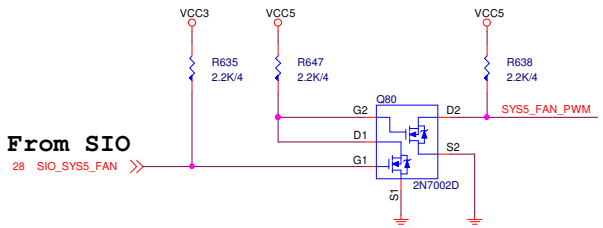
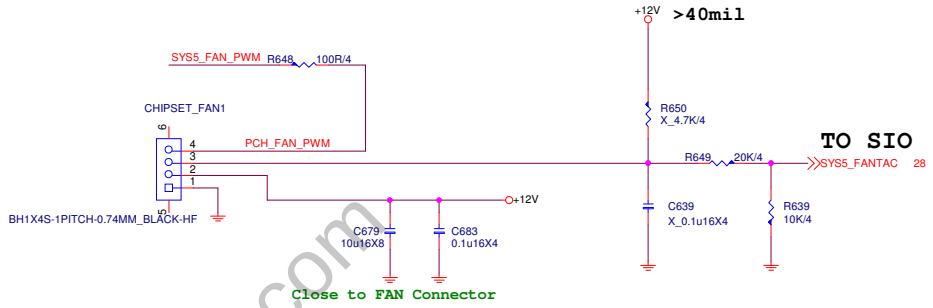
CHIPSET_FAN1





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Size: Custom	Document Description: PCH_FAN1	Rev: 11
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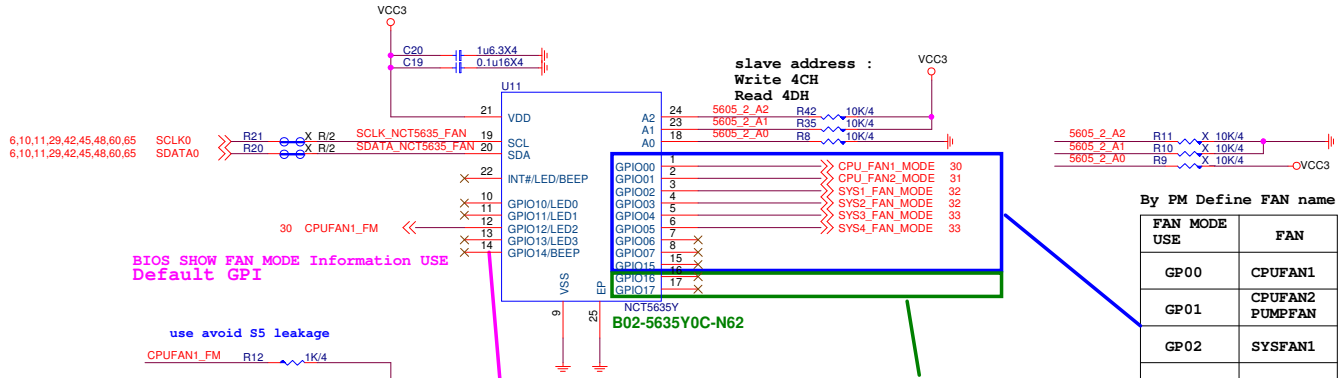

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2

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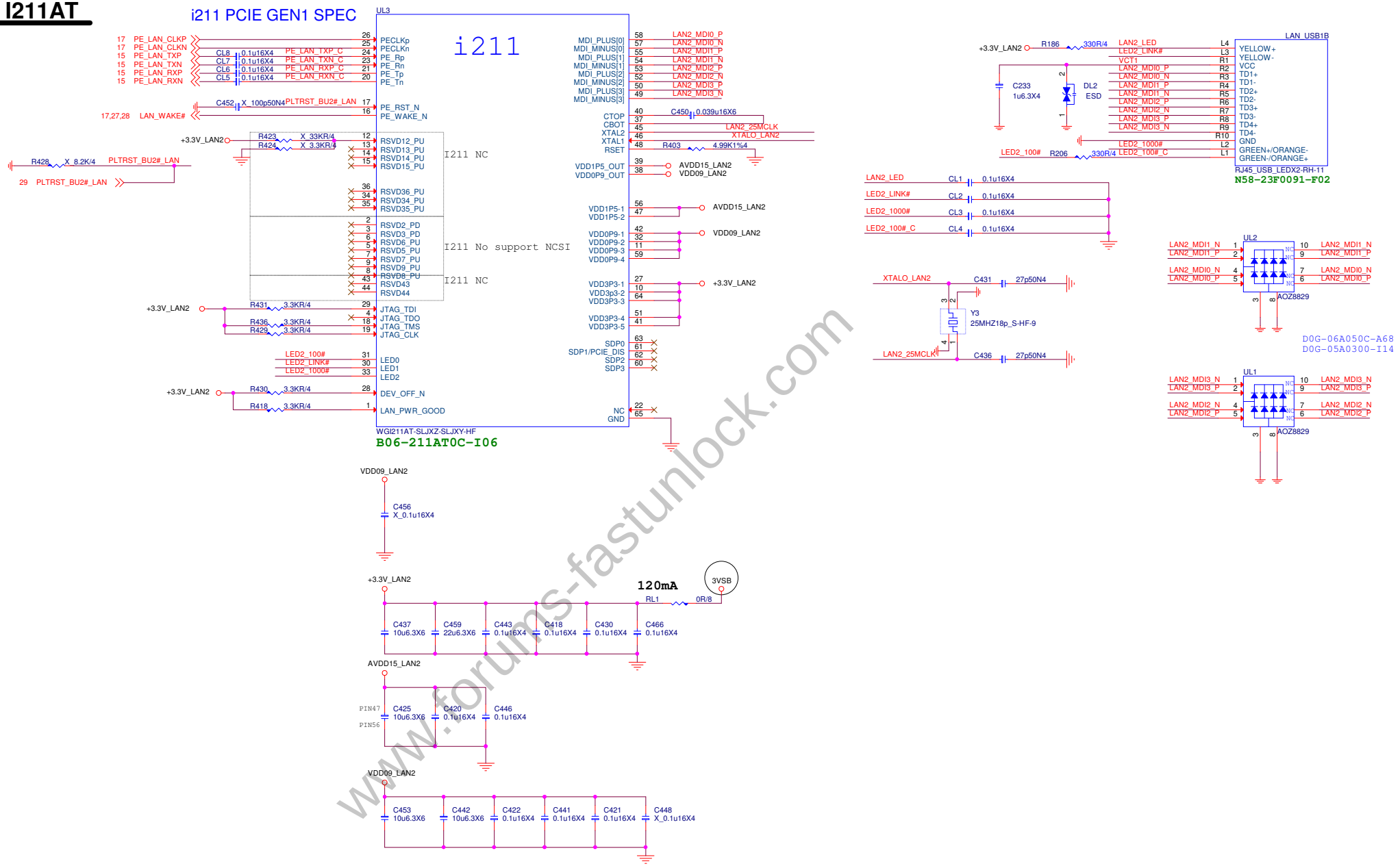
LAN-- I211AT



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Size: Custom	Document Description: LAN - I211AT	Rev: 11
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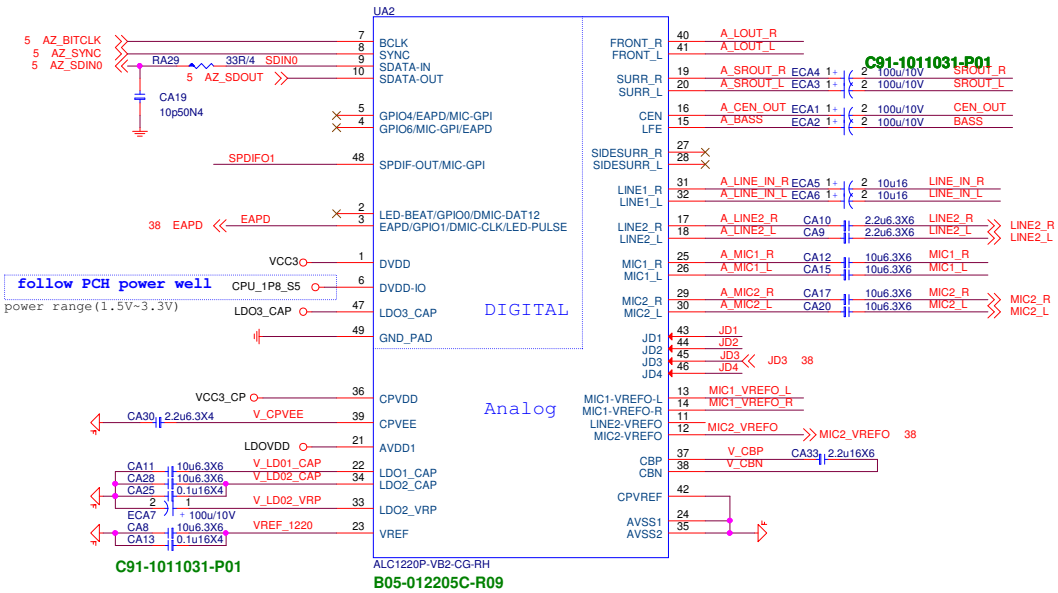
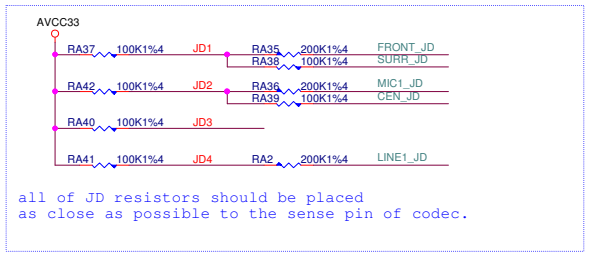
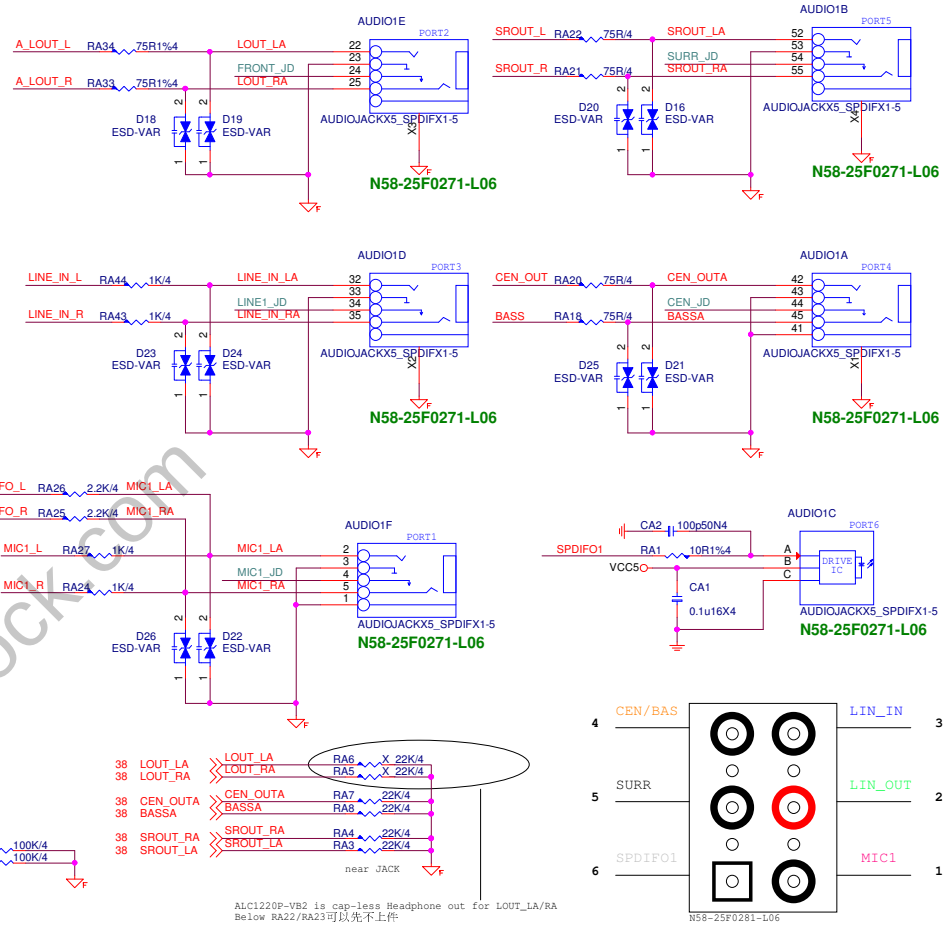
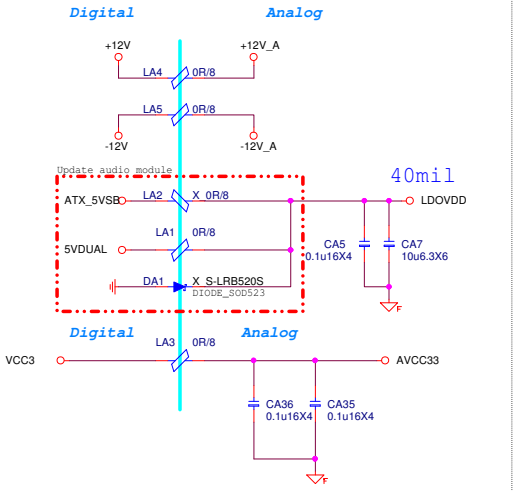
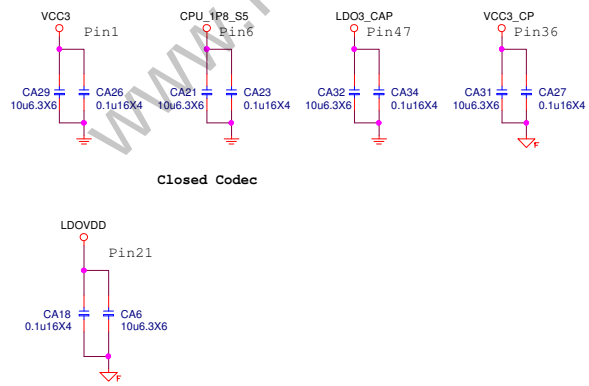
ALC1220P-VB2_48PIN

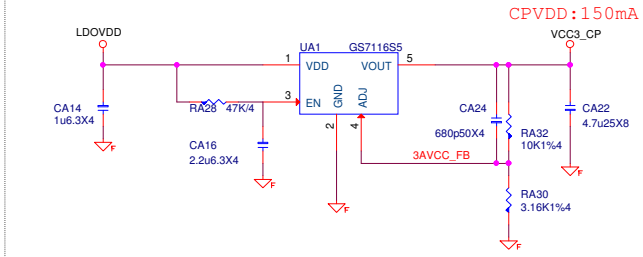


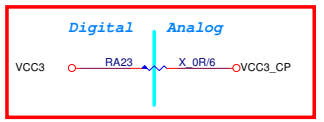




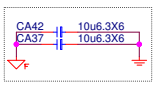








EMI



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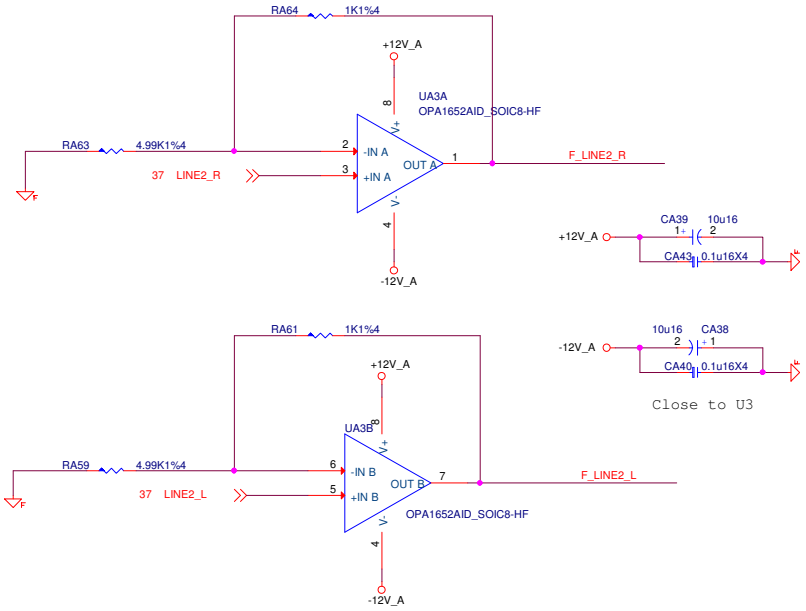
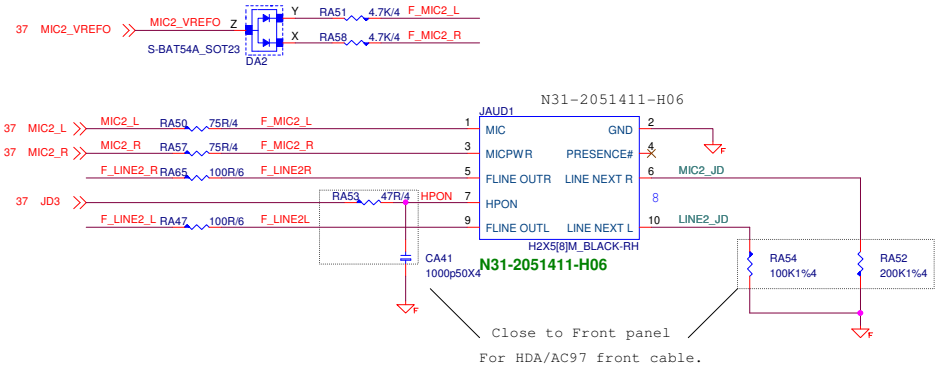
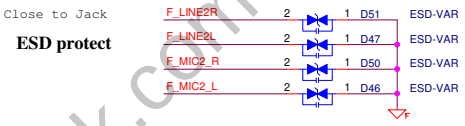
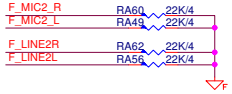


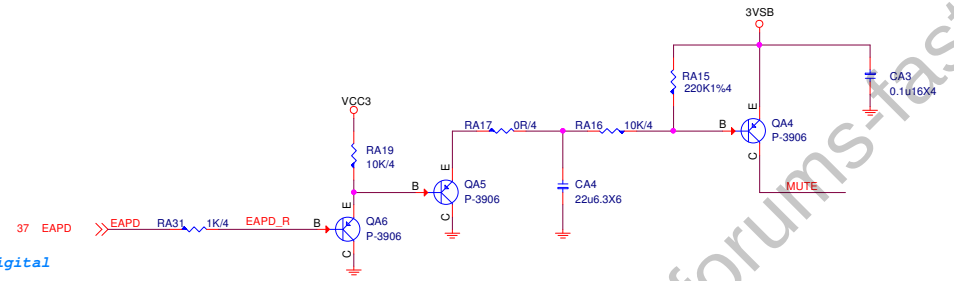




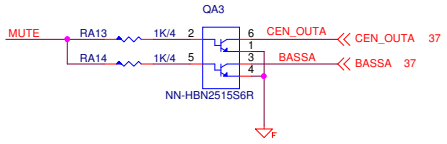


Rear Line OUT De-POP circuit

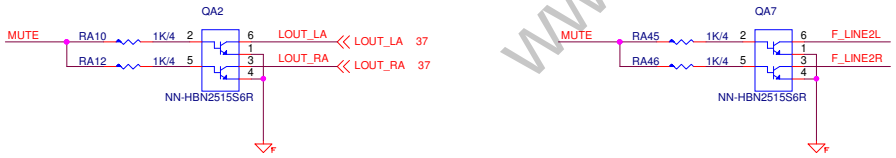
(De-pop circuit for Rear Line out & Front Headphone out)

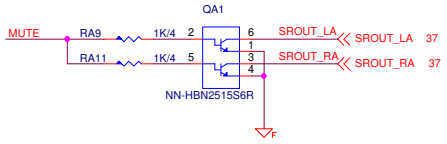


(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA,SROUT_RA, CEN_OUTA, BASSA to TVS)



Analog





Audio moat is transparent and width 40mil

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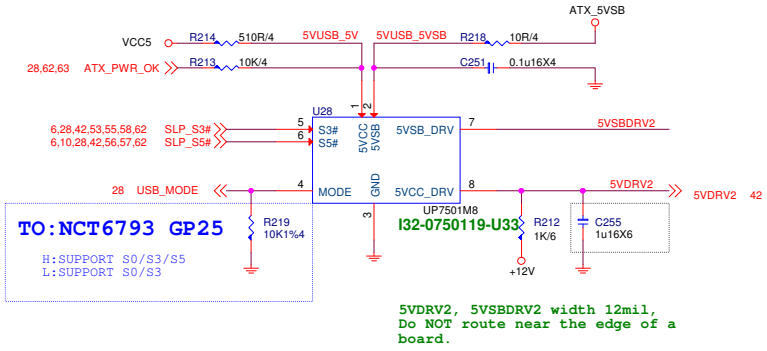
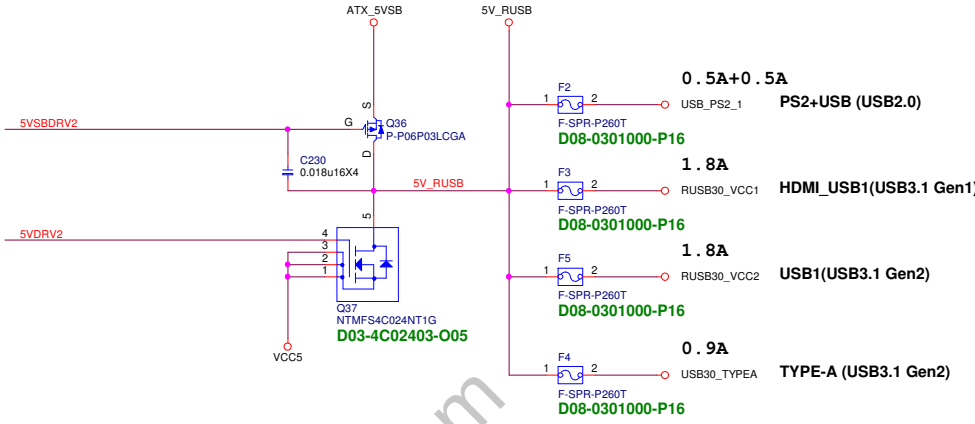
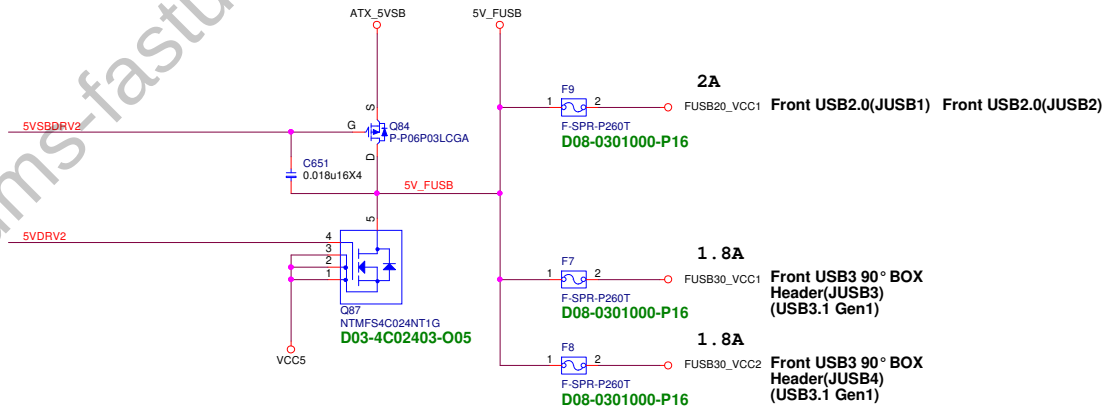
USB Power





Rear (6A)

Front (5.6A)



MSI	MICRO-STAR INT'L CO.,LTD	
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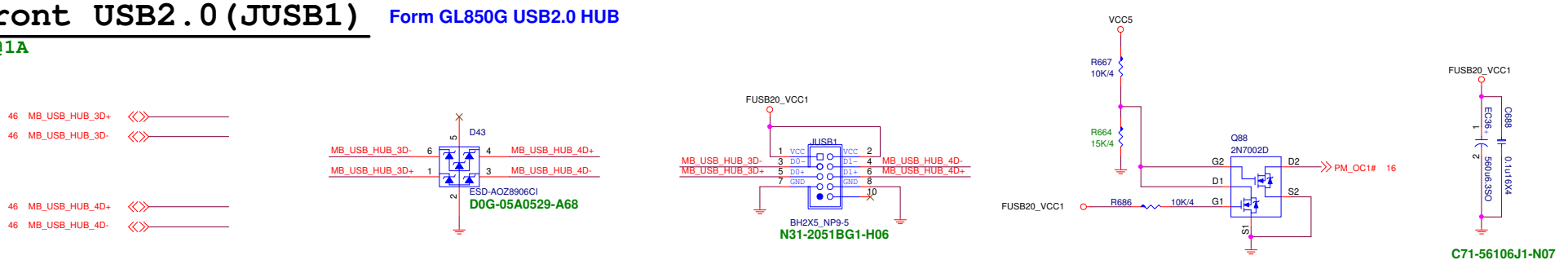
Front USB2.0(JUSB1)

Form GL850G USB2.0 HUB

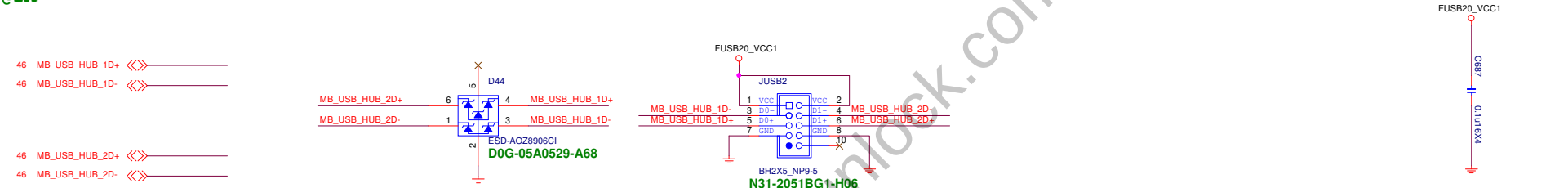
5V@1A



Front USB2.0(JUSB2)

Form GL850G USB2.0 HUB

5V@1A



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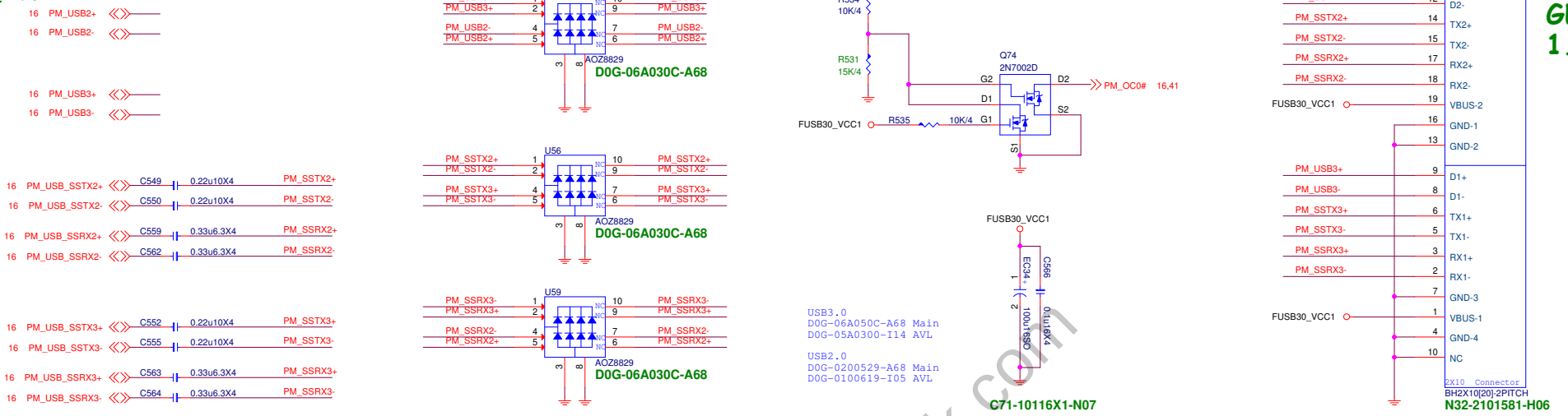
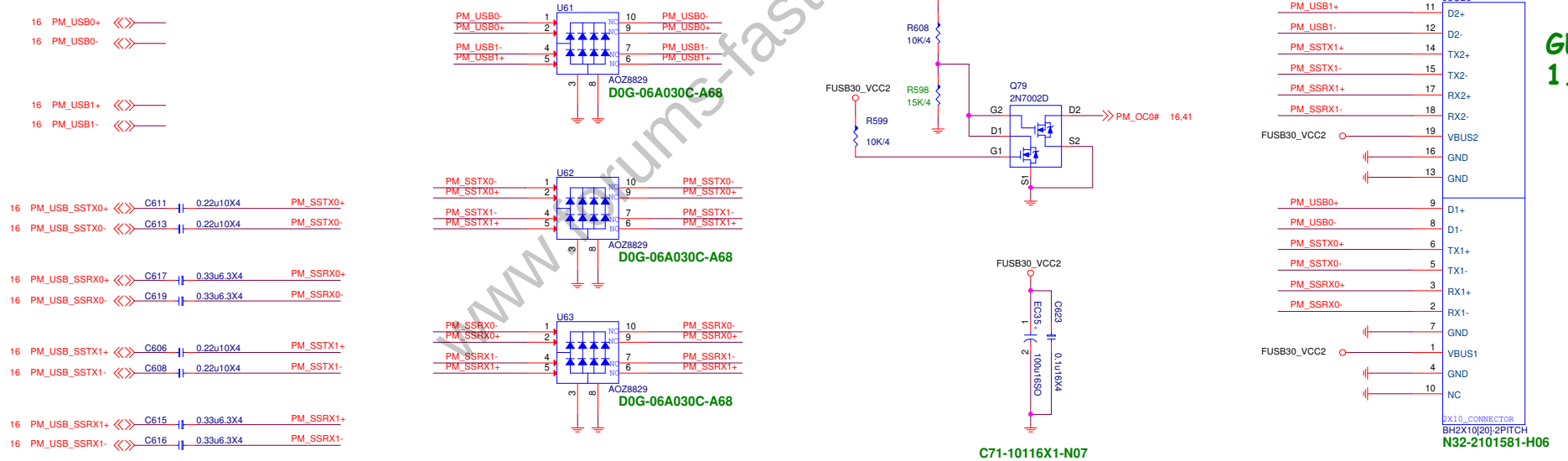
Front USB3 90° BOX Header(JUSB3)

5V@1.8A



Front USB3 90° BOX Header(JUSB4)

5V@1.8A



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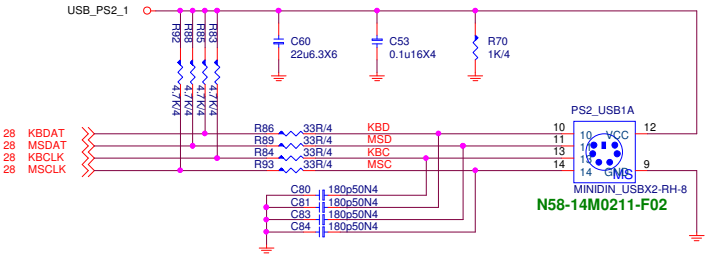
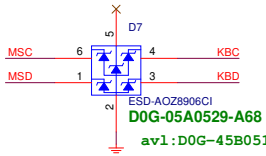
PS2+USB (USB2.0)

5V@1A

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



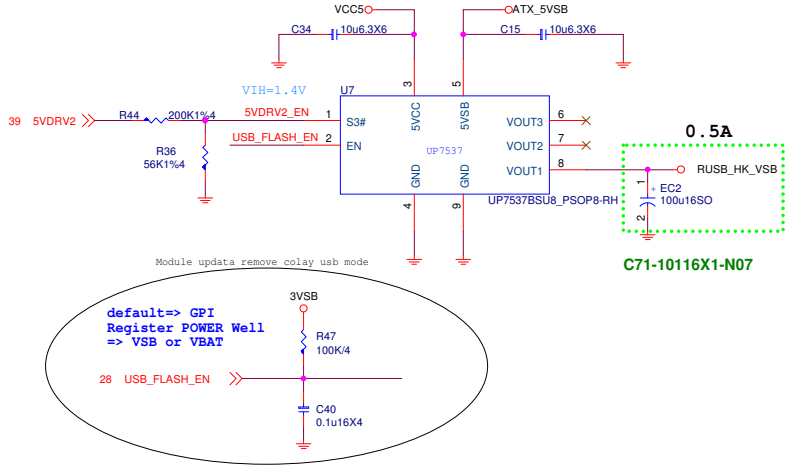
N58-14M0211-F02



D0G-05A0529-A68

avl:D0G-45B0510-I14

HOTKEY POWER

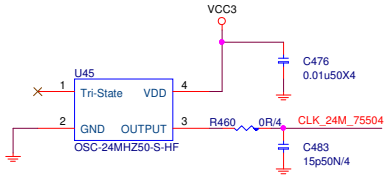


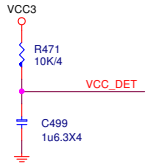
C71-10116X1-N07

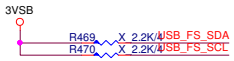
USB Flash BIOS

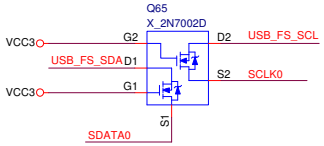
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

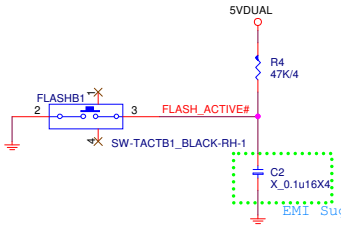
CLK running in S0,don't require in sleep





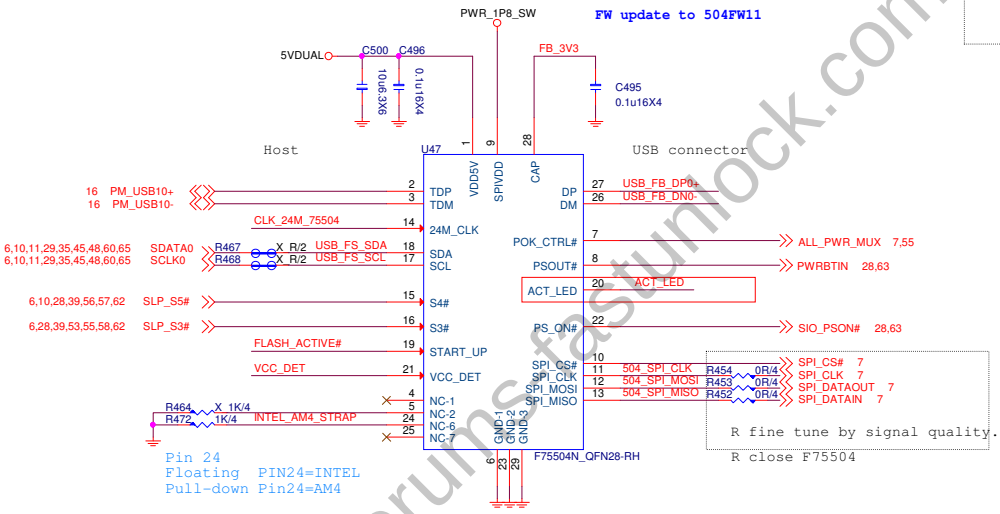


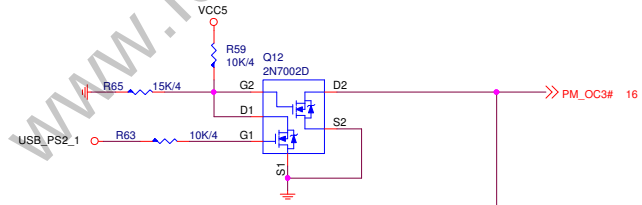


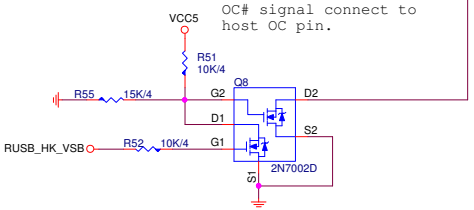


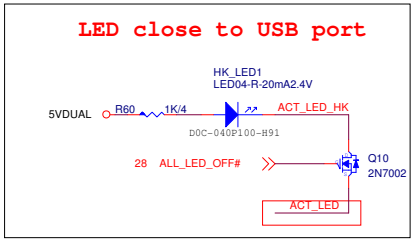
PWR_1P8_SW

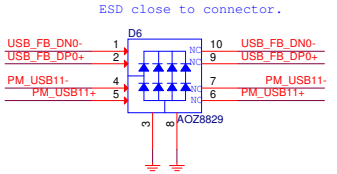
FW update to 504FW11

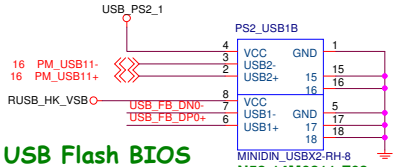








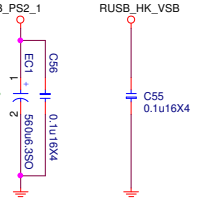




USB Flash BIOS

N58-14M0211-F02

1A



C71-56106J1-N07

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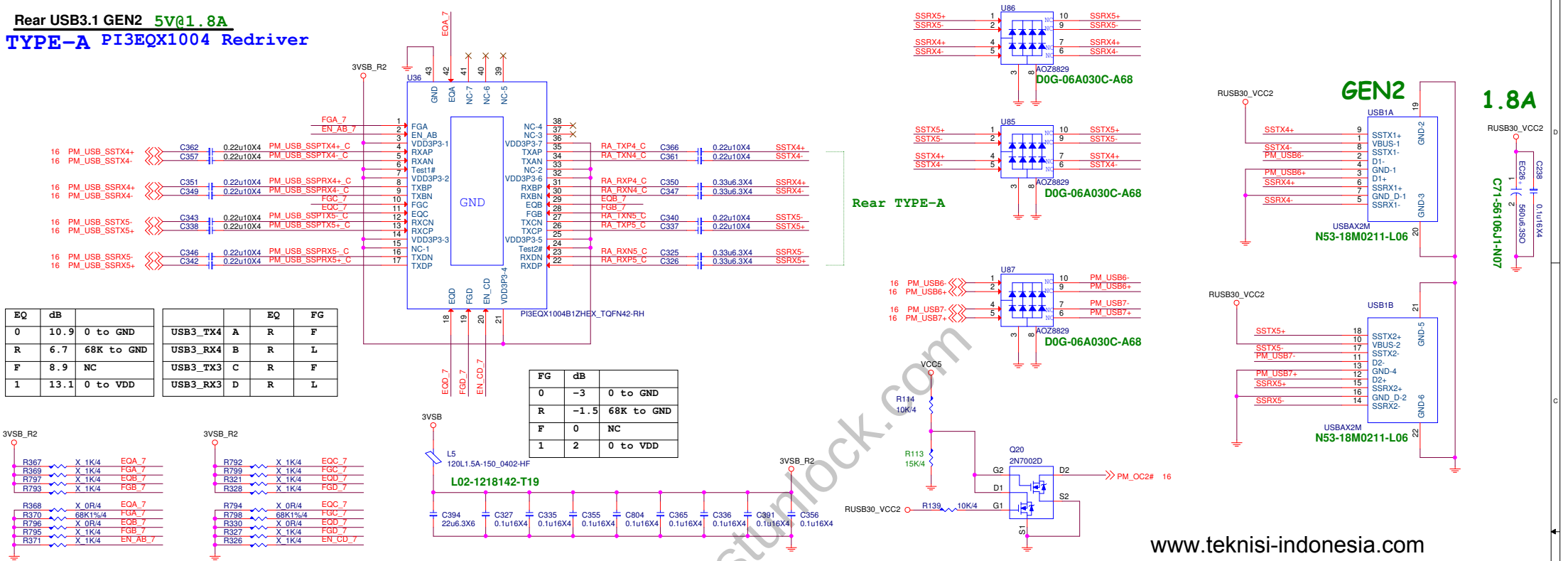
Rear USB3.1 GEN2 5V@1.8A

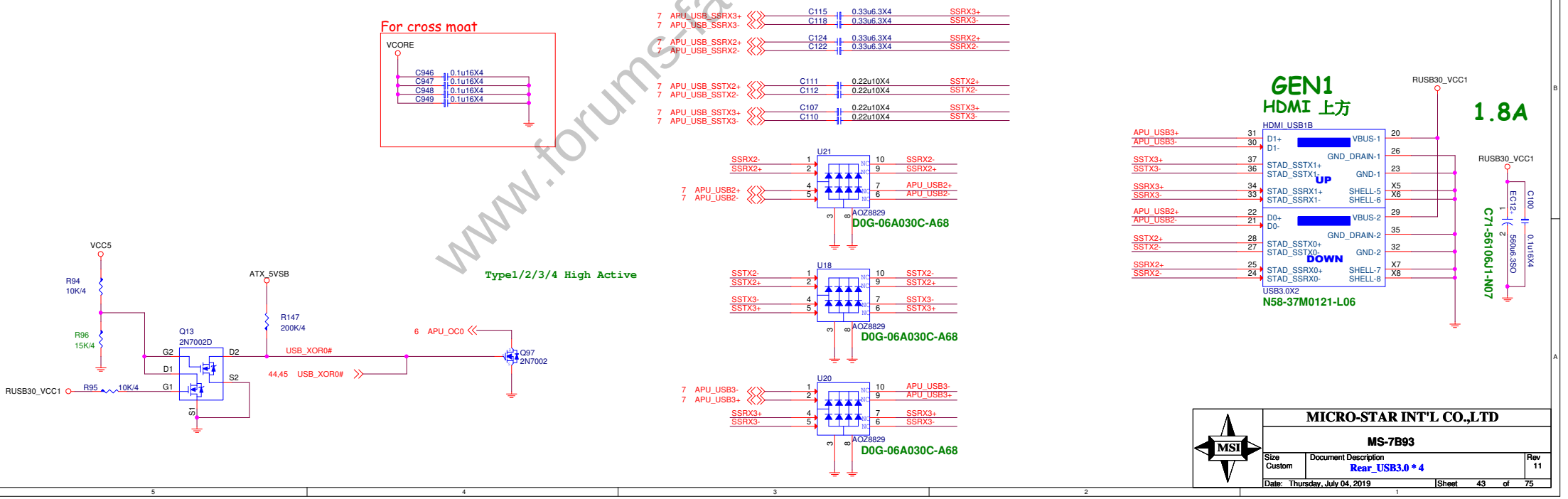
TYPE-A PI3EQX1004 Redriver



EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD



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Size: Custom	Document Description: Rear_USB3.0 * 4	Rev: 11
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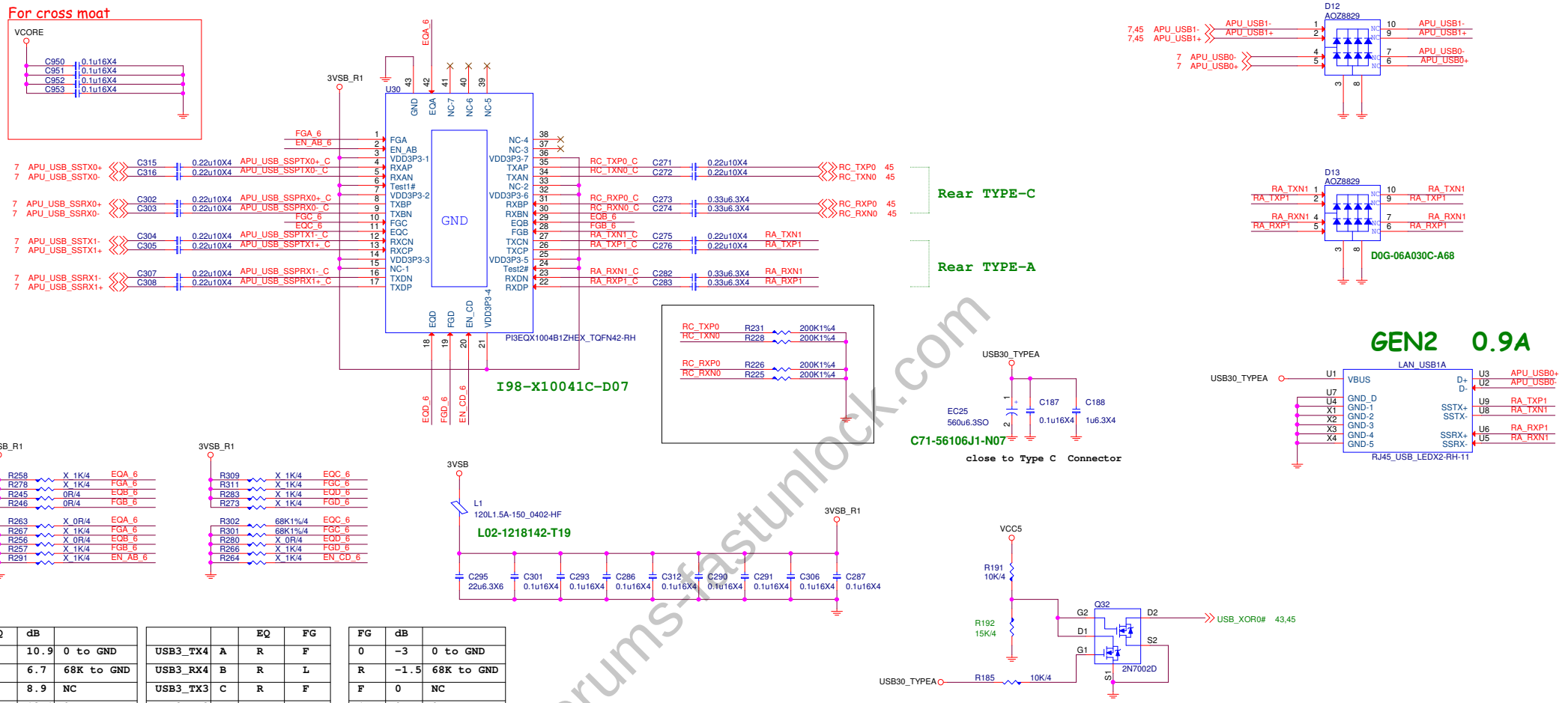
TYPE-A PI3EQX1004 Redriver



EQ	dB	
0	10.9	0 to GND
R	6.7	68K to GND
F	8.9	NC
1	13.1	0 to VDD

		EQ	FG
USB3_TX4	A	R	F
USB3_RX4	B	R	L
USB3_TX3	C	R	F
USB3_RX3	D	R	L

FG	dB	
0	-3	0 to GND
R	-1.5	68K to GND
F	0	NC
1	2	0 to VDD

MICRO-STAR INT'L CO.,LTD

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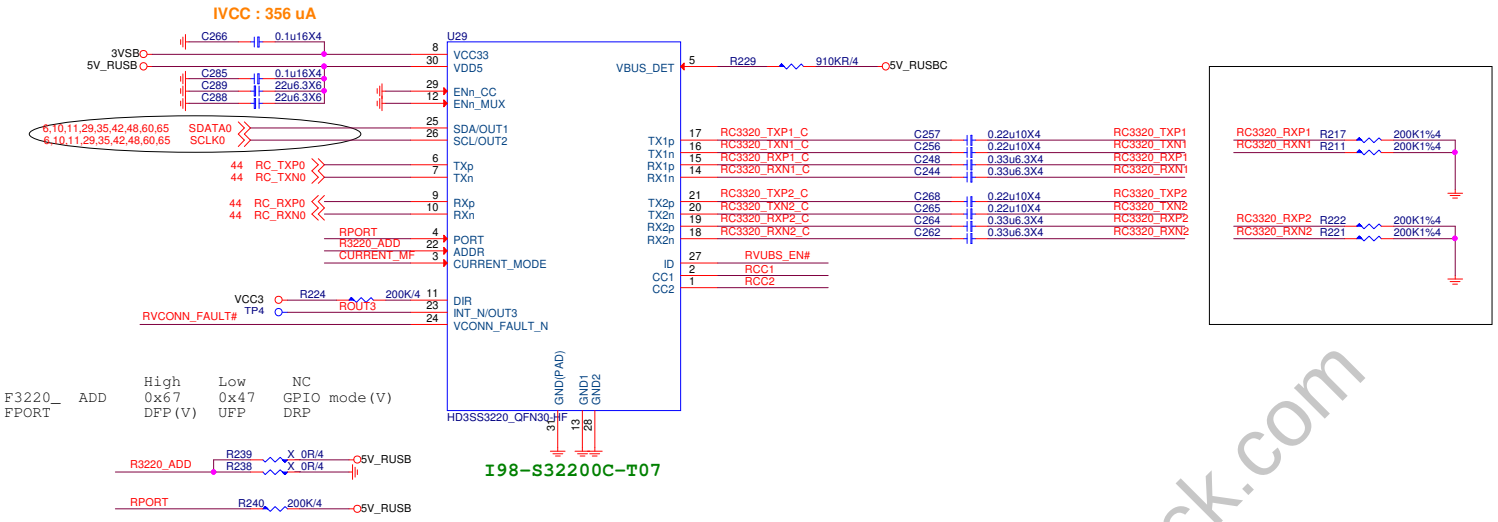
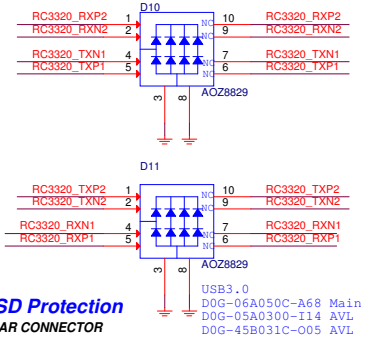
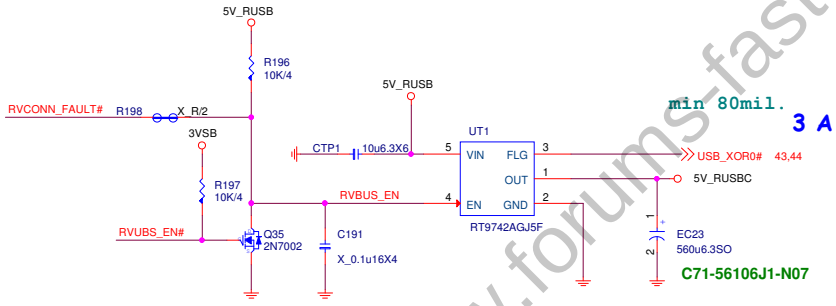
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

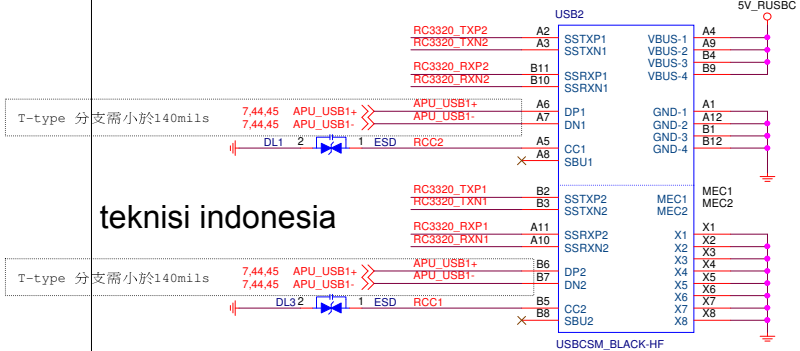




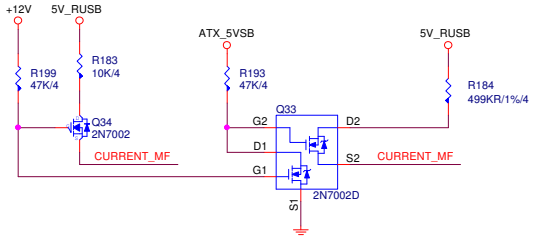
VBUS EN



GEN2 3A



Current Mode



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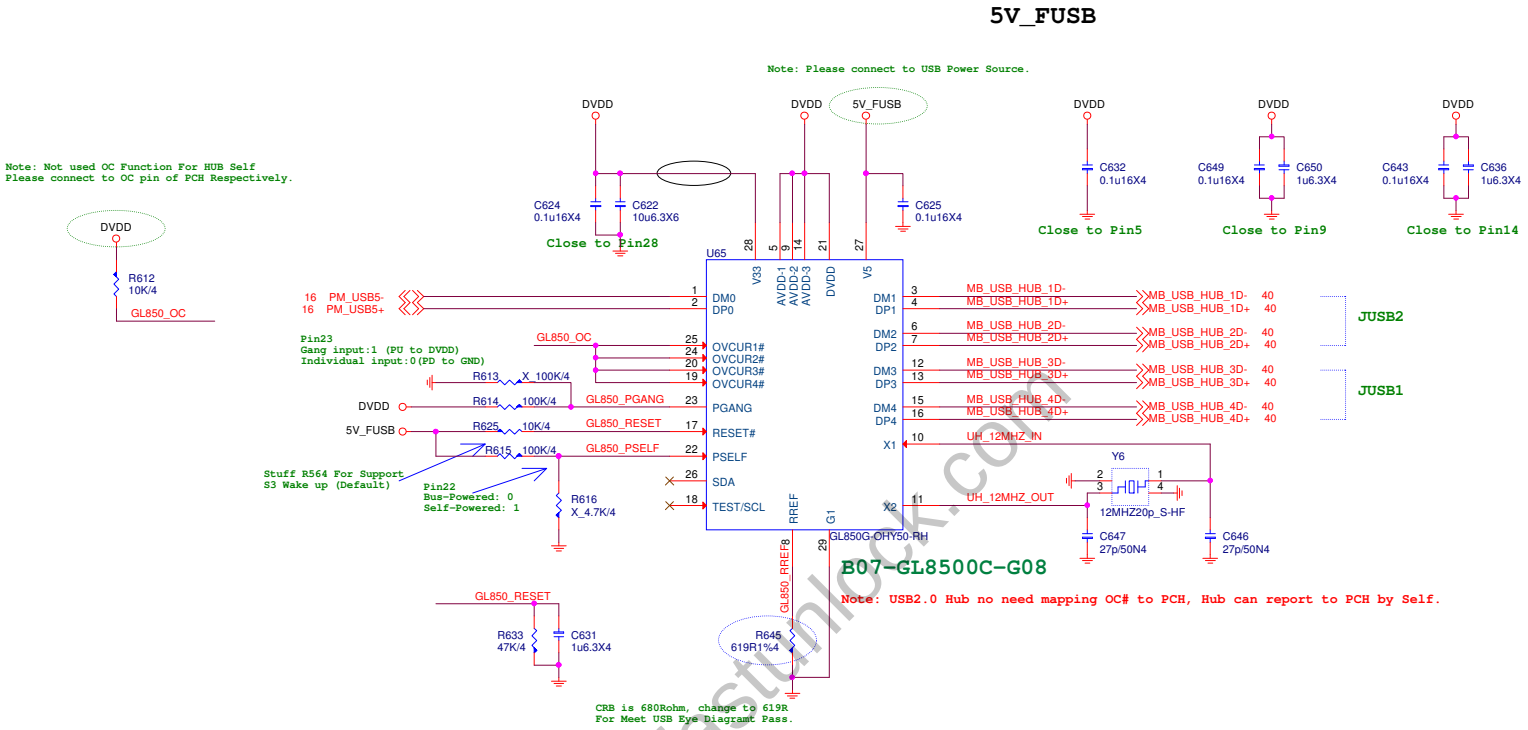
GL850G USB2.0 HUB



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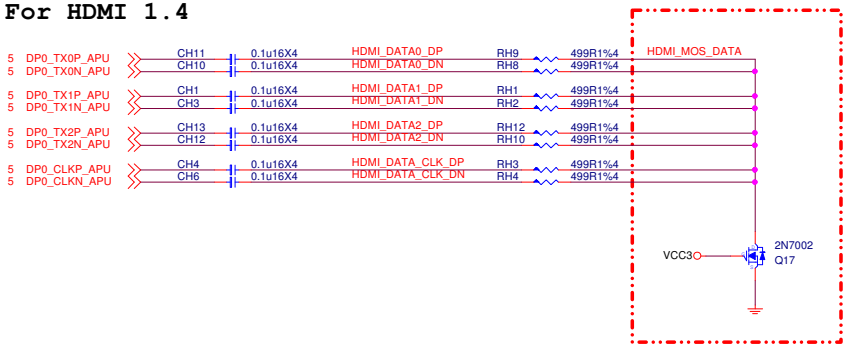
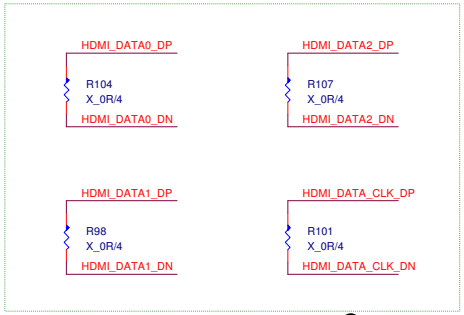
HDMI CONNECTOR

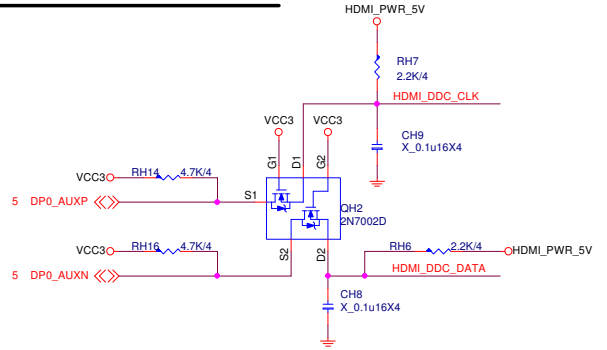
For HDMI 1.4



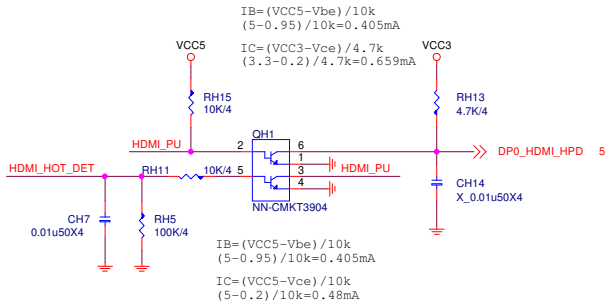
HDMI_MOS_DATA trace length <500mil
other platform please check design guide



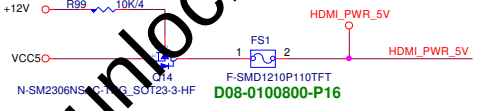
AUX Level Shifter



HPD Circuit

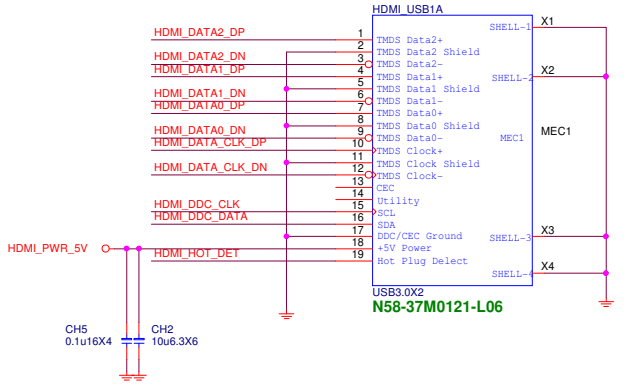


Connector Power

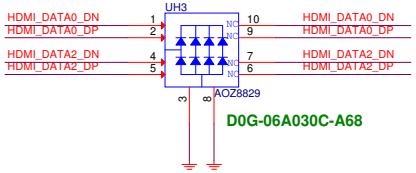


如果用DIODE SA測試電壓會不過

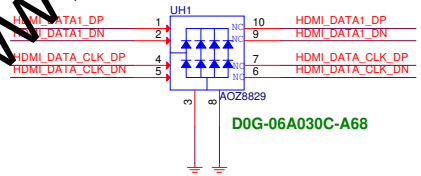
Connector



For EMI

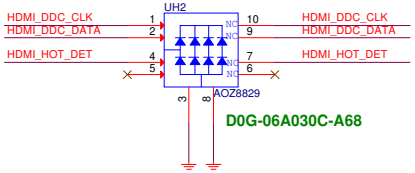


D0G-06A030C-A68



D0G-06A030C-A68

注意:耐壓5V零件



D0G-06A030C-A68

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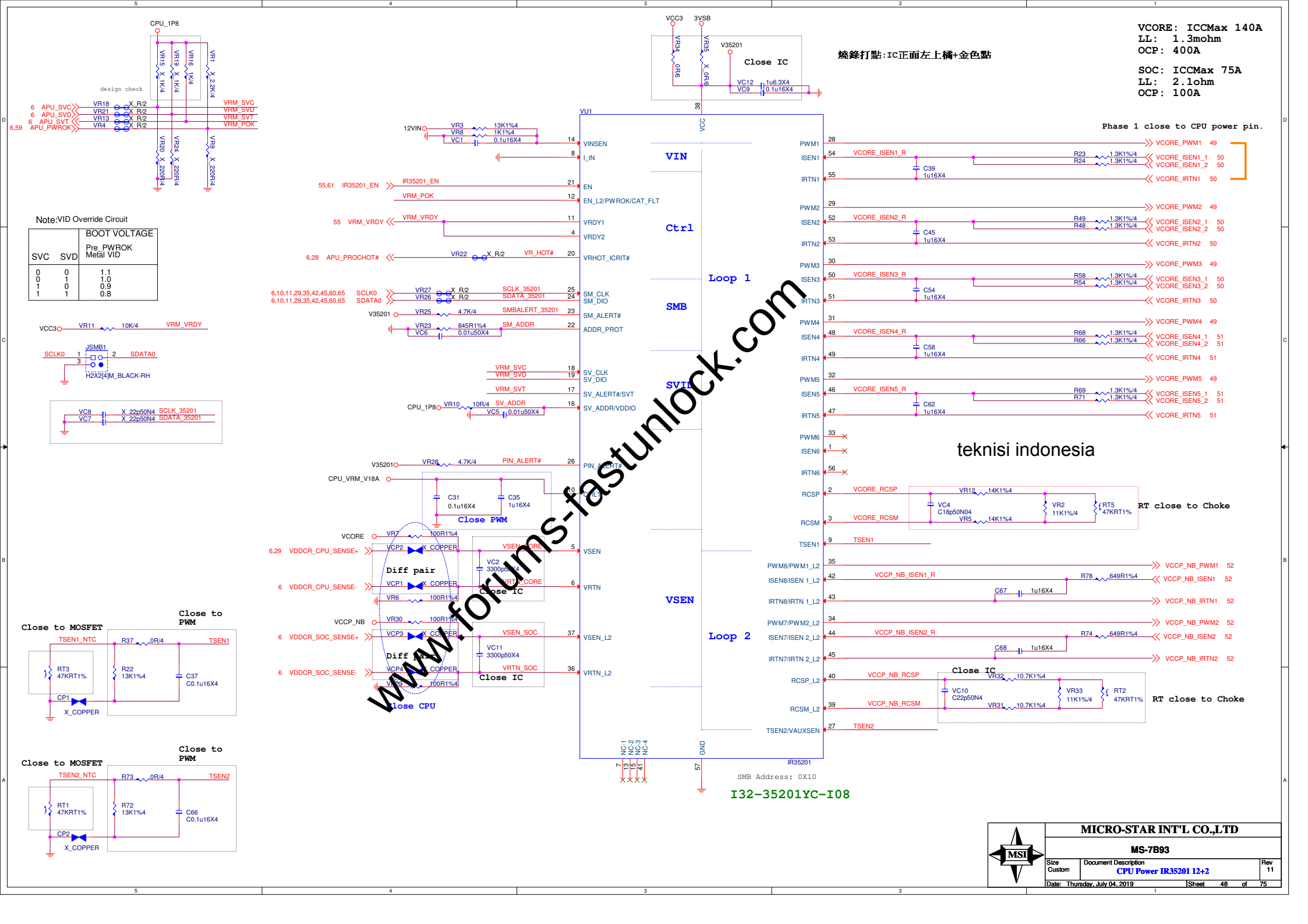
VCORE: ICCMax 140A
LL: 1.3mohm
OCP: 400A
SOC: ICCMax 75A
LL: 2.1ohm
OCP: 100A
燒錄打點:IC正面左上橘+金色點
Phase 1 close to CPU power pin.
Note:VID Override Circuit
BOOT VOLTAGE
Pre_PWROK Metal VID
SVC SVD
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
VU1
VIN
Ctrl
Loop 1
SMB
SVID
VSEN
Loop 2
VINSEN
I_IN
EN
EN_L2/PWROK/CAT_FLT
VRDY1
VRDY2
VRHOT_ICRIT#
SM_CLK
SM_DIO
SM_ALERT#
ADDR_PROT
SV_CLK
SV_DIO
SV_ALERT#/SVT
SV_ADDR/VDDIO
PIN_ALERT#
VSEN
VRTN
VSEN_L2
VRTN_L2
TSEN1
TSEN2/VAUXSEN
PWM1
ISEN1
IRTN1
PWM2
ISEN2
IRTN2
PWM3
ISEN3
IRTN3
PWM4
ISEN4
IRTN4
PWM5
ISEN5
IRTN5
PWM6
ISEN6
IRTN6
RCSP
RCSM
PWM8/PWM1_L2
ISEN8/ISEN 1_L2
IRTN8/IRTN 1_L2
PWM7/PWM2_L2
ISEN7/ISEN 2_L2
IRTN7/IRTN 2_L2
RCSP_L2
RCSM_L2
IR35201
SMB Address: 0X10
I32-35201YC-I08
Close IC
Close PWM
Diff pair
Close to PWM
Close to MOSFET
RT close to Choke
teknisi indonesia
www.forums-fastunlock.com
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MS-7B93
CPU Power IR35201 12+2
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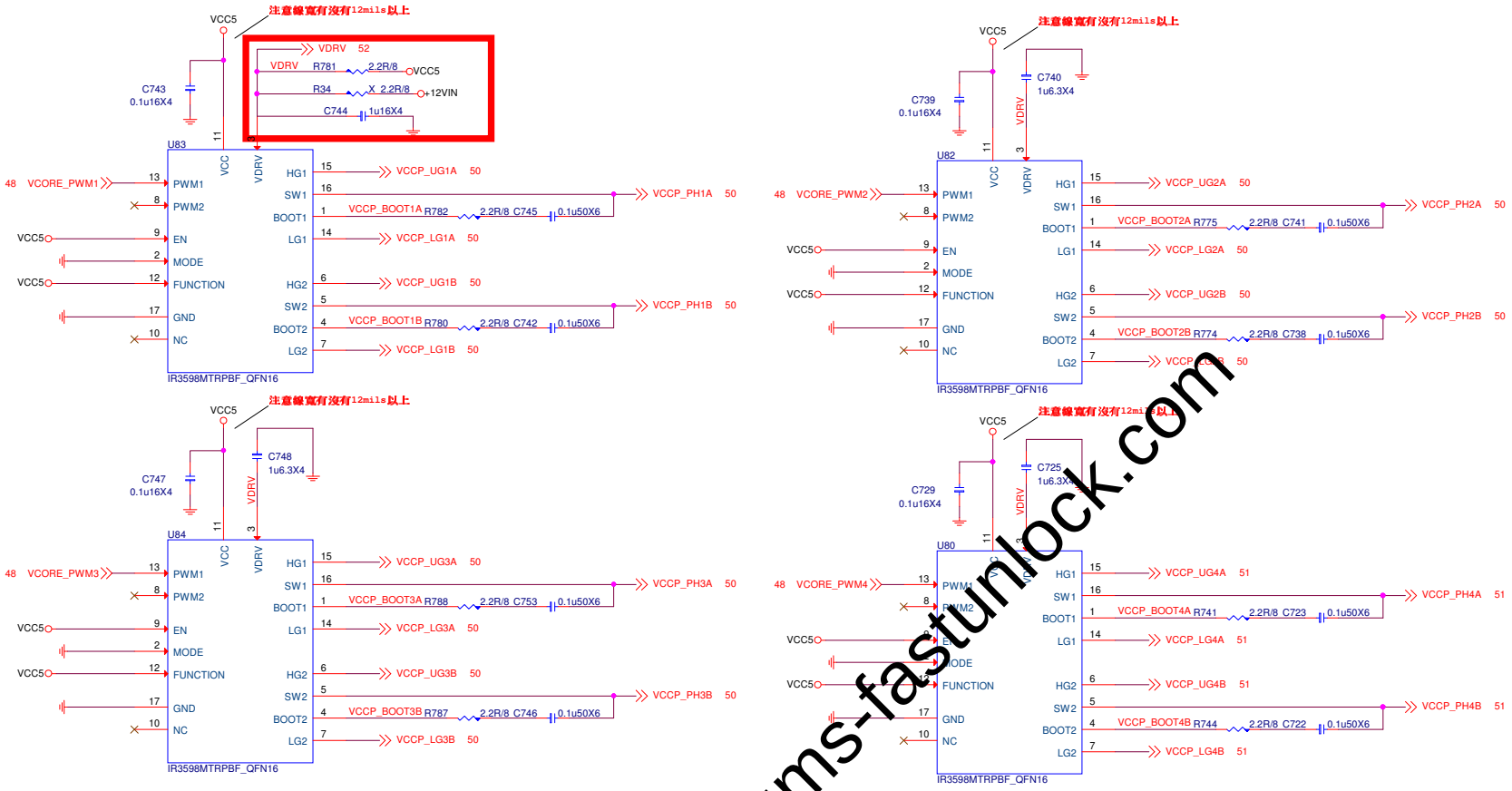
CPU_CORE Driver IC　　VCORE Double 10-PHASE



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Size: Custom	Document Description: CPU Power Driver IC IR3598
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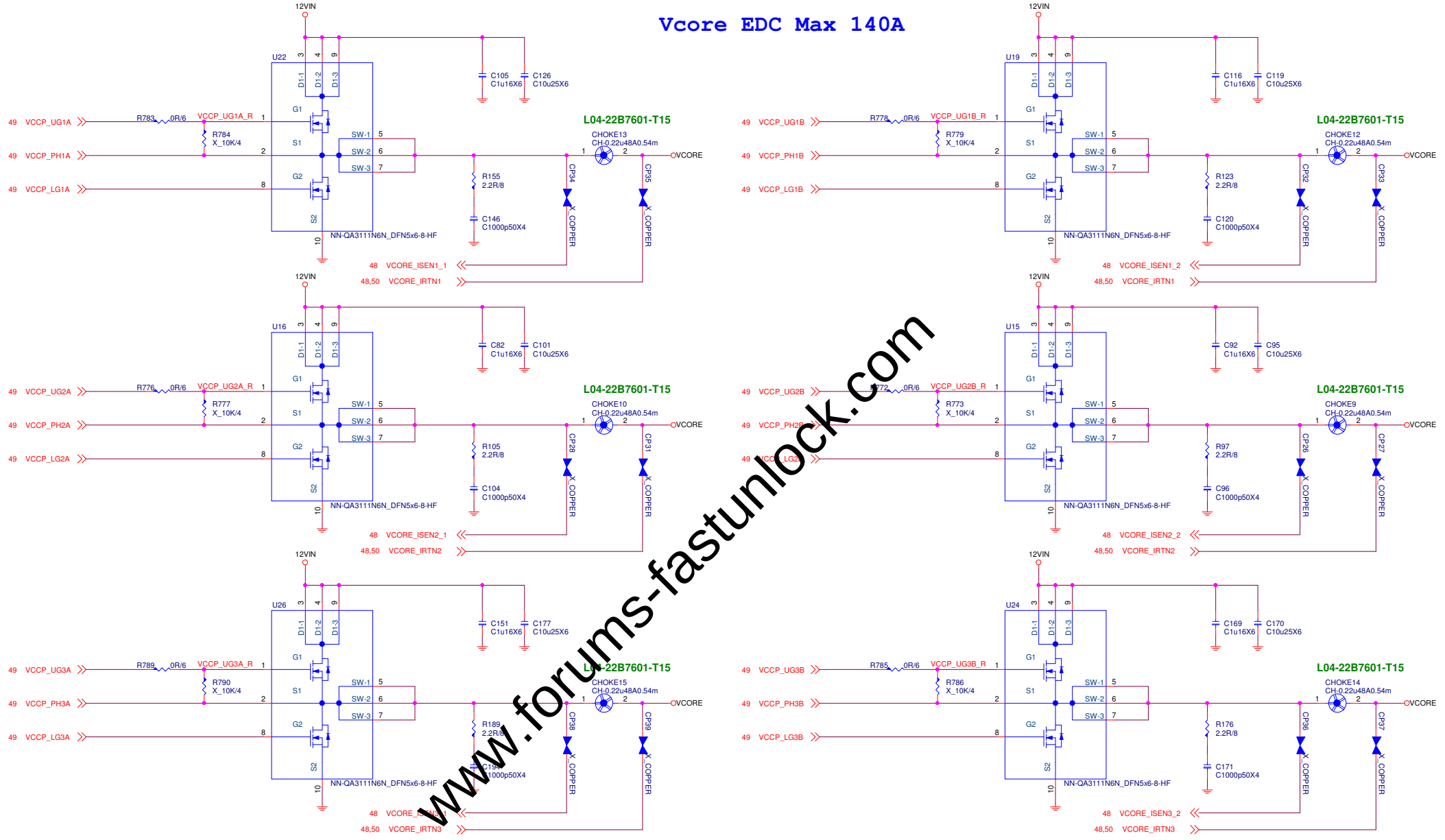
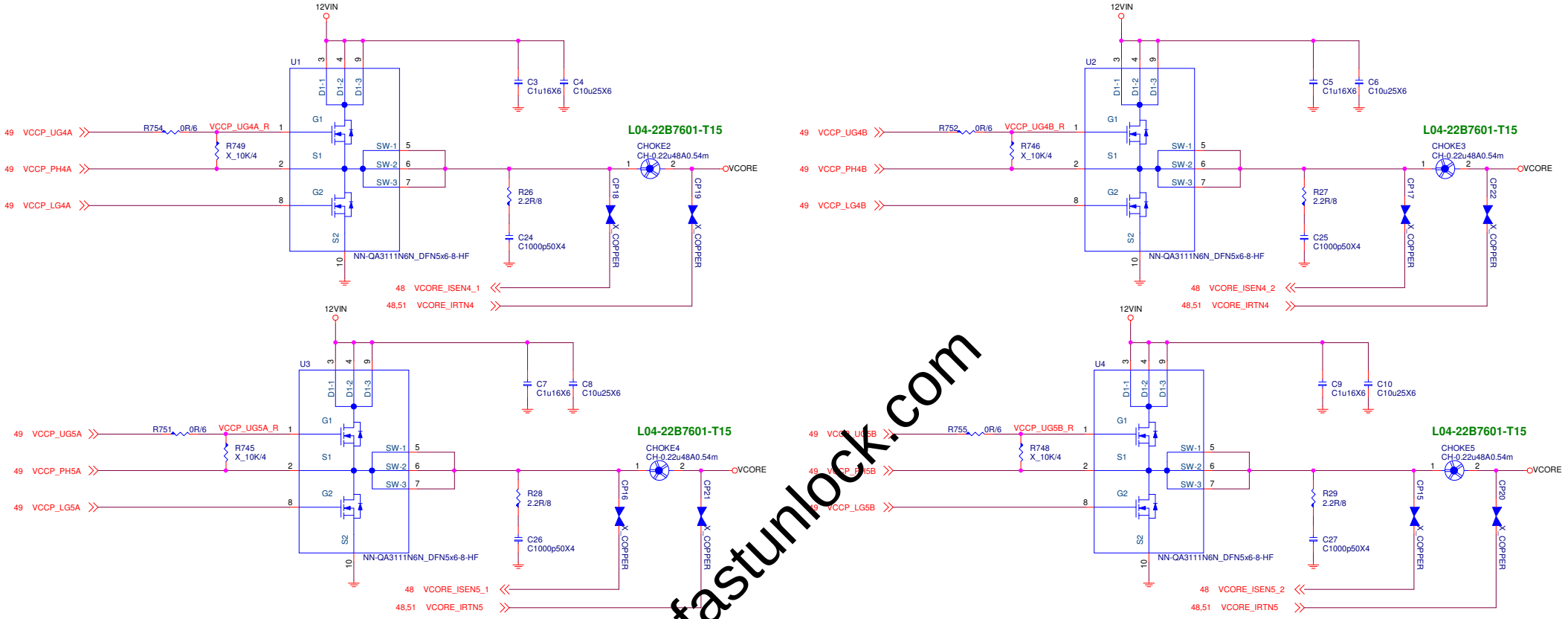
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD	
MS-7B93	
Size: Custom	Document Description: CPU Power Vocre Phase 1-6
Rev: 11	
Date: Thursday, July 04, 2019	Sheet 50 of 75



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: CPU Power Vocre Phase 7 - 10
Rev: 11	
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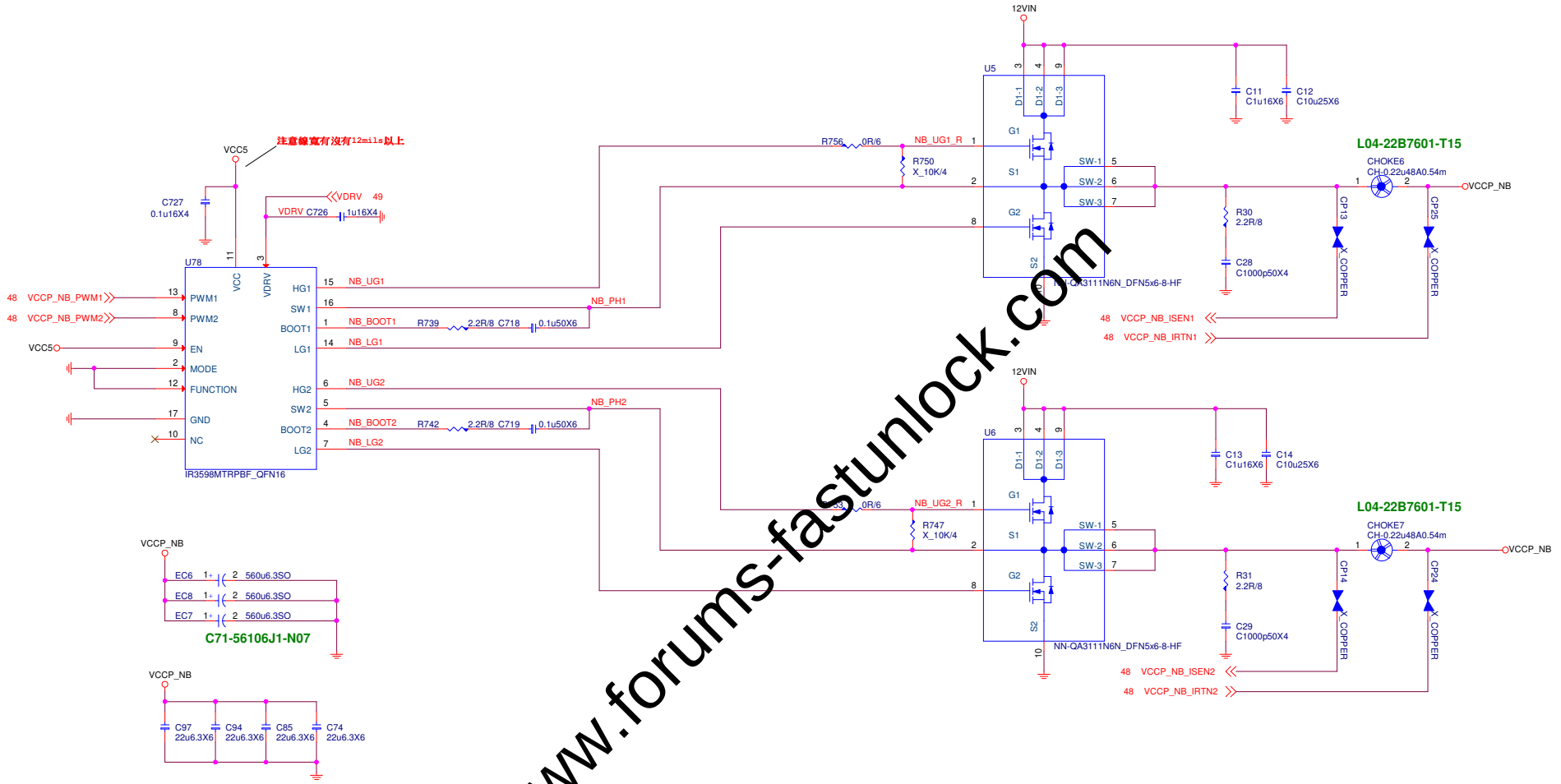
SOC EDC Max 75A



MICRO-STAR INT'L CO.,LTD		
MS-7B93		
Size: Custom	Document Description: CPU Power NB Phase 1-2	Rev: 11
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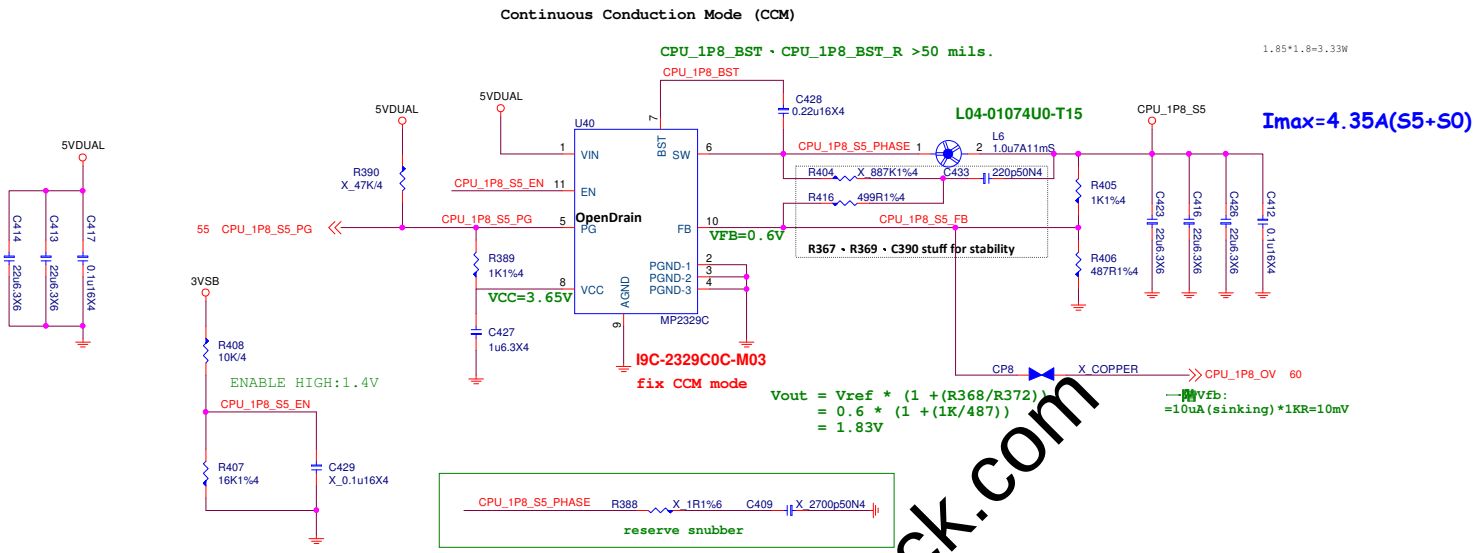
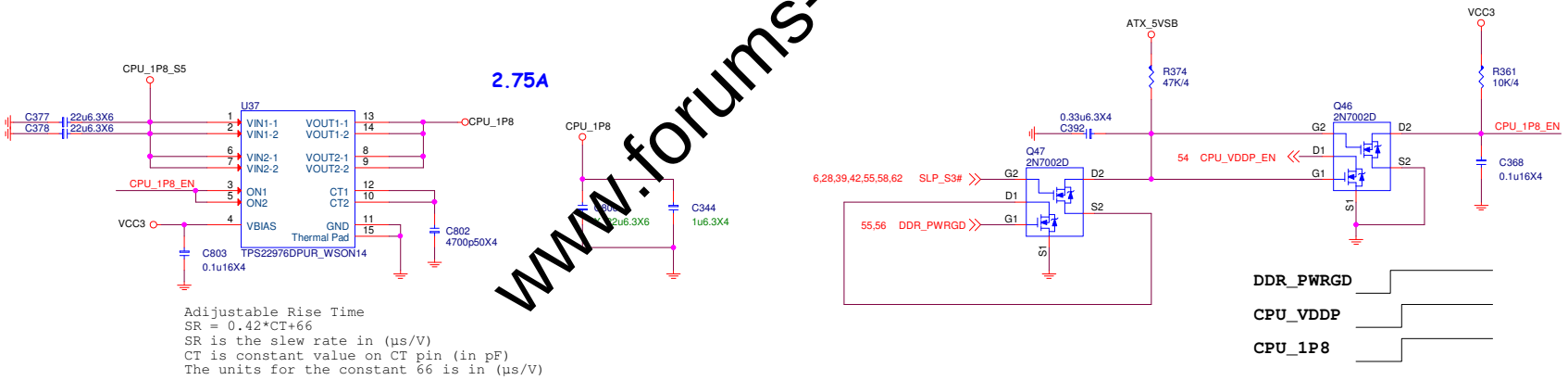
CPU 1.8V S5

CPU 1.8V_S5@0.5A
CHIP_1.8V_S5@0.1A
CPU_VDDP_S5@1A
AUDIO1.8V@0.25A



CPU 1.8V S0

CPU 1.8V_S0@2A
CHIP_1.8V@0.5A



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU Power 1.8_S0 / S5	11

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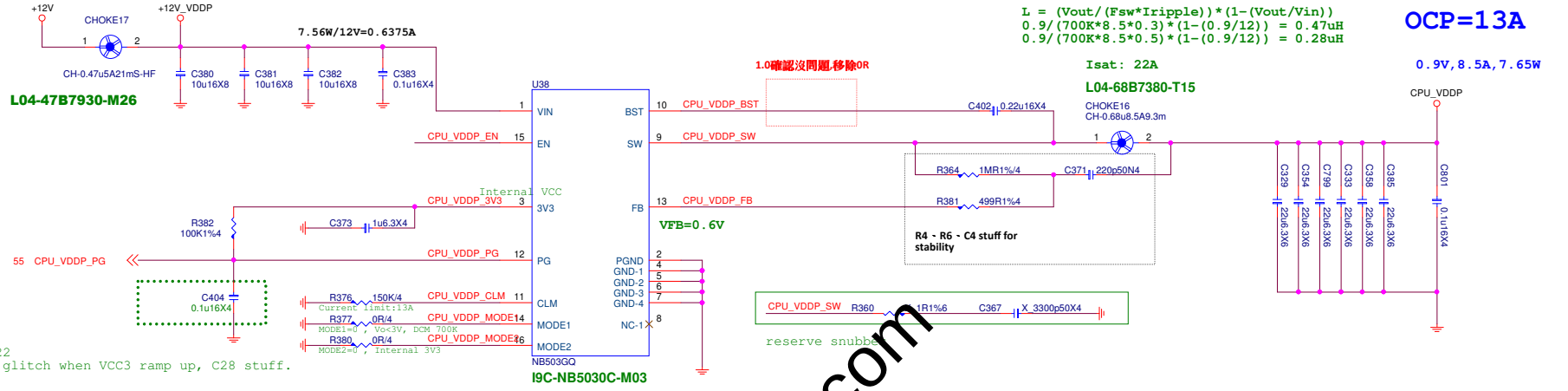
CPU_VDDP_S0

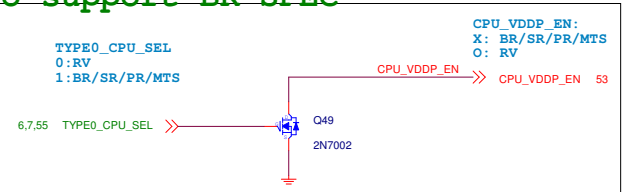
0.9V@S0:8.5A

S0:8.5A
S5:1A

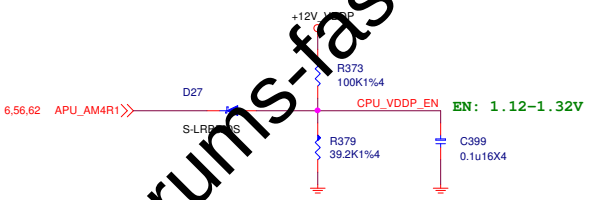
```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```

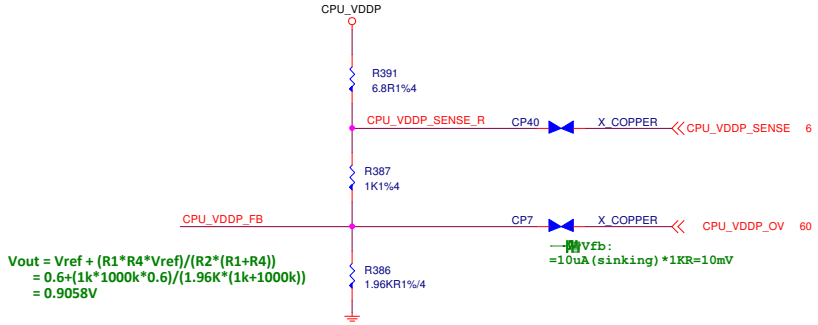


No support BR SPEC



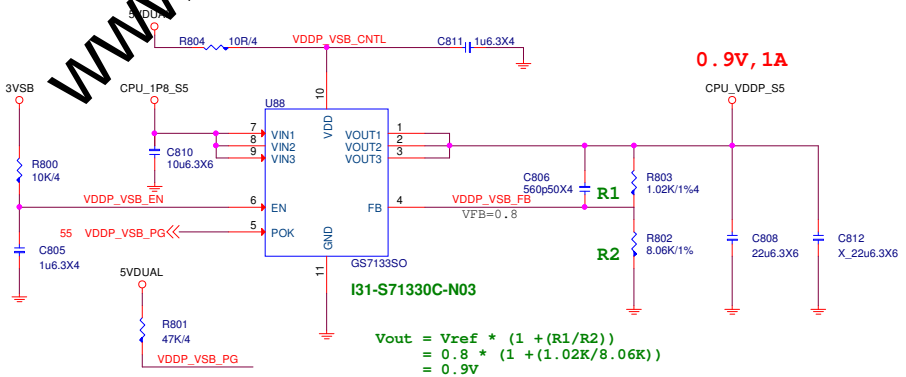
CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	SPEC no Support
NA	X	0	0	0
SR	2	1	CPU VDDP NOT SUPPORT TYPE2	2
RV/ZP	3	0	1	1
MTS	4	1	CPU VDDP NOT SUPPORT TYPE4	





CPU_VDDP_S5

0.9V
S5:1A



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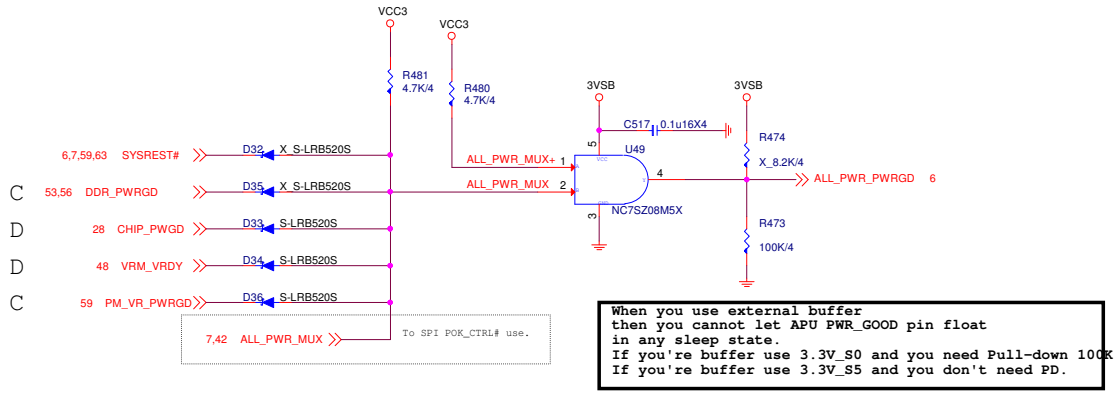
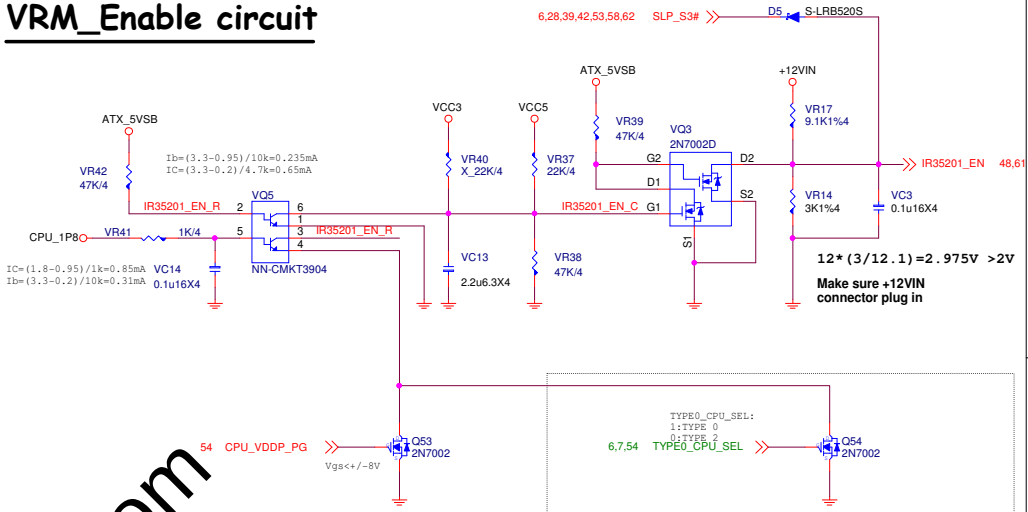
ALL POWER GOOD MUX

S0 PG



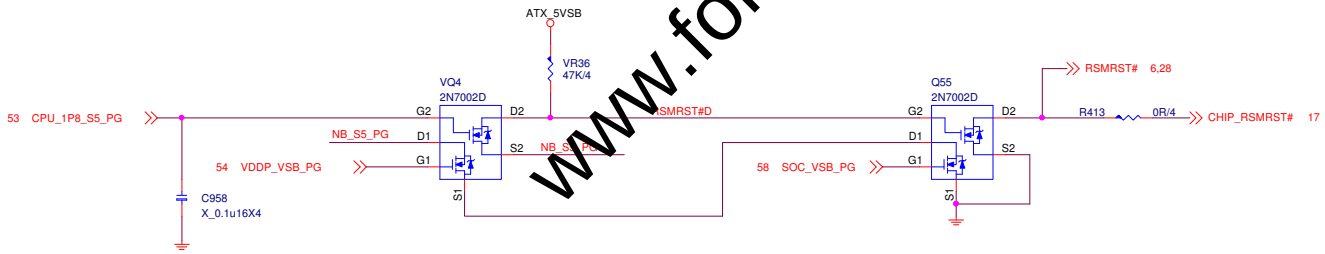
When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
~~DR~~	~~0~~	~~0~~	SPEC no Support
NA	X	0	0
SR	2	CPU VDDP1 NOT SUPPORT TYPE2	
RV/ZP	3	1	0
MTS	4	CPU VDDP1 NOT SUPPORT TYPE4	

S5 PG



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Size: Custom | Document Description: VRM PWRGD | Rev: 11

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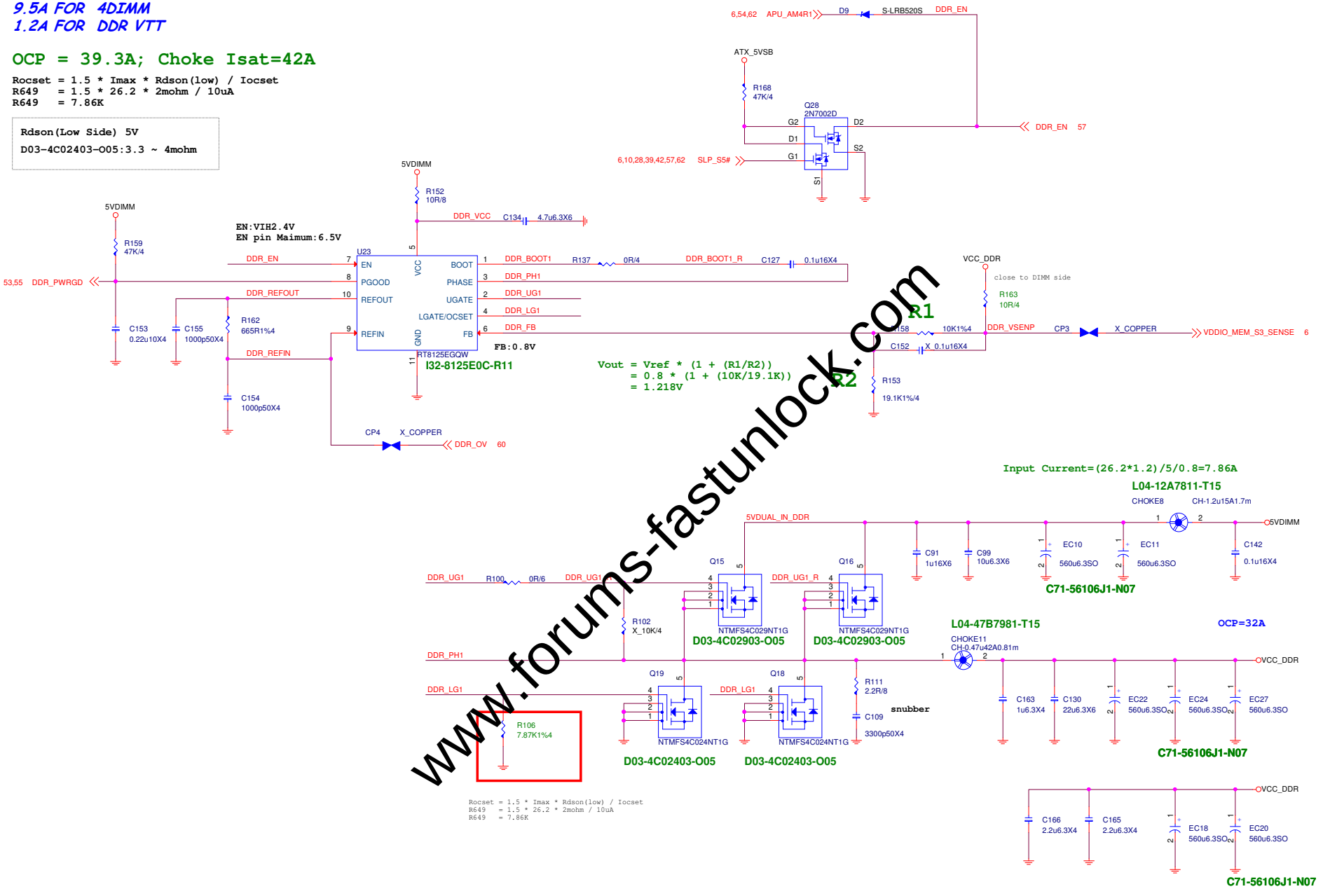
DDR4_1.2V@26.2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

OCP = 39.3A; Choke Isat=42A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649 = 1.5 * 26.2 * 2mohm / 10uA
R649 = 7.86K

Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~ 4mohm



MICRO-STAR INT'L CO.,LTD

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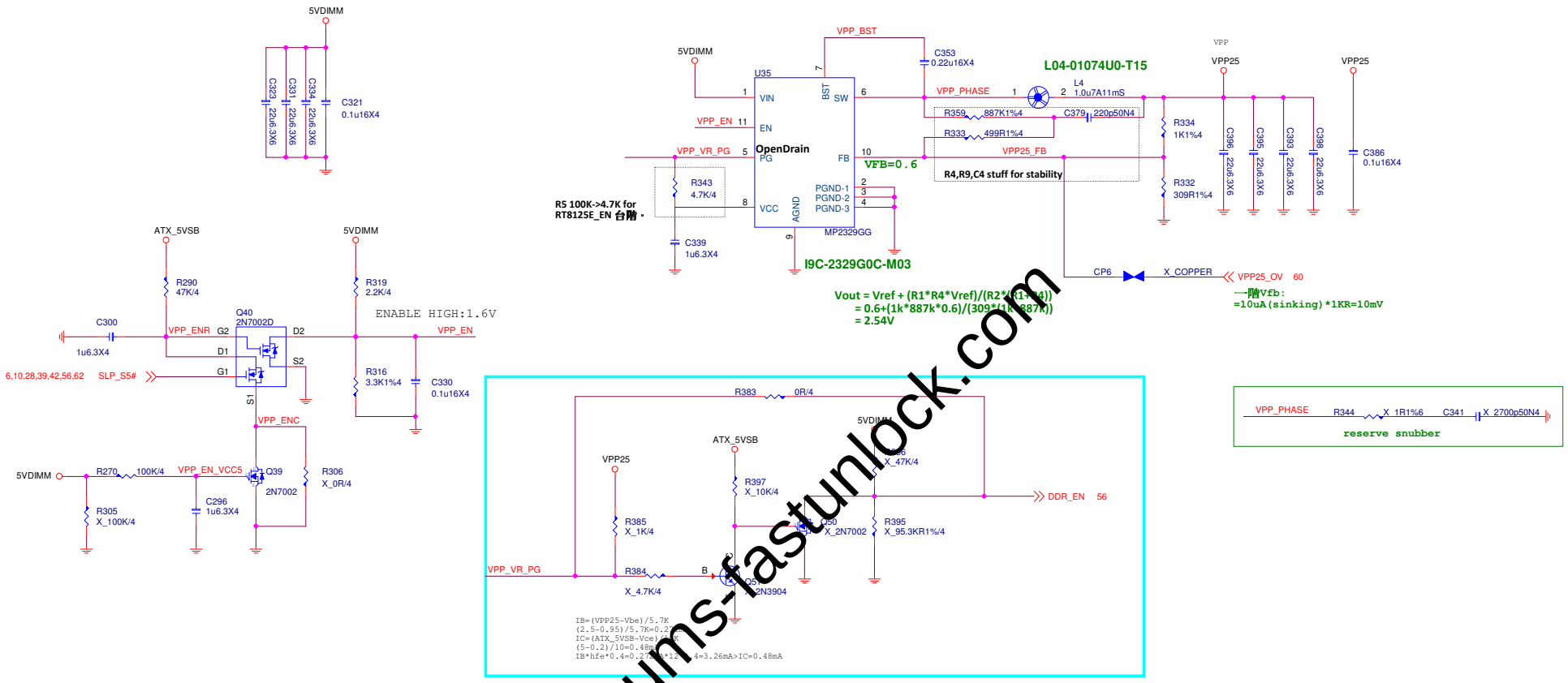
4DIMM : VPP25

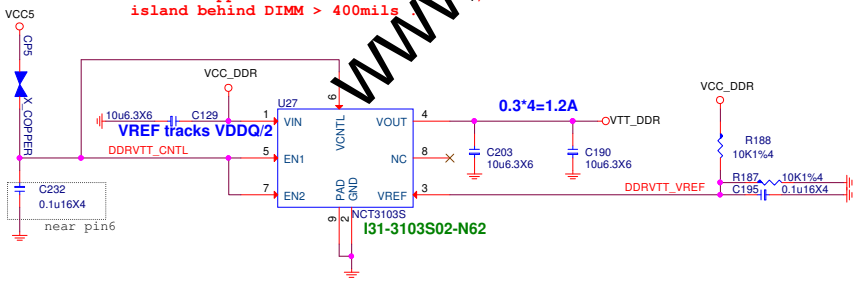
2.5V@2.24A

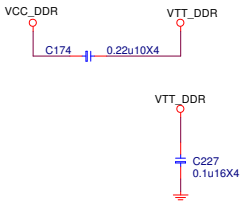
VPP_BST>50 mils.



DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils





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MS-7B93		
Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 11
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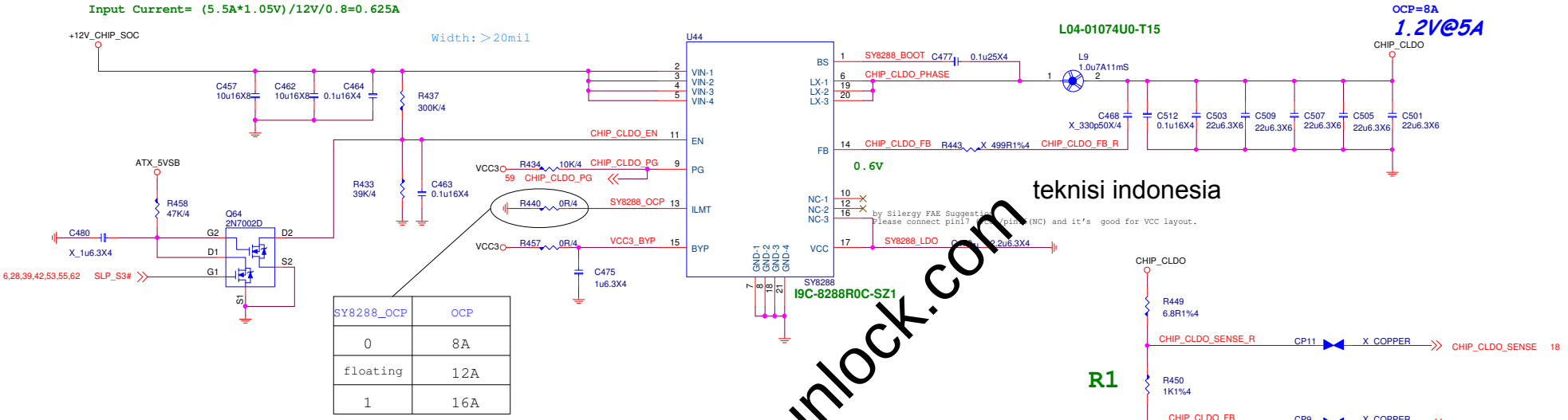
FOR Premium CHIP_CLDO

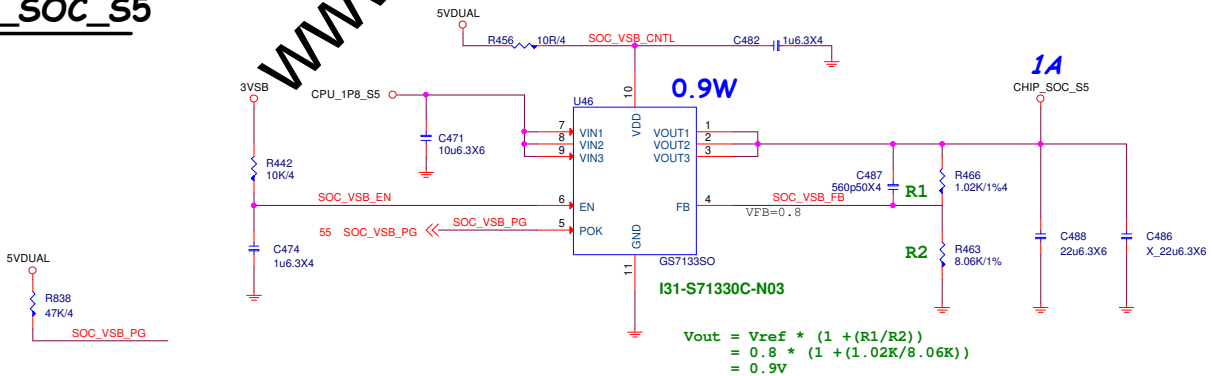
1.2V
S0:5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

FOR Premium CHIP_SOC_S5

1V@1A



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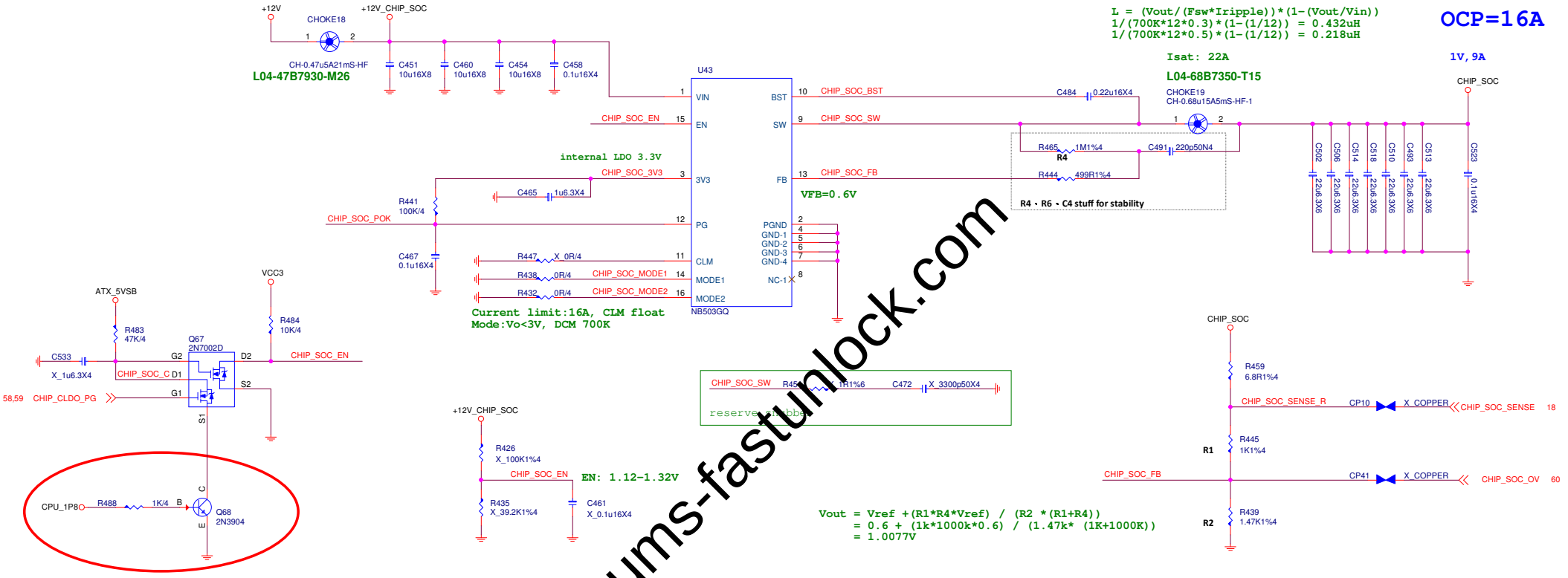
MS-7B93		
Size: Custom	Document Description: PROM - SY8288RAC / 1.05V	Rev: 11
Date: Thursday, July 04, 2019	Sheet 58 of 75	

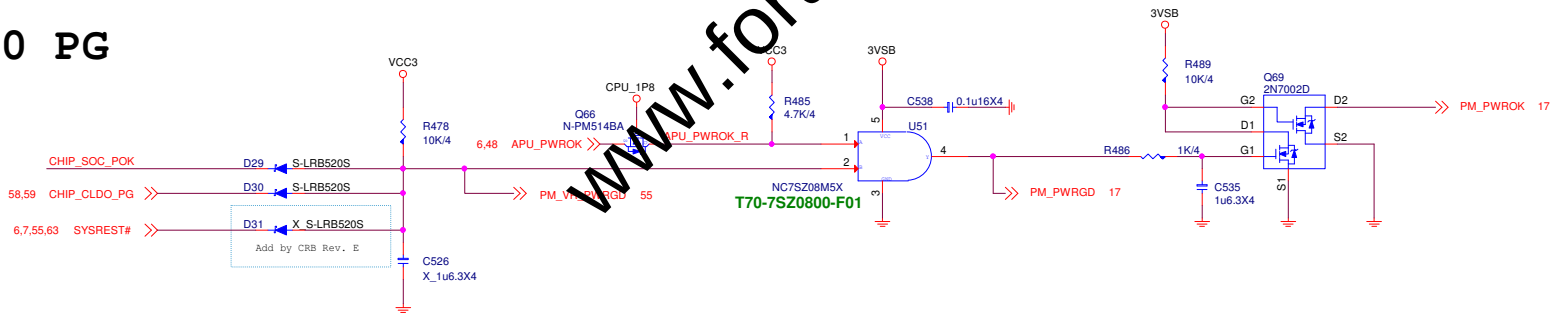
Premium-CHIP_SOC

1V@9A

```
Input Current = (12A*1V)/12V/0.8 = 1.25A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=12*SQRT((1/12)*(1-(1/12))) = 3.316A
Choke Irms =5 A
```



S0 PG



DDR_PWRGD
CPU_VDDP
CPU_1P8
CHIP_CLDO
VCC3
CHIP_SOC

MICRO-STAR INT'L CO.,LTD		
MS-7B93		
Size: Custom	Document Description: CHIP_SOC_NB503	Rev: 11
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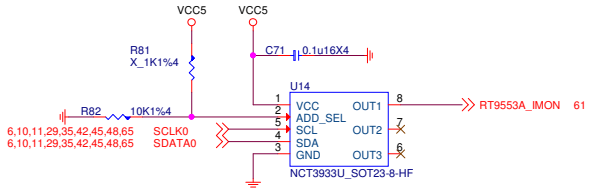
Over Voltage Control IC

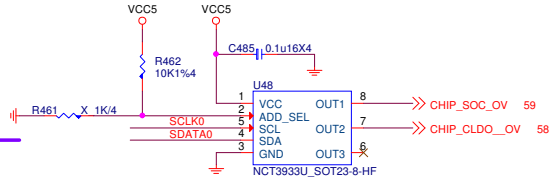
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

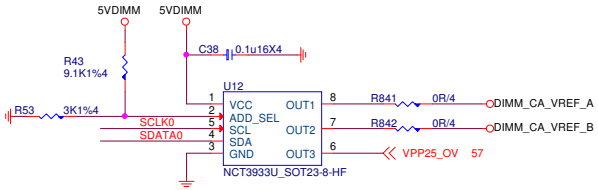
0x2A:RH=OPEN,RL=10K



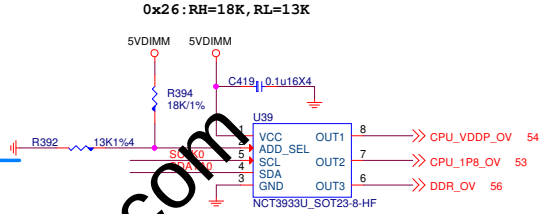
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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Size: Custom	Document Description: OV Control - NCT3933	Rev: 11
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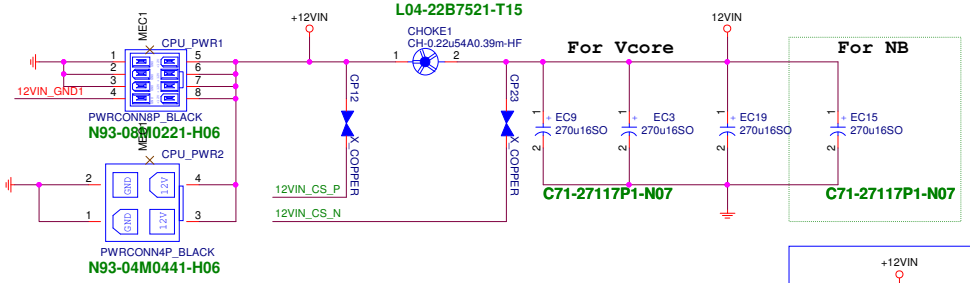
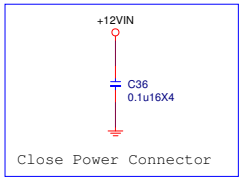
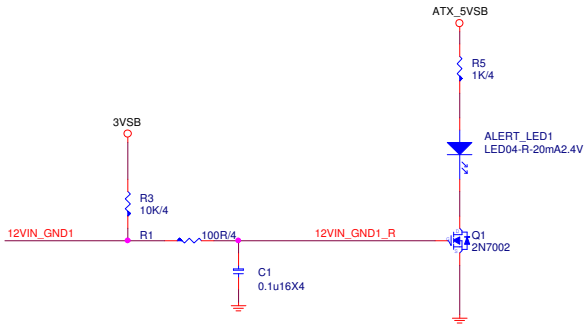
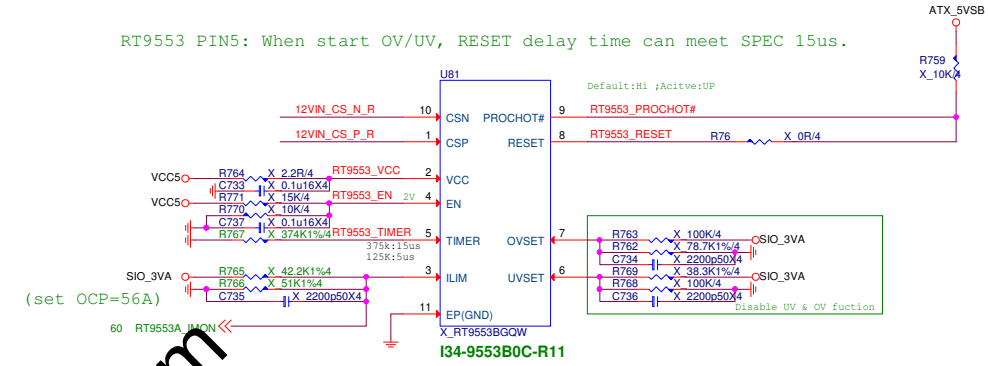
CPU POWER CONNECTOR





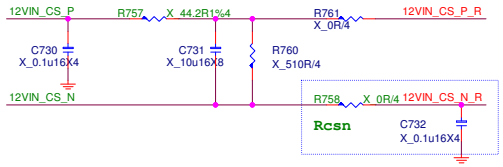


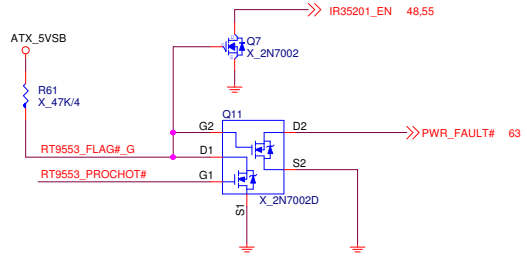
RT9553B CURRENT SENSE



Vcore			
D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	2	> output Vcore
D	=	0.166667	
I o = Icore(max)*0.8			
I core(max)	=	200	> Vcore current
I avg.	=	160	A
I ripple={ Io*√L*f*(1-D) } / Phase			
Phase	=	10	phase
I ripple	=	5.962248	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	2	pcs.

SOC			
D =Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.55	> output Vcore
D	=	0.129167	
I o = Icore(max)*0.8			
I core(max)	=	75	> Vcore current
I avg.	=	60	A
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	2	phase
I ripple	=	10.06153	A
How many pcs. Of Cap.			
I ripple(cap)	=	4700	m A
COE TEMP	=	1	
Input Cap.	=	3	pcs.





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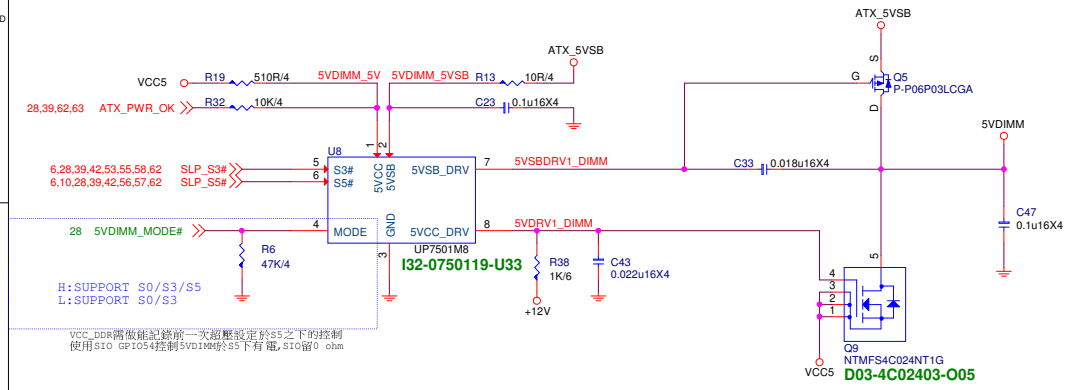
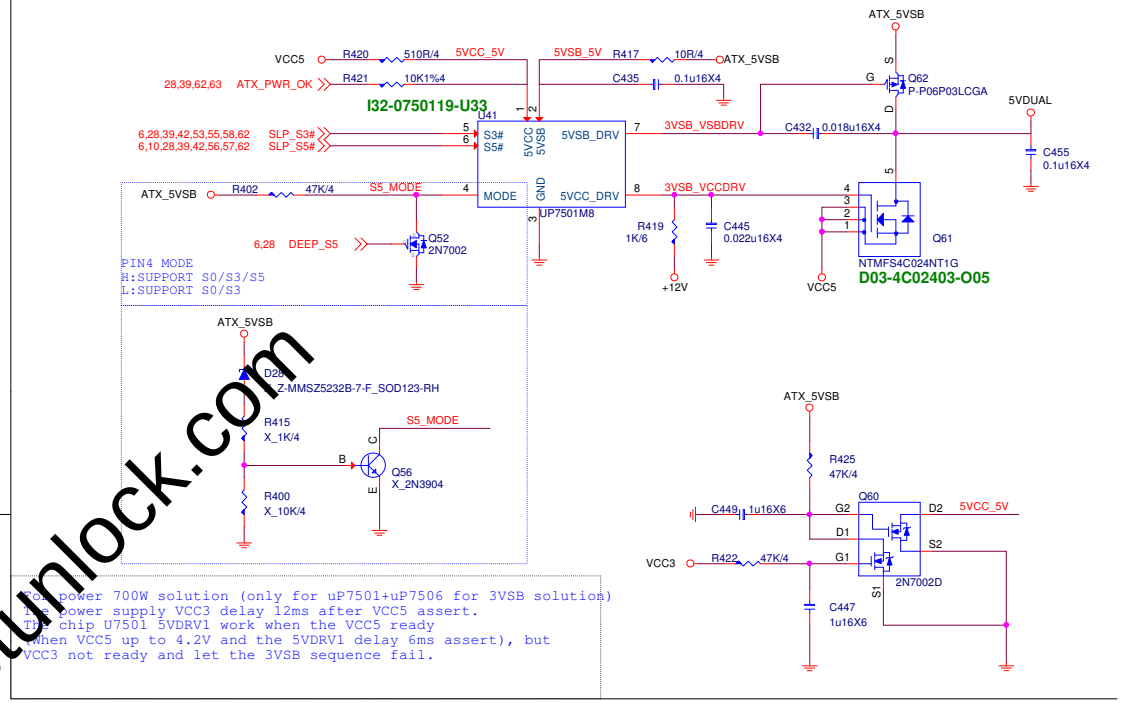
5VDIMM FOR DDR



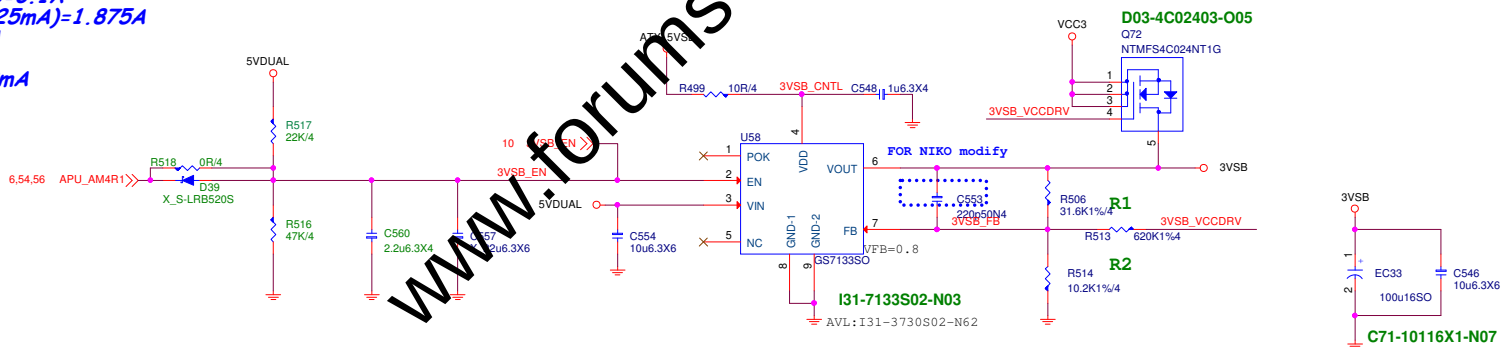
5VDUAL For 3VSB/CPU1.8V/VDDP



3VSB cost down

3.3V@3.125A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
*PCIE=(375mA*1125mA)=1.875A*
M.2WIFI= 0.78A
LAN=0.12A
USB TYPE C :0.9mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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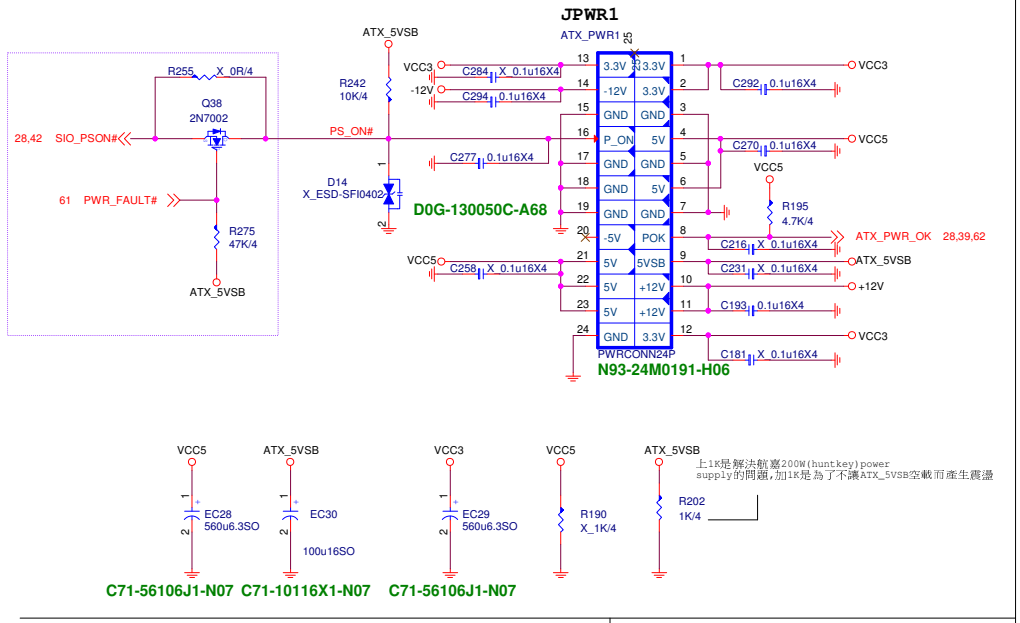
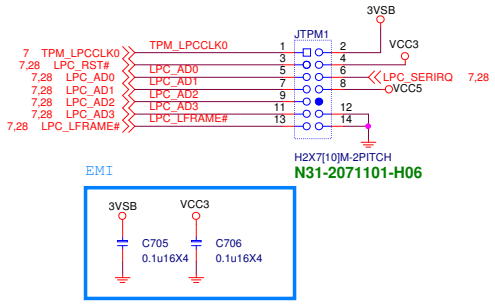
ATX POWER CONNECTOR

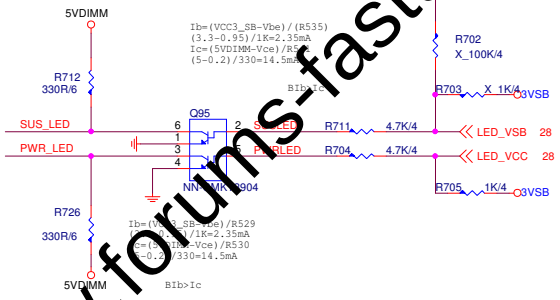


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

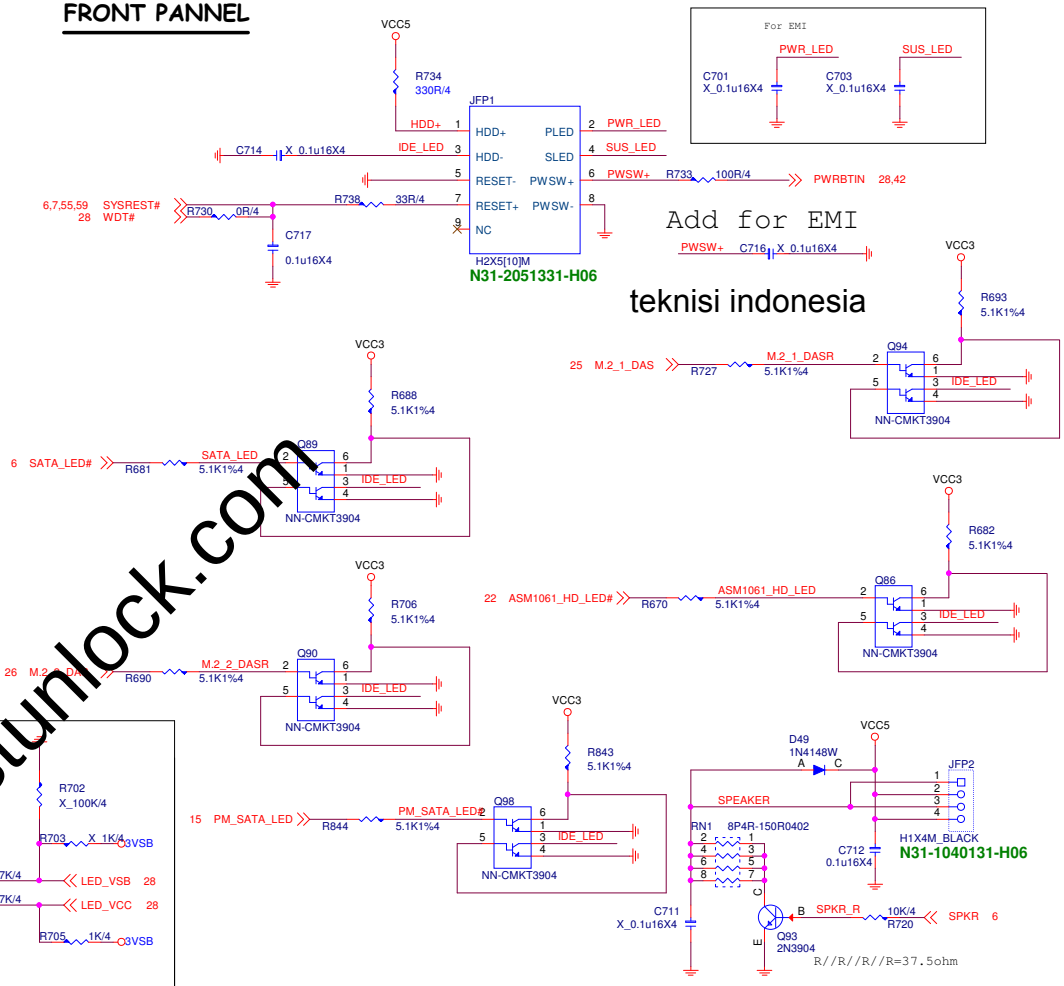
TPM



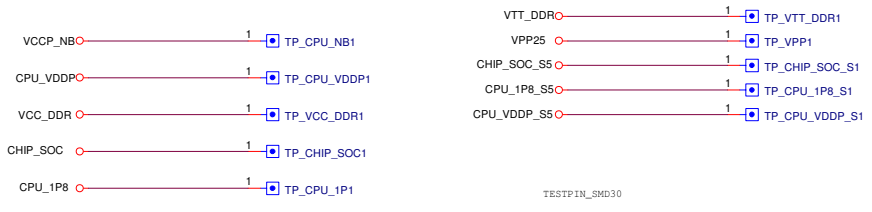
LED (for NCT6797D)



FRONT PANNEL

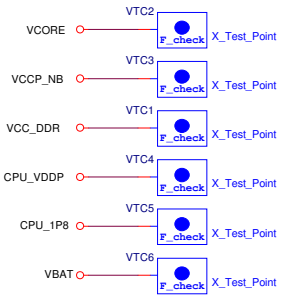


Voltage Mearsure Point



Factory check point

put bottom side



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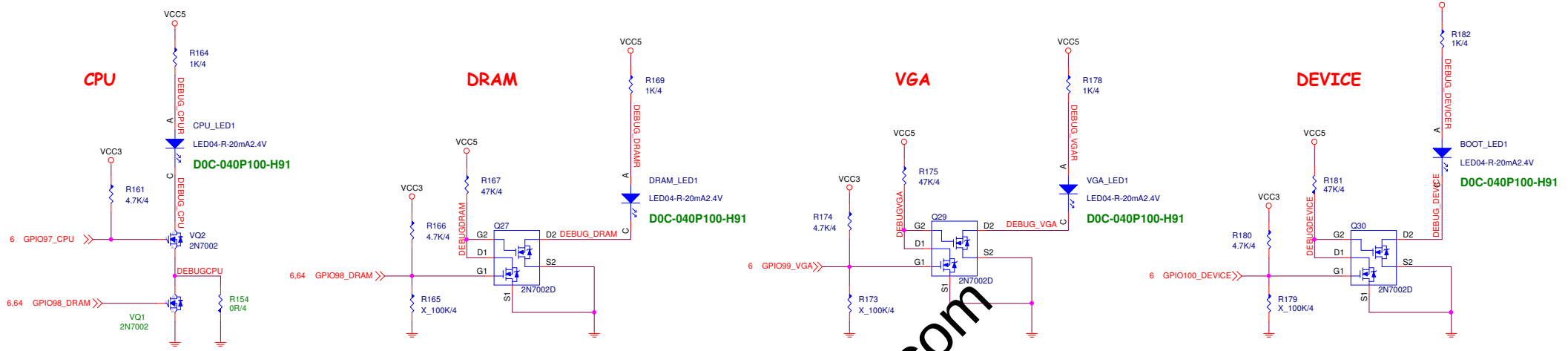
EZ Debug LED



LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07

AMD AMP Detect LED

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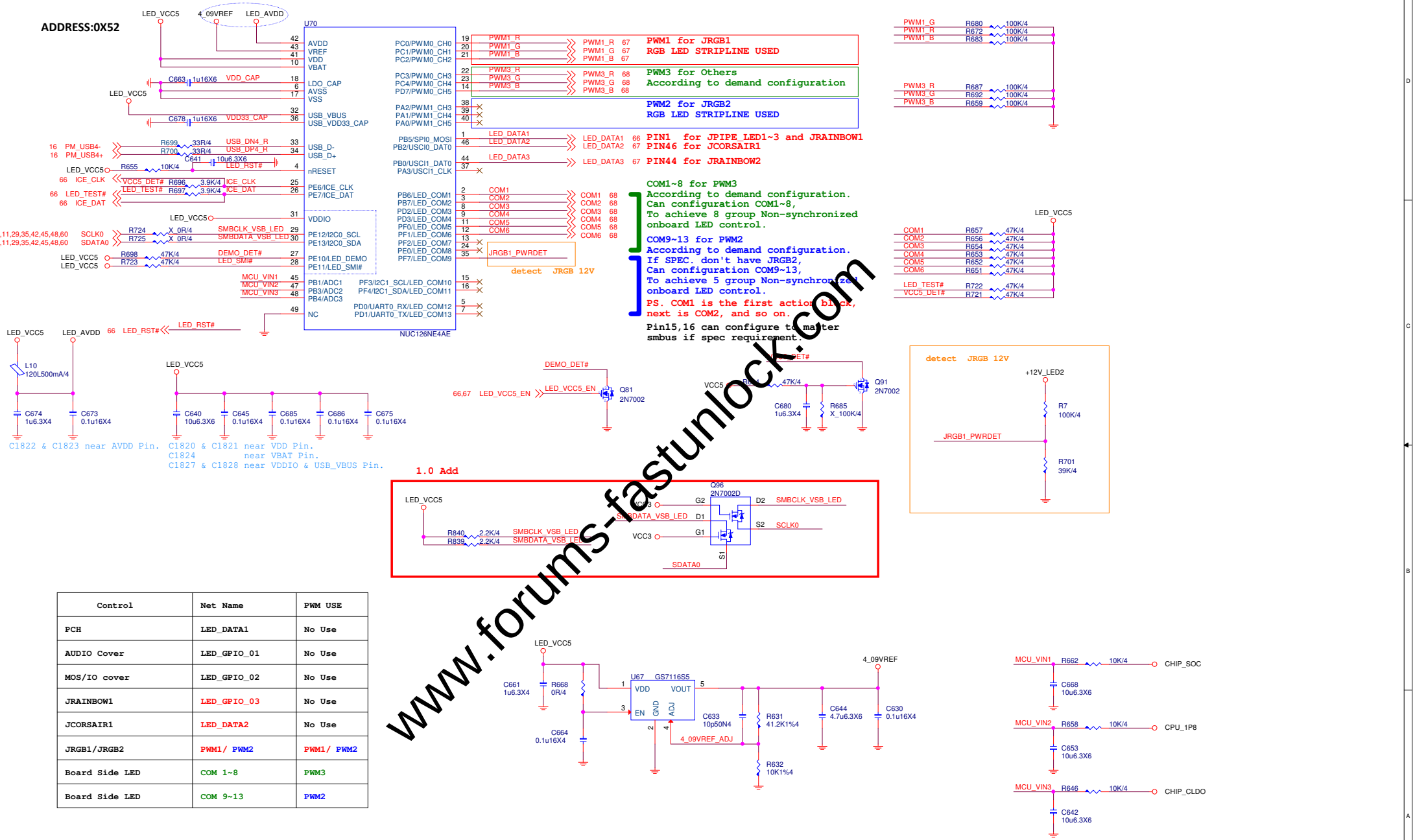
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

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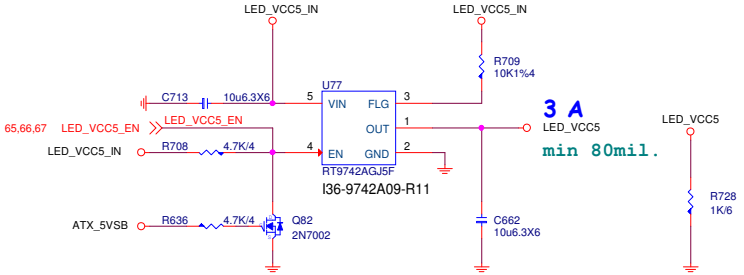
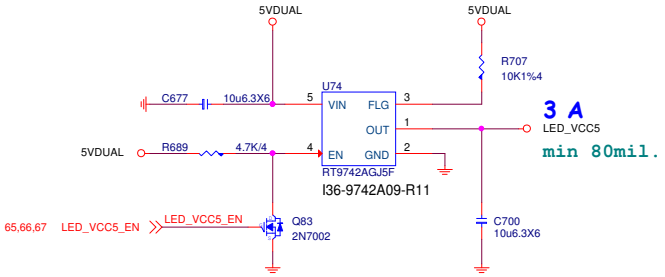
EXTERNAL POWER INPUT

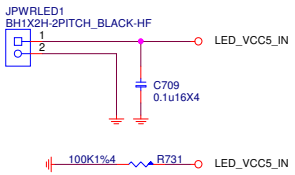




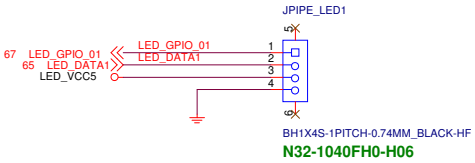
External Power

2A Connector

N32-1020CB1-H06



1 AUDIO/IO Cover LED

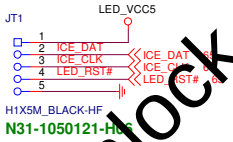


JPIPE:PIN1:output ,PIN2:input

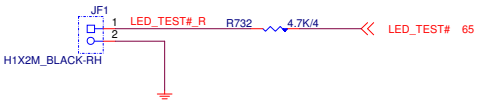
PIN2:MCU IN

PIN1:HEATSINK OUT

JT1 for FW update



JF1 for Factory test



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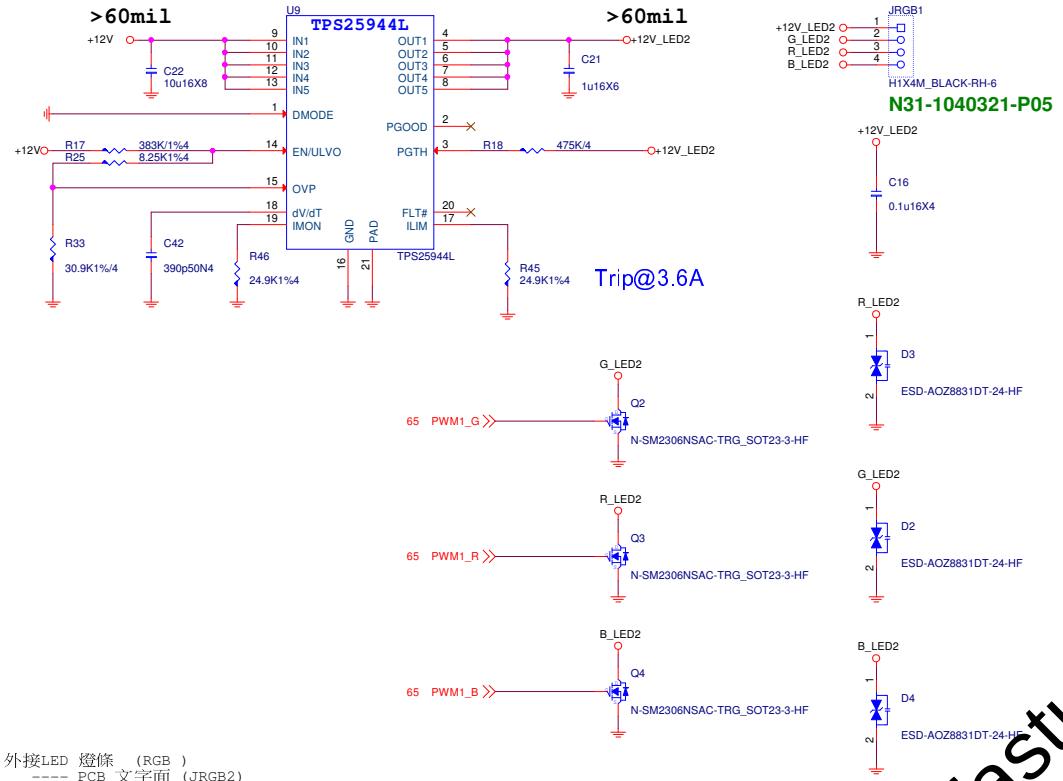
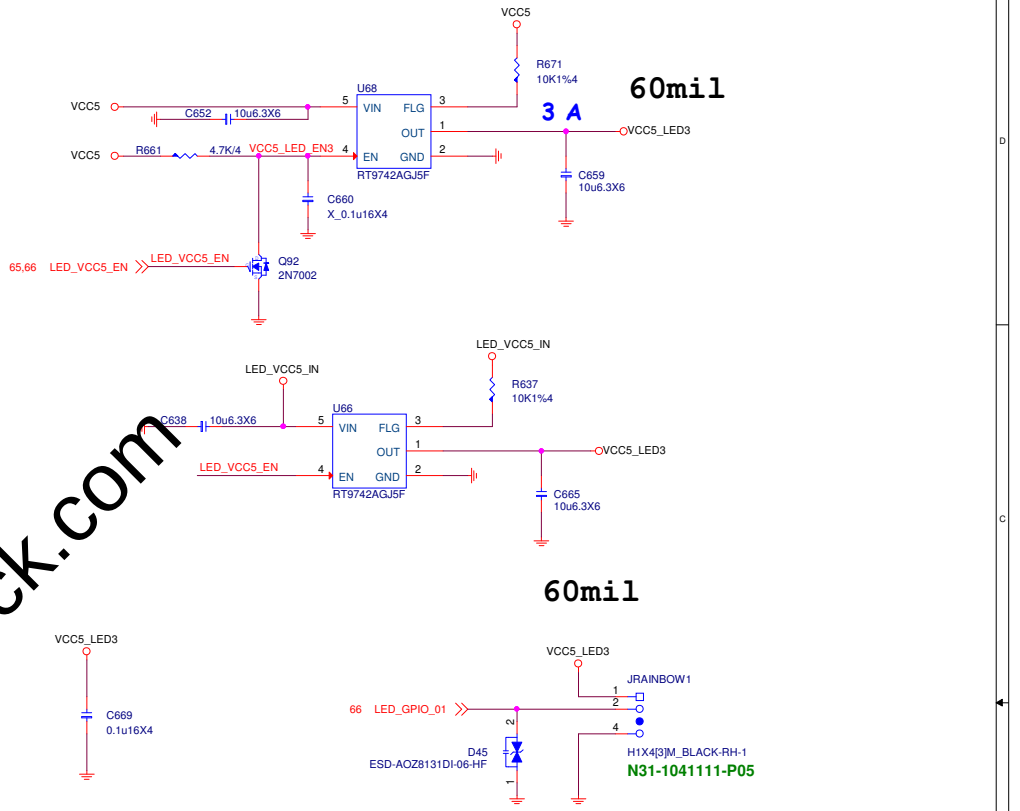
JRGB1

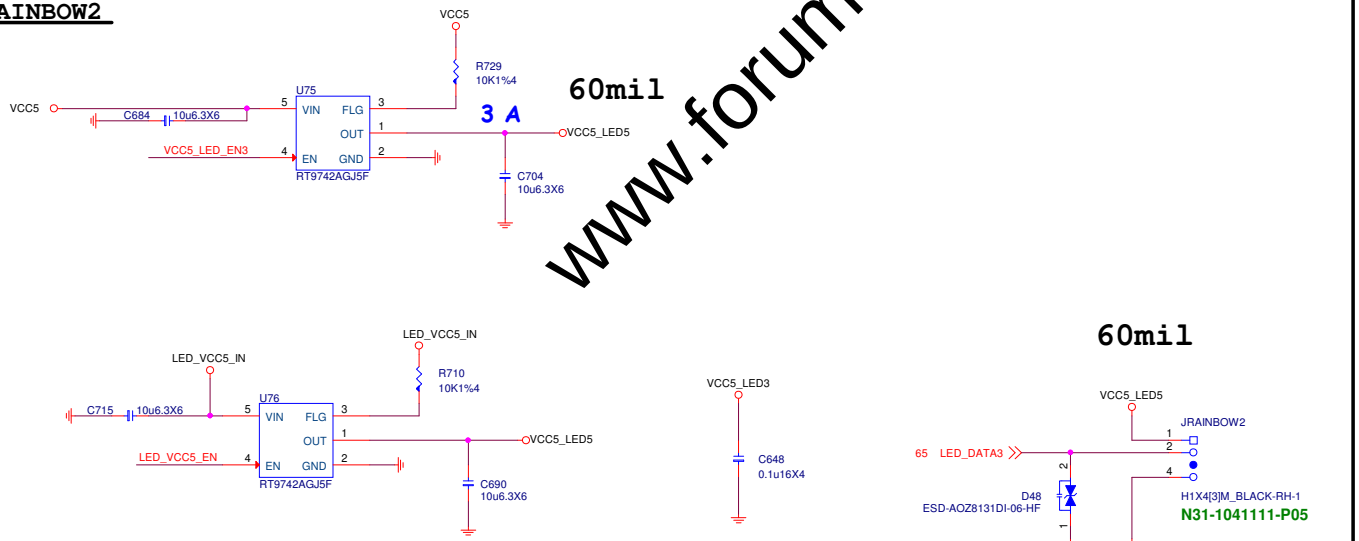


外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB2)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B)，燈條總輸出電流限制為3安培 (12 伏特)
長度限制為2公尺

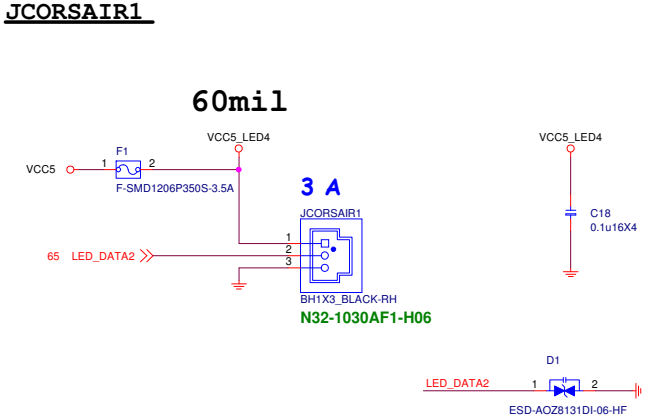
JRAINBOW1



JRAINBOW2



JCORSAIR1



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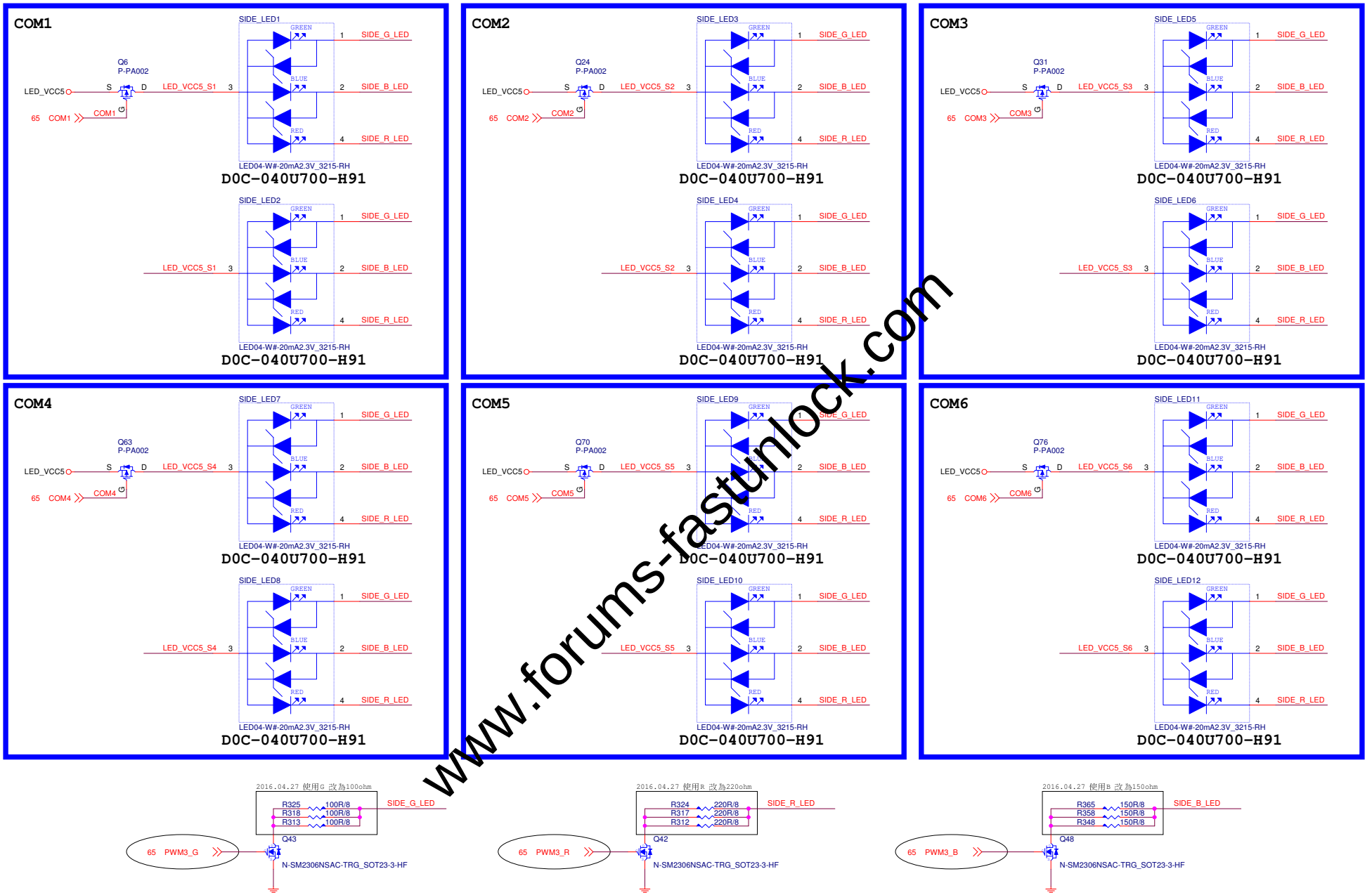
BOARD SIDE LED *12



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MS-7B93

Size	Document Description	Rev
Custom	LED - Mystic Light - 1	11

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MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7B93	
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CPU Socket

CPU2

E95-0000021-C22

E95-0000022-C22

Simulation

X_JS2 — SIM1 — X_PIN1*2

X_JS1 — SIM2 — X_PIN1*2

FM3 FM8 FM2 — X_FM120

FM1 FM4 FM6 — X_FM120

FM7 FM5 — X_FM120

Optics Orientation Holes

MH1 MH2 MH3 MH5 MH4 MH6 MH9 MH8 MH7 — X_MH001

Holes_4s_V8

C689 0.1u16X4

C676 0.1u16X4

BAT1_X1

BAT-BCR2032P

MANUAL PART

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

CFOS <MSI-BOM>

Y02-MU00170-CFO

Y02-MU00170-CFO

HDMI_LA1

Label

HDMI

HDMI LABEL

Y01-RHDMI03-000

NAHIMIC1 <MSI-BOM>

Y02-MU00100-NAH

Y02-MU00100-NAH

PCB

PCB

PCB1

7B93_10

PD0-07B9311-E48

PD0-07B9311-G37

AVL:

D06-0100161-F52

D06-0100101-K26

MOS HEATSINK

HS_NMOS — MEC1 MEC2

HS-0506270-RH

E31-0506270-A87

HS_WMOS — MEC1 MEC2 MEC3 MEC4 MEC5

HS-0506260-RH

E31-0506260-A87

PCH HEATSINK

HS_PCH — MEC1 MEC2

HSFAN-0406731-RH

E32-0406731-A87

PCH Heatsink OPT

PCH1000

PCH H270

X_E32-0406731-A87

Audio COVER

U52

Audio Cover

E21-7A62010-RH

IO COVER

U90

IO Cover

E22-7B93010-RH

DDR COVER

20190201 Remove DDR_COVER1

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