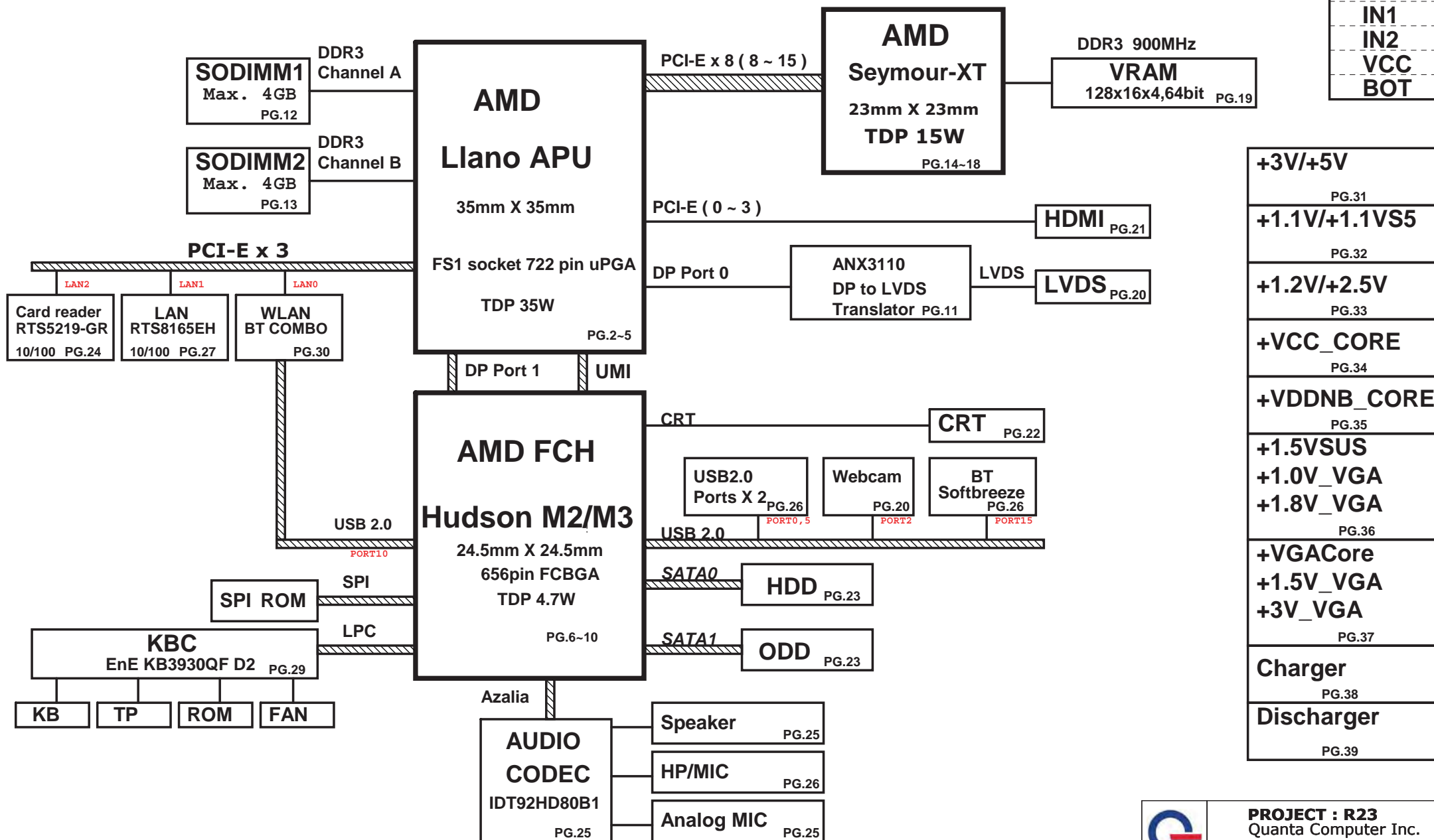


# R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM

## Stackup

TOP  
GND  
IN1  
IN2  
VCC  
BOT









---

5



Document N





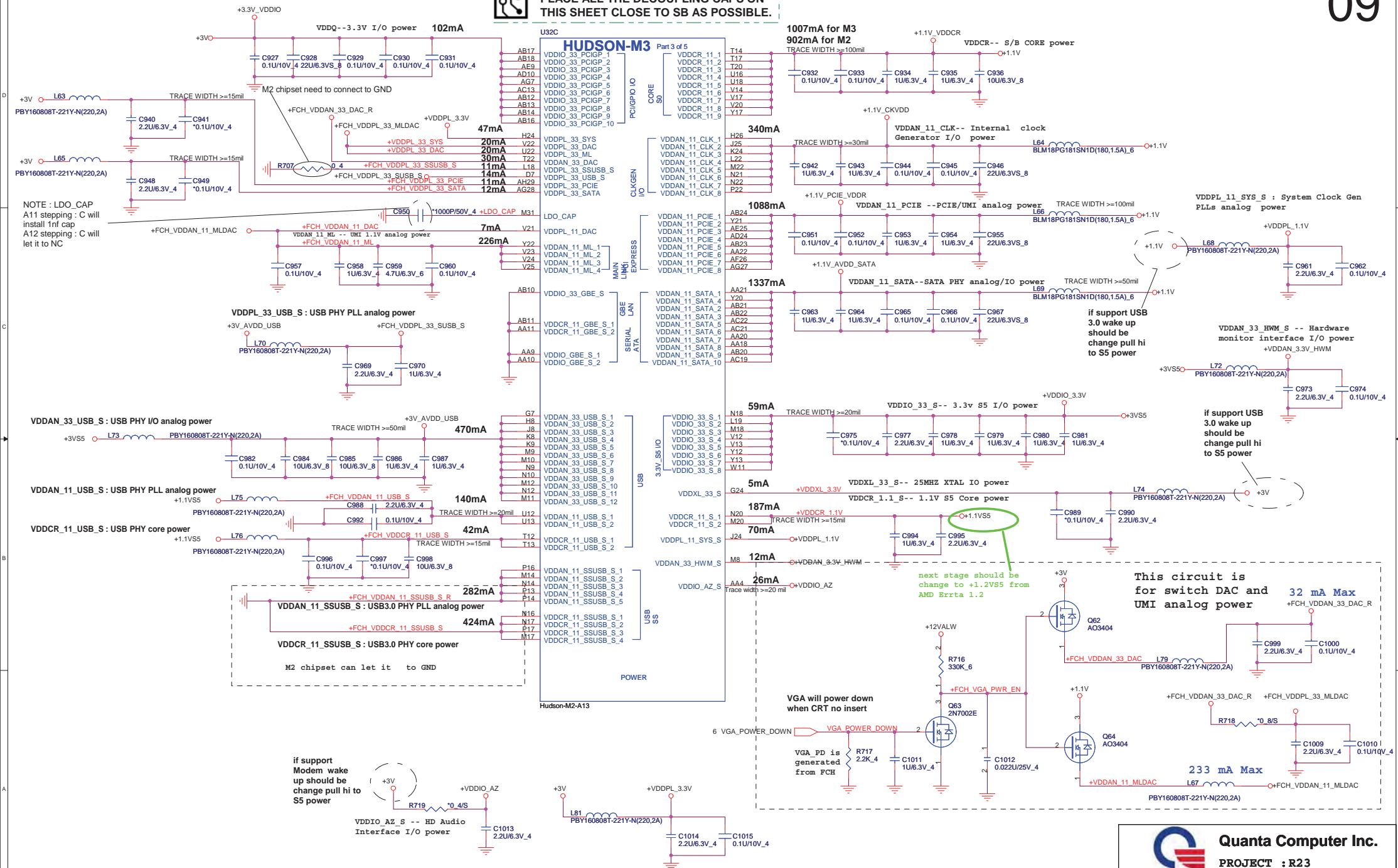








**PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.**



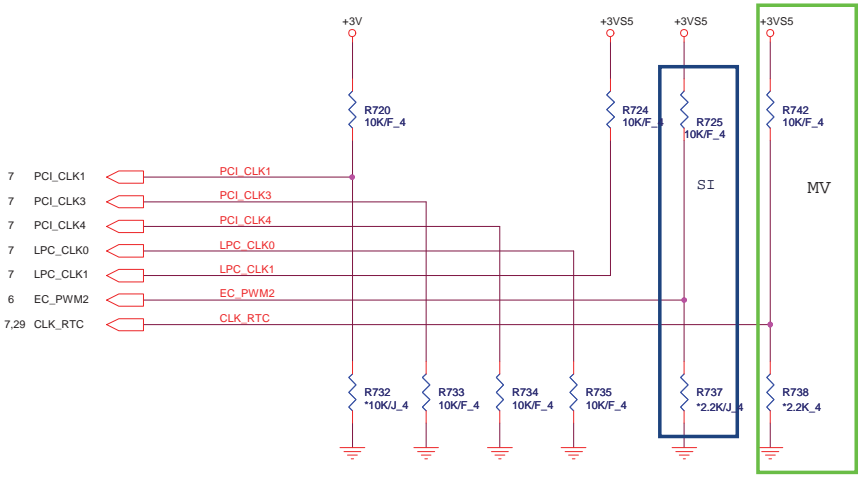
**Quanta Computer Inc.**

PROJECT : R23

Size	Document Number <b>Hudson-M3 POWER/GND</b>	Rev 1A
Date:	Wednesday, May 04, 2011	Sheet 9 of 40

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2  DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

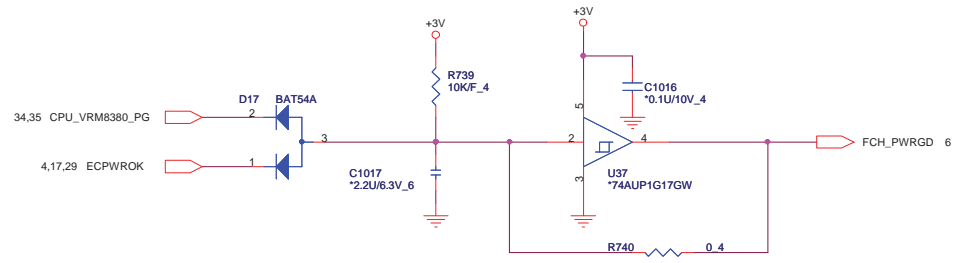
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI\_AD[27:23]

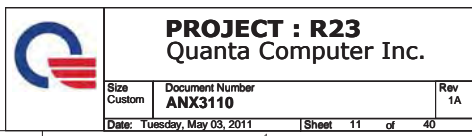
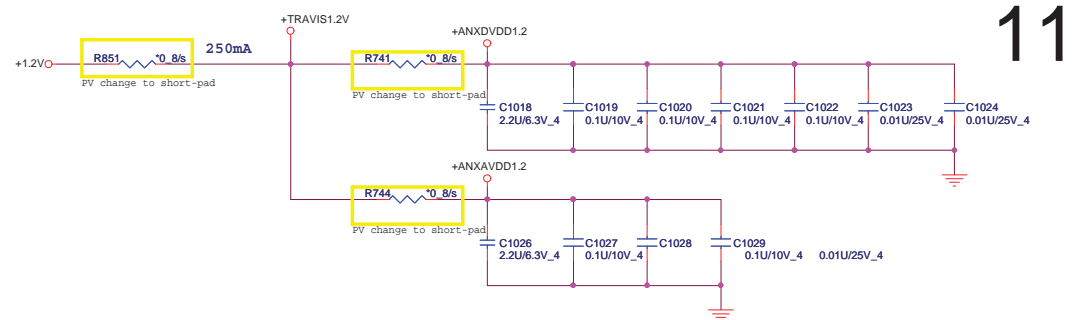


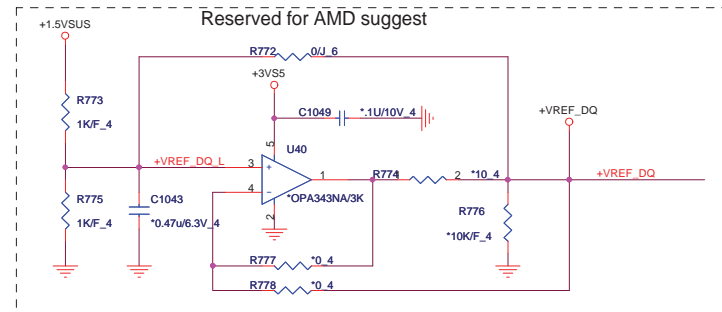
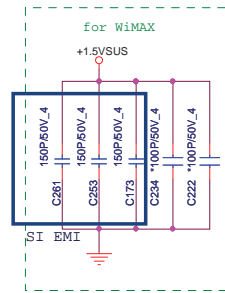
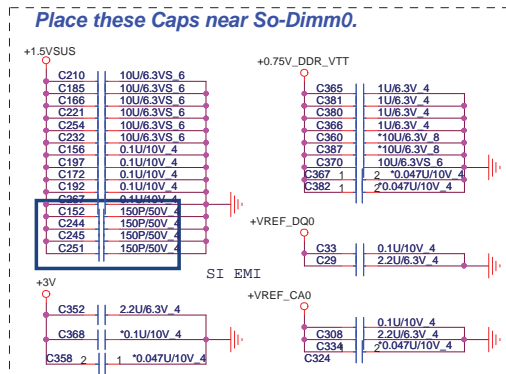
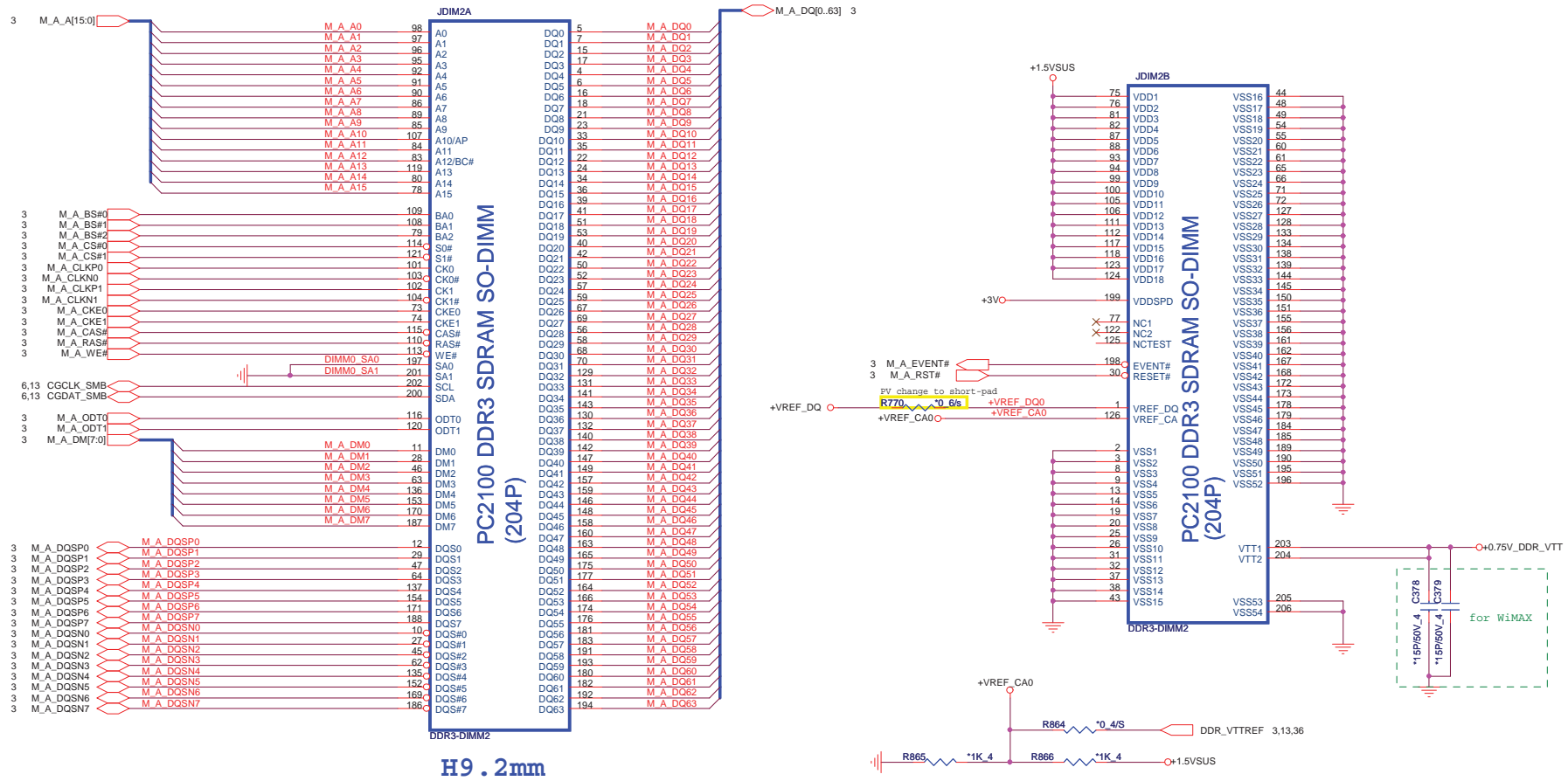
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL  DEFAULT	DISABLE ILA AUTORUN  DEFAULT	USE FC PLL  DEFAULT	USE DEFAULT PCIE STRAPS  DEFAULT	DISABLE PCI MEM BOOT  DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

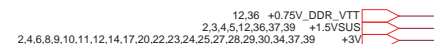
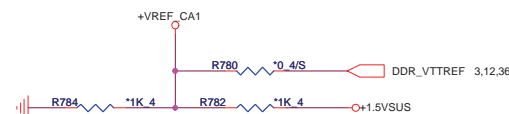
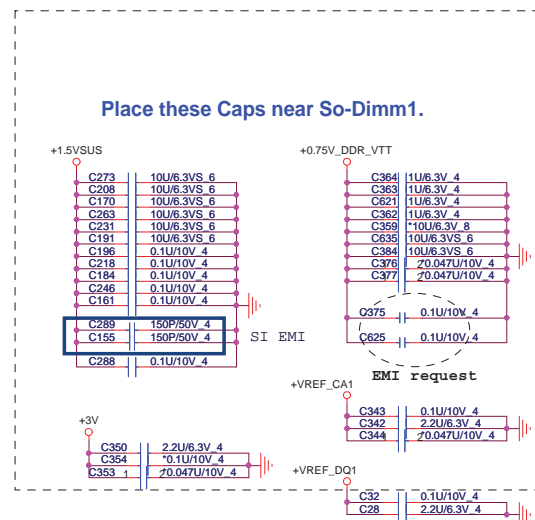
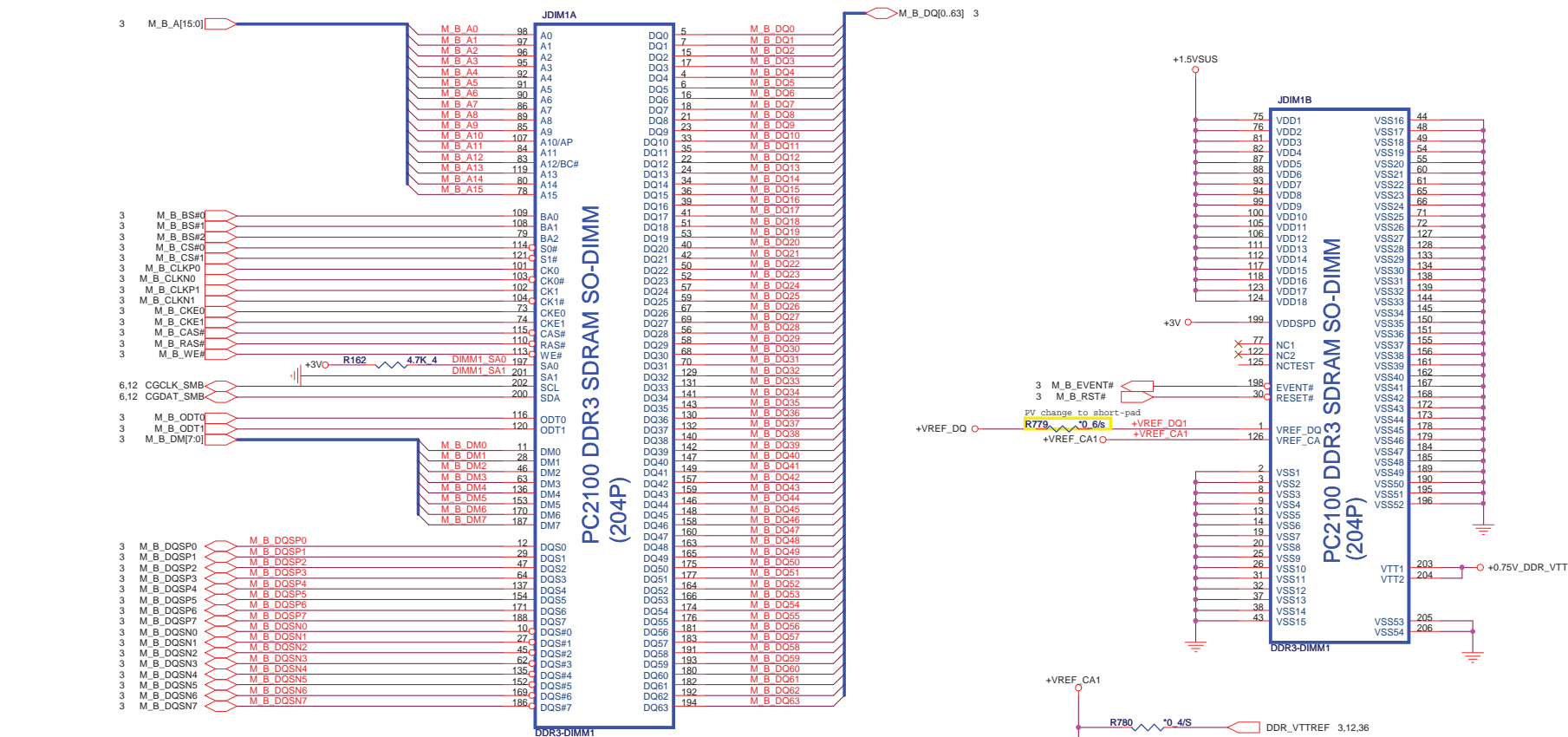


## 11





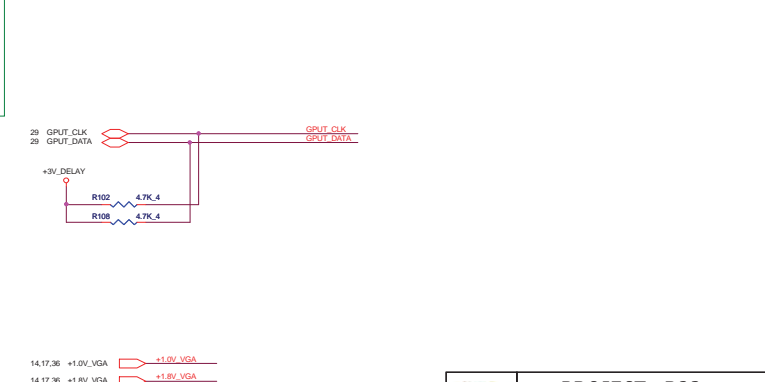
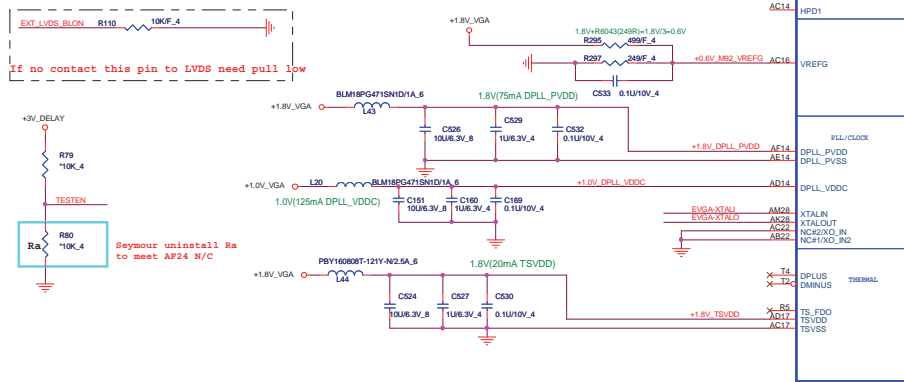
13.36 +0.75V\_DDR\_VTT  
2.3,4,5,13,36,37,39 +1.5VSUS  
2,4,6,8,9,10,11,13,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V







	U178	
	<b>Seymour-S3</b>	
TP198	AES	DIVCNTL_0 DIVDATA_18
TP199	LS	DIVCNTL_1
TP200	NS	DIVCNTL_2 INC
TP201	AES	DIVDATA_12 DIVDATA_16
TP202	AD8	DIVDATA_11 DIVDATA_20
TP203	ACU	DIVDATA_10 DIVDATA_22
TP204	AD7	DIVDATA_9 DIVDATA_12
TP205	ACS	DIVDATA_8 DIVDATA_14
TP206	AD6	DIVDATA_7 DIVCNTL_9
TP207	AB8	DIVDATA_6 DIVDATA_8
TP208	AB6	DIVDATA_5 DIVDATA_6
TP209	AB7	DIVDATA_4 DIVDATA_5



**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

GENERICC

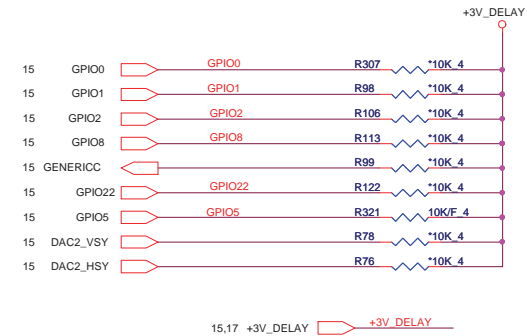
**PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

GPIO21\_BB\_EN



GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

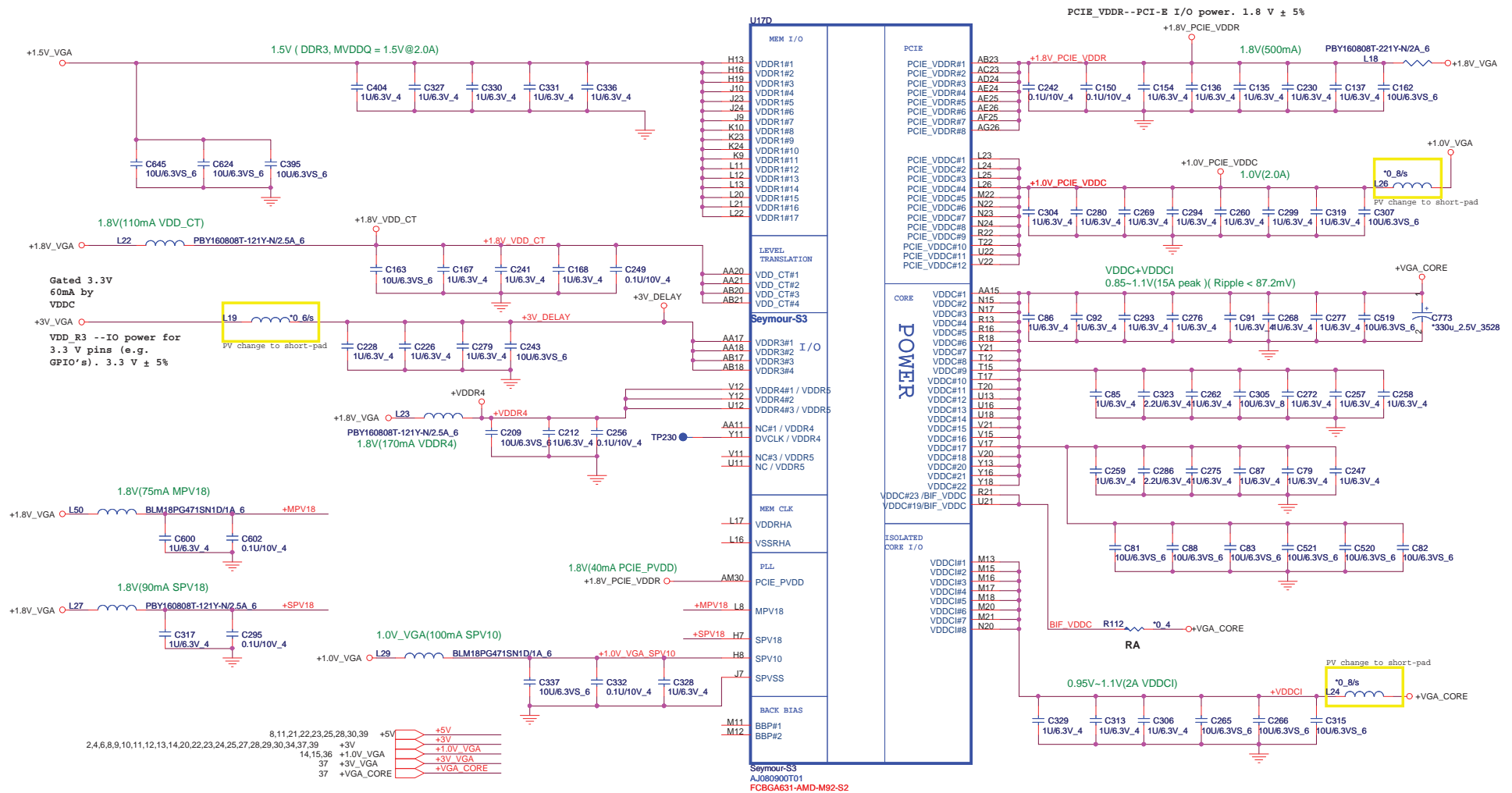
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.



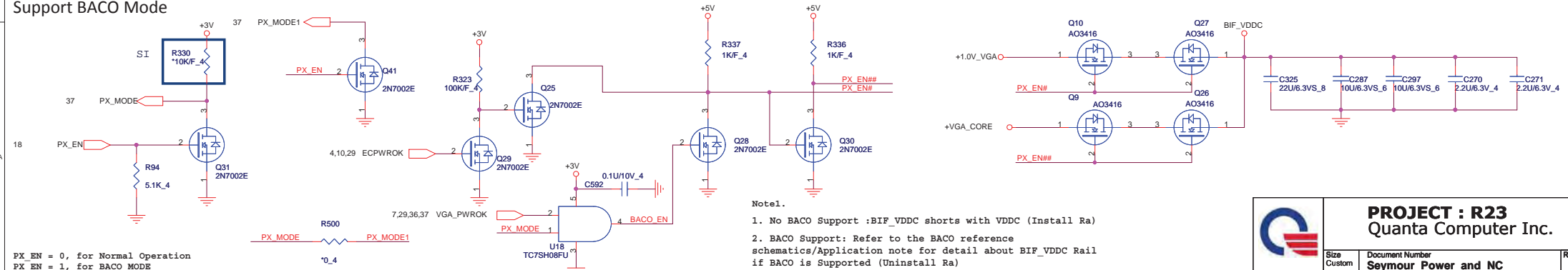
Custom	<b>Seymour GND / LVDS/ Straps</b>
--------	-----------------------------------

Date: Tuesday, May 03, 2011 Sheet 16 of 40

Rev



Support BACO Mode	
-------------------	--



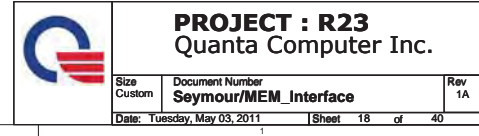
Notel.

1. No BACO Support :BIF\_VDDC shorts with VDDC (Install Ra)
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF\_VDDC Rail if BACO is Supported (Uninstall Ra)

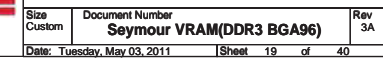


**PROJECT : R23**  
Quanta Computer Inc.

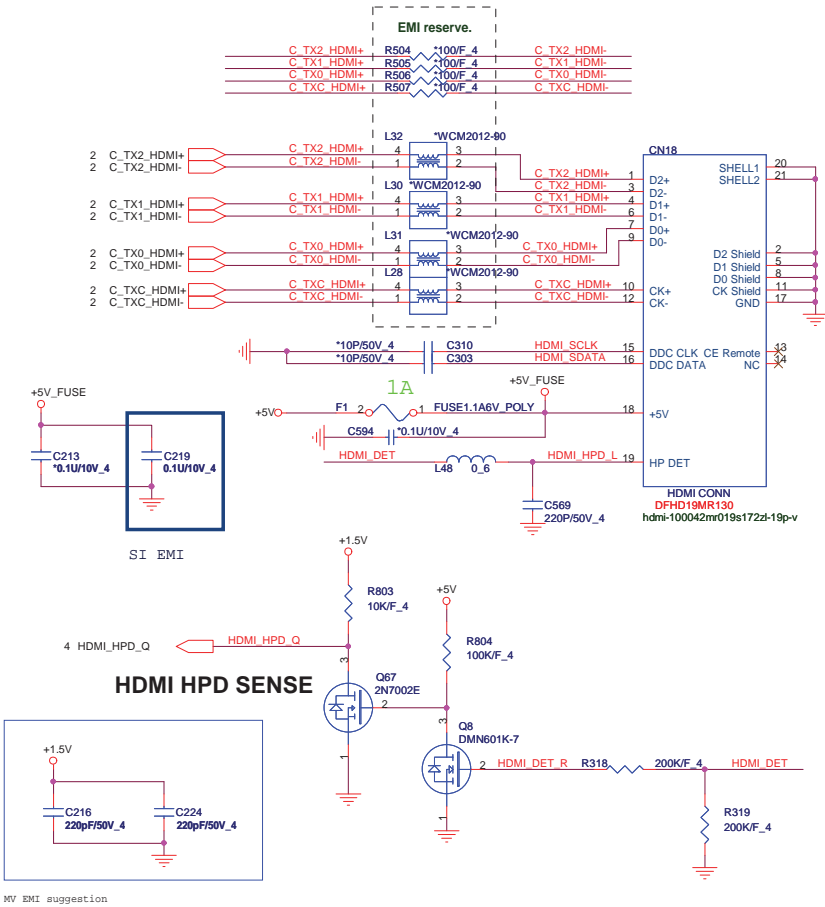
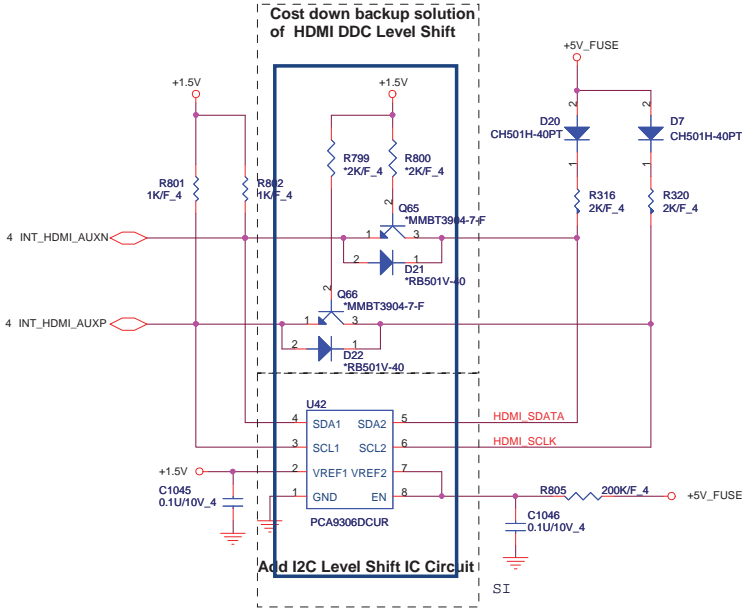
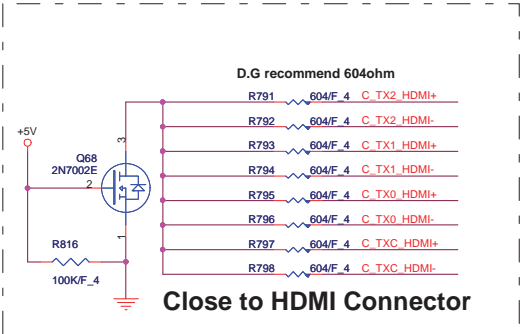
Size Custom	Document Number <b>Seymour_Power_and_NC</b>	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 17 of 40	

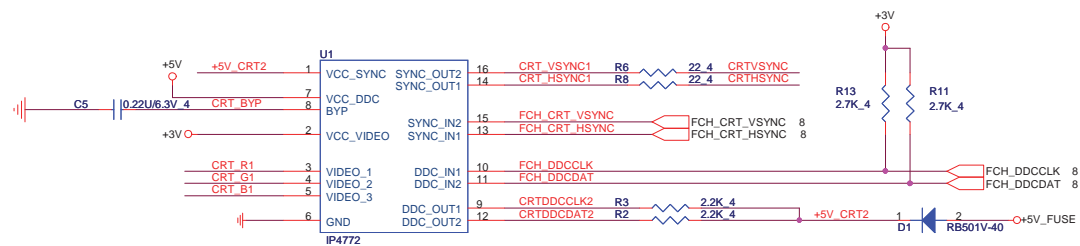




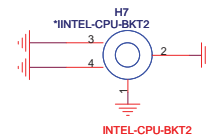
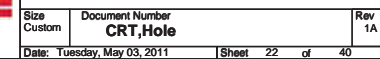
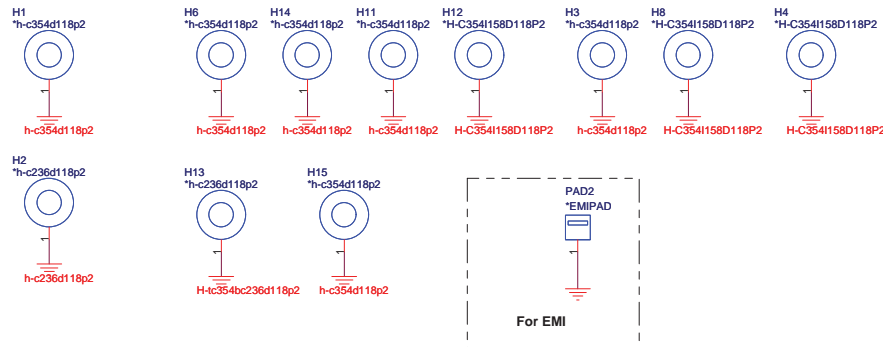
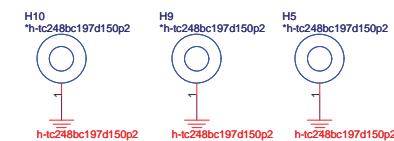




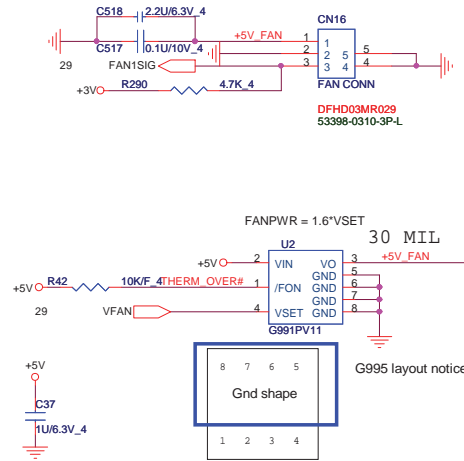




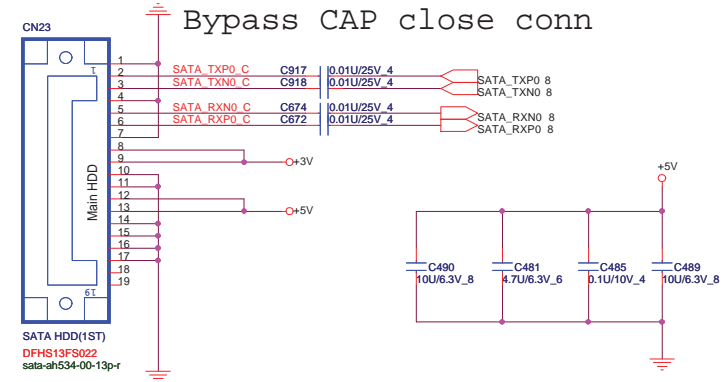
## CPU

**VGA**

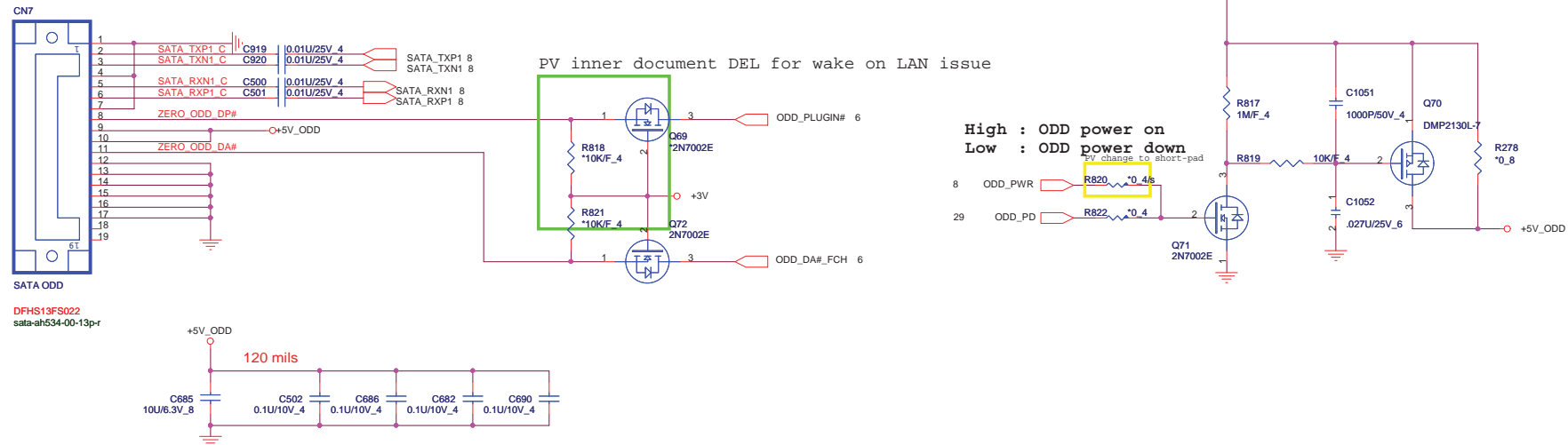
## CPU FAN



## SATA HDD CONNECTOR



## SATA ODD CONNECTOR SATA ODD







2,4,6,8,9,10,11,12,13,14,17,20,22,23,24,27,28,29,30,34,37,39 +3V  
8,11,17,21,22,23,28,30,39 +5V

Close to CODEC

Close to CODEC

HDA Bus

TO Digital MIC

Close to CODEC

Check SB side and  
vendor reply it  
should reserve only

Analog

Close to CODEC

Digital

Close to CODEC

Close to CODEC

TO Headphone jack

TO Audio Jack MIC

TO Internal Speakers

EMI Request

INT. SPEAKER

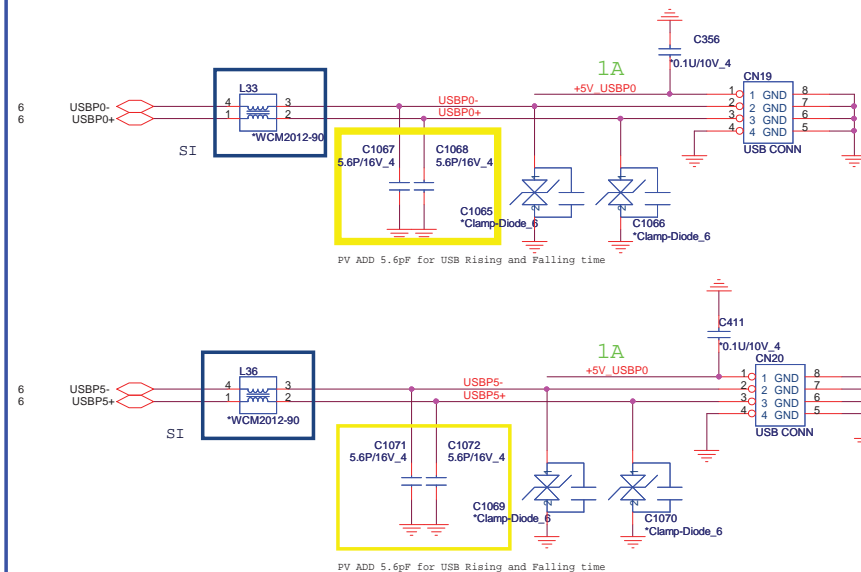
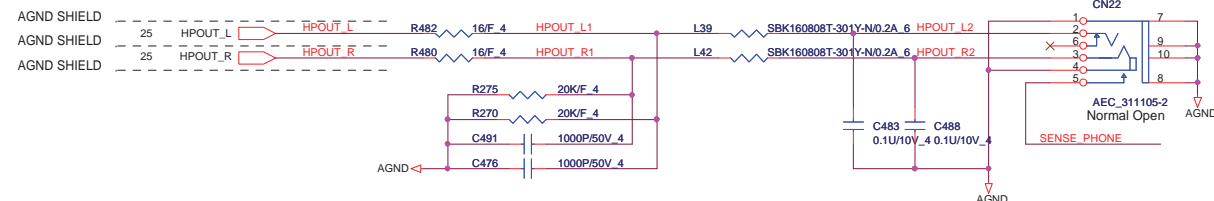
PV ADD 0ohm for EMI suggestion



**PROJECT : R23**  
Quanta Computer Inc.

Size Custom	Document Number <b>Azalia 92HD80</b>	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 25 of 40	

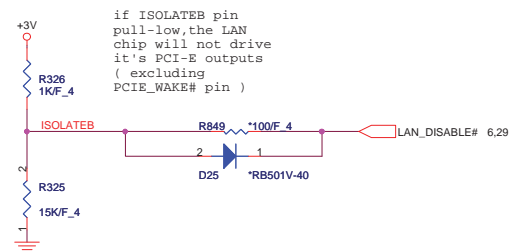
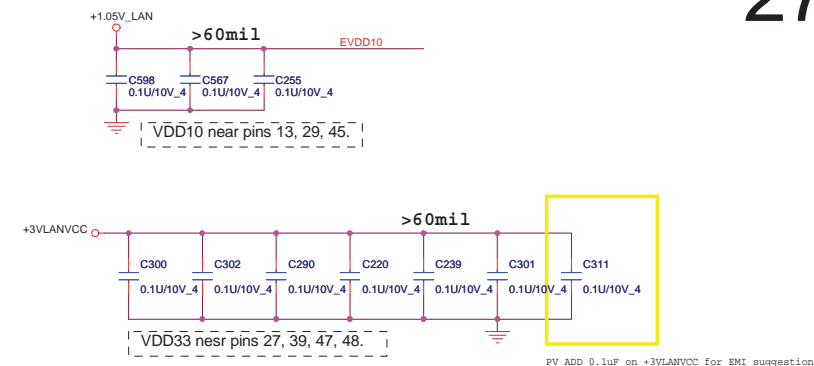
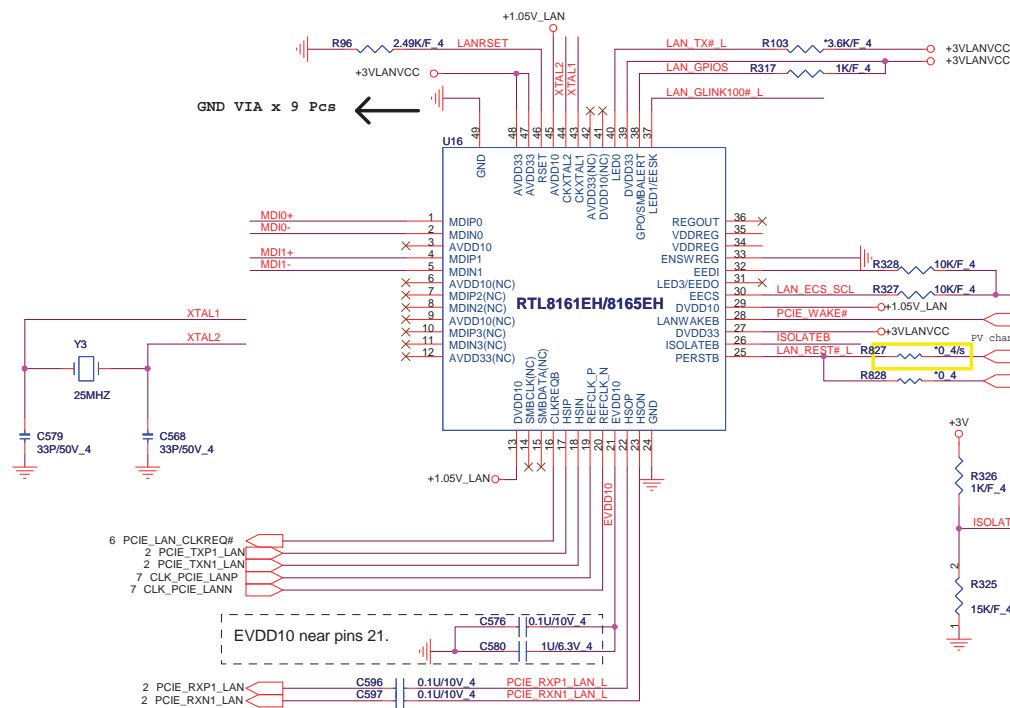
## 26

[illegible]

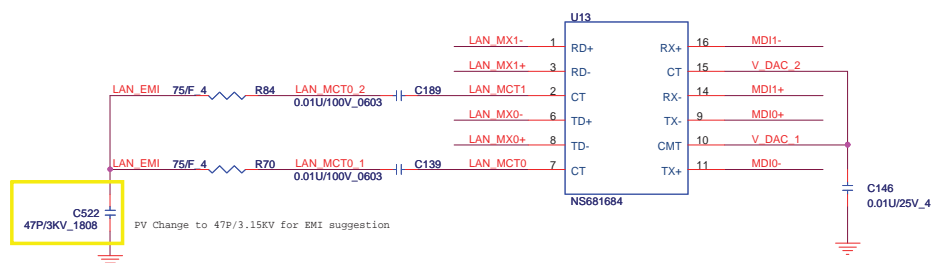
The MIC section schematic shows the microphone input circuit. It includes a microphone connected to the MIC\_IN\_L and MIC\_IN\_R pins of the AEC\_311105-2 module. The microphone is also connected to the MIC\_L and MIC\_R pins of the VREFOUT\_C pin. The circuit includes resistors R248, R246, R244, R245, capacitors C455, C456, C436, C688, C689, and the AEC\_311105-2 module.



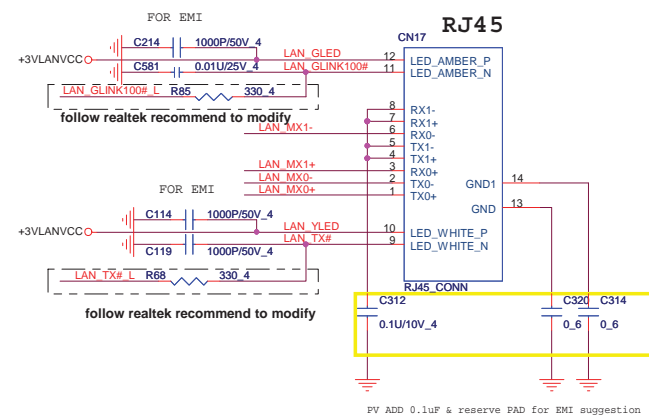
Size Custom	Document Number <b>USB/BT/Audio Jack</b>	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 26 of 40



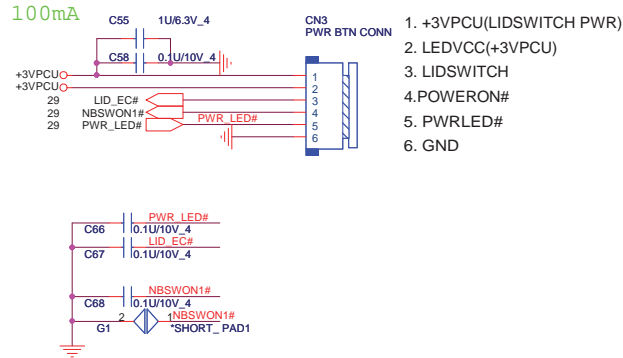
## Transformer for 10/100



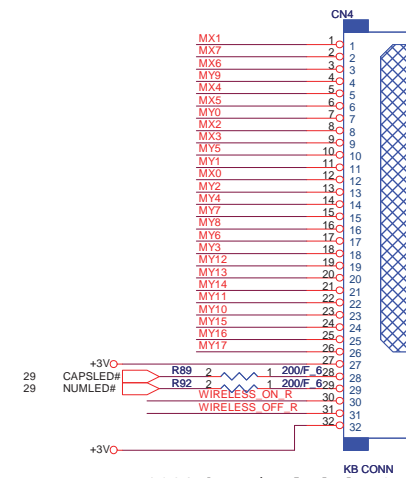
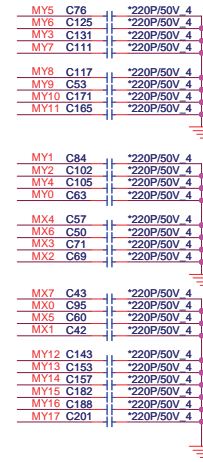
**Lan Con.**



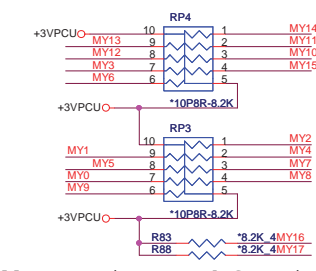
## POWER BOTTON CONNECT



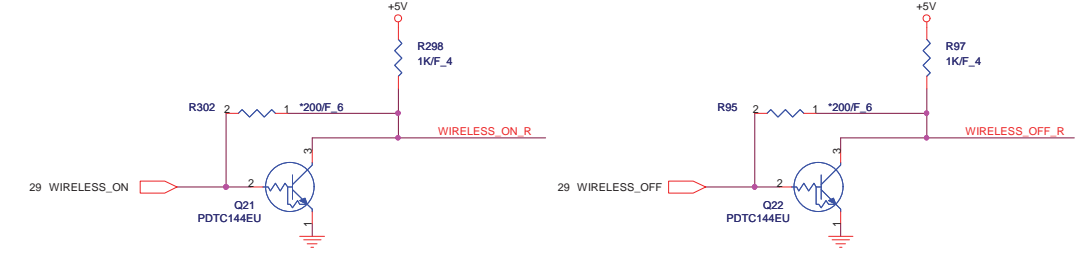
## KEYBOARD Con.



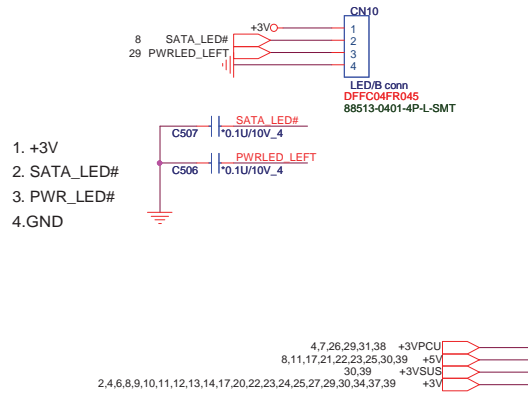
## KEYBOARD PULL-UP



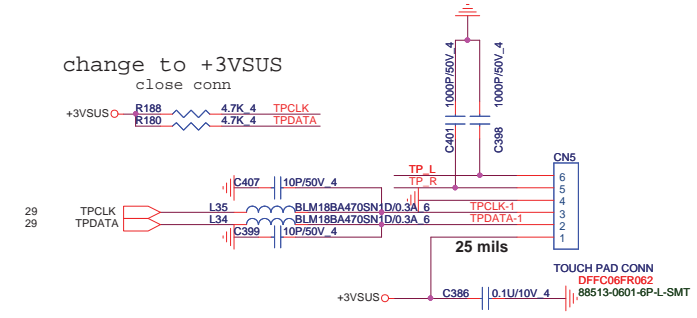
EC KB3930 has included K/B pull-up resistor and function



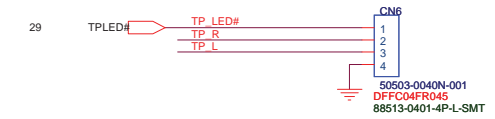
## LED Con.

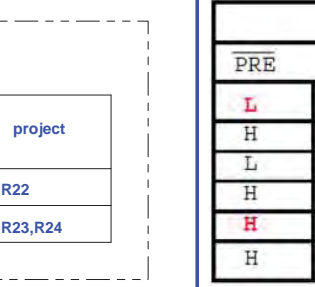
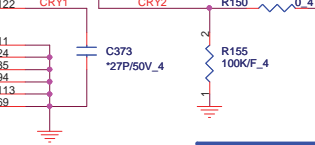
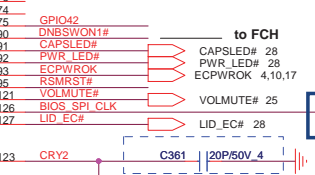
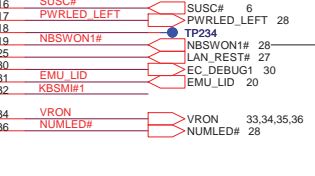
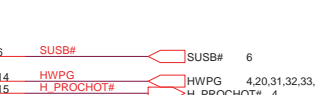
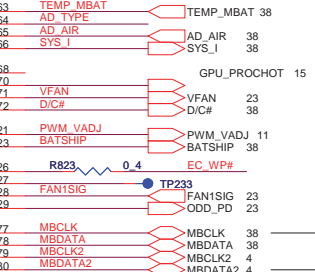
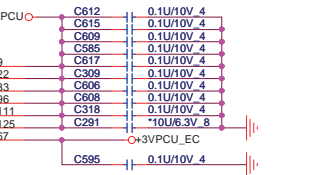
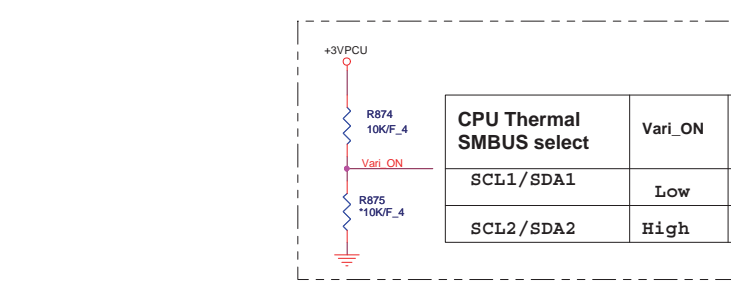
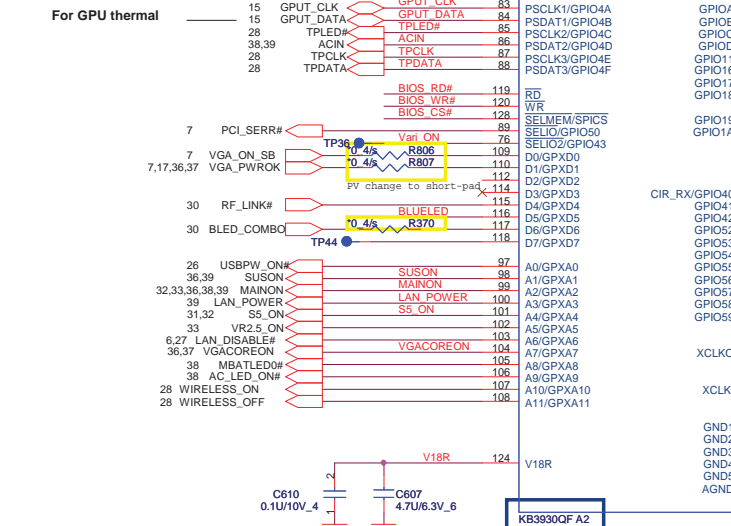
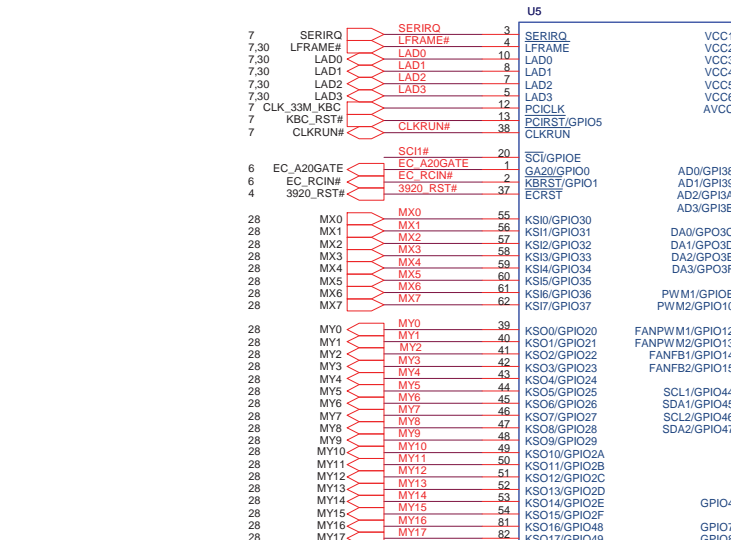


## TOUCH PAD Con.

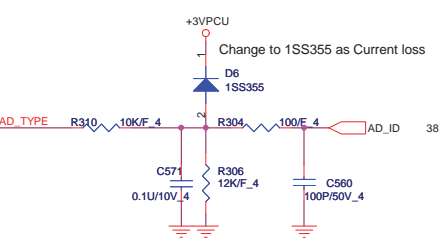


## To TOUCH PAD SW board

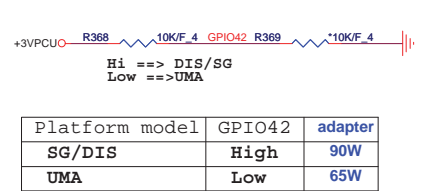




## Smart adapter Type check



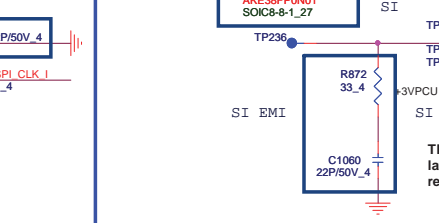
## Adapter select



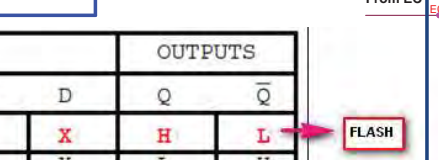
Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

Vender	Size	P/N
AMIC	128K	AKE35ZN0801
EON	128K	AKE35FNOQ00
Socket		DFHS08FS023

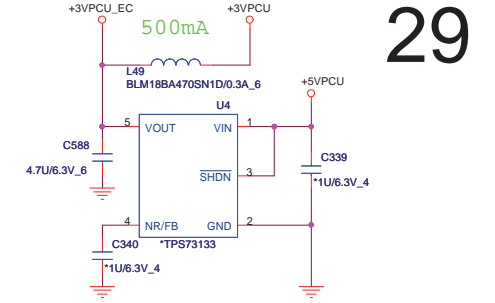
## 2M SPI EC ROM



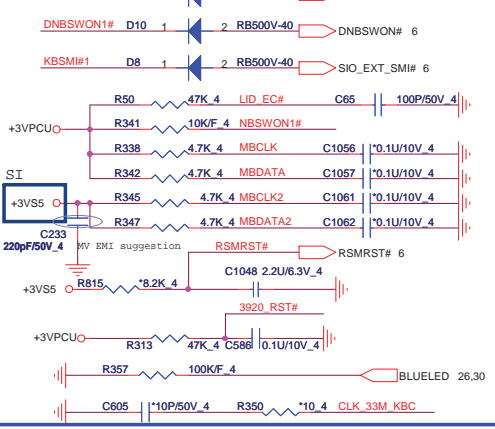
## 128K byte SPI EC ROM



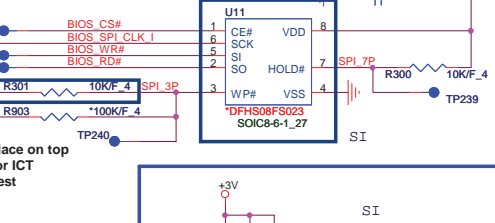
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q	Q̄



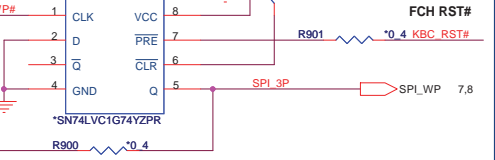
## Change to RB500 as Current loss



## 128K byte SPI EC ROM



## From EC

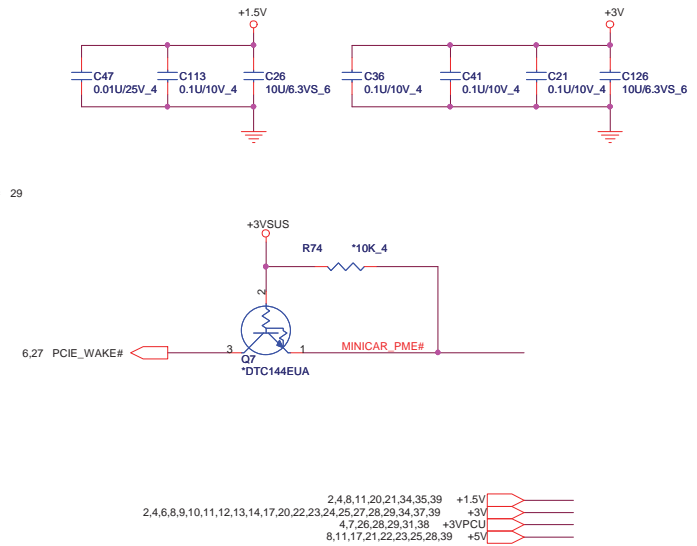
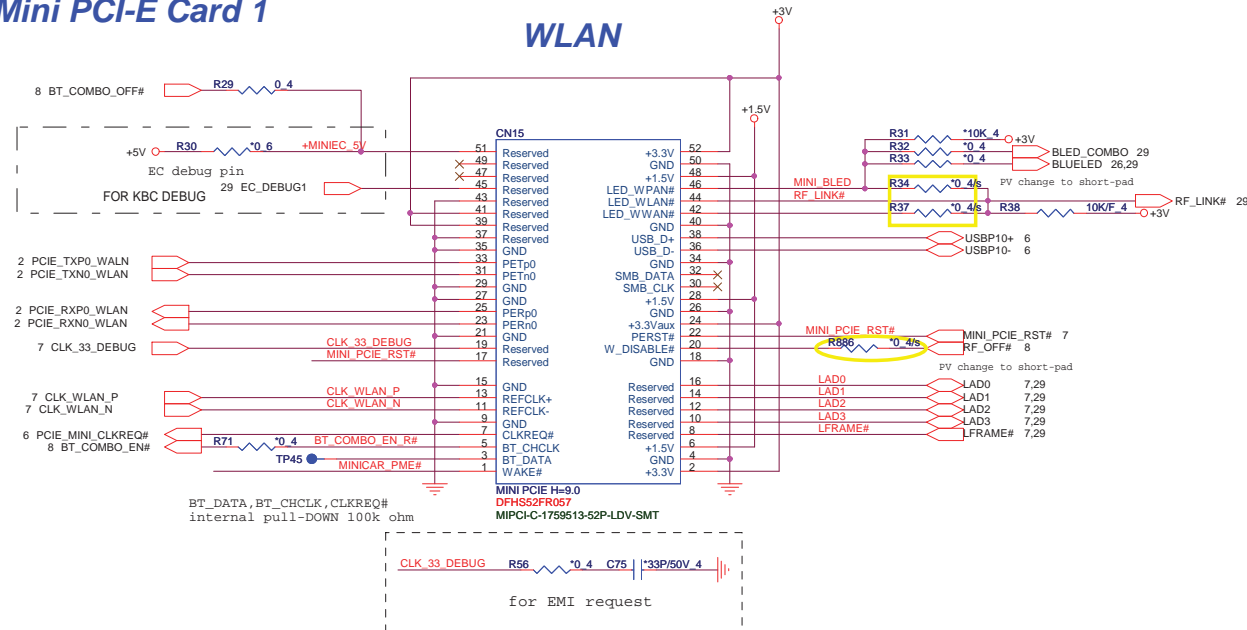


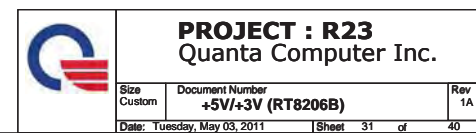
PROJECT : R23		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	EC (KB3926)ROM	1A
Date: Tuesday, May 03, 2011	Sheet 29 of 40	

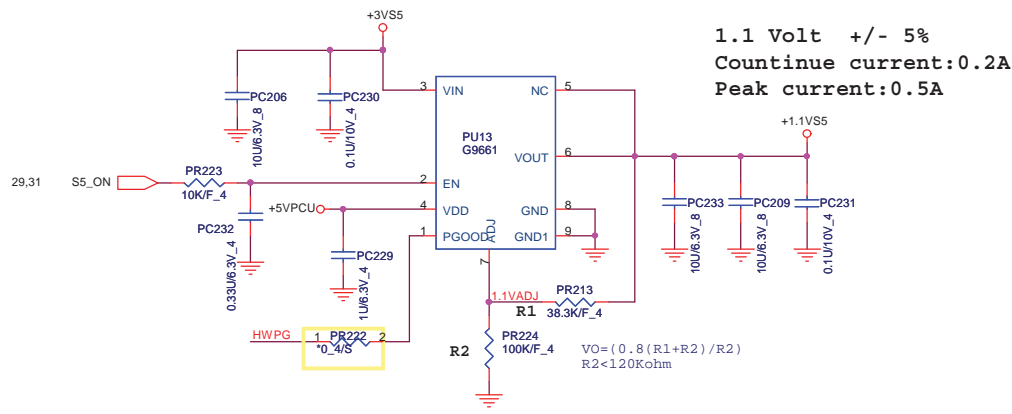
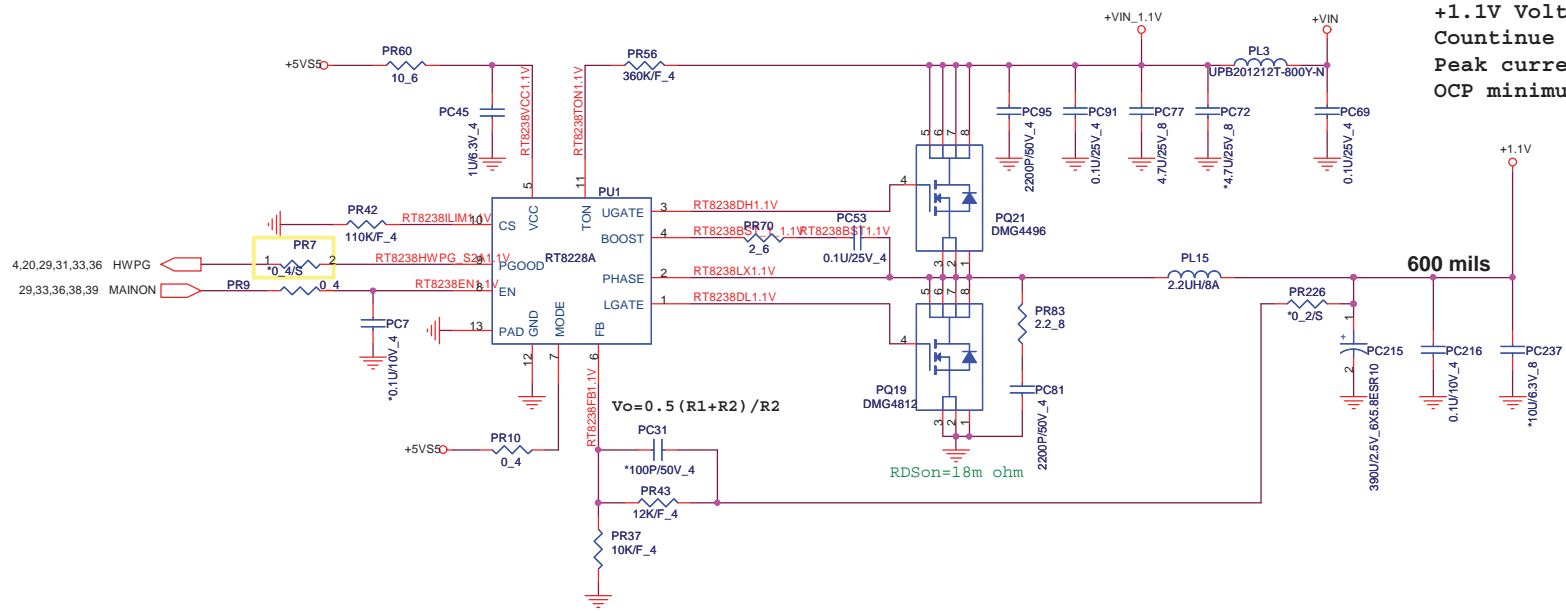


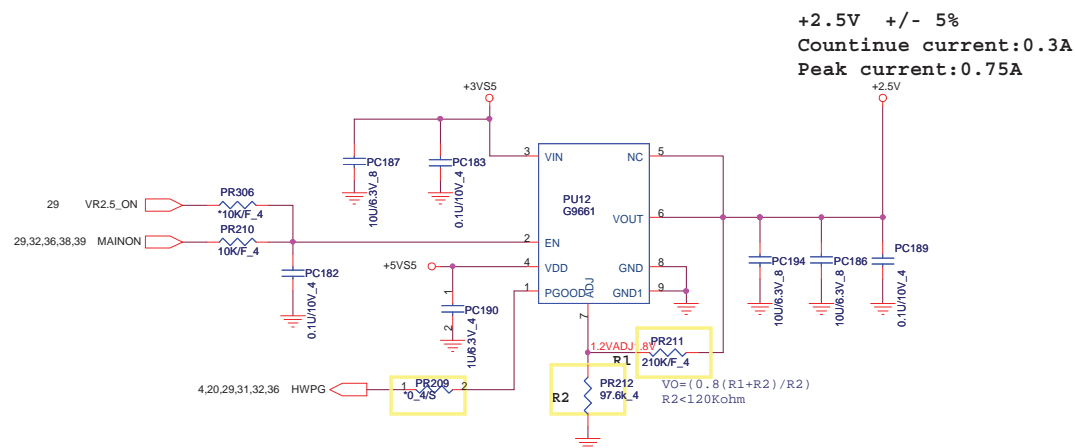
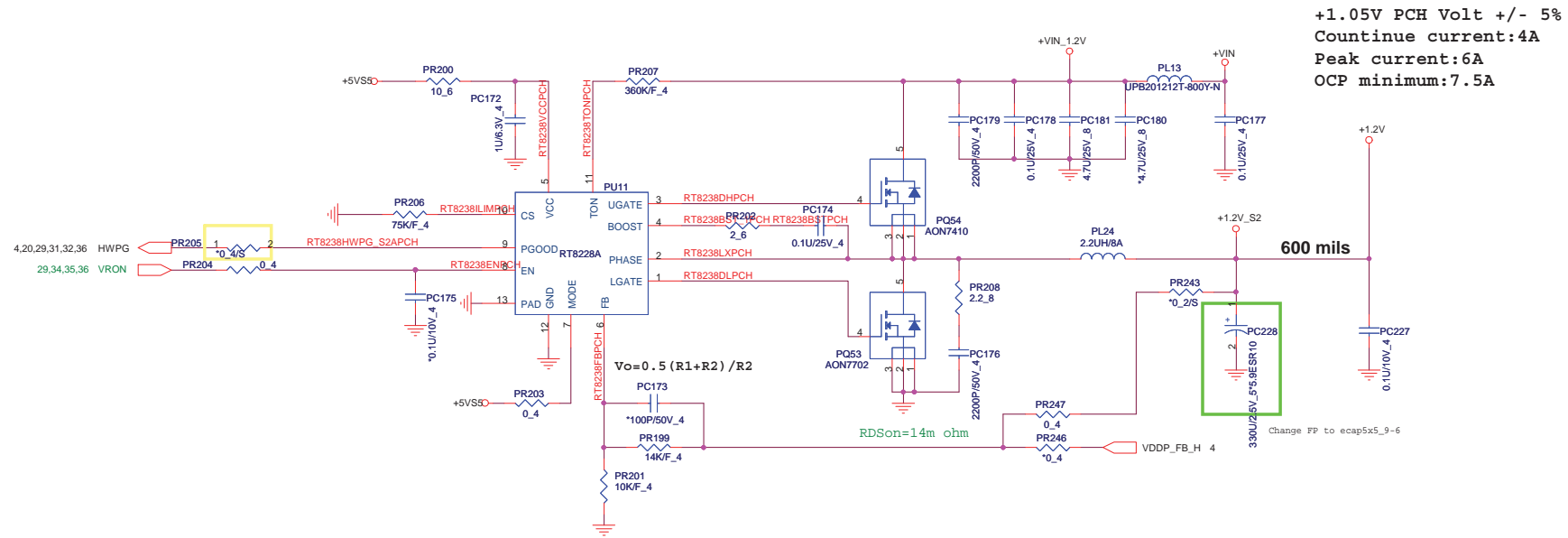
## Mini PCI-E Card 1

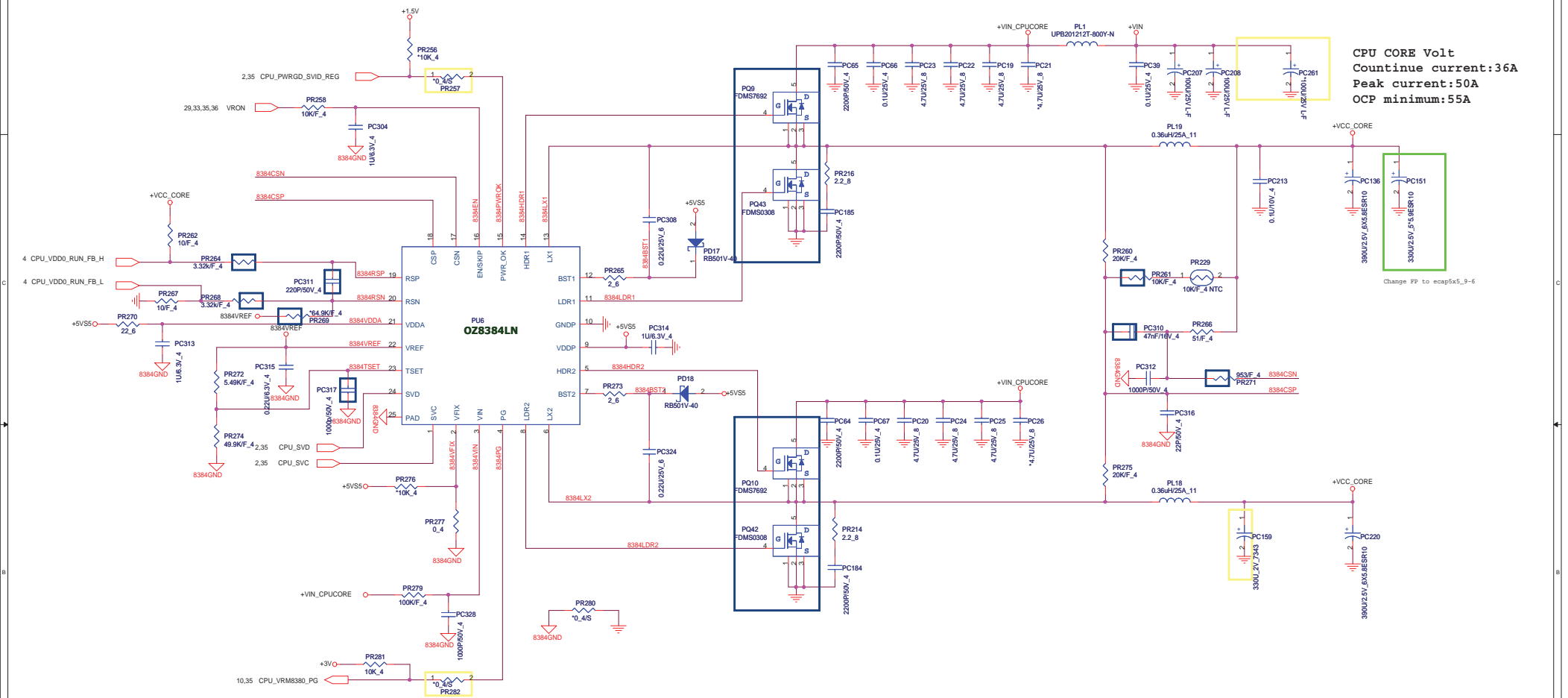
## WLAN

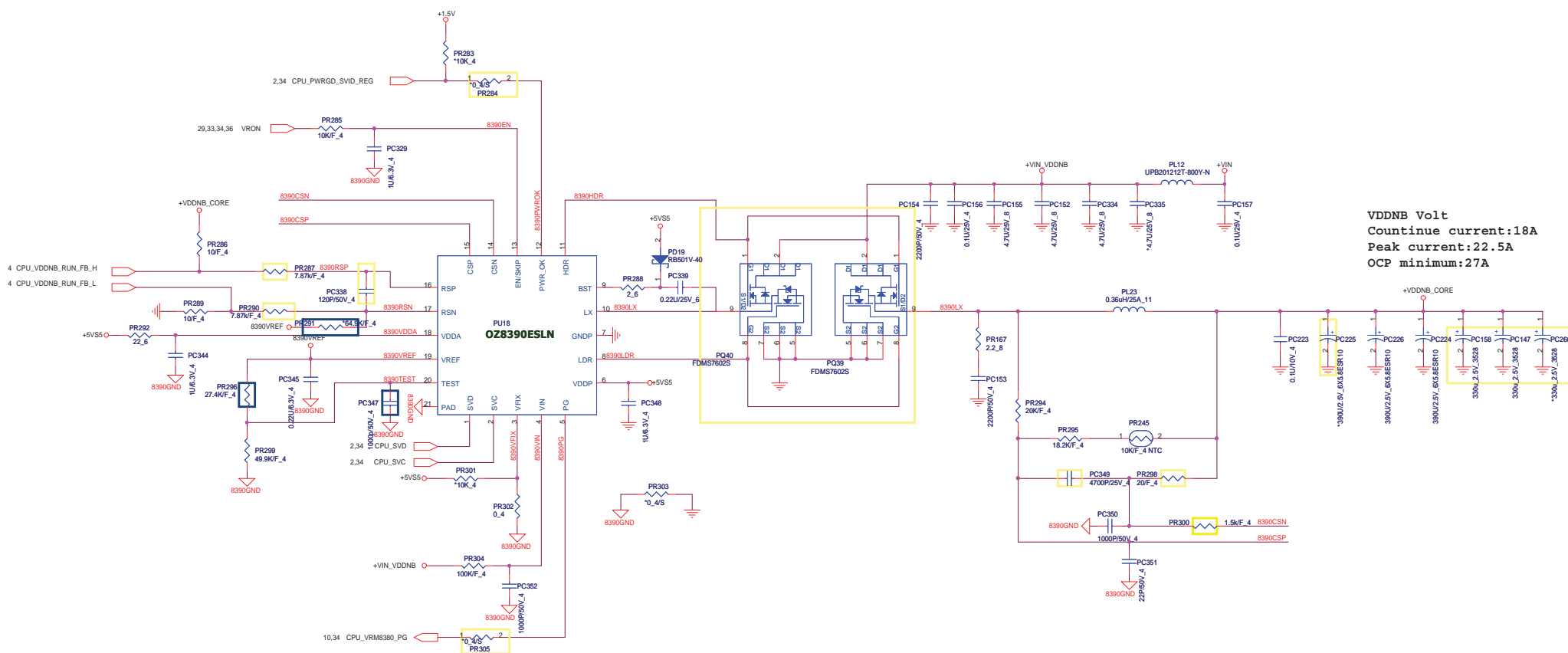






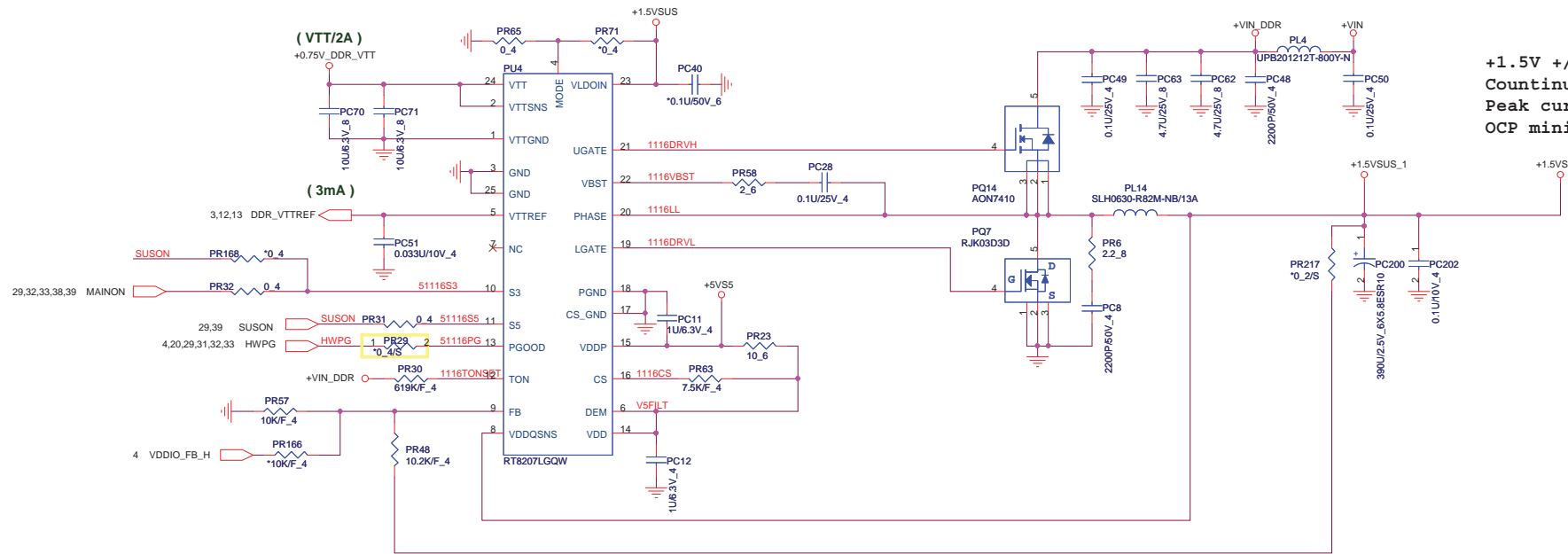






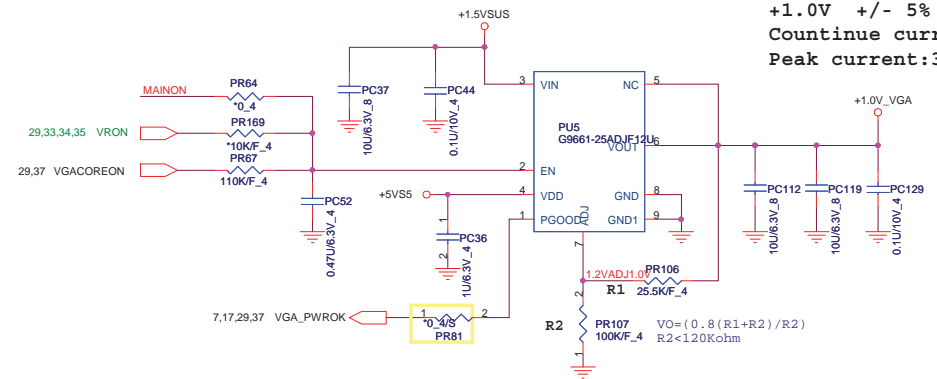


**+1.5V +/- 5%**  
**Countinue current:6A**  
**Peak current:12A**  
**OCp minimum 15A**

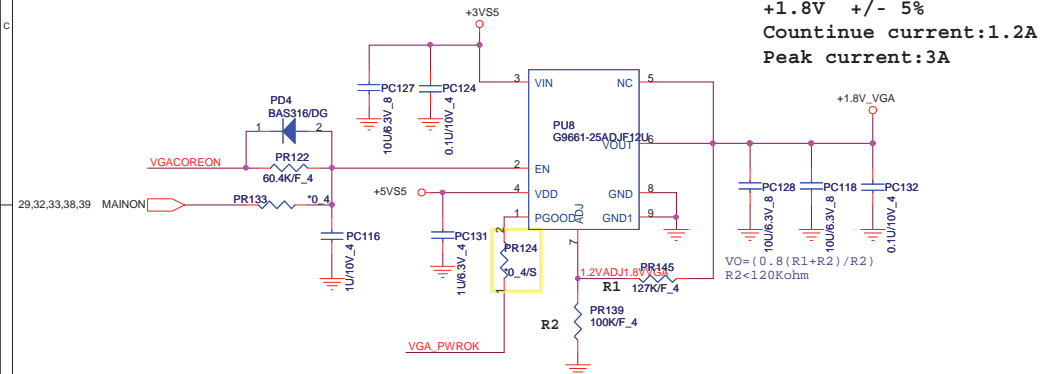


**SG & Discrete Only**

**+1.0V +/- 5%**  
**Countinue current:1.7A**  
**Peak current:3A**

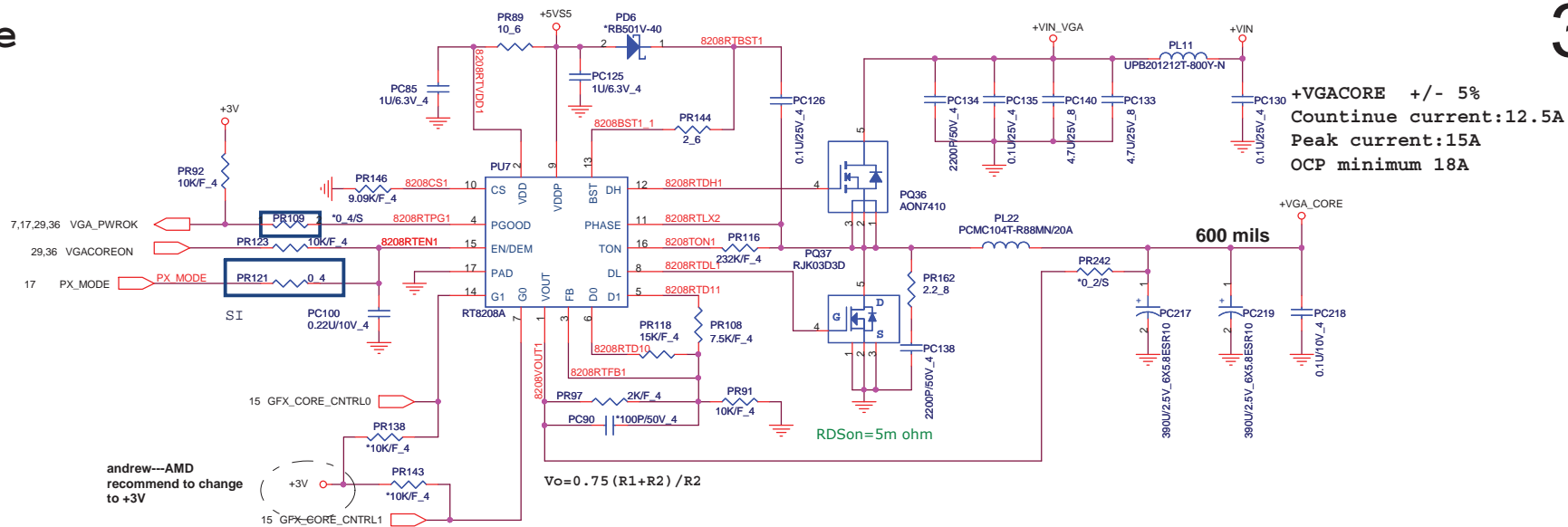


**+1.8V +/- 5%**  
**Countinue current:1.2A**  
**Peak current:3A**



# VGA Core

37



Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

