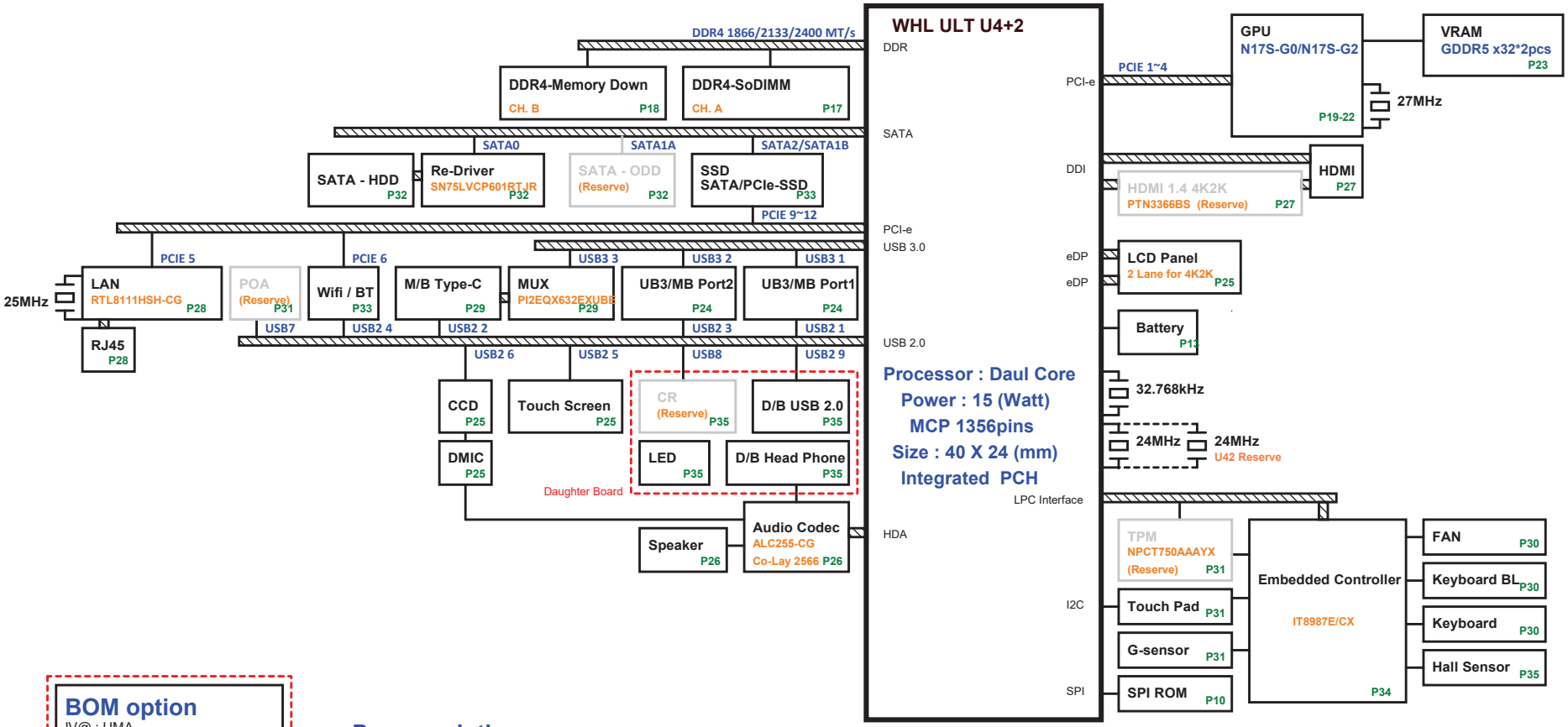
ZAW Whiskey Lake series Platform Block Diagram (DIS/UMA) 01



BOM option

IV@ : UMA
EV@ : DIS
TPC@ : Type-C function
TPC_N@ :No Type-C function
TSI@ : Touch screen I2C
TPM@ : Trusted Platform Module
PBA@ : Finger Print on touch pad
KBL@ : Keyboard back light
GS@ : G-Sensor function
GS_N@ : No G-Sensor function
SSD@ : Solid State Disk
ODD@ : Optical Disc Drive
EMC@ : eMMC function
RAM@ : On Board Memory
SP@ : Power & VGA
HDD_R@ : Hard Disc Redriver
HDD_N@ : NO Hard Disc Redriver
CNV@ : Intel WIFI
CNV_N@ :NO Intel WIFI
HDMI_R@ : HDMI Redirver
HDMI_N@ : No HDMI Redirver
Debug@ : for Debug Card
255@ : Codec 255
256@ : Codec 256
FOR15_17@ : Panel 15 or 17 inch
FOR14@ : Panel 14 inch

Power solution

Batery Charger BQ24780SRUYR P37	+VCC_CORE RT9610CGQW P42	+VGPU_CORE RT8813DGQW P46
+3VPCU/+5VPCU RT6258CGQUF P38	+VCCGT RT9610CGQW P43	+1.35V_GFX G5335QT2U P47
+3V/+5V JW7110DFNC P38	+VCCSA RT9610CGQW P43	+1V8_AON JW7110DFNC P48
+1V_S5 G5335QT2U P39	+1.8V_S5 JW5213DFND P44	+1.03_GFX G9336ADJTP1U P48
+1.2VSUS RT8231BGQW G9661MF11U P40	+1.5V JW5222RSOTB P44	Thermal protection TMP708AIDBVR P44

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: Block Diagram | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 1 of 48

+3V 4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,45,46
+VCCST 4,5,6

HDMI

U1A

27 IN_D2# → IN_D2# AL5 DDI1_TXN_0
27 IN_D2 → IN_D2 AL6 DDI1_TXP_0
27 IN_D1# → IN_D1# AJ5 DDI1_TXN_1
27 IN_D1 → IN_D1 AJ6 DDI1_TXP_1
27 IN_D0# → IN_D0# AF6 DDI1_TXN_2
27 IN_D0 → IN_D0 AF5 DDI1_TXP_2
27 IN_CLK# → IN_CLK# AE5 DDI1_TXN_3
27 IN_CLK → IN_CLK AE6 DDI1_TXP_3

AC4 DDI2_TXN_0
AC3 DDI2_TXP_0
AC1 DDI2_TXN_1
AC2 DDI2_TXP_1
AE4 DDI2_TXN_2
AE3 DDI2_TXP_2
AE1 DDI2_TXN_3
AE2 DDI2_TXP_3

EDP_TXN_0 AG4 INT_EDP_TXN0 → INT_EDP_TXN0 25
EDP_TXP_0 AG3 INT_EDP_TXP0 → INT_EDP_TXP0 25
EDP_TXN_1 AG2 INT_EDP_TXN1 → INT_EDP_TXN1 25
EDP_TXP_1 AG1 INT_EDP_TXP1 → INT_EDP_TXP1 25
EDP_TXN_2 AJ4 INT_EDP_TXN2 → INT_EDP_TXN2 25
EDP_TXP_2 AJ3 INT_EDP_TXP2 → INT_EDP_TXP2 25
EDP_TXN_3 AJ2 INT_EDP_TXN3 → INT_EDP_TXN3 25
EDP_TXP_3 AJ1 INT_EDP_TXP3 → INT_EDP_TXP3 25

EDP_AUX AH4 INT_EDP_AUXN → INT_EDP_AUXN 25
EDP_AUX_P AH3 INT_EDP_AUXP → INT_EDP_AUXP 25

DISP_UTILS AM7

DDI1_AUX AC7
DDI1_AUX_P AC6
DDI2_AUX AD4
DDI2_AUX_P AD3
DDI3_AUX AG7
DDI3_AUX_P AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_HPD_CON → HDMI_HPD_CON 27
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 PCH_TypeC_UPFb# → PCH_TypeC_UPFb# 29
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 R25448 *Short_0402 SIO_EXT_SCI# → SIO_EXT_SCI# 34
GPP_E17/EDP_HPD/DISP_MISC4 CM7 ULT_EDP_HPD → ULT_EDP_HPD 25

EDP_BKLTEN CK11 PCH_LVDS_BLON → PCH_LVDS_BLON 25
EDP_VDDEN CG11 PCH_DISP_ON → PCH_DISP_ON 25
EDP_BKLTCTL CH11 PCH_DPST_PWM → PCH_DPST_PWM 25

+3V → R25436 20K_1%_2 → SIO_EXT_SCI#

DISP_RCOMP signals should be shorted near balls and routed with typical impedance <20 mohms

+VCCIO → R2 24.9_1%_4 → EDP_RCOMP AM6 DISP_RCOMP

27 SDVO_CLK CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
27 SDVO_DATA CC9 GPP_E19/DPPB_CTRLDATA

CH4 GPP_E20/DPPC_CTRLCLK
CH3 GPP_E21/DPPC_CTRLDATA

CP4 GPP_E22/DPPD_CTRLCLK
CN3 GPP_E23/DPPD_CTRLDATA

CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

WHL_U_43E_IL_IP_DDR4
1 of 20

Type C change
+3V_S5 → PCH_TypeC_UPFb# R202 20K_1%_2

checklist REV 2.0 : PD 20K

Reserve EDP_HPD opposites circuit!

+3V → R10880 *10K_1%_2 → ULT_EDP_HPD → R1 100K_5%_4

PCH_DPST_PWM
PCH_LVDS_BLON
SPEC:0.033u
SCH:0.47u
C1 0.033u/16V_4
C2 *0.033u/16V_4
close SOC

JTAG_TDI_PCH R3 *Short_0201 XDP_TDI_CPU
JTAG_TDO_PCH R4 *Short_0201 XDP_TDO_CPU
JTAG_TMS_PCH R5 *Short_0201 XDP_TMS_CPU
XDP_TRST#_CPU R6 *Short_0201 PROC_TRST#
JTAGX_PCH R7 *Short_0201 XDP_TCK0
DCI Debug

U1D

+VCCST → R10 49.9_1%_2 CATERR#
+VCCST → R11 *1K_5%_2 JTAGX_PCH
R12 51_5%_2 JTAG_TMS_PCH
R13 51_5%_2 JTAG_TDI_PCH
R14 100_1%_2 JTAG_TDO_PCH
R17 *51_5%_2 JTAG_TCK_PCH
Close to Chipset

34,36,40 H_PROCHOT# → R9 499_1%_2 → THERMTRIP# R25479 *Short_0402 THERMTRIP#_CPU
C6618 0.1u/6.3V_2

CATERR# AA4 CATERR#
EC_PECI AR1 PECI
PROCHOT# Y4 PROCHOT#
THERMTRIP# BJ1 THERMTRIP#

34 EC_PECI
16 XDP_BPM0 → U1 BPM#_0
16 XDP_BPM1 → U2 BPM#_1
U3 BPM#_2
U4 BPM#_3

PROC_TCK T6 XDP_TCK0 → XDP_TCK0 16
PROC_TDI U6 XDP_TDI_CPU
PROC_TDO Y5 XDP_TDO_CPU
PROC_TMS T5 XDP_TMS_CPU
PROC_TRST# AB6 PROC_TRST#

PCH_TCK W6 JTAG_TCK_PCH → JTAG_TCK_PCH 16
PCH_TDI U5 JTAG_TDI_PCH
PCH_TDO W5 JTAG_TDO_PCH
PCH_TMS P5 JTAG_TMS_PCH
PCH_TRST# Y6 XDP_TRST#_CPU
PCH_JTAGX P6 JTAGX_PCH

CE9
CN3
14 DGPU_PW_CTRL# → CB34 GPP_E3/CPU_GP0
CC35 GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

PROC_PREQ# W2 XDP_PREQ#_CPU 16
PROC_PRDY# W1 XDP_PRDY#_CPU 16

R16 49.9_1%_2 PROC_POPIRCOMP BP27
R18 49.9_1%_2 PCH_OPI_RCOMP BW25
R20 49.9_1%_2 EDRAM_OPIO_RCOMP L5
R21 49.9_1%_2 EOPIO_RCOMP N5
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

4 of 20
WHL_U_43E_IL_IP_DDR4

PLACE NEAR CPU
+VCCST
XDP_TMS_CPU R15 *51_5%_2
XDP_TDI_CPU R19 51_5%_2
XDP_TDO_CPU R22 100_1%_2

+VCCIO
H_PROCHOT# R23 1K_5%_2
XDP_TCK0 R24 51_5%_2
XDP_TRST#_CPU R25 *51_5%_2

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

+VCCST
4,40 IMVP_PWRGD → Q85 DMG301NU-7
R825 *100K_1%_4
R821 1K/F_4
R822 1K/F_4
Q86
34,37,43 SYS_SHDN# → THERMTRIP#
METR3904-G

Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 1/15 eDP/DDI/MISC	1A

Date: Wednesday, February 27, 2019 Sheet 2 of 48

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

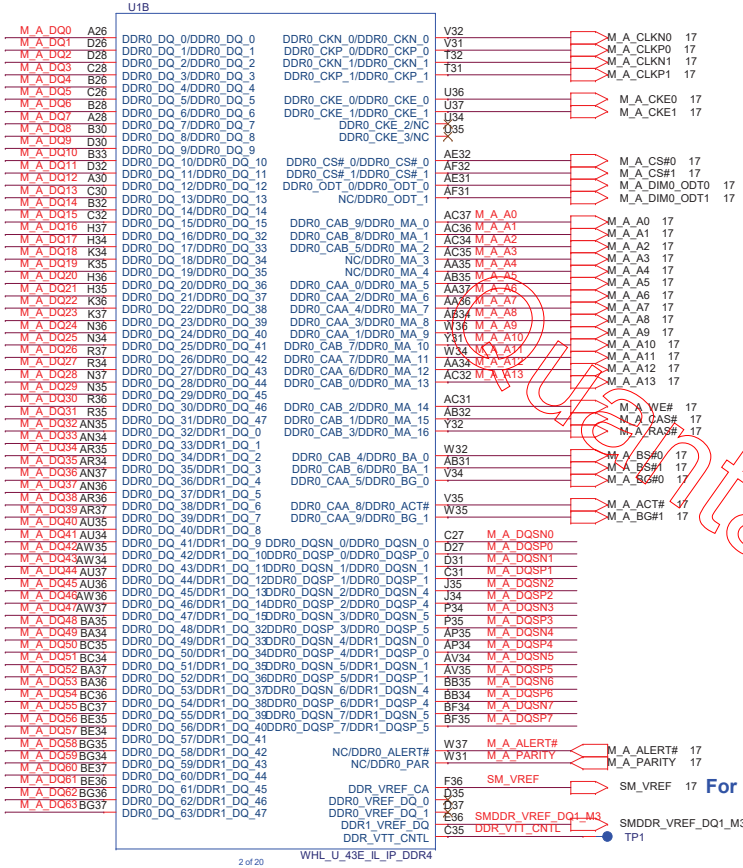
+3V_DEEP_SUS 4,10,11,13,14,15

WHL ULT Processor (DDR4)

03

WHL ULT Processor (MEM-A)

Interleave / Non-Interleave

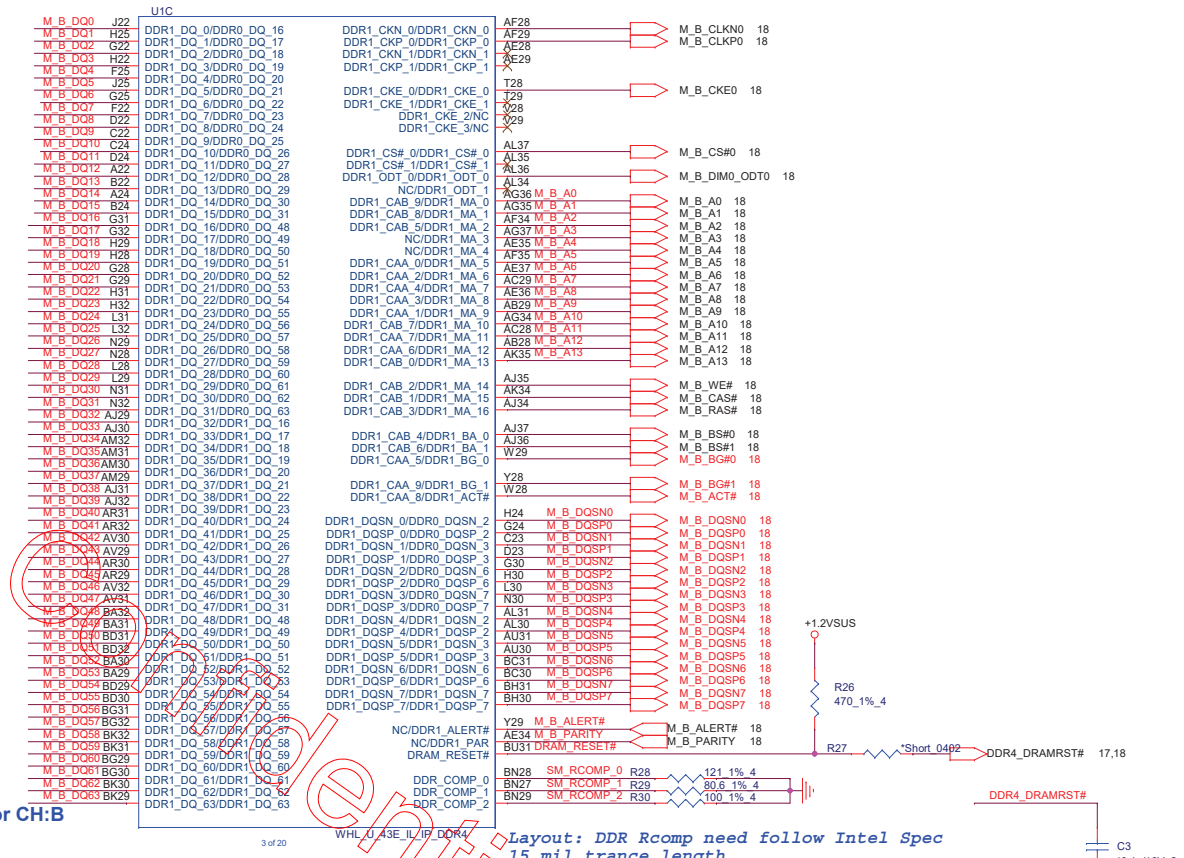


For CH:A

For CH:B

WHL ULT Processor (MEM-B)

Interleave / Non-Interleave



Layout: DDR Rcomp need follow Intel Spec 15 mil trance length

Quanta Computer Inc.

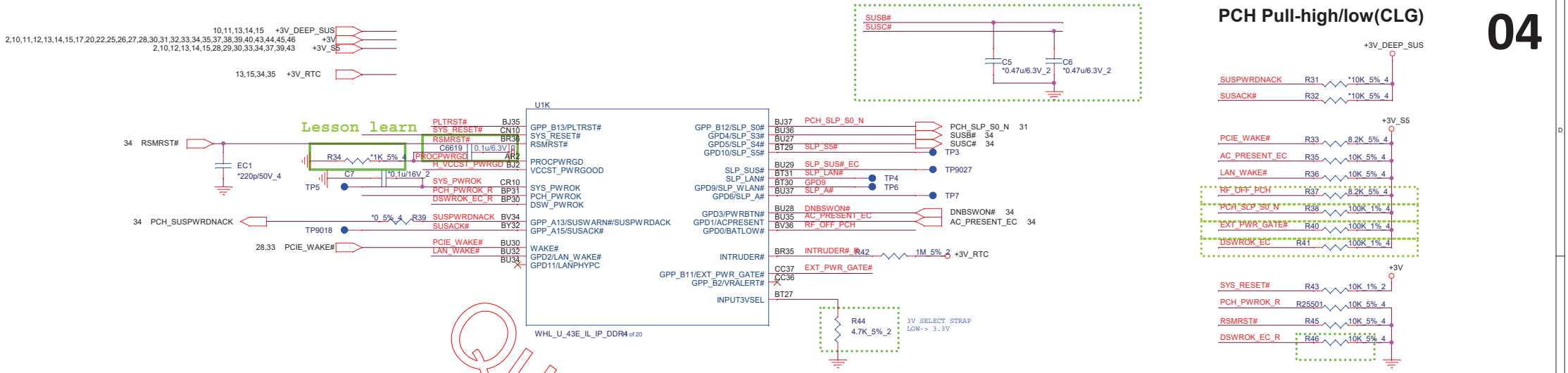
PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 2/15(DDR4 I/F)	1A

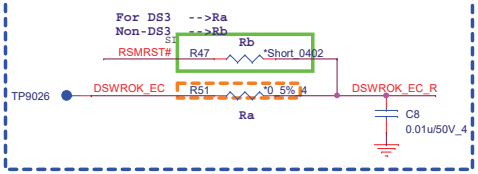
Date: Wednesday, February 27, 2019 Sheet 3 of 48

PCH Pull-high/low(CLG)

04

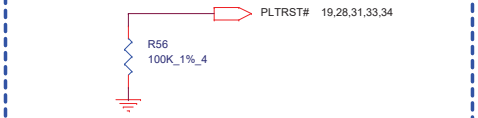


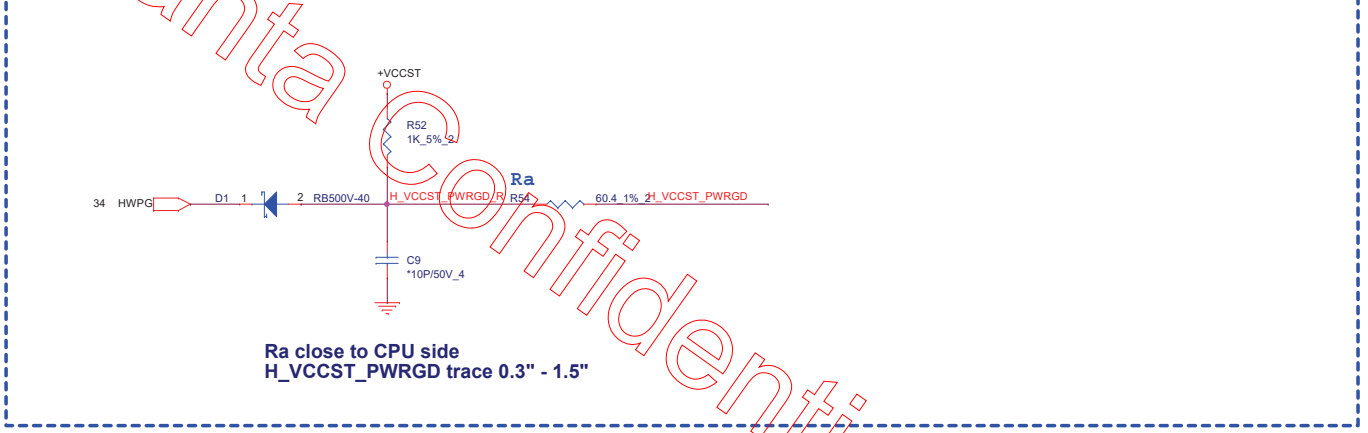
For DS3 Sequence



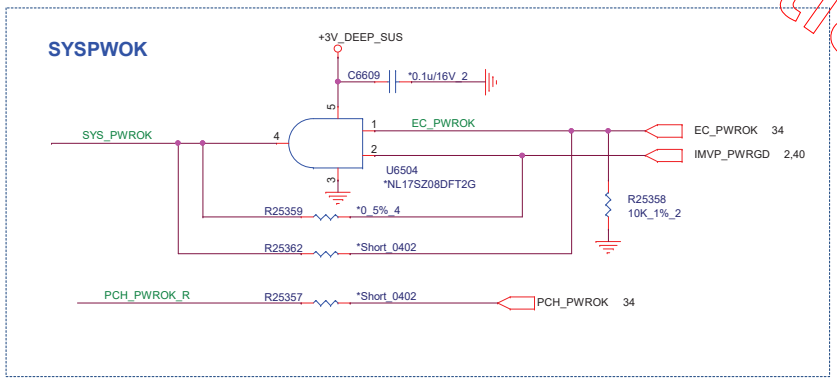
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

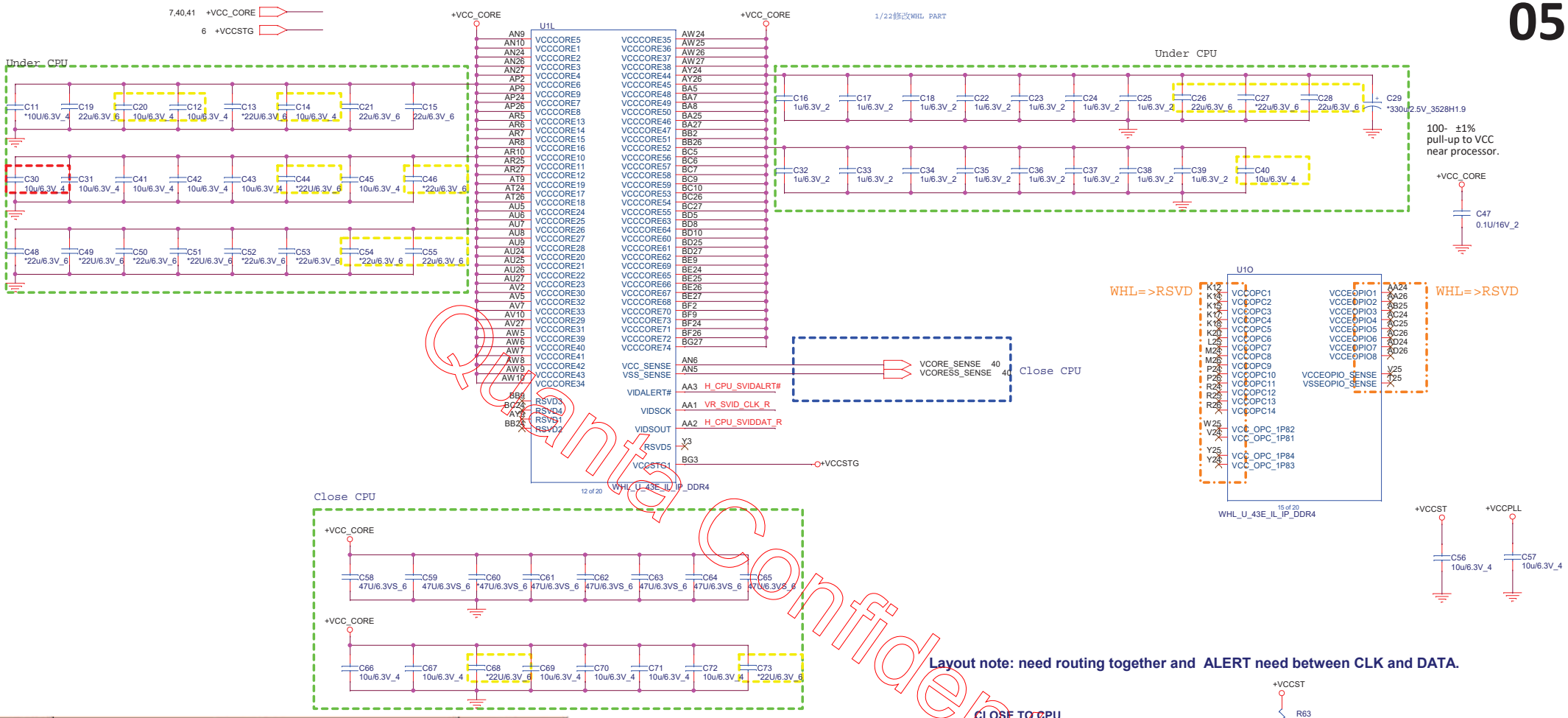




SYSPWOK



Quanta Computer Inc.		
PROJECT : ZAW		
Size	Document Number: KBL-U 3/15(PowerManger)	Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 4 of 48	

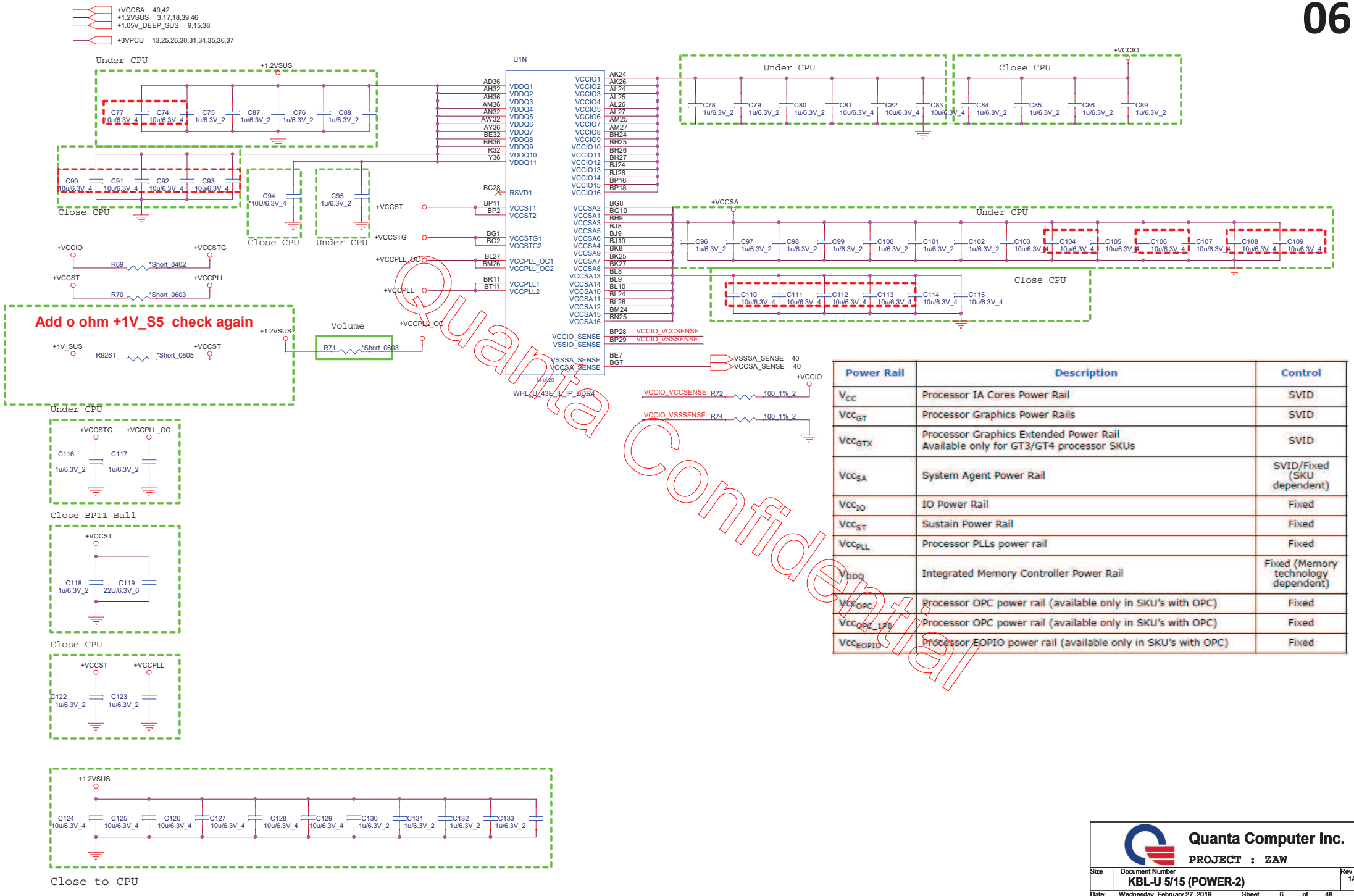


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT : ZAW

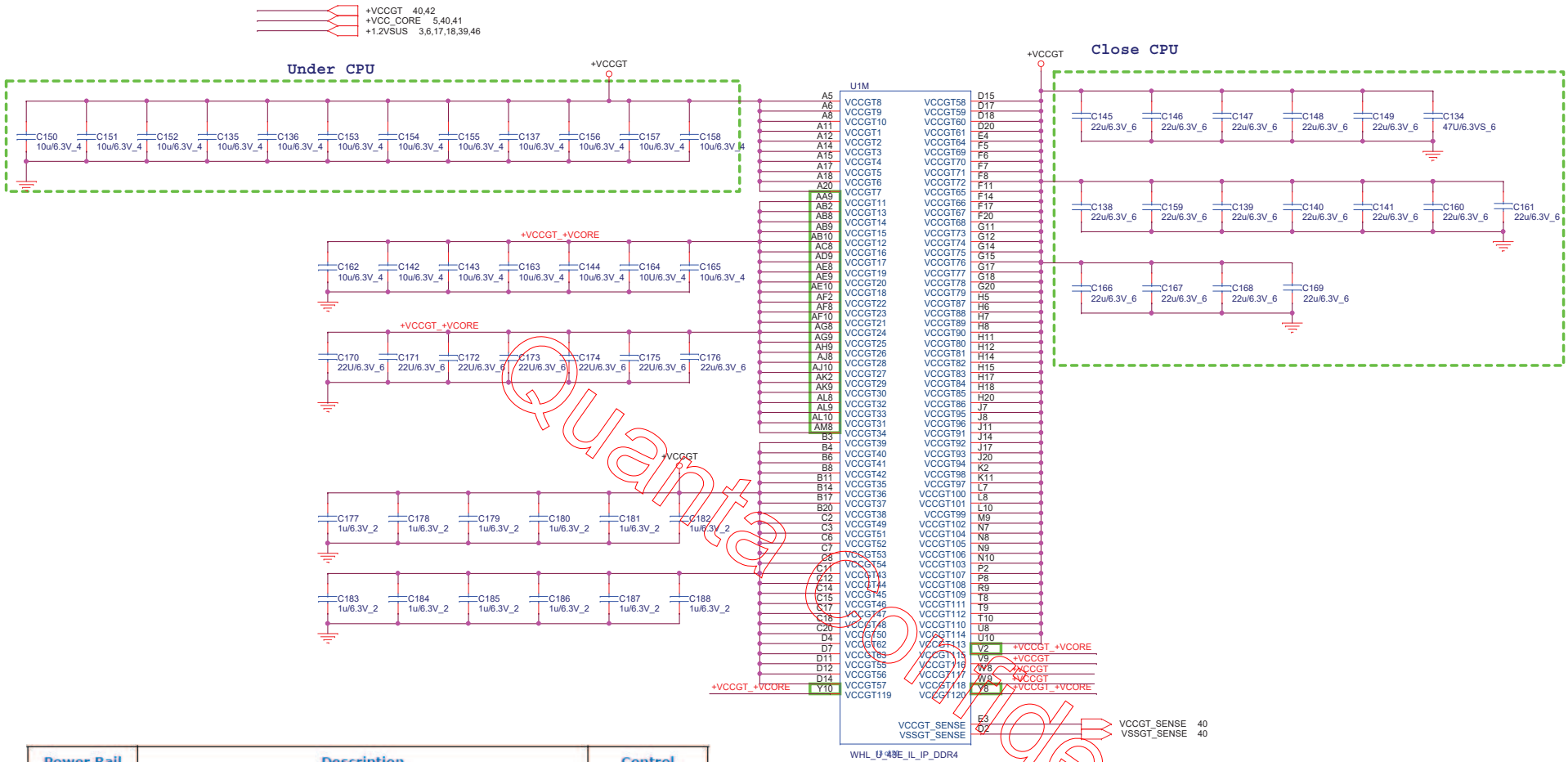
Size	Document Number	Rev
	KBL-U 4/15 (POWER-1)	1A

Date: Wednesday, February 27, 2019 Sheet 5 of 48



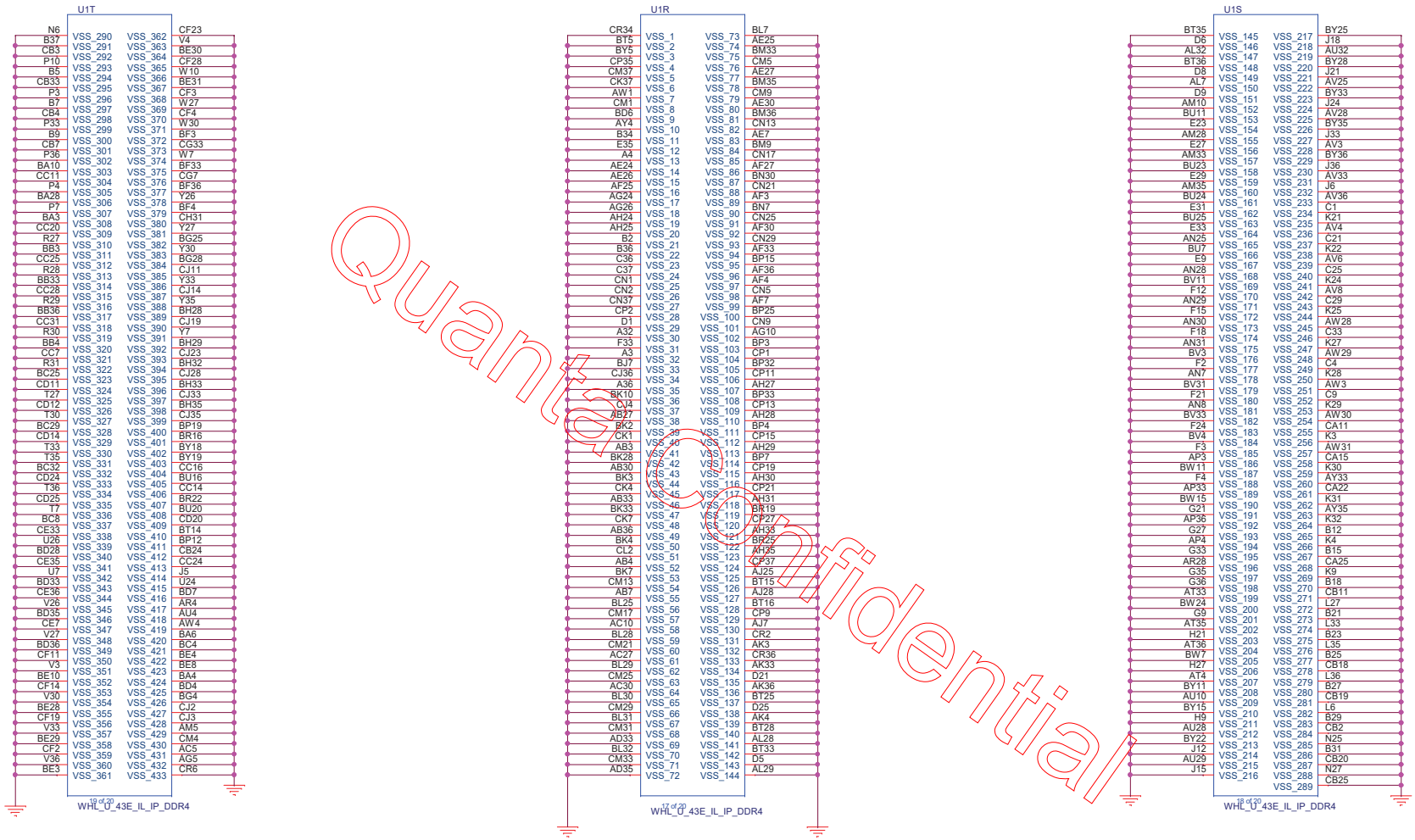
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: KBL-U 5/15 (POWER-2) | Rev: 1A
Date: Wednesday, February 27, 2019 | Sheet 6 of 48



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: KBL-U 6/15 (POWER-3) | Rev: 1A
Date: Wednesday, February 27, 2019 | Sheet 7 of 48



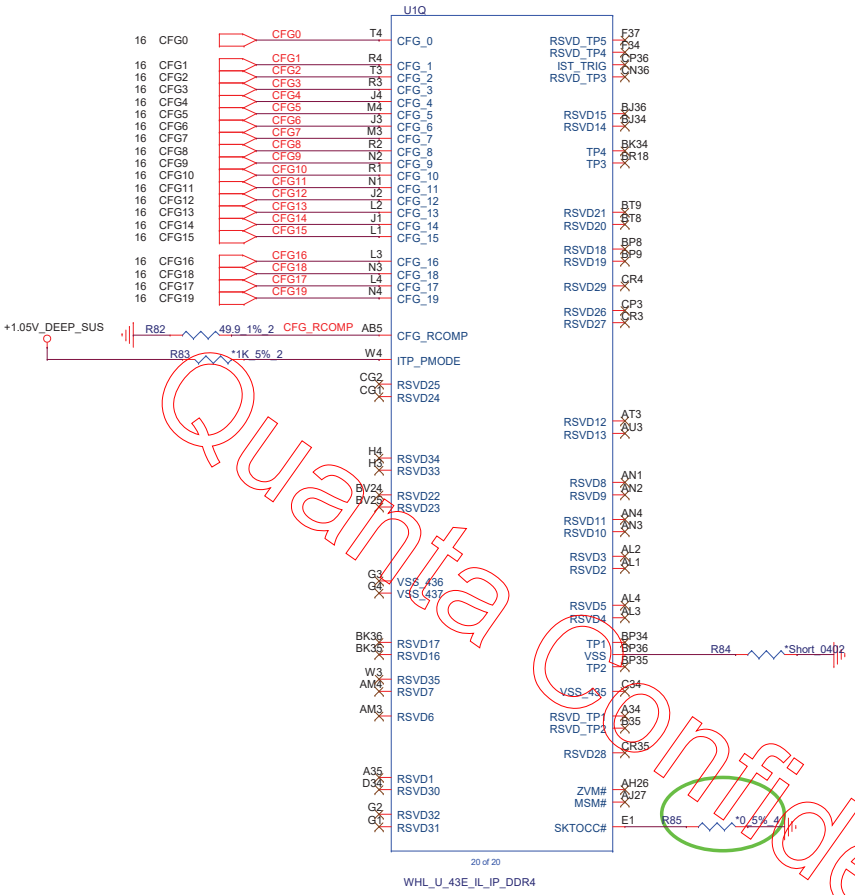
Quanta Computer Inc.

PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 7/15 (GND)	1A

Date: Wednesday, February 27, 2019 Sheet 8 of 48

+1.05V_DEEP_SUS 15,38



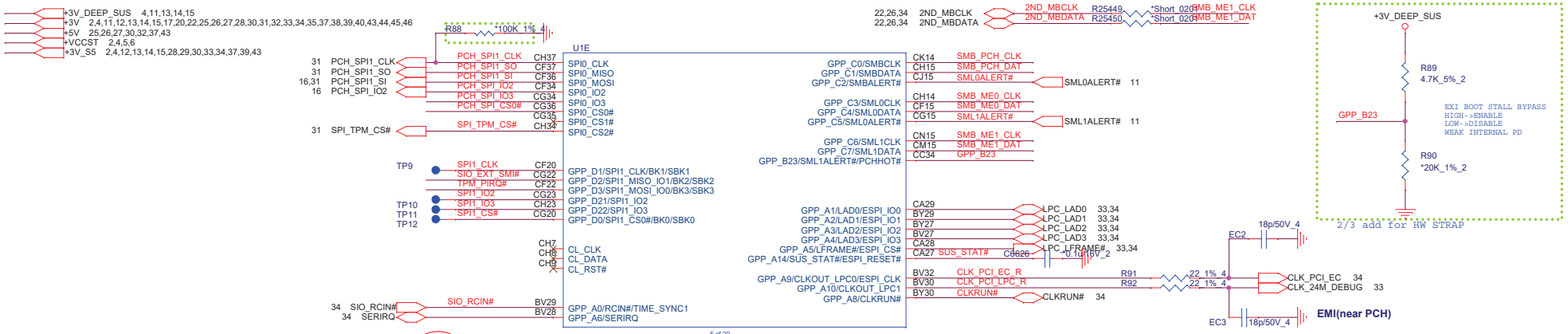
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R86 *1K_5%_2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R87 1K_5%_2

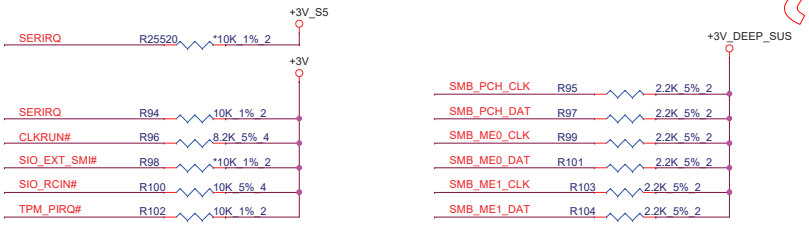
Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 8/15 (RSV)	1A

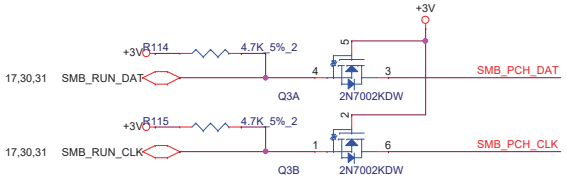
Date: Wednesday, February 27, 2019 Sheet 9 of 48



GPIO Pull UP



SMBus/Pull-up(CLG)



CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

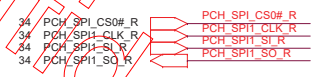
PCH SPI ROM(CLG)

Vender		Size	P/N	
Kabylake POA 3.3V	MXIC	16M	AKE3DZN0Z03	MX25L12873FM2I-10G
	Winbond	16M	AKE3DF-KN01	W25Q128JVSIQ
	GigaDevice	16M	AKE3DZN0Q02	GD25B127DSIGR

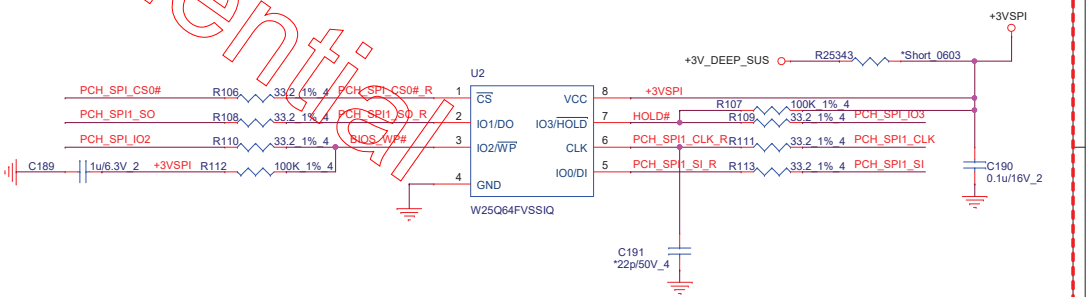
need place to TOP

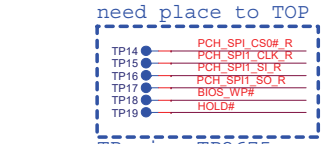
TP14 PCH_SPI_CS0#_R
TP15 PCH_SPI1_CLK_R
TP16 PCH_SPI1_SI_R
TP17 PCH_SPI1_SO_R
TP18 BIOS_WP#
TP19 HOLD#

TP size TP2675



PCH SPI ROM(CLG)





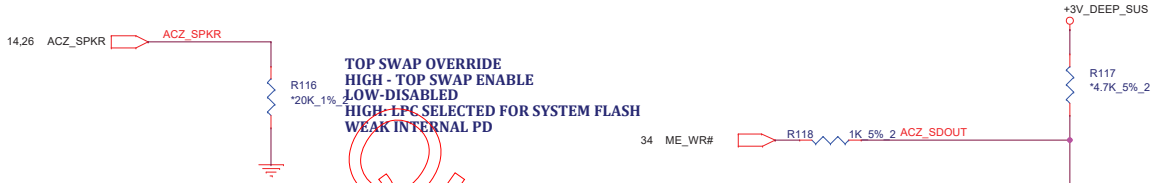
Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 09/15(SPI/LPC/SM)	1A

Date: Wednesday, February 27, 2019 Sheet 10 of 48

Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

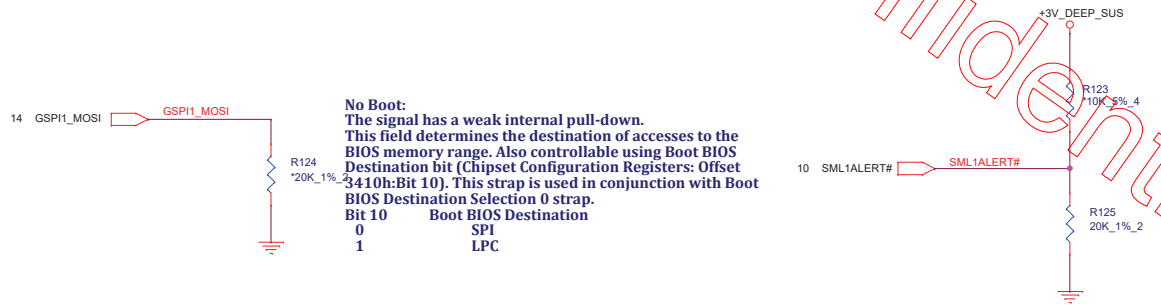


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

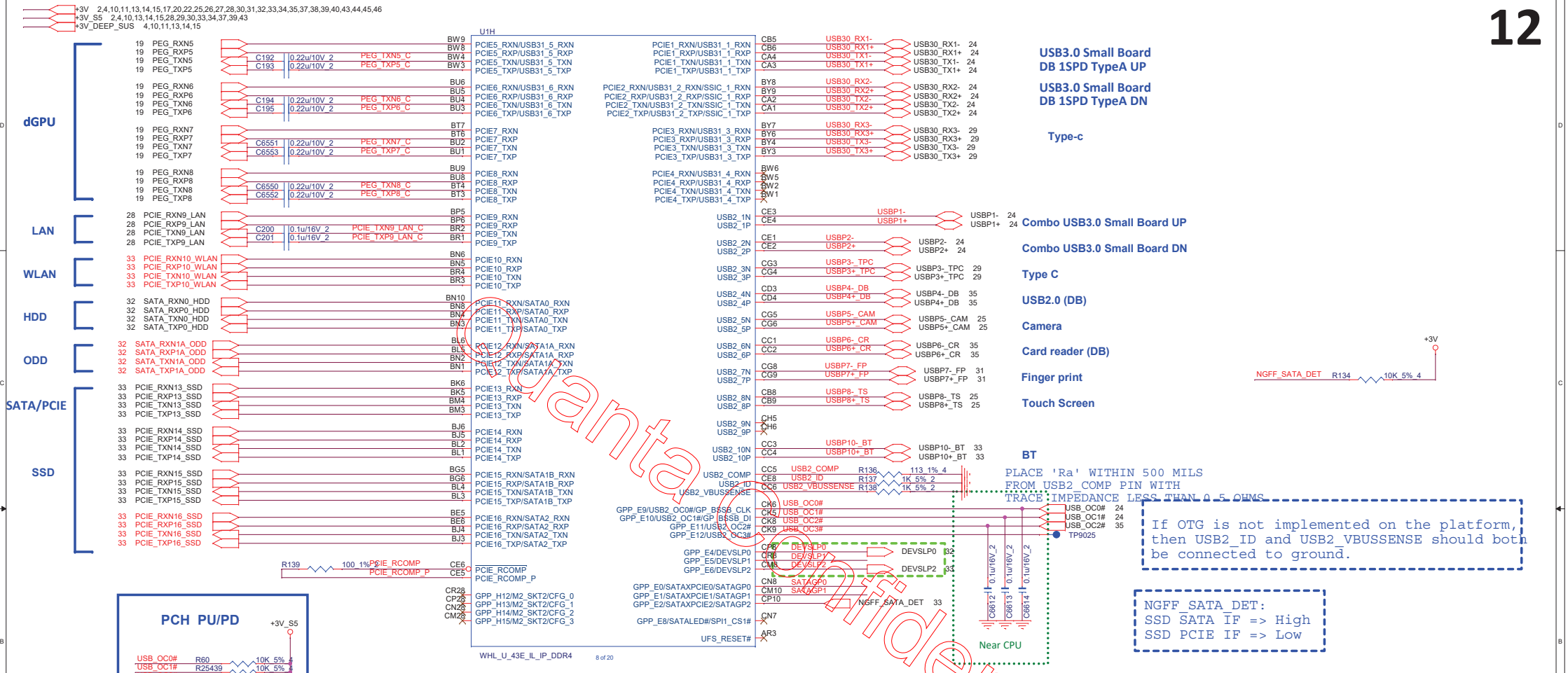
No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC

No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



USB3.0 Small Board
DB 1SPD TypeA UP

USB3.0 Small Board
DB 1SPD TypeA DN

Type-c

Combo USB3.0 Small Board UP

Combo USB3.0 Small Board DN

Type C

USB2.0 (DB)

Camera

Card reader (DB)

Finger print

Touch Screen

BT

PLACE 'Ra' WITHIN 500 MILS
FROM USB2_COMP PIN WITH
TRACE IMPEDANCE LESS THAN 0.5 OHMS

If OTG is not implemented on the platform, then USB2_ID and USB2_VBUSSENSE should both be connected to ground.

NGFF_SATA_DET:
SSD SATA IF => High
SSD PCIE IF => Low

SATAGP1:GPP_E1 - SATA#1/PCIE#8
SATA => High < Base U>
PCIE => Low

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port5	dGPU	Port0	VGA
Port6	dGPU	Port1	SSD
Port7	dGPU	Port2	Un-used
Port8	dGPU	Port3	Un-used
Port9	LAN	Port4	LAN
Port10	WLAN	Port5	WLAN
Port11	HDD		
Port12	ODD		
Port13	PCIE SSDx4		
Port14	PCIE SSDx4		
Port15	PCIE SSDx4		
Port16	PCIE SSDx4 /SATA SSD		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 Type A
PORT-2	USB3.0 Type A
PORT-3	Type C
PORT-4	NC

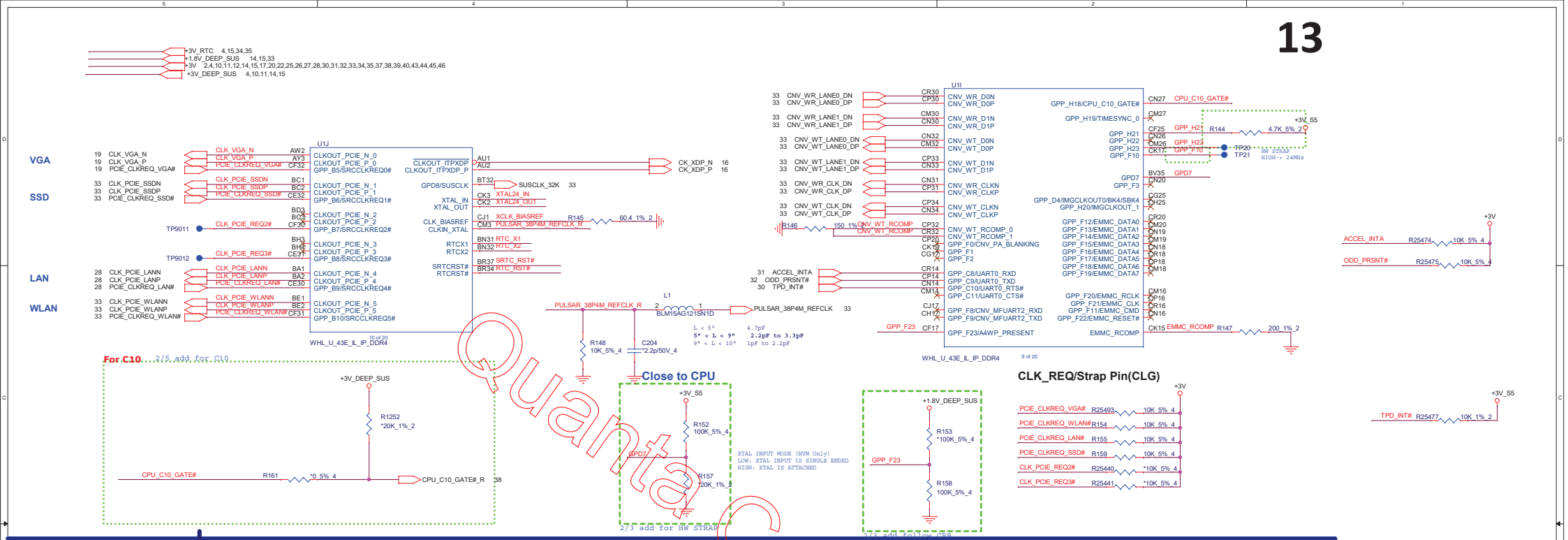
USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 Type A
PORT-2	Cobime USB3.0 Type A
PORT-3	Type C
PORT-4	USB 2.0 Small board
PORT-5	Camera
PORT-6	Card reader
PORT-7	Finger Print
PORT-8	Touch Screen
PORT-9	NC
PORT-10	BT (CNVI)

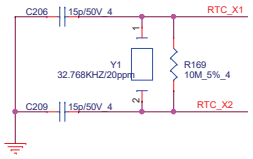
Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	WHL-U 11/15 (PCIE/USB)	1A

Date: Wednesday, February 27, 2019 Sheet 12 of 48

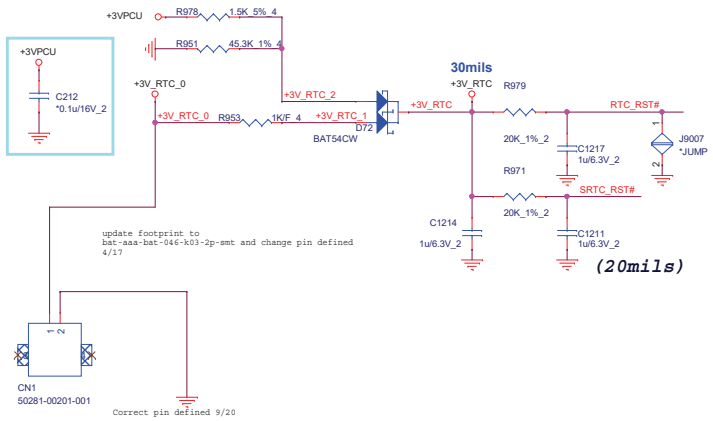


RTC Clock 32.768KHz

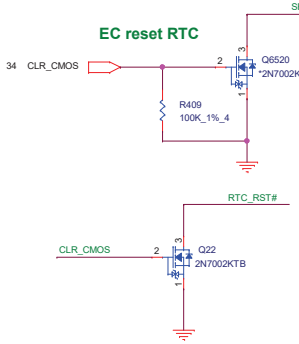


RTC Circuitry(RTC)

RTC Power trace width 20mils.

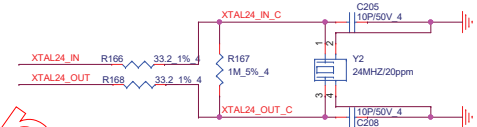


EC reset RTC



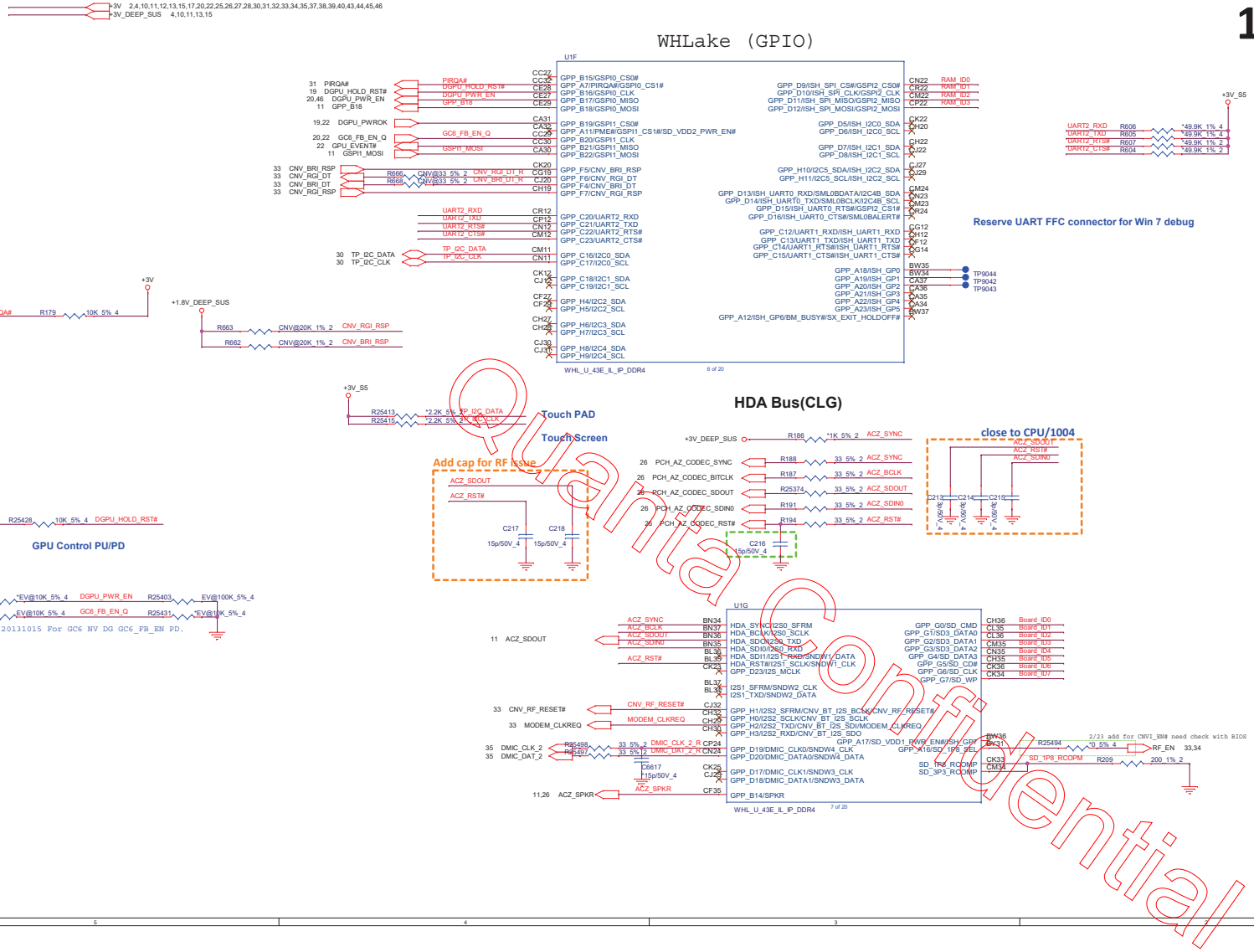
External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

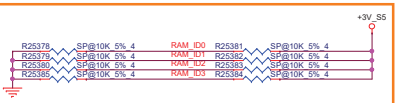


Quanta Computer Inc.			
PROJECT : ZAW			
Size	Document Number		Rev
	KBL-U 12/15 (CLK/EMMC)		1A
Date: Wednesday, February 27, 2019	Sheet 13	of 48	

WHLake (GPIO)

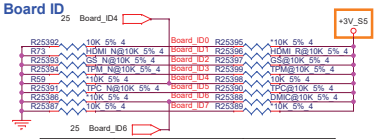


RAM ID

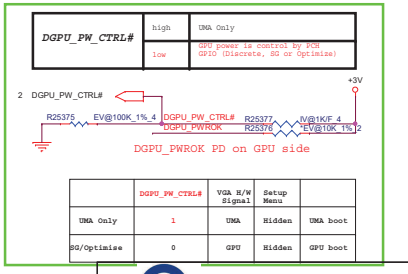


ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	Hynix 8Gb	H5AN8G6NCJR-VKC	AKD5QGSTW13
0	0	0	1	Micron 8Gb	MT40A512M16LY-075:E	AKD5LZSTL24
0	0	1	0	Micron 8Gb	MT40A512M16TB-062E:J	AKD5QGSTL23
1	1	1	1	With out on board memory		

Board ID

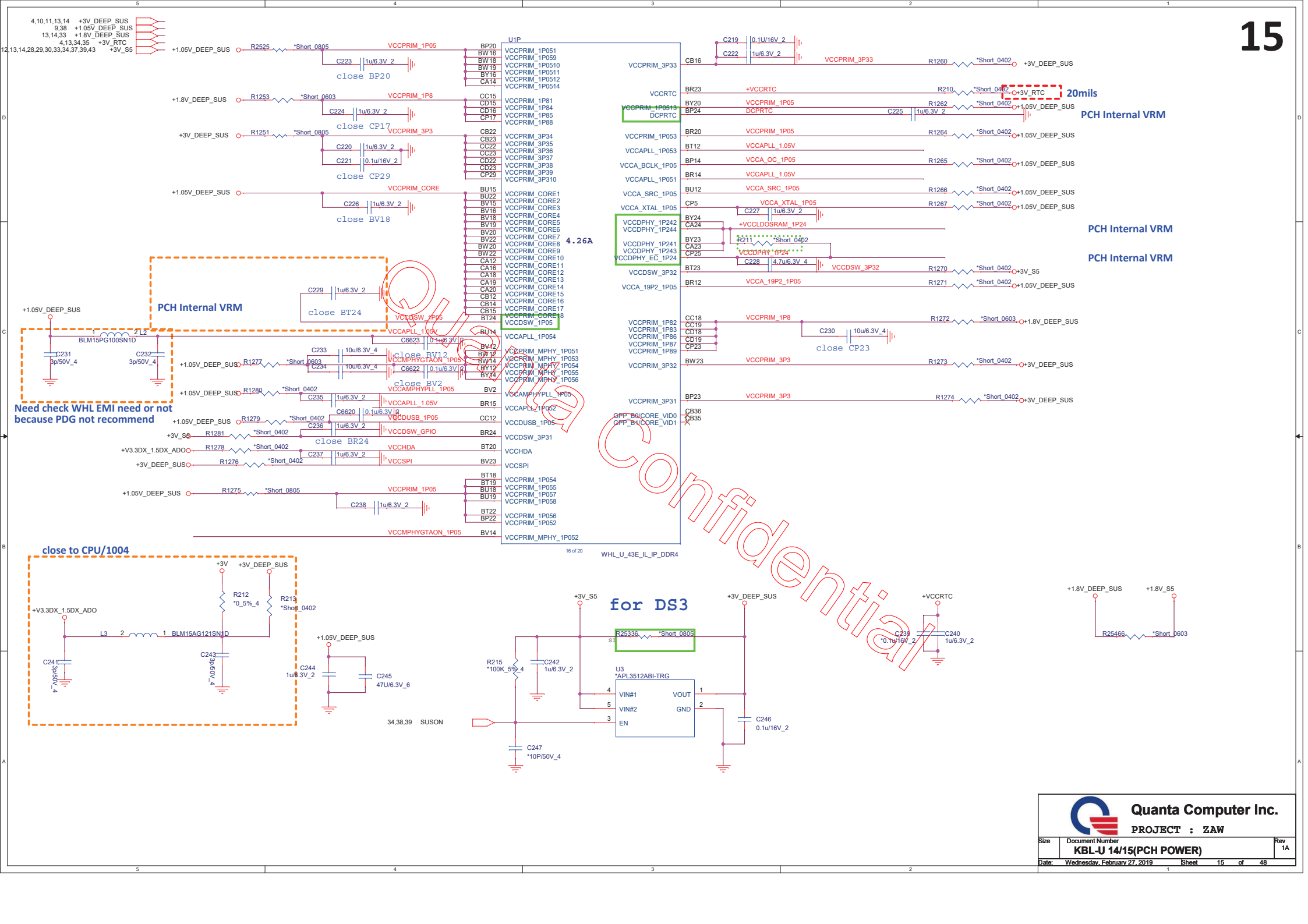


	Low	High
BOARD_ID0	Non eMMC	eMMC
BOARD_ID1	HDMI_N@	HDMI_R@
BOARD_ID2	Non G-sensor(GS_N@)	G-sensor(GS@)
BOARD_ID3	Non TPM(TPM_N@)	TPM(TPM@)
BOARD_ID4	Non Touch panel	Touch panel (Control by Cable)
BOARD_ID5	Non Type-C(TPC_N@)	Type-C(TPC@)
BOARD_ID6	Single MIC(Cable control)	Dual MIC (DMIC@)
BOARD_ID7	Reserved (Default)	Reserve



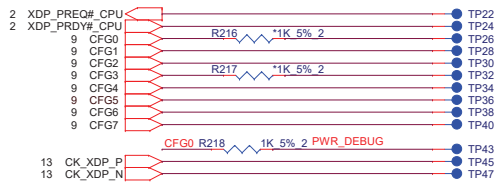
	DGPU_PW_CTRL#	VGA H/W Signal	Setup Menu	
UMA Only	1	UMA	Hidden	UMA boot
SG/Optimise	0	GPU	Hidden	GPU boot

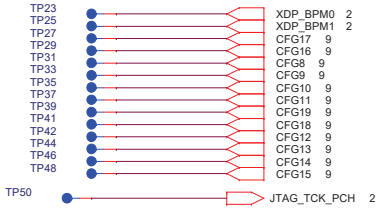
Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: KBL-U 13/15 (GPIO) | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 14 of 48

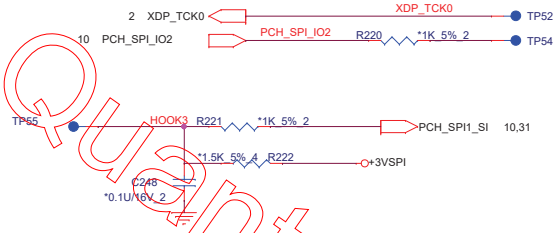


Quanta Computer Inc.	
PROJECT : ZAW	
Size	Document Number: KBL-U 14/15(PCH POWER) — Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 15 of 48

XDP Debug





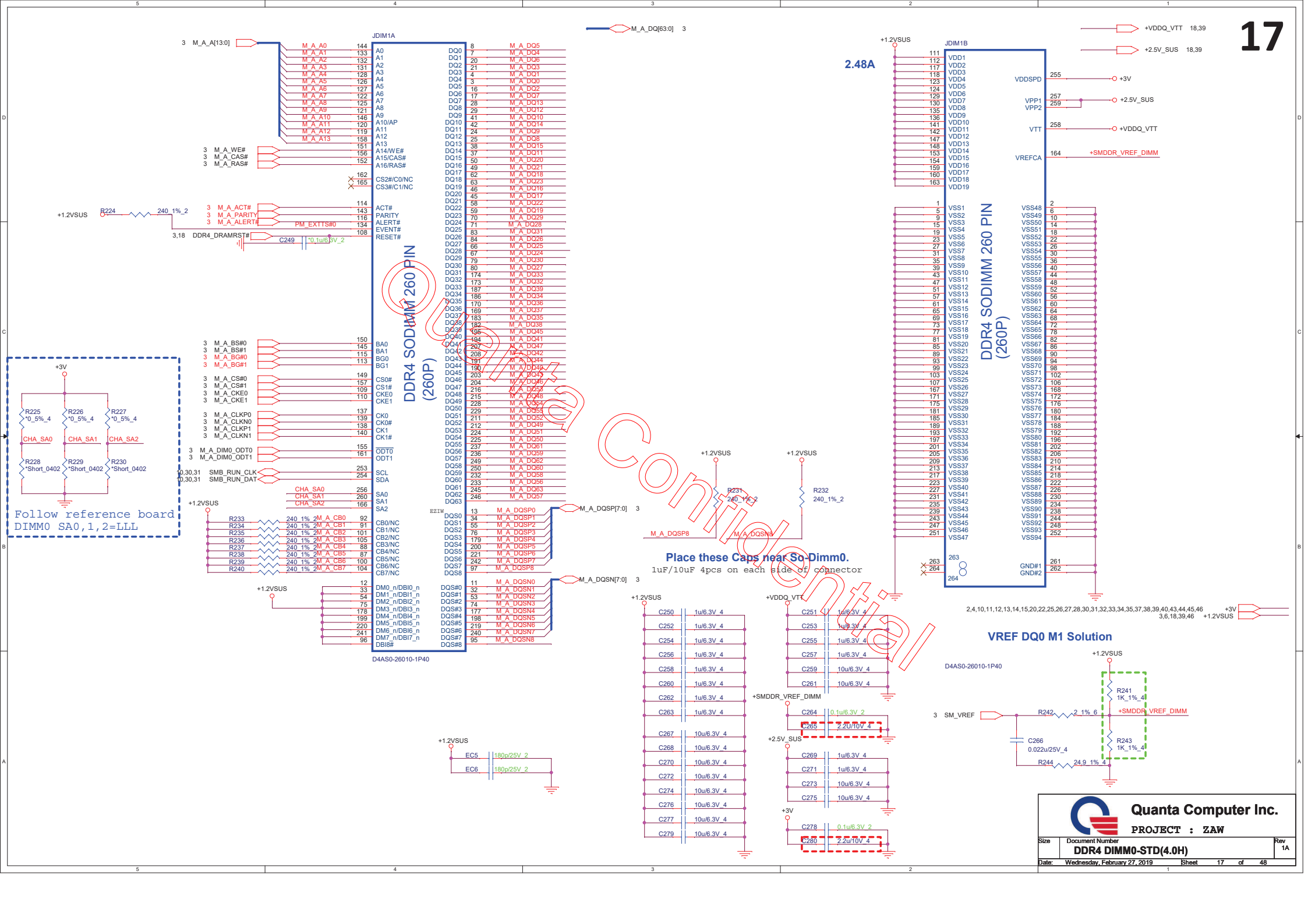


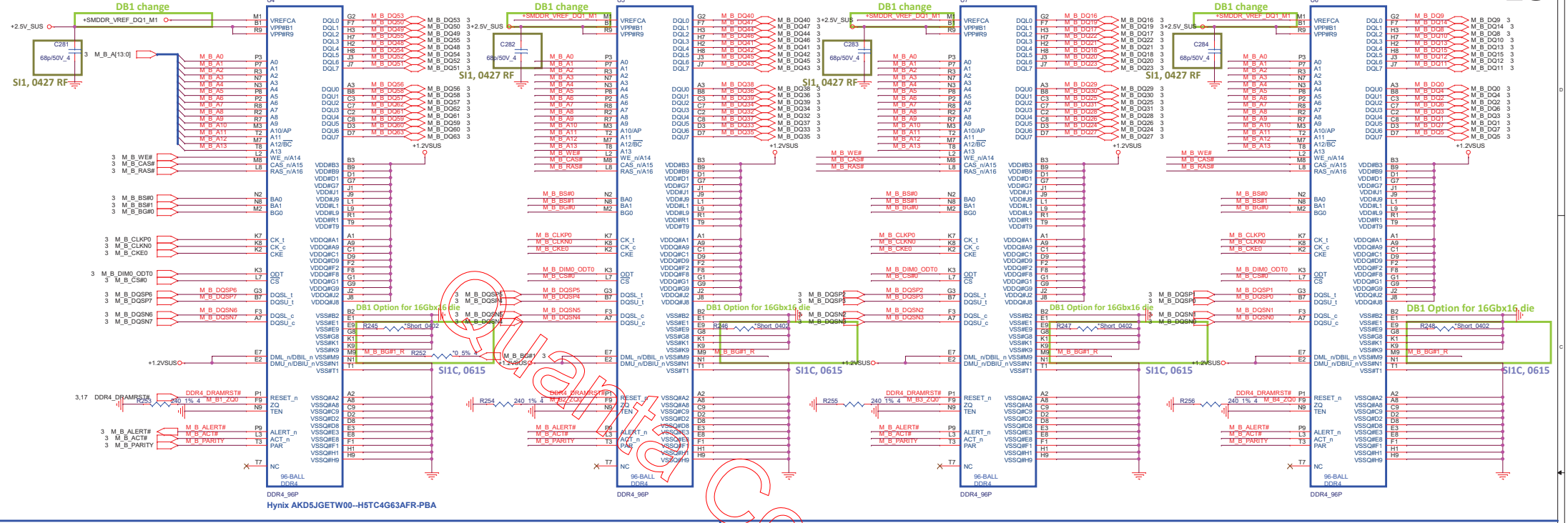
Quanta Computer Inc.

PROJECT : ZAW

Size	Document Number	Rev
	KBL-U 15/15 XDP&APS	1A

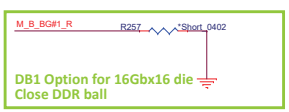
Date: Wednesday, February 27, 2019 Sheet 16 of 48

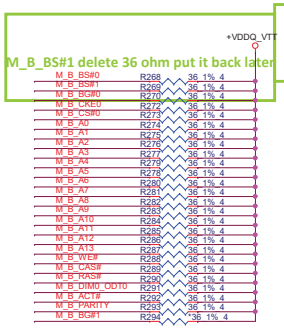

JDIM1A
DDR4 SODIMM 260 PIN (260P)
D4AS0-26010-1P40
JDIM1B
DDR4 SODIMM 260 PIN (260P)
2.48A
Quanta Confidential
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
Quanta Computer Inc.
PROJECT : ZAW
DDR4 DIMM0-STD(4.0H)
Rev 1A
Wednesday, February 27, 2019
Sheet 17 of 48

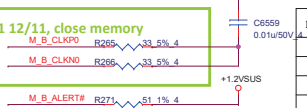


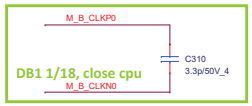
Vendor	P/N	Vendor P/N
MIC 16G	AKD5EG0TL00	MT40A1G16HBA-083E:A
Elpida		
SAMSUNG		

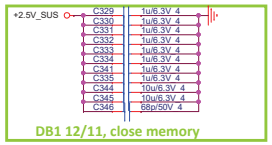
DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS



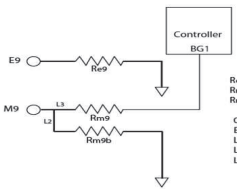


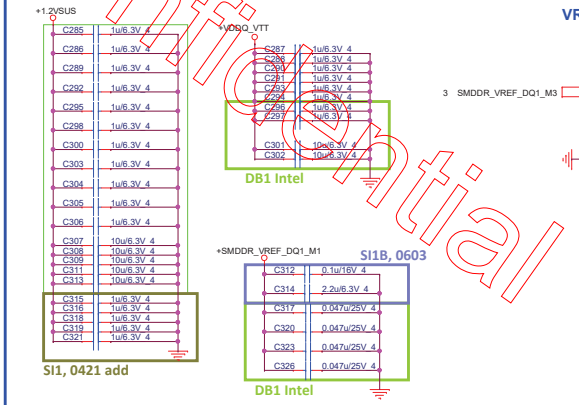


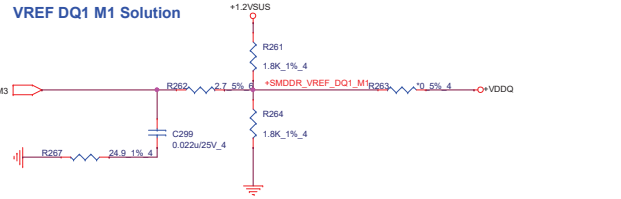


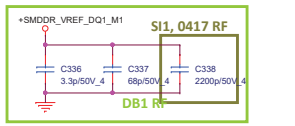


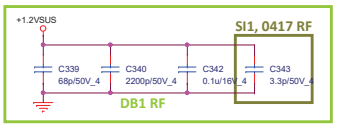
Memory 8G & Memory 16G TABLE			
	Memory 8G		Memory 16G
R278	0Ω	CS00002JB38	240Ω CS12402FB03
R279	0Ω	CS00002JB38	240Ω CS12402FB03
R280	0Ω	CS00002JB38	240Ω CS12402FB03
R281	0Ω	CS00002JB38	240Ω CS12402FB03
R282		UNINSTAL	INSTAL
R283		UNINSTAL	INSTAL
R284		UNINSTAL	INSTAL
R285		UNINSTAL	INSTAL
R290		INSTAL	UNINSTAL
R291		INSTAL	UNINSTAL
R292		INSTAL	UNINSTAL
R293		INSTAL	UNINSTAL







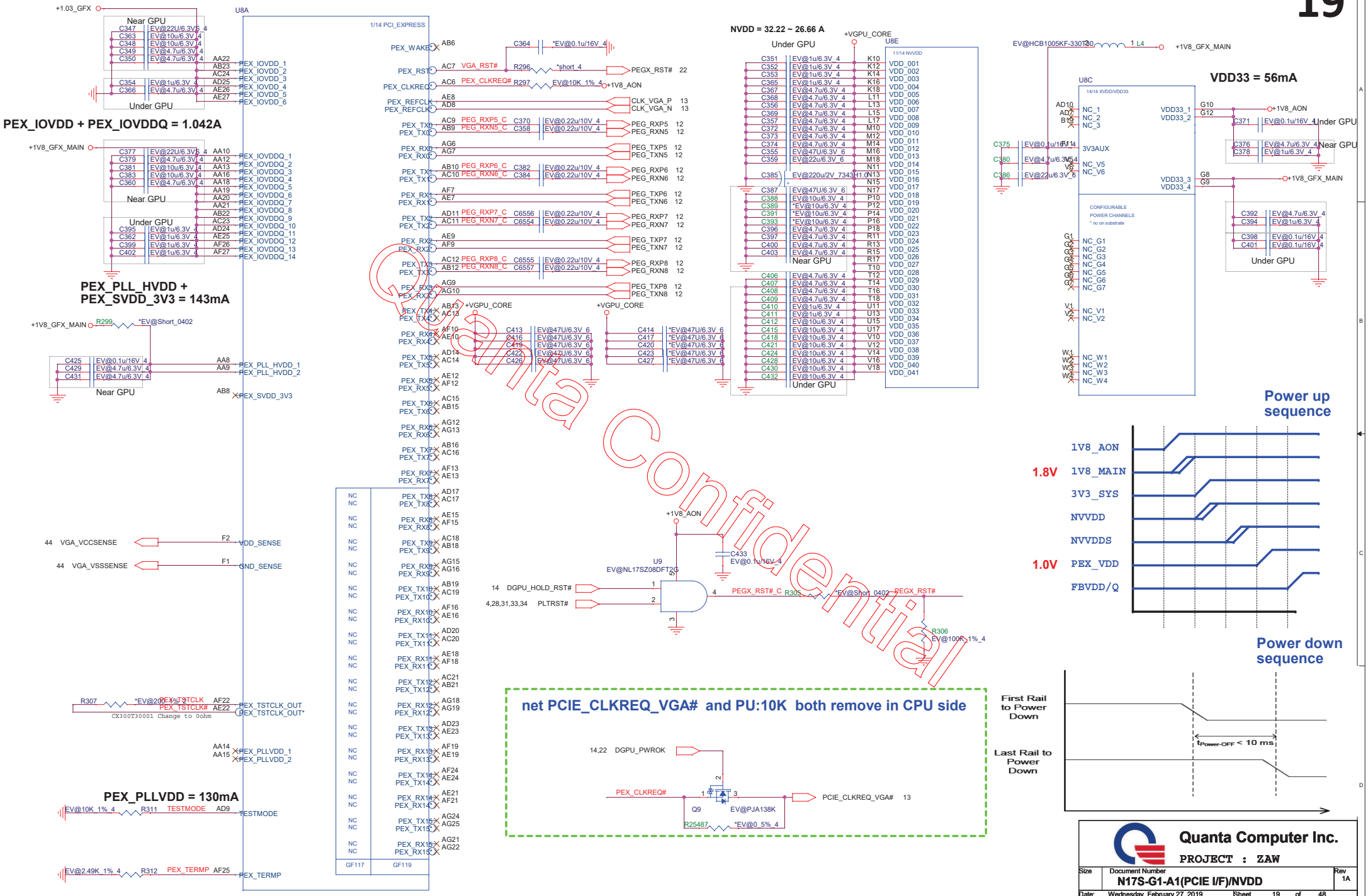


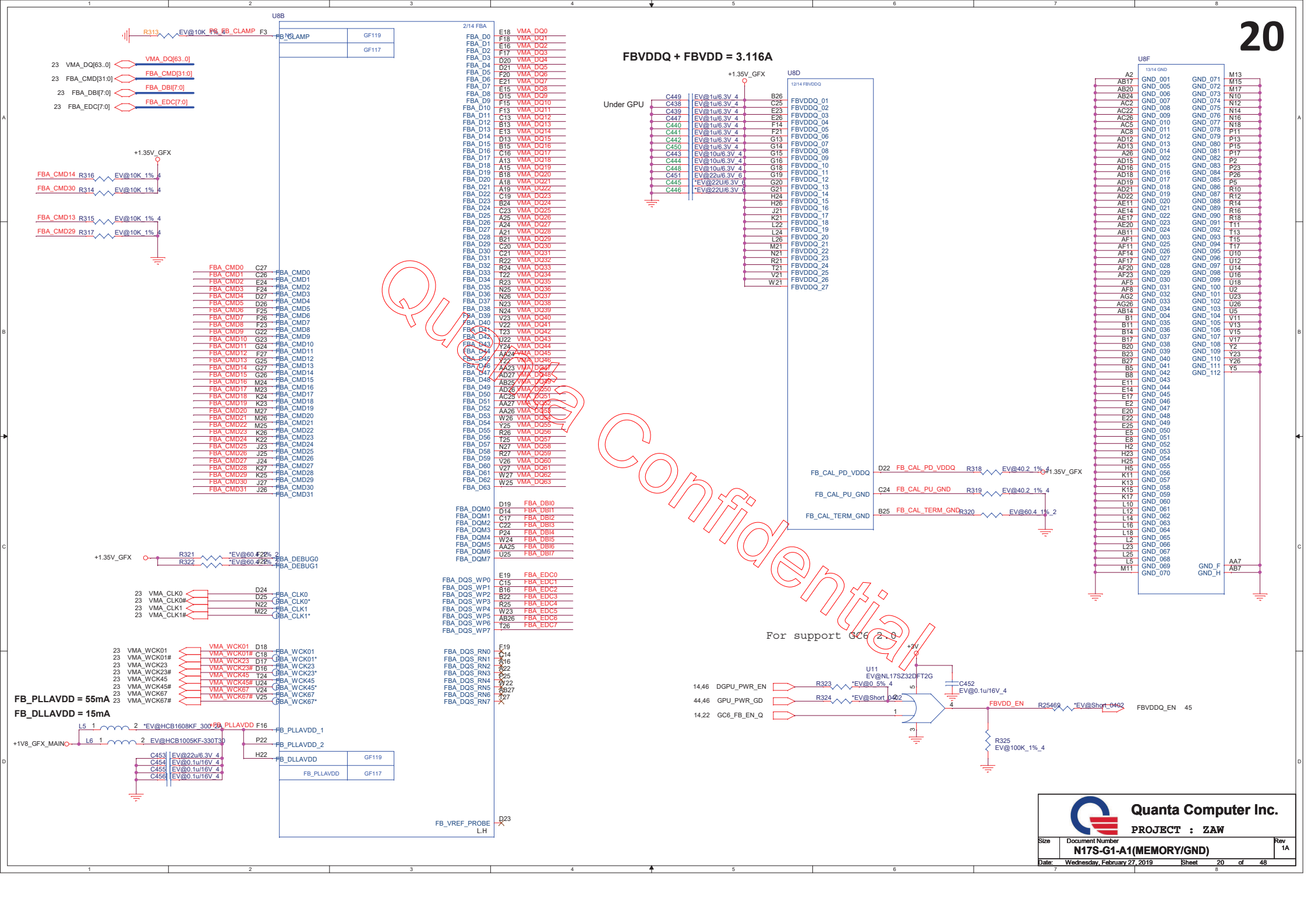


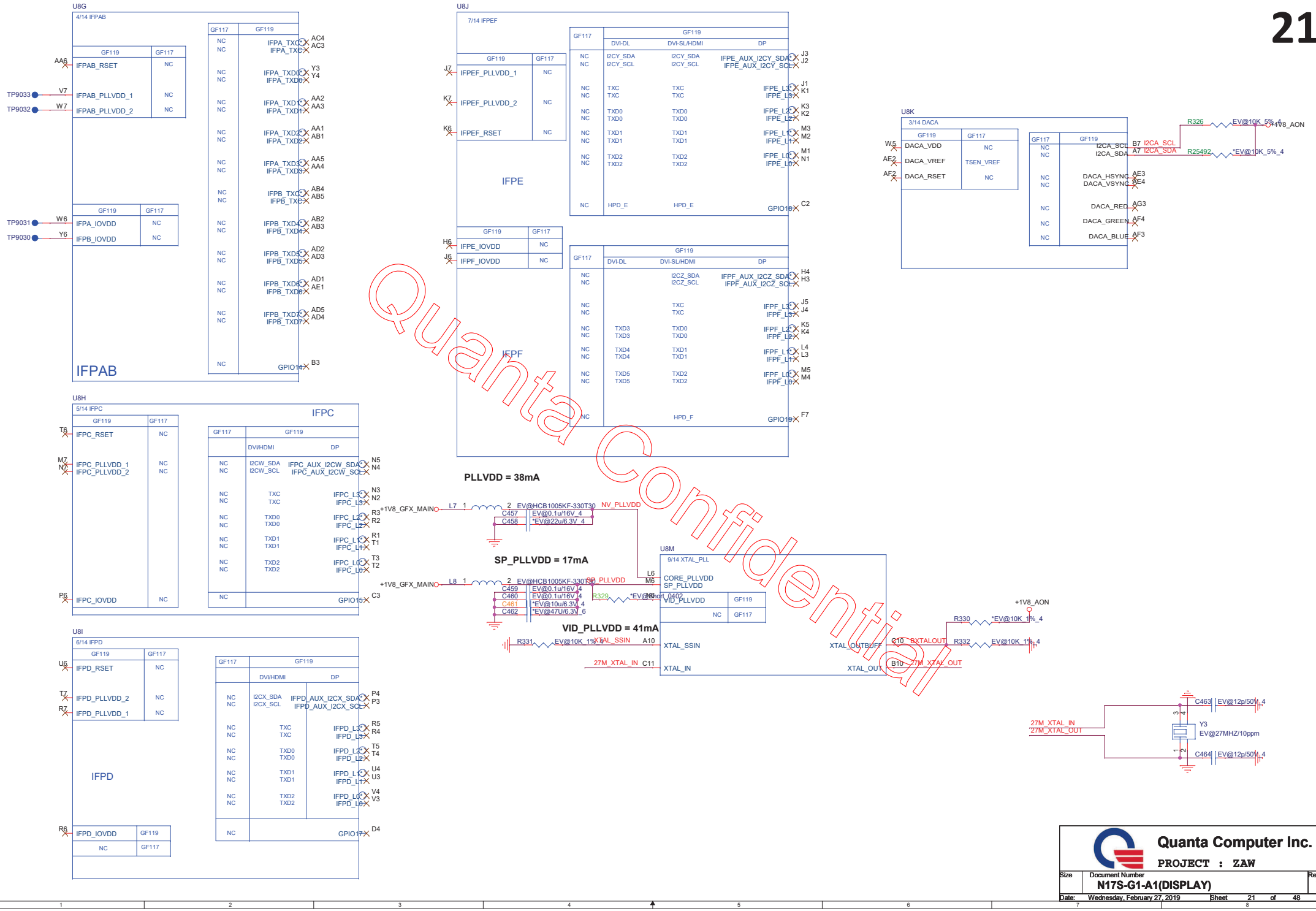
Quanta Computer Inc.
PROJECT : ZAW

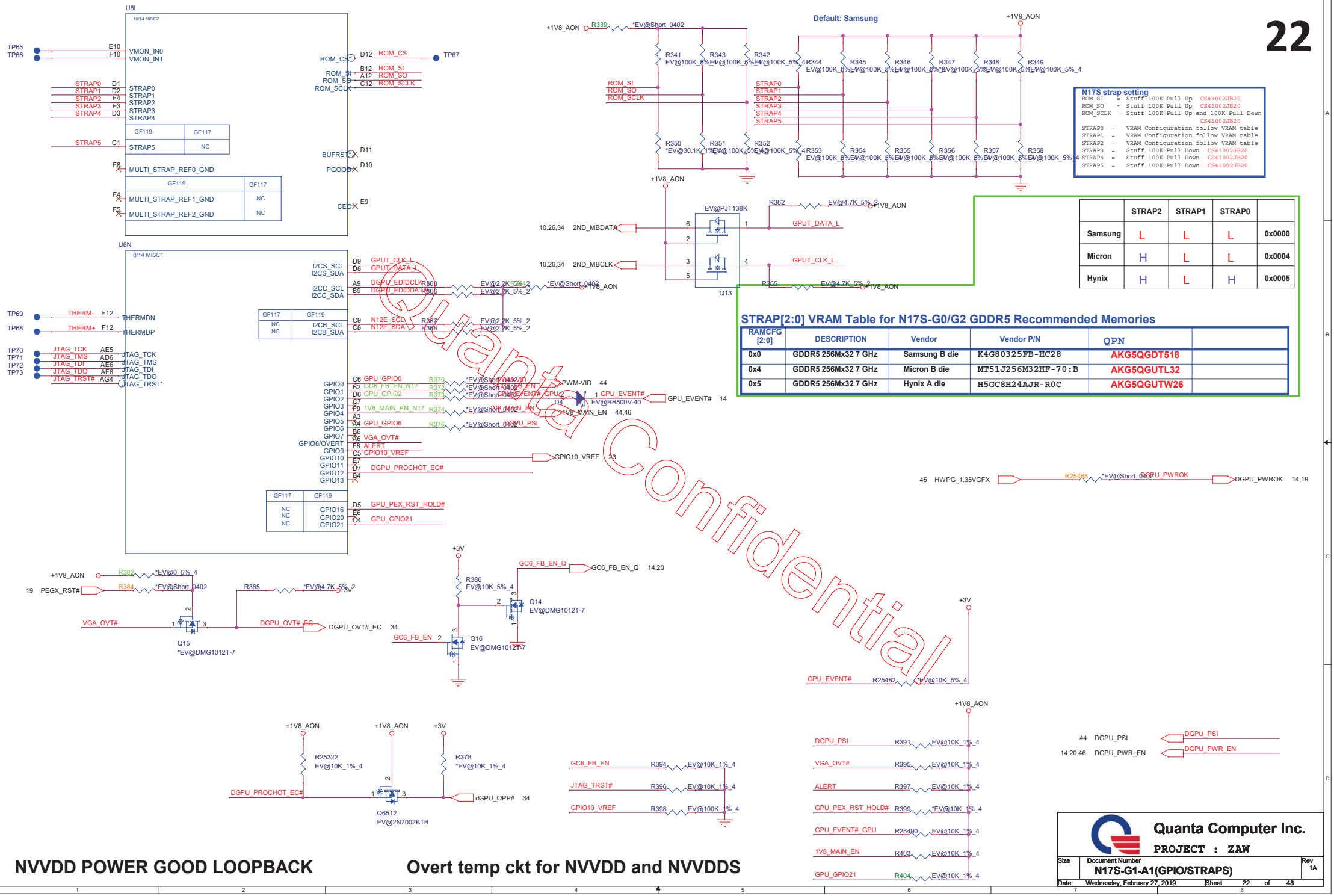
Size	Document Number	Rev
	DDR4 Memory Down (CH. B)	1A

Date: Wednesday, February 27, 2019 Sheet 18 of 48


PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up sequence
1V8_AON
1V8_MAIN
3V3_SYS
NVVDD
NVVDDS
PEX_VDD
FBVDD/Q
1.8V
1.0V
Power down sequence
First Rail to Power Down
Last Rail to Power Down
tPower-OFF < 10 ms
net PCIE_CLKREQ_VGA# and PU:10K both remove in CPU side
Quanta Confidential
Quanta Computer Inc.
PROJECT : ZAW
N17S-G1-A1(PCIE I/F)/NVDD
Wednesday, February 27, 2019


U8B
2/14 FBA
FBVDDQ + FBVDD = 3.116A
Under GPU
U8D
12/14 FBVDDQ
U8F
13/14 GND
FB_PLLAVDD = 55mA
FB_DLLAVDD = 15mA
Quanta Confidential
For support GC6 2.0
Quanta Computer Inc.
PROJECT : ZAW
Size
Document Number
N17S-G1-A1(MEMORY/GND)
Rev
1A
Date: Wednesday, February 27, 2019
Sheet 20 of 48


U8G
4/14 IFPAB
IFPAB
U8J
7/14 IFPEF
IFPE
IFPF
U8K
3/14 DACA
U8H
5/14 IFPC
IFPC
U8I
6/14 IFPD
IFPD
U8M
9/14 XTAL_PLL
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
Quanta Confidential



	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0000
Micron	H	L	L	0x0004
Hynix	H	L	H	0x0005

STRAP[2:0] VRAM Table for N17S-G0/G2 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	QPN	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT518	
0x4	GDDR5 256Mx32 7 GHz	Micron B die	MT51J256M32HF-70:B	AKG5QGUTL32	
0x5	GDDR5 256Mx32 7 GHz	Hynix A die	H5GC8H24AJR-R0C	AKG5QGUTW26	

NVVDD POWER GOOD LOOPBACK

Overt temp ckt for NVVDD and NVVDDS

Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	N17S-G1-A1(GPIO/STRAPS)	1A

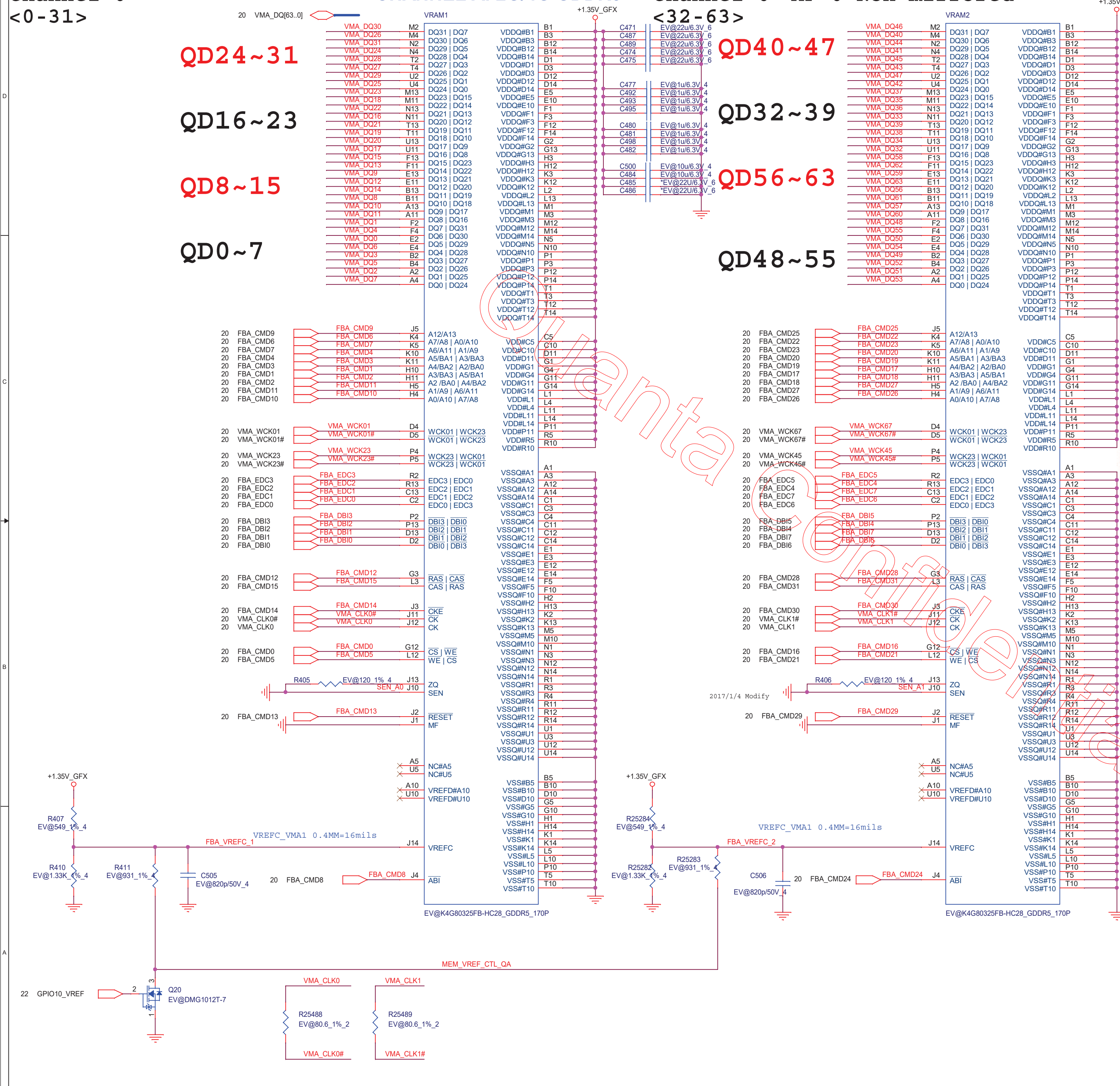
Date: Wednesday, February 27, 2019 Sheet 22 of 48

Channel 0 <0-31> MF=0 Non-mirrored

MF=0 Non-mirrored

CHANNEL A: 2G/4G GDDR5

Channel 0 <32-63> MF=0 Non-mirrored



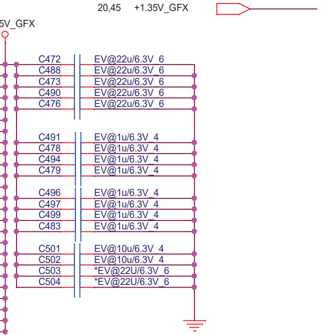


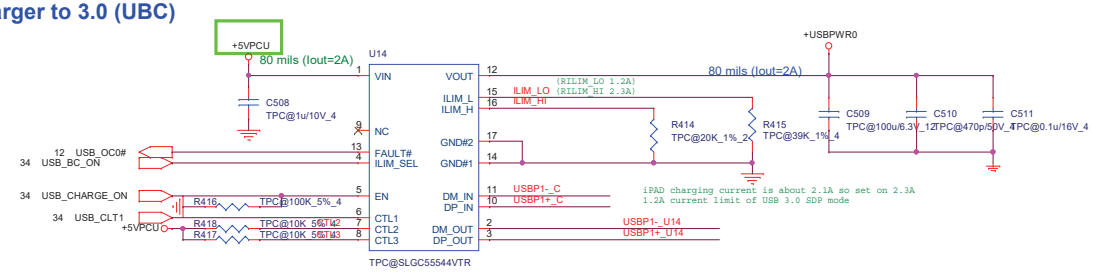
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

USB Charger to 3.0 (UBC)



	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

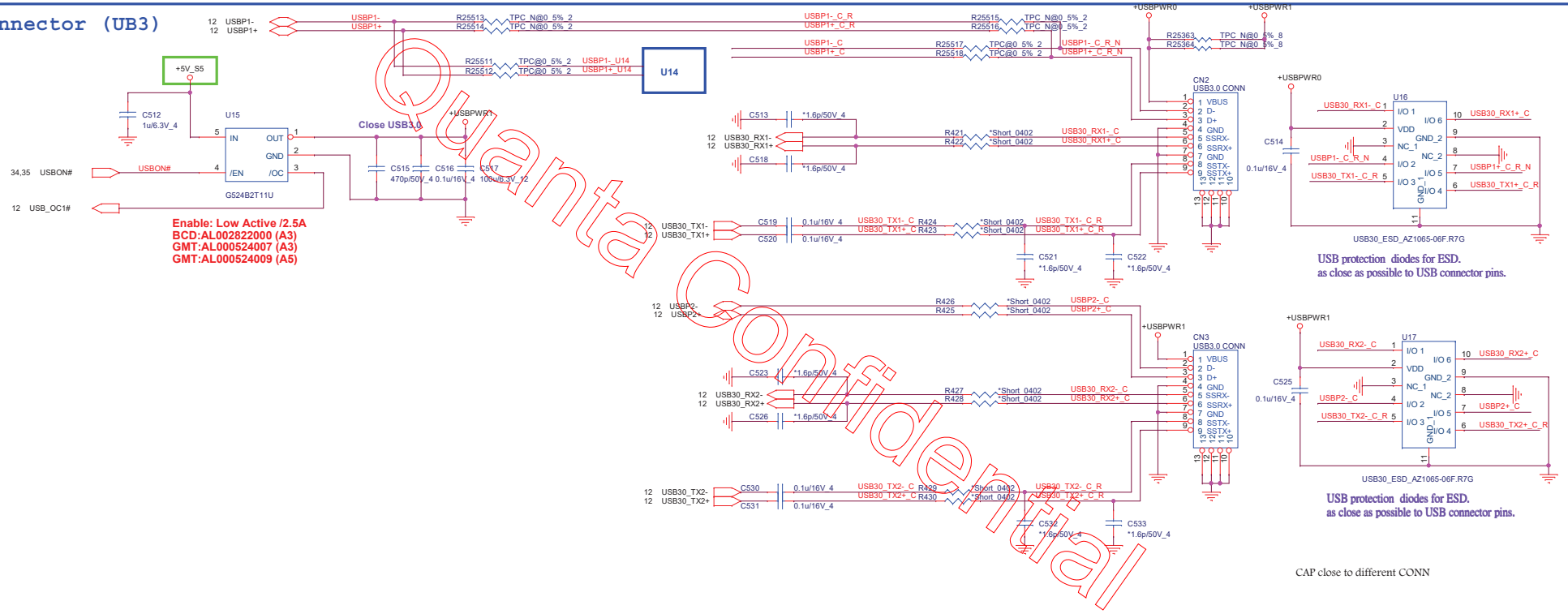
TI:AL002544001(TPS2544)
Silergy: AL055544000 (SLGC55544VTR)

RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

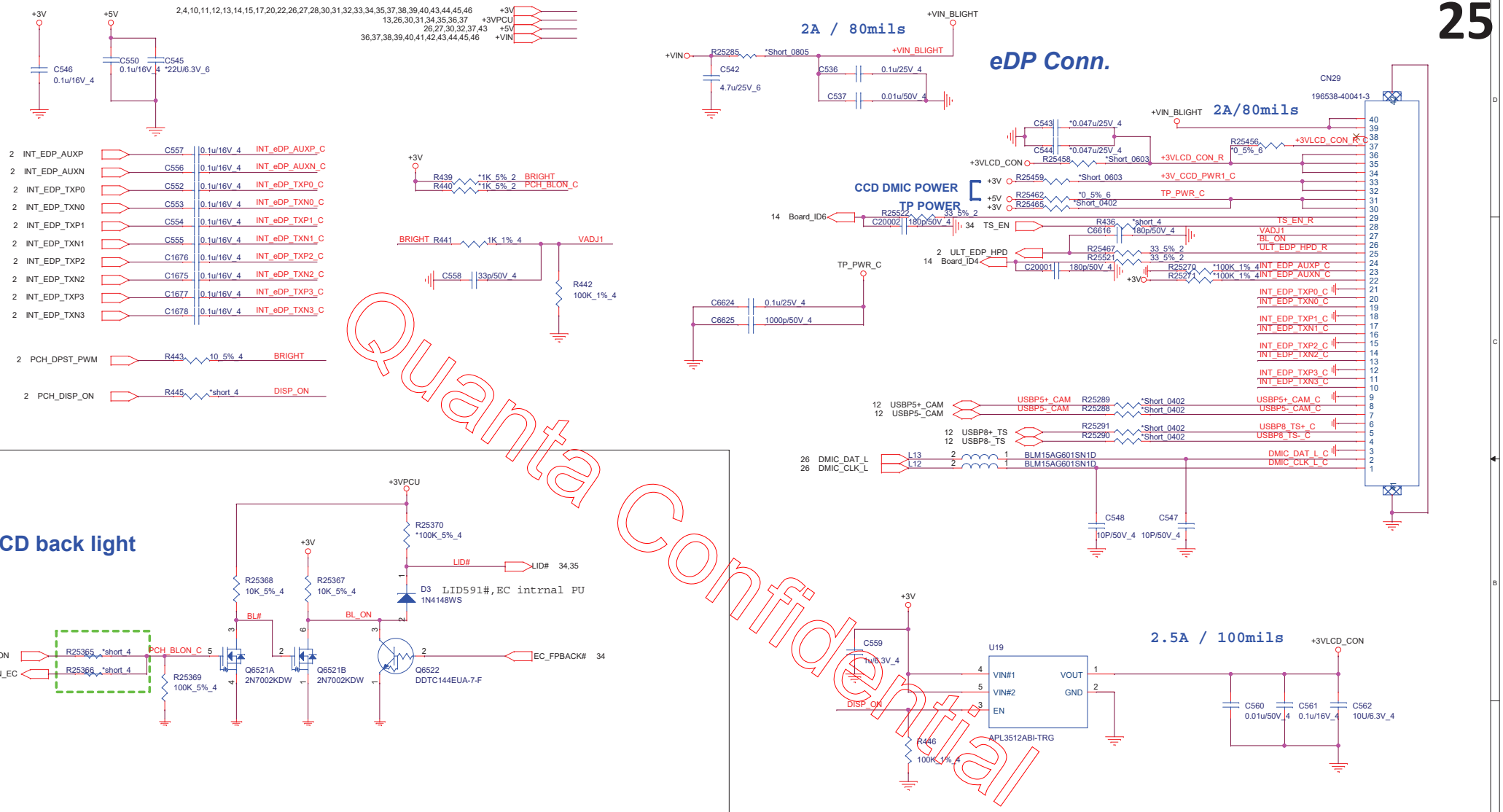
$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

+5VPCU 26,37,38,46
+5V_S5 29,35,37,39,40,41,42,44,45,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,45,46

USB 3.0 Connector (UB3)



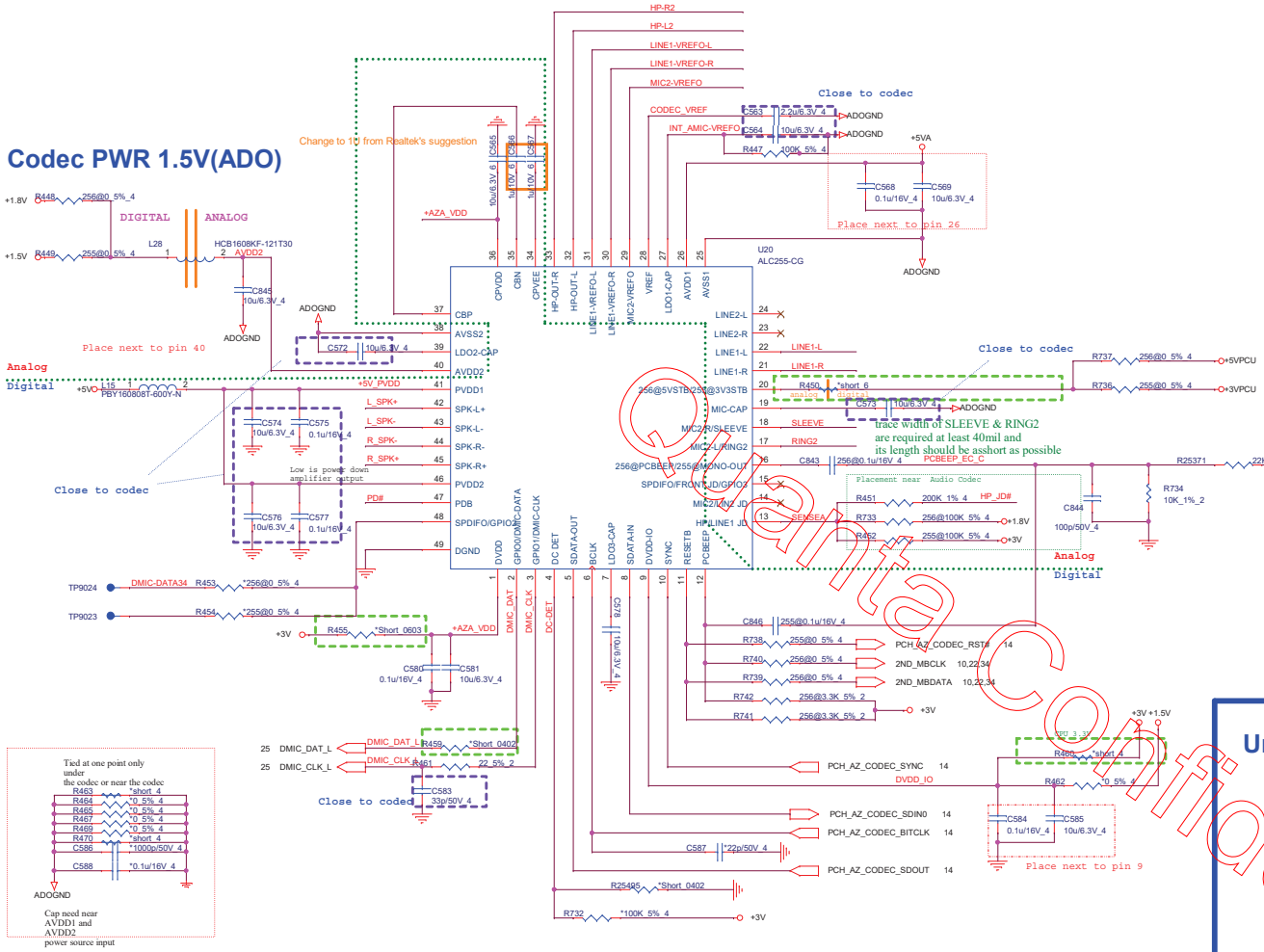
Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number | Rev
USB3/Charger | 1A
Date: Wednesday, February 27, 2019 | Sheet 24 of 48



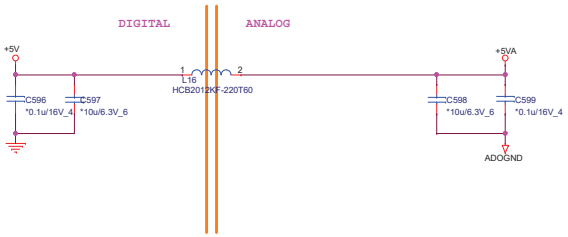
Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: eDP CONN/LID/CAM/D-MIC/TS | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 25 of 48

Codec(ADO)

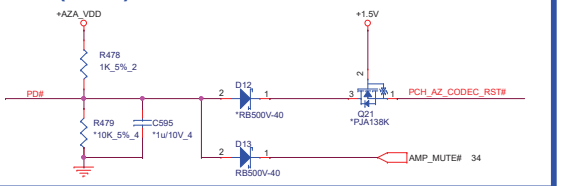
Codec PWR 1.5V(ADO)



Codec PWR 5V(ADO)



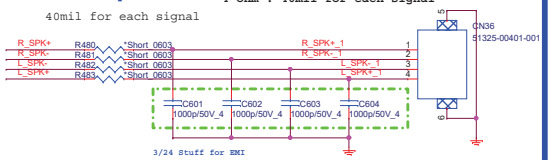
Mute(ADO)



Internal Speaker

4 ohm : 40mil for each signal

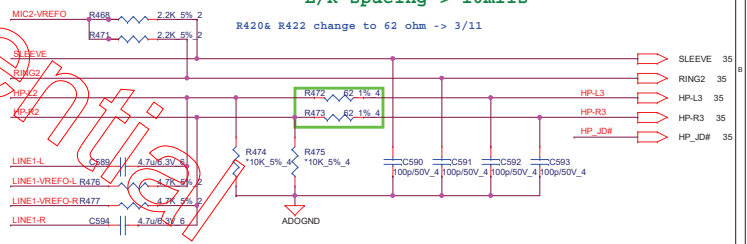
40mil for each signal



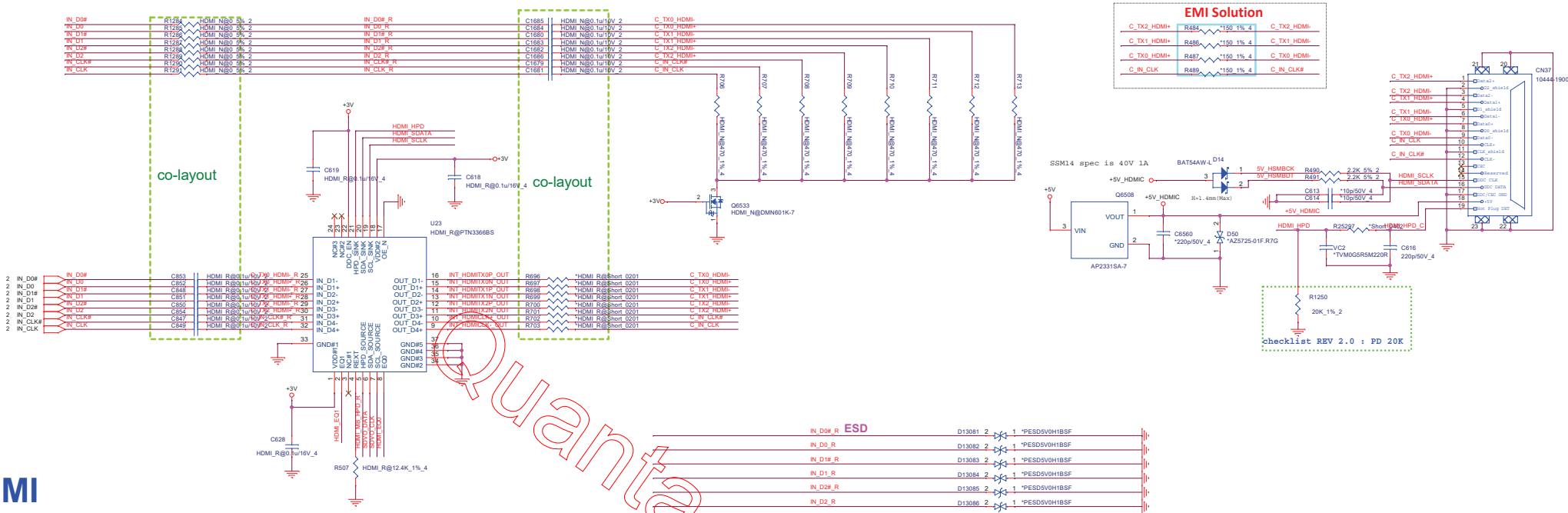
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils

R420& R422 change to 62 ohm -> 3/11



Quanta Computer Inc.		
PROJECT : ZAW		
Size	Document Number: Audio Codec/HP/SPK/Hole	Rev 1A
Date: Wednesday, February 27, 2019	Sheet 26 of 48	



HDMI

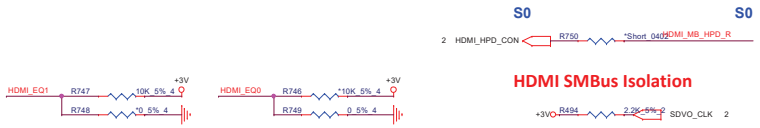
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

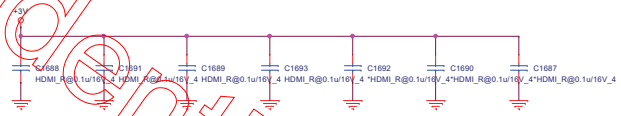
From PCH

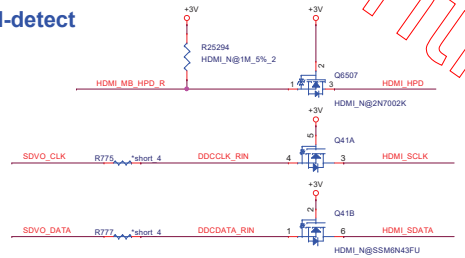
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB







LAN RTL8111HSH-CG

For LDO mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca ,Cb

* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)

Power trace Layout 寬度> 60mil

+1.05V_LAN_REGOUT — R25503 La *Short_0805 — C20000 0.1u/16V_4

+1.05V_LAN

PIN3	PIN8	PIN30	PIN22	PIN22	PIN22
Cc	Cd	Ce	Cf	Cg	Ch
C631 0.1u/16V_4	C632 0.1u/16V_4	C633 0.1u/16V_4	C634 0.1u/16V_4	C635 1u/6.3V_4	C636 0.1u/16V_4

LAN_AMBLED# — TP74
LAN_LED1 — TP75
LAN_LED2 — TP76

if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

+1.05V_LAN — R508 2.49K_1%_4 — +3V_LAN

LAN_AMBLED#
LAN_WLED#

+3V — R509 1K_5%_2 — ISOLATEB — R510 15K_1%_4

U24 RTL8111HSH-CG

Pin	Name
32	AVDD33#2
31	RSET
30	AVDD10#3
29	CKXTAL2
28	CKXTAL1
27	LED3/EED
26	LED1/GPO
25	LED2
33	GND

Add 9 GND VIAs with thermal PAD

LAN_XTAL1 — R511 10_5%_4 — XTAL1
Y4 25MHZ/30ppm
R512 680_5%_4 — XTAL2
C638 15p/50V_4
C639 15p/50V_4

MDI0+	1	MDIP0	
MDI0-	2	MDIN0	
	3	AVDD10#1	
MDI1+	4	MDIP1	
MDI1-	5	MDIN1	
MDI2+	6	MDIP2	
MDI2-	7	MDIN2	
	8	AVDD10#2	
	9	MDIP3	
	10	MDIN3	
	11	AVDD33#1	
	12	CLKREQB	
	13	HSIP	
	14	HSIN	
	15	REFCLK_P	
	16	REFCLK_N	
	24	REGOUT	+1.05V_LAN_REGOUT
	23	VDDREG	+3V_LAN
	22	DVDD10	+1.05V_LAN
	21	LANWAKEB	PCIE_WAKE#_R — R513 *short_4 — PCIE_WAKE# 4,33
	20	ISOLATEB	
	19	PERSTB	PLTRST# 4,19,31,33,34
	18	HSON	PCIE_RXN_LAN_L — C637 0.1u/16V_4 — PCIE_RXN9_LAN 12
	17	HSOP	PCIE_RXP_LAN_L — C640 0.1u/16V_4 — PCIE_RXP9_LAN 12

MDI3+ / MDI3- — CLK_PCIE_LANN 13, CLK_PCIE_LANP 13
PCIE_TXN9_LAN — PCIE_TXN9_LAN 12
PCIE_TXP9_LAN — PCIE_TXP9_LAN 12

For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

Leakage circuit (MPC)

CLK_PCIE_REQ4# have PU 10k.

S0 — 13 PCIE_CLKREQ_LAN#

+3V — R25444 *10K_5%_4 — Q6531 2N7002K — R25446 10K_5%_4
+3V — R25445 10K_5%_4 — MAIN POWER(3V_S0)
PCIE_REQ_LAN#_R

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8107ESH-CG/RTL8111HSH-CG

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3V_S5 — R25296 *Short_0805 — +3V_LAN

PIN11	PIN32	PIN11	PIN32
C641 0.1u/16V_4 Cj	C642 0.1u/16V_4 Ck	C643 *4.7u/6.3V_4 Cm	C644 *4.7u/6.3V_4 Cn

For Giga：Ub

Ub — U25

MDI2+	2	TD1+	MX1+	23	MDI2+_1
MDI2-	3	TD1-	MX1-	22	MDI2-_1
MDI3-	5	TD2+	MX2+	20	MDI3-_1
MDI3+	6	TD2-	MX2-	19	MDI3+_1
MDI0-	8	TD3+	MX3+	17	MDI0-_1
MDI0+	9	TD3-	MX3-	16	MDI0+_1
MDI1-	11	TD4+	MX4+	14	MDI1-_1
MDI1+	12	TD4-	MX4-	13	MDI1+_1
TRA_V_DAC	1	TCT1	MCT1	24	LAN_MCTG0 — RaR516 — 75_1%_8
TRA_V_DAC	4	TCT2	MCT2	21	LAN_MCTG1 — RbR517 — 75_1%_8
TRA_V_DAC	7	TCT3	MCT3	18	LAN_MCTG2 — RcR518 — 75_1%_8
TRA_V_DAC	10	TCT4	MCT4	15	LAN_MCTG3 — RdR519 — 75_1%_8
	25	GND			

NS892407
C645 0.01u/50V_4
C646 10p/3KV_1808

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

RJ45 — CN8 2RJ1622-001111F

MDI3-_1	8	9	11
MDI3+_1	7		
MDI1-_1	6		
MDI2-_1	5		
MDI2+_1	4		
MDI1+_1	3		
MDI0-_1	2	10	12
MDI0+_1	1		

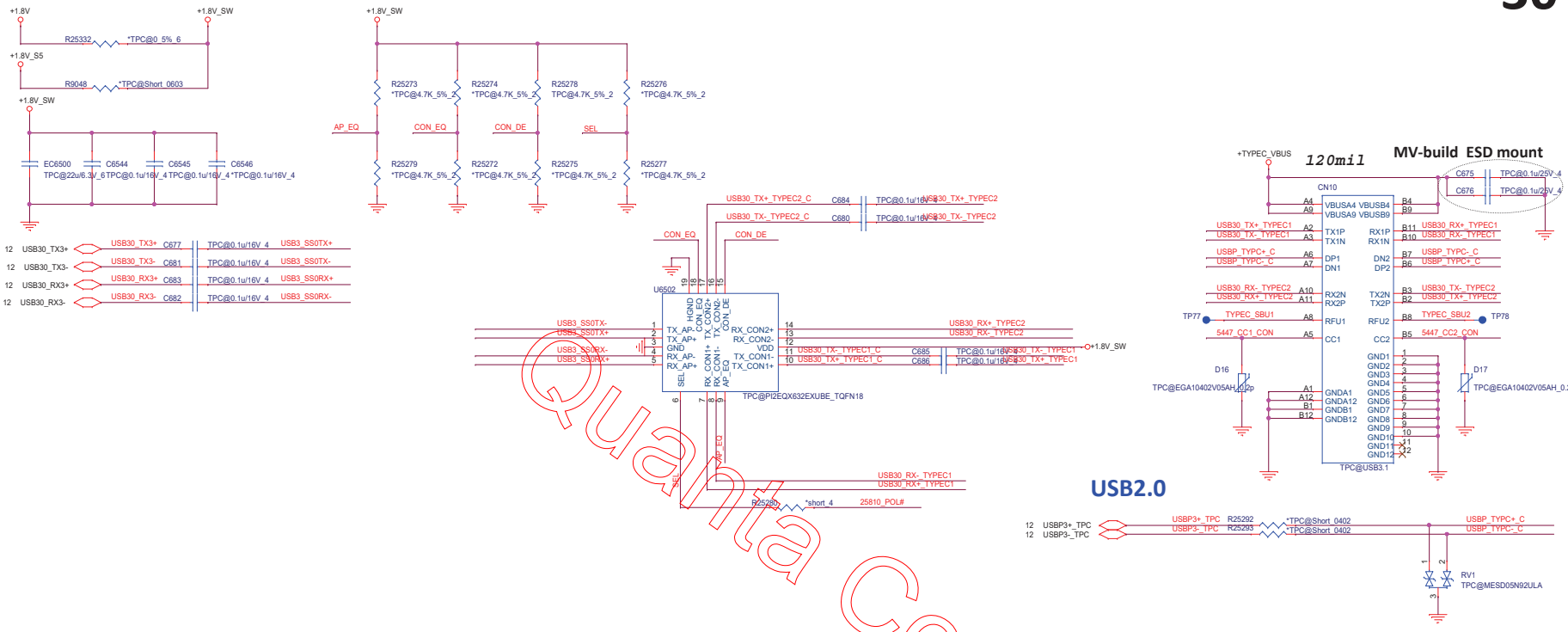
2018/11/06
Need change ther footprint

Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	LAN RTL8166EH/RTL8111HSH	1A

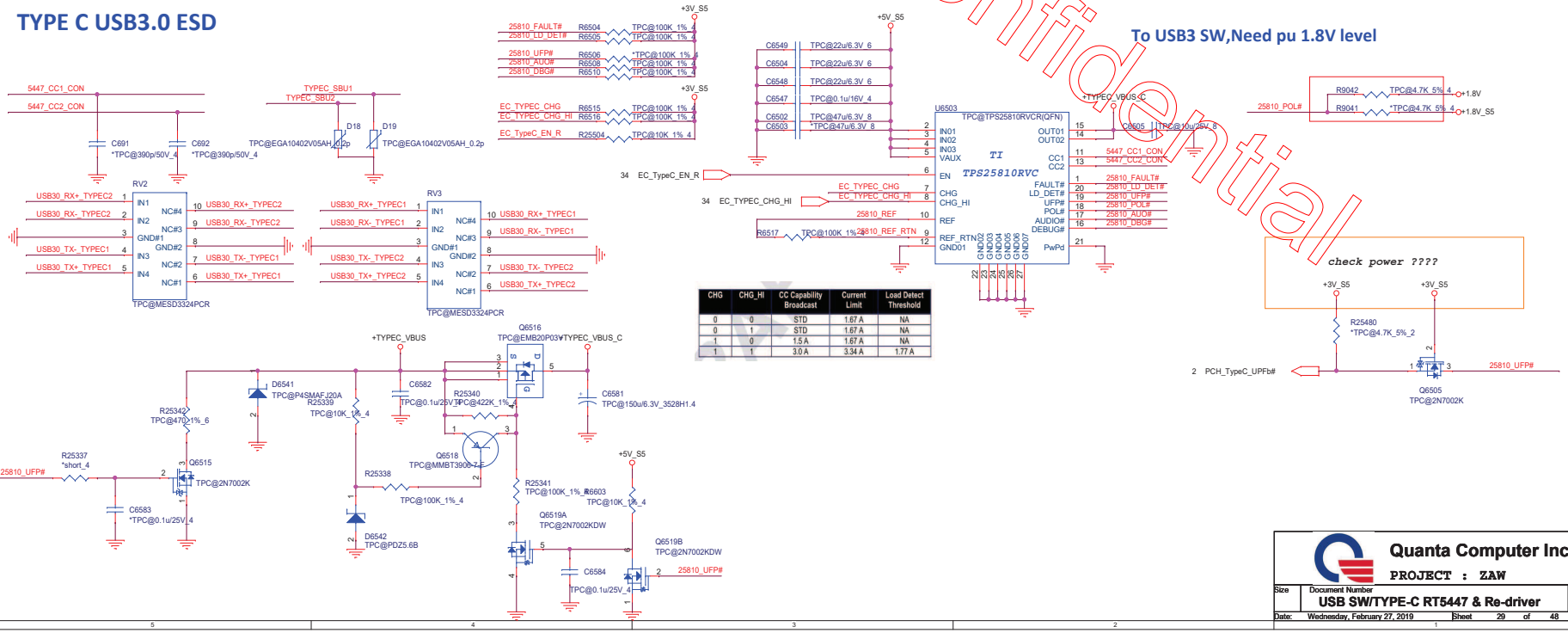
Date: Wednesday, February 27, 2019 Sheet 28 of 48

TYPE C and MUX PI2EQX632EXUBE



USB2.0

TYPE C USB3.0 ESD



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

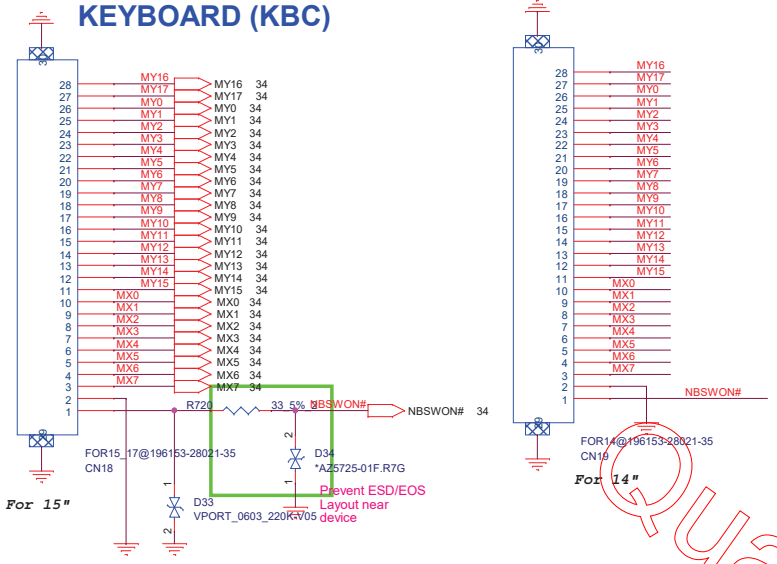
Quanta Computer Inc.

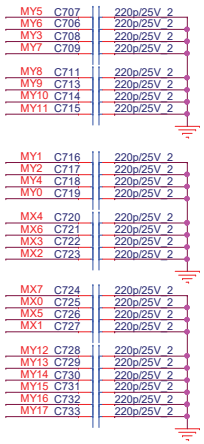
PROJECT : ZAW

Size	Document Number	Rev
	USB SW/TYPE-C RT5447 & Re-driver	1A

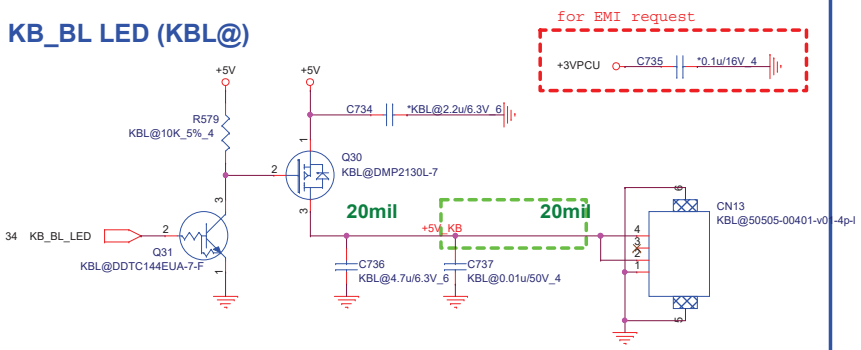
Date: Wednesday, February 27, 2019 Sheet 29 of 48

KEYBOARD (KBC)

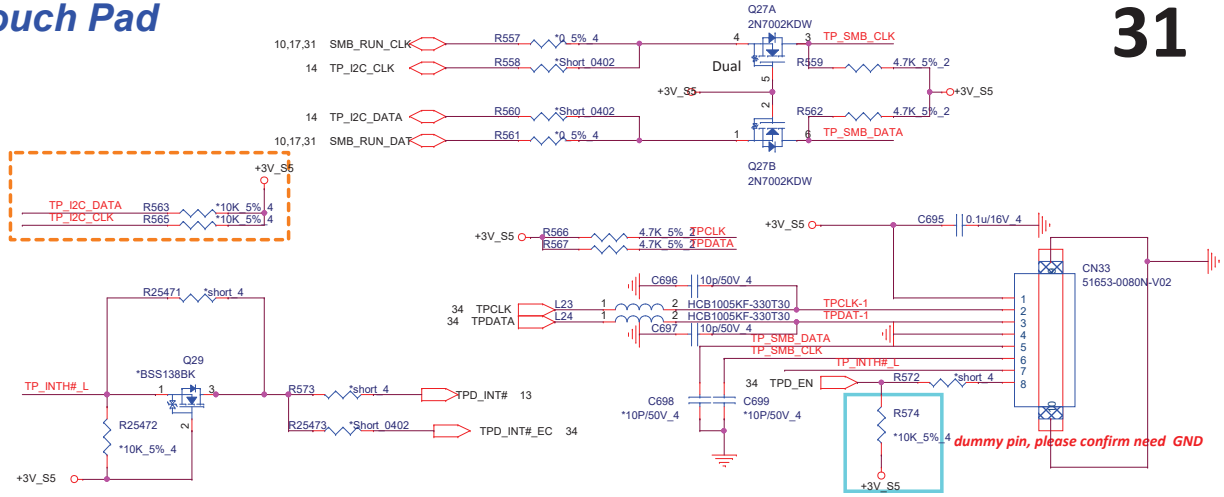




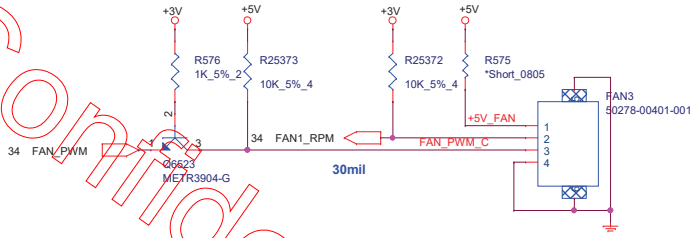
KB_BL LED (KBL@)



Touch Pad



FAN check pin define

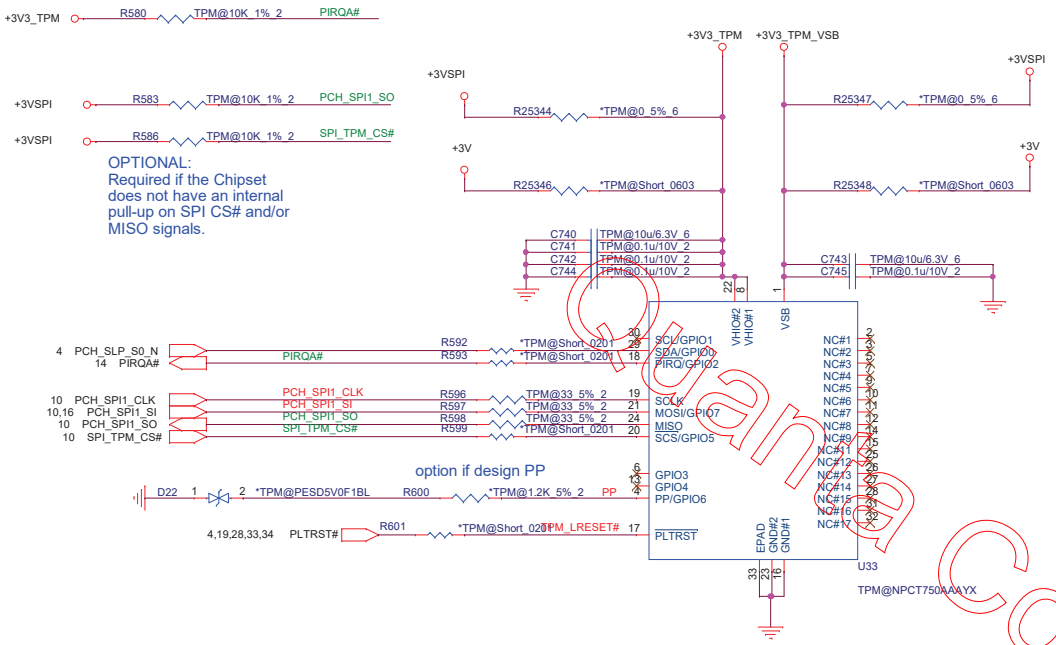


Quanta Computer Inc.
PROJECT : ZAW

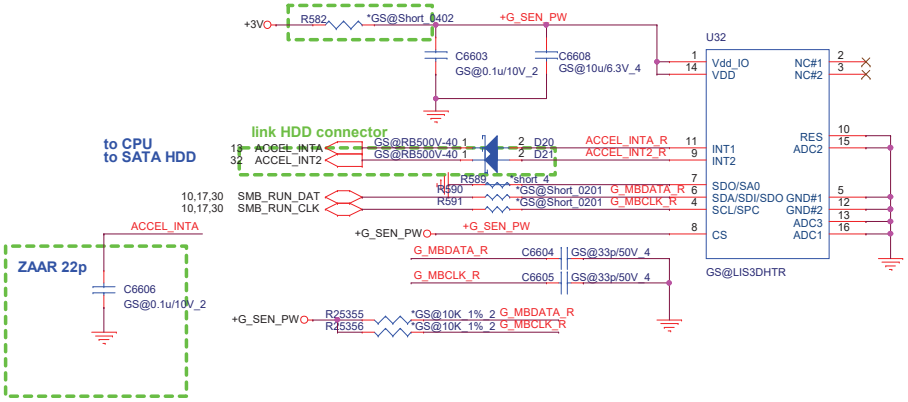
Size	Document Number	Rev
	KB/TP/FAN	1A

Date: Wednesday, February 27, 2019 Sheet 30 of 48

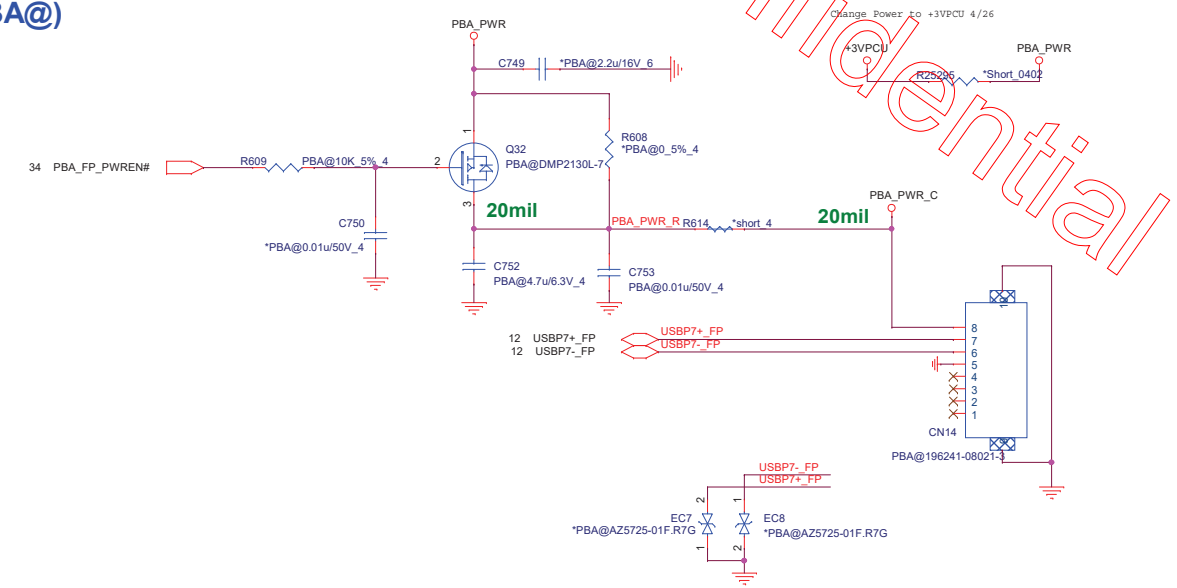
TPM NPCT750



G-sensor (GS@)



PBA (PBA@)



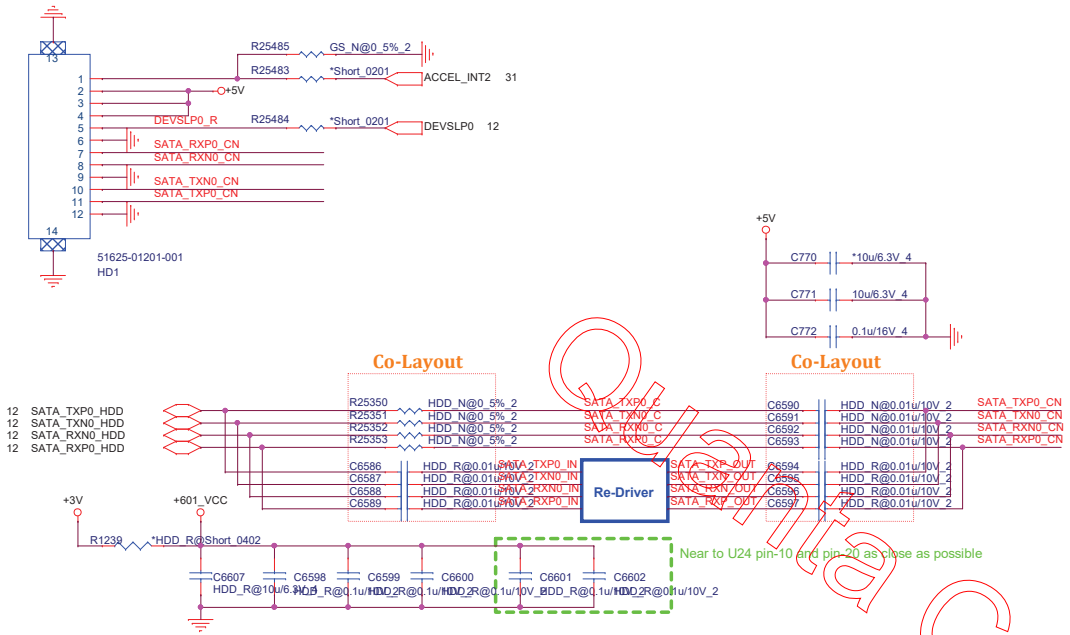
Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	TPM/G-Sensor/PBA	1A

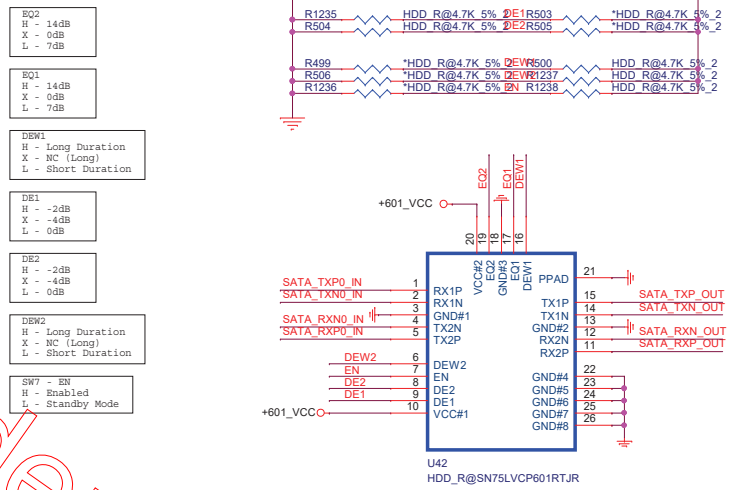
Date: Wednesday, February 27, 2019 Sheet 31 of 48

SATA HDD & LED

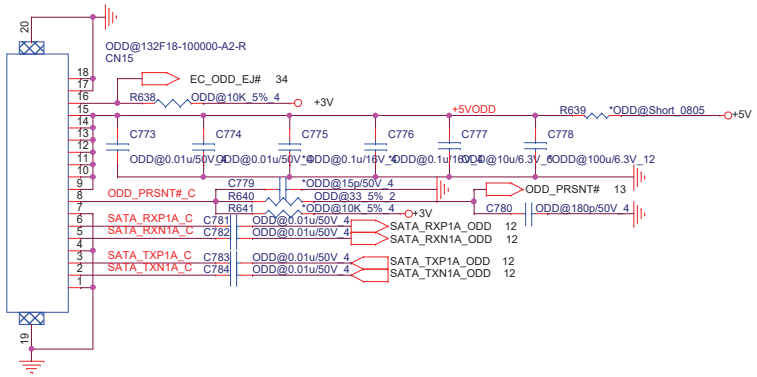
24,29,35,37,39,40,41,42,44,45,46 +5V_S5
25,26,27,30,37,43 +5V
2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,33,34,35,37,38,39,40,43,44,45,46 +3V
2,4,10,12,13,14,15,28,29,30,33,34,37,39,43 +3V_S5
9,15,38 +1.05V_DEEP_SUS



SATA HDD Re-driver



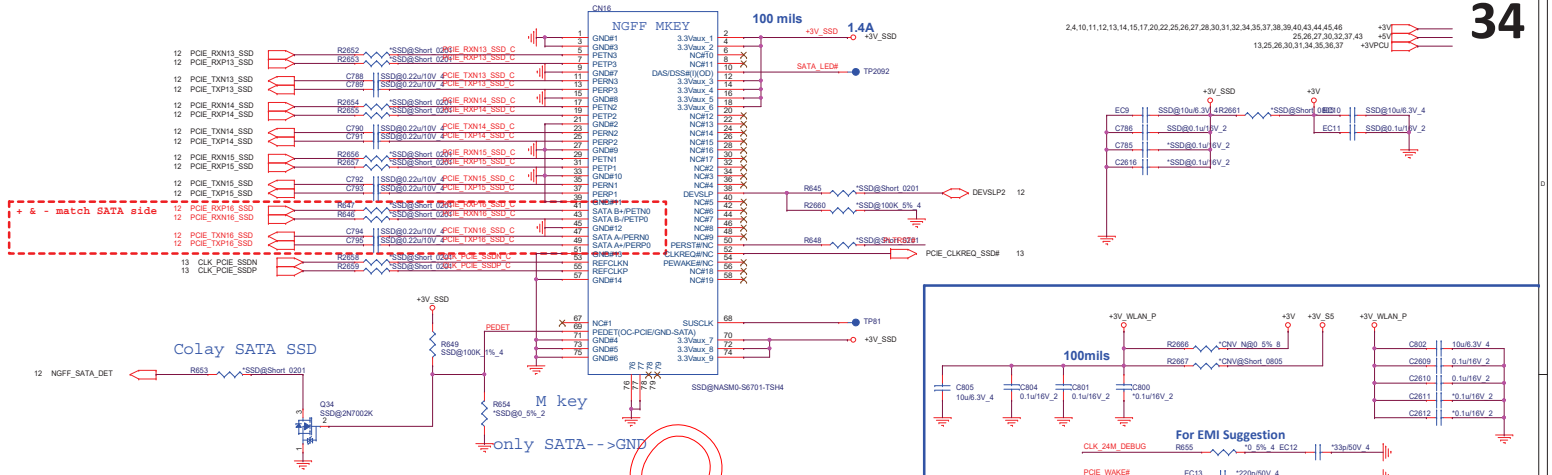
SATA ODD (ODD@)



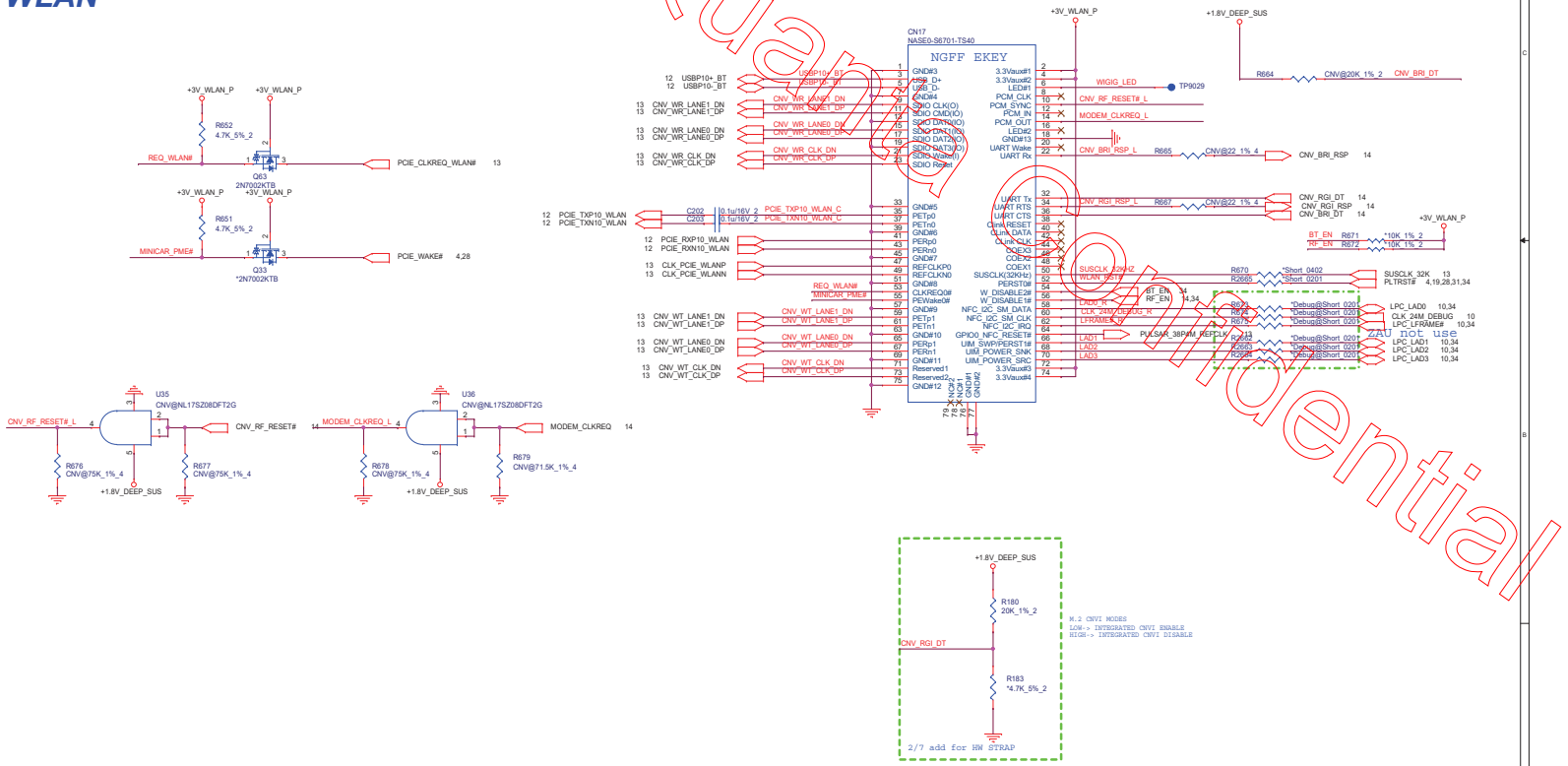
Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	HDD/ ODD	1A

Date: Wednesday, February 27, 2019 Sheet 32 of 48

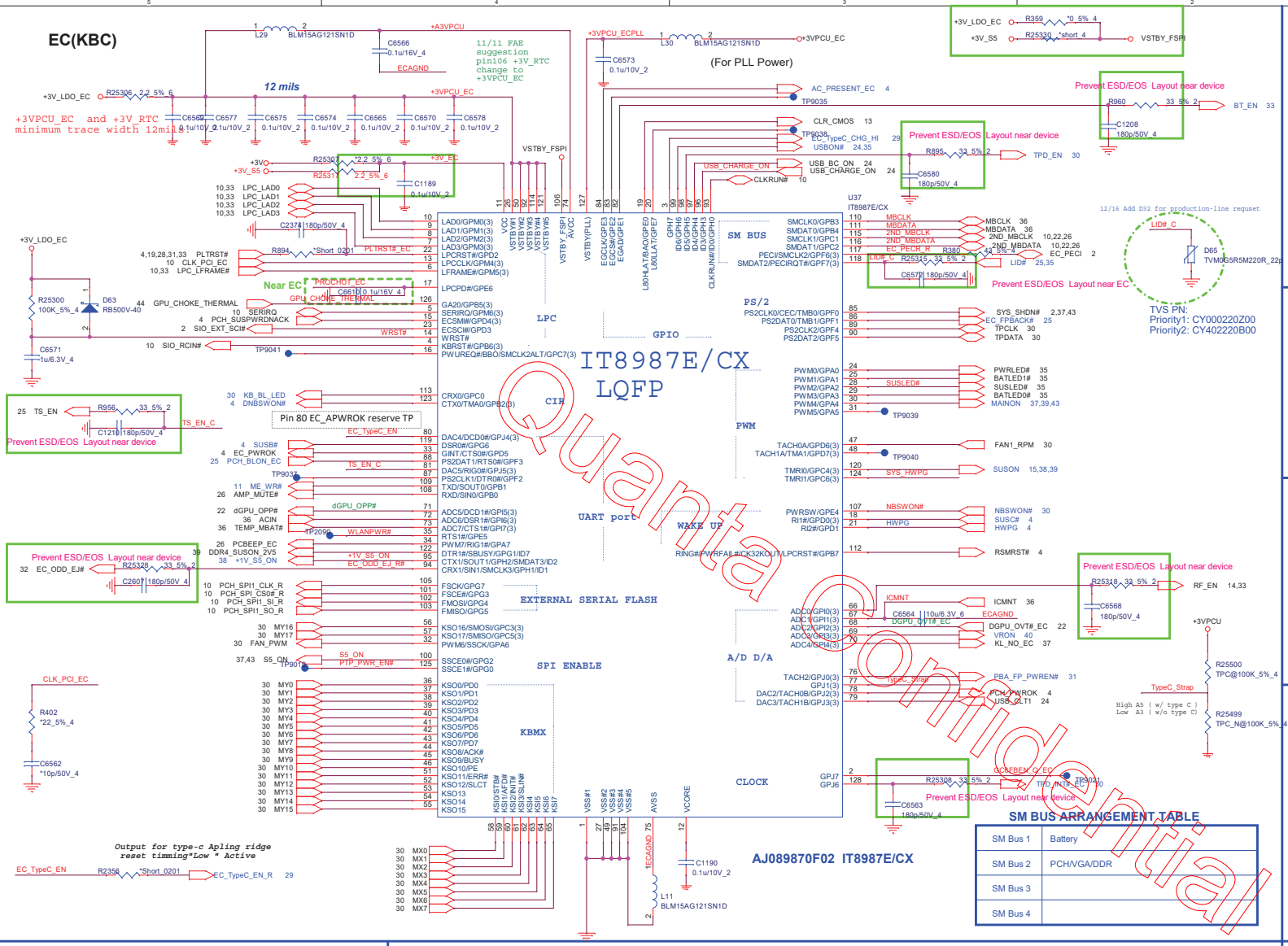


WLAN



Quanta Computer Inc.			
PROJECT : ZAW			
Size	Document Number		Rev
	HDD/WLAN(NGFF)		1A
Date: Wednesday, February 27, 2019	Sheet 33 of 48		

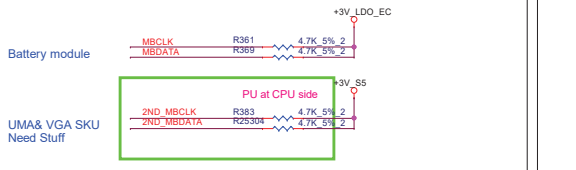
EC(KBC)



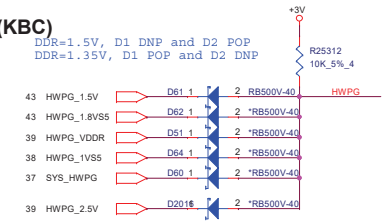
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA/DDR
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)

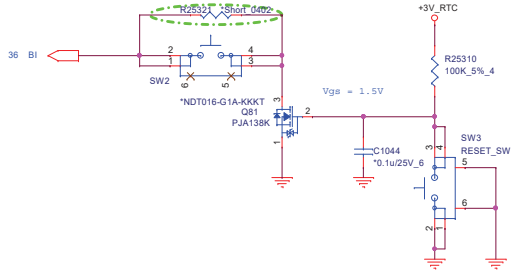


HWPG(KBC)



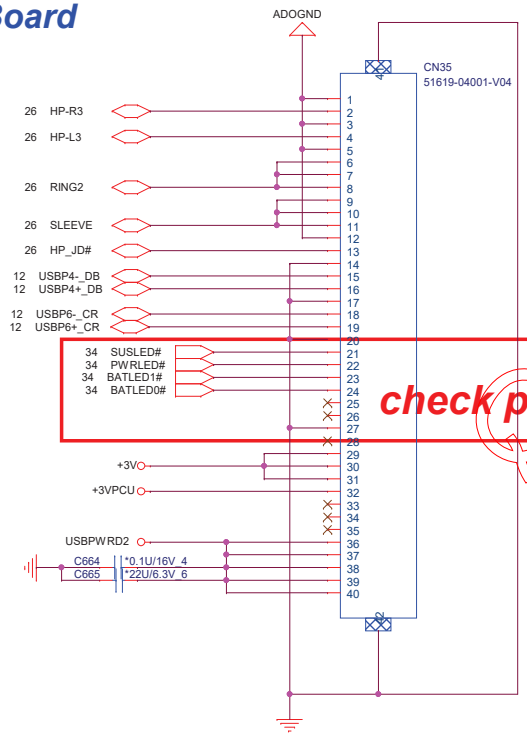
Reset SW (FSW)

Battery Detect Switch



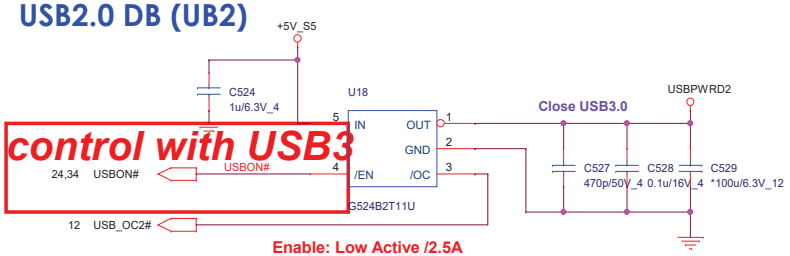
Quanta Computer Inc.	PROJECT : ZAW		
Size	Document Number: KBC IT8987		Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 34 of 48		

USB Board



check pin link to EC pin

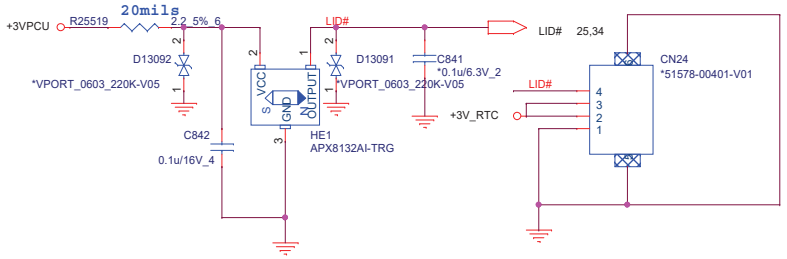
USB2.0 DB (UB2)



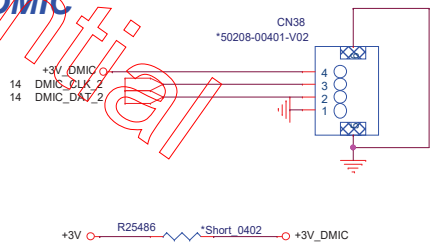
control with USB3

Enable: Low Active /2.5A
BCD:AL002822000
GMT:AL000524007

Hall Sensor



DMIC



Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	USB DB/Hall sensor/DMIC	1A
Date: Wednesday, February 27, 2019	Sheet 35 of 48	

Double Check ADP-IN Connector with ME

PR23	UMA	DIS
	41.2K Ohm CS34122FB19	33.2K Ohm CS33322FB13
	78W	95W

(1) BQ24780S : 1 μA/W (default)
(2) RT3602AJ : PSYS = 3.2V

CS34122FB19 RES CHIP 41.2K 1/16W +-1%(0402) For 78W
CS33322FB13 RES CHIP 33.2K 1/16W +-1% (0402) For 95W
CS32742FB14 RES CHIP 27.4K 1/16W +-1% (0402) For 116W

ACDET=16.4V

Double Check if BI pin PU Low

Double Check BATT Connector with ME

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

ILIM=0.793V
Rsr = 0.01ohm

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: Charger (BQ24780S) | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 36 of 48

+VIN 25,36,38,39,40,41,42,43,44,45,46
+3VPCU 13,25,26,30,31,34,35,36
+5VPCU 24,26,38,46
VL 43

+5V 25,26,27,30,32,43
+5V_S5 24,29,35,39,40,41,42,44,45,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,38,39,40,43,44,45,46
+3V_S5 2,4,10,12,13,14,15,28,29,30,33,34,39,43

+3VPCU
3.3 Volt +/- 5%
TDC : 6A
Width : 240mil
FSW : 500KHZ

To Thermal Protection

(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V

LDO=3.3V/100mA

High frequency noise eliminate circuit

Power Auto Recovery

VCC=5V
(DON'T Connect to External Load)

TDC : 5.26A
PEAK : 7A
Width : 220mil

TDC : 3.27A
PEAK : 4.36A
Width : 140mil

Soft-Start

+5VPCU
5 Volt +/- 5%
TDC : 8A
Width : 320mil
FSW : 750KHZ

(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V

LDO=5V/100mA

VCC=5V
(DON'T Connect to External Load)

TDC : 4.13A
PEAK : 5.5A
Width : 180mil

TDC : 3.53A
PEAK : 4.7A
Width : 160mil

Soft-Start

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: SYSTEM 5V/3V (RT6256B/RT6258C) | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 37 of 48

+VIN 25,36,37,39,40,41,42,43,44,45,46
+1.05V_DEEP_SUS 9,15
+5VPCU 24,26,37,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,39,40,43,44,45,46
+1V_SUS 6,40
+VCCIO 2,6,36,40,43

Fsw=550KHz

PR268 73.2K_1%_4
PC221 *0.01u/50V_4
G5335-TON-1
PU16
TON
PC81 *0.1u/25V_4
PC218 220p/50V_4
PC217 10u/25V_8
+VIN

+5VPCU
PR104 10_5%_6
G5335-VCC-1
NC
VCC
V+#1
V+#2
V+#3
V+#4
PC234 10u/6.3V_6

Double check PU high with HW
+3V
PR275 100K_1%_2
34 HWPG_1VS5
PR276 *Short_0201
G5335-PWRGD-1
PGOOD
+5VPCU
PR98 *0_5%_2
G5335-PFM-1
PFM
G5335-AGND-1
PR272 *Short_0201
Pulse-Skipping Mode
G5335-EN-1
EN

BST
G5335-BST-1
PR277 2.2_5%_6
PC235 0.1u/25V_4
LX#1
LX#2
LX#3
LX#4
LX#5
LX#6
G5335-LX-1
PL12 0.68uH/15.5A_7x7x3
PR99 *4.7_5%_6
PC82 *680p/50V_6

PGND#1
PGND#2
PGND#3
PGND#4
PGND#5
AGND
G5335-AGND-1

34 +1V_S5_ON
PR274 *Short_0201
G5335-SS-1
SS
FB
G5335-FB-1
PC228 *0.047u/6.3V_2
PC232 0.047u/6.3V_2
G5335QT2U
G5335-AGND-1 G5335-AGND-1

PR273 *Short_0402
G5335-AGND-1

PC230 22u/6.3V_6
PC222 22u/6.3V_6
PC227 22u/6.3V_6
PC220 22u/6.3V_6
PC224 22u/6.3V_6
PC219 *22u/6.3V_6
PC231 *22u/6.3V_6
PC233 0.1u/16V_4

PR9259 *short_2
R1
PR269 SP@6.34K_1%_4
PC225 *1000p/50V_4
R2
PR270 20K_1%_4
G5335-AGND-1

PJ3005 *short3720
+1.05V_DEEP_SUS
+1V_S5

Vo=0.8*(R1+R2)/R2
=1.0V

VFB=0.8V

Default Setting

	KBL U22	KBL U42	WHL U42/CML
R1	4.99K Ohm	4.99K Ohm	6.34K Ohm
	CS24992FB26	CS24992FB26	CS26342FB27
	1.0V	1.0V	1.05V

+1V_S5
1.0 Volt +/- 5%
TDC : 8.09A
Width : 340mil

Follow ZAV +VCCIO design

Delete

CPU_C10_GATE#_R PR9272 *0_5%_2
15,34,39 SUSON
PR9258 *Short_0201
PQ7 DDTC144EUA-7-F

+VIN
PR79 1M_5%_6
PR80 1M_5%_6
+1V_SUS
PR105 22_5%_8
PQ10 2N7002K
PQ25 2N7002K

+VIN
PR191 1M_5%_6
SUSD
PQ11 AO3404
+1V_SUS
PC152 *2200p/50V_4
+1.05V_DEEP_SUS
PC83 22u/6.3V_6

TDC : 0.19A
PEAK : 0.25A
Width : 20mil

ZAV add cap

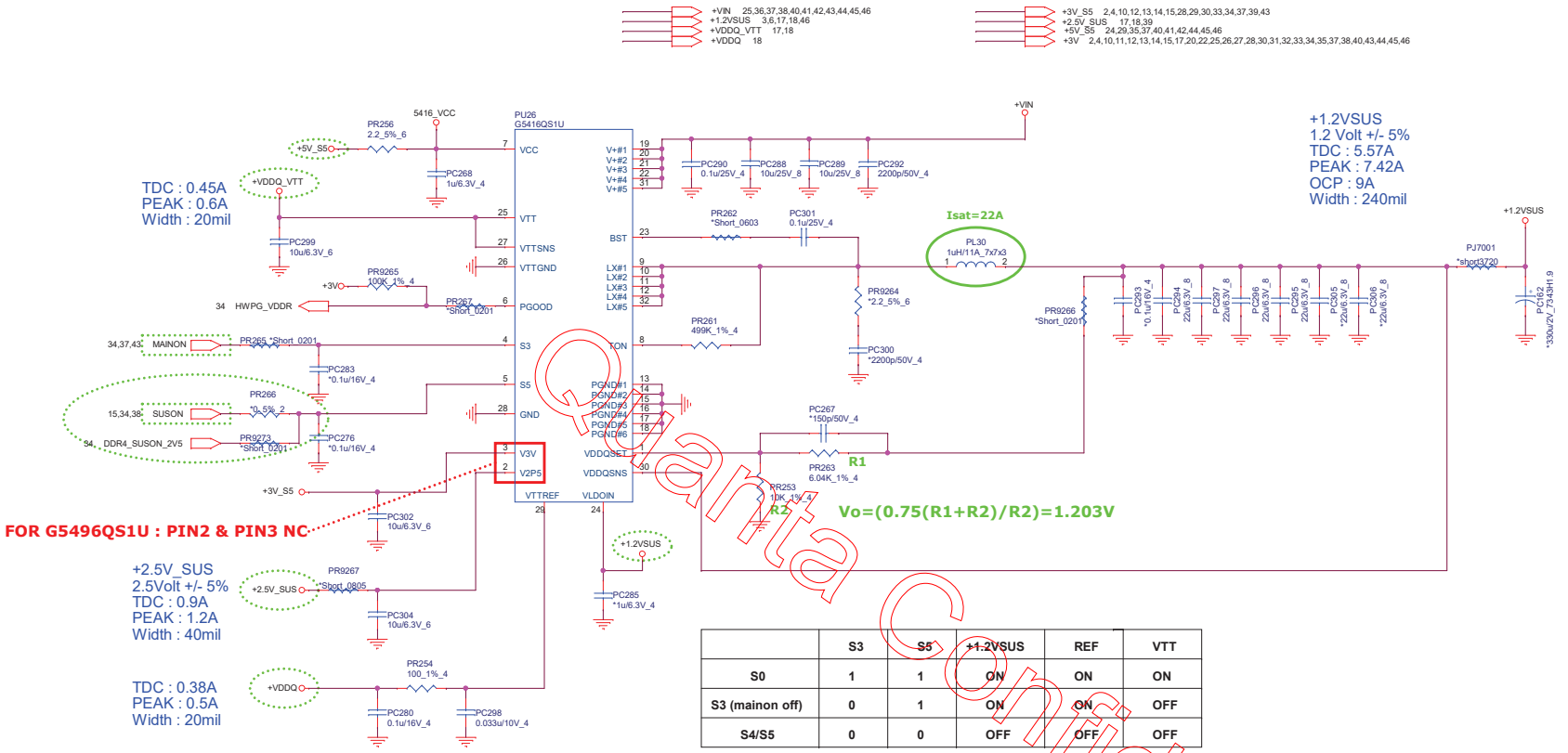
13 CPU_C10_GATE#_R
43 MAIND
PR2060 *Short_0201
PQ35 AON7408
+1.05V_DEEP_SUS
+VCCIO
PC236 *22u/6.3V_6

TDC : 3.6A
PEAK : 4.8A
Width : 160mil

Quanta Computer Inc.
PROJECT : ZAW

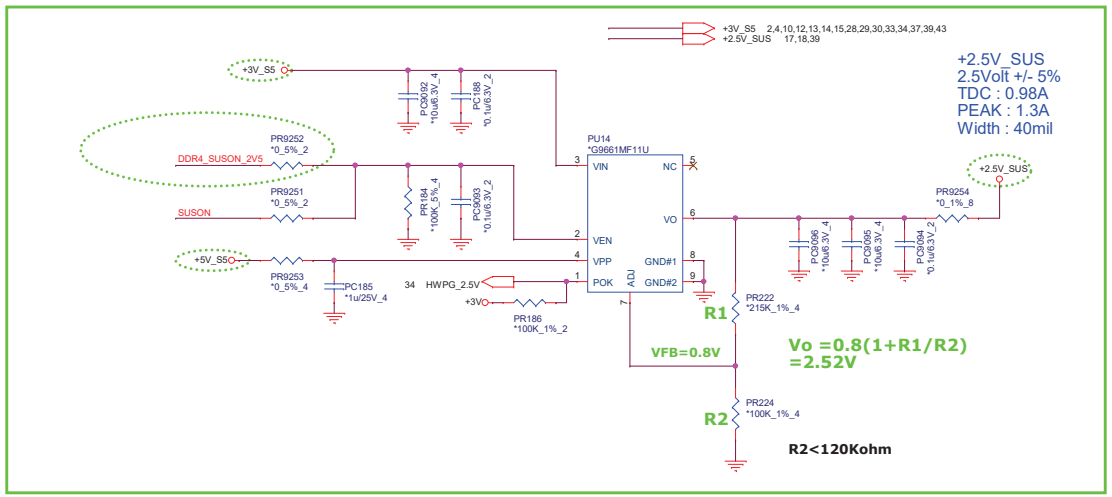
Size	Document Number	Rev
	+1V_S5 (G5335QT2U)	1A

Date: Wednesday, February 27, 2019 Sheet 38 of 48

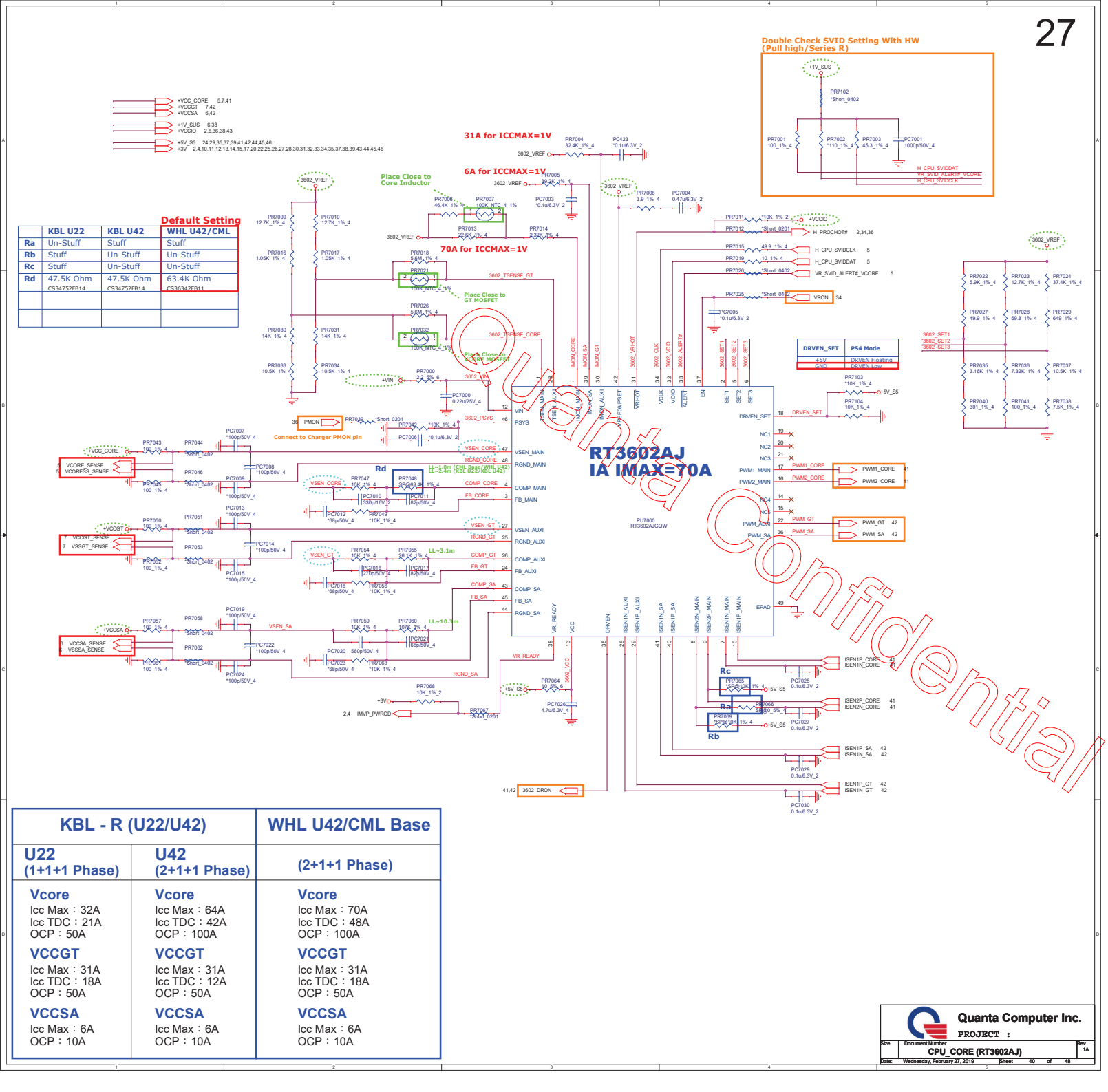


	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



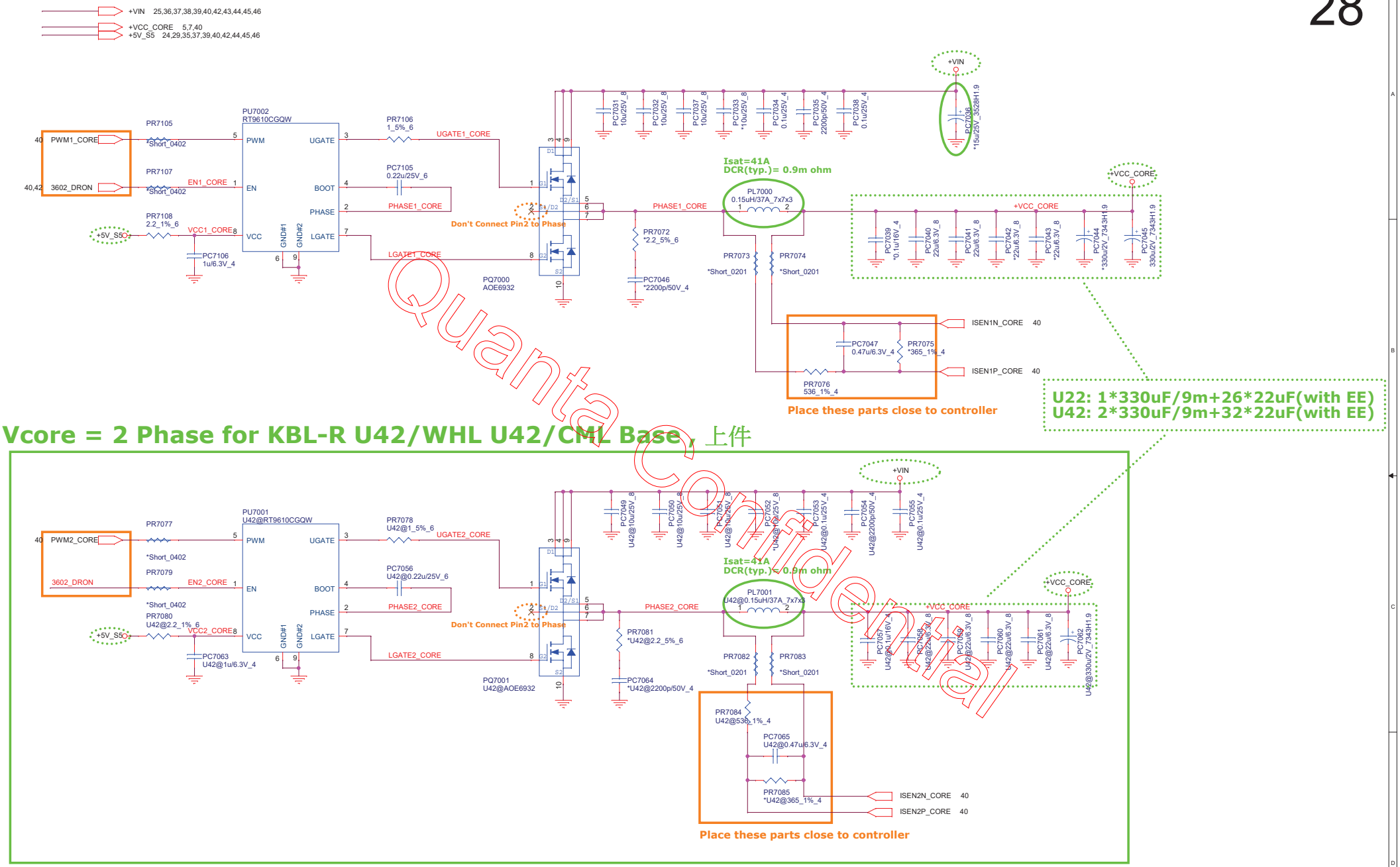
Quanta Computer Inc.	
PROJECT : ZAW	
Size	Document Number: DDR4_+1.2VSUS (G5416QS1U) — Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 39 of 48



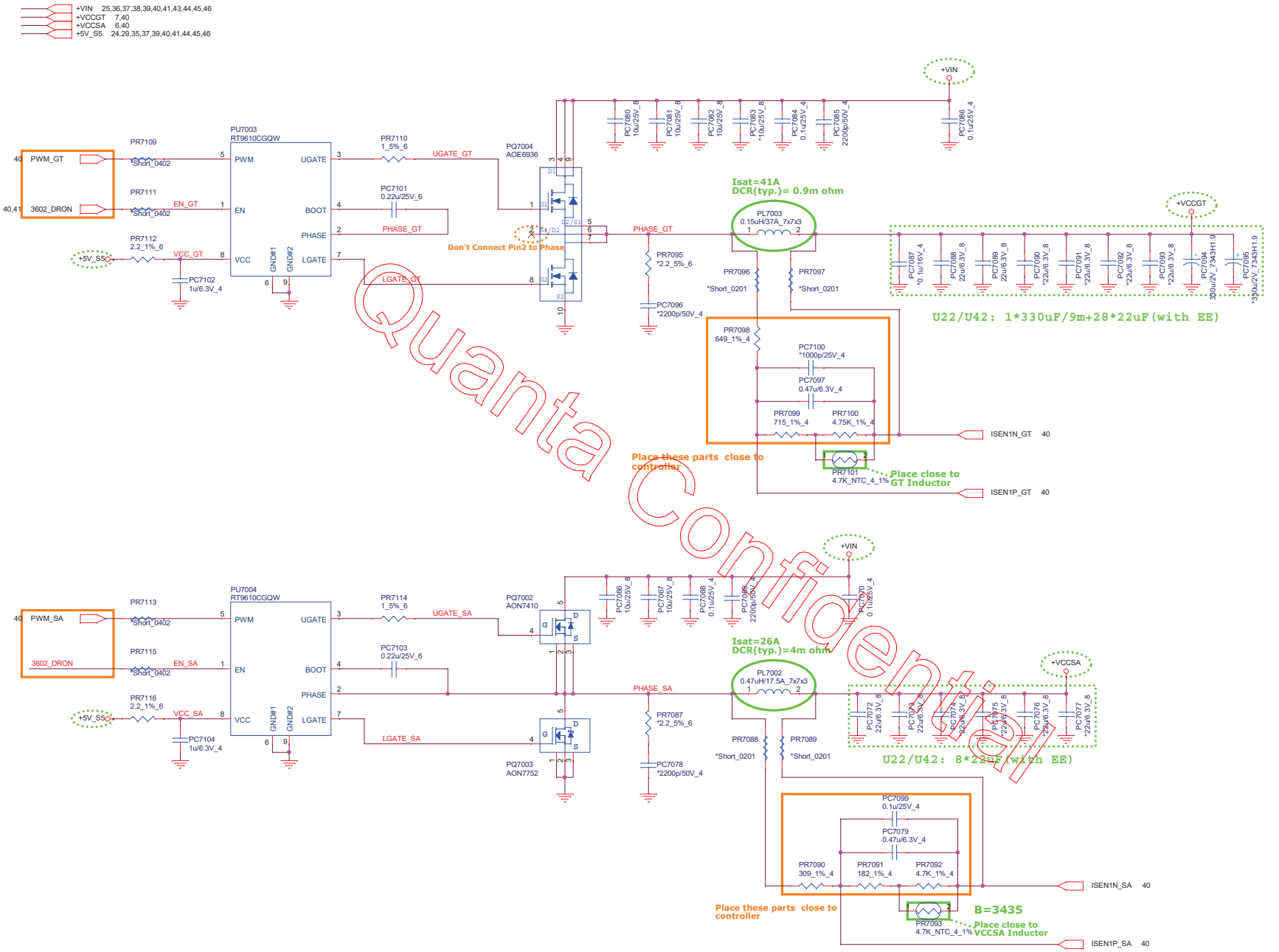
	KBL U22	KBL U42	WHL U42/CML
Ra	Un-Stuff	Stuff	Stuff
Rb	Stuff	Un-Stuff	Un-Stuff
Rc	Stuff	Un-Stuff	Un-Stuff
Rd	47.5K Ohm CS34752FB14	47.5K Ohm CS34752FB14	63.4K Ohm CS36342FB11

KBL - R (U22/U42)		WHL U42/CML Base
U22 (1+1+1 Phase)	**U42 (2+1+1 Phase)**	**(2+1+1 Phase)**
Vcore Icc Max：32A Icc TDC：21A OCP：50A	**Vcore** Icc Max：64A Icc TDC：42A OCP：100A	**Vcore** Icc Max：70A Icc TDC：48A OCP：100A
VCCGT Icc Max：31A Icc TDC：18A OCP：50A	**VCCGT** Icc Max：31A Icc TDC：12A OCP：50A	**VCCGT** Icc Max：31A Icc TDC：18A OCP：50A
VCCSA Icc Max：6A OCP：10A	**VCCSA** Icc Max：6A OCP：10A	**VCCSA** Icc Max：6A OCP：10A

Quanta Computer Inc.
PROJECT :
Size | Document Number | Rev
CPU_CORE (RT3602AJ) | 1A
Date: Wednesday, February 27, 2019 | Sheet 40 of 48



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: +VCC_CORE	Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 41 of 48	



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: VCCGT/VCCSA	Rev: 1A
Date: Wednesday, February 27, 2019	Sheet 42 of 48	

+3V_S5 2,4,10,12,13,14,15,28,29,30,33,34,37,39
+1.8V_S5 15,29,46
+1.8V 26,29
+1.5V 26
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,44,45,46
VL 37

+VIN 25,36,37,38,39,40,41,42,44,45,46
+5V 25,26,27,30,32,37
+VCCIO 2,6,36,38,40

+1.8V_S5
1.8Volt +/- 5%
TDC : 2.48A
PEAK : 3.3A
Width : 100mil

Double check PU high with HW

PU3004 JW5213DFND_TRPBF
PL551 1uH/3.35A_2.5x2.0x1.2
PJ9005 *short3720
PR568 20K_1%_4
PR567 10K_1%_4
Vo=0.6*(R1+R2)/R2
=1.8V

TDC : 0.3A
PEAK : 0.4A
Width : 20mil

Double check PU high with HW

PU3003 JW5222RSOTB_TRPBF
PL14 2.2uH/1.67A_2.5x2.0x1.2
PJ3008 *short3720
PR6418 22.6K_1%_4
PR283 15K_1%_4
Vo=(0.6(R1+R2)/R2)
=1.504V

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

Thermal protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C

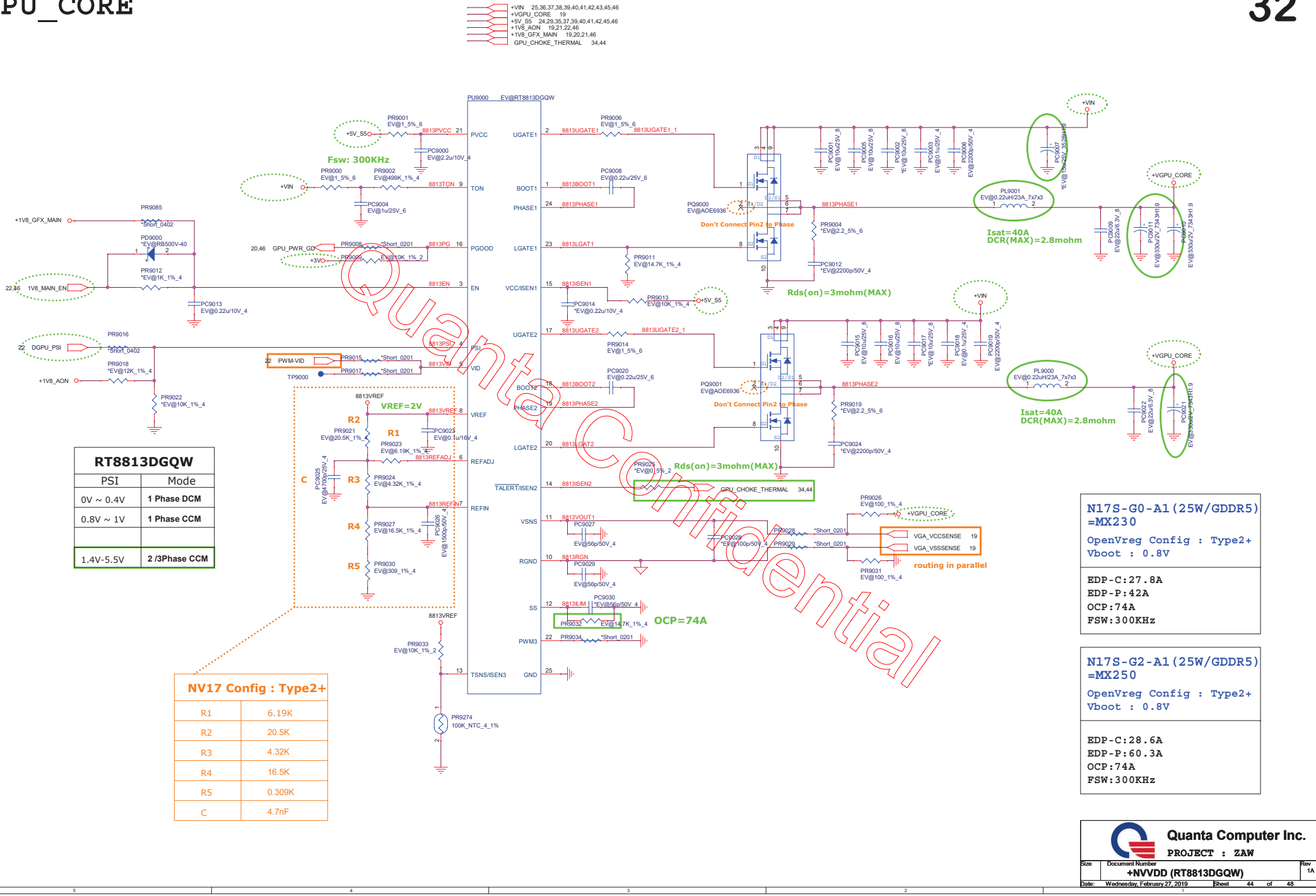
PU3002 TMP708AIDBVR
PR3020 150_5%_4
PR3021 29.4K_1%_4
PR3022 *Short_0201
Rset(Kohm)=0.0012T*T-0.9308T+96.147
=29.4K ohm
HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

PR126 Change to 220 ohm for bo bo sound issue.

ZAV:Stuff

Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: +1.8V_S5/+1.5V/Thermal Protect | Rev 1A
Date: Wednesday, February 27, 2019 | Sheet 43 of 48

VGPU_CORE



RT8813DGQW	
PSI	Mode
0V ~ 0.4V	1 Phase DCM
0.8V ~ 1V	1 Phase CCM
1.4V-5.5V	2 /3Phase CCM

NV17 Config : Type2+	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N17S-G0-A1(25W/GDDR5)
=MX230

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:27.8A
EDP-P:42A
OCP:74A
FSW:300KHz

N17S-G2-A1(25W/GDDR5)
=MX250

OpenVreg Config : Type2+
Vboot : 0.8V

EDP-C:28.6A
EDP-P:60.3A
OCP:74A
FSW:300KHz

Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	+NVVDD (RT8813DGQW)	1A
Date: Wednesday, February 27, 2019	Sheet 44 of 48	

1.35V_GFX

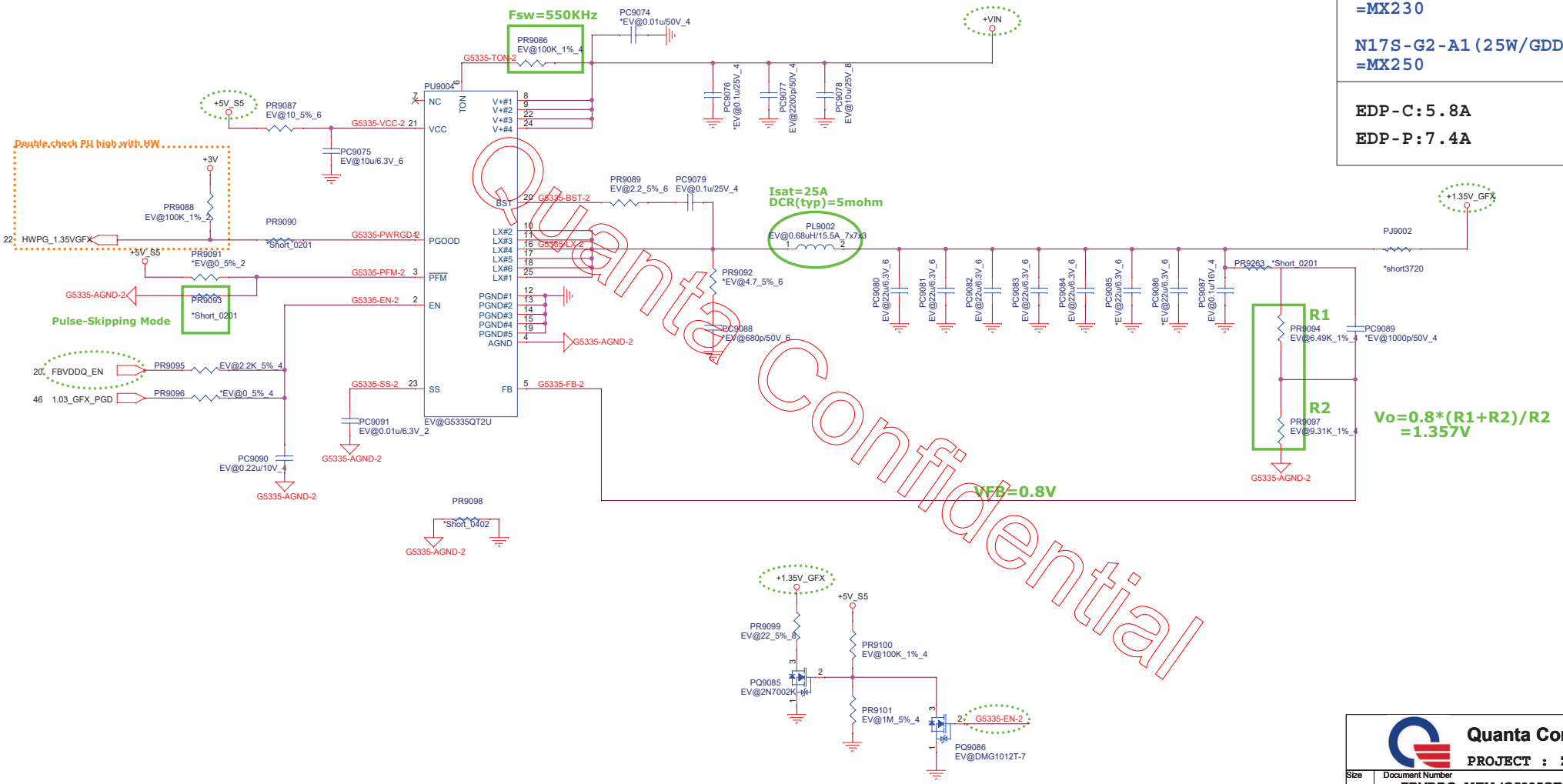
+VIN 25,36,37,38,39,40,41,42,43,44,46
+1.35V_GFX 20,23
+5V_S5 24,29,35,37,39,40,41,42,44,46
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,46

N17S-G0-A1(25W/GDDR5)
=MX230

N17S-G2-A1(25W/GDDR5)
=MX250

EDP-C:5.8A

EDP-P:7.4A



Quanta Computer Inc.
PROJECT : ZAW

Size	Document Number	Rev
	+FBVDDQ_MEM (G5335QT2U)	1A

Date: Wednesday, February 27, 2019 Sheet 45 of 48

+1.8V_S5 15,29,43
+1V8_GFX_MAIN 19,20,21,44
+1V8_AON 19,21,22,44
+5VPCU 24,26,37,38
+VIN 25,36,37,38,39,40,41,42,43,44,45

+1.2VSUS 3,6,17,18,39
+1.03_GFX 19
+5V_S5 24,29,35,37,39,40,41,42,44,45
+3V 2,4,10,11,12,13,14,15,17,20,22,25,26,27,28,30,31,32,33,34,35,37,38,39,40,43,44,45

N17S-G0
N17S-G2

+1.8V_MAIN
TDC : 0.9A
PEAK : 1.2A
Width : 40mil

N17S-G0
N17S-G2

+1.8V_AON
TDC : 0.75A
PEAK : 1A
Width : 40mil

N17S-G0
N17S-G2

+1V
TDC : 0.9A
PEAK : 1.1A
Width : 40mil

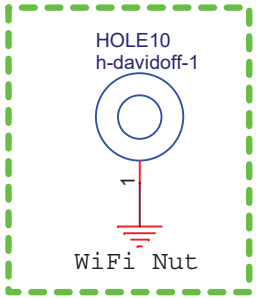
Double check PU high with HW

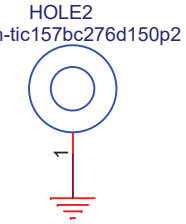
N17S : Vo=(1+R1/R2)*0.5=1.03V

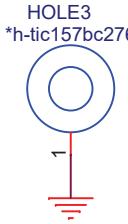
	R1	R2
N17S	133 ohm	124 ohm

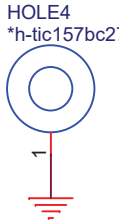
Quanta Computer Inc.
PROJECT : ZAW
Size | Document Number: +1.8V_AON/+1V_GFX (AOZ1331DI) | Rev: 1A
Date: Wednesday, February 27, 2019 | Sheet 46 of 48

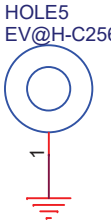
Hole

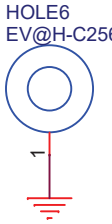


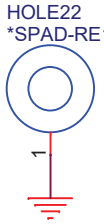


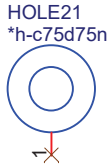


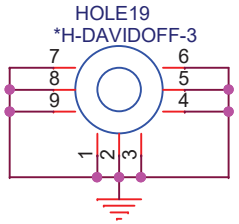


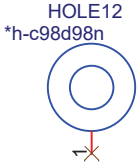


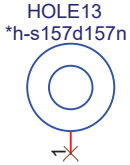


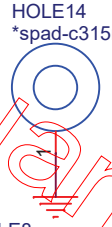


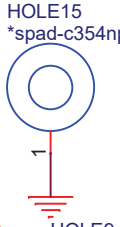


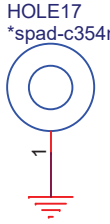


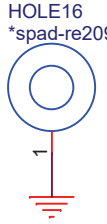


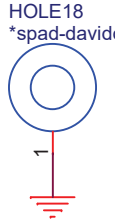


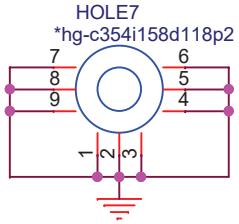


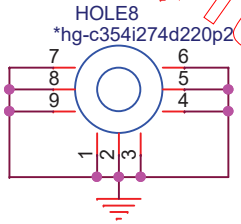


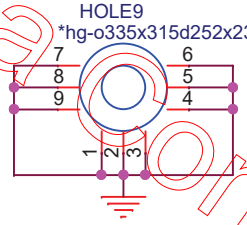


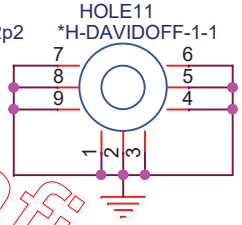


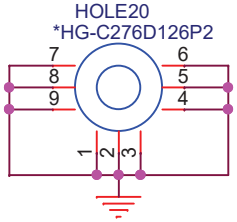


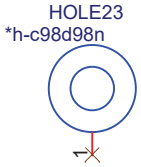


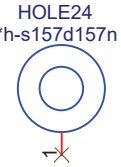








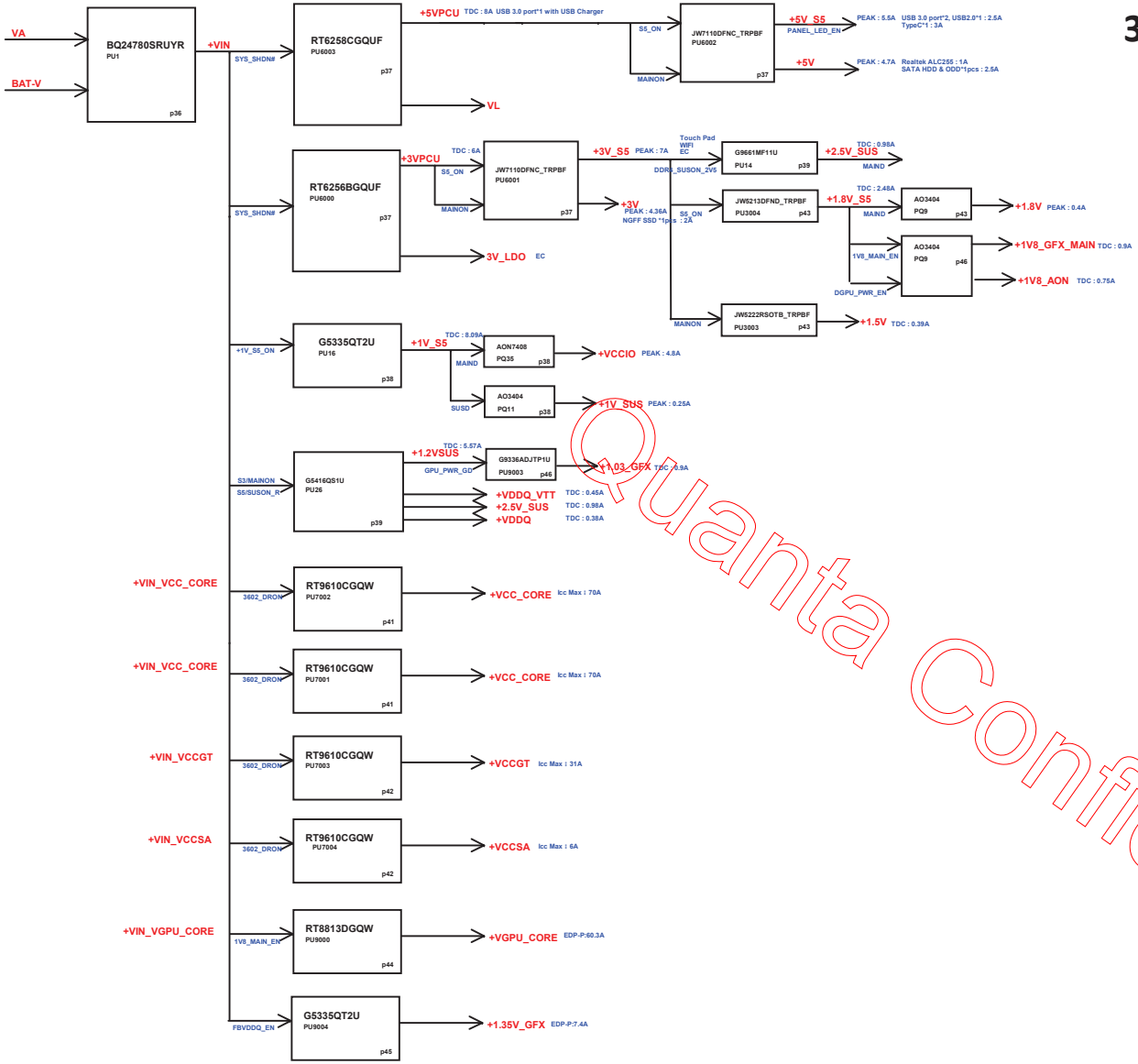




Quanta Computer Inc.

PROJECT : ZAW

Size	Document Number	Rev
	Hole	1A
Date: Wednesday, February 27, 2019	Sheet 47 of 48	



Quanta Computer Inc.
PROJECT : ZAU
Size | Document Number | Rev 1A
Power Tree
Date: Wednesday, February 27, 2019 | Sheet 48 of 48