Foxconn C51GM06

Fab :A

nVIDIA C51G (A01) + MCP51 (A01) Chipset for AMD M2 CPU

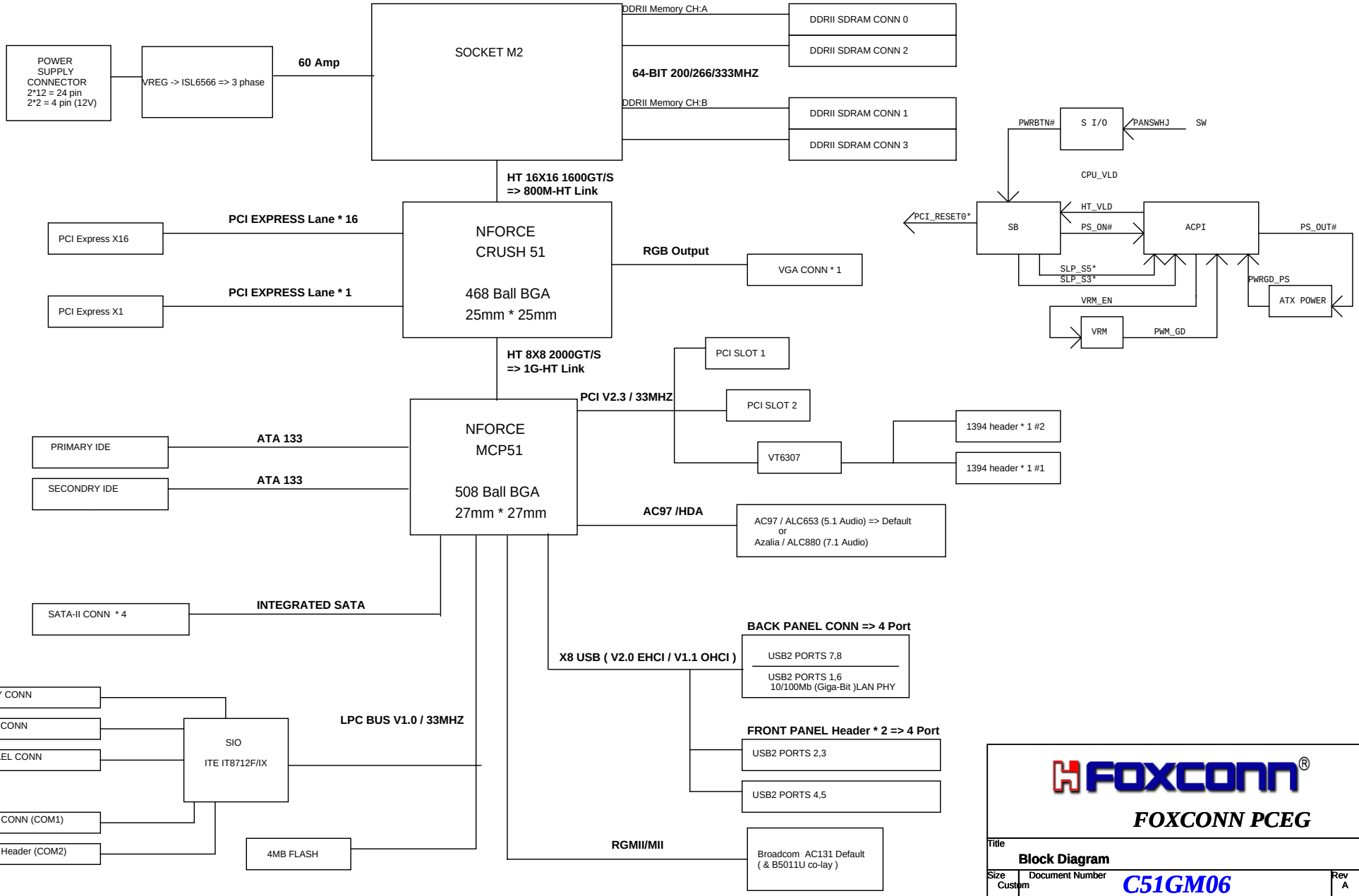
(Nov./23/2005)

FOXCONN®

FOXCONN PCEG

Title: Cover		
Size: C	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 1 of 38	

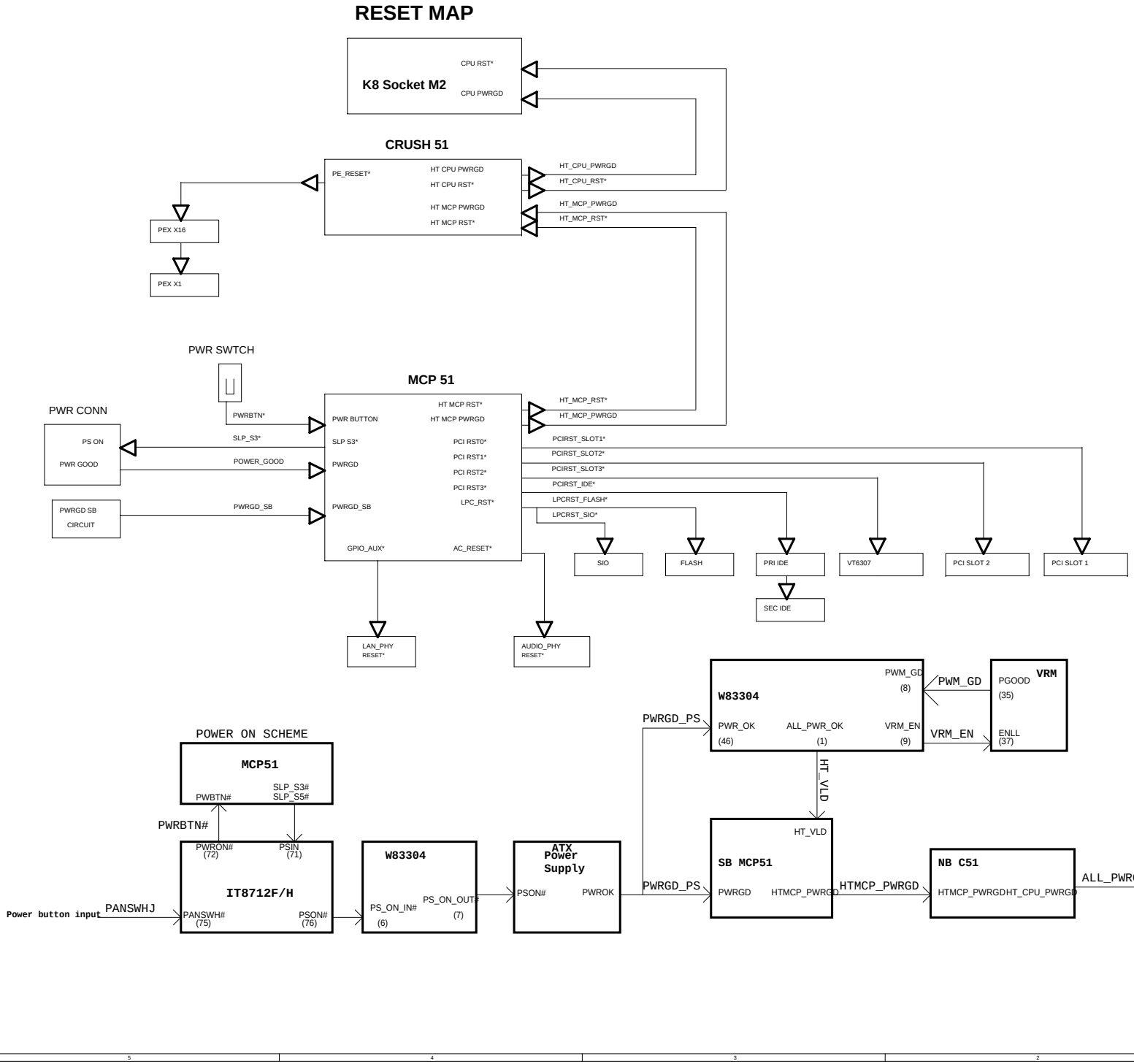
C51GM06 Block Diagram



FOXCONN PCEG

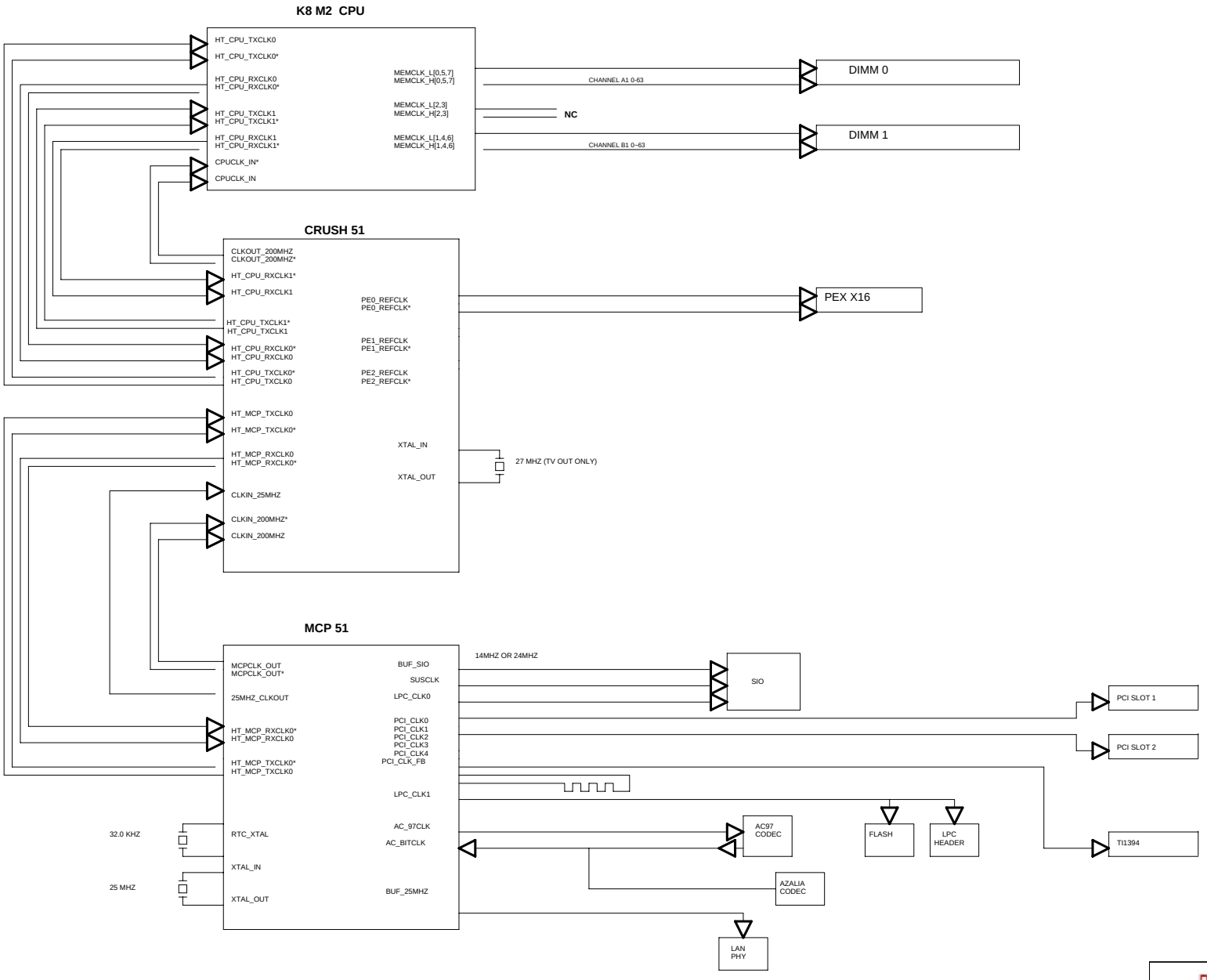
Title: Block Diagram		
Size: Custom	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 2 of 38	

RESET MAP



FOXCONN PCEG

Title	Reset Map	C51GM06
Size C	Document Number	Rev A
Date: Friday, April 14, 2006	Sheet 3 of 38	



FOXCONN PCEG

Title: Clock Distribution

Size: C | Document Number: C51GM06 | Rev: A

Date: Friday, April 14, 2006 | Sheet 4 of 38

CPU VID TABLE

VID [4..0]	VDD		VID [4..0]	VDD
0X00000	1.550V		0X10000	1.150V
0X00001	1.525V		0X10001	1.125V
0X00010	1.500V		0X10010	1.100V
0X00011	1.475V		0X10011	1.075V
0X00100	1.450V		0X10100	1.050V
0X00101	1.425V		0X10101	1.025V
0X00110	1.400V		0X10110	1.000V
0X00111	1.375V		0X10111	0.975V
0X01000	1.350V		0X11000	0.950V
0X01001	1.325V		0X11001	0.925V
0X01010	1.300V		0X11010	0.900V
0X01011	1.275V		0X11011	0.875V
0X01100	1.250V		0X11100	0.850V
0X01101	1.225V		0X11101	0.825V
0X01110	1.200V		0X11110	0.800V
0X01111	1.175V		0X11111	OFF

SMBUS ADDRESS MAP

DEVICE	SMBUS #	ADDRESS
DIMM 0	0	1010 000 = 0X50
DIMM 1	0	1010 001 = 0X51
DIMM 2	0	1010 010 = 0X52
DIMM 3	0	1010 011 = 0X53
SIO	1	0101 101 = 0X2D
PCI SLOT 1	1	ARP
PCI SLOT 2	1	ARP
TI 1394	1	ARP
DDC BUS	A	?
DDC BUS	B	?

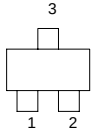
PCI INTERRUPT/IDSEL MAP

BACK PANEL SLOT	PCI BUS#	DEVICE#	IDSEL PIN	PCI SLOT INTA*	PCI SLOT INTB*	PCI SLOT INTC*	PCI SLOT INTD*	REQ/GNT
VT6307	01	0X06	22	P_INTZ*				1/1
PCI 2	01	0X08	23	P_INTW*	P_INTX*	P_INTY*	P_INTZ*	2/2
PCI 1	01	0X09	24	P_INTX*	P_INTY*	P_INTZ*	P_INTW*	3/3

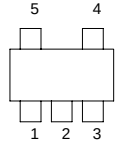
PCI DEVICE MAP

DEVICE	PCI BUS#	DEVICE#	FUNCTION	DEVICE ID
MCP 51	MCP51 LOGICAL PCI BUS 0	0X01-0X0F	--	--
MAC /MAC	0	XA	0	0X56/57
PCI-PCI BRIDGE	0	X9	0	0X005C
SATA1	0	X8	0	0X0055
SATA0	0	X8	0	0X0054
IDE	0	X6	0	0X0053
MODEM CODEC	0	X4	1	0X0058
AUDIO CODEC	0	X4	0	0X0059
USB 2.0	0	X2	1	0X005B
USB 1.1	0	X2	0	0X005A
SHAPE TRIM	0	X1	2	0X005F
LDT	0	X0	0	0X005E
SMBUS2	0	X1	1	0X0052
LEGACY SLAVE	0	?	?	0X00D3
LPC	0	X1	0	0X0050/51
LOGICAL PCI BUS	1	?	?	?
PCI SLOT 1				
PCI SLOT 2				
PCI SLOT 3				
PCI SLOT 4				
PCI SLOT 5				

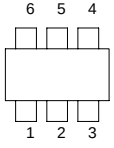
SOT23



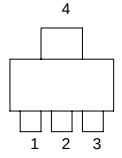
SOT23-5/SC70
SOT89-5



SOT23-6



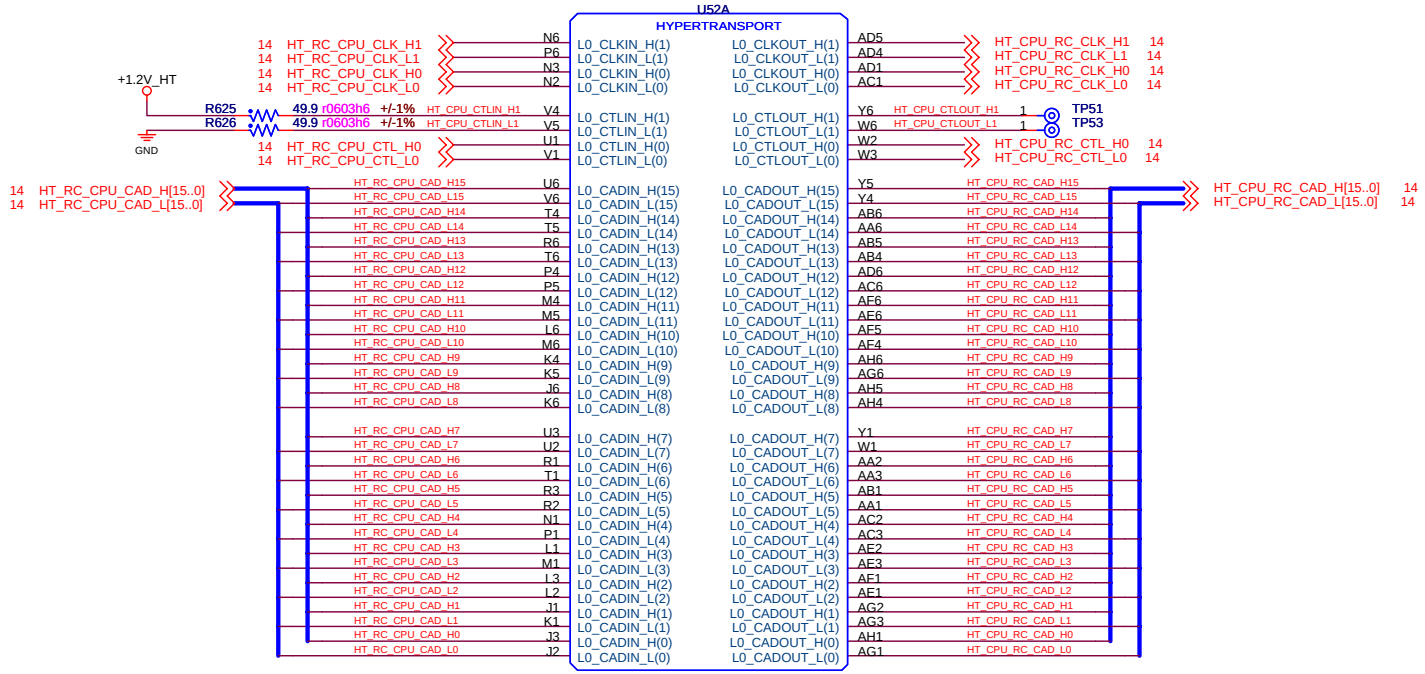
SOT223



FOXCONN®

FOXCONN PCEG

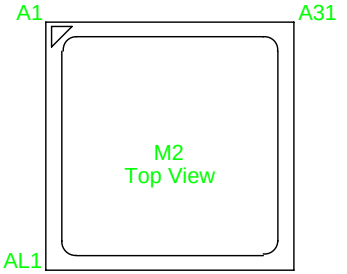
Title: PCI Device / VID Table		
Size: C	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 5 of 38	



Layout: Add stitching caps if crossing plane split

HyperTransport Net Naming Convention

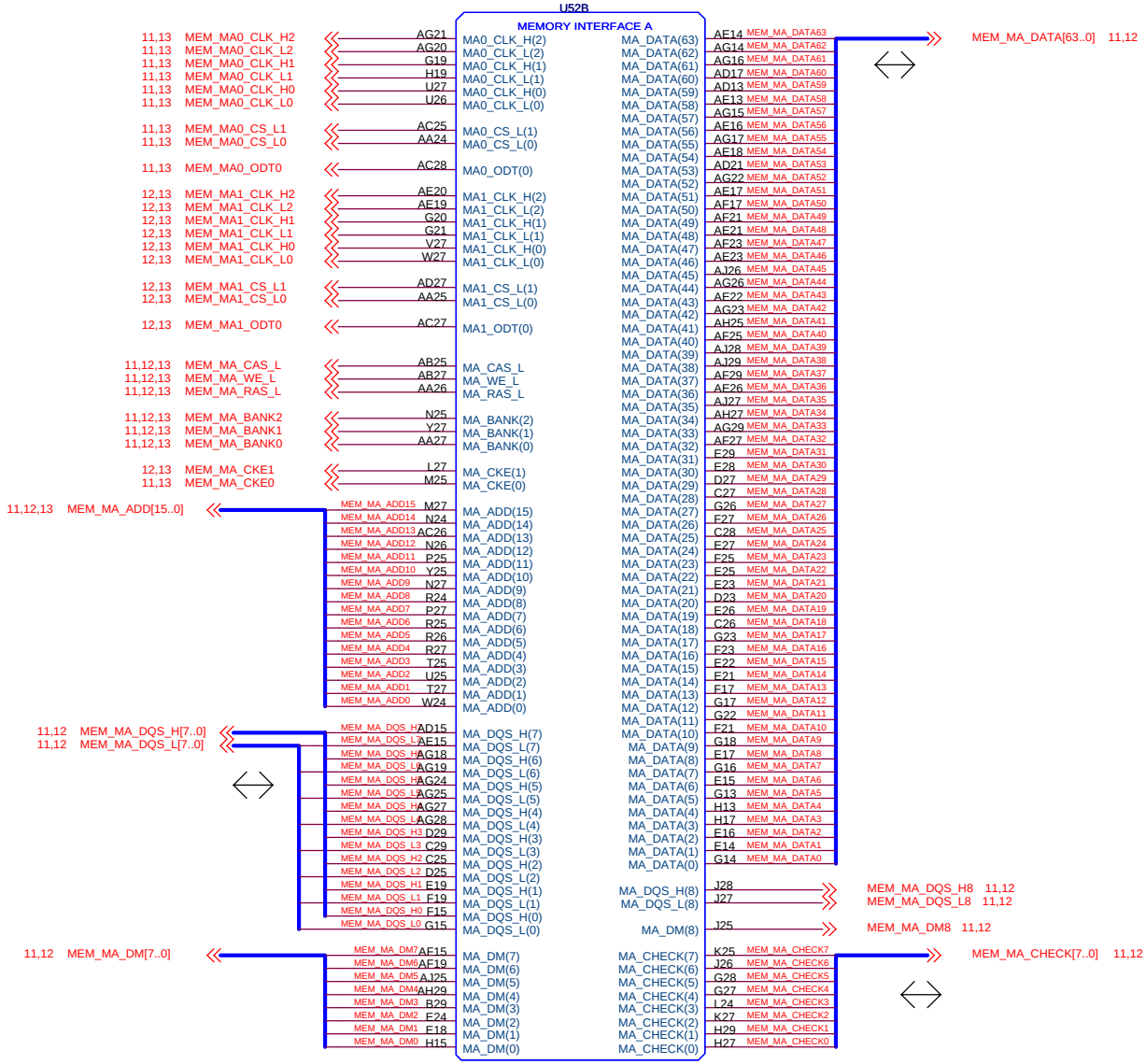
HT_"link driver"_"link receiver"_"function"_"polarity"_"number"



FOXCONN®

FOXCONN PCEG

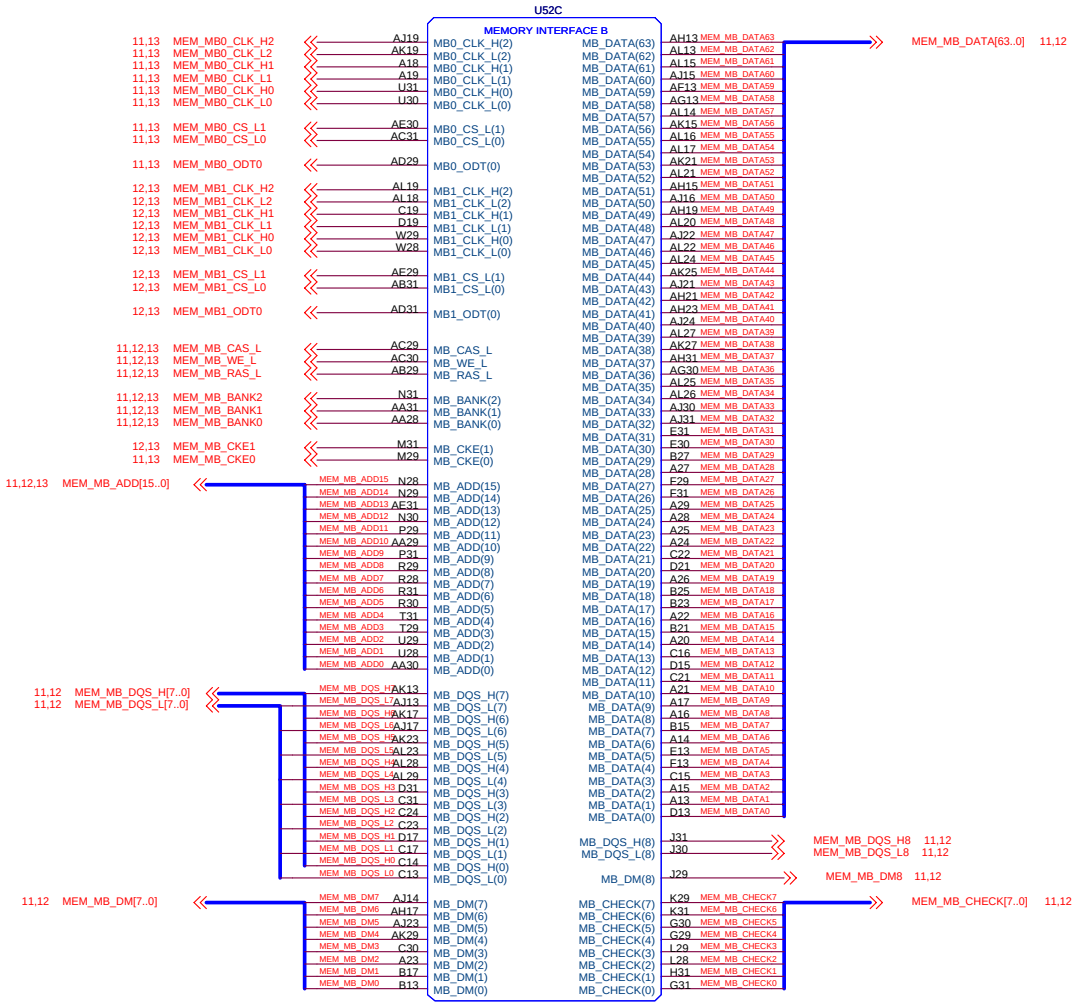
Title: Athlon 64-1 HyperTransport		
Size: B	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 6 of 38	



FOXCONN®

FOXCONN PCEG

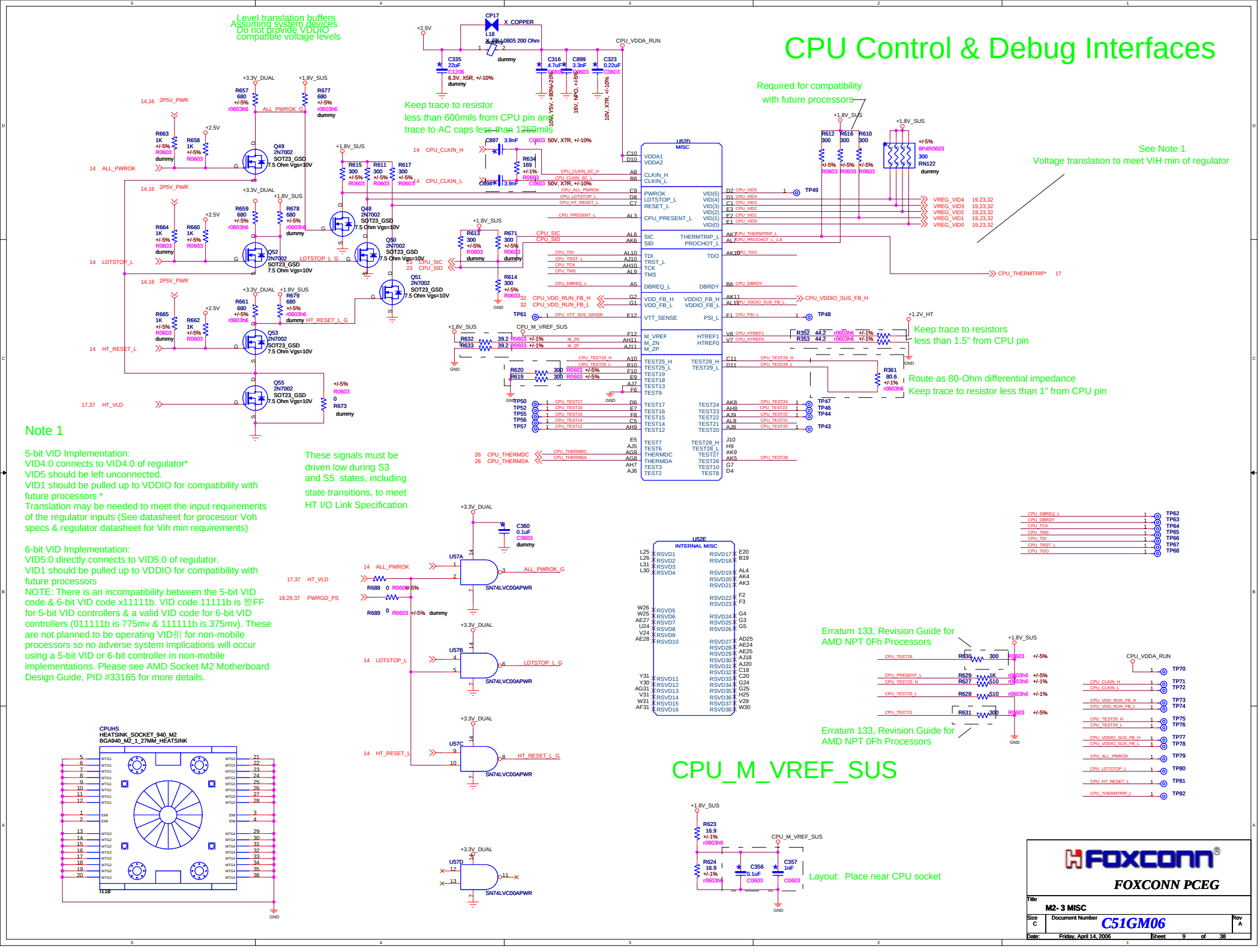
Title: Athlon 64- 2 DDR -1			
Size: Custom	Document Number: C51GM06		Rev: A
Date: Friday, April 14, 2006	Sheet 7 of 38		



FOXCONN PCEG

Title: M2- 2 DDR -2		
Size: Custom	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 8 of 38	

CPU Control & Debug Interfaces



Note 1

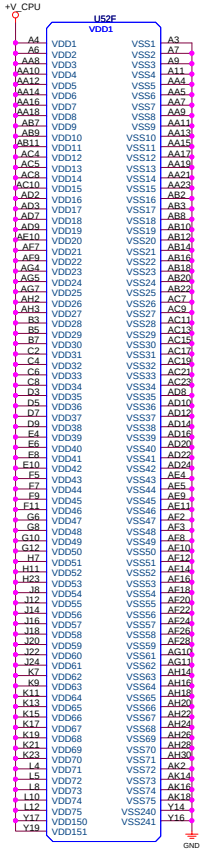
5-bit VID Implementation:
VID4:0 connects to VID4:0 of regulator*
VID5 should be left unconnected.
VID1 should be pulled up to VDDIO for compatibility with future processors *
Translation may be needed to meet the input requirements of the regulator inputs (See datasheet for processor Voh specs & regulator datasheet for Vih min requirements)

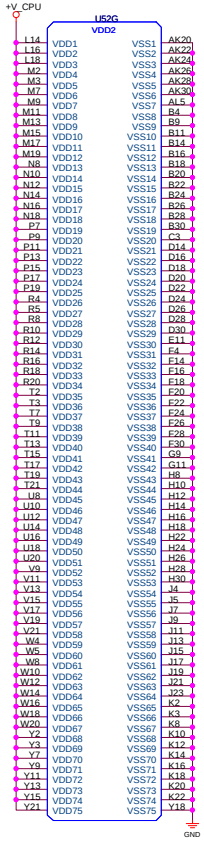
6-bit VID Implementation:
VID5:0 directly connects to VID5:0 of regulator.
VID1 should be pulled up to VDDIO for compatibility with future processors
NOTE: There is an incompatibility between the 5-bit VID code & 6-bit VID code x11111b. VID code 11111b is 為FF for 5-bit VID controllers & a valid VID code for 6-bit VID controllers (011111b is 775mv & 111111b is 375mv). These are not planned to be operating VID担 for non-mobile processors so no adverse system implications will occur using a 5-bit VID or 6-bit controller in non-mobile implementations. Please see AMD Socket M2 Motherboard Design Guide, PID #33165 for more details.

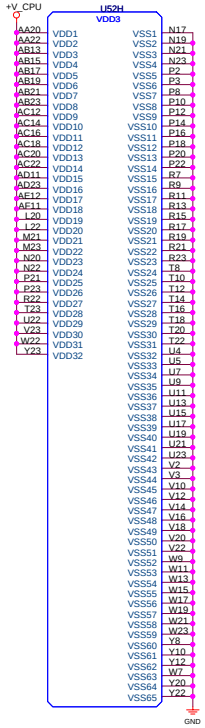
FOXCONN PCEG

Title: M2- 3 MISC			
Size: C	Document Number: C51GM06		Rev: A
Date: Friday, April 14, 2006		Sheet 9 of 38	

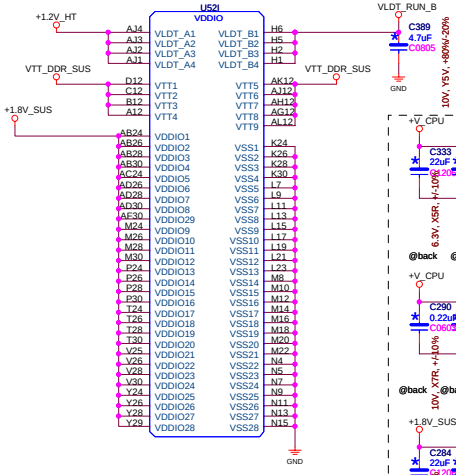
Processor Power & Ground



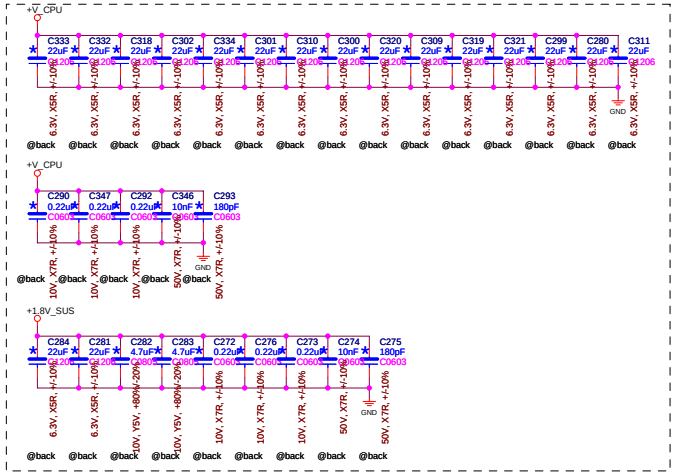




VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

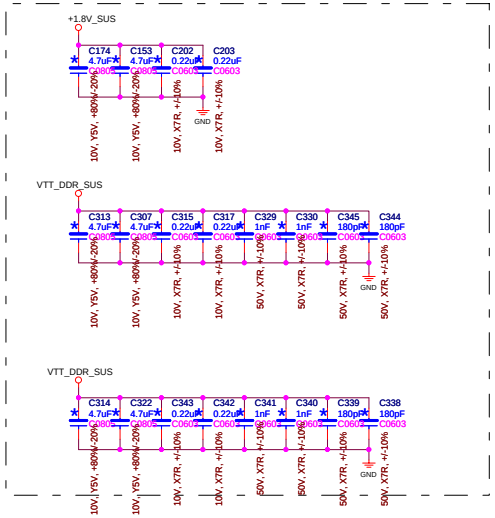


Bottomside Decoupling

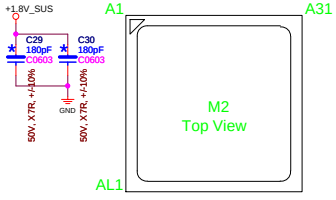


Decoupling Between Processor and DIMMs

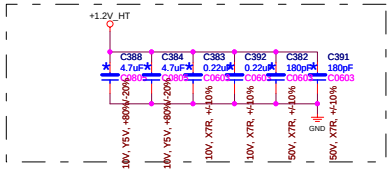
Place as close to processor as possible.



Decoupling Between Processor and DIMMs



Place near processor on VLDT pour.



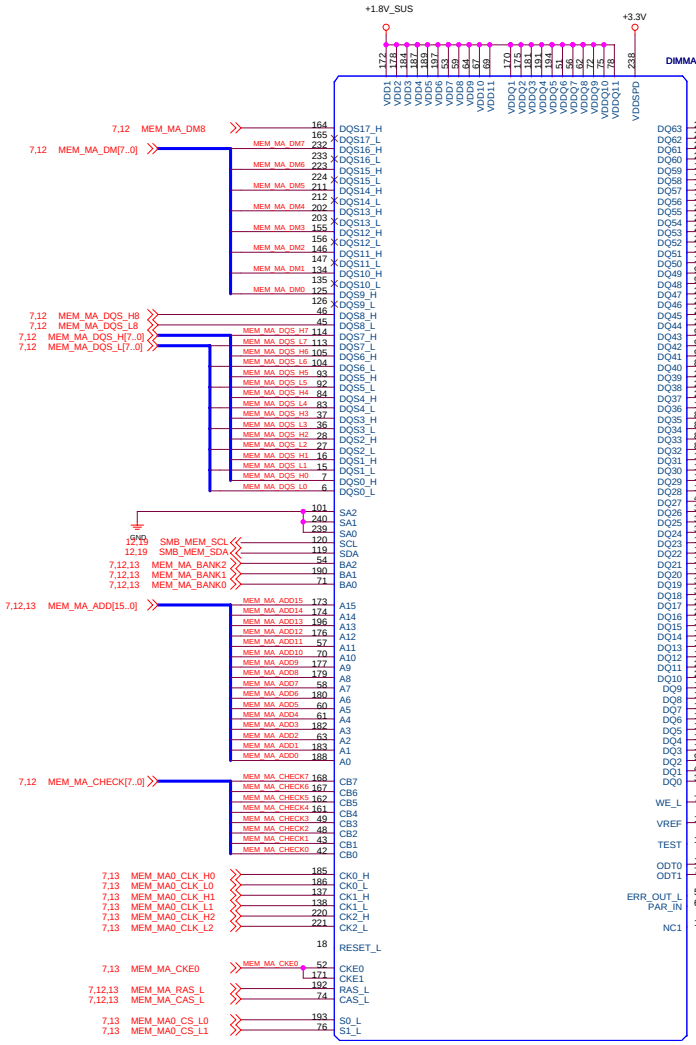
FOXCONN PCEG

Title	M2- 4 Power	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 10 of 38	

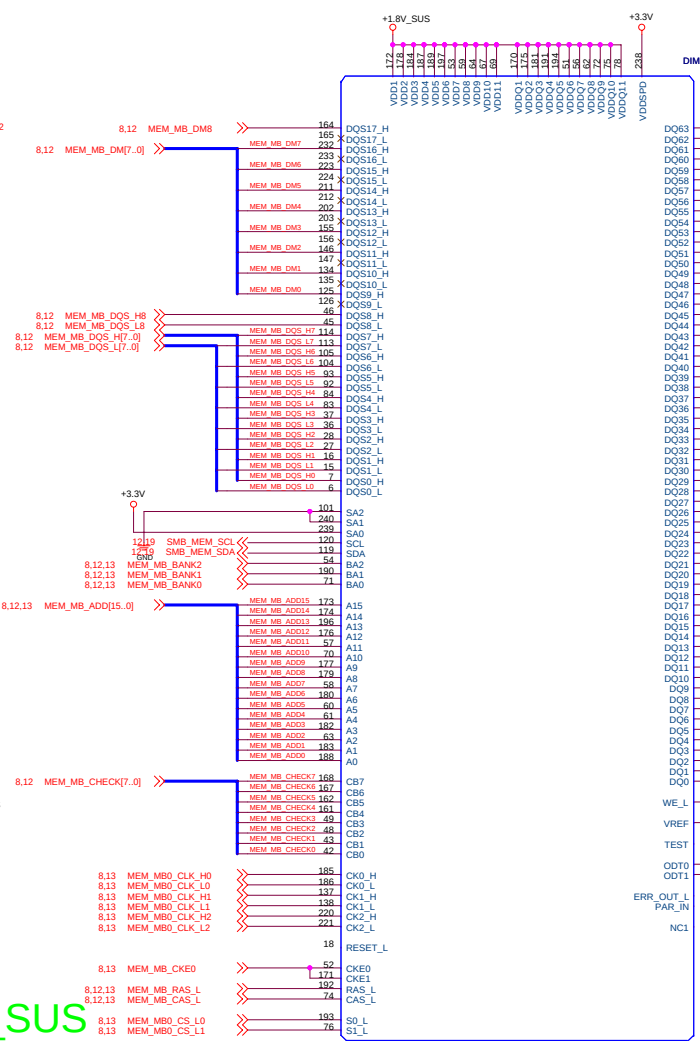
SMB_MEM BUS ADDRESS	
DIMM 0	1010 000
DIMM 1	1010 001
DIMM 2	1010 010
DIMM 3	1010 011

First Logical DDR2 DIMM

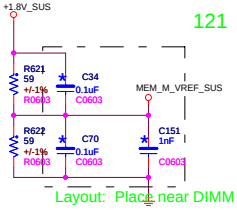
DIMMA0

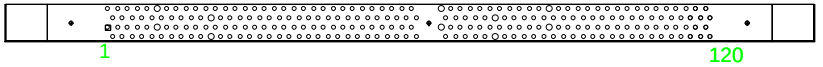


DIMMB0



MEM_M_VREF_SUS





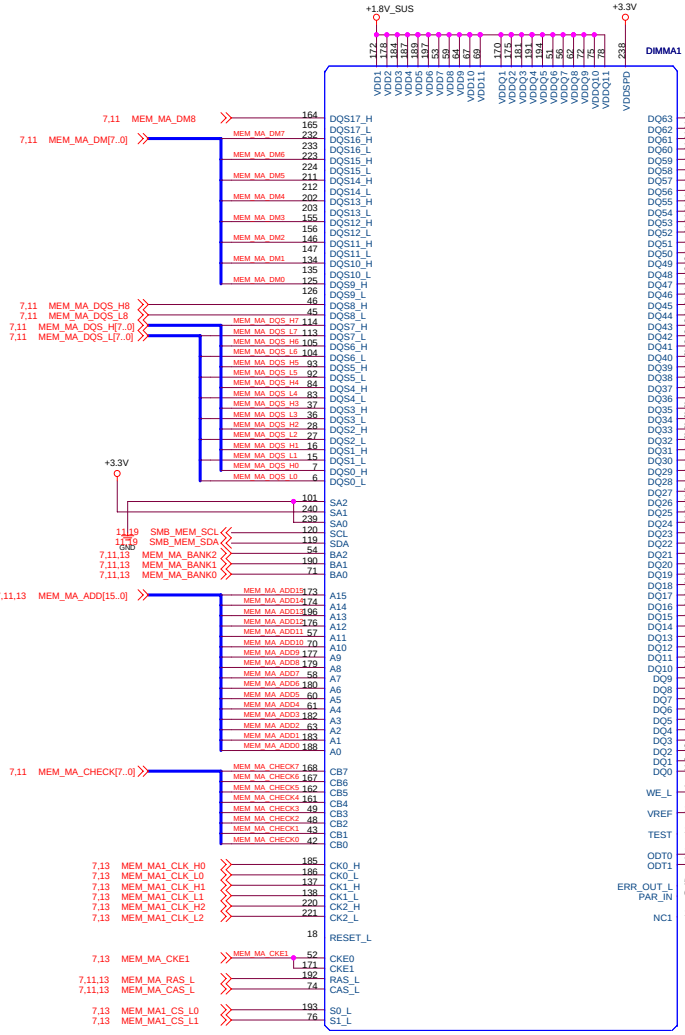
FOXCONN PCEG

Title	DDR SDRAM DIMM 1 - 2	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 11 of 38	

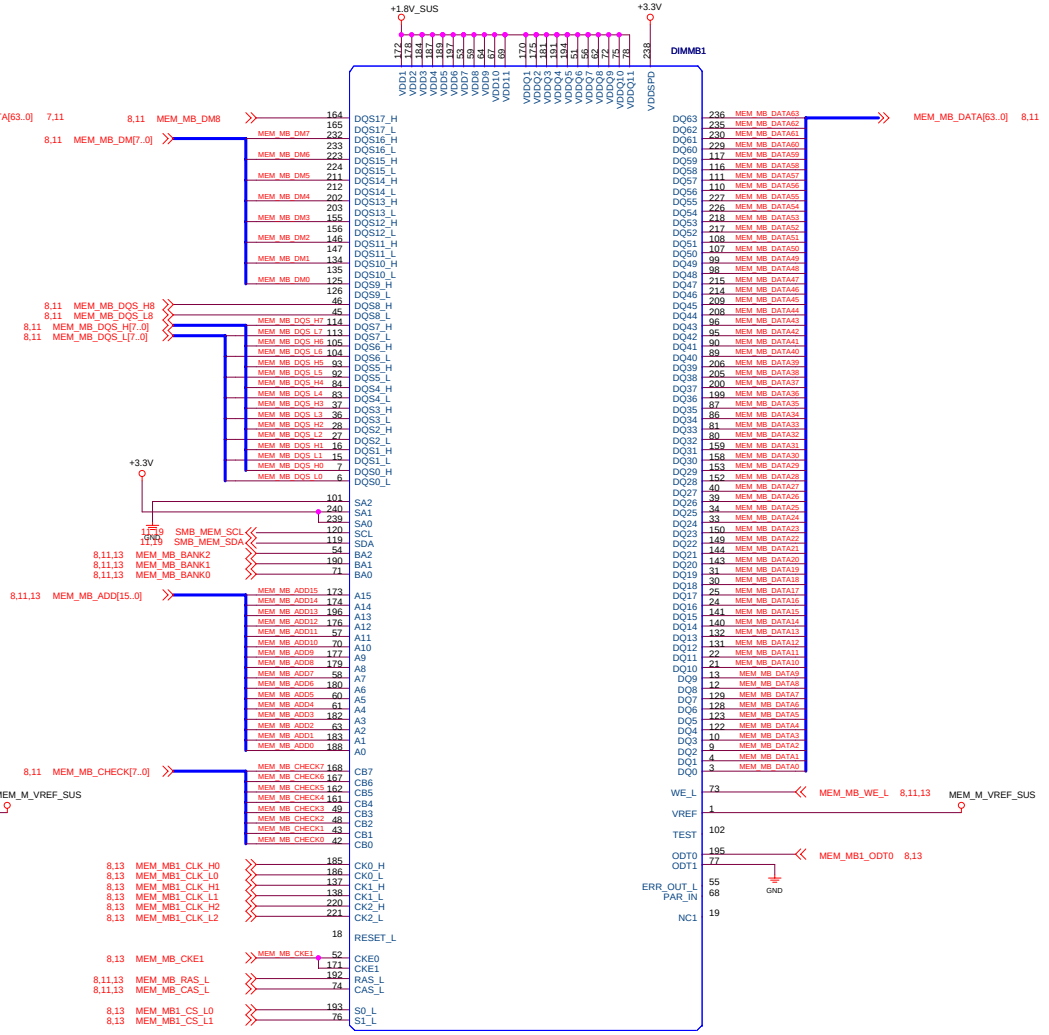
Second Logical DDR2 DIMM

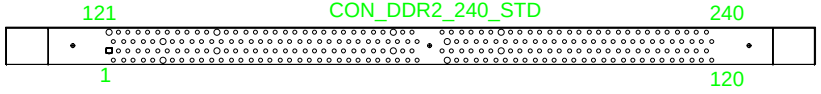
SMB_MEM BUS ADDRESS	
DIMM 0	1010 000
DIMM 1	1010 001
DIMM 2	1010 010
DIMM 3	1010 011

DIMMA1



DIMMB1





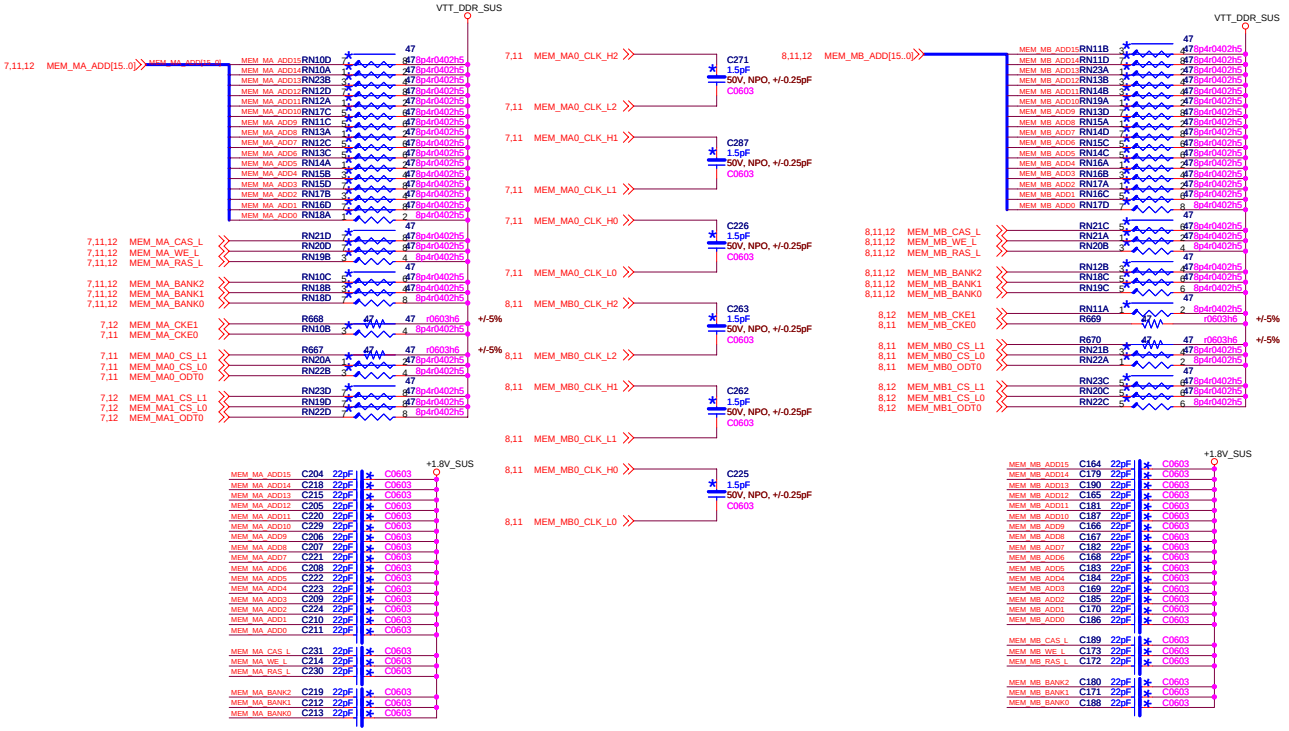
FOXCONN PCEG

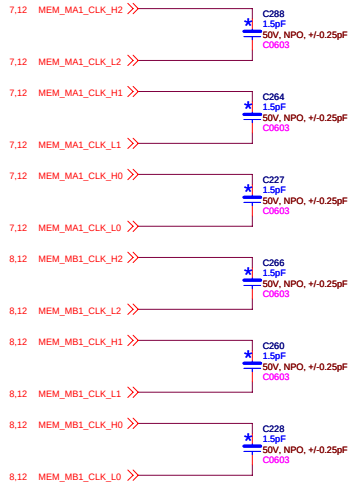
Title: DDR SDRAM DIMM 3 - 4

Size: C | Document Number: C51GM06 | Rev: A

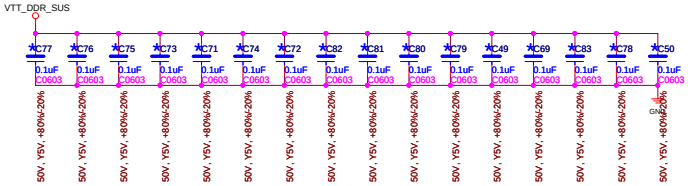
Date: Friday, April 14, 2006 | Sheet 12 of 38

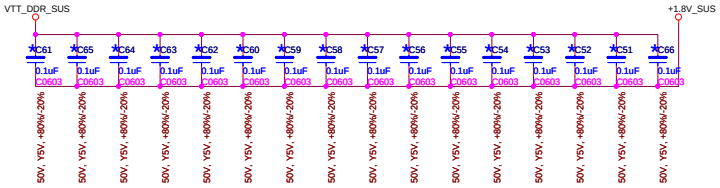
DDR2 Termination





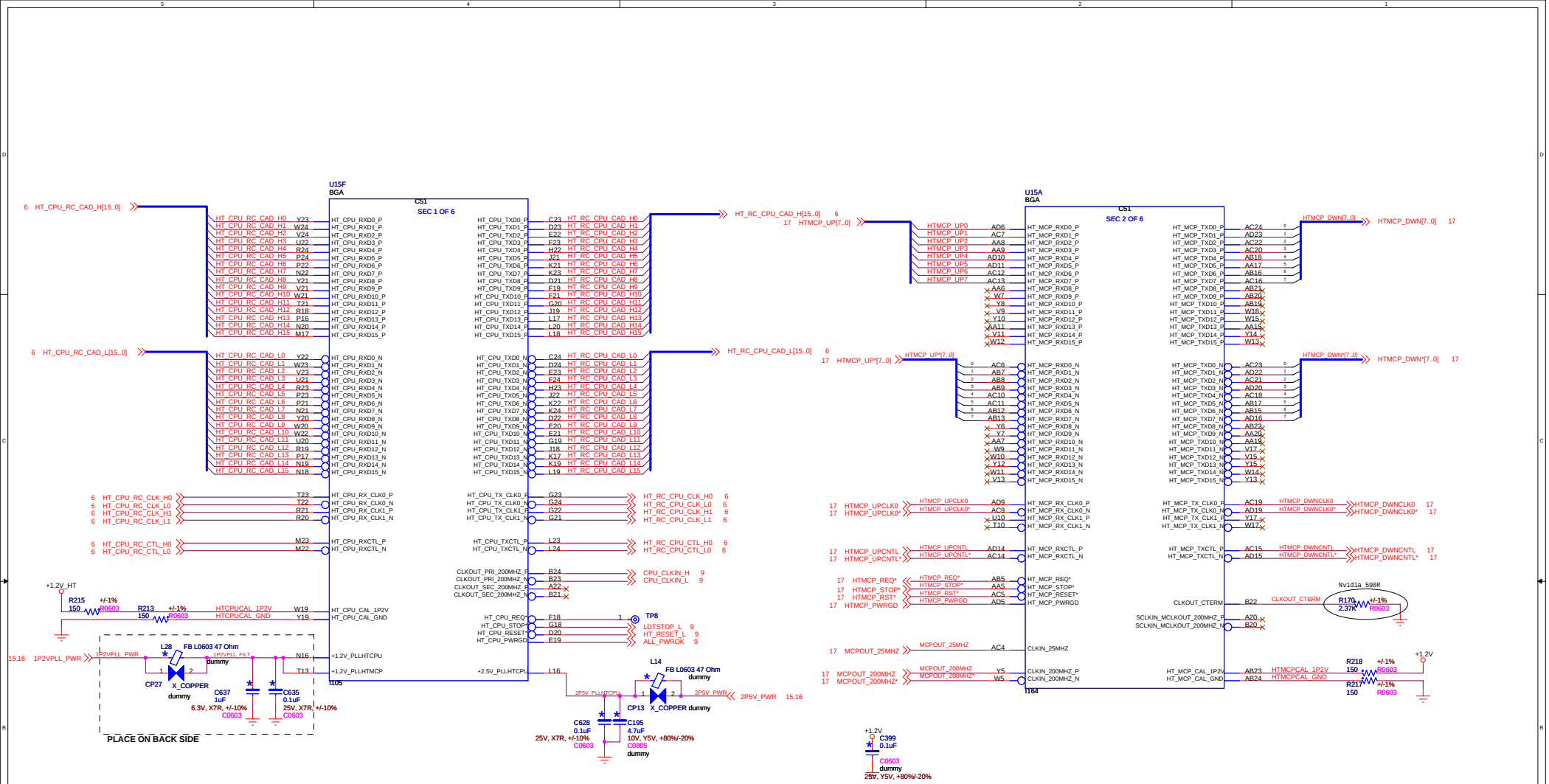
Layout: Spread out on VTT pour





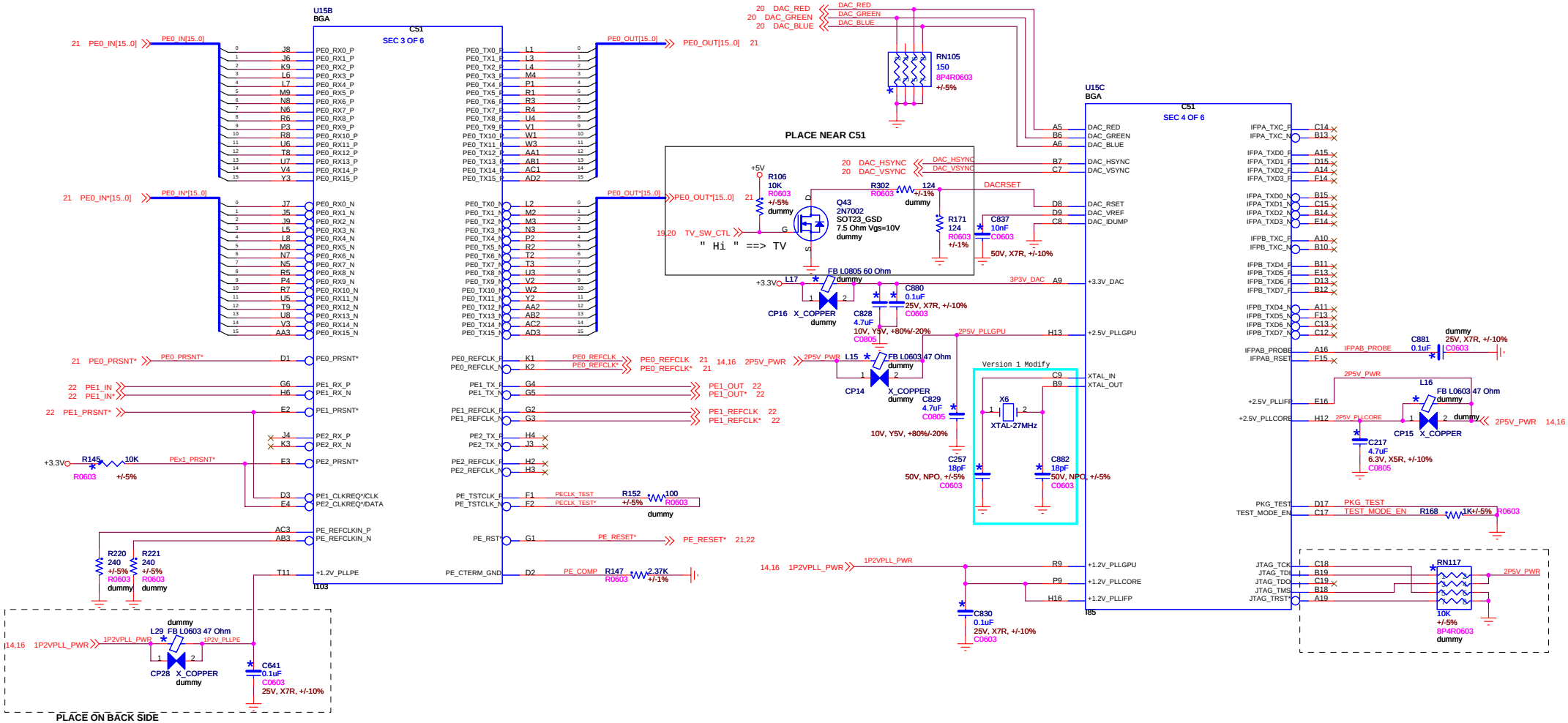
FOXCONN PCEG

Title	PCI Express Slot x16 & X1	
Size C	Document Number C51GM06	Rev A
Date: Monday, April 24, 2006	Sheet 13 of 38	



FOXCONN PCEG

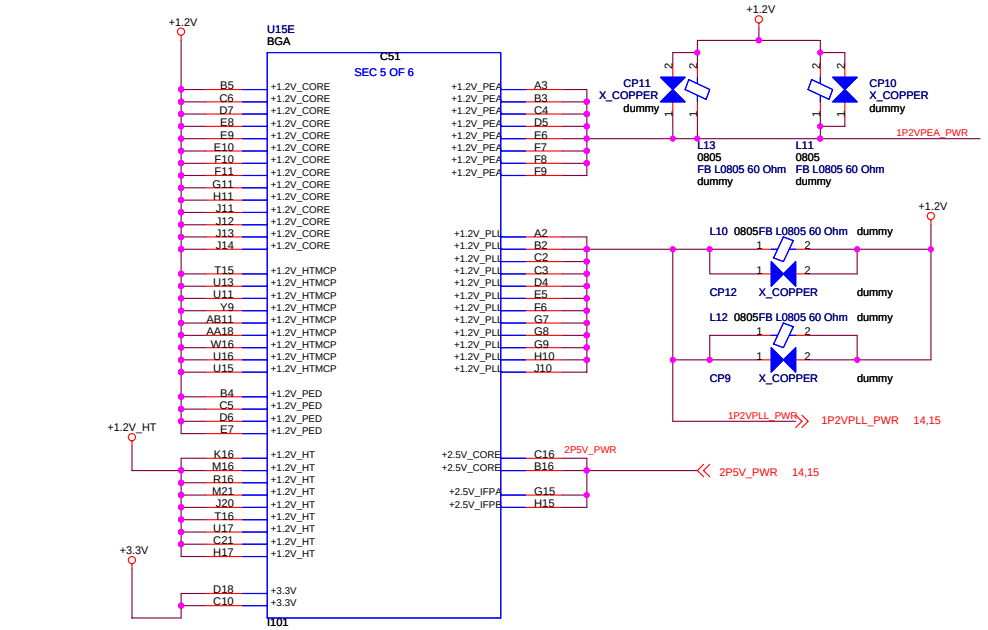
Title	C51G Part 1/6 , 2/6	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 14 of 38	

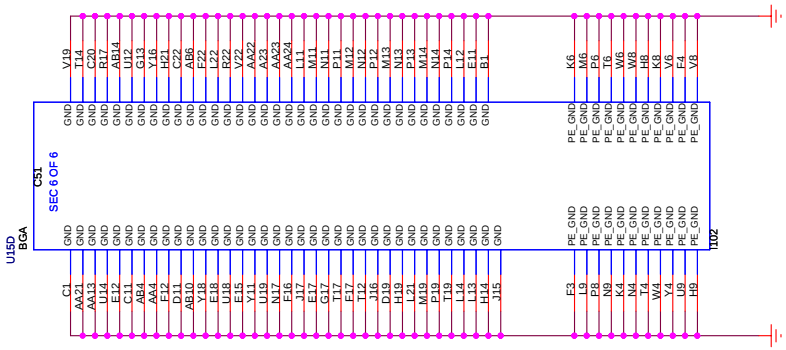


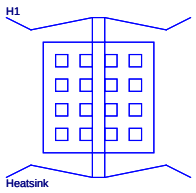
FOXCONN®

FOXCONN PCEG

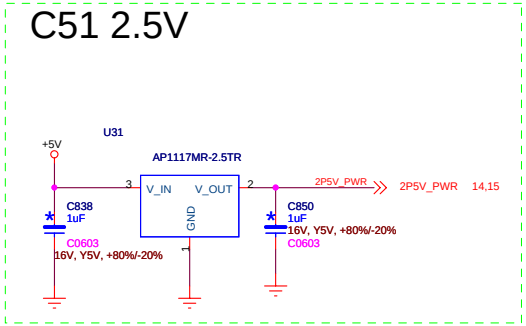
Title	C51G 3/6 , 4/6		
Size: Custom	Document Number: C51GM06		Rev: A
Date: Friday, April 14, 2006	Sheet 15 of 38		



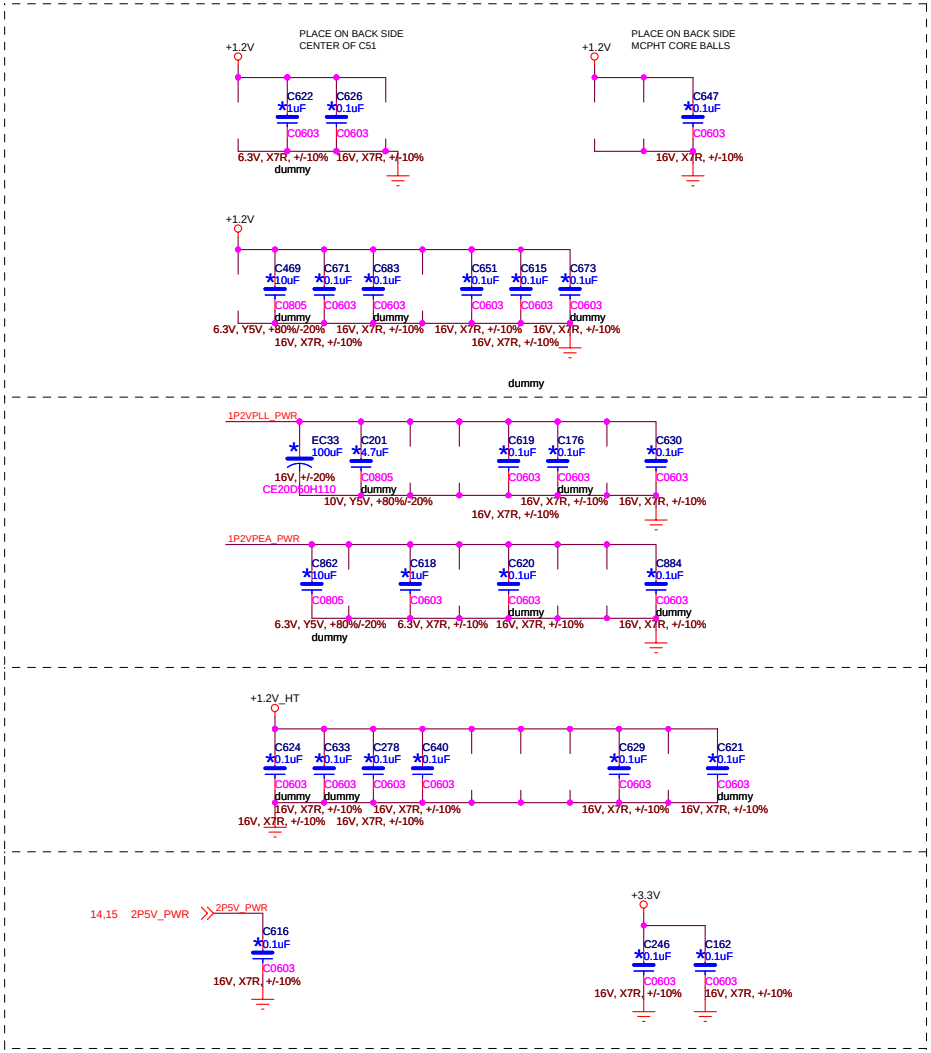




C51 2.5V



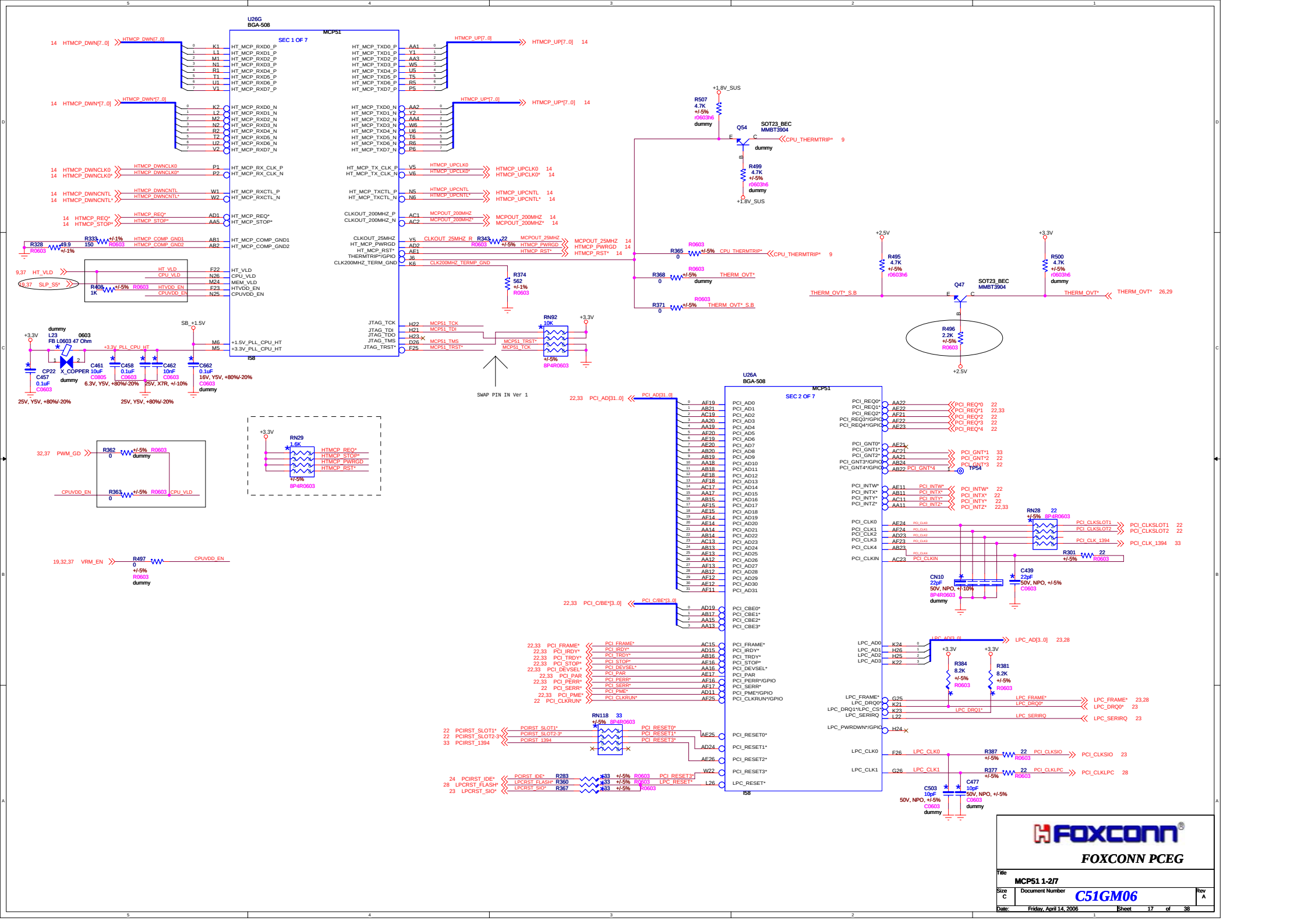
C51 DECOUPLING

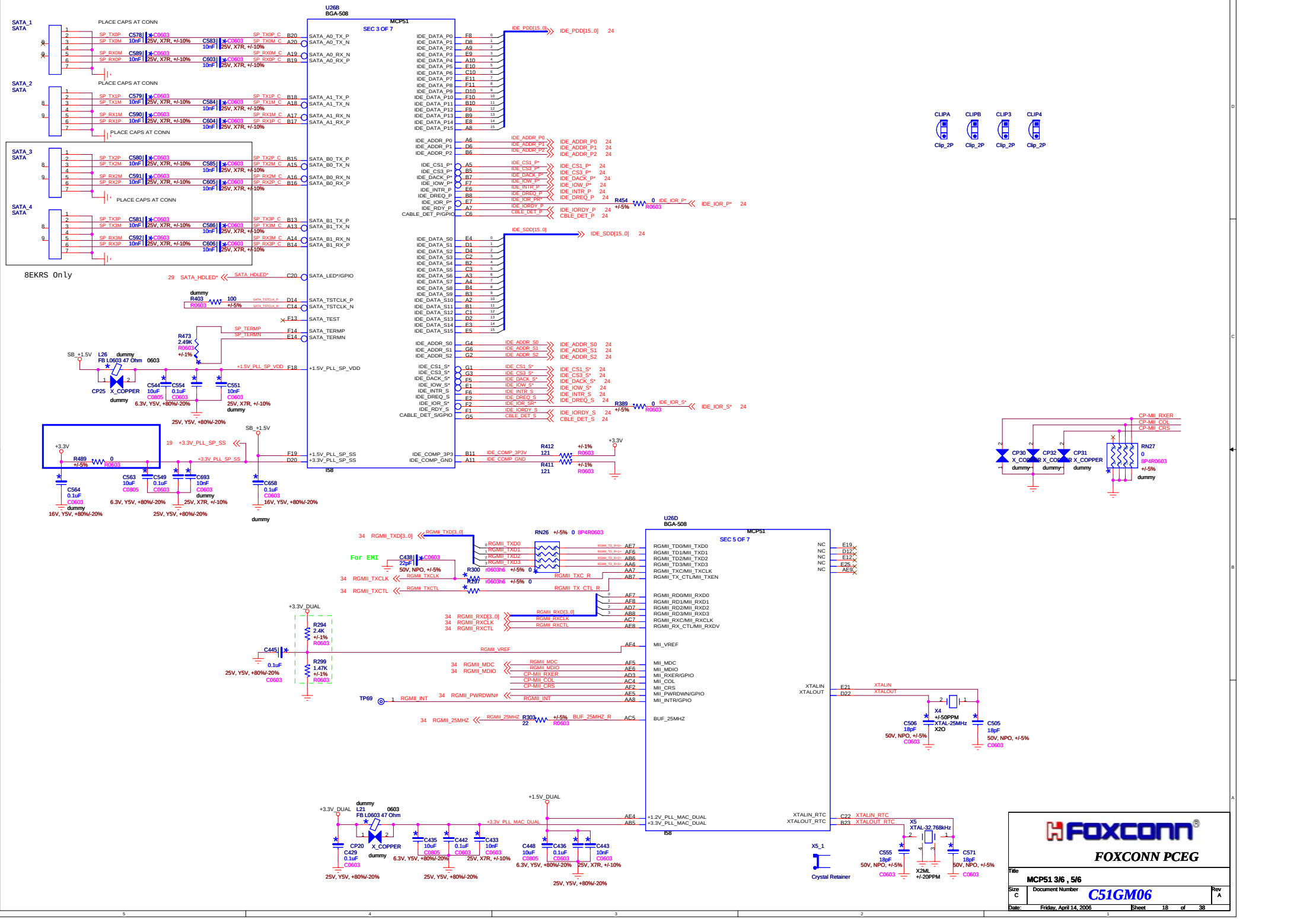


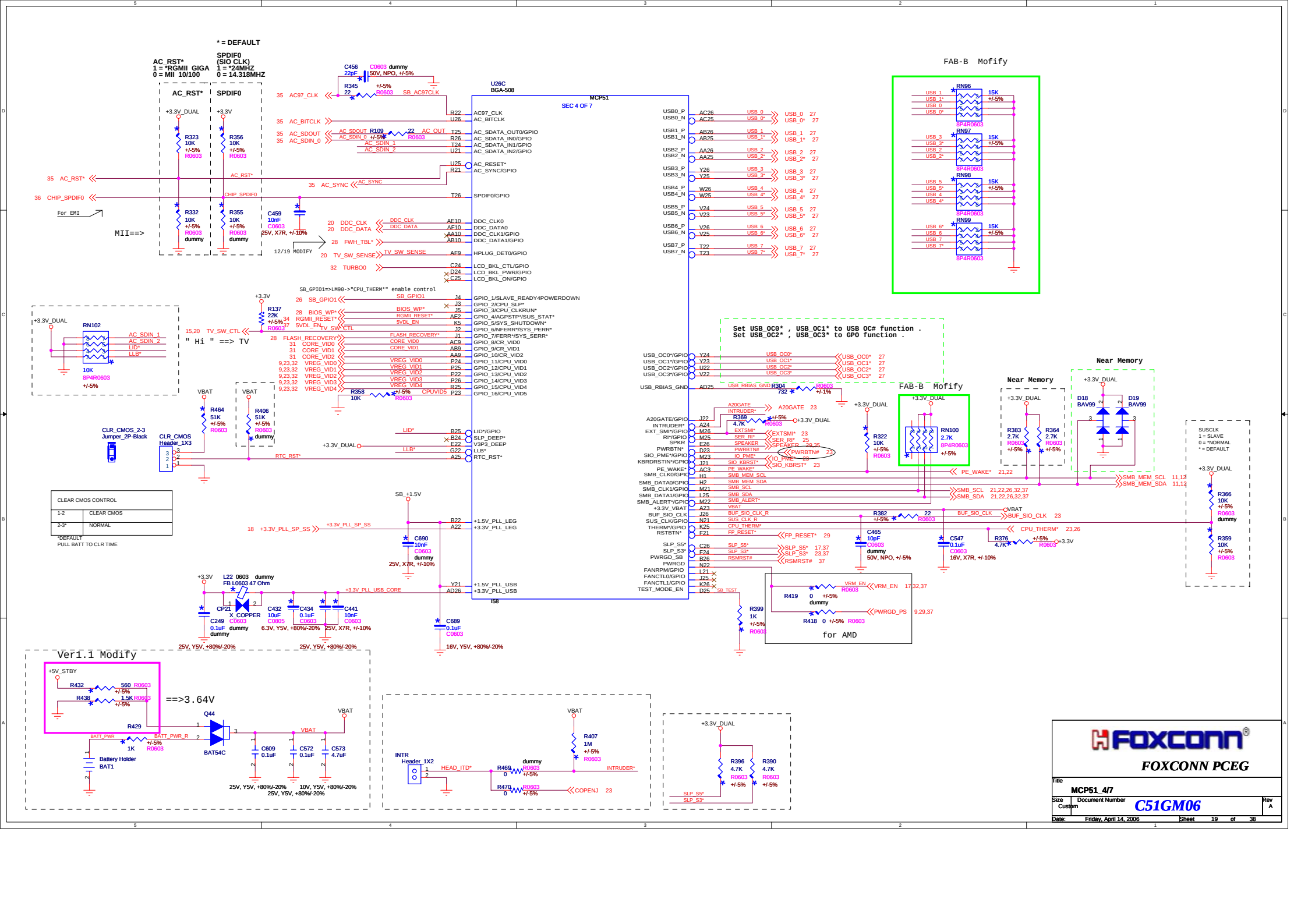
FOXCONN®

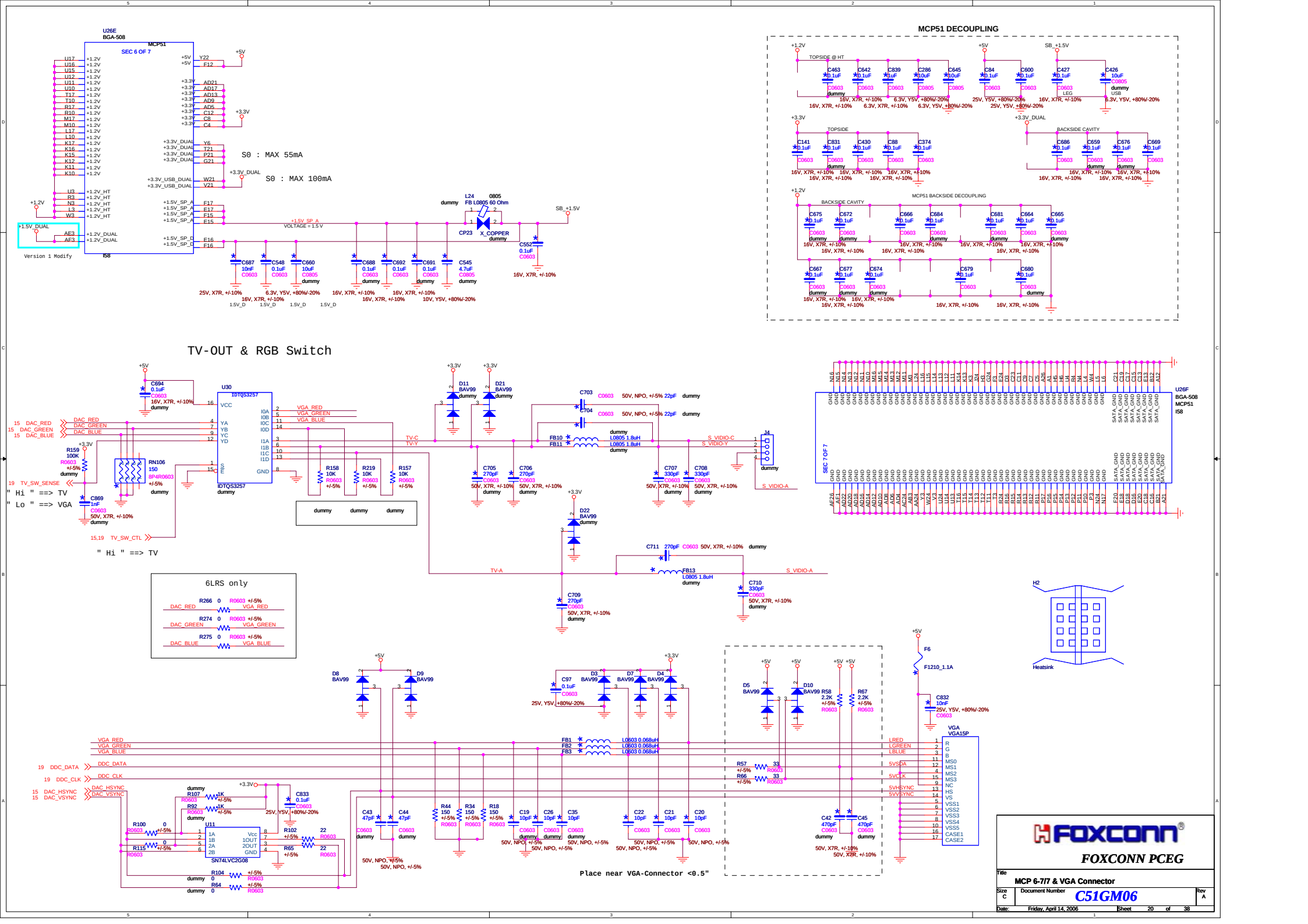
FOXCONN PCEG

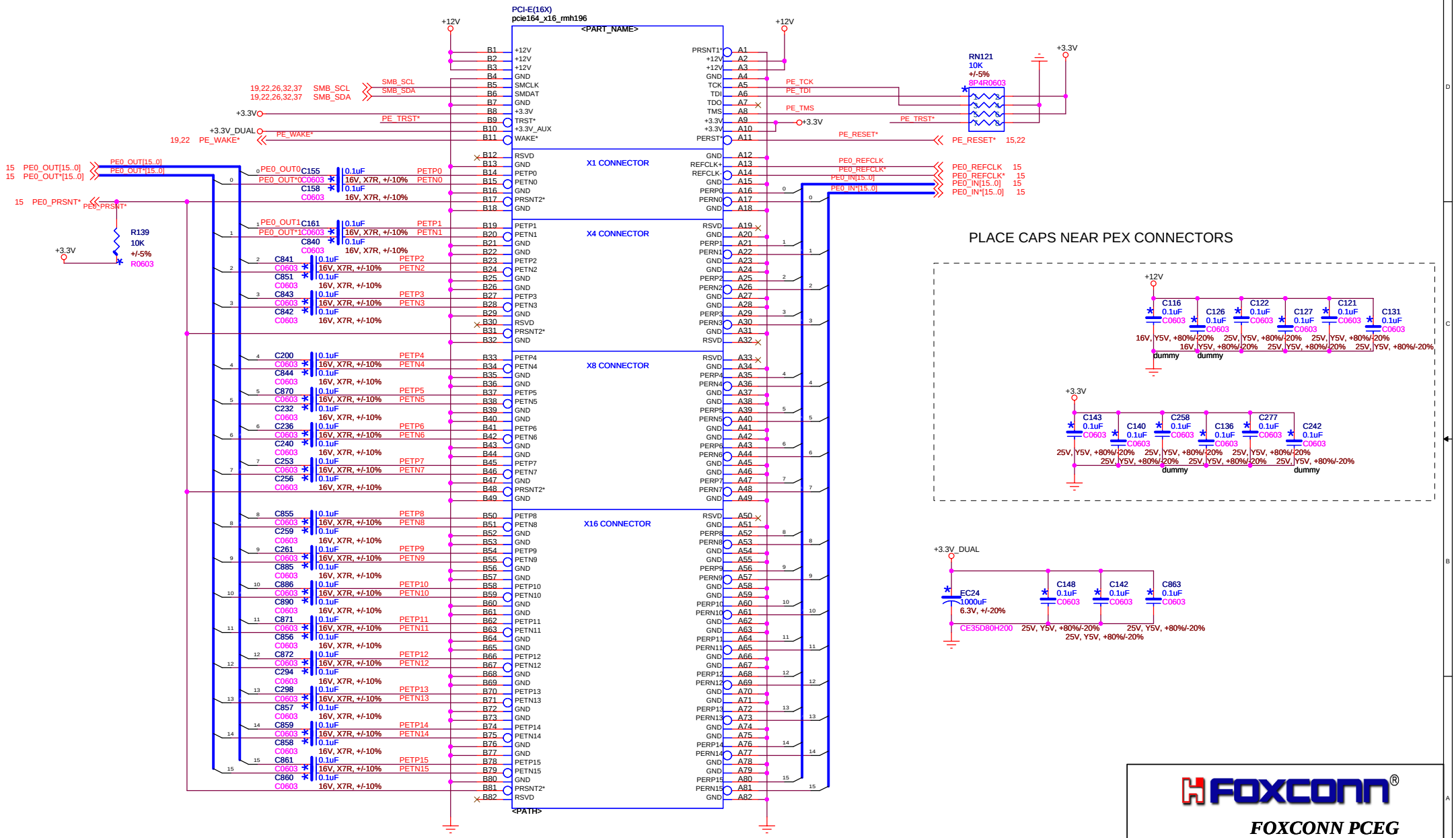
Title: C51G 5/6 , 6/6			
Size: Custom	Document Number: C51GM06		Rev: A
Date: Friday, April 14, 2006		Sheet 16 of 38	


U26G
BGA-508
MCP51
SEC 1 OF 7
HTMCP_DWN[7..0]
HTMCP_DWN*[7..0]
HTMCP_UP[7..0]
HTMCP_UP*[7..0]
HTMCP_DWNCLK0
HTMCP_DWNCNTL
HTMCP_REQ*
HTMCP_STOP*
HTMCP_COMP_GND1
HTMCP_COMP_GND2
HTMCP_UPCLK0
HTMCP_UPCNTL
MCPOUT_200MHZ
MCPOUT_25MHZ
HTMCP_PWRGD
HTMCP_RST*
HT_VLD
SLP_S5*
PWM_GD
VRM_EN
CPUVDD_EN
CPU_VLD
HTVDD_EN
MEM_VLD
CPUVDD_EN
+1.5V_PLL_CPU_HT
+3.3V_PLL_CPU_HT
SB_+1.5V
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
MCP51_TCK
MCP51_TDI
MCP51_TMS
MCP51_TRST*
SWAP PIN IN Ver 1
+1.8V_SUS
CPU_THERMTRIP*
THERM_OVT*
THERM_OVT* S.B
+2.5V
+3.3V
U26A
BGA-508
SEC 2 OF 7
PCI_AD[31..0]
PCI_C/BE*[3..0]
PCI_FRAME*
PCI_IRDY*
PCI_TRDY*
PCI_STOP*
PCI_DEVSEL*
PCI_PAR
PCI_PERR*
PCI_SERR*
PCI_PME*
PCI_CLKRUN*
PCI_REQ*0
PCI_REQ*1
PCI_REQ*2
PCI_REQ*3
PCI_REQ*4
PCI_GNT*0
PCI_GNT*1
PCI_GNT*2
PCI_GNT*3
PCI_GNT*4
PCI_INTW*
PCI_INTX*
PCI_INTY*
PCI_INTZ*
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK3
PCI_CLK4
PCI_CLKIN
PCI_RESET*0
PCI_RESET*1
PCI_RESET*2
PCI_RESET*3
PCI_RESET*
LPC_AD[3..0]
LPC_FRAME*
LPC_DRQ0*
LPC_DRQ1*/LPC_CS*
LPC_SERIRQ
LPC_PWRDWN*/GPIO
LPC_CLK0
LPC_CLK1
PCIRST_SLOT1*
PCIRST_SLOT2-3*
PCIRST_1394
PCIRST_IDE*
LPCRST_FLASH*
LPCRST_SIO*
FOXCONN PCEG
Title
MCP51 1-2/7
Size C
Document Number
C51GM06
Rev A
Date: Friday, April 14, 2006
Sheet 17 of 38


U26B
BGA-508
MCP51
SEC 3 OF 7
SATA_1
SATA_2
SATA_3
SATA_4
PLACE CAPS AT CONN
8EKRS Only
SATA_HDLED*
SATA_TSTCLK_P
SATA_TSTCLK_N
SATA_TEST
SATA_TERMP
SATA_TERMN
+1.5V_PLL_SP_VDD
+1.5V_PLL_SP_SS
+3.3V_PLL_SP_SS
IDE_DATA_P0
IDE_DATA_P1
IDE_DATA_P2
IDE_DATA_P3
IDE_DATA_P4
IDE_DATA_P5
IDE_DATA_P6
IDE_DATA_P7
IDE_DATA_P8
IDE_DATA_P9
IDE_DATA_P10
IDE_DATA_P11
IDE_DATA_P12
IDE_DATA_P13
IDE_DATA_P14
IDE_DATA_P15
IDE_PDD[15..0]
IDE_ADDR_P0
IDE_ADDR_P1
IDE_ADDR_P2
IDE_CS1_P*
IDE_CS3_P*
IDE_DACK_P*
IDE_IOW_P*
IDE_INTR_P
IDE_DREQ_P
IDE_IOR_P*
IDE_RDY_P
CABLE_DET_P/GPIO
IDE_IORDY_P
CBLE_DET_P
IDE_SDD[15..0]
IDE_DATA_S0
IDE_DATA_S1
IDE_DATA_S2
IDE_DATA_S3
IDE_DATA_S4
IDE_DATA_S5
IDE_DATA_S6
IDE_DATA_S7
IDE_DATA_S8
IDE_DATA_S9
IDE_DATA_S10
IDE_DATA_S11
IDE_DATA_S12
IDE_DATA_S13
IDE_DATA_S14
IDE_DATA_S15
IDE_ADDR_S0
IDE_ADDR_S1
IDE_ADDR_S2
IDE_CS1_S*
IDE_CS3_S*
IDE_DACK_S*
IDE_IOW_S*
IDE_INTR_S
IDE_DREQ_S
IDE_IOR_S*
IDE_RDY_S
CABLE_DET_S/GPIO
IDE_IORDY_S
CBLE_DET_S
IDE_COMP_3P3V
IDE_COMP_GND
I58
CLIPA
CLIPB
CLIP3
CLIP4
Clip_2P
CP-MII_RXER
CP-MII_COL
CP-MII_CRS
U26D
BGA-508
MCP51
SEC 5 OF 7
RGMII_TXD[3..0]
RGMII_TXCLK
RGMII_TXCTL
RGMII_TXC_R
RGMII_TX_CTL_R
RGMII_RXD[3..0]
RGMII_RXCLK
RGMII_RXCTL
RGMII_VREF
RGMII_MDC
RGMII_MDIO
RGMII_PWRDWN#
RGMII_INT
RGMII_25MHZ
BUF_25MHZ_R
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
+1.2V_PLL_MAC_DUAL
+3.3V_PLL_MAC_DUAL
Crystal Retainer
FOXCONN PCEG
MCP51 3/6 , 5/6
C51GM06
Friday, April 14, 2006
Sheet 18 of 38


* = DEFAULT
AC_RST*
1 = *RGMII GIGA
0 = MII 10/100
SPDIF0
(SIO CLK)
1 = *24MHZ
0 = 14.318MHZ
U26C
BGA-508
MCP51
SEC 4 OF 7
MII==>
" Hi " ==> TV
Set USB_OC0* , USB_OC1* to USB OC# function .
Set USB_OC2* , USB_OC3* to GPO function .
FAB-B Mofify
Near Memory
for AMD
Ver1.1 Modify
==>3.64V
CLEAR CMOS CONTROL
1-2 CLEAR CMOS
2-3* NORMAL
*DEFAULT
PULL BATT TO CLR TIME
SUSCLK
1 = SLAVE
0 = *NORMAL
* = DEFAULT
FOXCONN PCEG
Title
MCP51_4/7
Size Custom
Document Number C51GM06
Rev A
Date: Friday, April 14, 2006
Sheet 19 of 38


MCP51 DECOUPLING
TV-OUT & RGB Switch
6LRS only
" Hi " ==> TV
" Lo " ==> VGA
Place near VGA-Connector <0.5"
FOXCONN PCEG
MCP 6-7/7 & VGA Connector
C51GM06
Friday, April 14, 2006
Sheet 20 of 38


PCI-E(16X)
pcie164_x16_rmh196
<PART_NAME>
X1 CONNECTOR
X4 CONNECTOR
X8 CONNECTOR
X16 CONNECTOR
<PATH>
+12V
+3.3V
+3.3V_DUAL
SMB_SCL
SMB_SDA
PE_TRST*
PE_WAKE*
PE_TCK
PE_TDI
PE_TMS
PE_RESET*
PE0_REFCLK
PE0_REFCLK*
PE0_IN[15..0]
PE0_IN*[15..0]
PE0_OUT[15..0]
PE0_OUT*[15..0]
PE0_PRSNT*
RN121
10K
+/-5%
8P4R0603
R139
10K
+/-5%
R0603
PLACE CAPS NEAR PEX CONNECTORS
dummy
FOXCONN PCEG
Title
PCI Express Slot x16 & X1
Size
Custom
Document Number
C51GM06
Rev
A
Date:
Friday, April 14, 2006
Sheet
21
of
38

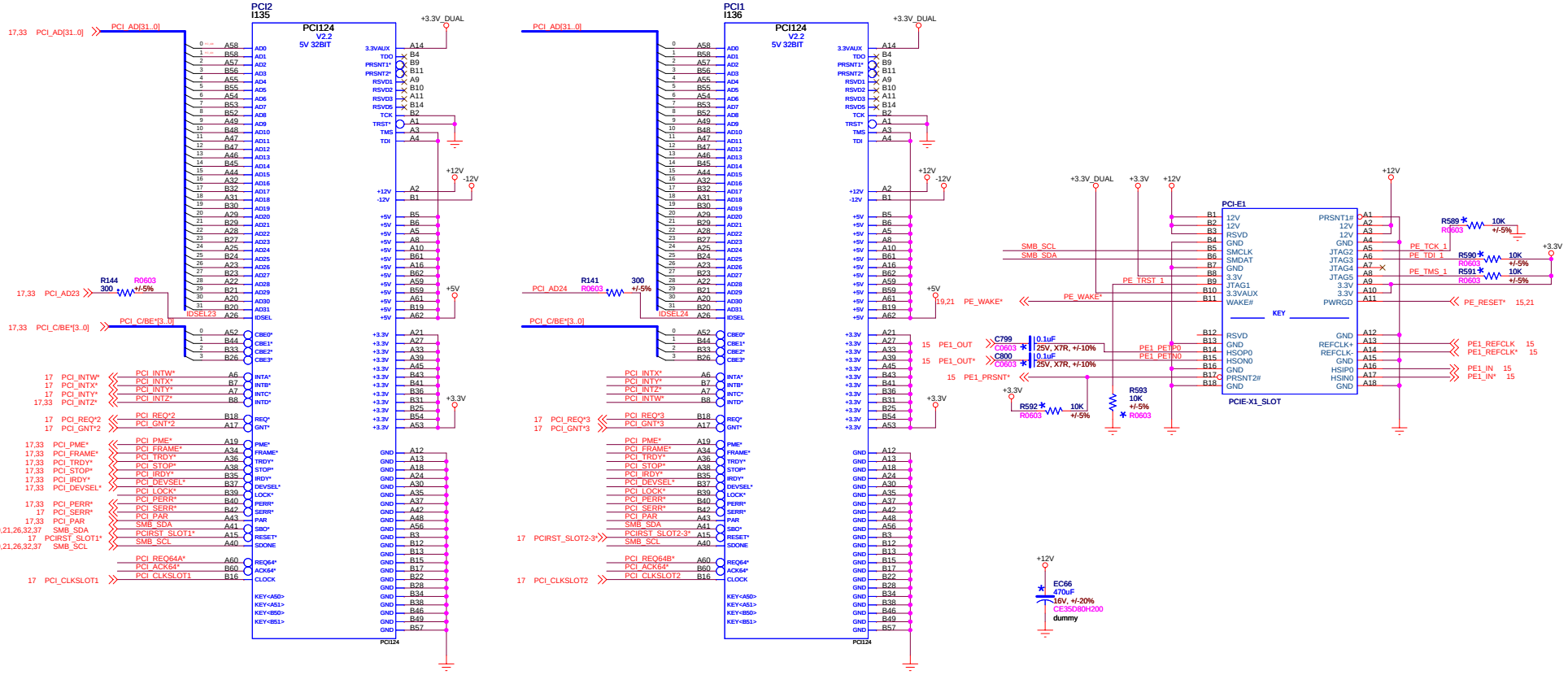
SLOT 2

IDSEL23

SLOT 1

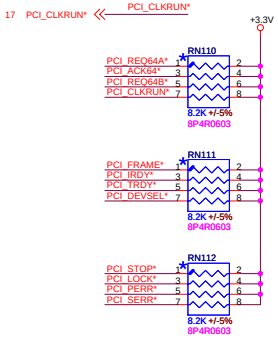
IDSEL24

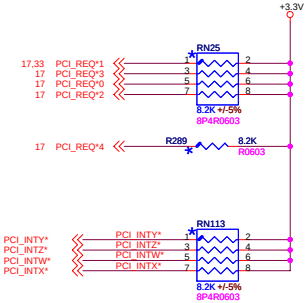
SLOT 1

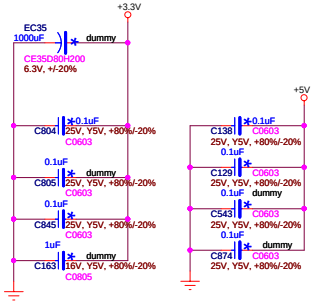


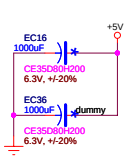
PCI1 IDSEL= A23 , PCI_REQ#=2 , Routin=W/X/Y/Z

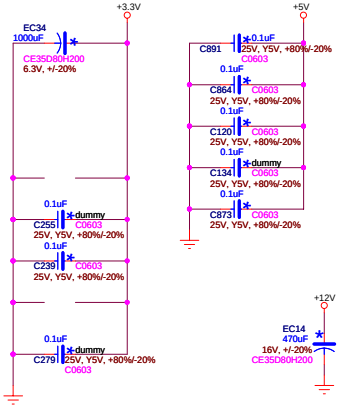
PCI2 IDSEL= A24 , PCI_REQ#=3 , Routin=X/Y/Z/W











FOXCONN PCEG

Title: PCI Slot 1 & 2		
Size: C	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 22 of 38	

Power On Strapping Options

	Symbol	value	Description
JP1	KBCEN	1	KBC is enabled.
		0	KBC is disabled.
JP2	KBC_IROM	1	KBC's ROM is built in.
		0	KBC's ROM is external.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, and PCIRST4# are enhanced open-drain. It will drive high about 10~20ns when the signal transit from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	RTS2#	1	Fan_Ctrl output default duty 100%
		0	Fan_Ctrl output default duty 50 %
JP6	SOUT2	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
		0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

The different function pins between IT8712F/I and IT8712F/H

Pin	IT8712F/IX	Pin	IT8712F/HX
5	SOUT2/JP6	5	SOUT2
20	JSBB2/GP27/FAN_CTL4	20	JSBB2/GP27
21	JSBB1/GP26/FAN_CTL5	21	JSBB1/GP26
22	JSBCY/GP25/FAN_TAC4	22	JSBCY/GP25
23	JSBCX/GP24/FAN_TAC5	23	JSBCX/GP24
36	VIDVCC	36	LPCPD#
48	GP50/CLKRUN#/PCIRST5#	48	CLKRUN#/GP50
91	VIN7/PCIRSTIN#	91	VIN7
95	VIN3/ATXPG	95	VIN3

Note:

If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Reserved for SIO Thermal SMI alert .

24MHz

Ver1.1 Modify

output to SB

Place C749 close to IT8712, and Do Not remove this 1uF Cap. of VREF.

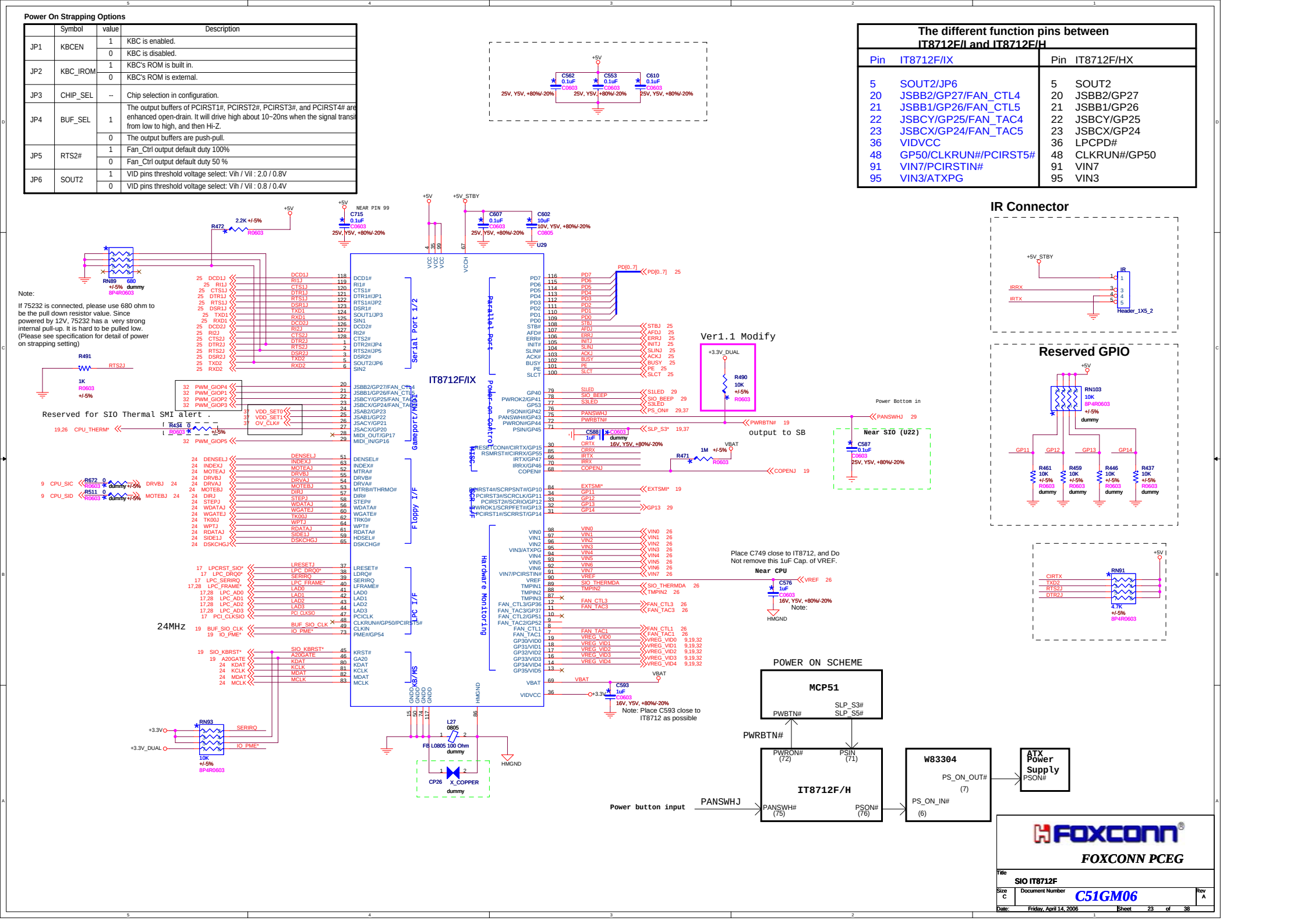
Note: Place C593 close to IT8712 as possible

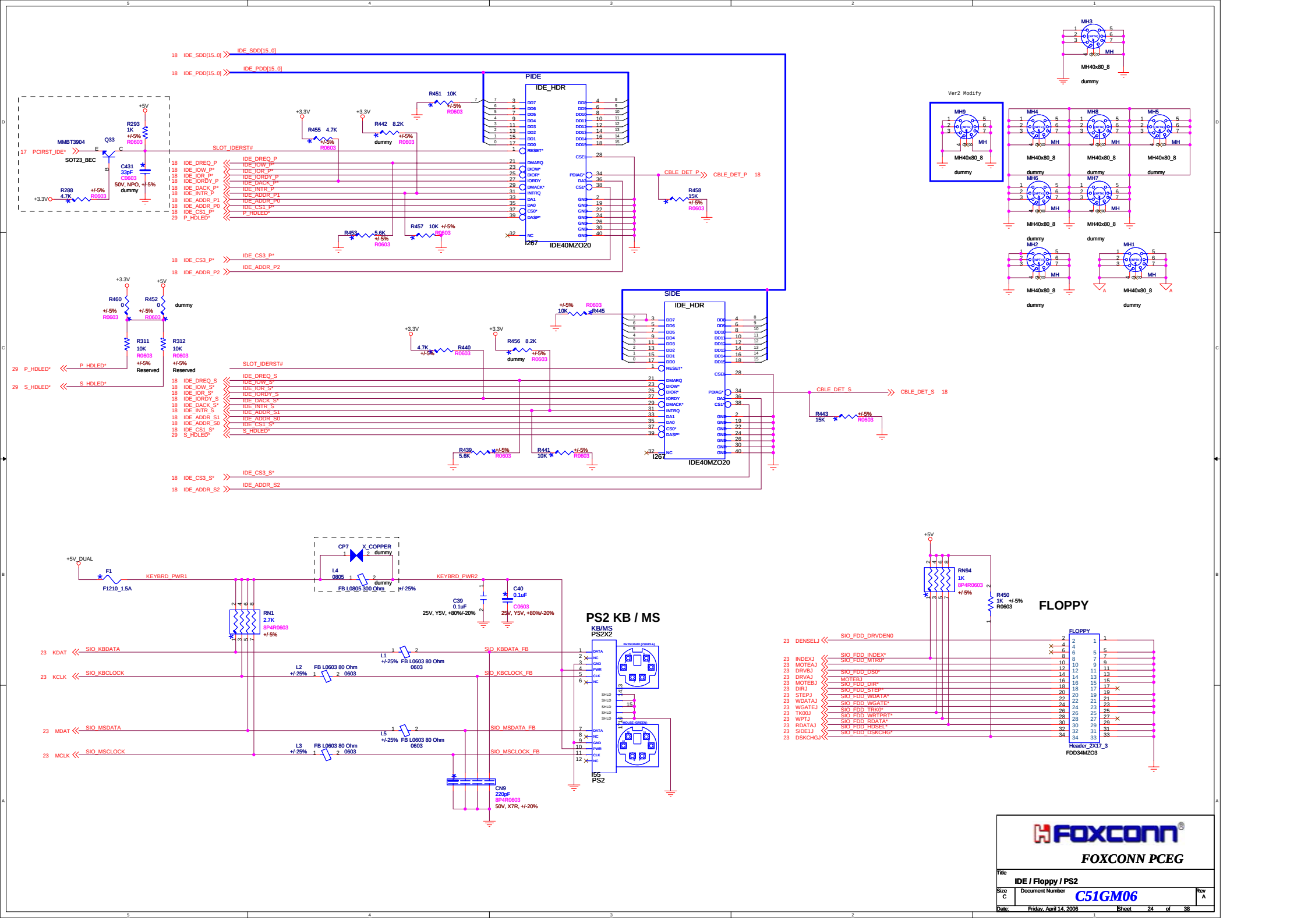
IR Connector

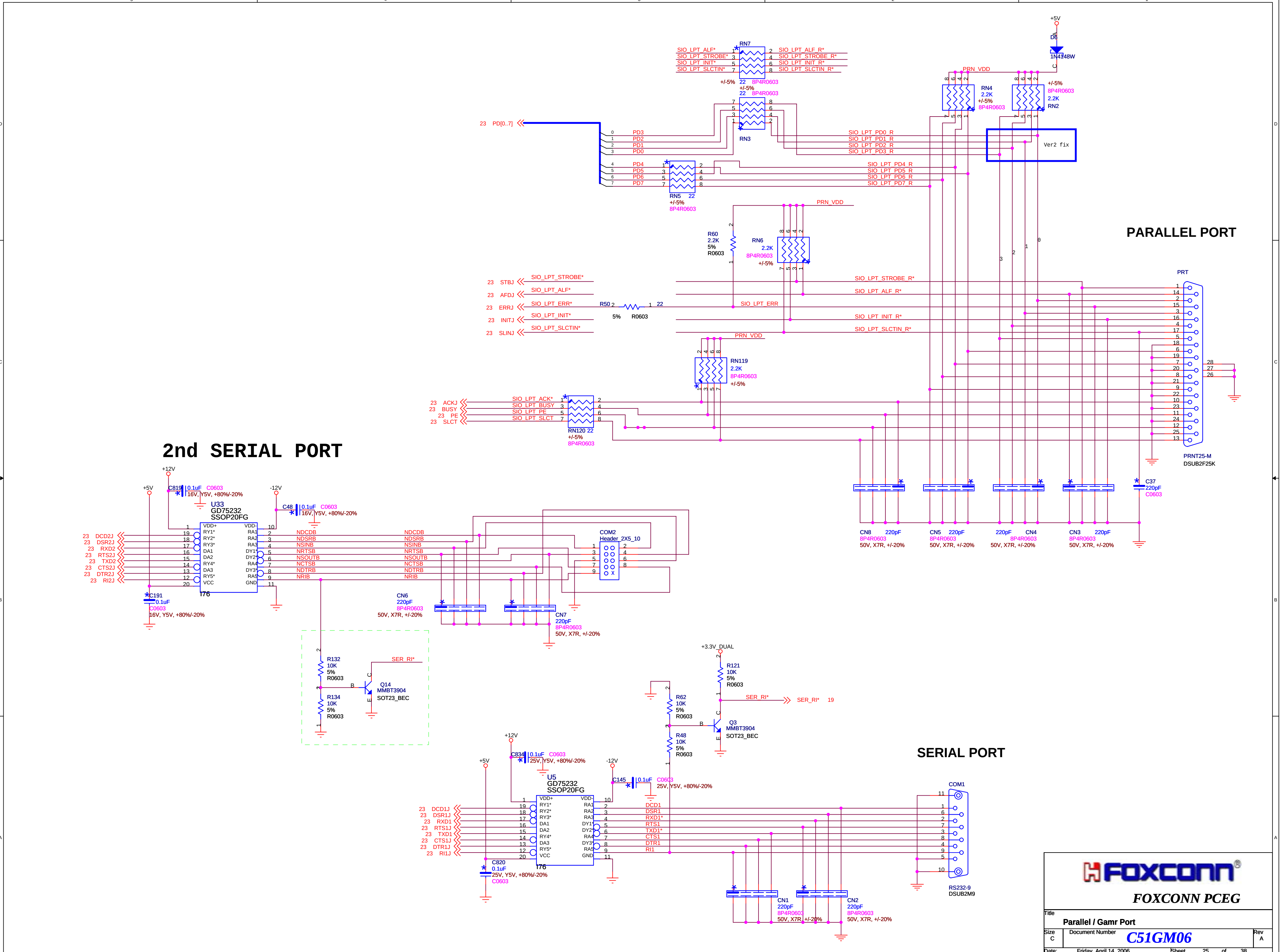
Reserved GPIO

POWER ON SCHEME

Power button input




PIDE
IDE_HDR
IDE40MZO20
SIDE
IDE_HDR
IDE40MZO20
PS2 KB / MS
KB/MS
PS2X2
FLOPPY
FLOPPY
FDD34MZO3
Ver2 Modify
MH3
MH9
MH4
MH8
MH5
MH6
MH7
MH2
MH1
MH40x80_8
dummy
FOXCONN PCEG
Title
IDE / Floppy / PS2
Size C
Document Number
C51GM06
Rev A
Date: Friday, April 14, 2006
Sheet 24 of 38

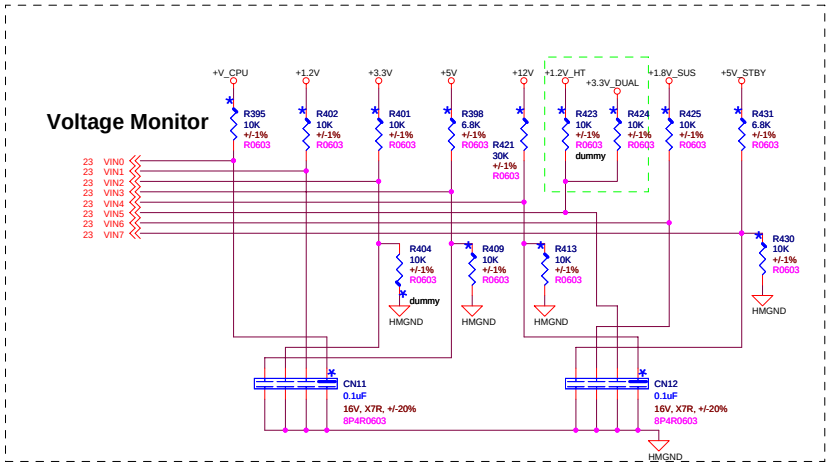


FOXCONN PCEG

Title: Parallel / Gamr Port

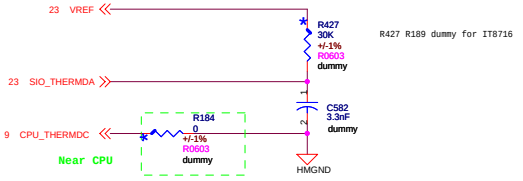
Size: C | Document Number: C51GM06 | Rev: A

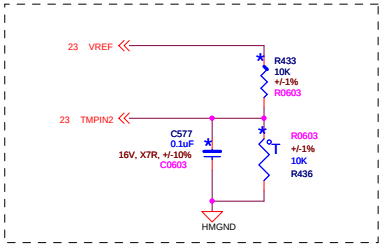
Date: Friday, April 14, 2006 | Sheet 25 of 38



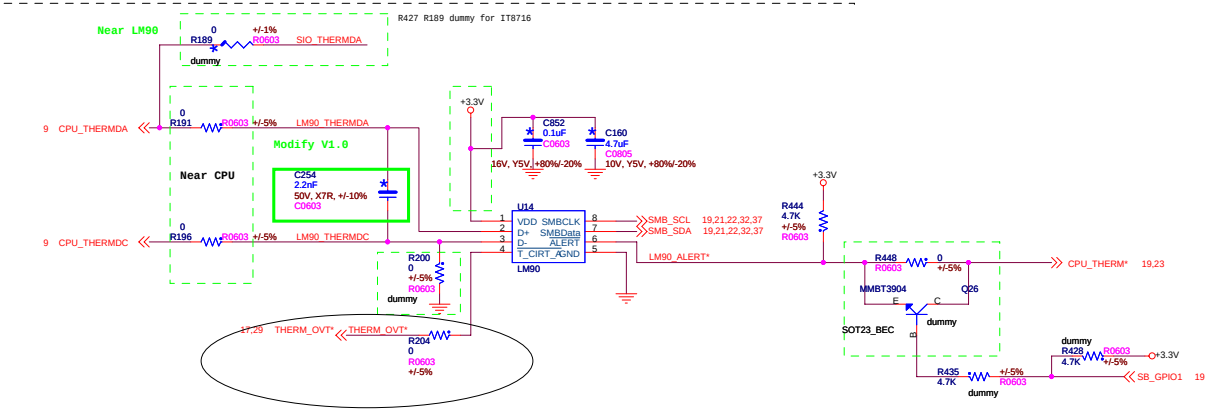
Thermal Controller

Thermal Diode layout notice:
a. Place T.D. close to IT8712F/H.
c. Recommanded trace widths & spacings is 10 miles.
b. Keep the trace away from; +12V, Fast data bus, CRTs.
d. Isolate GNDA, GND.





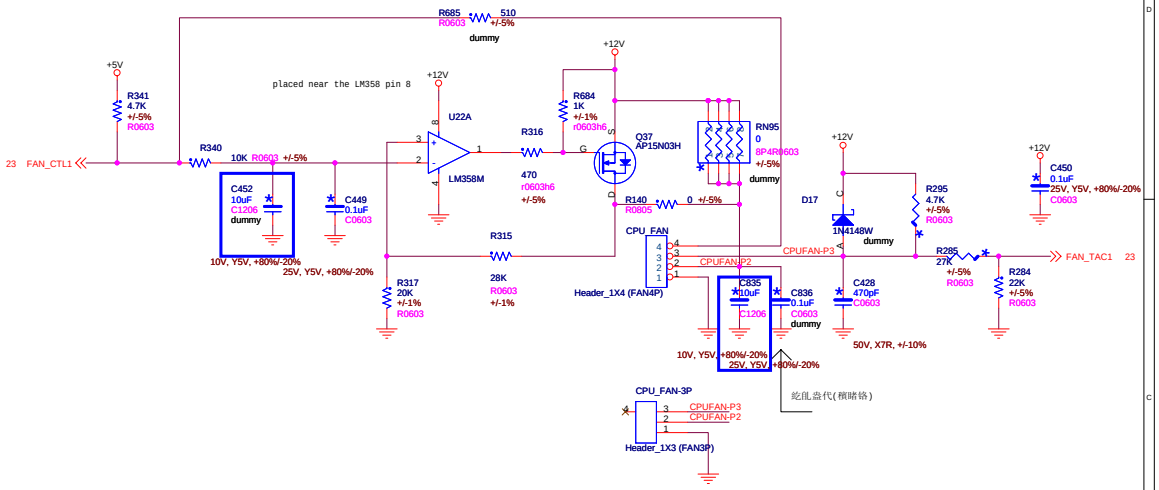
Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

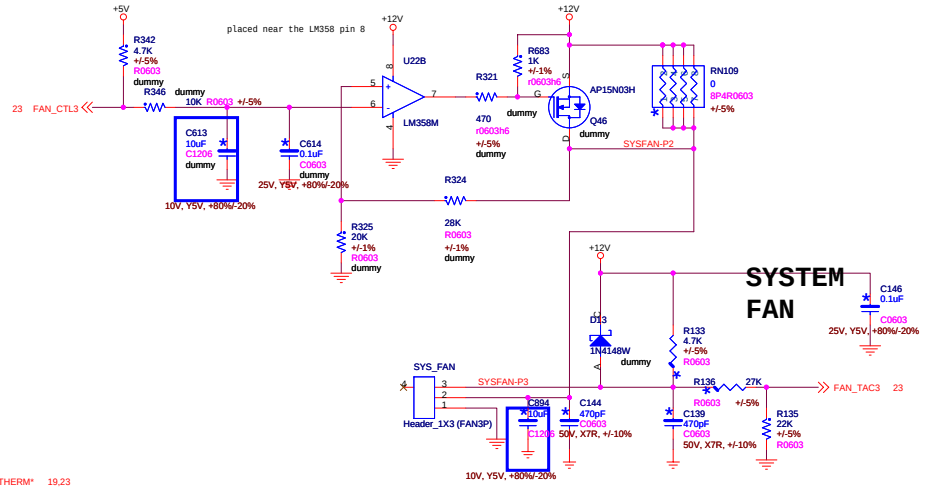


Need to check GPIO default value at power-on .

CPU FAN

New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense

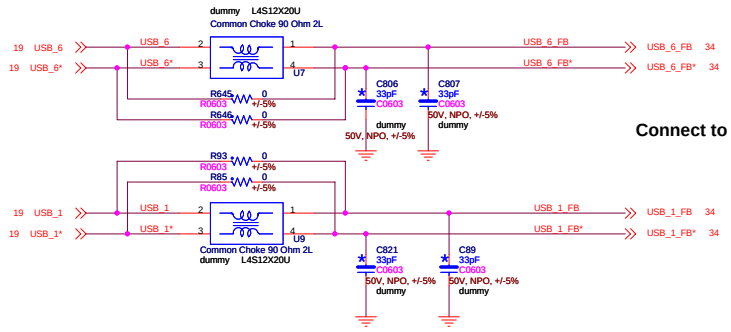




FOXCONN PCEG

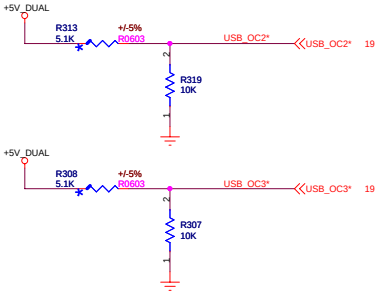
Title	Hardware Monitor / Over Volt. CKT	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 26 of 38	

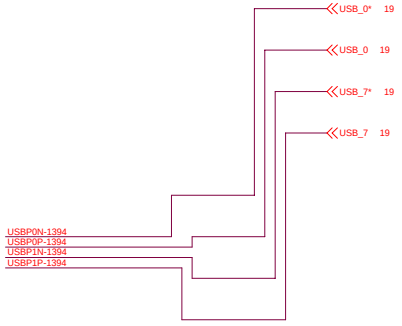
BACK PANEL LAN/USB -> Near Connector



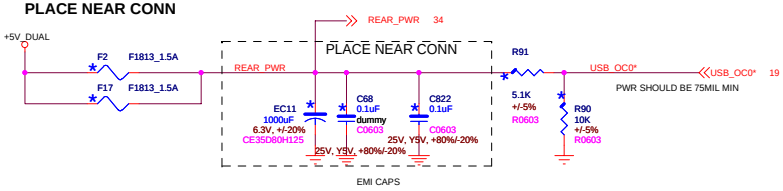
Connect to rear LAN/USB port

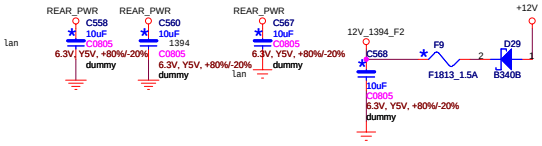
Set USB_OC2* , USB_OC3* to GPO function .

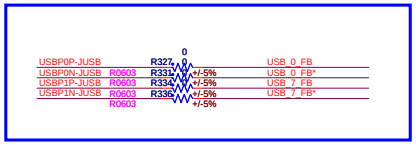




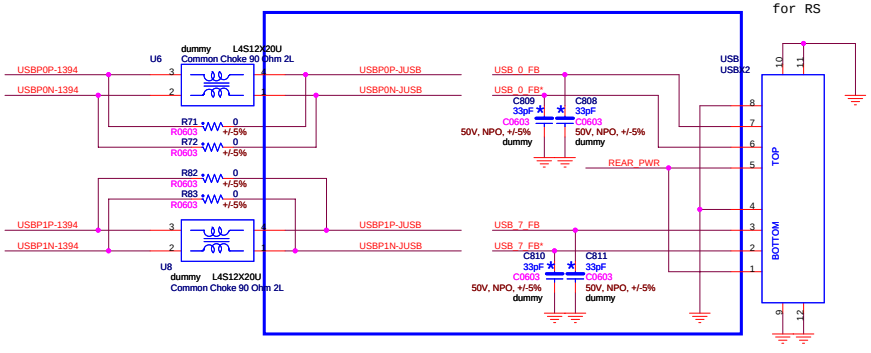
PLACE NEAR CONN



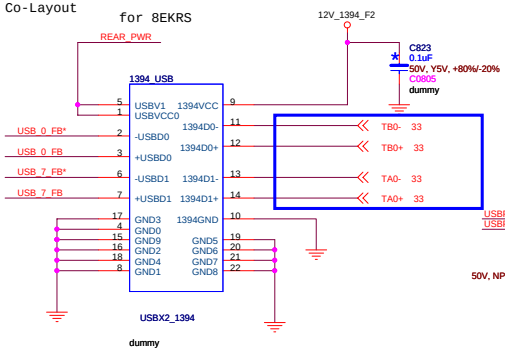




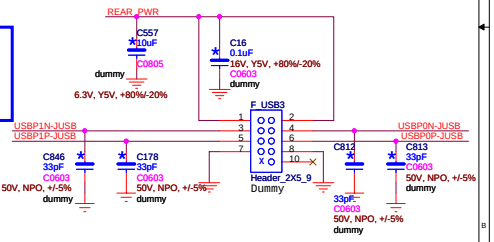
for RS Co-Layout



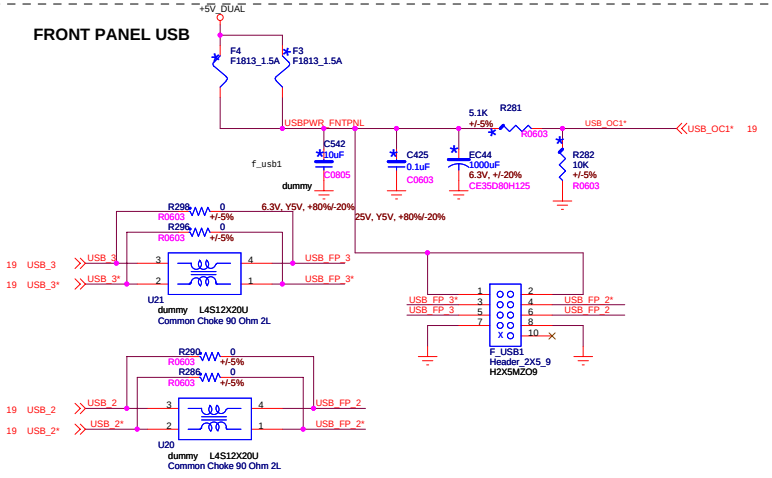
for 8EKRS

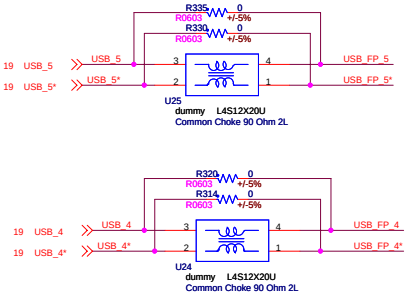


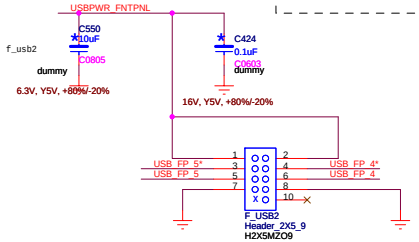
Acer F_USB3

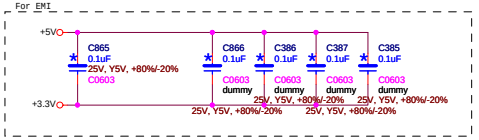


FRONT PANEL USB









FOXCONN PCEG

Title: USB Connector

Size: C | Document Number: C51GM06 | Rev: A

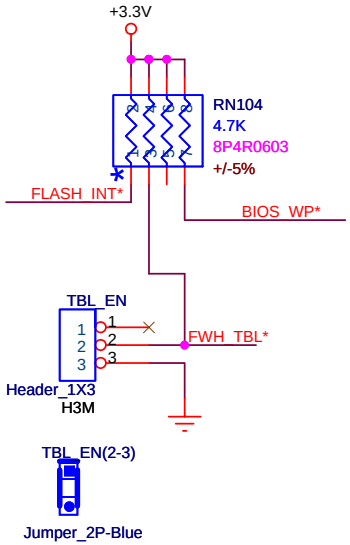
Date: Friday, April 14, 2006 | Sheet 27 of 38

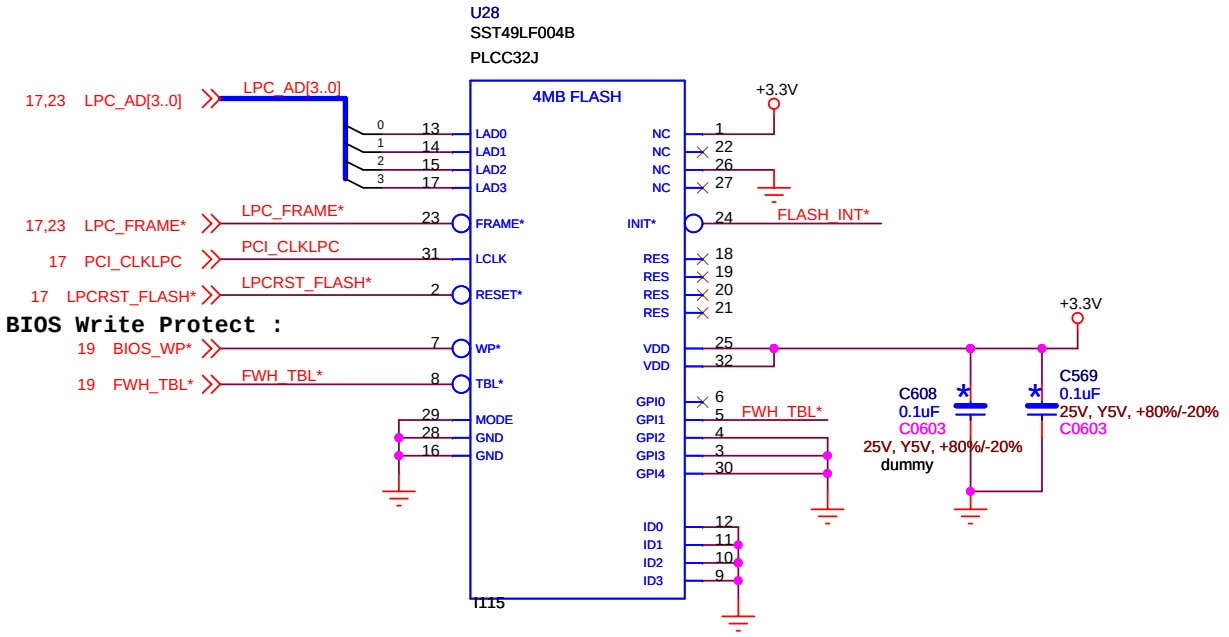
This is for BIOS socket BOM purpose

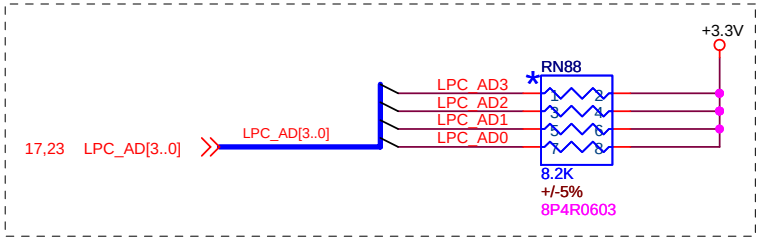
When low, prevents programming to the boot block sectors at the top of the device memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected.

BIOS TBL ENABLE
H DISABLE
L ENABLE DEFAULT

BIOS TBL ENABLE
1-2 DISABLE
2-3 ENABLE
DEFAULT

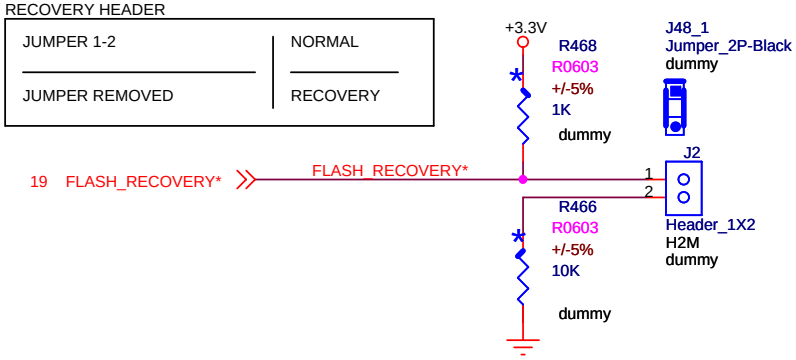




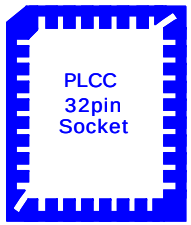


RECOVERY HEADER

JUMPER 1-2	NORMAL
JUMPER REMOVED	RECOVERY

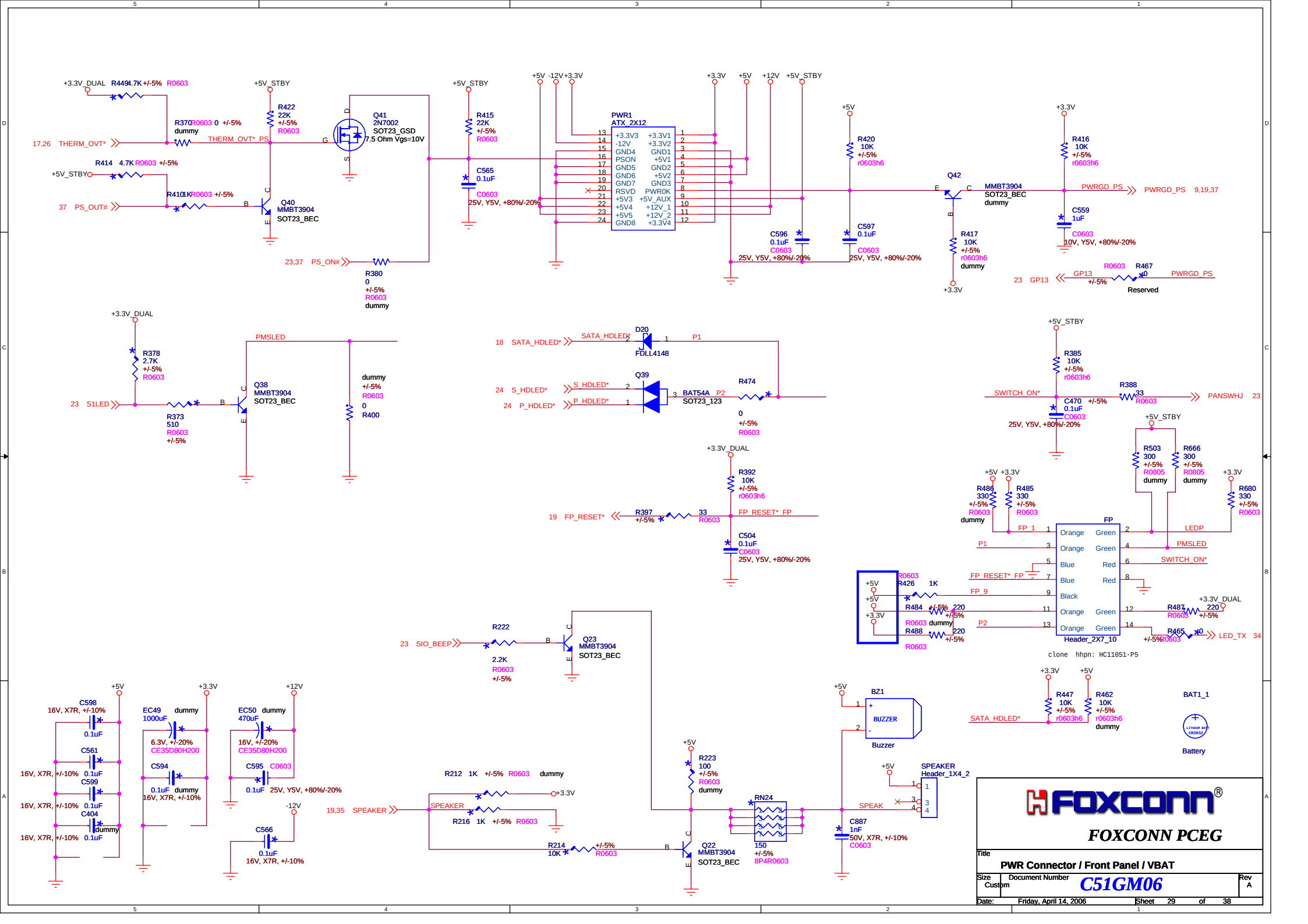


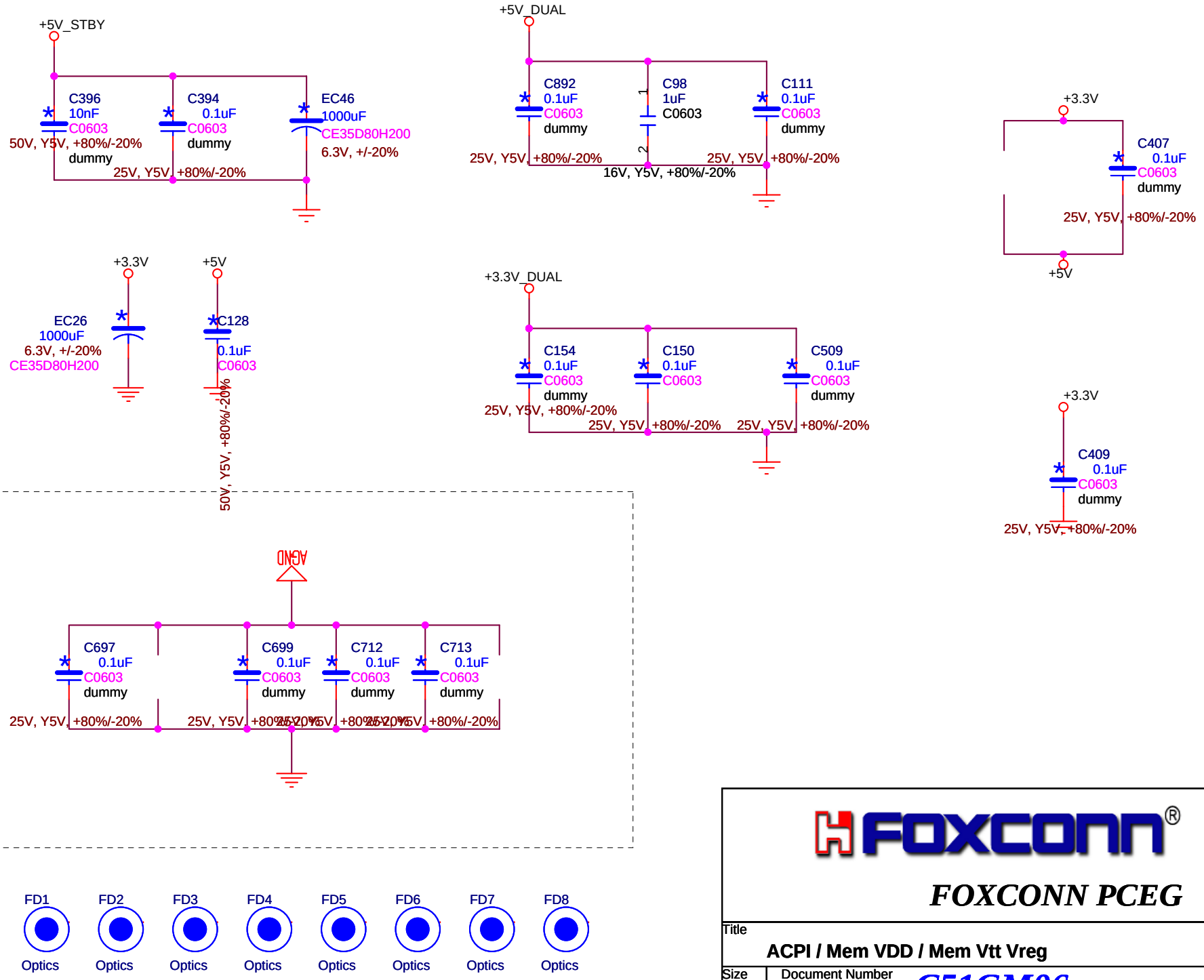
U28_1



FOXCONN PCEG

Title			
Flash ROM			
Size: Custom	Document Number: C51GM06		Rev: A
Date: Friday, April 14, 2006		Sheet 28 of 38	


+3.3V_DUAL R449 4.7K +/-5% R0603
+5V_STBY
R422 22K +/-5% R0603
R370 R0603 0 +/-5% dummy
17,26 THERM_OVT*
THERM_OVT* PS
Q41 2N7002 SOT23_GSD 7.5 Ohm Vgs=10V
R414 4.7K R0603 +/-5%
R410 1K R0603 +/-5%
37 PS_OUT#
Q40 MMBT3904 SOT23_BEC
23,37 PS_ON#
R380 0 +/-5% R0603 dummy
R415 22K +/-5% R0603
C565 0.1uF C0603 25V, Y5V, +80%/-20%
+5V -12V +3.3V
PWR1 ATX_2X12
+3.3V3 +3.3V1
-12V +3.3V2
GND4 GND1
PSON +5V1
GND5 GND2
GND6 +5V2
GND7 GND3
RSVD PWR0K
+5V3 +5V_AUX
+5V4 +12V_1
+5V5 +12V_2
GND8 +3.3V4
+3.3V +5V +12V +5V_STBY
R420 10K +/-5% r0603h6
C596 0.1uF C0603 25V, Y5V, +80%/-20%
C597 0.1uF C0603 25V, Y5V, +80%/-20%
Q42 MMBT3904 SOT23_BEC dummy
R417 10K +/-5% r0603h6 dummy
R416 10K +/-5% r0603h6
PWRGD_PS PWRGD_PS 9,19,37
C559 1uF C0603 10V, Y5V, +80%/-20%
23 GP13
R0603 R467 0 +/-5%
PWRGD_PS
Reserved
+3.3V_DUAL
R378 2.7K +/-5% R0603
23 S1LED
R373 510 R0603 +/-5%
Q38 MMBT3904 SOT23_BEC
PMSLED
dummy +/-5% R0603 0 R400
18 SATA_HDLED*
D20 FDLL4148
24 S_HDLED*
24 P_HDLED*
Q39 BAT54A SOT23_123
R474 0 +/-5% R0603
+3.3V_DUAL
R392 10K +/-5% r0603h6
19 FP_RESET*
R397 33 +/-5% R0603
C504 0.1uF C0603 25V, Y5V, +80%/-20%
+5V_STBY
R385 10K +/-5% r0603h6
SWITCH_ON*
R388 33 R0603
PANSWHJ 23
C470 0.1uF C0603 25V, Y5V, +80%/-20%
R503 300 +/-5% R0805 dummy
R666 300 +/-5% R0805 dummy
R486 330 +/-5% R0603 dummy
R485 330 +/-5% R0603
R680 330 +/-5% R0603
FP
FP_1 Orange Green LEDP
P1 Orange Green PMSLED
Blue Red SWITCH_ON*
FP_RESET* FP Blue Red
FP_9 Black
P2 Orange Green
Orange Green
Header_2X7_10
R426 1K R0603
R484 220 +/-5% R0603 dummy
R488 220 +/-5% R0603
R487 220 +/-5% R0603
R465 0 +/-5% R0603
LED_TX 34
clone hhpn: HC11051-P5
23 SIO_BEEP
R222 2.2K R0603 +/-5%
Q23 MMBT3904 SOT23_BEC
C598 16V, X7R, +/-10% 0.1uF
C561 16V, X7R, +/-10% 0.1uF
C599 16V, X7R, +/-10% 0.1uF
C404 dummy 16V, X7R, +/-10% 0.1uF
EC49 dummy 1000uF 6.3V, +/-20% CE35D80H200
C594 0.1uF dummy 16V, X7R, +/-10%
EC50 dummy 470uF 16V, +/-20% CE35D80H200
C595 C0603 0.1uF 25V, Y5V, +80%/-20%
C566 0.1uF 16V, X7R, +/-10%
R212 1K +/-5% R0603 dummy
SPEAKER
R216 1K +/-5% R0603
19,35 SPEAKER
R214 10K +/-5% R0603
R223 100 +/-5% R0603 dummy
Q22 MMBT3904 SOT23_BEC
RN24 150 +/-5% 8P4R0603
BZ1 BUZZER Buzzer
SPEAKER Header_1X4_2
SPEAK
C887 1nF 50V, X7R, +/-10% C0603
R447 10K +/-5% r0603h6
R462 10K +/-5% r0603h6 dummy
SATA_HDLED*
BAT1_1 Battery
FOXCONN®
FOXCONN PCEG
Title
PWR Connector / Front Panel / VBAT
Size Custom
Document Number C51GM06
Rev A
Date: Friday, April 14, 2006
Sheet 29 of 38



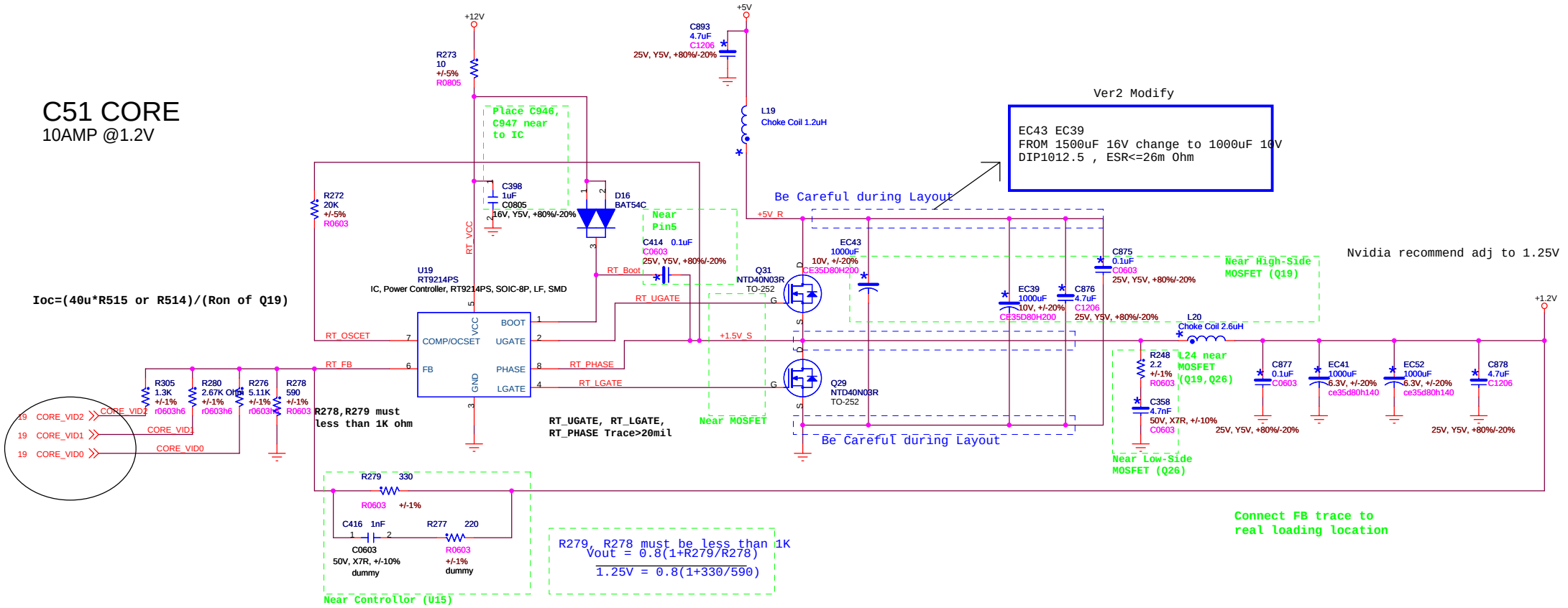
FOXCONN PCEG

Title: ACPI / Mem VDD / Mem Vtt Vreg

Size	Document Number	Rev
A	C51GM06	A

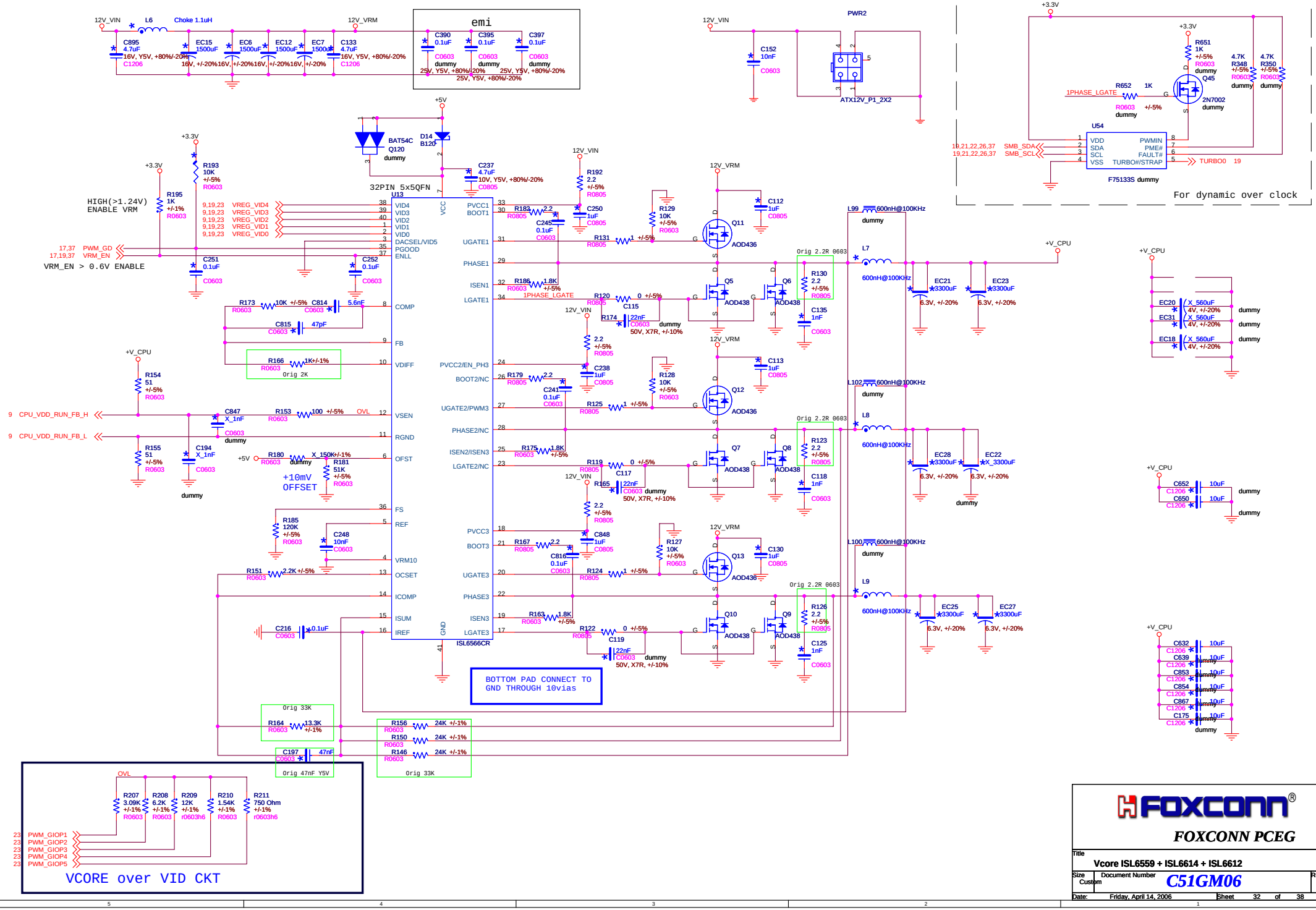
Date: Friday, April 14, 2006 Sheet 30 of 38

C51 CORE
10AMP @1.2V



FOXCONN PCEG

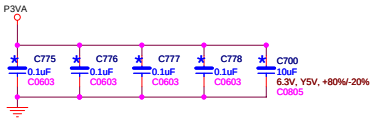
Title: CK804 Core / HT Vregs		
Size: Custom	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 31 of 38	


emi
32PIN 5x5QFN
U13
ISL6566CR
VCORE over VID CKT
For dynamic over clock
BOTTOM PAD CONNECT TO GND THROUGH 10vias
+10mV OFFSET
HIGH(>1.24V) ENABLE VRM
VRM_EN > 0.6V ENABLE
F75133S dummy
ATX12V_P1_2X2
FOXCONN PCEG
Vcore ISL6559 + ISL6614 + ISL6612
C51GM06
Friday, April 14, 2006
Sheet 32 of 38

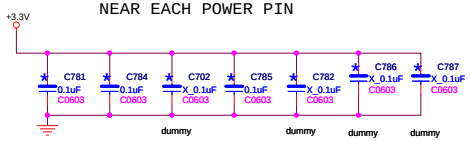
IEEE-1394

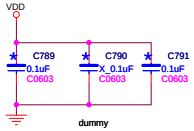
INTF# AD22

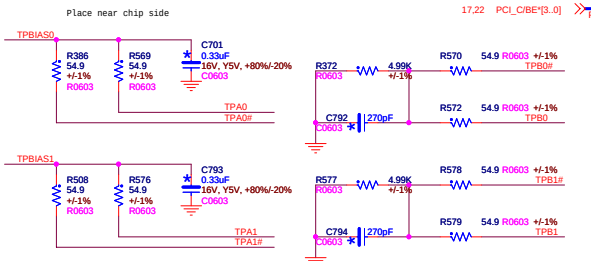
Did not support S3 wake-up

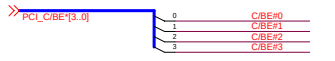


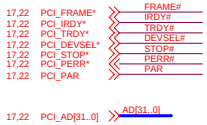
NEAR EACH POWER PIN

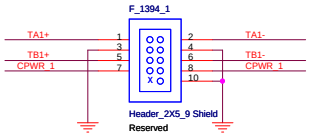


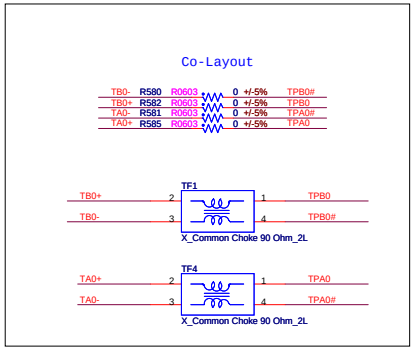


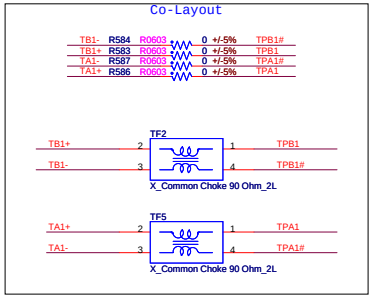


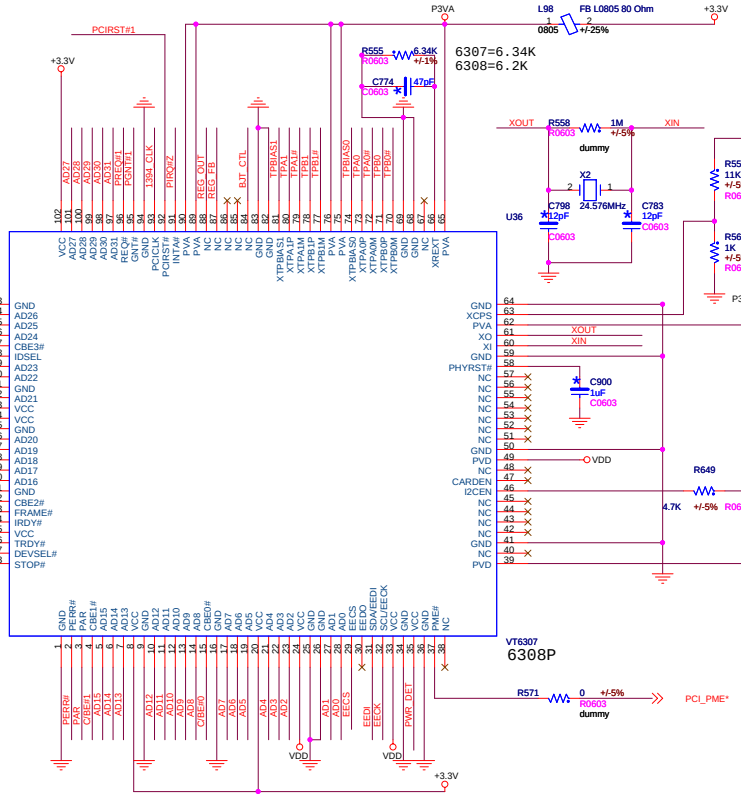


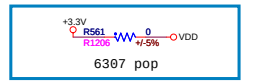


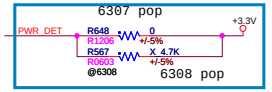


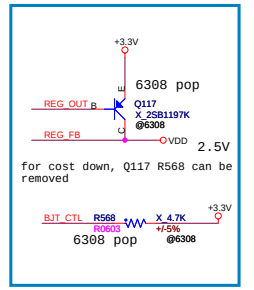


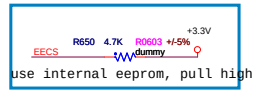


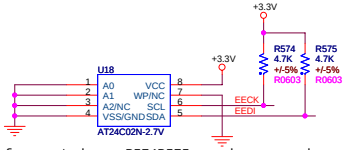




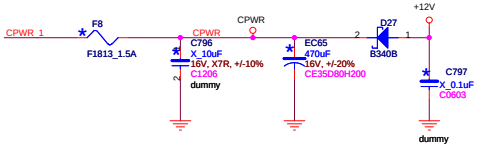






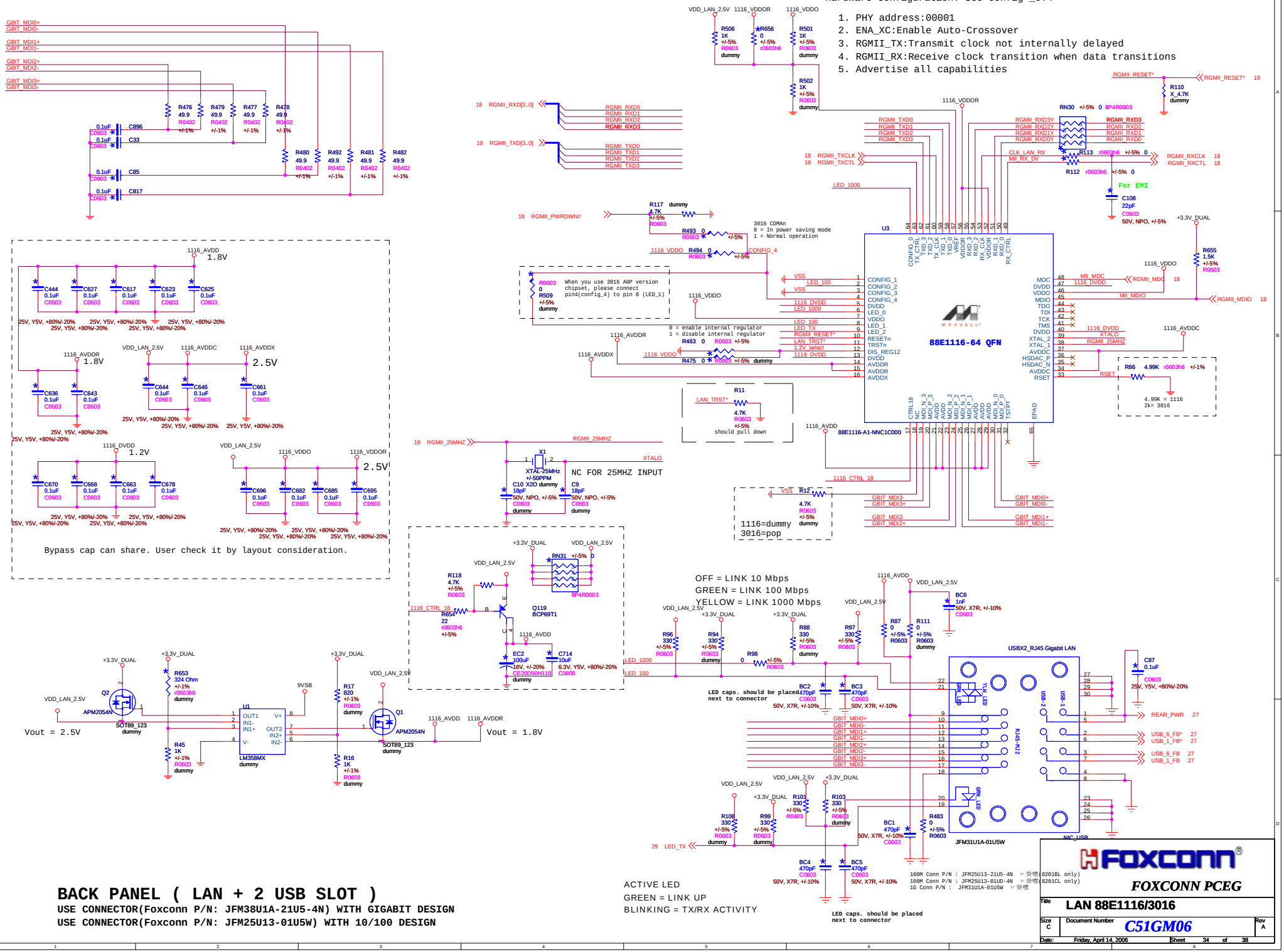


for cost down, R574R575 can be removed



FOXCONN PCEG

Title: VIA1394		
Size: C	Document Number: C51GM06	Rev: A
Date: Friday, April 14, 2006	Sheet 33 of 38	



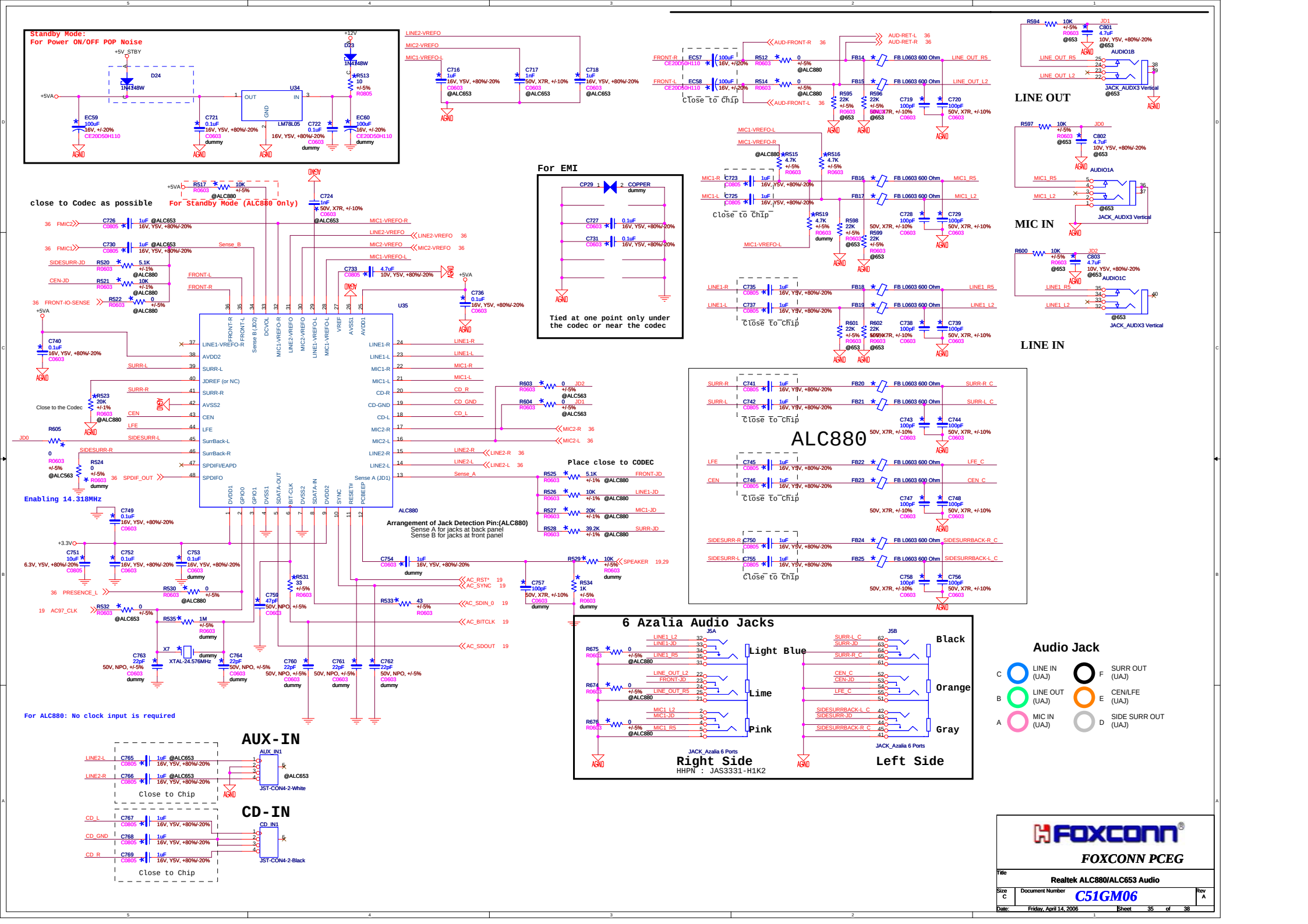
BACK PANEL (LAN + 2 USB SLOT)

USE CONNECTOR(Foxconn P/N: JFM38U1A-21U5-4N) WITH GIGABIT DESIGN

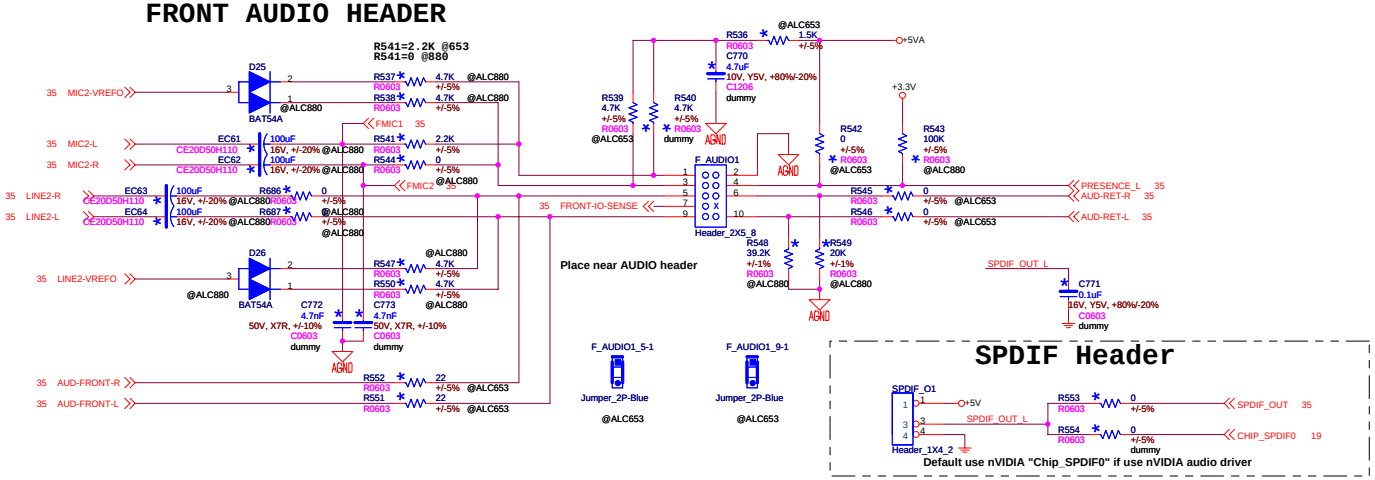
USE CONNECTOR(Foxconn P/N: JFM25U13-01U5W) WITH 10/100 DESIGN

FOXCONN PCEG

Title	LAN 88E1116/3016	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 34 of 38	


Standby Mode:
For Power ON/OFF POP Noise
close to Codec as possible
For Standby Mode (ALC880 Only)
For EMI
Tied at one point only under the codec or near the codec
Close to Chip
Close to the Codec
Place close to CODEC
Enabling 14.318MHz
ALC880
Arrangement of Jack Detection Pin:(ALC880)
Sense A for jacks at back panel
Sense B for jacks at front panel
For ALC880: No clock input is required
LINE OUT
MIC IN
LINE IN
6 Azalia Audio Jacks
Right Side
Left Side
HHPN : JAS3331-H1K2
Audio Jack
AUX-IN
CD-IN
FOXCONN PCEG
Realtek ALC880/ALC653 Audio
C51GM06
Friday, April 14, 2006
Sheet 35 of 38

FRONT AUDIO HEADER

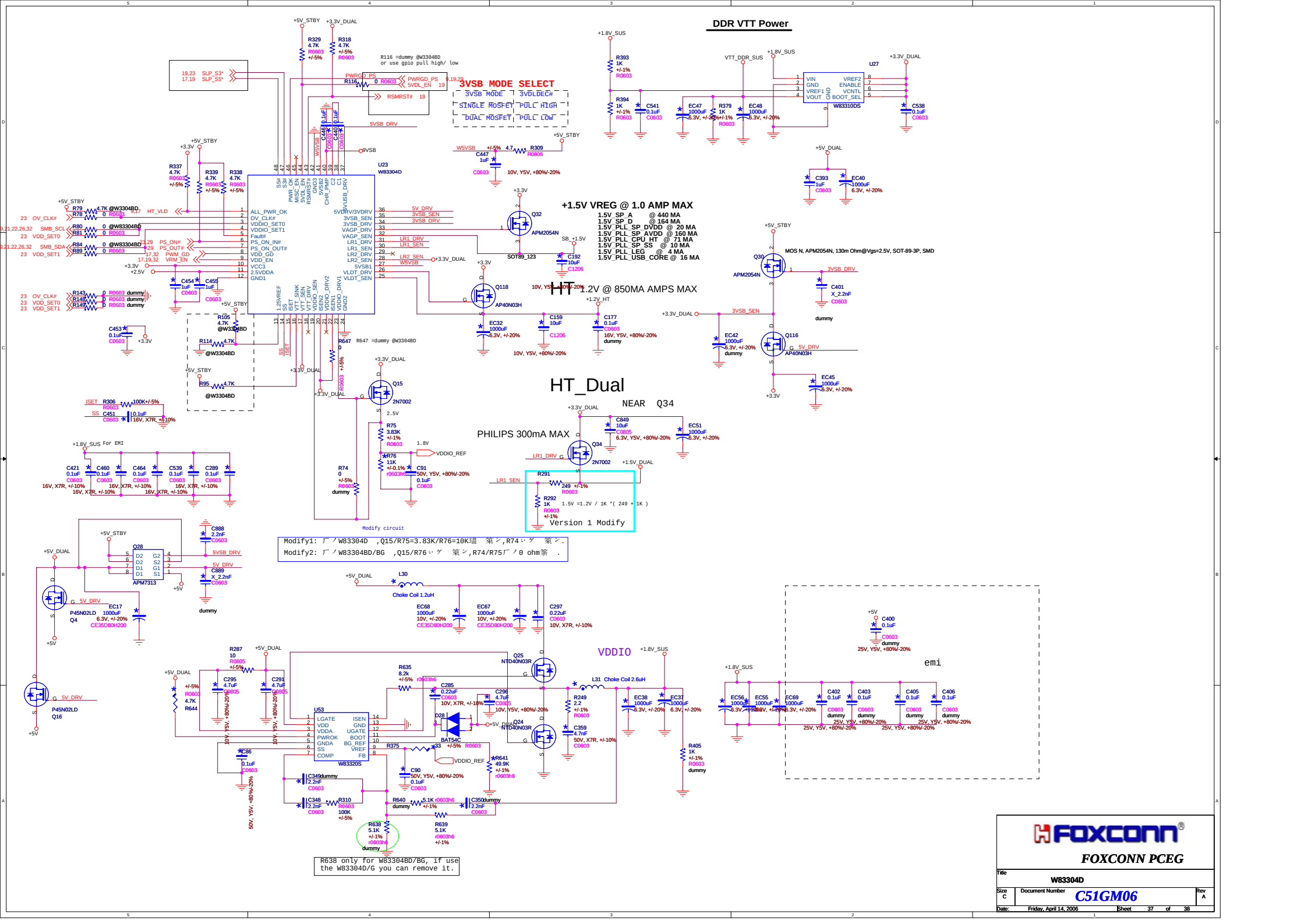


SPDIF Header

Default use nVIDIA "Chip_SPDIF0" if use nVIDIA audio driver

FOXCONN PCEG

Title	Realtek ALC880/ALC653 Audio_Header	
Size C	Document Number C51GM06	Rev A
Date: Friday, April 14, 2006	Sheet 36 of 38	


DDR VTT Power
3VSB MODE SELECT
3VSB_MODE 3VDLDET#
SINGLE MOSFET PULL HIGH
DUAL MOSFET PULL LOW
+1.5V VREG @ 1.0 AMP MAX
1.5V_SP_A @ 440 MA
1.5V_SP_D @ 164 MA
1.5V_PLL_SP_DVDD @ 20 MA
1.5V_PLL_SP_AVDD @ 160 MA
1.5V_PLL_CPU_HT @ 71 MA
1.5V_PLL_SP_SS @ 10 MA
1.5V_PLL_LEG @ 4 MA
1.5V_PLL_USB_CORE @ 16 MA
HT 1.2V @ 850MA AMPS MAX
HT_Dual
NEAR Q34
PHILIPS 300mA MAX
VDDIO
emi
Version 1 Modify
Modify1: 廠ㄨW83304D ,Q15/R75=3.83K/R76=10K璿 築ン,R74い ゲ 築ン.
Modify2: 廠ㄨW83304BD/BG ,Q15/R76い ゲ 築ン,R74/R75廠ㄨ0 ohm築 .
R638 only for W83304BD/BG, if use the W83304D/G you can remove it.
FOXCONN PCEG
W83304D
C51GM06
Friday, April 14, 2006
Sheet 37 of 38

12/14
(1)Add R365,R323,R204,R191,R196,C852,C160,U14,R444,R448,R329
(2)Delete R368,R500,R332,R189
(3)Change R496,R495---->4.7k
(4)Change R374------>562ohm
(5)Add Q48,Q49,Q50,Q51,Q52,Q53,R657,R658,R659,R660,R661,R662

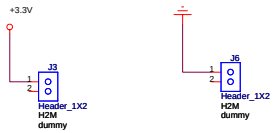
12/15
(1)Add EC68,R503,R666
(2)Delete R498,R499,R497,R509,R511,R510
(3)change page 13 RN to 0402

12/19
(1)Change R658,R660,R662 to 1kohm
(2)dummy R220,R221,R152,J4,RN8,RN9
(3)Add C20,C21,C22,D5,D10,C829,C830,R137,R667,R668,R669,R670
(4)change RN26,RN30,R300,R297,R113,R112 to Oohm
(5)FWH_TBL* change gpio pin

12/21
(1)dummy R613,Q2,R653,EC10,R45,U1,R17,R16,Q1
(2)ADD RN31,Q119,R654,R118

12/22
(1)dummy EC68,C734,C732,R638
(2)add C192,D29,F9

12/27
(1)dummy C281,C333,C332,C280,C273



FOXCONN PCEG

Title: SSTL-2 Termination Resistors

Size: Custom | Document Number: C51GM06 | Rev: A

Date: Friday, April 14, 2006 | Sheet 38 of 38