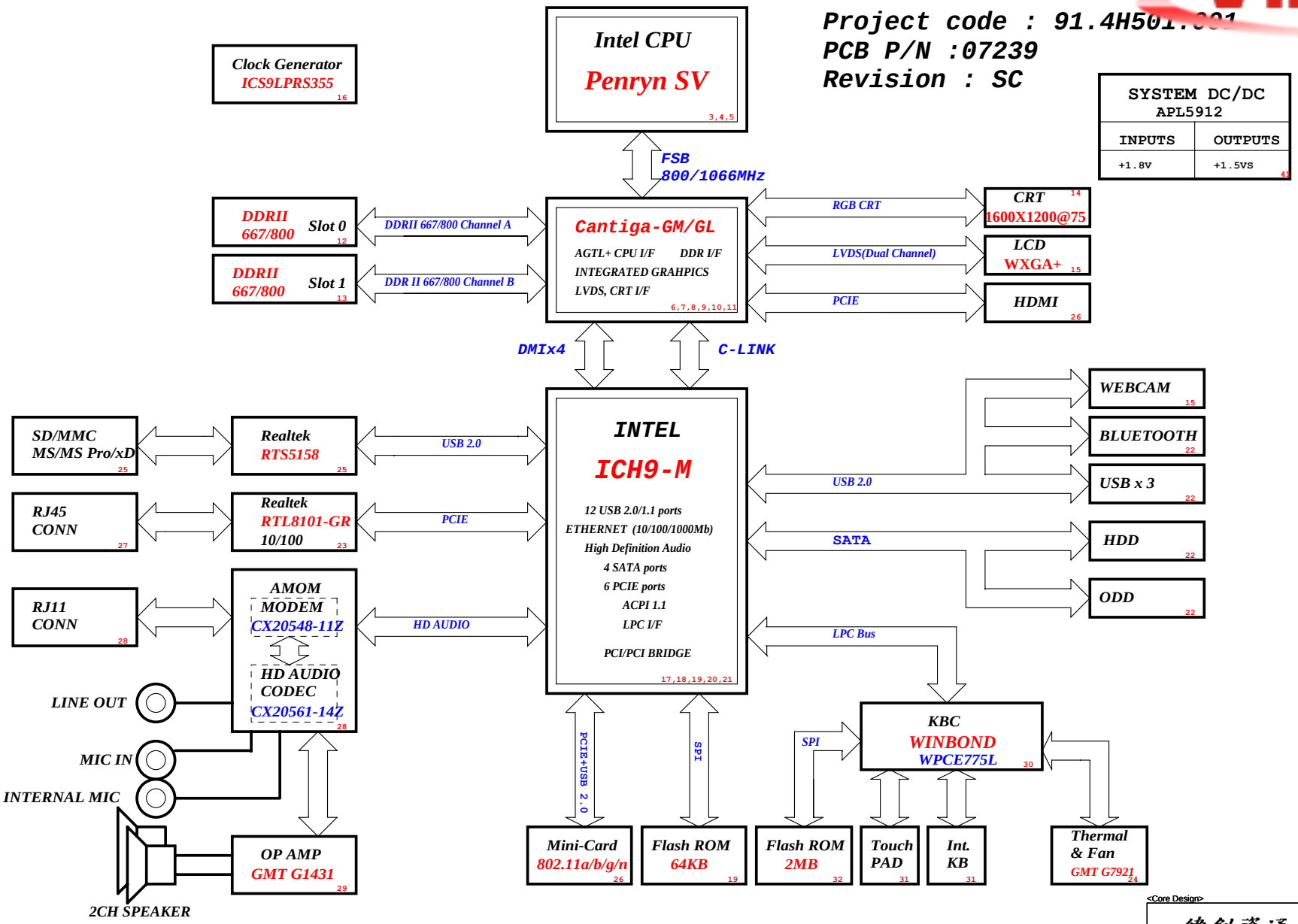
Warrior Intel UMA Block Diagram

Project code : 91.4H501.001
PCB P/N :07239
Revision : SC



SYSTEM DC/DC APL5912	
INPUTS	OUTPUTS
+1.8V	+1.5VS 43

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
DCBATOUT	+0.9VS +1.8V 39

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
+5VALW	+1.05V 40

MAXIM CHARGER MAX8731	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 34

CPU DC/DC ISL6269CCRZ	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 22A 36,37

SYSTEM DC/DC	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 38

PCB LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: Block Diagram

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A3	Warrior	SC

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

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LANE1	LAN
LANE2	MiniCard WLAN

USB Table

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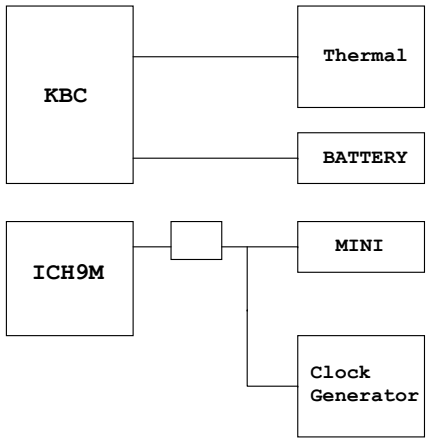
USB	
Pair	Device
0	USB3
1	FREE
2	External USB3
3	FREE
4	External USB2
5	FREE
6	WLAN
7	BLUETOOTH
8	CARD_READER
9	FREE
10	CAMERA
11	FREE

SMBus



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Title: Table of Content

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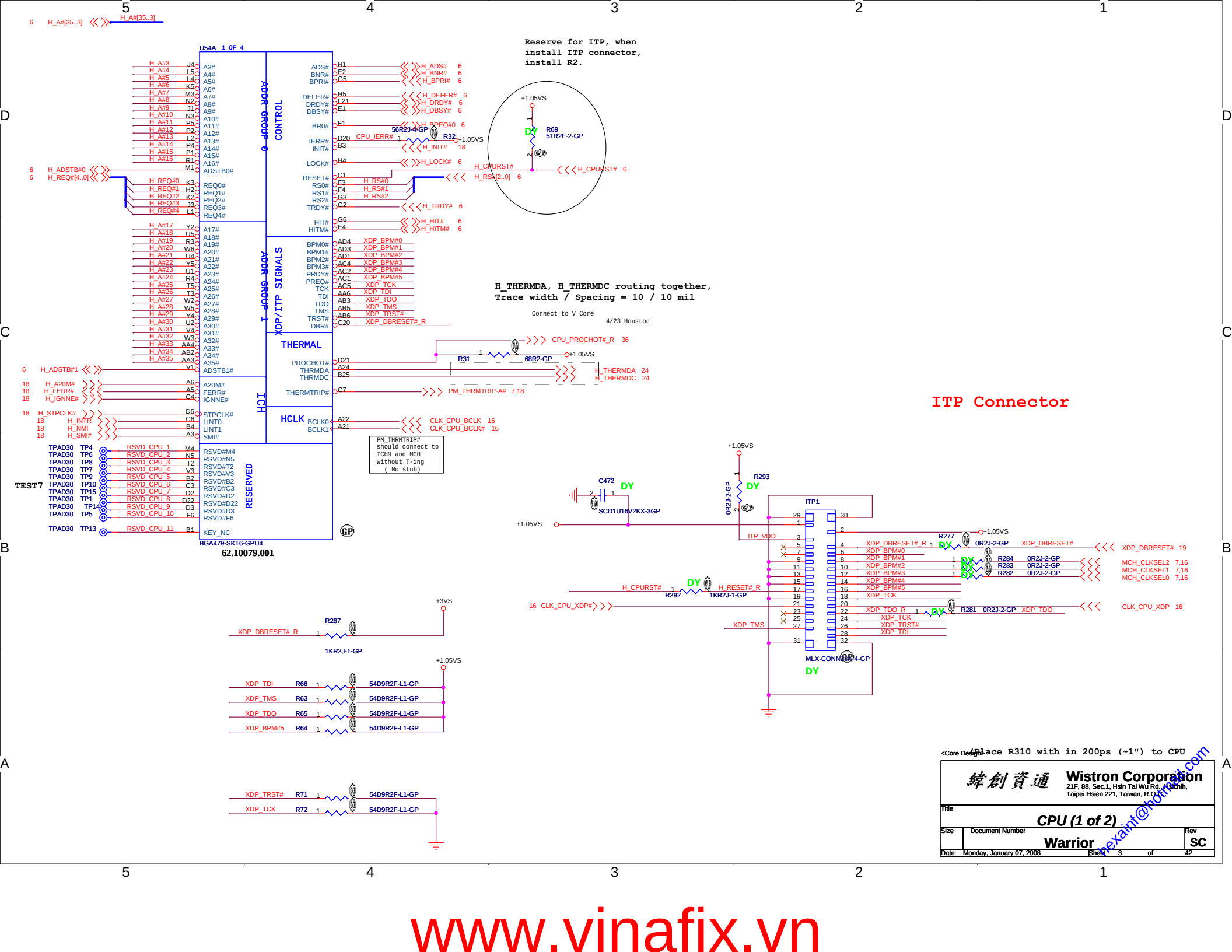

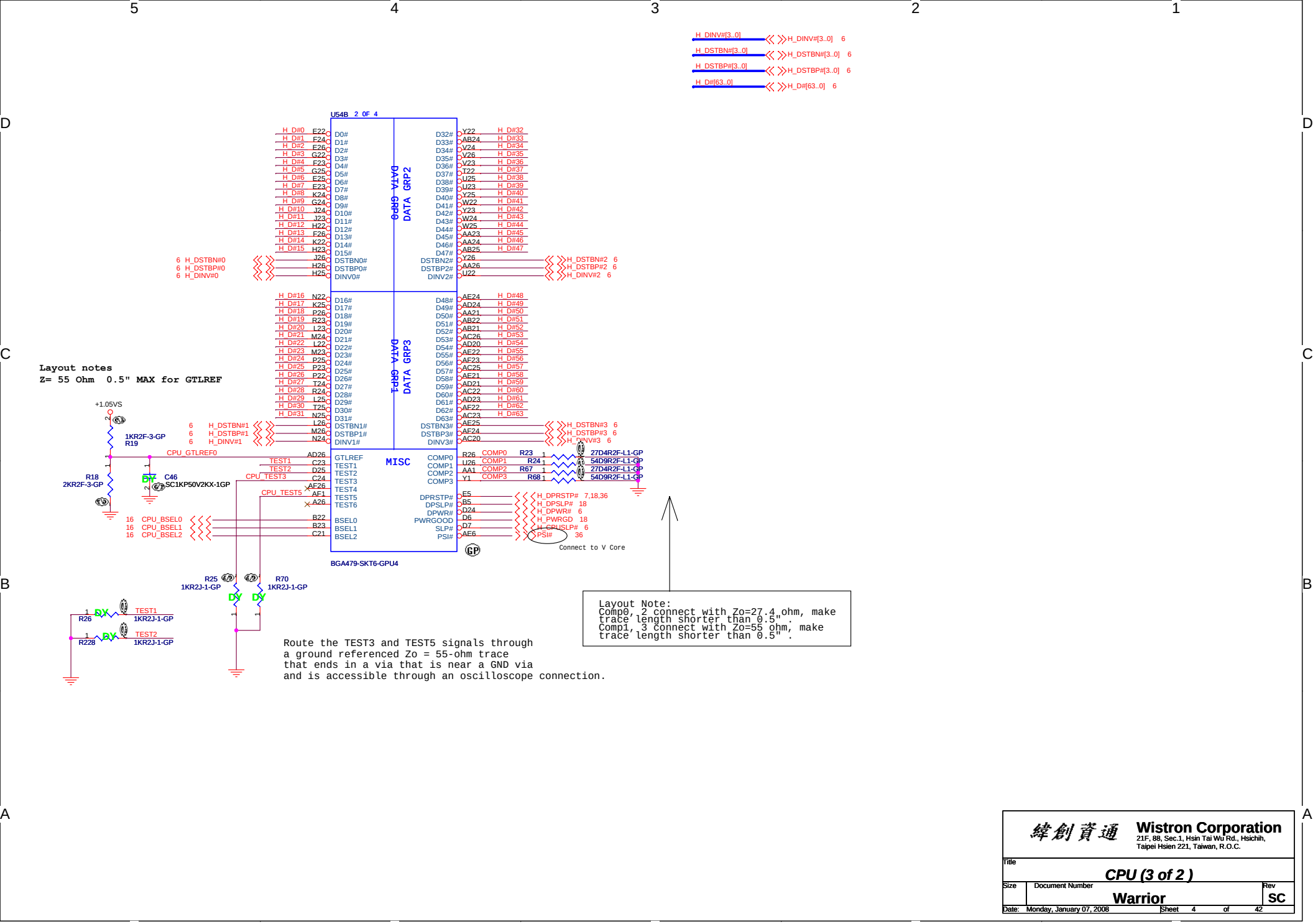

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Title	***CPU (3 of 2)***
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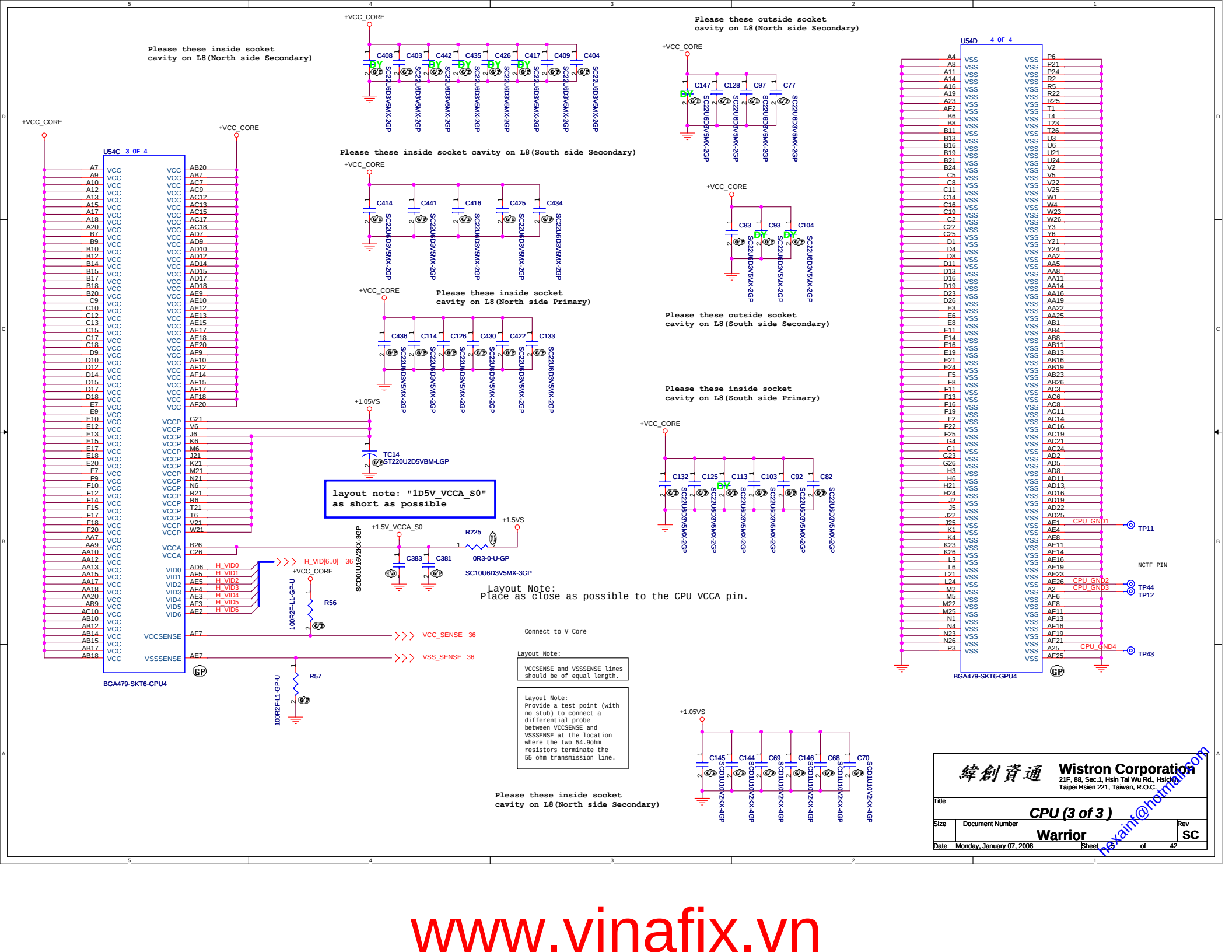

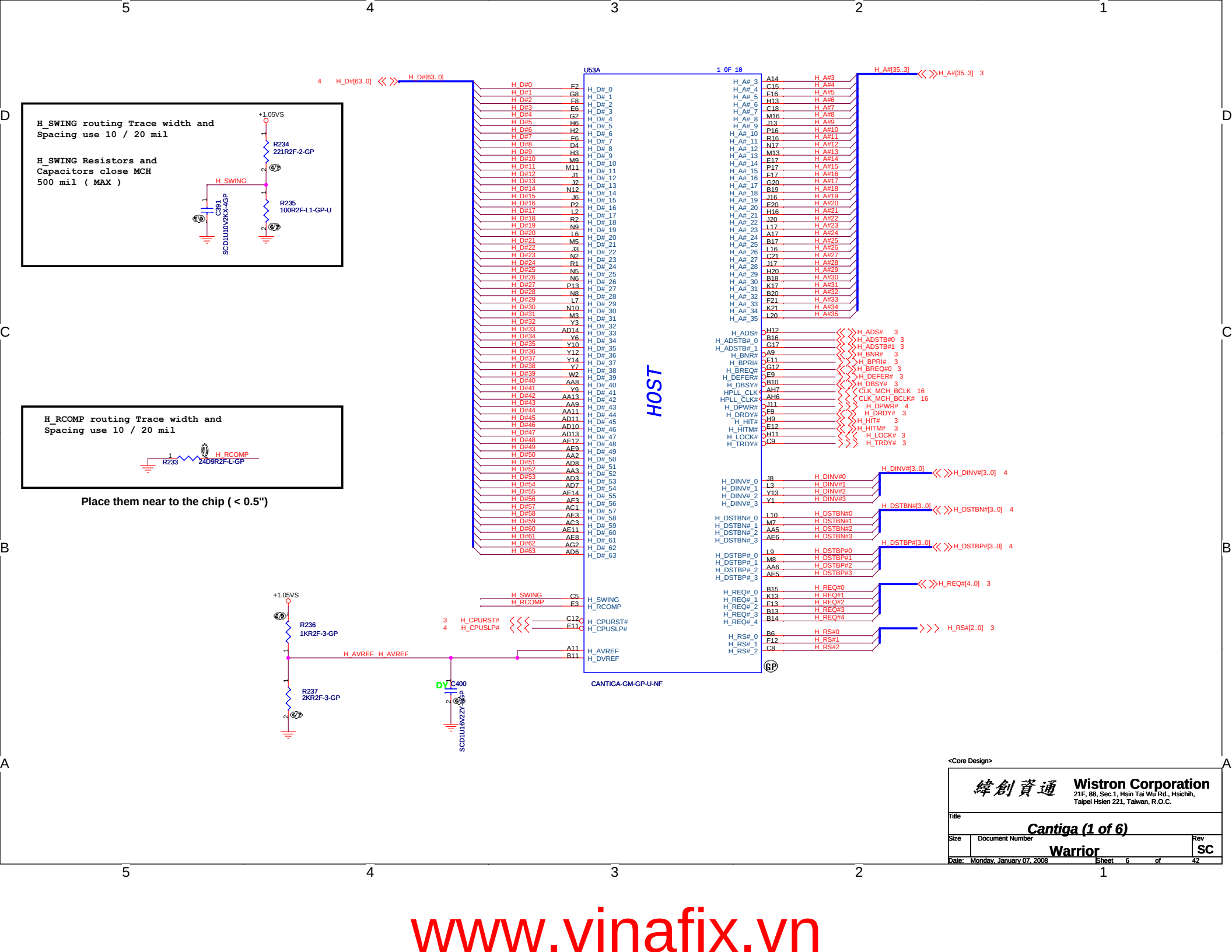

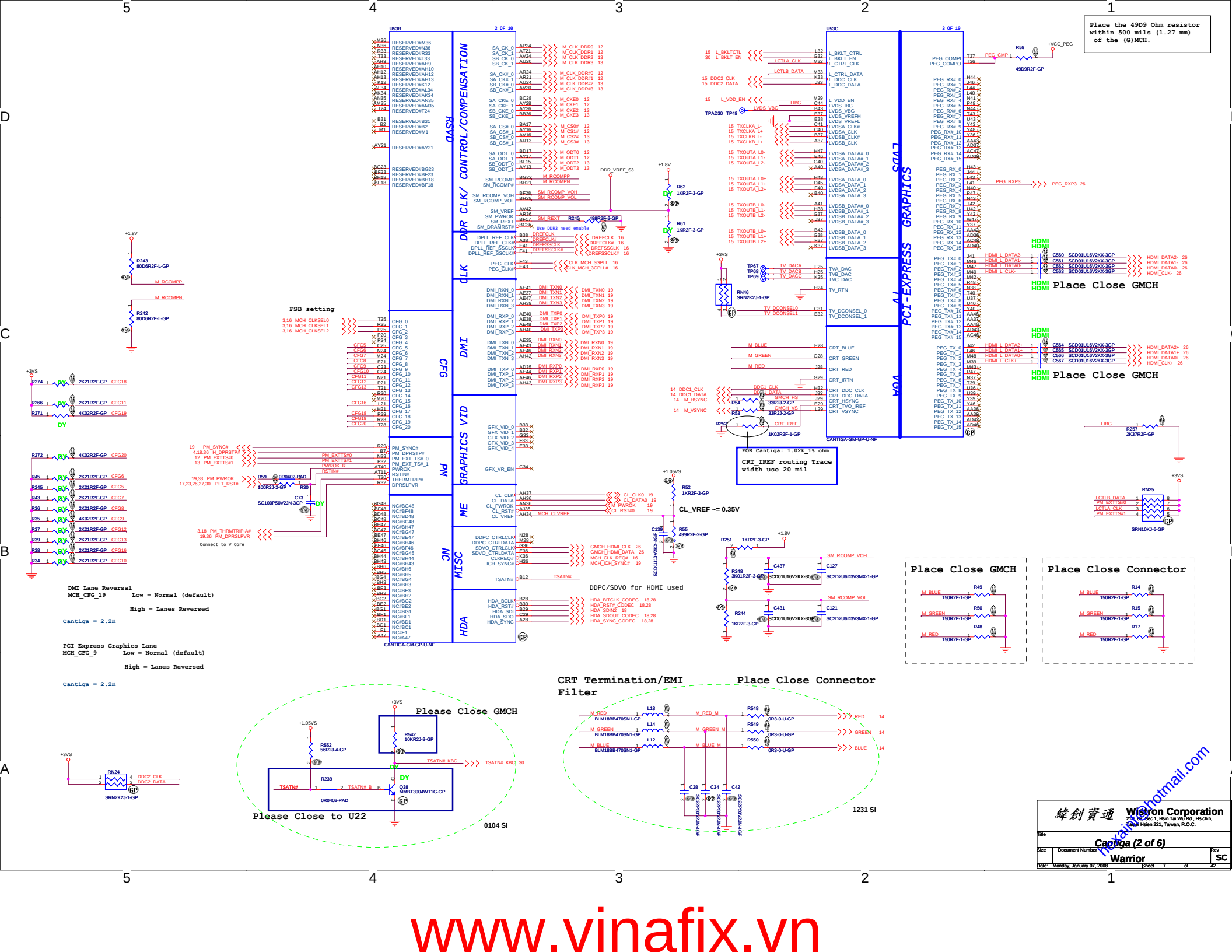

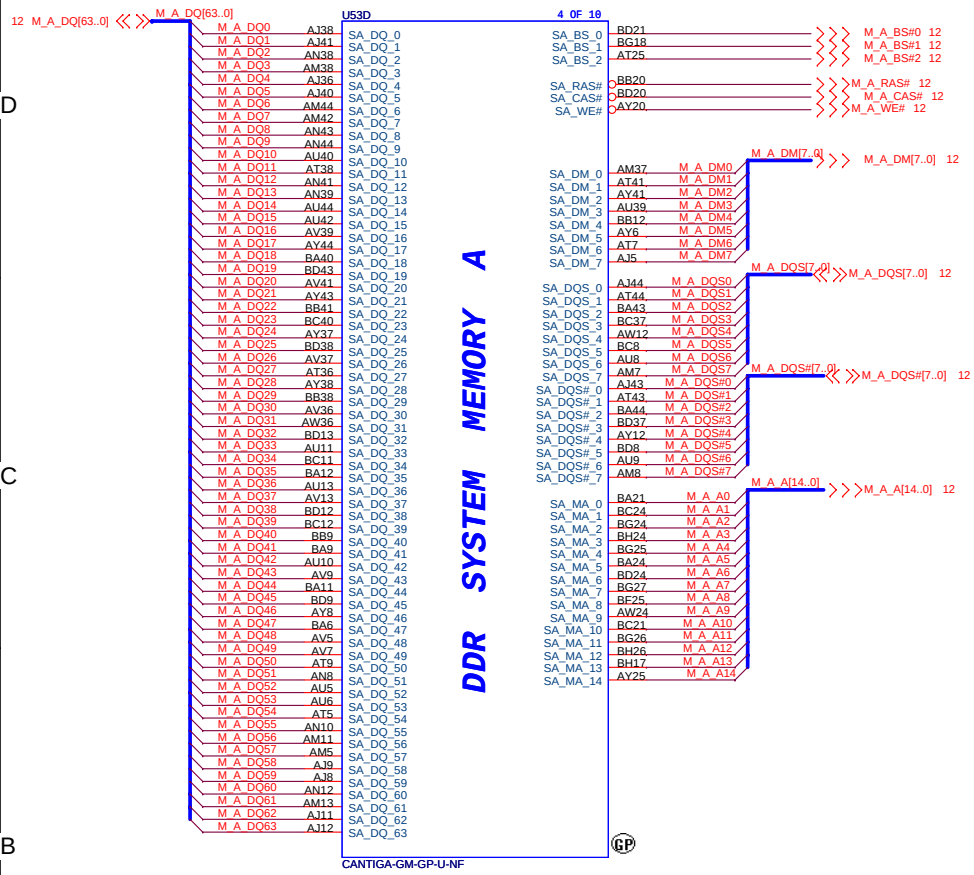

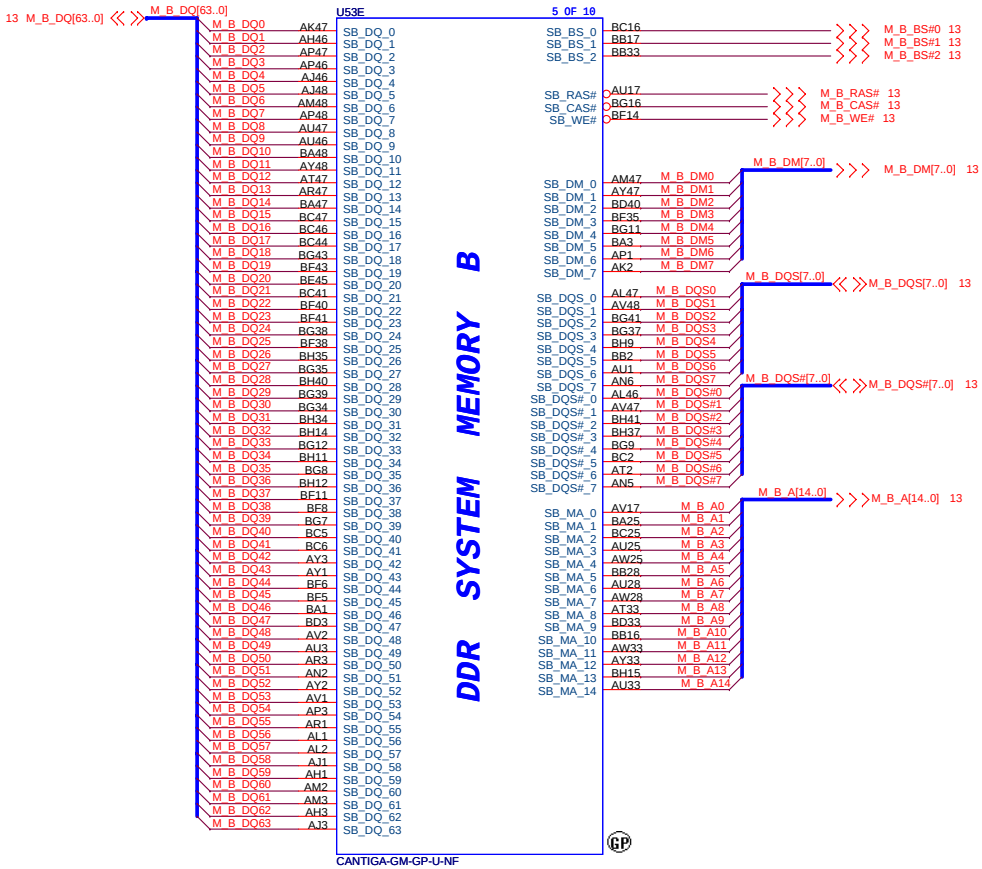

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Title	***Cantiga (3 of 6)***
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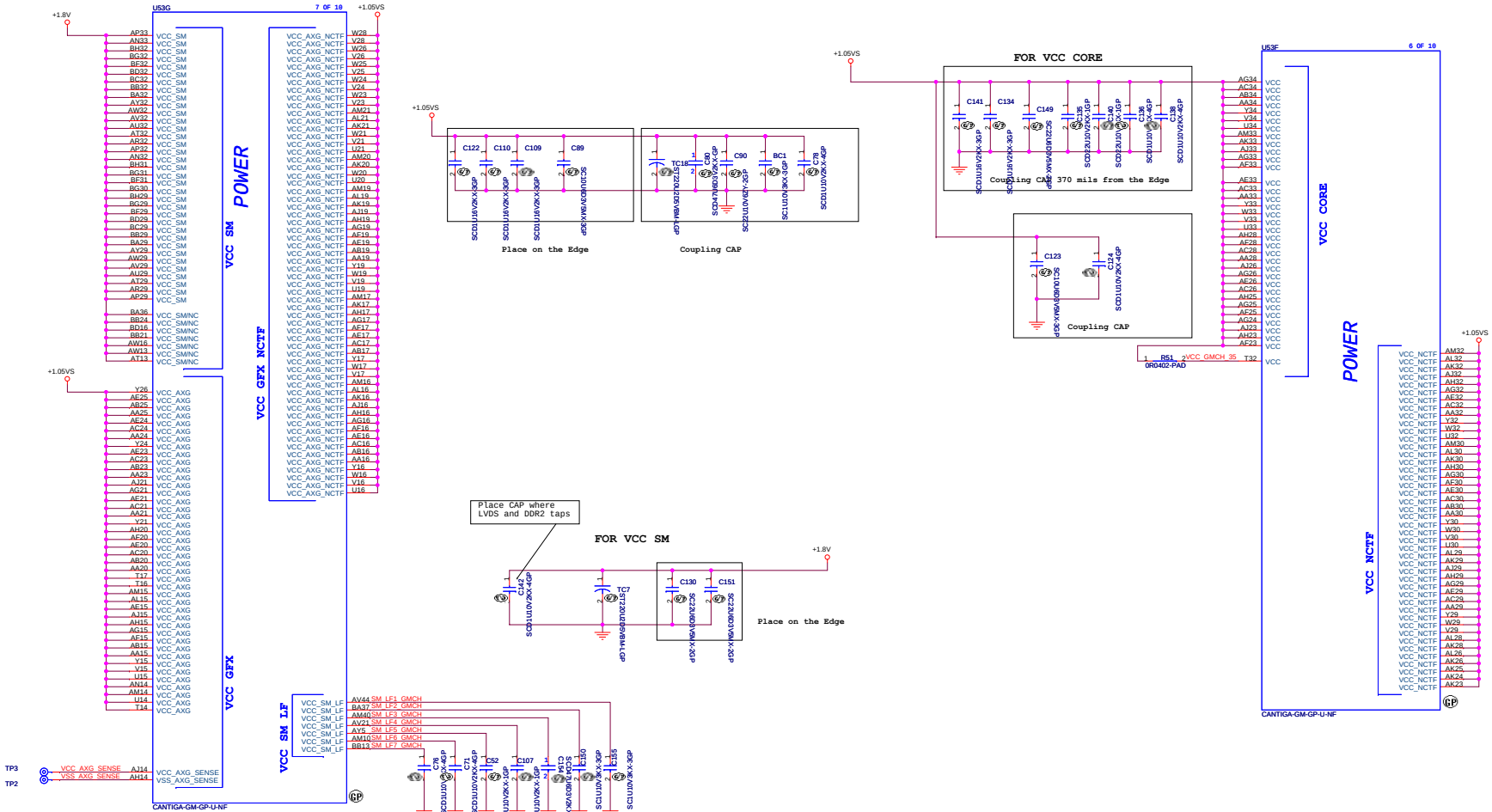

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Title	Cantiga (4 of 6)
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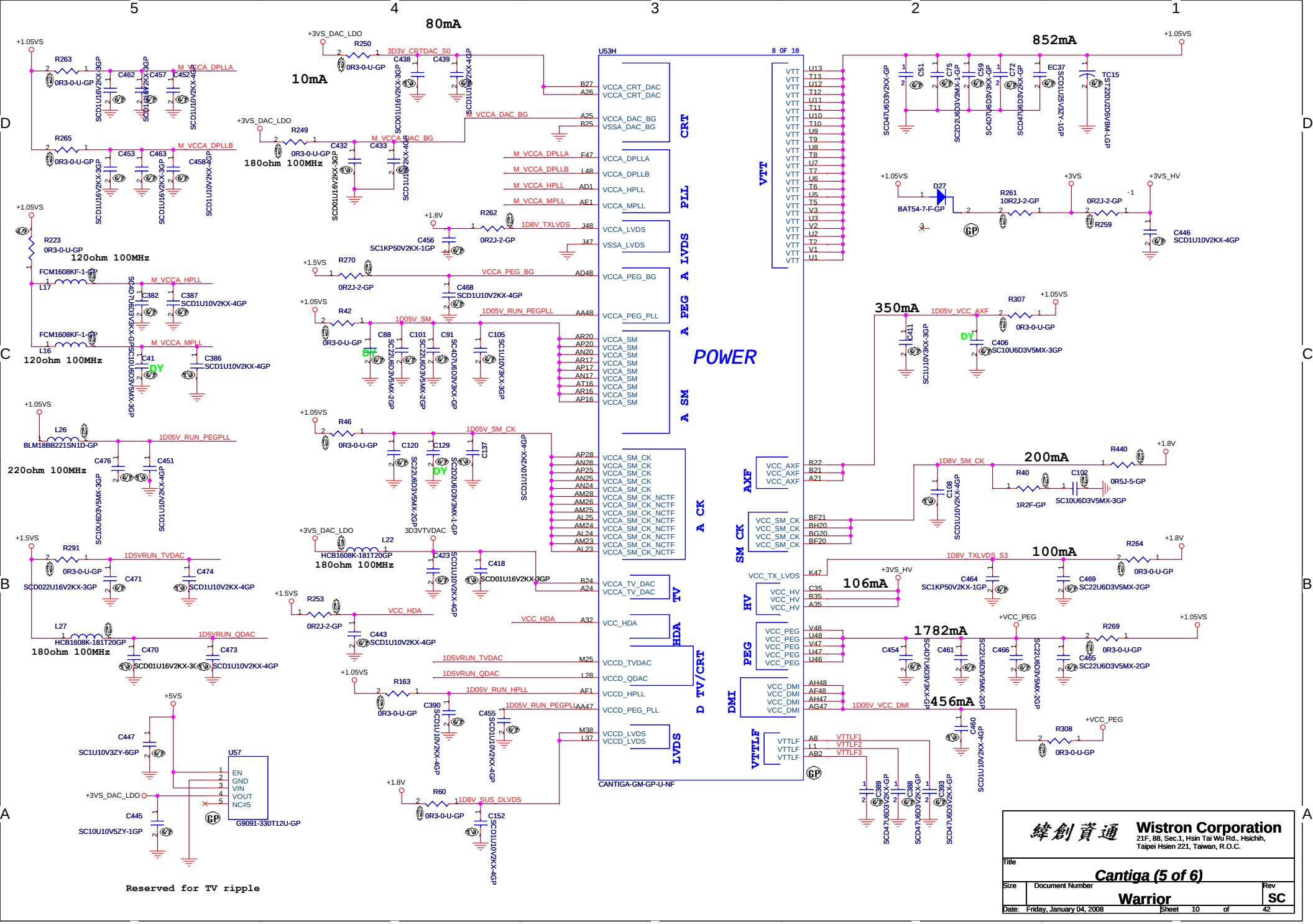

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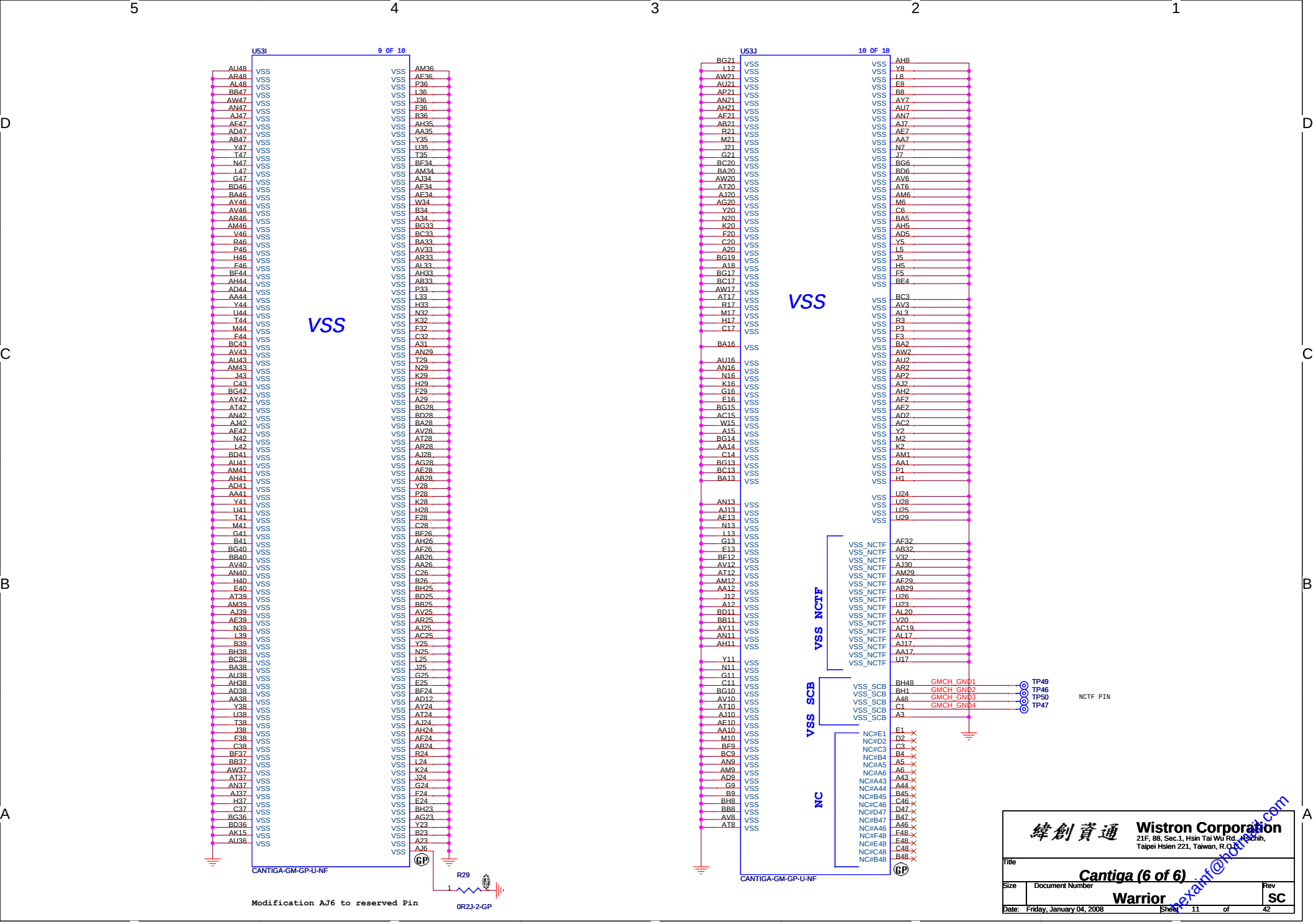

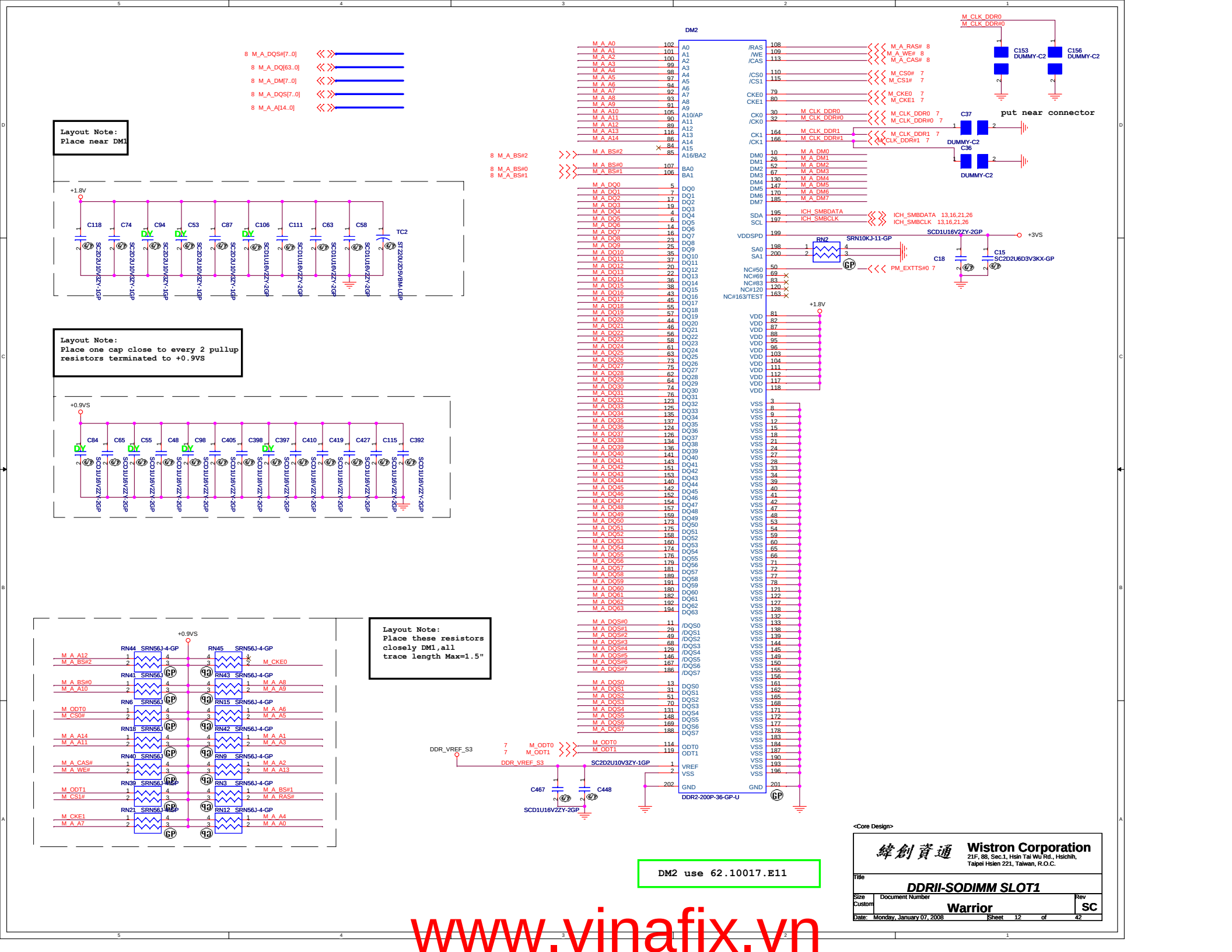

DM2 use 62.10017.E11

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Title: DDRII-SODIMM SLOT1

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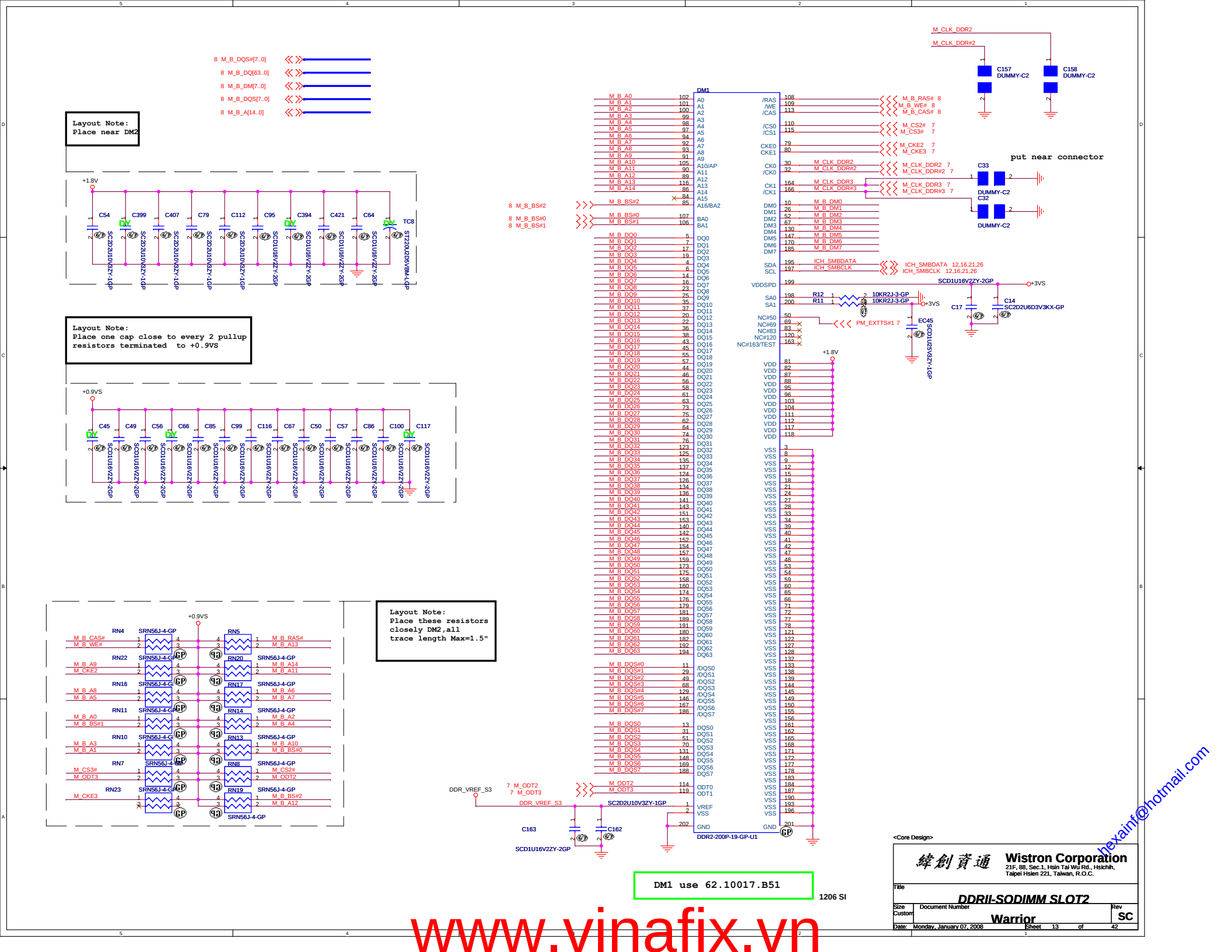
Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"
DM1
DDR2-200P-19-GP-U1
DM1 use 62.10017.B51
1206 SI
put near connector
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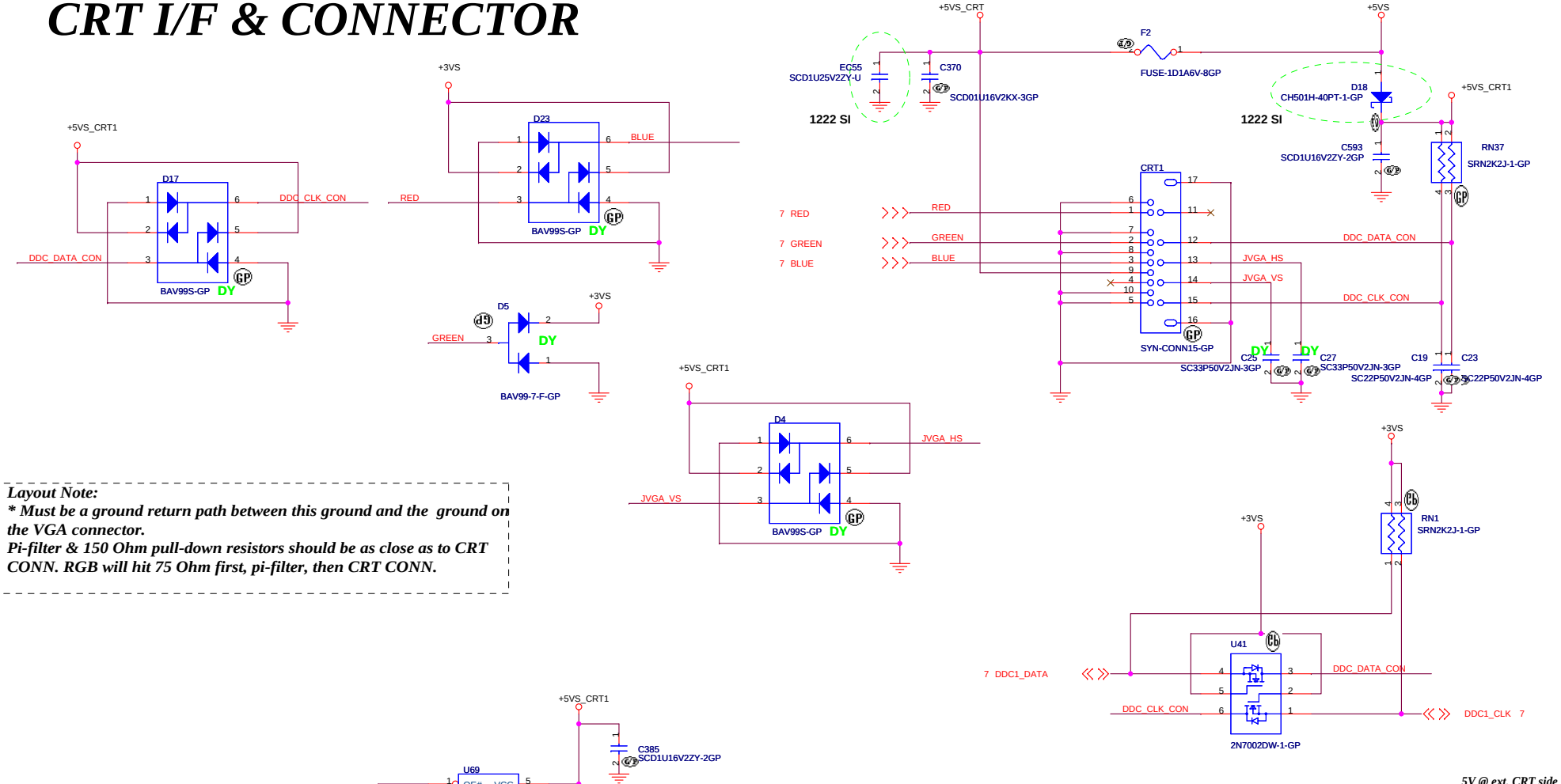
CRT I/F & CONNECTOR



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V @ ext. CRT side

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Title: **CRT Connector**		
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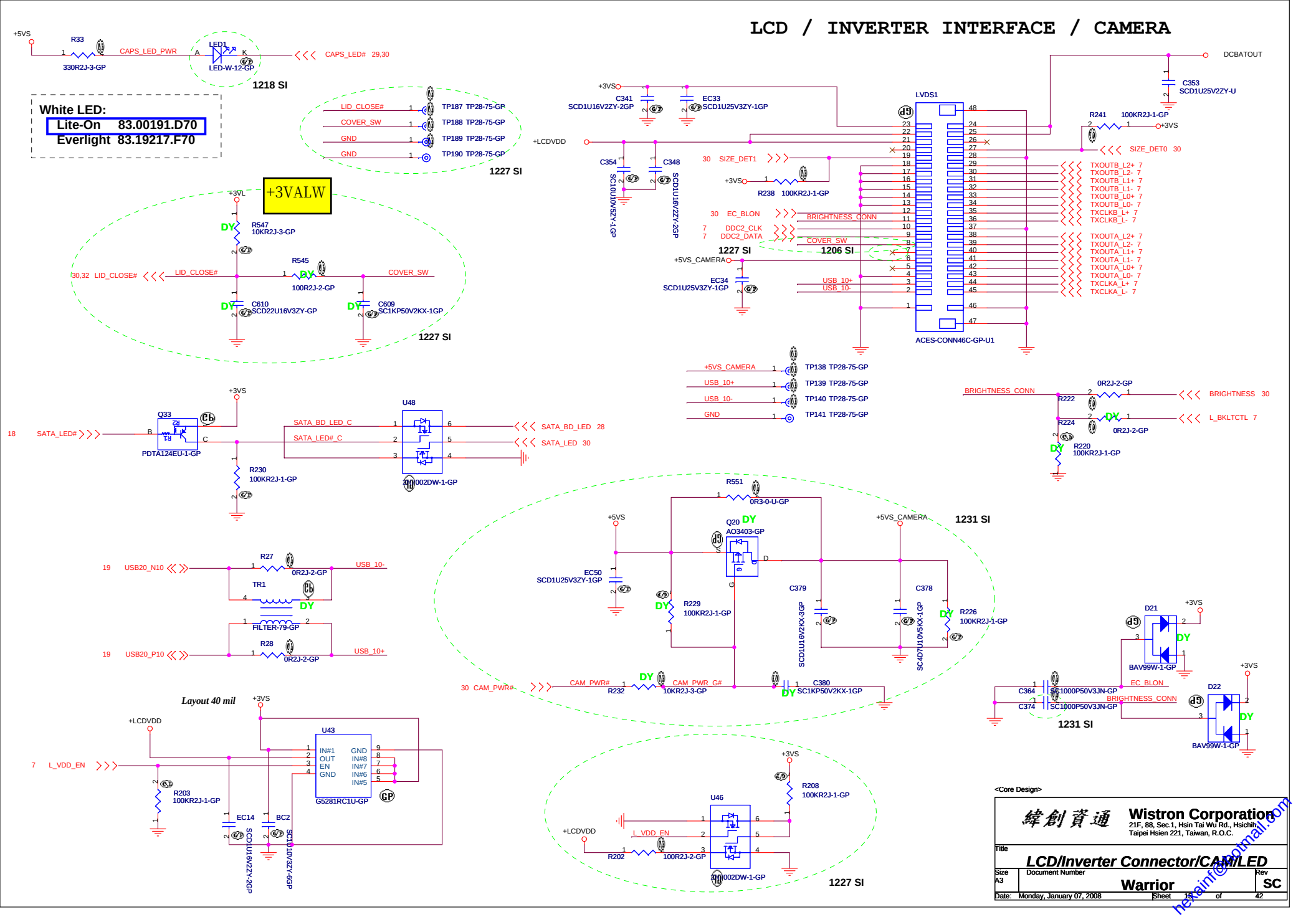
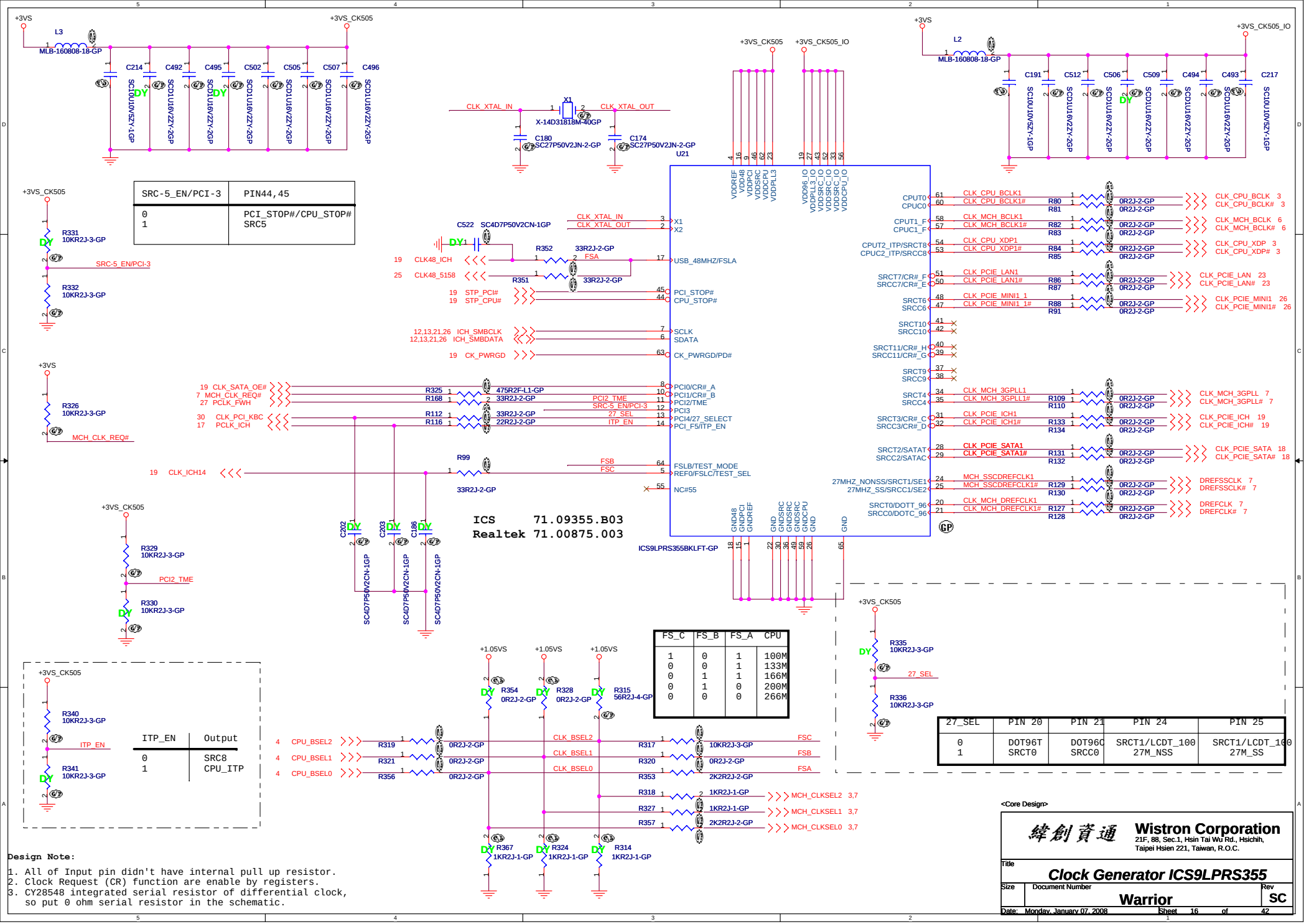
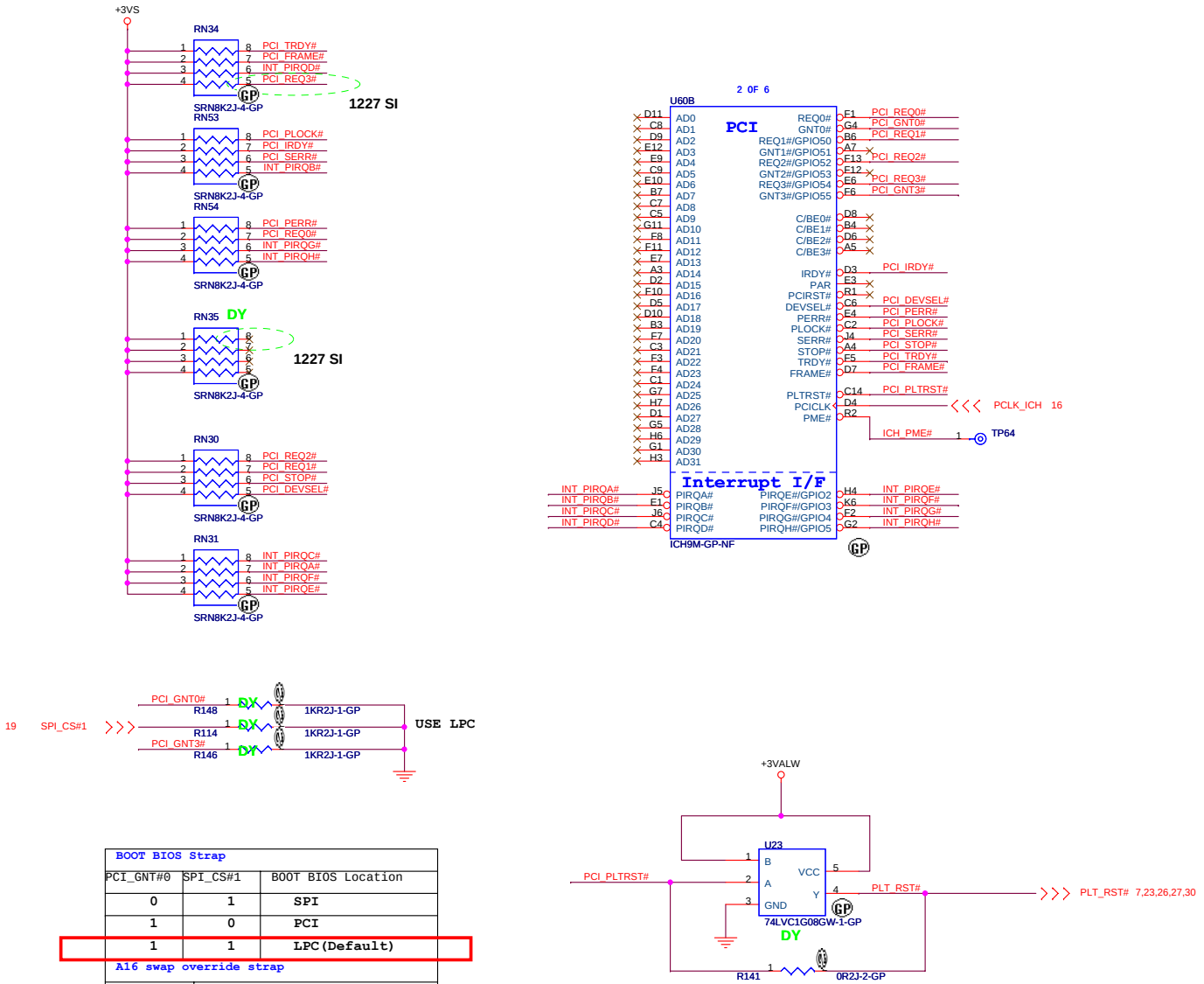
LCD / INVERTER INTERFACE / CAMERA







BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

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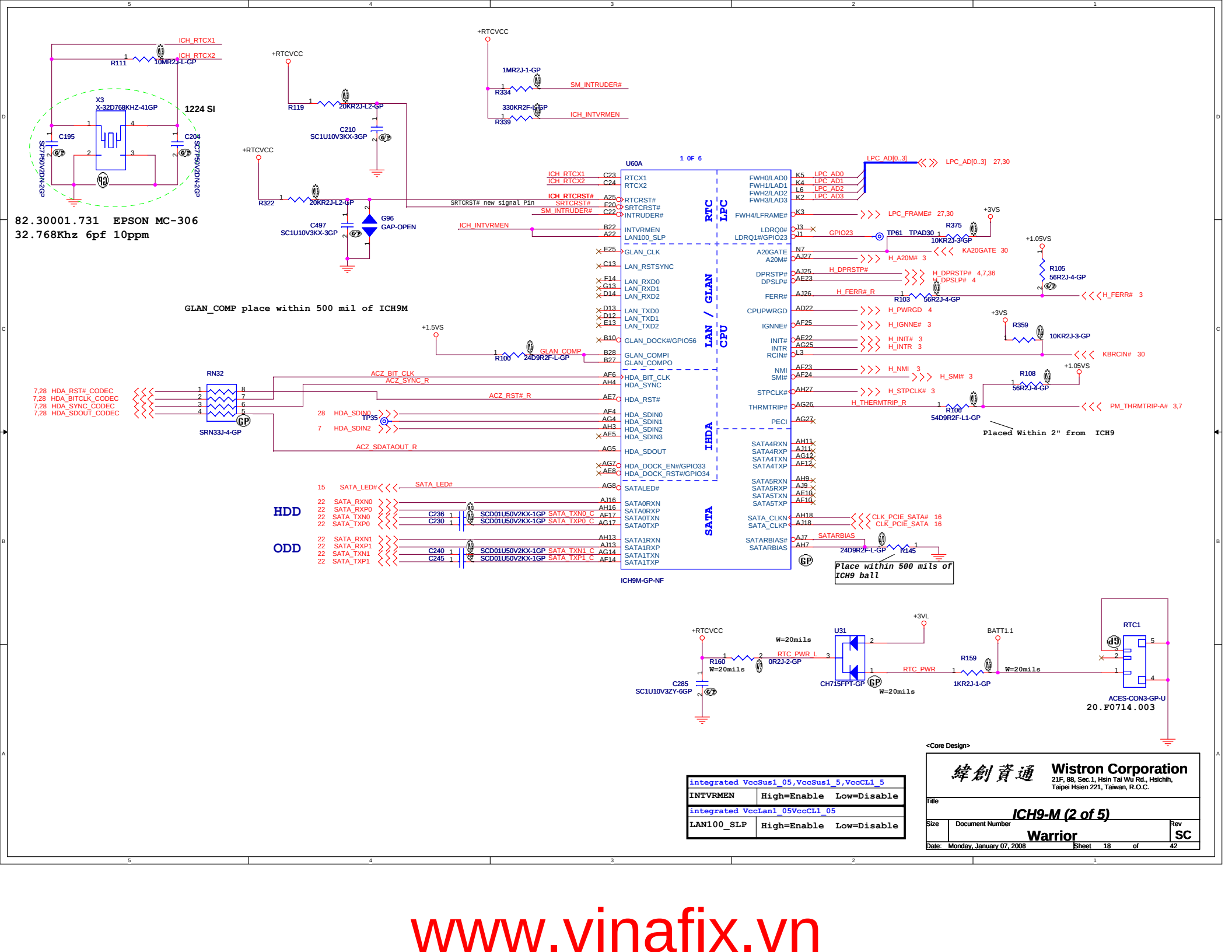
82.30001.731 EPSON MC-306
32.768Khz 6pf 10ppm
GLAN_COMP place within 500 mil of ICH9M
Placed Within 2" from ICH9
Place within 500 mils of ICH9 ball
ICH9M-GP-NF
HDD
ODD
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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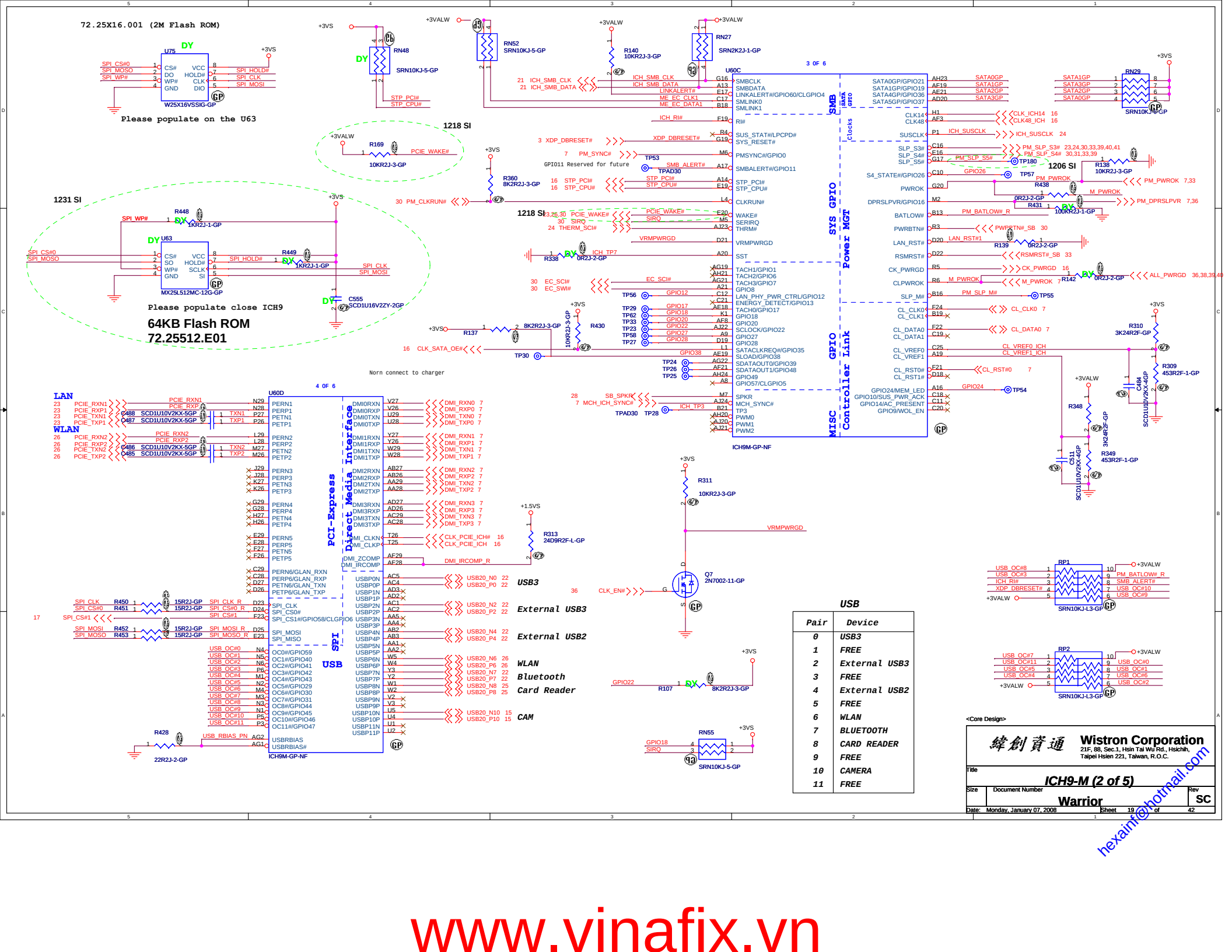
72.25X16.001 (2M Flash ROM)
U75
W25X16VSSIG-GP
Please populate on the U63
1218 SI
1231 SI
U63
MX25L512MC-12G-GP
Please populate close ICH9
64KB Flash ROM
72.25512.E01
Norn connect to charger
4 OF 6
U60D
ICH9M-GP-NF
PCI-Express
Direct Media Interface
SPI
USB
LAN
WLAN
USB3
External USB3
External USB2
WLAN
Bluetooth
Card Reader
CAM
3 OF 6
U60C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
USB
Pair
Device
0
USB3
1
FREE
2
External USB3
3
FREE
4
External USB2
5
FREE
6
WLAN
7
BLUETOOTH
8
CARD READER
9
FREE
10
CAMERA
11
FREE
<Core Design>
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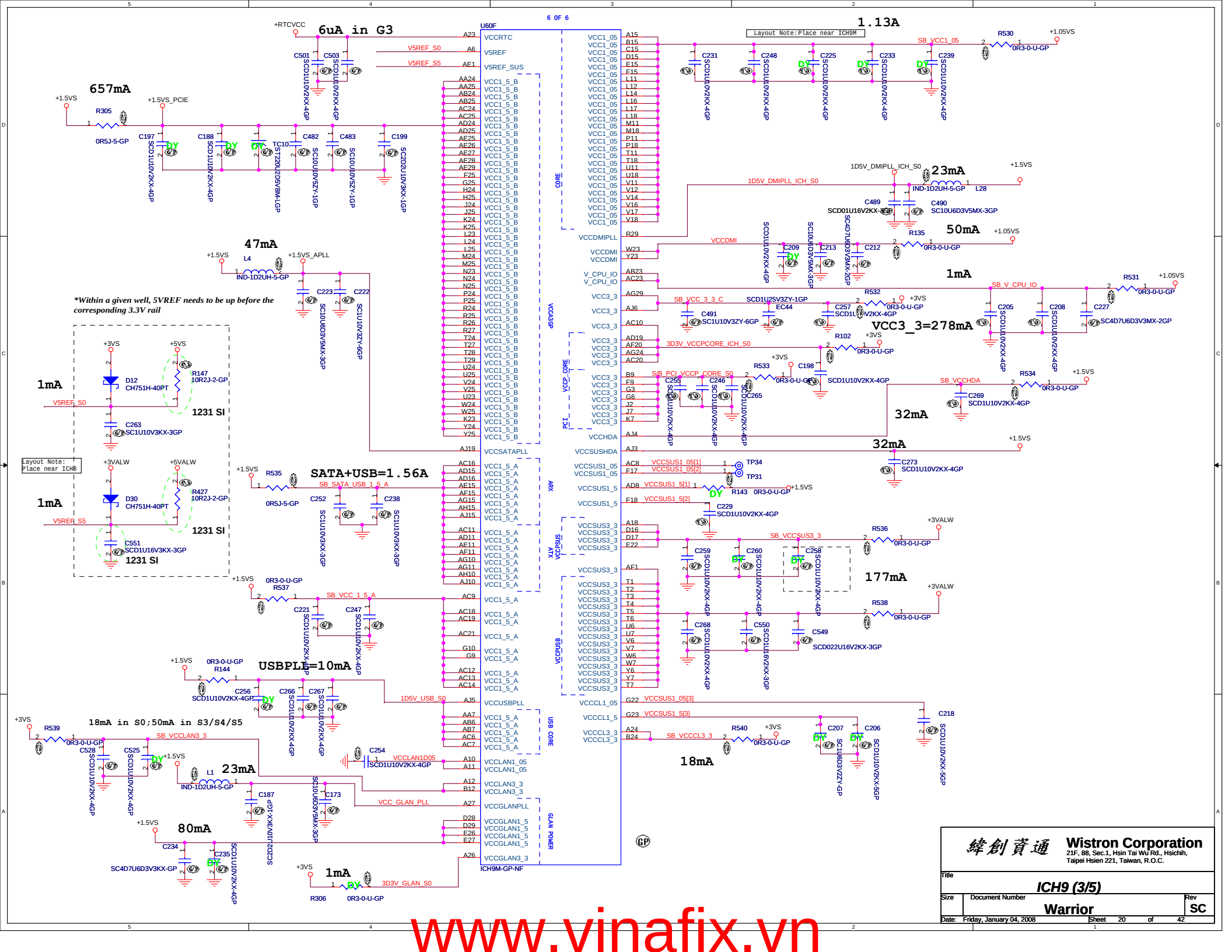
6 OF 6
U60F
ICH9M-GP-NF
6uA in G3
657mA
47mA
1.13A
23mA
50mA
1mA
VCC3_3=278mA
32mA
SATA+USB=1.56A
USBPLL=10mA
177mA
18mA in S0;50mA in S3/S4/S5
80mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH8
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ICH9 (3/5)
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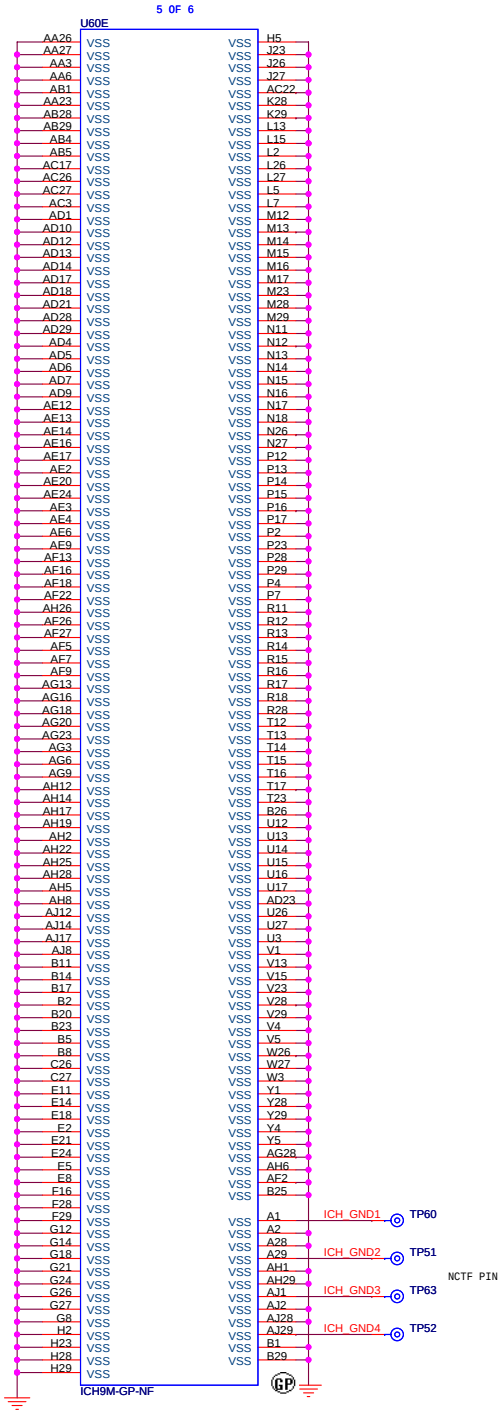

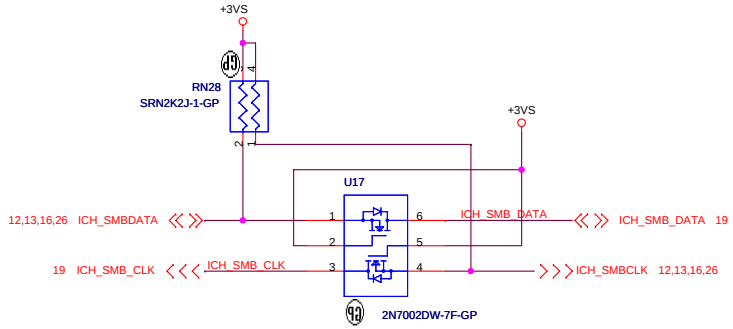

SMBUS

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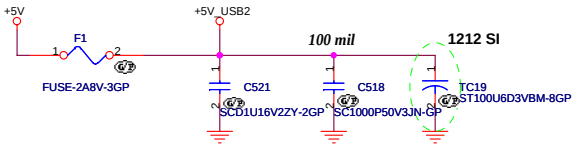
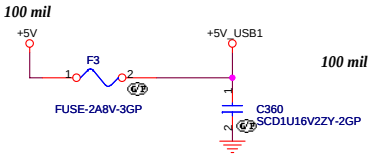
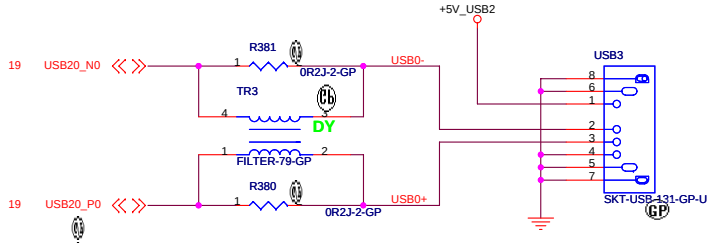
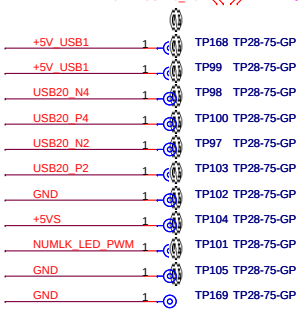
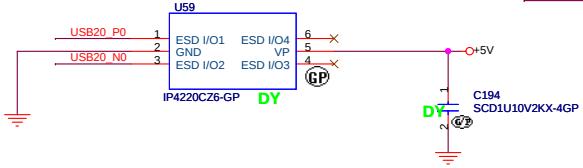
USB PORT

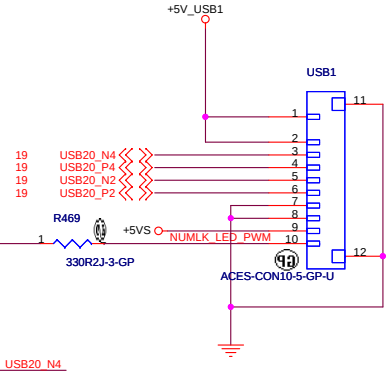


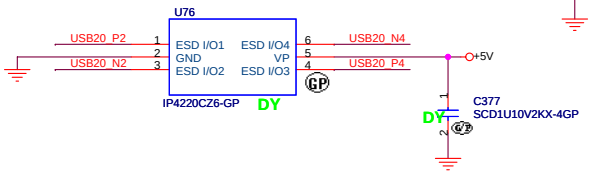




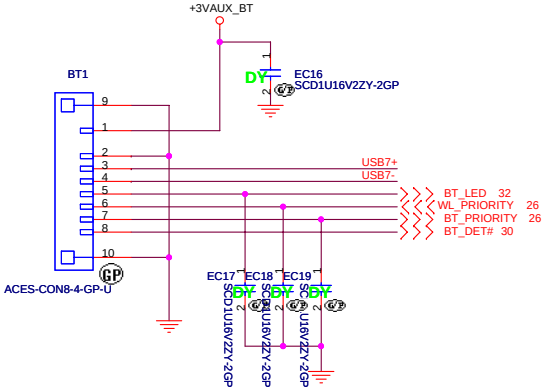


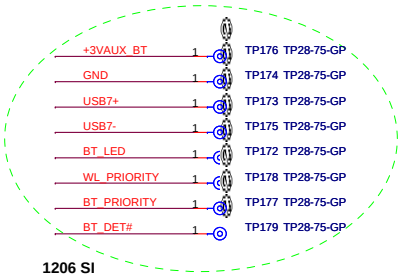


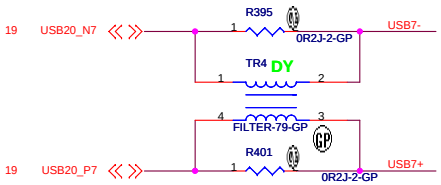


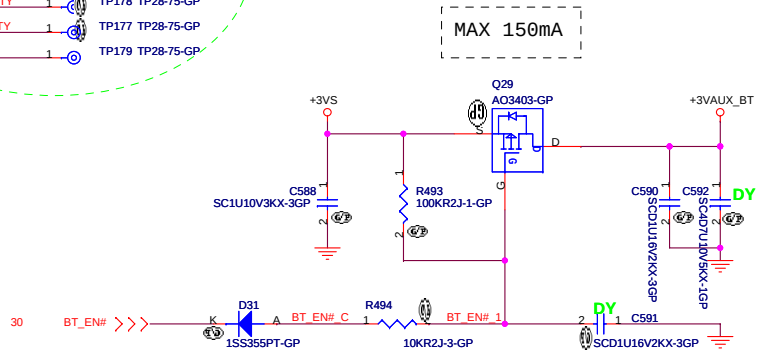


BLUETOOTH

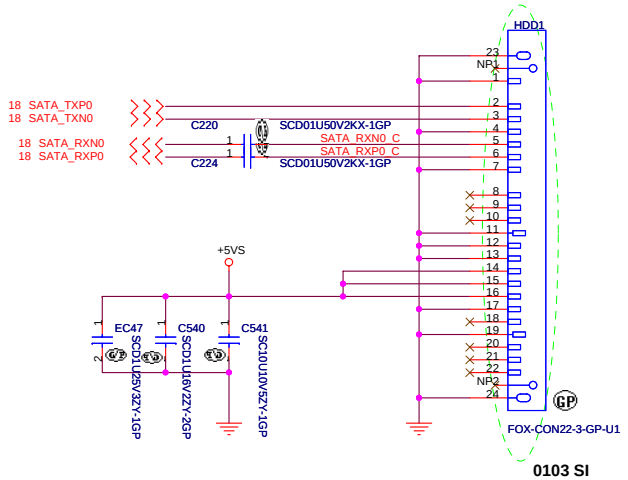




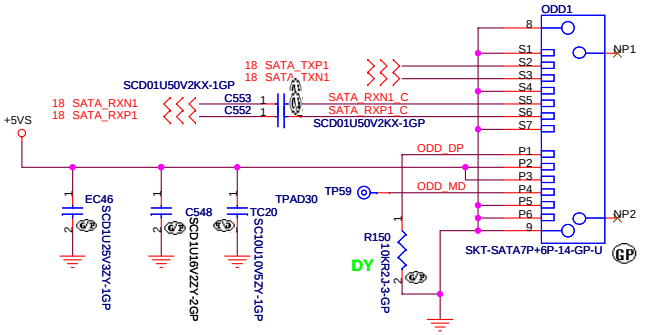


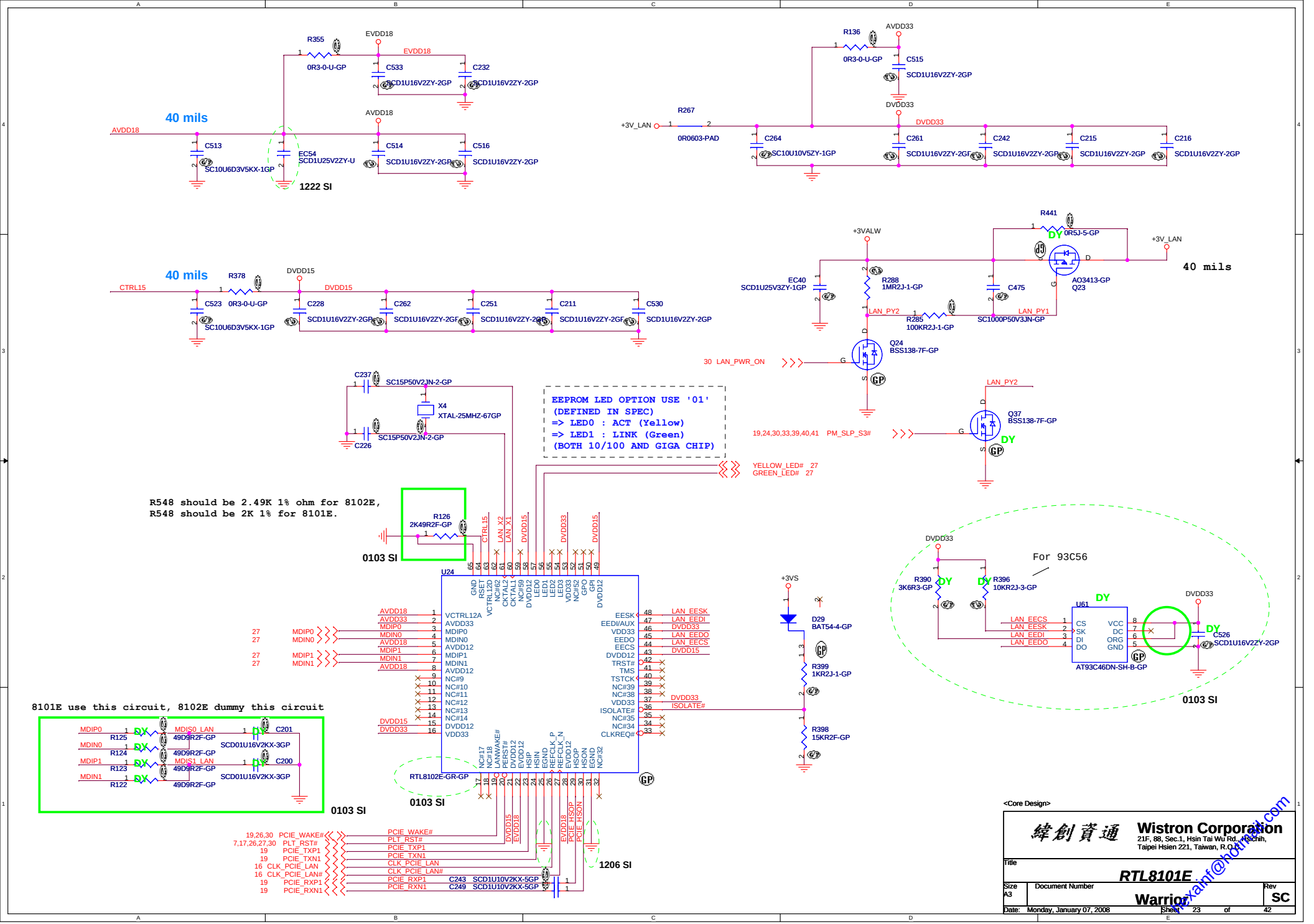


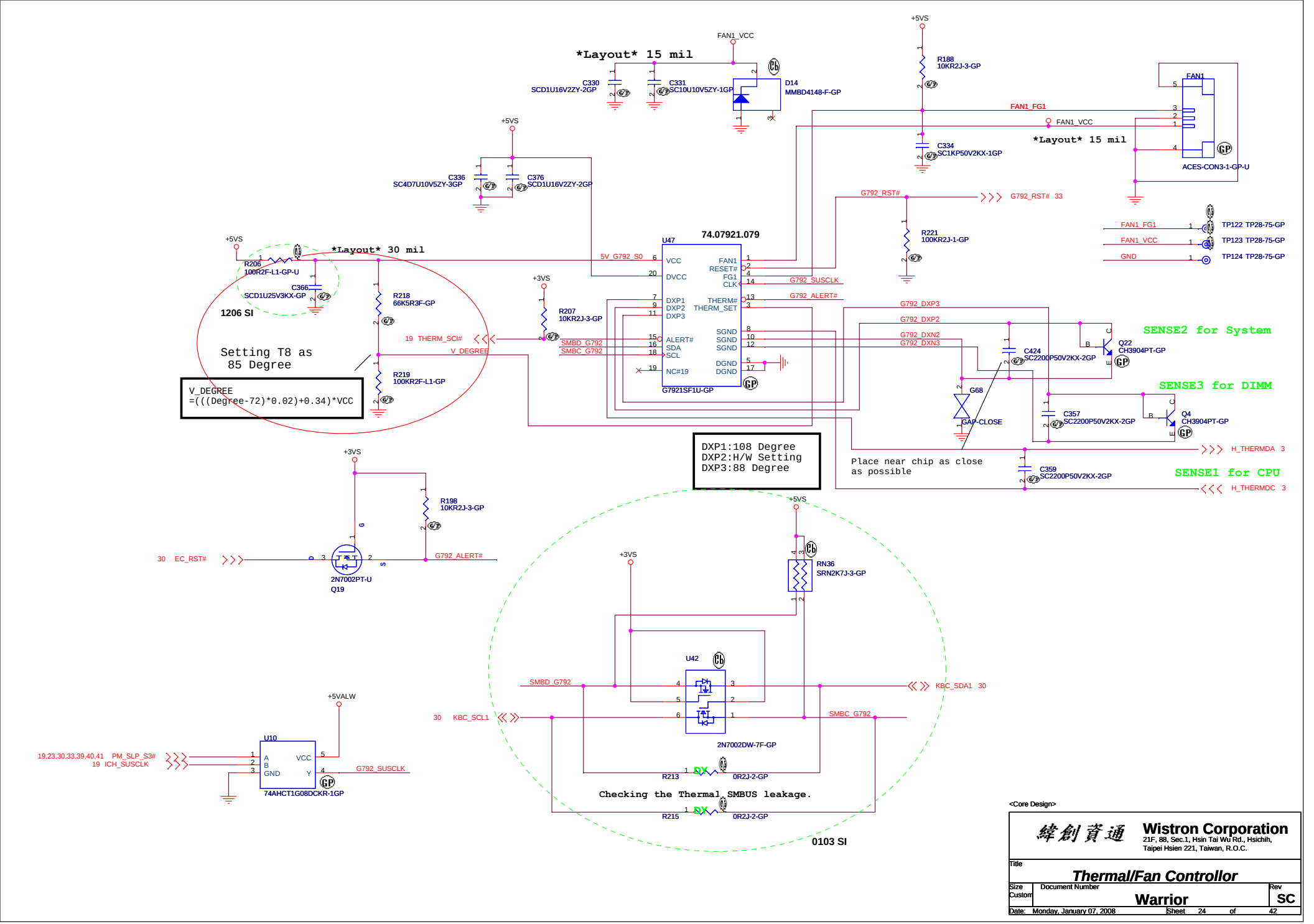
SATA HD Connector

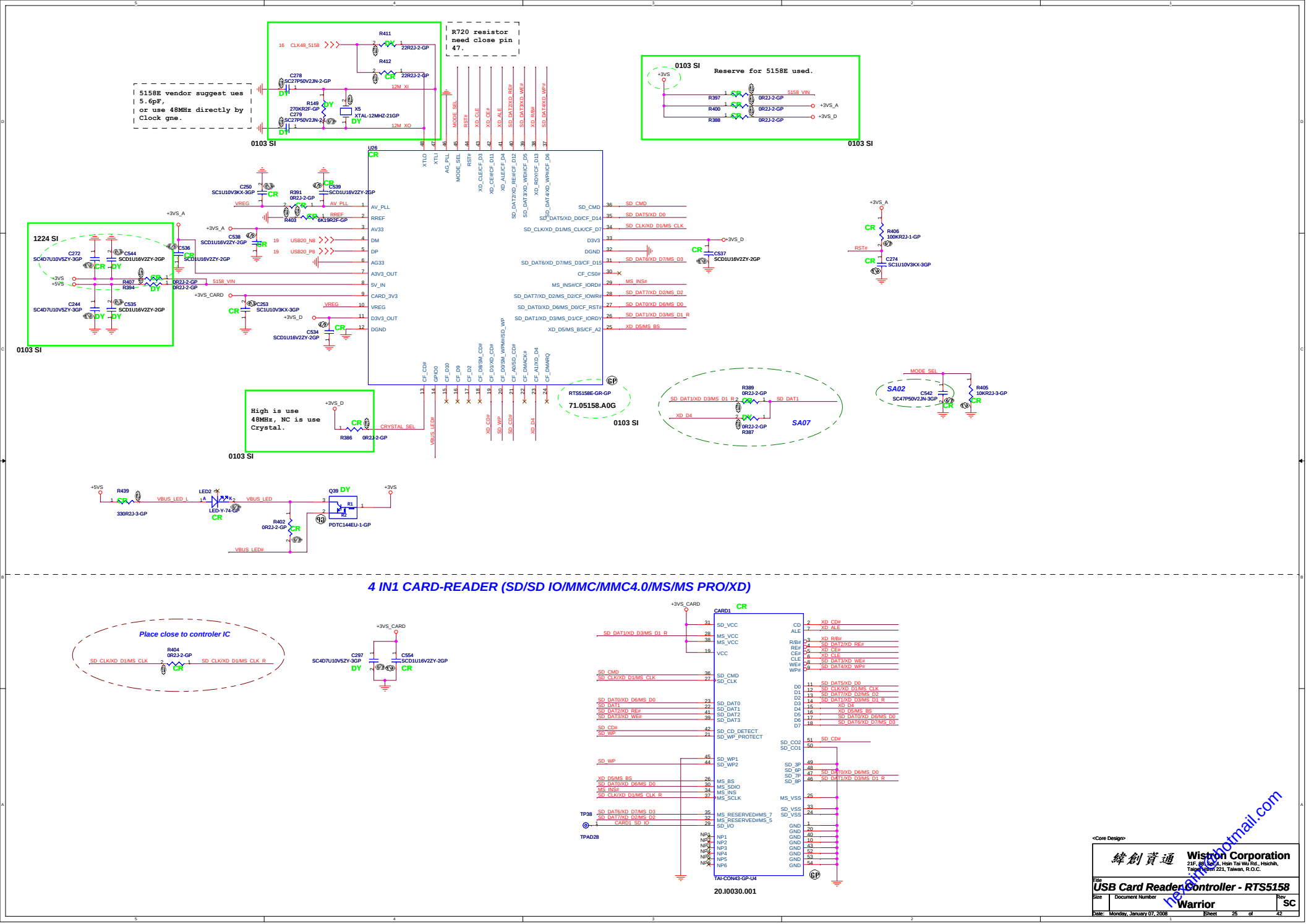


ODD Connector

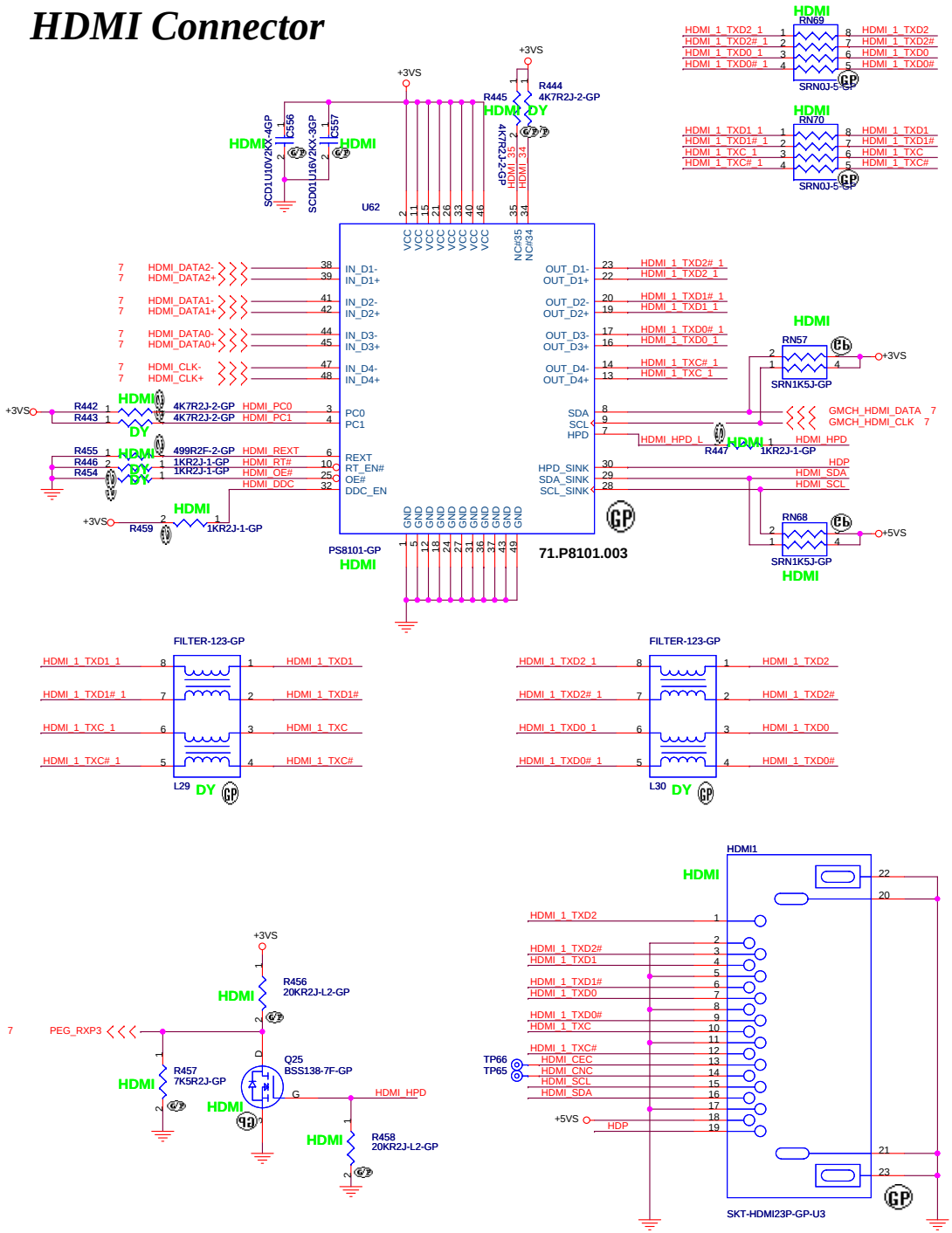




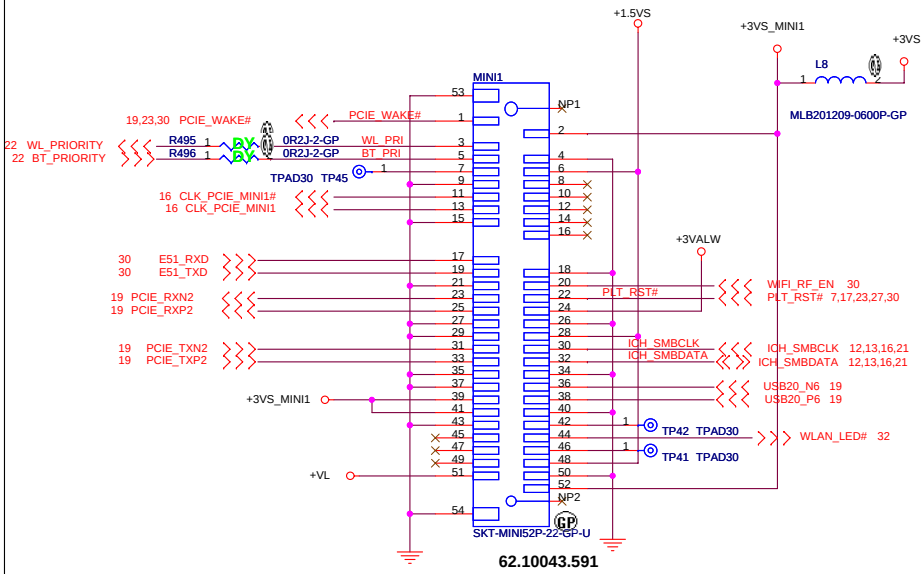


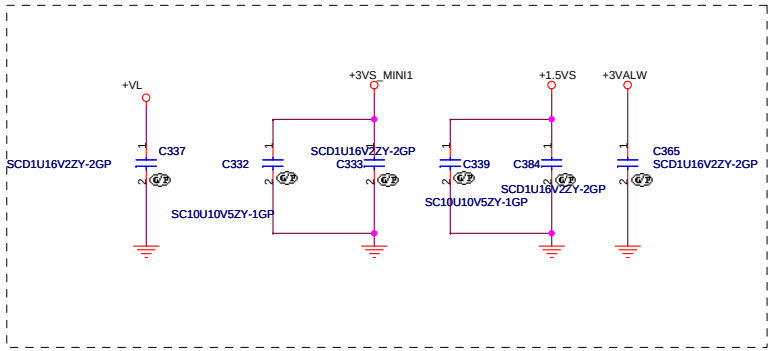


HDMI Connector



Mini Card Connector1(802.11a/b/g)





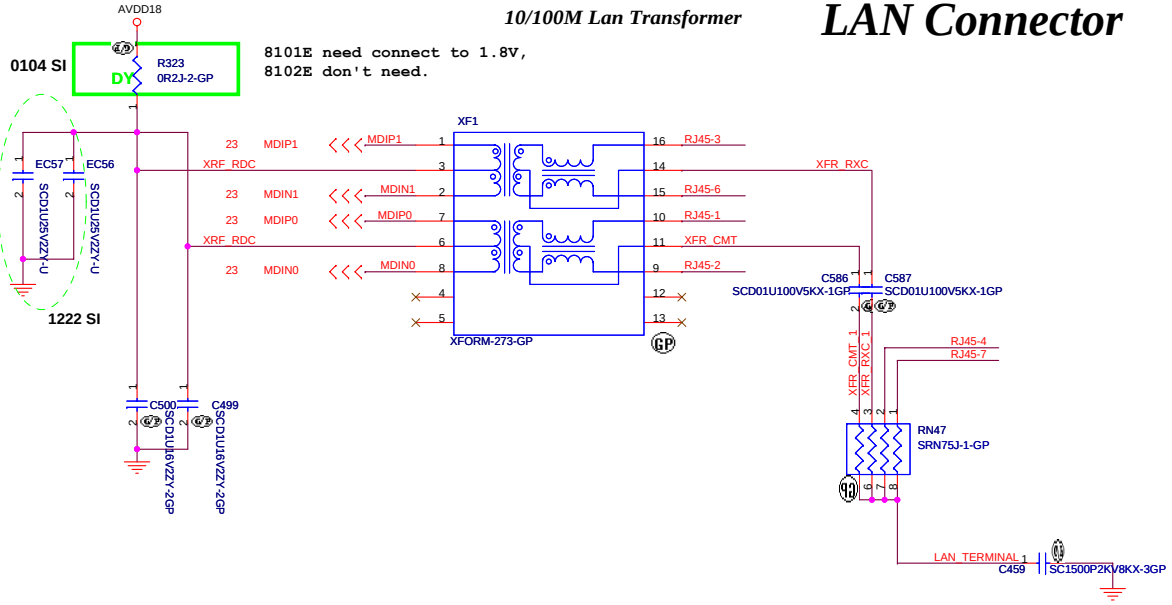
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MINI CARD/HDMI CONN .***
Size A3 / Document Number	**Warrior** / Rev **SC**
Date: Monday, January 07, 2008	Sheet 26 of 42

LAN Connector

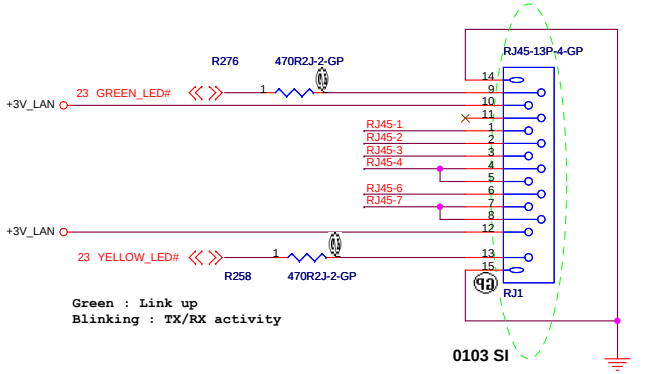
10/100M Lan Transformer

8101E need connect to 1.8V,
8102E don't need.



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

PIN A1 : GREEN
PIN A3 : ORANGE
PIN B2 : YELLOW



Remark:
Add trace width to 20mils
for RJ1 pin4, 5 and pin 7, 8.

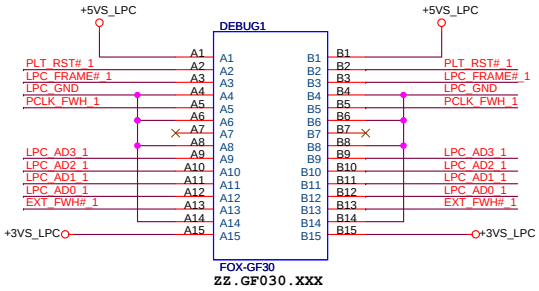
Golden Finger for Debug Board

TOP VIEW (A)

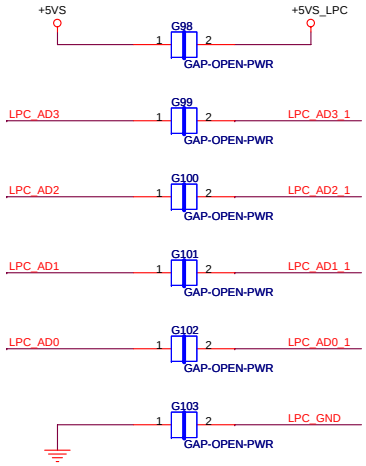
A15	(B1)
A14	(B2)
:	:
:	:
A2	(B14)
A1	(B15)

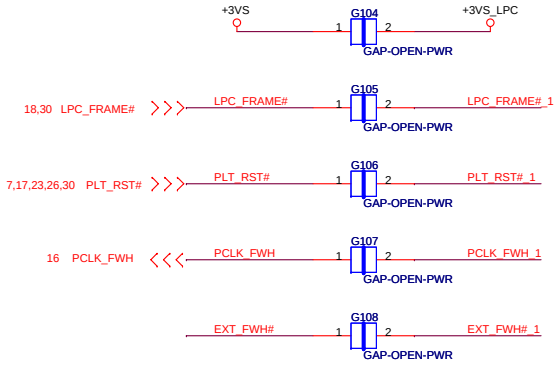
BOTTOM VIEW (B)

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

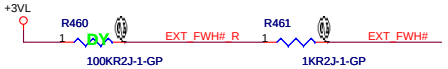


Please put near board edge.





LPC_AD[0..3] 18,30



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Title: **LAN CONN/Debug**

Size	Document Number	Rev
A3	Warrior	SC

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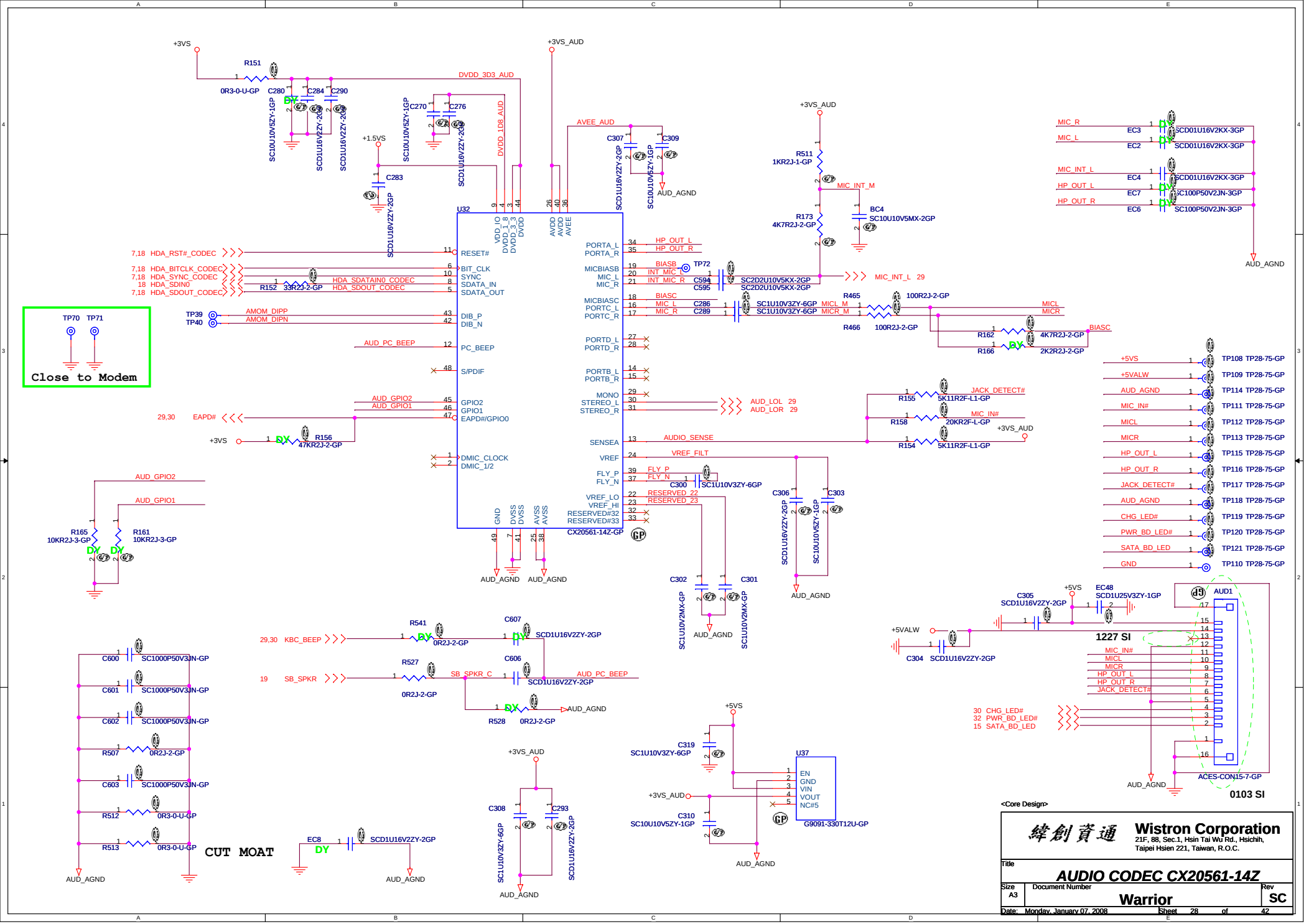
CLOSE TO TRANSFORMER



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<core_design>
<Core Design>
</core_design>

Title: **AUDIO CODEC CX20561-14Z**

Size	Document Number	Rev
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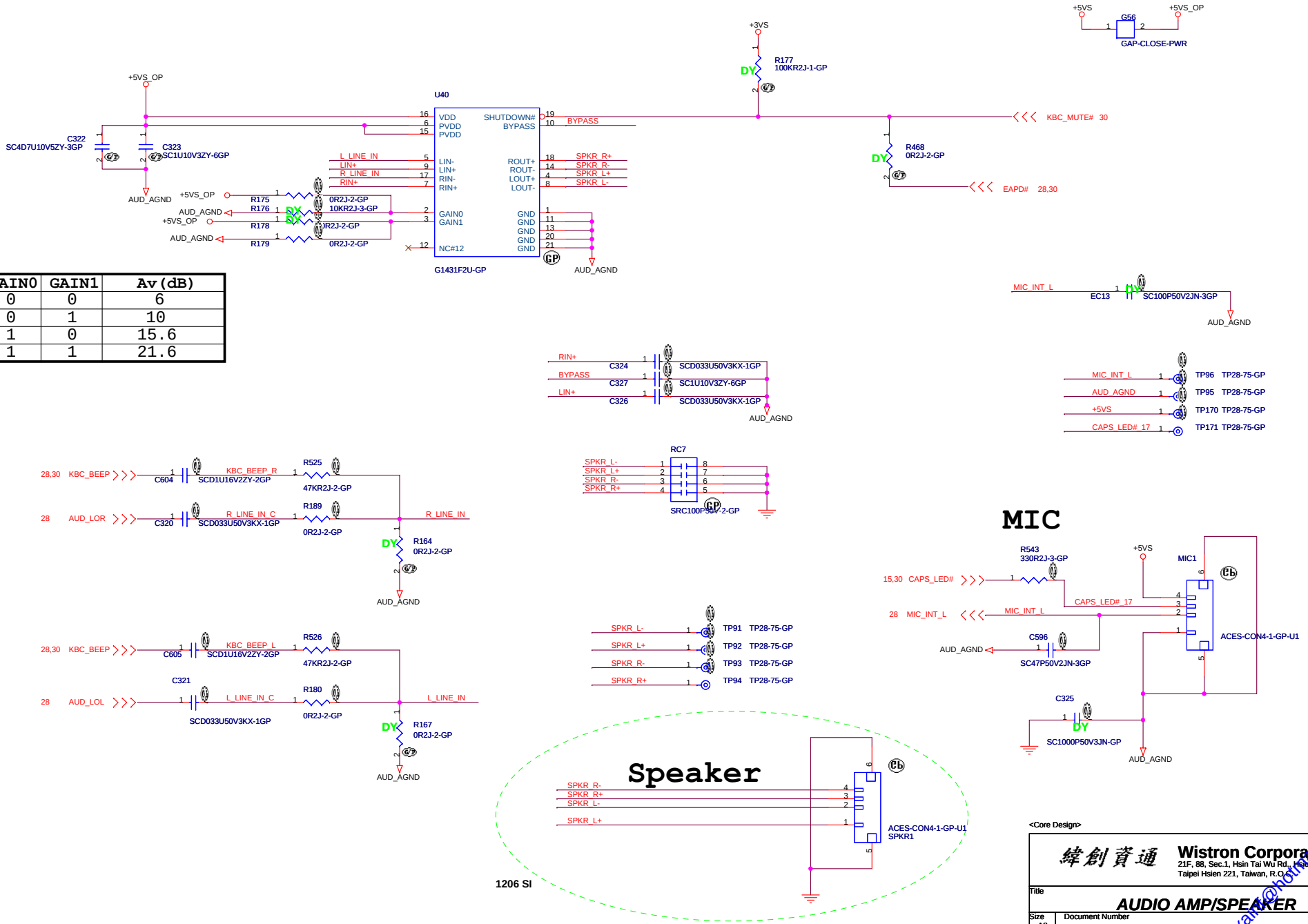
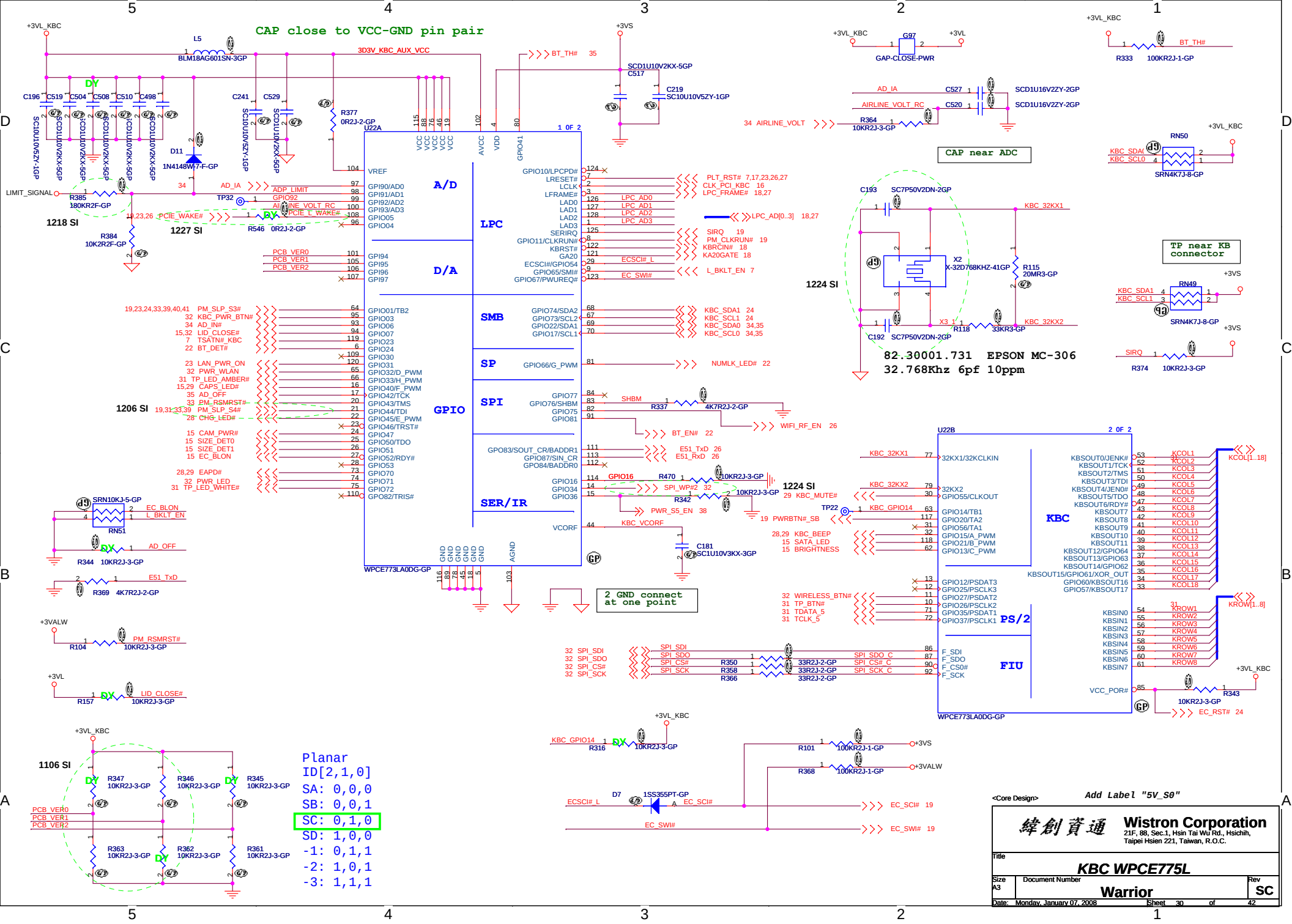
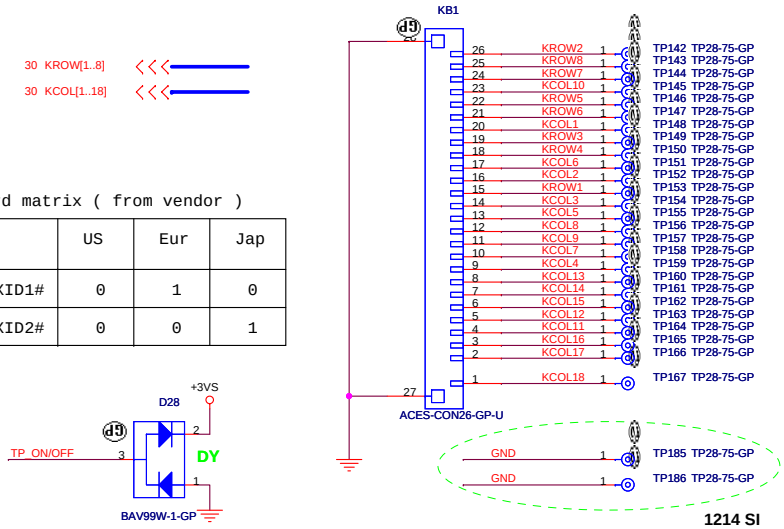


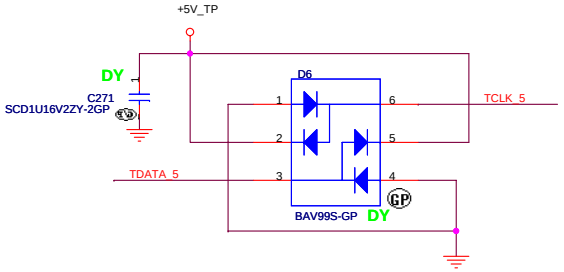


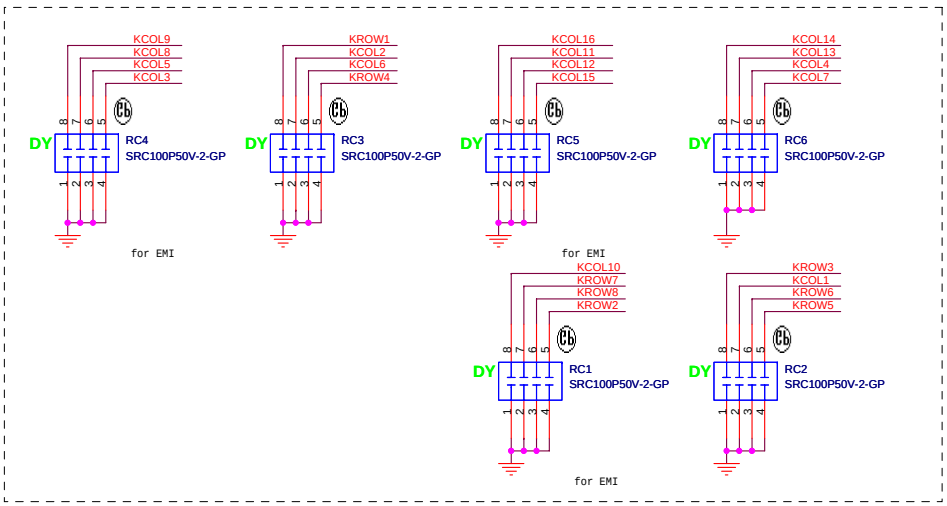
Internal KeyBoard Connector



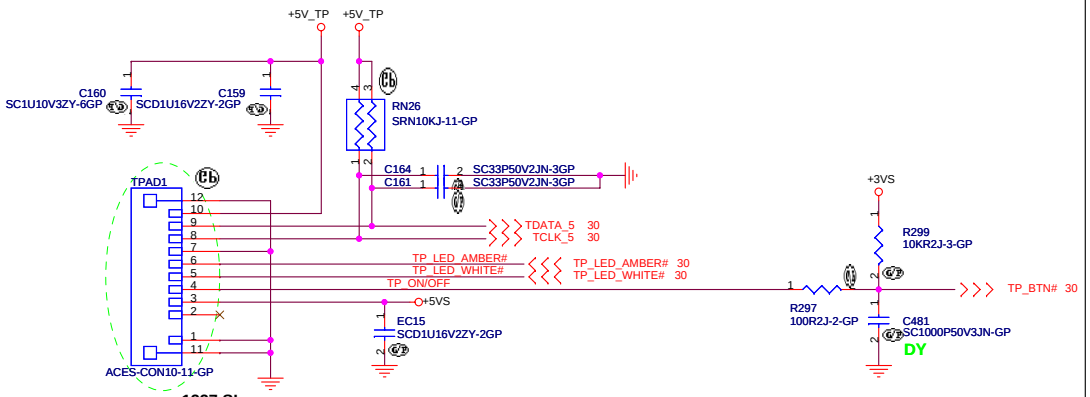
Keyboard matrix (from vendor)

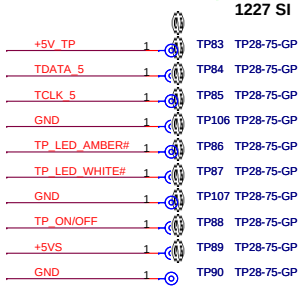
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



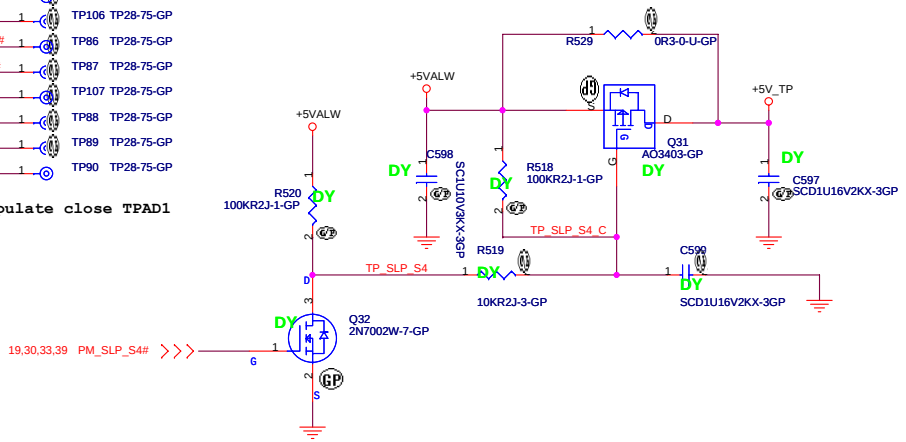


TouchPad Connector





Please populate close TPAD1



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Title: KeyBoard-CONN

Size: A3 | Document Number: Warrior | Rev: SC

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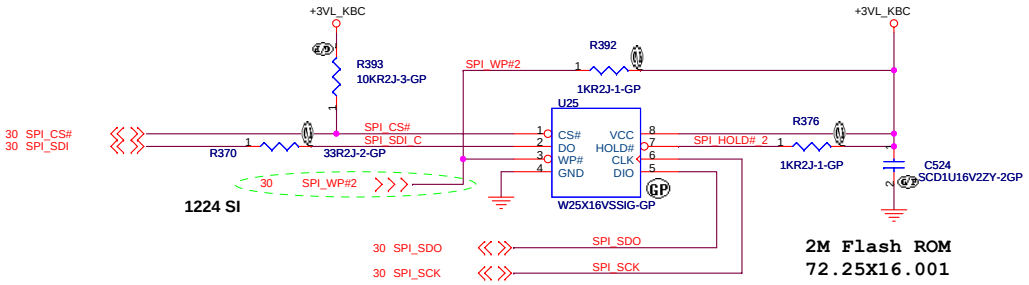

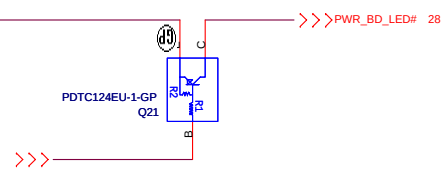

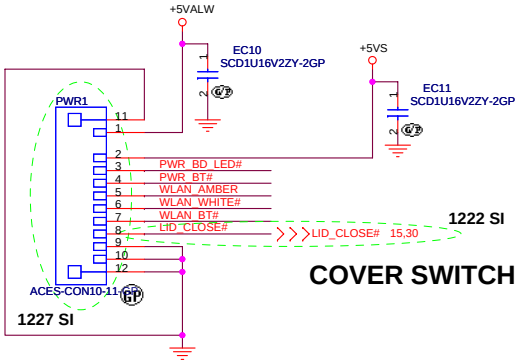

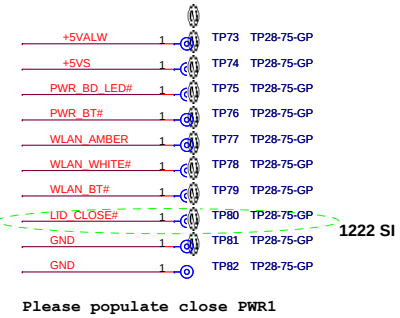

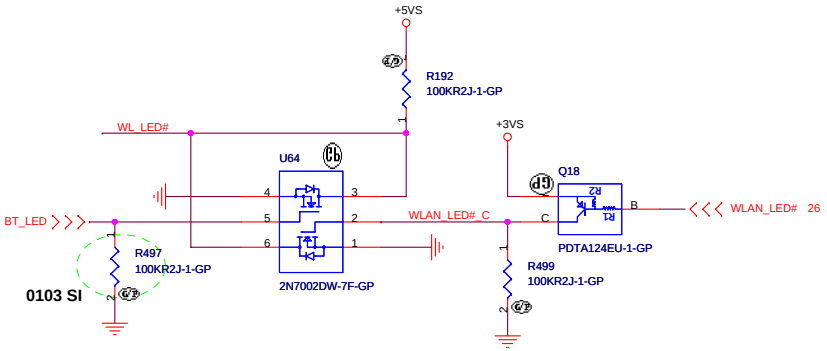

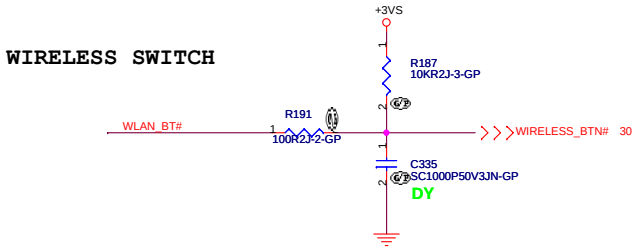

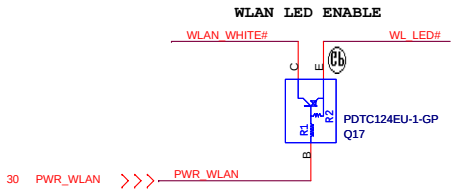

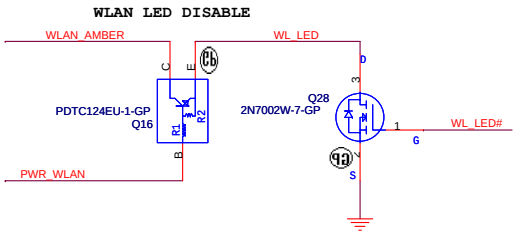

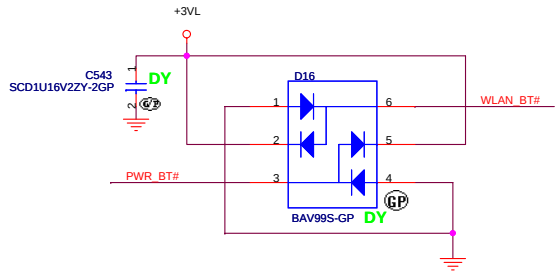

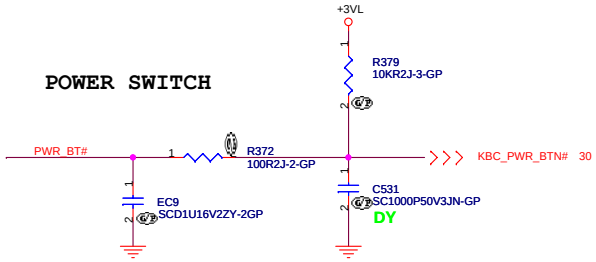

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Title: FWH and CONN.

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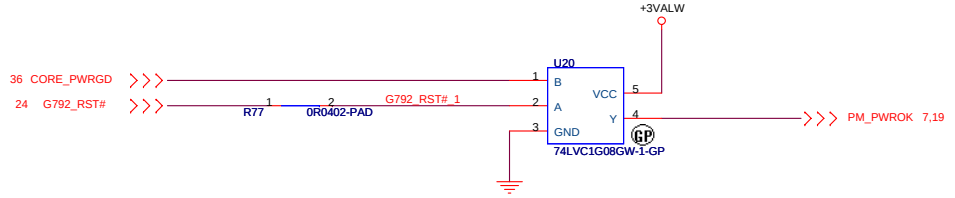
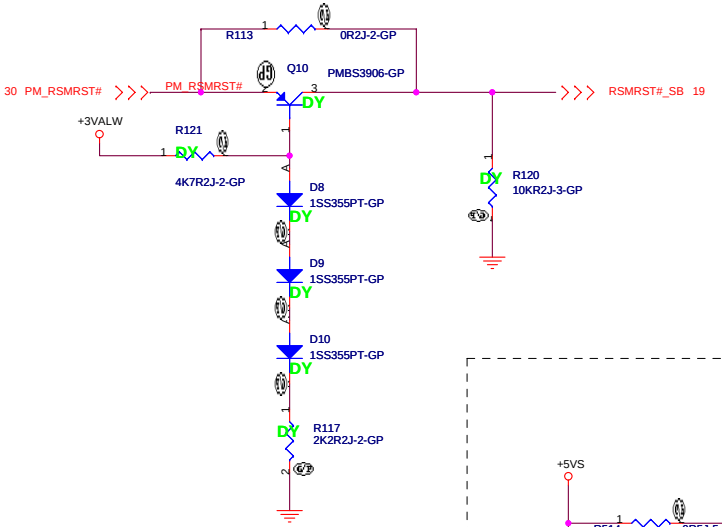
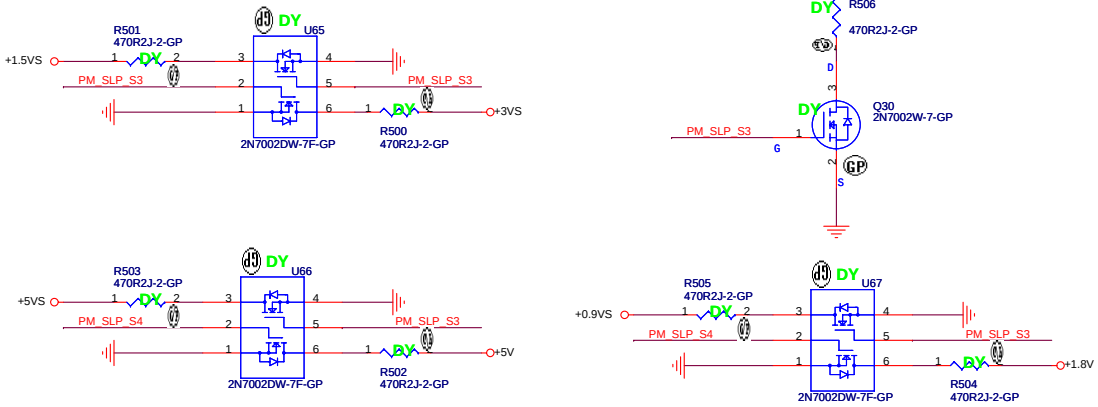
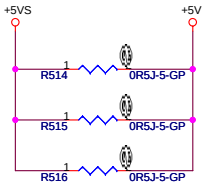




Discharge Circuit



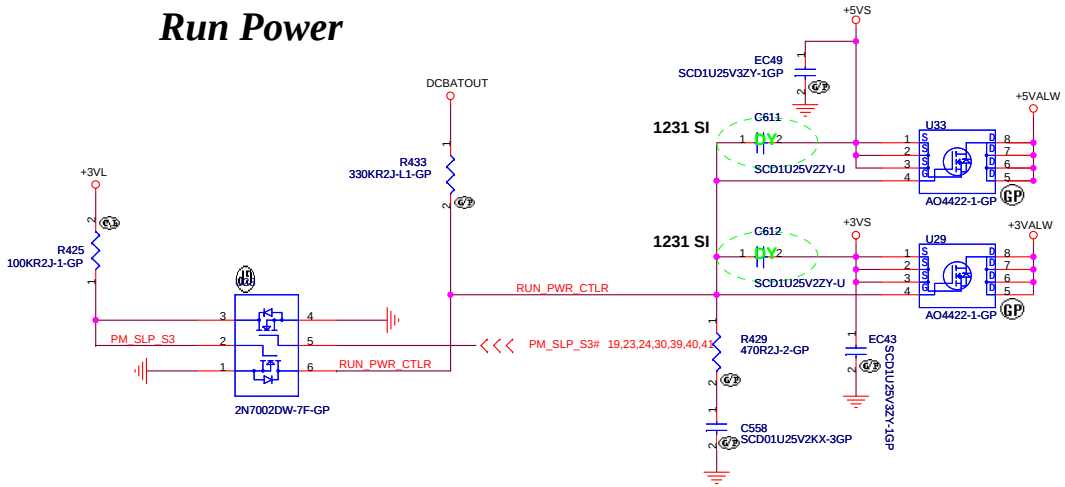


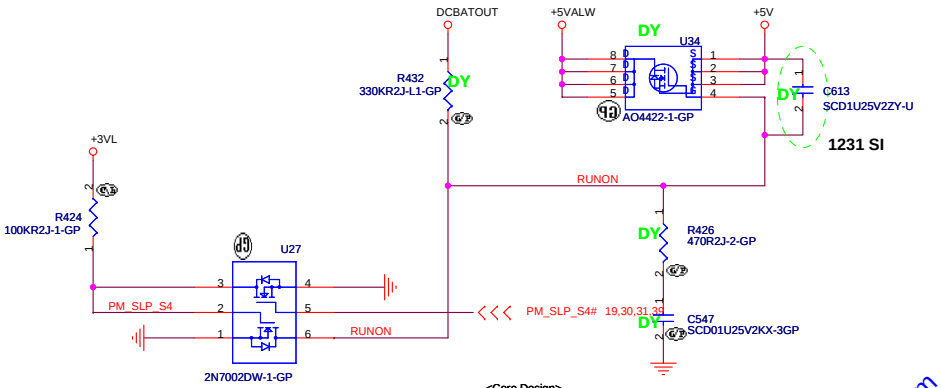
Populate close U34

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer

+5VALW to +5V Transfer

Run Power





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Title: PWRPLANE

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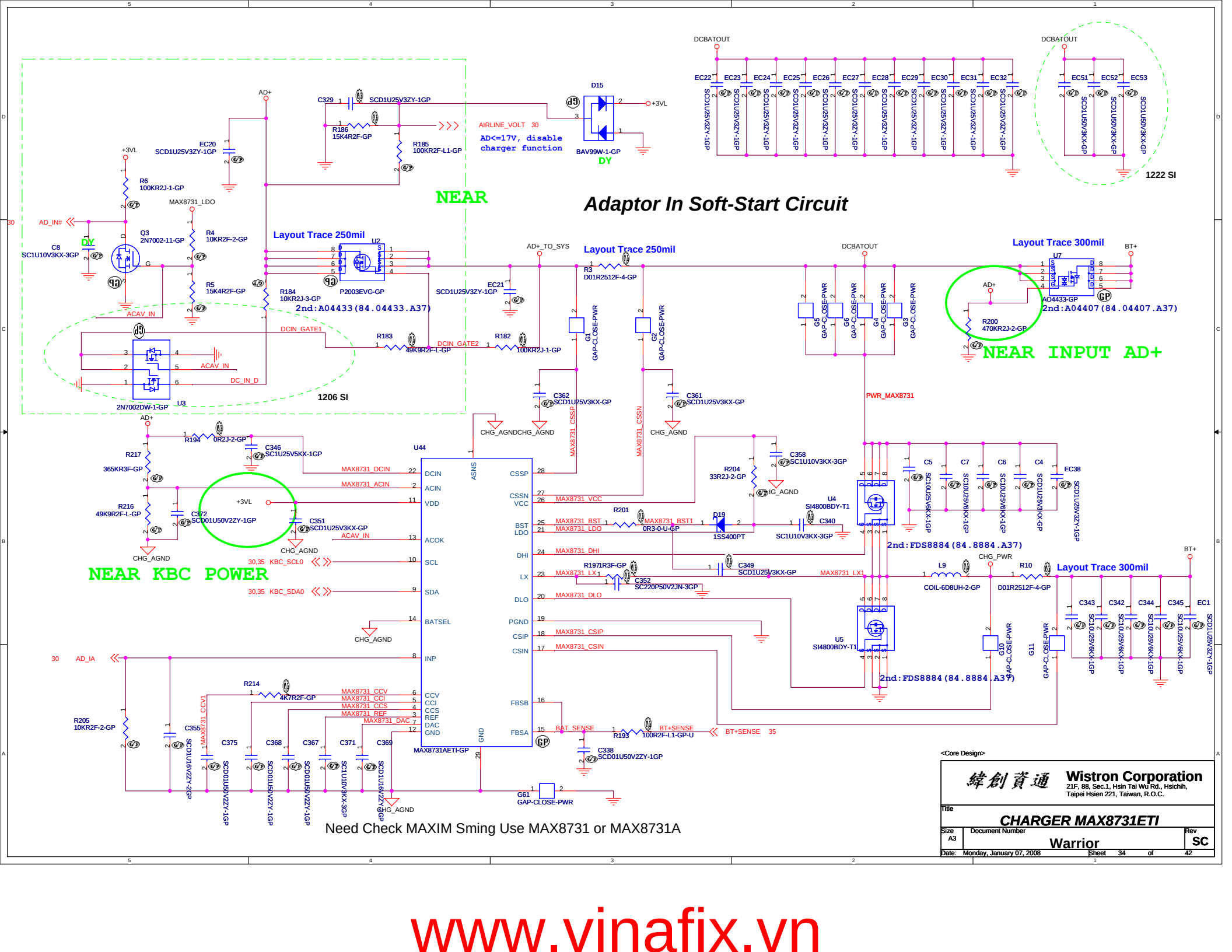

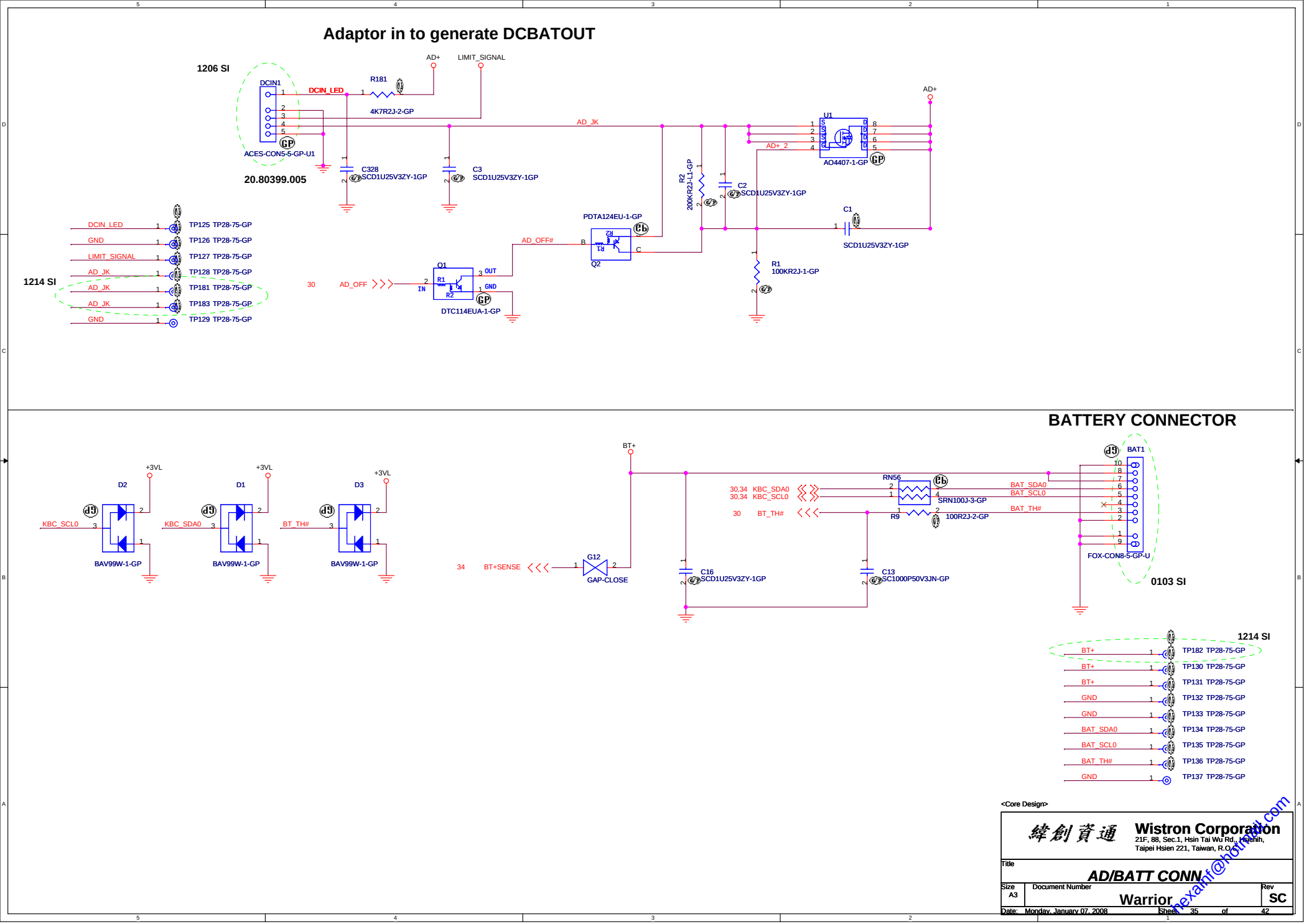

<Core Design>

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Title: AD/BATT CONN

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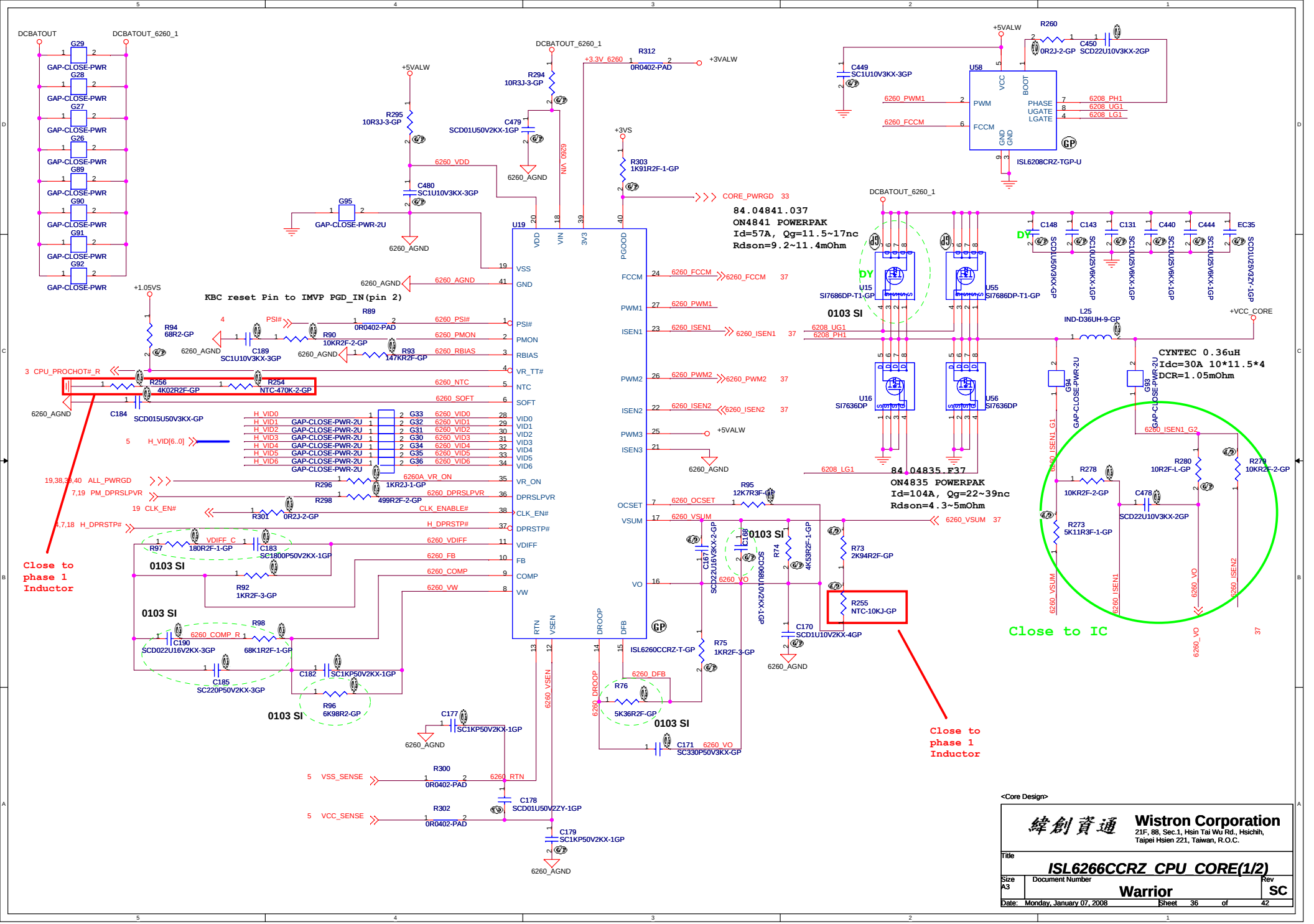
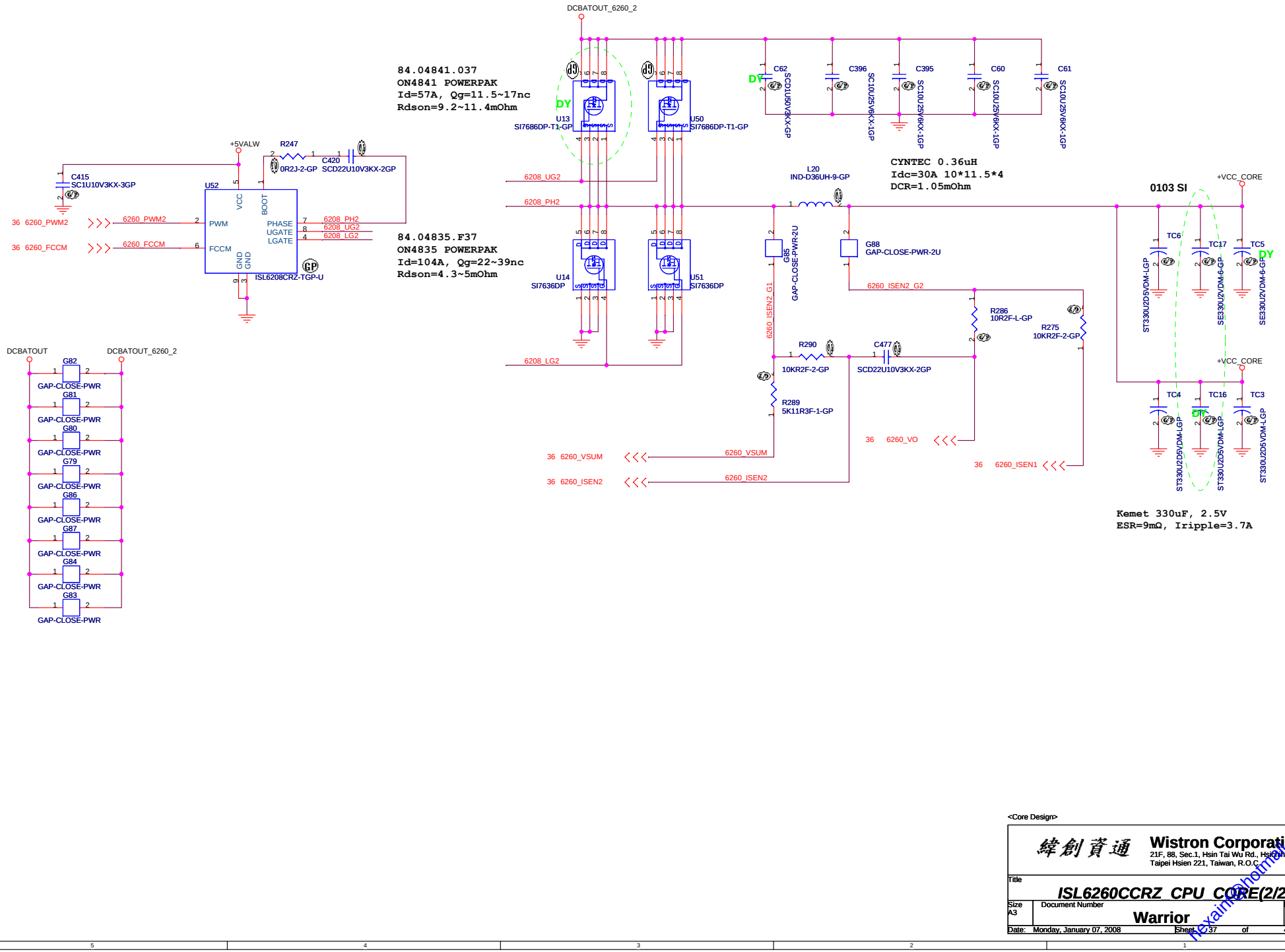
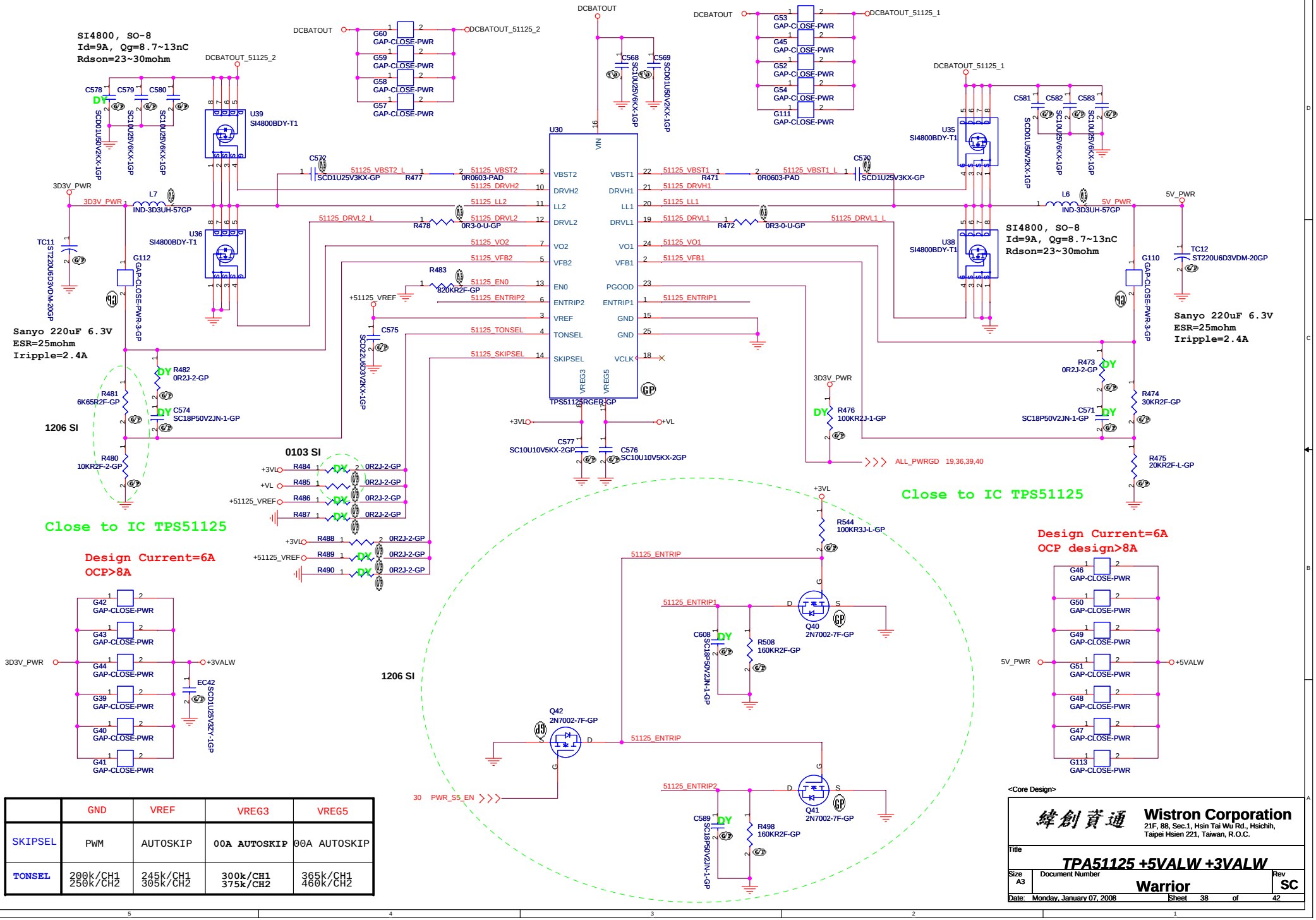
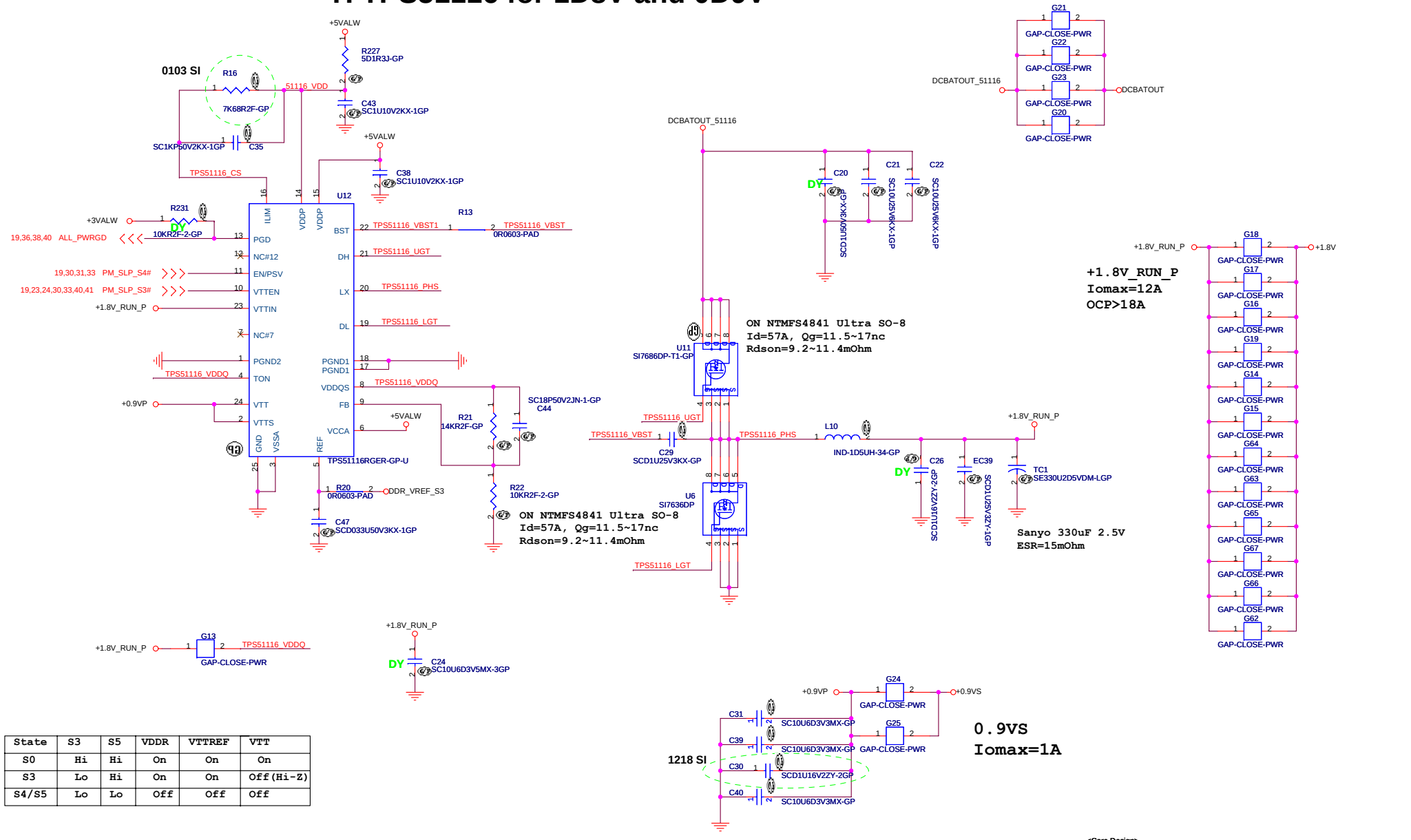






	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	AUTOSKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: Warrior | Rev: SC

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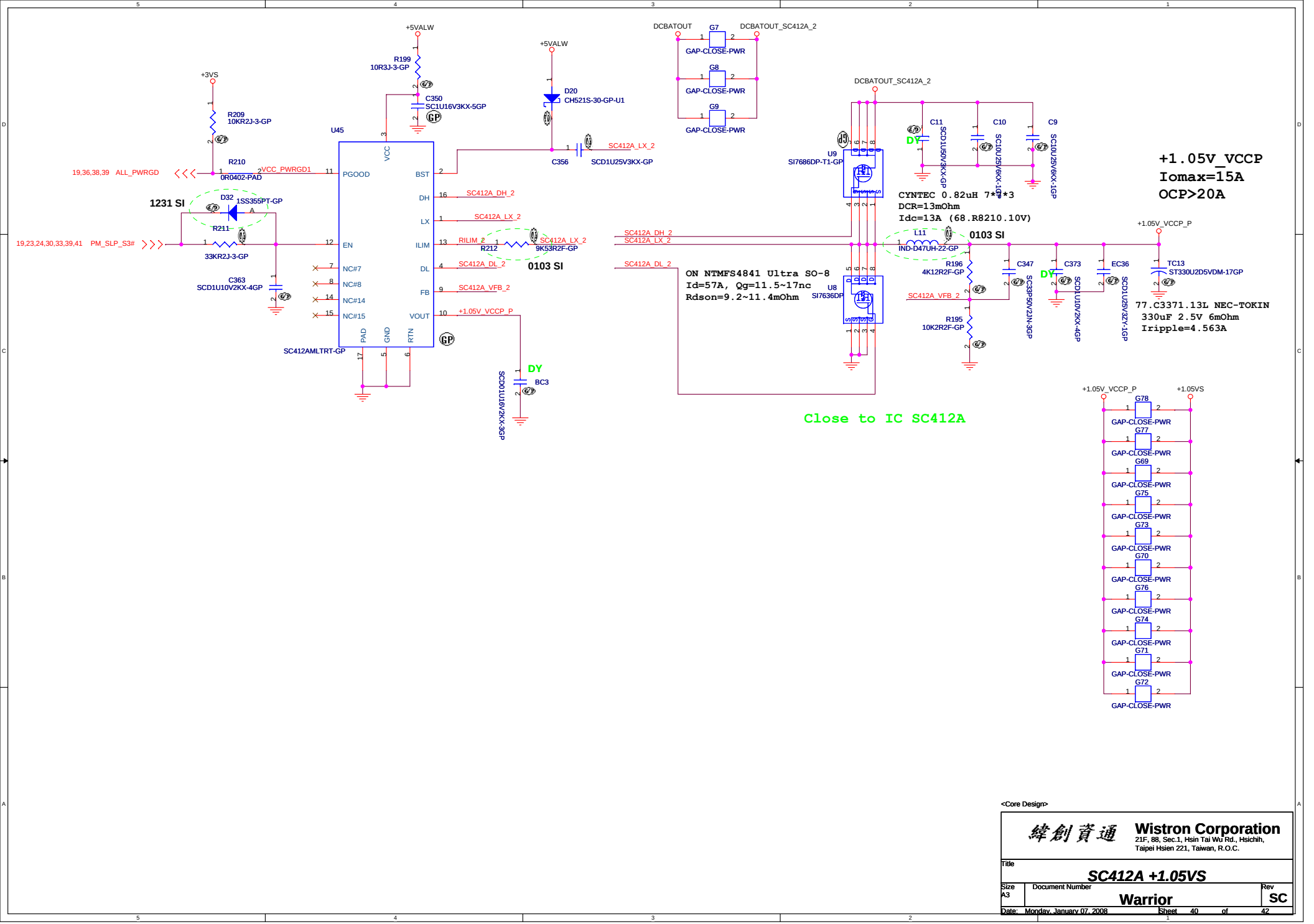

<Core Design>

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Size	Document Number	Rev
A3	**Warrior**	SC

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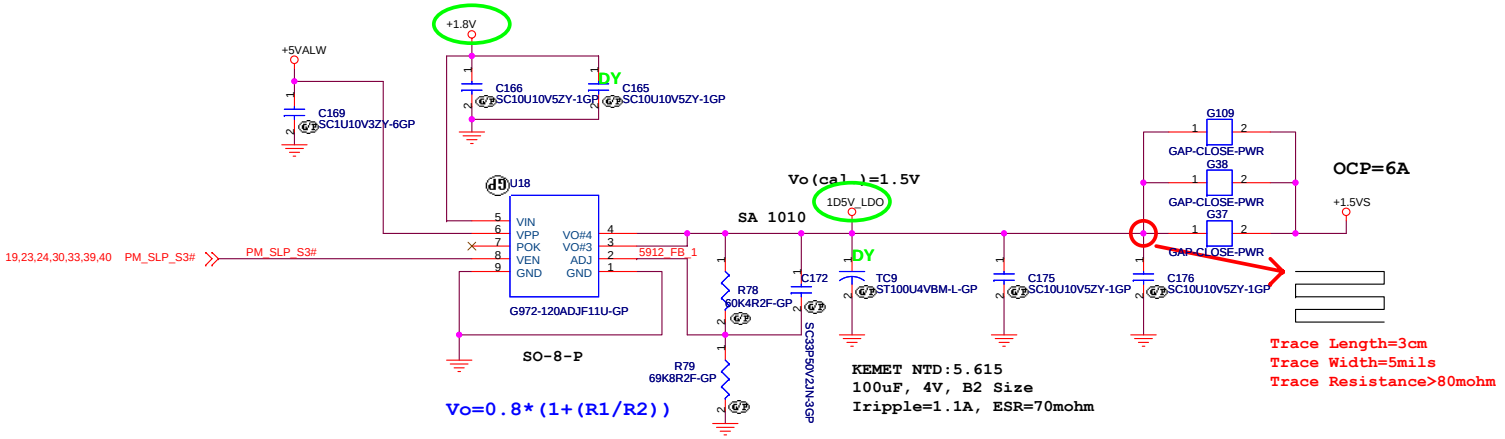

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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Size	Document Number	Rev
A3	Warrior	SC

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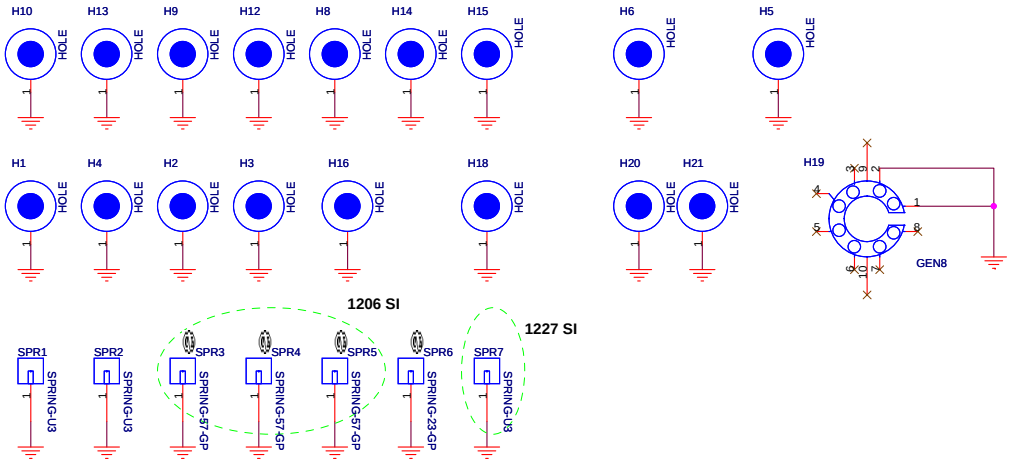

SPR1-2: 34.40U07.001
SPR3-5: 34.42T14.002
SPR6 : 34.39S07.003
SPR7 : 34.40U07.001

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MISC***

Size: A3 | Document Number: **Warrior** | Rev: **SC**

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