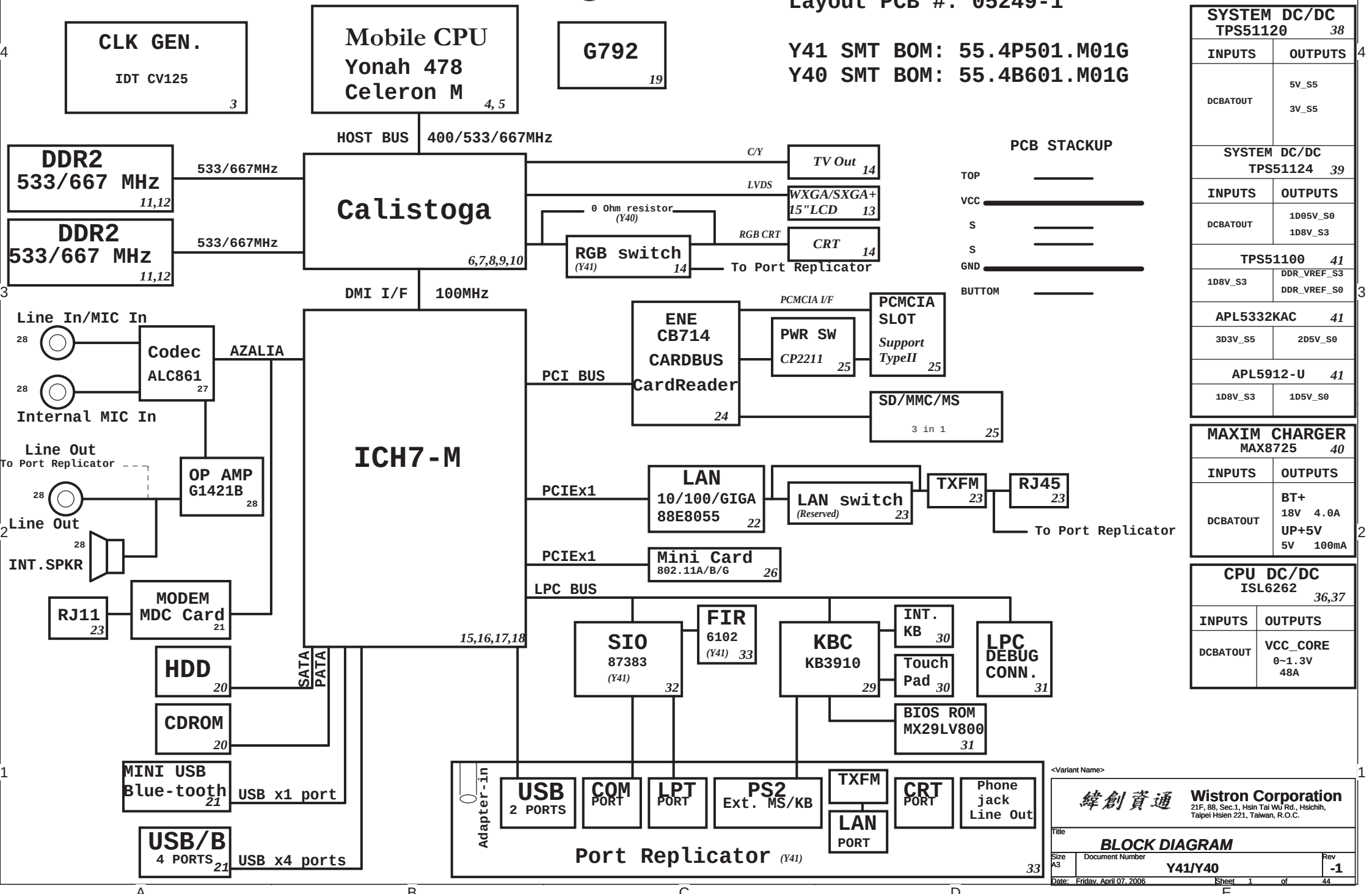
Y41/Y40 Block Diagram

Project code: 91.4P501.001
PCB P/N : 48.4P501.011
Layout PCB #: 05249-1

Y41 SMT BOM: 55.4P501.M01G
Y40 SMT BOM: 55.4B601.M01G



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BUTTOM	

SYSTEM DC/DC TPS51120 *38*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC TPS51124 *39*

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 *41*

1D8V_S3	DDR_VREF_S3 DDR_VREF_S0

APL5332KAC *41*

3D3V_S5	2D5V_S0

APL5912-U *41*

1D8V_S3	1D5V_S0

MAXIM CHARGER MAX8725 *40*

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 *36,37*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLOCK DIAGRAM***

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Friday, April 07, 2006 | Sheet 1 of 44

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 24

	IDSEL	INT -> PIRQ	REQ/GNT
CB714	22	A->G, B->E,	0

Device SSID/SVID

Device	SSID	SVID
LAN 88E8055	10C1	1734
Codec ALC861	10C1	1734

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Variant Name>

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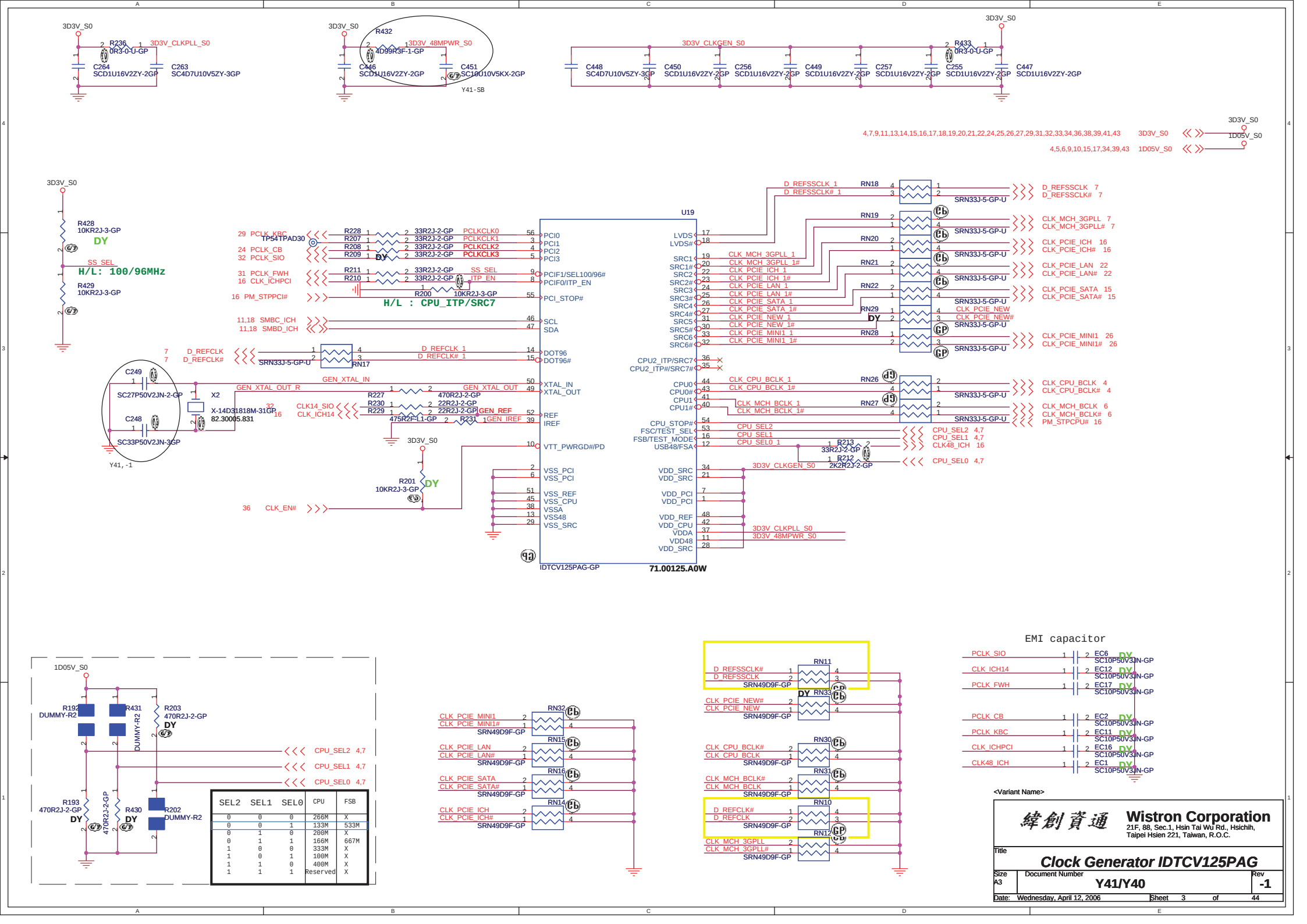
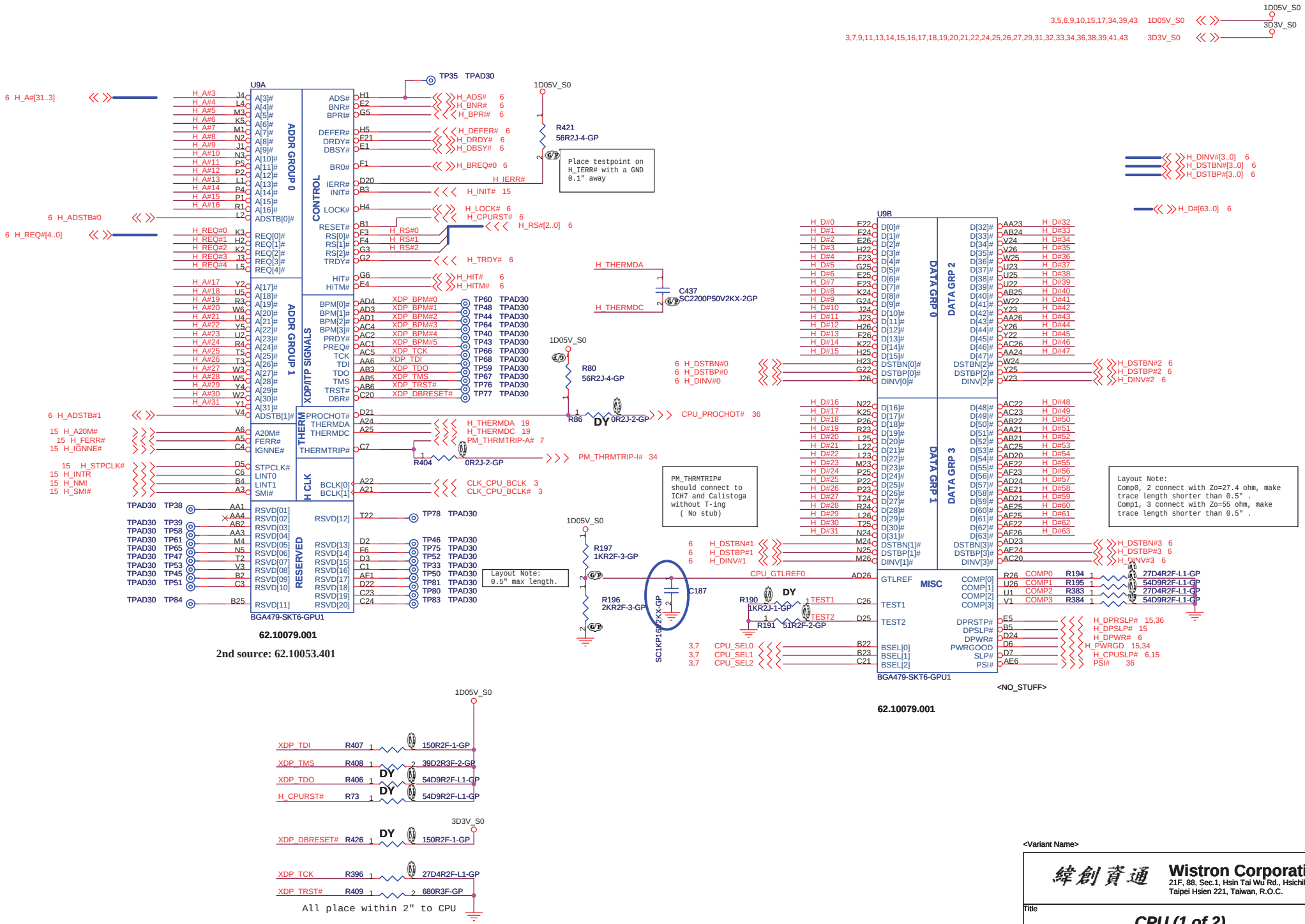
Title: Reference

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Friday, April 07, 2006 | Sheet 2 of 44


3D3V_S0
R236 0R3-0-U-GP
3D3V_CLKPLL_S0
C264 SCD1U16V2ZY-2GP
C263 SC4D7U10V5ZY-3GP
R432 4D99R3F-1-GP
3D3V_48MPWR_S0
C446 SCD1U16V2ZY-2GP
C451 SC10U10V5KX-2GP
Y41-SB
3D3V_CLKGEN_S0
C448 SC4D7U10V5ZY-3GP
C450 SCD1U16V2ZY-2GP
C256 SCD1U16V2ZY-2GP
C449 SCD1U16V2ZY-2GP
C257 SCD1U16V2ZY-2GP
R433 0R3-0-U-GP
C255 SCD1U16V2ZY-2GP
C447 SCD1U16V2ZY-2GP
4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43
3D3V_S0
1D05V_S0
4,5,6,9,10,15,17,34,39,43
R428 10KR2J-3-GP
DY
SS_SEL
H/L: 100/96MHz
R429 10KR2J-3-GP
29 PCLK_KBC
TP54TPAD30
24 PCLK_CB
32 PCLK_SIO
31 PCLK_FWH
16 CLK_ICHPCI
16 PM_STPPCI#
R228 R207 R208 R209 33R2J-2-GP
PCLKCLK0
PCLKCLK1
PCLKCLK2
PCLKCLK3
R211 R210 33R2J-2-GP
SS_SEL
ITP_EN
R200 10KR2J-3-GP
H/L : CPU_ITP/SRC7
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
11,18 SMBC_ICH
11,18 SMBD_ICH
SCL
SDA
7 D_REFCLK
7 D_REFCLK#
SRN33J-5-GP-U
RN17
D_REFCLK_1
D_REFCLK#_1
DOT96
DOT96#
C249 SC27P50V2JN-2-GP
C248 SC33P50V2JN-3GP
X2
X-14D31818M-31GP
82.30005.831
Y41,-1
GEN_XTAL_OUT_R
GEN_XTAL_IN
GEN_XTAL_OUT
R227 470R2J-2-GP
R230 R229 22R2J-2-GP
475R2F-L1-GP
R231
GEN_IREF
32 CLK14_SIO
16 CLK_ICH14
GEN_REF
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#/PD
R201 10KR2J-3-GP
36 CLK_EN#
VSS_PCI
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
U19
IDTCV125PAG-GP
71.00125.A0W
LVDS
LVDS#
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
VDD_SRC
VDD_SRC
VDD_PCI
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
VDD_SRC
D_REFSSCLK_1
D_REFSSCLK#_1
RN18
SRN33J-5-GP-U
D_REFSSCLK 7
D_REFSSCLK# 7
RN19
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL#_1
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
RN20
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
CLK_PCIE_ICH 16
CLK_PCIE_ICH# 16
RN21
CLK_PCIE_LAN_1
CLK_PCIE_LAN_1#
CLK_PCIE_LAN 22
CLK_PCIE_LAN# 22
RN22
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
CLK_PCIE_SATA 15
CLK_PCIE_SATA# 15
RN29
CLK_PCIE_NEW_1
CLK_PCIE_NEW_1#
CLK_PCIE_NEW
CLK_PCIE_NEW#
RN28
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_PCIE_MINI1 26
CLK_PCIE_MINI1# 26
RN26
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
RN27
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 16
CPU_SEL2
CPU_SEL1
CPU_SEL0_1
R213 33R2J-2-GP
R212 2K2R2J-2-GP
CPU_SEL2 4,7
CPU_SEL1 4,7
CLK48_ICH 16
CPU_SEL0 4,7
3D3V_CLKGEN_S0
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
1D05V_S0
R193 DUMMY-R2
R431 DUMMY-R2
R203 470R2J-2-GP
DY
CPU_SEL2 4,7
CPU_SEL1 4,7
CPU_SEL0 4,7
R193 470R2J-2-GP
R430 470R2J-2-GP
R202 DUMMY-R2
SEL2 SEL1 SEL0 CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
RN32
SRN49D9F-GP
CLK_PCIE_LAN
CLK_PCIE_LAN#
RN15
CLK_PCIE_SATA
CLK_PCIE_SATA#
RN16
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN14
D_REFSSCLK#
D_REFSSCLK
RN11
CLK_PCIE_NEW#
CLK_PCIE_NEW
RN33
CLK_CPU_BCLK#
CLK_CPU_BCLK
RN30
CLK_MCH_BCLK#
CLK_MCH_BCLK
RN31
D_REFCLK#
D_REFCLK
RN10
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN12
EMI capacitor
PCLK_SIO
EC6 SC10P50V3JN-GP
CLK_ICH14
EC12 SC10P50V3JN-GP
PCLK_FWH
EC17 SC10P50V3JN-GP
PCLK_CB
EC2 SC10P50V3JN-GP
PCLK_KBC
EC11 SC10P50V3JN-GP
CLK_ICHPCI
EC16 SC10P50V3JN-GP
CLK48_ICH
EC1 SC10P50V3JN-GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator IDTCV125PAG
Size A3
Document Number
Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 3 of 44


U9A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
BGA479-SKT6-GPU1
62.10079.001
2nd source: 62.10053.401
U9B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
BGA479-SKT6-GPU1
62.10079.001
<NO_STUFF>
R421 56R2J-4-GP
R80 56R2J-4-GP
R86 0R2J-2-GP
R404 0R2J-2-GP
R197 1KR2F-3-GP
R196 2KR2F-3-GP
C437 SC2200P50V2KX-2GP
C187 SC1KP16V2KX-GP
R190 1KR2J-1-GP
R191 51R2F-2-GP
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)
Layout Note: 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
R407 150R2F-1-GP
R408 39D2R3F-2-GP
R406 54D9R2F-L1-GP
R73 54D9R2F-L1-GP
R426 150R2F-1-GP
R396 27D4R2F-L1-GP
R409 680R3F-GP
All place within 2" to CPU
R194 27D4R2F-L1-GP
R195 54D9R2F-L1-GP
R383 27D4R2F-L1-GP
R384 54D9R2F-L1-GP
DY
1D05V_S0
3D3V_S0
Wistron Corporation
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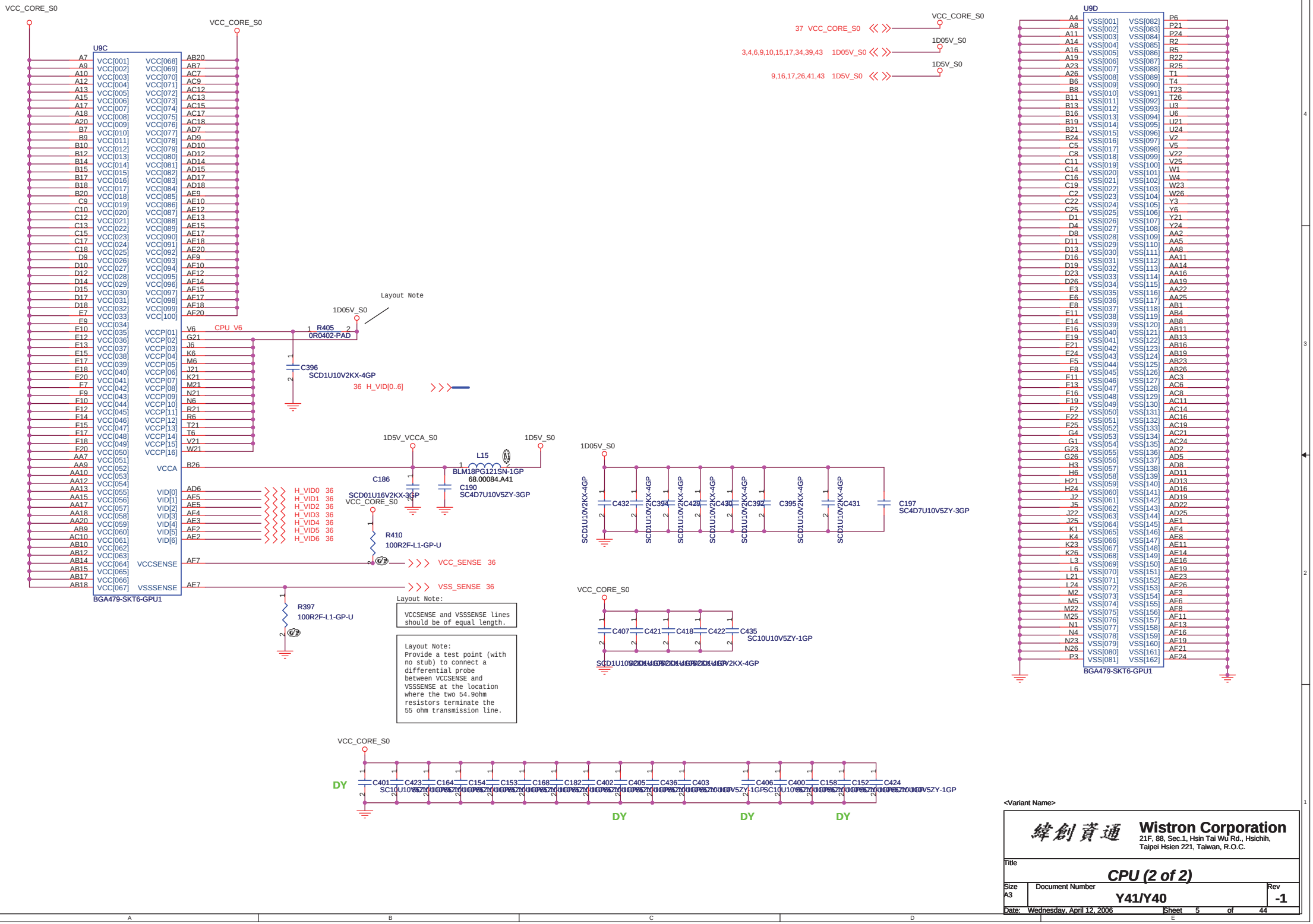
Title
CPU (1 of 2)
Size A3
Document Number Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 4 of 44


VCC_CORE_S0
U9C
BGA479-SKT6-GPU1
CPU_V6
R405
0R0402-PAD
Layout Note
1D05V_S0
C396
SCD1U10V2KX-4GP
36 H_VID[0..6]
1D5V_VCCA_S0
1D5V_S0
L15
BLM18PG121SN-1GP
68.00084.A41
C186
SCD01U16V2KX-3GP
C190
SC4D7U10V5ZY-3GP
H_VID0 36
H_VID1 36
H_VID2 36
H_VID3 36
H_VID4 36
H_VID5 36
H_VID6 36
R410
100R2F-L1-GP-U
VCC_SENSE 36
VSS_SENSE 36
R397
100R2F-L1-GP-U
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
37 VCC_CORE_S0
3,4,6,9,10,15,17,34,39,43 1D05V_S0
9,16,17,26,41,43 1D5V_S0
C432
C394
C429
C430
C392
C395
C431
C197
SC4D7U10V5ZY-3GP
C407
C421
C418
C422
C435
SC10U10V5ZY-1GP
C401
C423
C164
C154
C153
C168
C182
C402
C405
C436
C403
C406
C400
C158
C152
C424
DY
U9D
BGA479-SKT6-GPU1
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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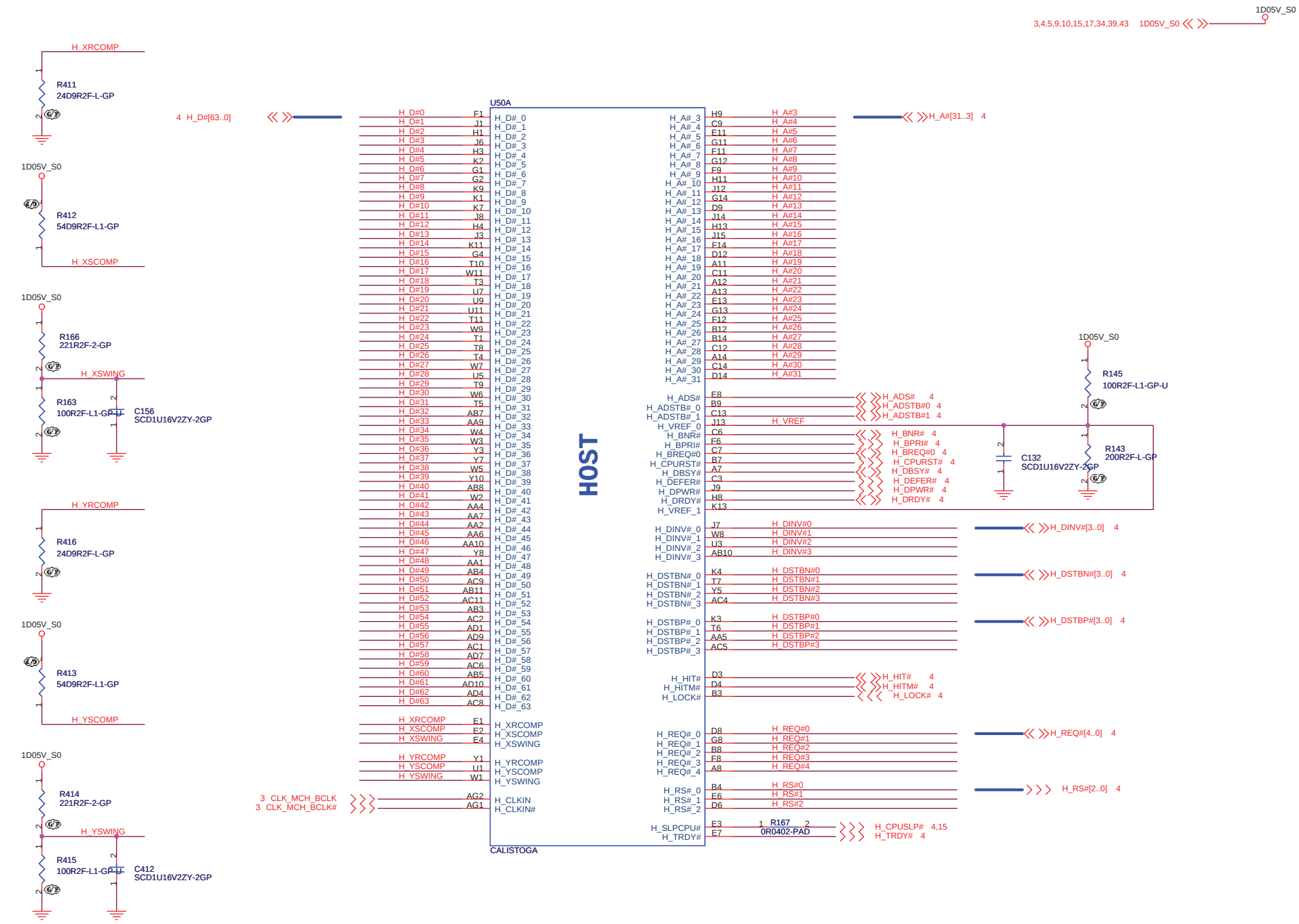
Title
CPU (2 of 2)
Size A3
Document Number
Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 5 of 44



Place them near to the chip (< 0.5")

<Variant Name>

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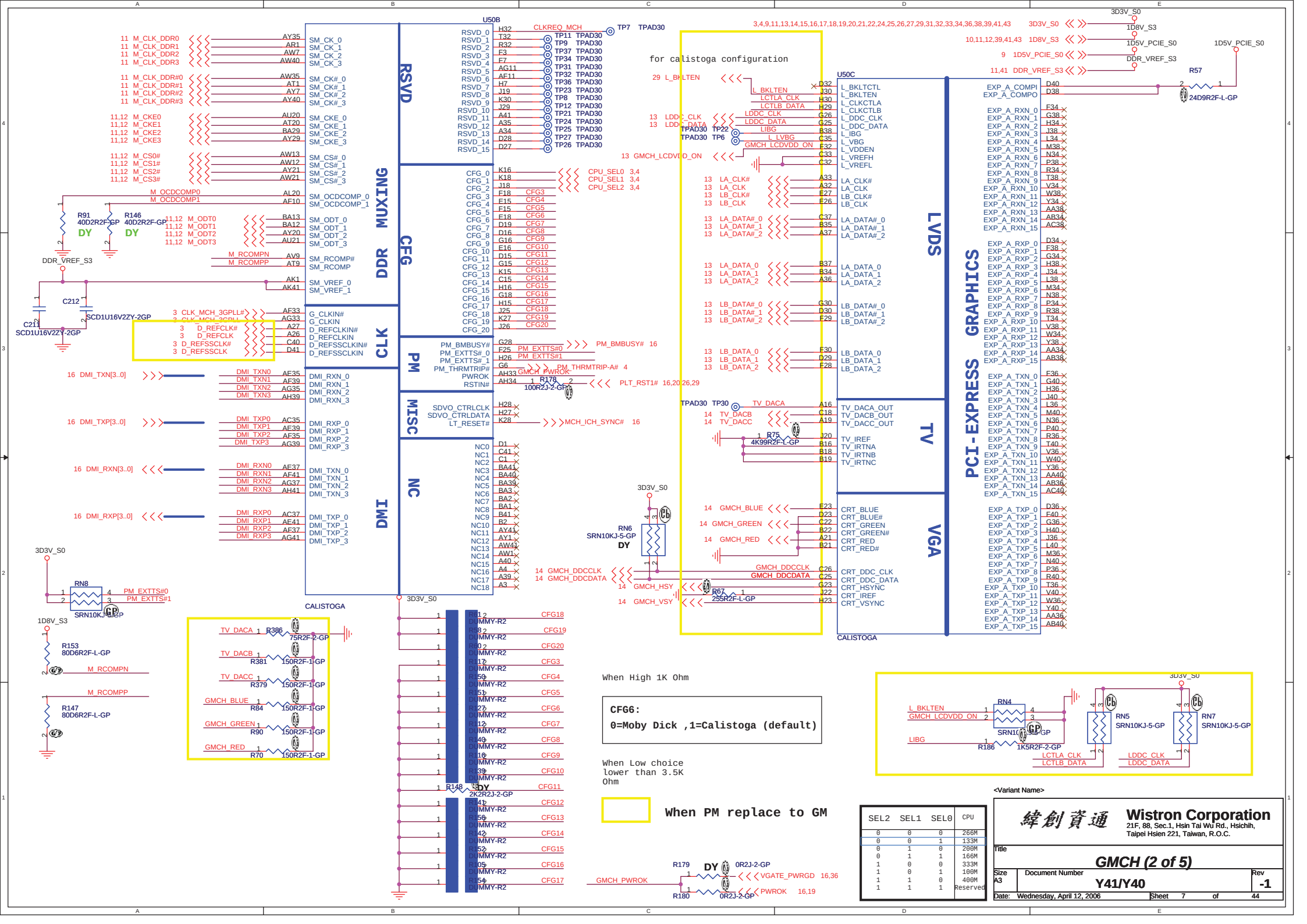
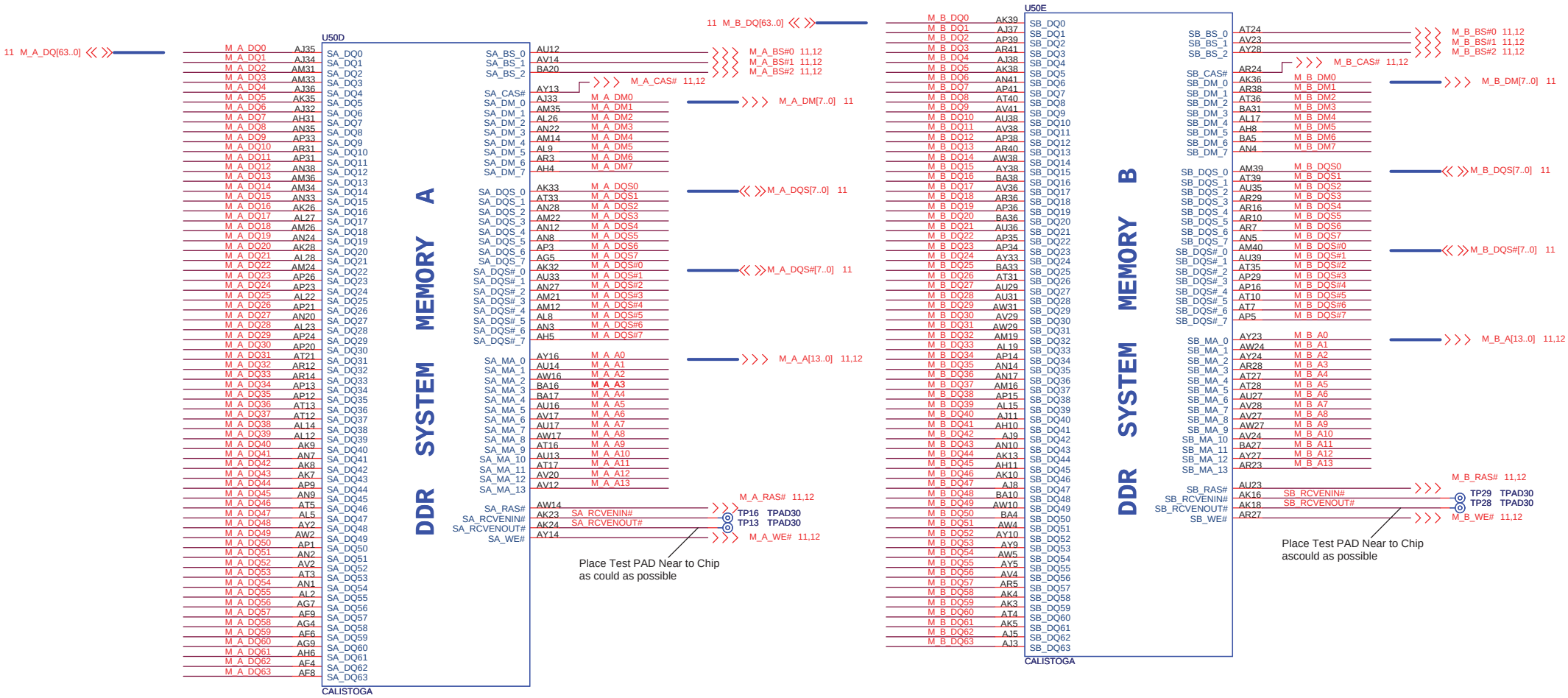
Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 6 of 44


U50B
RSVD
CFG
MUXING
DDR
CLK
PM
MISC
NC
DMI
U50C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
for calistoga configuration
When High 1K Ohm
When Low choice lower than 3.5K Ohm
When PM replace to GM
CFG6:
0=Moby Dick ,1=Calistoga (default)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GMCH (2 of 5)
Y41/Y40
-1
Wednesday, April 12, 2006
SEL2 SEL1 SEL0 CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved



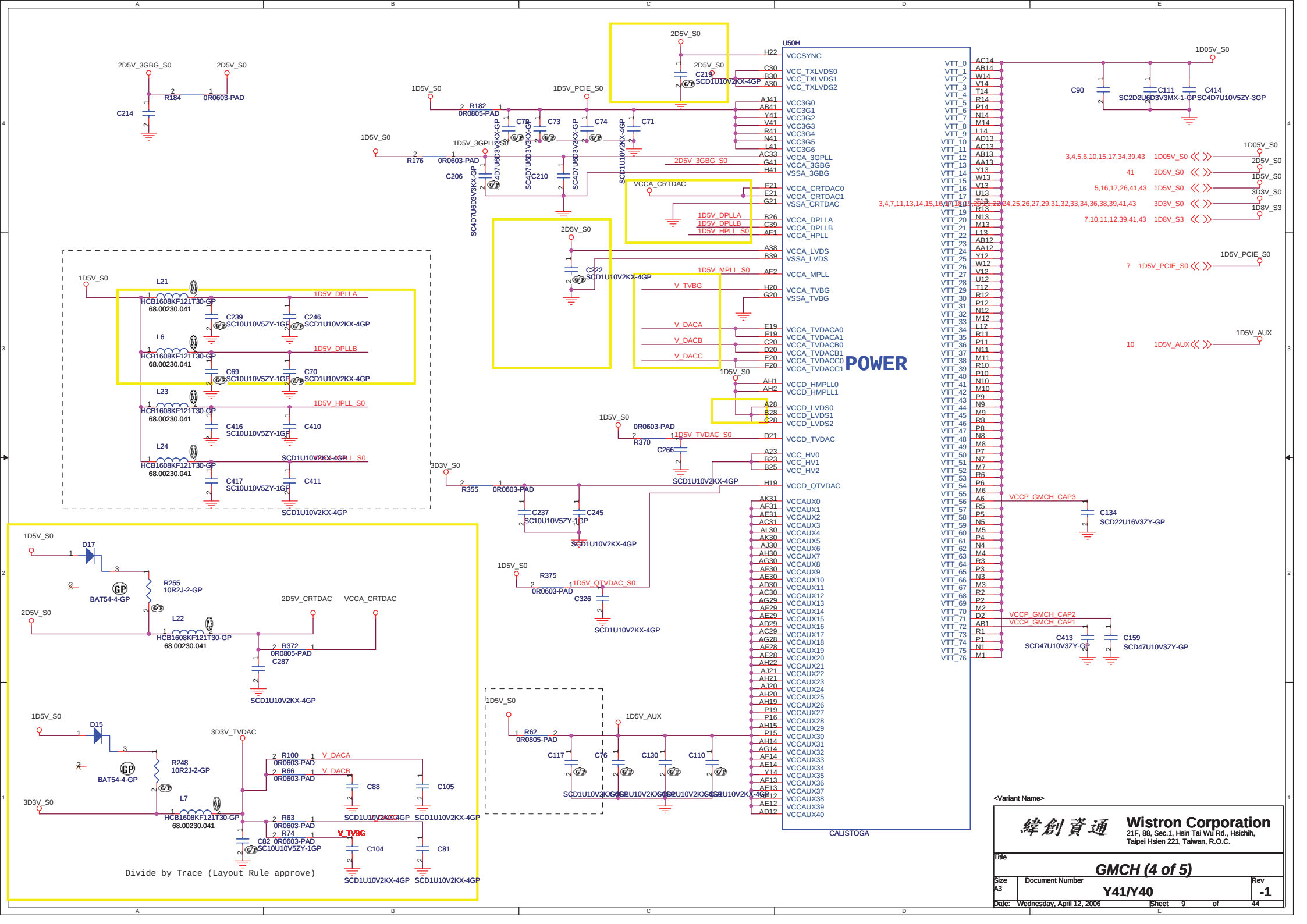
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH (3 of 5)**

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 8 of 44



Wistron Corporation
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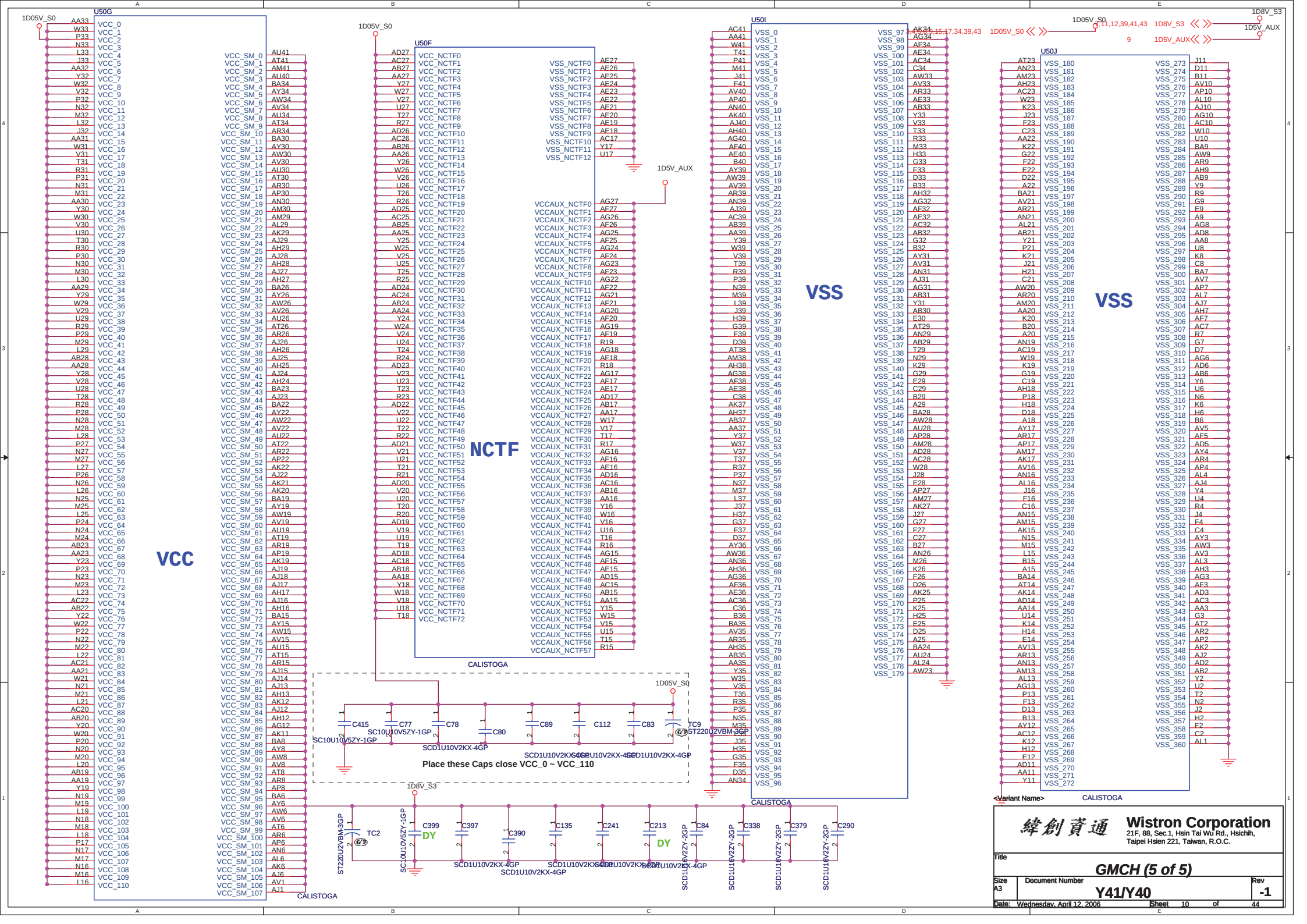
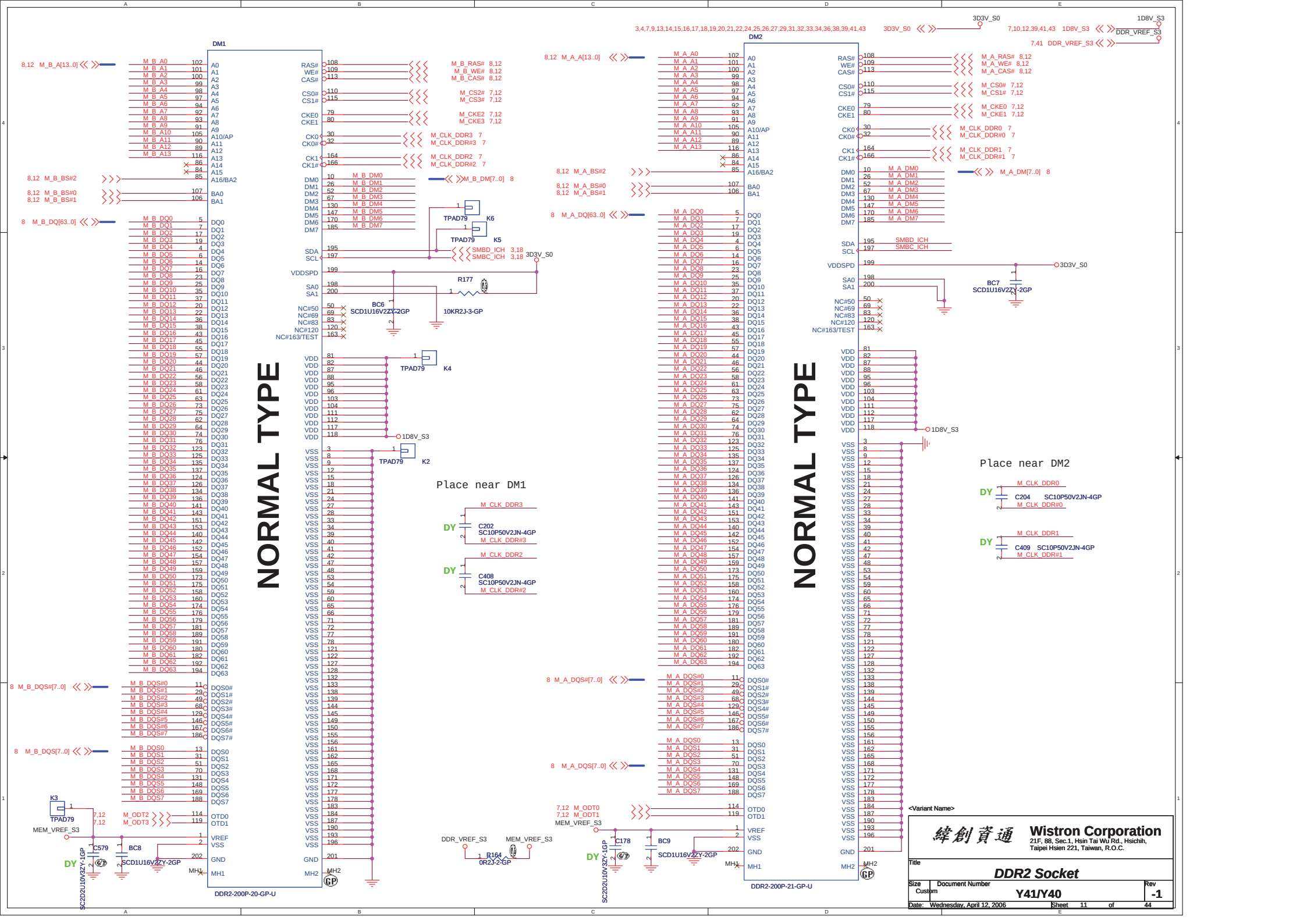
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>
Title: GMCH (4 of 5)
Size: A3
Document Number: Y41/Y40
Rev: -1
Date: Wednesday, April 12, 2006
Sheet 9 of 44


U50G
VCC
U50F
NCTF
U50I
VSS
U50J
VSS
CALISTOGA
1D05V_S0
1D8V_S3
1D5V_AUX
Place these Caps close VCC_0 ~ VCC_110
C415
C77
C78
C80
C89
C112
C83
TC9
SC10U10V5ZY-1GP
SCD1U10V2KX-4GP
ST220U2VBM-3GP
TC2
C399
C397
C390
C135
C241
C213
C84
C338
C379
C290
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (5 of 5)
Size A3
Document Number
Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
Sheet 10 of 44


DM1
DM2
NORMAL TYPE
NORMAL TYPE
DDR2-200P-20-GP-U
DDR2-200P-21-GP-U
Place near DM1
Place near DM2
M_B_A[13..0]
M_B_DQ[63..0]
M_B_DQS#[7..0]
M_B_DQS[7..0]
M_A_A[13..0]
M_A_DQ[63..0]
M_A_DQS#[7..0]
M_A_DQS[7..0]
M_B_DM[7..0]
M_A_DM[7..0]
M_B_RAS# 8,12
M_B_WE# 8,12
M_B_CAS# 8,12
M_CS2# 7,12
M_CS3# 7,12
M_CKE2 7,12
M_CKE3 7,12
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
SMBD_ICH 3,18
SMBC_ICH 3,18
3D3V_S0
1D8V_S3
DDR_VREF_S3
MEM_VREF_S3
M_A_RAS# 8,12
M_A_WE# 8,12
M_A_CAS# 8,12
M_CS0# 7,12
M_CS1# 7,12
M_CKE0 7,12
M_CKE1 7,12
M_CLK_DDR0 7
M_CLK_DDR#0 7
M_CLK_DDR1 7
M_CLK_DDR#1 7
SMBD_ICH
SMBC_ICH
M_ODT2 7,12
M_ODT3 7,12
M_ODT0 7,12
M_ODT1 7,12
TPAD79 K6
TPAD79 K5
TPAD79 K4
TPAD79 K2
TPAD79 K3
R177 10KR2J-3-GP
R164 0R2J-2-GP
BC6 SCD1U16V2ZY-2GP
BC7 SCD1U16V2ZY-2GP
BC8 SCD1U16V2ZY-2GP
BC9 SCD1U16V2ZY-2GP
C579 SC22D2U10V3Z7-1GP
C178 SC22D2U10V3Z7-1GP
C202 SC10P50V2JN-4GP
C408 SC10P50V2JN-4GP
C204 SC10P50V2JN-4GP
C409 SC10P50V2JN-4GP
DY
GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
Y41/Y40
Rev
-1
Date: Wednesday, April 12, 2006
Sheet 11 of 44

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN13 SRN56J-5-GP
- M_CKE2 7,11
- M_B_BS#2 8,11
- M_B_A12
- M_B_A9

M_A_A[13..0] 8,11

M_B_A[13..0] 8,11

R389 56R2J-4-GP
R387 56R2J-4-GP
R367 56R2J-4-GP M_A_A9
R368 56R2J-4-GP M_B_A8
- M_ODT1 7,11
- M_ODT3 7,11

RN42 SRN56J-5-GP
- M_B_A5
- M_B_A3
- M_B_A1
- M_B_A10

RN48 SRN56J-5-GP
- M_B_A13
- M_ODT2 7,11
- M_CS2# 7,11
- M_B_RAS# 8,11

RN44 SRN56J-5-GP
- M_B_BS#1 8,11
- M_B_A0
- M_B_A2
- M_B_A4

RN41 SRN56J-5-GP
- M_B_A6
- M_B_A7
- M_B_A11
- M_CKE3 7,11

RN46 SRN56J-5-GP
- M_B_BS#0 8,11
- M_B_WE# 8,11
- M_CS3# 7,11
- M_B_CAS# 8,11

RN47 SRN56J-5-GP
- M_A_A13
- M_ODT0 7,11
- M_CS0# 7,11
- M_A_RAS# 8,11

RN43 SRN56J-5-GP
- M_A_BS#1 8,11
- M_A_A0
- M_A_A2
- M_A_A4

RN49 SRN56J-5-GP
- M_A_BS#0 8,11
- M_A_WE# 8,11
- M_A_CAS# 8,11
- M_CS1# 7,11

RN40 SRN56J-5-GP
- M_CKE0 7,11
- M_A_BS#2 8,11
- M_A_A12
- M_A_A8

RN25 SRN56J-5-GP
- M_A_A6
- M_A_A7
- M_A_A11
- M_CKE1 7,11

RN45 SRN56J-5-GP
- M_A_A5
- M_A_A3
- M_A_A1
- M_A_A10

Decoupling Capacitor

1D8V_S3
- 7,10,11,39,41,43 1D8V_S3
- DDR_VREF_S0
- 41,43 DDR_VREF_S0

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C216 SCD1U16V2ZY-2GP DY
C228 SCD1U16V2ZY-2GP
C223 SCD1U16V2ZY-2GP
C384 SCD1U16V2ZY-2GP
C231 SCD1U16V2ZY-2GP
C294 SCD1U16V2ZY-2GP
C296 SCD1U16V2ZY-2GP DY
C385 SCD1U16V2ZY-2GP
C252 SCD1U16V2ZY-2GP
C375 SCD1U16V2ZY-2GP
C240 SCD1U16V2ZY-2GP

C229 SCD1U16V2ZY-2GP DY
C382 SCD1U16V2ZY-2GP
C377 SCD1U16V2ZY-2GP
C227 SCD1U16V2ZY-2GP
C361 SCD1U16V2ZY-2GP
C220 SCD1U16V2ZY-2GP
C224 SCD1U16V2ZY-2GP
C371 SCD1U16V2ZY-2GP DY
C226 SCD1U16V2ZY-2GP
C230 SCD1U16V2ZY-2GP
C254 SCD1U16V2ZY-2GP

1D8V_S3

Place these Caps near DM1

C86 SC2D2U6D3V3MX-1-GP
C92 SC2D2U6D3V3MX-1-GP
C108 SC2D2U6D3V3MX-1-GP
C123 SC2D2U6D3V3MX-1-GP
C131 SC2D2U6D3V3MX-1-GP

C267 SCD1U16V2ZY-2GP DY
C247 SCD1U16V2ZY-2GP DY
C383 SCD1U16V2ZY-2GP DY
C324 SCD1U16V2ZY-2GP

1D8V_S3

Place these Caps near DM2

C116 SC2D2U6D3V3MX-1-GP
C79 SC2D2U6D3V3MX-1-GP
C133 SC2D2U6D3V3MX-1-GP
C96 SC2D2U6D3V3MX-1-GP
C85 SC2D2U6D3V3MX-1-GP

C308 SCD1U16V2ZY-2GP DY
C253 SCD1U16V2ZY-2GP DY
C376 SCD1U16V2ZY-2GP DY
C381 SCD1U16V2ZY-2GP

<Variant Name>

緯創資通 **Wistron Corporation**
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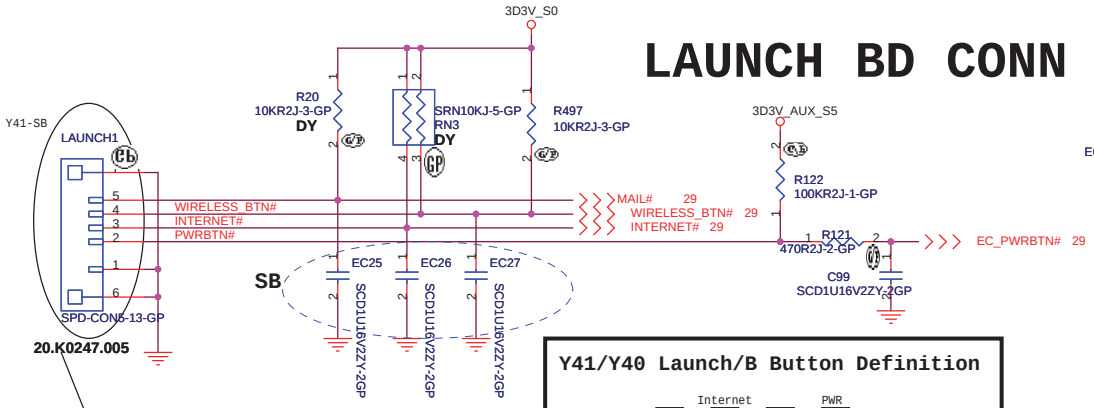
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	Y41/Y40	-1

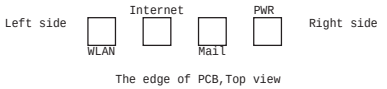
Date: Wednesday, April 12, 2006 Sheet 12 of 44

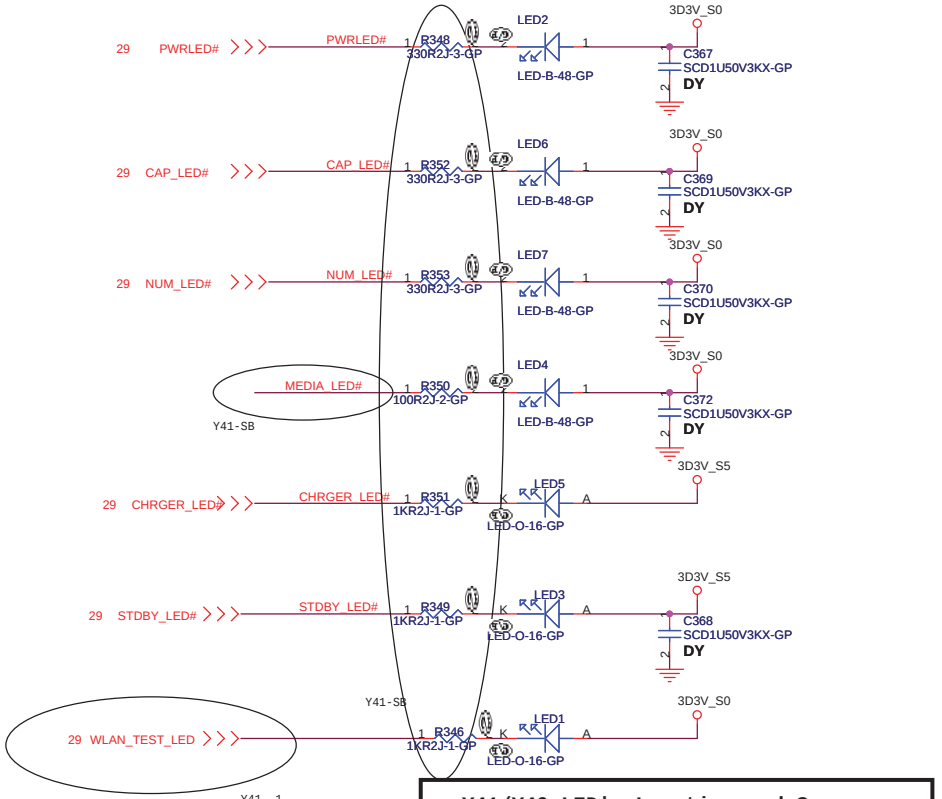
LAUNCH BD CONN



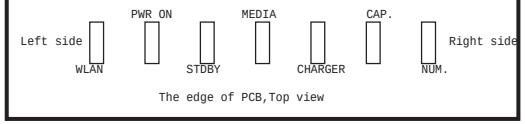
The pin1 of M/B side connects
the pin5 of Launch/B side.

Y41/Y40 Launch/B Button Definition

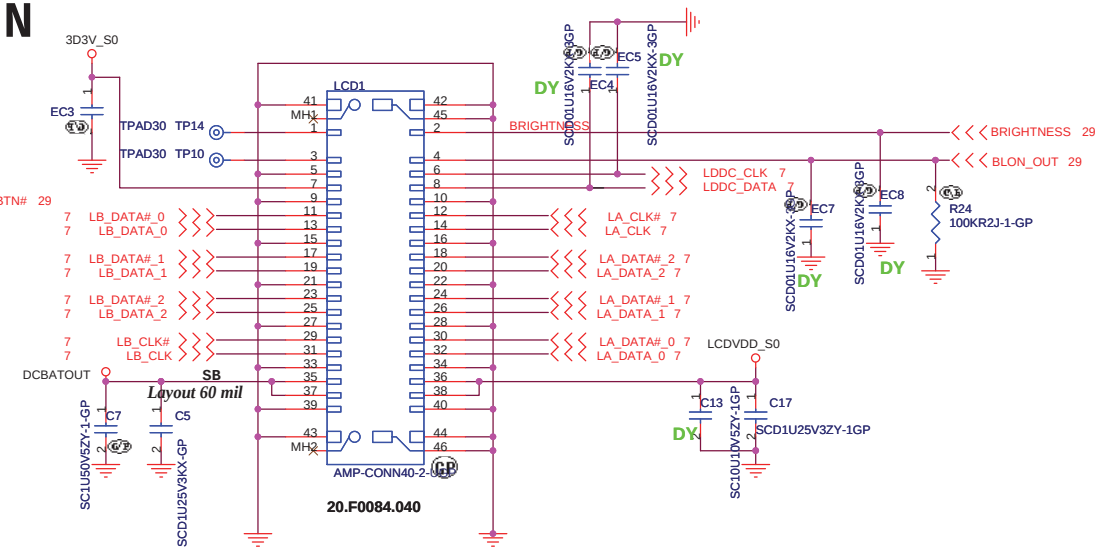


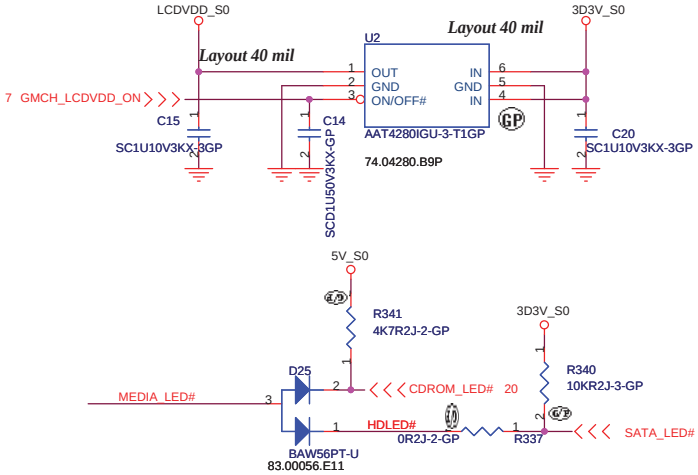


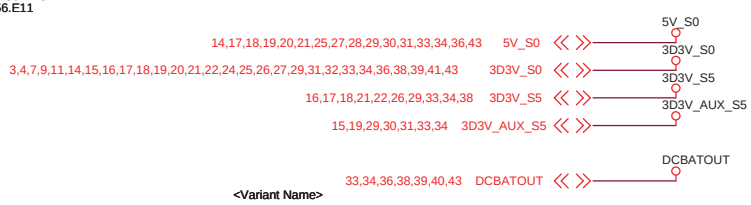
Y41/Y40 LED's Location and Sequence



LCD/INVERTER







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD / LAUNCH / LEDs

Size	Document Number	Rev
Custom	Y41/Y40	-1

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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

CRT_RED_SYS
CRT_GREEN_SYS
CRT_BLUE_SYS

L30 FCB1608CF-GP
L27 FCB1608CF-GP
L31 FCB1608CF-GP
L28 FCB1608CF-GP
L32 FCB1608CF-GP
L29 FCB1608CF-GP

CRT_R
CRT_G
CRT_B

R183 150R2F-1-GP
R181 150R2F-1-GP
R171 150R2F-1-GP

C565 SC1D8P50V2CC-GP
C566 SC1D8P50V2CC-GP
C567 SC1D8P50V2CC-GP
C184 SC1D8P50V2CC-GP
C180 SC1D8P50V2CC-GP
C169 SC1D8P50V2CC-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

5V_S0
D18 CH751H-40PT
RN50 SRN4K7J-8-GP
5V_CRT_S0
C420 SCD01U16V2KX-3GP

CRT1
VIDEO-15-42-GP-U
20.20378.015

DAT_DDC1_5
JVGA_HS
JVGA_VS
CLK_DDC1_5

C419 SC100P50V2JN-3GP
C147 SC22P50V2JN-4GP
C404 SC100P50V2JN-3GP
C155 SC22P50V2JN-4GP

Hsync & Vsync level shift

33 GMCH_HSY_DOCK
7 GMCH_HSY
7 GMCH_VSY
33 GMCH_VSY_DOCK

R160 0R2J-2-GP Y40_DY
R157 0R2J-2-GP Y40_DY
R159 47R2J-2-GP HSYNC_4
R158 47R2J-2-GP VSYNC_4

C160 SCD1U16V2ZY-2GP
U10A
U10B
TSAHCT125PW-GP
CRT_HSYNC1
CRT_VSYNC1
R162 0R2J-2-GP JVGA_HS
R161 0R2J-2-GP JVGA_VS

For System CRT

3D3V_S0

DDC_CLK & DATA level shift

RN51 SRN4K7J-8-GP
Y41-SB
R498 0R2J-2-GP Y40_DY DAT_DDC1_5
R499 0R2J-2-GP Y40_DY CLK_DDC1_5
GMCH_DDCDATA_DOCK 33
GMCH_DDCCLK_DOCK 33
7 GMCH_DDCDATA
7 GMCH_DDCCLK
2SK3019-N-2GP Q28
2SK3019-N-2GP Q27

23,29,33 DOCK_IN#
Q26 DTC115EE-2-GP
R241 2K2R2F-GP
VGA_SYS_ON#
R187 4K7R2F-GP
Q25 DTC115EE-2-GP

U47 SNCB3Q3306APWRGP
U49 SNCB3Q3306APWRGP
U48 SNCB3Q3306APWRGP
C576 SCD1U16V2ZY-2GP
C577 SCD1U16V2ZY-2GP
C578 SCD1U16V2ZY-2GP
R294 0R2J-2-GP
R289 0R2J-2-GP
R328 0R2J-2-GP

7 GMCH_RED
7 GMCH_GREEN
7 GMCH_BLUE
CRT_RED_DOCK 33
CRT_GREEN_DOCK 33
CRT_BLUE_DOCK 33

TV OUT CONN

7 TV_DACC
7 TV_DACB

L16 MLB201209-0150A-GP
L18 MLB201209-0150A-GP
C193 DY SC33P50V3JN-GP
C243 DY SC33P50V3JN-GP
C200 SC6P50V2CN-1GP
C205 SC6P50V2CN-1GP
C238 SC6P50V2CN-1GP
C217 SC6P50V2CN-1GP
R204 150R2F-1-GP
R226 150R2F-1-GP
CRMA_1
LUMA_1

TVOUT1 MINDIN4-29-GP
GND GND CRMA LUMA GND GND

Reverse type

D22 D19 BAV99PT-GP-U
TVout

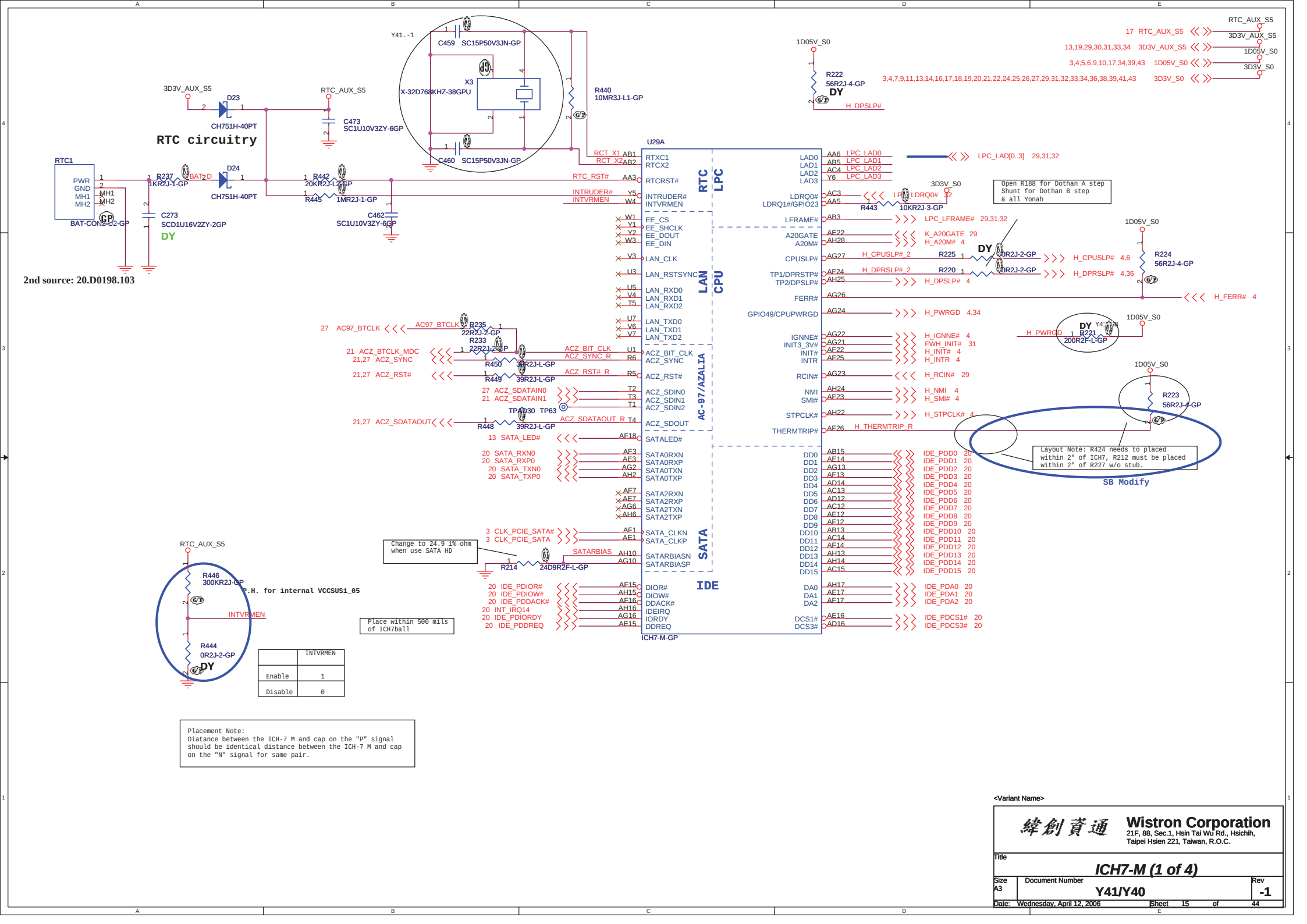
D16 D14 D13 BAV99PT-GP-U

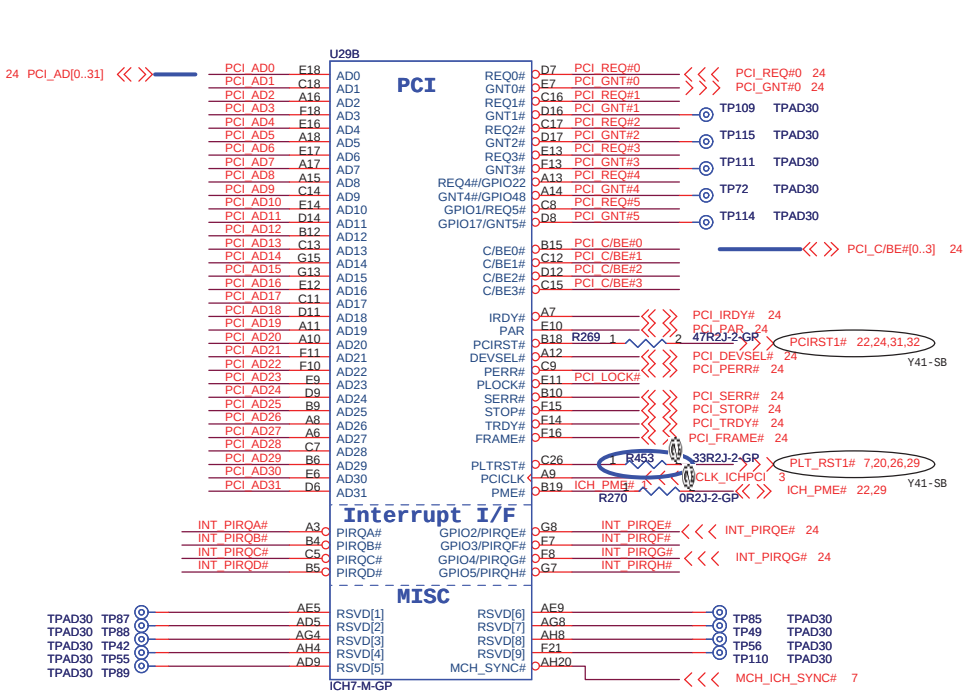
13,17,18,19,20,21,25,27,28,29,30,31,33,34,36,43 5V_S0
2,4,7,9,11,13,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

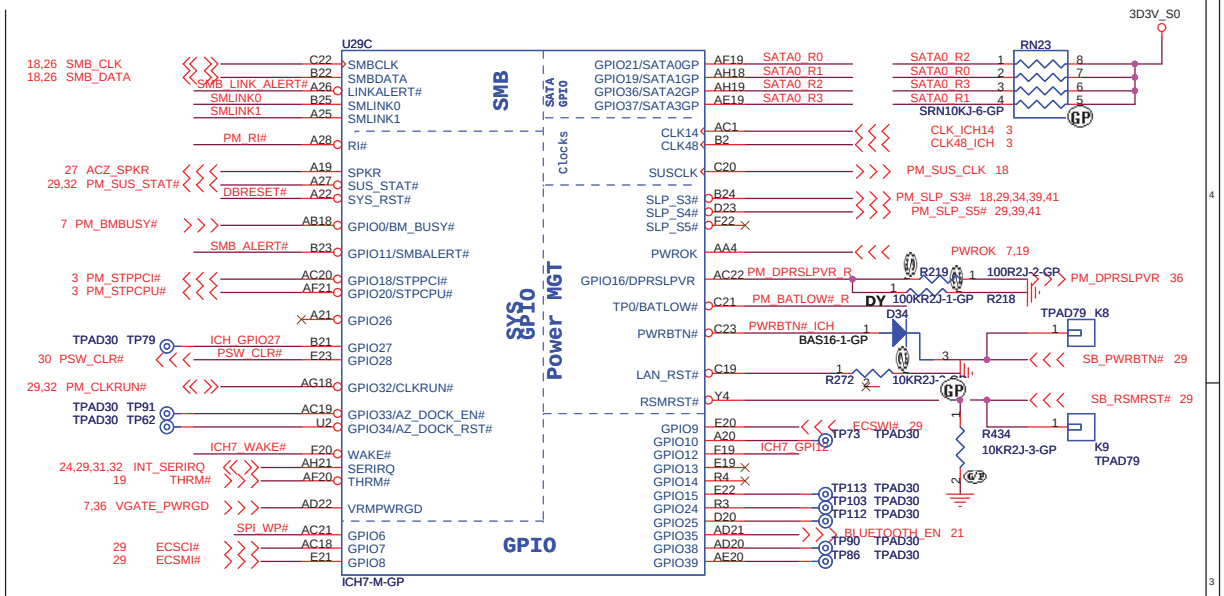
<Variant Name>

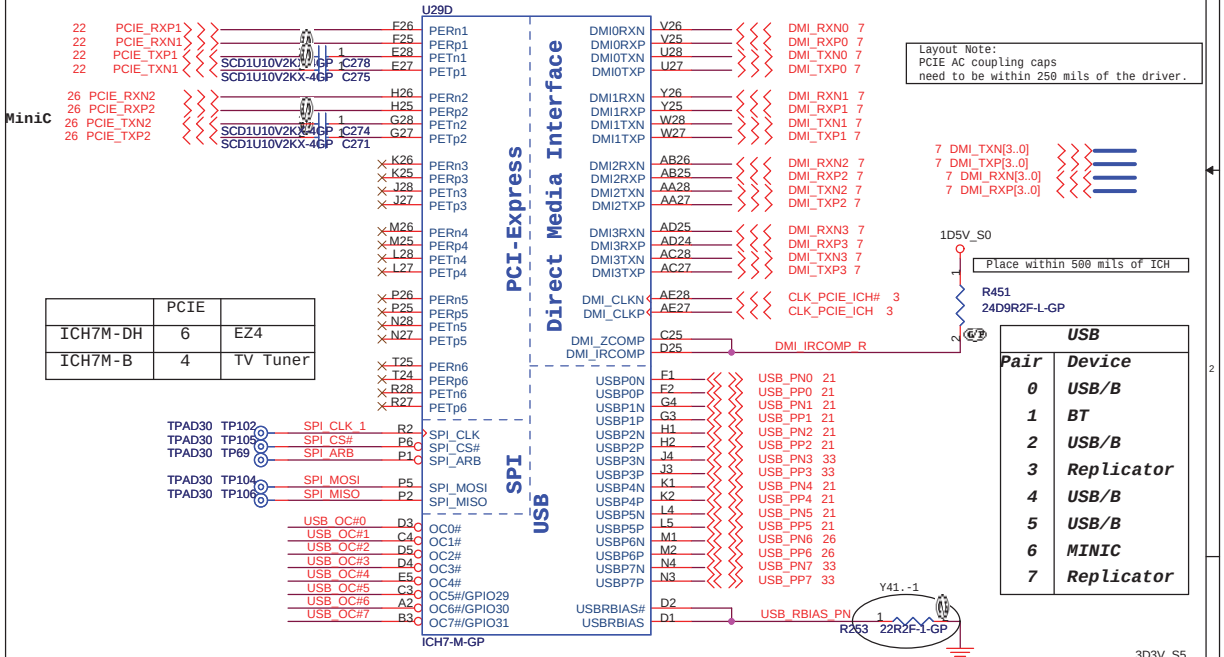
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Y41/Y40
Rev: -1
Date: Friday, May 26, 2006
Sheet 14 of 44

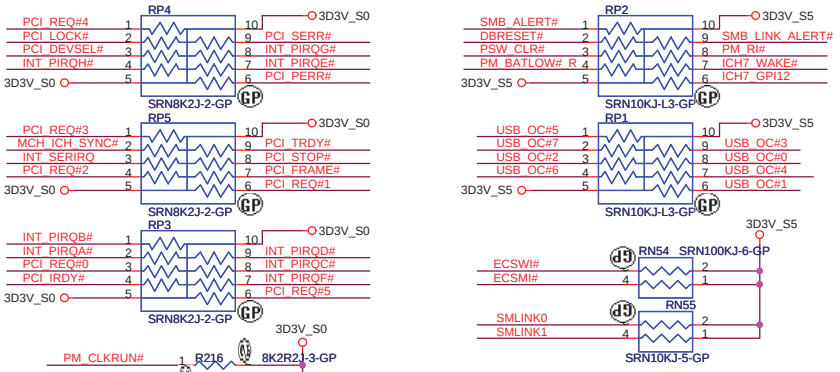

RTC circuitry
2nd source: 20.D0198.103
U29A
ICH7-M-GP
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
SB Modify
Layout Note: R424 needs to placed within 2" of ICH7, R212 must be placed within 2" of R227 w/o stub.
Open R188 for Dothan A step
Shunt for Dothan B step
& all Yonah
Change to 24.9 1% ohm when use SATA HD
Place within 500 mils of ICH7ball
P.H. for internal VCCSUS1_05
Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.
INTVRMEN
Enable 1
Disable 0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH7-M (1 of 4)
Y41/Y40
-1
Wednesday, April 12, 2006
15
44

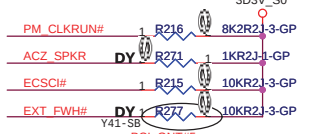


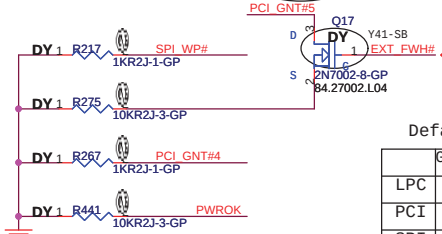




ICH7 Pullups







Default:H

	GNT5#	GNT4#
LPC	H	H
PCI	H	L
SPI	L	H

T=22ms

Boot from various source

	PCIE	
ICH7M-DH	6	EZ4
ICH7M-B	4	TV Tuner

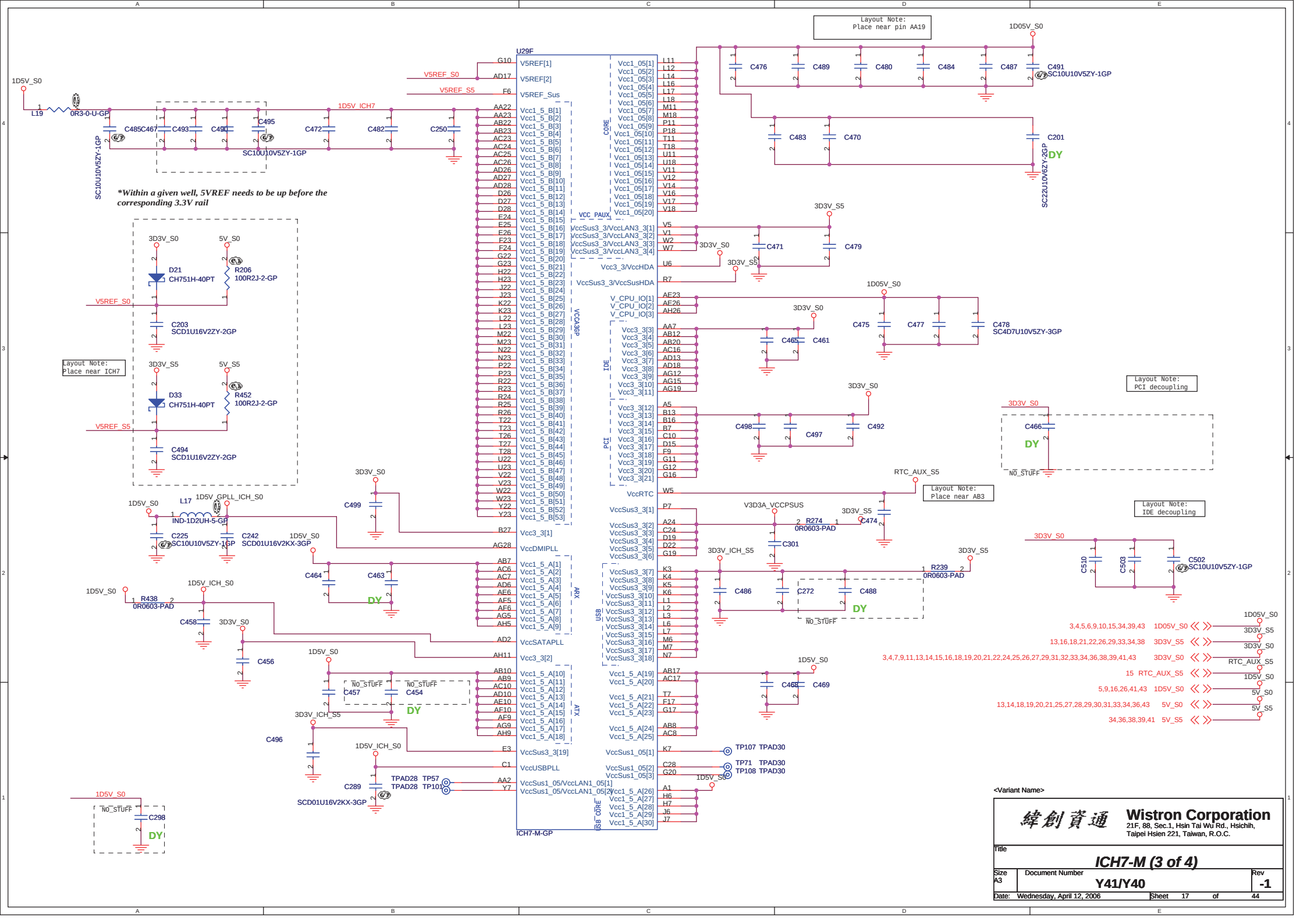
USB	
Pair	Device
0	USB/B
1	BT
2	USB/B
3	Replicator
4	USB/B
5	USB/B
6	MINIC
7	Replicator

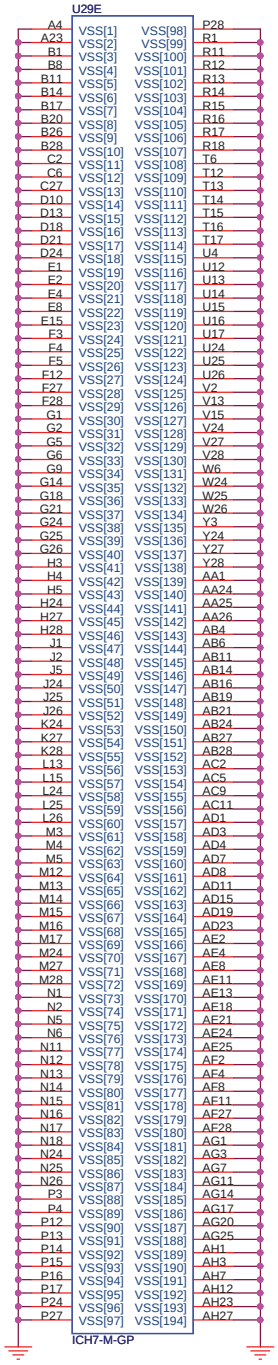
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.

Place within 500 mils of ICH

<variant_name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ICH7-M (2 of 4)
Size A3	Document Number Y41/Y40
Rev	-1
Date: Wednesday, April 12, 2006	Sheet 16 of 44


U29F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: PCI decoupling
Layout Note: Place near AB3
Layout Note: IDE decoupling
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
Y41/Y40
Rev
-1
Date: Wednesday, April 12, 2006
Sheet 17 of 44



5V_S0
3D3V_S5
3D3V_S0
13,14,17,19,20,21,25,27,28,29,30,31,33,34,36,43 5V_S0
13,16,17,21,22,26,29,33,34,38 3D3V_S5
3,4,7,9,11,13,14,15,16,17,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

32K suspend clock output

3D3V_S5

U30

16,29,34,39,41 PM_SLP_S3#
16 PM_SUS_CLK

OE VCC
A Y
GND

NC7SZ126P5X-GP

32KHZ

R240 100R2J-2-GP

G792_32K 19

73.7S126.AAH

R238
240KR3-GP
63.24434.15L

SMBUS

3D3V_S5 5V_S0 3D3V_S0

RN34
SRN4K7J-8-GP

RN24
SRN4K7J-8-GP

Q13
2N7002-8-GP

16,26 SMB_CLK
16,26 SMB_DATA

SMBC_ICH 3,11
SMBD_ICH 3,11

Q12
2N7002-8-GP

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

84.27002.L04

<Variant Name>

Wistron Corporation
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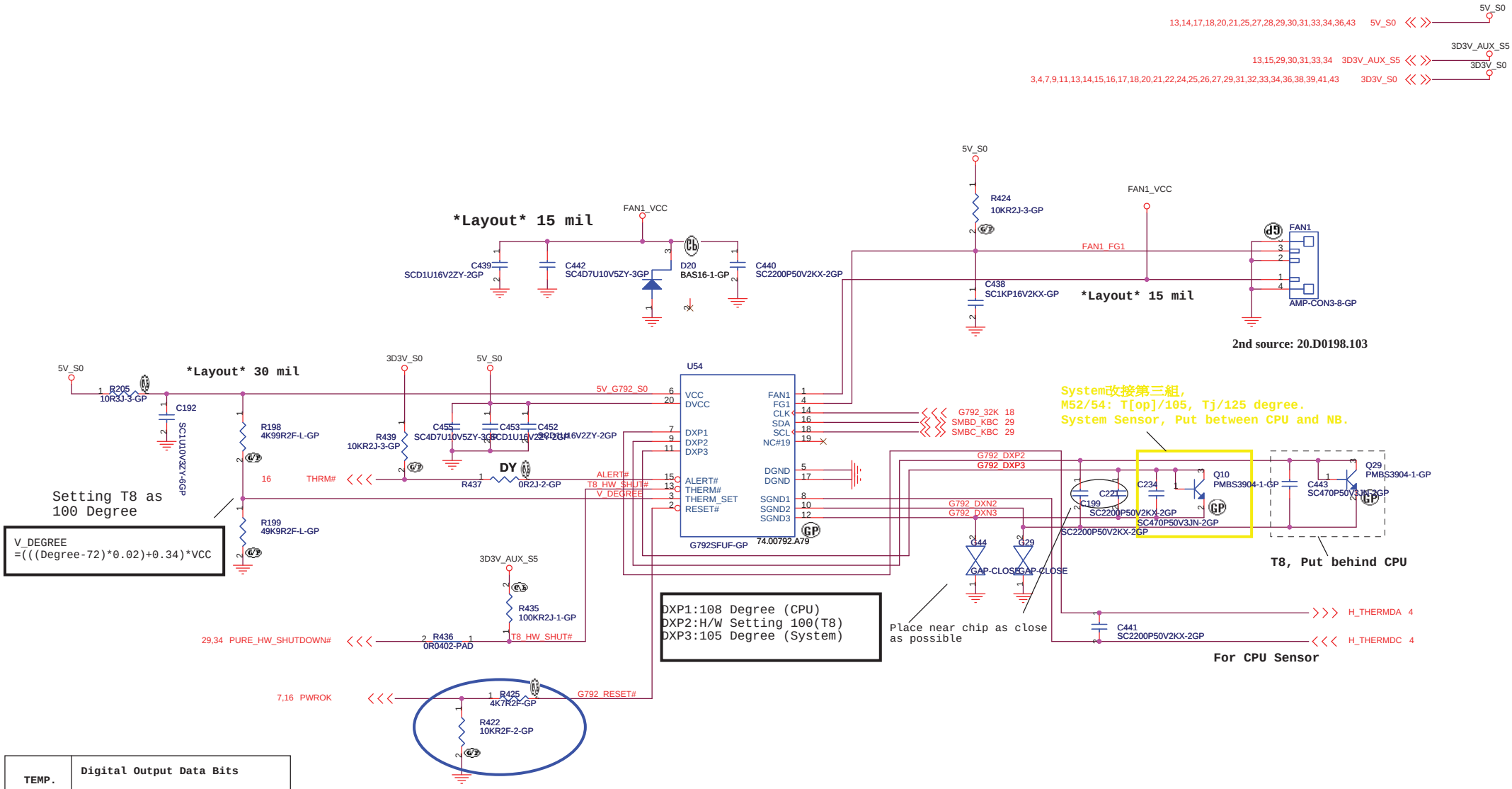
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH7-M (4 of 4)/ODD*

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 18 of 44



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

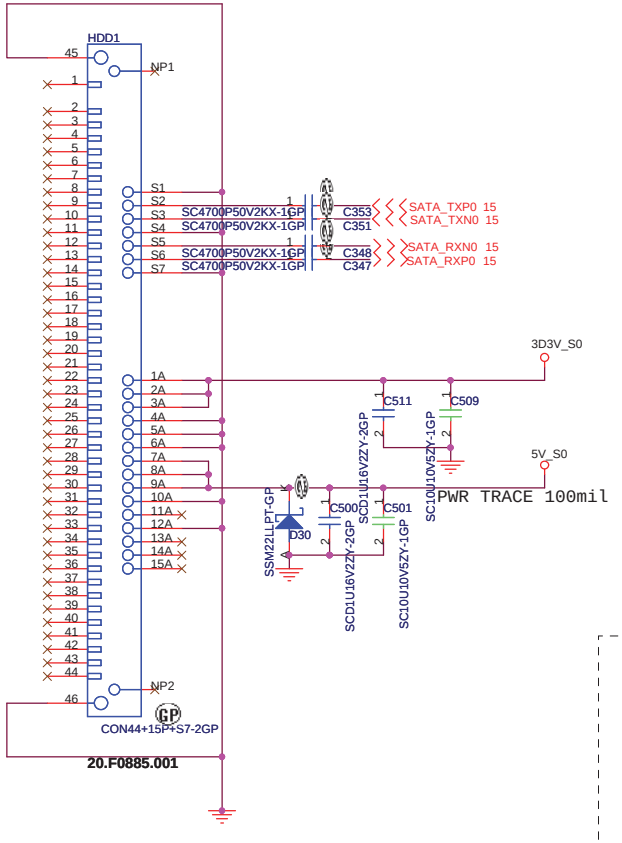
Title: Thermal/Fan Controllor G792

Size: Custom | Document Number: Y41/Y40 | Rev: -1

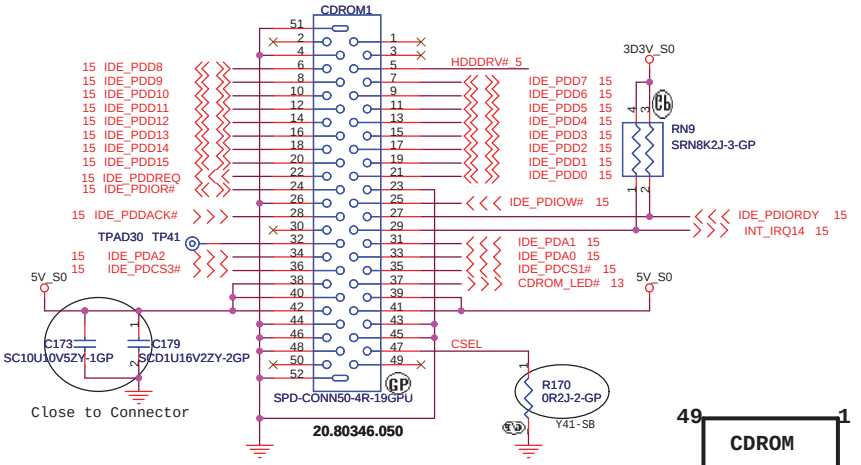
Date: Wednesday, April 12, 2006 | Sheet 19 of 44

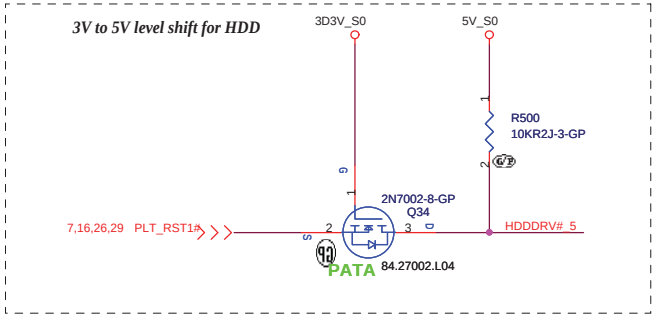
5V_S0
3D3V_S0
13,14,17,18,19,21,25,27,28,29,30,31,33,34,36,43 5V_S0
3,4,7,9,11,13,14,15,16,17,18,19,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

SATA Connector



CDROM Connector

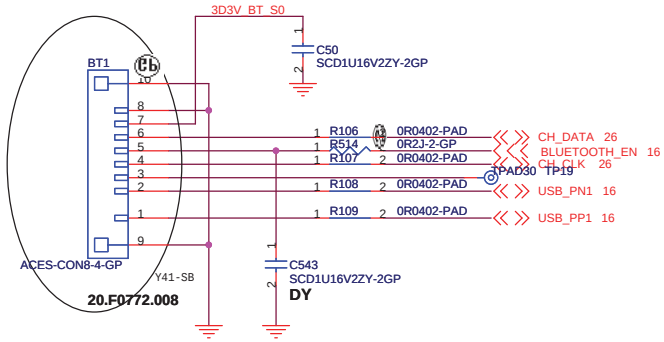


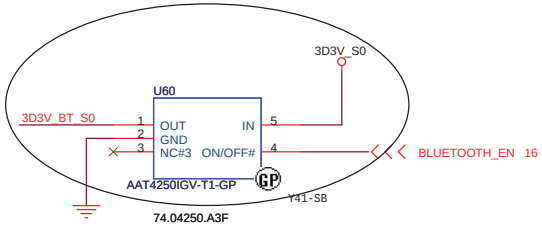


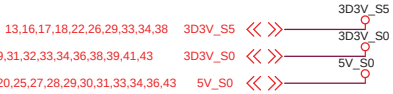
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

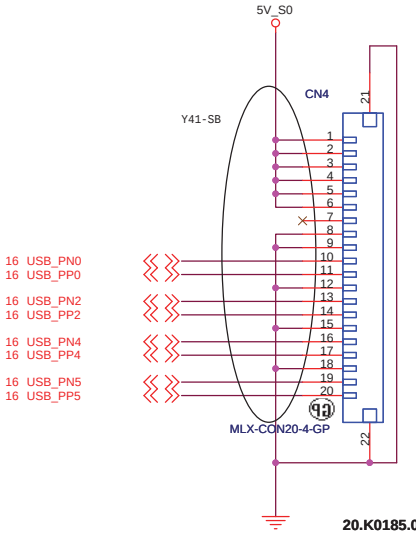
Title	SATA/PATA HDD ULi-M5285	
Size A3	Document Number Y41/Y40	Rev -1
Date: Wednesday, April 12, 2006	Sheet 20 of 44	





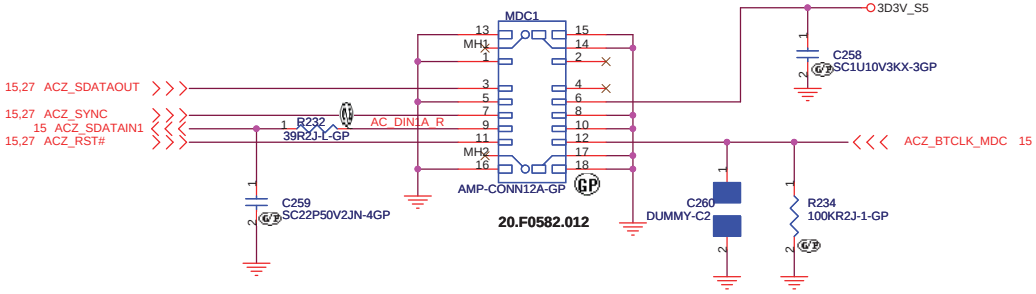


USB PORT



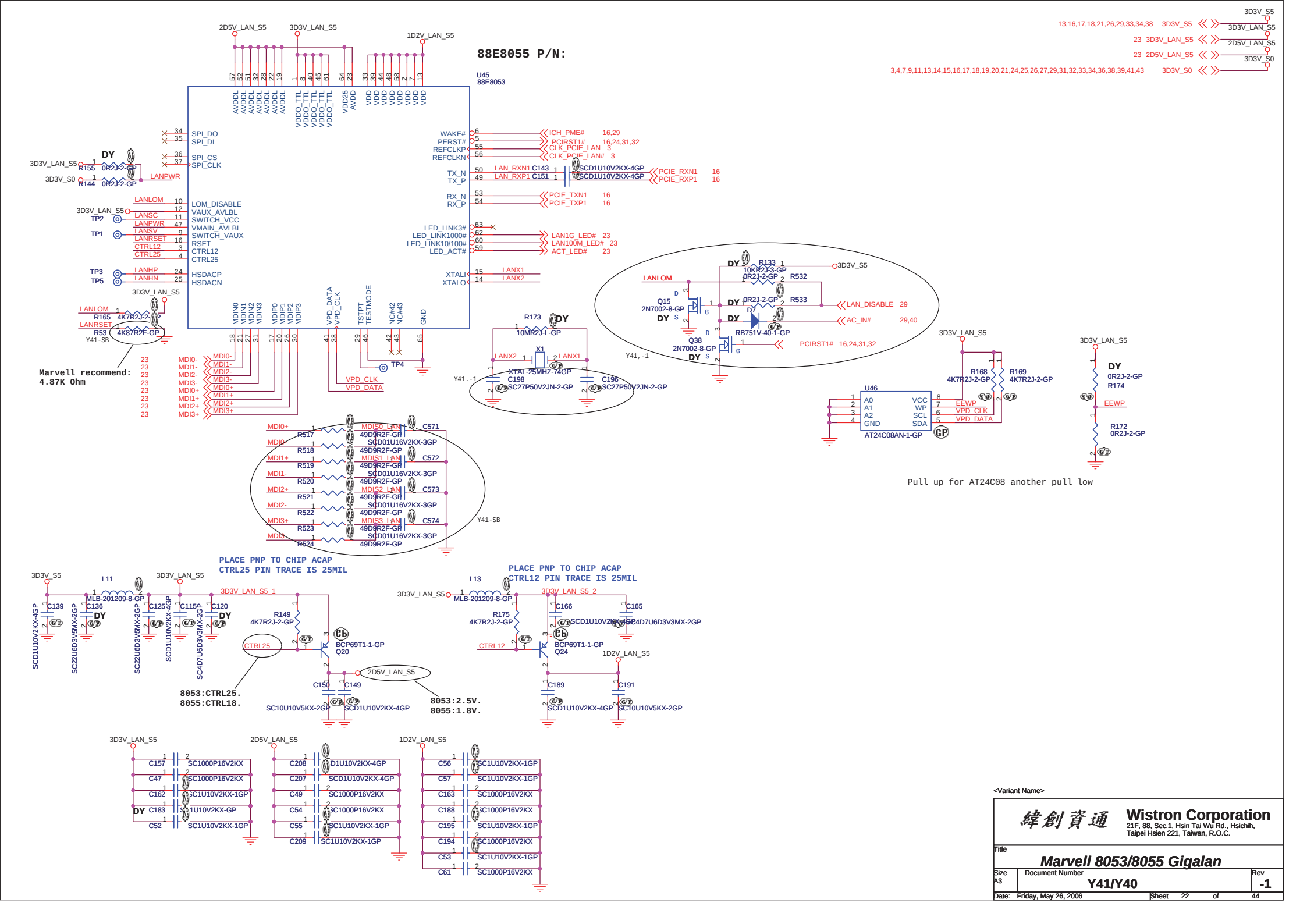
Cable length = 120mm.

MDC 1.5 CONN



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB and MDC I/F		
Size: A3	Document Number: Y41/Y40	Rev: -1
Date: Wednesday, April 12, 2006	Sheet 21 of 44	


88E8055 P/N:
U45
88E8053
2D5V_LAN_S5
3D3V_LAN_S5
1D2V_LAN_S5
SPI_DO
SPI_DI
SPI_CS
SPI_CLK
LANPWR
LOM_DISABLE
VAUX_AVLBL
SWITCH_VCC
VMAIN_AVLBL
SWITCH_VAUX
RSET
CTRL12
CTRL25
HSDACP
HSDACN
WAKE#
PERST#
REFCLKP
REFCLKN
TX_N
TX_P
RX_N
RX_P
XTALI
XTALO
LED_LINK3#
LED_LINK1000#
LED_LINK10/100#
LED_ACT#
MDIN0
MDIN1
MDIN2
MDIN3
MDIP0
MDIP1
MDIP2
MDIP3
VPD_DATA
VPD_CLK
TSTPT
TESTMODE
NC#42
NC#43
GND
Marvell recommend:
4.87K Ohm
Y41-SB
Y41,-1
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
8053:CTRL25.
8055:CTRL18.
8053:2.5V.
8055:1.8V.
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
Pull up for AT24C08 another pull low
U46
AT24C08AN-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
Marvell 8053/8055 Gigalan
Size
A3
Document Number
Y41/Y40
Rev
-1
Date: Friday, May 26, 2006
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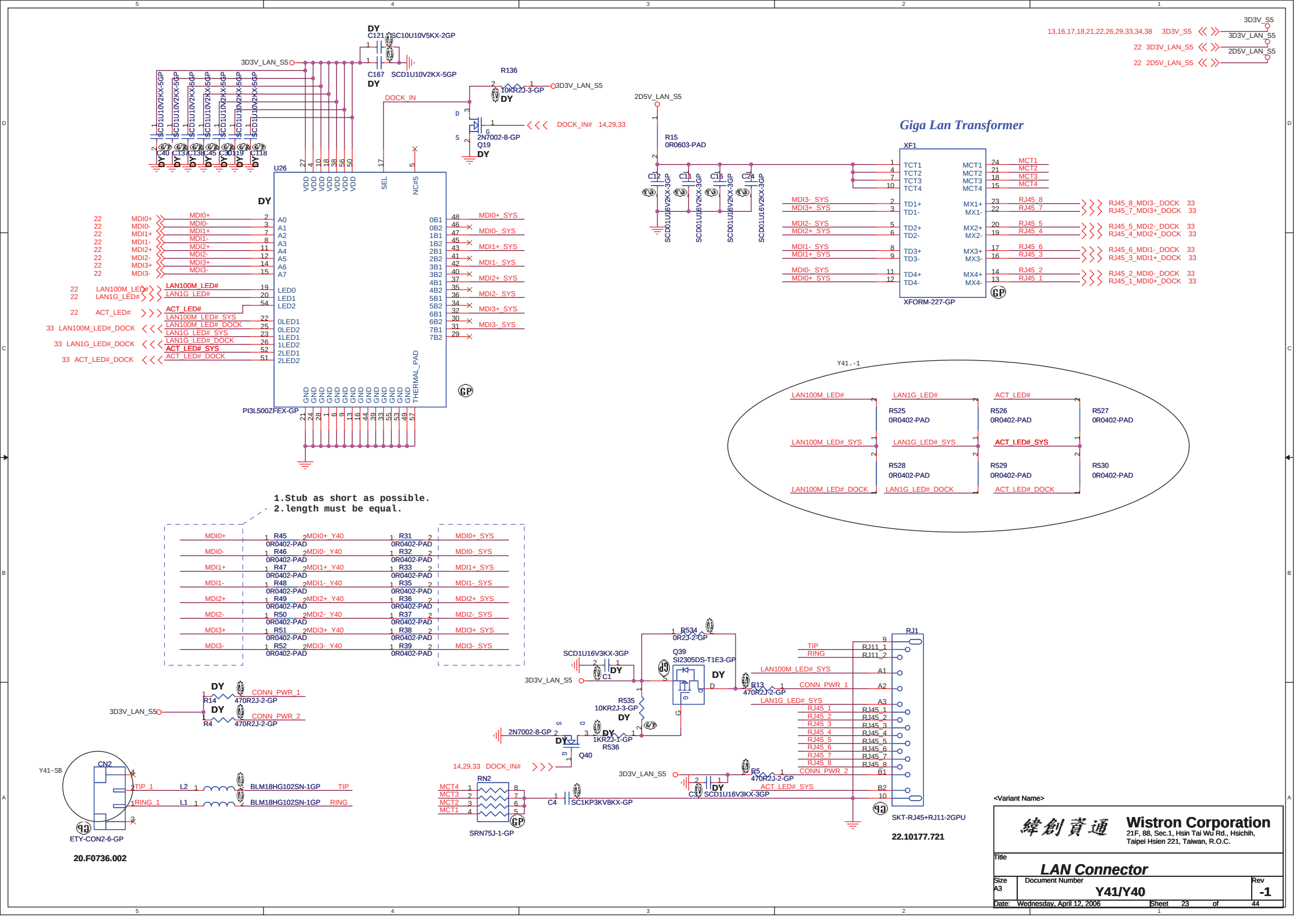
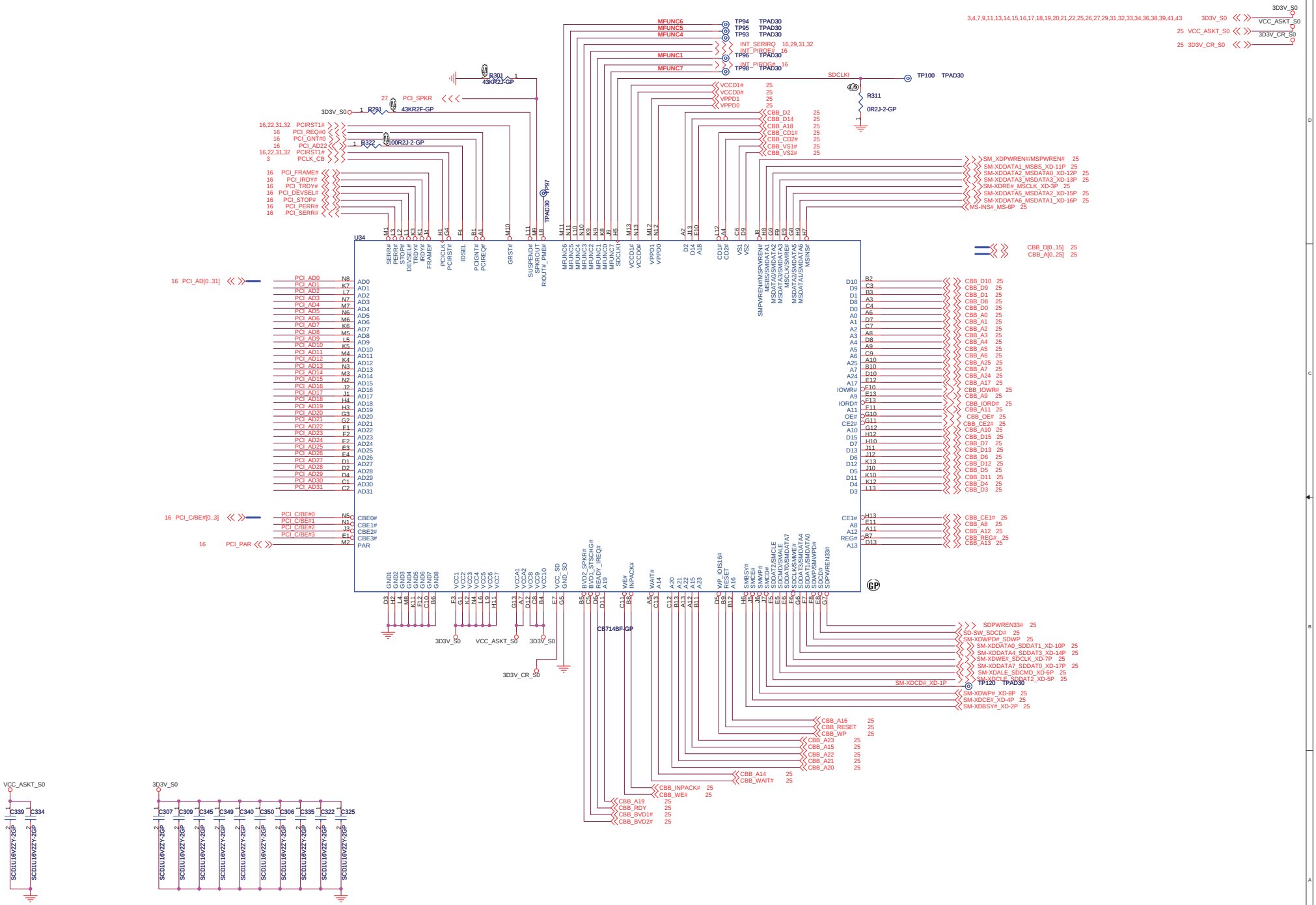

Giga Lan Transformer
XFORM-227-GP
PI3L500ZFEX-GP
1.Stub as short as possible.
2.length must be equal.
ETY-CON2-6-GP
SKT-RJ45+RJ11-2GPU
SRN75J-1-GP
20.F0736.002
22.10177.721
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN Connector
Y41/Y40
Wednesday, April 12, 2006



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CardBus CB714***

Size	Document Number	Rev
C	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 24 of 44

Cardbus I/F

PCMCIA Socket

ENE Power switch

CBB_D[0..15] 24
CBB_A[0..25] 24
CBB_IORD# 24
CBB_IOWR# 24
CBB_OE# 24
CBB_WE# 24
CBB_REG# 24
CBB_RDY 24
CBB_WP 24
CBB_RESET 24
CBB_WAIT# 24
CBB_INPACK# 24
CBB_CE1# 24
CBB_CE2# 24
CBB_BVD1# 24
CBB_BVD2# 24
CBB_CD1# 24
CBB_CD2# 24
CBB_VS1# 24
CBB_VS2# 24

PCMCIA1
NP1 NP2
CBB_D3 CBB_D4 CBB_D11 CBB_D5 CBB_D12 CBB_D6 CBB_D13 CBB_D7 CBB_D14 CBB_D15
CBB_A10 CBB_A11 CBB_A9 CBB_A8 CBB_A17 CBB_A13 CBB_A18 CBB_A14 CBB_A19 CBB_A20 CBB_A21
CBB_A16 CBB_A22 CBB_A15 CBB_A23 CBB_A12 CBB_A24 CBB_A7 CBB_A25 CBB_A6 CBB_A5 CBB_A4 CBB_A3 CBB_A2 CBB_A1 CBB_A0
CBB_D0 CBB_D8 CBB_D1 CBB_D9 CBB_D2 CBB_D10
CBB_CD1# CBB_CE1# CBB_CE2# CBB_OE# CBB_VS1# CBB_IORD# CBB_IOWR# CBB_WE# CBB_RDY CBB_VS2# CBB_RESET CBB_WAIT# CBB_INPACK# CBB_REG# CBB_BVD2# CBB_BVD1# CBB_WP CBB_CD2#
CARDBUS4519GP-U

VCC_ASKT_S0
C504 SC4D7U10V5ZY-3GP
C505 SC1K1P6V2KX-GP
C506 SCD1U25V3ZY-1GP
VPP_ASKT_S0
C507 SCD1U25V3ZY-1GP
C508 SC4D7U10V5ZY-3GP

Place close to pin 19.
C320 DUMMY-C2

Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

PC1 CARDBUS2519GP-U Y41-SB

47K
C512 SCD01U16V2KX-3GP DY

62.10024.731

5V_S0 3D3V_S0 VCC_ASKT_S0 3D3V_CR_S0
13,14,17,18,19,20,21,27,28,29,30,31,33,34,36,43 5V_S0
3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,26,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0
24 VCC_ASKT_S0
24 3D3V_CR_S0

C342 SC1U10V3ZY-6GP
C341 SCD1U16V2ZY-2GP
C333 SCD1U16V2ZY-2GP
C330 SC1U10V3ZY-6GP
TP99TPAD28
4K7R2J-2-GP R316 AG1-910-01
U36 TPS2211AIDBR-1GP
3.3V 3.3V 5V 5V 12V
SHDN# AVCC AVCC AVCC AVPP OC# GND
2211_SHDN#
VCCD0# VCCD1# VPPD0 VPPD1

C323 SC1U10V3ZY-6GP
C332 SCD1U16V2ZY-2GP
C331 SCD1U16V2ZY-2GP

CARD1 MEMCARD-21P-1-GP
SD_VCC MS_VCC SD_DAT0 SD_DAT1 SD_DAT2 SD_DAT3 SD_CLK SD_CMD SD_WP_SW SD_CD_SW NP1 NP2 NP3
MS_DATA0 MS_DATA1 MS_DATA2 MS_DATA3 MS_BS MS_INS MS_SCLK SD_GND SD_GND MS_GND MS_GND GND GND

SM-XDDATA7_SDDAT0_XD-17P SD-D0_SD-7P
SM-XDDATA0_SDDAT1_XD-10P SD-D1_SD-8P
SM-XDCLE_SDDAT2_XD-5P SD-D2_SD-9P
SM-XDDATA4_SDDAT3_XD-14P SD-D3_SD-1P
SM-XDALE_SDCMD_XD-6P SD-CLK_SD-5P SD-CMD_SD-2P
SM-XDWPD#_SDWP SD-WP
0R0402-PAD R462 R459 R473 R470 R468 R338
TP123 TPAD28

MS-D0_MS-4P MS-D1_MS-3P MS-D2_MS-5P MS-D3_MS-7P MS-BS_MS-2P MS-CLK_MS-8P
R465 R464 R466 R467 R463 0R0402-PAD
SM-XDDATA2_MSDATA0_XD-12P SM-XDDATA6_MSDATA1_XD-16P SM-XDDATA5_MSDATA2_XD-15P SM-XDDATA3_MSDATA3_XD-13P SM-XDDATA1_MSBS_XD-11P SM-INS#_MS-6P
R537 0R2J-2-GP SD-SW_SDCD# SM-SW_SDCD#

Cardreader P/N:20.I0033.011

SB
R345 R344 R343 R472 R469 R302 10KR2J-3-GP 2K2R2F-GP 43KR2J-GP
DY
SM-XDBSY#_XD-2P SM-XDRE#_MSCLK_XD-3P SM-XDCE#_XD-4P SM-XDCLE_SDDAT2_XD-5P SM-XDALE_SDCMD_XD-6P SM-XDWE#_SDCLK_XD-7P SM-XDDATA7_SDDAT0_XD-17P SM-XDDATA4_SDDAT3_XD-14P SM-XDDATA0_SDDAT1_XD-10P
R461 R471 R460 43KR2J-GP
SM-XDWP#_XD-8P
R342 2K2R2F-GP

Placement: Close Chip
SD-CLK_SD-5P MS-CLK_MS-8P
R323 R324 22R2J-2-GP
SM-XDWE#_SDCLK_XD-7P SM-XDRE#_MSCLK_XD-3P
R308 R312 0R2J-2-GP
Placement: Close Socket
C327 C336 SC10P50V2JN-4GP

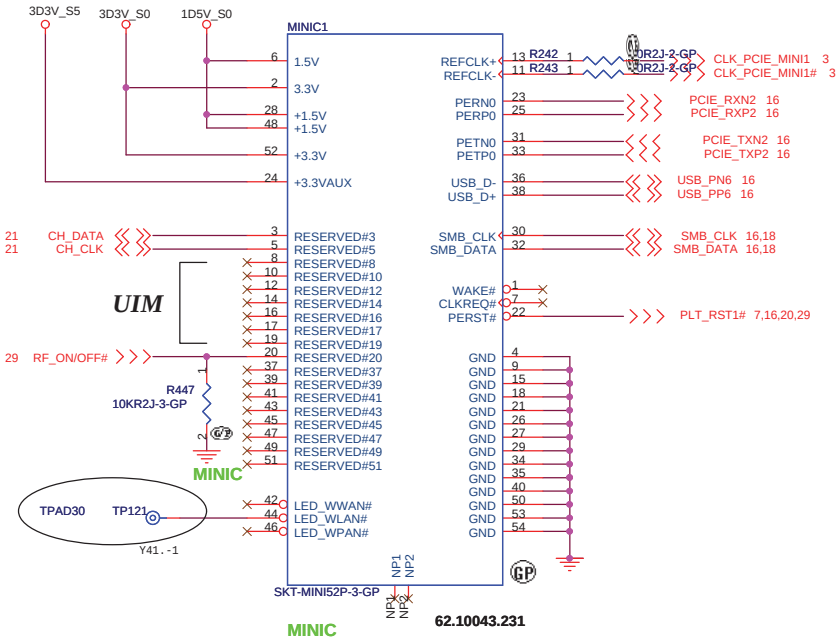
POWER SWITCH
U33 AAT4250IGV-T1-GP
OUT GND NC#3 IN ON/OFF#
C319 SCD1U16V2ZY-2GP
C312 SC1U10V3ZY-6GP
R286 10KR2J-3-GP
R279 43KR2J-GP
2N7002-8-GP Q18
SM_XDPWREN#/MSPWREN#
SDPWREN33#
74.04250.A3F

<Variant Name>

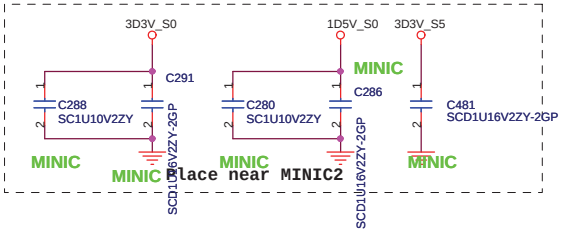
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA/CardReader
Size: A3
Document Number: Y41/Y40
Rev: -1
Date: Wednesday, April 12, 2006
Sheet 25 of 44

Mini Card Connector



Change part to P/N:62.10043.241



3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,27,29,31,32,33,34,36,38,39,41,43 3D3V_S0

13,16,17,18,21,22,29,33,34,38 3D3V_S5

24,25 3D3V_CR_S0

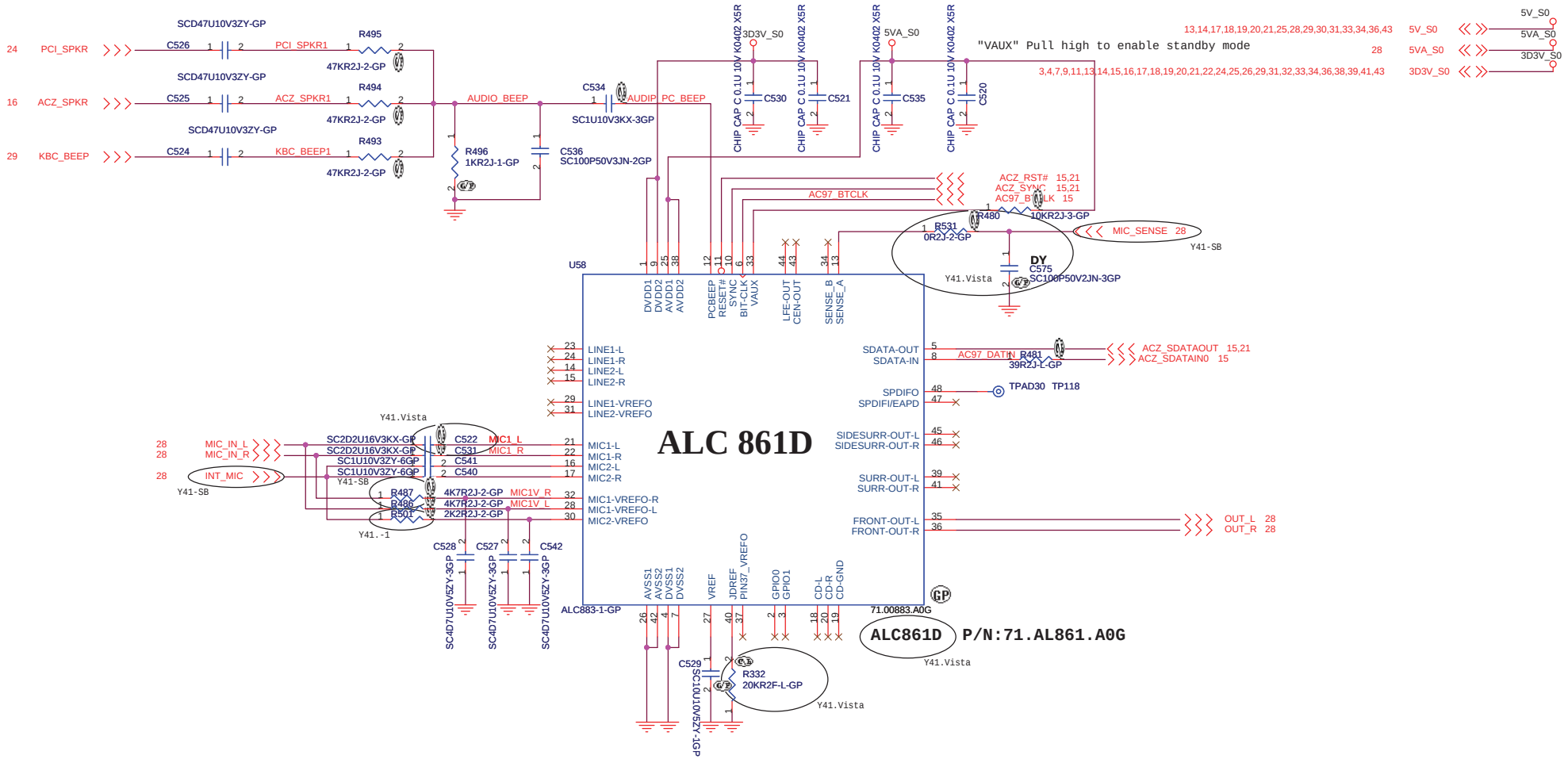
5,9,16,17,41,43 1D5V_S0

3D3V_S0
3D3V_S5
3D3V_CR_S0
1D5V_S0

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINI CARD		
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 26 of 44	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input

<Variant Name>

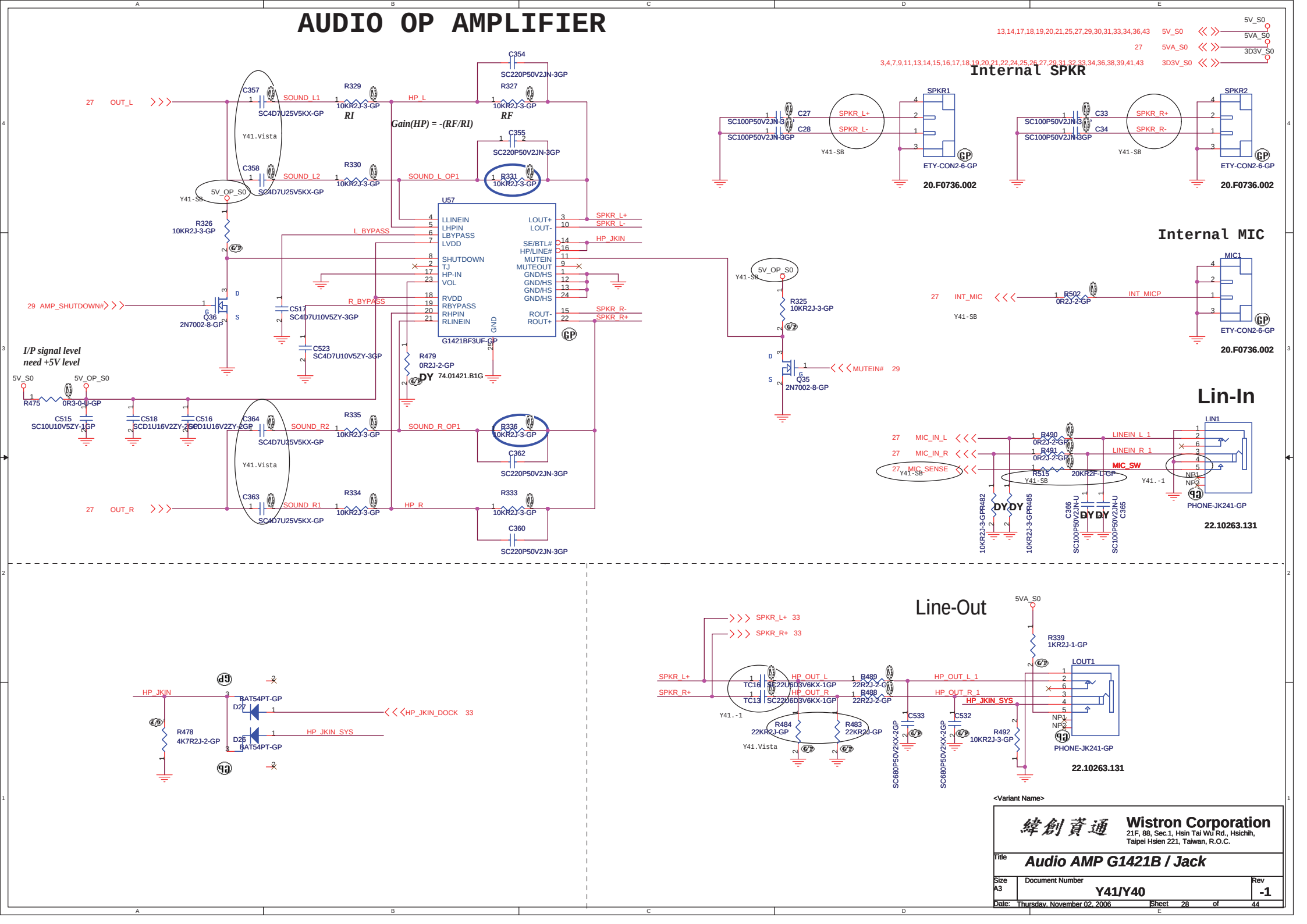
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC861**

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Thursday, November 02, 2006 | Sheet 27 of 44

AUDIO OP AMPLIFIER



Internal SPKR

Internal MIC

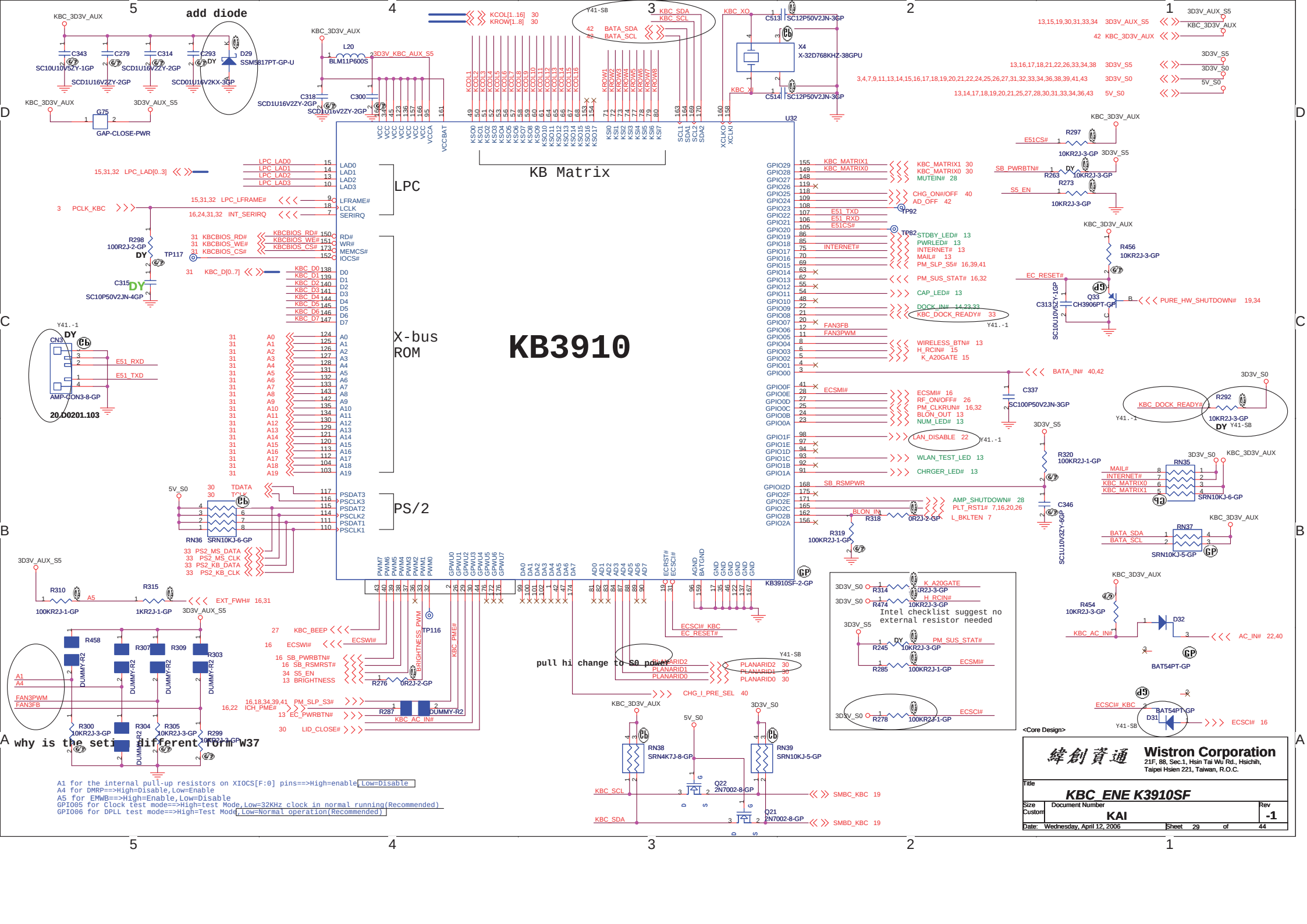
Lin-In

Line-Out

<Variant Name>

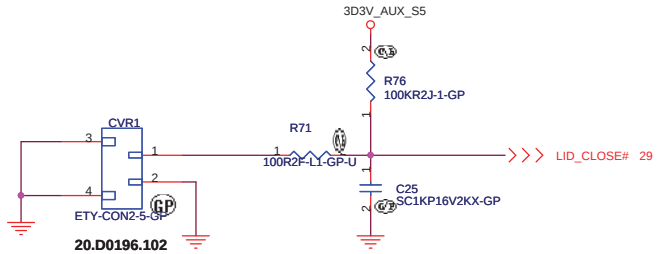
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Audio AMP G1421B / Jack***	
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Thursday, November 02, 2006	Sheet 28 of 44	


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
add diode
pull hi change to S0 power
why is the seti different form W37
Intel checklist suggest no external resistor needed
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=Test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC_ENE K3910SF
KAI
-1
Wednesday, April 12, 2006
29
44

Internal KeyBoard Connector

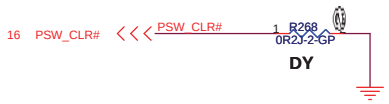
COVER SWITCH

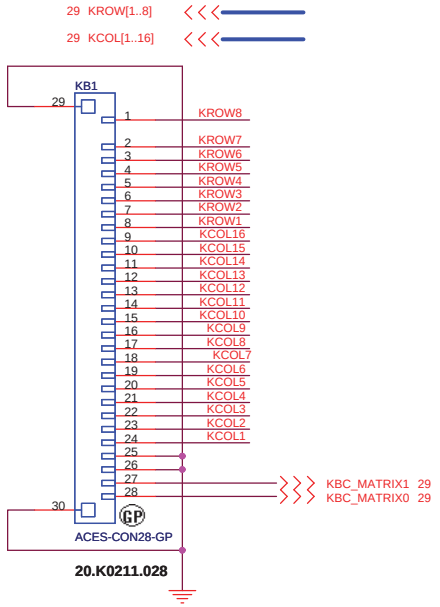


Keyboard matrix (from vendor)

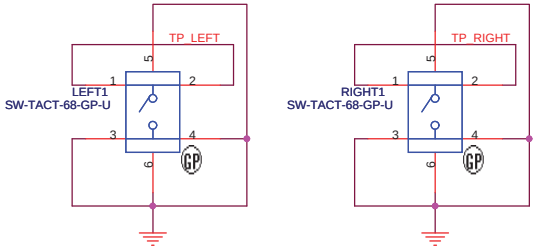
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON

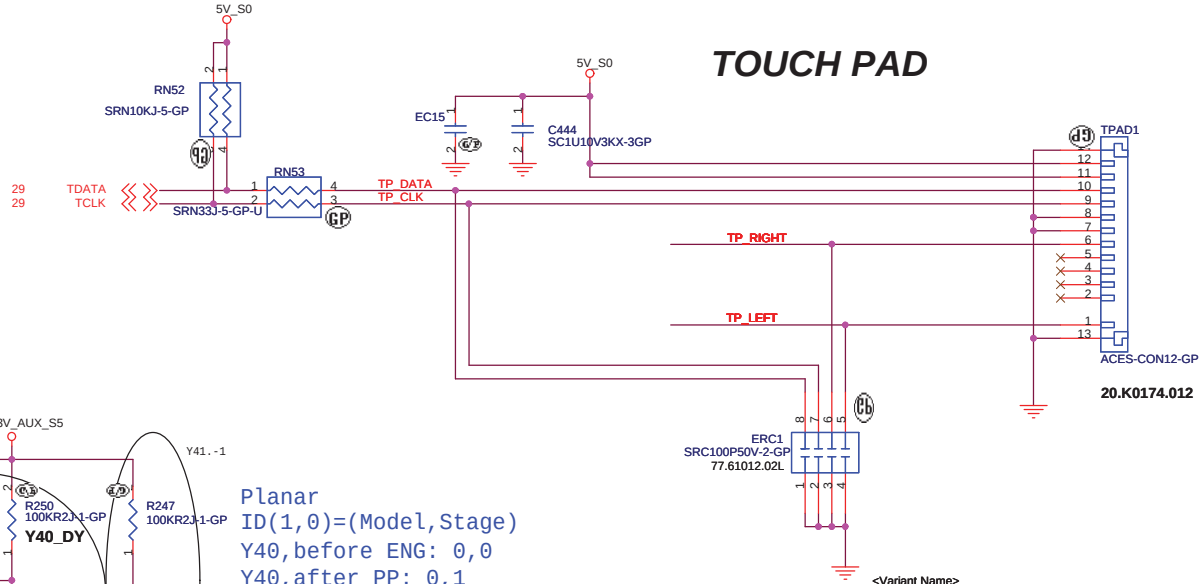


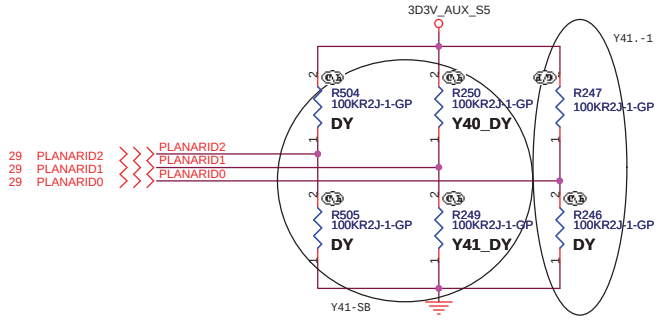


SCROLL KEY



TOUCH PAD





Planar
ID(1,0)=(Model,Stage)
Y40,before ENG: 0,0
Y40,after PP: 0,1
Y41,before ENG: 1,0
Y41,after PP: 1,1

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

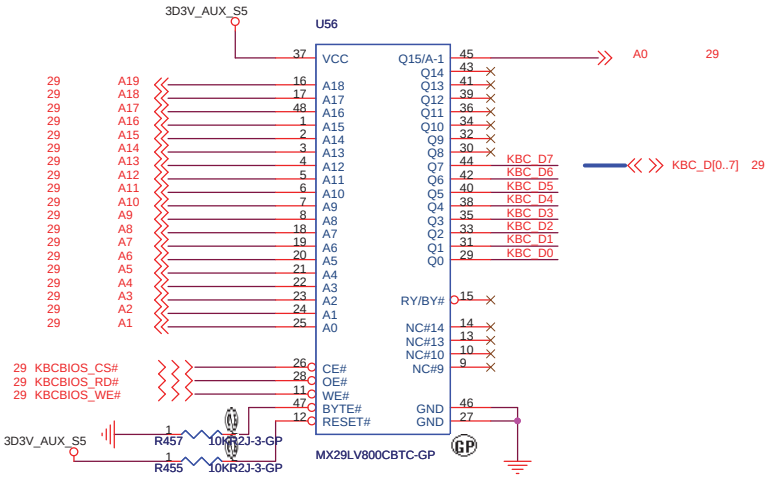
Title: KEYBOARD/TOUCHPAD

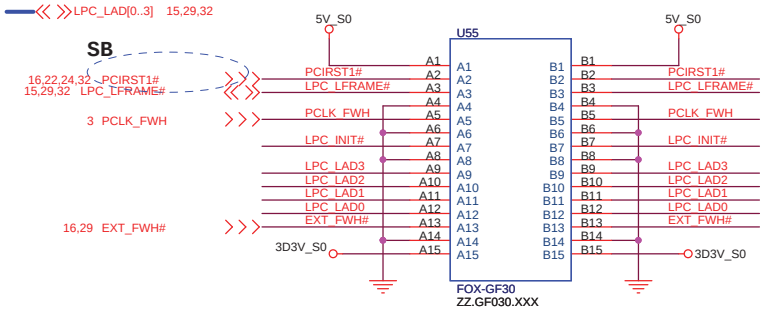
Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 30 of 44

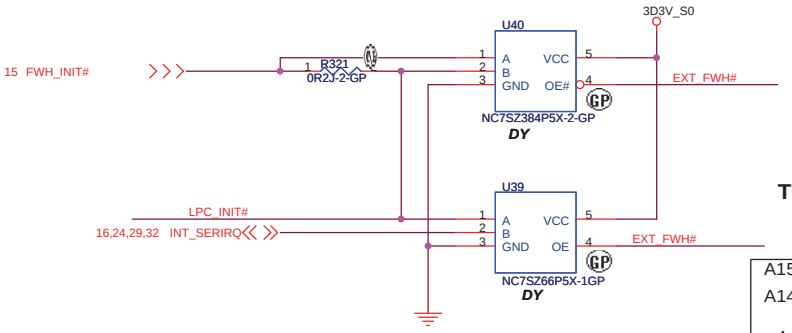
5V_S0
13,14,17,18,19,20,21,25,27,28,29,30,33,34,36,43 5V_S0 3D3V_S5
13,16,17,18,21,22,26,29,33,34,38 3D3V_S5 3D3V_S0
3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,32,33,34,36,38,39,41,43 3D3V_S0 3D3V_AUX_S5
13,15,19,29,30,33,34 3D3V_AUX_S5

GOLDEN FINGER FOR DEBUG BOARD





Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

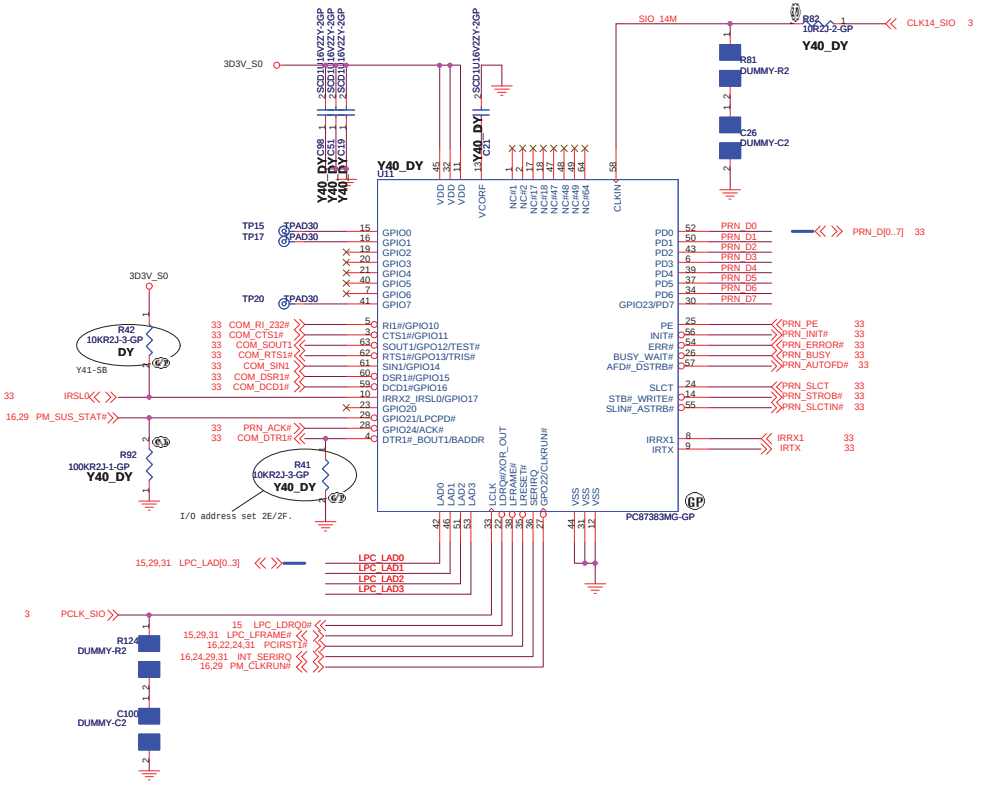
(BOTTOM VIEW)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BIOS : SPI/Debug***

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 31 of 44



3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,33,34,36,38,39,41,43

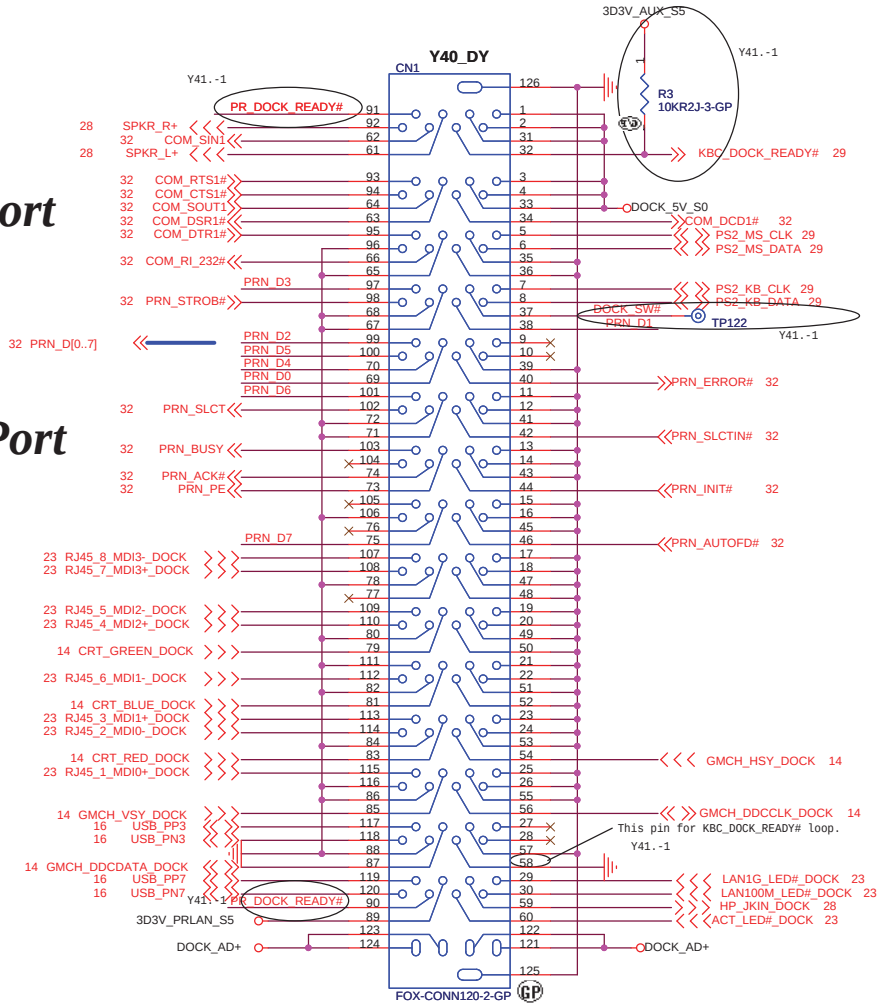
3D3V_S0

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIO PC87383-VS***	
Size C	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 32 of 44	

Serial Port

Printer Port



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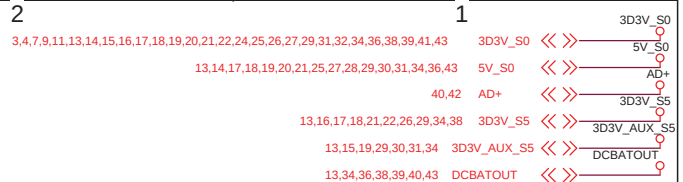
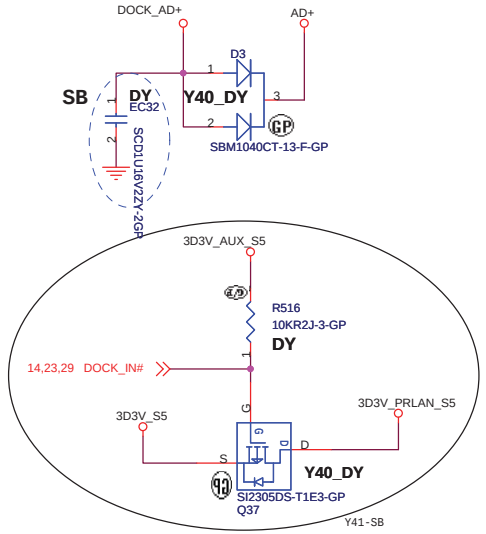
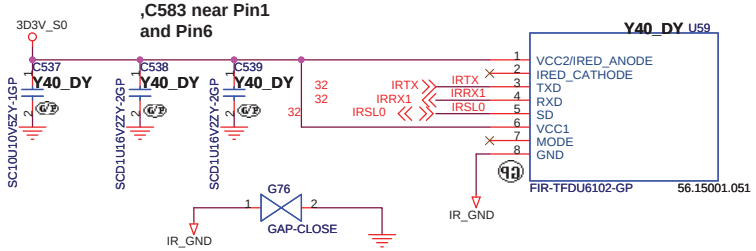


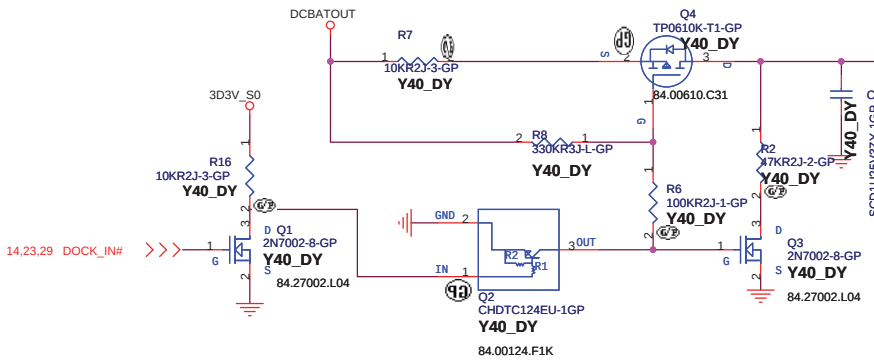


VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

Place C581 ,C583 near Pin1 and Pin6





<Variant Name>

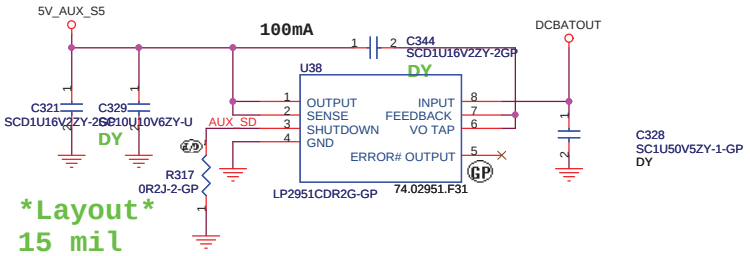
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

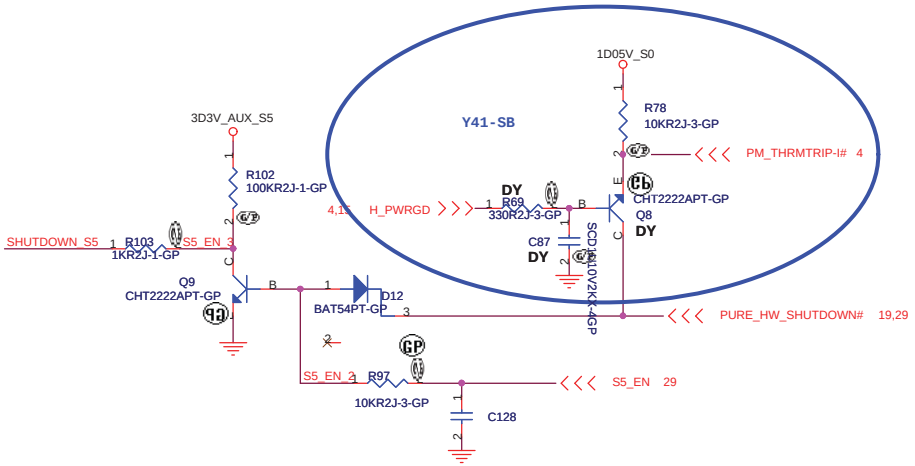
Title: **Port Replicator/FIR**

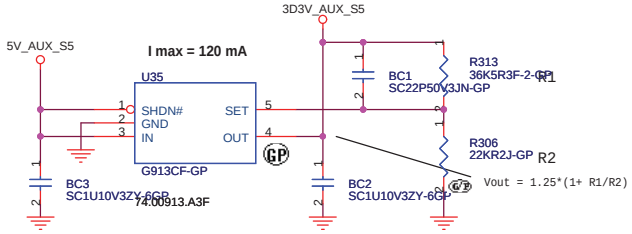
Size	Document Number	Rev
A3	Y41/Y40	-1

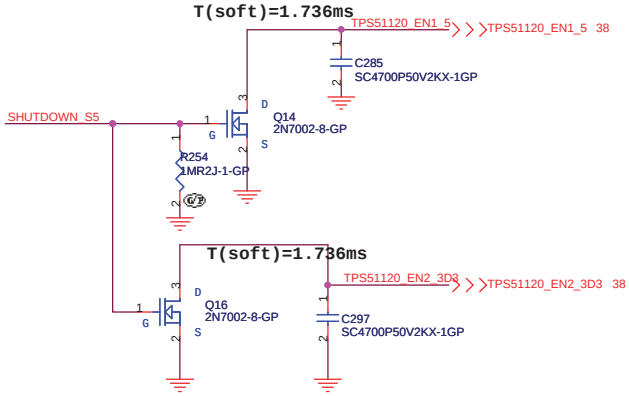
Date: Friday, May 26, 2006 Sheet 33 of 44

Aux Power

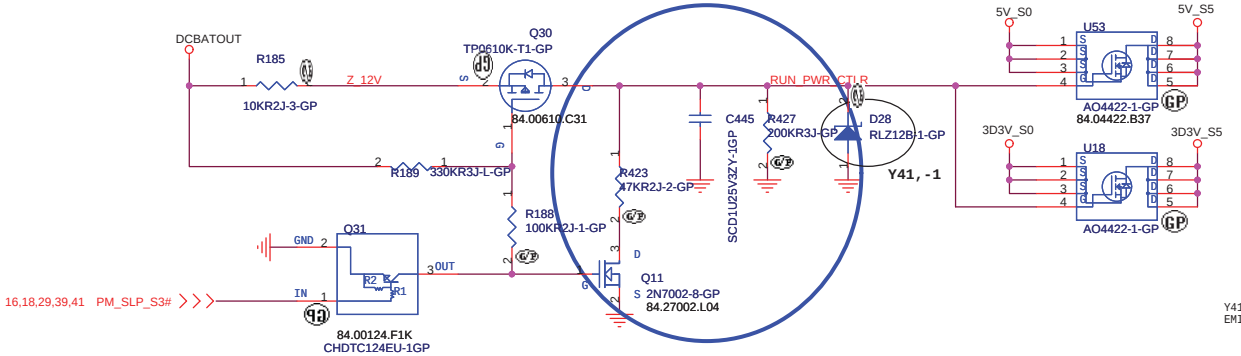


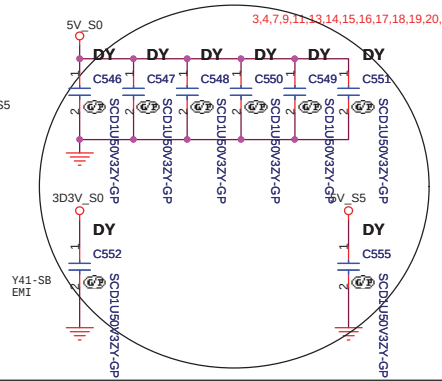


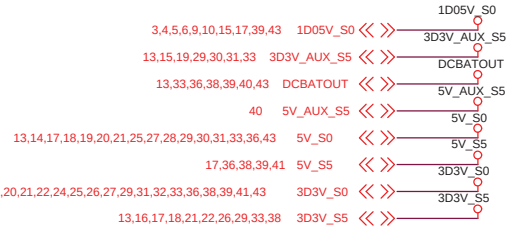




Run Power







<Variant Name>

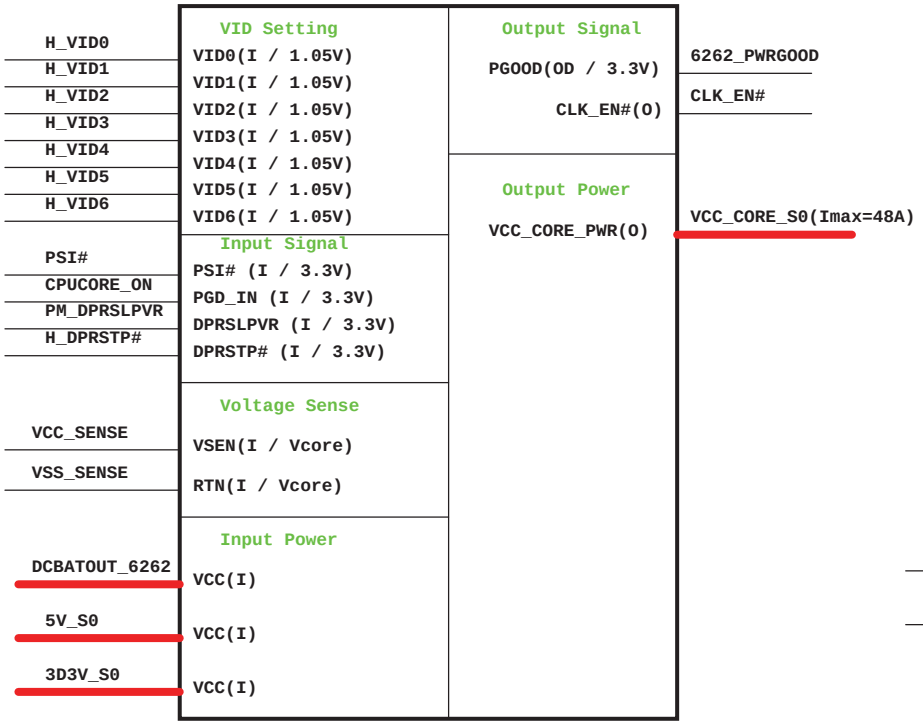
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN and AUX POWER**

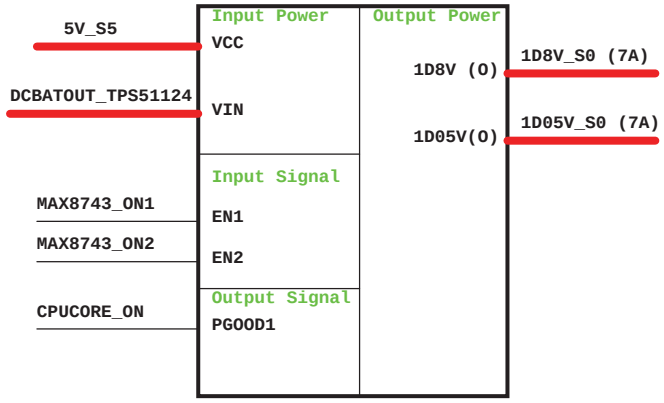
Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Wednesday, April 12, 2006 Sheet 34 of 44

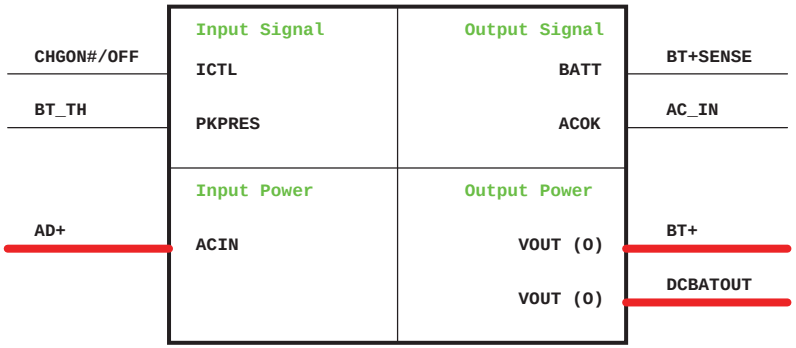
CPU_CORE
Intersil ISL6262



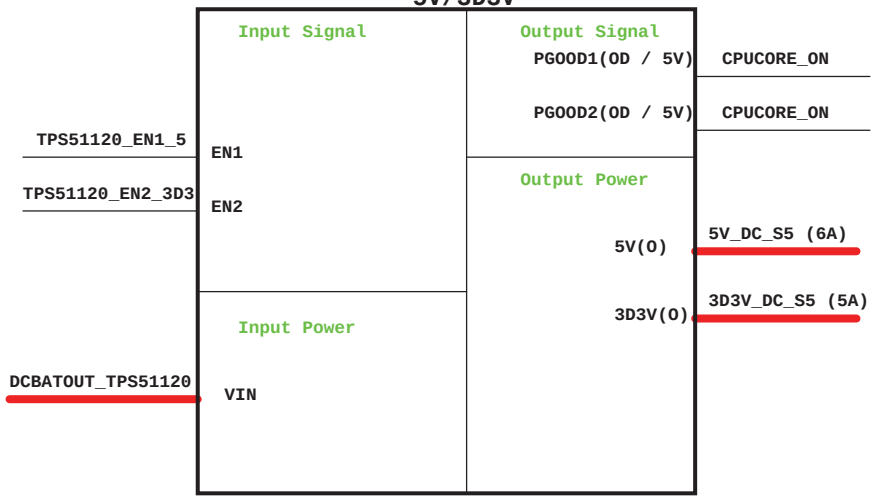
MAX8743
1D8V/1D05V



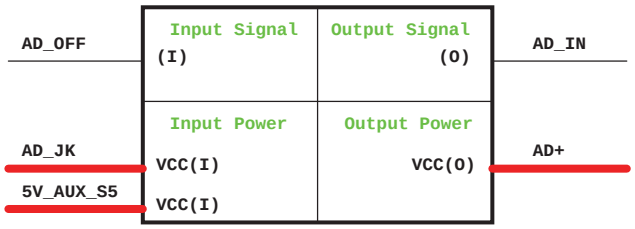
Charger Max8725



TPS51120
5V/3D3V



Adapter



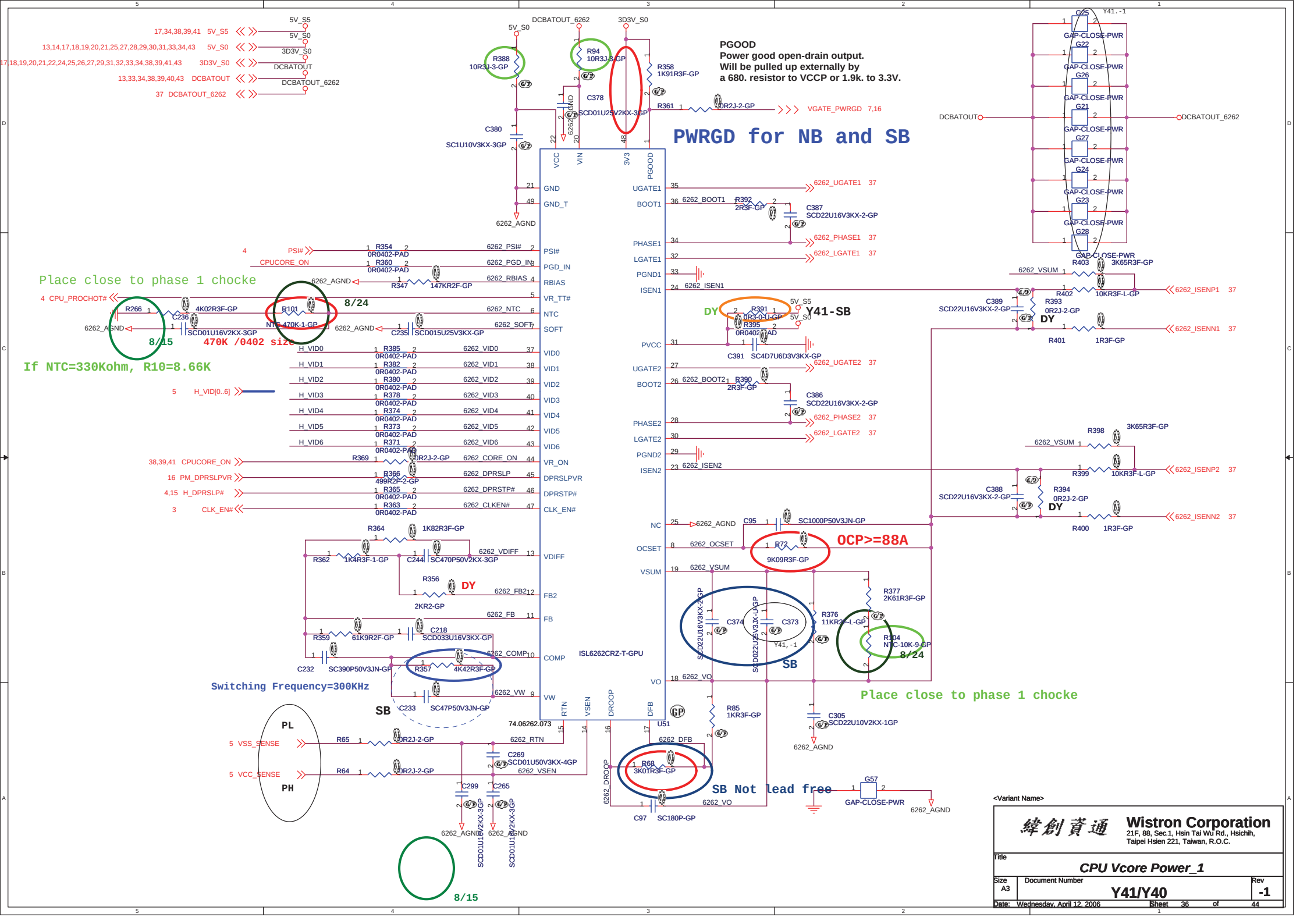
<Variant Name>

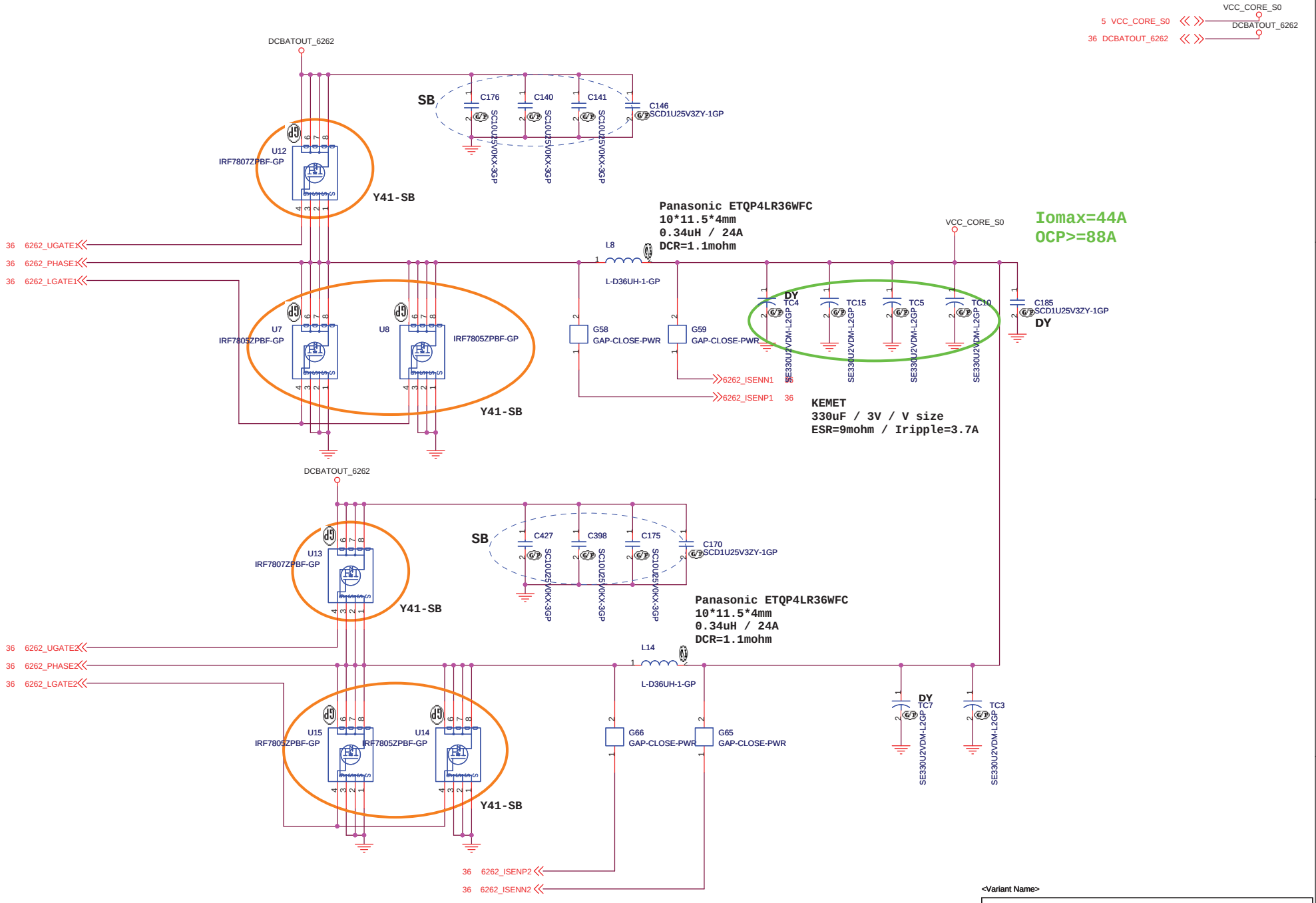
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Friday, April 07, 2006 Sheet 35 of 44


PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
PWRGD for NB and SB
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
8/24
8/15
470K /0402 size
Y41-SB
DY
OCP>=88A
SB
SB Not lead free
Switching Frequency=300KHz
ISL6262CRZ-T-GPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
Y41/Y40
Date: Wednesday, April 12, 2006
Sheet 36 of 44



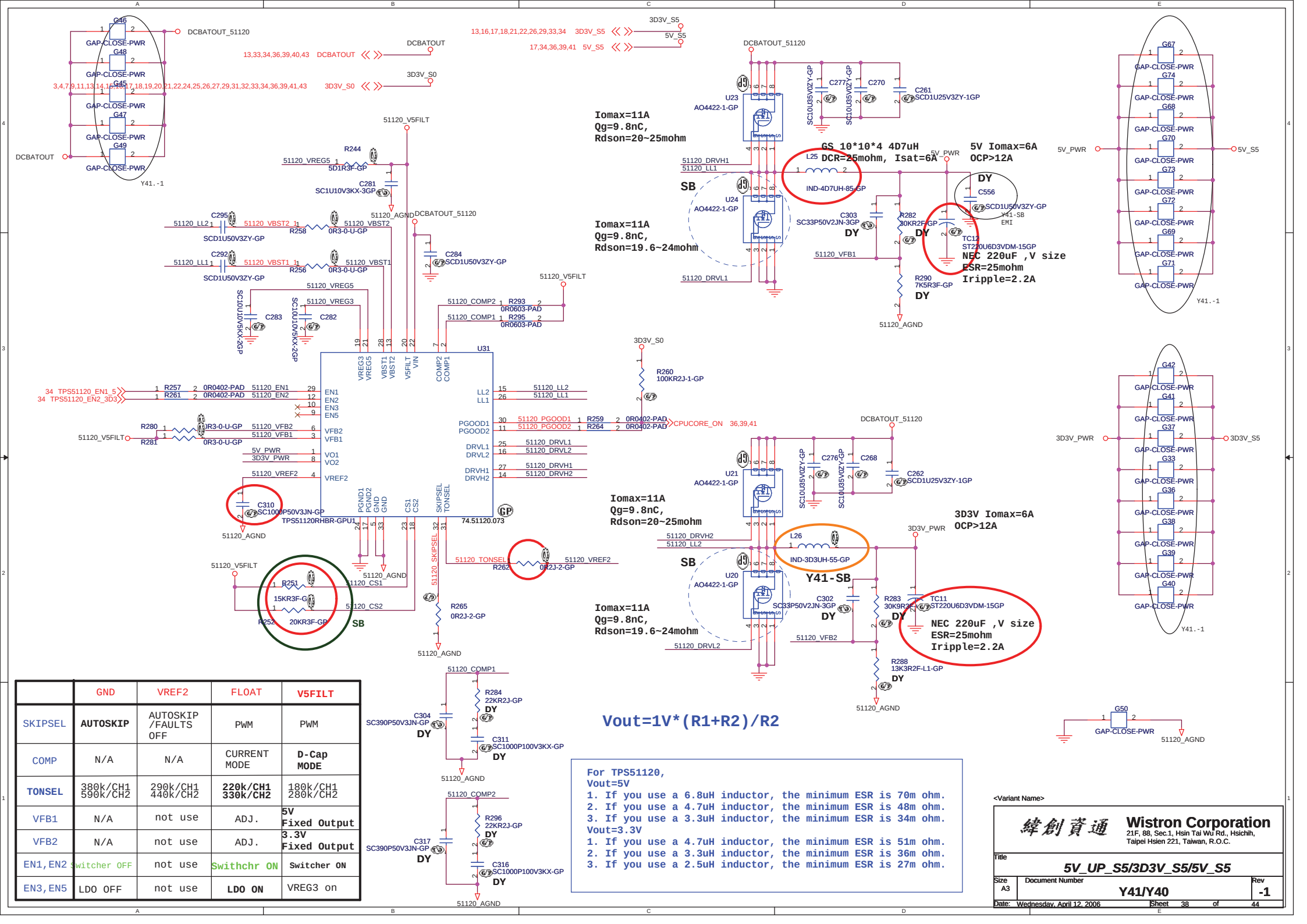
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU Vcore Power_2***

Size	Document Number	Rev
A3	**Y41/Y40**	-1

Date: Wednesday, April 12, 2006 Sheet 37 of 44



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

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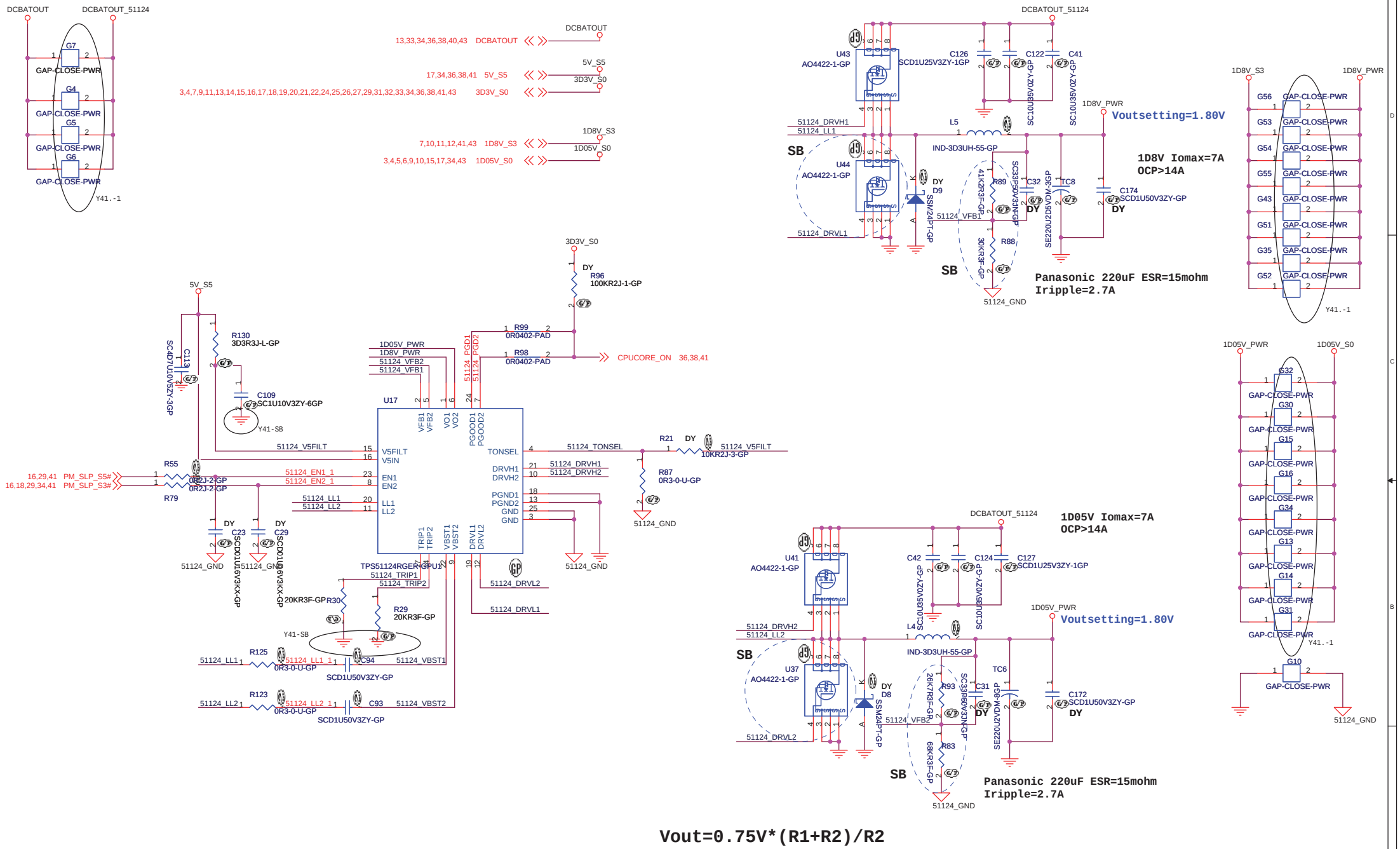
<variant_name>

Title: 5V_UP_S5/3D3V_S5/5V_S5

Size: A3 | Document Number: Y41/Y40 | Rev: -1

Date: Wednesday, April 12, 2006 | Sheet 38 of 44



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

<Variant Name>

緯創資通 Wistron Corporation
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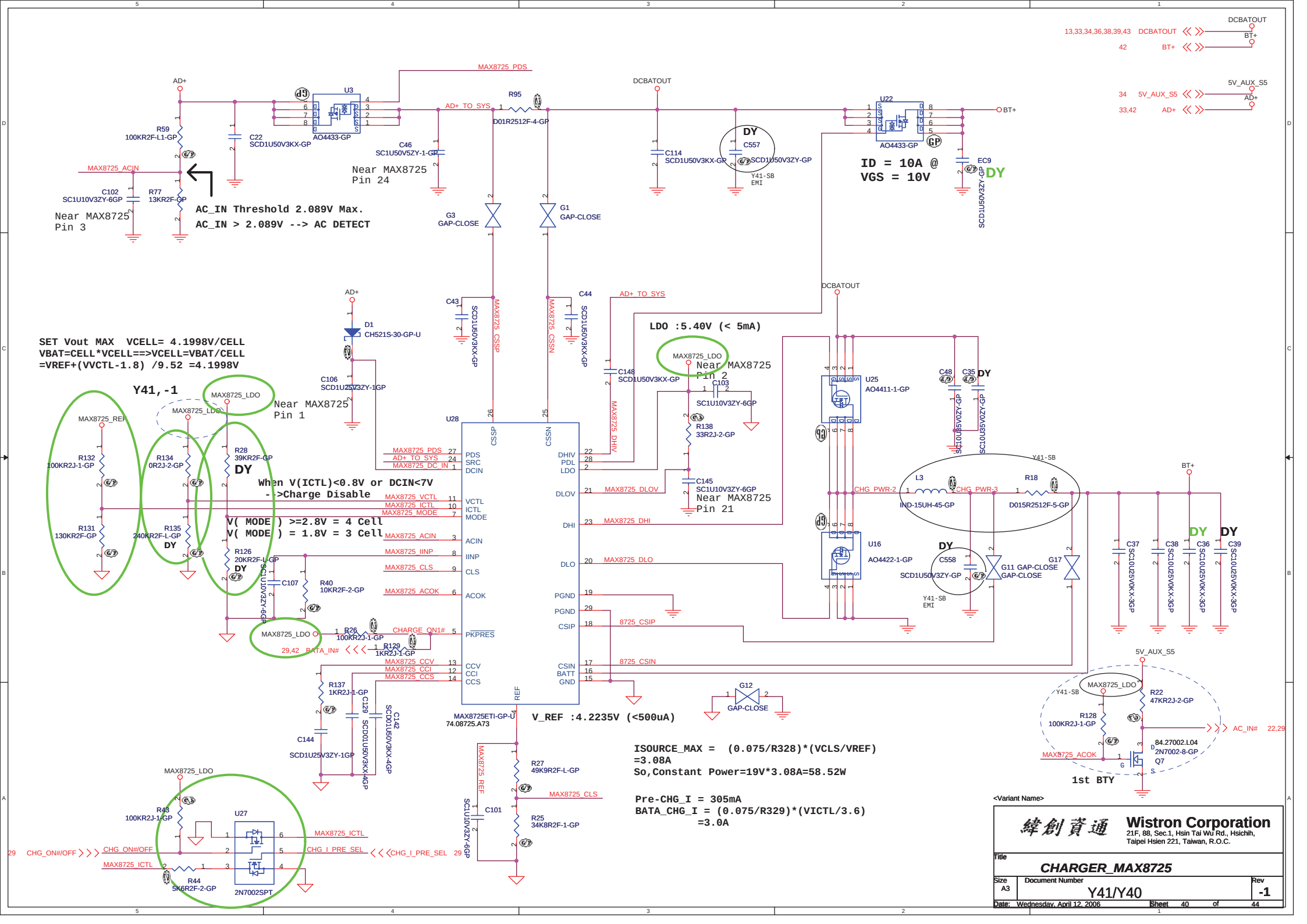
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size	Document Number	Rev
A3	Y41/Y40	-1

Date: Friday, May 26, 2006 Sheet 39 of 44


DCBATOUT
13,33,34,36,38,39,43 DCBATOUT
BT+
42 BT+
5V_AUX_S5
34 5V_AUX_S5
AD+
33,42 AD+
MAX8725_PDS
AD+_TO_SYS
R95
D01R2512F-4-GP
U3
AO4433-GP
R59
100KR2F-L1-GP
C22
SCD1U50V3KX-GP
C46
SC1U50V5ZY-1-GP
Near MAX8725
Pin 24
C114
SCD1U50V3KX-GP
DY
C557
SCD1U50V3ZY-GP
Y41-SB
EMI
U22
AO4433-GP
ID = 10A @
VGS = 10V
EC9
SCD1U50V3ZY-GP
MAX8725_ACIN
C102
SC1U10V3ZY-6GP
R77
13KR2F-GP
Near MAX8725
Pin 3
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
G3
GAP-CLOSE
G1
GAP-CLOSE
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
Y41,-1
MAX8725_LDO
Near MAX8725
Pin 1
MAX8725_REF
R132
100KR2J-1-GP
R134
0R2J-2-GP
R131
130KR2F-GP
R135
240KR2F-L-GP
DY
R28
39KR2F-GP
DY
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
R126
20KR2F-L-GP
DY
C107
SC1U10V3ZY-6GP
R40
10KR2F-2-GP
D1
CH521S-30-GP-U
C106
SCD1U25V3ZY-1GP
C43
SCD1U50V3KX-GP
C44
SCD1U50V3KX-GP
MAX8725_CSSP
MAX8725_CSSN
U28
CSSP
CSSN
MAX8725_PDS 27
AD+_TO_SYS 24
MAX8725_DC_IN 1
PDS
SRC
DCIN
MAX8725_VCTL 11
MAX8725_ICTL 10
MAX8725_MODE 7
VCTL
ICTL
MODE
MAX8725_ACIN 3
ACIN
MAX8725_IINP 8
IINP
MAX8725_CLS 9
CLS
MAX8725_ACOK 6
ACOK
PKPRES
MAX8725_CCV 13
MAX8725_CCI 12
MAX8725_CCS 14
CCV
CCI
CCS
REF
DHIV 22
PDL 28
LDO 2
DLOV 21
DHI 23
DLO 20
PGND 19
PGND 29
CSIP 18
CSIN 16
BATT 15
GND 17
MAX8725_DHIV
MAX8725_DLOV
MAX8725_DHI
MAX8725_DLO
8725_CSIP
8725_CSIN
MAX8725ETI-GP-U
74.08725.A73
V_REF :4.2235V (<500uA)
LDO :5.40V (< 5mA)
MAX8725_LDO
Near MAX8725
Pin 2
C148
SCD1U50V3KX-GP
C103
SC1U10V3ZY-6GP
R138
33R2J-2-GP
C145
SC1U10V3ZY-6GP
Near MAX8725
Pin 21
U25
AO4411-1-GP
C48
C35
DY
SC10U35V0ZY-GP
SC10U35V0ZY-GP
Y41-SB
L3
IND-15UH-45-GP
CHG_PWR-2
CHG_PWR-3
R18
D015R2512F-5-GP
U16
AO4422-1-GP
DY
C558
SCD1U50V3ZY-GP
Y41-SB
EMI
G11 GAP-CLOSE
GAP-CLOSE
G17
C37
C38
C36
DY
C39
DY
SC1U25V0KX-3GP
R26
100KR2J-1-GP
CHARGE_ON1#
R129
1KR2J-1-GP
29,42 BATA_IN#
R137
1KR2J-1-GP
C129
SCD01U50V3KX-4GP
C142
C144
SCD1U25V3ZY-1GP
G12
GAP-CLOSE
ISOURCE_MAX = (0.075/R328)*(VCLS/VREF)
=3.08A
So,Constant Power=19V*3.08A=58.52W
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R329)*(VICTL/3.6)
=3.0A
R27
49K9R2F-L-GP
MAX8725_CLS
R25
34K8R2F-1-GP
C101
SC1U10V3ZY-6GP
MAX8725_REF
MAX8725_LDO
R43
100KR2J-1-GP
U27
MAX8725_ICTL
CHG_ON#/OFF
CHG_I_PRE_SEL
29 CHG_ON#/OFF
CHG_I_PRE_SEL 29
R44
5K6R2F-2-GP
2N7002SPT
5V_AUX_S5
Y41-SB
MAX8725_LDO
R22
47KR2J-2-GP
R128
100KR2J-1-GP
AC_IN# 22,29
MAX8725_ACOK
84.27002.L04
2N7002-8-GP
Q7
1st BTY
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER_MAX8725
Size A3
Document Number
Y41/Y40
Rev -1
Date: Wednesday, April 12, 2006
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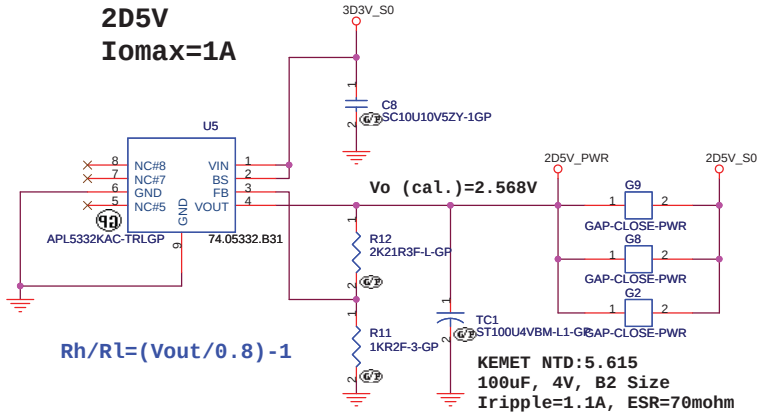
2D5V
Iomax=1A



1D5V_S0
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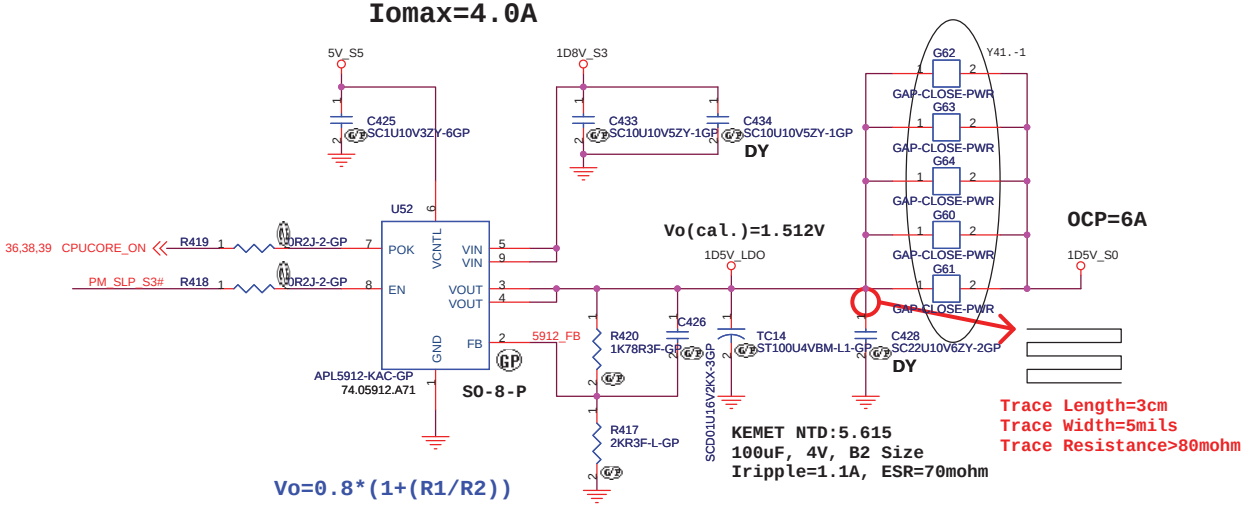

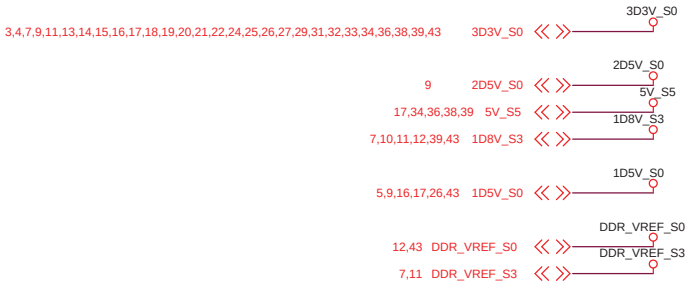

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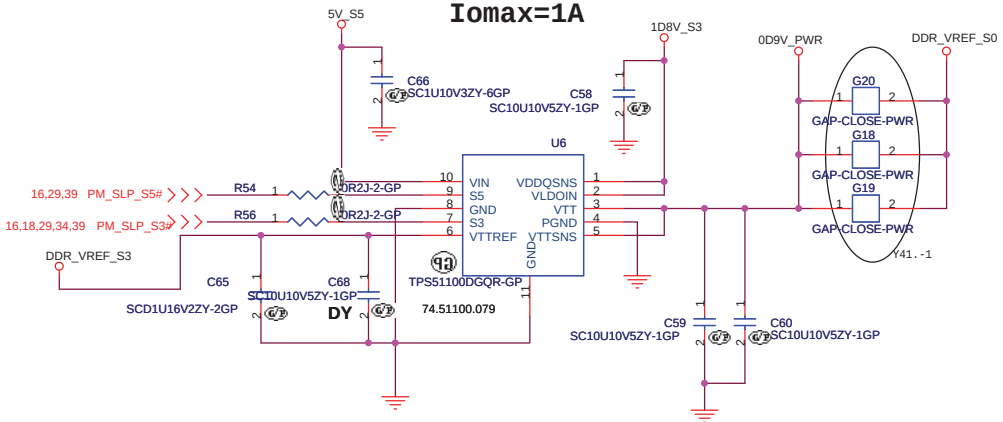
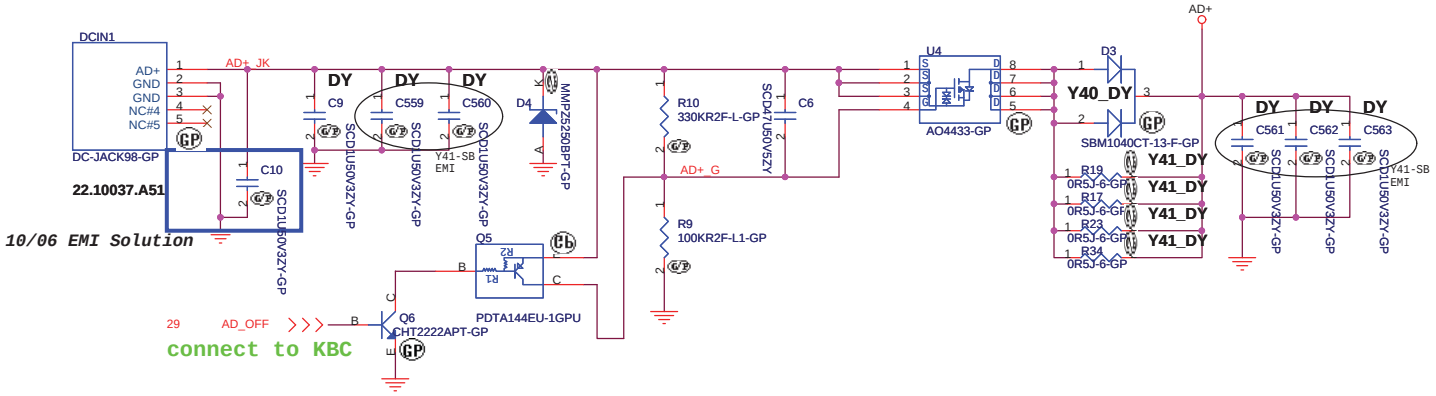


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

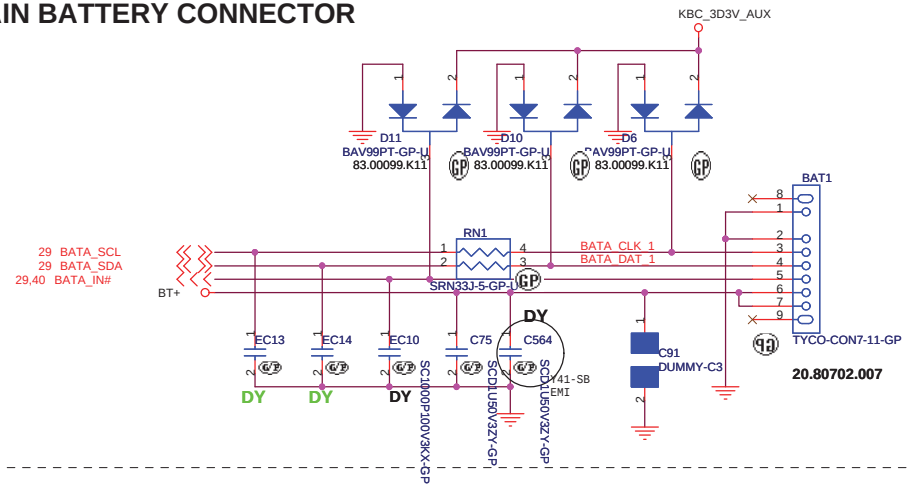
Title	0D9V/1D5V/2D5V	
Size A3	Document Number Y41/Y40	Rev -1
Date: Wednesday, April 12, 2006	Sheet 41 of 44	

ADAPTER IN CIRCUIT



33,40 AD+
29 KBC_3D3V_AUX
40 BT+

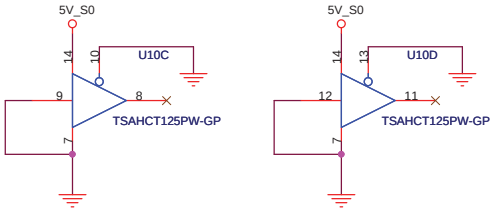
MAIN BATTERY CONNECTOR



<Variant Name>

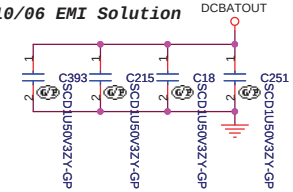
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

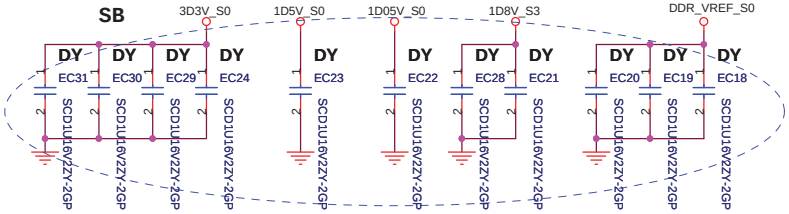
Title	***AD/BATT CONN***	
Size A3	Document Number Y41/Y40	Rev -1
Date: Wednesday, April 12, 2006	Sheet 42 of 44	

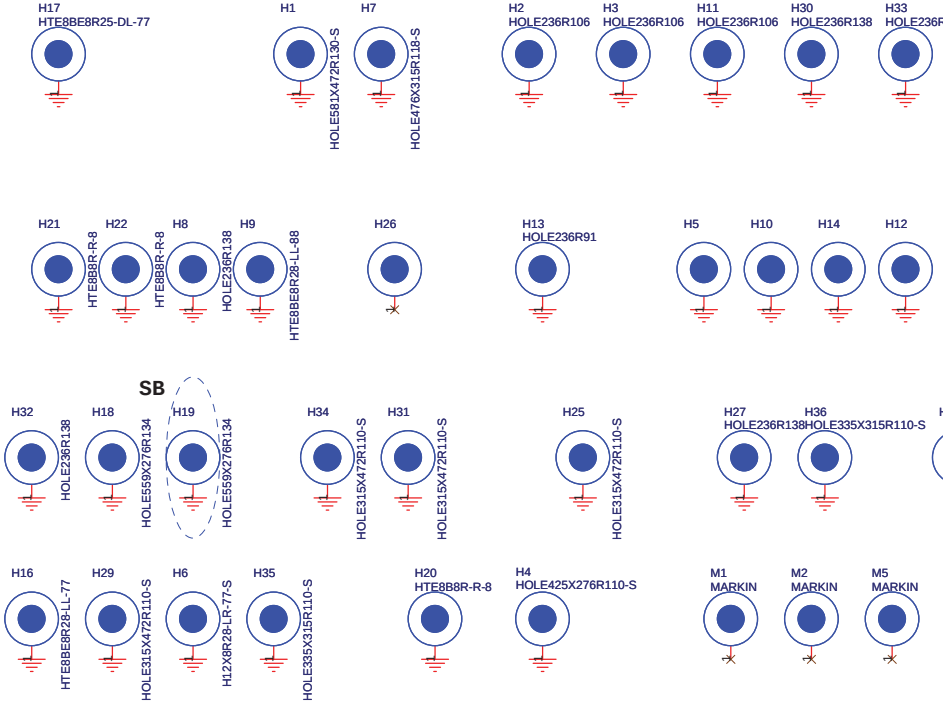


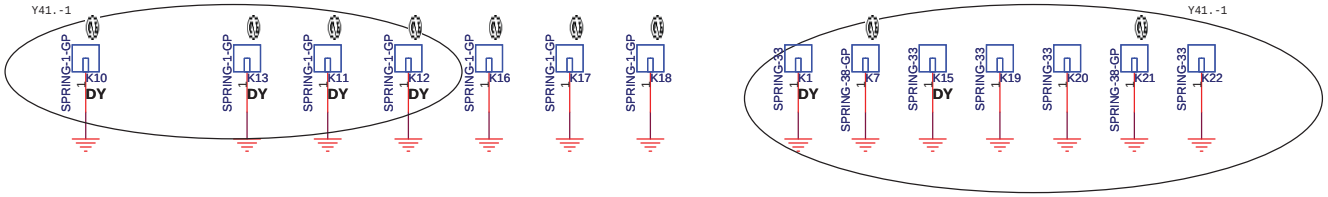
3,4,7,9,11,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,31,32,33,34,36,38,39,41 3D3V_S0 — 3D3V_S0
13,14,17,18,19,20,21,25,27,28,29,30,31,33,34,36 5V_S0 — 5V_S0
13,33,34,36,38,39,40 DCBATOUT — DCBATOUT
7,10,11,12,39,41 1D8V_S3 — 1D8V_S3
3,4,5,6,9,10,15,17,34,39 1D05V_S0 — 1D05V_S0
5,9,16,17,26,41 1D5V_S0 — 1D5V_S0
12,41 DDR_VREF_S0 — DDR_VREF_S0

10/06 EMI Solution









<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SPRING & BOSS & EMI***	
Size A3	Document Number **Y41/Y40**	Rev **-1**
Date: Wednesday, April 12, 2006	Sheet 43 of 44	

PRT modification list for Layout:

MINIC1, 62.10043.241
CDROM1, 20.80338.050
CN1, 20.80591.120
U9, 62.10079.001
U45, 71.88055.A03
U58, 71.AL861.00G

PRT modification list for Y41/Y41 BOM:

FAN1, 20.F0714.003
MINIC1, 62.10043.241
LAUNCH1, 20.K0196.005
U36, 74.02211.B39
U45, 71.88055.A03
U58, 71.AL861.00G
XF1, 68.2410S.30B
D2,D3 83.10R04.E87(Y41)
U50, 71.945GM.B0U
U29, 71.ICH7M.C0U
LCD1, 20.F0853.040
C6, 78.47494.41L
C280,C288, 78.10593.4FL
78.10221.2F1 <> 78.10221.2FL

H32, 34.46I14.001
H27, 34.46I14.001
H18, 34.46I14.001
H14, 34.4B604.001
H10, 34.4B604.001
H30, 34.4B601.001
H33, 34.4B601.001
H5, 34.4B602.001
H8, 34.4B603.001

Del K2~K6,K8,K9

Change parts to meet vista as below:
78.22521.5BL; 2.2uF 16V 0603 X5R; C522,C531.(Original:78.10593.4BL,1uF)
78.47521.51L(SCH放78.47522.51L); 4.7uF 16V 0805 X5R; C363,C364,C357,C358.(Original:78.22591.41L,2.2uF)
63.22334.1DL; 22K Ohm F 0402; R483,R484.(Original:63.10234.1DL,1K Ohm)
C575 Dummy.(Original:78.10134.1FL,100pF)
64.20025.6DL; 20K Ohm F 0402; R332.(Original:64.51015.6DL,5.1K Ohm)
63.R0034.1DL; 0 Ohm J 0402; R531.(Original:63.47034.1DL,47 Ohm)
71.AL861.A0G; ALC861-VD; U58.(Original:71.AL861.00G,ALC861)

Daughter Board information:

LAUNCH/B Layout Revision: 05572-1.
LAUNCH/B PCB P/N: 48.4P502.011

USB/B Layout Revision: 05573-1.
USB/B PCB P/N: 48.4P503.011

Port Replicator/B Layout Revision: 05579-1.
Port replicator/B PCB P/N: 48.4P504.011

Key part list:

Modification list:

<Variant Name>

緯創資通 Wistron Corporation
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Title: *Remark*

Size: A3 | Document Number: Y41/Y40 | Rev: -1

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