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22	PCH(3)_SYS PWR CONTR		52	X		82	X	
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25	PCH(6)_CPU,GPIO,MISC		55	VA and VCCRTC				
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27	PCH(8)_VCCIN_AUX_Decoupling		57	eDP connector				
28	Power Monitor		58	Silego Controller				
29	Type-C Debug		59	+5VSB & +3P3VSB				
30	Touch Con & Key		60	+1P2V_DUAL&++0P6V_DDR_VDDQ				

CAD Note:

Property: BUILD-OPT
DNP = Do Not Place

DBG_S – Replace with board short for MP
DBG_R – Replace with lower cost component for MP
DBG_N – Install for Non-Debug Builds
DBG_D – Remove from BOM (Depopulate) for MP
DBG_T – Used for Telemetry in MP as needed
DBG_TS – Used for Telemetry in MP as needed. This part needs to be replaced with a short if telemetry is not needed.

<Variant Name>

Title:	Table of Contents	
Engineer:	<OrgAddr1>	
Size: A3	Project Name: EDAN_A_EV1	Rev: <RevCode>
Date: Tuesday, May 21, 2019	Sheet 1 of 82	

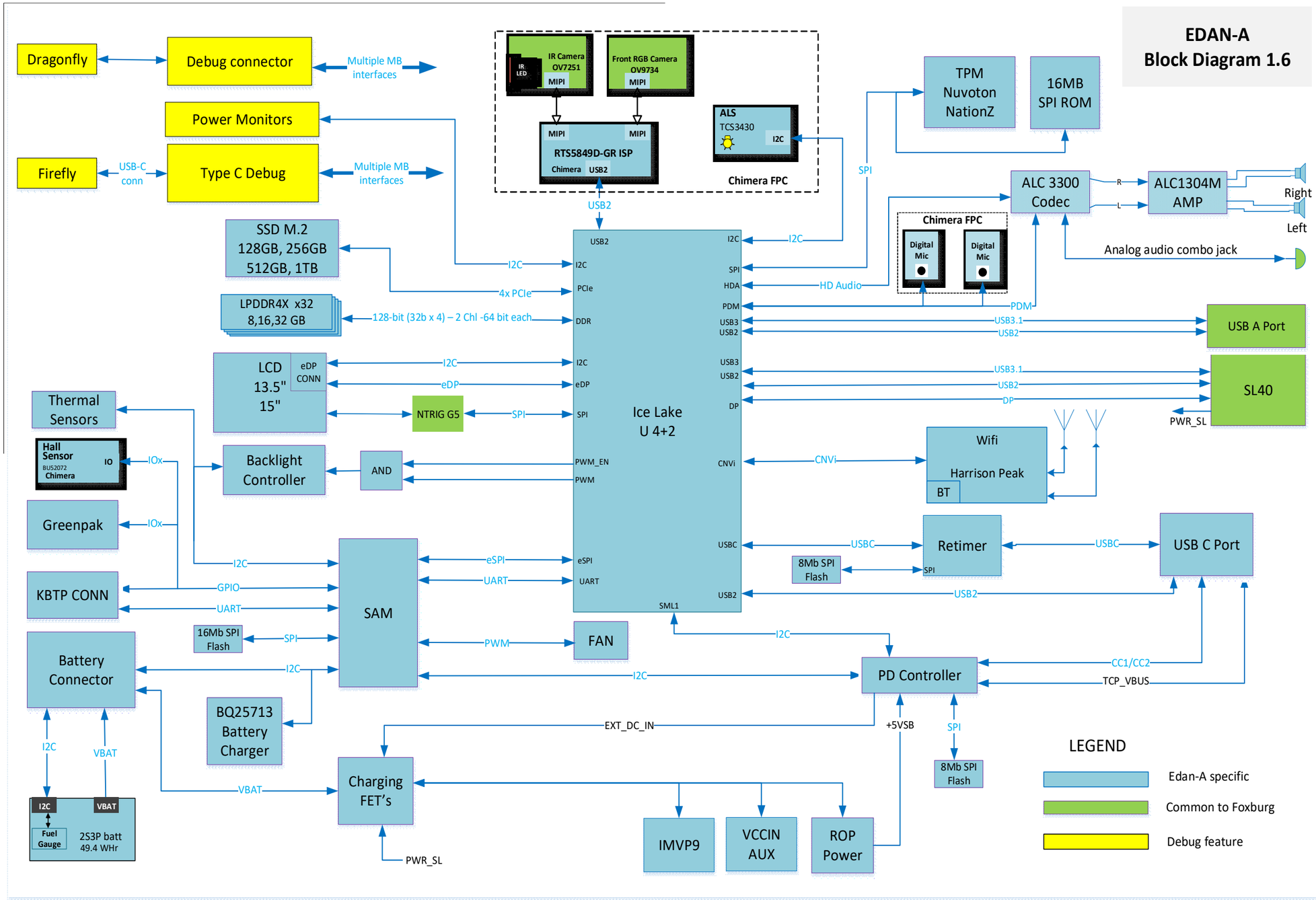
CAD Note:

Defaults: Footprint SMD 0201, Cap tmp Coeff X5R, 1% resistors

Title:	Build Options		
Engineer:	*<OrgAddr1>*		
Size: A3	Project Name: **EDAN_A_EV1**		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 2 of 82		

LAST UPDATE - Oct 25 2018

EDAN-A Block Diagram 1.6



Title:	BLOCK DIAGRAM	
<OrgName>	Engineer:	<OrgAddr1>
Size: A1	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 3 of 80	

<Variant Name>

Title: CLCOK DISTRIBUTION

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
A3	EDAN_A_EV1	2.89.6
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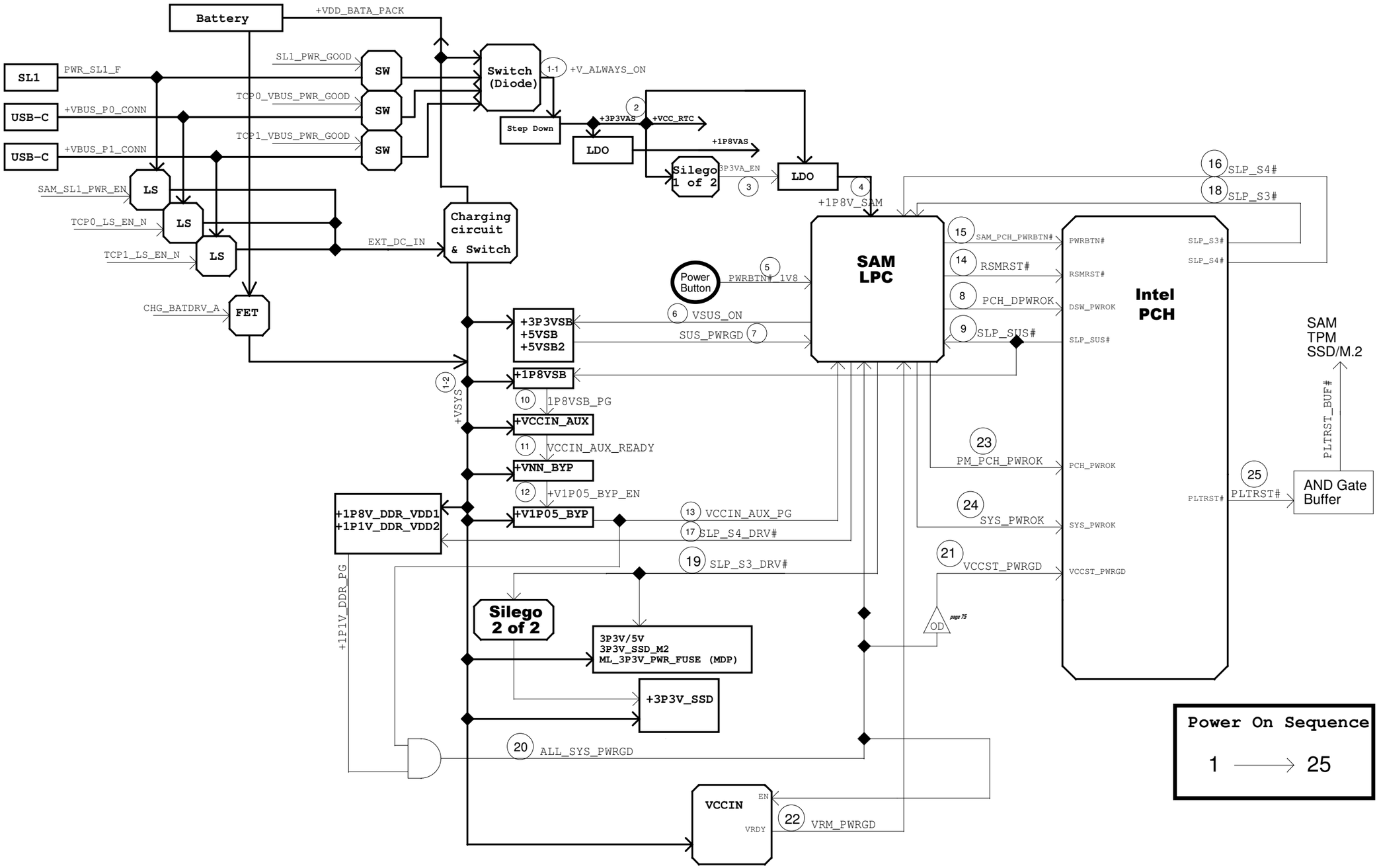
SIGNAL & RESET MAP

Last Update - Feb 13 2018



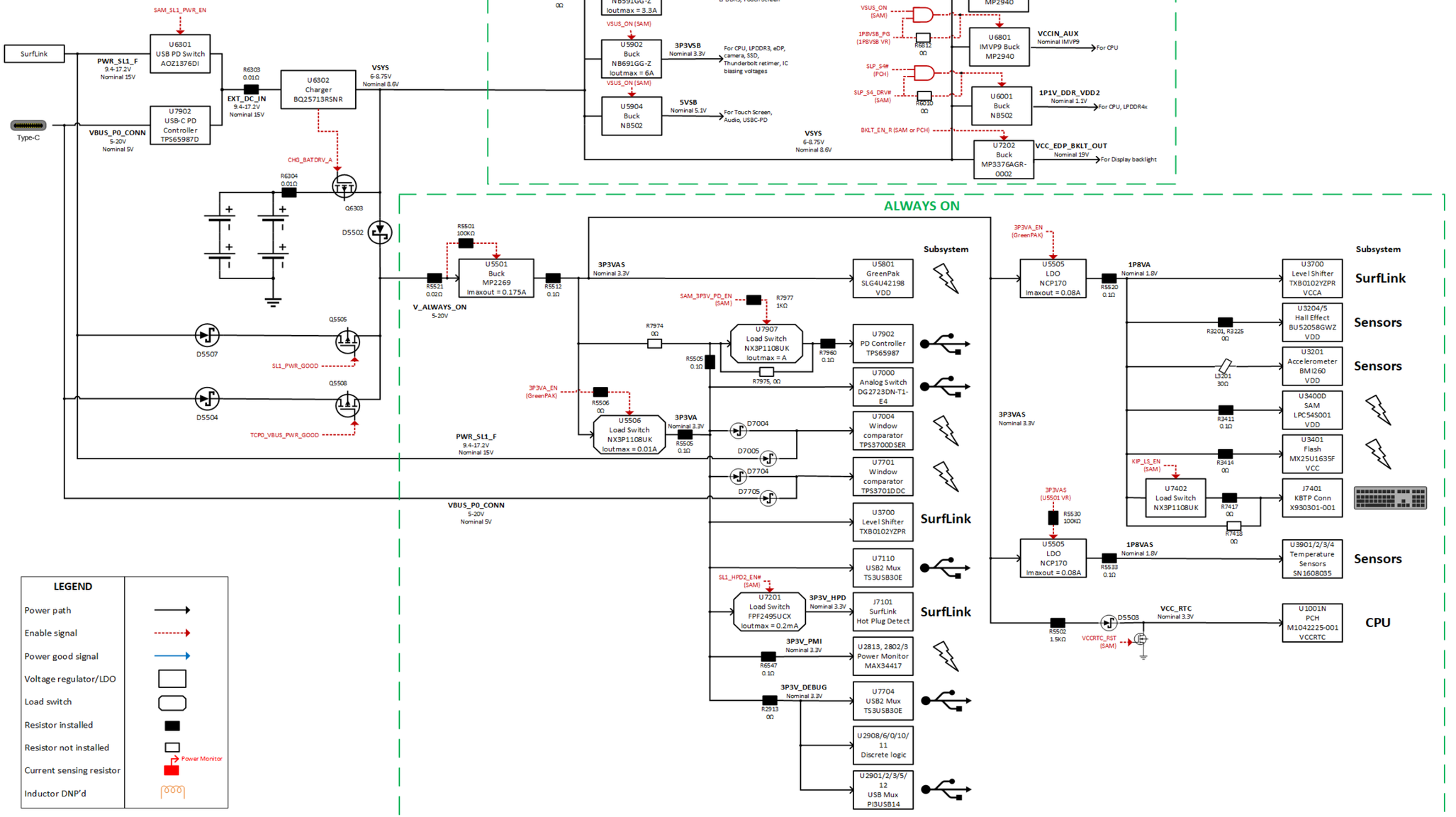
<Core Design>

Title:	SIGNAL&RESET MAP		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 5 of 82		

LAST UPDATE - Sept 13 2018

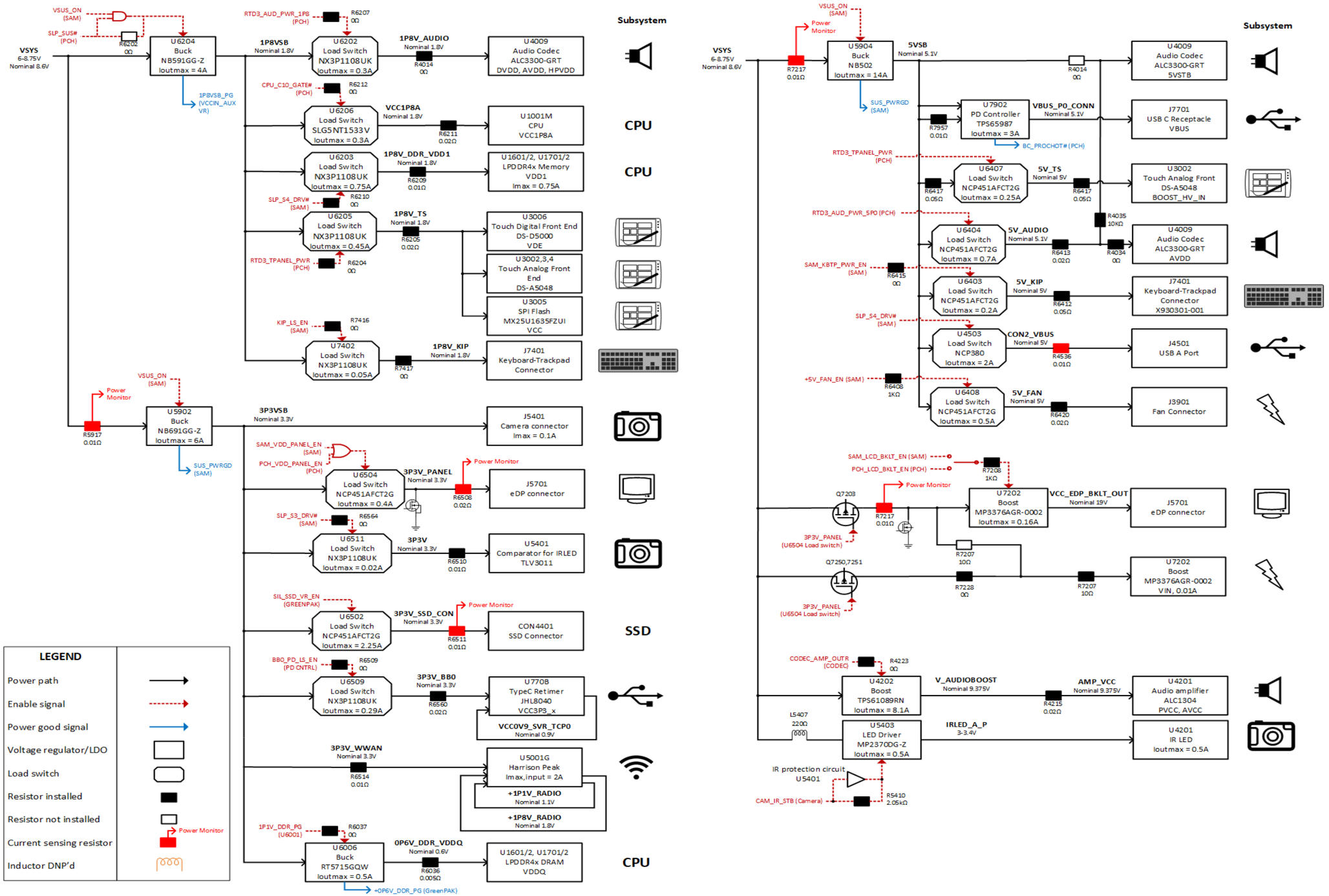
EDAN/HOOK Power Flow EV1

Power Input, Intermediate Power Buses and Always ON



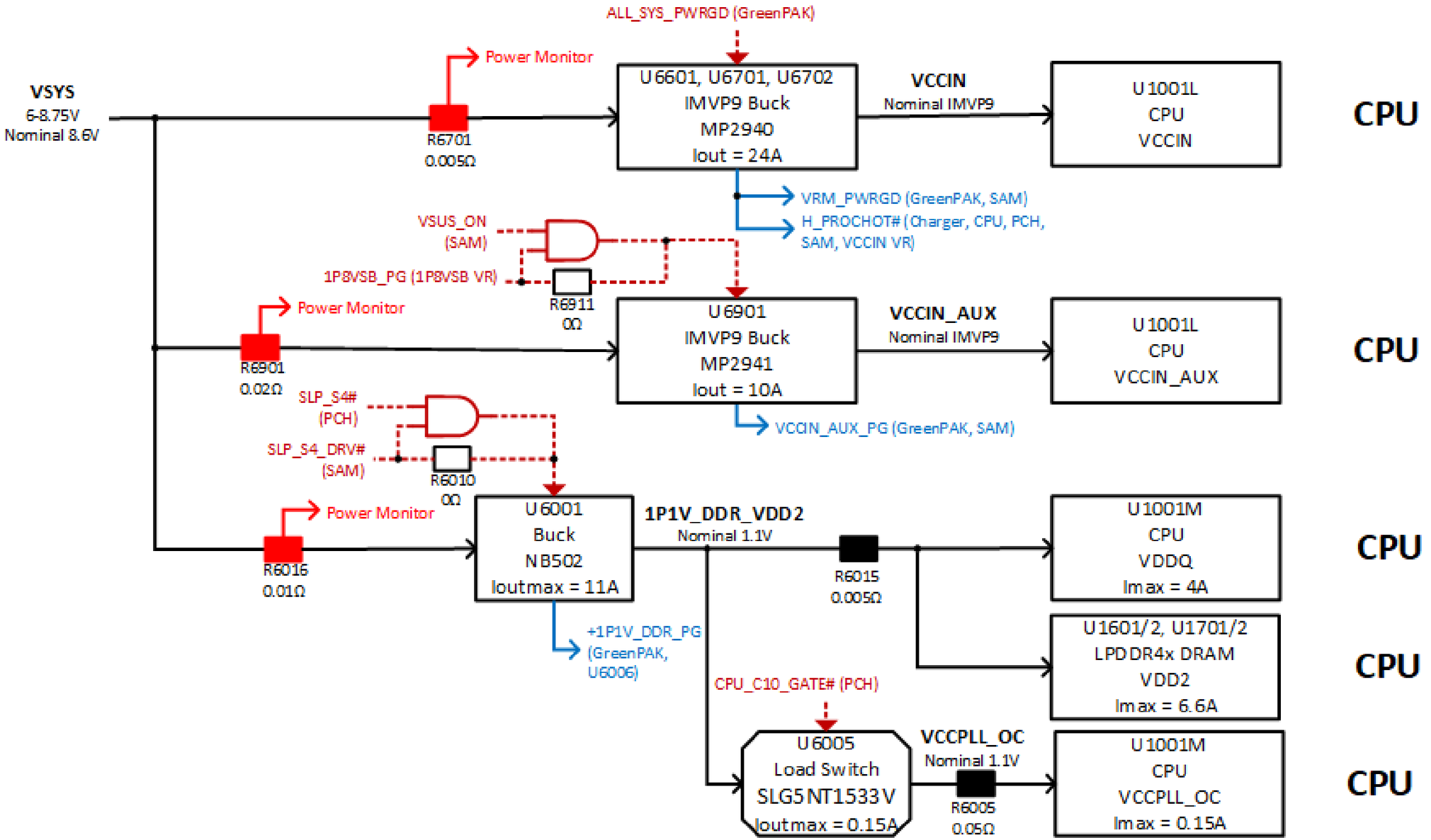
LAST UPDATE – SEPT. 13 2018

POINT OF LOAD REGULATORS AND LOAD SWITCHES



LAST UPDATE – SEPT. 13 2018

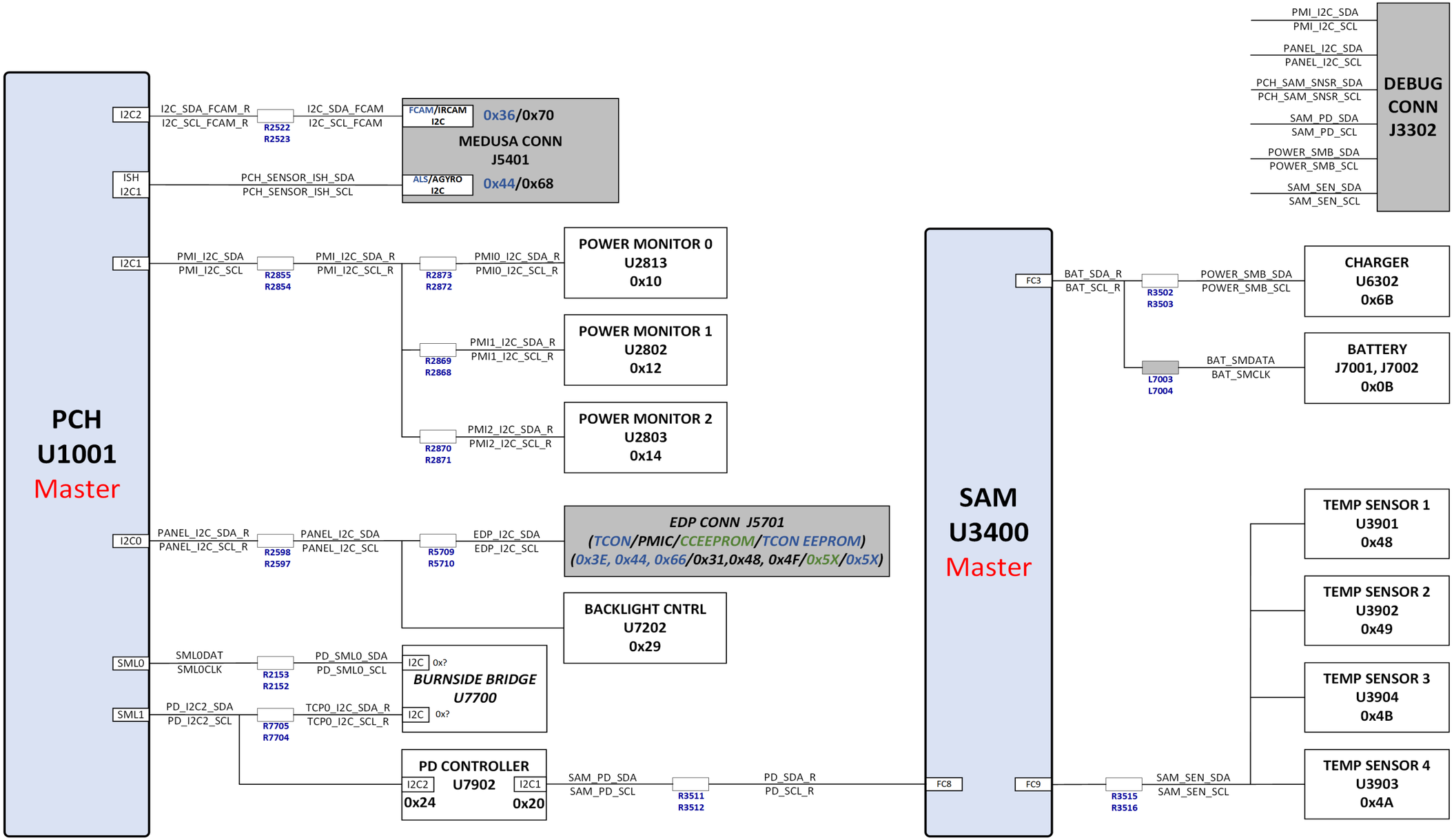
CPU Power Delivery



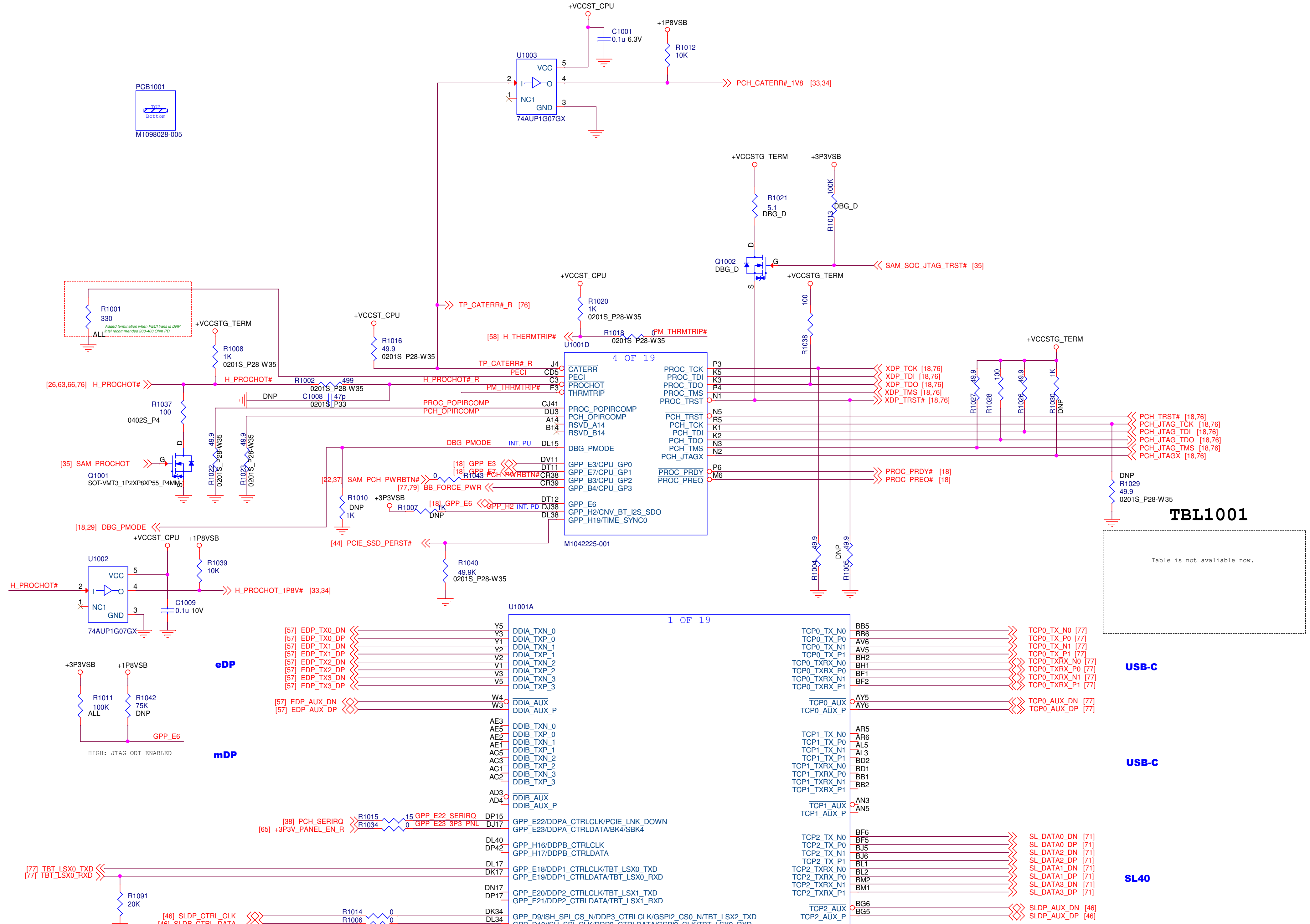
<Core Design>

Title:	POWER FLOW (3 OF 3)		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 8 of 82		

LAST UPDATE - APR.2018 (OUTDATED)



Title: 09. I2C MAP
Engineer: <OrgAddrT>
Size: A1 | Project Name: EDAN_A_EV1 | Rev: 1.00
Date: Tuesday, May 21, 2019 | Sheet 9 of 82


+VCCST_CPU
+1P8VSB
C1001
0.1u 6.3V
R1012
10K
U1003
VCC
NC1
GND
74AUP1G07GX
PCH_CATERR#_1V8 [33,34]
PCB1001
M1098028-005
+VCCSTG_TERM
+3P3VSB
R1021
5.1
DBG_D
Q1002
SAM_SOC_JTAG_TRST# [35]
R1001
330
ALL
+VCCSTG_TERM
R1008
1K
0201S_P28-W35
TP_CATERR#_R [76]
R1020
1K
[58] H_THERMTRIP#
R1018
PM_THRMTRIP#
U1001D
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CATERR
PECI
PROCHOT
THRMTRIP
PROC_POPIRCOMP
PCH_OPIRCOMP
RSVD_A14
RSVD_B14
DBG_PMODE
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_E6
GPP_H2/CNV_BT_I2S_SDO
GPP_H19/TIME_SYNC0
PROC_TCK
PROC_TDI
PROC_TDO
PROC_TMS
PROC_TRST
PCH_TRST
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
PCH_JTAGX
PROC_PRDY
PROC_PREQ
M1042225-001
XDP_TCK [18,76]
XDP_TDI [18,76]
XDP_TDO [18,76]
XDP_TMS [18,76]
XDP_TRST# [18,76]
PCH_TRST# [18,76]
PCH_JTAG_TCK [18,76]
PCH_JTAG_TDI [18,76]
PCH_JTAG_TDO [18,76]
PCH_JTAG_TMS [18,76]
PCH_JTAGX [18,76]
PROC_PRDY# [18]
PROC_PREQ# [18]
[26,63,66,76] H_PROCHOT#
[35] SAM_PROCHOT
Q1001
SOT-VMT3_1P2XP8XP55_P4MM
[22,37] SAM_PCH_PWRBTN#
[77,79] BB_FORCE_PWR
[18,29] DBG_PMODE
[44] PCIE_SSD_PERST#
R1040
49.9K
TBL1001
Table is not available now.
U1002
H_PROCHOT#
H_PROCHOT_1P8V# [33,34]
74AUP1G07GX
R1011
100K
R1042
75K
DNP
GPP_E6
HIGH: JTAG ODT ENABLED
eDP
mDP
U1001A
1 OF 19
[57] EDP_TX0_DN
[57] EDP_TX0_DP
[57] EDP_TX1_DN
[57] EDP_TX1_DP
[57] EDP_TX2_DN
[57] EDP_TX2_DP
[57] EDP_TX3_DN
[57] EDP_TX3_DP
[57] EDP_AUX_DN
[57] EDP_AUX_DP
[38] PCH_SERIRQ
[65] +3P3V_PANEL_EN_R
[77] TBT_LSX0_TXD
[77] TBT_LSX0_RXD
[46] SLDP_CTRL_CLK
[46] SLDP_CTRL_DATA
LOW: 1.8V FOR BSSB SINGAL THROUGH LS
[57] EDP_HPD
[71] SL1_DP_HPD
GPP_E17 reserved for GPU_EVENT# for SB
[30,65] PCH_VDD_PANEL_EN
[34,72] PCH_LCD_BKLT_EN
[72] PCH_BKLT_CTRL_PWM
TCP0_TX_N0 [77]
TCP0_TX_P0 [77]
TCP0_TX_N1 [77]
TCP0_TX_P1 [77]
TCP0_TXRX_N0 [77]
TCP0_TXRX_P0 [77]
TCP0_TXRX_N1 [77]
TCP0_TXRX_P1 [77]
TCP0_AUX_DN [77]
TCP0_AUX_DP [77]
USB-C
USB-C
SL_DATA0_DN [71]
SL_DATA0_DP [71]
SL_DATA2_DN [71]
SL_DATA2_DP [71]
SL_DATA1_DN [71]
SL_DATA1_DP [71]
SL_DATA3_DN [71]
SL_DATA3_DP [71]
SLDP_AUX_DN [46]
SLDP_AUX_DP [46]
SL40
USBA_EN [45]
EDP_I2C_INT [57,76]
TP1001
M1042225-001

Pull up or down straps required

DDP1 I2C/TBT LSX #0/BSSB-LS#0 VCC

GPP_E19/DDP1_CTRLDATA	
0	1.8V
1	3.3V

DDP2 I2C/TBT LSX #1/BSSB-LS#1 VCC

GPP_E21/DDP2_CTRLDATA	
0	1.8V
1	3.3V

eSPI Flash Sharing Mode

GPP_H2	
0 DEFAULT	Master Attached
1	Slave Attached

W x H 437 x 328 mm

<OrgName> Title: CPU(1)_Disp,Type-C,MISC

Engineer: <OrgAddr1>

Size	Project Name	Rev
A2	EDAN_A_EV1	0.23

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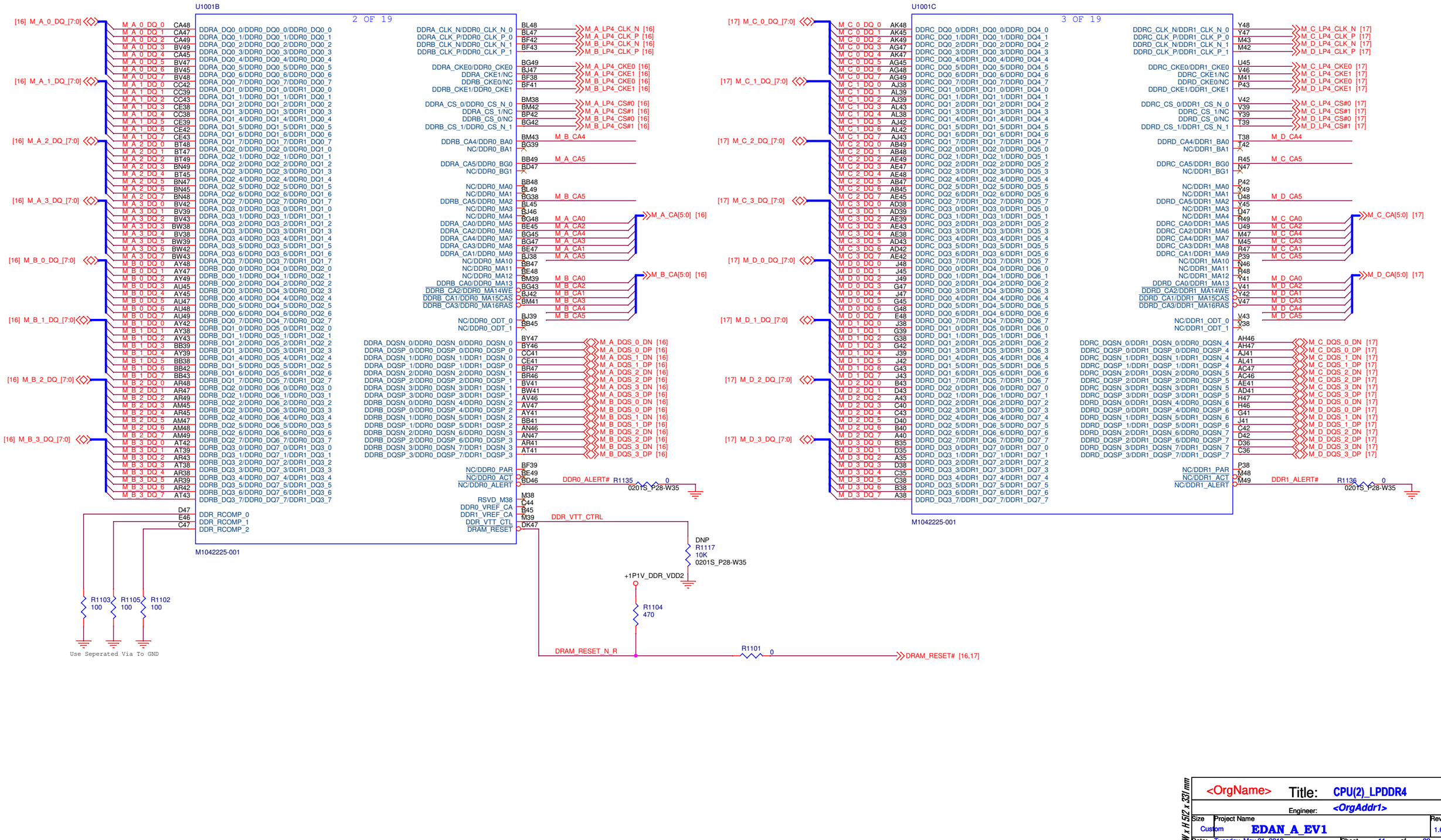
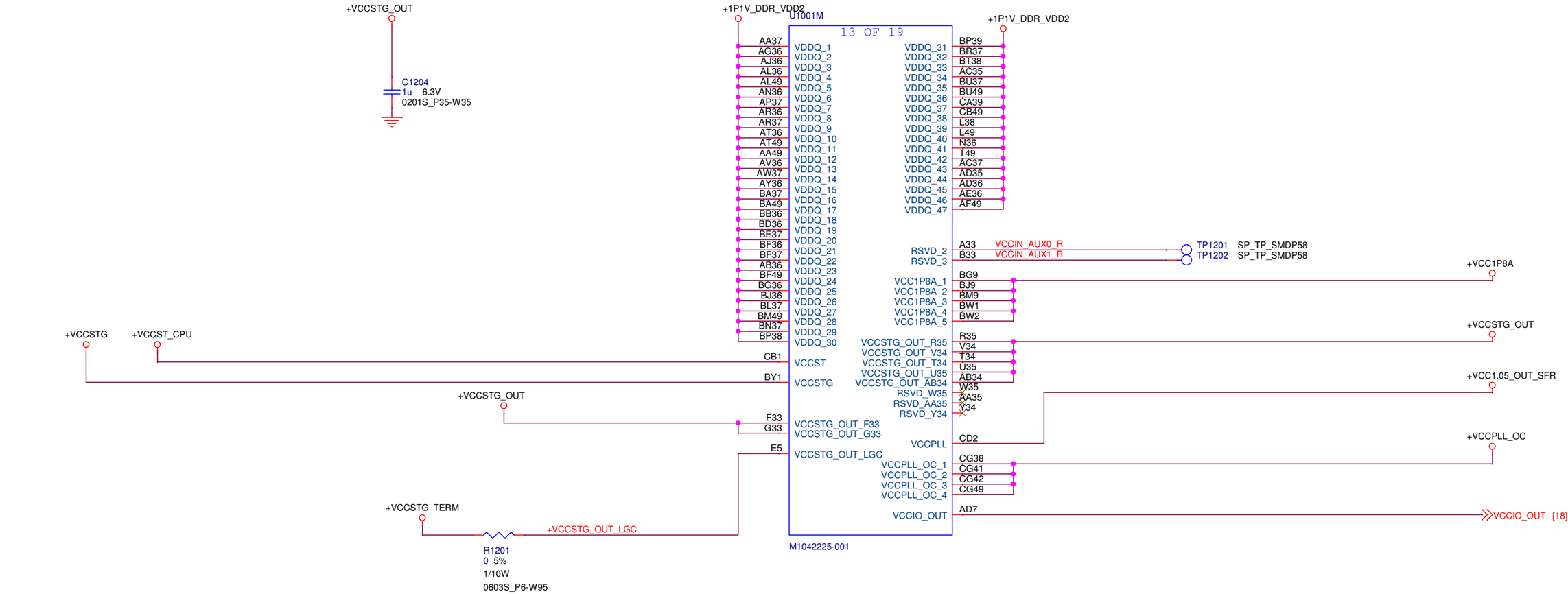
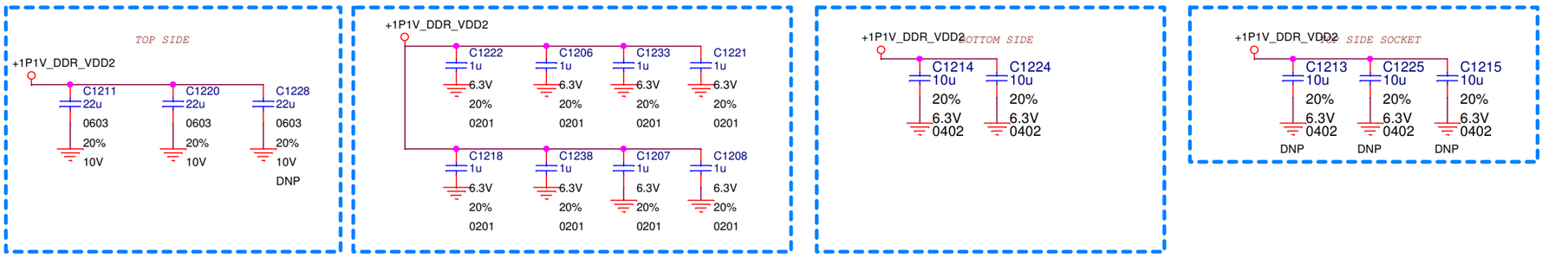
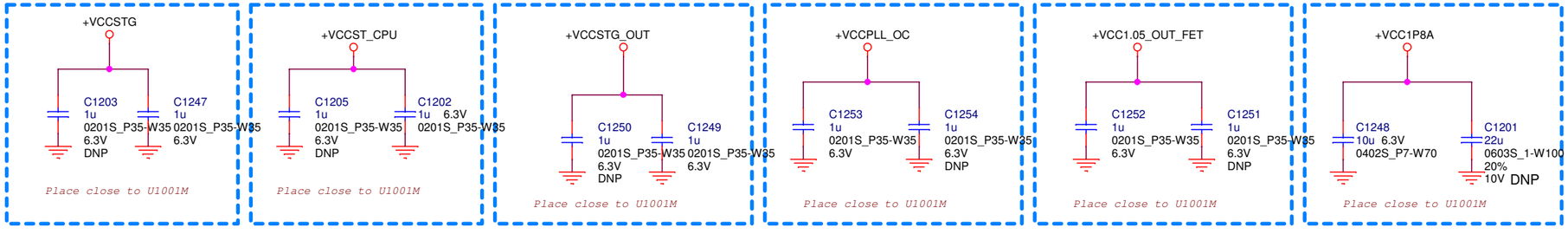


<OrgName>	Title: CPU(2)_LPDDR4
	Engineer: <OrgAddr1>
Size: Custom	Project Name: EDAN_A_EV1
Rev: 1.00	
Date: Tuesday, May 21, 2019	Sheet 11 of 82

W x H 522 x 331 mm







W x H 437 x 328 mm

<OrgName>	Title: CPU(3)_ICL_POWER1	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
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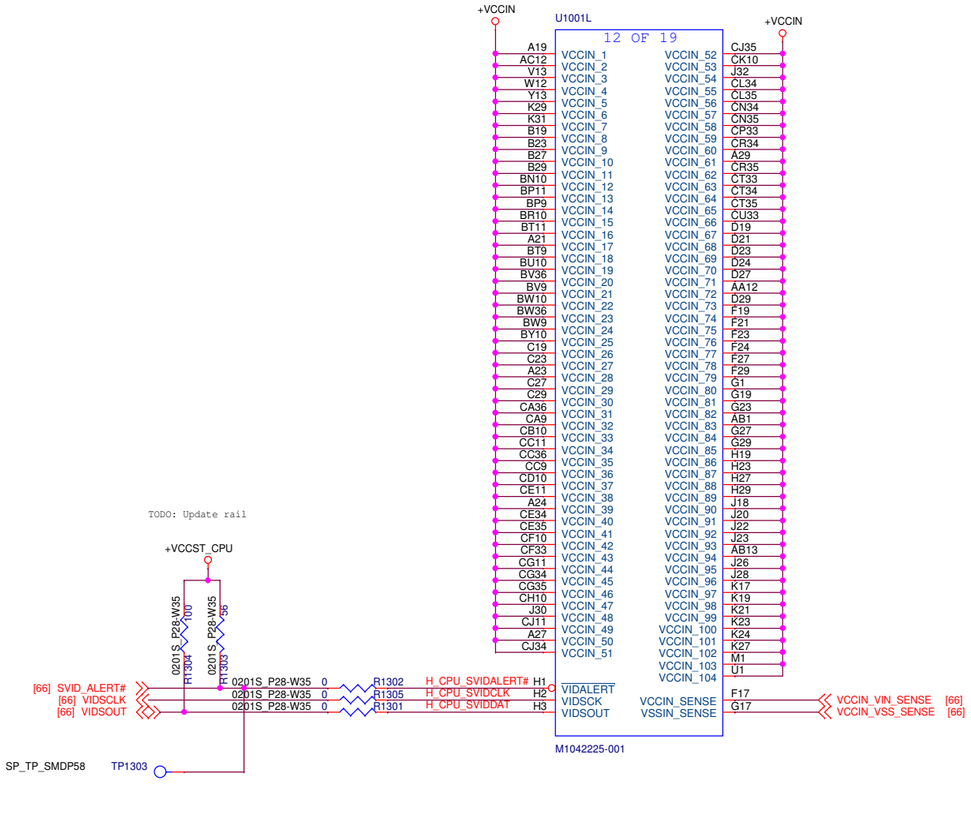
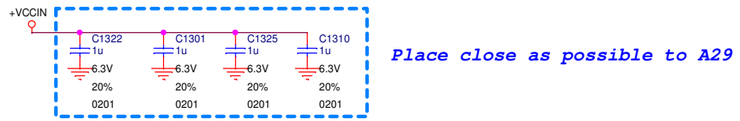
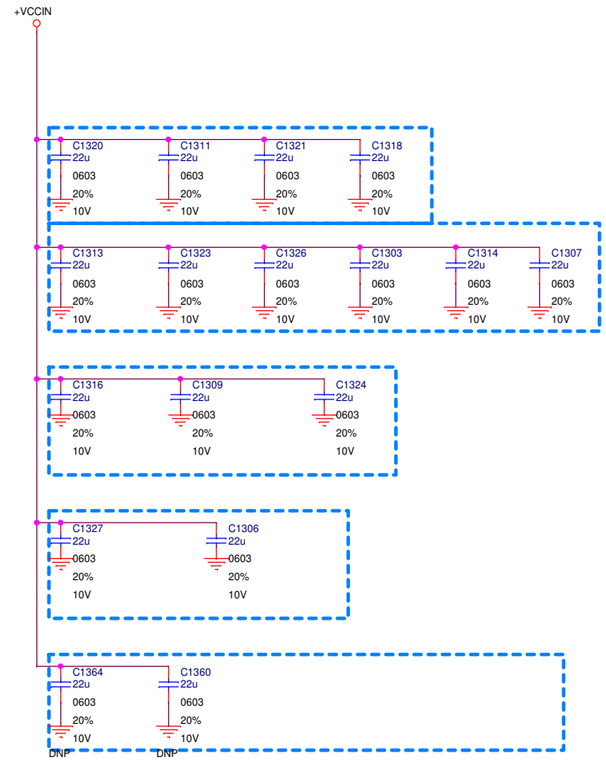


BACKSIDE CAP



Place close as possible to A29

PRIMARY SIDE



W x H 512 x 331 mm	<OrgName>	Title: CPU(4)_ICL_POWER2	
		Engineer: <OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
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A11	VSS_1	VSS_75	AF45
A46	VSS_2	VSS_76	AF47
BA45	VSS_3	VSS_77	AG1
BA47	VSS_4	VSS_78	AG11
BB11	VSS_5	VSS_79	AG3
BB3	VSS_6	VSS_80	AG38
BB7	VSS_7	VSS_81	AG39
BC37	VSS_8	VSS_82	AG41
BD3	VSS_9	VSS_83	A31
BD38	VSS_10	VSS_84	AG42
BD39	VSS_11	VSS_85	AG43
BD41	VSS_12	VSS_86	AG5
A48	VSS_13	VSS_87	AG9
BD42	VSS_14	VSS_88	AH2
BD43	VSS_15	VSS_89	AH37
BD45	VSS_16	VSS_90	AH45
BD49	VSS_17	VSS_91	AH49
BD5	VSS_18	VSS_92	AJ2
BD6	VSS_19	VSS_93	AJ3
BD7	VSS_20	VSS_94	A34
BE1	VSS_21	VSS_95	AK37
BE2	VSS_22	VSS_96	AL2
BF3	VSS_23	VSS_97	AL45
A49	VSS_24	VSS_98	AL47
BF45	VSS_25	VSS_99	AL6
BF47	VSS_26	VSS_100	AM2
BF7	VSS_27	VSS_101	AM37
BG3	VSS_28	VSS_102	AN2
BG41	VSS_29	VSS_103	AN38
BG7	VSS_30	VSS_104	AN39
BH37	VSS_31	VSS_105	A36
BJ1	VSS_32	VSS_106	AN41
BJ2	VSS_33	VSS_107	AN42
BJ3	VSS_34	VSS_108	AN43
AA45	VSS_35	VSS_109	AN45
BJ41	VSS_36	VSS_110	AN49
BJ43	VSS_37	VSS_111	AN6
BJ45	VSS_38	VSS_112	AR1
BJ49	VSS_39	VSS_113	AR11
BJ7	VSS_40	VSS_114	AR2
BM11	VSS_41	VSS_115	AR3
BM3	VSS_42	VSS_116	A39
BM45	VSS_43	VSS_117	AR7
BM47	VSS_44	VSS_118	AR9
BM5	VSS_45	VSS_119	AT3
AA47	VSS_46	VSS_120	AT45
BM6	VSS_47	VSS_121	AT47
BM7	VSS_48	VSS_122	AT5
BP1	VSS_49	VSS_123	AT6
BP2	VSS_50	VSS_124	AT7
BP3	VSS_51	VSS_125	AU37
BP43	VSS_52	VSS_126	AV11
BP7	VSS_53	VSS_127	A42
BR45	VSS_54	VSS_128	AV3
BR49	VSS_55	VSS_129	AV38
AB11	VSS_56	VSS_130	AV39
AB3	VSS_57	VSS_131	AV41
AB38	VSS_58	VSS_132	AV42
AB39	VSS_59	VSS_133	AV43
AB41	VSS_60	VSS_134	AV45
A17	VSS_61	VSS_135	AV49
AB42	VSS_62	VSS_136	AV7
AB43	VSS_63	VSS_137	AY3
AB5	VSS_64	VSS_138	A44
AB6	VSS_65	VSS_139	AY7
AC45	VSS_66	VSS_140	B17
AC49	VSS_67	VSS_141	B2
AD10	VSS_68	VSS_142	B21
AD11	VSS_69	VSS_143	B24
AD34	VSS_70	VSS_144	B3
AD37	VSS_71	VSS_145	B31
A3	VSS_72	VSS_146	B48
AE6	VSS_73	VSS_147	BA1
AF37	VSS_74	VSS_148	BA2

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BT3	VSS_149	VSS_223	CR37
BT39	VSS_150	VSS_224	CR45
BT41	VSS_151	VSS_225	CR49
BT42	VSS_152	VSS_226	CT37
BT43	VSS_153	VSS_227	CT39
BT7	VSS_154	VSS_228	CT42
BU45	VSS_155	VSS_229	CT9
BU47	VSS_156	VSS_230	CU45
BV1	VSS_157	VSS_231	CU47
BV11	VSS_158	VSS_232	CU49
BV2	VSS_159	VSS_233	CV3
BV3	VSS_160	VSS_234	CV34
BV7	VSS_161	VSS_235	CV35
BW3	VSS_162	VSS_236	CV5
BW37	VSS_163	VSS_237	CV9
BW5	VSS_164	VSS_238	CY41
BW6	VSS_165	VSS_239	CY45
BW7	VSS_166	VSS_240	CY49
BY37	VSS_167	VSS_241	CY9
BY45	VSS_168	VSS_242	D13
BY49	VSS_169	VSS_243	D17
C11	VSS_170	VSS_244	D31
C13	VSS_171	VSS_245	D44
C14	VSS_172	VSS_246	D49
C17	VSS_173	VSS_247	DA10
C21	VSS_174	VSS_248	DA33
C24	VSS_175	VSS_249	DA9
C31	VSS_176	VSS_250	DB32
C34	VSS_177	VSS_251	DB35
C39	VSS_178	VSS_252	DB38
C48	VSS_179	VSS_253	DB45
C49	VSS_180	VSS_254	DB47
C6	VSS_181	VSS_255	DB49
CA3	VSS_182	VSS_256	DC3
CA38	VSS_183	VSS_257	DC49
CA41	VSS_184	VSS_258	DC5
CA42	VSS_185	VSS_259	DC6
CA43	VSS_186	VSS_260	DD37
CA7	VSS_187	VSS_261	DD42
CB37	VSS_188	VSS_262	DE10
CB45	VSS_189	VSS_263	DE13
CB47	VSS_190	VSS_264	DE17
CC3	VSS_191	VSS_265	DE18
CC7	VSS_192	VSS_266	DE20
CE37	VSS_193	VSS_267	DE22
CE45	VSS_194	VSS_268	DE23
CE49	VSS_195	VSS_269	DE26
CE9	VSS_196	VSS_270	DE28
CG37	VSS_197	VSS_271	DE29
CG39	VSS_198	VSS_272	DE33
CG43	VSS_199	VSS_273	DE45
CG45	VSS_200	VSS_274	DE6
CG47	VSS_201	VSS_275	DF13
CG9	VSS_202	VSS_276	DF22
CH3	VSS_203	VSS_277	DF28
CH5	VSS_204	VSS_278	DF33
CJ37	VSS_205	VSS_279	DF35
CJ42	VSS_206	VSS_280	DF39
CJ9	VSS_207	VSS_281	DG10
CK45	VSS_208	VSS_282	DG12
CK49	VSS_209	VSS_283	DG13
CK9	VSS_210	VSS_284	DG15
CL37	VSS_211	VSS_285	DG22
CL42	VSS_212	VSS_286	DG23
CL49	VSS_213	VSS_287	DG47
CM45	VSS_214	VSS_288	DG6
CM47	VSS_215	VSS_289	DH1
CM9	VSS_216	VSS_290	DH3
CN3	VSS_217	VSS_291	DH45
CN37	VSS_218	VSS_292	DH5
CN39	VSS_219	VSS_293	DJ19
CN5	VSS_220	VSS_294	DJ21
CP9	VSS_221	VSS_295	DJ27
CR32	VSS_222	VSS_296	DJ31

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DJ33	VSS_297	VSS_362	F11
DJ36	VSS_298	VSS_363	F31
DJ42	VSS_299	VSS_364	F45
DK3	VSS_300	VSS_365	F47
DK4	VSS_301	VSS_366	F8
DK49	VSS_302	VSS_367	G21
DK6	VSS_303	VSS_368	G24
DK8	VSS_304	VSS_369	G3
DL10	VSS_305	VSS_370	G31
DL13	VSS_306	VSS_371	G36
DL44	VSS_307	VSS_372	G49
DL47	VSS_308	VSS_373	G5
DM47	VSS_309	VSS_374	H17
DN15	VSS_310	VSS_375	H21
DN19	VSS_311	VSS_376	H24
DN24	VSS_312	VSS_377	H31
DN31	VSS_313	VSS_378	H33
DN36	VSS_314	VSS_379	H36
DN42	VSS_315	VSS_380	H45
DP45	VSS_316	VSS_381	H49
DR49	VSS_317	VSS_382	J10
DT1	VSS_318	VSS_383	J13
DT10	VSS_319	VSS_384	J16
DT15	VSS_320	VSS_385	J36
DT20	VSS_321	VSS_386	J6
DT27	VSS_322	VSS_387	K11
DT3	VSS_323	VSS_388	K33
DT32	VSS_324	VSS_389	K8
DT37	VSS_325	VSS_390	L36
DT42	VSS_326	VSS_391	L39
DT49	VSS_327	VSS_392	L41
DT6	VSS_328	VSS_393	L42
DT7	VSS_329	VSS_394	L43
DT8	VSS_330	VSS_395	L45
DU1	VSS_331	VSS_396	L47
DU10	VSS_332	VSS_397	M10
DU15	VSS_333	VSS_398	M3
DU2	VSS_334	VSS_399	M36
DU20	VSS_335	VSS_400	M5
DU27	VSS_336	VSS_401	N45
DU32	VSS_337	VSS_402	N49
DU37	VSS_338	VSS_403	P11
DU48	VSS_339	VSS_404	P41
DU49	VSS_340	VSS_405	P8
DU7	VSS_341	VSS_406	R3
DV2	VSS_342	VSS_407	R37
DV44	VSS_343	VSS_408	T11
DV48	VSS_344	VSS_409	T36
DV8	VSS_345	VSS_410	T41
DW1	VSS_346	VSS_411	T43
DW10	VSS_347	VSS_412	T45
DW2	VSS_348	VSS_413	T47
DW20	VSS_349	VSS_414	U3
DW27	VSS_350	VSS_415	U37
DW44	VSS_351	VSS_416	U5
DW46	VSS_352	VSS_417	V11
DW48	VSS_353	VSS_418	V36
DW49	VSS_354	VSS_419	V45
DW7	VSS_355	VSS_420	V49
E11	VSS_356	VSS_421	V9
E34	VSS_357	VSS_422	W37
E36	VSS_358	VSS_423	Y36
E39	VSS_359	VSS_424	Y38
E42	VSS_360	VSS_425	Y43
E6	VSS_361	VSS_426	Y9
		VSS_427	DE15

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CFG4	
0 **Default**	enable eDP
1	Disable eDP

TP1516

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[18] CFG0 AG6 CFG_0
[18] CFG1 AE7 CFG_1
[18] CFG2 AG7 CFG_2
[18] CFG3 AD9 CFG_3
[18] CFG4 AE9 CFG_4
[18] CFG5 AB9 CFG_5
[18] CFG6 AJ6 CFG_6
[18] CFG7 AB7 CFG_7
TP1519 CFG8 V10 CFG_8
TP1520 CFG9 AJ5 CFG_9
TP1521 CFG10 Y10 CFG_10
AJ7 CFG_11
AB10 CFG_12
AL7 CFG_13
AL9 CFG_14
AJ9 CFG_15
CFG16 V6 CFG_16
[18] CFG17 V7 CFG_17
CFG18 Y6 CFG_18
Y7 CFG_19
R1507 49.9 0201S_P28-W35 CFG_RCOMP AD6 CFG_RCOMP
TP1528 BPM_N_0 T9 BPM_N_0
TP1529 BPM_N_1 T7 BPM_N_1
T10 BPM_N_2
T6 BPM_N_3
SP_TP_SMDP58 TP1518 BPM_N_2
SP_TP_SMDP58 TP1514 BPM_N_3
Place outside of thermal module
BJ11 RSVD_68
BL10 RSVD_69
AV1 RSVD_TP_AV1
AT2 RSVD_TP_AT2
AT1 RSVD_TP_AT1
AU1 RSVD_TP_AU1
AU2 RSVD_TP_AU2
AV2 RSVD_TP_AV2
DP3 RSVD_83
DT2 RSVD_84
AR10 RSVD_85
AP10 RSVD_87
BP36 RSVD_86
BM36 RSVD_88
J15 VSS_430
K15 VSS_431
C5 SKTOCC
D4 RSVD_D4
A5 RSVD_70
R1502 0

RSVD_TP_1 A47
RSVD_TP_2 B47
RSVD_60 C1
RSVD_61 E1
RSVD_TP_CT32 CT32
RSVD_TP_CV32 CV32
RSVD_G15 G15
RSVD_F15 F15
RSVD_TP_BW11 BW11
RSVD_TP_CA11 CA11
VSS_428 C16
VSS_429 A16
RSVD_58 C2
RSVD_59 A4
RSVD_71 DP5
RSVD_72 DR5
RSVD_65 D14
RSVD_66 E16
RSVD_TP_DV6 DV6
RSVD_TP_DW6 DW6
RSVD_TP_DP2 DP2
RSVD_TP_DP1 DP1
RSVD_TP_DW4 DW4
RSVD_TP_DV4 DV4
TP_3 CM33
TP_4 DB10
RSVD_TP_R1 R1
RSVD_TP_DW3 DW3
RSVD_TP_DV3 DV3
RSVD_TP_DH49 DH49
RSVD_TP_DL8 DL8
TP_1 DW47
TP_2 DV47
VSS_432 DU47
RSVD_TP_P10 P10

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N34 RSVD_TP_N34
AK10 RSVD_TP_AK10
BT36 RSVD_7
AH10 RSVD_TP_AH10
BC10 RSVD_TP_BC10
CH33 RSVD_TP_CH33
CJ32 RSVD_12
AM10 RSVD_TP_AM10
TP1501 FIVR_VLOAD_TCSS BH10 RSVD_TP_BH10
J34 RSVD_TP_J34
Y11 RSVD_9
L34 RSVD_10
AJ11 RSVD_17
CG32 RSVD_21
CK33 RSVD_22
BP41 RSVD_20
AL11 RSVD_23
BG11 RSVD_24
AN11 RSVD_16
M13 RSVD_18
M34 RSVD_19
DU42 RSVD_42
DW42 RSVD_43
D33 RSVD_44
L13 RSVD_45
K13 RSVD_47

RSVD_TP_DA11 DA11
RSVD_TP_CL32 CL32
RSVD_TP_CN32 CN32
RSVD_32 CY35
RSVD_33 DB37
RSVD_34 DF37
IST_TP_0 BF11
IST_TP_1 BD11
IST_TRIG_0 BE10
IST_TRIG_1 BF10
PCH_IST_TP0 CW33
PCH_IST_TP1 CY32
RSVD_27 CY37
RSVD_28 CV37
VCCIN_AUX_OUT C33
RSVD_35 G34
RSVD_46 H34
RSVD_48 DJ34
RSVD_49 DK31
RSVD_50 DK15
RSVD_51 CP3
RSVD_52 CP5
RSVD_53 AN9
RSVD_54 AN7
RSVD_36 AF10
RSVD_37 AE11
RSVD_38 H5
RSVD_39 D1
RSVD_40 DJ40
RSVD_41 DK40

M1042225-001

CFG4
R1501 1K 0201S_P28-W35

CFG16
CFG18
R1503 49.9
R1504 49.9

<OrgName>

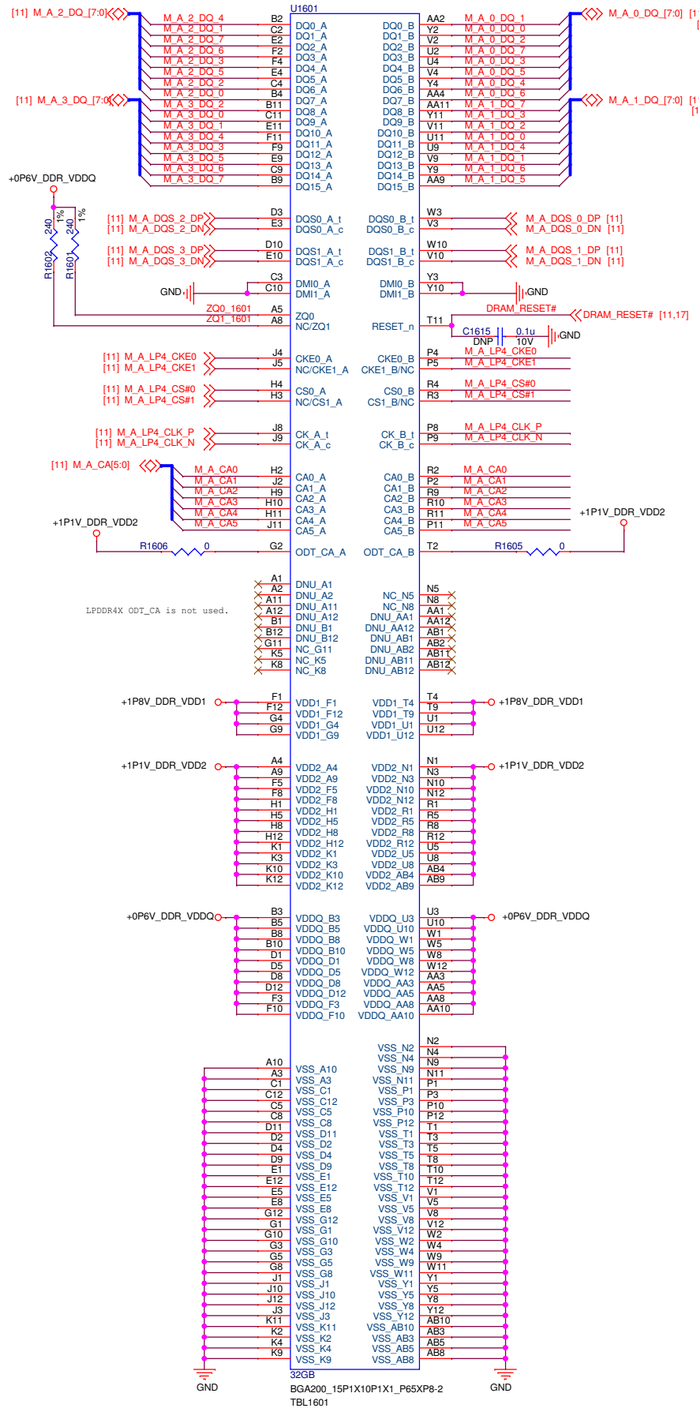
Title: CPU(6)_CFG,RESERVED

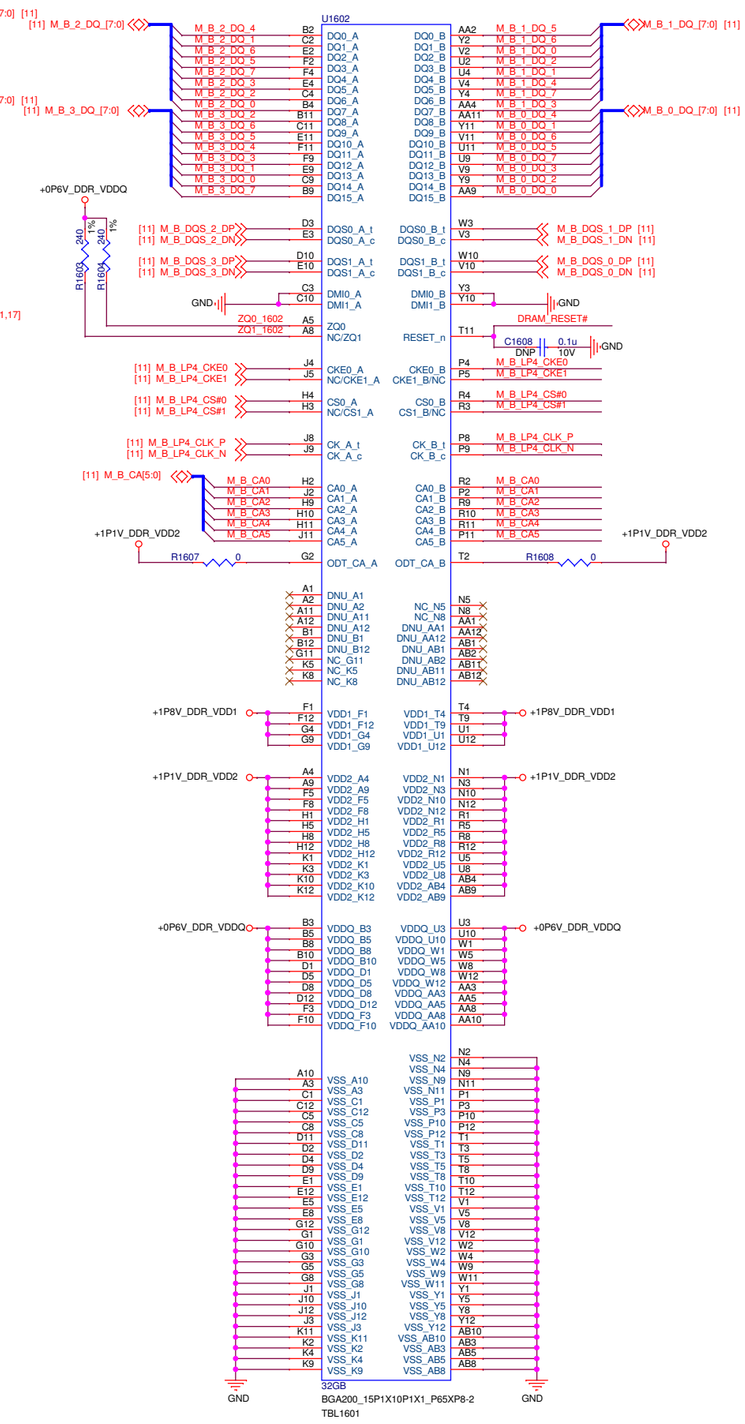
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00

Date: Tuesday, May 21, 2019 Sheet 15 of 82

W x H 367 x 237 mm

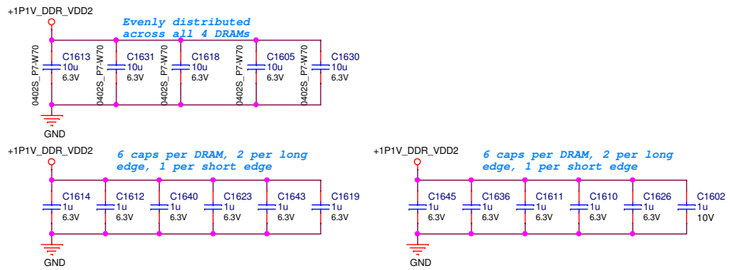




LPDDR4X x32 **Performance**	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1μF (0402)
		evenly distribute among all drams	5x 10μF (0603)
	VDDQ	4 per Dram, 2 per short edge	16x 1μF (0402)
		evenly distribute among all drams	5x 10μF (0603)
	VDD1	4 per dram, 1 per corner (connected to edge and inner BGA)	16x 1μF (0402)
		Evenly distribute	5x 10μF (0603)

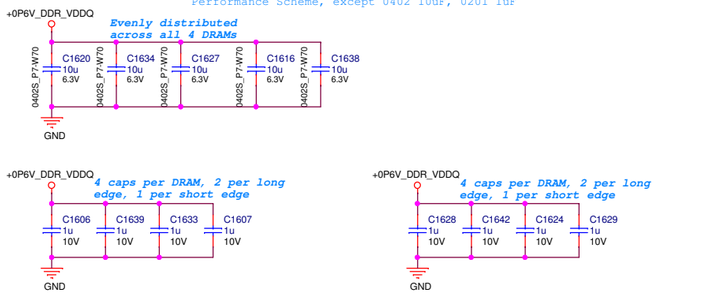
VDD2 Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



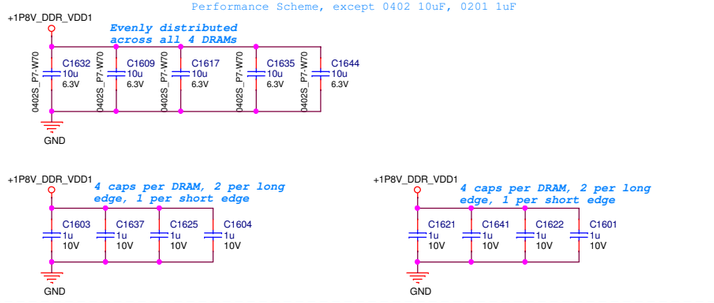
VDDQ Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



VDD1 Decoupling

Performance Scheme, except 0402 10uF, 0201 1uF



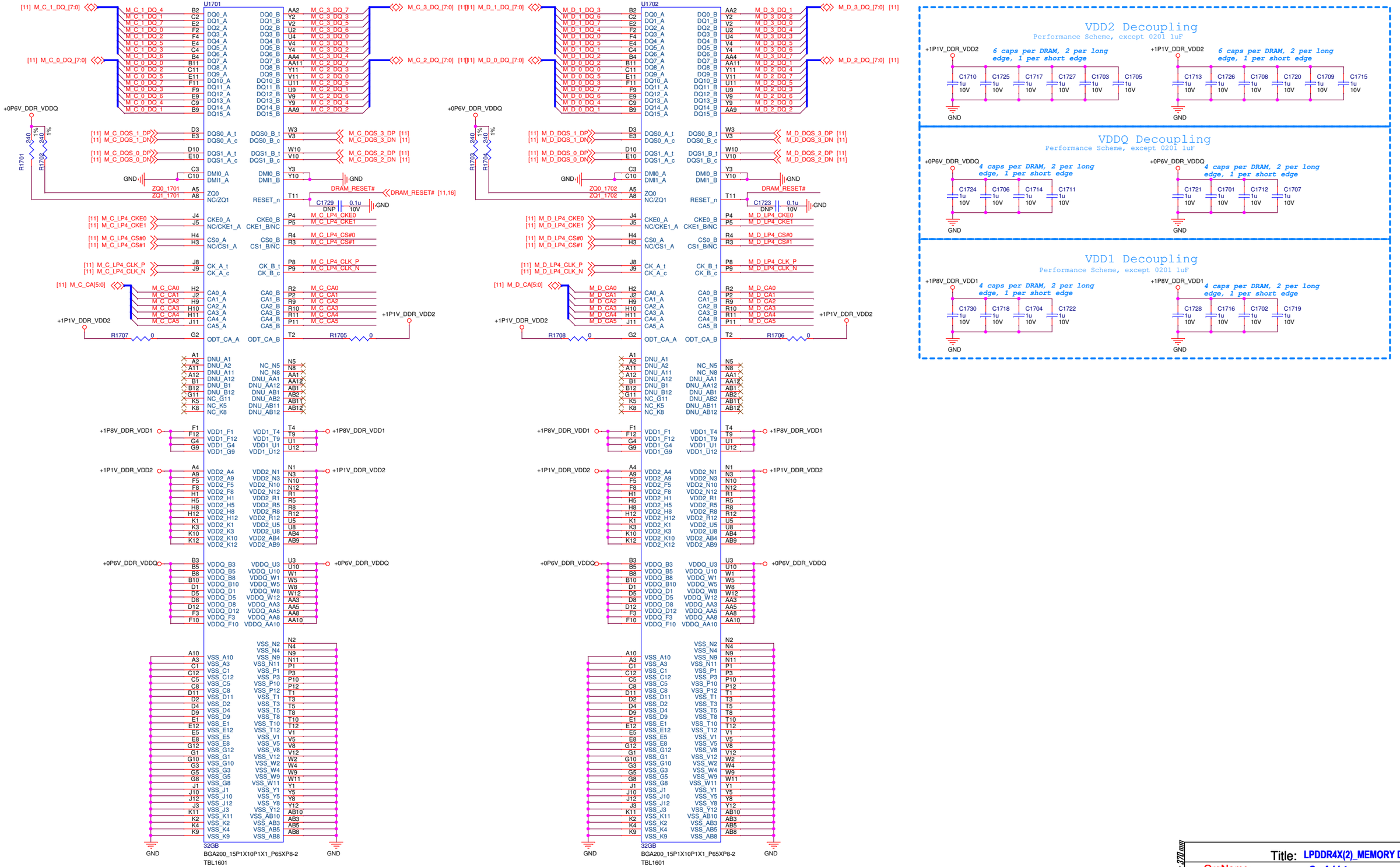
MEMORY TABLE 1601			
Manufacturer	MPN	Size	MSPN
Samsung	K4U6E3S4AA-MGCL	16Gb (2GB)	M1100585-001
Samsung	K4UBE3D4AA-MGCL	32Gb(4GB)	M1100590-001
Samsung	K4UCE3Q4AA-MGCL	64Gb (8GB)	M1100591-001
Hynix	H9HCNNNBKMALHR-NEE	16Gb (2GB)	M1102096-001
Hynix	H9HCNNNCPMALHR-NEE	32Gb(4GB)	M1102097-001

Title: LPDDR4X(1)_MEMORY DOWN

<OrgName> Engineer: <OrgAddr1>

Size: Custom | Project Name: EDAN_A_EV1 | Rev: 1.00

Date: Tuesday, May 21, 2019 | Sheet 16 of 82



VDD2 Decoupling

Performance Scheme, except 0201 1uF

+1P1V_DDR_VDD2 — *6 caps per DRAM, 2 per long edge, 1 per short edge*

C1710 1u 10V, C1725 1u 10V, C1717 1u 10V, C1727 1u 10V, C1703 1u 10V, C1705 1u 10V

+1P1V_DDR_VDD2 — *6 caps per DRAM, 2 per long edge, 1 per short edge*

C1713 1u 10V, C1726 1u 10V, C1708 1u 10V, C1720 1u 10V, C1709 1u 10V, C1715 1u 10V

GND

VDDQ Decoupling

Performance Scheme, except 0201 1uF

+0P6V_DDR_VDDQ — *4 caps per DRAM, 2 per long edge, 1 per short edge*

C1724 1u 10V, C1706 1u 10V, C1714 1u 10V, C1711 1u 10V

+0P6V_DDR_VDDQ — *4 caps per DRAM, 2 per long edge, 1 per short edge*

C1721 1u 10V, C1701 1u 10V, C1712 1u 10V, C1707 1u 10V

GND

VDD1 Decoupling

Performance Scheme, except 0201 1uF

+1P8V_DDR_VDD1 — *4 caps per DRAM, 2 per long edge, 1 per short edge*

C1730 1u 10V, C1718 1u 10V, C1704 1u 10V, C1722 1u 10V

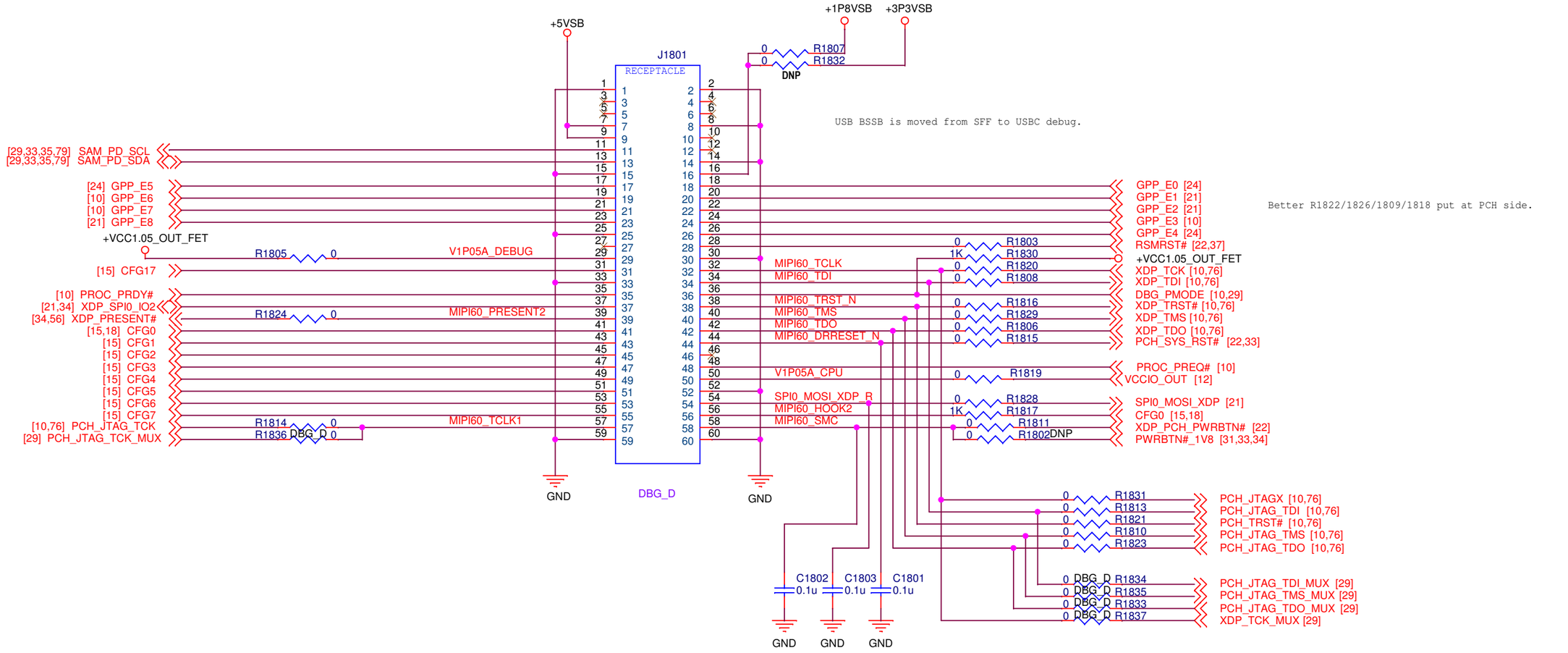
+1P8V_DDR_VDD1 — *4 caps per DRAM, 2 per long edge, 1 per short edge*

C1728 1u 10V, C1716 1u 10V, C1702 1u 10V, C1719 1u 10V

GND

Title:	LPDDR4X(2)_MEMORY DOWN	
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 17 of 82	

W: 11.692" x 8.270"



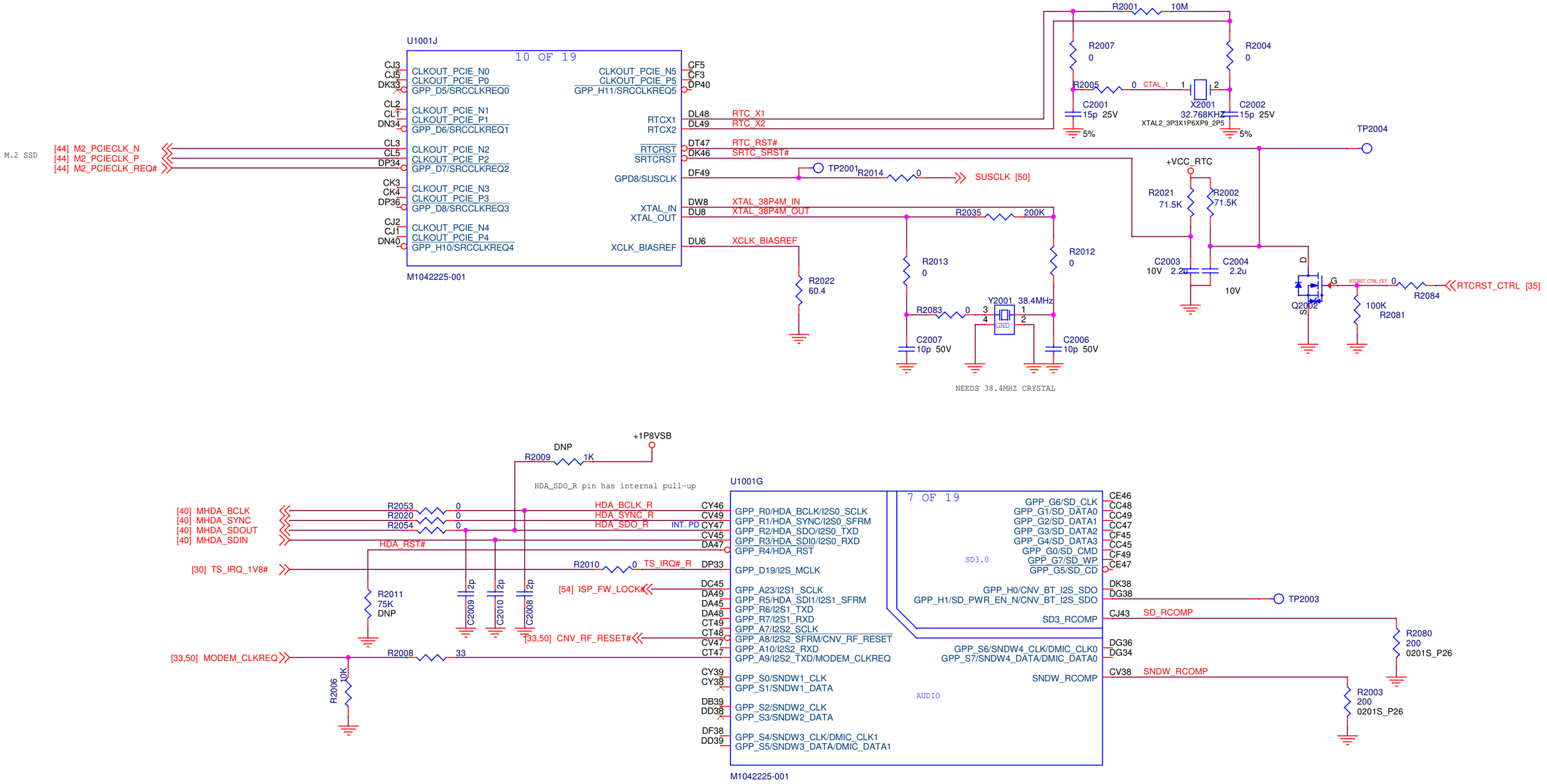
Signal	Pin #	Interface	Pin #	Signal
GND	1	PCH-V5A, USB,I2C	2	GND
USB2_DP	3		4	USB3_TX_DP
USB2_DN	5		6	USB3_TX_DN
VBUS	7		8	GND
VBUS	9		10	USB3_RX_DP
I2C_SCL	11		12	USB3_RX_DN
I2C_SDA	13		14	GND
GND	15		16	+V3P3A_PCH_VREF_TRACE
MIPI60_FN13	17		18	MIPI60_FN8
MIPI60_FN14	19		20	MIPI60_FN9
MIPI60_FN15	21		22	MIPI60_FN10
MIPI60_FN_CLK2	23		24	MIPI60_FN11
GND	25		26	MIPI60_FN12
I2C_2_SCL	27		28	PM_RSMRST_N*
+V1.05A_VREF_DEBUG	29	CPU-V5A	30	GND
MIPI60_NOA_STB0_DP	31		32	MIPI60_TCLK
GND	33		34	MIPI60_TDI
MIPI60_PRDY_N	35		36	DBG_PMODE_MIPI60_RST_R_N
MIPI60_PRESENT1_N	37		38	MIPI60_TRST_N
MIPI60_OVERRIDE	39		40	MIPI60_TMS
MIPI60_NOA0_N	41		42	MIPI60_TDO
MIPI60_NOA1_N	43		44	MIPI60_DRRESET_N
MIPI60_NOA2_N	45		46	I2C_2_SDA
MIPI60_NOA3_N	47		48	MIPI60_PREQ_N
MIPI60_NOA4_N	49		50	+V1.05A_CPU_VREF_TRACE
MIPI60_NOA5_N	51		52	GND
MIPI60_NOA6_N	53		54	SPI0_MOSI_SYS_PWROK_MIPI60
MIPI60_NOA7_N	55		56	MIPI60_HOOK2_CPU_BOOT_STALL
MIPI60_TCLK1	57		58	SMC_ONOFF_MIPI60_N
GND	59		60	GND

Title:	SFF		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 18 of 82		

W x H 392 x 254 mm

Title:					
<OrgName>	Engineer:	<OrgAddr1>			
Size: Custom	Project Name: EDAN_A_EV1				Rev: 1.00
Date: Tuesday, May 21, 2019			Sheet 19 of 82		

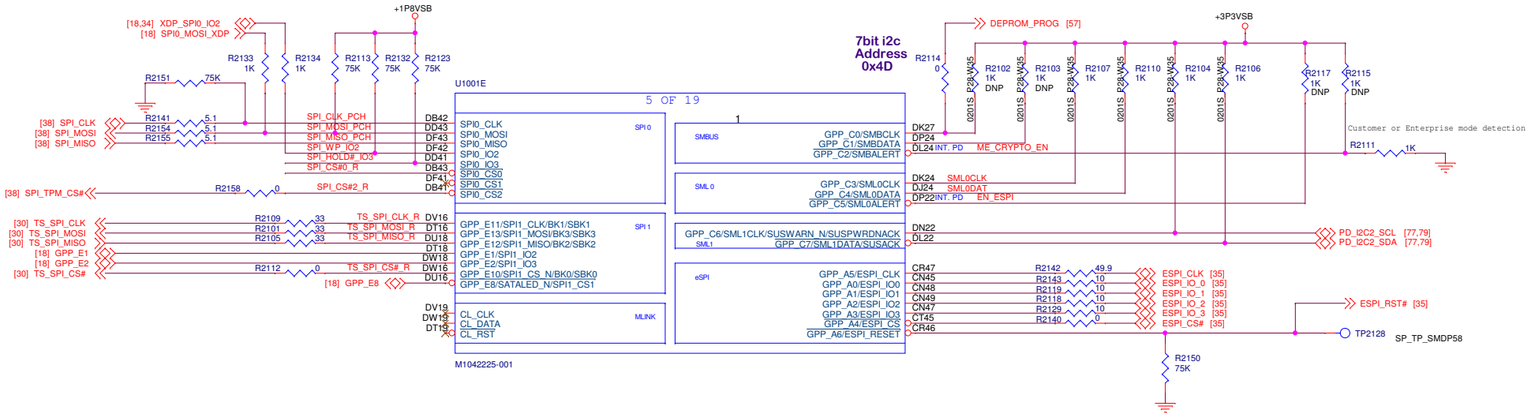
W x H 372 x 241 mm

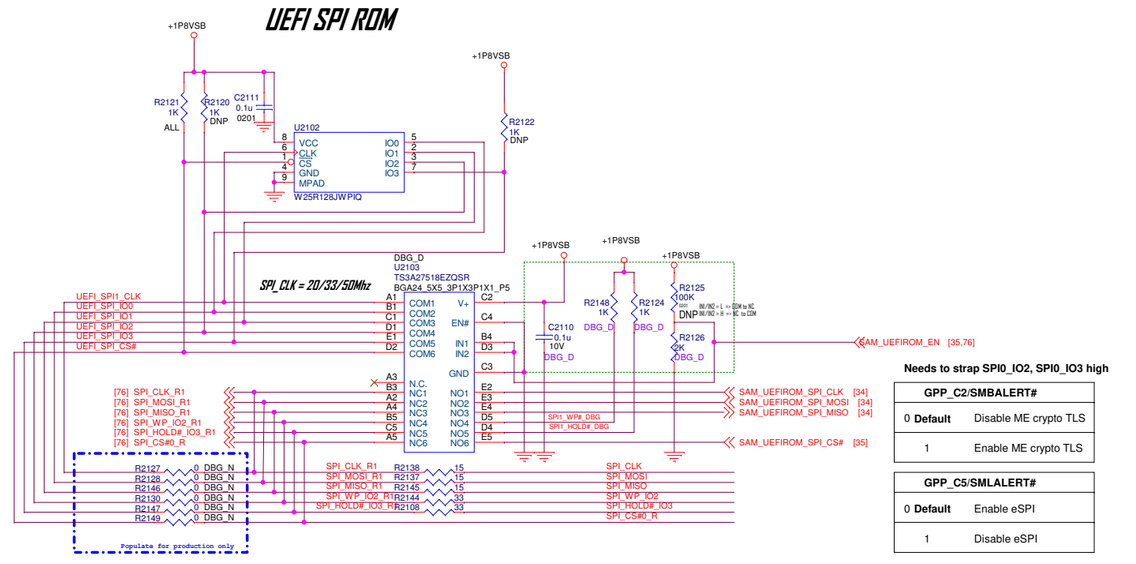


GPP_R2/HDA_SDO	
0 **Default**	Enable Flash Security
1	Disable Flash Security

Title:	PCH(1)_SD,HDA,RTC,CLK		
Engineer:	<OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 20 of 82		

W x H 417 x 270mm





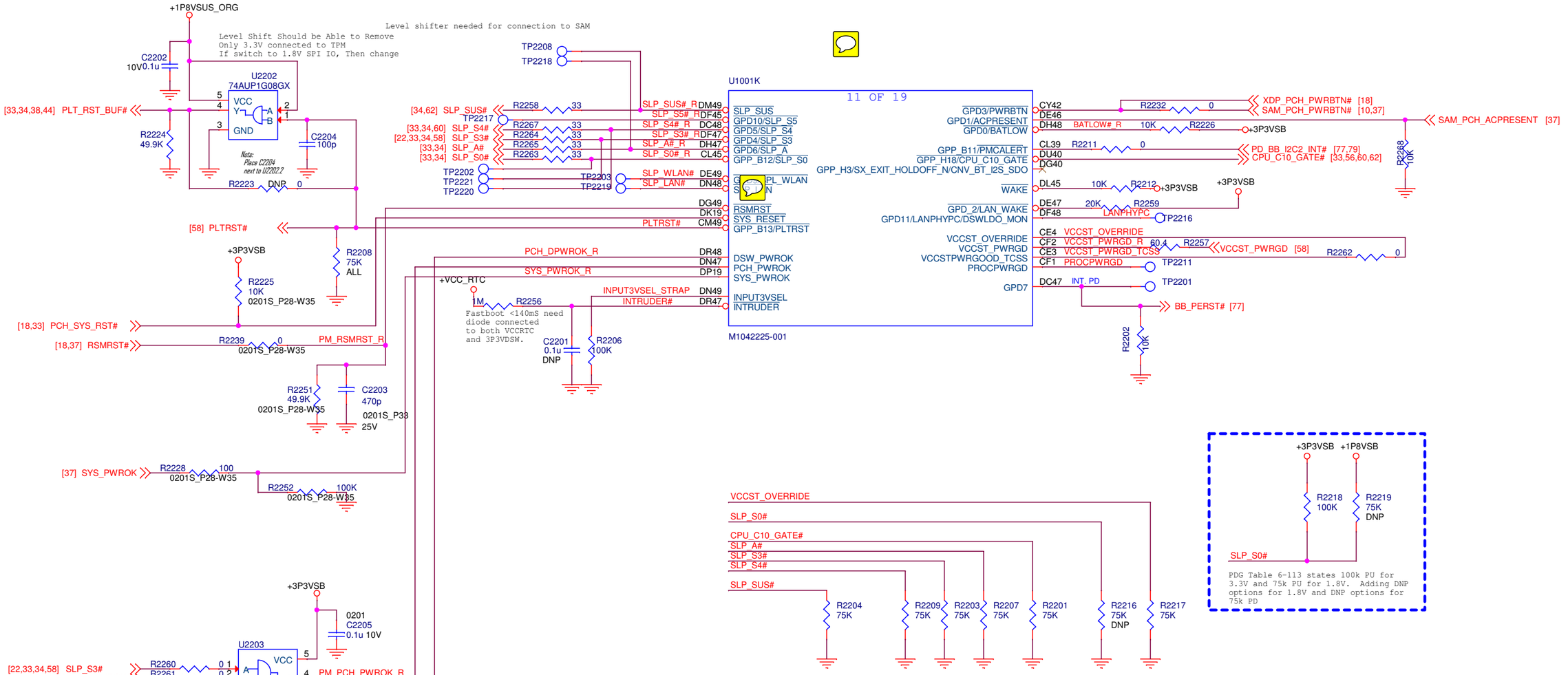
Needs to strap SPI0_IO2, SPI0_IO3 high

GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SMLALERT#	
0 **Default**	Enable eSPI
1	Disable eSPI

W x H 417 x 277mm

Title: PCH(2)_CLK,SMB,LPC,SPI		
Engineer: <OrgAddr1>		
Size: A2	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 21 of 82	



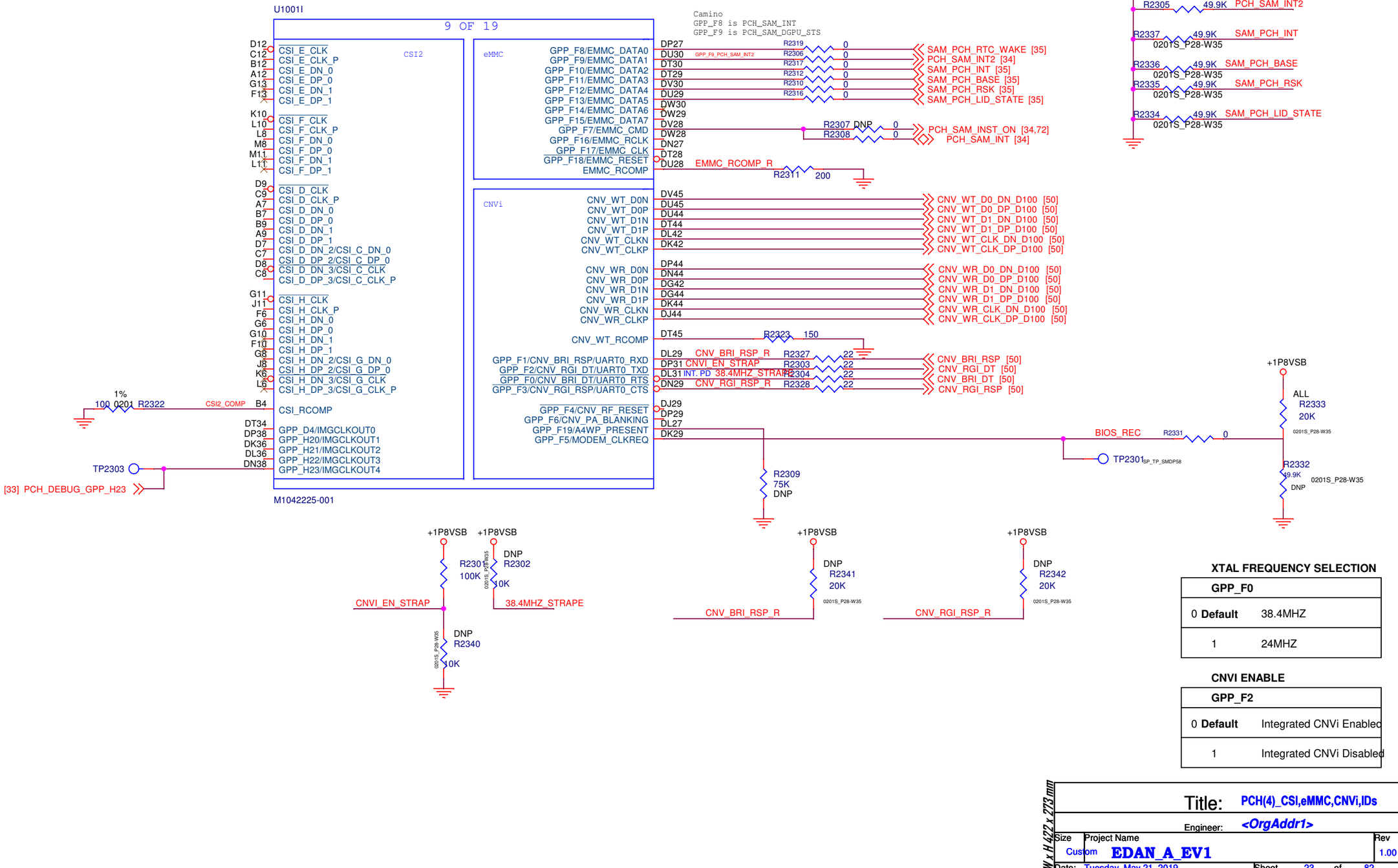
PCH Signal Glitch Free Implementation Requirements

VCCDSW 3V SELECT STRAP

INPUT3VSEL	
0	3.3V
1	3.0V

Title: PCH(3)_SYS PWR CONTR			
Engineer: <OrgAddr1>			
Size: A3	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 22 of 82		

Please place testpoints at back of SoC and as close as possible.



XTAL FREQUENCY SELECTION

GPP_F0	
0 **Default**	38.4MHZ
1	24MHZ

CNVI ENABLE

GPP_F2	
0 **Default**	Integrated CNVi Enabled
1	Integrated CNVi Disabled

Title:	PCH(4)_CSI,eMMC,CNVi,IDs	
Engineer:	<OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 23 of 82	

W x H 422 x 273 mm

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PCIE M.2 SSD

[44] PCIE_SSD_RX0_DN
[44] PCIE_SSD_RX0_DP
[44] PCIE_SSD_TX0_DN
[44] PCIE_SSD_TX0_DP

[44] PCIE_SSD_RX1_DN
[44] PCIE_SSD_RX1_DP
[44] PCIE_SSD_TX1_DN
[44] PCIE_SSD_TX1_DP

[44] PCIE_SSD_RX2_DN
[44] PCIE_SSD_RX2_DP
[44] PCIE_SSD_TX2_DN
[44] PCIE_SSD_TX2_DP

[44] PCIE_SSD_RX3_DN
[44] PCIE_SSD_RX3_DP
[44] PCIE_SSD_TX3_DN
[44] PCIE_SSD_TX3_DP

CV7 PCIE7_RXN
CV6 PCIE7_RXP
DD3 PCIE7_TXN
DD5 PCIE7_TXP

CT6 PCIE8_RXN
CT7 PCIE8_RXP
DA3 PCIE8_TXN
DA5 PCIE8_TXP

CP7 PCIE9_RXN
CP6 PCIE9_RXP
DA2 PCIE9_TXN
DA1 PCIE9_TXP

CM7 PCIE10_RXN
CM6 PCIE10_RXP
CY3 PCIE10_TXN
CY4 PCIE10_TXP

CK7 PCIE11_RXN/SATA0_RXN
CK6 PCIE11_RXP/SATA0_RXP
CW2 PCIE11_TXN/SATA0_TXN
CW1 PCIE11_TXP/SATA0_TXP

CJ6 PCIE12_RXN/SATA1A_RXN
CJ7 PCIE12_RXP/SATA1A_RXP
CW5 PCIE12_TXN/SATA1A_TXN
CW3 PCIE12_TXP/SATA1A_TXP

CG7 PCIE13_RXN
CG6 PCIE13_RXP
CT3 PCIE13_TXN
CT5 PCIE13_TXP

CE6 PCIE14_RXN
CE7 PCIE14_RXP
CT2 PCIE14_TXN
CT1 PCIE14_TXP

CC5 PCIE15_RXN/SATA1B_RXN
CC6 PCIE15_RXP/SATA1B_RXP
CR3 PCIE15_TXN/SATA1B_TXN
CR4 PCIE15_TXP/SATA1B_TXP

CA6 PCIE16_RXN/SATA2_RXN
CA5 PCIE16_RXP/SATA2_RXP
CP1 PCIE16_TXN/SATA2_TXN
CP2 PCIE16_TXP/SATA2_TXP

[18] GPP_E0 — DW12 GPP_E0/SATAXPCIE0/SATAGP0
CR42 GPP_A12/SATAXPCIE1/SATAGP1
CR43 GPP_A13/SATAXPCIE2/SATAGP2

[45] USBA_OVCUR# — DW14 GPP_E9/USB_OC0
TP2402 — CT43 GPP_A16/USB_OC3

[79] TCP0_OC#
[18] GPP_E4 — DU12 GPP_E4/DEVSLP0
[18] GPP_E5 — DU11 GPP_E5/DEVSLP1
[57,76] TCON_VENDOR_ID — CV48 GPP_A11/SATA_DEVSLP2

DT38 GPP_H12/M2_SKT2_CFG0
DW38 GPP_H13/M2_SKT2_CFG1
[33,50] BT_DISABLE# — DV38 GPP_H14/M2_SKT2_CFG2
[33,50] WLAN_DISABLE# — DU38 GPP_H15/M2_SKT2_CFG3

PCIE_RCOMPN DN1 — PCIE_RCOMPN
R2401 100 PCIE_RCOMPP DN3 — PCIE_RCOMPP
0201S_P28-W35

M1042225-001

PCIE1_RXN/USB31_1_RXN DJ8
PCIE1_RXP/USB31_1_RXP DJ6
PCIE1_TXN/USB31_1_TXN DJ2
PCIE1_TXP/USB31_1_TXP DJ1

USB3_SL1_RXN4 [71]
USB3_SL1_RXP4 [71]
USB3_SL1_TXN4 [71]
USB3_SL1_TXP4 [71]

USB3 SL40

PCIE2_RXN/USB31_2_RXN DG9
PCIE2_RXP/USB31_2_RXP DG7
PCIE2_TXN/USB31_2_TXN DJ3
PCIE2_TXP/USB31_2_TXP DJ5

USB3_USBA_RX_DN [45]
USB3_USBA_RX_DP [45]
USB3_USBA_TX_DN [45]
USB3_USBA_TX_DP [45]

USB3 TYPE A AND BSSB

PCIE3_RXN/USB31_3_RXN DE7
PCIE3_RXP/USB31_3_RXP DE9
PCIE3_TXN/USB31_3_TXN DF3
PCIE3_TXP/USB31_3_TXP DF5

PCIE4_RXN/USB31_4_RXN DC7
PCIE4_RXP/USB31_4_RXP DC9
PCIE4_TXN/USB31_4_TXN DF2
PCIE4_TXP/USB31_4_TXP DF1

PCIE5_RXN/USB31_5_RXN DA6
PCIE5_RXP/USB31_5_RXP DA7
PCIE5_TXN/USB31_5_TXN DE4
PCIE5_TXP/USB31_5_TXP DE3

PCIE6_RXN/USB31_6_RXN CY7
PCIE6_RXP/USB31_6_RXP CY6
PCIE6_TXN/USB31_6_TXN DD1
PCIE6_TXP/USB31_6_TXP DD2

USB2N_1 DN8
USB2P_1 DP8
USB2_SL1_DN [71]
USB2_SL1_DP [71]

USB2 SL40

USB2N_2 DK11
USB2P_2 DJ11
USB2_USBA_DN [45]
USB2_USBA_DP [45]

USB2 USB-A PORT

USB2N_3 DP13
USB2P_3 DN13

USB2N_4 DK10
USB2P_4 DJ10
USB2_TCP0_DN [77]
USB2_TCP0_DP [77]

USB2 USB-C PORT1

USB2N_5 DL5
USB2P_5 DL3

USB2N_6 DP11
USB2P_6 DN11
CAM_USB_DM_SOC [54]
CAM_USB_DP_SOC [54]

USB2 Camera

USB2N_7 DK13
USB2P_7 DJ13

USB2N_8 DN6
USB2P_8 DP6

USB2N_9 DL2
USB2P_9 DL1

USB2N_10 DP10
USB2P_10 DN10

USB_ID — DL6 10K R2405

USB_VBUSSENSE — DL11 10K R2408

USB2_COMP — DN5 USB2_COMP R2402 113

UFS_RESET — CD3 TP2401

+1P8VSB
0201S_P28-W35 R2410 49.9K TCON_VENDOR_ID

Title: PCH(5)_PCIE,USB		
Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 24 of 82	

W x H 412 x 267 mm

SAM NEED DECIDE TO SET UEFI_TOP_SWAP HIGH OR LOW BEFORE ASSERT PCH_PWROK

[35] SAM_PCH_TOP_SWAP

R2518 100K DNP

+1P8V_PANEL

No reboot strap
Low: Disable (Default)
High:Enable

R2583 2.2K R2584 2.2K

[33,57] PANEL_I2C_SDA
[33,57] PANEL_I2C_SCL

+1P8VSB

R2533 100K R2536 100K R2524 100K R2509 100K

U1001F

6 OF 19

CH48	GPP_B16/GSPI0_CLK		GPP_D13/ISH_UART0_RXD
INT. PD CF48	GPP_B18/GSPI0_MOSI		GPP_D14/ISH_UART0_TXD
CF47	GPP_B17/GSPI0_MISO		GPP_D15/ISH_UART0_RTS_N/GSPI2_CS1_N/IMGCLKOUT5
CH49	GPP_B15/GSPI0_CS0		GPP_D16/ISH_UART0_CTS_N/CNV_WCEN
INT. PD CH47	GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1		
CL47			GPP_C12/UART1_RXD/ISH_UART1_RXD
CK47	GPP_B20/GSPI1_CLK		GPP_C13/UART1_TXD/ISH_UART1_TXD
CK46	GPP_B22/GSPI1_MOSI		GPP_C14/UART1_RTS_N/ISH_UART1_RTS
CH45	GPP_B21/GSPI1_MISO		GPP_C15/UART1_CTS_N/ISH_UART1_CTS
INT. PD CL48	GPP_B19/GSPI1_CS0		
	GPP_B23/SML1ALERT_N/PCHHOT_N/GSPI1_CS1		GPP_B5/ISH_I2C0_SDA
			GPP_B6/ISH_I2C0_SCL
DP21	GPP_C8/UART0_RXD		
DK21	GPP_C9/UART0_TXD		GPP_B7/ISH_I2C1_SDA
DL21	GPP_C10/UART0_RTS		GPP_B8/ISH_I2C1_SCL
DJ22	GPP_C11/UART0_CTS		
DT22			GPP_B9/I2C5_SDA/ISH_I2C2_SDA
DW22	GPP_C20/UART2_RXD		GPP_B10/I2C5_SCL/ISH_I2C2_SCL
DV22	GPP_C21/UART2_TXD	Should really be a space here in the symbol >	GPP_D0/ISH_GP0
DU22	GPP_C22/UART2_RTS		GPP_D1/ISH_GP1
	GPP_C23/UART2_CTS		GPP_D2/ISH_GP2
			GPP_D3/ISH_GP3
DT24	GPP_C16/I2C0_SDA		GPP_D17/ISH_GP4
DT23	GPP_C17/I2C0_SCL		GPP_D18/ISH_GP5
			GPP_E15/ISH_GP6
DW23	GPP_C18/I2C1_SDA		GPP_E16/ISH_GP7
DU23	GPP_C19/I2C1_SCL		
DU41	GPP_H4/I2C2_SDA		
DV41	GPP_H5/I2C2_SCL		
DW41	GPP_H6/I2C3_SDA		
DT41	GPP_H7/I2C3_SCL		
DT40			
DW40	GPP_H8/I2C4_SDA/CNV_MFUART2_RXD		
	GPP_H9/I2C4_SCL/CNV_MFUART2_TXD		

M1042225-001

[29,33,34] SAMTX_PCHRX
[29,33,34] PCHTX_SAMRX
[29,33,34,76] PCHRTS_SAMCTS
[29,33,34,76] SAMRTS_PCHCTS

[62] RTD3_AUD_PWR_1P8
[64] RTD3_AUD_PWR_5P0
[31,33] VOL_UP#
[31,33] VOL_DOWN#

ALL
R2598 0
R2597 0
ALL

PANEL_I2C_SDA_R
PANEL_I2C_SCL_R

[28,33,76] PMI_I2C_SDA
[28,33,76] PMI_I2C_SCL

[77] PD_SML0_SCL 0 R2501
[77] PD_SML0_SDA 0 R2502

Removed connections from pins DK24 and DJ24 (page21)
Connecting them to page 25 PMI_I2C I2C1
0ohm straps refdes changed to match with page number

[54,76] PCH_SENSOR_I2C_SDA
[54,76] PCH_SENSOR_I2C_SCL

DV33 TPANEL_RST#_R R2511 0 TPANEL_RST# [30,33,35]
DW33
DT33 RTD3_CAM_PWREN_R R2517 1K RTD3_TPANEL_PWR [62,64]
DU33 FLASH_PROTECT#_R R2515 0 RTD3_CAM_PWREN [54,76]
FLASH_PROTECT# [30]

TP2523
TP2518

DK22 R2513 0 Debug UART PCH_DBG_RX [29,33,76]
DW24 R2505 0 PCH_DBG_TX [29,33,76]
DV24
DU24 MEM_CONFIG

+3P3VSB
R2590 100K R2589 100K

CN43
CN42
CN41
CL43
CL41
CJ39
DU36
DV36 ACS_INT# [54]
DW36 TP2532
DT36 GPP_D3
DU34
DW34
DT14 TP2501
DU14 ISH_SAM_INT [34]

+3P3VSB
DBG_D R2525 1K
-4mA sync capability on 3.3V GPIO
A
DBG_D LED2501 RED
K Red

R2599 DBG_D0 ISH_DBG

+1P8VSB
R2537 10K DNP
MEM_CONFIG
LOW: A,B,C,D CHANNEL ENABLE
HIGH: A,C CHANNEL ENABLE
R2526 10K

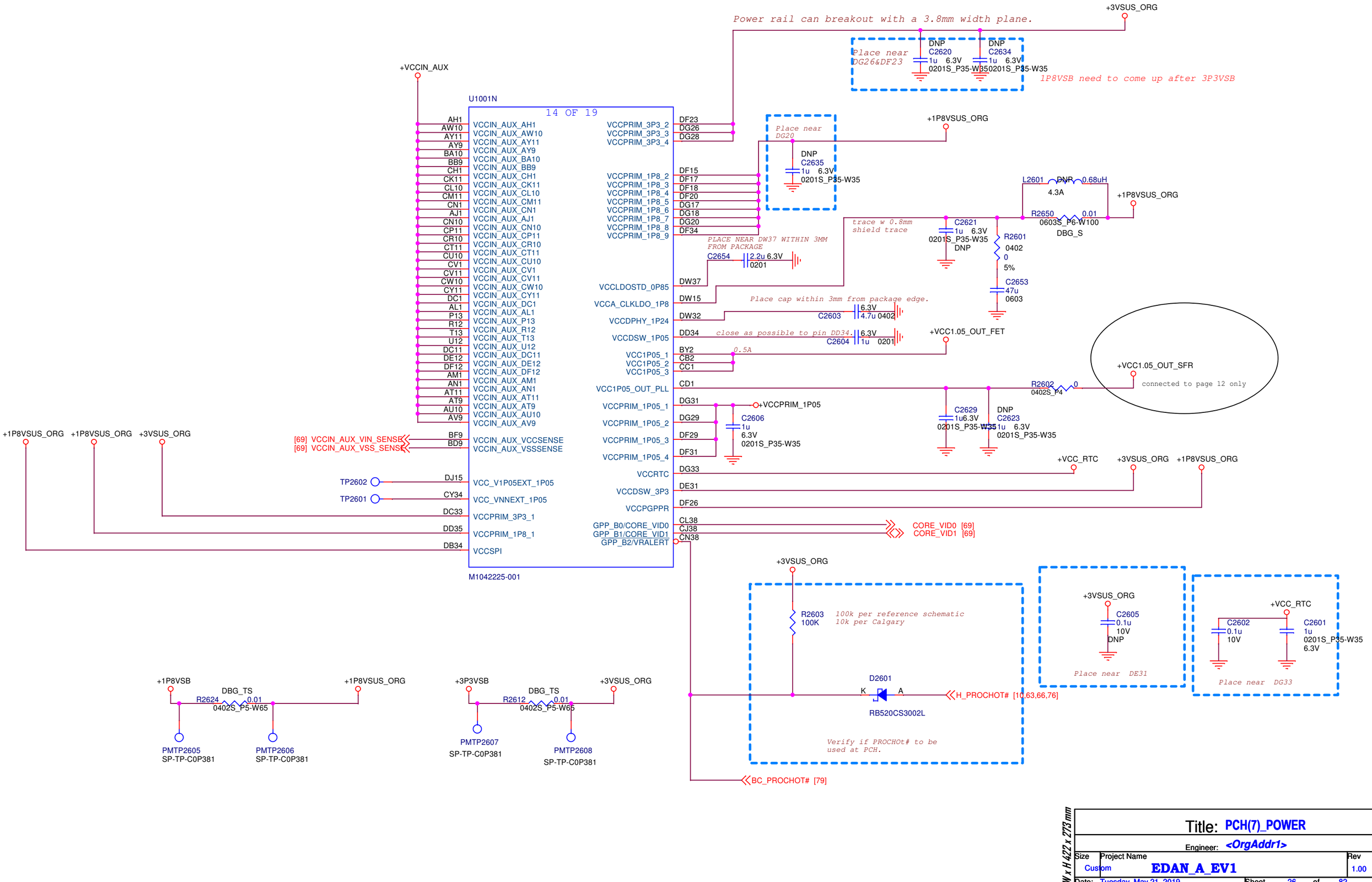
R2508 49.9K 0201S_P28-W35 ISH_SAM_INT
R2572 49.9K 0201S_P28-W35 RTD3_AUD_PWR_1P8
R2595 49.9K 0201S_P28-W35 RTD3_AUD_PWR_5P0
R2559 49.9K 0201S_P28-W35 RTD3_TPANEL_PWR
R2596 10K 0201S_P28-W35 DNP TPANEL_RST#
R2592 49.9K 0201S_P28-W35 ALL RTD3_CAM_PWREN

CPUNSSC Clock Frequency

GPP_B23/SML1ALERT#/ PCHHOT#/GSPI1_CS1#	
0 **Default**	38.4MHz (crystal)
1	19.2MHz (internal divider)

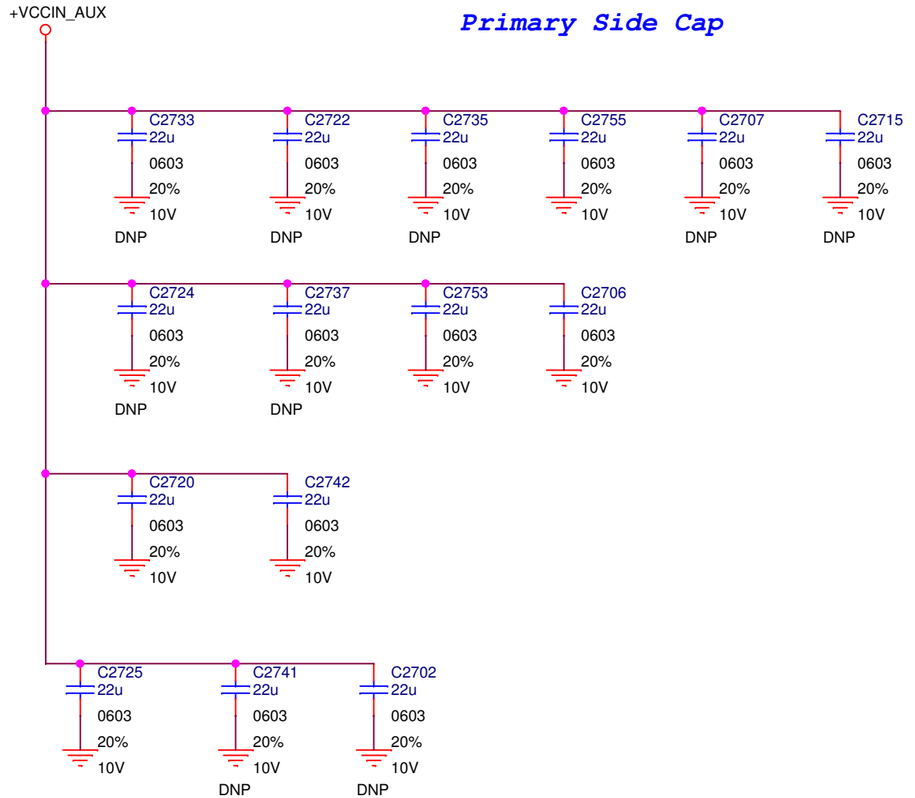
W x H 417 x 270mm

Title: PCH(6)_CPU,GPIO,MISC
Engineer: <OrgAddr1>
Size: Custom | Project Name: EDAN_A_EV1 | Rev: 1.00
Date: Tuesday, May 21, 2019 | Sheet 25 of 82



W x H 422 x 273 mm

Title: PCH(7)_POWER		
Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 26 of 82	



W x H 377 x 244 mm

Title: PCH(8)_decoupling		
Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 27 of 82	

+3P3VSB — R2801 DBG_TS_0.1 — +3P3V_PMI

+3P3V_PMI
Imax=0.0042A

+3P3V_PMI — 2K / 2K — R2862 / R2863 — ALL ALL — Ir*2 = 730uA

[25,33,76] PMI_I2C_SCL — ALL R2854 0 — PMI1_I2C_SCL_R [76]
[25,33,76] PMI_I2C_SDA — ALL R2855 0 — PMI1_I2C_SDA_R [76]

Changed Build-opt to ALL for pull-ups and 0ohm as Burnside Bridge is connected to the same I2C

DBG_T R2874 0 0201S_P28-W35 — PM_DBG_I2C_SCL [29]
DBG_T R2875 0 0201S_P28-W35 — PM_DBG_I2C_SDA [29]
to debug connector

MAX34417 VDD Average Supply Current
700uA PDNB=VIO and SLOW=GND
10uA PDNB=VIO and SLOW=VIO
2uA PDNB=GND

6x700uA=4.2mA
3.3Vx4.2mA=13.86mW

U2813 — A — Address(7b) = 0x10

Avila +VSYS while Carmel monitors +3P3VAS

[69] PM_VCCIN_AUX_IN+ / [69] PM_VCCIN_AUX_IN- — A3 / A2 — IN1+ / IN1-
[34] PM_+1P8V_SAM+ / [34] PM_+1P8V_SAM- — A1 / B1 — IN2+ / IN2-
[63] PM_VSYS+ / [63] PM_VSYS- — D1 / C1 — IN3+ / IN3-
[62] PM_1P8VSB_IN+ / [62] PM_1P8VSB_IN- — D3 / D2 — IN4+ / IN4-

VDD A4 — +3P3V_PMI — DBG_T C2825 0.1u 10V 0201S_P33-W39 — GND
VIO B2
SCL C4 — PMI0_ADDR
SDA D4
PDN B3 — PMI0_PDN_N R2856 10K 0201S_P28-W35 — +3P3V_PMI
SLOW C3 — GND
ADDR C2 — PMI0_ADDR
GND B4 — DBG_T R2866 0 0201S_P28-W35 — GND

MAX34417 — DBG_T — +3P3V_PMI

Ir=12uA

U2802 — B — Address(7b) = 0x12

Avila +5VSB while Carmel monitors PM_BLADE_IN+

[59] PM_5VSB_IN+ / [59] PM_5VSB_IN- — A3 / A2 — IN1+ / IN1-
[59] PM_3P3VSB_IN+ / [59] PM_3P3VSB_IN- — A1 / B1 — IN2+ / IN2-
[65] PM_3P3V_SSD+ / [65] PM_3P3V_SSD- — D1 / C1 — IN3+ / IN3-
[65] PM_3P3V_WWAN+ / [65] PM_3P3V_WWAN- — D3 / D2 — IN4+ / IN4-

VDD A4 — +3P3V_PMI — DBG_T C2801 0.1u 10V 0201S_P33-W39 — GND
VIO B2
SCL C4
SDA D4
PDN B3 — PMI1_PDN_N R2865 10K 0201S_P28-W35 — +3P3V_PMI
SLOW C3 — GND
ADDR C2 — PMI1_ADDR — DBG_T R2864 499 0201S_P28-W35 — GND
GND B4 — GND GND

MAX34417 — DBG_T

Part B
5VSB
3P3 VSB
1P8 VSB
3P3V WWAN

U2803 — C — Address(7b) = 0x14

[67] PM_VCCIN_IN+ / [67] PM_VCCIN_IN- — A3 / A2 — IN1+ / IN1-
[60] PM_1P1V_DDR_VDD2_IN+ / [60] PM_1P1V_DDR_VDD2_IN- — A1 / B1 — IN2+ / IN2-
[65] PM_3P3V_PANEL_IN+ / [65] PM_3P3V_PANEL_IN- — D1 / C1 — IN3+ / IN3-
[72] PM_BKLT_IN+ / [72] PM_BKLT_IN- — D3 / D2 — IN4+ / IN4-

VDD A4 — +3P3V_PMI — DBG_T C2802 0.1u 10V 0201S_P33-W39 — GND
VIO B2
SCL C4
SDA D4
PDN B3 — PMI2_PDN_N R2867 10K 0201S_P28-W35 — +3P3V_PMI
SLOW C3 — GND
ADDR C2 — PMI2_ADDR — DBG_T R2850 931 0201S_P28-W35 — GND
GND B4 — GND GND

MAX34417 — DBG_T

Part C
3P3 Panel
Display Backlight
3P3V SSD

Title:	Power Monitor		
Engineer:	<OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 28 of 82		

W:11.577 x 8.173 mm

keep USB2 traces as short as possible between muxes

U2901 PI3USB14-AZHE DBG_D
U2902 PI3USB14-AZHE DBG_D
U2903 PI3USB14-AZHE DBG_D
U2905 PI3USB14-AZHE DBG_D
U2906 74LVC1G32GX DBG_D
U2908 SN74LV1T02DCKR DBG_D
U2909 74AUP1G08GX DFN5_P85XP85XP4_P48
U2910 SN74LV1T08DCKR DBG_D
U2911 SN74LV1T08DCKR DBG_D
U2912 PI3USB14-AZHE DBG_D

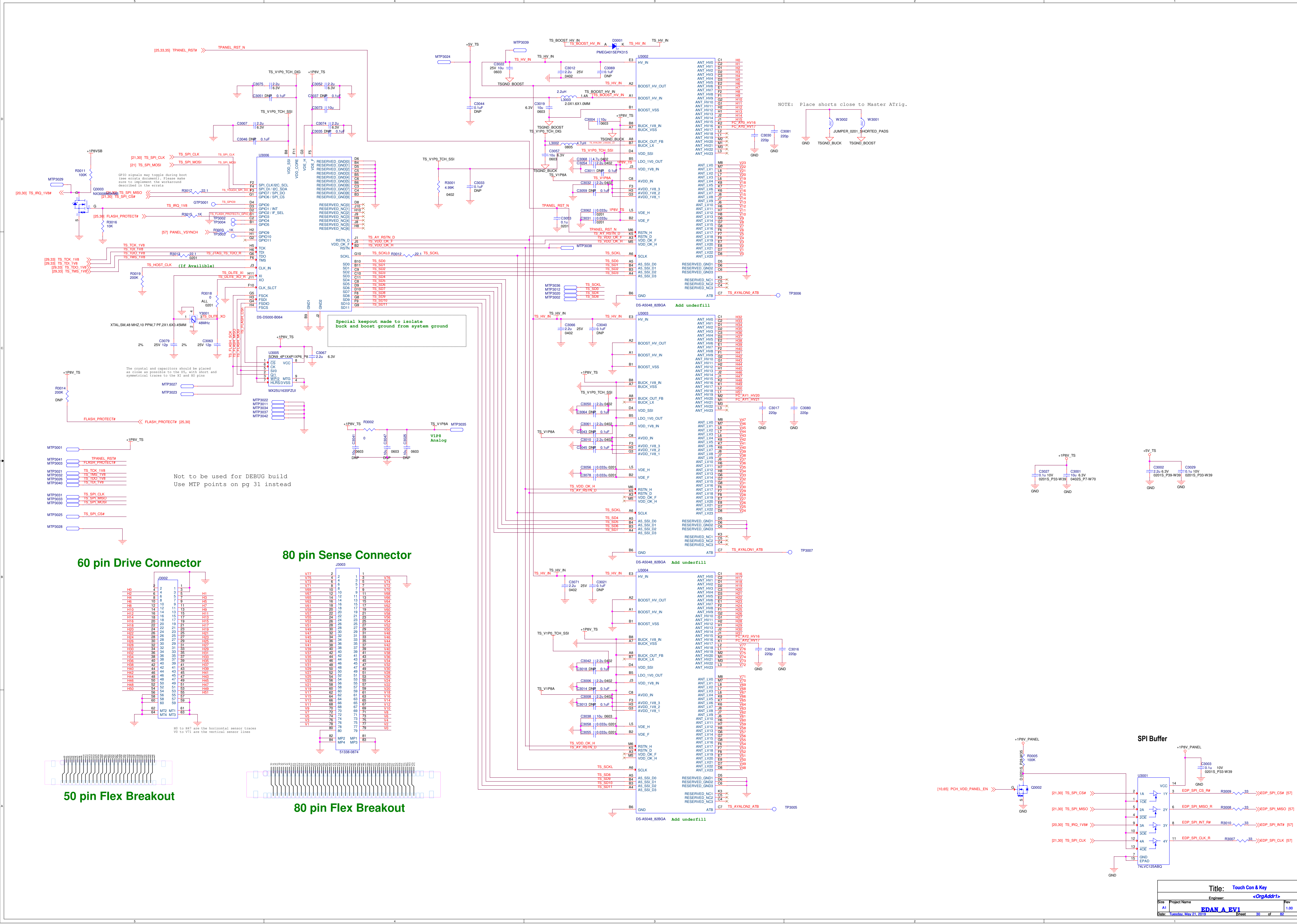
Q2902 Q2905

R2923 100K 1% 0201 DBG_D
R2909 100K 1% 0201 DBG_D
R2903 0 DBG_D
R2910 0 DBG_D
R2917 100K 1% 0201 DBG_D
R2916 100K 1% 0201 DBG_D
R2915 100K 1% 0201 DBG_D
R2914 100K 1% 0201 DBG_D
R2907 100K 0201 DBG_D
R2901 100K DBG_D
R2905 1K DBG_D
R2924 100K DBG_D
R2902 0 0201S_P28-W35
R2908 DBG_N 0
R2906 DBG_N 0

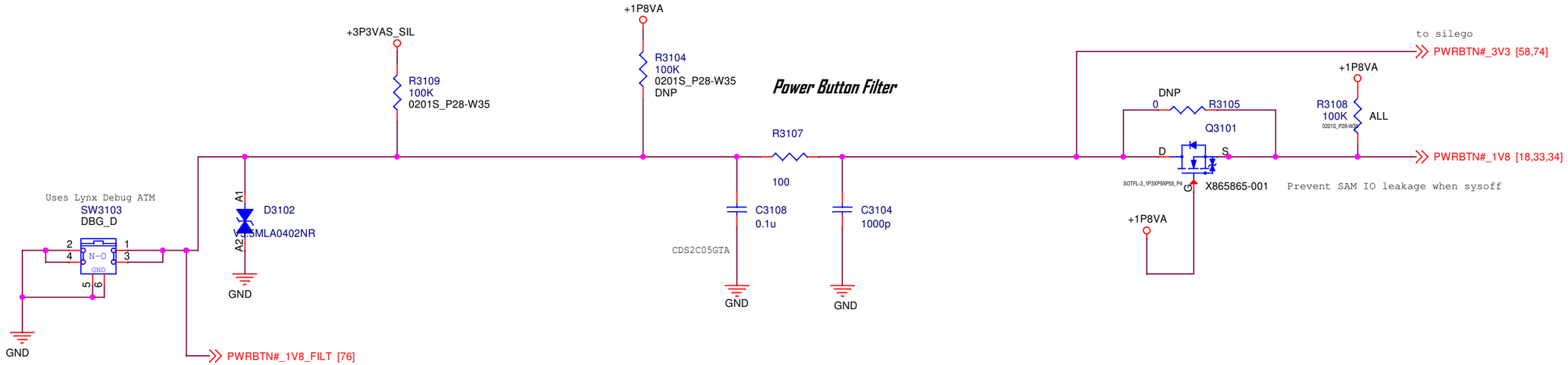
Debug MUX Selection table for Camino POC2

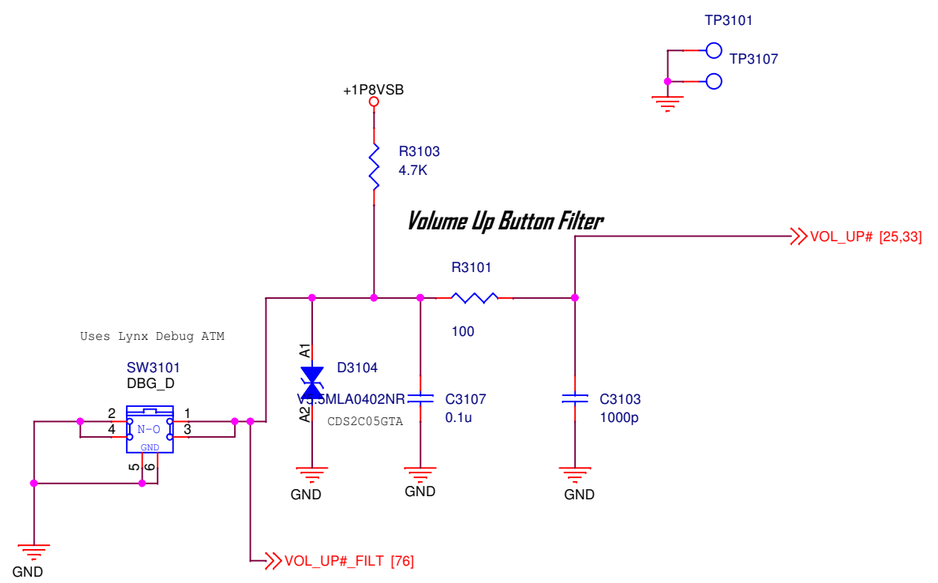
MUX0_EN#	PD_USB2_MUX_FLIP	USBC_MUX3_SEL	USBC_MUX2_SEL	USBC_MUX1	USBC_MUX0	PD_SAM_DBG_ACC_MODE	USBC_MUX4_SEL	USB-C OUTPUT SIGNALS	Function
1	0	X	X	X	X	0	X	USB2_TCP0_DP & USB2_TCP0_DN on A-side, TCP0_BB_SBU1, TCP0_BB_SBU2	Normal function w/ polarity-A
1	1	X	X	X	X	0	X	USB2_TCP0_DP & USB2_TCP0_DN on B-side, TCP0_BB_SBU1, TCP0_BB_SBU2	Normal function w/ polarity-B
0	X	0	0	X	X	1	0	SWD_CLK, SWD_DIO, SWD_SWO SAM_RESET#, SAM_DBG_RX, SAM_DBG_TX	SAM Programming + SAM DBG (Debug Default mode)
0	X	0	1	X	X	1	1	PCH_JTAG_TCK, PCH_JTAG_TDI, PCH_JTAG_TDO, PCH_JTAG_TMS, XDP_TCK_MUX, SAM_DBG_TX	PCH/CPU JTAG Mode + SAM Logging
0	X	1	0	X	X	1	0	PCH_DBG_TX, PCH_DBG_RX, PM_DBG_I2C_SCL PM_DBG_I2C_SDA, SAM_DBG_RX, SAM_DBG_TX	PCH UART + PM I2C + SAM DBG
0	X	1	1	0	0	1	0	SAM_BLADE_UART_TX_DBG, SAM_BLADE_UART_RX_DBG, LTE_UART_TX, LTE_UART_RX, SAM_DBG_RX, SAM_DBG_TX	Blade UART & LTE + SAM DBG
0	X	1	1	0	1	1	0	TS_TCK_1V8, TS_TDI_1V8, TS_TDO_1V8, TS_TMS_1V8, SAM_DBG_RX, SAM_DBG_TX	Touch JTAG + SAM DBG
0	X	1	1	1	0	1	0	KIP_SWD_CLK, KIP_SWD_DIO, KIP_TRACE_SWO, SAM_KIP_RST, SAM_DBG_RX, SAM_DBG_TX	KIP Programming + SAM DBG
0	X	1	1	1	1	1	0	SAMTX_PCHRX, PCHTX_SAMRX, SAM_PD_SCL, SAM_PD_SDA, SAM_DBG_RX, SAM_DBG_TX	SAM-PCH UART + SAM-PD I2C + SAM DBG

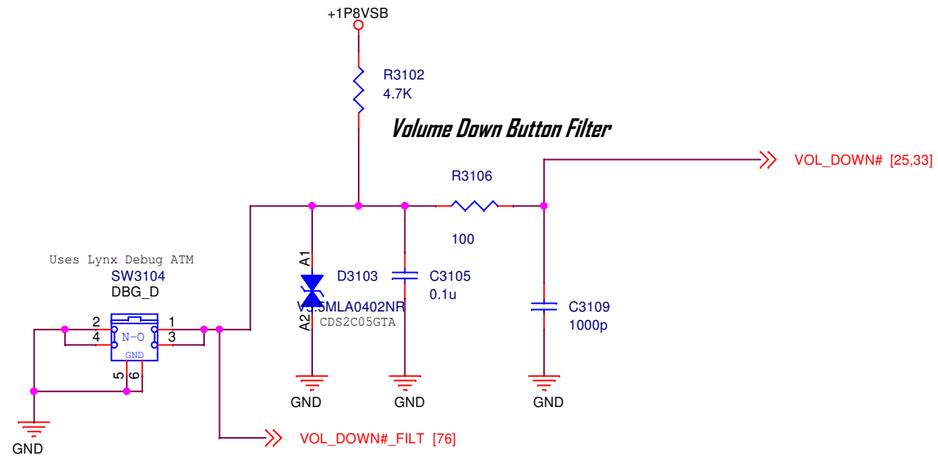
Title: Type-C Debug
Engineer: <OrgAddr1>
Size: Custom
Project Name: EDAN_A_EV1
Rev: 1.00
Date: Tuesday, May 21, 2019
Sheet 29 of 82
W x H 377 x 244 mm



NOTE: Place shorts close to Master ATrig.
JUMPER_0201_SHORTED_PADS
GPIO signals may toggle during boot (see errata document). Please make sure to implement the workaround described in the errata
Special keepout made to isolate buck and boost ground from system ground
The crystal and capacitors should be placed as close as possible to the D5, with short and symmetrical traces to the XI and XO pins
XTAL,SM,48 MHZ,10 PPM,7 PF,2X1.6X0.45MM
Not to be used for DEBUG build
Use MTP points on pg 31 instead
V1P8 Analog
DS-D5000-B064
DS-A5048_82BGA
Add underfill
MX25U1635FZUI
60 pin Drive Connector
80 pin Sense Connector
50 pin Flex Breakout
80 pin Flex Breakout
H0 to H87 are the horizontal sensor traces
V0 to V71 are the vertical sensor lines
51338-0874
SPI Buffer
74LVC125ABQ
Title: Touch Con & Key
Engineer: <OrgAddr1>
Size A1
Project Name EDAN_A_EV1
Rev 1.00
Date: Tuesday, May 21, 2019
Sheet 30 of 82







Report errors to Steven

WxH 422 x 273 mm

Title: Button & Diagnostic Conn

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		1.00
Date: Tuesday, May 21, 2019	Sheet 31 of 82	

W x H 322 x 225 mm

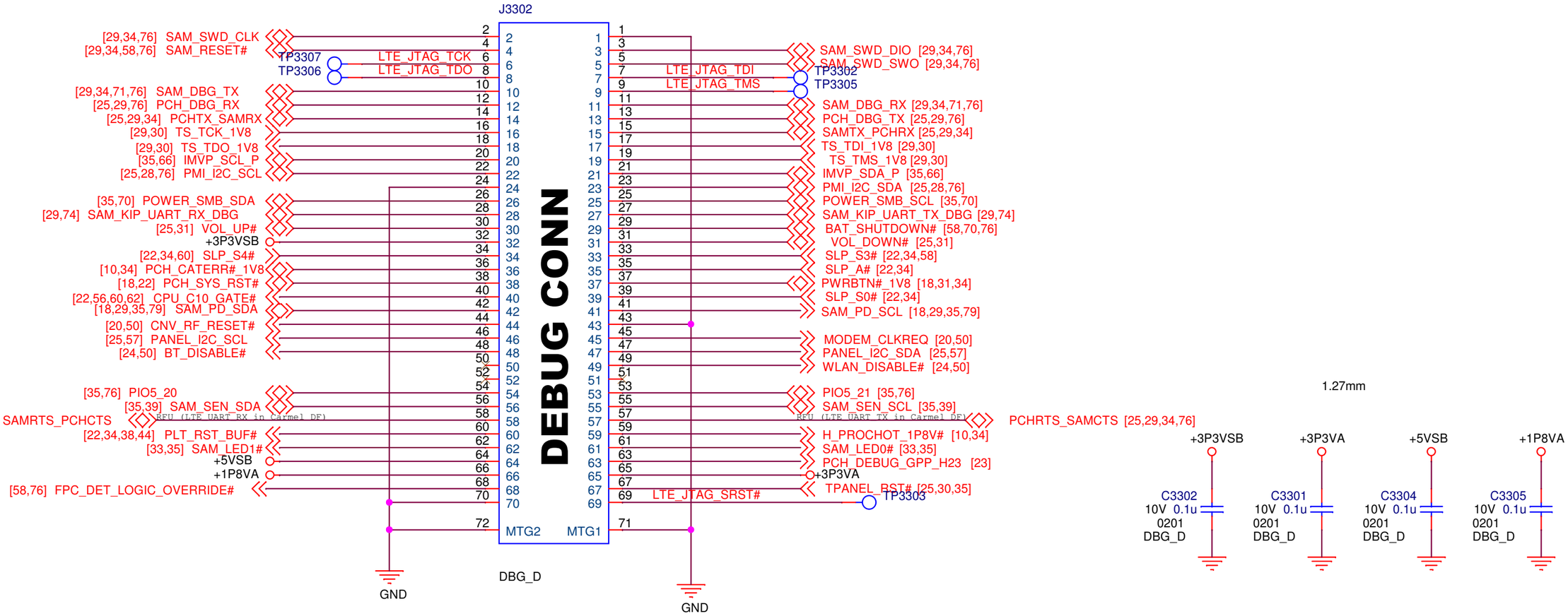
Cethera Sensor Connection

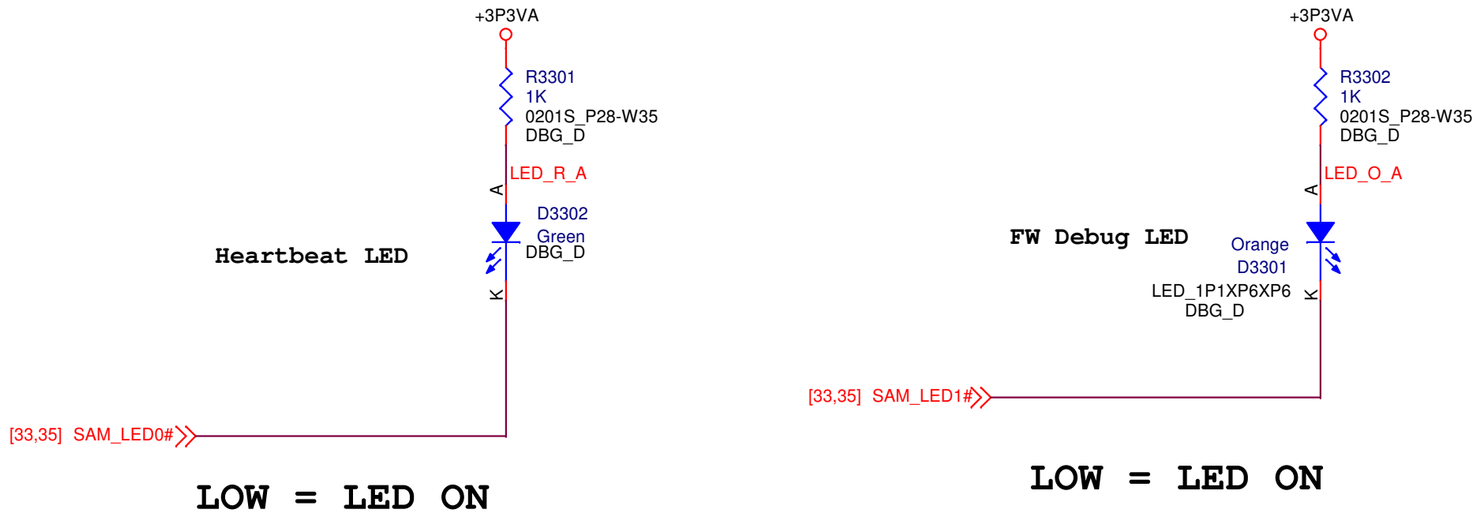
Title:

Engineer: <OrgAddr1>

Size	Project Name	Rev
A2	EDAN_A_EV1	1.00

Date: Tuesday, May 21, 2019 Sheet 32 of 82

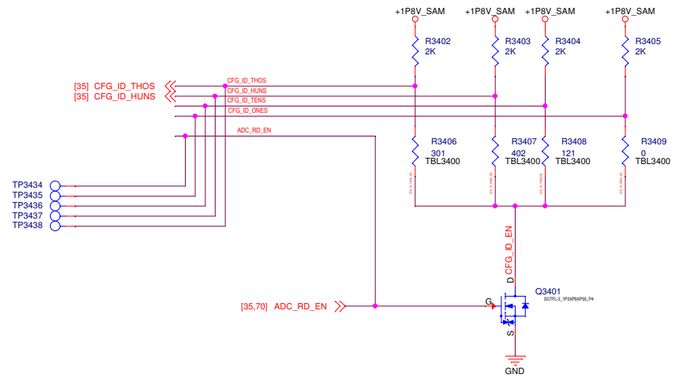

J3302
DEBUG CONN
MTG2
MTG1
DBG_D
[29,34,76] SAM_SWD_CLK
[29,34,58,76] SAM_RESET#
TP3307
TP3306
LTE_JTAG_TCK
LTE_JTAG_TDO
[29,34,71,76] SAM_DBG_TX
[25,29,76] PCH_DBG_RX
[25,29,34] PCHTX_SAMRX
[29,30] TS_TCK_1V8
[29,30] TS_TDO_1V8
[35,66] IMVP_SCL_P
[25,28,76] PMI_I2C_SCL
[35,70] POWER_SMB_SDA
[29,74] SAM_KIP_UART_RX_DBG
[25,31] VOL_UP#
+3P3VSB
[22,34,60] SLP_S4#
[10,34] PCH_CATERR#_1V8
[18,22] PCH_SYS_RST#
[22,56,60,62] CPU_C10_GATE#
[18,29,35,79] SAM_PD_SDA
[20,50] CNV_RF_RESET#
[25,57] PANEL_I2C_SCL
[24,50] BT_DISABLE#
[35,76] PIO5_20
[35,39] SAM_SEN_SDA
[25,29,34,76] SAMRTS_PCHCTS
RFU (LTE UART RX in Carmel DF)
[22,34,38,44] PLT_RST_BUF#
[33,35] SAM_LED1#
+5VSB
+1P8VA
[58,76] FPC_DET_LOGIC_OVERRIDE#
GND
SAM_SWD_DIO [29,34,76]
SAM_SWD_SWO [29,34,76]
LTE_JTAG_TDI
LTE_JTAG_TMS
TP3302
TP3305
SAM_DBG_RX [29,34,71,76]
PCH_DBG_TX [25,29,76]
SAMTX_PCHRX [25,29,34]
TS_TDI_1V8 [29,30]
TS_TMS_1V8 [29,30]
IMVP_SDA_P [35,66]
PMI_I2C_SDA [25,28,76]
POWER_SMB_SCL [35,70]
SAM_KIP_UART_TX_DBG [29,74]
BAT_SHUTDOWN# [58,70,76]
VOL_DOWN# [25,31]
SLP_S3# [22,34,58]
SLP_A# [22,34]
PWRBTN#_1V8 [18,31,34]
SLP_S0# [22,34]
SAM_PD_SCL [18,29,35,79]
MODEM_CLKREQ [20,50]
PANEL_I2C_SDA [25,57]
WLAN_DISABLE# [24,50]
PIO5_21 [35,76]
SAM_SEN_SCL [35,39]
RFU (LTE UART TX in Carmel DF)
PCHRTS_SAMCTS [25,29,34,76]
H_PROCHOT_1P8V# [10,34]
SAM_LED0# [33,35]
PCH_DEBUG_GPP_H23 [23]
+3P3VA
TPANEL_RST# [25,30,35]
LTE_JTAG_SRST#
TP3303
GND
1.27mm
+3P3VSB
+3P3VA
+5VSB
+1P8VA
C3302
10V 0.1u
0201
DBG_D
C3301
10V 0.1u
0201
DBG_D
C3304
10V 0.1u
0201
DBG_D
C3305
10V 0.1u
0201
DBG_D


+3P3VA
R3301
1K
0201S_P28-W35
DBG_D
LED_R_A
A
D3302
Green
DBG_D
K
Heartbeat LED
[33,35] SAM_LED0#
LOW = LED ON

+3P3VA
R3302
1K
0201S_P28-W35
DBG_D
LED_O_A
A
Orange
D3301
LED_1P1XP6XP6
DBG_D
K
FW Debug LED
[33,35] SAM_LED1#
LOW = LED ON

System Aggregator Module

Configuration ID TBD



TBL 3400

SKU ID - ADC0 - CFG_ID_ONES - PIO0_15/ADC0_3						
Hex number	Binary	Decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	dTPM + Wifi
1	0001	1	121	115	309	n/a
2	0010	2	210	310	464	No TPM + Wifi
3	0011	3	301	465	607	n/a
4	0100	4	402	608	755	
5	0101	5	510	756	904	
6	0110	6	634	905	1078	
7	0111	7	806	1079	1271	
8	1000	8	1000	1272	1485	Reserved for SW ID
9	1001	9	1300	1486	1756	n/a
A	1010	10	1740	1757	2060	Reserved for SW ID
B	1011	11	2370	2061	2398	n/a

Memory ID - ADC1 - CFG_ID_TENS - PIO0_16/ADC0_4						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	LP4x_2GB_K4U6E3S4AA-MGCL_SAMSUNG_M1100585-001
1	0001	1	121	115	309	LP4x_4GB_K4UBE3D4AA-MGCL_SAMSUNG_M1100590-001
2	0010	2	210	310	464	LP4x_8GB_K4UCE3Q4AA-MGCL_SAMSUNG_M1100591-001
3	0011	3	301	465	607	
4	0100	4	402	608	755	
5	0101	5	510	756	904	LP4x_2GB_H9HCNNNBKMALHR-NEE_Hynix_M1102096-001
6	0110	6	634	905	1078	LP4x_4GB_H9HCNNNCPMALHR-NEE_Hynix_M1102097-001

Build ID - ADC2 - CFG_ID_HUNS - PIO2_0/ADC0_7						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	EV1
1	0001	1	121	115	309	EV1.1
2	0010	2	210	310	464	EV1.5
3	0011	3	301	465	607	EV2
4	0100	4	402	608	755	DV

Program ID - ADC3 - CFG_ID_THOS - PIO2_1/ADC0_8						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	
0	0000	0	1	0	114	
1	0001	1	121	115	309	
2	0010	2	210	310	464	
3	0011	3	301	465	607	Edan

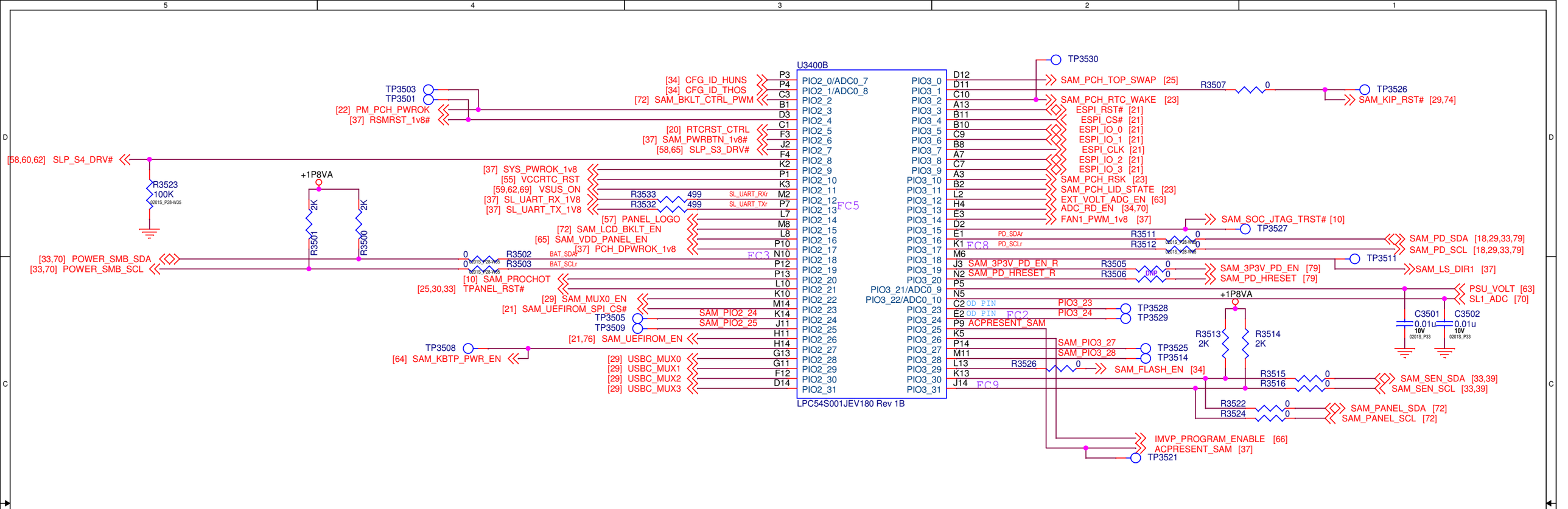
W x H 402 x 298 mm

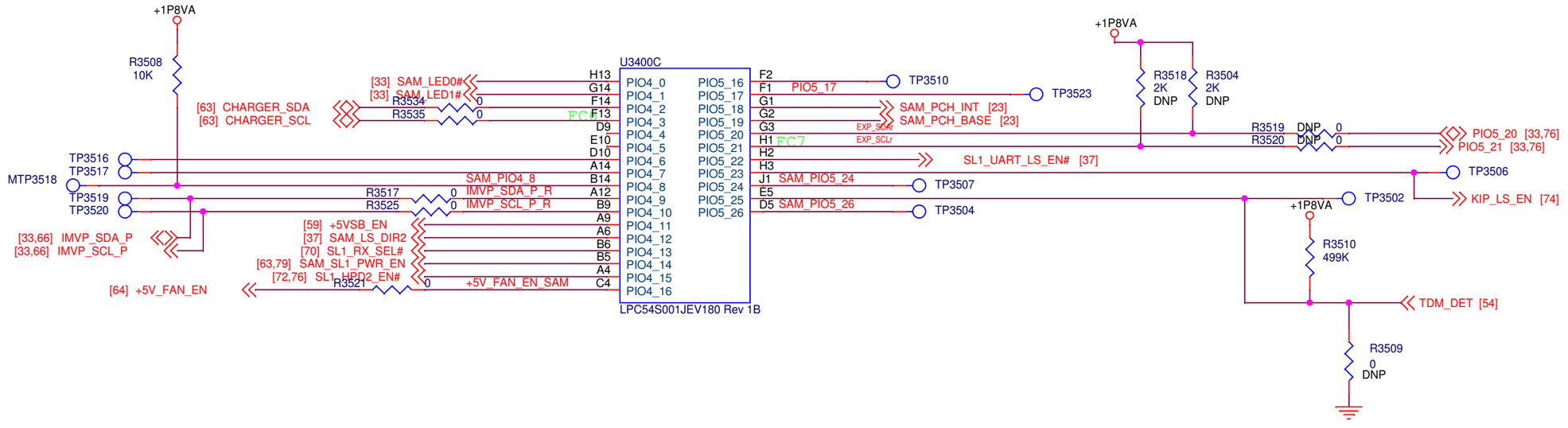
Title: **SAM Power, ADC, & Debug**

<OrgName> Engineer: <OrgAddr1>

Size A2 | Project Name: **EDAN_A_EV1** | Rev 1.00

Date: Tuesday, May 21, 2019 | Sheet 34 of 82





Title: SAM Buses			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 35 of 82		

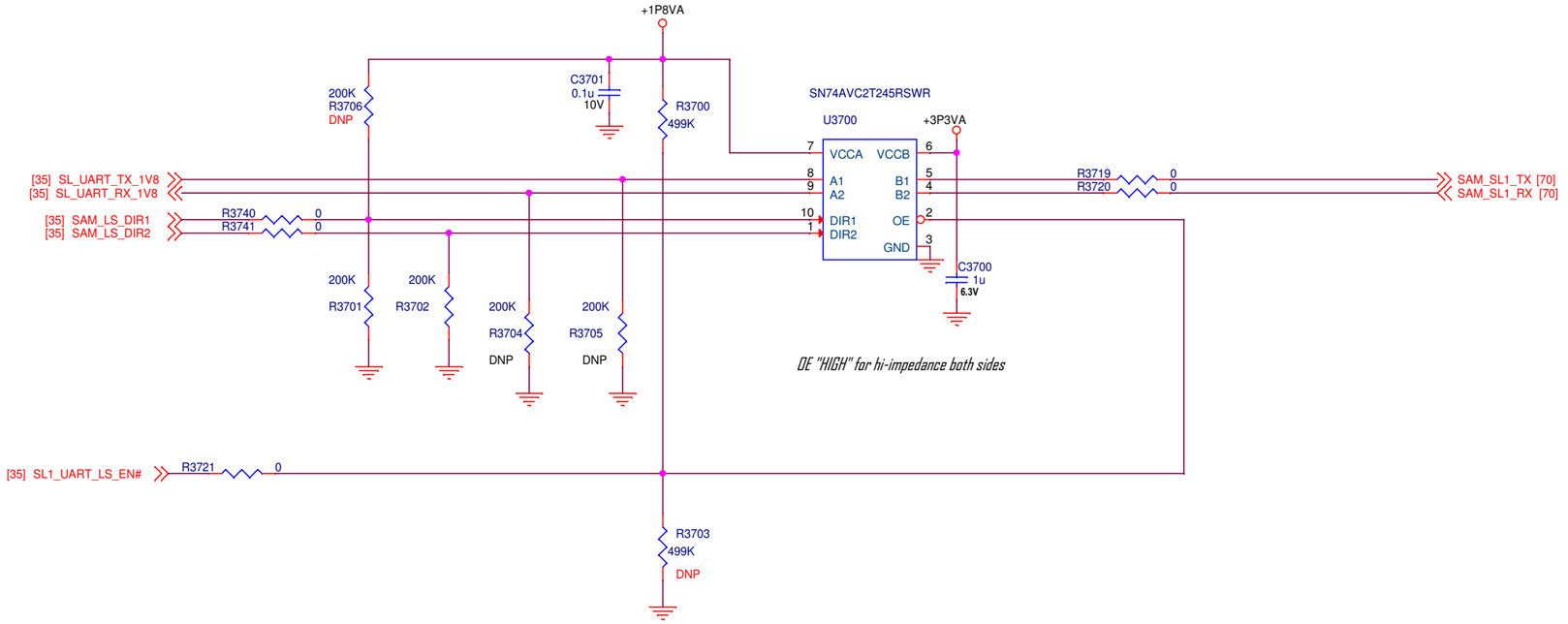
W x H 397 x 257 mm

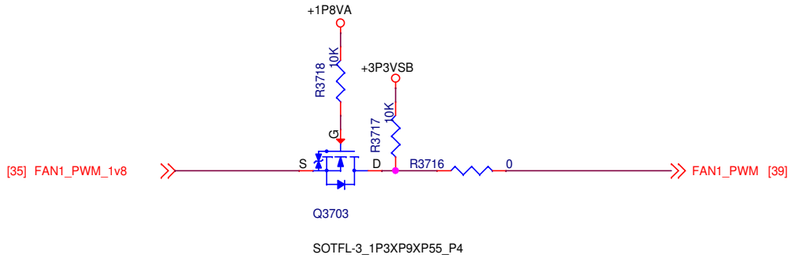
Title: *Blank*

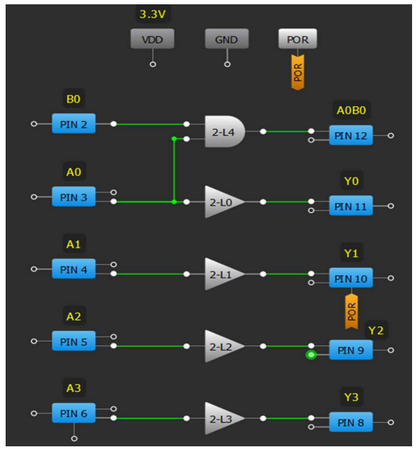
<OrgName> Engineer: *<OrgAddr1>*

Size	Project Name	Rev
A1	**EDAN_A_EV1**	1.00

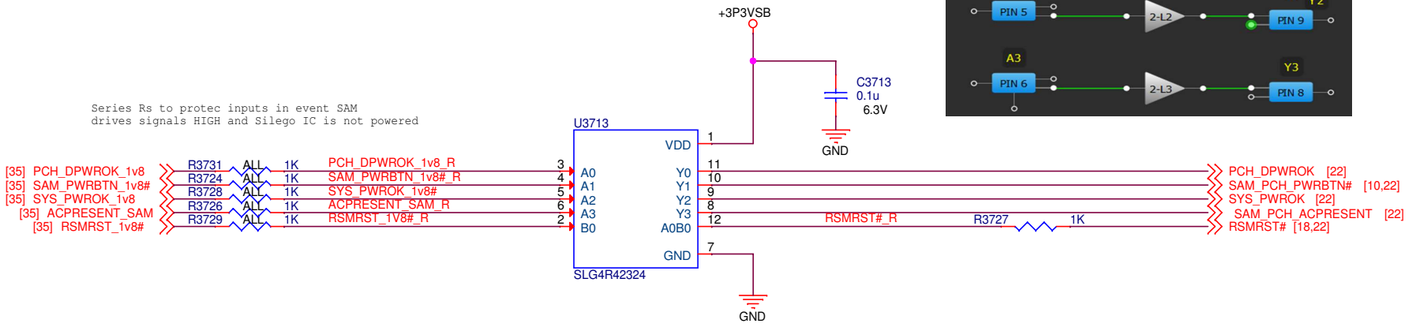
Date: Tuesday, May 21, 2019 Sheet 36 of 82







[29,79] PD_SAM_DBG_ACC_MODE — R3709 0 — PD_SAM_DBG_ACC_MODE_1V8 [34]



20170908sjs1428
title is: SAM Level shifters

Report errors to Steven

WxH 472 x 305mm

Title: SAM Level Shifters

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00

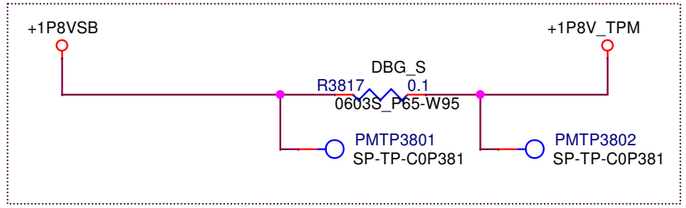
Date: Tuesday, May 21, 2019 Sheet 37 of 82

Trusted Platform Module

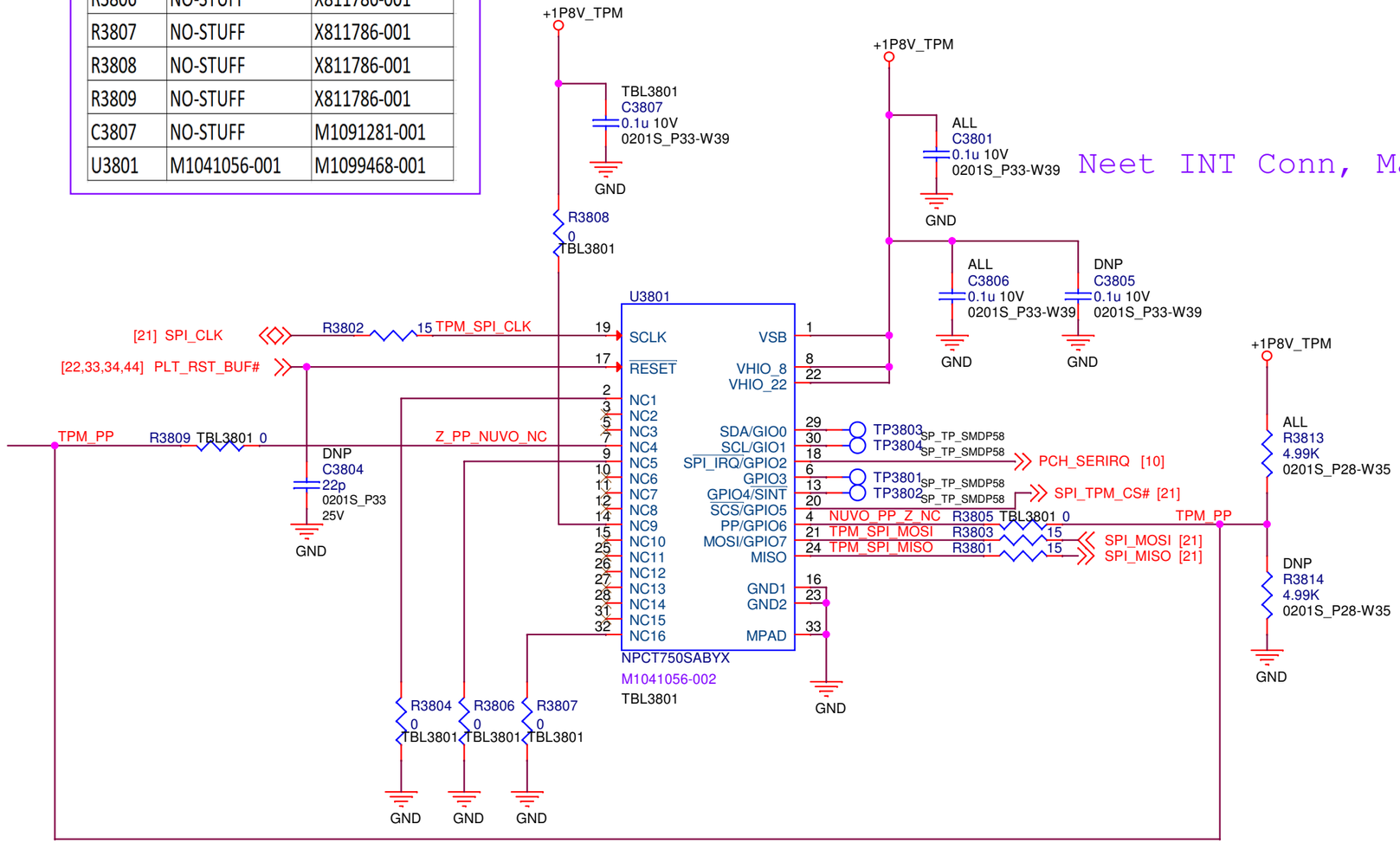
TBL3801

TBL3801

Ref	Nuvoton	NationZ
R3804	NO-STUFF	X811786-001
R3805	X811786-001	NO-STUFF
R3806	NO-STUFF	X811786-001
R3807	NO-STUFF	X811786-001
R3808	NO-STUFF	X811786-001
R3809	NO-STUFF	X811786-001
C3807	NO-STUFF	M1091281-001
U3801	M1041056-001	M1099468-001



Neet INT Conn, May need add'l cfg for NatZ



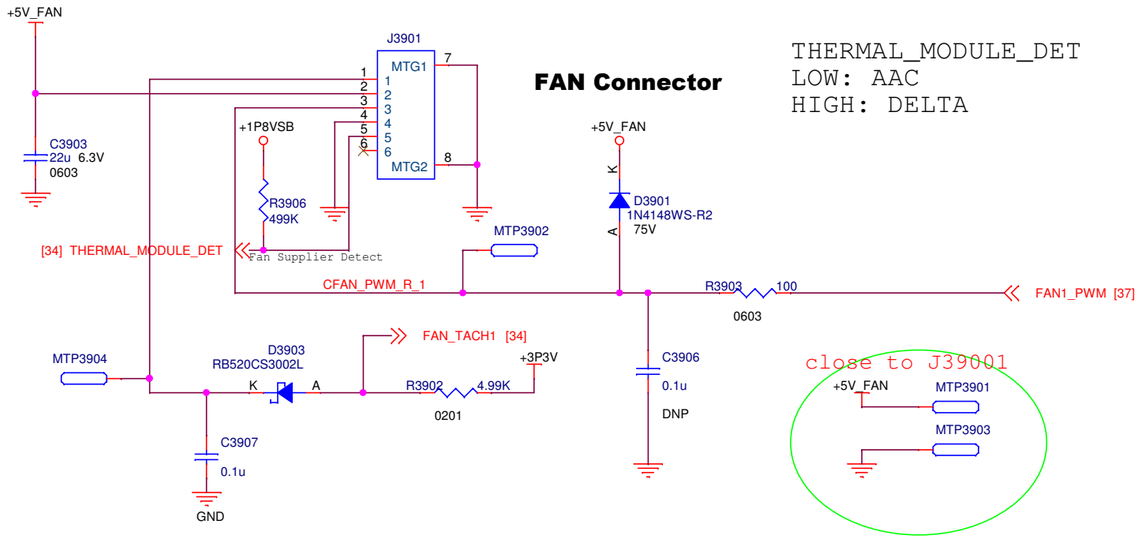
W x H 357 x 231 mm

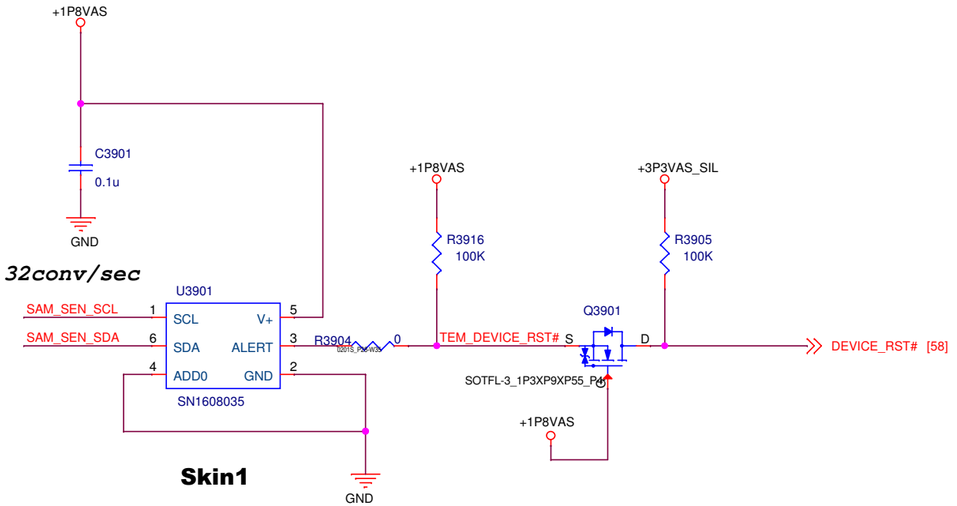
Title: TPM			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 38 of 82		

+5V_FAN
Imax=0.7A
Trace Width>30mil

FAN Connector

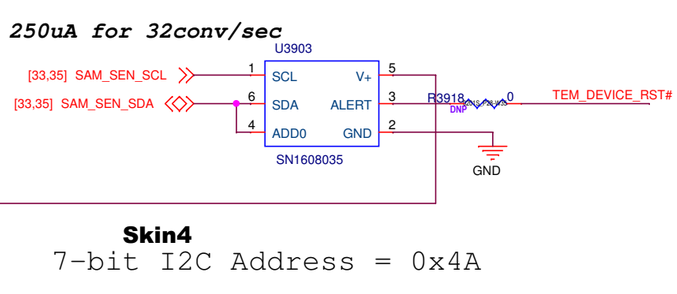
THERMAL_MODULE_DET
LOW: AAC
HIGH: DELTA





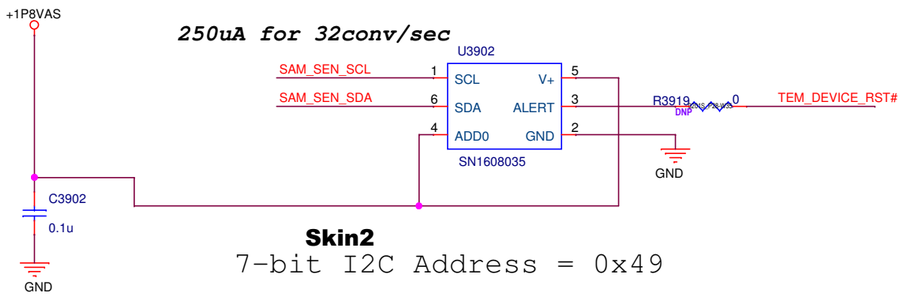
Skin1

7-bit I2C Address = 0x48



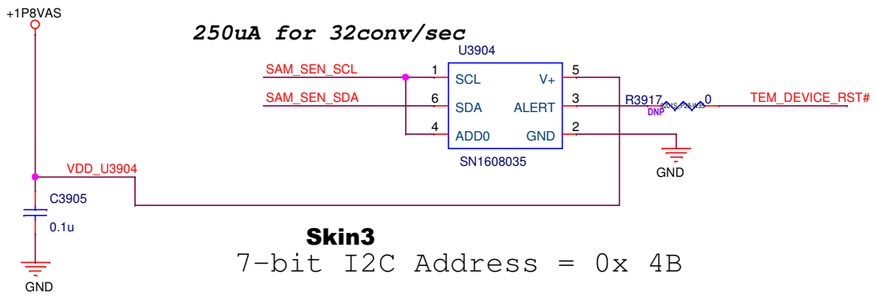
Skin4

7-bit I2C Address = 0x4A



Skin2

7-bit I2C Address = 0x49



Skin3

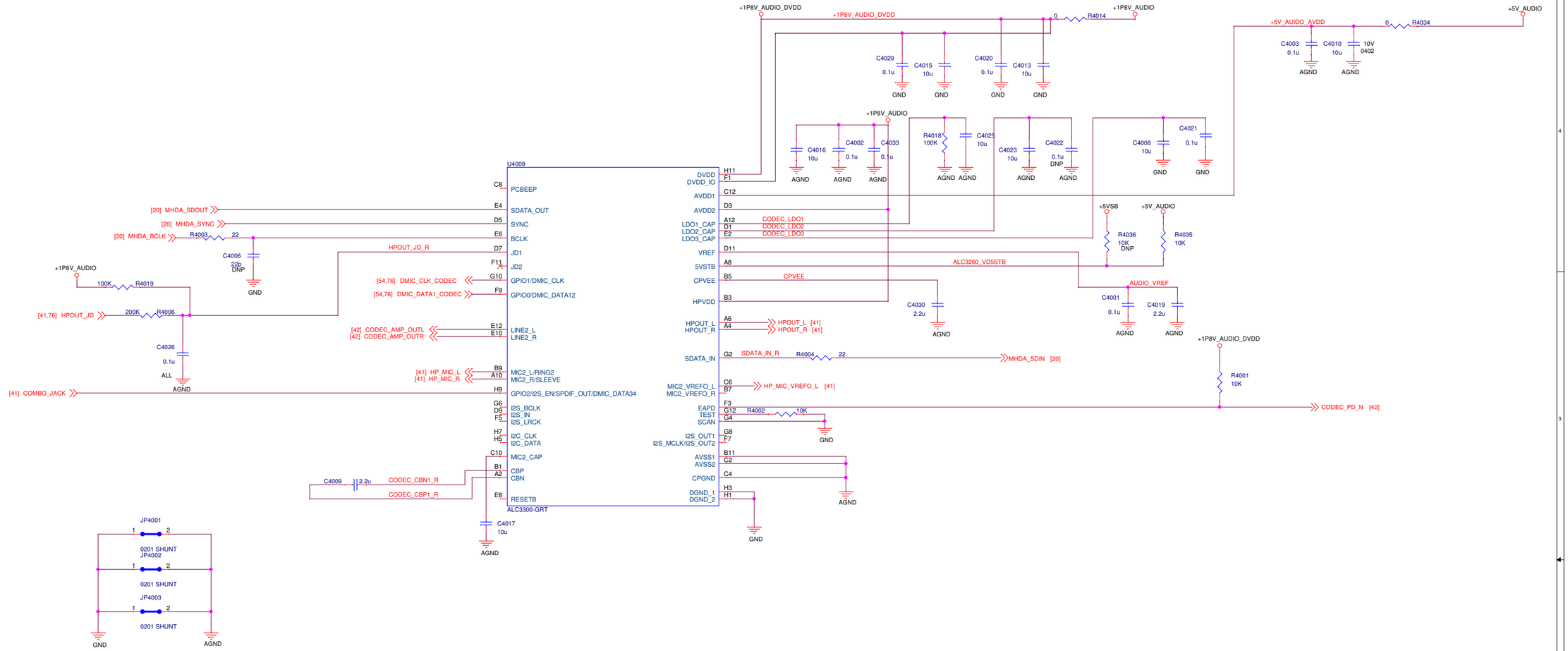
7-bit I2C Address = 0x 4B

temp sensor for the right location testing

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

20170908sjs1321
title is: Temp Sensor/ System Fan

	Title:	Temp Sensor/System Fan	
<OrgName>	Engineer:	<OrgAddr1>	
Size A3	Project Name: EDAN_A_EV1		Rev 1.00
Date: Tuesday, May 21, 2019	Sheet 39 of 82		

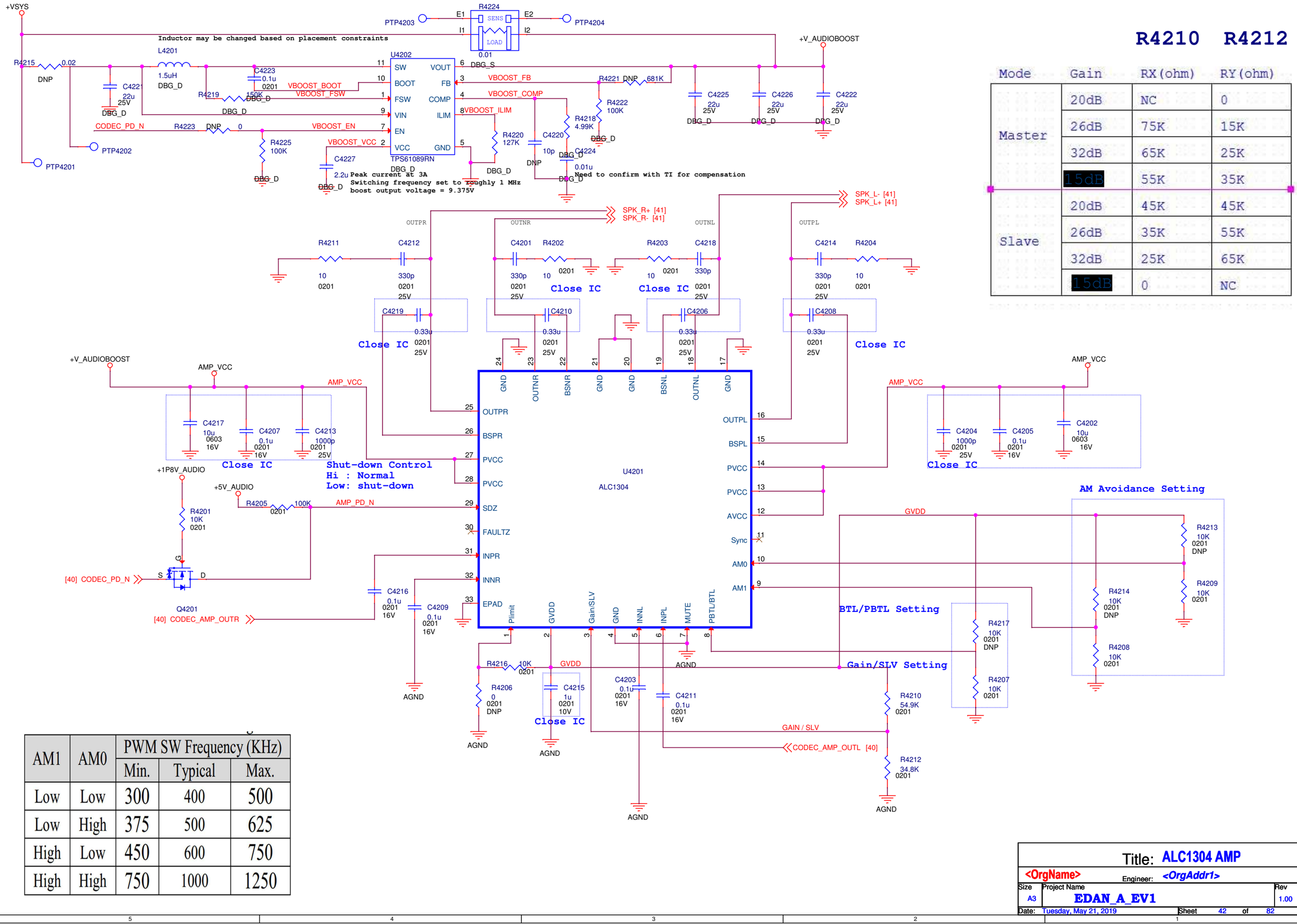

U4009
ALC3300-GRT
DVDD
DVDD_IO
AVDD1
AVDD2
LDO1_CAP
LDO2_CAP
LDO3_CAP
VREF
5VSTB
CPVEE
HPVDD
HPOUT_L
HPOUT_R
SDATA_IN
MIC2_VREFO_L
MIC2_VREFO_R
EAPD
TEST
SCAN
I2S_OUT1
I2S_MCLK/I2S_OUT2
AVSS1
AVSS2
CPGND
DGND_1
DGND_2
PCBEEP
SDATA_OUT
SYNC
BCLK
JD1
JD2
GPIO1/DMIC_CLK
GPIO0/DMIC_DATA12
LINE2_L
LINE2_R
MIC2_L/RING2
MIC2_R/SLEEVE
GPIO2/I2S_EN/SPDIF_OUT/DMIC_DATA34
I2S_BCLK
I2S_IN
I2S_LRCK
I2C_CLK
I2C_DATA
MIC2_CAP
CBP
CBN
RESETB
+1P8V_AUDIO_DVDD
+1P8V_AUDIO
+5V_AUDIO
+5V_AUDIO_AVDD
+5VSB
AUDIO_VREF
CODEC_LDO1
CODEC_LDO2
CODEC_LDO3
ALC3260_VD5STB
CPVEE
SDATA_IN_R
HPOUT_L [41]
HPOUT_R [41]
MHDA_SDIN [20]
HP_MIC_VREFO_L [41]
CODEC_PD_N [42]
[20] MHDA_SDOUT
[20] MHDA_SYNC
[20] MHDA_BCLK
HPOUT_JD_R
[54,76] DMIC_CLK_CODEC
[54,76] DMIC_DATA1_CODEC
[42] CODEC_AMP_OUTL
[42] CODEC_AMP_OUTR
[41] HP_MIC_L
[41] HP_MIC_R
[41,76] HPOUT_JD
[41] COMBO_JACK
CODEC_CBN1_R
CODEC_CBP1_R
R4003 22
R4019 100K
R4006 200K
R4004 22
R4002 10K
R4001 10K
R4014 0
R4034 0
R4018 100K
R4036 10K DNP
R4035 10K
C4006 22p DNP
C4026 0.1u
C4009 2.2u
C4017 10u
C4029 0.1u
C4015 10u
C4020 0.1u
C4013 10u
C4016 10u
C4002 0.1u
C4033 0.1u
C4025 10u
C4023 10u
C4022 0.1u DNP
C4008 10u
C4021 0.1u
C4030 2.2u
C4001 0.1u
C4019 2.2u
C4003 0.1u
C4010 10u 10V 0402
JP4001
JP4002
JP4003
0201 SHUNT
GND
AGND

HP/MIC1 Combo Jack

[40] HP_MIC_VREFO_L
R4104 2.2K
L4101 place close to CON4101
L4101 GBK160808T-121Y 120 OHM,100MHZ
[40] HP_MIC_R
C4104 4.7u
MIC1_CR
R4101 1K
MIC1_CR_F
[40] HP_MIC_L
C4105 4.7u
C4107 4700p
AGND
R4105 22K
AGND
C4103 100p
AGND
R4107 0
GND
AGND
[76] HP_MIC_LR_CON
[76] HPOUT_R_CON
[76] HPOUT_L_CON
This is the Lynx combo jack. Schematic symbol is only used for the footprint (Screw on connector). Therefore, it is DNP.
DNP
J4103
1 MIC
3 RIGHT
4 DET
5 LEFT
2 GND
AGND
[40] COMBO_JACK
R4106 22K
C4106 10u
AGND
[40] HPOUT_L
R4102 10
HPOUT_L_F
L4102 GBK160808T-121Y 120 OHM,100MHZ
[40] HPOUT_R
R4103 10
HPOUT_R_F
L4103 GBK160808T-121Y 120 OHM,100MHZ
R4110 10K
AGND
R4111 10K
AGND
C4101 100p
AGND
C4102 100p
AGND
D4104 V18MLA0402NR CDS2C05GTA
D4102 V18MLA0402NR CDS2C05GTA
D4103 V18MLA0402NR CDS2C05GTA
GND
C4108 100p
GND
[40,76] HPOUT_JD
D4101 V18MLA0402NR CDS2C05GTA
GND

[76] SPK_L+_CON
LYNX Speaker Connector
J4101
[42] SPK_L+
R4114 0
C4121 1000p
GND
C4122 1000p
[42] SPK_L-
R4115 0
SPK_L+_CON
SPK_L-_CON
D4105 V18MLA0402NR
GND
D4106 V18MLA0402NR
GND
X872411-001
MTG1
MTG2
GND
[76] SPK_L-_CON
LYNX Speaker Connector
[76] SPK_R+_CON
J4102
[42] SPK_R+
R4116 0
C4123 1000p
GND
C4124 1000p
[42] SPK_R-
R4117 0
SPK_R+_CON
SPK_R-_CON
D4108 V18MLA0402NR
GND
D4107 V18MLA0402NR
GND
X872411-001
MTG1
MTG2
GND
[76] SPK_R-_CON

Title: Universal Jack / Speaker HDR /DMIC HDR		
<OrgName>	Engineer: <OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 41 of 82	



R4210 R4212

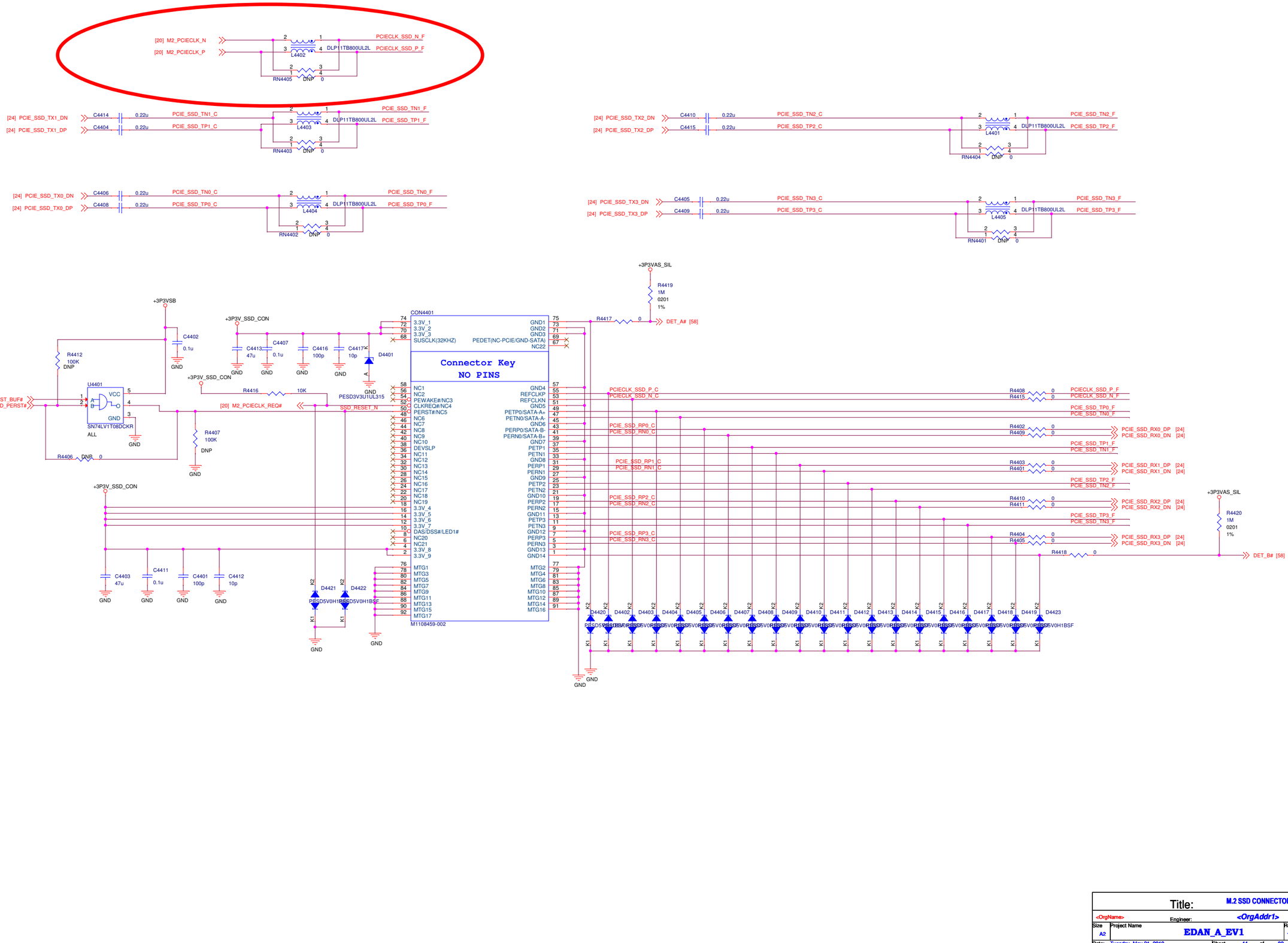
Mode	Gain	RX(ohm)	RY(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	15dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	15dB	0	NC

AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

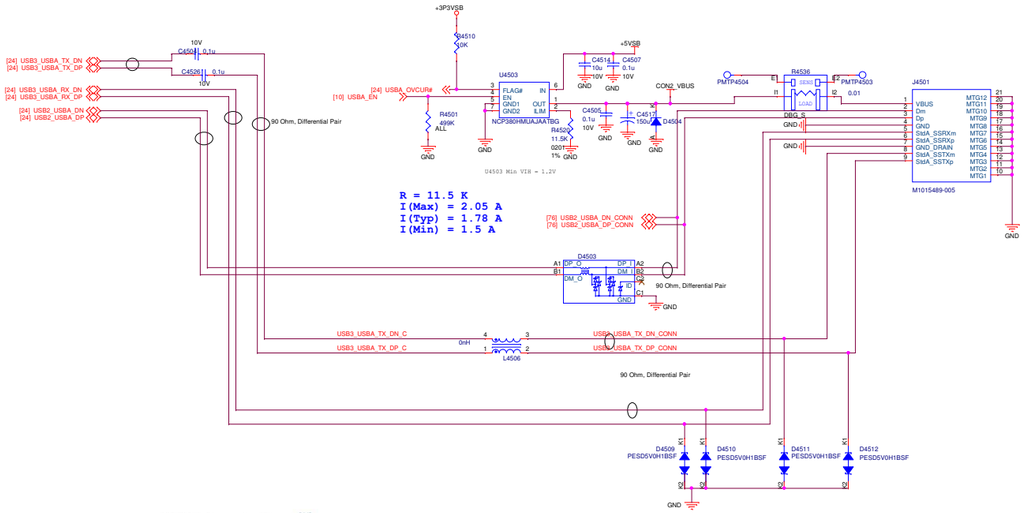
Title: ALC1304 AMP			
<OrgName>	Engineer: <OrgAddr1>		
Size: A3	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019		Sheet 42 of 82	

Title:					
<OrgName>	Engineer:	<OrgAddr1>			
Size: Custom	Project Name: EDAN_A_EV1				Rev: 1.00
Date: Tuesday, May 21, 2019			Sheet 43 of 82		

W = H: 297 x 477 mm

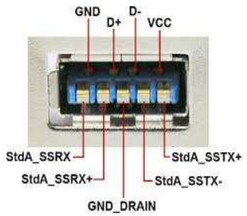


Title:	M.2 SSD CONNECTOR		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 44 of 82		

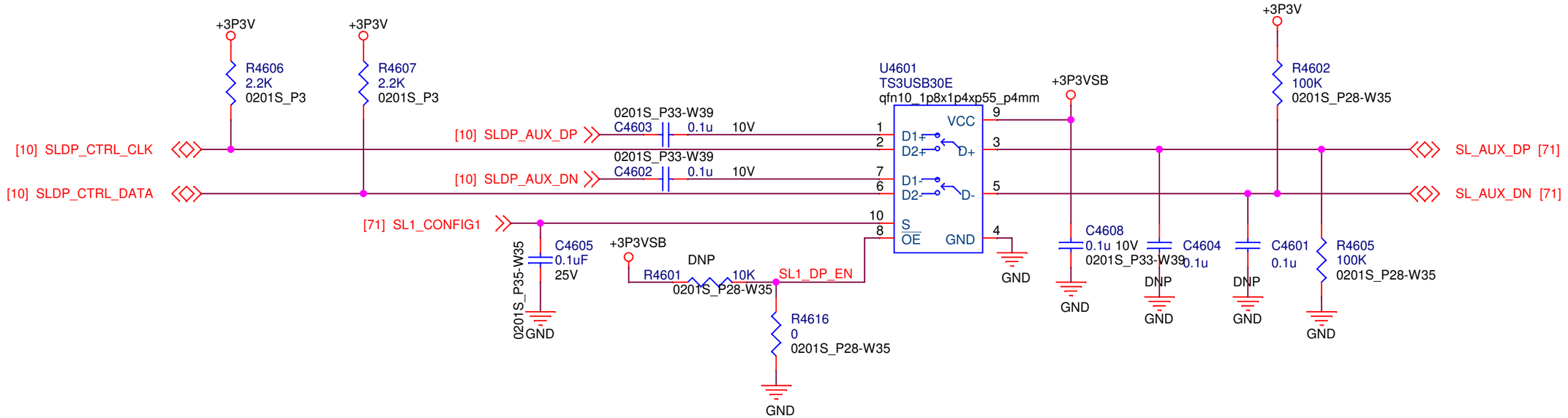


USB 3.0 Connector Pinouts[44]

Pin	Color	Signal name ("A" Connector)	Signal name ("B" Connector)	Description
Shell	N/A	Shield		Metal housing
1	Red	VBUS		Power
2	White	D−		USB 2.0 differential pair
3	Green	D+		
4	Black	GND		Ground for power return
5	Blue	StdA_SSRX−	StdB_SSTX−	SuperSpeed transmitter differential pair
6	Yellow	StdA_SSRX+	StdB_SSTX+	
7	N/A	GND_DRAIN		Ground for signal return
8	Purple	StdA_SSTX−	StdB_SSRX−	SuperSpeed receiver differential pair
9	Orange	StdA_SSTX+	StdB_SSRX+	



Title:	USB3.0 Port		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A1	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 45 of 82		



TS3USB30E

EN	S	Connection
L	**L**	AUX for DP [D1 to D]
L	**H**	DDC for HDMI [D2 to D]
H	X	HI-Z

W x H 337 x 218 mm

Title:	DP Dongle Control	
<OrgName>	Engineer:	<OrgAddr1>
Size: A4	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 46 of 82	

Title: mDP

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00

Date: Tuesday, May 21, 2019 Sheet 47 of 82

W x H 392 x 254 mm

<Core Design>

uSD

Microsoft

Date: Tuesday, May 21, 2019 | Engineer: <OrgName> | Sheet 48 of 82 | Rev

Title: **Camera IR**

<OrgName> Engineer: *<OrgAddr1>*

Size	Project Name	Rev
Custom	**EDAN_A_EV1**	2.89.6
Date: Tuesday, May 21, 2019	Sheet 49 of 82	

W x H 420 x 260 mm

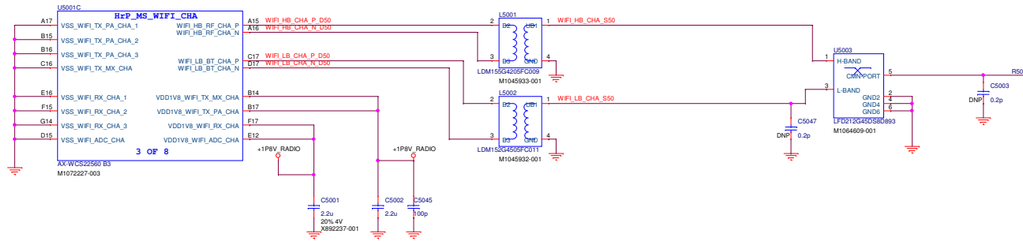
LAYOUT NOTE:
WIFI*D50 and WIFI*S50 routed with impedance control

Non-50-Ohm System -> Follow Intel Layout

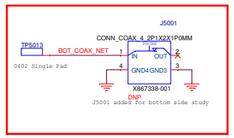
WiFi Harrison Peak

BT ON CHA LB

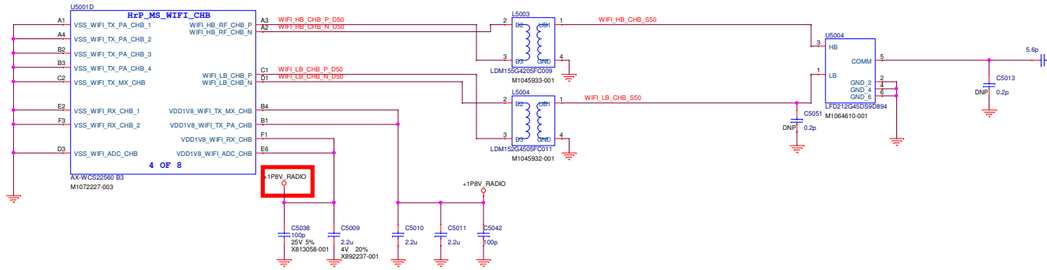
Filters and switches need to be reviewed by RF team and ME

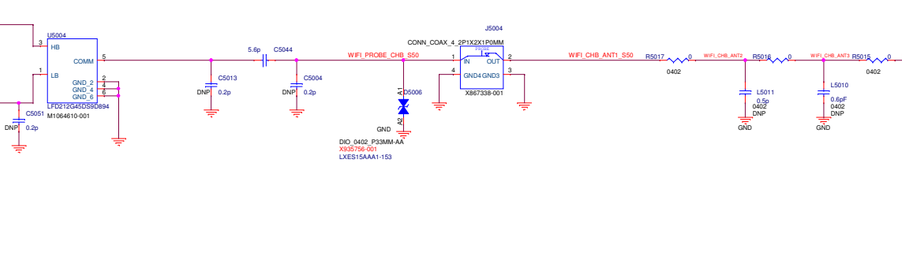


Right antenna connector

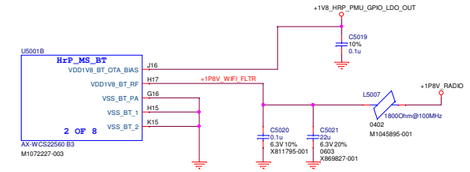


Non-50-Ohm System -> Follow Intel Layout

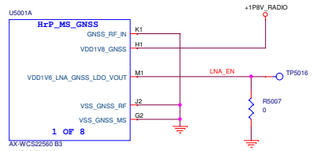


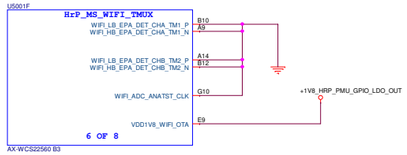


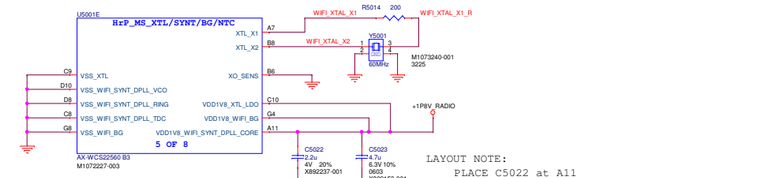
Left antenna spring clip



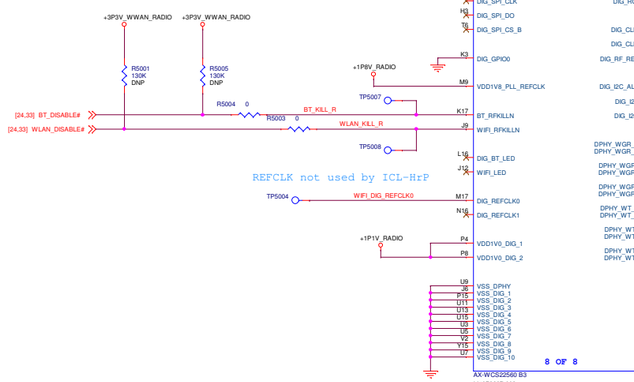
Confirm CNV strapping for ICL-HrP only

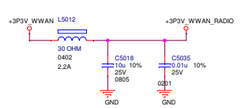


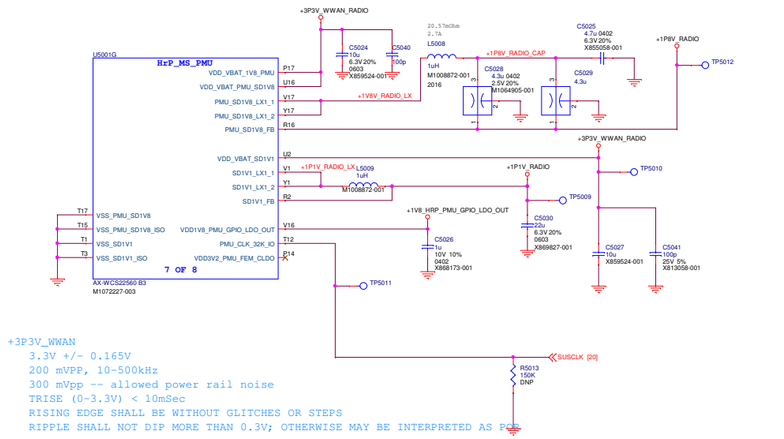




LAYOUT NOTE:
PLACE C5022 at A11
PLACE 4.7UF C5023 as close as possible to A11







LAYOUT NOTE:
CNV*D100 nets routed as 85-Ohm differential pairs

LAYOUT NOTE:
PLACE CNV_WT* TPS NEAR U5001;
Stubbs should be minimized and limited to just a VIA for access
Consider removing CNV_WT* TPs in later builds

+3P3V_WWAN
3.3V +/- 0.165V
200 mVPP, 10-500kHz
300 mVpp -- allowed power rail noise
TRISE (0-3.3V) < 10mSec
RISING EDGE SHALL BE WITHOUT GLITCHES OR STEPS
RIPPLE SHALL NOT DIP MORE THAN 0.3V; OTHERWISE MAY BE INTERPRETED AS PCIE

Title:	Wi-Fi_BT Coex		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A1	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 50 of 80		

W x H 377 x 244 mm

Title: Empty

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00
Date: Tuesday, May 21, 2019	Sheet 51 of 82	

W x H 387 x 250 mm

Title: Camera power

<OrgName>

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	2.89.6

Date: Tuesday, May 21, 2019 Sheet 52 of 82

Place close to pin 23,25

W x H 437 x 328 mm

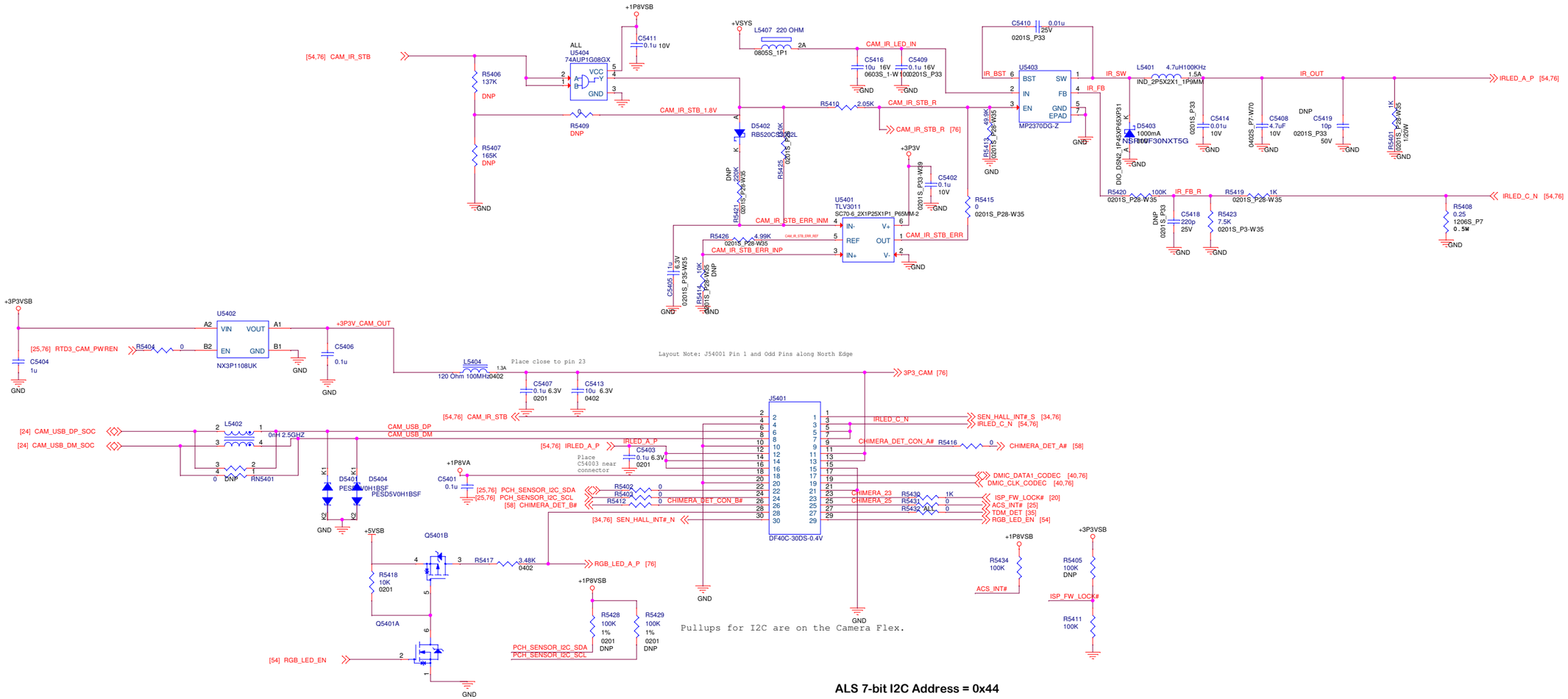
Title: Blank

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	2.89.6

Date: Tuesday, May 21, 2019 Sheet 53 of 82

Sensor Connector to IR and RGB Cameras, Left and Right Microphones, and ALS Sensor



Pullups for I2C are on the Camera Flex.

ALS 7-bit I2C Address = 0x44

Check with Camera/RF/Power team for regulation, filtering, and component info
Power regulation, Privacy LED and sensors moved locally on sensor board. IRLED Buck regulation local to mb

Odd side of the J54001 connector faces the North edge of the PCB

Title: Camera Front			
<OrgName>	Engineer: <OrgAddr1>		
Size: A2	Project Name: EDAN_A_EV1		Rev: 2.89.6
Date: Tuesday, May 21, 2019	Sheet 54 of 82		

W x H 282 x 254 mm

+V_ALWAYS_ON
Iin=0.28A
Trace Width>30mil

+VSYS
D5502 40V
A K
RB520CS3002L
DBG_S
R5521 0.02
0603S_P6-W100
+V_ALWAYS_ON
C5506
0.1uF 25V
0201S_P35-W35
GND

+V_ALWAYS_ON
R5501 100K
C5507
10u
25V
0805S_1P2
GND

Effective Capacitance
2.2uF_0.55mm => @15V=0.255uF
2.2uF_0.55mm => @20V=0.194uF
22 uF_1.45mm => @20V =2.566uF

+3P3VAS
Imax<=0.175A

PWR_SL1_F
D5507 40V
A K
RB520CS3002L
PWR_SL1_F_S
R5517
100K
0201S_P28-W35
C5510
0.01u 25V
0201S_P33
Q5505
TRA-P CNL,SM,DFN1010D-3,120 mOHM,30 V,2.
D2
D1
S
G
PWR_SL1_F_S_DRI
R5516
200K
0201S_P3
Q5507A
[70] SL1_PWR_GOOD
R5518
249K
DNP
DNP
C5509
0.1u 10V
0201S_P33-W39
Q5507B
GND

MODE
FLOAT PFM/PWM
PU PWM

U5501
VIN1
MODE
EN
PG
BIAS
VCC
NC
AGND
PGND-8
PGND-3
SW
BST
FB
FRQ
SS
MP2269GD-Z
DNP
R5532
1K
INT_LDO_5VCC
10V
20%
C5520
1u
3P3VA_GND
3P3VAS_SW
C5512
1u
25V
3P3VAS_BST
3P3VAS_FB
IND,PMC,6.8uH,330mOhm,1.2A,SM,3.2X2.5X1.
L5501 6.8uH
C5513
5.6p
R5514
1M
R5510
324K
C5505
22u 10V
0603S_1-W100
C5508
22u 10V
0603S_1-W100
DBG_S
R5512 0.1
0603S_P65-W95
TP5501
PMTP5503
SP-TP-C0P381
PMTP5504
SP-TP-C0P381
+3P3VAS_FREQ
+3P3VAS_SS
C5521
12n
R5515
165K

fs = 86500/(R+6.5)
500KHz

R5507
0201 SHUNT
3P3VA_GND

+VBUS_P0_CONN
D5504 40V
A K
RB520CS3002L

+3P3VAS_BATLDO
[70] BAT_LDO
D5501
A K
RB520CS3002L
200mA
+3P3VAS
D5503
A K
R5502 1.5K
RB520CS3002L
+VCC_RTC
C5511
0.1u
10V
DNP
0201S_P33-W39
R5508
0
R5522
200K
0201S_P3
DNP
[35] VCCRTC_RST
R5503 499
VCCRTC_RST_R
Q5501
SOTFL-3_1P3XP9XP55_P4
R5504
100K
0201S_P28-W35

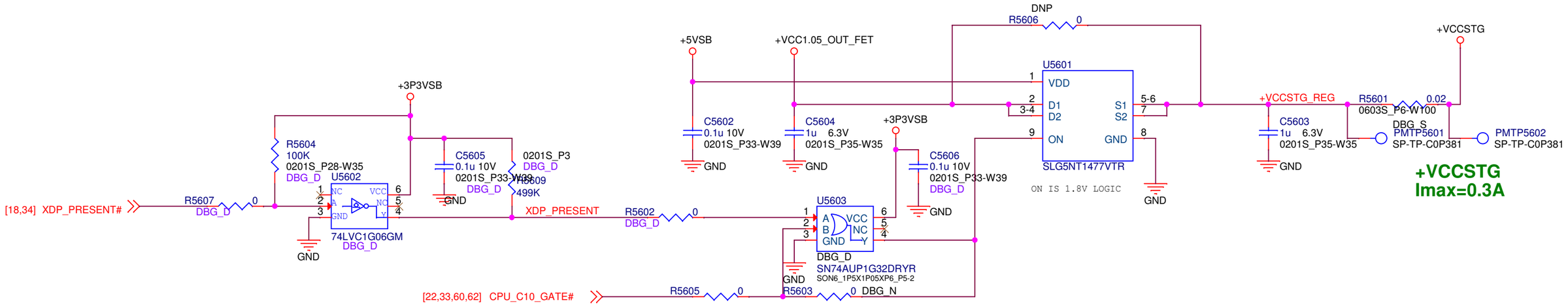
+VCC_RTC
Imax=0.0002A

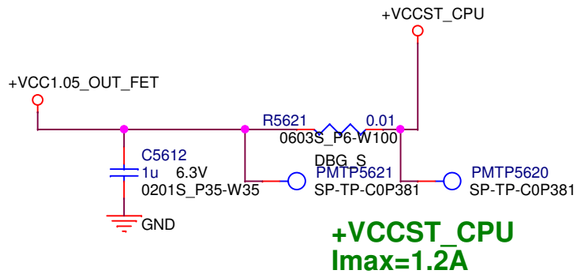
+3P3VAS
R5529
100K
0201S_P28-W35
DNP
[58] 3P3VA_EN
U5505
VIN VOUT
EN
GND EPAD
NCP170AMX180TCG
1P8VA_REG
C5501
0.1u 10V
0201S_P33-W39
C5502
1u 6.3V
0201S_P35-W35
C5518
10u 10V
0603S_1-W100
DBG_S
R5520 0.1
0603S_P65-W95
+1P8VA
Imax=0.08A

+3P3VAS
C5503
1u
U5506
VIN VOUT
EN GND
NX3P1108UK
3P3VA_EN
R5506 0
+3P3VA_REG
C5504
0.1u
R5505 0.1
DBG_S
PTP5502
+3P3VA
PTP5501
+3P3VA
Imax=0.01A

+3P3VAS
R5530
100K
0201S_P28-W35
U5502
VIN VOUT
EN
GND EPAD
NCP170AMX180TCG
1P8VAS_REG
C5523
0.1u 10V
0201S_P33-W39
C5522
1u 6.3V
0201S_P35-W35
C5524
10u 10V
0603S_1-W100
DBG_S
R5533 0.1
0603S_P65-W95
+1P8VAS
Imax=???A

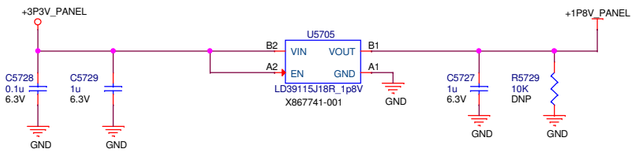
Title: VA AND VCCRTC
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: EDAN_A_EV1
Rev: 1.00
Date: Tuesday, May 21, 2019
Sheet 55 of 82
W x H 447 x 289 mm

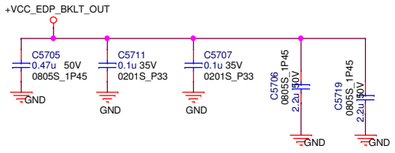


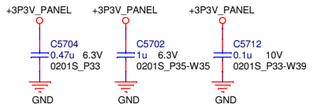


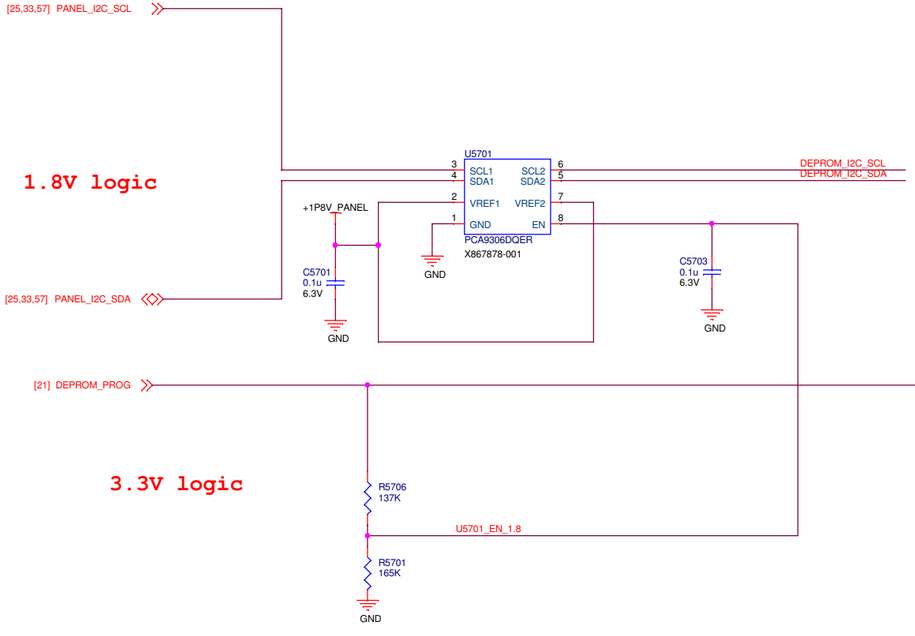
Title: +VCCSTG			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 56 of 82		

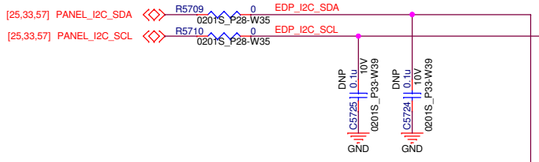
W x H 377 x 244 mm

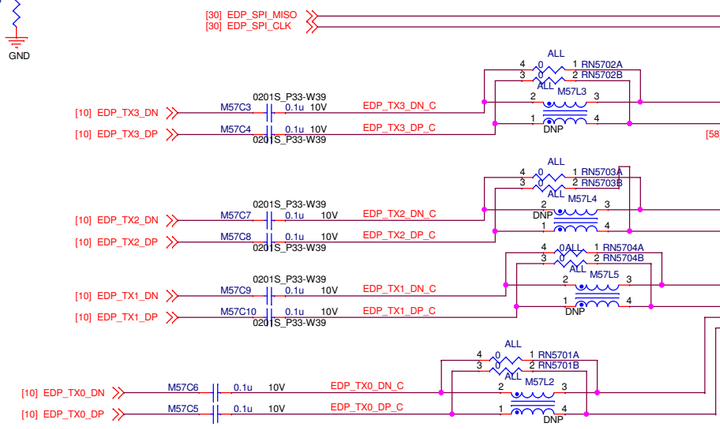


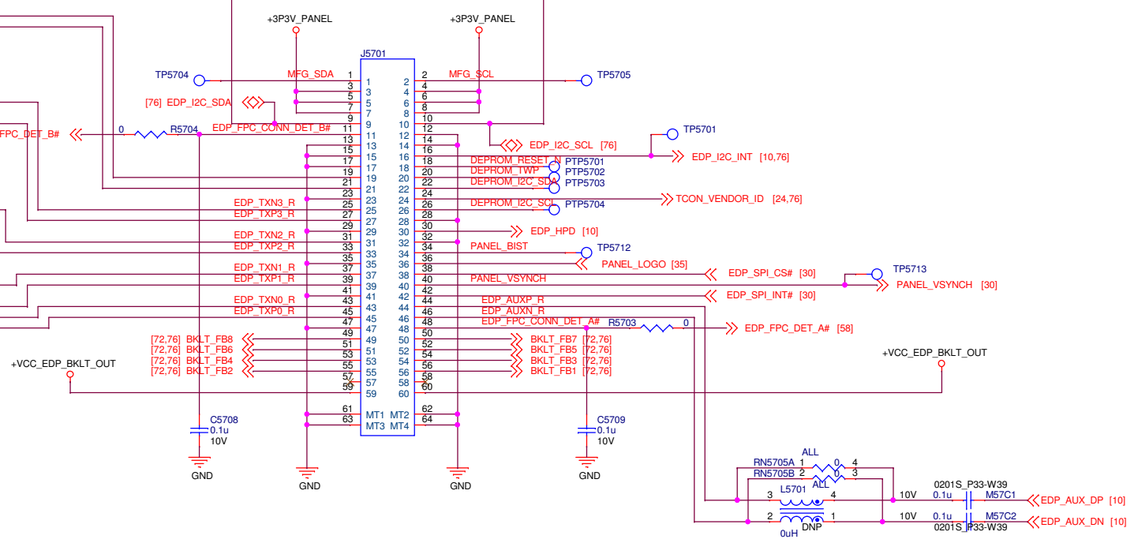


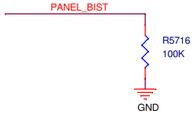


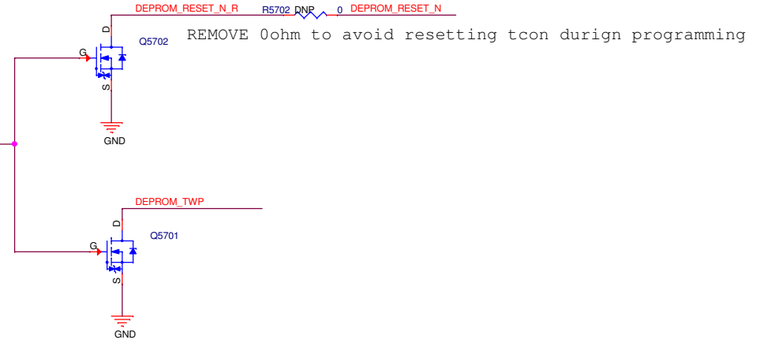








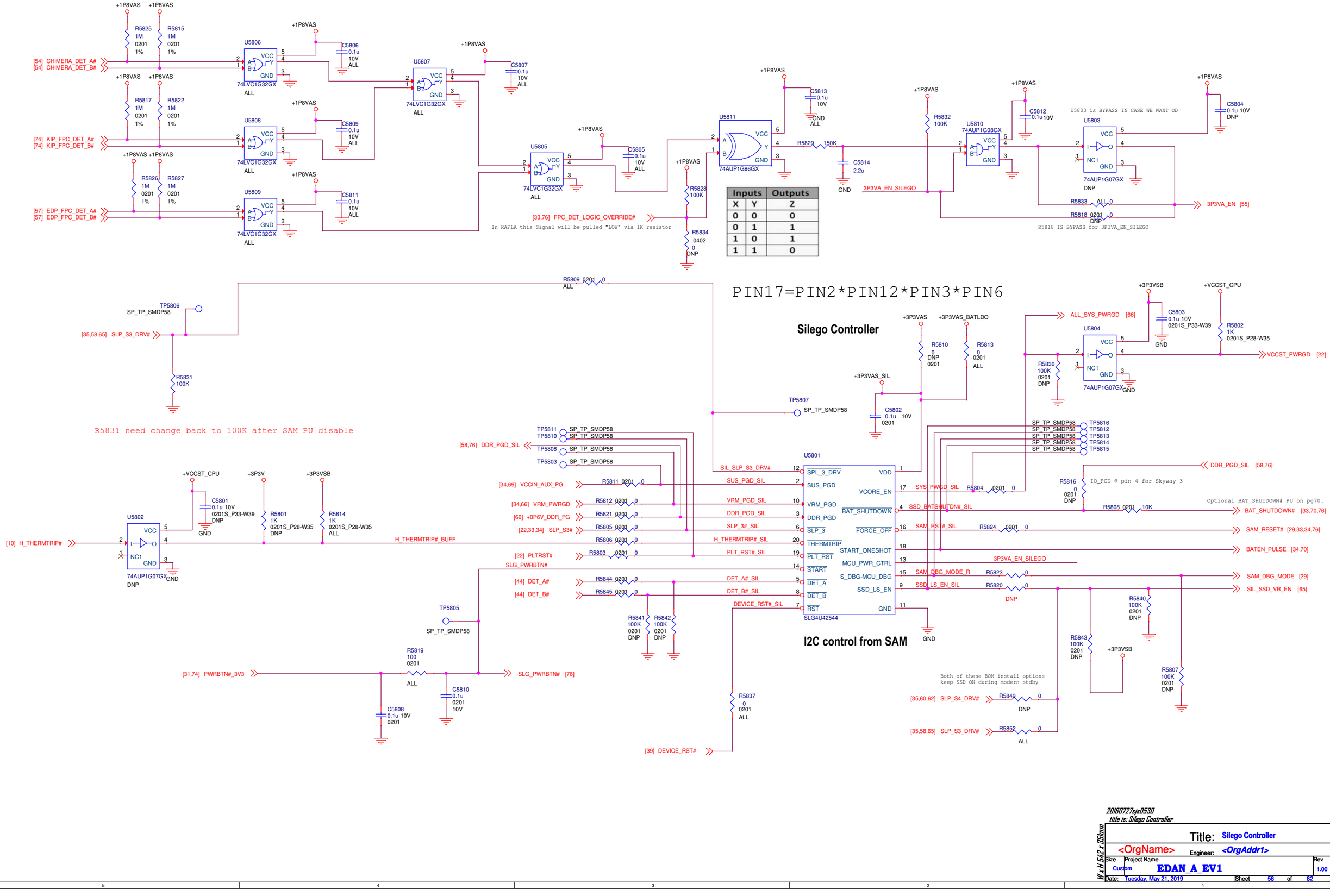




The SCL switch conducts if EN is = 1 V higher than SCL1
The SDA switch conducts if EN is = 1 V higher than SDA1
VIO(Max) = 5V
200K PU not needed when VREF1 = VREF2
If EN > Vref1+0.7V => device will NOT properly isolate the two sides when both sides are high

W x H 602 x 390 mm

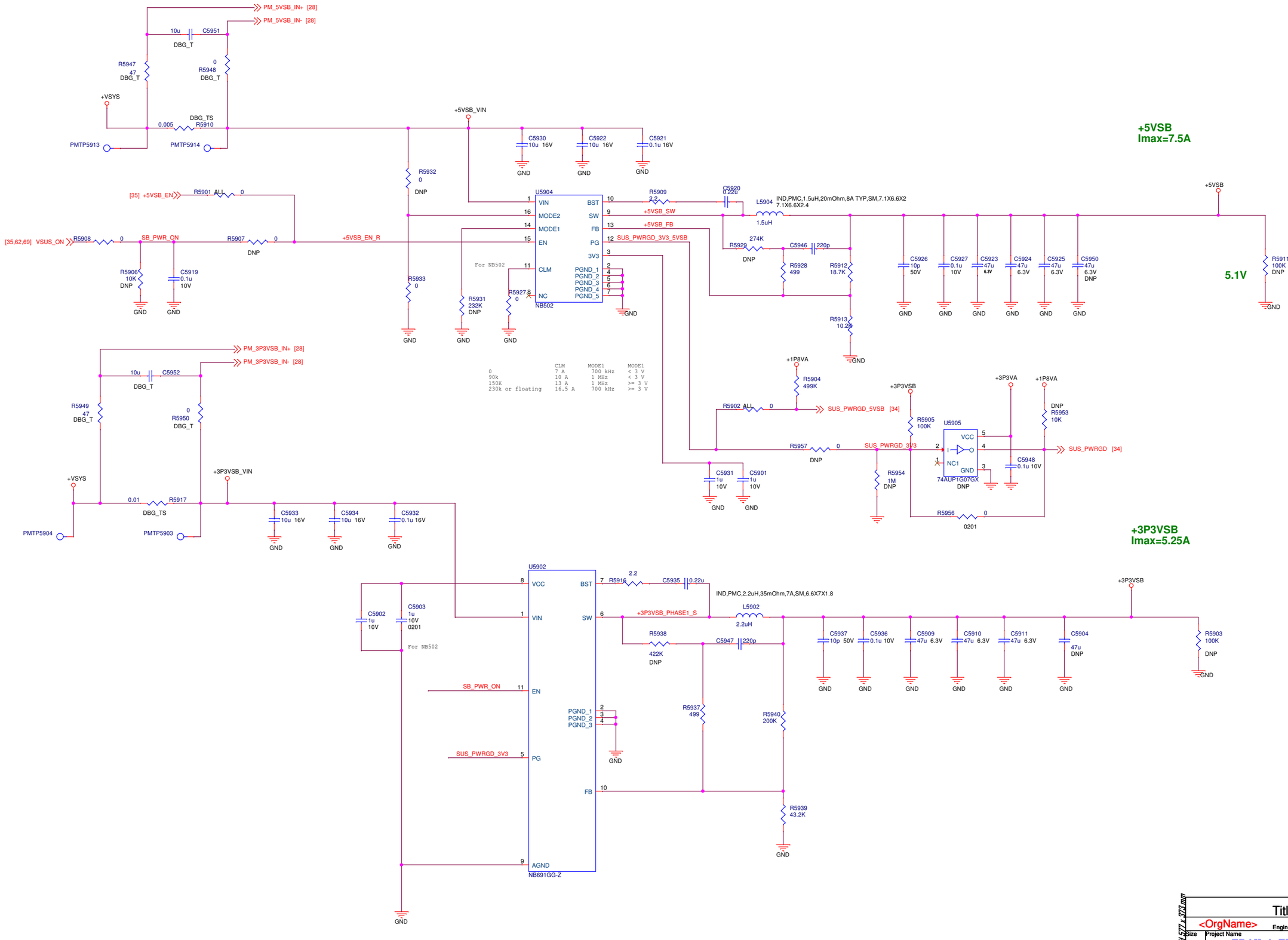
Title: eDP connector			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019		Sheet 57 of 76	

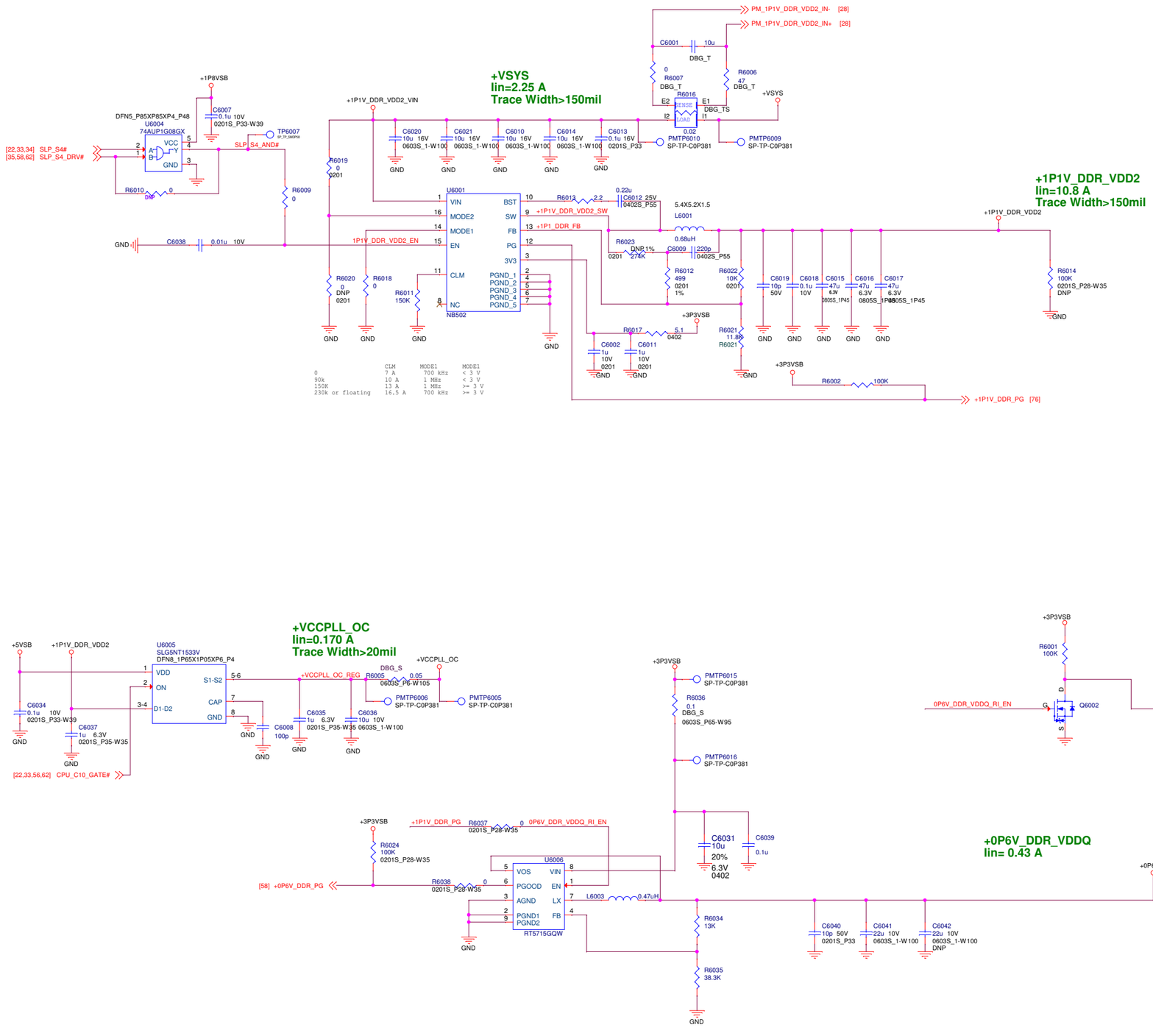


20160727gis0530
title is: Silego Controller

	Title: Silego Controller			
<OrgName>	Engineer: <OrgAddr1>			
Size: Custom	Project Name: EDAN_A_EV1			Rev: 1.00
Date: Tuesday, May 21, 2019		Sheet 58 of 82		

W x H: 542 x 351mm

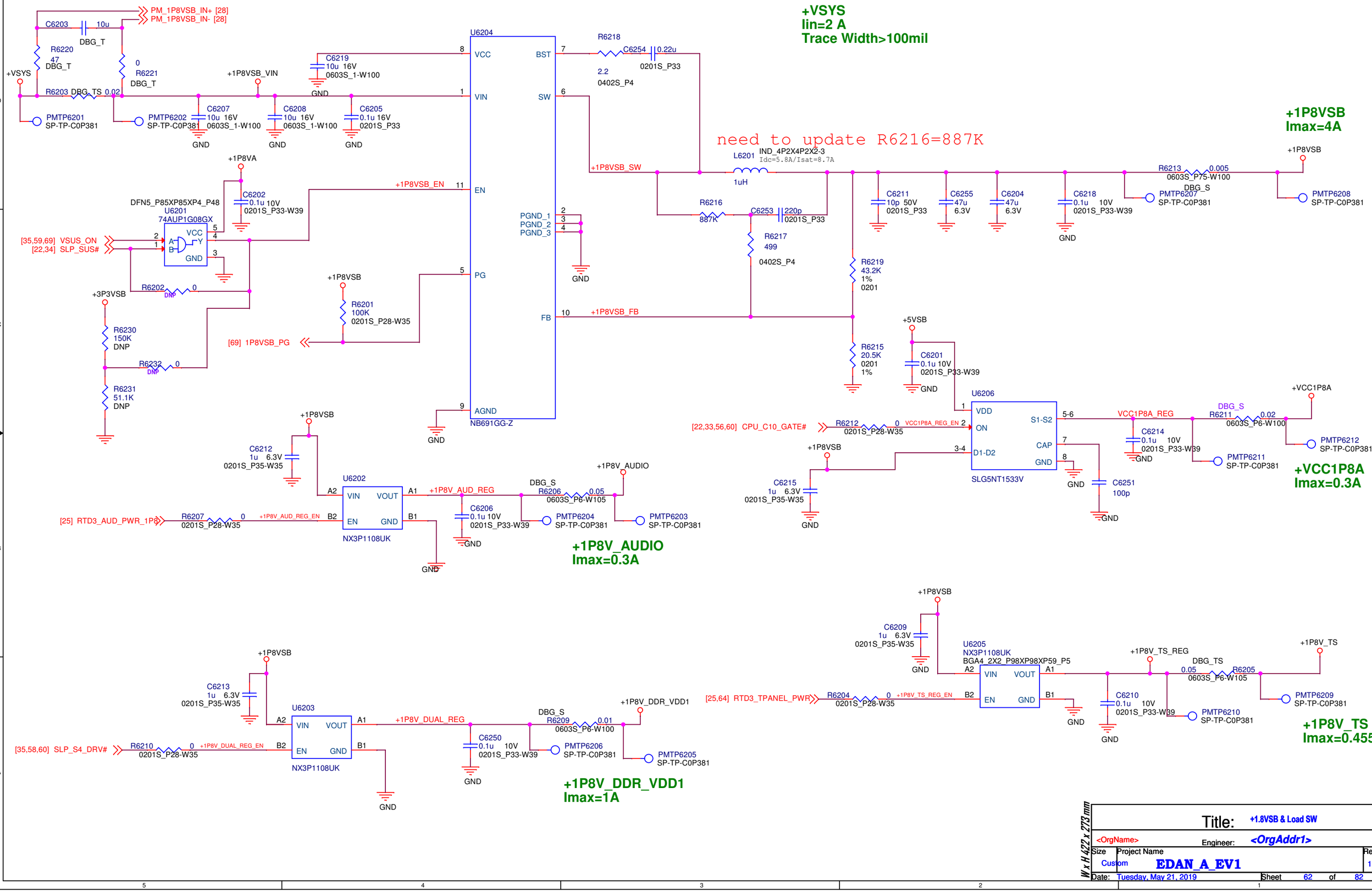

PM_5VSB_IN+ [28]
PM_5VSB_IN- [28]
10u C5951 DBG_T
R5947 47 DBG_T
R5948 0 DBG_T
+VSYS
0.005 R5910 DBG_TS
PMTP5913
PMTP5914
+5VSB_VIN
C5930 10u 16V
C5922 10u 16V
C5921 0.1u 16V
GND
R5932 0 DNP
[35] +5VSB_EN
R5901 ALL 0
[35,62,69] VSUS_ON
R5908 0
SB_PWR_ON
R5907 0 DNP
+5VSB_EN_R
R5906 10K DNP
C5919 0.1u 10V
R5933 0
R5931 232K DNP
R5927 0
For NB502
U5904
VIN
MODE2
MODE1
EN
CLM
NC
BST
SW
FB
PG
3V3
PGND_1
PGND_2
PGND_3
PGND_4
PGND_5
NB502
R5909 2.2
C5920 0.22u
L5904 IND,PMC,1.5uH,20mOhm,8A TYP,SM,7.1X6.6X2 7.1X6.6X2.4
1.5uH
+5VSB_SW
+5VSB_FB
SUS_PWRGD_3V3_5VSB
R5929 274K DNP
C5946 220p
R5928 499
R5912 18.7K
R5913 10.2K
+5VSB
Imax=7.5A
C5926 10p 50V
C5927 0.1u 10V
C5923 47u 6.3V
C5924 47u 6.3V
C5925 47u 6.3V
C5950 47u 6.3V DNP
R5911 100K DNP
5.1V
CLM MODE1 MODE1
0 7 A 700 kHz < 3 V
90k 10 A 1 MHz < 3 V
150K 13 A 1 MHz >= 3 V
230k or floating 16.5 A 700 kHz >= 3 V
PM_3P3VSB_IN+ [28]
PM_3P3VSB_IN- [28]
10u C5952 DBG_T
R5949 47 DBG_T
R5950 0 DBG_T
+VSYS
+3P3VSB_VIN
0.01 R5917 DBG_TS
PMTP5904
PMTP5903
C5933 10u 16V
C5934 10u 16V
C5932 0.1u 16V
+1P8VA
R5904 499K
R5902 ALL 0
SUS_PWRGD_5VSB [34]
+3P3VSB
R5905 100K
R5957 0 DNP
SUS_PWRGD_3V3
U5905
VCC
NC1
GND
74AUP1G07GX DNP
+3P3VA
DNP R5953 10K
SUS_PWRGD [34]
C5948 0.1u 10V
C5931 1u 10V
C5901 1u 10V
R5954 1M DNP
R5956 0 0201
+3P3VSB
Imax=5.25A
U5902
VCC
VIN
EN
PG
AGND
BST
SW
FB
PGND_1
PGND_2
PGND_3
NB691GG-Z
R5916 2.2
C5935 0.22u
IND,PMC,2.2uH,35mOhm,7A,SM,6.6X7X1.8
L5902 2.2uH
+3P3VSB_PHASE1_S
C5902 1u 10V
C5903 1u 10V 0201
For NB502
SB_PWR_ON
SUS_PWRGD_3V3
R5938 422K DNP
C5947 220p
R5937 499
R5940 200K
R5939 43.2K
C5937 10p 50V
C5936 0.1u 10V
C5909 47u 6.3V
C5910 47u 6.3V
C5911 47u 6.3V
C5904 47u DNP
R5903 100K DNP
Title: +5VSB & +3P3VSB
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: EDAN_A_EV1
Rev: 1.00
Date: Tuesday, May 21, 2019
Sheet 59 of 82



Title:	+1P2V_DUAL&+VTT
<OrgName>	Engineer: <OrgAddr1>
Size: A2	Project Name: EDAN_A_EV1
Rev:	1.00
Date:	Tuesday, May 21, 2019
Sheet	60 of 82

Title:	VNN BYPASS Rails			
<OrgName>	Engineer:	<OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1			Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 61 of 82			

W x H 420 x 260 mm


+VSYS
Iin=2 A
Trace Width>100mil
need to update R6216=887K
+1P8VSB
Imax=4A
+1P8V_AUDIO
Imax=0.3A
+VCC1P8A
Imax=0.3A
+1P8V_DDR_VDD1
Imax=1A
+1P8V_TS
Imax=0.455A
U6204
NB691GG-Z
U6201
74AUP1G08GX
U6202
NX3P1108UK
U6203
NX3P1108UK
U6205
NX3P1108UK
U6206
SLG5NT1533V
L6201
IND_4P2X4P2X2-3
Idc=5.8A/Isat=8.7A
1uH
Title: +1.8VSB & Load SW
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: EDAN_A_EV1
Rev: 1.00
Date: Tuesday, May 21, 2019
Sheet 62 of 82
W x H 422 x 273 mm

R6328 need change back to 100K after SAM PU disable

Place L6302 close to L6301 as place holder for larger inductor.

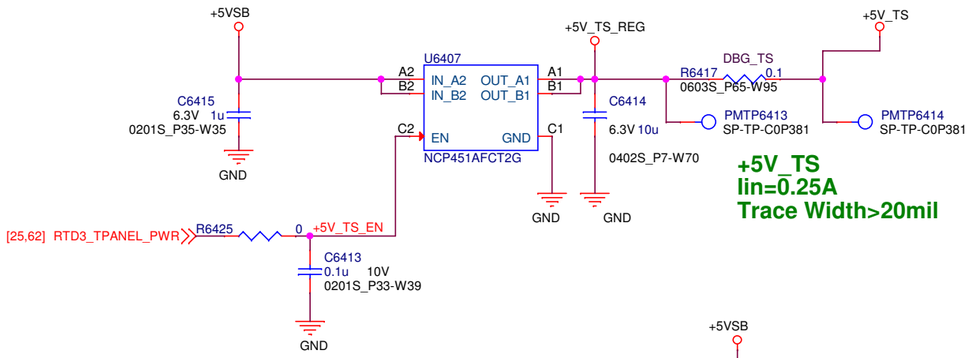
+VSYS: 6V(TBD) to 8.75V

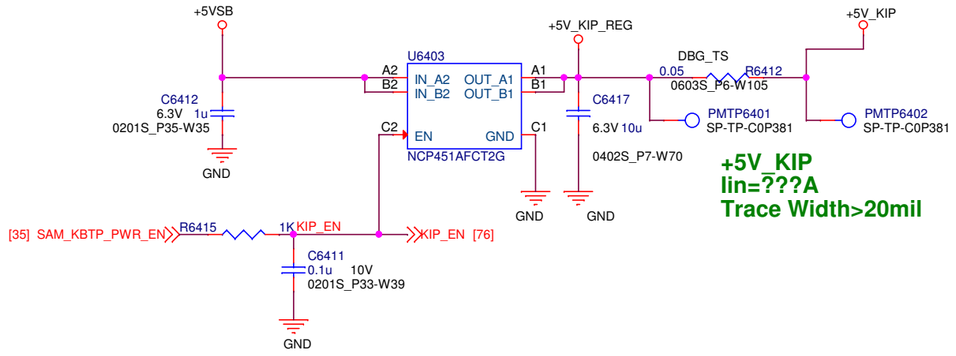
PWR_SL1_F MAX Voltage: 17.2V
PSU_VOLT MAX Voltage: 0.697V

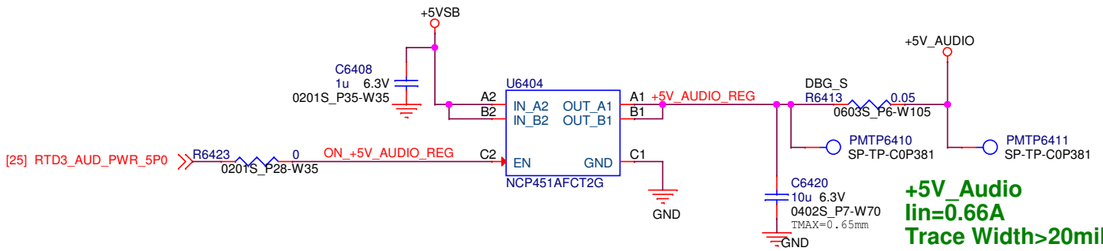
ILIM_HIZ current limit equation - (VILIM_HIZ - 1 V) / 40 = ACP - ACN

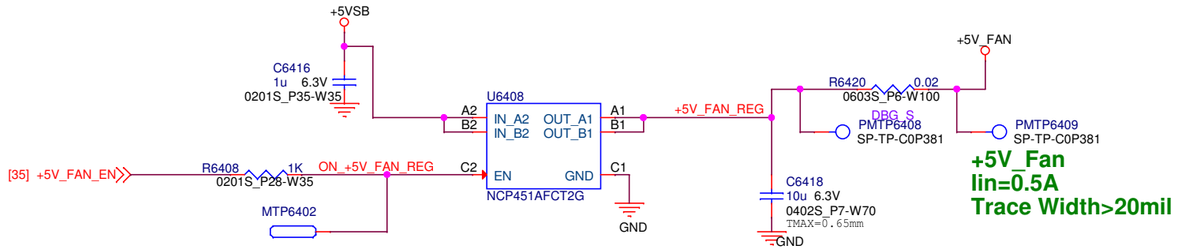
7-bit I2C Address = 0x6B

Title:	CHARGER
<OrgName>	Engineer: <OrgAddr1>
Size: A2	Project Name: EDAN_A_EV1
Rev: 1.00	
Date: Tuesday, May 21, 2019	Sheet 63 of 82

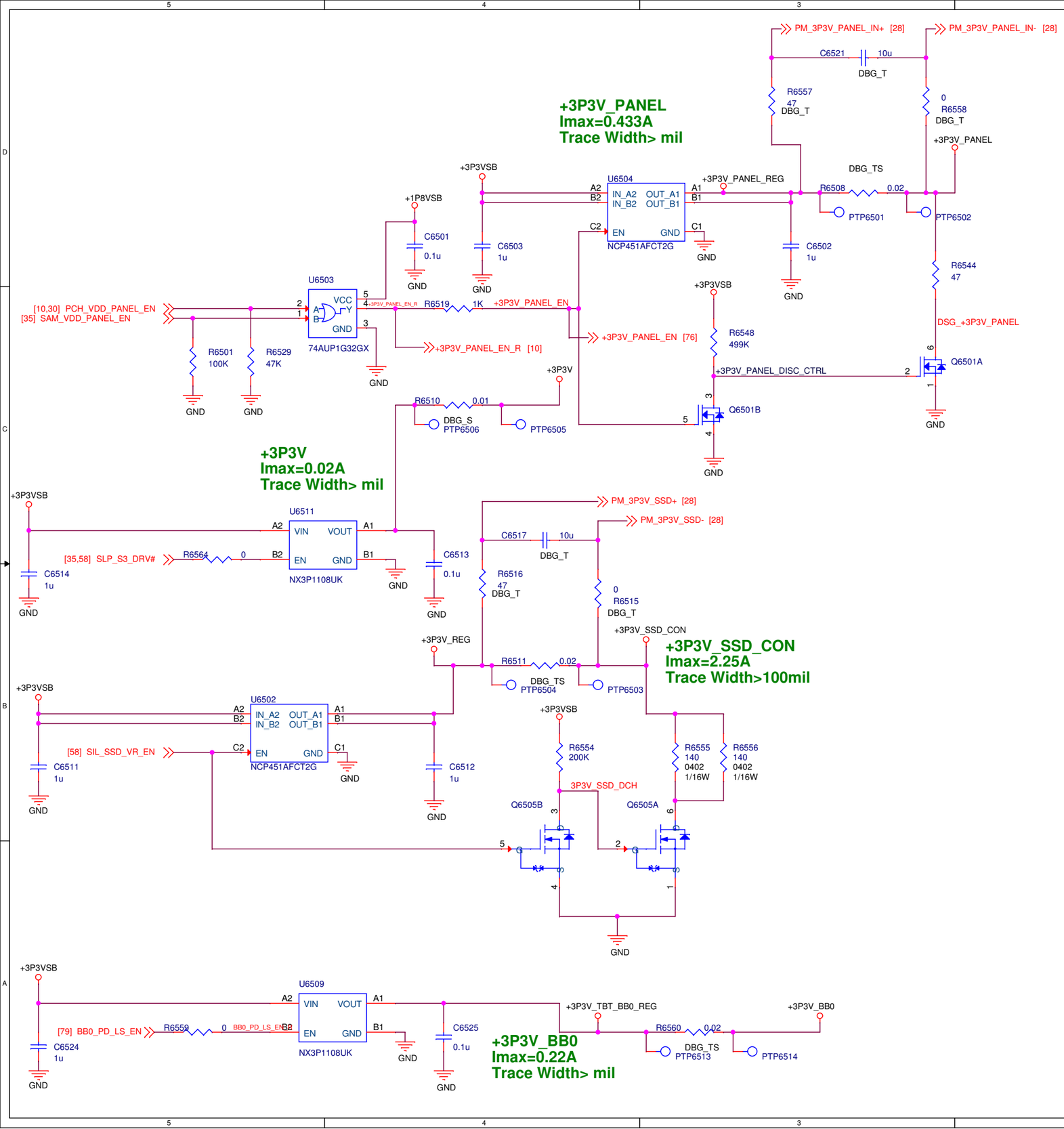




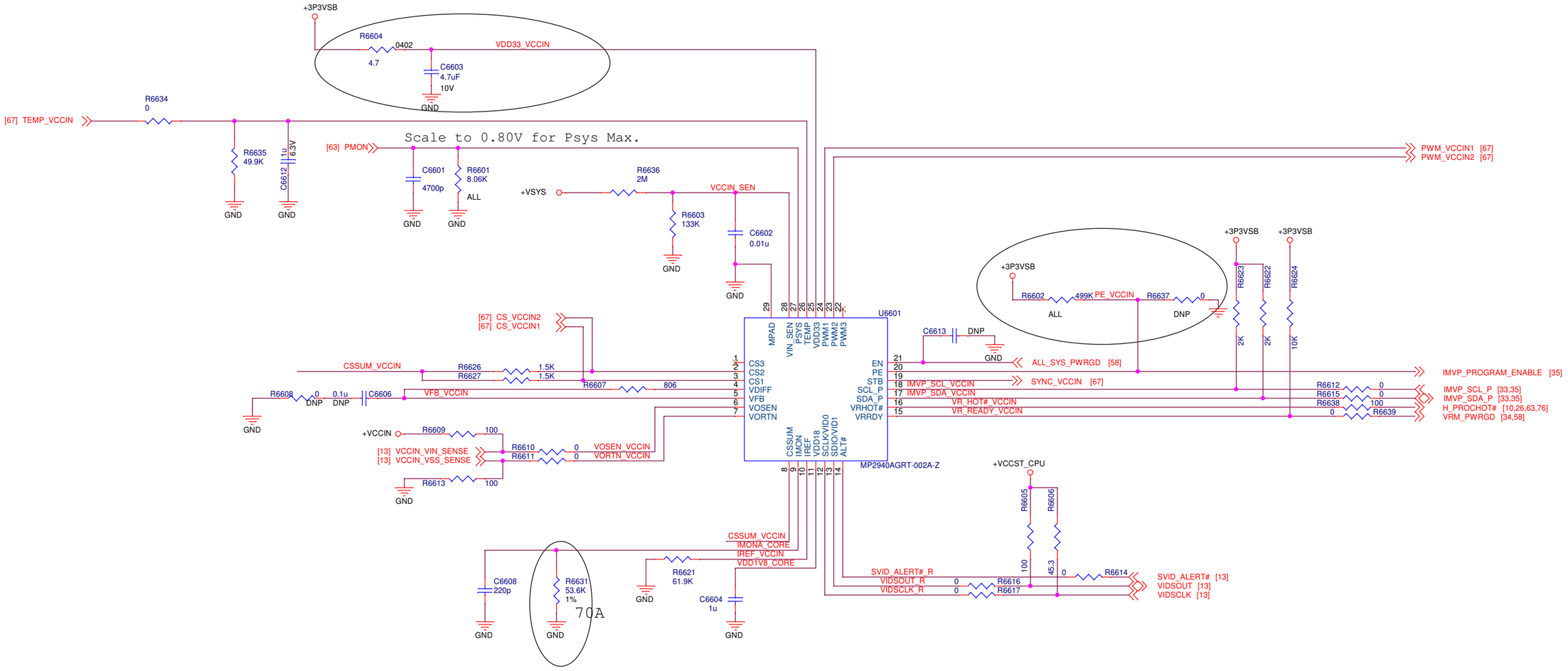




Title: +5V Load SW			
<OrgName> Engineer: <OrgAddr1>			
Size: A3	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 64 of 82		



Title:	+3P3V Load SW		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A3	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 65 of 82		



Full P/N	Customer	CPU SKU/Rail	Project Name
MP2940AGRT-0020-Z	Microsoft	ICL-U42 VccIN	ICL-U42 ref design
MP2940AGRT-0021-Z	Microsoft	ICL-U42 VccIN_AUX	ICL-U42 ref design
MP2940AGRT-0022-Z	Microsoft	ICL-Y VccIN	ICL-Y ref design
MP2940AGRT-0023-Z	Microsoft	ICL-Y VccIN_AUX	ICL-Y ref design

W x H 17 x 825 mm

Title: CONTROLLER: CORE, SA

<OrgName> Engineer: <OrgAddr1>

Size: Custom | Project Name: EDAN_A_EV1 | Rev: 1.00

Date: Tuesday, May 21, 2019 | Sheet 66 of 82

Need to find 1.5W Sense resistor

ICCMAX: 70A
ITDC: 39A

U6701
MP86902B
DRIVE CONTROL
PWM 15
SYNC 16
VTEMPFLT 17
VCC 20
CS 18
AGND 19
BST 21
VIN1 1
VIN14 14
SW2 2
SW3 3
SW4 4
PGND13 13
PGND12 12
PGND511 5-11
HSFET
LSFET
[66] PWM_VCCIN1
[66] SYNC_VCCIN
[66] TEMP_VCCIN
[66] CS_VCCIN1
+3P3VSB
C6702 6.3V 1u
C6701 1u 0201
VCCIN1_SW
L6704 0.15uH 30A IND_6P8X6P8X2P4-3
C6721 470p DNP
R6721 0 DNP
+VCCIN_IN
Place at DrMOS
C6714 1u 0402 25V
C6730 10u 16V 0603
C6731 10u 16V 0603
C6704 47u
C6705 47u
[28] PM_VCCIN_IN+
[28] PM_VCCIN_IN-
C6703 10u DBG_T
R6702 0 DBG_T
R6701 DBG_T
R6703 47 DBG_T
+VSYS
PMTP6702
PMTP6704
E1
E2
I1
I2
+VCCIN
0.005 DBG_TS
R6724 1K 0201S_P28-W35 DNP
TP6702
TP6701
C6712 180uF

U6702
MP86902B
DRIVE CONTROL
PWM 15
SYNC 16
VTEMPFLT 17
VCC 20
CS 18
AGND 19
BST 21
VIN1 1
VIN14 14
SW2 2
SW3 3
SW4 4
PGND13 13
PGND12 12
PGND511 5-11
HSFET
LSFET
[66] PWM_VCCIN2
SYNC_VCCIN
TEMP_VCCIN
[66] CS_VCCIN2
+3P3VSB
C6711 6.3V 1u
C6707 1u 10V 0201S_P4-W40
VCCIN2_SW
L6703 0.15uH 30A
C6723 470p 50V 0402S_P55 DNP
R6723 0 0603S_P-W95 DNP
Place at DrMOS
C6713 1u 25V 0402
C6732 10u 16V 0603
C6733 10u 16V 0603
C6743 47u
C6744 47u
C6709 47u DNP
C6706 47u DNP

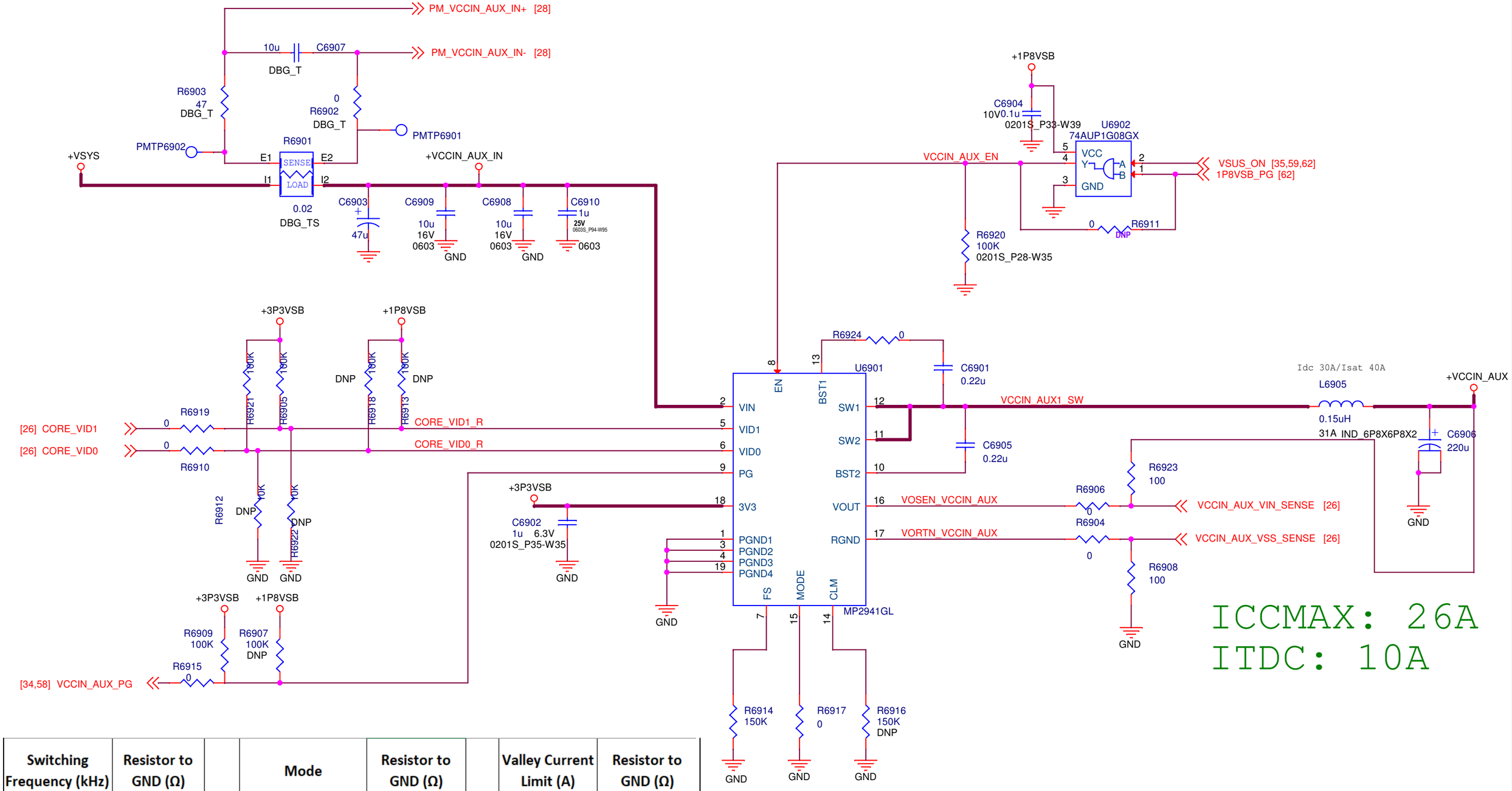
GND

<Core Design>

W x H 357 x 241 mm	Title: IA and SA	
Size: CustomEDAN_A_EV1	Document Number	Rev: <RevCod
Date: Tuesday, May 21, 2019	Sheet 67 of 82	

<Core Design>

Title <Title>		
Size Custom	Document Number EDAN_A_EV1	Rev <RevCode>
Date: Tuesday, May 21, 2019	Sheet 68 of 82	



Switching Frequency (kHz)	Resistor to GND (Ω)		Mode	Resistor to GND (Ω)		Valley Current Limit (A)	Resistor to GND (Ω)
500	0		Non-interleaving, slew down	0		14	0
700	90k		Non-interleaving, decay	Float		20	90k
1000	150k		Interleaving, slew down	90k		26	150k
1200	Float		Interleaving, decay	150k		32	Float

W x H 357 x 241 mm

Title: GT Controller			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 69 of 82		

TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

U7000 DG2723DN-T1-E4

[37] SAM_SL1_TX
[37] SAM_SL1_RX
[35] SL1_RX_SEL#
[35] SL1_ADC
[34,35] ADC_RD_EN
[34,76] SL1_PSU_DET
[55] SL1_PWR_GOOD
[34,58] BATEN_PULSE
[33,58,76] BAT_SHUTDOWN#
[33,35] POWER_SMB_SDA
[33,35] POWER_SMB_SCL
[34] BAT_DET#
[55] BAT_LDO
[76] BAT_SMDATA
[76] BAT_SMCLK
[76] BATA_DET#_CON

SL1_HPD2 [71,76]
SL1_HPD1A [71,76]
SL1_HPD1B [71,76]
BATEN_PULSE_CONN [76]
BAT_LDO_PACK [76]

PSU Voltage Comparator
(9.4V-17.2V)

INA+	<400mV	OUTA=Low
INB+	>400mV	OUTB=Low

TPS3700DSER

SL1 port discharger limits PSU anti-arc pulse voltage

Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

M1106392-001 J7001

TP7007 NO-MSPN-00270 SHUNT-NO-MSPN-00270

20160823sjs0632 : SL1 Power, Battery Connector — Report errors to Steven

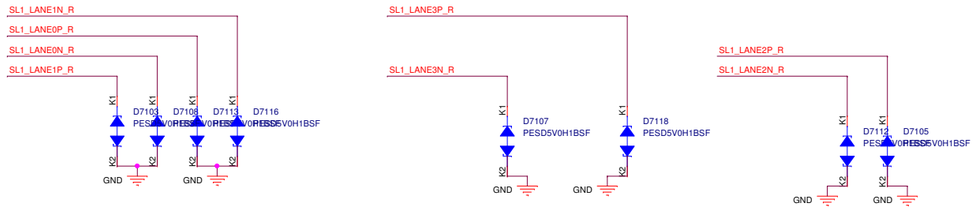
Title: SL1 Power, Battery Conn

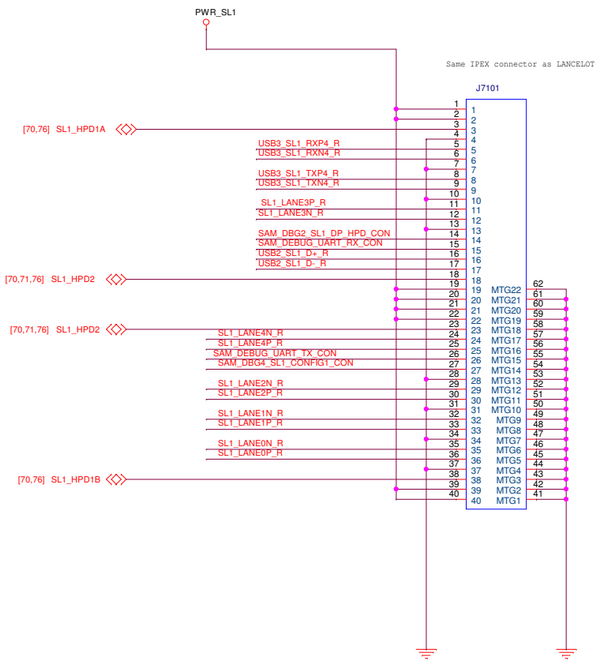
<OrgName> Engineer: <OrgAddr1>

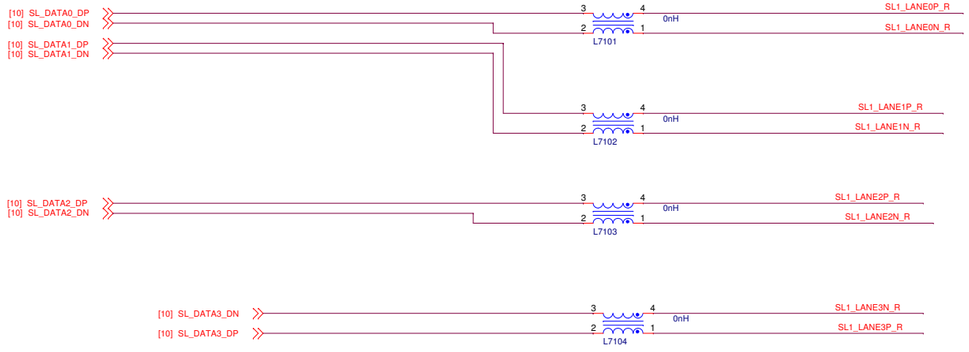
Size: Custom — Project Name: EDAN_A_EV1 — Rev: 1.00

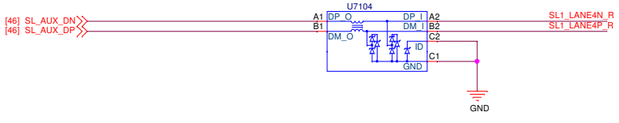
Date: Tuesday, May 21, 2019 — Sheet 70 of 82

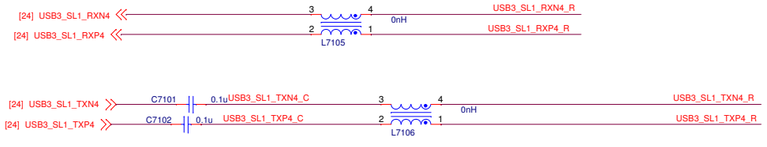
W=H 502 x 325 mm

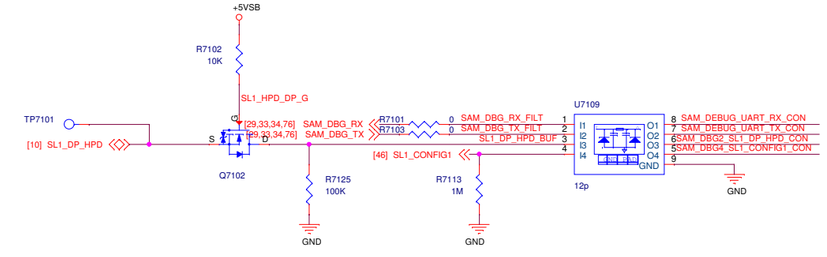


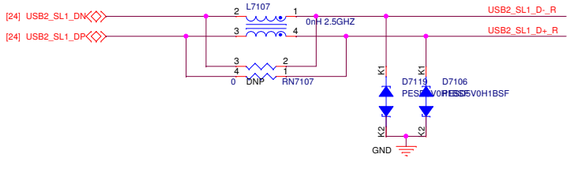


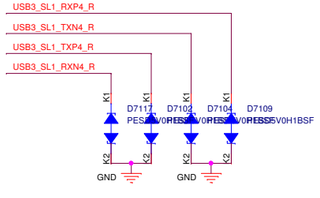




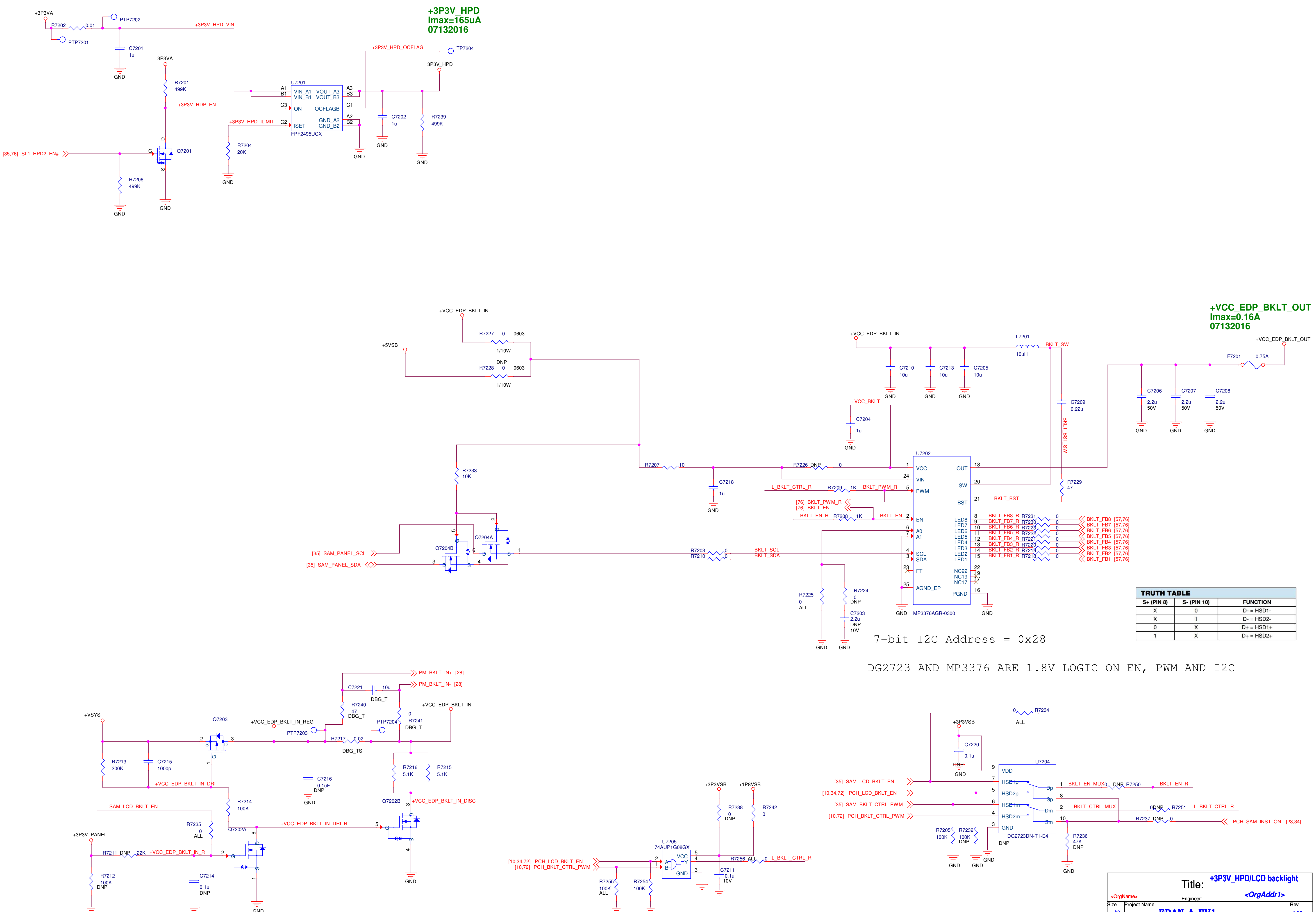








Title:	SL1 SINGNALS		
<OrgName>	Engineer:	<OrgAddr1>	
Size: A2	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 71 of 82		



TRUTH TABLE

S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+

7-bit I2C Address = 0x28

DG2723 AND MP3376 ARE 1.8V LOGIC ON EN, PWM AND I2C

Title: +3P3V_HPD/LCD backlight

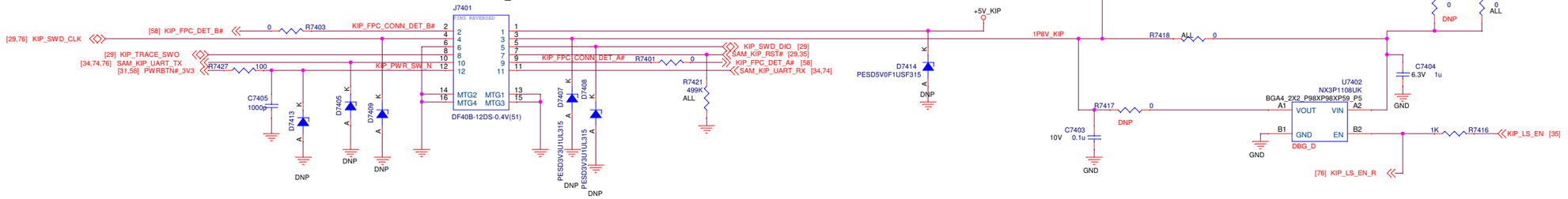
<OrgName> Engineer: <OrgAddr1>

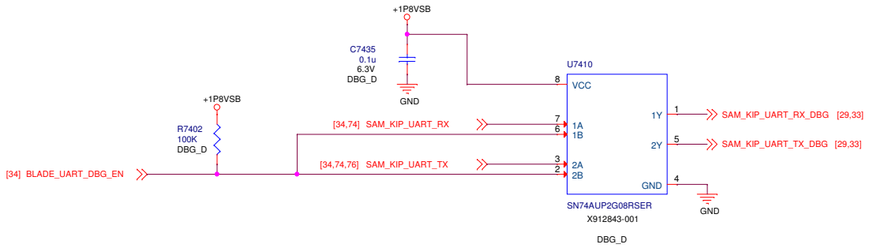
Size	Project Name	Rev
A2	EDAN_A_EV1	1.00

Date: Tuesday, May 21, 2019 Sheet 72 of 82

Title:	PCIe GPU	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 73 of 82	

KBTP CONNECTOR
Pin1 Top Left





KIP UART Debug gated Sniffer (Dual AND gate,)
Place U7410 close to J7401 UART lines to minimize stubs

Title: **Blade Interface**		
<OrgName>	Engineer: *<OrgAddr1>*	
Size: A2	Project Name: **EDAN_A_EV1**	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 74 of 82	

W x H 357 x 231 mm

Title:	Power Protect		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 75 of 82		

MTP7674 MTP7631 MTP7669 MTP7607 MTP7655 — XDP_TCK [10,18] / XDP_TDI [10,18] / XDP_TDO [10,18] / XDP_TMS [10,18] / XDP_TRST# [10,18]

MTP7619 MTP7656 MTP7657 MTP7639 MTP7613 MTP7671 — SPI_CLK_R1 [21] / SPI_MOSI_R1 [21] / SPI_MISO_R1 [21] / SPI_WP_IO2_R1 [21] / SPI_HOLD#_IO3_R1 [21] / SPI_CS#0_R [21]

MTP7690 — EDP_I2C_INT [10,57]

MTP7659 — KIP_SWD_CLK [29,74]

MTP7684 — 1P8V_KIP [74]

MTP7667 — SAM_KIP_UART_TX [34,74]

MTP7638 MTP7687 MTP7651 MTP7612 MTP7675 MTP7629 — PCH_TRST# [10,18] / PCH_JTAG_TCK [10,18] / PCH_JTAG_TDI [10,18] / PCH_JTAG_TDO [10,18] / PCH_JTAG_TMS [10,18] / PCH_JTAGX [10,18]

MTP7682 — SAM_UEFIROM_EN [21,35]

MTP7654 MTP7647 — PMI_I2C_SDA [25,28,33] / PMI_I2C_SCL [25,28,33]

MTP7658 MTP7608 — BKLT_PWM_R [72] / BKLT_EN [72]

MTP7694 MTP7695 MTP7696 MTP7923 MTP7649 MTP7699 MTP7670 MTP7927 — BKLT_FB8 [57,72] / BKLT_FB7 [57,72] / BKLT_FB6 [57,72] / BKLT_FB5 [57,72] / BKLT_FB4 [57,72] / BKLT_FB3 [57,72] / BKLT_FB2 [57,72] / BKLT_FB1 [57,72]

MTP7653 MTP7676 — PMI1_I2C_SCL_R [28] / PMI1_I2C_SDA_R [28]

MTP7609 — +3P3V_PANEL_EN [65]

MTP7602 — PIO5_20 [33,35]

MTP7666 — PIO5_21 [33,35]

MTP7673 — SLG_PWRBTN# [58]

MTP7630 — PCH_SENSOR_I2C_SDA [25,54]

MTP7683 — PCH_SENSOR_I2C_SCL [25,54]

MTP76122 MTP76123 MTP76124 MTP76125 — HP_MIC_LR_CON [41] / HPOUT_R_CON [41] / HPOUT_L_CON [41] / HPOUT_JD [40,41]

MTP76129 MTP76130 — DMIC_DATA1_CODEC [40,54] / DMIC_CLK_CODEC [40,54]

MTP76142 MTP76143 MTP76144 MTP76145 — SPK_R+_CON [41] / SPK_R-_CON [41] / SPK_L+_CON [41] / SPK_L-_CON [41]

MTP7635 — +5V_KIP

MTP7626 — PWR_SL1_F

MTP7604 — +1P1V_DDR_VDD2

MTP7679 — +0P6V_DDR_VDDQ

MTP7625 — +VCCPLL_OC

MTP7681 — +3P3VSB

MTP7648 — +5VSB

MTP7627 — +VCCSTG

MTP7636 — +VCC_RTC

MTP7652 — +1P8VSB

MTP7693 — +VCC1P8A

MTP7634 — +1P8V_DDR_VDD1

MTP7606 — RGB_LED_A_P [54]

MTP7691 — RTD3_CAM_PWREN [25,54]

MTP7614 — IRLED_C_N [54]

MTP7644 — IRLED_A_P [54]

MTP7672 — 3P3_CAM [54]

MTP7661 — CAM_IR_STB [54]

MTP7664 — CAM_IR_STB_R [54]

MTP7645 — SL1_EN_N [63]

MTP7620 — SEN_HALL_INT#_S [34,54]

MTP7677 — SEN_HALL_INT#_N [34,54]

MTP7628 — PWRBTN#_1V8_FILT [31]

MTP76100 — VOL_UP#_FILT [31]

MTP76101 — VOL_DOWN#_FILT [31]

MTP76110 MTP7642 MTP7663 — SAM_SWD_SWO [29,33,34] / SAM_SWD_CLK [29,33,34] / SAM_SWD_DIO [29,33,34]

MTP7617 MTP7697 MTP76104 — SL1_HPD2 [70,71] / SL1_HPD1A [70,71] / SL1_HPD1B [70,71]

MTP76173 — BAT_LDO_PACK [70]

MTP76174 — SL1_HPD2_EN#_MTP R7601 1K — SL1_HPD2_EN# [35,72]

+VDD_BATA_PACK

MTP7633 MTP7650 MTP7688 MTP7643 MTP7668 MTP76111 MTP7618 MTP7640 — MTP7959 MTP7610 MTP7660 MTP7680 MTP76112 MTP76113 MTP7605 MTP7622

Place close to J7702

PWR_SL1

MTP76154 MTP76155 MTP76156 MTP76157 MTP76158 MTP76159 MTP76160 MTP76161 — MTP76162 MTP76163 MTP76164 MTP76165 MTP76166 MTP76167 MTP76168 MTP76169

Place close to J7101

MTP7616 — GND MTP Close to J5401

MTP7685 — GND MTP Close to J5401

MTP76131 — GND MTP close to U5505

MTP76132 — GND MTP close to J5701

MTP76133 — GND MTP close to J5701

MTP76134 — GND MTP close to J5401

MTP76135 — GND MTP close to J7701

MTP76136 — GND MTP close to J7701

MTP76137 — GND MTP close to J7701

MTP76138 — GND MTP close to J7701

MTP76139 — GND MTP close to J7701

MTP76140 — GND MTP close to J7701

MTP76170

MTP76171

MTP76172

GND

MTP76190 — Place Close(Under) to JP4001

AGND

MTP76197 — H_PROCHOT# [10,26,63,66]

MTP7646 — DDR_PGD_SIL [58]

MTP7698 — +1P1V_DDR_PG [60]

MTP76102 MTP7662 — EDP_I2C_SCL [57] / EDP_I2C_SDA [57]

MTP76103 MTP76105 MTP76106 MTP76107 MTP7615 MTP76108 MTP7689 MTP76109 — SAM_PIO0_3 [34] / SAM_PIO0_4_ISP0 [34] / SAM_PIO0_5_ISP1 [34] / SAM_PIO0_6_ISP2 [34] / SAMRTS_PCHCTS [25,29,33,34] / TCON_VENDOR_ID [24,57] / PCHRTS_SAMCTS [25,29,33,34] / TP_CATERR#_R [10]

MTP76175 — SL1_PSU_DET [34,70]

MTP76177 MTP76178 MTP76179 MTP76180 MTP76181 MTP76188 MTP76189 — BATEN_PULSE_CONN [70] / BAT_SMCLK [70] / BAT_SMDATA [70] / BATA_DET#_CON [70] / BAT_SHUTDOWN# [33,58,70] / KIP_LS_EN_R [74] / KIP_EN [64]

MTP76191 MTP76192 MTP76193 MTP76194 — PCH_DBG_TX [25,29,33] / PCH_DBG_RX [25,29,33] / SAM_DBG_TX [29,33,34,71] / SAM_DBG_RX [29,33,34,71]

MTP76196 — FPC_DET_LOGIC_OVERRIDE# [33,58]

In RAFLA this Signal will be pulled "LOW" via 1K resistor

+VBUS_P0_CONN

MTP76114 MTP76115 MTP76116 MTP76117 MTP76118 MTP76119

+3P3V_PANEL +VSYS EXT_DC_IN +3P3VA +3P3V +3P3V_SSD_CON +3P3V_BB0

MTP76176 MTP76182 MTP76183 MTP76184 MTP76185 MTP76186 MTP76187

+VCC_EDP_BKLT_OUT

MTP76120 MTP76121

+1P8V_AUDIO

MTP7603

+VCCST_CPU

MTP7621

+VCCIN

MTP7637

+VCCIN_AUX

MTP7665

+5V_KIP

MTP7632

+1P8VA

MTP7692

+5V_AUDIO

MTP7624

MTP76141 — SAM_RESET# [29,33,34,58]

MTP76126 MTP76127 — USB2_USBA_DN_CONN [45] / USB2_USBA_DP_CONN [45]

MTP76128 — CON2_VBUS

MTP76146 MTP76147 MTP76148 MTP76149 — TCP0_CONN_CC1 [77] / USB2_TCP0_CONN_A_DP [77] / USB2_TCP0_CONN_A_DN [77] / TCP0_CONN_SBU1 [77]

MTP76150 MTP76151 MTP76152 MTP76153 — TCP0_CONN_SBU2 [77] / USB2_TCP0_CONN_B_DN [77] / USB2_TCP0_CONN_B_DP [77] / TCP0_CONN_CC2 [77]

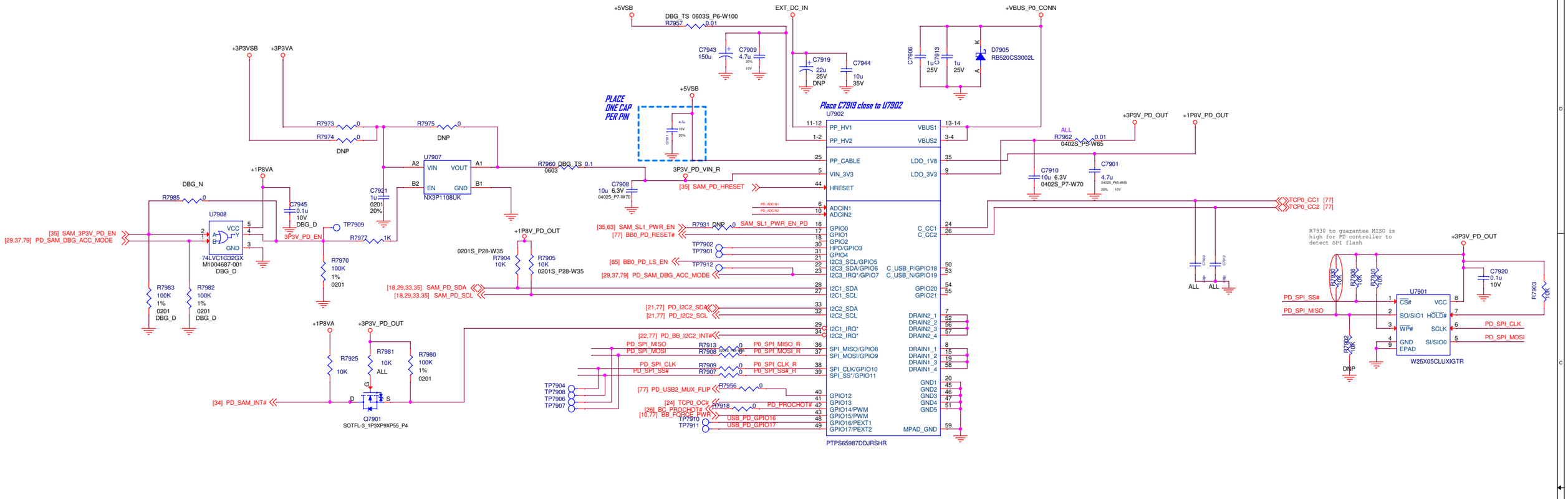
W x H 427 x 276 mm

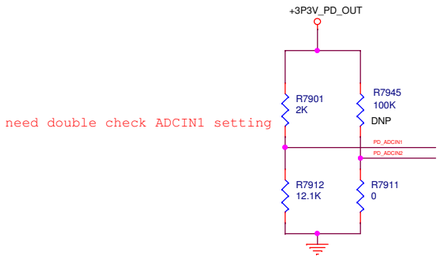
Title: Frames, Holes, & Mechanical			
<OrgName>	Engineer: <OrgAddr1>		
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 76 of 82		

U7700A
EE_DI
EE_DO
EE_CS#
EE_CLK
TDI
TMS
TCK
TDO
THERMDA
TEST_EDM
FUSE_VQPS_64
MONDC
MONDC_SVR
TEST_PWR_GOOD
TEST_EN
ATEST_P
ATEST_N
I2C_SCL
I2C_SDA
I2C_INT
FORCE_PWR
FLASH_BUSY
POC_GPIO_5
POC_GPIO_6
POC_GPIO_10
POC_GPIO_11
POC_GPIO_12
PERST
SMBUS_SCL
SMBUS_SDA
RESET
XTAL_25_IN
XTAL_25_OUT
RSENSE
RBIAS
QUTZ 9999HF
M1111477-001
+3P3VSB
+VCC3P3_LC_TCP0
BB0_TEST_PWR_GOOD
BB0_RESET#
BB0_PD_RESET# [79]
BB0_FORCE_PWR_R
BB_FORCE_PWR [10,79]
BB0_POC_GPIO_5
BB0_POC_GPIO_6
BB0_FLASH_SHARE_EN
BB0_FLASH_MASTER
BB0_POC_GPIO_12
BB_PERST# [22]
PD_SML0_SCL [25]
PD_SML0_SDA [25]
PD_I2C2_SCL [21,79]
PD_I2C2_SDA [21,79]
PD_BB_I2C2_INT# [22,79]
TCP0_XTAL_25_OUT
TCP0_XTAL_25_IN
Y7701
ALL
25MHz
D7701
RB520CS3002L
3P3V_RT_FLASH
U7702
MX25L8006EZUI-12G
TCP0_EE_CS#
TCP0_EE_DO
TCP0_EE_CLK
TCP0_EE_DI
U7700C
QUTZ 9999HF
M1111477-001
VCCP3P3_SVR_TCP0
+3P3V_BB0
+3P3V_PD_OUT
U7703
NX20P0407UK
TCP0_CC1
TCP0_CC2
TCP0_SBU1
TCP0_SBU2
TCP0_SBUEN
TCP0_CONN_CC1
TCP0_CONN_CC2
TCP0_CONN_SBU1
TCP0_CONN_SBU2
+VBUS_P0_CONN
J7701
M1084960-001
TCP0_TX_CONN_P0
TCP0_TX_CONN_N0
TCP0_TX_CONN_P1
TCP0_TX_CONN_N1
TCP0_TXRX_CONN_P0
TCP0_TXRX_CONN_N0
TCP0_TXRX_CONN_P1
TCP0_TXRX_CONN_N1
USB2_TCP0_CONN_A_DP
USB2_TCP0_CONN_A_DN
USB2_TCP0_CONN_B_DP
USB2_TCP0_CONN_B_DN
Use 25V cap on the connector side to protect pin short to VBUS
U7700D
ASSRXP1
ASSRXN1
ASSTXP1
ASSTXN1
ASSRXP2
ASSRXN2
ASSTXP2
ASSTXN2
PA_LSTX_SBU1
PA_LSRX_SBU2
PA_AUX_P
PA_AUX_N
BSSRXP1
BSSRXN1
BSSTXP1
BSSTXN1
BSSRXP2
BSSRXN2
BSSTXP2
BSSTXN2
BSBU1
BSBU2
TCP0_BB_SBU1 [29]
TCP0_BB_SBU2 [29]
[10] TBT_LSX0_TXD
[10] TBT_LSX0_RXD
[10] TCP0_AUX_DP
[10] TCP0_AUX_DN
TCP0_AUX_DP_R
TCP0_AUX_DN_R
D7703
D7707
D7710
D7711
D7716
D7718
D7712
D7714
ESDL2011PFCT5G
D7708
D7702
D7709
D7715
PESD24VF1BL
PESD24VF1BL
+3P3V_DEBUG
U7704
TS3USB30E
USB2_TCP0_DP [24]
USB2_TCP0_DN [24]
[79] PD_USB2_MUX_FLIP
USB2_TCP_MUX_EN#
[29] MUX0_EN#
Q7701
U7704 Layout Short during PV/DV
+VCC3P3_LC_TCP0
+VCC0V9_SVR_TCP0
+VCC3V3_TCP0
+VCC3V3A_TCP0
U7700B
VCC3P3_ANA
VCC3P3_LC
VCC0P9_SVR_1
VCC0P9_SVR_2
VCC0P9_SVR_PB_ANA_1
VCC0P9_SVR_PB_ANA_2
VCC0P9_SVR_ANA_1
VCC0P9_SVR_ANA_2
VCC0P9_LC
VCC0P9_LVR
VCC0P9_LVR_SENSE
VCC3P3_SX
VCC3P3_SVR_1
VCC3P3_SVR_2
VCC3P3A
SVR_IND_1
SVR_IND_2
SVR_VSS_1
SVR_VSS_2
QUTZ 9999HF
M1111477-001
L7706
0.68uH
+VCC0P9_SVR_TCP0_PHASE
BB_FORCE_PWR
BB0_FLASH_SHARE_EN
BB0_FLASH_MASTER
BB0_POC_GPIO_12
BB0_POC_GPIO_5
BB0_POC_GPIO_6
BB0_POC_GPIO_12: Has internal PU
BB_FORCE_PWR:
'0' - By default
'1' - For debug only/FW update
BB0_FLASH_SHARE_EN (internal-PU)
'0' - Flash isn't shared, 1 flash per re-timer
'1' - Flash is shared between 2 re-timers
BB0_FLASH_MASTER (internal-PU)
'0' - Set re-timer to be slave on shared flash SPI I/F
'1' - Set re-timer to be master on shared flash SI I/F
TCP0_DBG0_A_DP
TCP0_DBG1_A_DN
TCP0_DBG2_B_DP
TCP0_DBG3_B_DN
USB2_TCP0_CONN_A_DP
USB2_TCP0_CONN_A_DN
USB2_TCP0_CONN_B_DP
USB2_TCP0_CONN_B_DN
DLP11TB800UL2L
RN7704 0 DNP
RN7703 0 DNP
D7721 PESD5V0H1BSF
D7720 PESD5V0H1BSF
D7719 PESD5V0H1BSF
D7722 PESD5V0H1BSF
20160609sjs1551
title is: Blank_602x390
Report errors to Steven
Title: Blank_602x390
<OrgName>
Engineer: <OrgAddr1>
Size: Custom
Project Name: EDAN_A_EV1
Rev: 1.00
Date: Tuesday, May 21, 2019
Sheet 77 of 94
Width 602 x 390mm

Title:	Blank
<OrgName>	Engineer: <OrgAddr1>
Size: Custom	Project Name: EDAN_A_EV1
Rev: 1.00	
Date: Tuesday, May 21, 2019	Sheet 78 of 94

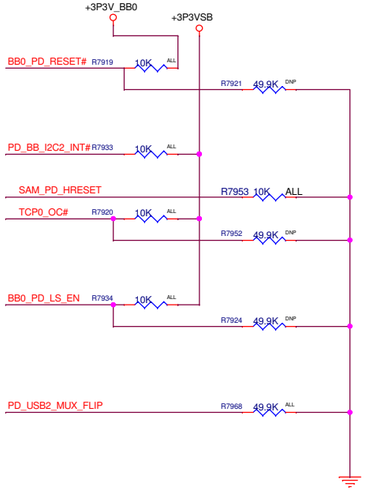
Width 610mm x 330mm



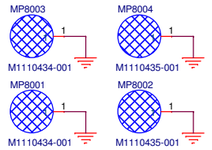


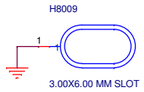
ADCIN1: EXTERNAL BUS POWER
ADCIN2: I2C SETTINGS

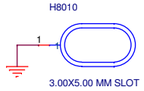
7-BIT I2C ADDRESS
I2C1 - 0X20
I2C2- 0X38

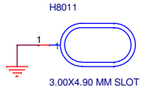


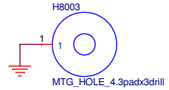
Title:	Type C Power		
<OrgName>	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: EDAN_A_EV1		Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 79 of 82		

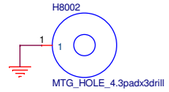


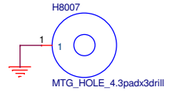


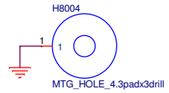


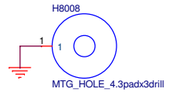


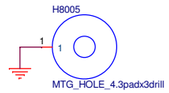


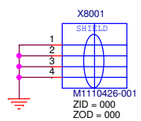


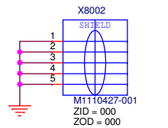


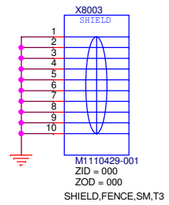


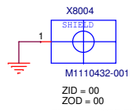


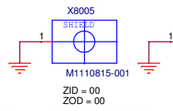


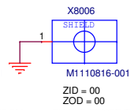


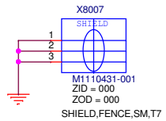


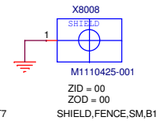












Width 610mm x 390mm

Title: Mechanical

<OrgName> Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00

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Title:	ACC Radio	
<OrgName>	Engineer:	<OrgAddr1>
Size: A2	Project Name: EDAN_A_EV1	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet 81 of 82	

Title:	Holes, Shields & Fences
<OrgName>	Engineer: <OrgAddr1>
Size: Custom	Project Name: EDAN_A_EV1
Date: Tuesday, May 21, 2019	Sheet 82 of 82

Width 610mm x 390mm