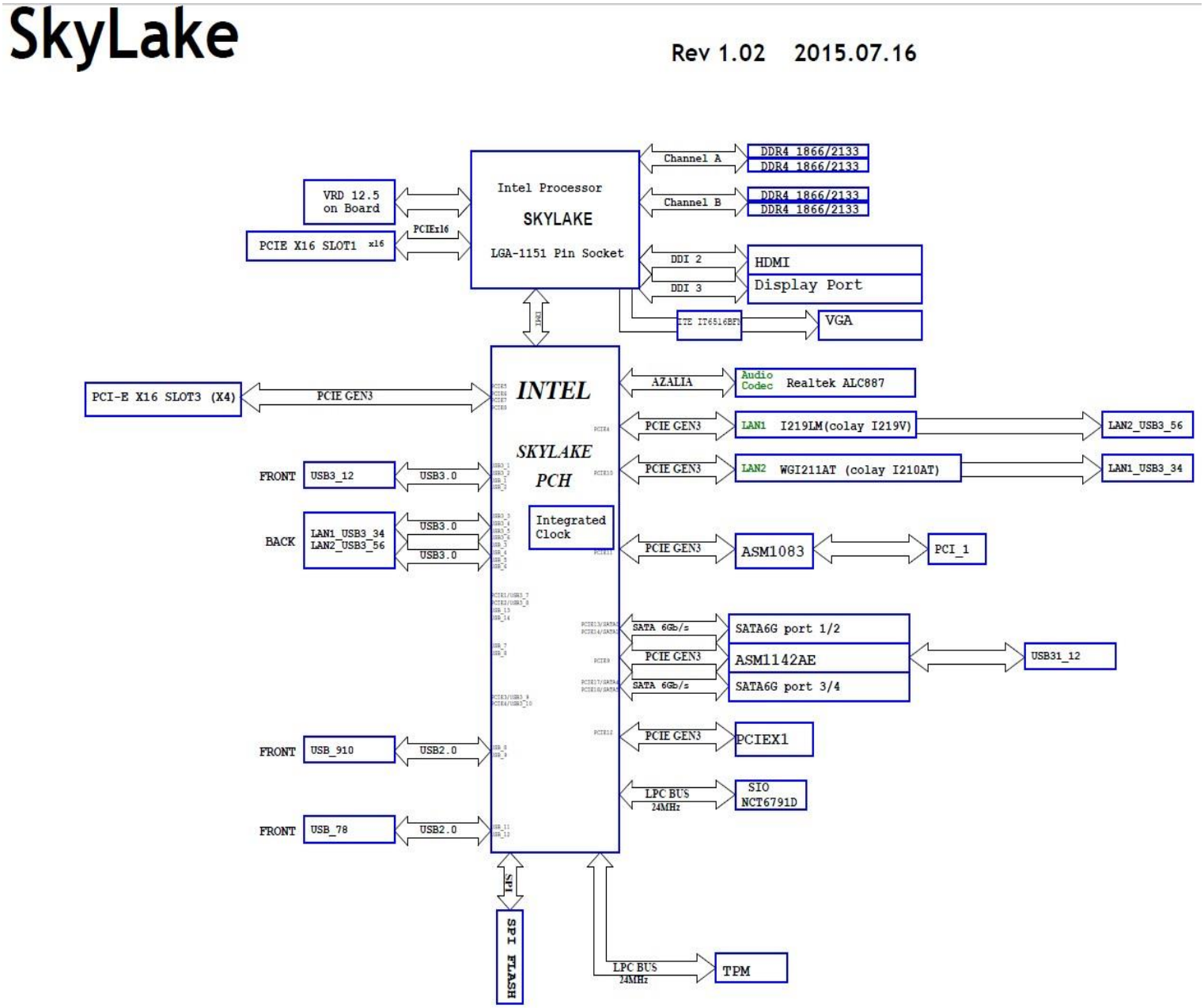
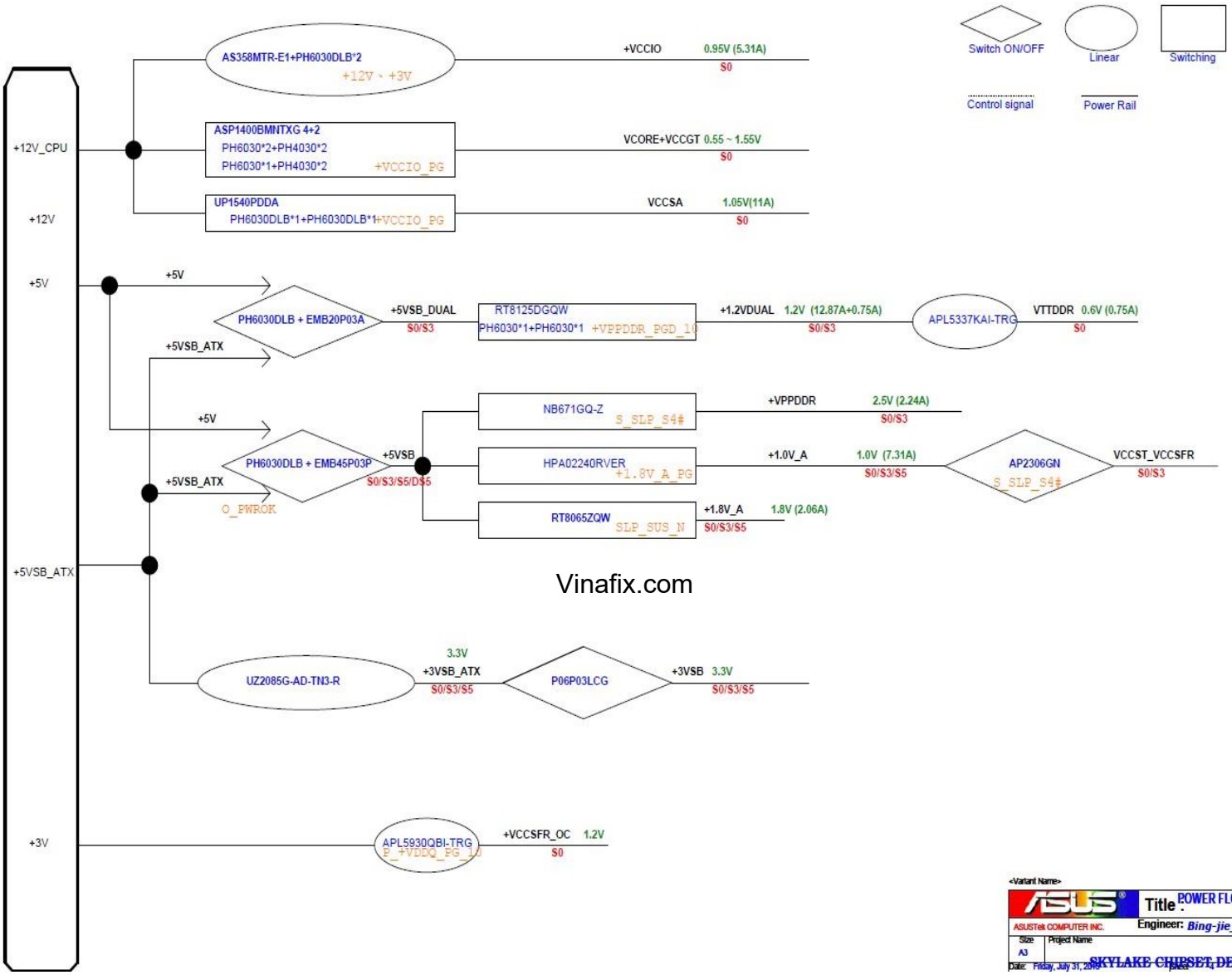
## 1. BLOCK DIAGRAM



## 2. POWER FLOW






<Variant Name>

ASUSTeK COMPUTER INC.

Title : POWER FLOW

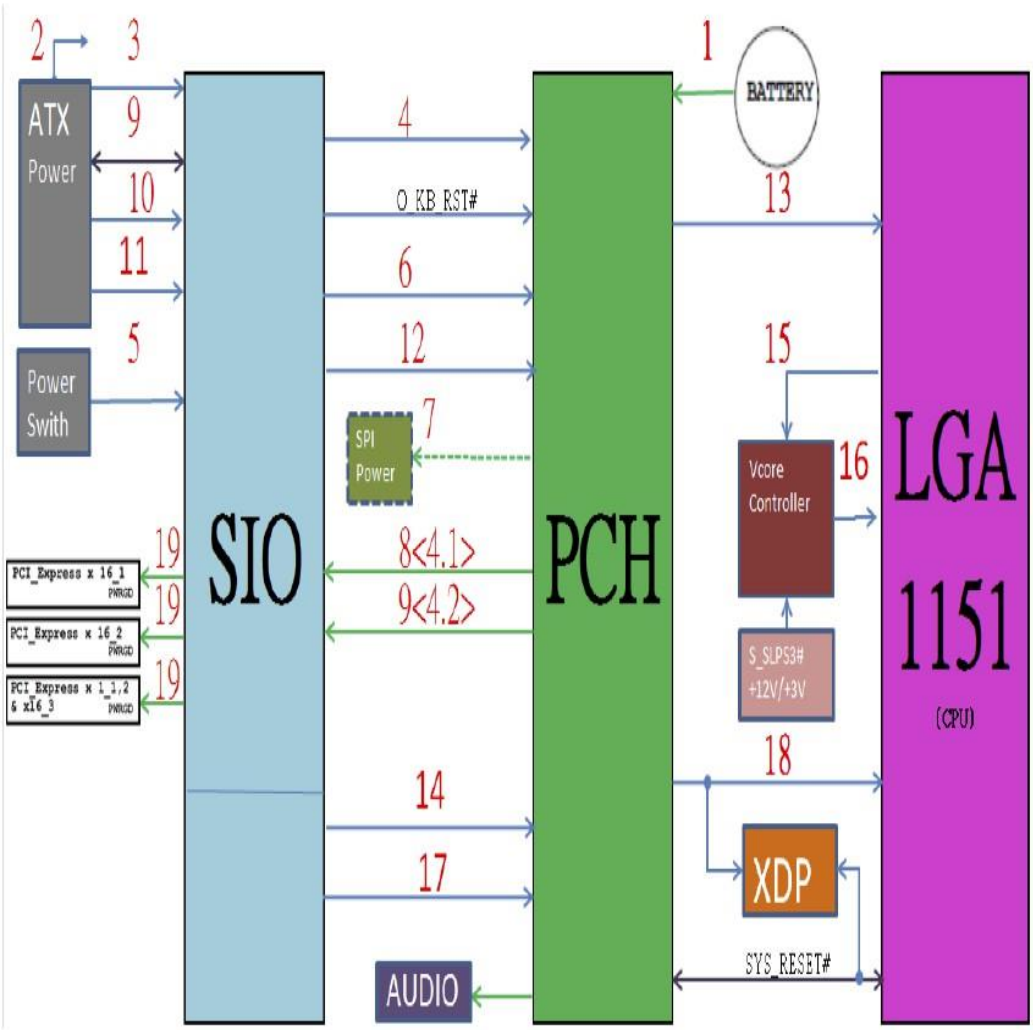
Engineer: Bing-jie_Wa

Size: A3 | Project Name

Date: Friday, July 31, 2015 | Sheet

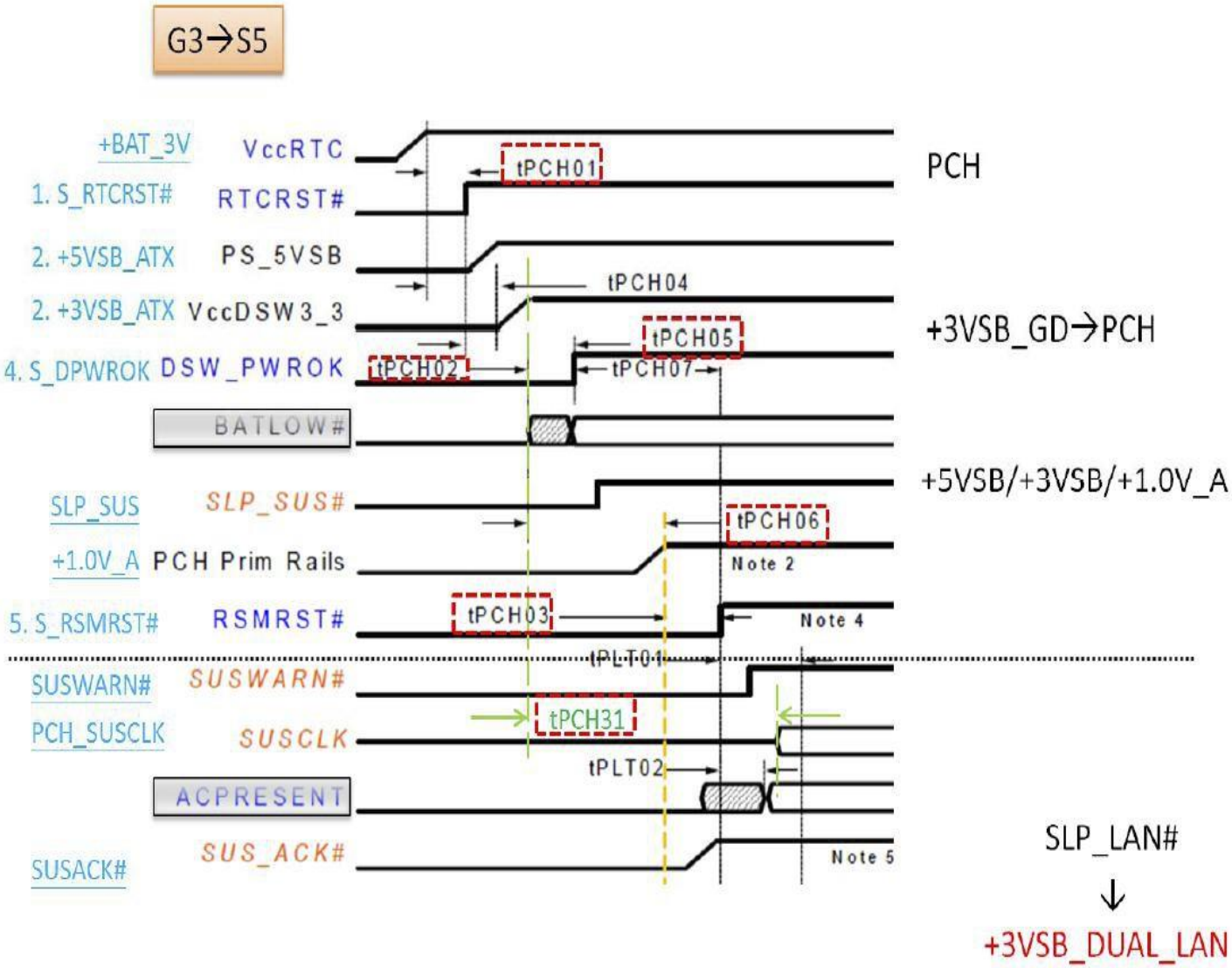
SKYLAKE CHIPSET DEMO

## 3. POWER ON SEQUENCE

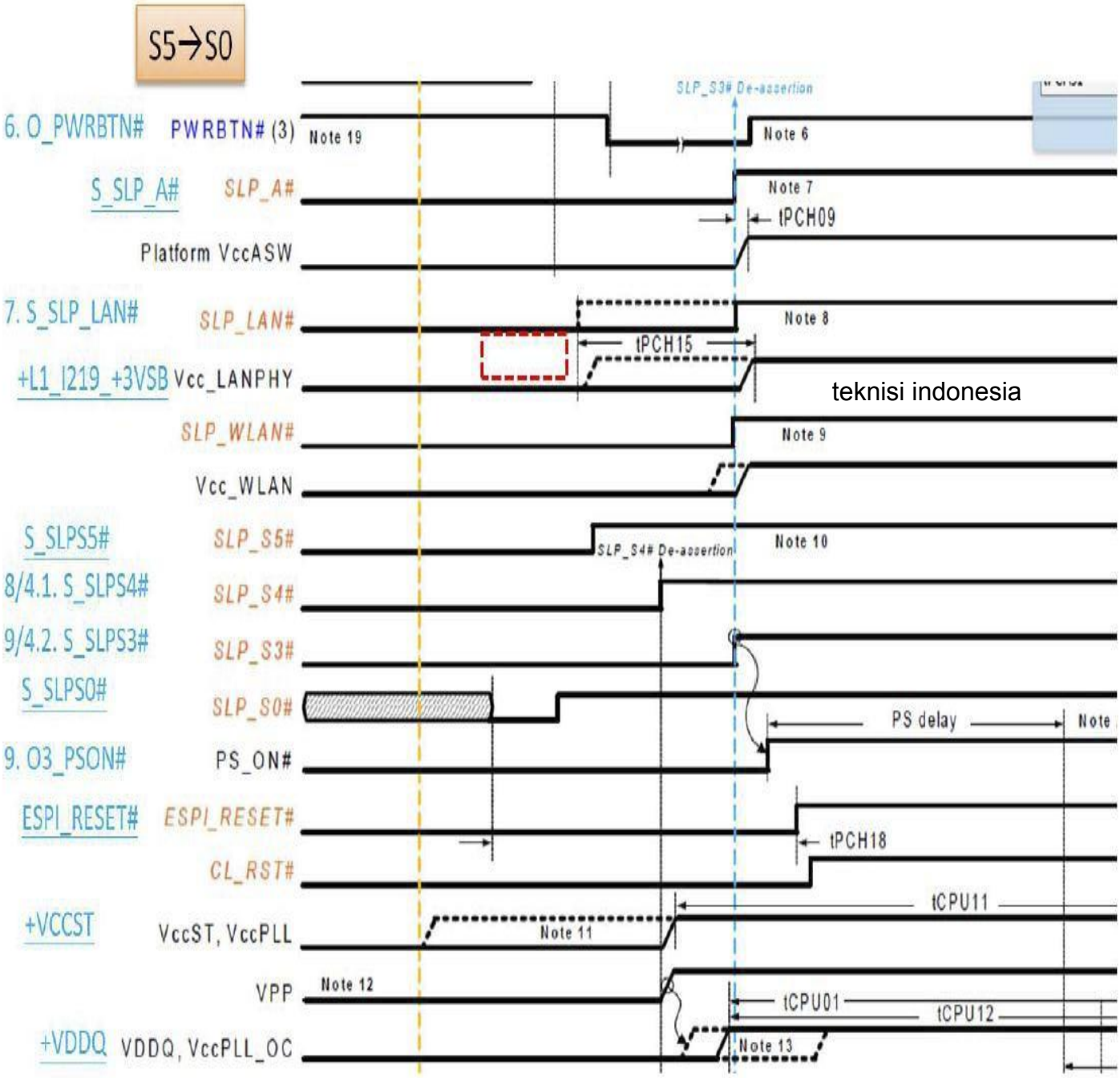


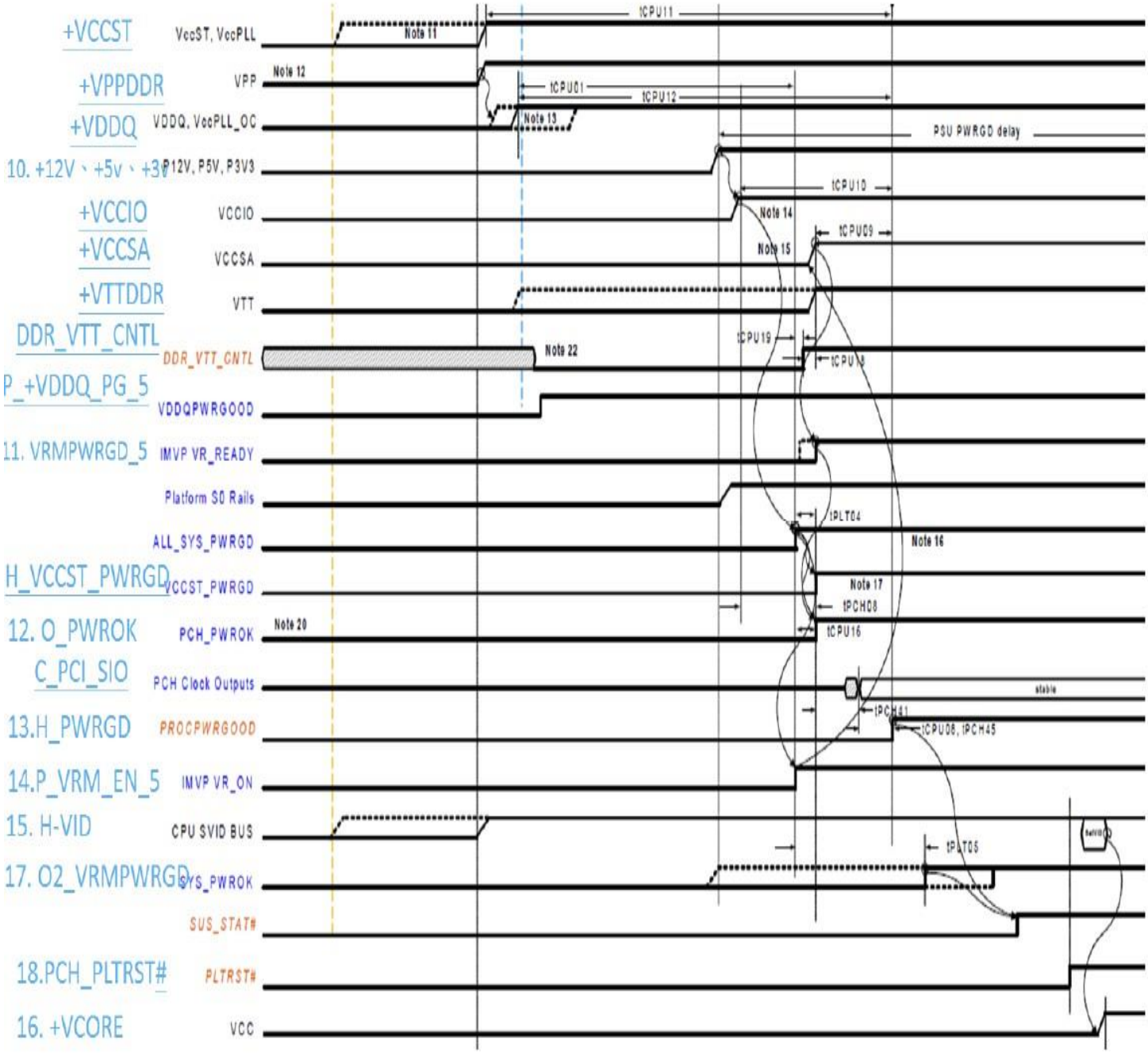

| Signal Measure Point | |
|---|---|
| Sequence | Net Name |
| 1 | S_RTCRST# |
| 2 | +5VSB_ATX;+3VSB_ATX |
| 3 | +5VSB;+3VSB |
| 4 | O_RSMRST# |
| 5 | O_PWRBTN#IN |
| 6 | O_PWRBTN# |
| 7 | S_SLP_LAN# |
| 8/<4.1> | S_SLPS4# |
| 9/<4.2> | S_SLPS3# |
| 9 | O_PSON# /O3_PSON# |
| 10 | 12V,5V,3V |
| 11 | VRMPWRGD_5/B_ATX_PWROK |
| 12 | O_PWROK |
| 13 | H_PWRGD |
| 14 | P_VRM_EN_5 |
| 15 | H_VIDDATA/ H_VIDCLK |
| 17 | O2_VRMPWRGD |
| 18 | H_CPURST# /PCH_PLTRST# |
| 16 | +VCORE |
| 19 | O_PCIRST#_PCIEX16_1<br>O_PCIRST#_PCIEX16_2<br>O_PCIRST#_PCIEX16_3 |

## 4. Timing Diagram for G3 to S5

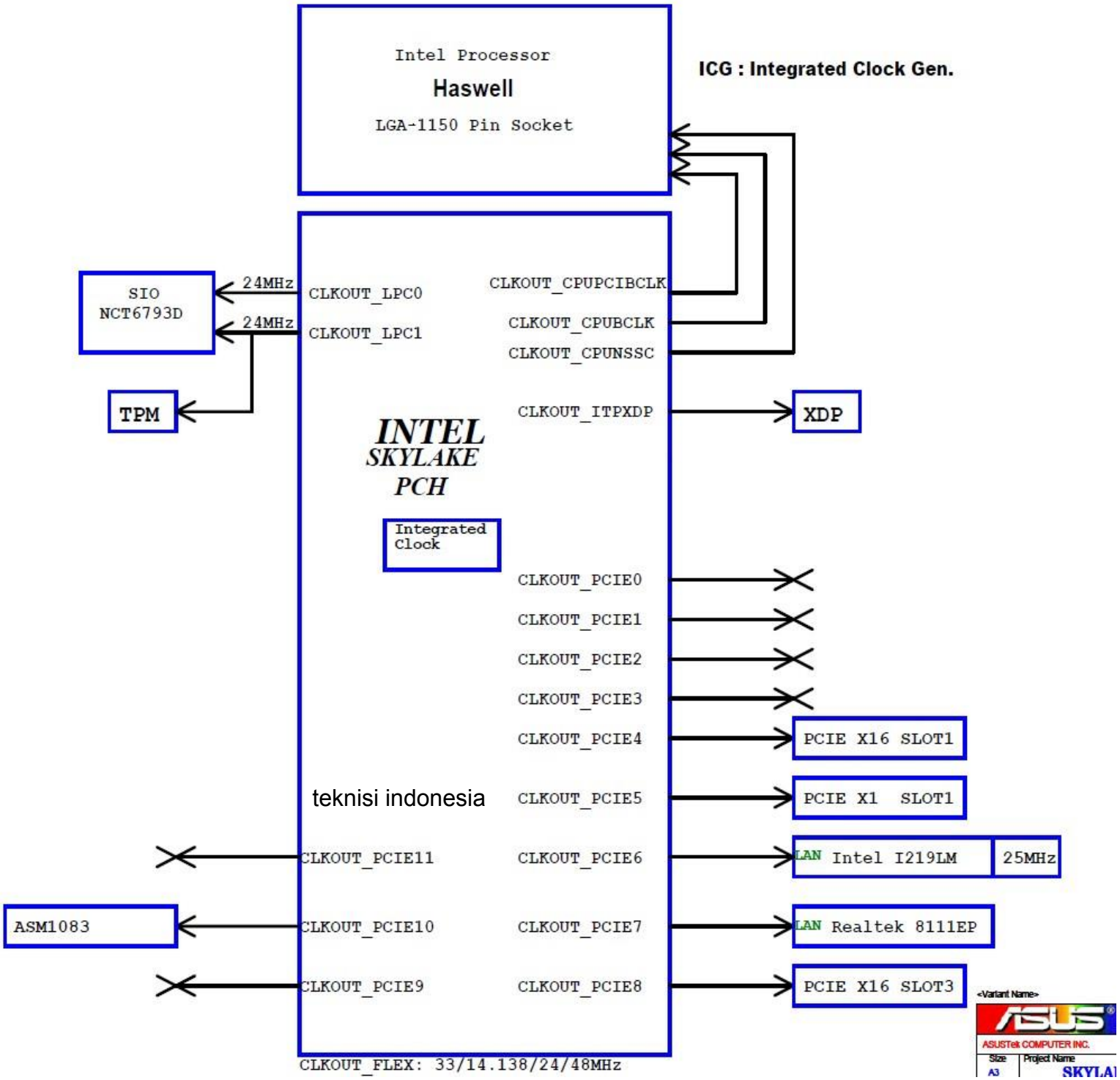


**Timing Diagram for S5 to S0/M0**




+VCCST
VccST, VccPLL
+VPPDDR
VPP
+VDDQ
VDDQ, VccPLL_OC
10. +12V、+5v、+3v
P12V, P5V, P3V3
+VCCIO
VCCIO
+VCCSA
VCCSA
+VTTDDR
VTT
DDR_VTT_CNTL
DDR_VTT_CNTL
P_+VDDQ_PG_5
VDDQPWRGOOD
11. VRMPWRGD_5
IMVP VR_READY
Platform S0 Rails
ALL_SYS_PWRGD
H_VCCST_PWRGD
VCCST_PWRGD
12. O_PWROK
PCH_PWROK
C_PCI_SIO
PCH Clock Outputs
13.H_PWRGD
PROCPWRGOOD
14.P_VRM_EN_5
IMVP VR_ON
15. H-VID
CPU SVID BUS
17. O2_VRMPWRGD
SYS_PWROK
SUS_STAT#
18.PCH_PLTRST#
PLTRST#
16. +VCORE
VCC
Note 11
Note 12
Note 13
Note 14
Note 15
Note 16
Note 17
Note 20
Note 22
tCPU11
tCPU01
tCPU12
PSU PWRGD delay
tCPU10
tCPU09
tCPU19
tPLT04
tPCH08
tCPU16
stable
tPCH41
tCPU08, tPCH45
tPLT05

5. **Frequency Flow**



## 6. Voltage Measure Point

| Voltage Measure Point | | |
|---|---|---|
| **Station** | **Net Name** | **Diode resistance** |
| **PU702** | +3VSB_ATX | 336 |
| **PQ605** | +5VSB | 494 |
| **PL201** | +VCCGT | 484 |
| **PL704** | +VCCSA | 508 |
| **EATX12V** | 12V_CPU | 552 |
| **OQ760** | +3VSB | 320 |
| **PC550** | VTT_DDR | 430 |
| **EATXPWR** | +5VSB_ATX | 585 |
| **PQ611** | +5VSB_DUAL | 485 |
| **EATXPWR** | +12V | 491 |
| **EATXPWR** | +5V | 408 |
| **EATXPWR** | +3V | 312 |
| | | |
| | | |

## 7.Signal Measure Point

| | | Signal Measure Point | |
|---|---|---|---|
| **Station** | **Sequence** | **Net Name** | **Diode resistance** |
| **SR119**<br>**SR121** | 1 | S_RTCRST#<br>S_SRTCRST# | 778<br>778 |
| **NA** | 2 | AC Power Switch ON | NA |
| **PQ605**<br>**OQ760** | 3 | +5VSB<br>+3VSB | 494<br>320 |
| **SR83** | 3.1 | S_DPWROK | 35 |
| **PD701** | 4 | O_RSMRST# | 35 |
| **O1R6** | 5 | PWRBTN# | 846 |
| **O1R14** | 6 | O_PWRBTN#R | 532 |
| **SD5** | 7/4.2 | S_SLPS3# | 501 |
| **NA** | 7 | S_SLP_A# | NA |
| **NA** | 7.1 | S_SLP_LAN# | NA |
| **PQ532** | 8/4.1 | S_SLP_S4# | 522 |
| **EATXPWR** | 9 | ATX_PSON#_R | 580 |
| **EATXPWR**<br>**EATXPWR**<br>**EATXPWR** | 10 | +12V<br>+5V<br>+3V | 491<br>408<br>312 |
| **NA** | 11 | P_PWROK_PS | NA |
| **O1R12** | 12 | O_PWROK | 27 |
| **SR75** | 13 | H_CPUPWRGD | 446 |
| **HR210**<br>**PR109** | 14 | H_SVID_DATA<br>H_SVID_CLK | 502<br>505 |
| **PC168** | 15 | VCORE | 436 |
| **SQ6** | 16 | P_VR_READY_10 | 458 |
| **SR2** | 17 | S_PLTRST# | 466 |
| **ESDC3** | 18 | H_CPURST# | 430 |
| **XC74**<br>**XC71** | 19 | O_X1_RST#<br>O_X16_RST# | 588<br>582 |