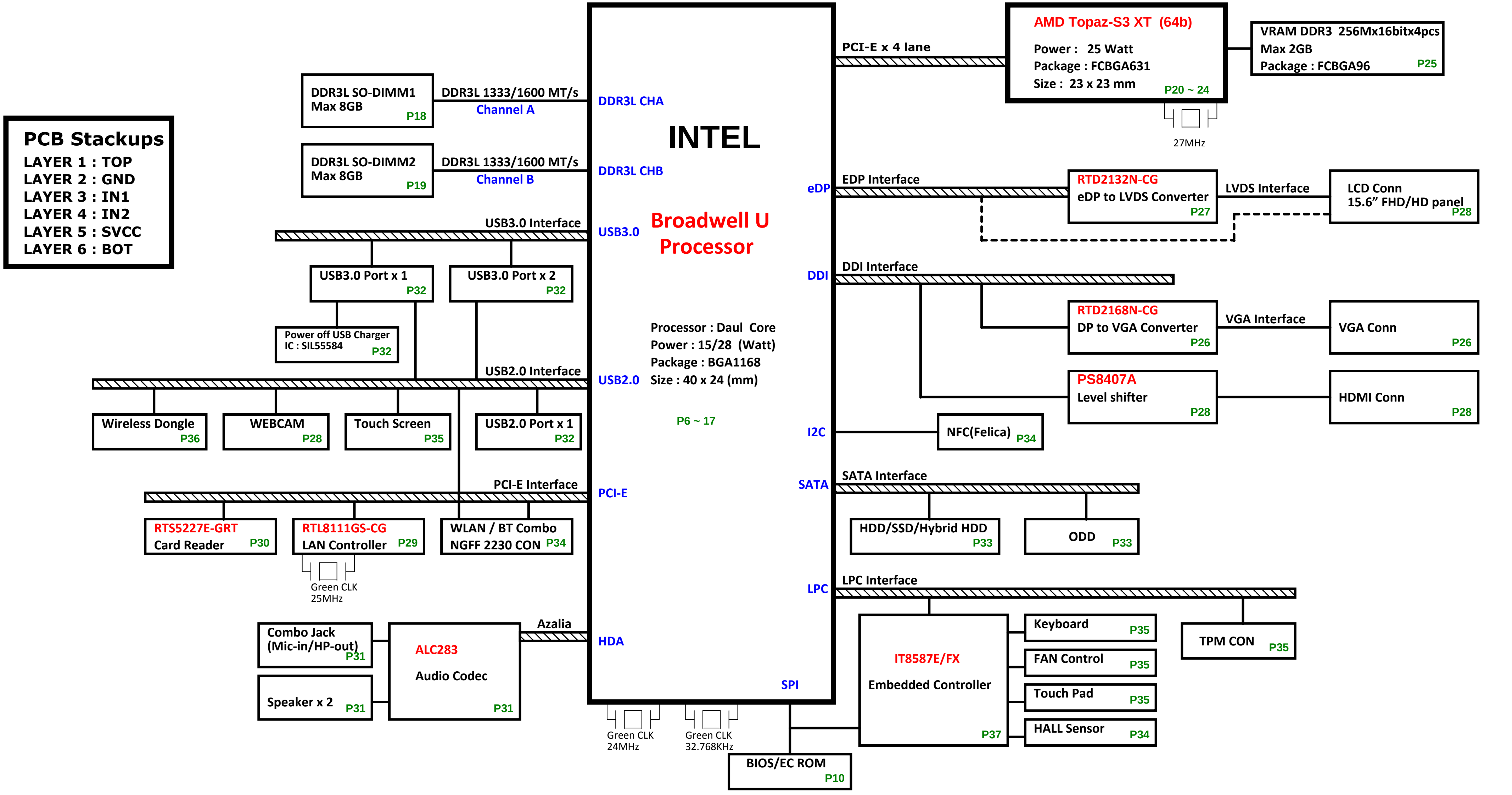
FH9 DIS (15.6") Broadwell Platform Block Diagram



Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

Date: Wednesday, November 19, 2014 Sheet 1 of 48

Table of Contents

Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal
3V_RTC	3V	ON	ON	ON	ON	ON	
VIN	19V	ON	ON	ON	ON	OFF	Adaptor in
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in
5V_S5	5V	ON	ON	ON	ON	OFF	S5_ON
3V_S5	3.3V	ON	ON	ON	ON	OFF	S5_ON
1.35V_S3	1.35V	ON	ON	OFF	OFF	OFF	S3_ON
5V_S3	5V	ON	ON	OFF	OFF	OFF	S3_ON
3VDUAL_LAN	3.3V	ON	OFF	OFF	OFF	OFF	LAN_ON_EC
3V_WLAN	3.3V	ON	OFF	OFF	OFF	OFF	WLAN_ON
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1
3V_S0	3.3V	ON	OFF	OFF	OFF	OFF	S0_ON_2
1.5V_S0	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_3
1.05V_S0	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
1.05V_VCCST	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_1
DDR_VTERM	0.675V	ON	OFF	OFF	OFF	OFF	DDR_PG
VCC_CORE	1.7V	ON	OFF	OFF	OFF	OFF	H_VR_EN_MCP
VGA_CORE	1V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
3V_GPU	3.3V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.8V_GPU	1.8V	ON	OFF	OFF	OFF	OFF	GPU_ON
1.5V_GPU	1.5V	ON	OFF	OFF	OFF	OFF	1.8VGPU_PG
0.95V_GPU	0.95V	ON	OFF	OFF	OFF	OFF	GPU_ON

Function List

USB2		PCIE		Display		USB3		SATA	
Port 0	Co-lay USB3.0	Port 1	Card Reader	eDP Port 1	LVDS or eDP	Port 1	USB3.0 Conn	Port 0	HDD
Port 1	Co-lay USB3.0	Port 2	USB3.0 Conn	eDP Port 2	NC	Port 2	USB3.0 Conn	Port 1	ODD
Port 2	Co-lay USB3.0	Port 3	WLAN	DDI Port 1	HDMI	Port 3	Card Reader	Port 2	NC
Port 3	Touch screen	Port 4	GLAN	DDI Port 2	CRT	Port 4	USB3.0 Conn	Port 3	NC
Port 4	Camera	Port 5	GPU(TOPAZ)						
Port 5	USB2.0 Conn								
Port 6	Bluetooth								
Port 7	USB HUB								

Function Select

S@	TOPAZ + VRAM
L@	RTD2132N-CG
E@	Internal eDP
V@	RTD2168
N@	NFC
M@	MMB
TS@	Touch screen
WL@	Wireless Dongle

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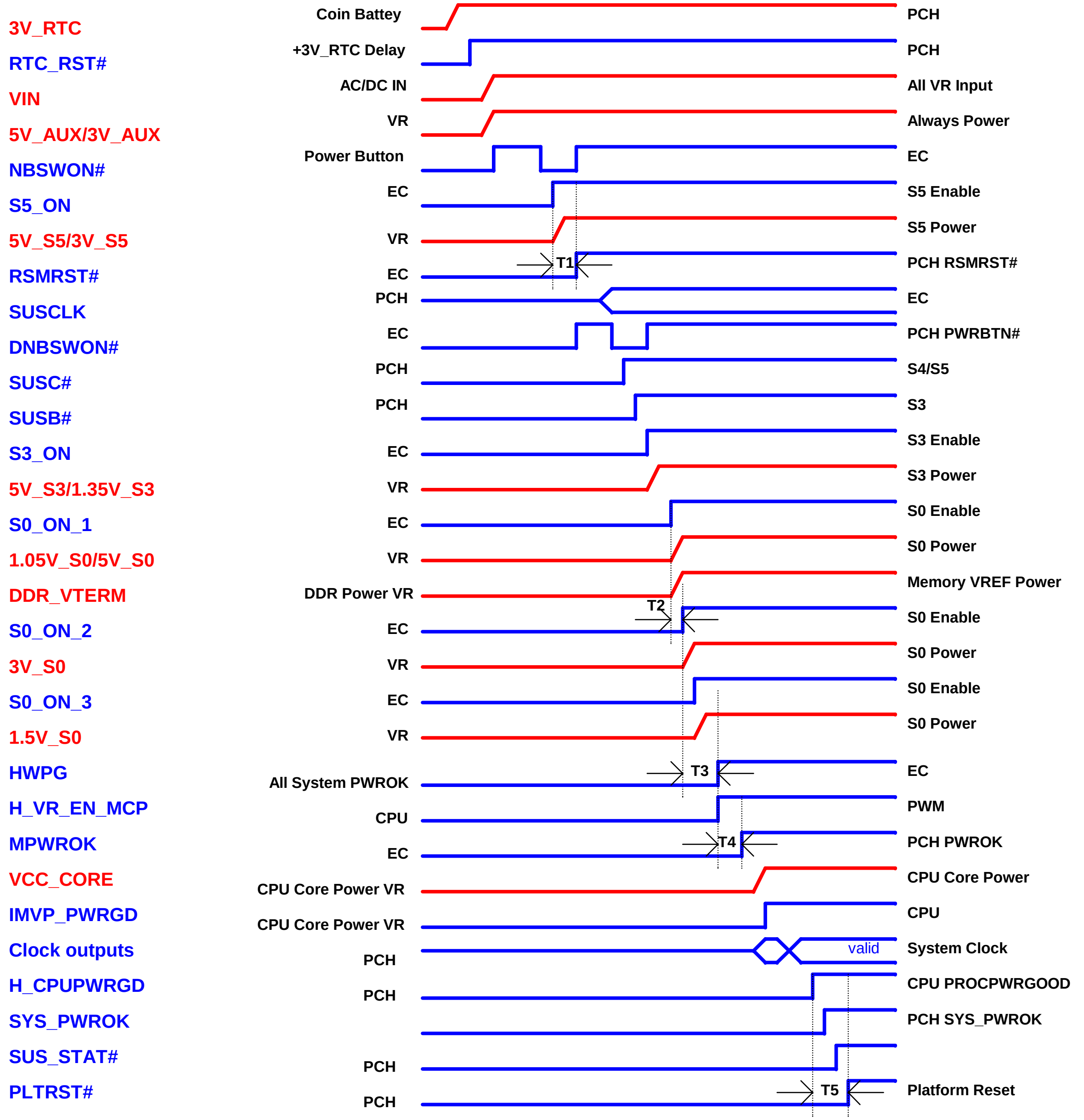
PROJECT : FH9

Size	Document Number	Rev
	FRONT PAGE	2A

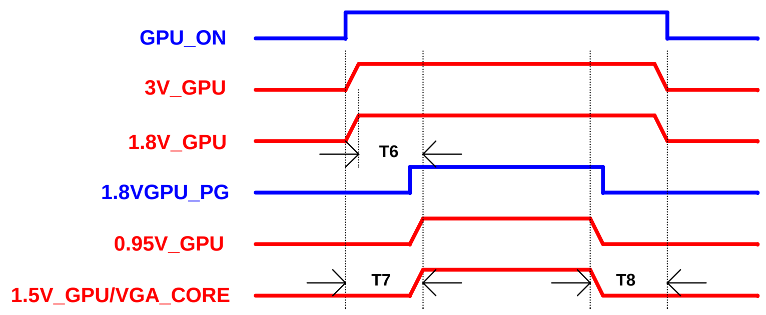
System Power On Sequencing Timing Diagram



System Power Sequence

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
T2: S0_ON_1 TO S0_ON_2 = 500us
T3: S0_ON_2 TO VRON = 10ms
T4: HWPG TO MPWROK = 110ms (spec：>5~ 99ms)
T5: H_CPUPWRGD to PLTRST# >1ms

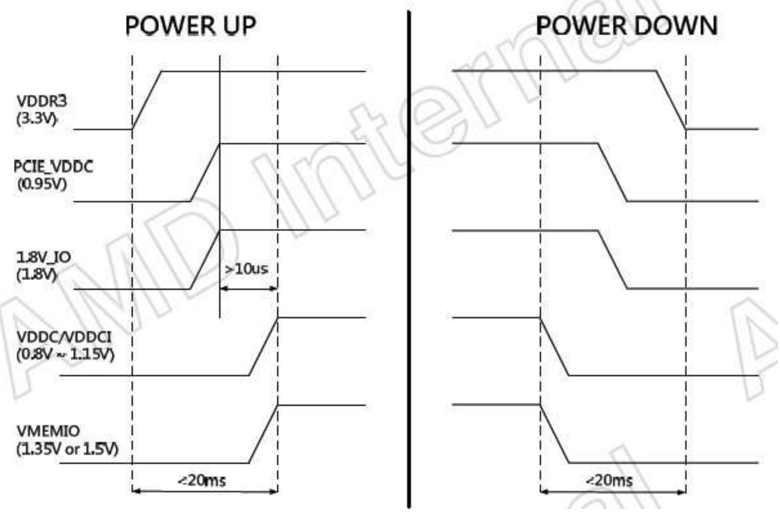
dGPU Power On/Off Sequencing Timing Diagram



dGPU Power Sequence

T6：1.8V_GPU to 1.5V_GPU > 10us
T7：3V_GPU to 1.5V_GPU < 20ms
T8：1.5V_GPU to 3V_GPU < 20ms

POWER UP / POWER DOWN SEQUENCE



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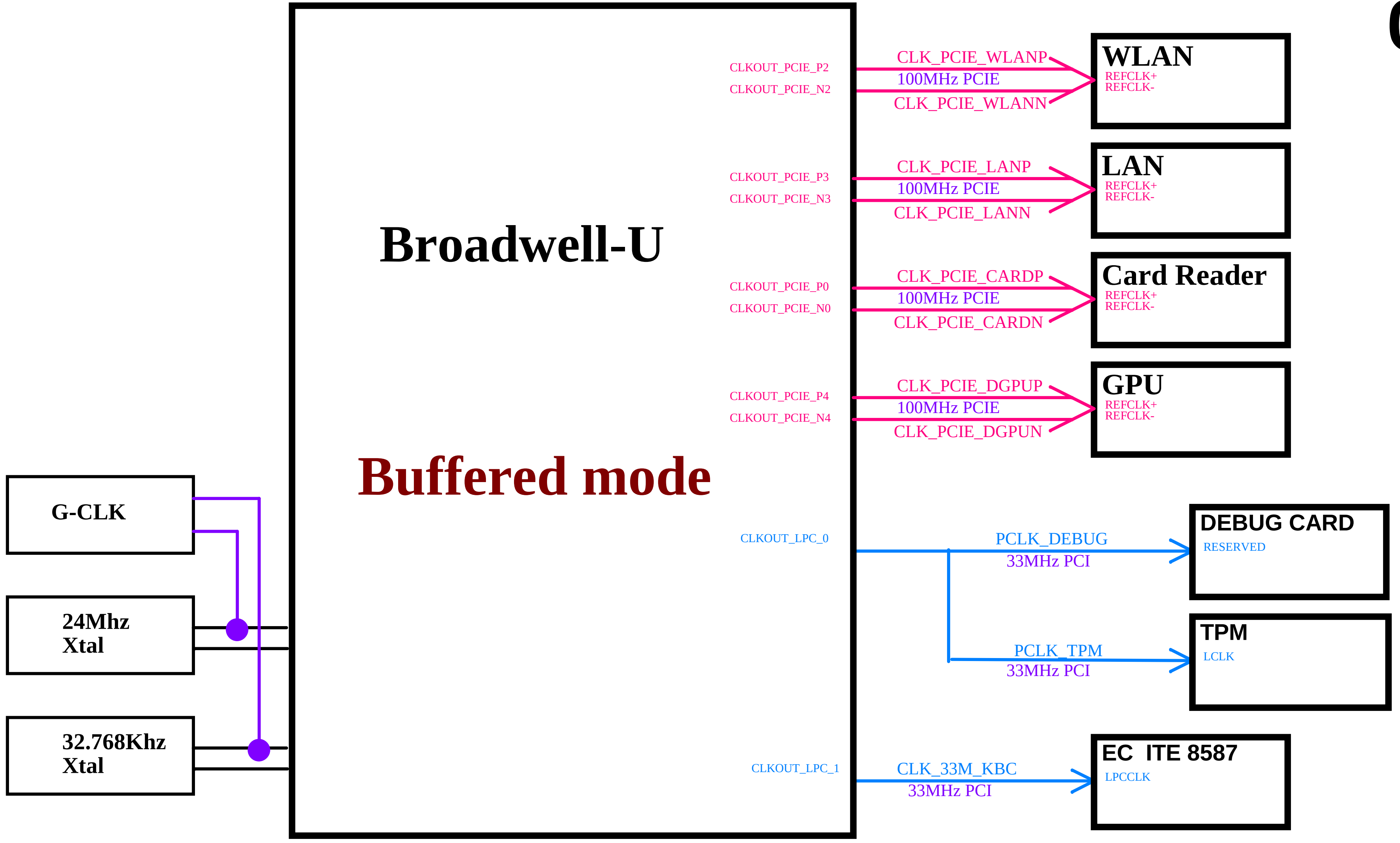
PROJECT : FH9

Size	Document Number	Rev
	Power Sequence	2A

Date: Wednesday, November 19, 2014 Sheet 3 of 48



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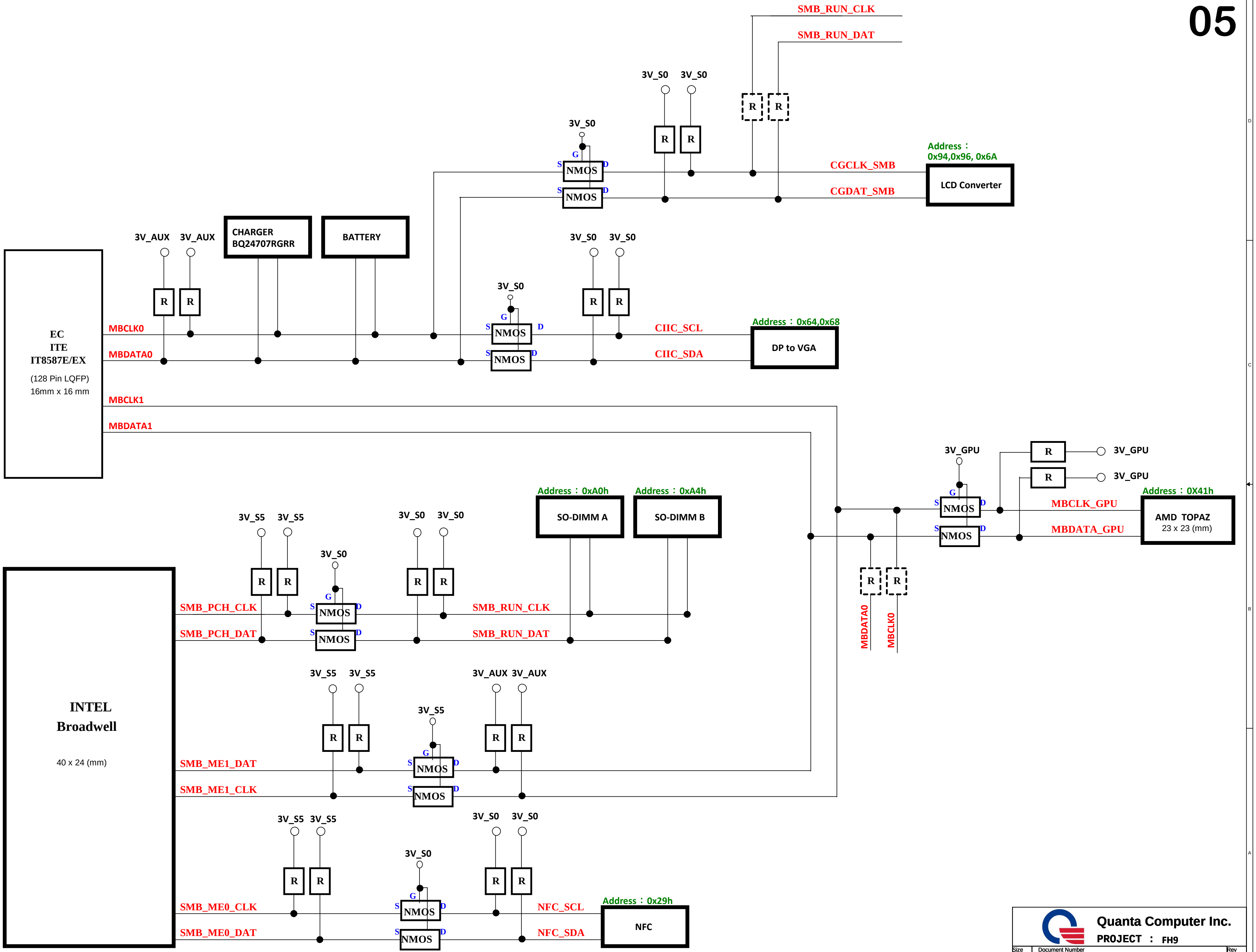
PROJECT : FH9

Size	Document Number	Rev
	Clock Distribution	2A

Date: Wednesday, November 19, 2014 | Sheet 4 of 48



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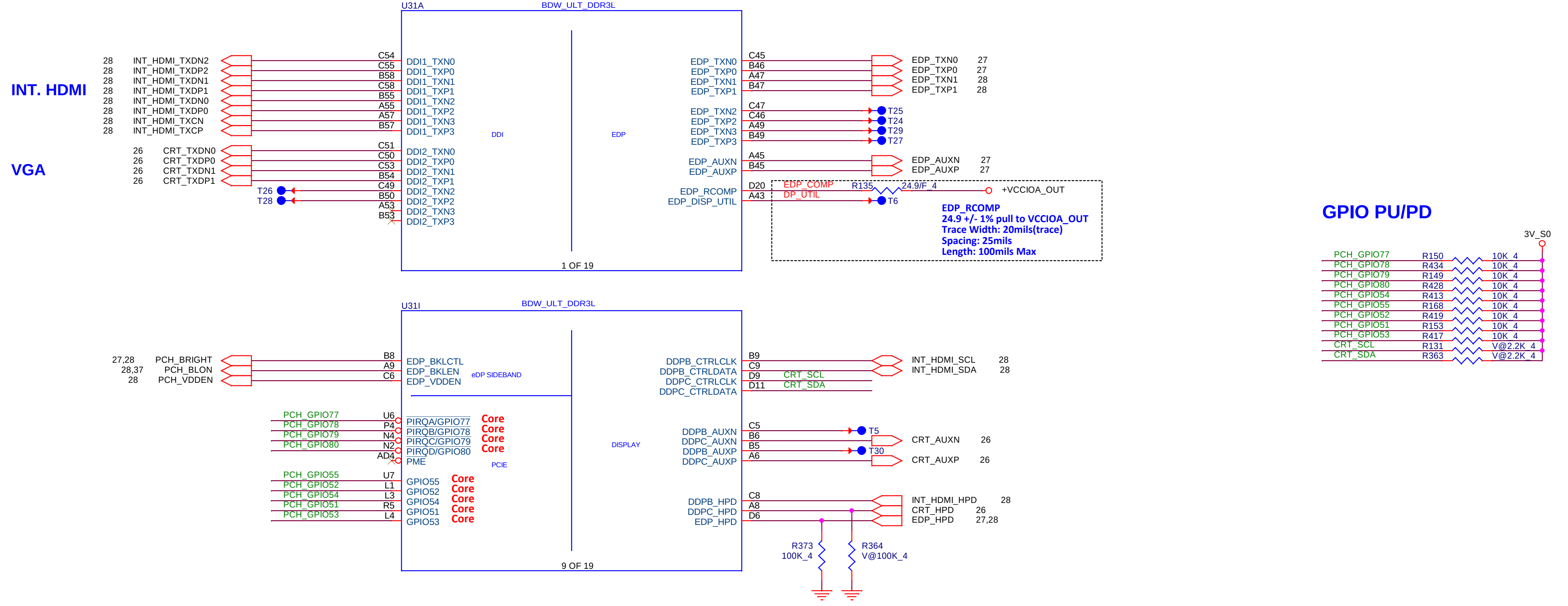
PROJECT ： FH9

Size | Document Number: SMBUS Address | Rev 2A

Date: Wednesday, November 19, 2014 | Sheet 5 of 48

Broadwell Type-U ULT (DISPLAY)

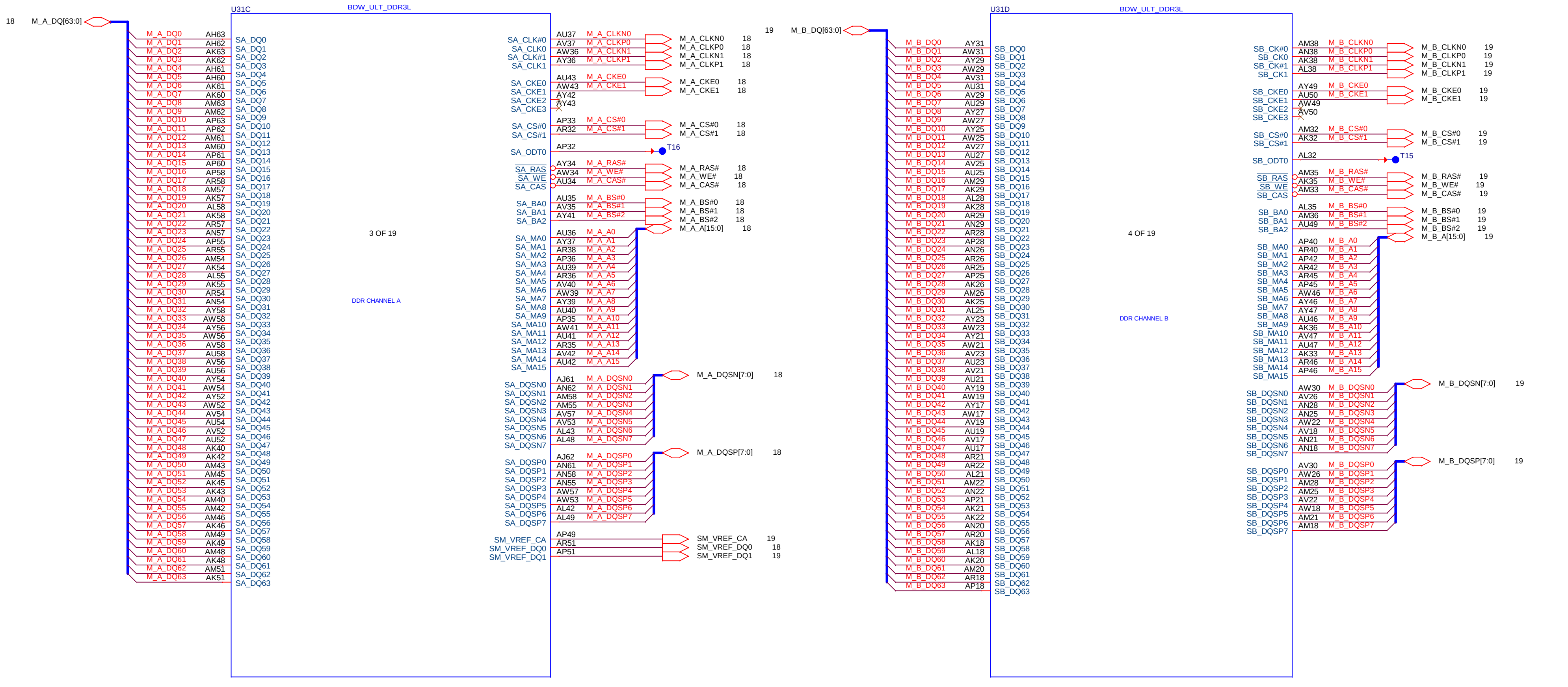


Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number: BDW MCP(DISPLAY/eDP)	Rev 2A
Date: Wednesday, November 19, 2014	Sheet 6 of 48	

07

Boardwell Type-U ULT (DDR3L CHA)

Boardwell Type-U ULT (DDR3L CHB)



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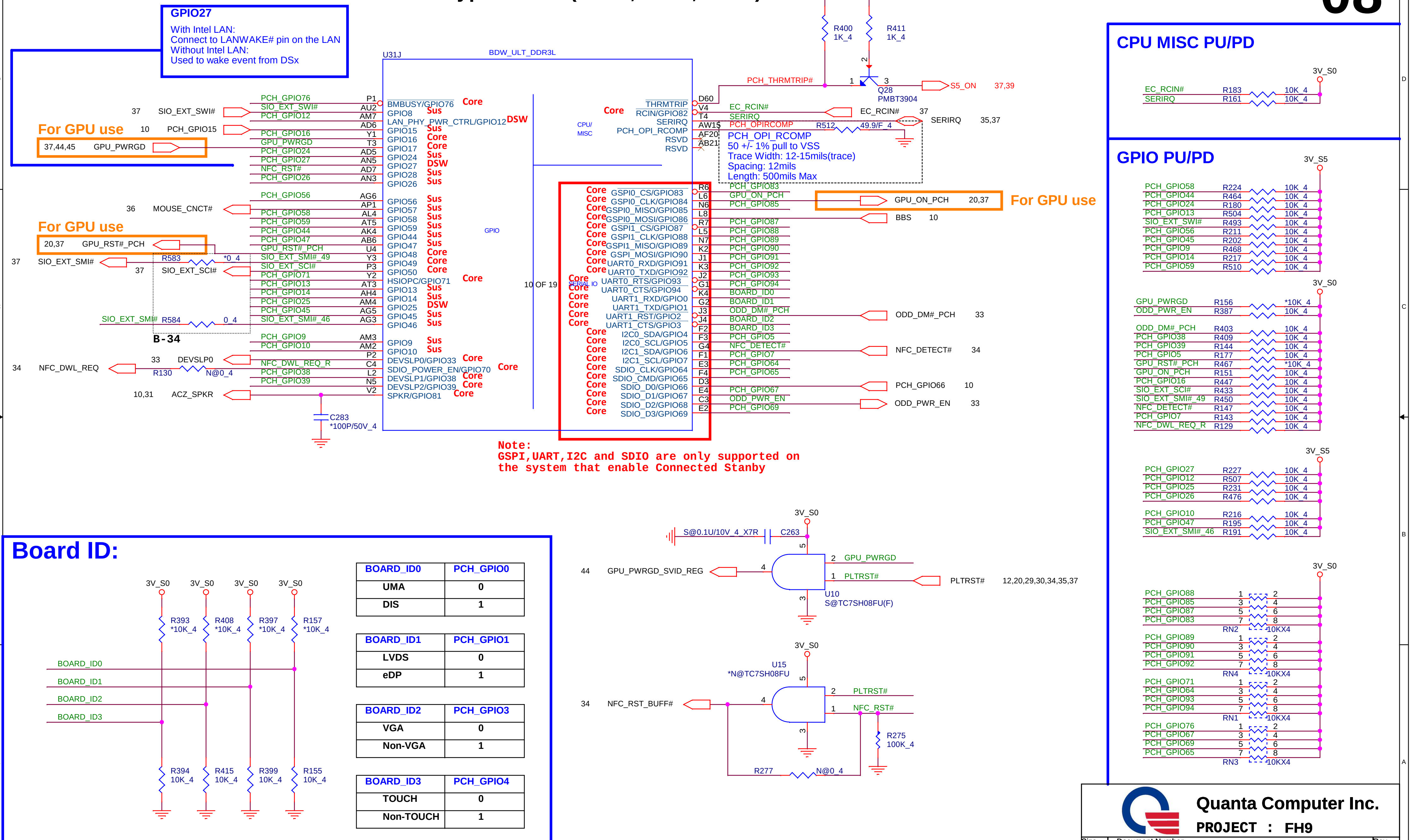
PROJECT : FH9		
Size	Document Number: BDW MCP(LPDDR3)	Rev 2A
Date: Wednesday, November 19, 2014	Sheet 7 of 48	

Broadwell Type-U ULT(GPIO,LPIO,MISC)

08



BOARD_ID0	PCH_GPIO0
UMA	0
DIS	1

BOARD_ID1	PCH_GPIO1
LVDS	0
eDP	1

BOARD_ID2	PCH_GPIO3
VGA	0
Non-VGA	1

BOARD_ID3	PCH_GPIO4
TOUCH	0
Non-TOUCH	1

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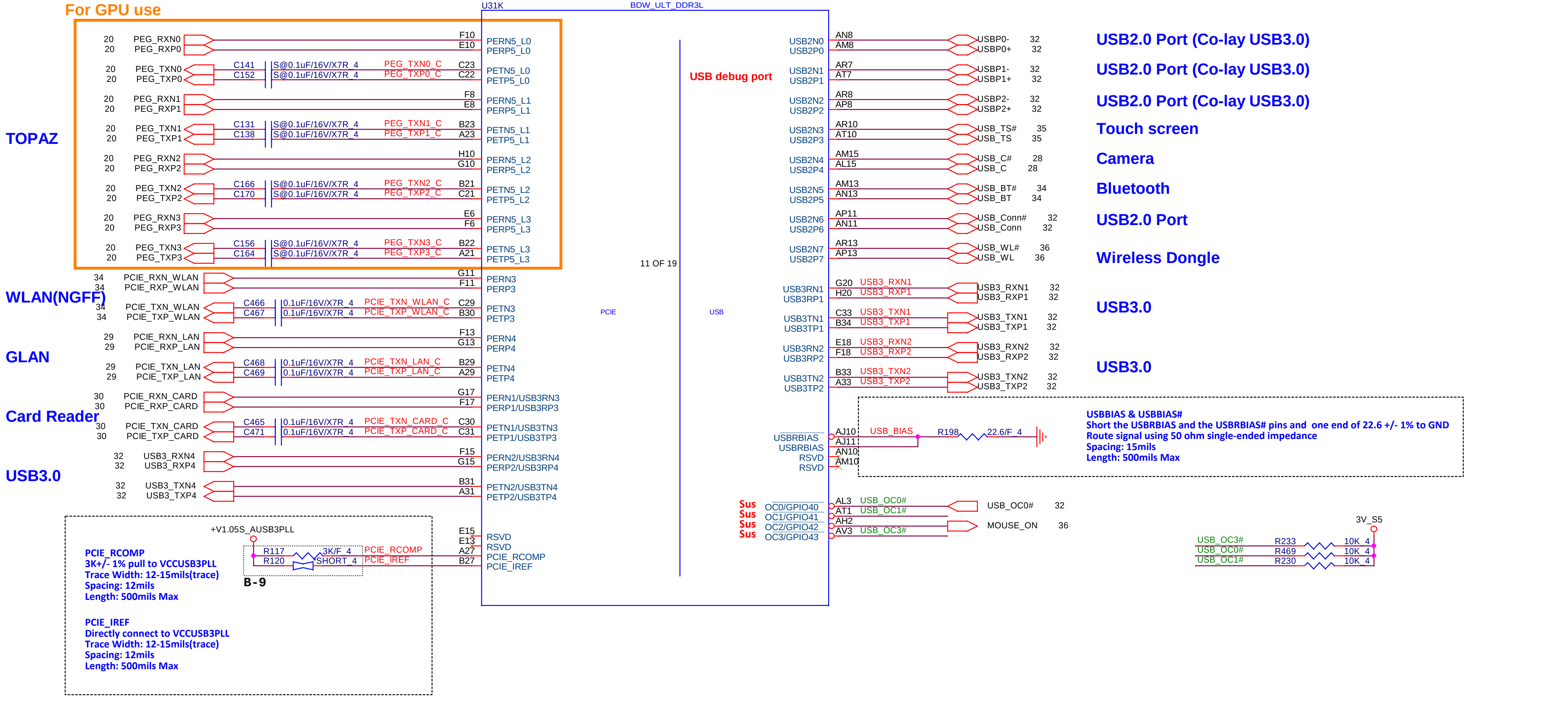
PROJECT : FH9

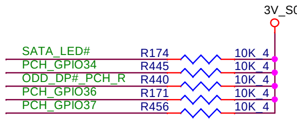
Size | Document Number: BDW PCH(GPIO/LPIO/MISC) | Rev 2A

Date: Wednesday, November 19, 2014 | Sheet 8 of 48

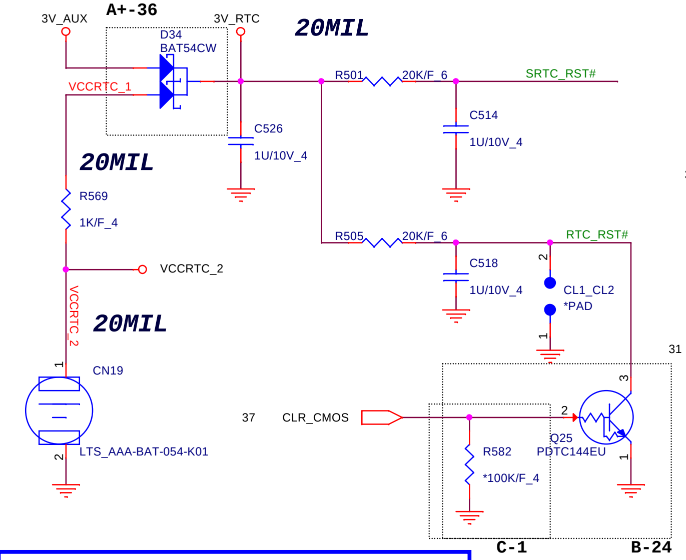
Broadwell Type-U ULT (PCIE,USB)



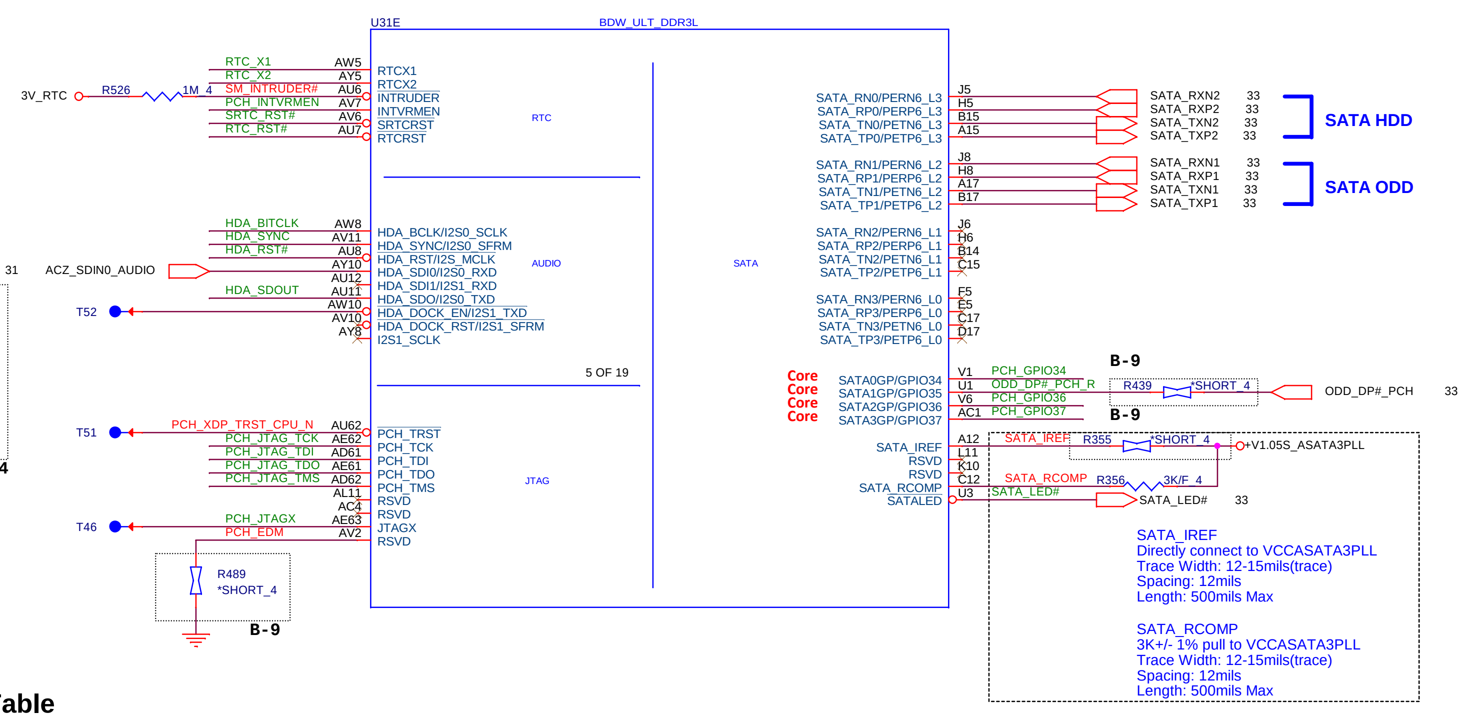
Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number: BDW PCH(PCIE/USB)	Rev 2A
Date: Wednesday, November 19, 2014	Sheet 9 of 48	



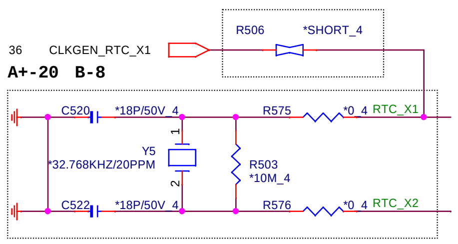
RTC Circuitry(RTC)



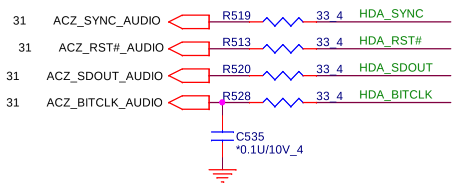
Broadwell Type-U ULT (RTC,HDA,JTAG,SATA)



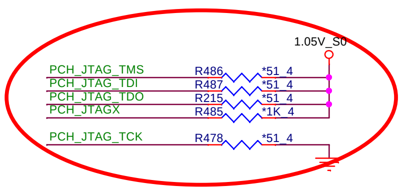
RTC XTAL 32.768KHz



HDA Audio (CLG)

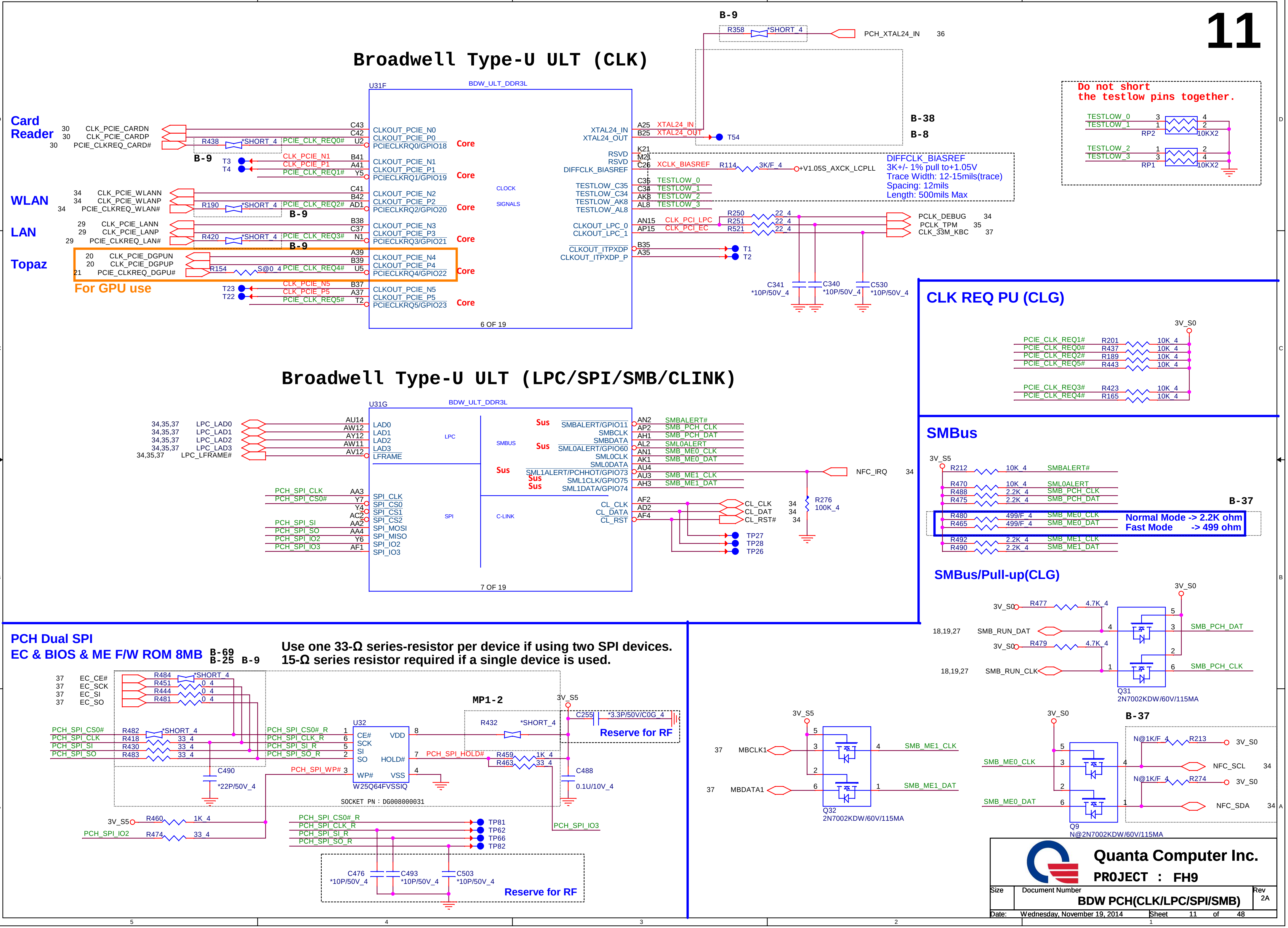


PCH JTAG Debug (CLG)



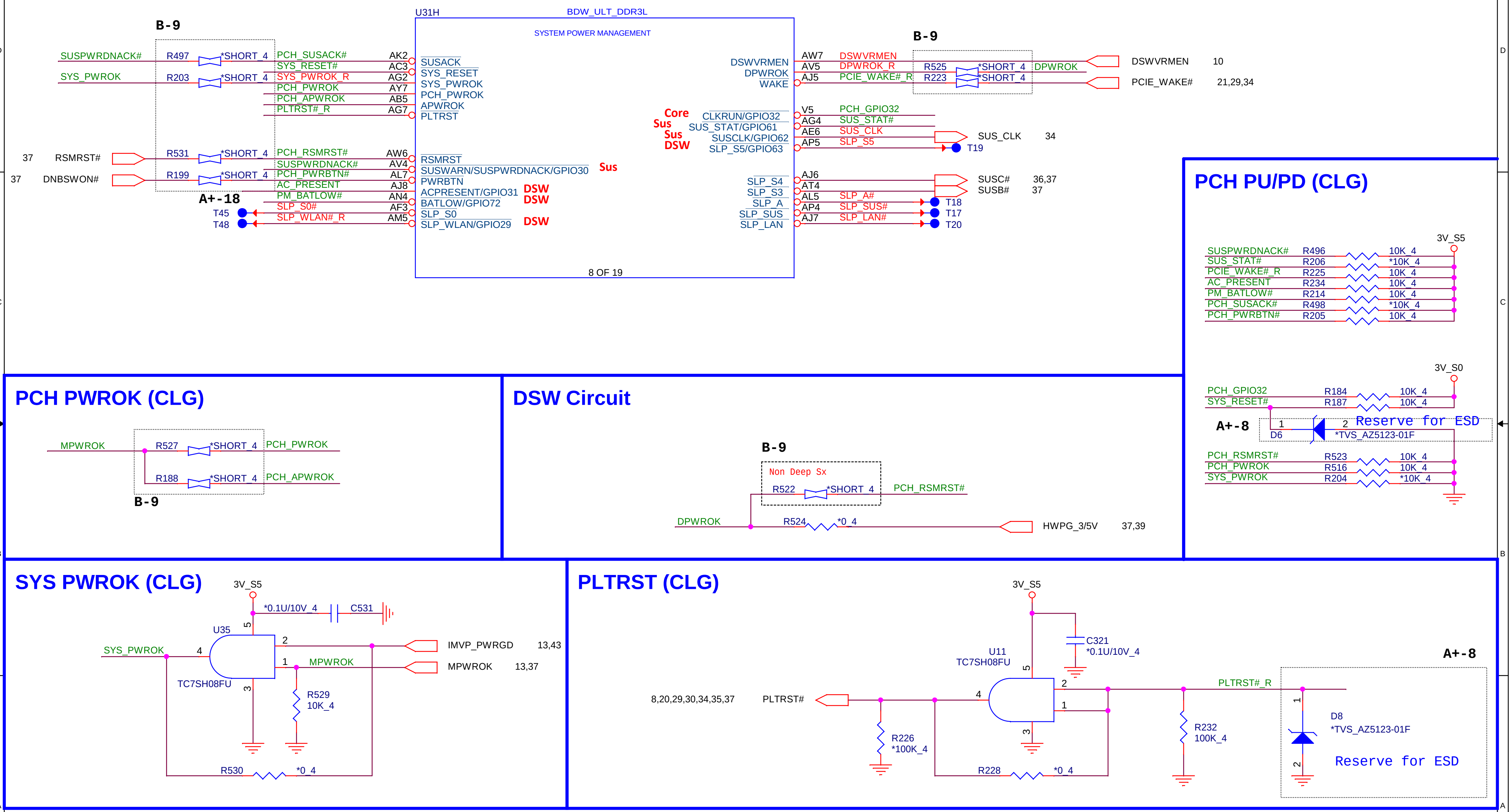
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Schematic
HDA_SDO/I2S0_TXD	Flash Descriptor Security Override	PWROK	0 = Enable Flash Descriptor security. (Int PD) 1 = Disable Flash Descriptor Security	3V_S5 R518 *1K_4 HDA_SDOUT HDA_SDOUT 37
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = DCPSUSx are powered from an ext. power source 1 = Integrated VRM enabled (330K PU VccRTC)	3V_RTC R515 330K_4 PCH_INTVRMEN R517 *330K_4
DSWVRMEN	DeepSx Well On-Die VRM Enable	ALWAYS	0 = Disable Integrated DSW On-Die VRM 1 = Enable Integrated DSW On-Die VRM (Must be PU)	3V_RTC R514 330K_4 DSWVRMEN 12
GPIO15	TLS Confidentiality	RSMRST#	0 = Disable Intel ME Crypto TLS cipher suite (Int PD) 1 = Enable Intel ME Crypto Transport	8 PCH_GPIO15 3V_S5 R197 8.2K_4 R200 *1K_4
SPKR/GPIO81	No reboot mode setting	PWROK	0 = Disable No Reboot mode (Int PD). 1 = Enable No Reboot mode.	3V_S0 R181 *1K_4 ACZ_SPKR 8,31
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit	PWROK	0 = Boot from SPI 1 = Boot from LPC	3V_S0 R392 *1K_4 R396 *1K_4 BBS 8
SDIO_D0/GPIO66	Top Swap Override	PWROK	0 = Disable Top Swap mode. (Int PD) 1 = Enable Top Swap mode.	+V3.3S_1.8S_LPSS_SDIO R391 *1K_4 R389 1K_4 PCH_GPIO66 8



11
Broadwell Type-U ULT (CLK)
U31F
BDW_ULT_DDR3L
Card Reader
CLK_PCIE_CARDN
CLK_PCIE_CARDP
PCIE_CLKREQ_CARD#
R438 *SHORT_4 PCIE_CLK_REQ0#
B-9
CLK_PCIE_N1
CLK_PCIE_P1
PCIE_CLK_REQ1#
WLAN
CLK_PCIE_WLANN
CLK_PCIE_WLANP
PCIE_CLKREQ_WLAN#
R190 *SHORT_4 PCIE_CLK_REQ2#
LAN
CLK_PCIE_LANN
CLK_PCIE_LANP
PCIE_CLKREQ_LAN#
R420 *SHORT_4 PCIE_CLK_REQ3#
Topaz
CLK_PCIE_DGPUN
CLK_PCIE_DGPUP
PCIE_CLKREQ_DGPU#
R154 S@0_4 PCIE_CLK_REQ4#
For GPU use
CLK_PCIE_N5
CLK_PCIE_P5
PCIE_CLK_REQ5#
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0/GPIO18
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1/GPIO19
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2/GPIO20
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3/GPIO21
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4/GPIO22
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5/GPIO23
Core
CLOCK SIGNALS
XTAL24_IN
XTAL24_OUT
RSVD
RSVD
DIFFCLK_BIASREF
TESTLOW_C35
TESTLOW_C34
TESTLOW_AK8
TESTLOW_AL8
CLKOUT_LPC_0
CLKOUT_LPC_1
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
6 OF 19
B-9
R358 *SHORT_4
PCH_XTAL24_IN 36
B-38
B-8
T54
XCLK_BIASREF R114 3K/F_4 +V1.05S_AXCK_LCPLL
DIFFCLK_BIASREF
3K+/- 1% pull to+1.05V
Trace Width: 12-15mils(trace)
Spacing: 12mils
Length: 500mils Max
TESTLOW_0
TESTLOW_1
TESTLOW_2
TESTLOW_3
CLK_PCI_LPC
CLK_PCI_EC
R250 22_4
R251 22_4
R521 22_4
PCLK_DEBUG 34
PCLK_TPM 35
CLK_33M_KBC 37
C341 *10P/50V_4
C340 *10P/50V_4
C530 *10P/50V_4
Do not short the testlow pins together.
RP2 10KX2
RP1 10KX2
CLK REQ PU (CLG)
3V_S0
PCIE_CLK_REQ1# R201 10K_4
PCIE_CLK_REQ0# R437 10K_4
PCIE_CLK_REQ2# R189 10K_4
PCIE_CLK_REQ5# R443 10K_4
PCIE_CLK_REQ3# R423 10K_4
PCIE_CLK_REQ4# R165 10K_4
Broadwell Type-U ULT (LPC/SPI/SMB/CLINK)
U31G
BDW_ULT_DDR3L
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME#
LAD0
LAD1
LAD2
LAD3
LFRAME
LPC
SMBUS
SPI
C-LINK
Sus
SMBALERT/GPIO11
SMBCLK
SMBDATA
SML0ALERT/GPIO60
SML0CLK
SML0DATA
SML1ALERT/PCHHOT/GPIO73
SML1CLK/GPIO75
SML1DATA/GPIO74
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT
SML0ALERT
SMB_ME0_CLK
SMB_ME0_DAT
SMB_ME1_CLK
SMB_ME1_DAT
NFC_IRQ 34
R276 100K_4
PCH_SPI_CLK
PCH_SPI_CS0#
PCH_SPI_SI
PCH_SPI_SO
PCH_SPI_IO2
PCH_SPI_IO3
SPI_CLK
SPI_CS0
SPI_CS1
SPI_CS2
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
CL_CLK
CL_DATA
CL_RST
CL_CLK 34
CL_DAT 34
CL_RST# 34
TP27
TP28
TP26
7 OF 19
SMBus
3V_S5
R212 10K_4 SMBALERT#
R470 10K_4 SML0ALERT
R488 2.2K_4 SMB_PCH_CLK
R475 2.2K_4 SMB_PCH_DAT
R480 499/F_4 SMB_ME0_CLK
R465 499/F_4 SMB_ME0_DAT
Normal Mode -> 2.2K ohm
Fast Mode -> 499 ohm
B-37
R492 2.2K_4 SMB_ME1_CLK
R490 2.2K_4 SMB_ME1_DAT
SMBus/Pull-up(CLG)
3V_S0
R477 4.7K_4
SMB_RUN_DAT
R479 4.7K_4
SMB_RUN_CLK
SMB_PCH_DAT
SMB_PCH_CLK
Q31
2N7002KDW/60V/115MA
PCH Dual SPI
EC & BIOS & ME F/W ROM 8MB
B-69
B-25
B-9
Use one 33-Ω series-resistor per device if using two SPI devices.
15-Ω series resistor required if a single device is used.
EC_CE#
EC_SCK
EC_SI
EC_SO
R484 *SHORT_4
R451 0_4
R444 0_4
R481 0_4
R482 *SHORT_4
R418 33_4
R430 33_4
R483 33_4
C490 *22P/50V_4
PCH_SPI_CS0#_R
PCH_SPI_CLK_R
PCH_SPI_SI_R
PCH_SPI_SO_R
U32
CE#
SCK
SI
SO
WP#
VDD
HOLD#
VSS
W25Q64FVSSIQ
SOCKET PN：DG008000031
MP1-2
R432 *SHORT_4
PCH_SPI_HOLD#
R459 1K_4
R463 33_4
PCH_SPI_WP#
C255 *3.3P/50V/C0G_4
Reserve for RF
C488 0.1U/10V_4
R460 1K_4
R474 33_4
TP81
TP62
TP66
TP82
C476 *10P/50V_4
C493 *10P/50V_4
C503 *10P/50V_4
Reserve for RF
MBCLK1
MBDATA1
SMB_ME1_CLK
SMB_ME1_DAT
Q32
2N7002KDW/60V/115MA
B-37
SMB_ME0_CLK
SMB_ME0_DAT
N@1K/F_4 R213
N@1K/F_4 R274
NFC_SCL 34
NFC_SDA 34
Q9
N@2N7002KDW/60V/115MA
Quanta Computer Inc.
PROJECT : FH9
Size
Document Number
BDW PCH(CLK/LPC/SPI/SMB)
Rev
2A
Date: Wednesday, November 19, 2014
Sheet 11 of 48

Broadwell U-Type ULT (SYSTEM POWER MANAGEMENT)



Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	BDW PCH(PWR MANAGEMENT)	2A
Date: Wednesday, November 19, 2014	Sheet 12 of 48	

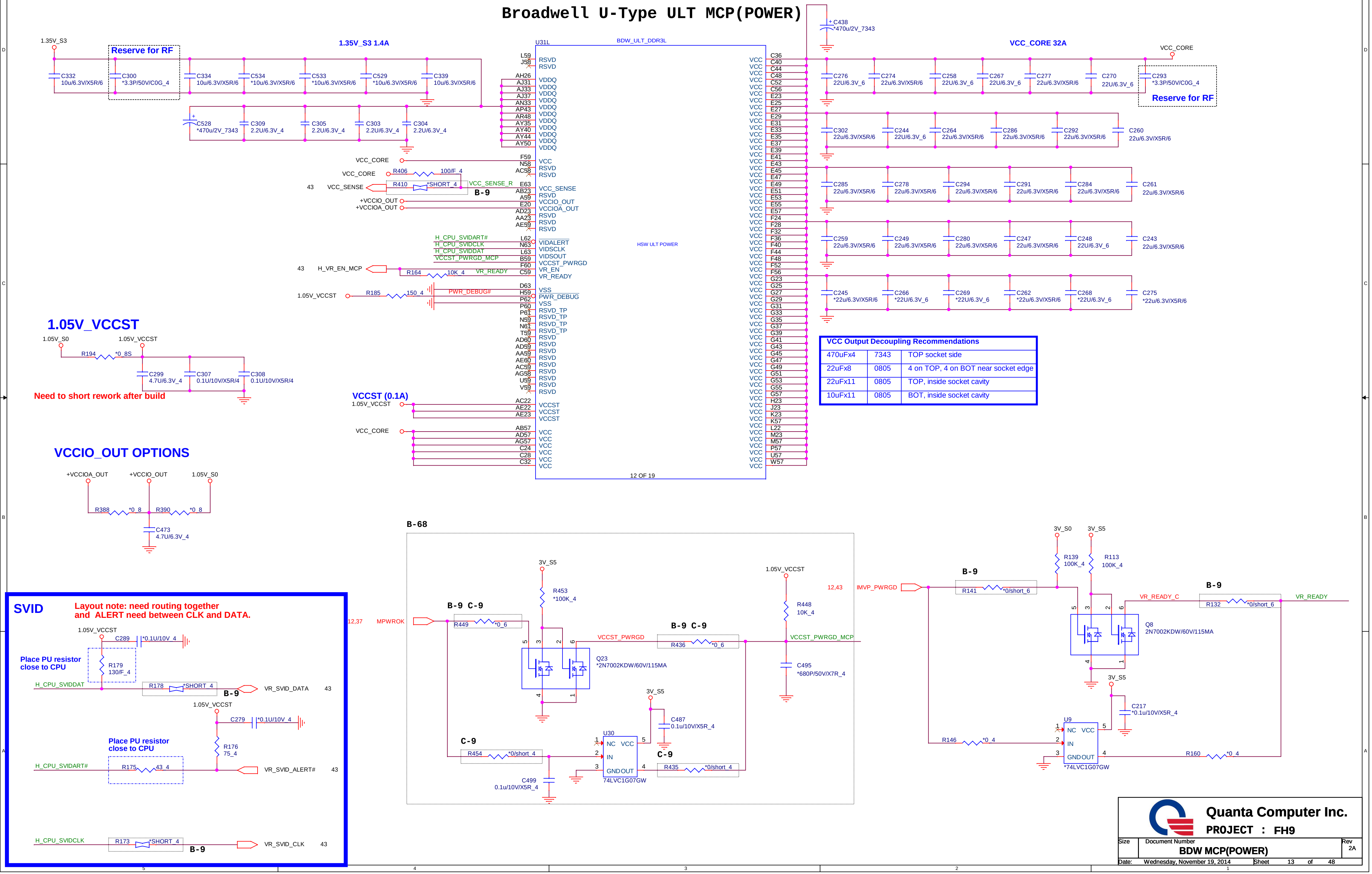
Broadwell U-Type ULT MCP(POWER)

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity



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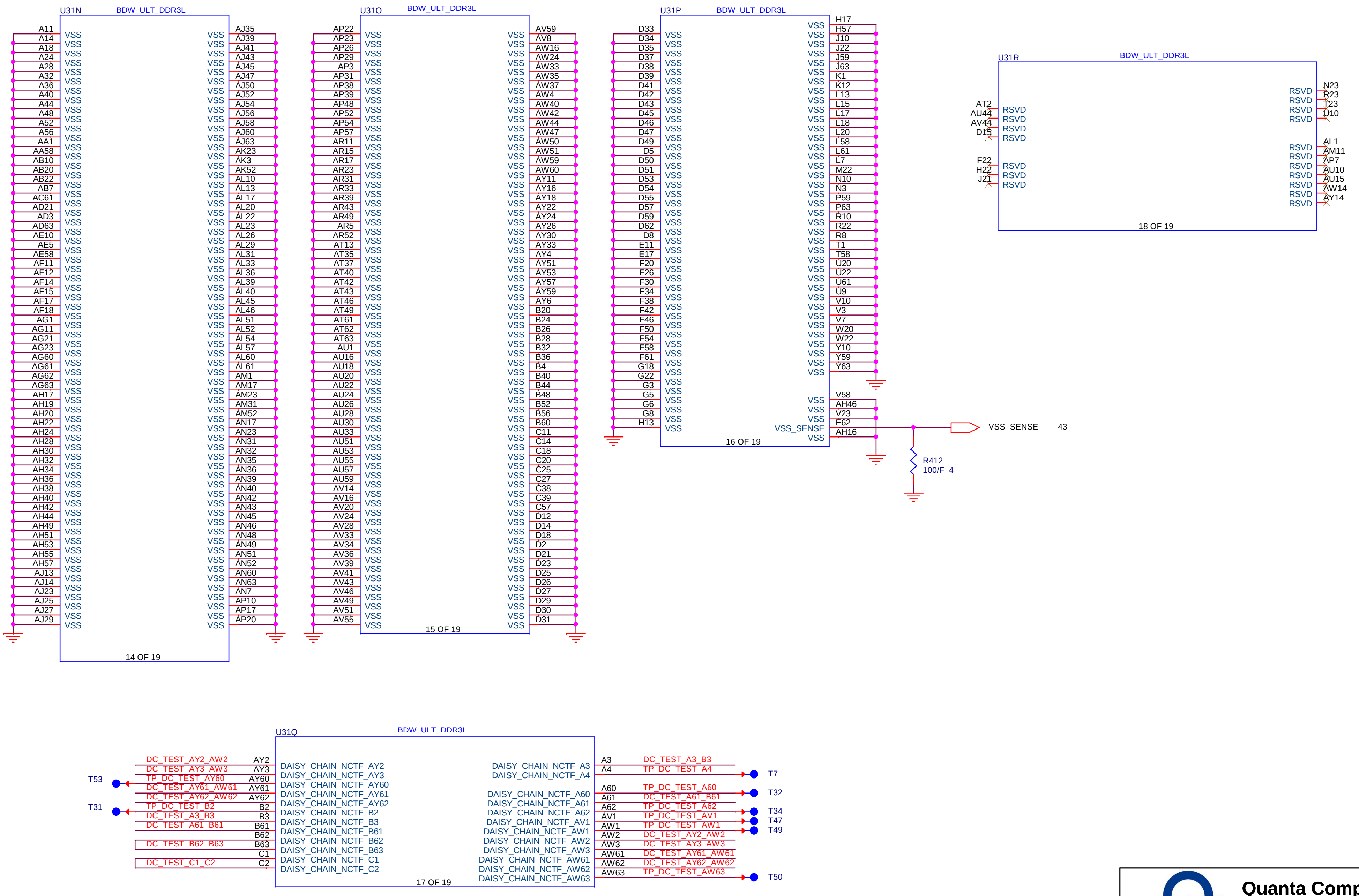
PROJECT : FH9

Size	Document Number	Rev
	BDW MCP(POWER)	2A

Date: Wednesday, November 19, 2014 Sheet 13 of 48

Broadwell U-Type ULT (RSVD,GND)



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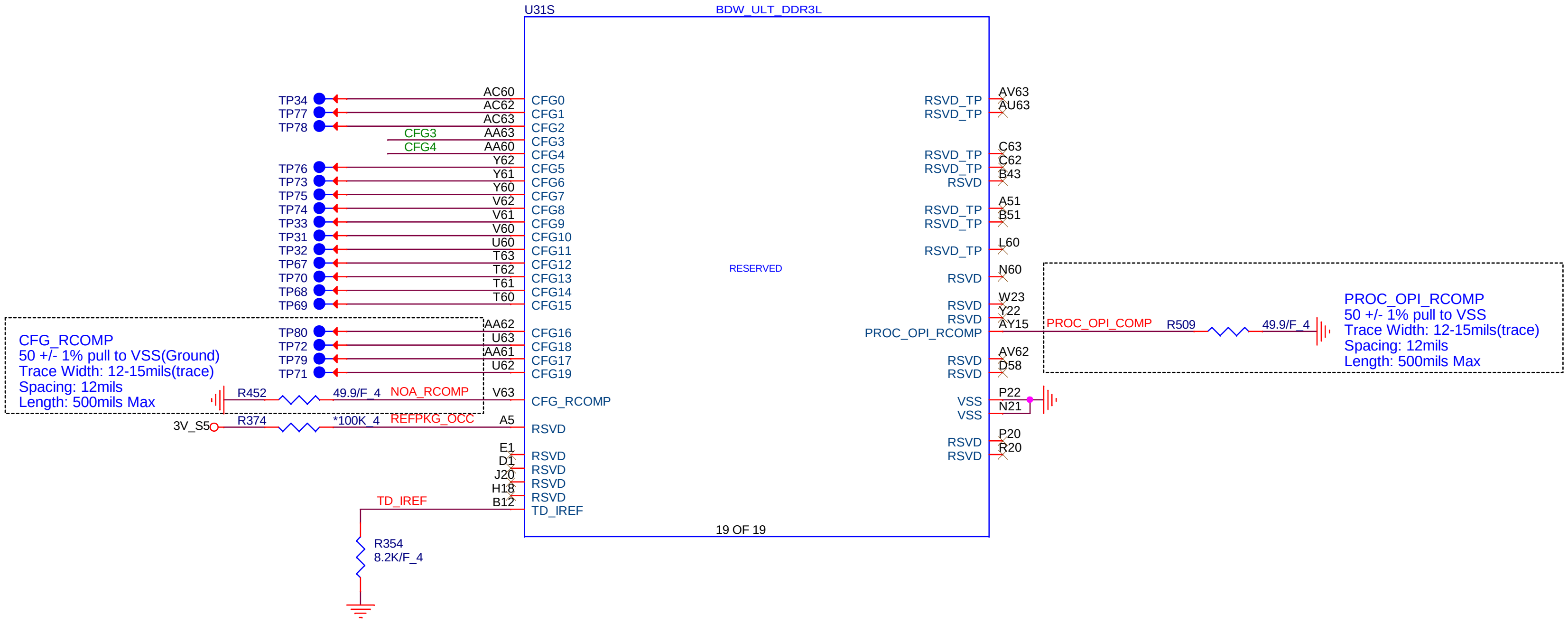
PROJECT : FH9

Size	Document Number	Rev
	BDW MCP(GND/DAISY/RSVD)	2A
Date: Wednesday, November 19, 2014	Sheet 14 of 48	

Broadwell U-Type ULT PCH (CFG)



Processor Strapping

	1	0	
CFG3 **MSR Privacy Bit Feature**	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R471 *1K_4
CFG4 **eDP Enable**	DISABLED	ENABLED	CFG4 R210 1K_4

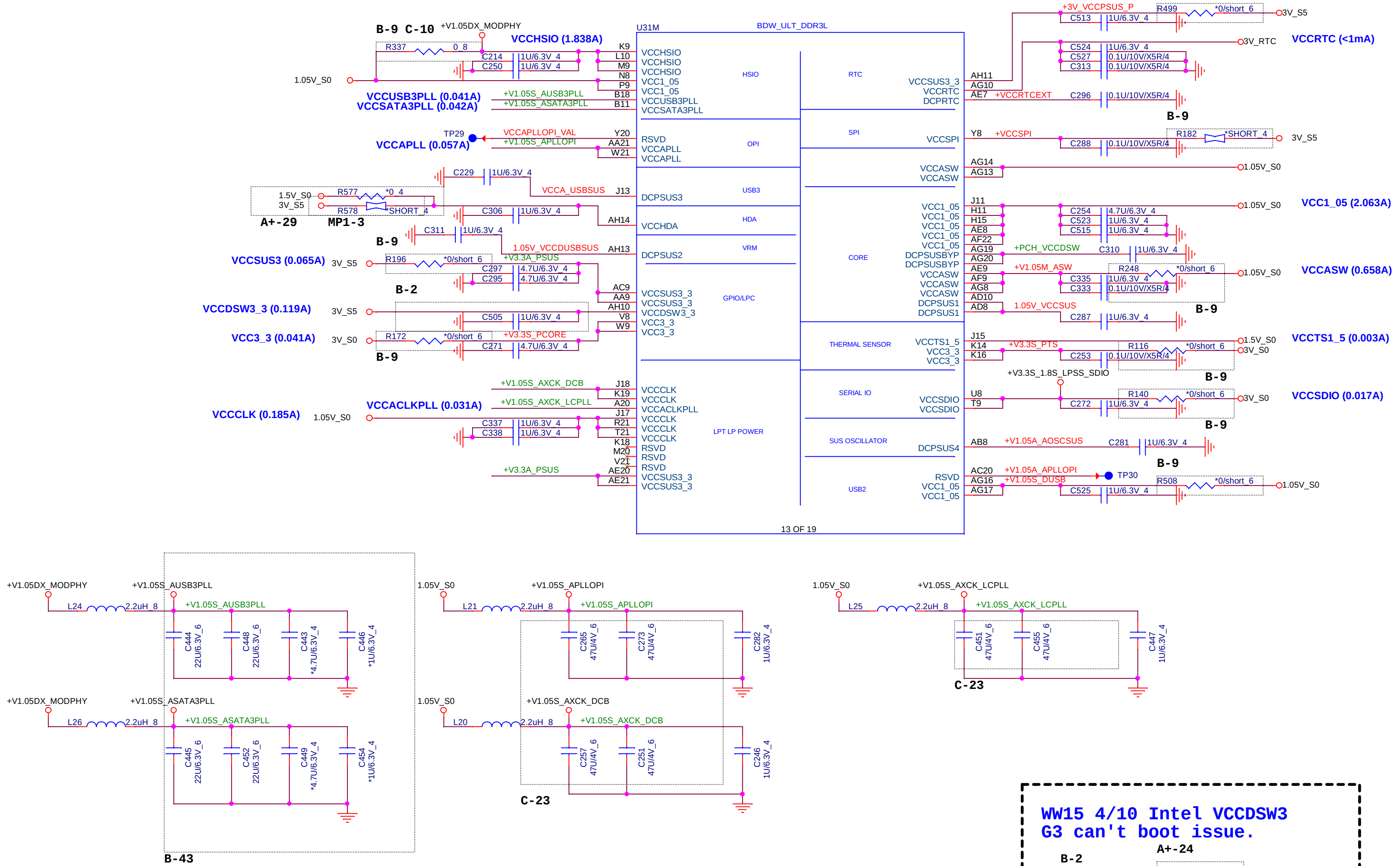
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	BDW MCP(CFG)	2A

Date: Wednesday, November 19, 2014 Sheet 15 of 48

Broadwell U-Type ULT PCH(POWER)



WW15 4/10 Intel VCCDSW3
G3 can't boot issue.

B-2 A+-24

3V_S5 — C312 1 2 *0.47u/6.3V_4 — +PCH_VCCDSW

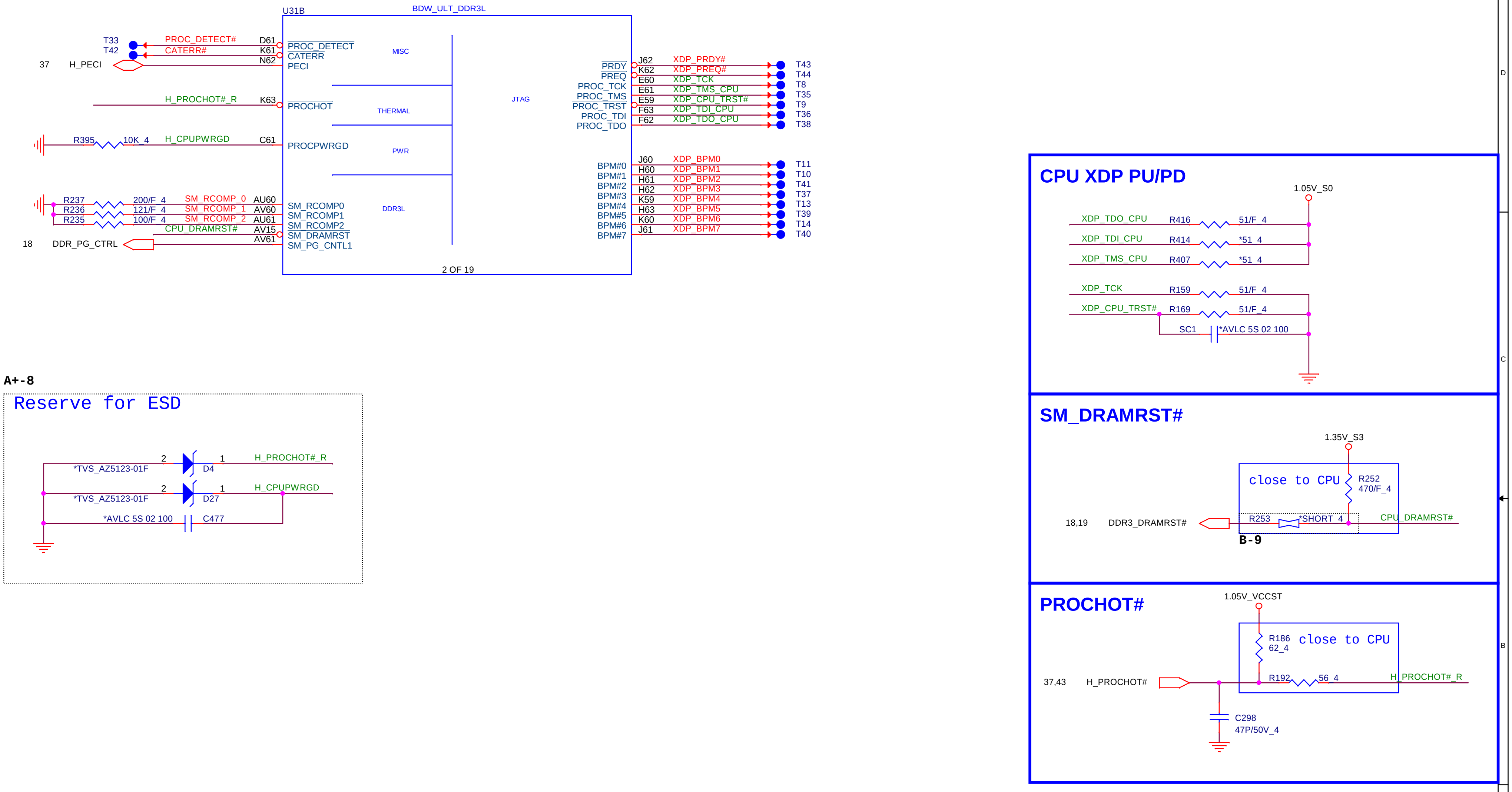
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	BDW PCH(POWER)	2A

Date: Wednesday, November 19, 2014 Sheet 16 of 48

Broadwell U-Type ULT MCP(SIDEBAND)



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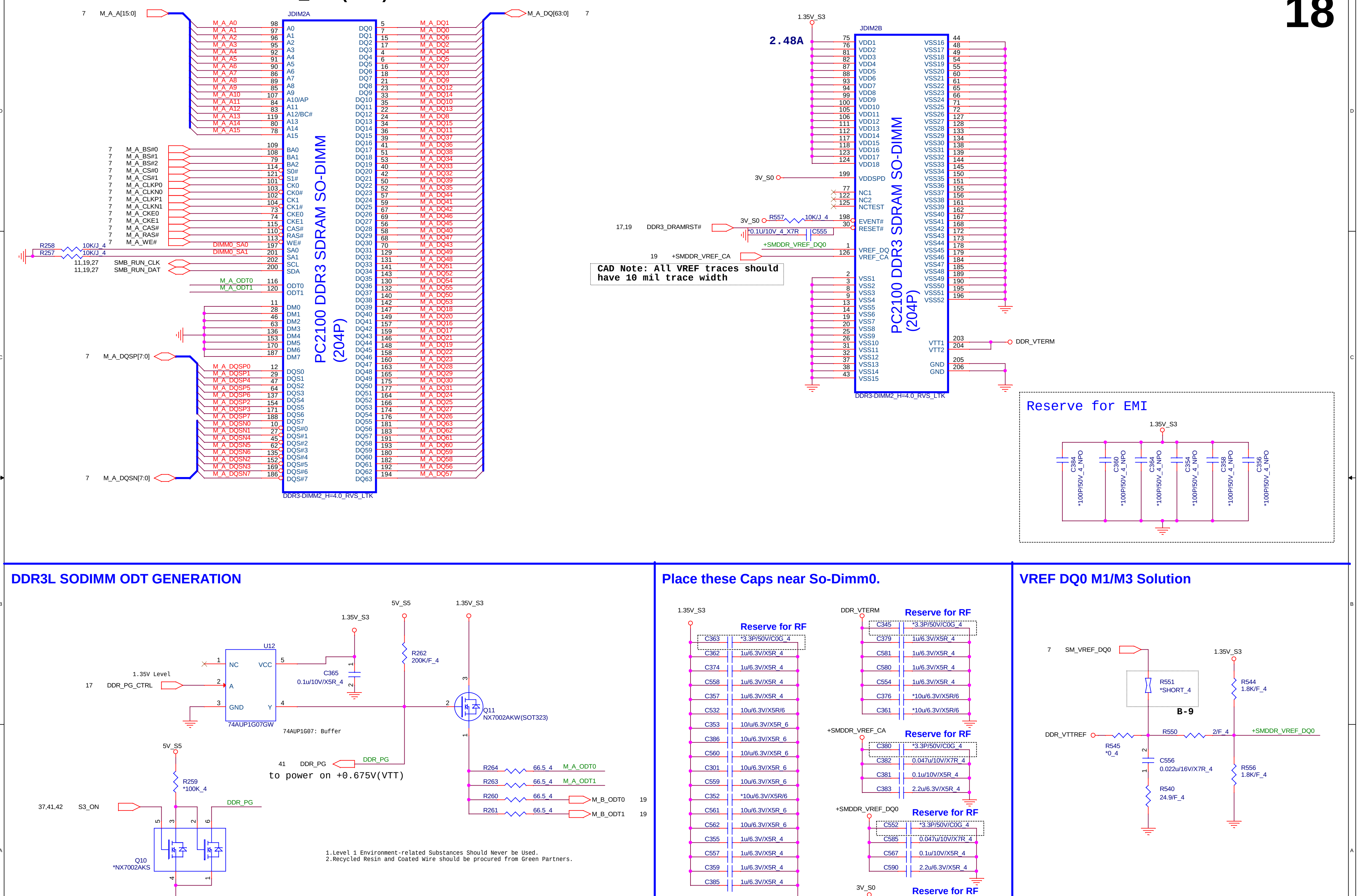
PROJECT : FH9

Size	Document Number	Rev
	BDW MCP(SIDEBAND)	2A
Date: Wednesday, November 19, 2014	Sheet 17 of 48	

DDR_RVS(DDR)



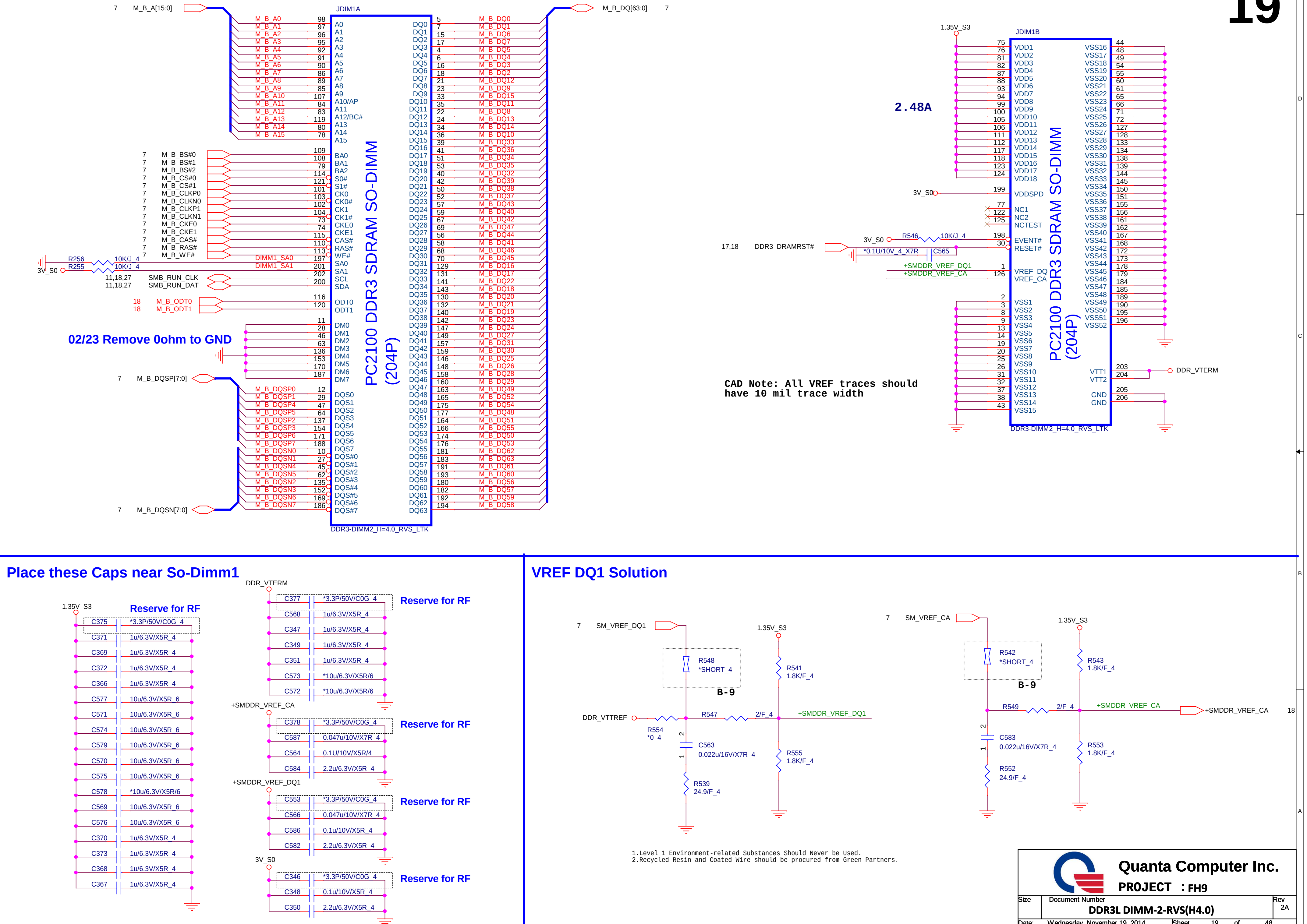
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	DDR3L DIMM-1-RVS(H4.0)	2A

Date: Thursday, November 20, 2014 Sheet 18 of 48

DDR_RVS(DDR)



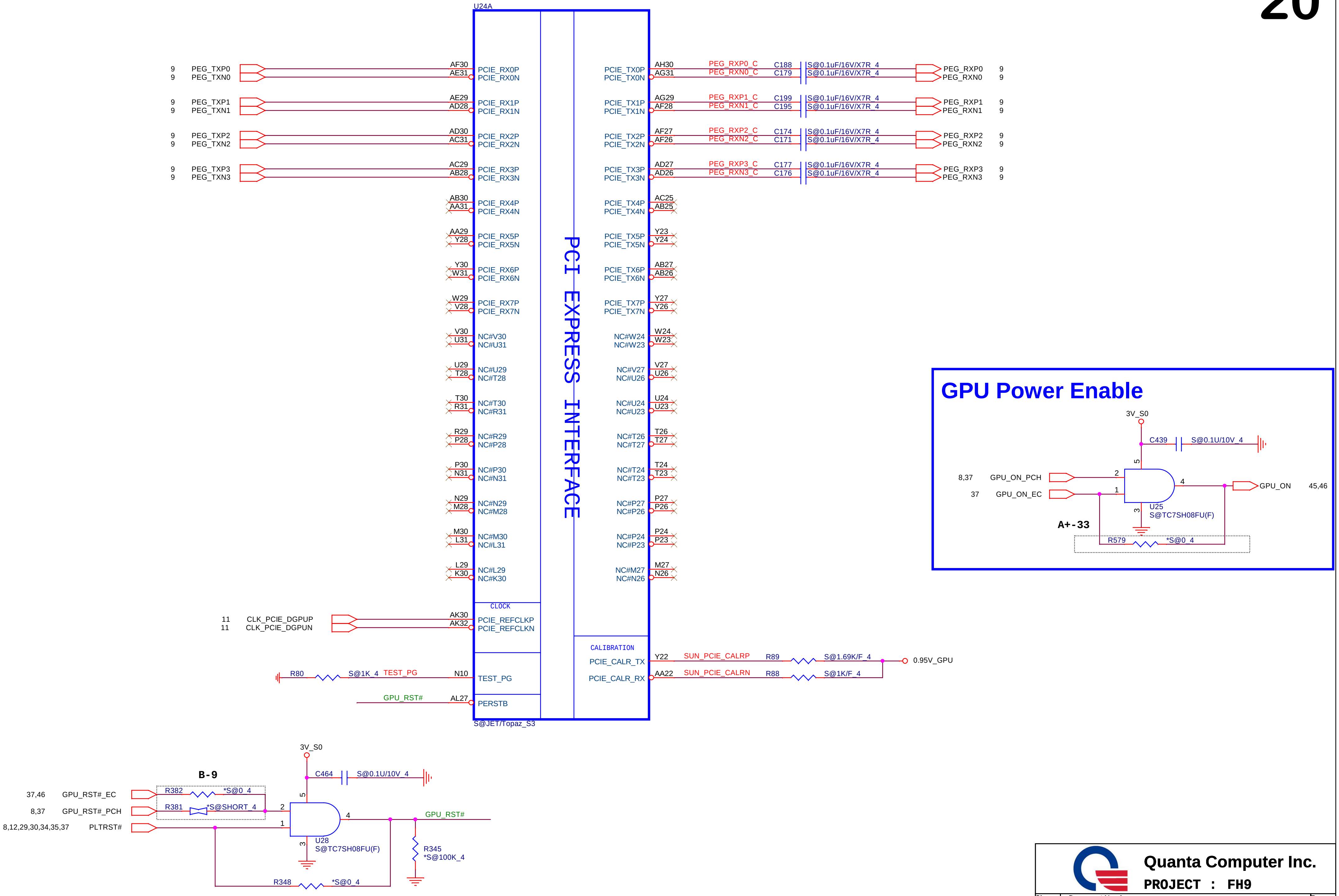
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	DDR3L DIMM-2-RVS(H4.0)	2A

Date: Wednesday, November 19, 2014 Sheet 19 of 48

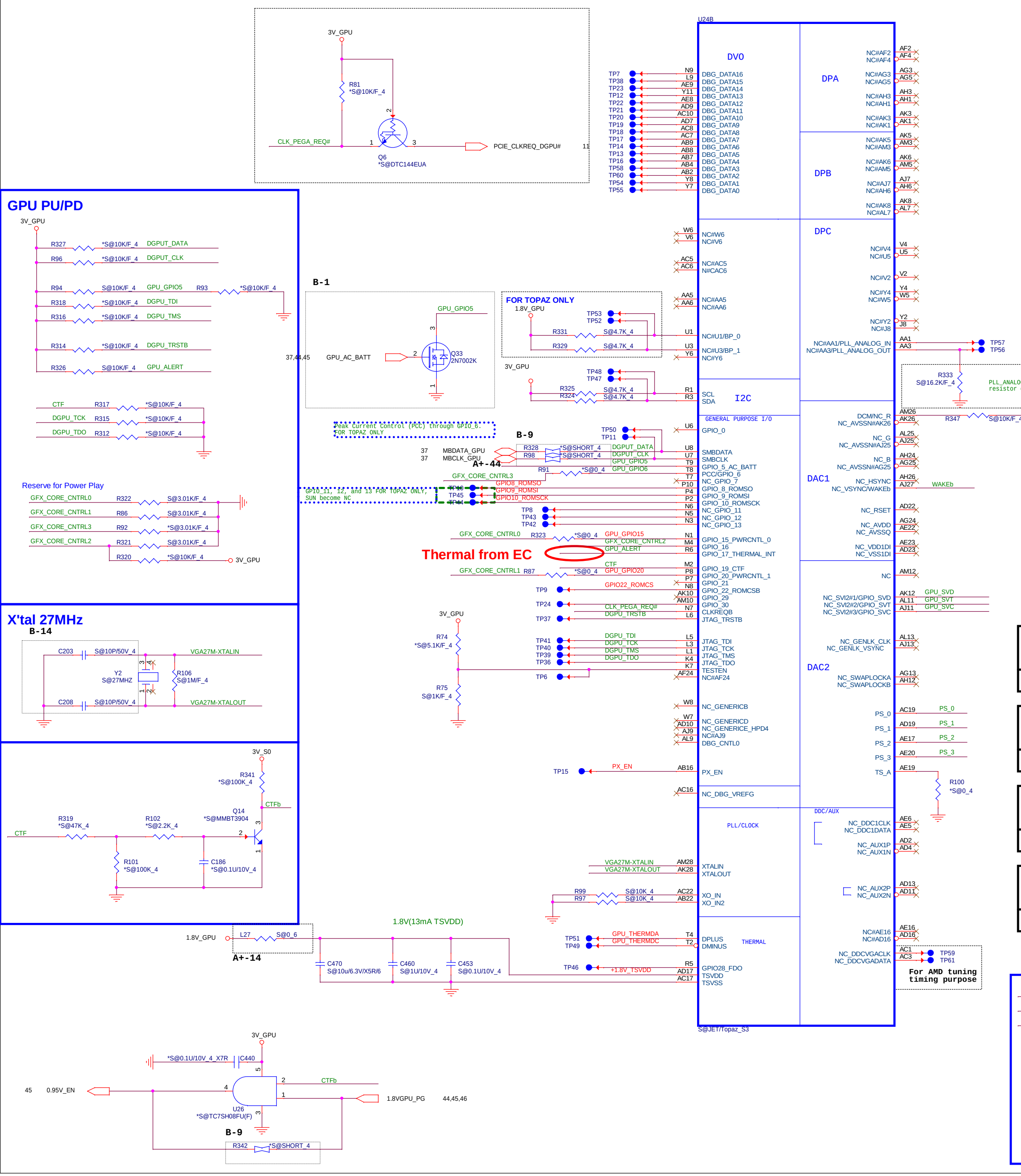


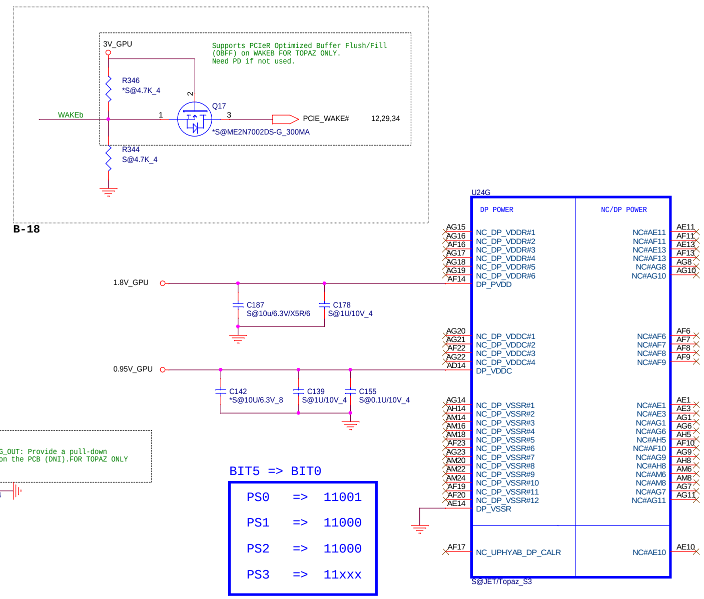
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	JET/TOPAZ S3 PCIE_Interface	2A

Date: Wednesday, November 19, 2014 Sheet 20 of 48





BIT5 => BIT0

PS0	=>	11001
PS1	=>	11000
PS2	=>	11000
PS3	=>	11xxx

PS_3[3:1]	Vendor	Type	Vendor P/N	Quanta P/N	R375	R376	C472
000	Hynix	256Mx16 *4	H5TC4G63AFR-11C	AKD5PGWTW20	NC	4.75K	NC
001	Samsung	256Mx16 *4	K4W4G1646D-BC11	AKD5PGST513	8.45K	2K	NC

A+-40

Table 3–21 Resistor Divider Lookup Table for Bits [3:

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

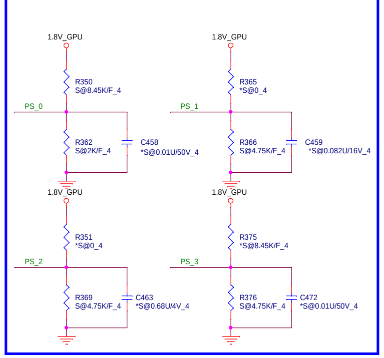
PS	R_pu	R_pd	C
PS	R350	R362	C458
PS_0	8.45K	2K	NC

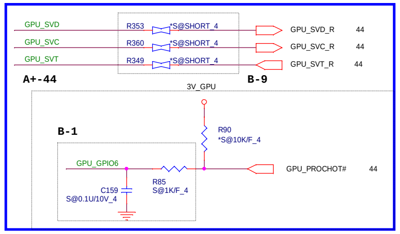
PS	R_pu	R_pd	C
PS	R365	R366	C459
PS_1	NC	4.75K	NC

PS	R_pu	R_pd	C
PS	R351	R369	C463
PS_2	NC	4.75K	NC

PS	R_pu	R_pd	C
PS	R375	R376	C472
PS_3	NC	4.75K	NC

MLPS Circuit

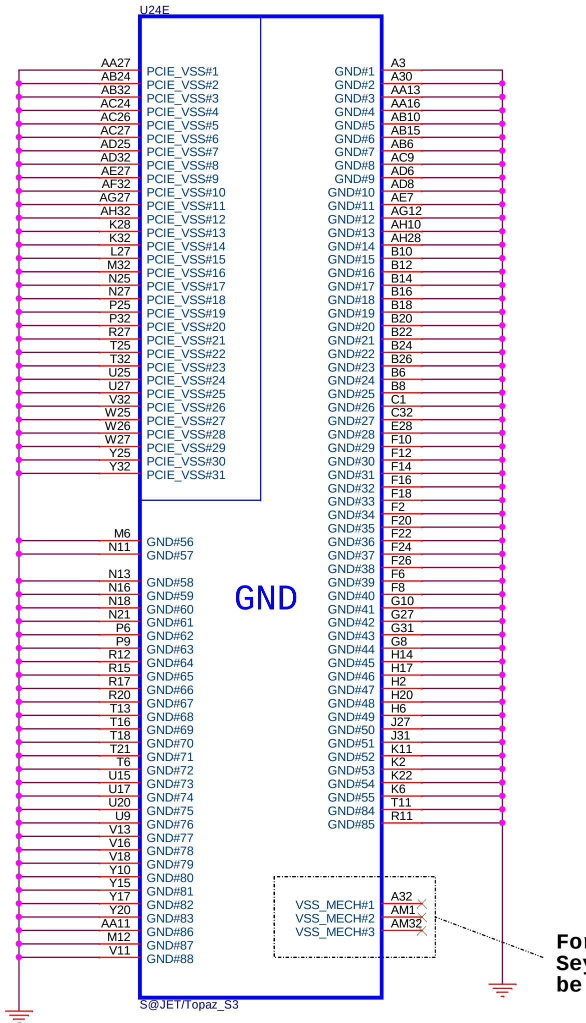


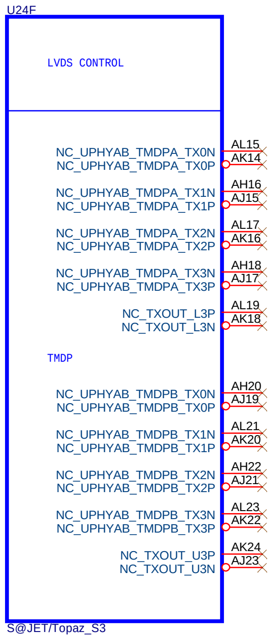


Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	JET/TOPAZ_S3_Main	2A
Date: Wednesday, November 19, 2014	Sheet 21 of 48	





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

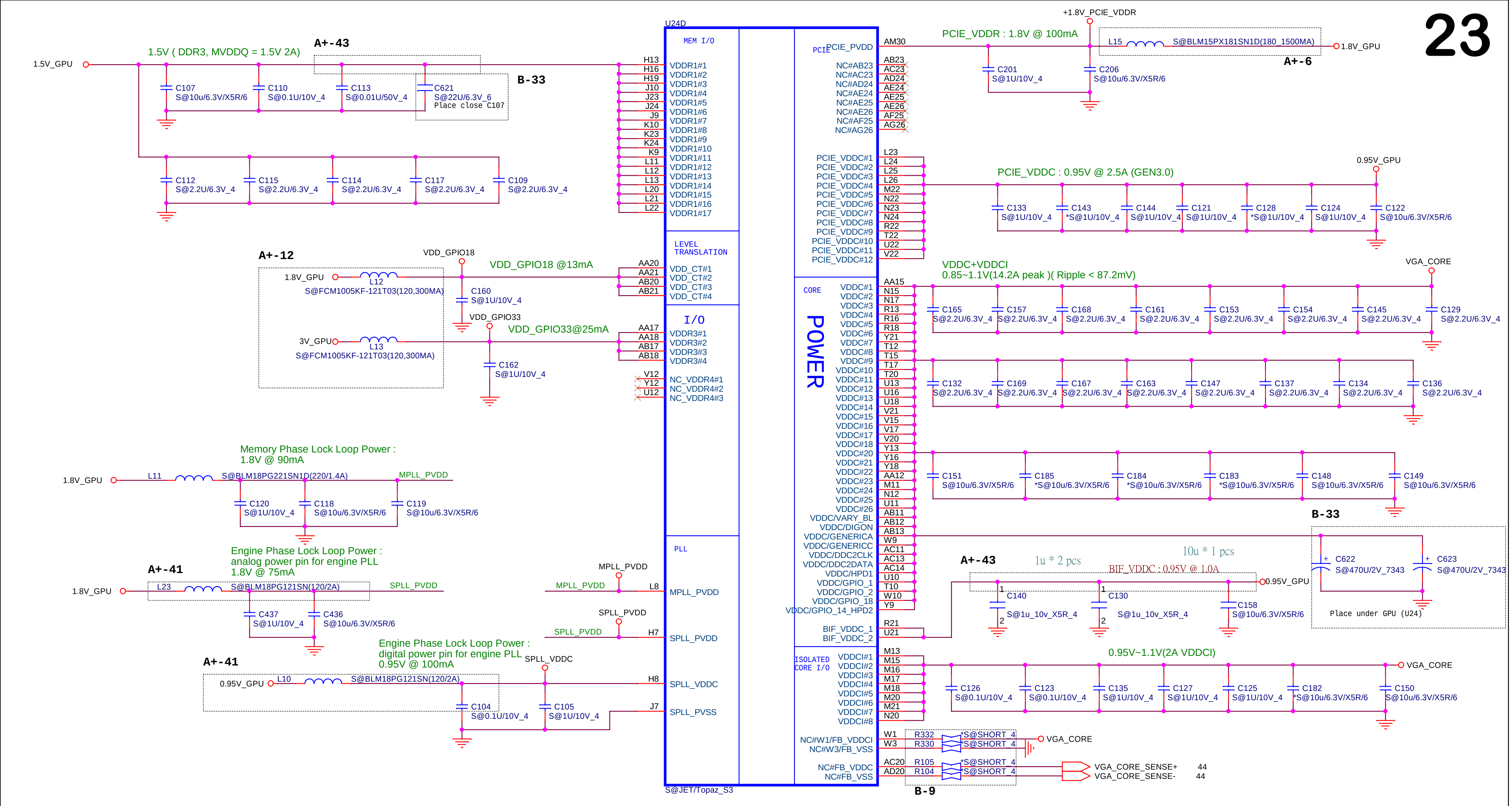
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

Memory Aperture size

GPIO_9 BIOSROM		GPIO_13 ROMIDCFG2	GPIO_12 ROMIDCFG1	GPIO_11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	Reserved	0	1	1
0	512M	Not Supported		
0	1G	Not Supported		
0	2G	Not Supported		
0	4G	Not Supported		

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



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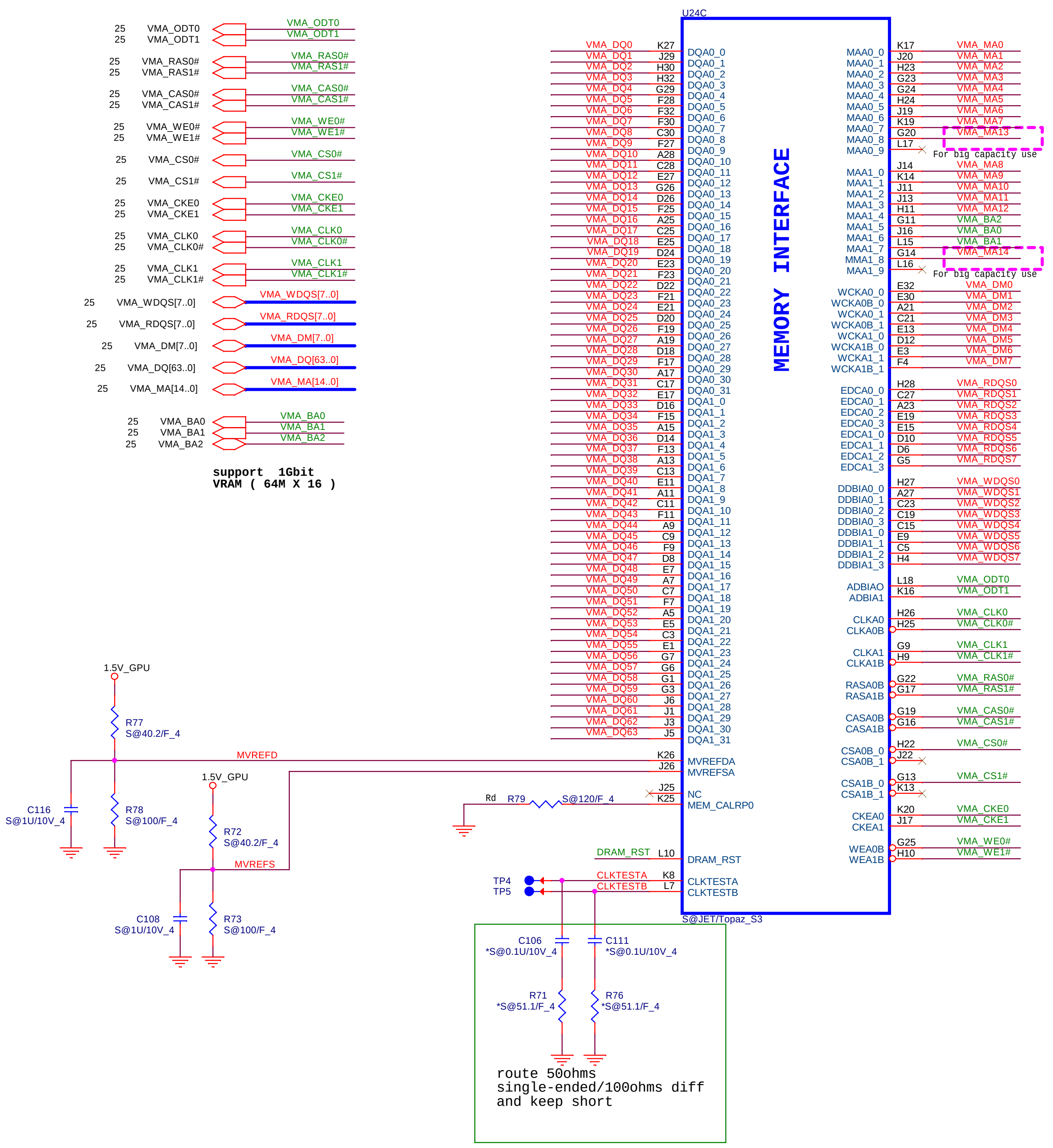
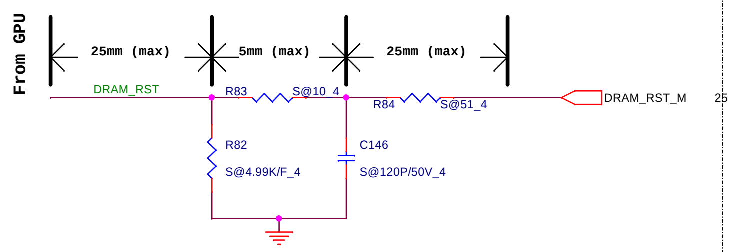
PROJECT : FH9

Size	Document Number	Rev
	JET/TOPAZ_S3_Power_and_NC	2A

Date: Wednesday, November 19, 2014 Sheet 23 of 48



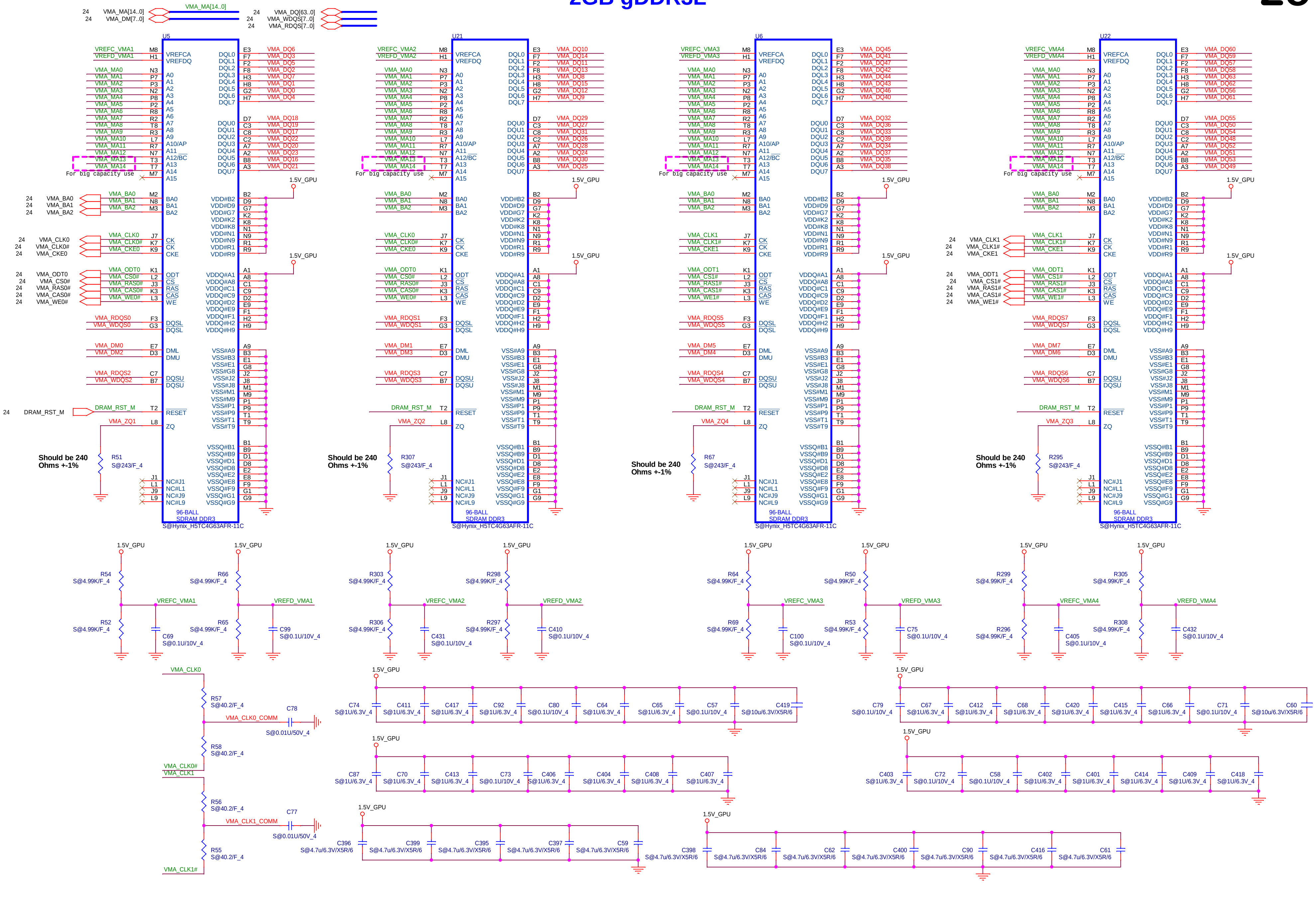


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

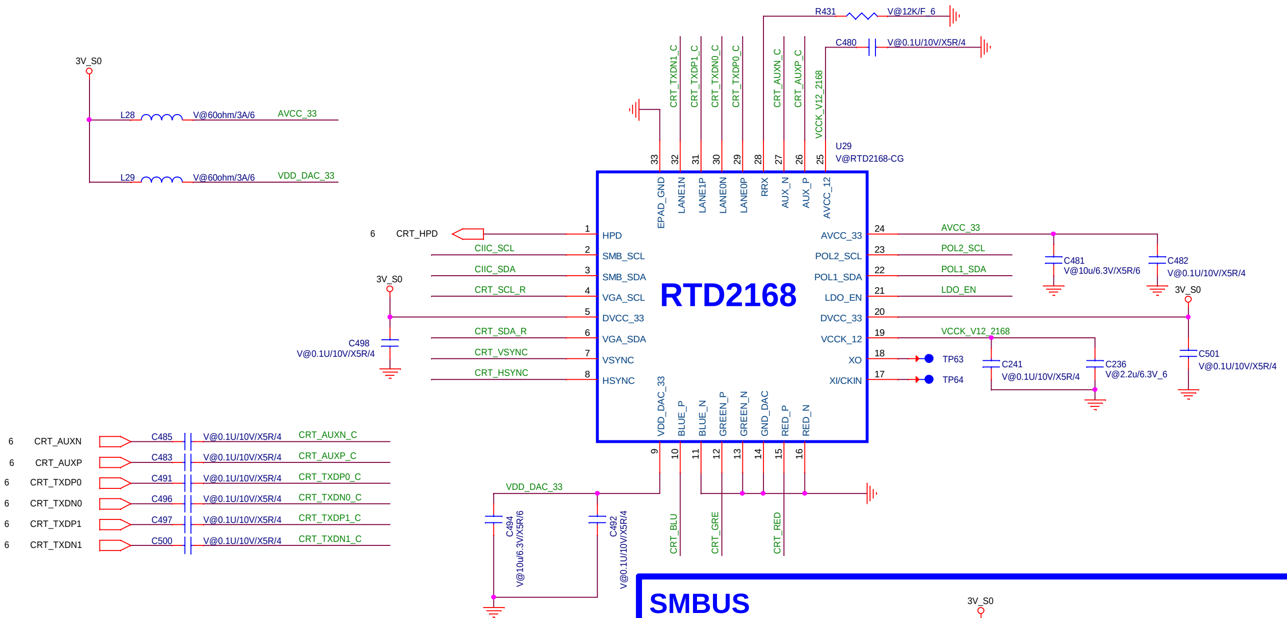
Quanta Computer Inc.	
PROJECT : FH9	
Size	Document Number: JET/TPOAZ_S3_MEM_Interface	Rev 2A
Date: Wednesday, November 19, 2014	Sheet 24 of 48

2GB gDDR3L



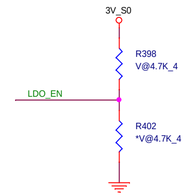
	Quanta Computer Inc.		
	PROJECT : FH9		
Size	Document Number: JET/TOPAZ_S3_VRAM_DDR3 BGA96		Rev 2A
Date: Wednesday, November 19, 2014		Sheet 25 of 48	

DP to VGA converter (Low level Only)



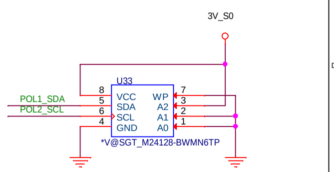
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO



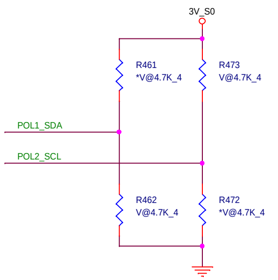
EEPROM MODE

I2C address=0xA8



Mode Configuration

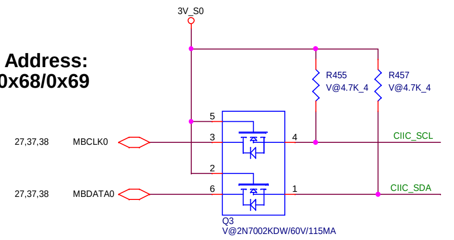
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



RTD2168 Supports three operation mode for system design.
Reserve 4.7K resistor pull high/low for mode selection

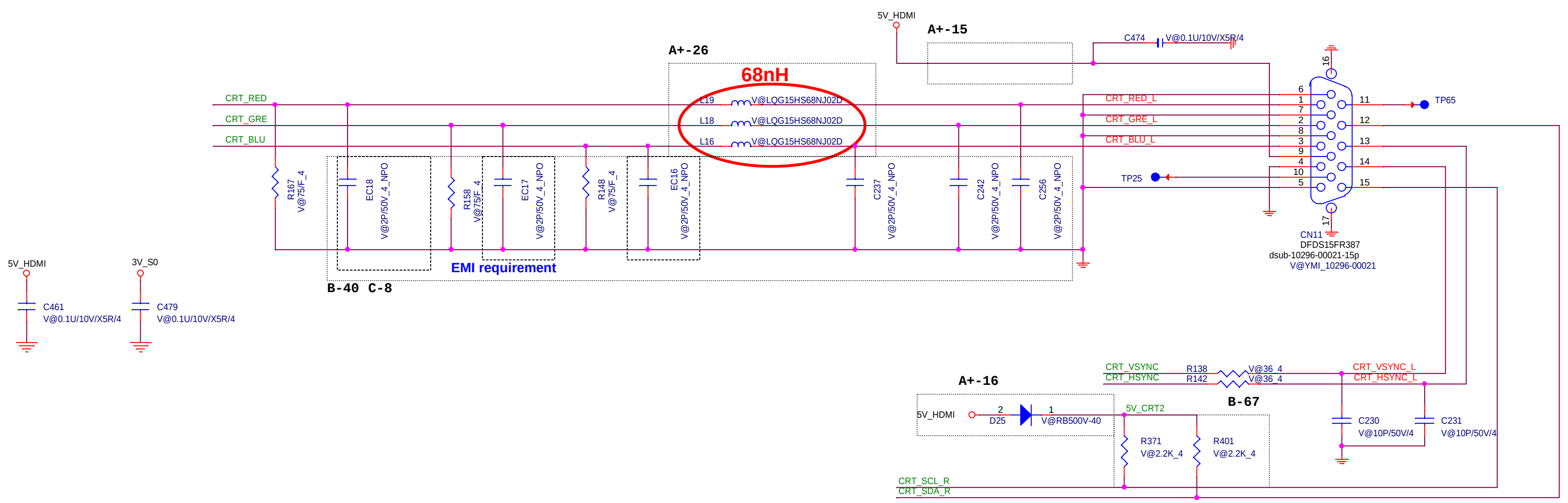
SMBUS

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



CRT PORT

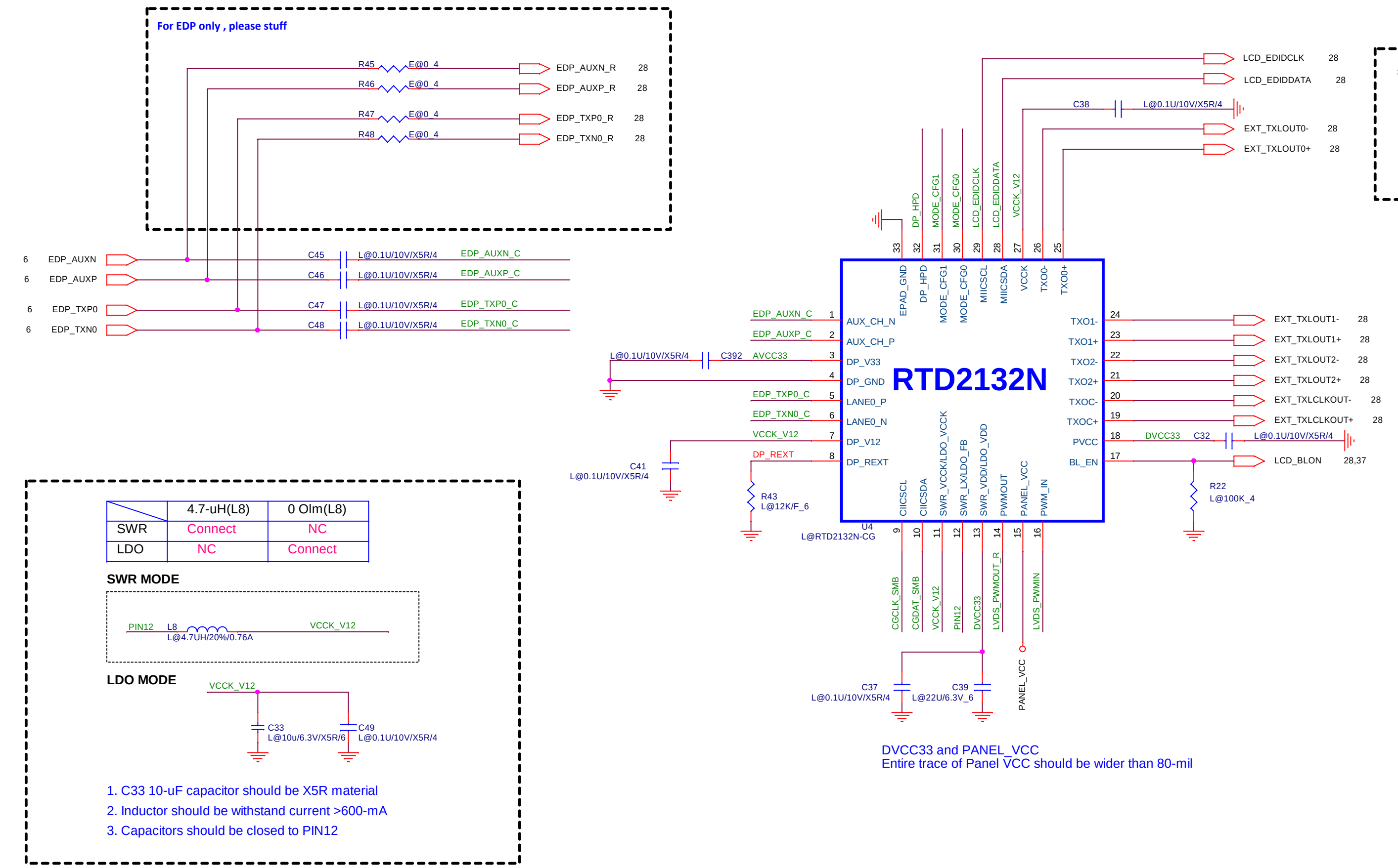
CRT CONN/DDC LEVEL SHIFT



Quanta Computer Inc.
PROJECT : FH9

Size	Document Number	Rev
	DP to VGA (RTD2168)/CRT	2A
Date: Wednesday, November 19, 2014	Sheet 26 of 48	

Converter RTD2132N-CG



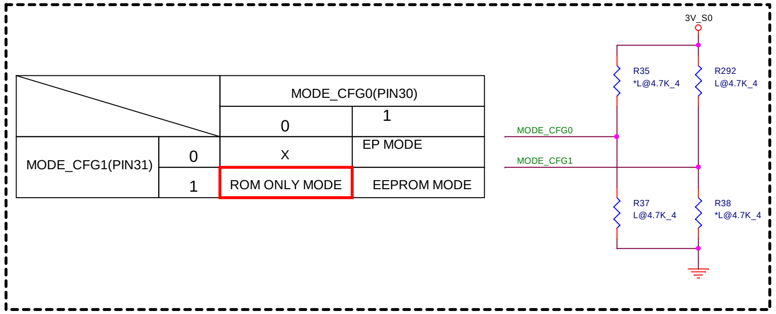
	4.7-uH(L8)	0 Olm(L8)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE

LDO MODE

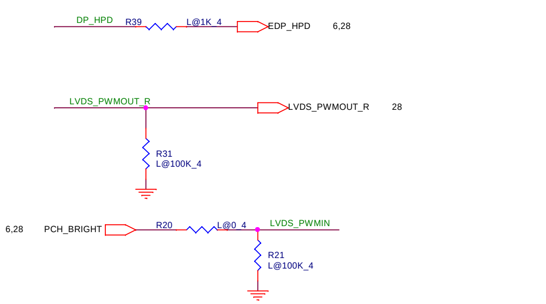
1. C33 10-uF capacitor should be X5R material
2. Inductor should be withstand current >600-mA
3. Capacitors should be closed to PIN12

Mode Configuration



		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

HPD/ Back Light/ BL PWM



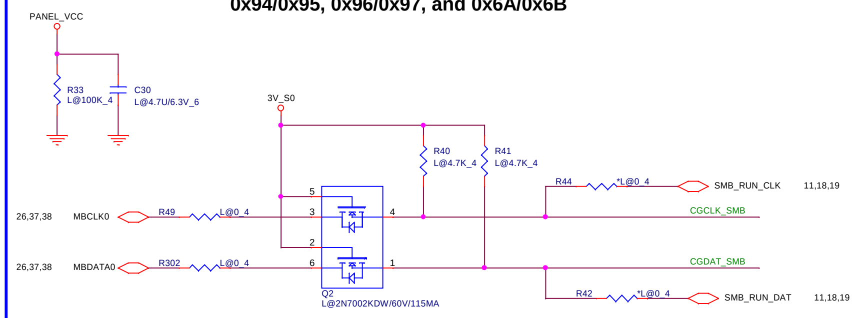
Reserve EEPROM

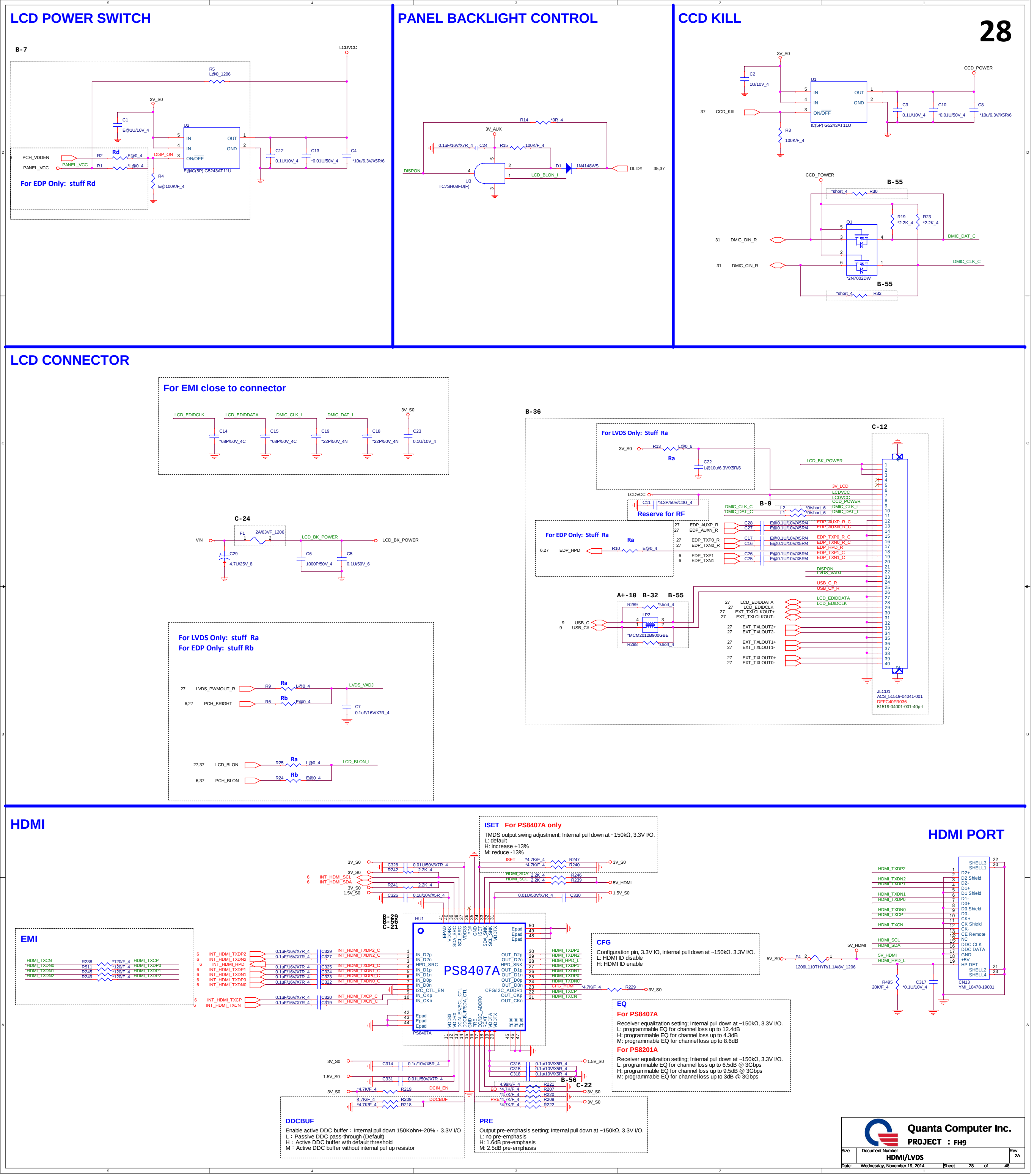
Address=0xA8

Reserve colay with RTD2132N

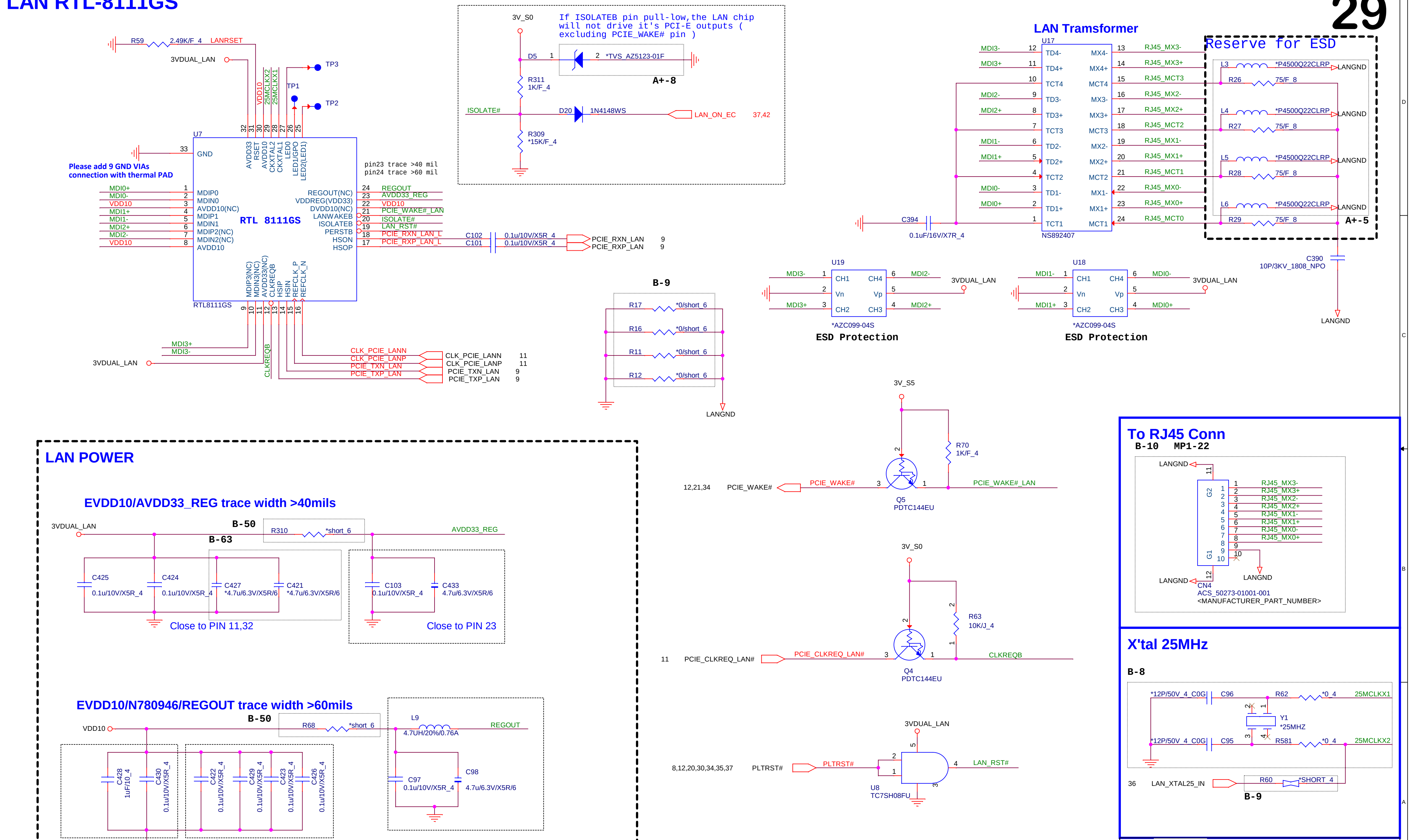
SMBUS & Panel VCC

RTD2132N Slave Address:
0x94/0x95, 0x96/0x97, and 0x6A/0x6B




LCD POWER SWITCH
For EDP Only: stuff Rd
PANEL BACKLIGHT CONTROL
CCD KILL
LCD CONNECTOR
For EMI close to connector
For LVDS Only: Stuff Ra
Reserve for RF
For EDP Only: Stuff Ra
For LVDS Only: stuff Ra
For EDP Only: stuff Rb
HDMI
EMI
HDMI PORT
PS8407A
ISET For PS8407A only
TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%
CFG
Configuration pin, 3.3V IO, internal pull down at ~150kΩ. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
EQ
For PS8407A
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB
For PS8201A
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 6.5dB @ 3Gbps
H: programmable EQ for channel loss up to 9.5dB @ 3Gbps
M: programmable EQ for channel loss up to 3dB @ 3Gbps
DDCBUF
Enable active DDC buffer : Internal pull down 150Kohm+-20% , 3.3V I/O
L : Passive DDC pass-through (Default)
H : Active DDC buffer with default threshold
M : Active DDC buffer without internal pull up resistor
PRE
Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis
Quanta Computer Inc.
PROJECT : FH9
Size
Document Number
HDMI/LVDS
Rev
2A
Date: Wednesday, November 19, 2014
Sheet 28 of 48

LAN RTL-8111GS



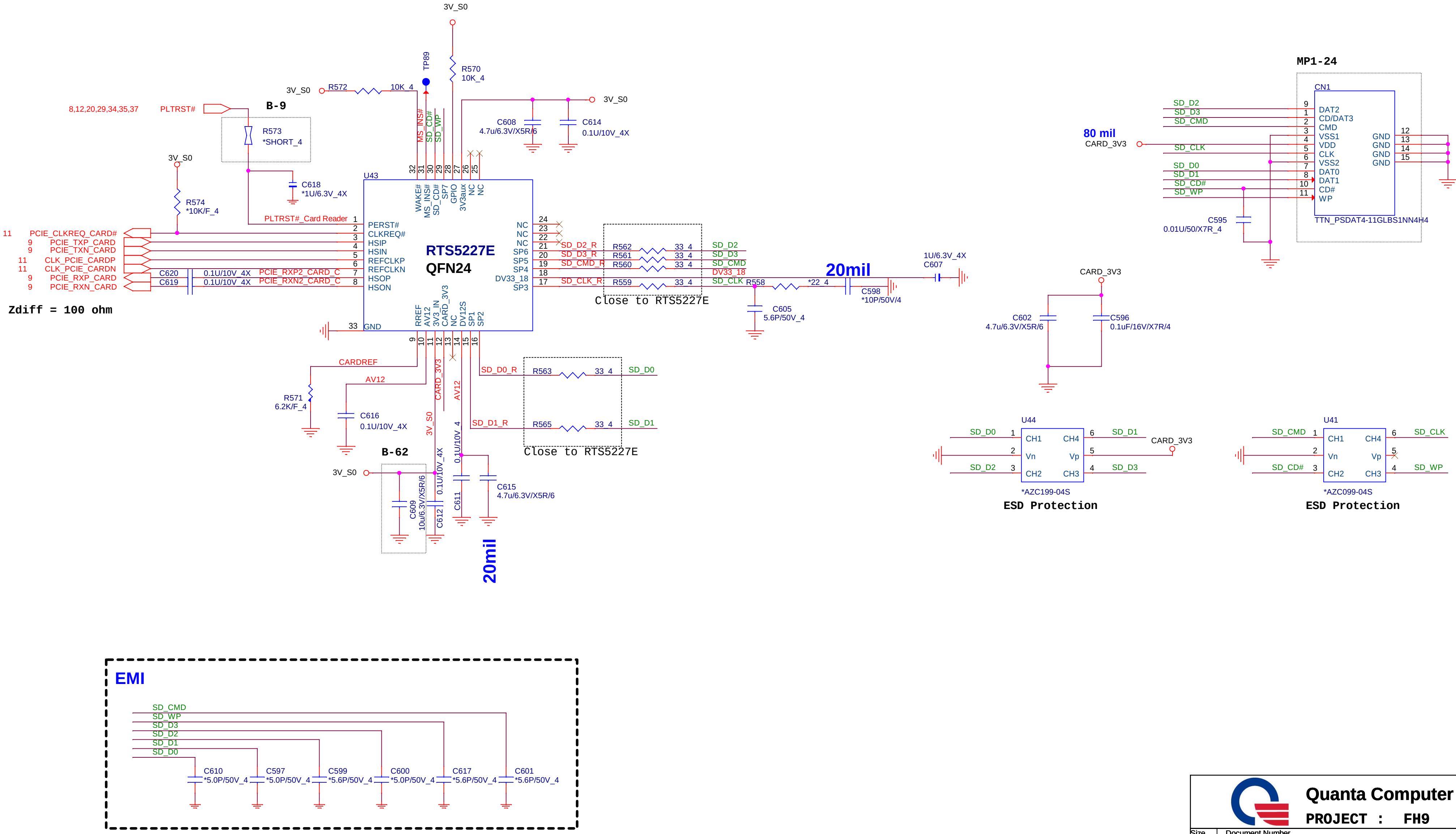
Quanta Computer Inc.

PROJECT : FH9

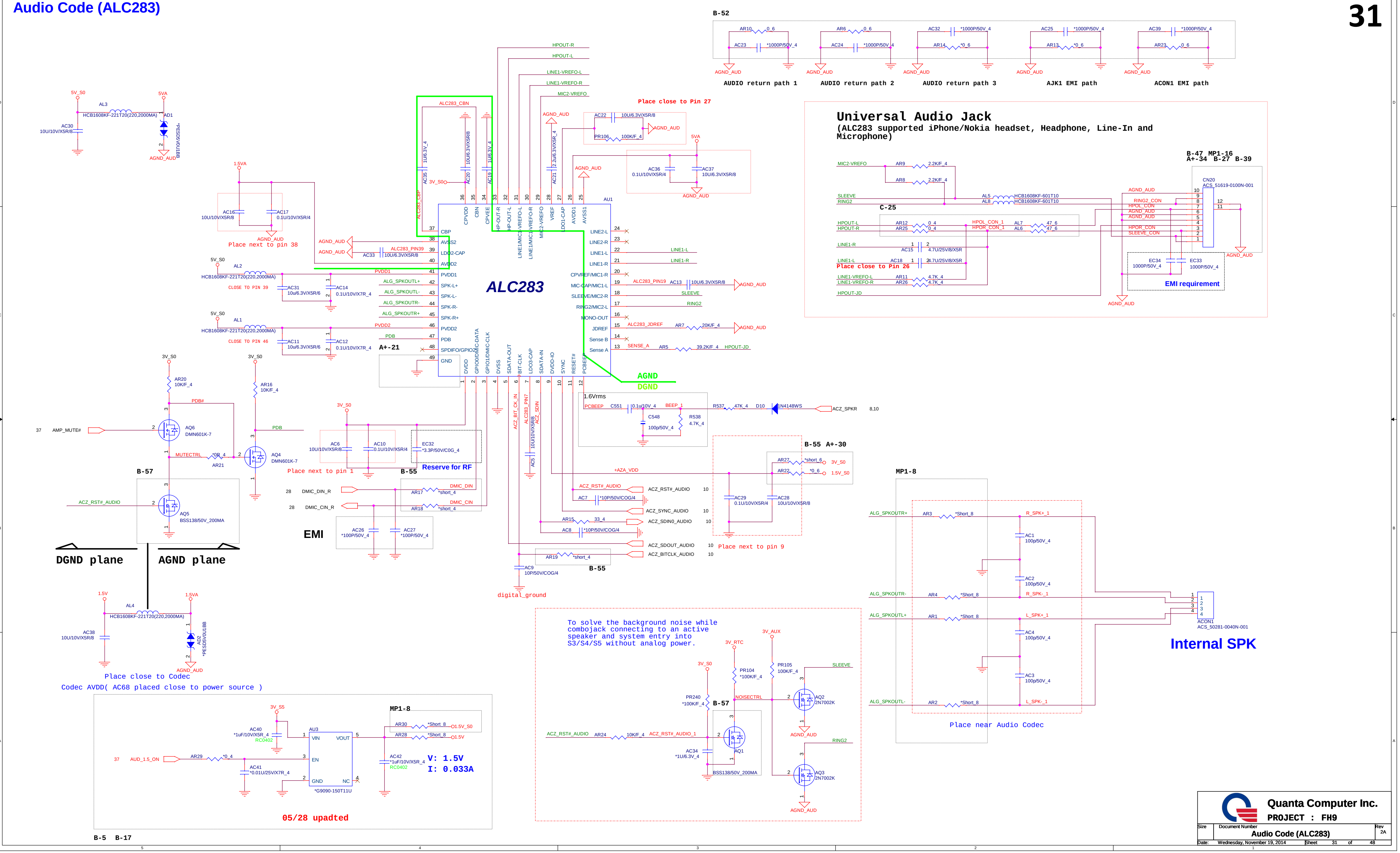
Size	Document Number	Rev
	LAN RTL8111GS/RJ45 conn	2A

Date: Wednesday, November 19, 2014 Sheet 29 of 48

Card Reader RTS5227E



Audio Code (ALC283)



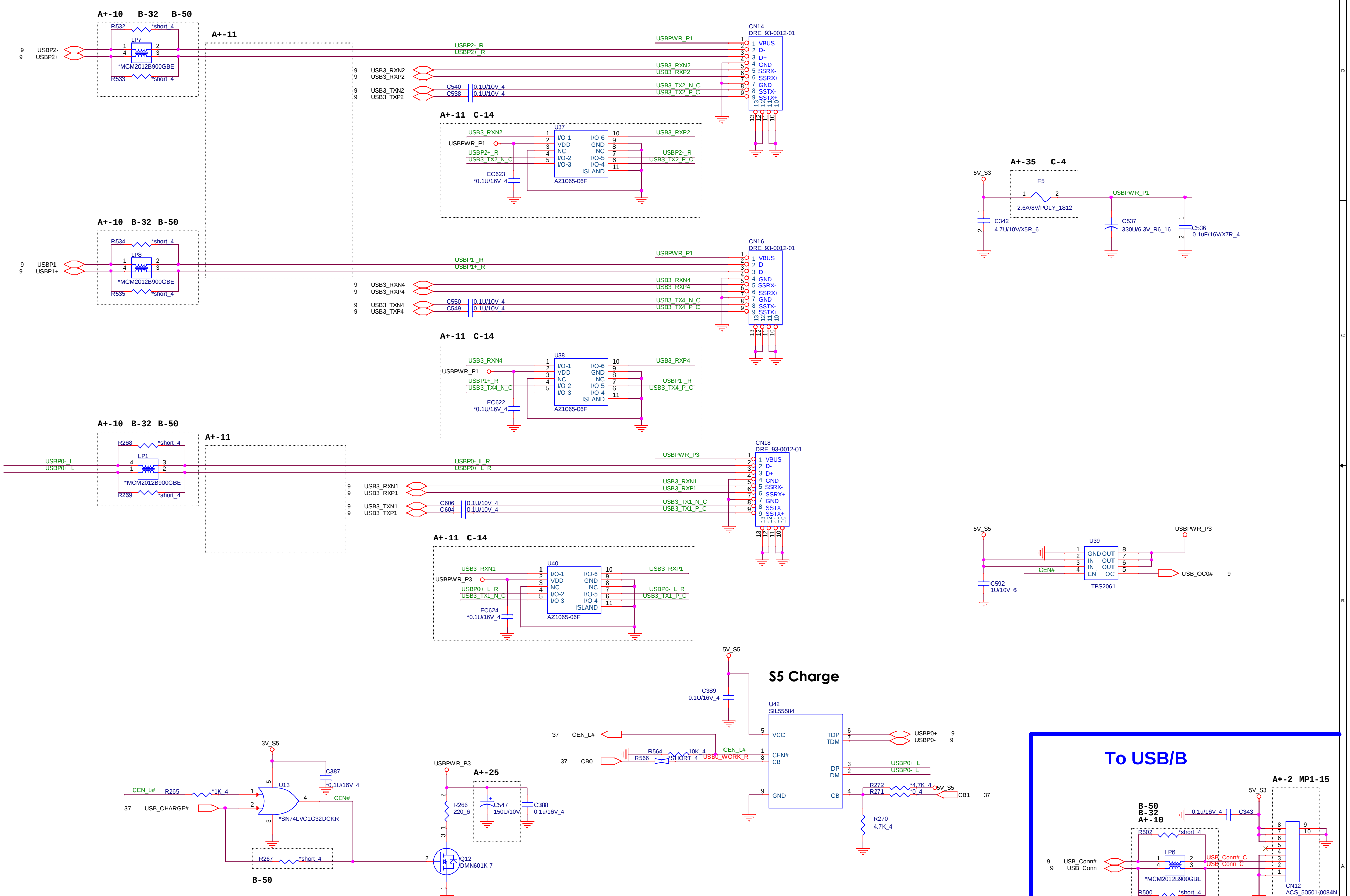
Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	Audio Code (ALC283)	2A

Date: Wednesday, November 19, 2014 Sheet 31 of 48

USB 3.0



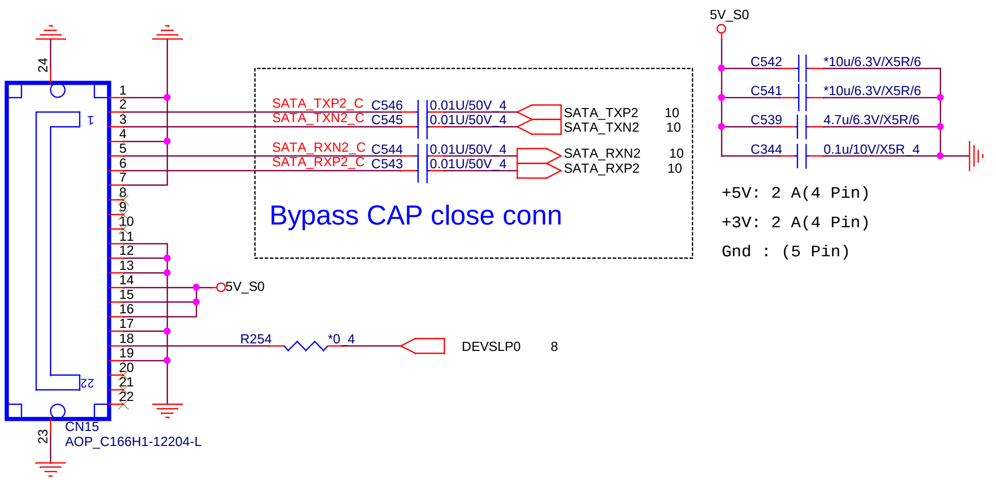
CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG55584 only)

Quanta Computer Inc.

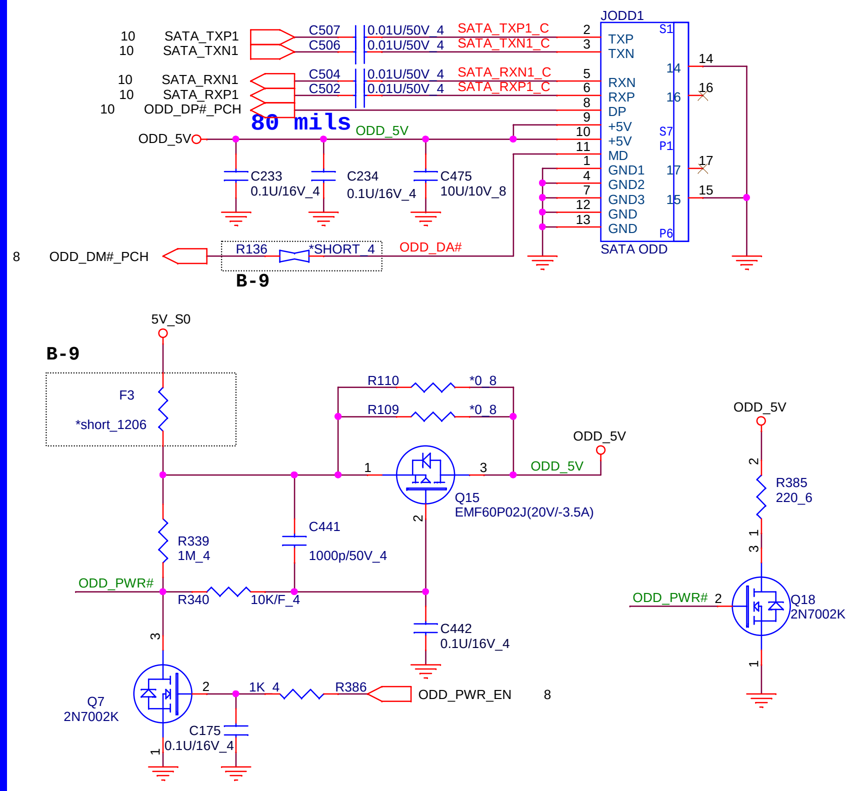
PROJECT : FH9

Size	Document Number	Rev
	USB3.0/Charger/USB2.0	2A

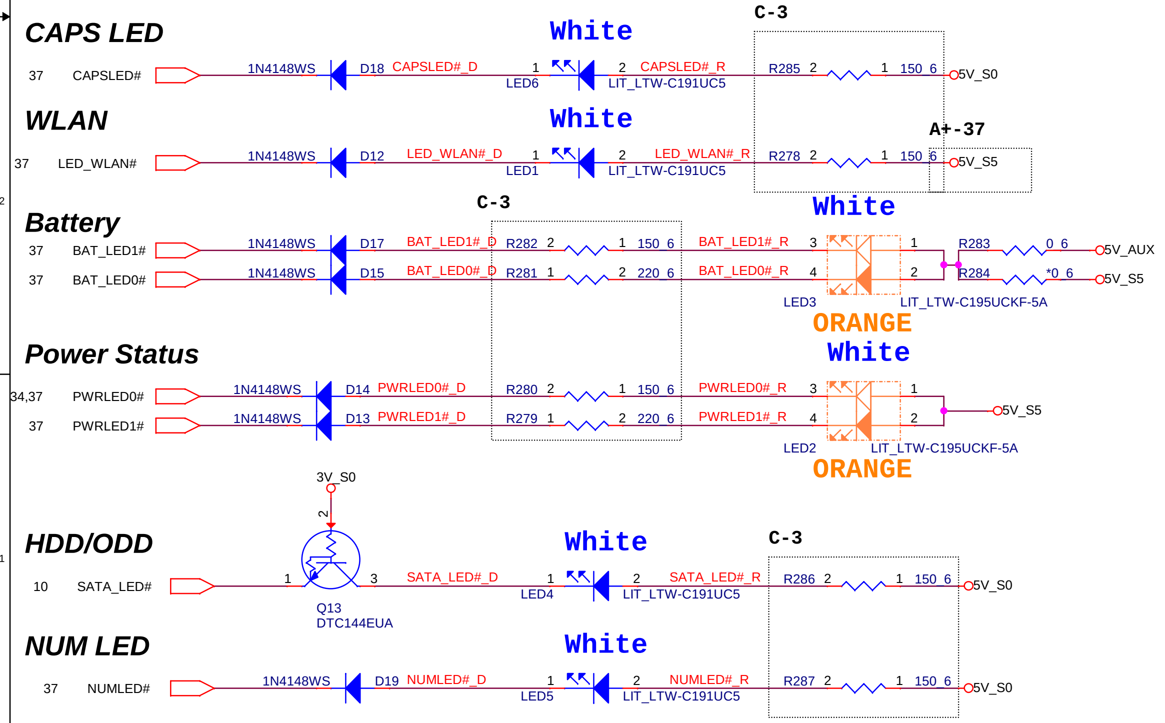
SATA HDD Connector



SATA ODD Connector



LED



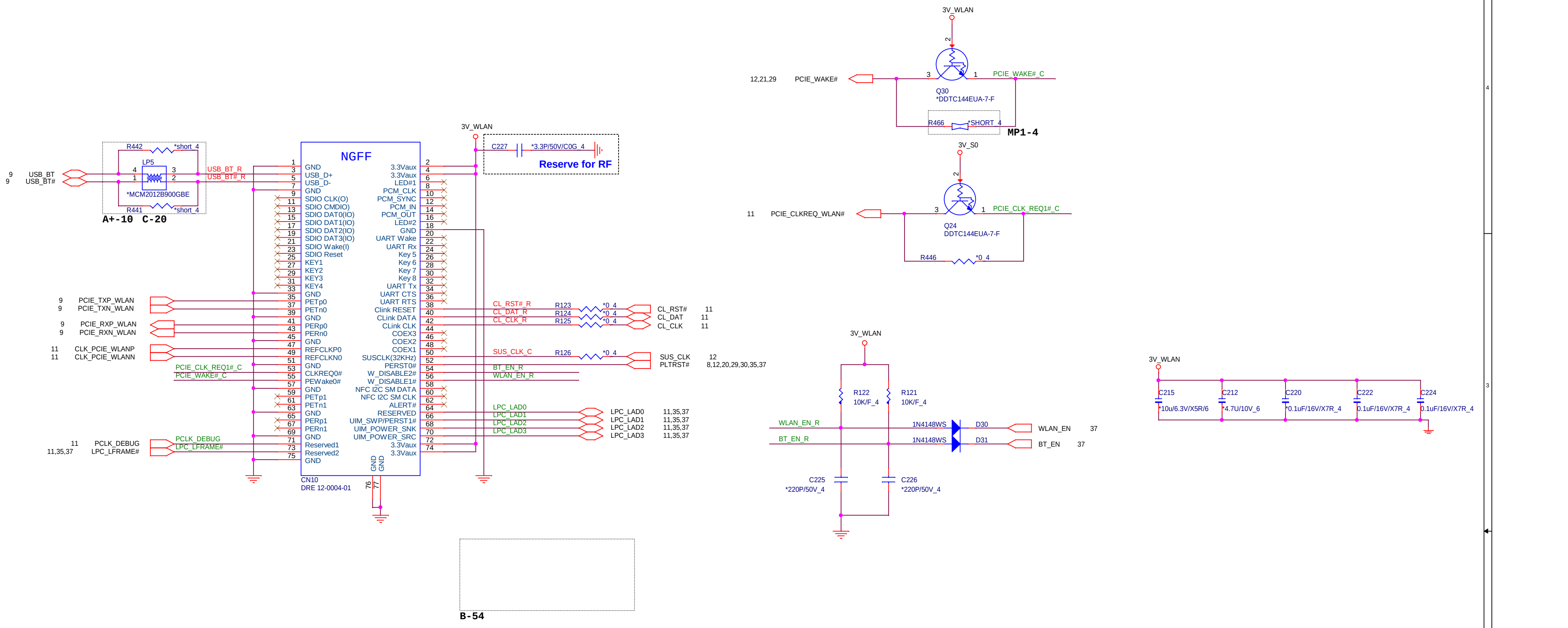
Quanta Computer Inc.

PROJECT : FH9

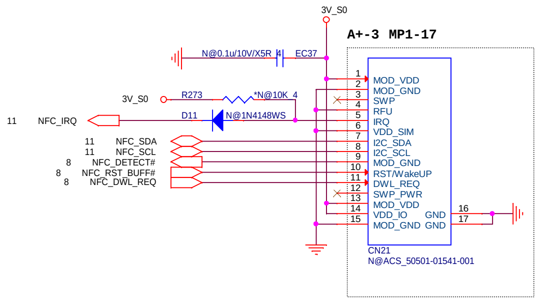
Size	Document Number	Rev
	HDD/ODD/LED	2A

Date: Wednesday, November 19, 2014 Sheet 33 of 48

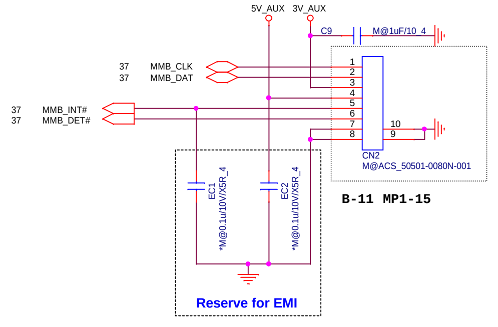
WLAN + BT(NGFF Socket Slot A-SD)



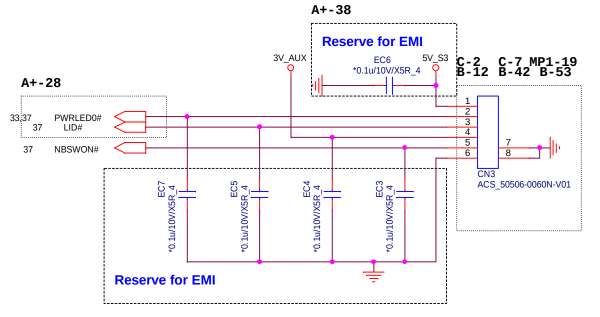
NFC



TO MMB/B



TO PWR/B

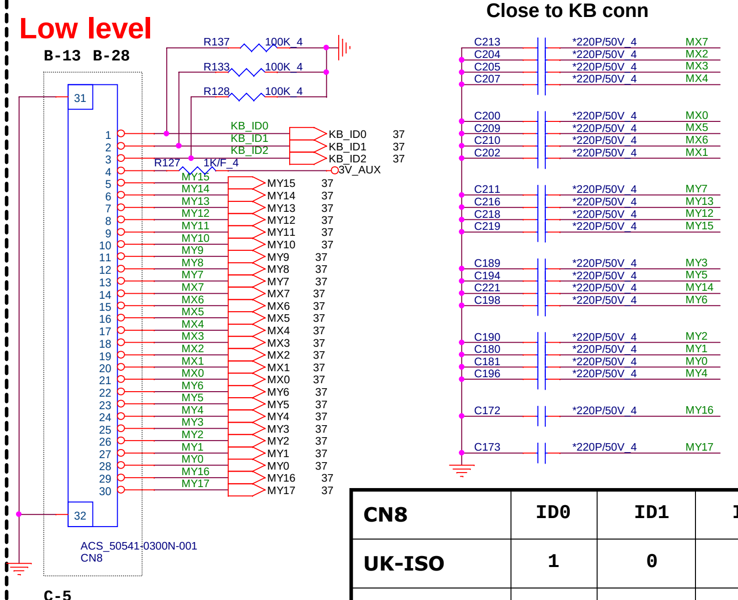


Quanta Computer Inc.			
PROJECT : FH9			
Size	Document Number: WLAN/BT/NFC/MMB/PWR		Rev 2A
Date: Wednesday, November 19, 2014	Sheet 34	of	48

Keyboard Connector

Low level

B-13 B-28

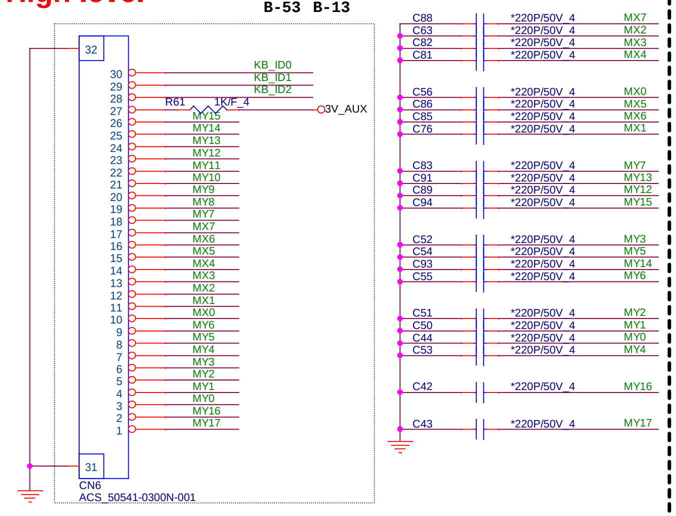


C-5

CN8	ID0	ID1	ID2
UK-ISO	1	0	1
US-ISO	0	1	1
JP-Low-ISO	1	1	1
JP-High-ISO	0	0	1

High level

B-53 B-13

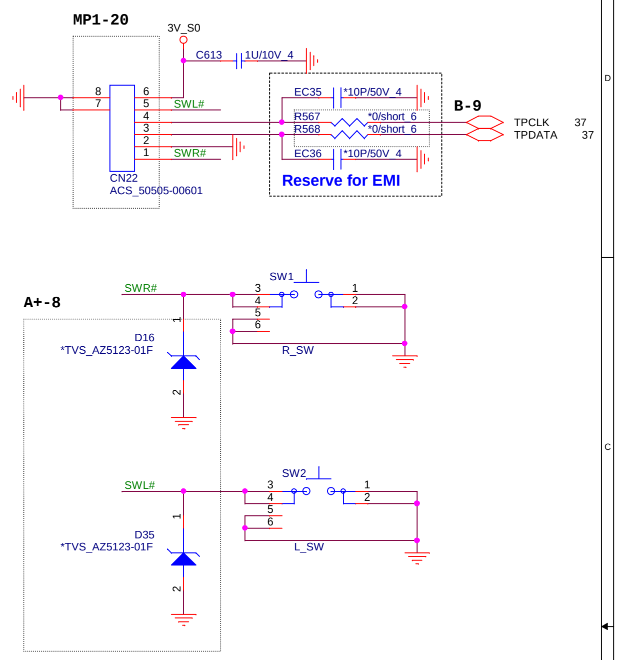


CN6	ID0	ID1	ID2
UK-CHO	1	0	0
US-CHO	0	1	0
JP-Low-CHO	1	1	0

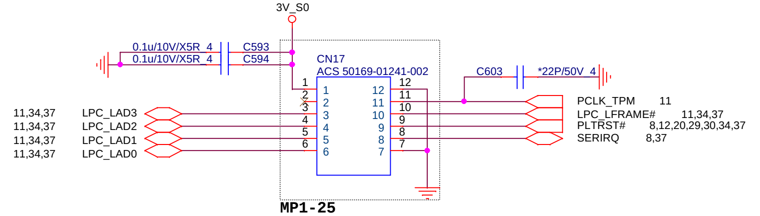
Touch Pad Connector

35

MP1-20

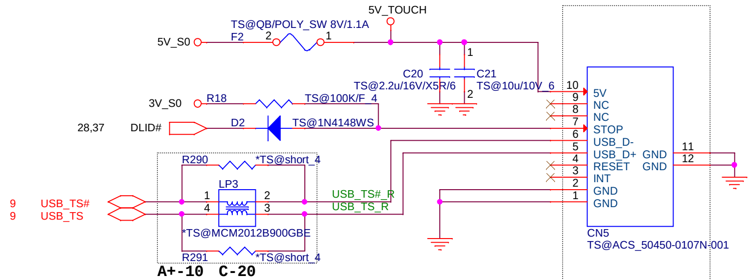


TPM



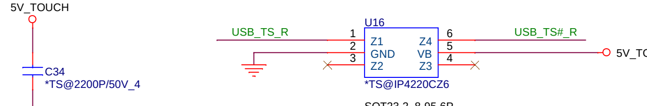
MP1-25

Touch Screen



A+-10 C-20

B-45 MP-21

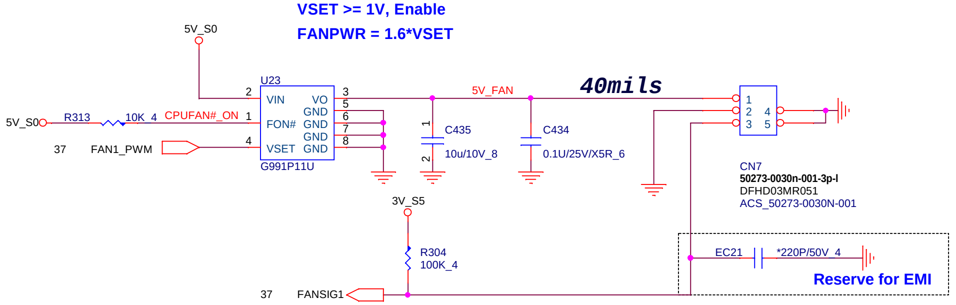


ESD Protection

FAN Control

VSET >= 1V, Enable

FANPWR = 1.6*VSET



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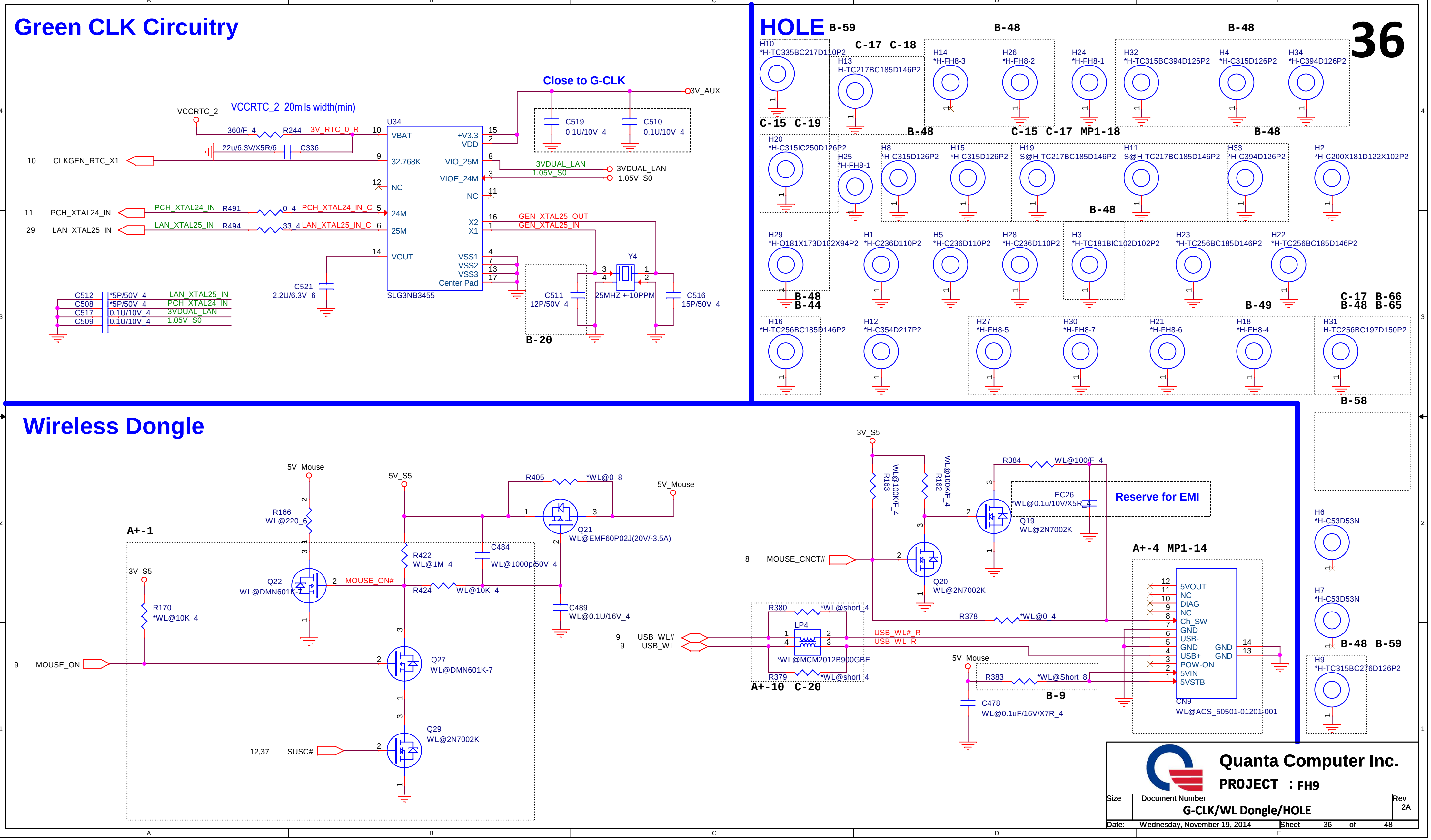
PROJECT : FH9

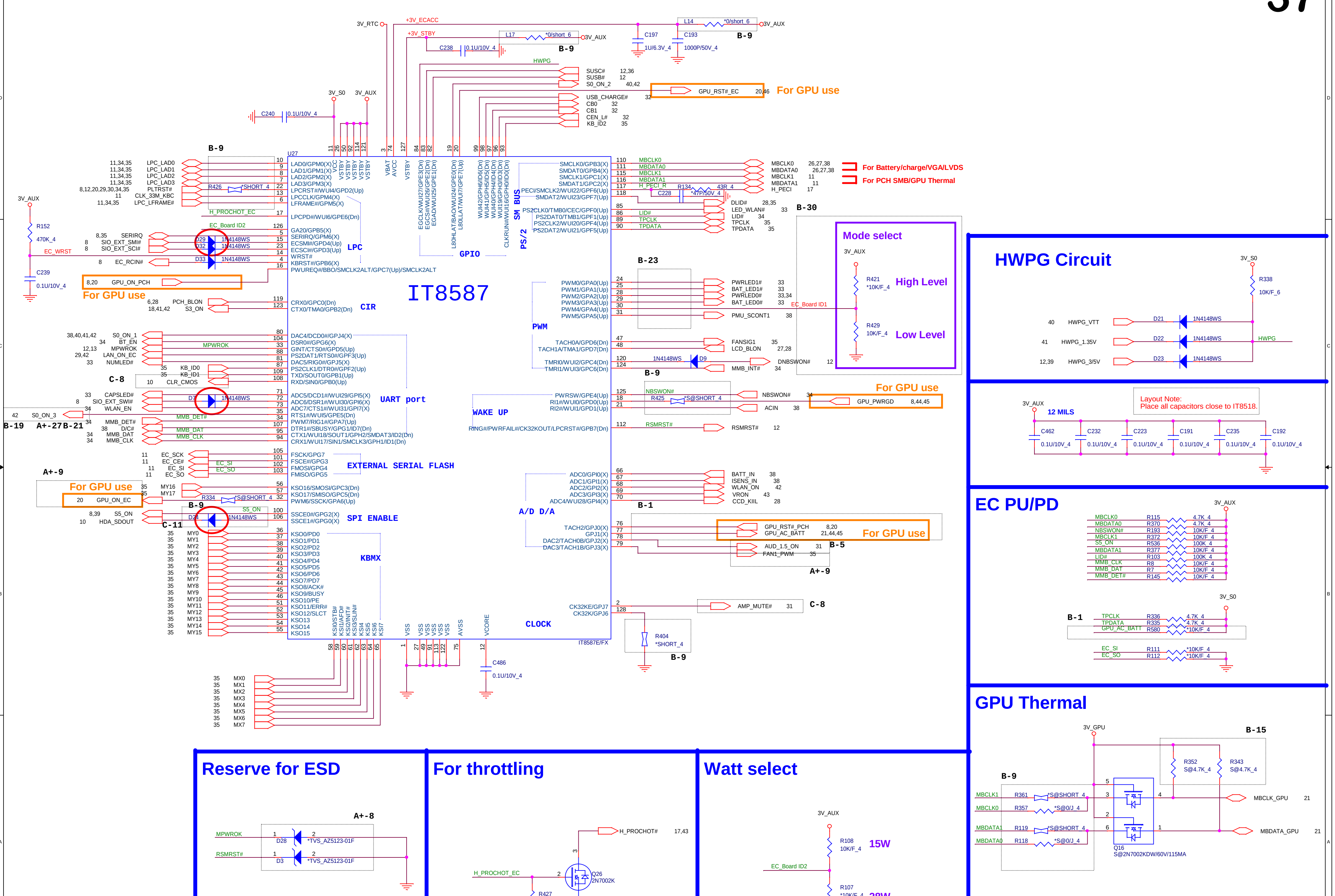
Size	Document Number	Rev
	KB/FAN/TP/TPM/Touch screen	2A

Date: Wednesday, November 19, 2014 Sheet 35 of 48



Green CLK Circuitry
Close to G-CLK
VCCRTC_2 20mils width(min)
VCCRTC_2
3V_AUX
U34
SLG3NB3455
VBAT
32.768K
NC
24M
25M
VOUT
+V3.3
VDD
VIO_25M
VIOE_24M
X2
X1
VSS1
VSS2
VSS3
Center Pad
CLKGEN_RTC_X1
PCH_XTAL24_IN
LAN_XTAL25_IN
R244 360/F_4
3V_RTC_0_R
C336 22u/6.3V/X5R/6
R491 0_4
PCH_XTAL24_IN_C
R494 33_4
LAN_XTAL25_IN_C
C519 0.1U/10V_4
C510 0.1U/10V_4
3VDUAL_LAN
1.05V_S0
GEN_XTAL25_OUT
GEN_XTAL25_IN
Y4 25MHZ +-10PPM
C511 12P/50V_4
C516 15P/50V_4
C521 2.2U/6.3V_6
C512 *5P/50V_4 LAN_XTAL25_IN
C508 *5P/50V_4 PCH_XTAL24_IN
C517 0.1U/10V_4 3VDUAL_LAN
C509 0.1U/10V_4 1.05V_S0
B-20
HOLE
36
Wireless Dongle
5V_Mouse
5V_S5
3V_S5
R166 WL@220_6
R405 *WL@0_8
Q21 WL@EMF60P02J(20V/-3.5A)
Q22 WL@DMN601K-7
MOUSE_ON#
R422 WL@1M_4
C484 WL@1000p/50V_4
R424 WL@10K_4
C489 WL@0.1U/16V_4
R170 *WL@10K_4
MOUSE_ON
Q27 WL@DMN601K-7
Q29 WL@2N7002K
SUSC#
A+-1
R163 WL@100K/F_4
R162 WL@100K/F_4
R384 WL@100/F_4
EC26 *WL@0.1u/10V/X5R_4
Reserve for EMI
Q19 WL@2N7002K
Q20 WL@2N7002K
MOUSE_CNCT#
USB_WL#
USB_WL
R380 *WL@short_4
LP4 *WL@MCM2012B900GBE
R379 *WL@short_4
R378 *WL@0_4
USB_WL#_R
USB_WL_R
R383 *WL@Short_8
C478 WL@0.1uF/16V/X7R_4
A+-10 C-20
B-9
A+-4 MP1-14
CN9 WL@ACS_50501-01201-001
5VOUT
NC
DIAG
Ch_SW
GND
USB-
USB+
POW-ON
5VIN
5VSTB
Quanta Computer Inc.
PROJECT : FH9
Size
Document Number
G-CLK/WL Dongle/HOLE
Rev 2A
Date: Wednesday, November 19, 2014
Sheet 36 of 48

EC IT8587

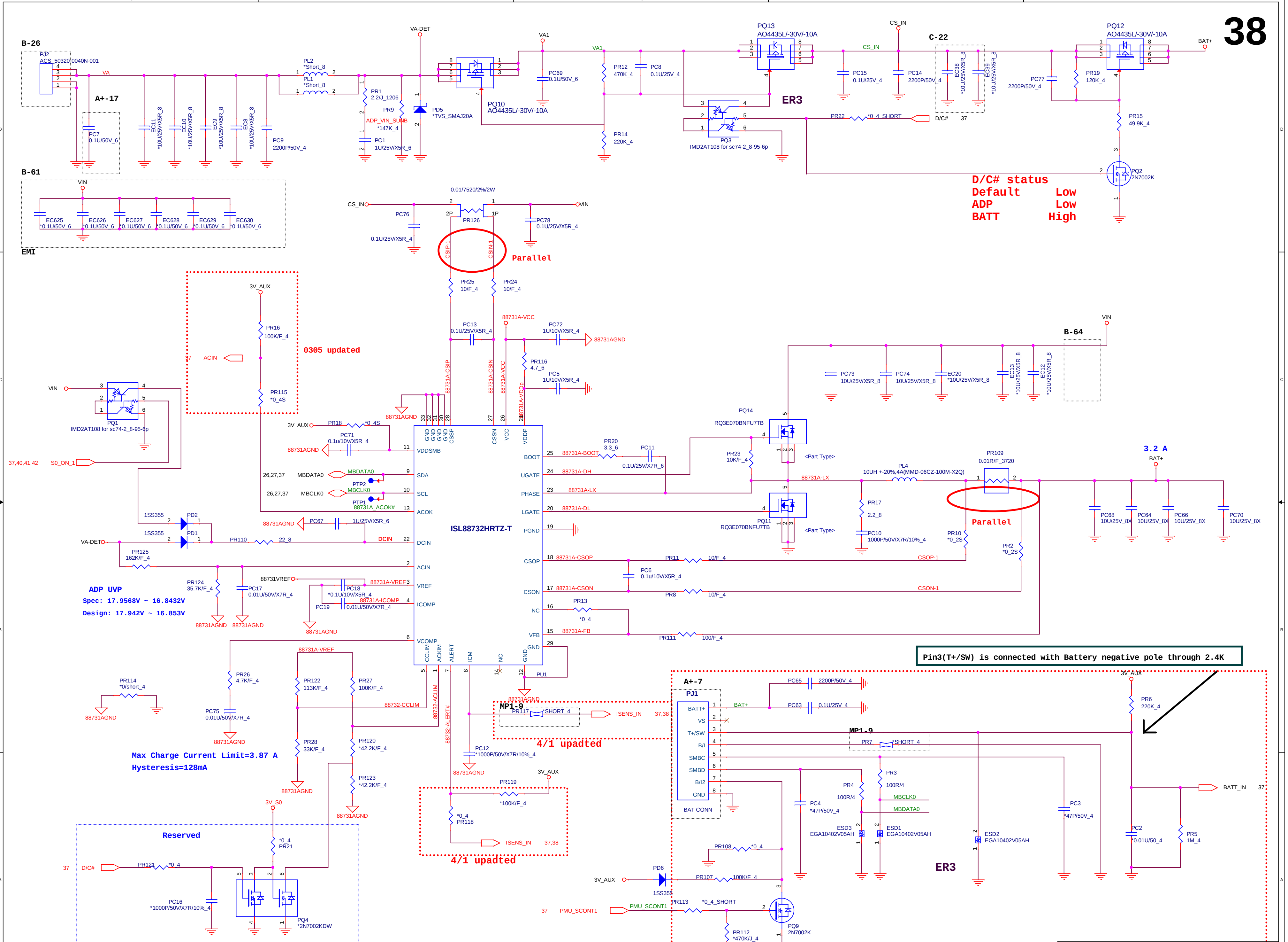


Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	EC_ITE8587	2A

Date: Wednesday, November 19, 2014 Sheet 37 of 48



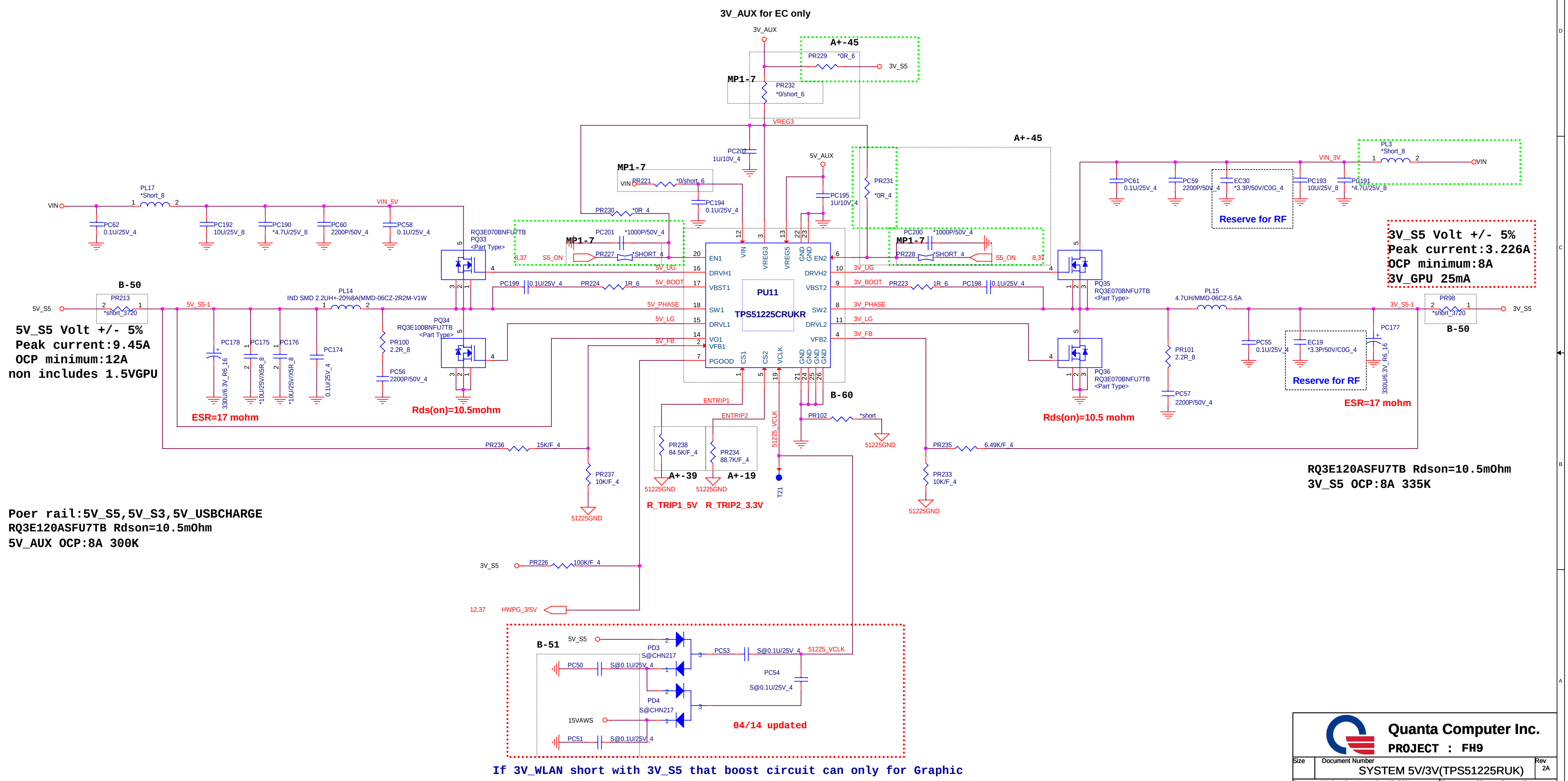
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.

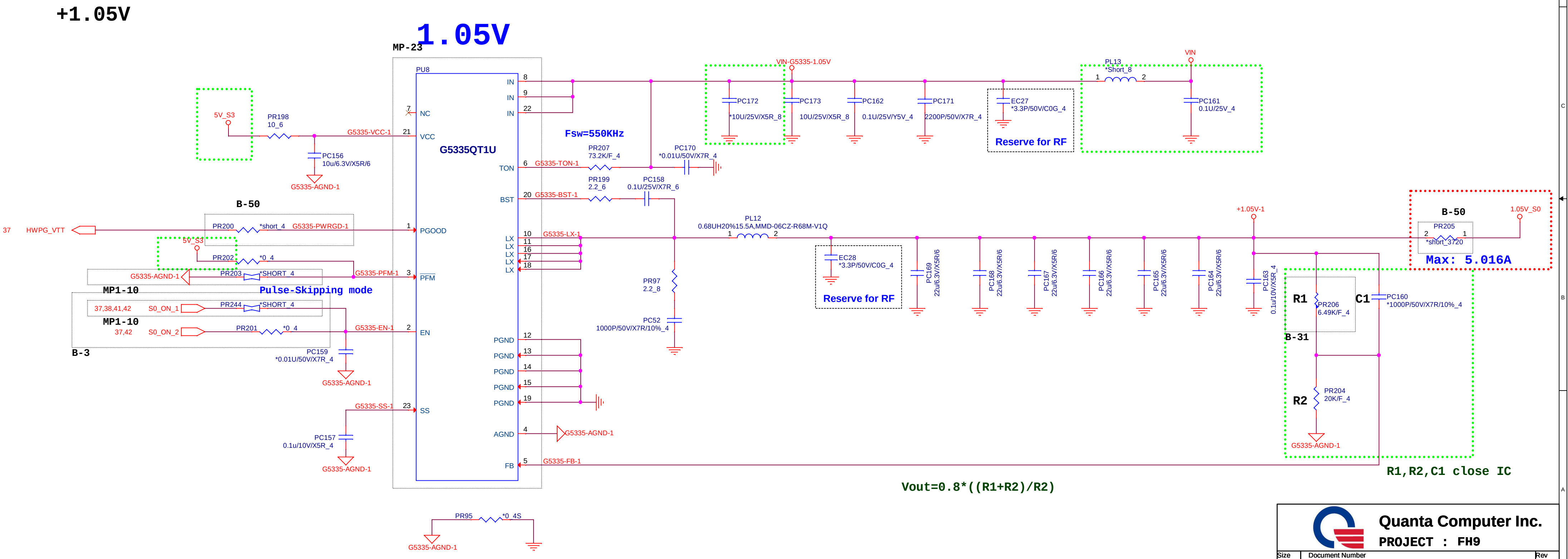
PROJECT : FH9

Size	Document Number	Rev
	VIN/CHARGER-ISL88732	2A

Date: Wednesday, November 19, 2014 Sheet 38 of 48



3V_AUX for EC only
3V_AUX
A+-45
PR229 *0R_6
3V_S5
MP1-7
PR232 *0/short_6
VREG3
A+-45
PC202 1U/10V_4
5V_AUX
MP1-7
VIN PR221 *0/short_6
PC194 0.1U/25V_4
PC195 1U/10V_4
PR231 *0R_4
PR230 *0R_4
PL17 *Short_8
VIN
VIN_5V
PC62 0.1U/25V_4
PC192 10U/25V_8
PC190 *4.7U/25V_8
PC60 2200P/50V_4
PC58 0.1U/25V_4
RQ3E070BNFU7TB
PQ33
<Part Type>
MP1-7
PC201 *1000P/50V_4
PR227 *SHORT_4
8,37 S5_ON
5V_UG
5V_BOOT
PC199 0.1U/25V_4
PR224 1R_6
5V_PHASE
5V_LG
5V_FB
B-50
5V_S5
PR213 *short_3720
5V_S5-1
PL14
IND SMD 2.2UH+-20%8A(MMD-06CZ-2R2M-V1W
PQ34
RQ3E100BNFU7TB
<Part Type>
PC178 330U/6.3V_R6_16
PC175 *10U/25V/X5R_8
PC176 *10U/25V/X5R_8
PC174 0.1U/25V_4
PR100 2.2R_8
PC56 2200P/50V_4
5V_S5 Volt +/- 5%
Peak current:9.45A
OCP minimum:12A
non includes 1.5VGPU
ESR=17 mohm
Rds(on)=10.5mohm
PU11
TPS51225CRUKR
EN1 DRVH1 VBST1 SW1 DRVL1 VO1 VFB1 PGOOD
VIN VREG3 VREG5 GND GND CS1 CS2 VCLK
EN2 DRVH2 VBST2 SW2 DRVL2 VFB2
B-60
ENTRIP1
ENTRIP2
PR238 84.5K/F_4
PR234 88.7K/F_4
A+-39
A+-19
51225GND
R_TRIP1_5V R_TRIP2_3.3V
51225_VCLK
T21
PR102 *short
PR236 15K/F_4
PR237 10K/F_4
PR235 6.49K/F_4
PR233 10K/F_4
MP1-7
PC200 *1000P/50V_4
PR228 *SHORT_4
S5_ON 8,37
3V_UG
3V_BOOT
PR223 1R_6
PC198 0.1U/25V_4
3V_PHASE
3V_LG
3V_FB
PQ35
RQ3E070BNFU7TB
<Part Type>
PQ36
RQ3E070BNFU7TB
<Part Type>
Rds(on)=10.5 mohm
PL15
4.7UH/MMD-06CZ-5.5A
PR101 2.2R_8
PC57 2200P/50V_4
PC55 0.1U/25V_4
EC19 *3.3P/50V/C0G_4
Reserve for RF
PC177 330U/6.3V_R6_16
ESR=17 mohm
3V_S5-1
PR98 *short_3720
B-50
3V_S5
VIN_3V
PL3 *Short_8
VIN
PC61 0.1U/25V_4
PC59 2200P/50V_4
EC30 *3.3P/50V/C0G_4
PC193 10U/25V_8
PC191 *4.7U/25V_8
Reserve for RF
3V_S5 Volt +/- 5%
Peak current:3.226A
OCP minimum:8A
3V_GPU 25mA
RQ3E120ASFU7TB Rdson=10.5mOhm
3V_S5 OCP:8A 335K
Poer rail:5V_S5,5V_S3,5V_USBCHARGE
RQ3E120ASFU7TB Rdson=10.5mOhm
5V_AUX OCP:8A 300K
3V_S5 PR226 100K/F_4
12,37 HWPG_3/5V
B-51
5V_S5
PD3 S@CHN217
PC53 S@0.1U/25V_4
51225_VCLK
PC50 S@0.1U/25V_4
PC54 S@0.1U/25V_4
PD4 S@CHN217
15VAWS
PC51 S@0.1U/25V_4
04/14 updated
If 3V_WLAN short with 3V_S5 that boost circuit can only for Graphic



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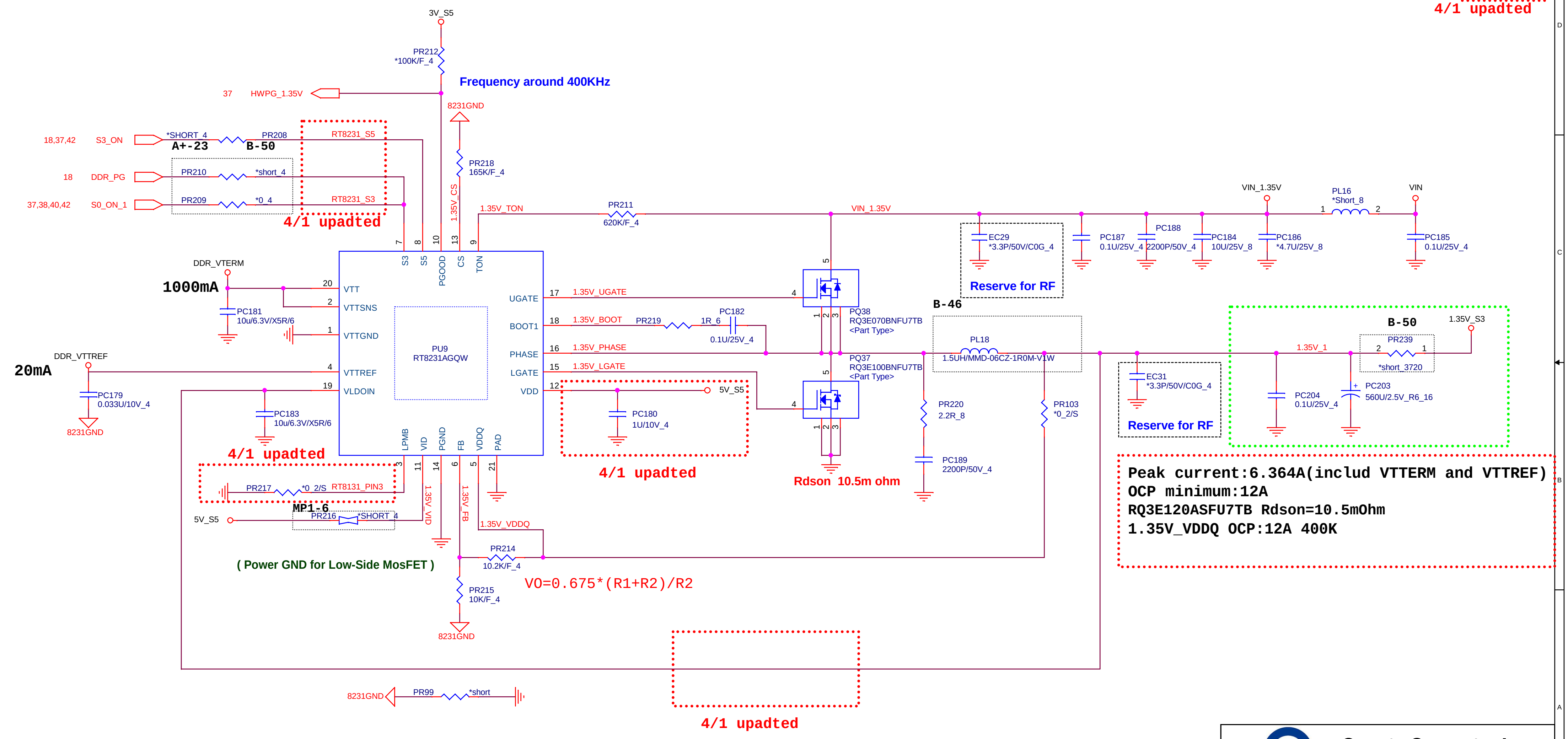
PROJECT : FH9

Size	Document Number	Rev
	1.05V-G5335	2A

Date: Wednesday, November 19, 2014 Sheet 40 of 48

1.35V_VDDQ(RT8231AGQW)

4/1 upadted

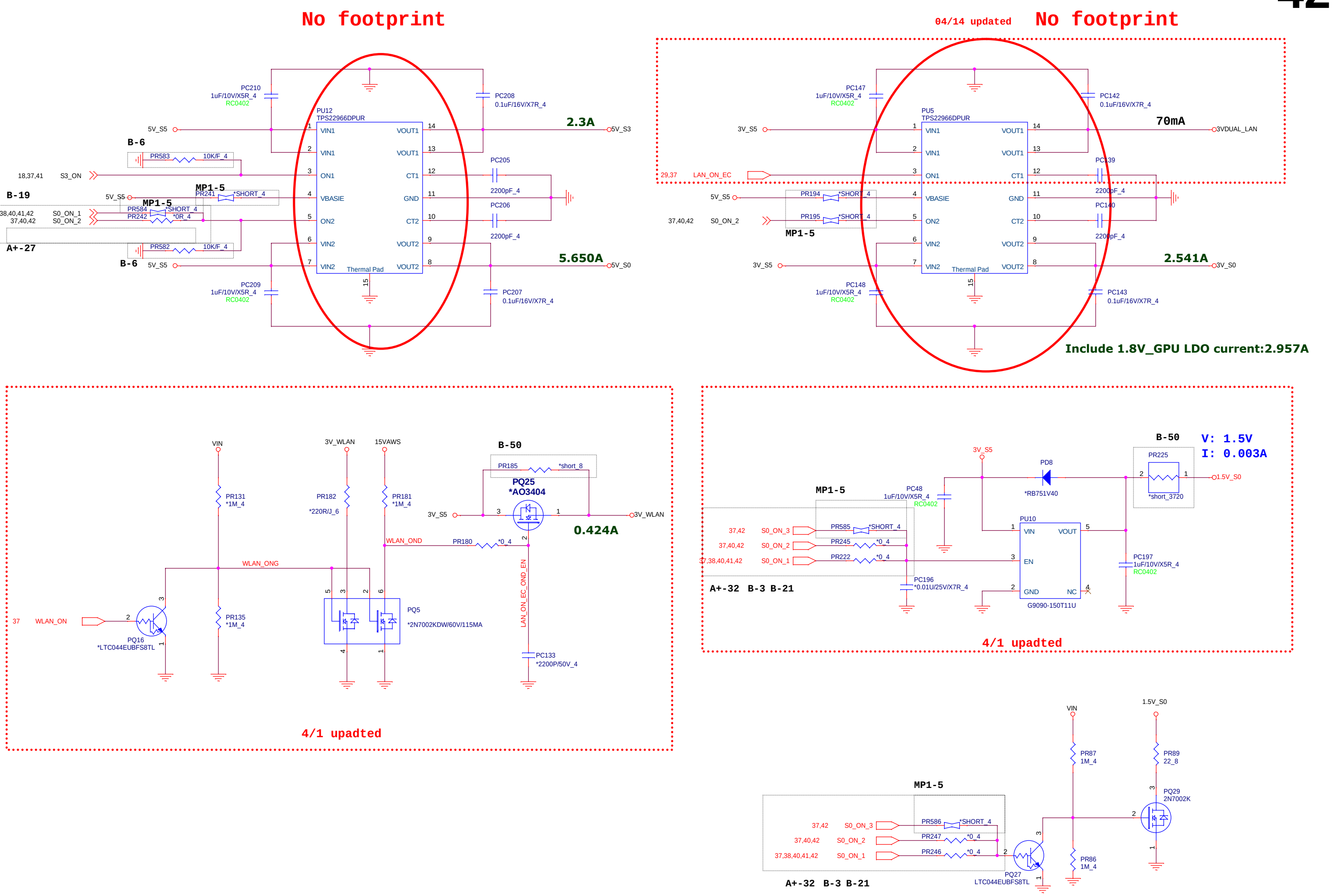


Quanta Computer Inc.

PROJECT : FH9

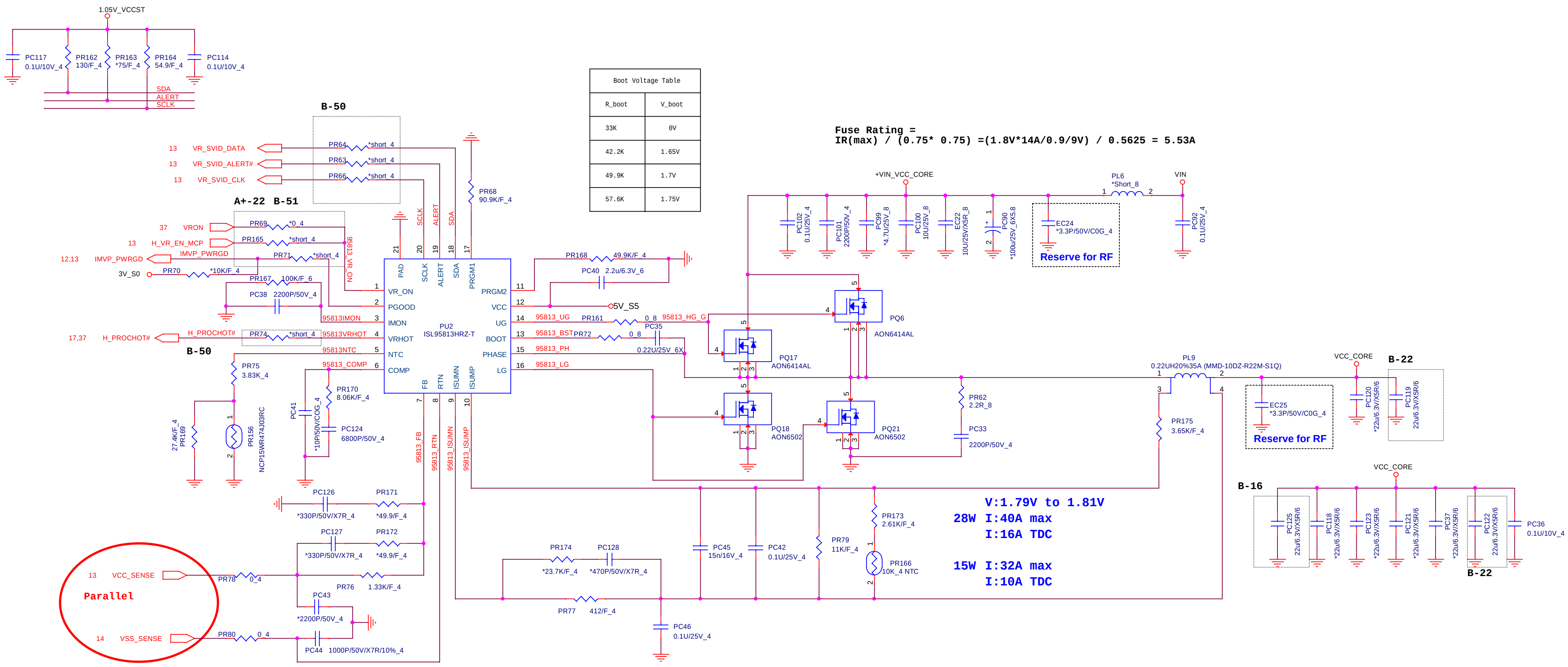
Size	Document Number	Rev
	DDR3L 1.35V(RT8231AGQW)	2A

Date: Wednesday, November 19, 2014 Sheet 41 of 48



Quanta Computer Inc.		
PROJECT : FH9		
Size	Document Number: SWITCH	Rev 2A
Date: Wednesday, November 19, 2014	Sheet 42 of 48	

CPU Core



Boot Voltage Table

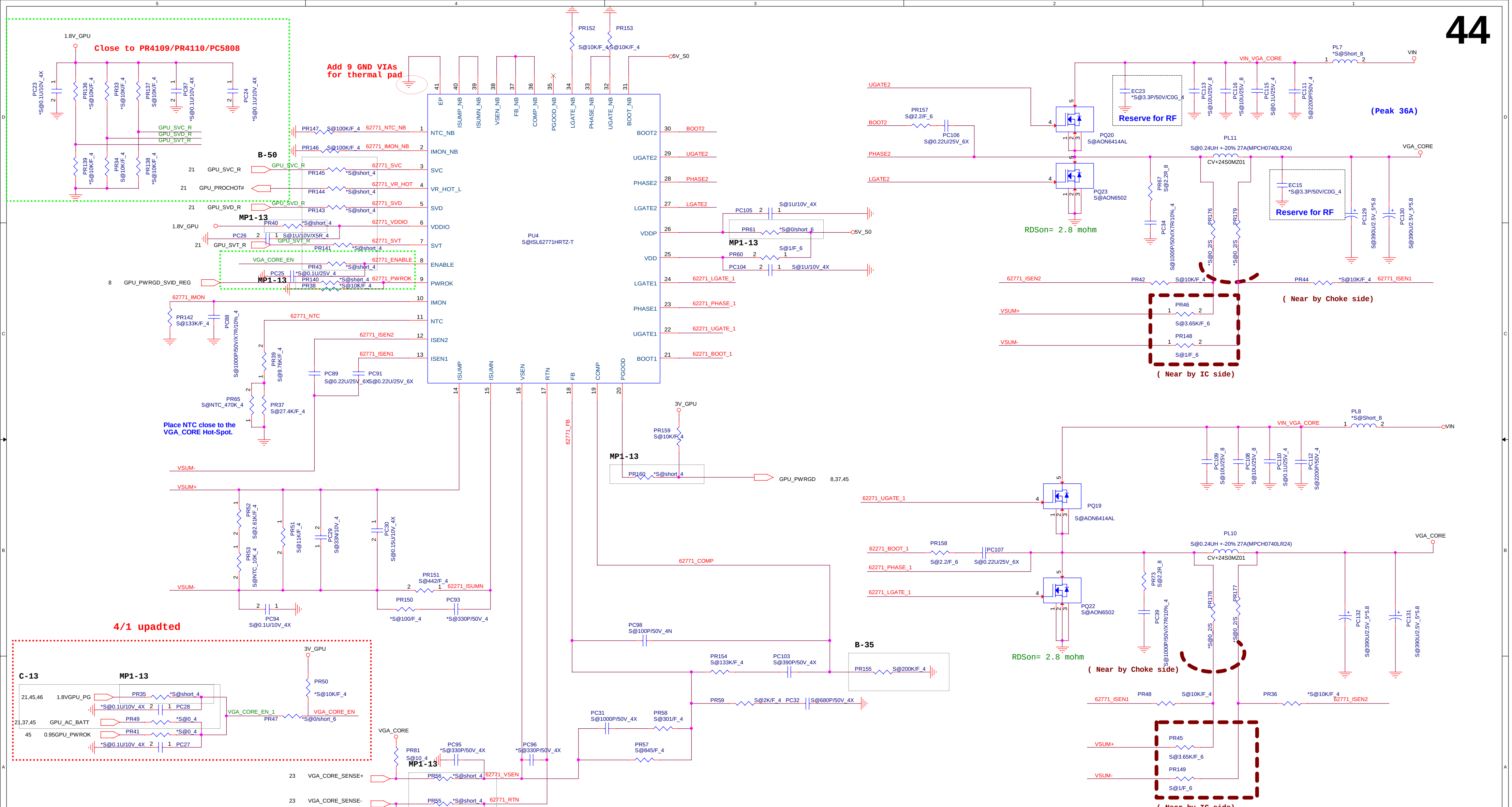
R_boot	V_boot
33K	0V
42.2K	1.65V
49.9K	1.7V
57.6K	1.75V

Fuse Rating =
IR(max) / (0.75* 0.75) =(1.8V*14A/0.9/9V) / 0.5625 = 5.53A

B-41

		28W	15W
(Iccmax)	PR68	113K(CS41132FB17)	90.9K(CS39092FB11)
(IMON)	PR167	105K(CS41053F919)	100K(CS41003F932)
(Loadline)	PR76	1.65K(CS21652FB29)	1.33K(CS21332FB11)
(OCP)	PR77	510(CS15102FB19)	412(CS14122FB15)

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



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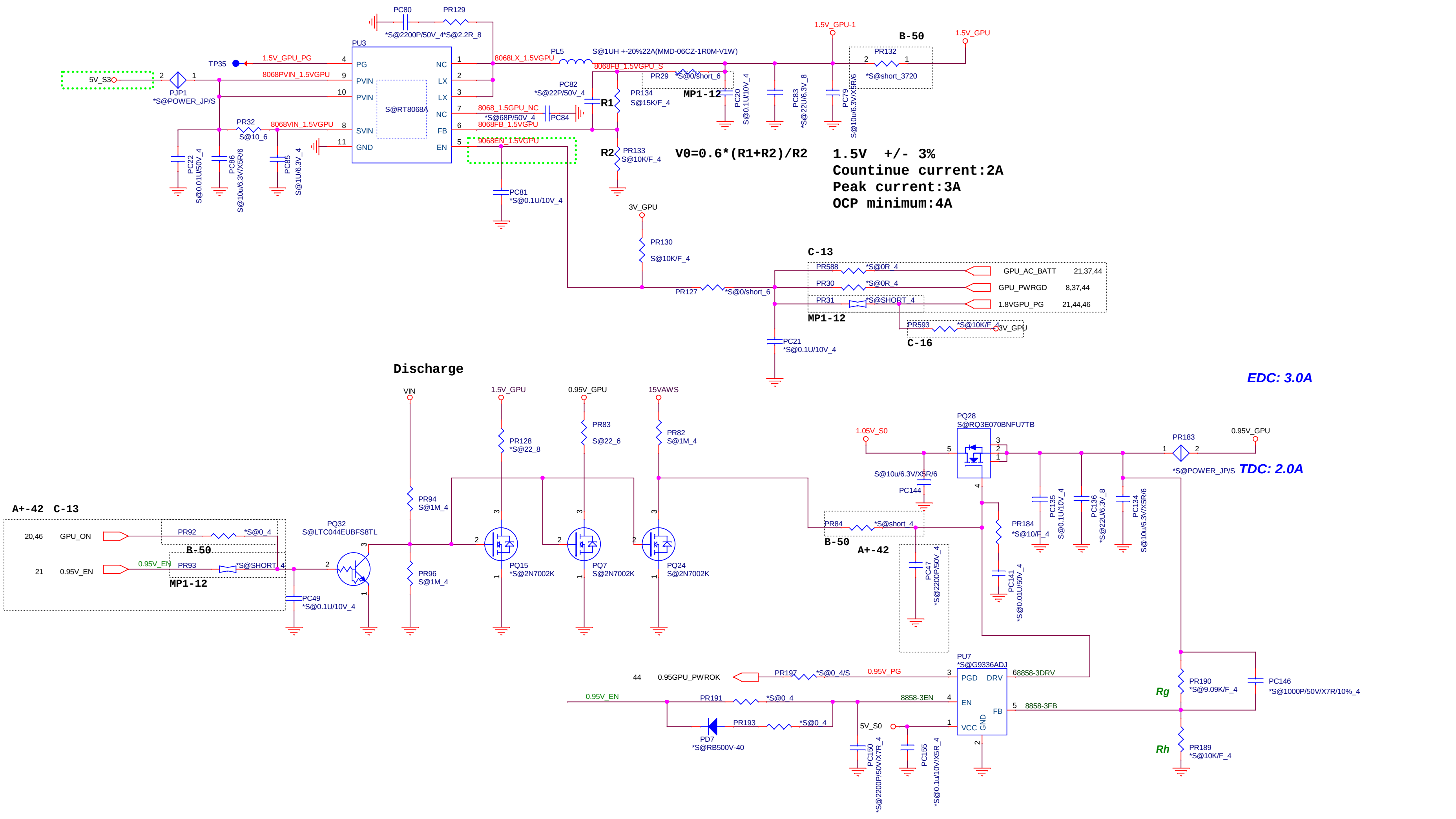
PROJECT : FH9

Size | Document Number: VGA CORE(INTERSIL 62771) | Rev 2A

Date: Wednesday, November 19, 2014 | Sheet 44 of 48

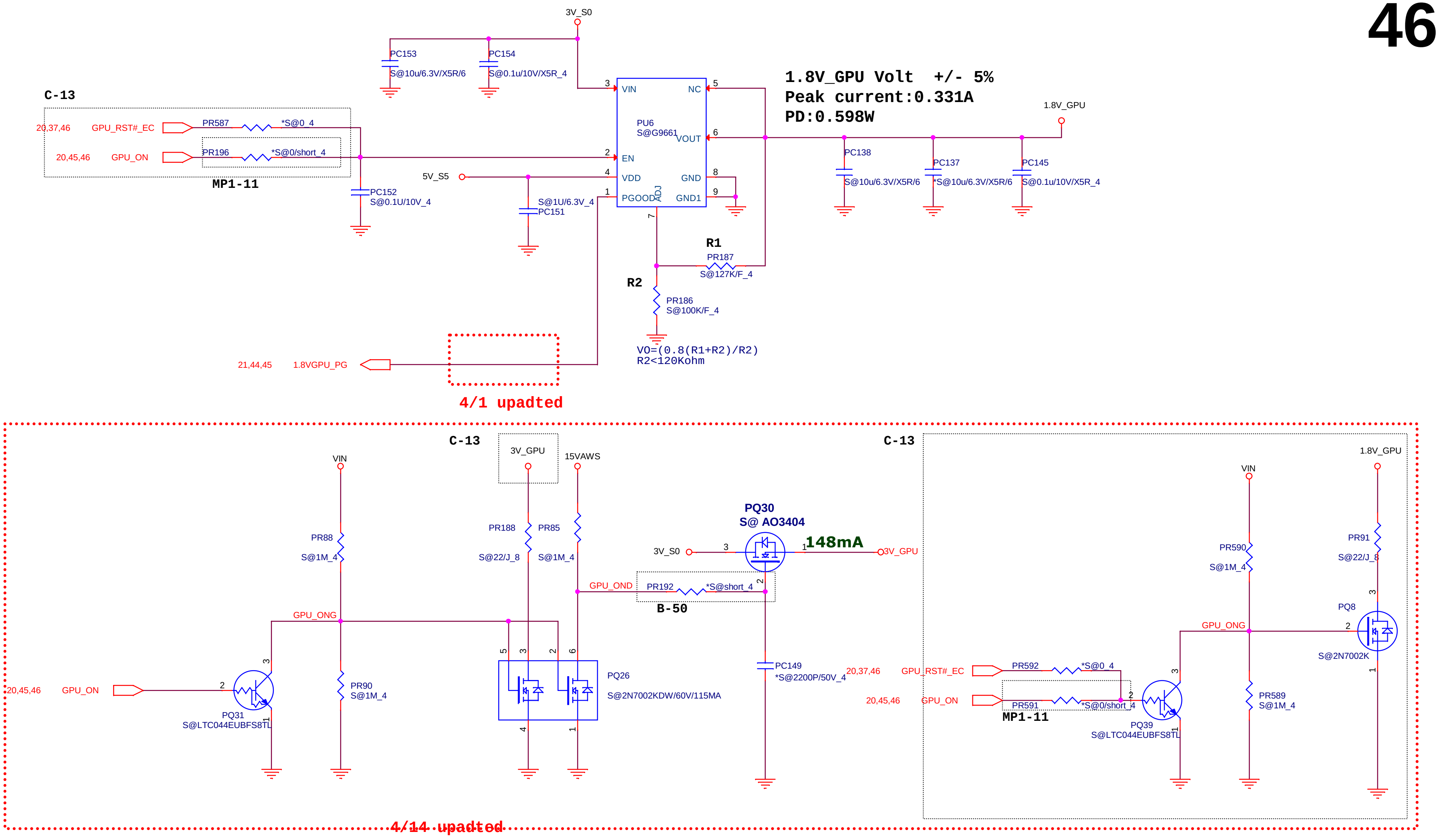


Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	1.5GPU/0.95_GPU(RT8068A)	2A

Date: Wednesday, November 19, 2014 Sheet 45 of 48

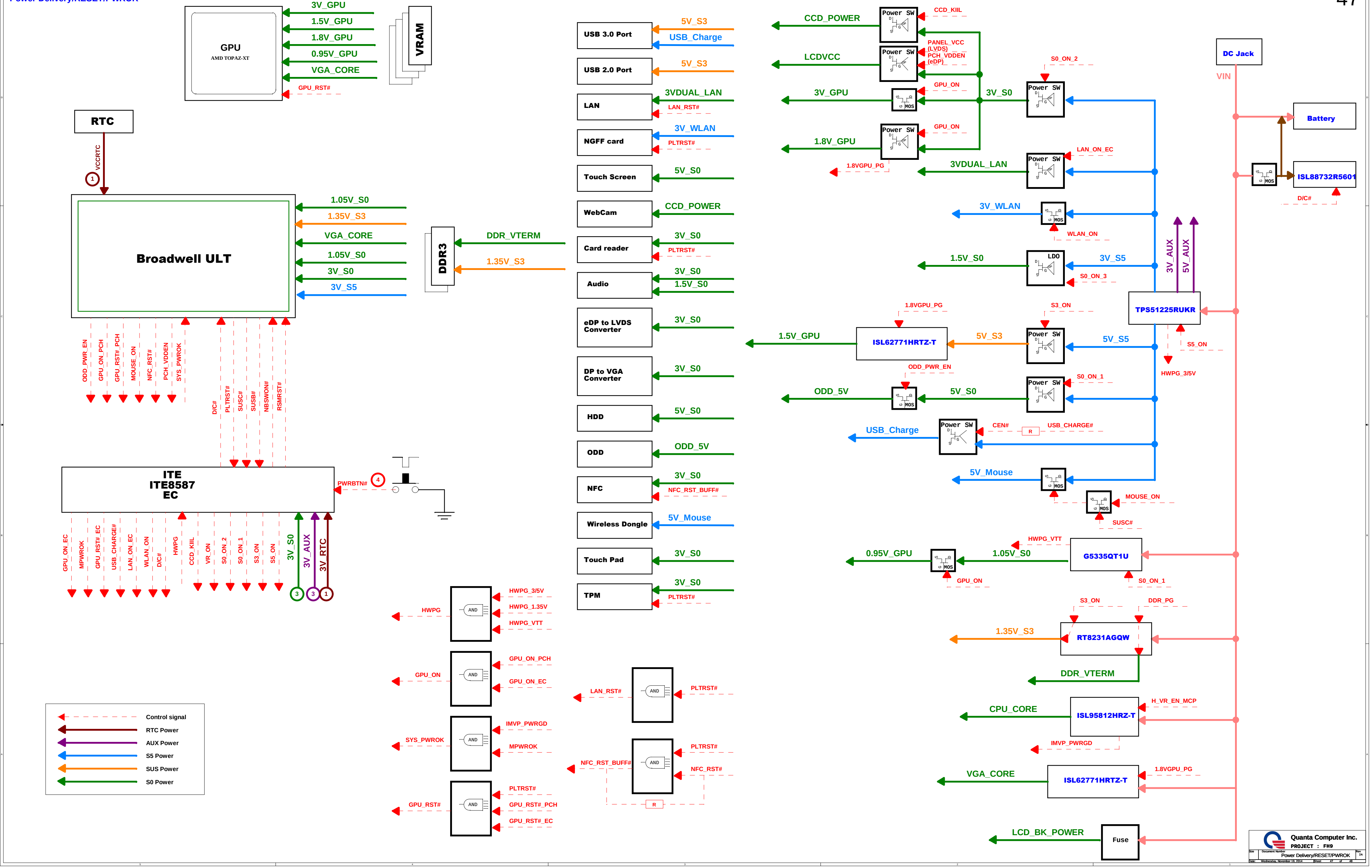


Quanta Computer Inc.

PROJECT : FH9

Size	Document Number	Rev
	1.8V_GPU&3V_GPU	2A

Date: Wednesday, November 19, 2014 Sheet 46 of 48


GPU
AMD TOPAZ-XT
3V_GPU
1.5V_GPU
1.8V_GPU
0.95V_GPU
VGA_CORE
GPU_RST#
VRAM
RTC
VCCRTC
Broadwell ULT
1.05V_S0
1.35V_S3
VGA_CORE
1.05V_S0
3V_S0
3V_S5
DDR3
DDR_VTERM
1.35V_S3
ODD_PWR_EN
GPU_ON_PCH
GPU_RST#_PCH
MOUSE_ON
NFC_RST#
PCH_VDDEN
SYS_PWROK
D/C#
PLTRST#
SUSC#
SUSB#
NBSWON#
RSMRST#
ITE
ITE8587
EC
PWRBTN#
GPU_ON_EC
MPWROK
GPU_RST#_EC
USB_CHARGE#
LAN_ON_EC
WLAN_ON
D/C#
HWPG
CCD_KIIL
VR_ON
S0_ON_2
S0_ON_1
S3_ON
S5_ON
3V_S0
3V_AUX
3V_RTC
Control signal
RTC Power
AUX Power
S5 Power
SUS Power
S0 Power
HWPG
HWPG_3/5V
HWPG_1.35V
HWPG_VTT
GPU_ON
GPU_ON_PCH
GPU_ON_EC
SYS_PWROK
IMVP_PWRGD
MPWROK
GPU_RST#
PLTRST#
GPU_RST#_PCH
GPU_RST#_EC
AND
USB 3.0 Port
5V_S3
USB_Charge
USB 2.0 Port
5V_S3
LAN
3VDUAL_LAN
LAN_RST#
NGFF card
3V_WLAN
PLTRST#
Touch Screen
5V_S0
WebCam
CCD_POWER
Card reader
3V_S0
PLTRST#
Audio
3V_S0
1.5V_S0
eDP to LVDS Converter
3V_S0
DP to VGA Converter
3V_S0
HDD
5V_S0
ODD
ODD_5V
NFC
3V_S0
NFC_RST_BUFF#
Wireless Dongle
5V_Mouse
Touch Pad
3V_S0
TPM
3V_S0
PLTRST#
LAN_RST#
PLTRST#
NFC_RST_BUFF#
PLTRST#
NFC_RST#
R
CCD_POWER
Power SW
CCD_KIIL
LCDVCC
PANEL_VCC (LVDS)
PCH_VDDEN (eDP)
3V_GPU
GPU_ON
MOS
1.8V_GPU
GPU_ON
1.8VGPU_PG
3V_S0
S0_ON_2
3VDUAL_LAN
LAN_ON_EC
3V_WLAN
WLAN_ON
1.5V_S0
LDO
3V_S5
S0_ON_3
1.8VGPU_PG
ISL62771HRTZ-T
1.5V_GPU
5V_S3
S3_ON
5V_S5
ODD_PWR_EN
ODD_5V
5V_S0
S0_ON_1
USB_Charge
CEN#
USB_CHARGE#
5V_Mouse
MOUSE_ON
SUSC#
DC Jack
VIN
Battery
ISL88732R5601
D/C#
3V_AUX
5V_AUX
TPS51225RUKR
S5_ON
HWPG_3/5V
0.95V_GPU
1.05V_S0
HWPG_VTT
G5335QT1U
GPU_ON
S0_ON_1
S3_ON
DDR_PG
1.35V_S3
RT8231AGQW
DDR_VTERM
CPU_CORE
ISL95812HRZ-T
H_VR_EN_MCP
IMVP_PWRGD
VGA_CORE
ISL62771HRTZ-T
1.8VGPU_PG
LCD_BK_POWER
Fuse
Quanta Computer Inc.
PROJECT : FH9
Power Delivery/RESET/PWROK

Change List

Item	Stage	Page	Owner	Change explanation
01	A->A+	36	FJ	delete R458, change SUSC# control for unstable when mouse_on is High SUSC# is LOW
02	A->A+	32	HW	change CN12 footprint to 50501-00801-001-8p-l
03	A->A+	34	HW	change CN21 footprint to 50501-0150n-001-15p-l
04	A->A+	36	HW	change CN9 FP to 50501-0120n-001-12p-l
05	A->A+	29	ESD	change L3~L6 PN to CY4500Q2Z00, F/P to qfn2-3_3x3_3-2_77 for ME hight limit
06	A->A+	23	HW	change L15 PN to CX5PX181000, F/P to f1x0_5-0_8 for DGS STD part
07	A->A+	38	PWR	change PJ1 F/P to bat-btd-08cabdab-8p-l for DFAD08MR071
08	A->A+	12,17,29 35,37	ESD	change D3,D4,D5,D6,D8,D16,D27,D28,D35 PN to BC512301Z02, F/P to d-1x0_6-0_6h for DGS STD part
09	A->A+	37	EE	exchange EC signal: GPU_ON_EC & FAN1_PWM for FAN DAC control
10	A->A+	28,32,34 35,36	EMI	exchange LP1~LP8 PN to CX12B900000, F/P to choke-dlw21s-4p for STD part
11	A->A+	32	ESD	change U37,U38,U40 PN to BC106506000, F/P to esd10-4_1x2-8-11p for STD part, reserve EC622~624 ,and DEL U14,U36
12	A->A+	23	EE	change L12,L13 PN to CX121T03000, F/P to RC0402 for STD part
13	A->A+	27	EE	change L22 PN to CX08T600000, F/P to RC0603 for STD part
14	A->A+	21	EE	change L27 to 0ohm_6 for AMD CRB no request
15	A->A+	26	EE	Change connection around D26 for solve when "5V_HDMI" to GND short, D26 will break at first
16	A->A+	26	EE	change D25 PN to BCRB500VZ29, F/P to DSM for STD part
17	A->A+	38	PWR	change PC7 F/P to CC0603
18	A->A+	12	EE	Delete D/C# to AC_PRESENT through R243, will cause D/C# lock unknow state.
19	A->A+	39	EE	change PR234 to 8.8K(CS38872FB18) to modify the OCP of 3V_S0
20	A->A+	10	EE	reserve R575,R576 for GREEN CLK & X'TAL option
21	A->A+	31	PWR	connect AU1.49 to GND for better disssipate heat
22	A->A+	43	EE	stuff PR165(CPU control), unstuff PR69(EC control),for CPU contol VR-EN power sequency
23	A->A+	41	EE	stuff PR210(DDR_PG control), unstaff PR209(S0_ON_1),for contol DDR_VTERM power sequency
24	A->A+	16	EE	unstuff C312 only reserve for WW15 4/10 Intel VCCDSW3 G3 can't boot issue.
25	A->A+	32	SMT	change C547 F/P to ECAP6_3X6_1-7_2 for solve SMT solder open easily issue
26	A->A+	26	EE	change L16,L18,L19 F/P to RC0402 for CVA6802JN17
27	A->A+	27	EE	reserve S0_ON_3 for control 5V_S0 to meet intel DGS power sequency
28	A->A+	34	EE	change PWR/B LED controled by PWRLED0#
29	A->A+	16	EE	reserve (R577, R578)1.5V_S0 for VCCHDA by intel :If the circuit is designed and configured for HD Audio VCCHDA should be connected to 3.3V or 1.5V
30	A->A+	31	EE	reserve Audio Codec DVDD-IO to 1.5V_S0 (AR22), default stuff AR27 (3V_S0)
31	A->A+	40	EE	reserve S0_ON_1(PR244) to control 1.05V_S0
32	A->A+	41	EE	reserve S0_ON_2(PR245,PR246,PR247) to control 1.5V_S0
33	A->A+	20	EE	reserve GPU_ON_EC(R579) to control GPU_ON directly
34	A->A+	31	EE	change CN20 F/P to 50501-00801-001-8p-l
35	A->A+	32	EE	change F5 P/N to DK300WFU007, F/P to f3_18x1_52-2_665
36	A->A+	10	EE	change D34 P/N to BCBAT54CZ01, F/P to sot323_213-2_1-1_3-bat54sw-7-f and delete D36 for DGS
37	A->A+	33	EE	change WLAN LED power source to 5V_S5 by FJ SPEC
38	A->A+	34	EE	change PWR/B LED power source to 5V_S3 by FJ SPEC
39	A->A+	39	PWR	change PR238 to 84.5K
40	A->A+	21	EE	add Topaz PS_3 bits strap table
41	A->A+	23	EE	Change L10,L23 PN to CX8PG121009 for RDC STD parts
42	A->A+	45	EE	un-stuff PC47, PR93, Stuff PR92(0.95V_GPU control by GPU_ON) for GPU power sequency.
43	A->A+	23	EE	DEL net alias BIF_VDDC. DEL VMEMIO power symbol for same net name.
44	A->A+	21	EE	unstuff R95,R85,R90,C159 for 3V_GPU leakage from EC
45	A->A+	39	EE	unstuff PR229,PR231,stuff PR232,PR228 for 3V_S0 have leakage level while AC is inserted
				B stage
1	A+->B	21,37	EE	delete R95, add Q33 on GPU_AC_BATT to avoid 3V_GPU leakage from EC. Change GPU_AC_BATT# net name to GPU_AC_BATT.Reserve R580 PU to 3V_S0 for GPU_AC_BATT. delete GPU_PROCHOT# control from EC and add GPIO as TP90, stuff C159, R85 to avoid 3V_GPU leakage from EC.
2	A+->B	16	EE	change +VCC_DSW net name to 3V_S5 for same net.
3	A+->B	40,42	EE	Stuff PR244, un-stuff PR201, 1.05V_S0 controled by S0_ON_1; stuff PR245,PR247, un-stuff PR246,PR222, 1.5V_S0 controled by S0_ON_2
4	A+->B	40,43	EE	Stuff PR244, un-stuff PR201, 1.05V_S0 controled by S0_ON_1; stuff PR245,PR247, un-stuff PR246,PR222, 1.5V_S0 controled by S0_ON_2
5	A+->B	31,37	PWR	Add AU3,AR28,AR29,AC40,AC41,AC42 for Audio codec sequence. EC add LDO enable pin AUD_1.5_ON.
6	A+->B	42	PWR	Add PR583,PR582 for S3_ON/S0_ON_2 PD for pulse issue.
7	A+->B	28	EE	un-stuff R1,R4,C1,U2, stuff R5 for LVDS BOM for H/W C/D.
8	A+->B	10,11,29	EE	un-stuff Y3,Y5,R359,R503,C456,C457,C520,C522; change R62 to RC0402 unstaff & add R581 for green CLK solution.
9	A+->B	9,10,11, 12,13,16, 17,18,19, 20,21,23, 28,29,30, 33,35,36, 37	EE	change 0 ohm to shrot pad for SMT rule: R120; R489,R355,R439;R438,R190,R420,R358,R484,R451, R444,R481,R482;R527,R188,R522,R497,R203,R531,R199,R525,R223;R449,R436,R141,R132,R178,R173,R410; R337,R196,R172,R508,R140,R116,R248,R182,R499;R253;R551;R548,R542;R381;R328,R98,R353,R360,R349, R332,R330,R105,R104;R342;L2,L1;R17,R16,R11,R12,R60;R573;R136,F3;R567,R568;R383;L17,R426,L14, R425,R404,R334,R361,R119.
10	A+->B	29	ME	change CN4 to 10pin (DFWF10MR004) for STD part
11	A+->B	34	ME	change CN2 to DFFC08FR031, F/P to 50501-00801-001-8p-l
12	A+->B	34	ME	change CN3 to DFFC06FR050, F/P to 88194-0641-6p-l
13	A+->B	35	ME	change CN6 to DFFC30FR093, F/P to 50696-0300m-001-30p-l, change CN8 to DFFC30FR093, F/P to 50696-0300m-001-30p-l
14	A+->B	21	EE	change C203,C208 to 10p for X'tal
15	A+->B	37	EE	change R343,R352 to 4.7K for EC sometime can not detect GPU thermal
16	A+->B	43	EE	Stuff PC125 for USB3.0 can't reconize device issue
17	A+->B	31	EE	un-stuff AR29,AC40,AU3,AC42, stuff AR30 for audio codec 1.5V power change to 1.5V_S0
18	A+->B	21	EE	un-stuff R346, Q17, stuff Q17 for GPU S3,S4 will wake up.
19	A+->B	37,42	EE	un-stuff PR242, add PR584, del PR243, change 5V_S0 control by S0_ON_1 , change EC S0_ON_3 to TP54
20	A+->B	36	EE	change C511 to 12p for X'tal
21	A+->B	37,42	EE	change 1.5V_S0 controled by S0_ON_3: ADD PR585, PR586
22	A+->B	43	EE	stuff PC119, PC122 for USB3.0 TSSC
23	A+->B	37	EE	Del EC EC_Board ID, change to TP90 for unuse pin.
24	A+->B	10	EE	stuff Q25 and add R582 for EC clear CMOS.
25	A+->B	11	EE	change R451,R444,R481,R418,R430,R483 to 33ohm for SPI signal waveform.
26	A+->B	38	PWR	change PJ2 pin define for FJ in common use
27	A+->B	31	PWR	change CN20 to 10 pin & add sleeve, ring2 pin for MIC cross talk issue
28	A+->B	35	EE	reverse CN8(low SKU) KB CON for ME change location form BOT to TOP
29	A+->B	28	EE	change HDMI level shifter to PS8407A for 4Kx2K eye diagram fail
30	A+->B	37	EE	ADD High SKU,LOW SKU BOARD ID for MMB
31	A+->B	40	PWR	PR206 change to 6.49K
32	A+->B	28,32	EE	change USB LP1,LP6,LP7,LP8,LP2 to 0 ohm for C/D
33	A+->B	23	EE	add 22uF(C621) for 1.5V_GPU ripple, add 470uF*2(C622,C623) for VGA_CORE ripple.
34	A+->B	08	BIOS	cahnge to GPIO46 reserve GPIO49 as SMI event control pin for more customer request function.
35	A+->B	44	PWR	cahnge PR155 to 200K ohm for VGA_CORE offset.
36	A+->B	28	EE	cahnge LCD conn power & signal pin define to avoid RTD2132 damaged.
37	A+->B	11	EE	change R213, R274 to 1K & R480, R465 to 499 ohm for NFC fast mode.
38	A+->B	11	EE	DEL Y3,C456,C457,R359,R367,R368 and ADD T54 for VCC_CORE layout spacing.
39	A+->B	31	PWR	Reverse CN20 pin define for typo.
40	A+->B	26	EE	change EC16,EC17,EC18,C237,C242,C256 to 5p for VSIS fine-tuned.
41	A+->B	43	PWR	change PR167 to 105K(CS41053F919) for Imon adjustment
42	A+->B	34	EE	change CN3 FP to 50506-00641-v01-6p-l
43	A+->B	16	EE	follow PDG:change C444,C448,C445,C452 22F, unstuff C443,C446,C449,C454
44	A+->B	36	ME	change H16 FP to H-FH8-2
45	A+->B	35	ME	change CN5 to DFHD10MS119 and reverse pin define.
46	A+->B	41	PWR	Change PL18 to CV-10M0MZ02 for Standard part
47	A+->B	42	PWR	change CN20 for SCH & BRD pindefine not mactch.
48	A+->B	36	ME	change H16 FP back to H-TC256BC185D146P2, H26 to H-FH8-2, H3 to H-TC181BIC102D102P2, H4,H8,H15,H20 to H-C315D126P2, H9 to H-TC315BC236D126P2, H10 to H-TC315BC217D110P2, H14 to H-FH8-3, H29 to H-O181X173D102X94P2,H32 to H-TC315BC394D126P2, H31 to H-TC197BC256D150P2, H33 to H-C394D126P2, H34 to H-C394D126P2, for layout
49	A+->B	36	ME	change H18 FP to H-FH8-4, H21 to H-FH8-6, H27 to H-FH8-5, H30 to H-FH8-7
50	A+->B	39,40,41 42,43,45 46,44,32 29	EE/PWR	change PR98,PR213,PR205,PR200,PR239,PR210,PR225,PR185,6P,R63,PR64,PR66,PR165,PR71,PR74,PR132 PR31,PR196,PR192,PR84,PR92,PR35,PR145,PR144,PR143,PR141,PR43,R532,R533,R534,R535,R267,R269 R267,R502,R500,R310,R68 to short PAD
51	A+->B	39	PWR	change PC50, PC51 to 0.1uF/0402
52	A+->B	31	PWR	unstuff AR13,AR14,AC23,AC24,AC25,AC32,AC39 for audio noise.
53	A+->B	34,35	ME	change PWR CONN(CN3) to DFFC06FR106 , High SKU KB CON(CN6) to DFFC30FR091
54	A+->B	34	EE	Del TP83,TP84,TP85,TP86,TP87,TP88
55	A+->B	31	EE	change to short pad: AR17,AR18,AR19,AR27,R289,R288,R30,R32
56	A+->B	28	EE	change HU1 to PS8201A & R221 to 3.3K ohm for C/D
57	A+->B	31	PWR	change AQ1,AQ5 F/P to sot323_213-2_1-1_3-1_1h
58	A+->B	36	ME	Del H17
59	A+->B	36	ME	change H9 F/P to H-TC315BC276D126P2, H10 to H-TC335BC217D110P2
60	A+->B	39	PWR	change PU11 to TPS51225CRUKR(AL051225001) for MMB
61	A+->B	38	EMI	reserve EC625~EC630 for EMI
62	A+->B	30	EE	change C609 to 10uF for vender suggest.
63	A+->B	29	EE	Unstuff C421 & C427 for vender suggest
64	A+->B	38	PWR	Del EC14 for ME request
65	A+->B	36	ME	change H31 F/P to h-tc217bc256d150p2
66	A+->B	36	ME	change H31 F/P to h-tc197bc256d150p2
67	A+->B	26	EE	change R371 & R401 to 2.2K for verder suggest.
68	A+->B	13	EE	stuff R454,R435,U30,C487,C499; un-stuff R453,Q23,C495; change R448 to 10k ohm for VCCST_PWRGD to VR_EN timing.
69	A+->B	11	EE	change R474,R463 to 33 ohm, R451,R444,R481 to 0 ohm for SPI signal quilty.
				C stage
1	B->C	10	EE	unstaff R582 for PDTC144EU already have internal PD.
2	B->C	34	ME	Change CN3 to DFFC06FR050 for ASSY. line request ME change connector type.
3	B->C	33	EE	change R285,R278,R282,R280,R286,R287 to 150 ohm, R281,R279 to 220 ohm for LED brightness.
4	B->C	32	EE	change F5 to DK260TPU003, F/P to f1812 for STD parts.
5	B->C	35	ME	change CN8 to DFFC30FR091, F/P to 50541-0300n-001-30p-l for ASSY. line request.
6	B->C	37	EE	swap U27 AMP_MUTE# & CLR_CMOS (pin 108 & 2) for G3 boot to S0 will have a pluse to clear CMOS.
7	B->C	34	EE	change CN3 F/P to 50506-00641-v01-6p-l for DGS.
8	B->C	26	EE	change EC16,EC17,EC18,C237,C242,C256 to 2pF for VSIS.
9	B->C	13	EE	change R449,R436 to 0ohm and un-stuff, R454, R435 to short PAD for reducing 0ohm.
10	B->C	16	EE	change R337 to 0 ohm from short pad for follow intel CRB add 0ohm.
11	B->C	37	EE	change D24 direction for ME can't unlock issue
12	B->C	28	EE	change JLCD1 F/P to 51519-04001-001-40p-L for DGS change

Item	Stage	Page	Owner	Change explanation
13	B->C	44,45,46	EE	for reserve EC control GPU power sequence: PR92 change to 0ohm un-stuff, PR93 change to 0ohm stuff. PR196 change to 0ohm stuff. reserve PR587 for GPU_RST#_EC control. add dis-charge SCH for option. PR31 change to 0ohm and reserve PR588 for GPU_AC_BATT control 1.5V_GPU. PR35 change to 0ohm stuff, VGA_CORE reserve control 0.95_EN change to GPU_AC_BATT.
14	B->C	32	EE	stuff U37,U38,U40 for USB3 ESD solution
15	B->C	36	ESD	change H20 F/P to H-C315IC285D126P2for ESD request.
16	B->C	45	EE	reserve PR593 PU to 3V_GPU.
17	B->C	36	ME	change H31 F/P to H-TC236BC185D146P2, H11,H19 to H-TC217BC185D146P2 , H31 to H-TC256BC197D150P2 for ME change
18	B->C	36	ME	change H13 F/P to H-TC217BC185D146P2 for ME change.
19	B->C	36	ME	change H20 F/P to H-C315IC250D126P2 for ME change.
20	B->C	34,35,36	EE	change R380,R379,R290,R291,R441,R442 to short pad, un-stuff LP3,LP4,LP5 for C/D.
21	B->C	28	EE	change HU1 to PS8407A and R221 to 4.99Kohm for HDMI EA item 7-10
22	B->C	38	EMI	Reserve EC38, EC39(10u/25V) on CS_IN
23	B->C	16	EE	Change the cap's value of C265,C273,C257,C251,C451,C455 from 4.7U/6.3V_4 to 47U/4V_6 And del C290, C252, C450 for meet Intel DG suggestion
24	B->C	28	EE	cahnge F1 to DK200UFU002 for PDC suggest DGS.
25	B->C	31	PWR	change AR12,AR25 to 0ohm, AL6,AL7 to 47ohm for pop noise.
				MP1 stage
01	C->D	10	EE	R506 change short PAD from 0 ohm for cost down
02	C->D	11	EE	R432 change short PAD from 0 ohm for cost down
03	C->D	16	EE	R578 change short PAD from 0 ohm for cost down
04	C->D	34	EE	R466 change short PAD from 0 ohm for cost down
05	C->D	42	PWR	PR194/PR195/PR584/PR241/PR586/PR585 change short PAD from 0 ohm for cost down
06	C->D	41	PWR	PR216 change short PAD from 0 ohm for cost down
07	C->D	39	PWR	PR221/PR232/PR227/PR228 change short PAD from 0 ohm for cost down
08	C->D	31	ADO	AR1/AR2/AR3/AR4/AR30 change short PAD from 0 ohm for cost down
09	C->D	38	PWR	PR117/PR7 change short PAD from 0 ohm for cost down
10	C->D	40	PWR	PR203/PR244 change short PAD from 0 ohm for cost down
11	C->D	46	PWR	PR591/PR196 change short PAD from 0 ohm for cost down
12	C->D	45	PWR	PR29/PR31/PR93 change short PAD from 0 ohm for cost down
13	C->D	44	PWR	PR40/PR140/PR35/PR160/PR56/PR55/PR61 change short PAD from 0 ohm for cost down
14	C->D	36	ME	CN9 change PN to DFFC12FR117 & DFFC12FS000 , and F/P to 50501-01201-001-12p-l for ME request.
15	C->D	32,34	ME	CN2,CN12 change PN to DFFC08FR093 & DFFC08FR055,F/P to 50501-0080n-001-8p-l for ME request.
16	C->D	31	ME	CN20 change PN to DFFC10FR123,F/P to 51619-0100n-001-10p-l for ME request.
17	C->D	34	ME	CN21 change PN to DFFC15FR010 & DFFC15FR013, F/P to 50501-01541-001-15p-l for ME request.
18	C->D	36	ME	H11,H19 change PN to FBAJ2003010 for ASSY request.
19	C->D	34	ME	CN3 change PN to DFFC06FR177 & DFFC06FR172,F/P to 50506-0060n-v01-6p-l for ME request
20	C->D	35	ME	CN22 add 2nd source PN DFFC06FR179 for ME request
21	C->D	35	ME	CN5 change to DFHD10MS236 & DFHD10MS235 for ME request
22	C->D	36	ME	CN4 change to DFHD10MS237 & DFHD10MS238, F/P to 50273-01001-001-10p-l for ME request
23	C->D	40	EE	PU8 del pin24.25 for layout symbol change
24	C->D	30	EE	CN1 DFHD11MR028 EOL, change to DFHD11FR163
25	C->D	35	EE	CN17 change to DFHS12FS032,F/P to 50169-01241-002-12p-ldh for SMT add Mylar