COMPAL CONFIDENTIAL

MODEL NAME : CAZ20
PCB NO : LA-E132P
BOM P/N : 431A4431L0X

Steamboat 14" NonAR

Kabylake U

2016-11-09
REV : 1.0 (A00)

@ : Nopop Component

EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)
GT3@ : KBL-U 2+3e Component
INFI@ : Infinity SKU Component

MB PCB

Part Number	Description
DA800189010	PCB 1S1 LA-E132P REV0 MB NON-AR 1

Layout Dell logo

REV:A00
PWB:

Power CKT : 1107

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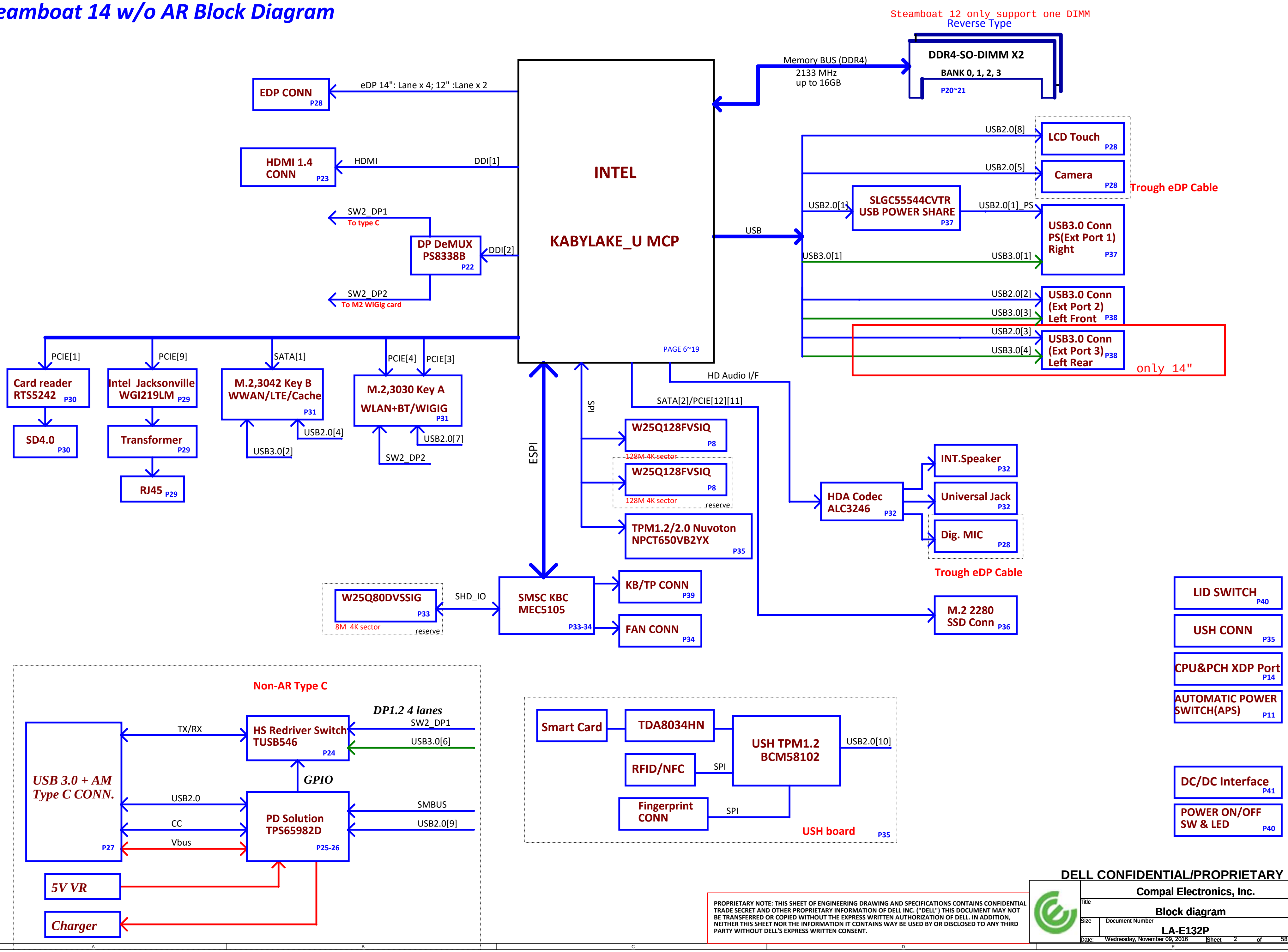
Steamboat 14 w/o AR Block Diagram



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Block diagram

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NonAR config

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

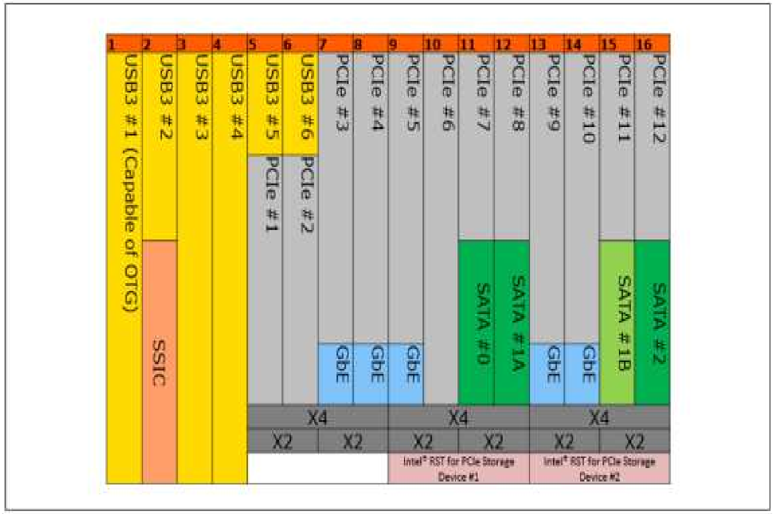
power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader (PCIE)
USB3.0-6		PCIE-2		Type-C Port
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	NA
		PCIE-8	SATA-1	M.2 3042(SATA Cache)
		PCIE-9		LOM
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

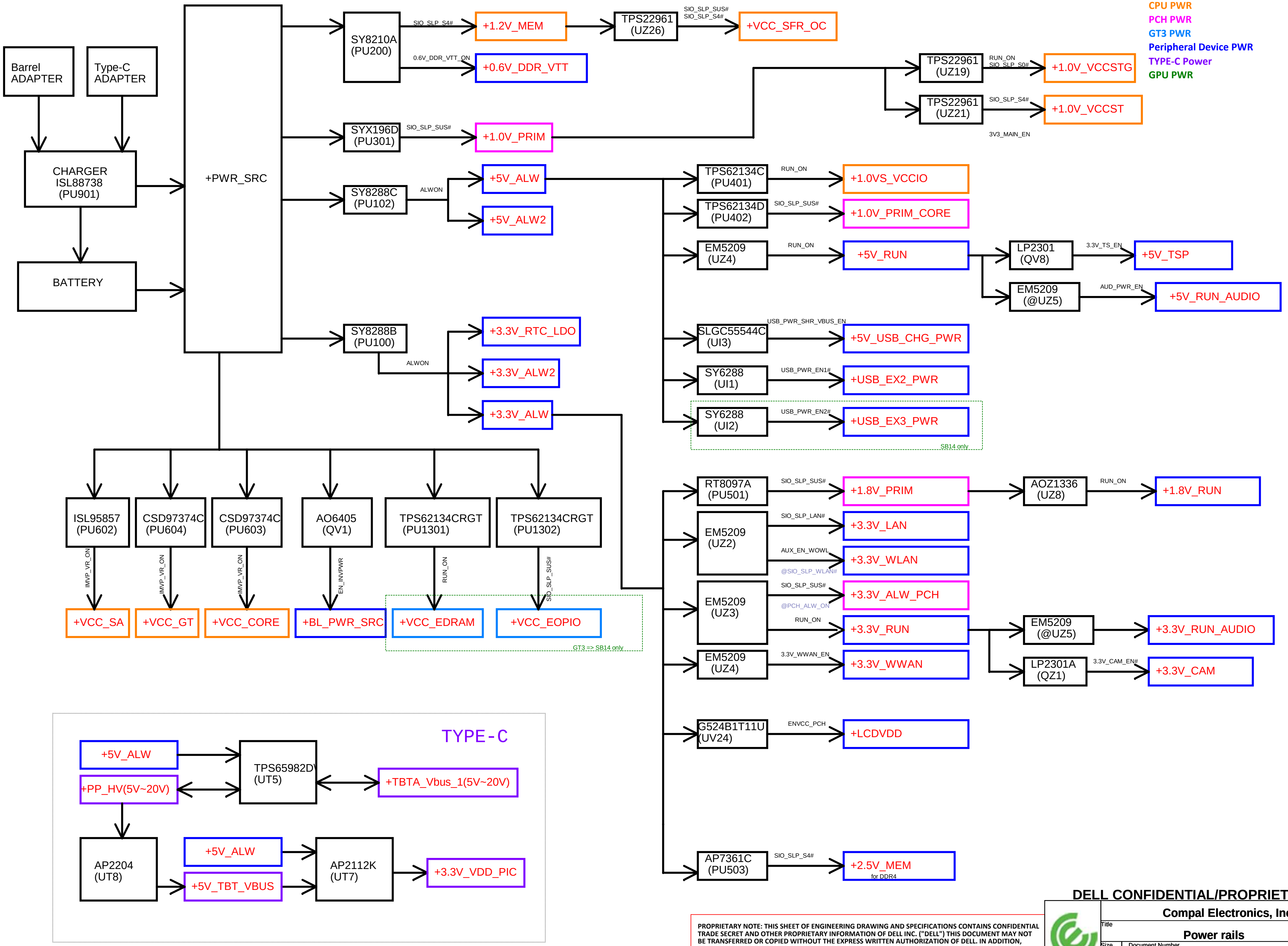
USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	Type-C Port
10	USH

High Speed I/O (HSIO) Lane Multiplexing in KBL U



Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm ± 10%)			39.4		41.40000
					1.05156

AR use 1086PP
Non AR use 1080PP



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Power rails

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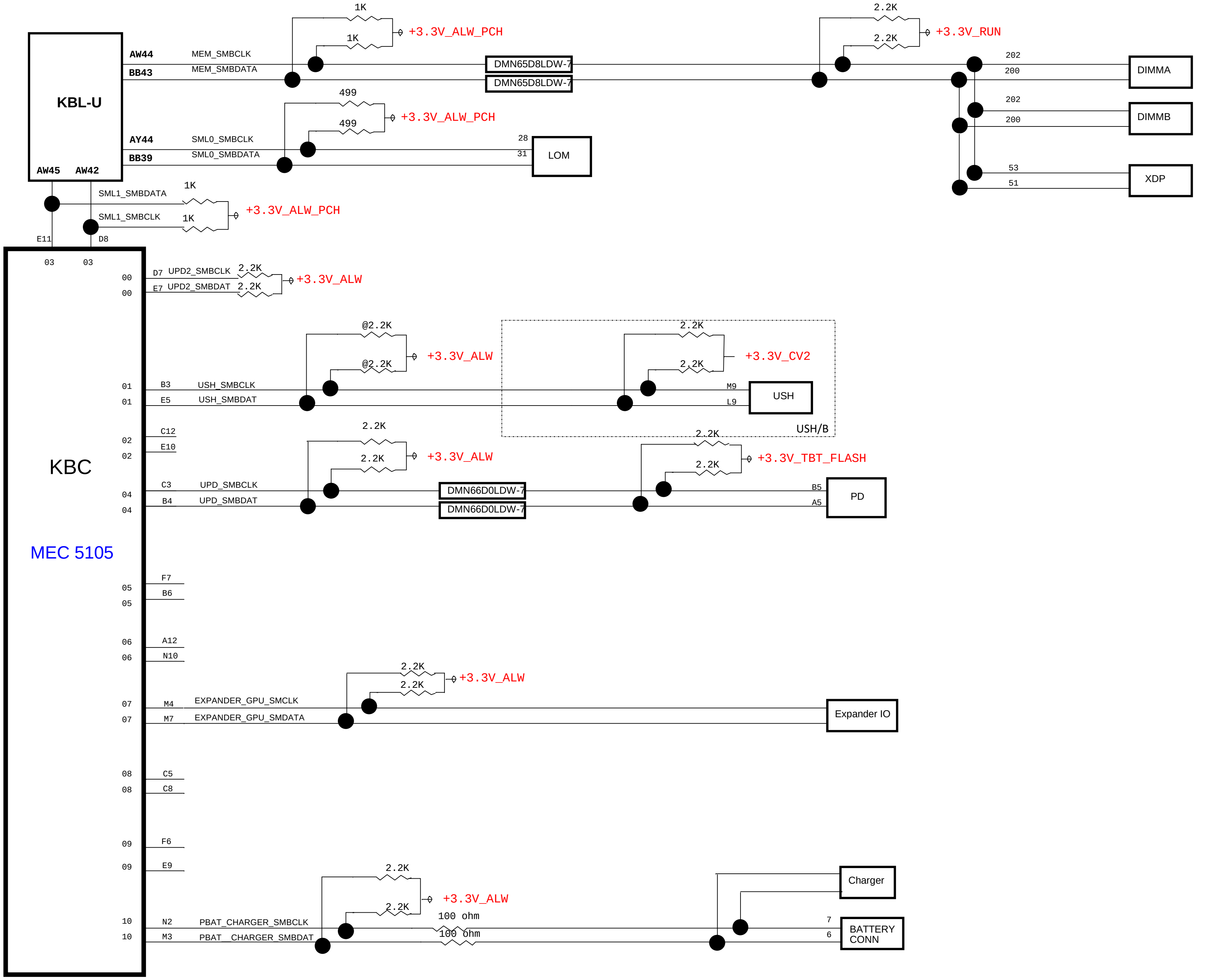

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Port assignment

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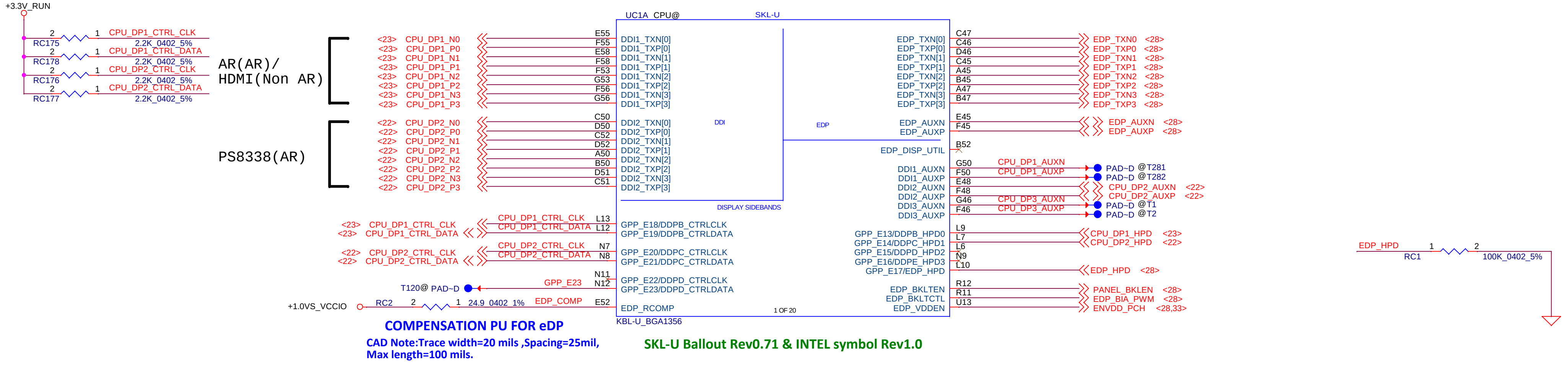
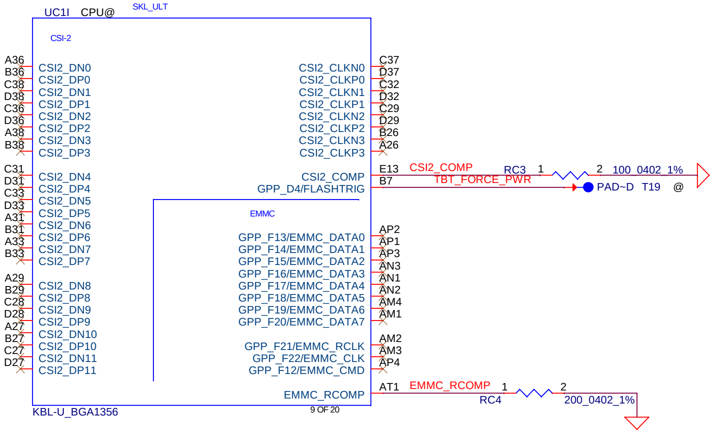


COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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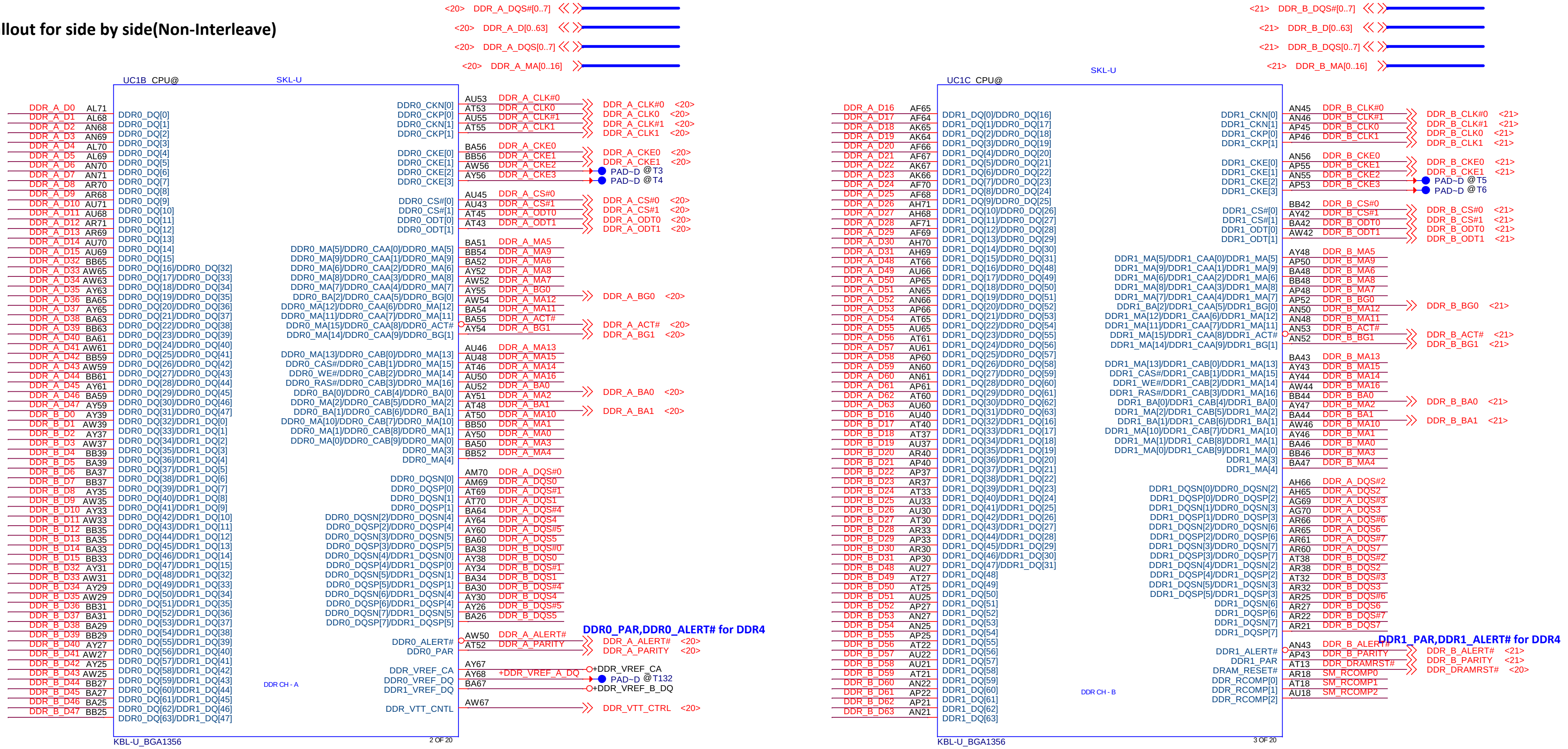
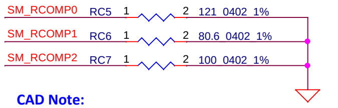
For DDR4

DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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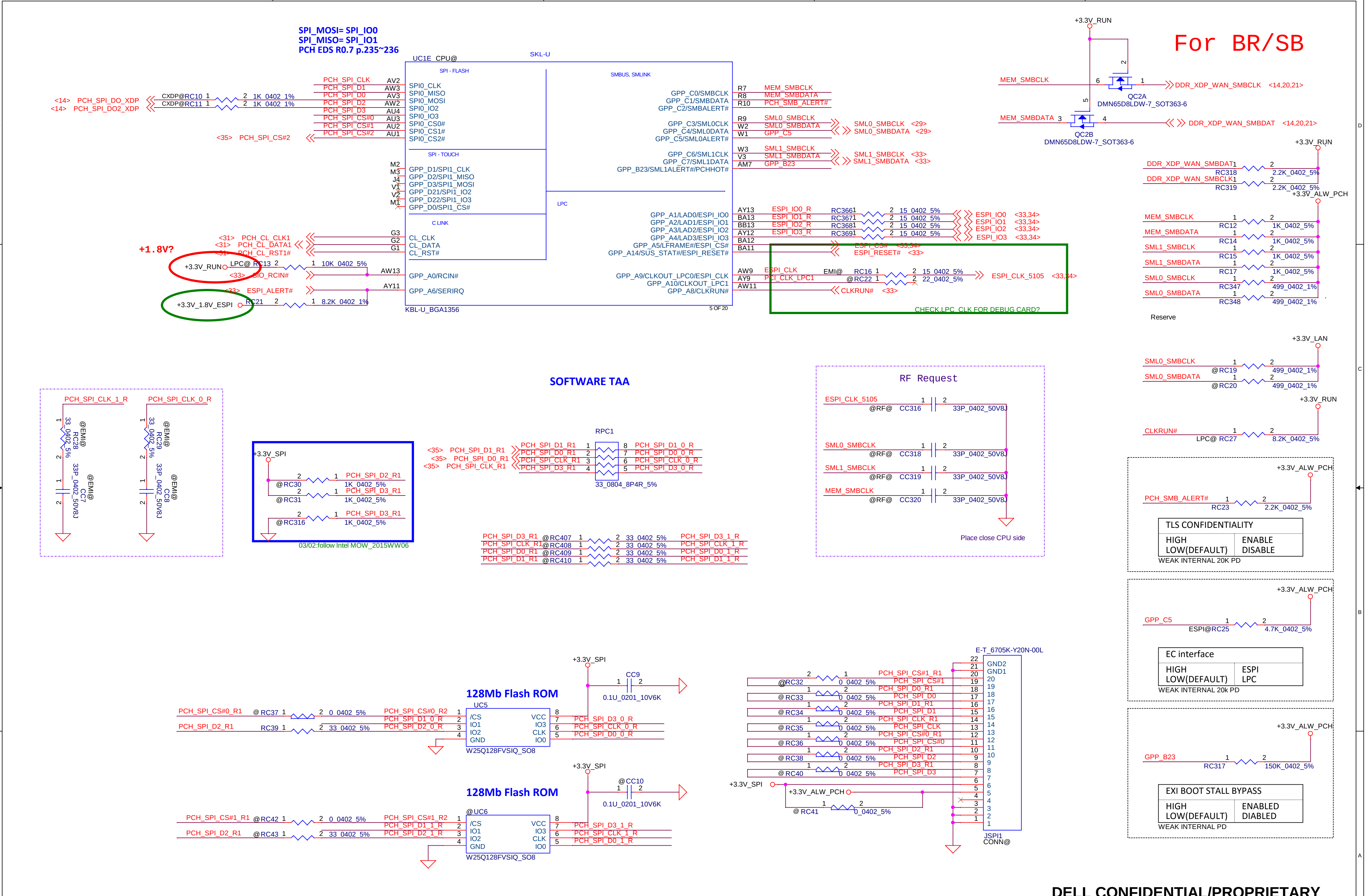

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

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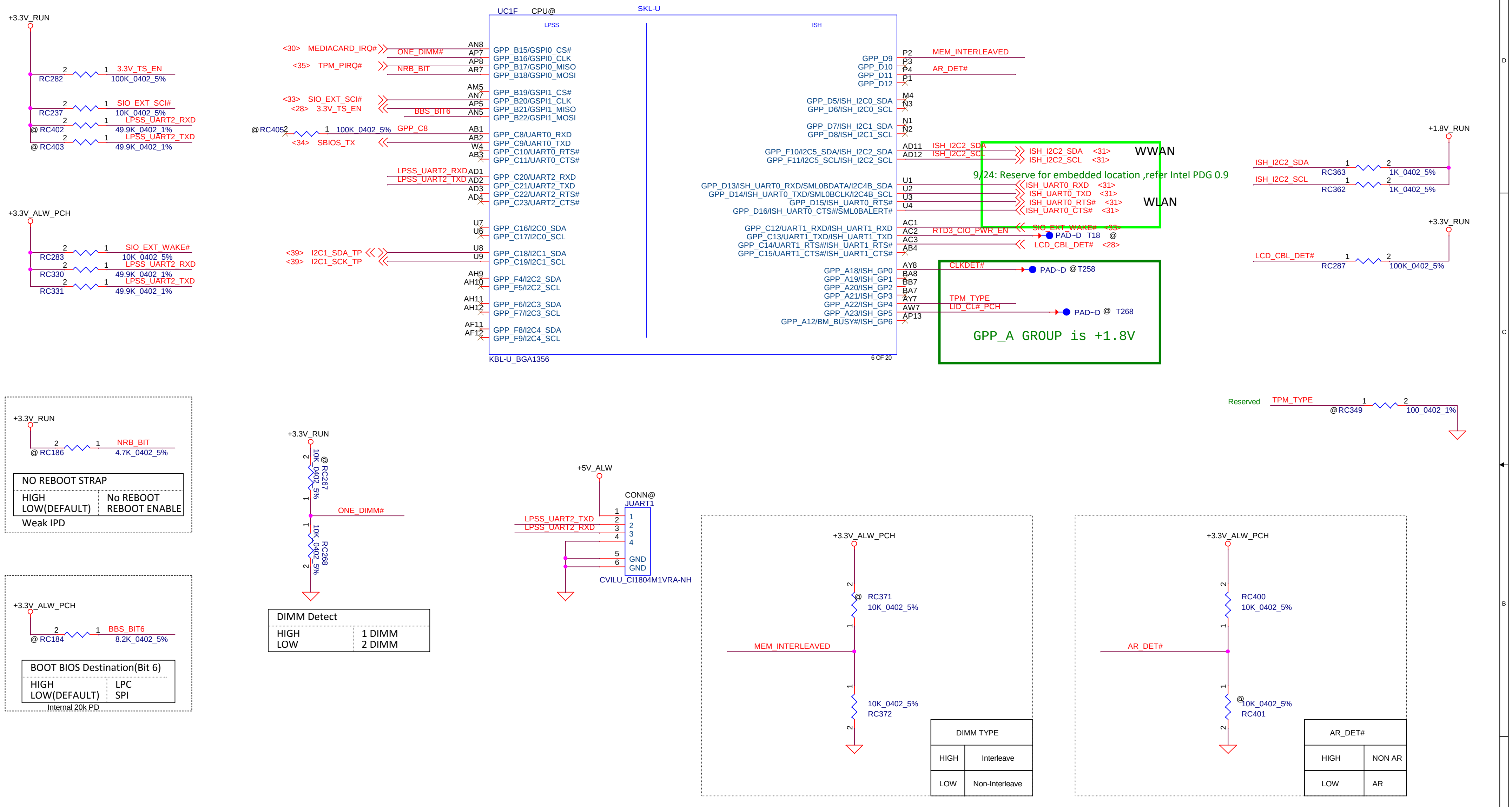
For BR/SB



NO REBOOT STRAP	
HIGH LOW(DEFAULT)	No REBOOT REBOOT ENABLE
Weak IPD	

DIMM Detect	
HIGH LOW	1 DIMM 2 DIMM

BOOT BIOS Destination(Bit 6)	
HIGH LOW(DEFAULT)	LPC SPI

DIMM TYPE	
HIGH	Interleave
LOW	Non-Interleave

AR_DET#	
HIGH	NON AR
LOW	AR

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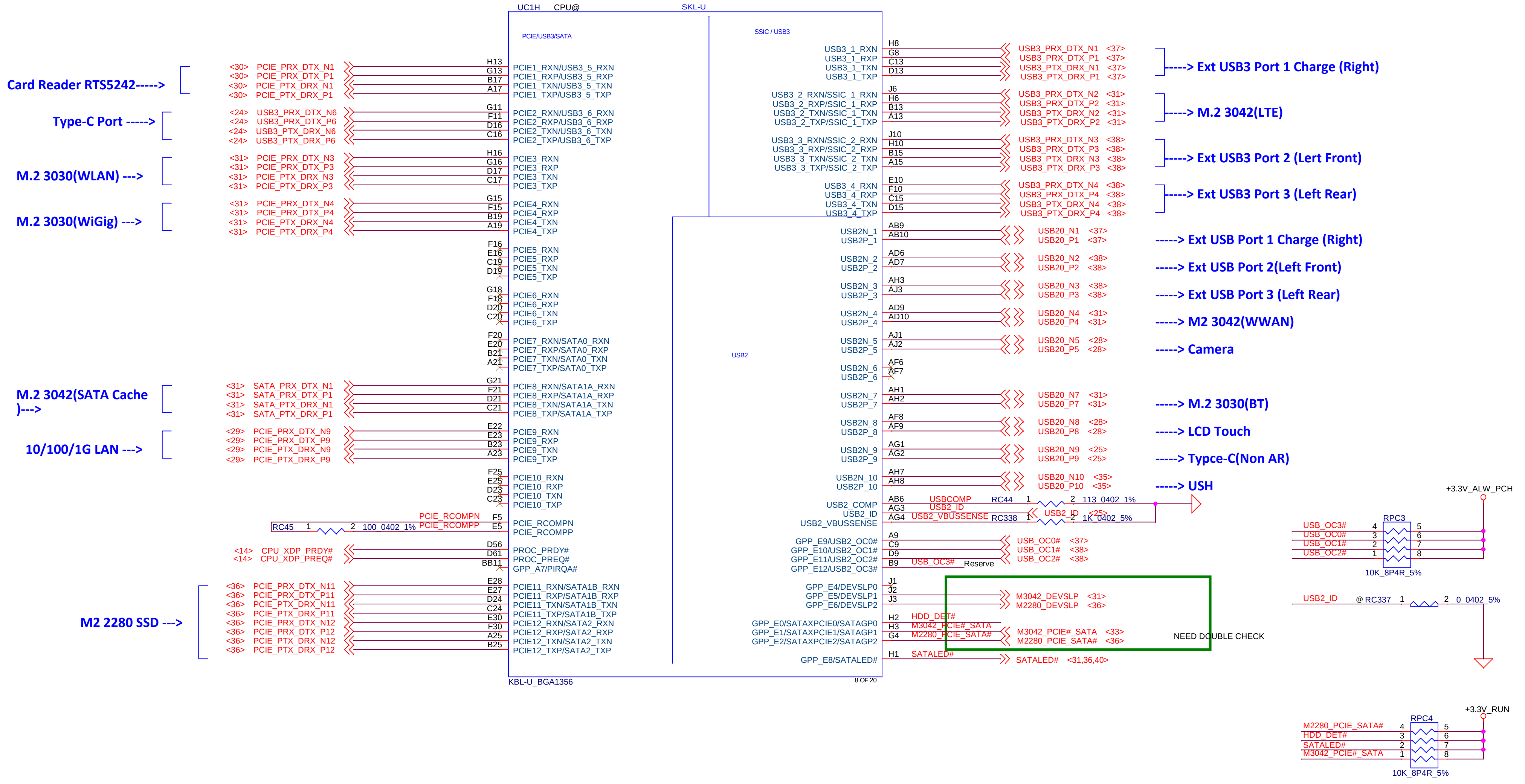
For NON AR, Steamboat



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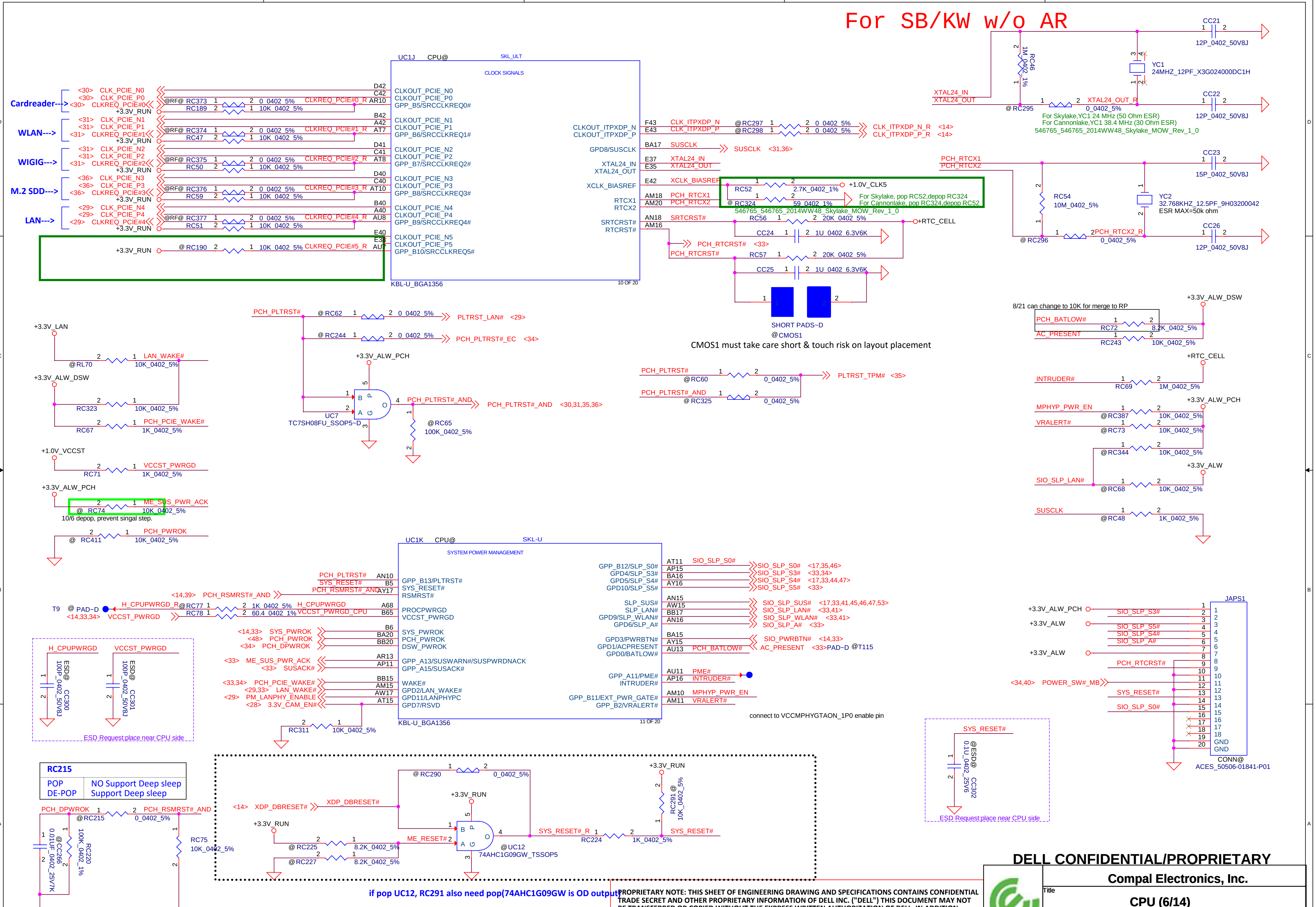

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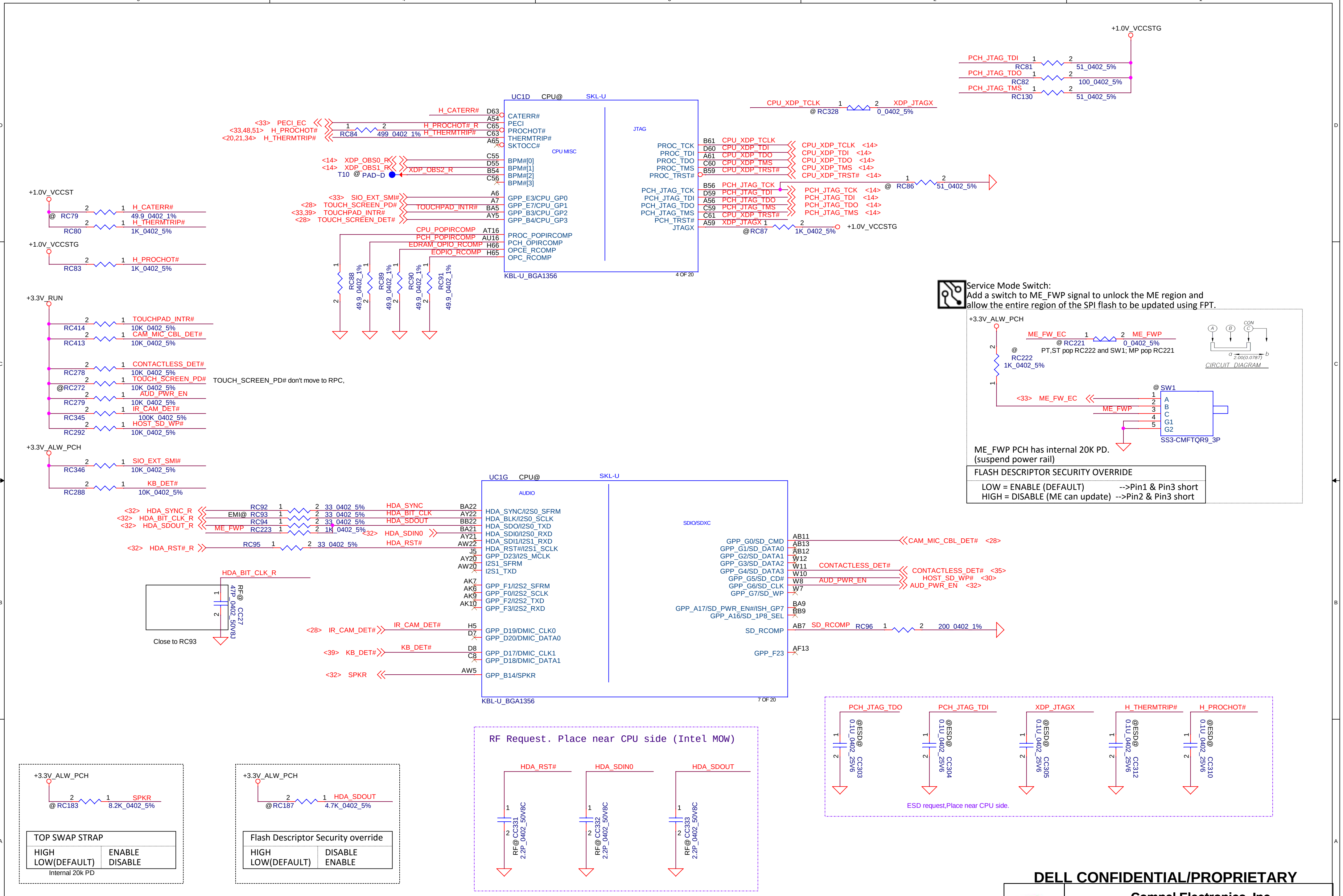

TOUCH_SCREEN_PD# don't move to RPC,

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.

PT,ST pop RC222 and SW1; MP pop RC221

ME_FWP PCH has internal 20K PD.
(suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

Close to RC93

RF Request. Place near CPU side (Intel MOW)

ESD request,Place near CPU side.

TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Internal 20k PD

Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

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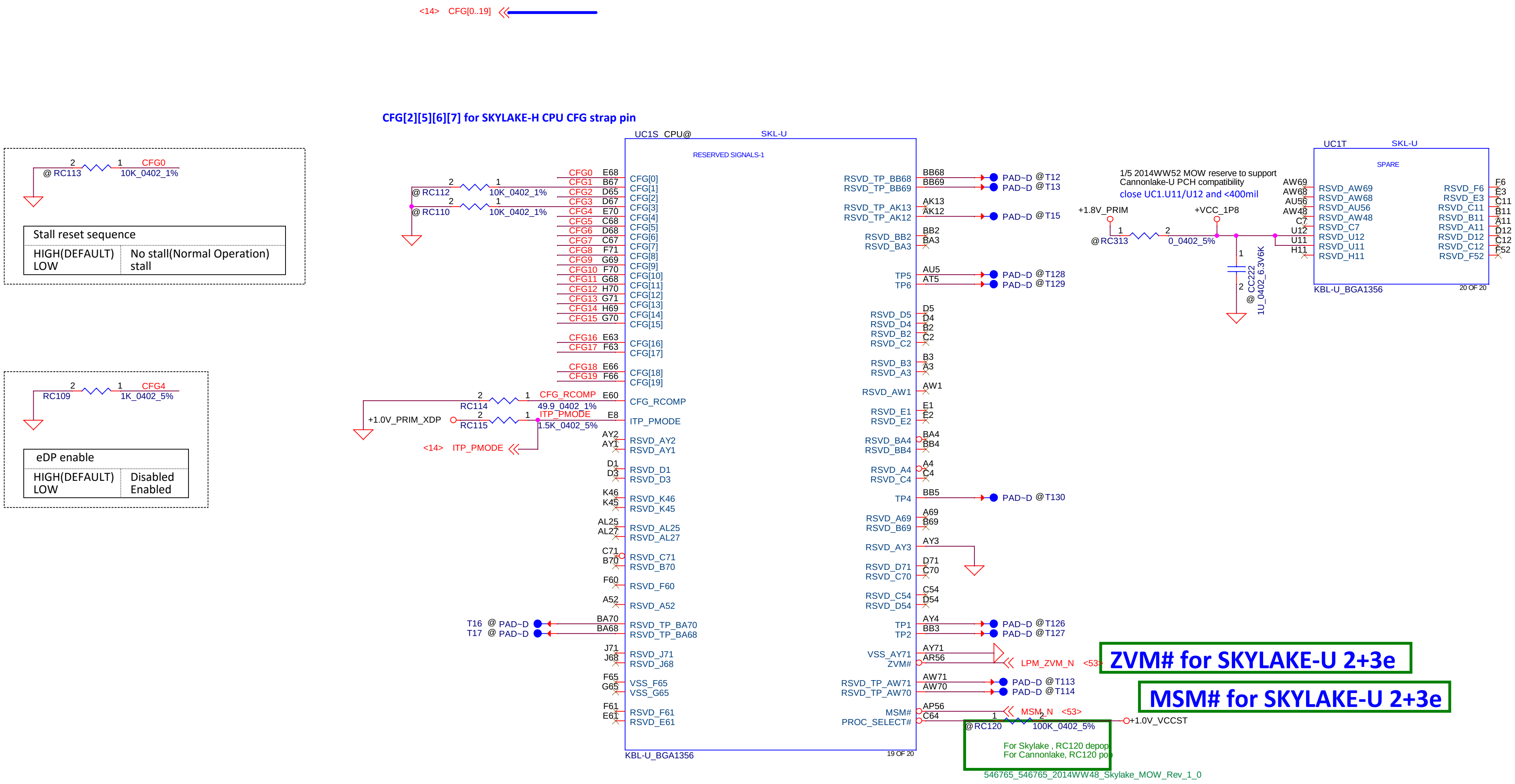

CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin

Stall reset sequence	
HIGH(DEFAULT) LOW	No stall(Normal Operation) stall

eDP enable	
HIGH(DEFAULT) LOW	Disabled Enabled

1/5 2014WW52 MOW reserve to support
Cannonlake-U PCH compatibility

close UC1.U11/U12 and <400mil

ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

For Skylake , RC120 depop
For Cannonlake, RC120 pop

546765_546765_2014WW48_Skylake_MOW_Rev_1_0

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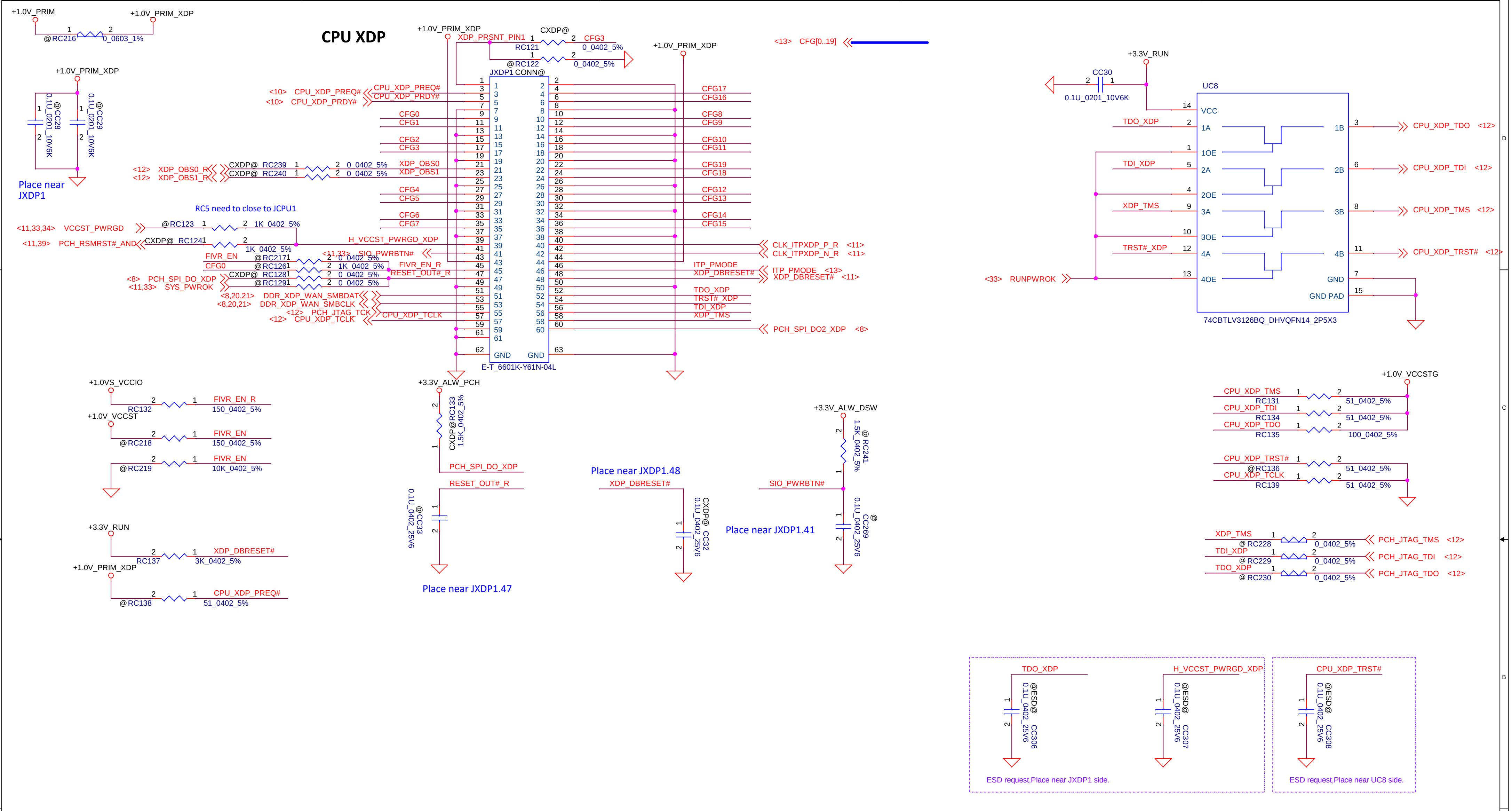

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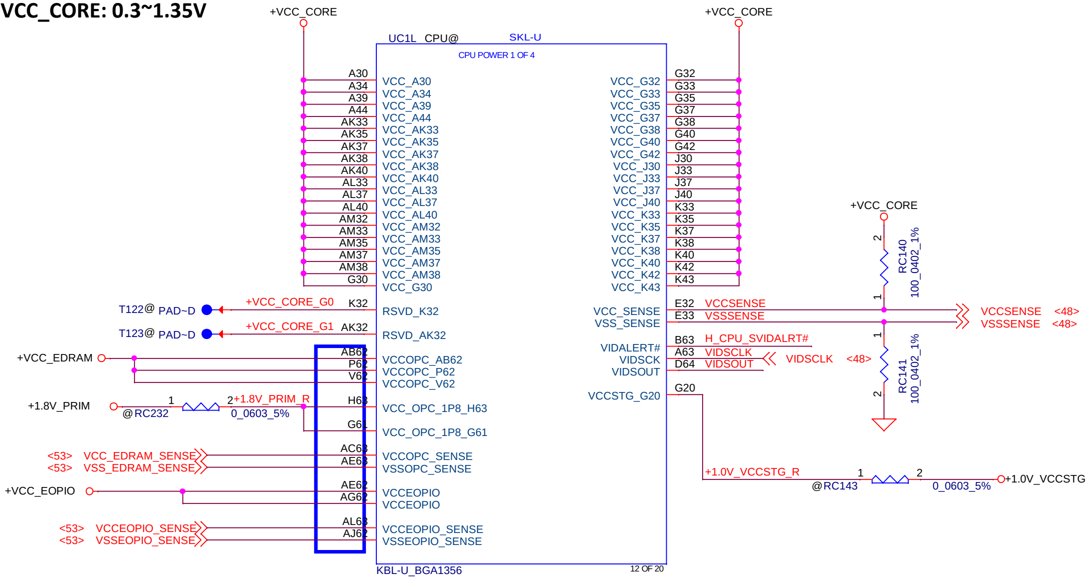
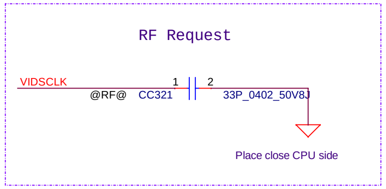
+VCC_CORE: 0.3~1.35V

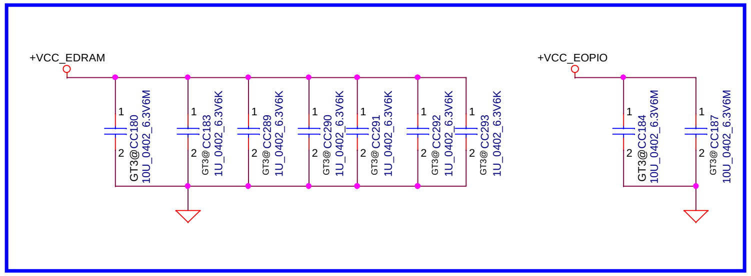
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

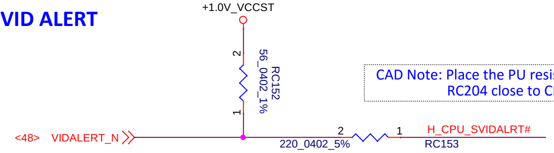


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)



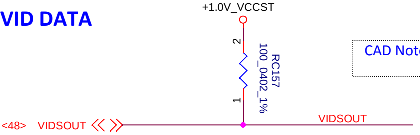


SVID ALERT



CAD Note: Place the PU resistors close to CPU
RC204 close to CPU 300 - 1500mils

SVID DATA



CAD Note: Place the PU resistors close to CPU
RC208close to CPU 300 - 1500mils

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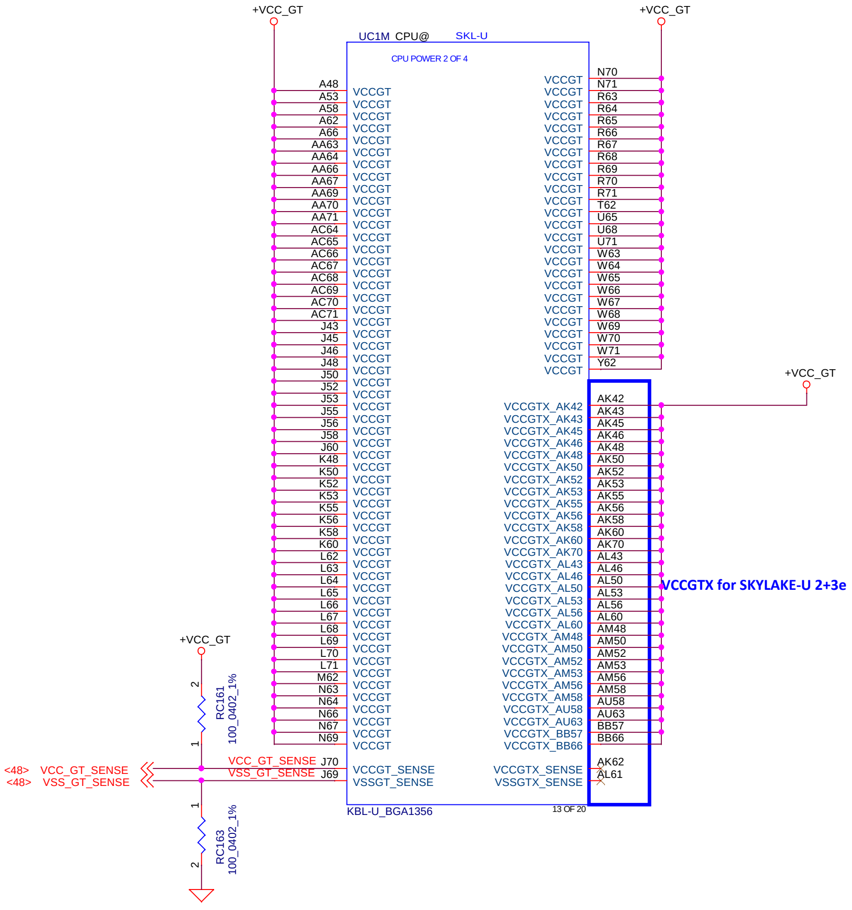
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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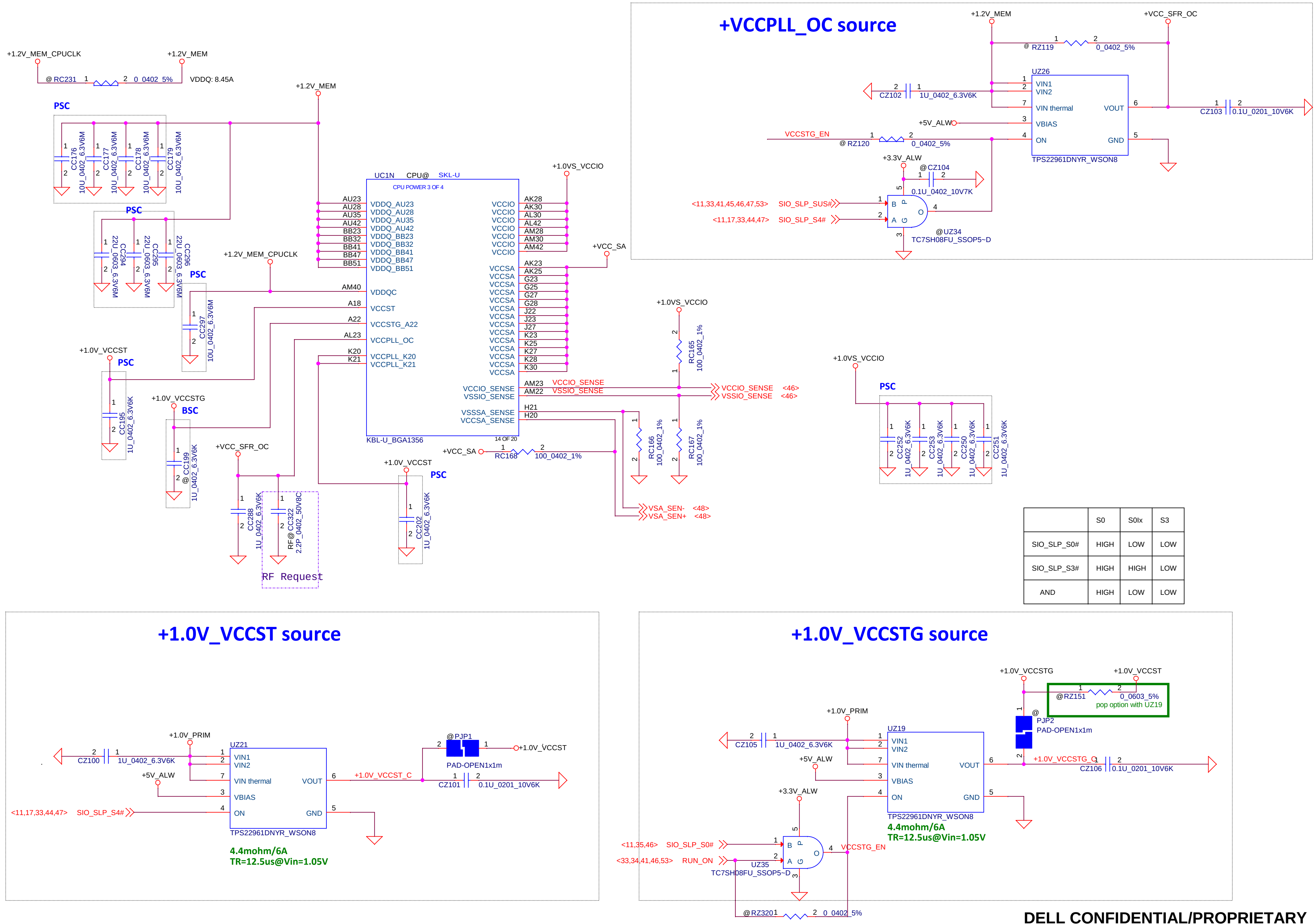

	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

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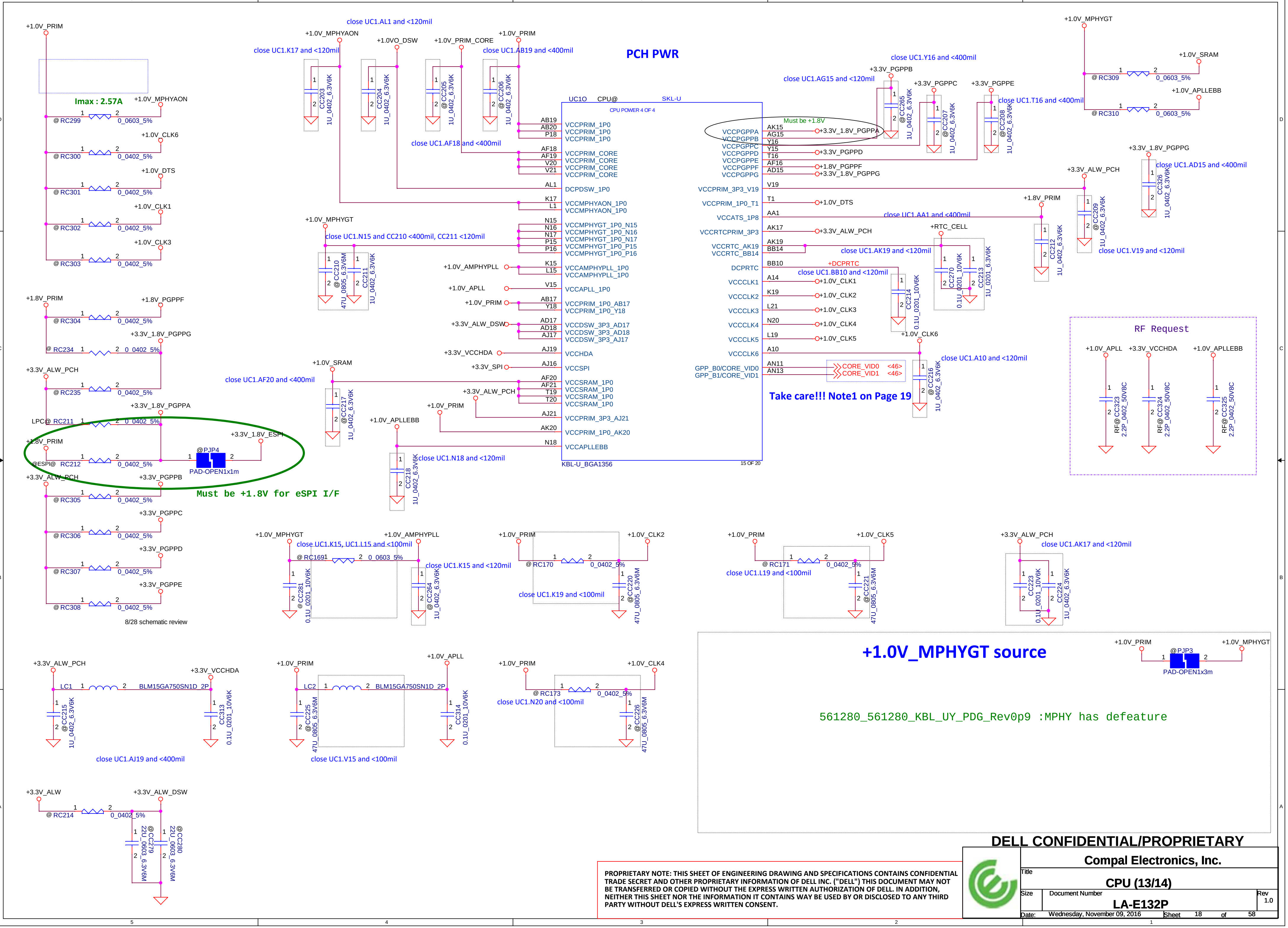

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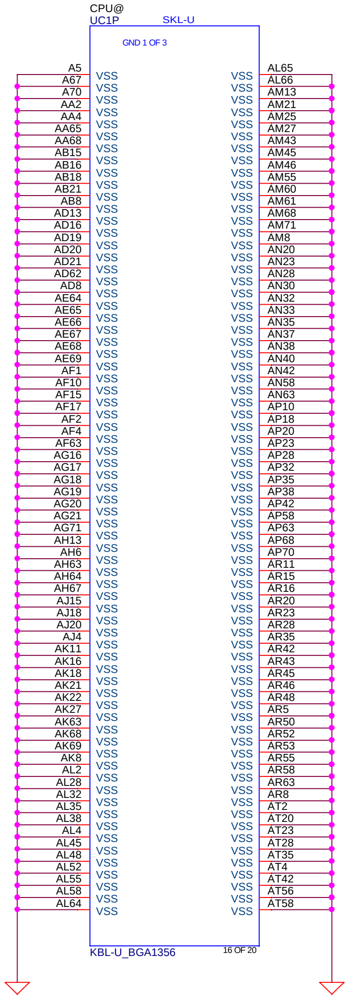
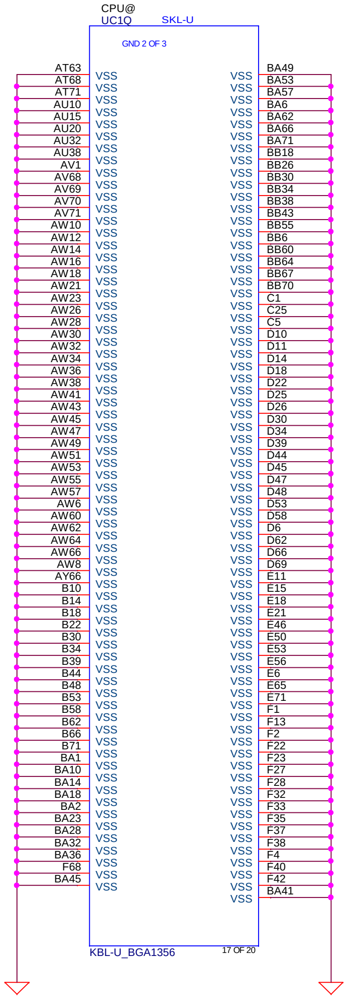
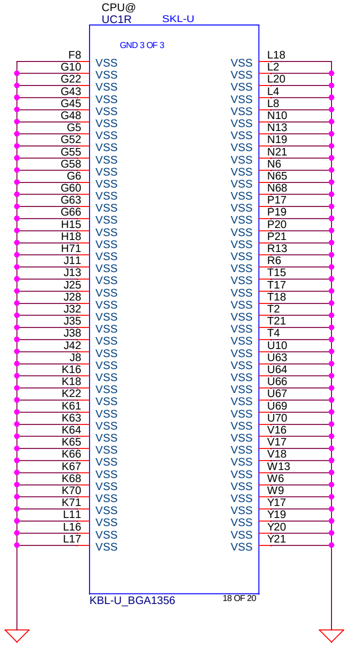


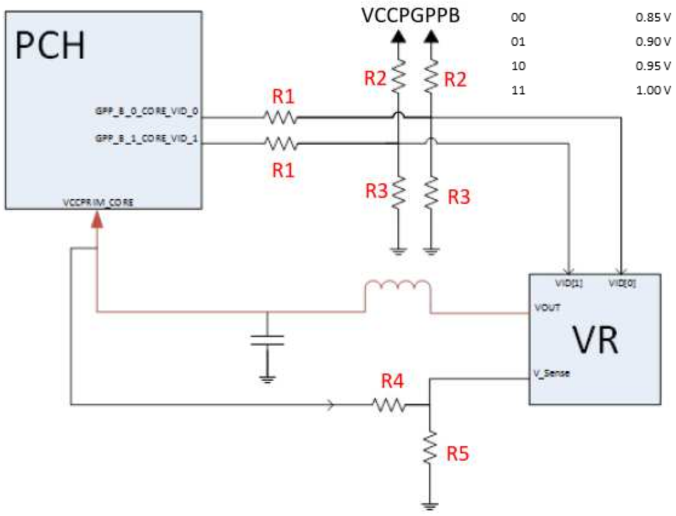




Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424

CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Compal Electronics, Inc.

Title
CPU (14/14)
Size
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LA-E132P
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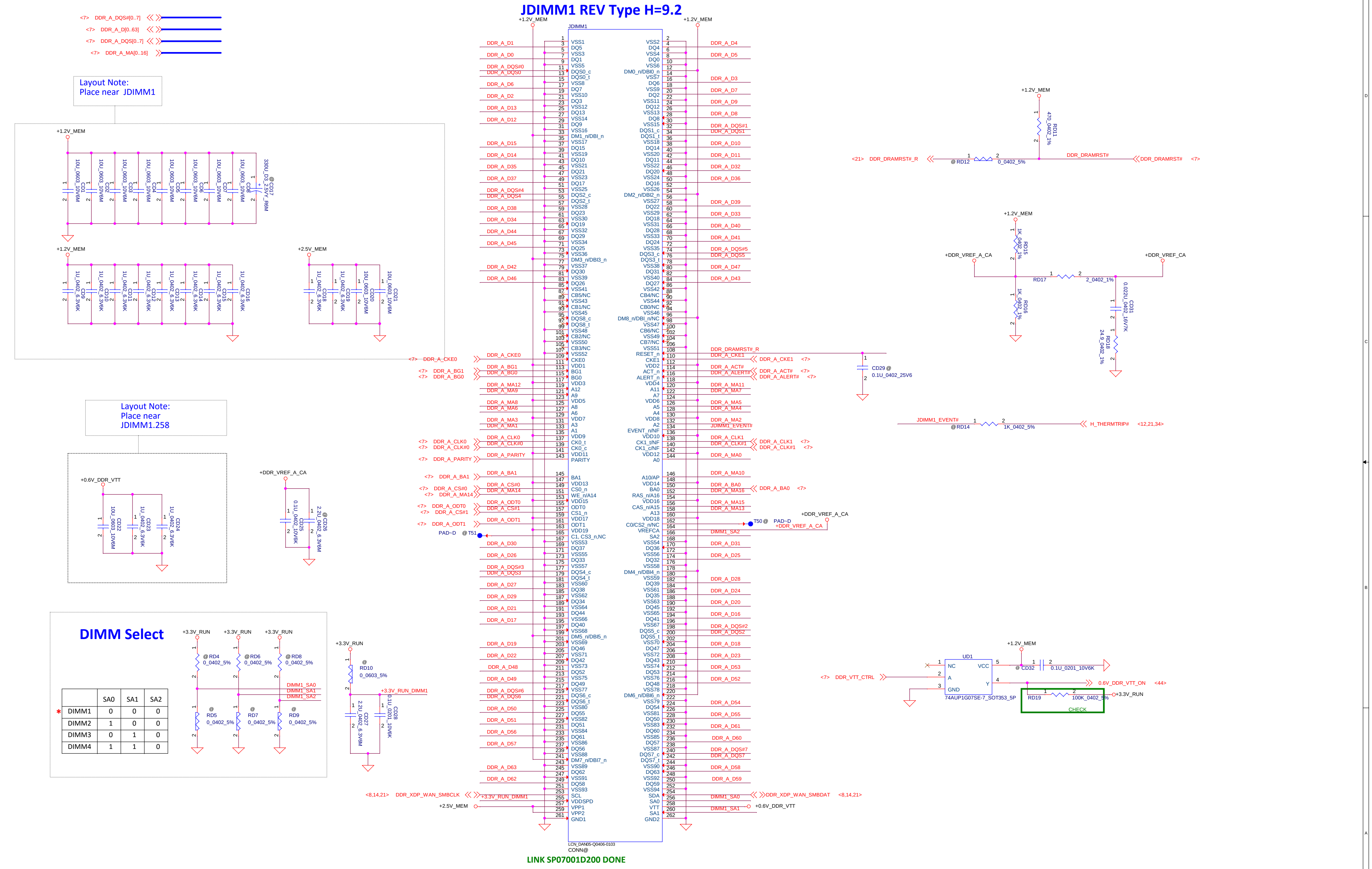
For DDR4



Layout Note:
Place near JDIMM1

Layout Note:
Place near
JDIMM1.258

DIMM Select

	SA0	SA1	SA2
* DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

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Title
DDR4

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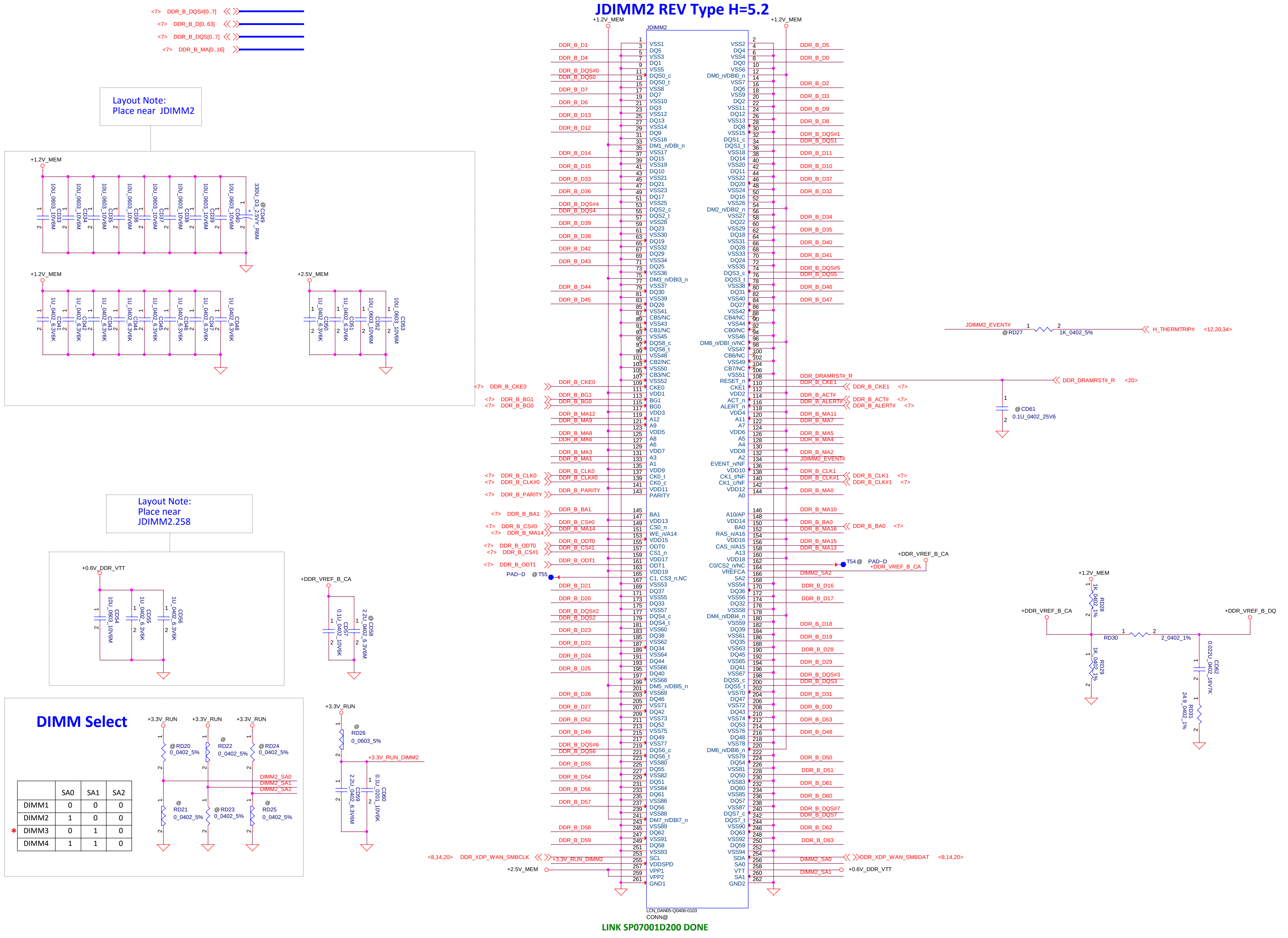
For DDR4

JDIMM2 REV Type H=5.2



Layout Note:
Place near JDIMM2

Layout Note:
Place near
JDIMM2.258

DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
* DIMM3	0	1	0
DIMM4	1	1	0

LINK SP07001D200 DONE

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Title
DDR4

Size
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LA-E132P
Rev
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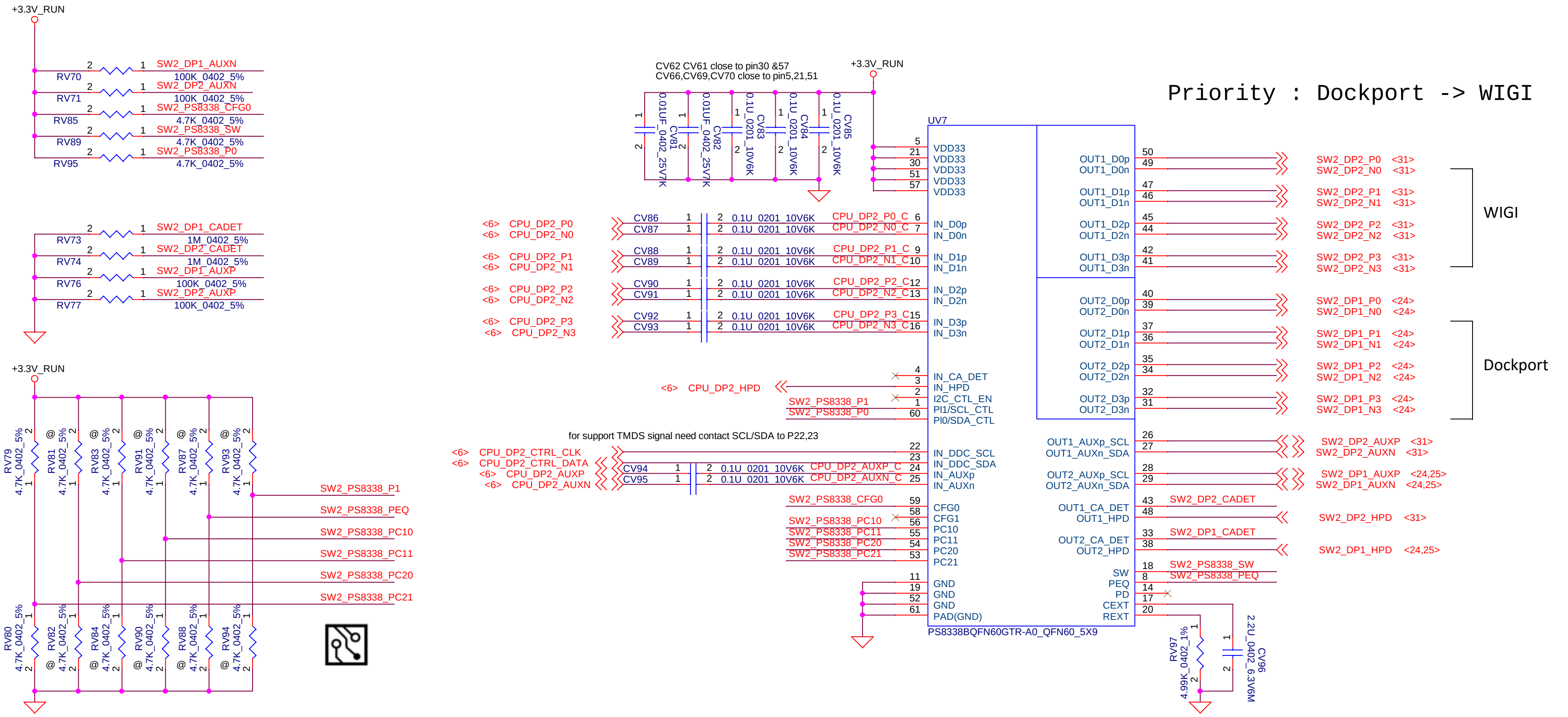
Date: Wednesday, November 09, 2016

For Steamboat12/14 &Kirkwood



CV62 CV61 close to pin30 &57
CV66,CV69,CV70 close to pin5,21,51

Priority : Dockport -> WIGI

for support TMDS signal need contact SCL/SDA to P22,23

```
Port switching control or priority configuration. Internal pull down ~150KΩ,
3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected  (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)
```

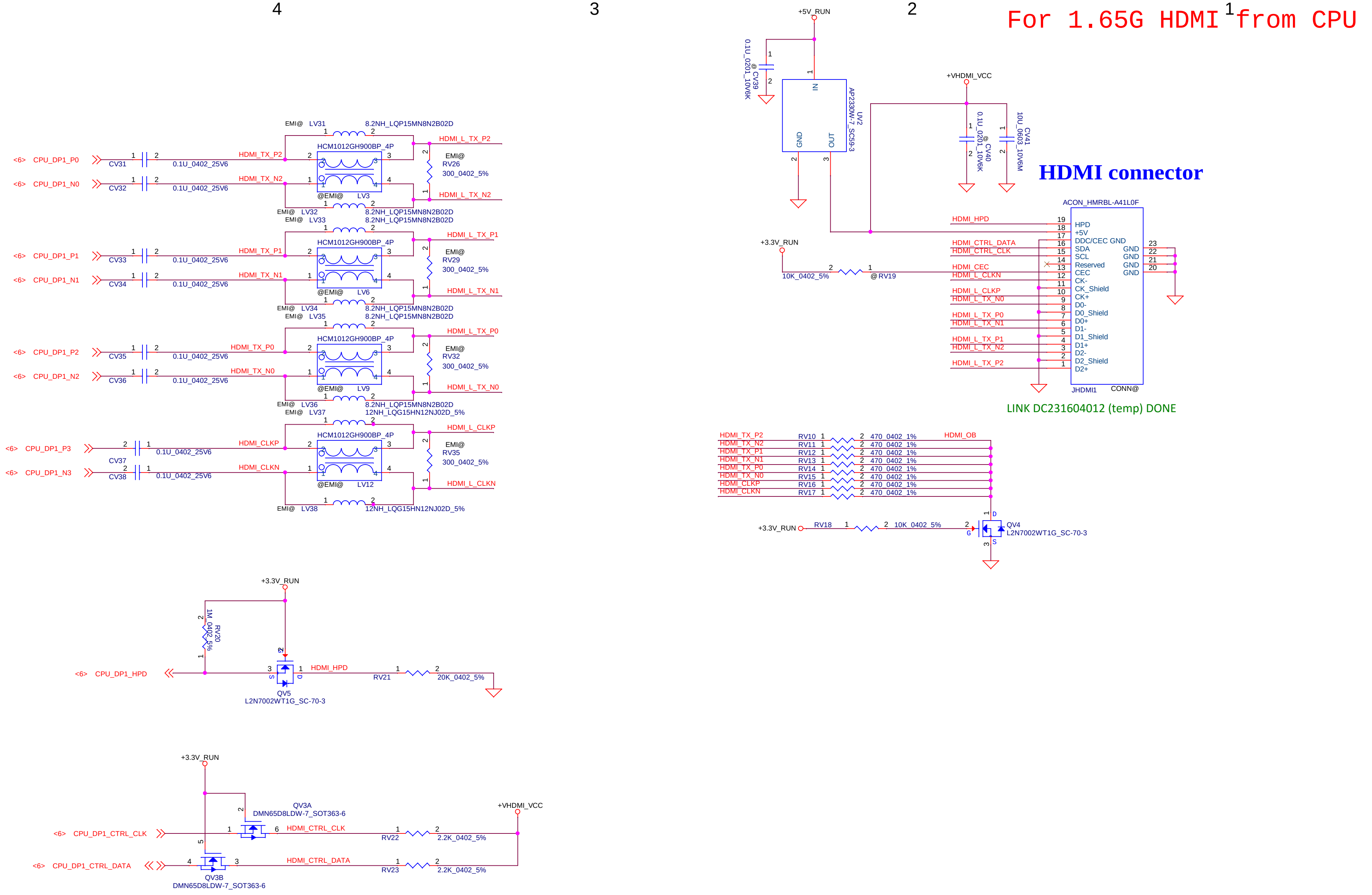
vender sugguest MUX use LLEQ PEQ=M and PI0=H !!

```
Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2
```

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

Compal Electronics, Inc.
Title
DP SW2 PS8338
Size Document Number
LA-E132P
Rev 1.0
Date: Wednesday, November 09, 2016 Sheet 22 of 58

For 1.65G HDMI from CPU



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Compal Electronics, Inc.

Title HDMI CONN		
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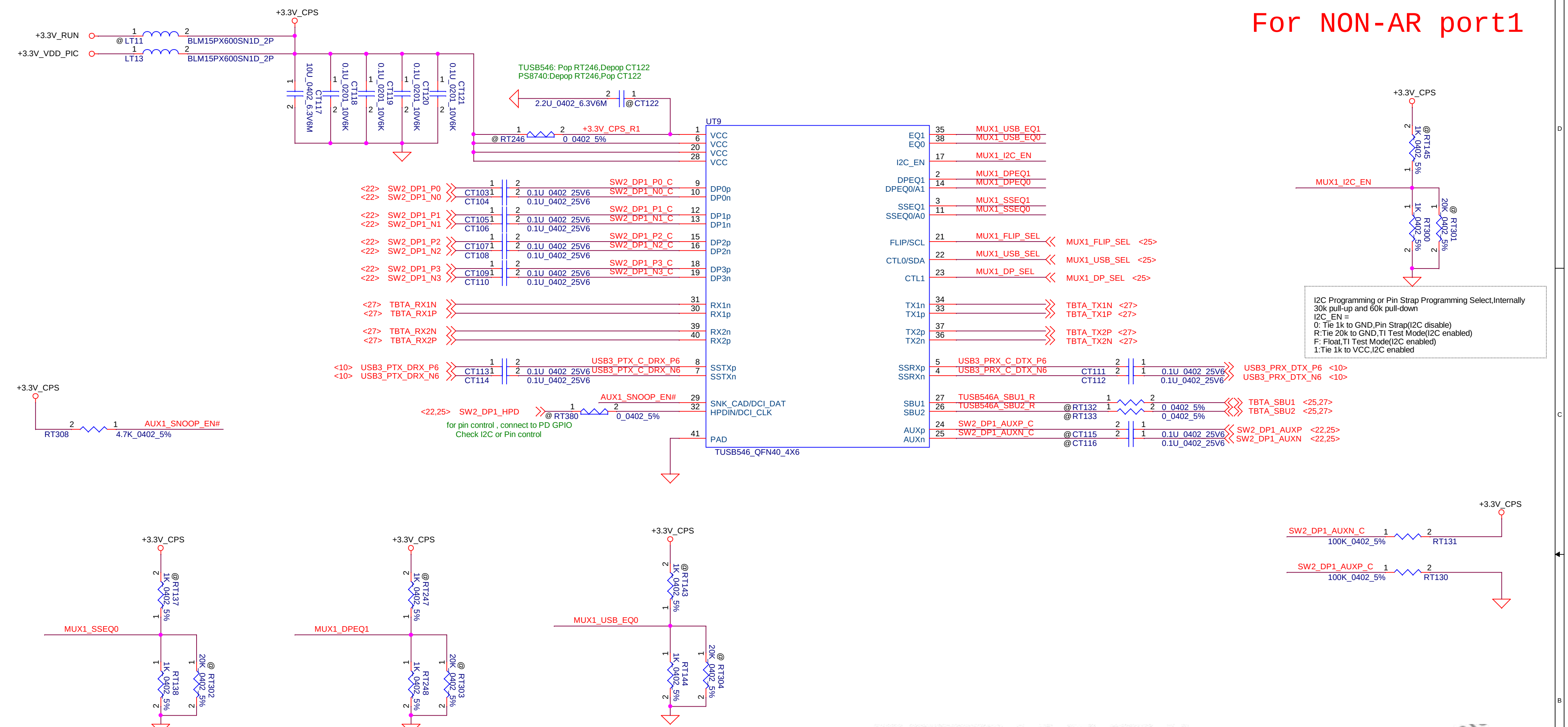
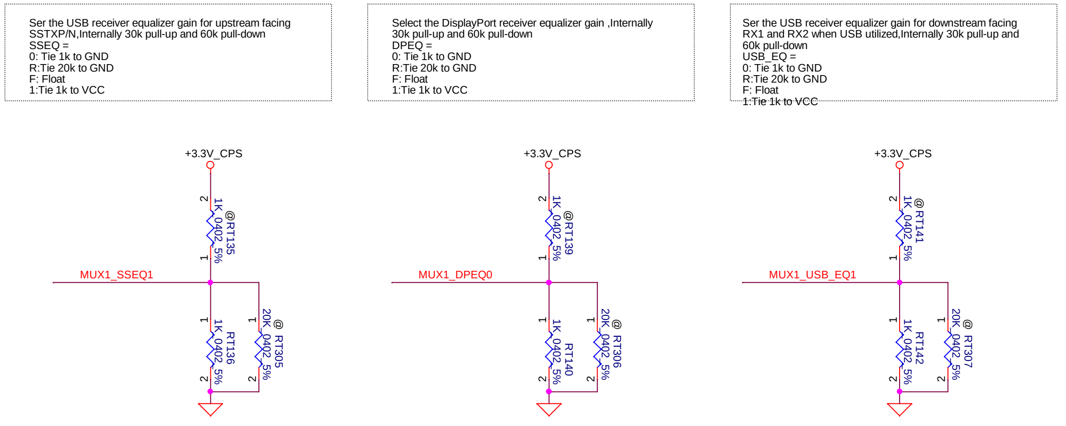
For NON-AR port1



I2C Programming or Pin Strap Programming Select,Internally 30k pull-up and 60k pull-down
I2C_EN =
0: Tie 1k to GND,Pin Strap(I2C disable)
R:Tie 20k to GND,TI Test Mode(I2C enabled)
F: Float,TI Test Mode(I2C enabled)
1:Tie 1k to VCC,I2C enabled

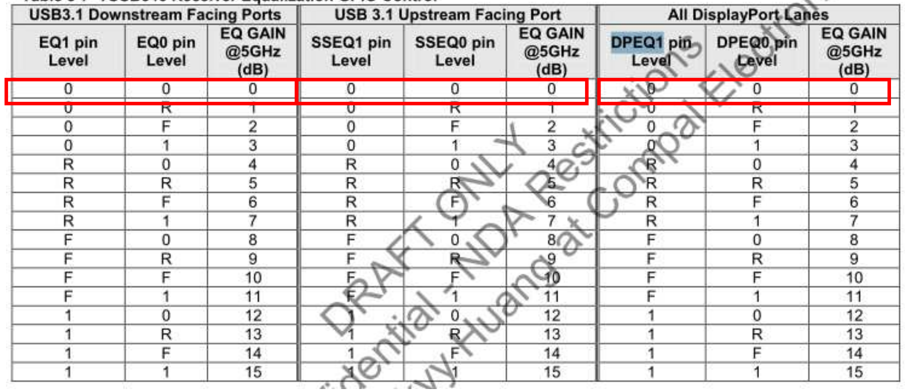


Ser the USB receiver equalizer gain for upstream facing SSTXP/N,Internally 30k pull-up and 60k pull-down
SSEQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC

Select the DisplayPort receiver equalizer gain ,Internally 30k pull-up and 60k pull-down
DPEQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC

Ser the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB utilized,Internally 30k pull-up and 60k pull-down
USB_EQ =
0: Tie 1k to GND
R:Tie 20k to GND
F: Float
1:Tie 1k to VCC

Table 8-7 TUSB546 Receiver Equalization GPIO Control



USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Compal Electronics, Inc.

Title	DP/USB3 Repeater SW TUSB546
Size	
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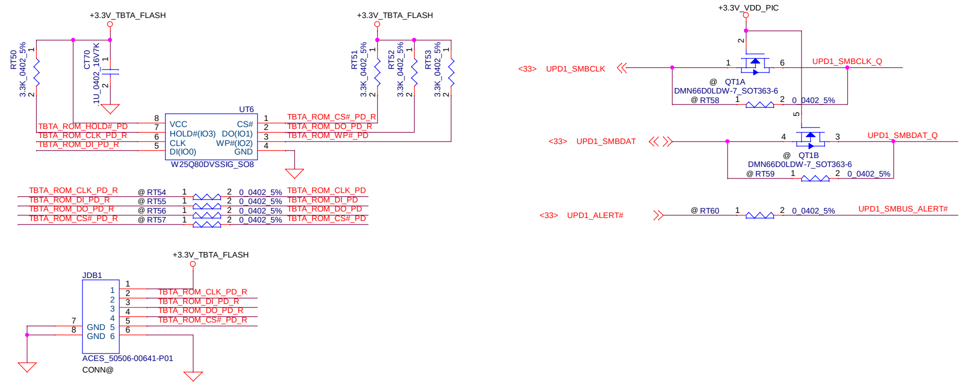
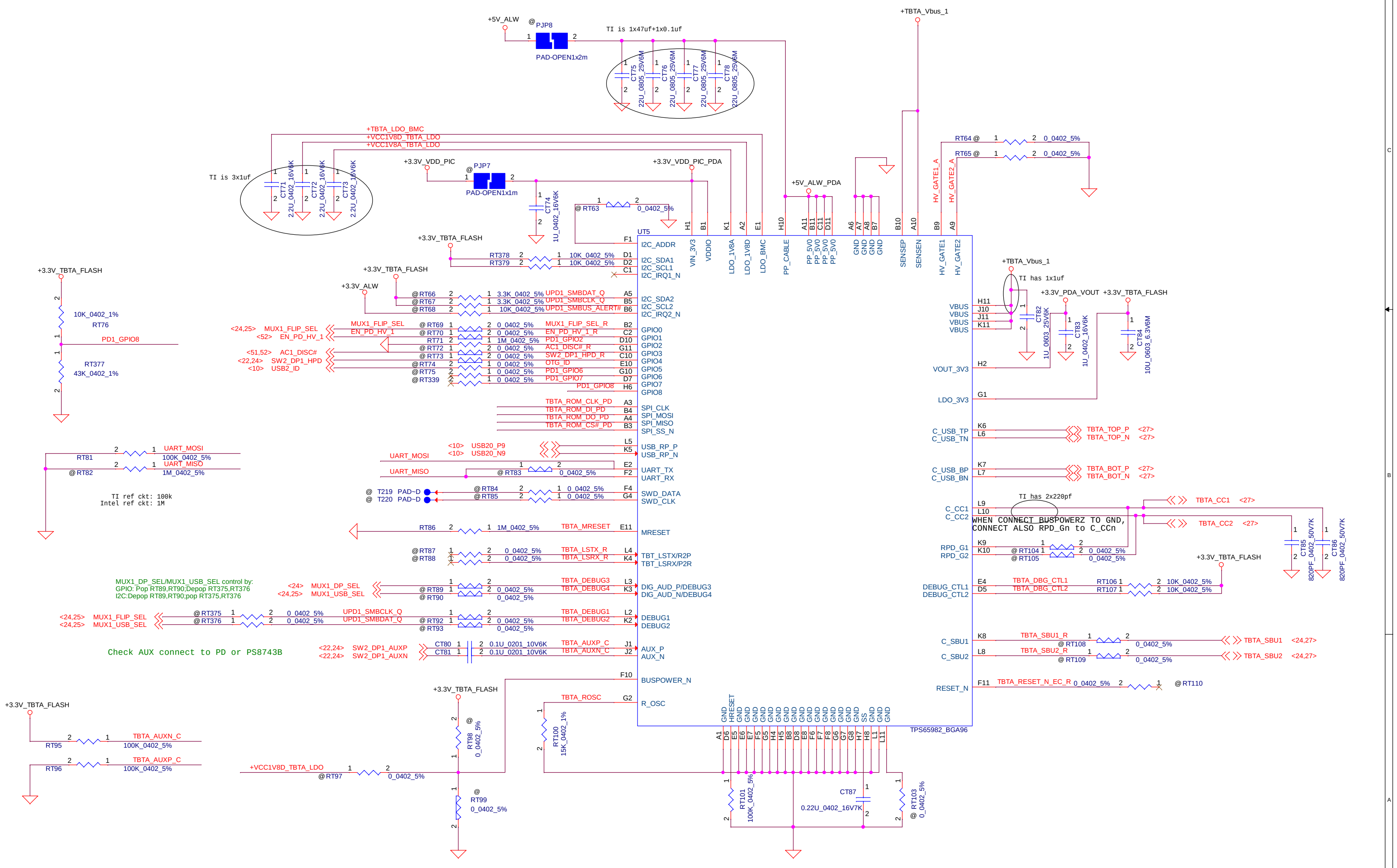
For NON-AR port1



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max/" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max/" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.



Need Link TPS65982D

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Title	**[Type C]PD Controller TI**
Size	Document Number **LA-E132P** Rev 1.0
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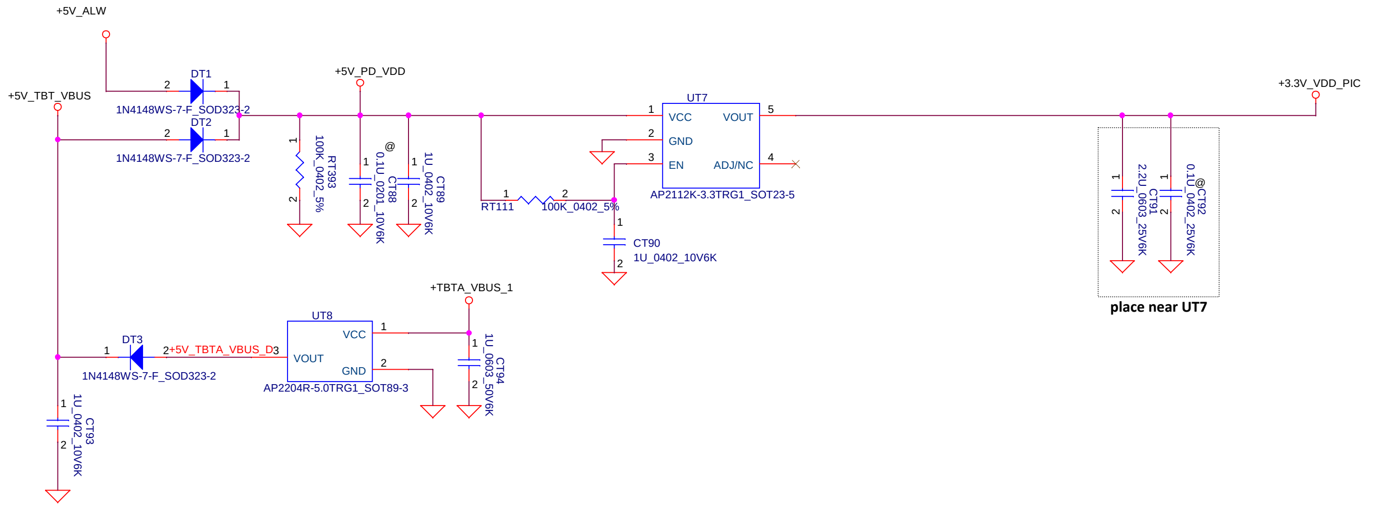

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Title
[Type C]PD Power

Size
Document Number
LA-E132P
Rev
1.0

Date: Wednesday, November 09, 2016
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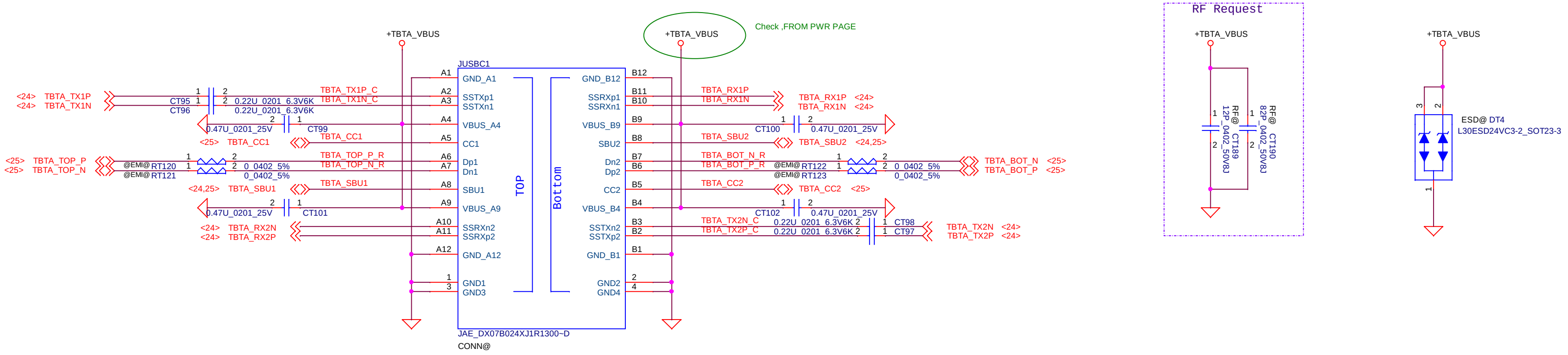
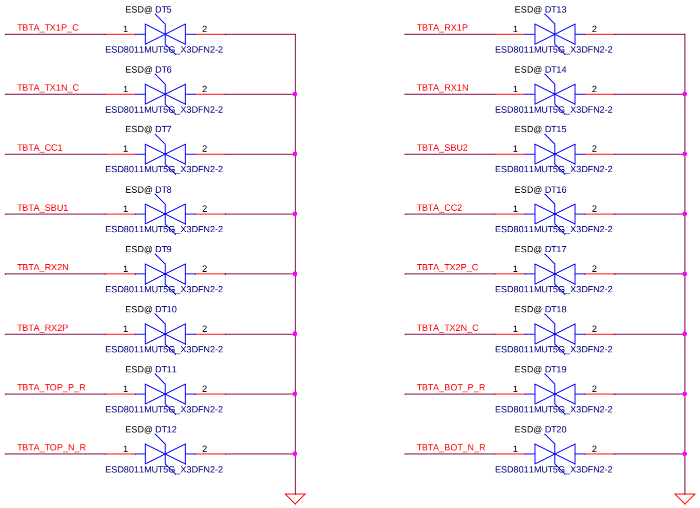
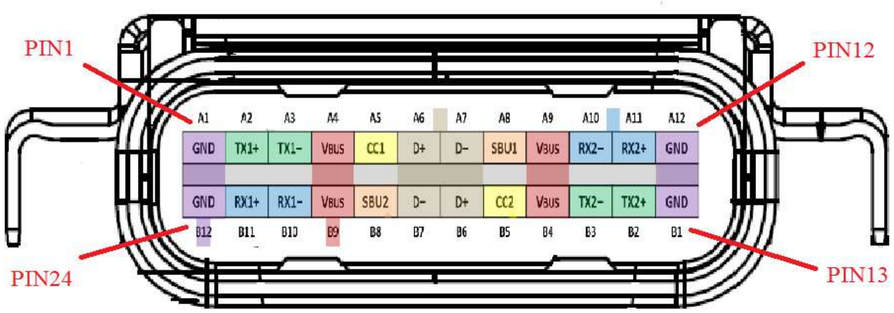
For NON AR Config



Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done





Compal Electronics, Inc.

Title
USB 3.0 CONN TYPE C

Size | Document Number **LA-E132P** | Rev 1.0

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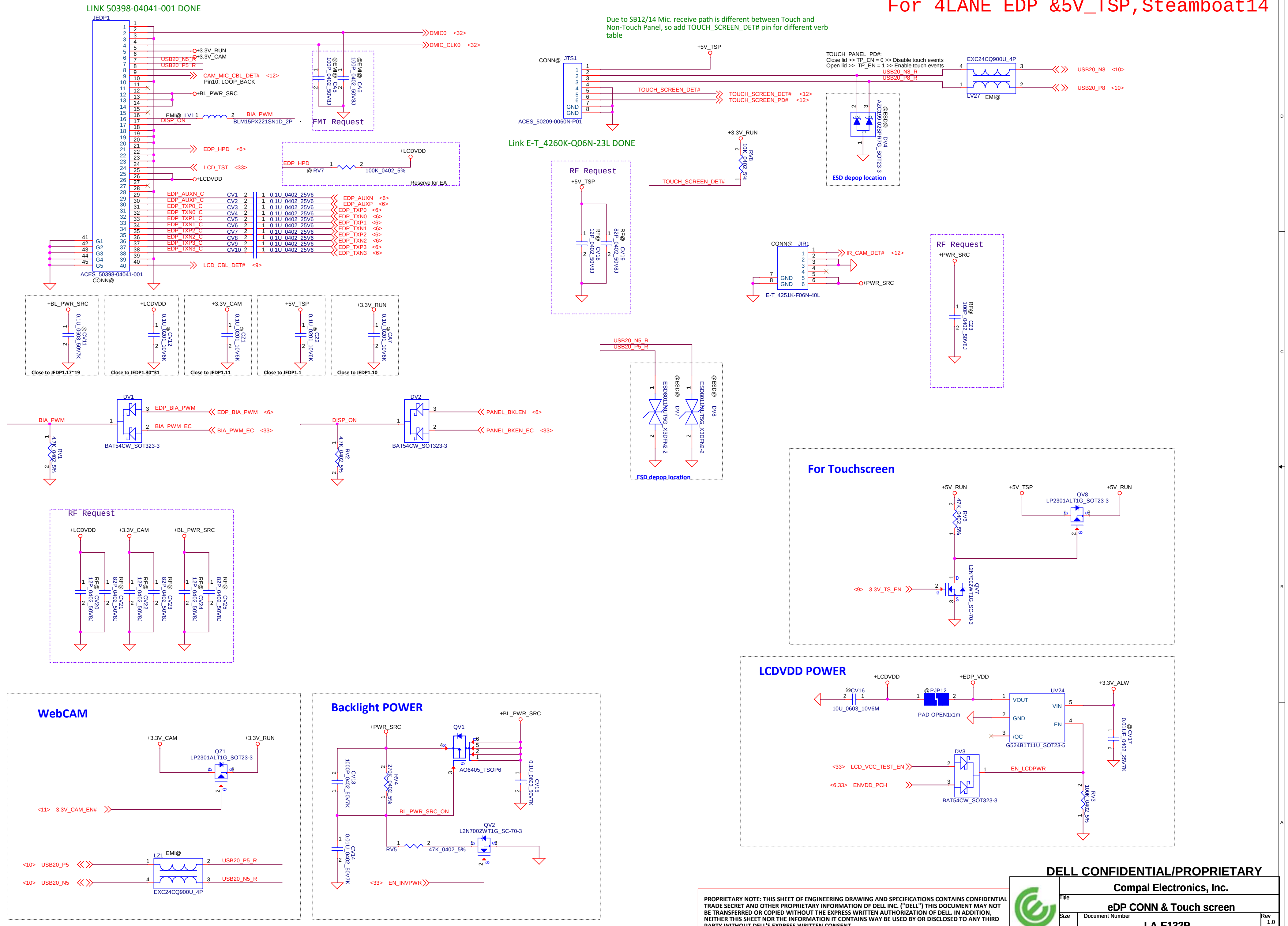
For 4LANE EDP &5V_TSP,Steamboat14

Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table



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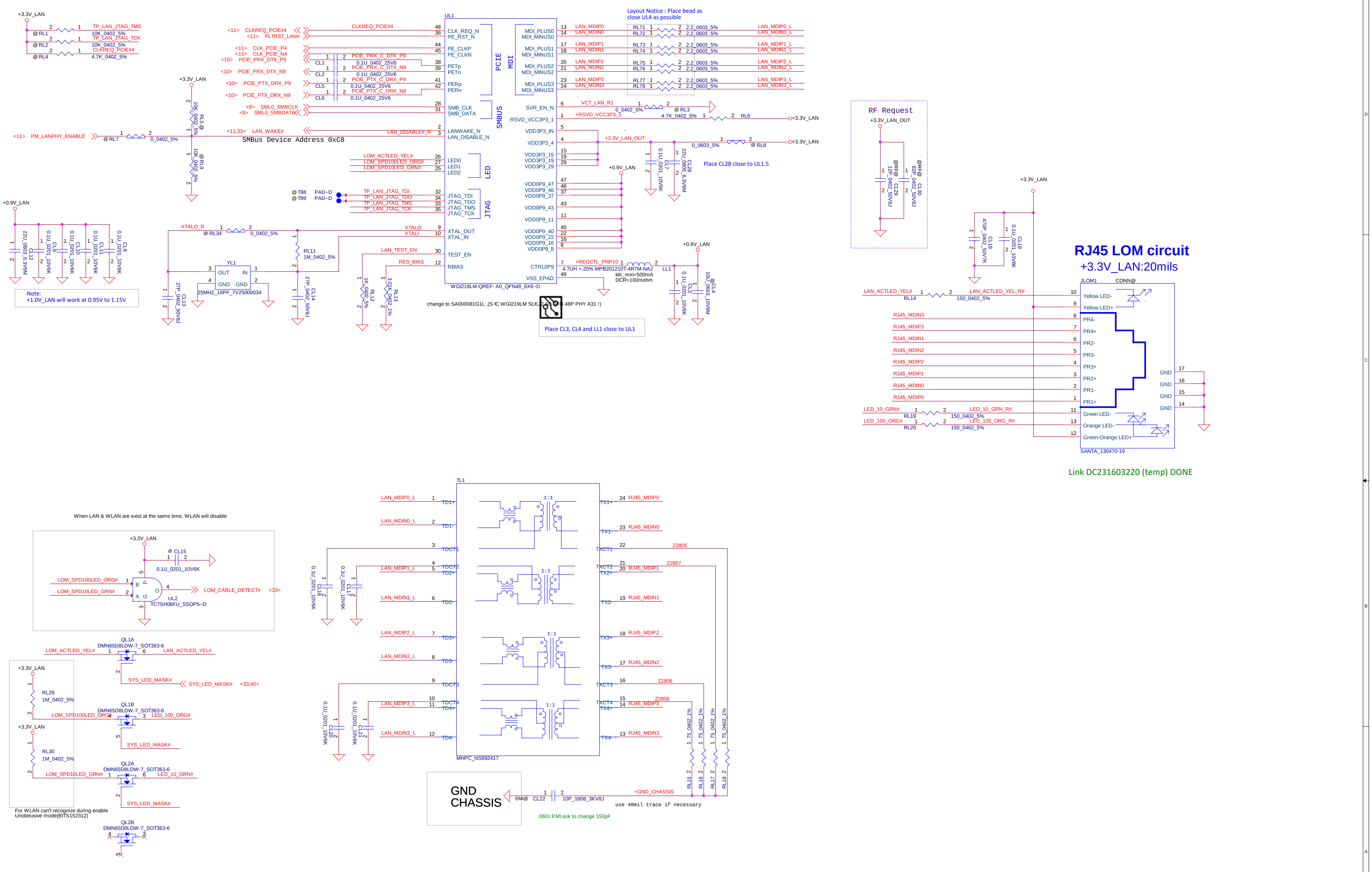
Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size | Document Number: LA-E132P | Rev 1.0

Date: Wednesday, November 09, 2016 | Sheet 28 of 58



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Compal Electronics, Inc.

Title
LAN Clarkvillie & RJ45

Size
Document Number
LA-E132P
Rev
1.0

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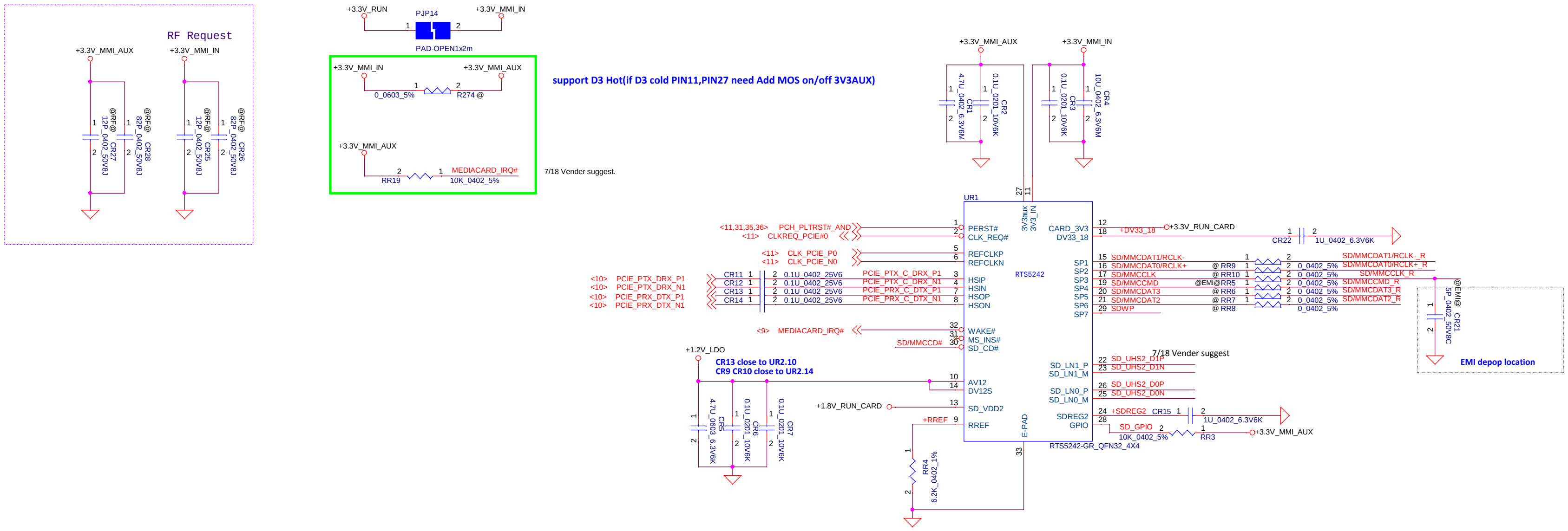
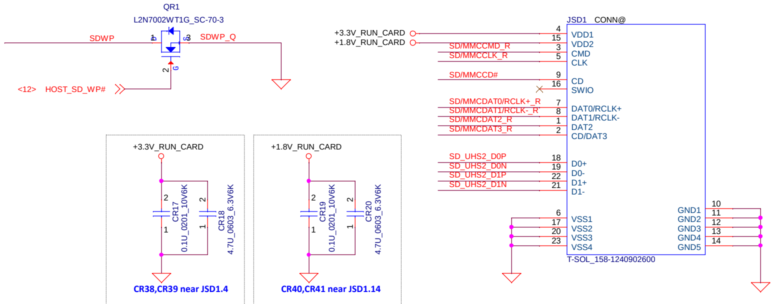
For PCIE Interface



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	Low	Low	Write Enable
Low	Low	High	Write Protect(FW LOCK)



LINK SP071603151 (temp) DONE

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Compal Electronics, Inc.

Title
Card Reader RTS5242
Size Document Number
LA-E132P
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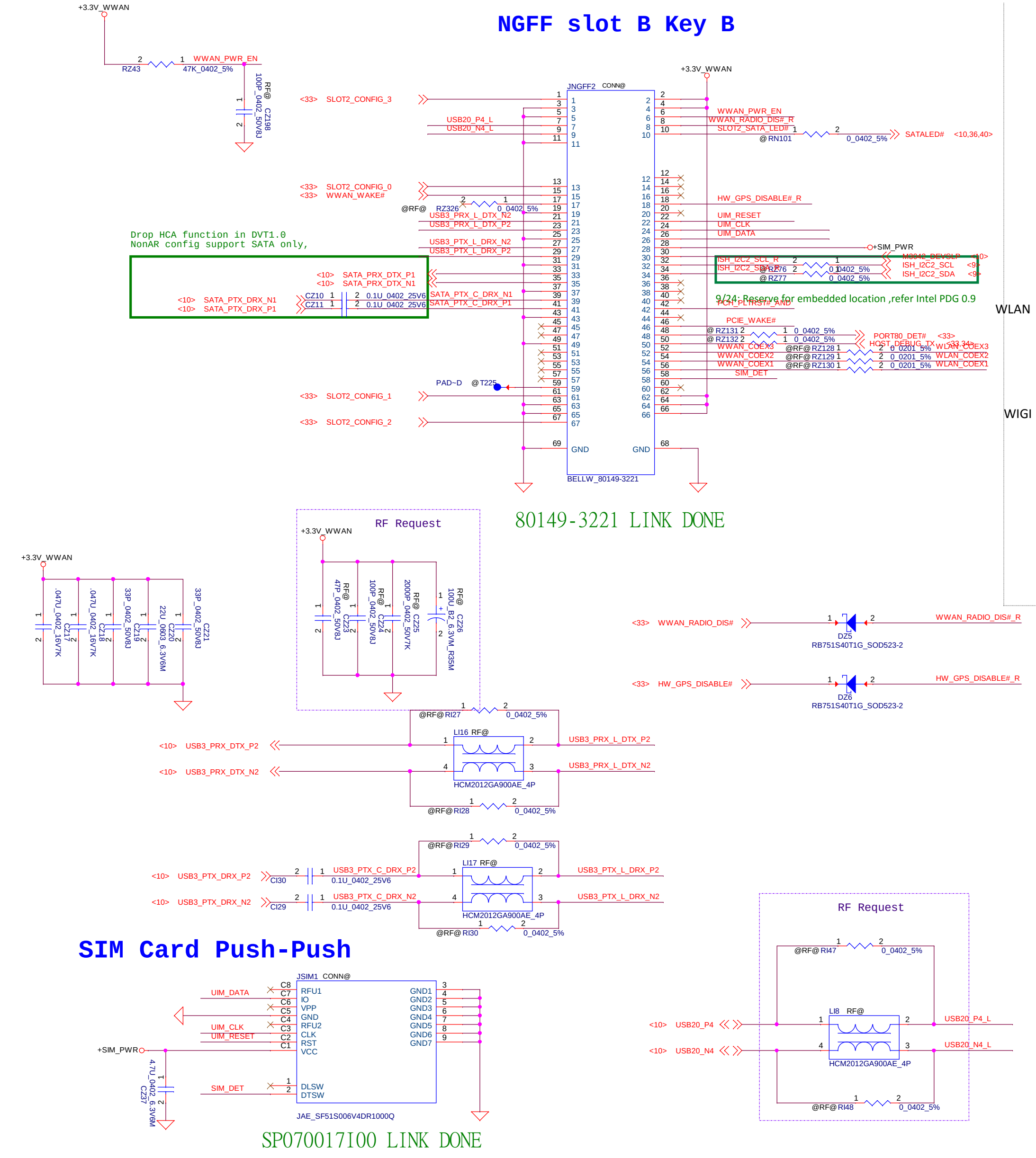
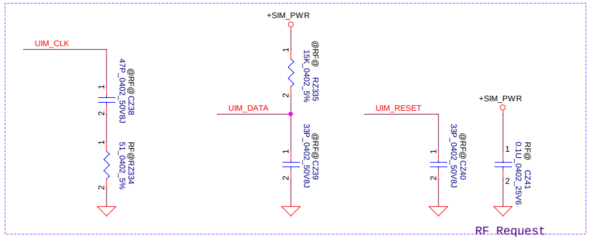
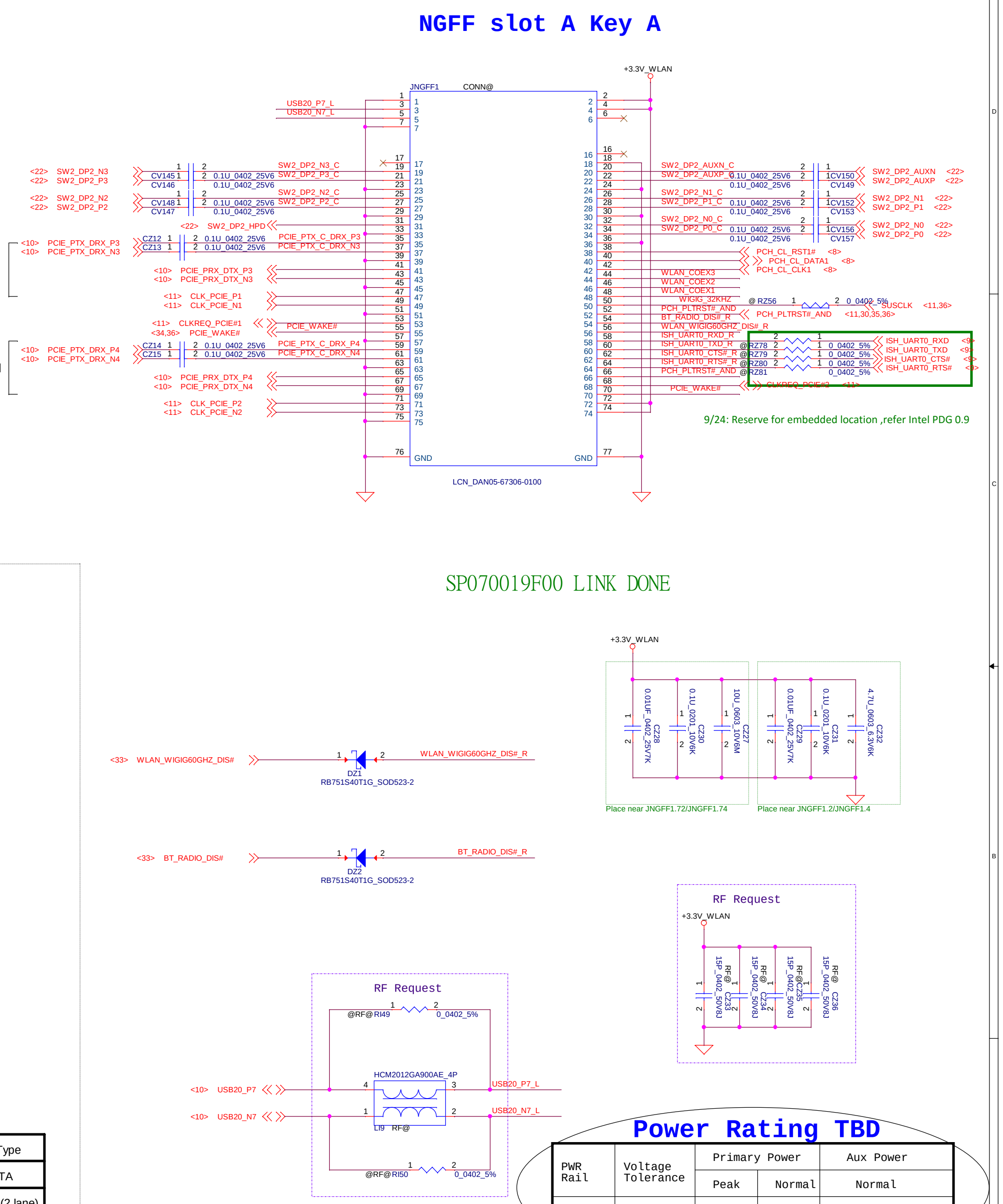
for no AR,Brekenridge 12/14/15 UMA/Steamboat

NGFF slot B Key B





NGFF slot A Key A



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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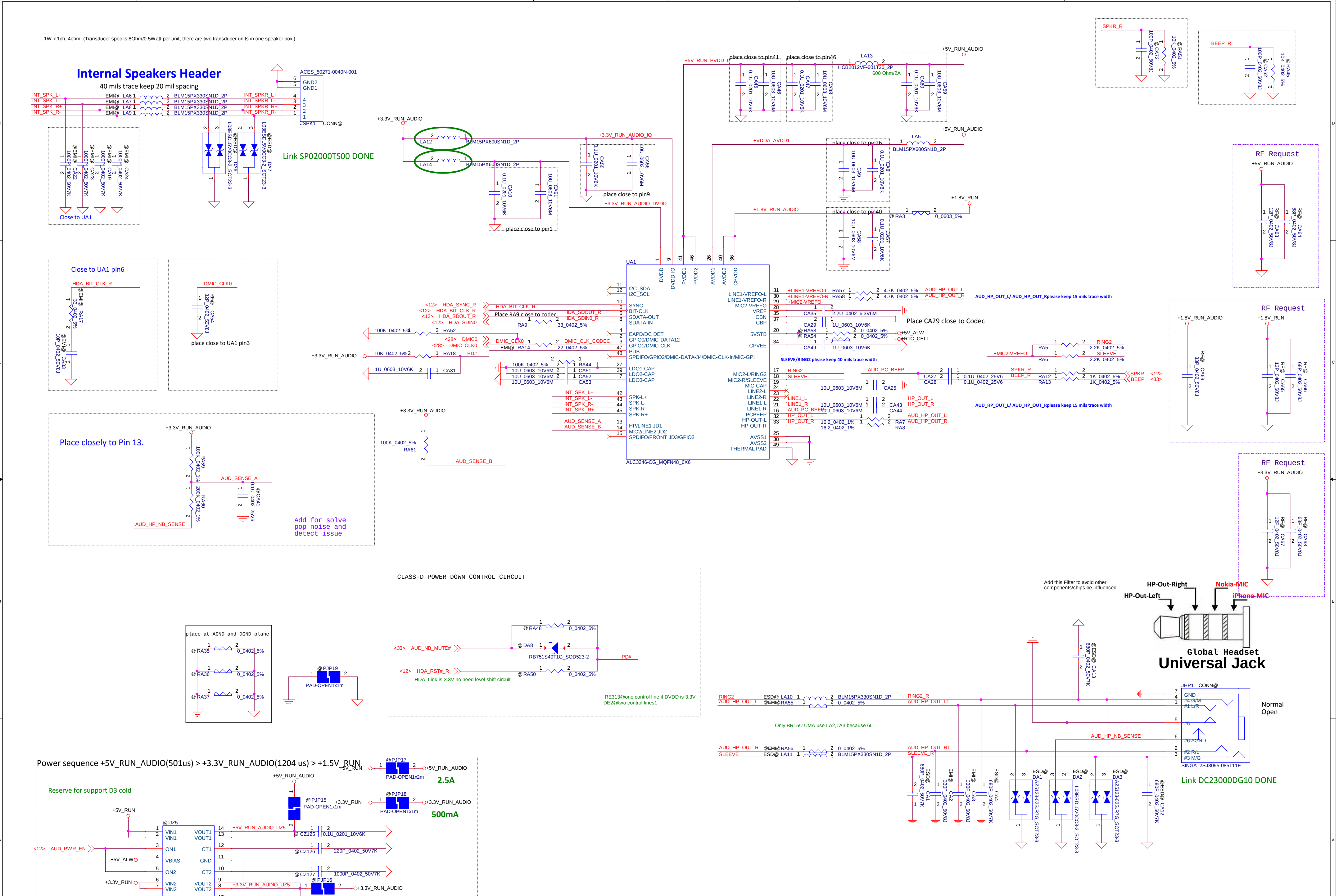
Title NGFF Card
Size Document Number LA-E132P Rev 1.0
Date: Wednesday, November 09, 2016 Sheet 31 of 58



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title ***Codec ALC3246***

Size	Document Number	Rev
C	***LA-E132P***	1.0

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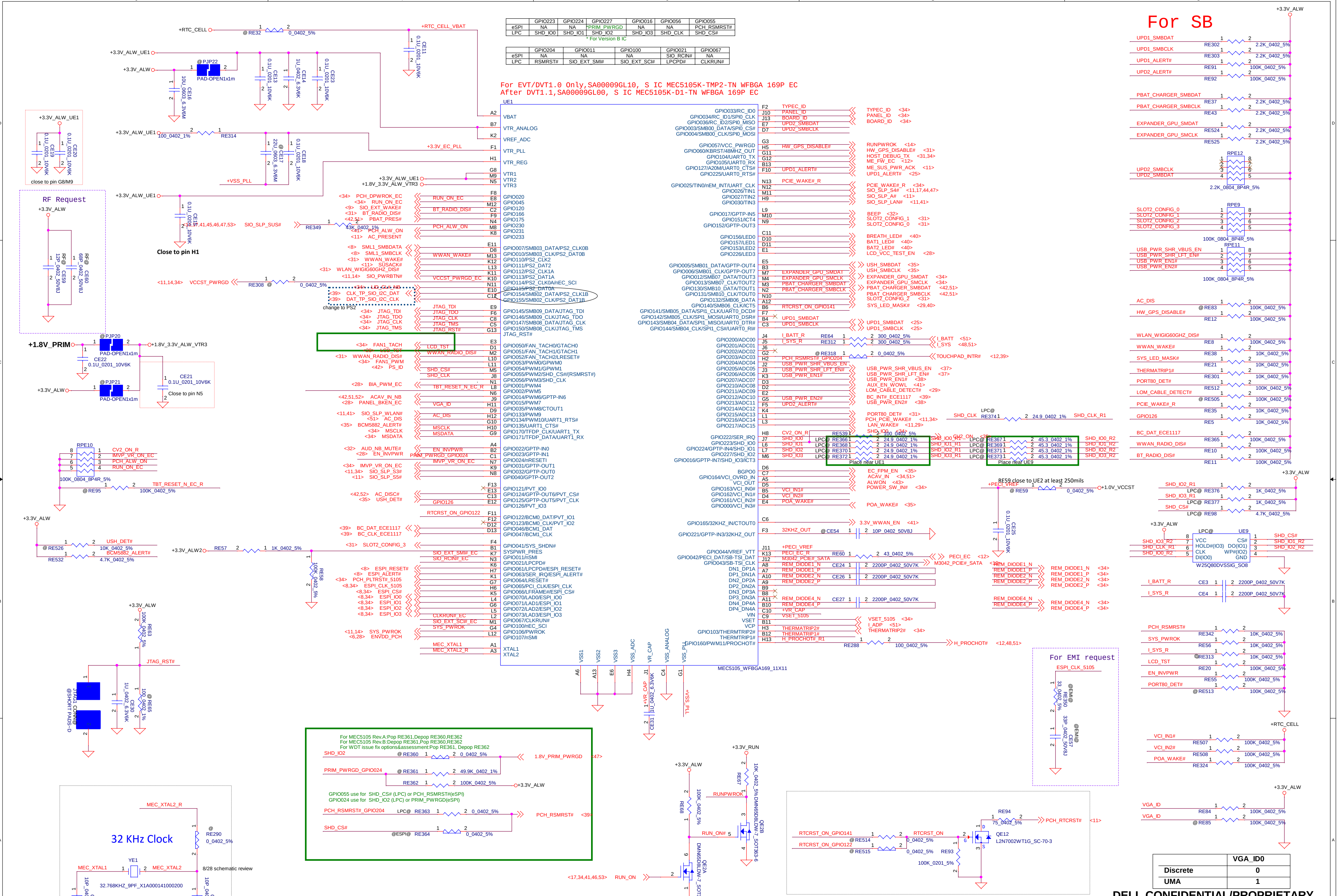

	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	*PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

For EVT/DVT1.0 Only,SA00009GL10, S IC MEC5105K-TMP2-TN WFBGA 169P EC
After DVT1.1,SA00009GL00, S IC MEC5105K-D1-TN WFBGA 169P EC

	VGA_ID0
Discrete	0
UMA	1

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Compal Electronics, Inc.

Title
EC MEC5105

Size
Document Number
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1.0

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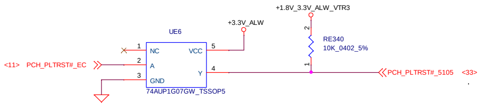
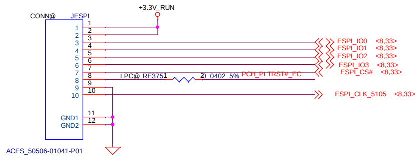
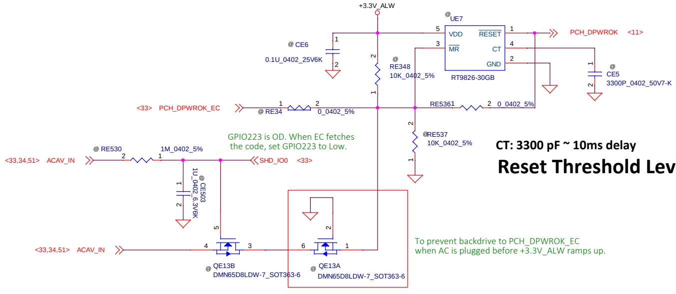




PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

WDT option	
MEC5105 rev.B	Pop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348 Depop RE362, RE536, RE537
MEC5105 rev.C	Pop RE362, RE536 Depop RE361, QE13, CE503, RE530, UE7, CE5,CE6, RE348, RE537



GPIO223 is OD. When EC fetches the code, set GPIO223 to Low.

CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V

To prevent backdrive to PCH_DPWROK_EC when AC is plugged before +3.3V_ALW ramps up.

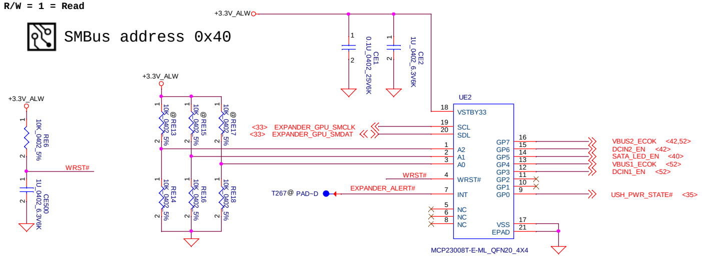
In DC mode, ACAV_IN is LOW. This circuit doesn't affect PCH_DPWROK.
In AC mode, 1. ACAV_IN is high. GPIO223 is tri-state. QE13B is ON. QE13A can prevent backdrive to PCH_DPWROK.
2. EC fetches code and the drives GPIO223 to LOW to turn off QE13B. When QE13B is off, un-plug/plug AC will not affect DSW_DPWROK.
3. When WDT occurs, GPIO223 is tri-state (EC reset). ACAV_IN charges CE503. When AC is removed, ACAV_IN goes LOW immediately.
QE13B still kepps on according to RC discharging rate. PCH_DPWROK is LOW because ACAV_IN is LOW.

Control Byte

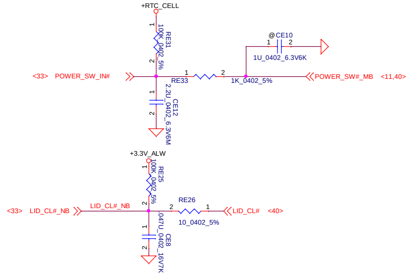
0	1	0	0	A2	A1	A0	R/W

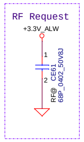
R/W = 0 = Write
R/W = 1 = Read

SMBus address 0x40

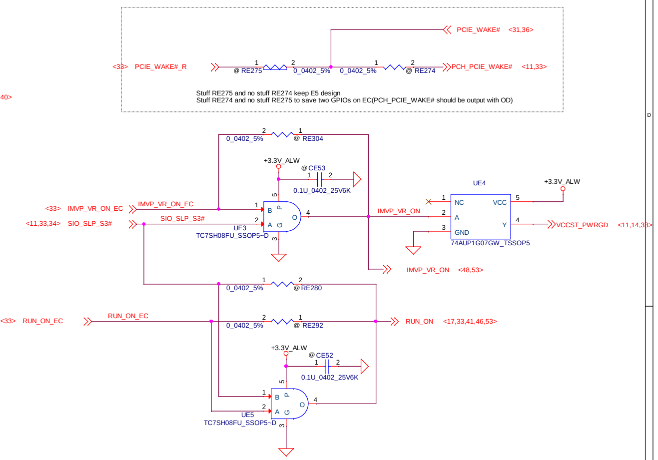


Link Microchip MCP23008 SA0000ADQ00 OK (9/6)

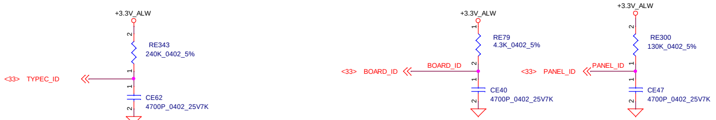




For SB



Stuff RE275 and no stuff RE274 keep E5 design
Stuff RE274 and no stuff RE275 to save two GPIOs on EC(PCH_PCIE_WAKE# should be output with OD)



	RE343	CE62	REV
*	240K	4700p	Single Port ACE w/o AR
	130K	4700p	Single Port ACE w/AR
	62K	4700p	Dual Port ACE w/o AR
	33K	4700p	Dual Port ACE w/AR
	8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4.3K	4700p	.
	2K	4700p	
	1K	4700p	

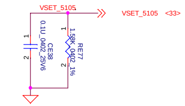
PD_ACE_DET# rise time is measured from 5%~68%.

	RE79	CE40	REV
	240K	4700p	X00
	130K	4700p	X01
	62K	4700p	X02
	33K	4700p	X03
	8.2K	4700p	X04
*	4.3K	4700p	A00
	2K	4700p	
	1K	4700p	

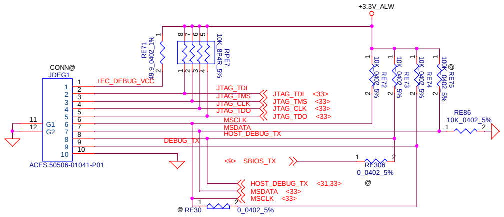
BOARD_ID rise time is measured from 5%~68%.

	RE300	CE47	PANEL SIZE
	240K	4700p	12"
*	130K	4700p	14"
	33K	4700p	15"
	4.3K	4700p	17"

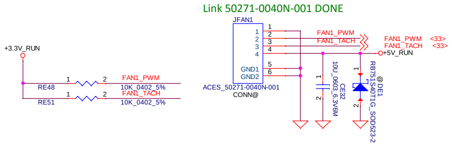
PANEL_ID rise time is measured from 5%~68%.



Rest=1.58K , Tp=96 degree???

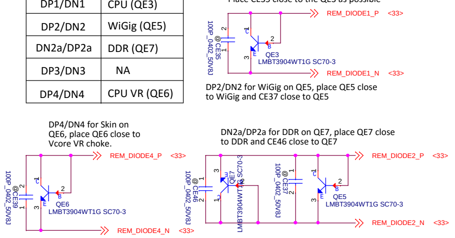


Link 50271-0040N-001 DONE



Thermal diode mapping

5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

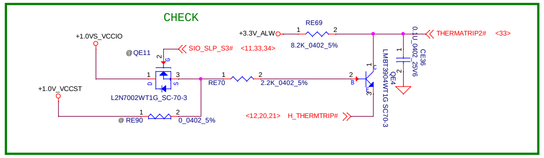


Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7



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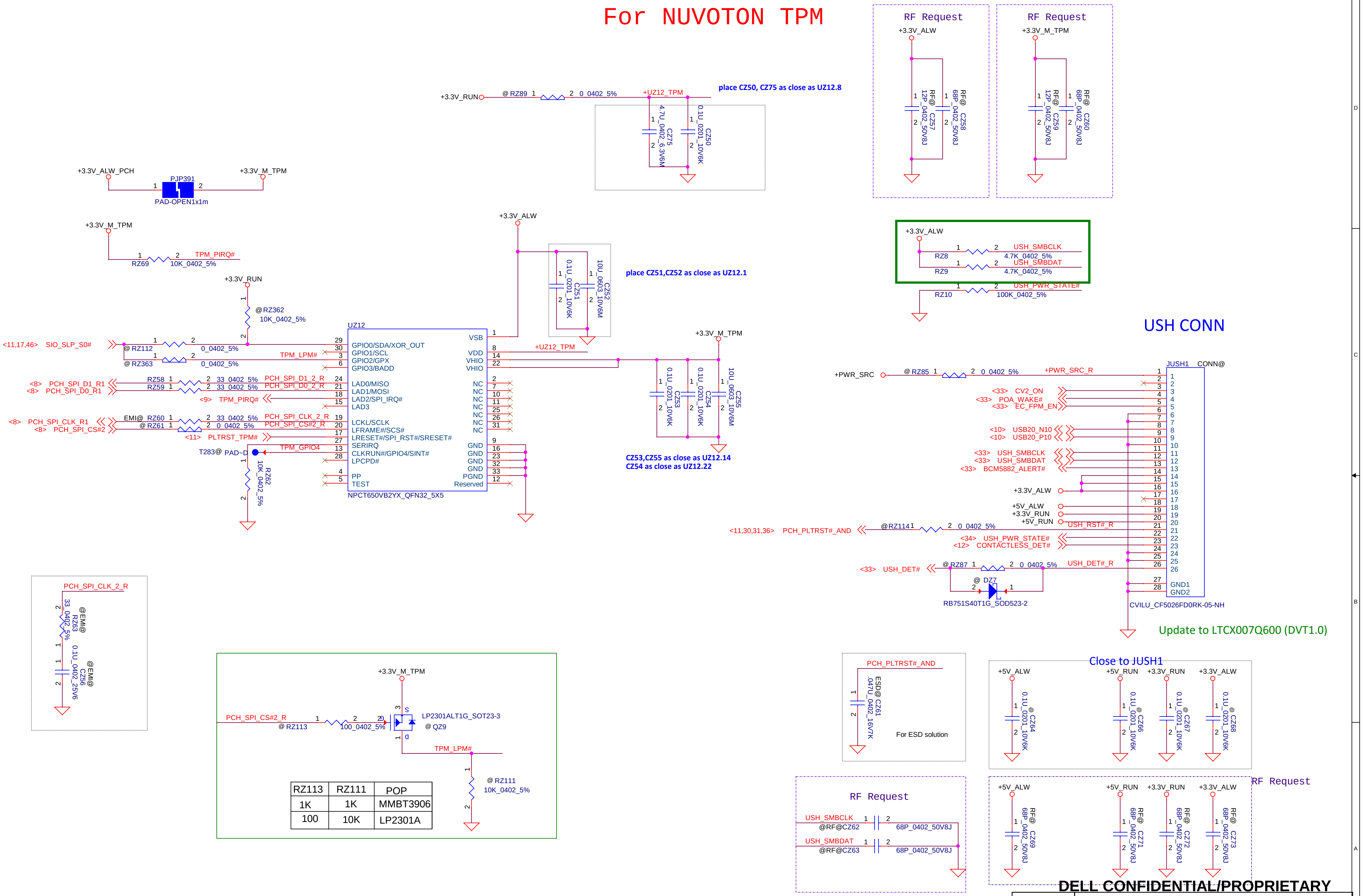
Title
MEC5105 support
Size
Document Number
LA-E132P
Rev
1.0
Date: Wednesday, November 09, 2016

For NUVOTON TPM



RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

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Compal Electronics, Inc.

Title
USH & TPM

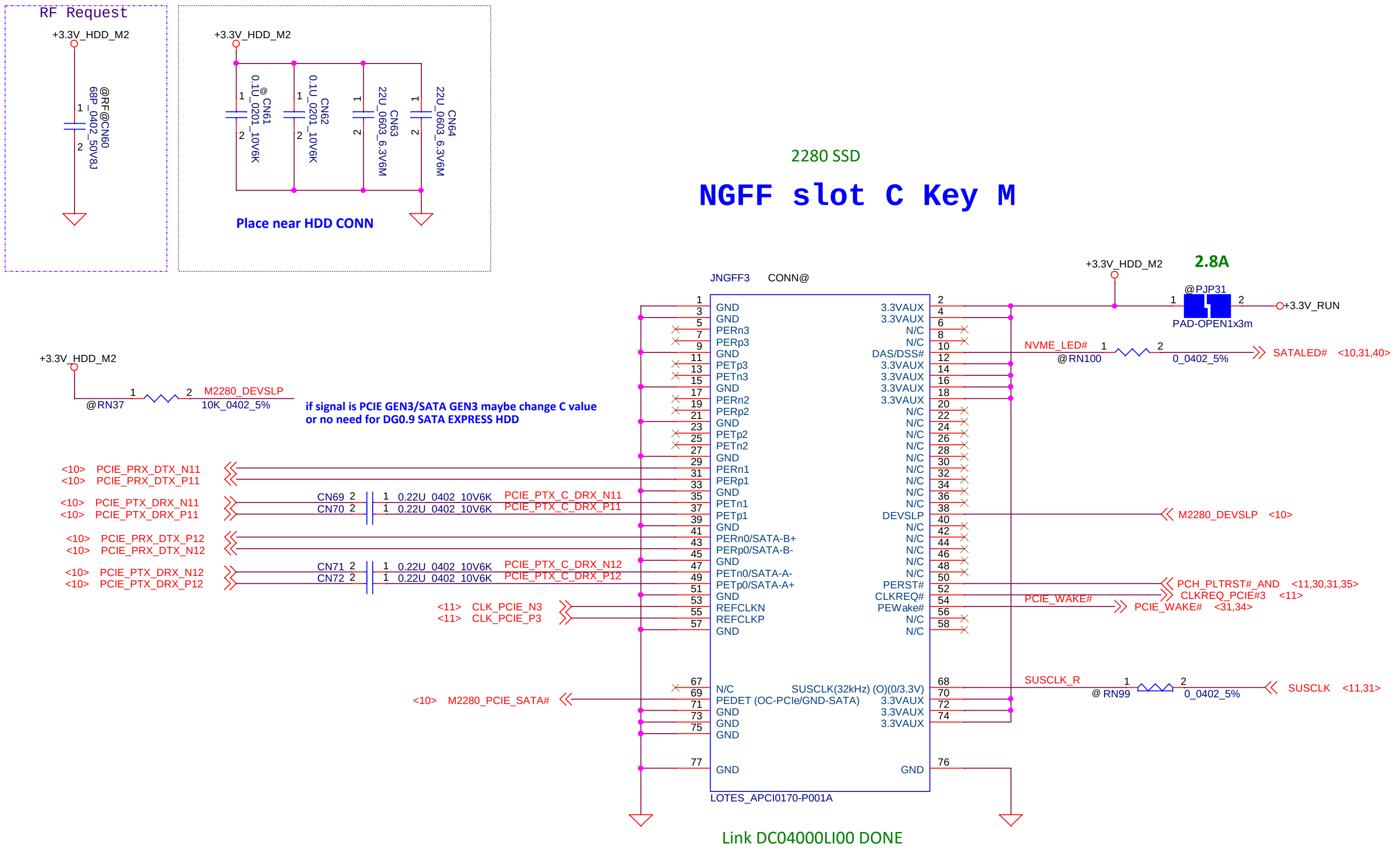
Size | Document Number **LA-E132P** | Rev 1.0

Date: Wednesday, November 09, 2016 | Sheet 35 of 58

For Brekenridge 12/14/15 UMA/Steamboat

2280 SSD

NGFF slot C Key M



Link DC04000LI00 DONE

DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Title
M2 2280 Socket
Size
Document Number
LA-E132P
Rev
1.0
Date: Wednesday, November 09, 2016
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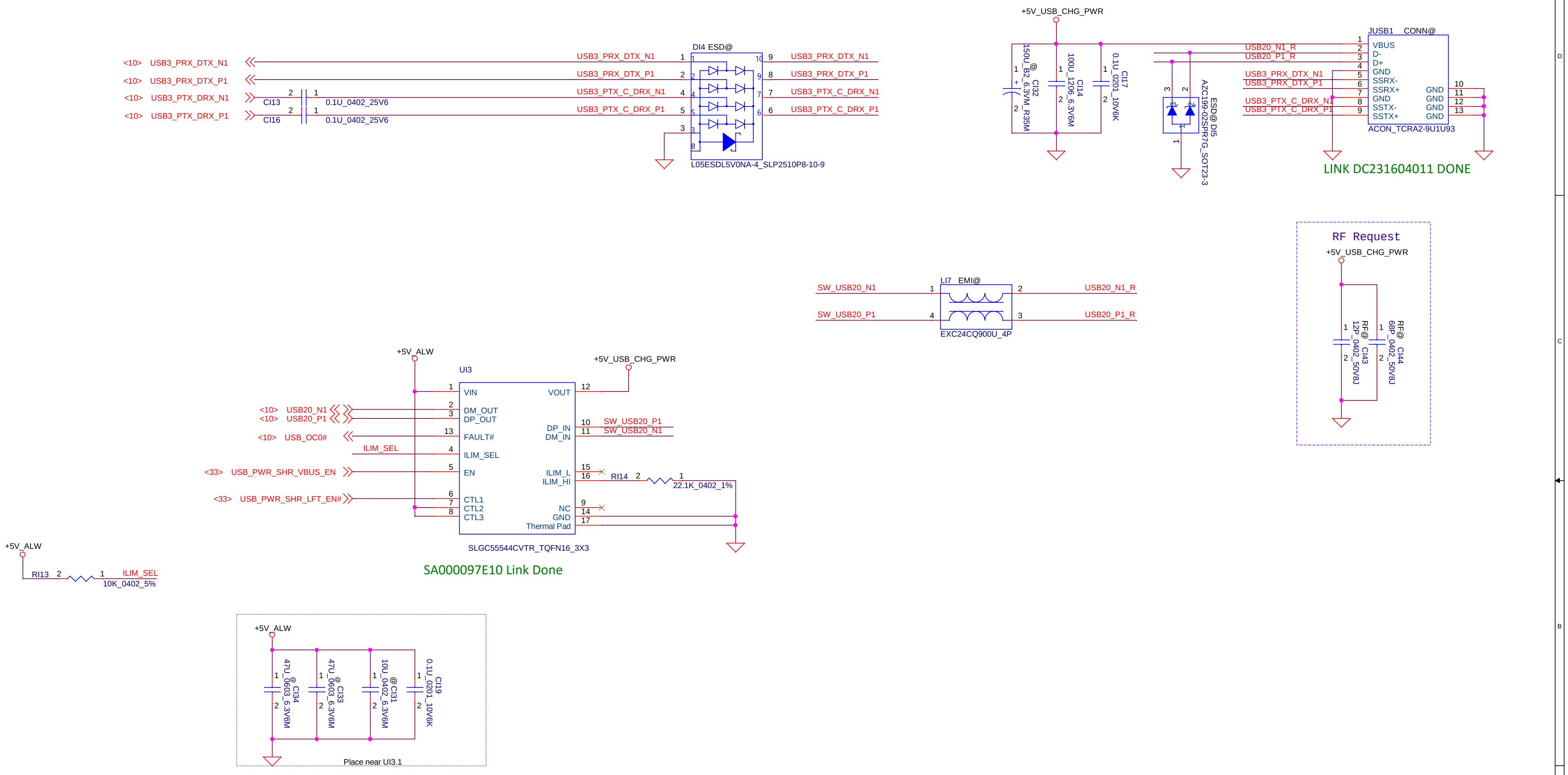

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title
JUSB1+PS

Size
Document Number
LA-E132P
Rev
1.0

Date: Wednesday, November 09, 2016
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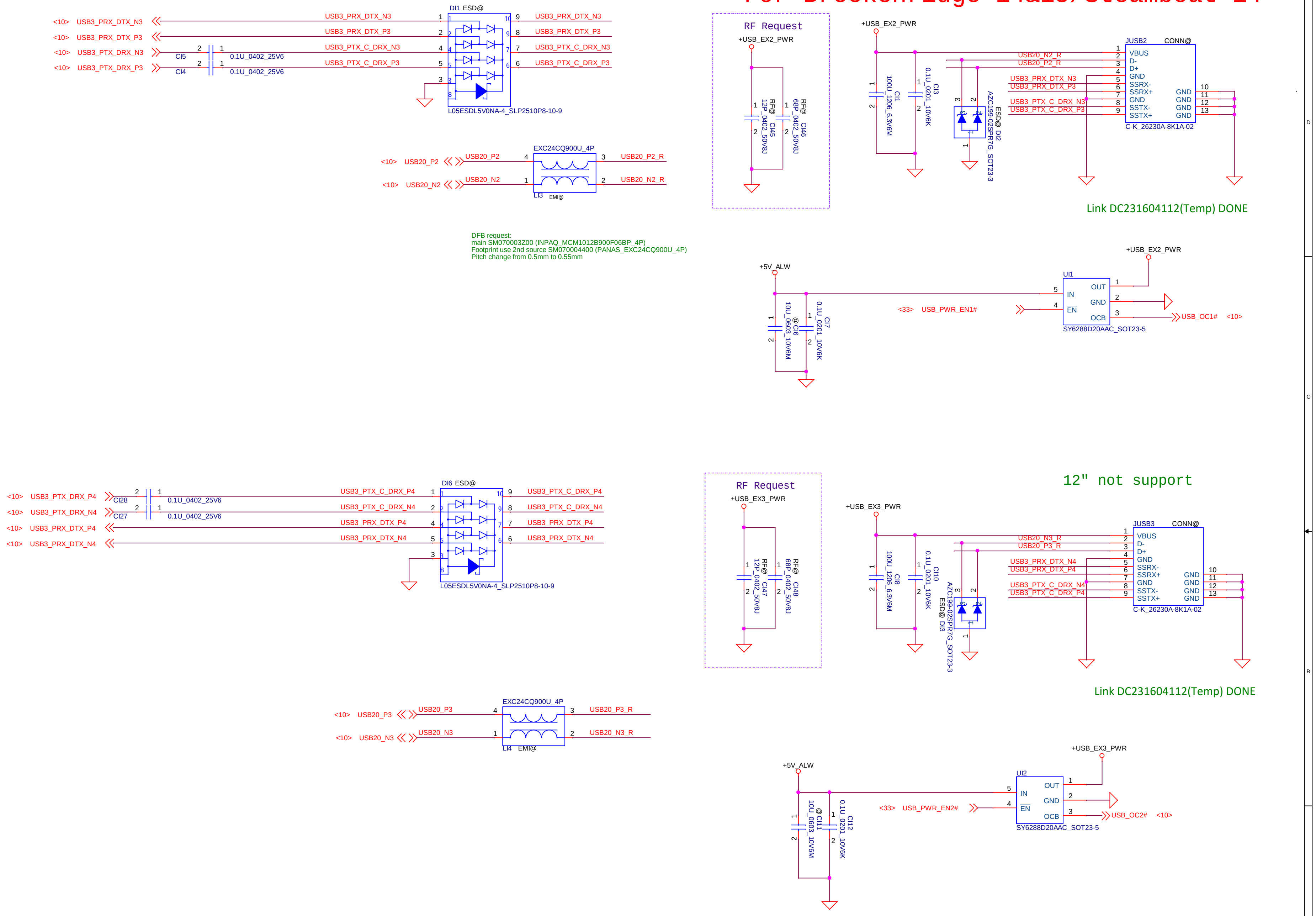
For Breckenridge 14&15/Steamboat 14



Link DC231604112(Temp) DONE

DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

12" not support

Link DC231604112(Temp) DONE

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Compal Electronics, Inc.

Title
JUSB2&JUSB3

Size
Document Number
LA-E132P
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1.0

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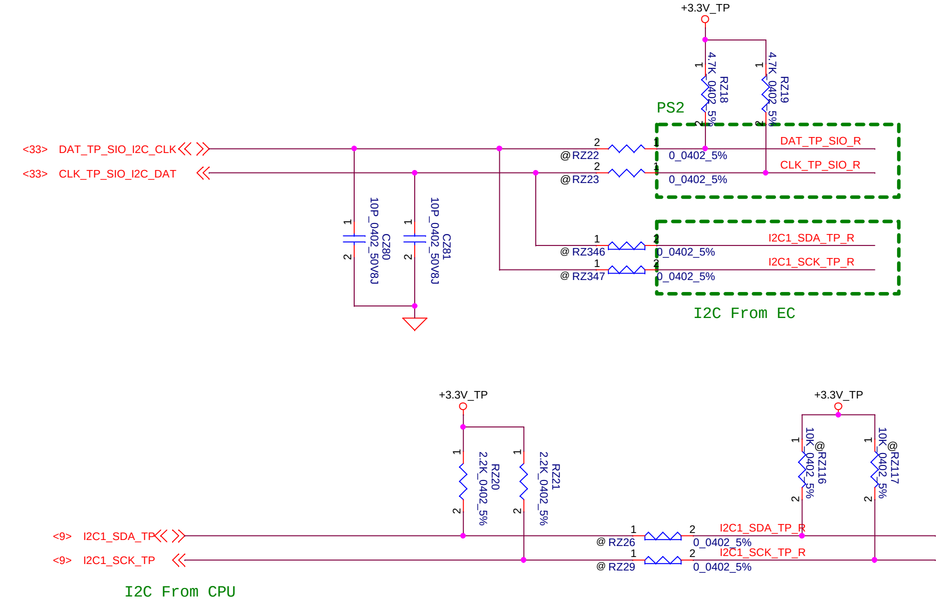
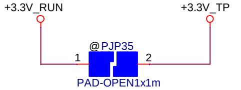
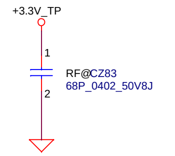
Touch Pad



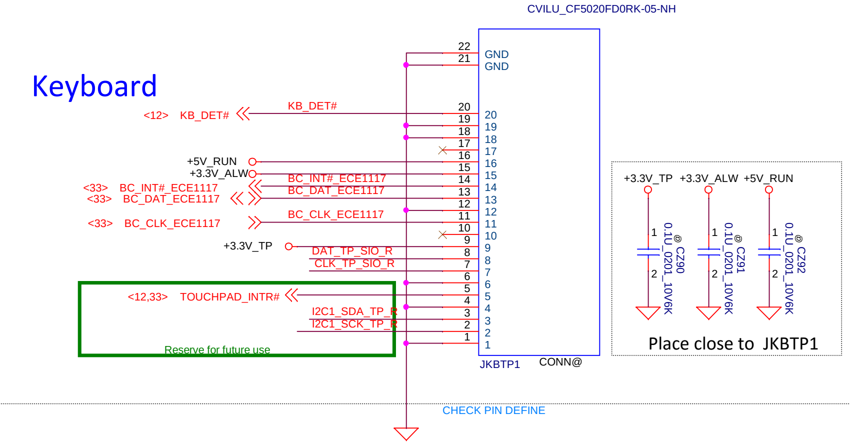
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues



RF Request



Keyboard



Update to LTCX007Q500 (DVT1.0)

@EDP Cable nonTS_HD-HD Cam

Part Number	Description
DC02C00DX00	H-CONN SET 1S1 MB-LCD-CAM HD NTS

@EDP Cable nonTS_FHD-HD Cam

Part Number	Description
DC02C00DW00	H-CONN SET 1S1 MB-LCD-CAM FHD NTS

@EDP Cable nonTS_FHD-IR

Part Number	Description
DC02C00DY00	H-CONN SET 1S1 MB-LCD-CAM FHD IR NTS

@EDP Cable TS_FHD-HD Cam

Part Number	Description
DC02C00E300	H-CONN SET 1S1 MB-LCD-CAM FHD TS

@EDP Cable infinity nonTS_FHD-3mm RGB

Part Number	Description
DC02C00DZ00	H-CONN SET 1S1 MB-LCD-CAM FHD INF NTS

@EDP Cable infinity TS_FHD-3mm RGB

Part Number	Description
DC02C00E400	H-CONN SET 1S1 MB-LCD-CAM FHD INF TS

@EDP Cable infinity TS_QHD-3mm RGB

Part Number	Description
DC02C00E500	H-CONN SET 1S1 MB-LCD-CAM QHD INF TS

@LED Cable

Part Number	Description
DC02002LY00	H-CONN SET 1S1 MB-LED/B

@FP FFC

Part Number	Description
NBX00023800	FFC 12P F P=0.5 PAD=0.3 66MM FP-USH 1S1

@TP FFC

Part Number	Description
NBX00023900	FFC 20P F P=0.5 PAD=0.3 118MM MB-TP 1S1

@USH Board FFC

Part Number	Description
NBX00023A00	FFC 26P F P=0.5 PAD=0.3 50MM MB-USH 1S1

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

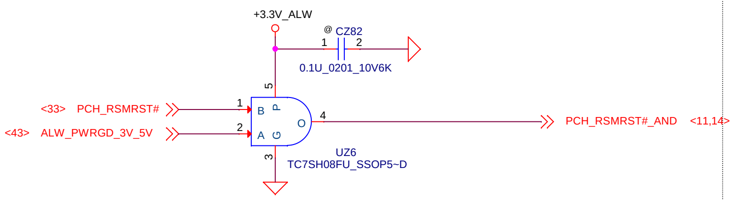
@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

RSMRST circuit



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Compal Electronics, Inc.
Title
Keyboard
Size Document Number
LA-E132P
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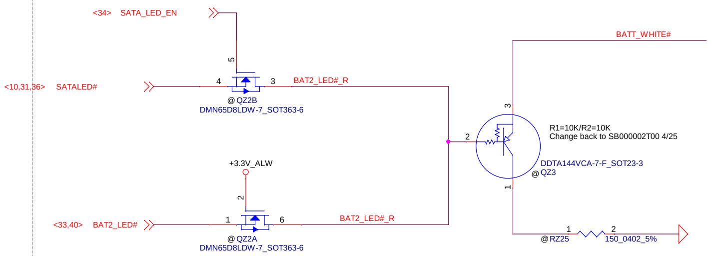
Date: Wednesday, November 09, 2016 Sheet 39 of 58

HDD LED MUX

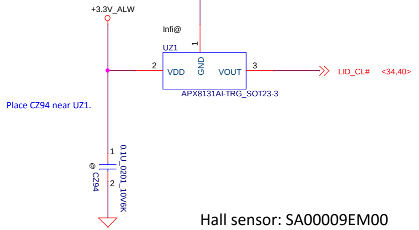
means EC can switch battery white led and HDD LED by hot key “Fn+H”



R1=10K/R2=10K
Change back to SB000002T00 4/25

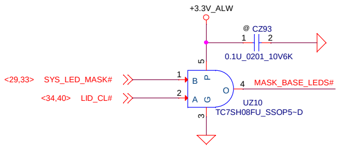
Battery LED

LID SWITCH



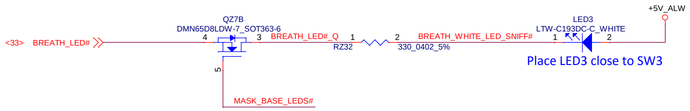
Place CZ94 near UZ1.

Hall sensor: SA00009EM00
(MAX hight is 1.45mm)



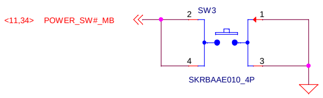
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

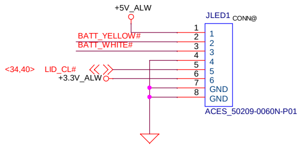


Place LED3 close to SW3

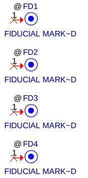
POWER & INSTANT ON SWITCH



LED board CONN

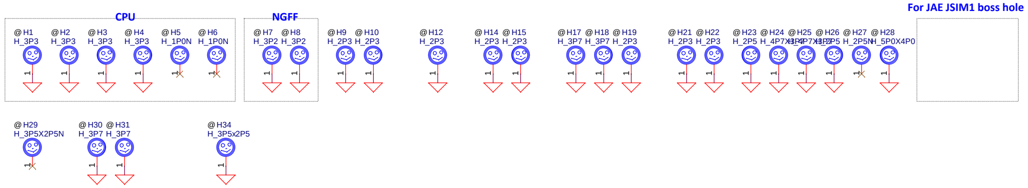


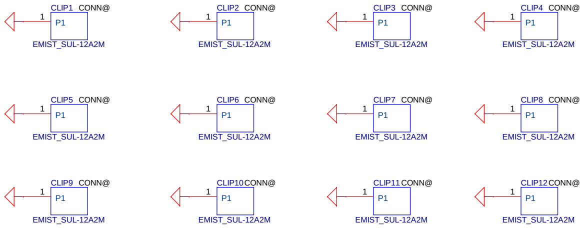
Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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Compal Electronics, Inc.
Title
PAD, LED
Size Document Number
LA-E132P
Rev 1.0
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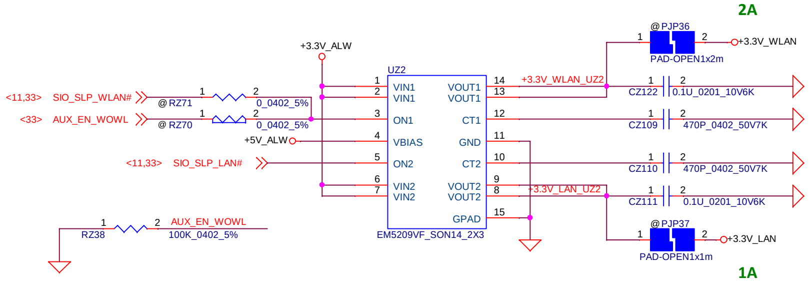
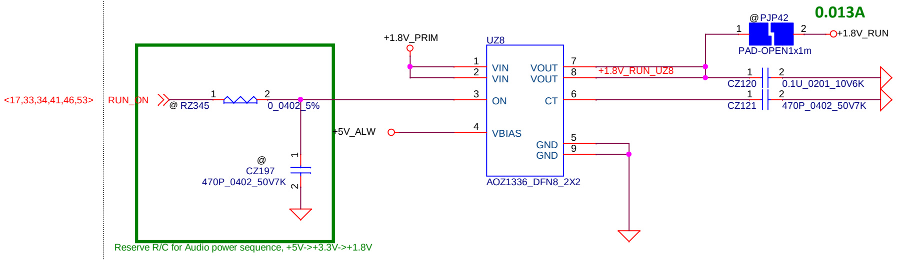
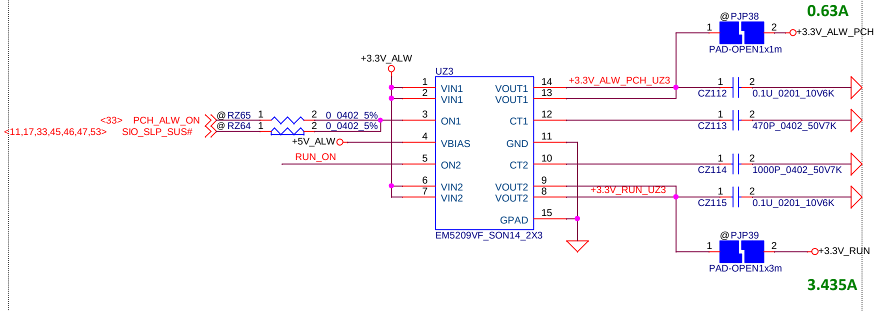
+3.3V_WLAN/+3.3V_LAN source



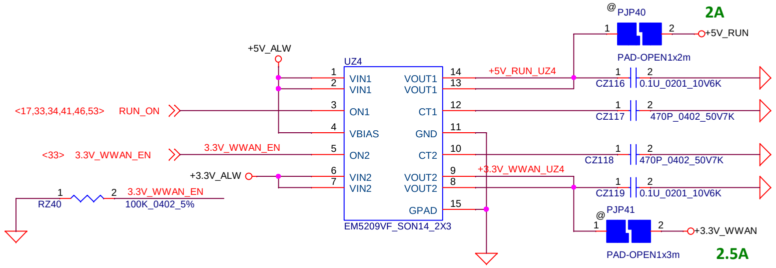
+1.8V_RUN source

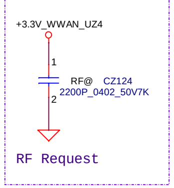


+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source





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	Compal Electronics, Inc.
Title	Power control
Size	Document Number LA-E132P
Rev	1.0
Date:	Wednesday, November 09, 2016
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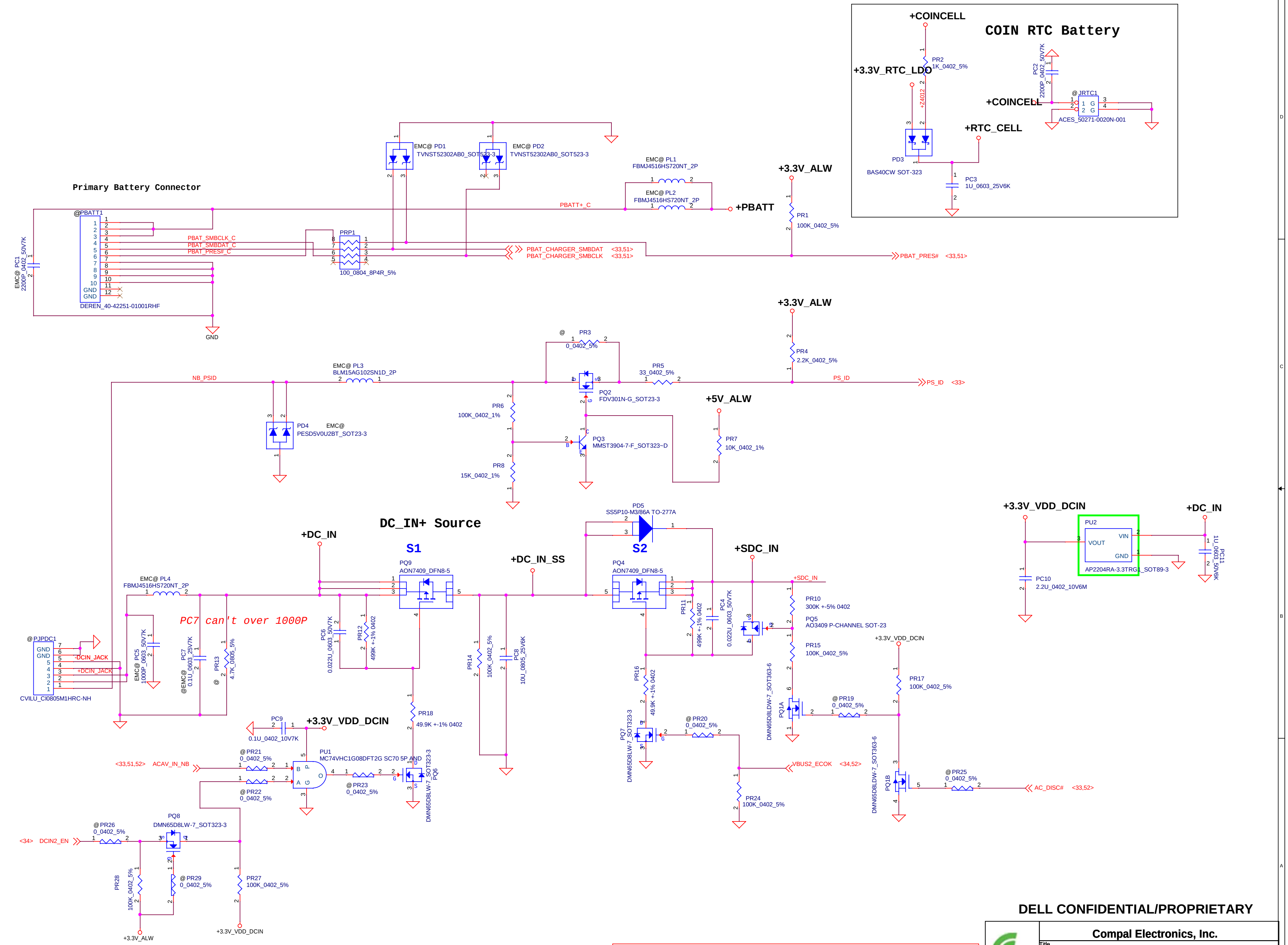

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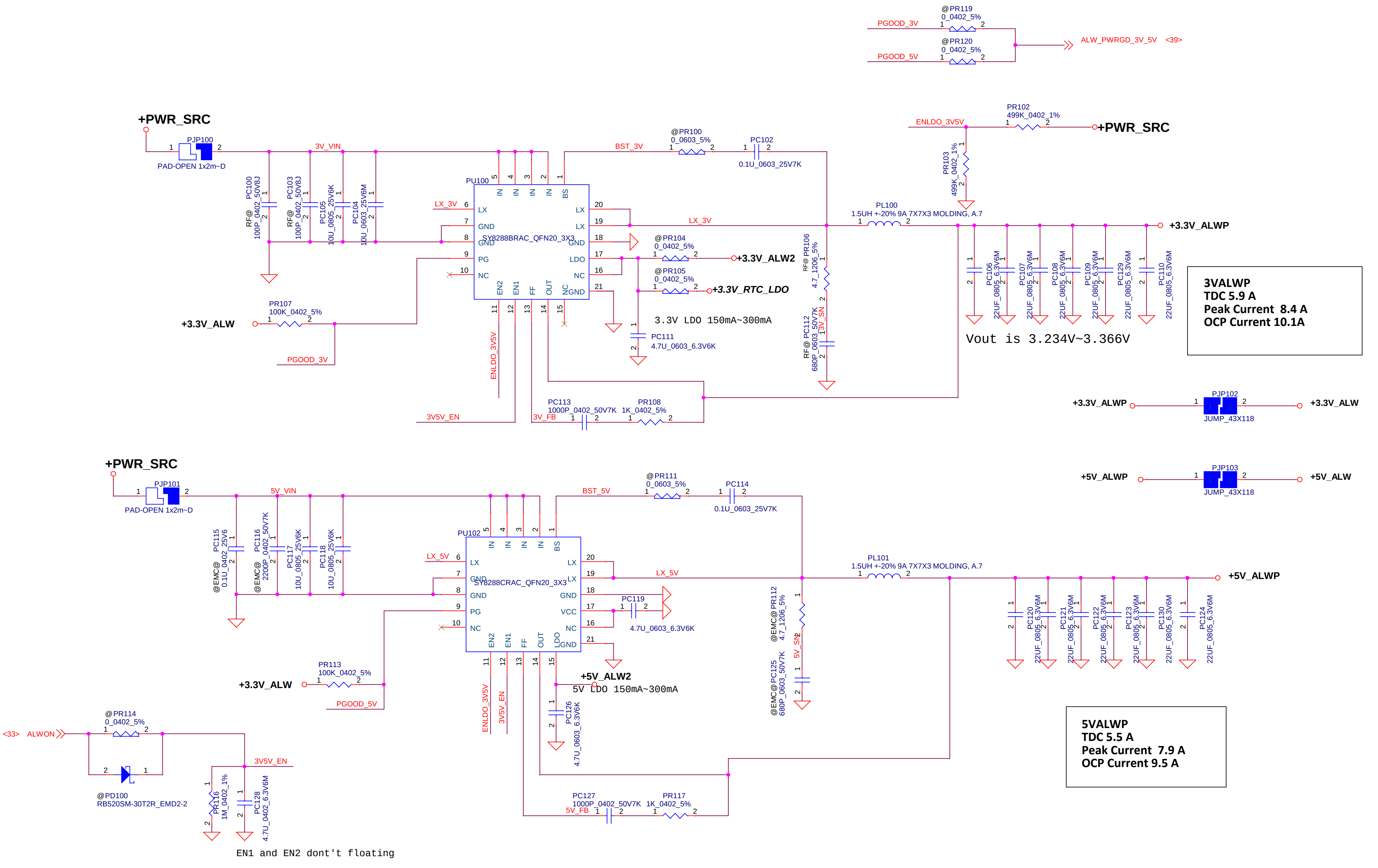
Compal Electronics, Inc.

Title
+DCIN

Size
Document Number
LA-E131P
Rev
1.0

Date: Wednesday, November 09, 2016



3VALWP
TDC 5.9 A
Peak Current 8.4 A
OCP Current 10.1A

5VALWP
TDC 5.5 A
Peak Current 7.9 A
OCP Current 9.5 A

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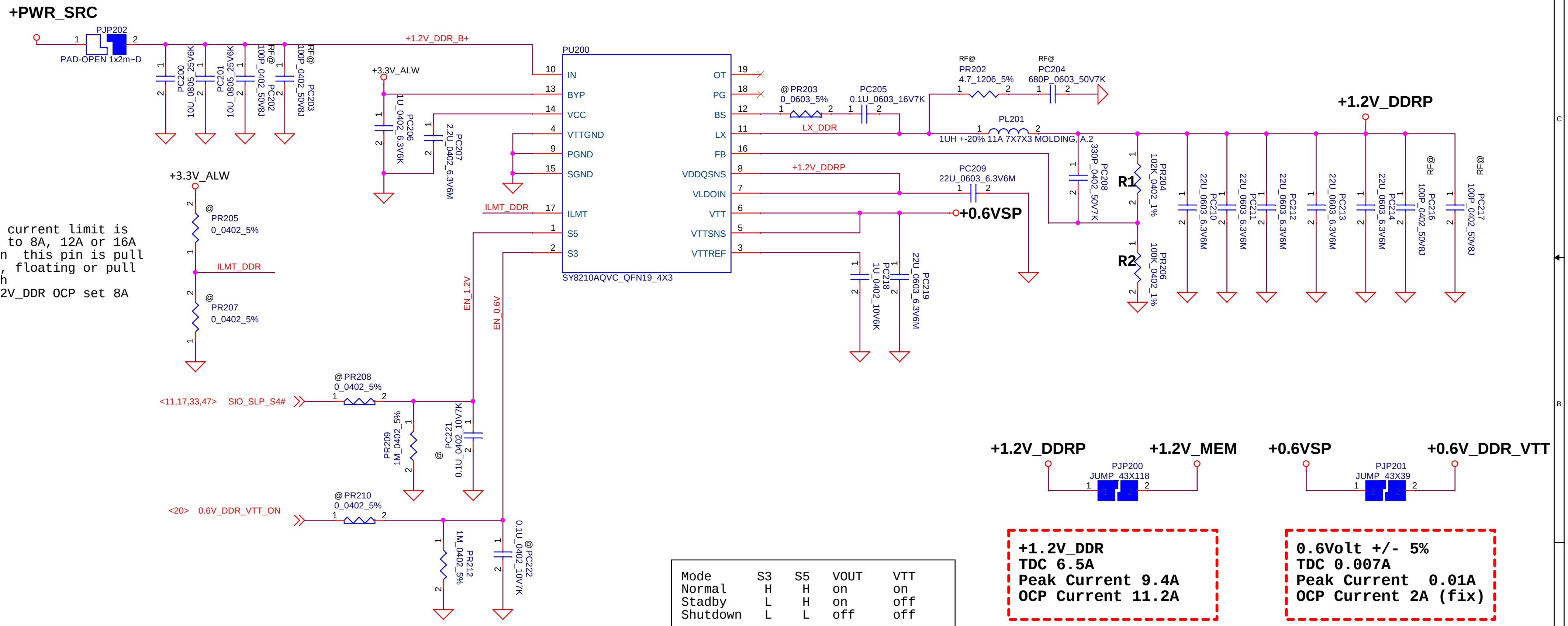
Compal Electronics, Inc.

Title
+5V_ALW/3.3V_ALW

Size Document Number Rev
LA-E131P 1.0

Date: Wednesday, November 09, 2016 Sheet 43 of 58



The current limit is
set to 8A, 12A or 16A
when this pin is pull
low, floating or pull
high
+1.2V_DDR OCP set 8A

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.5A
Peak Current 9.4A
OCP Current 11.2A

0.6Volt +/- 5%
TDC 0.007A
Peak Current 0.01A
OCP Current 2A (fix)

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Compal Electronics, Inc.
Title
+1.2V_MEN/+0.6V_DDR_VTT
Size Document Number
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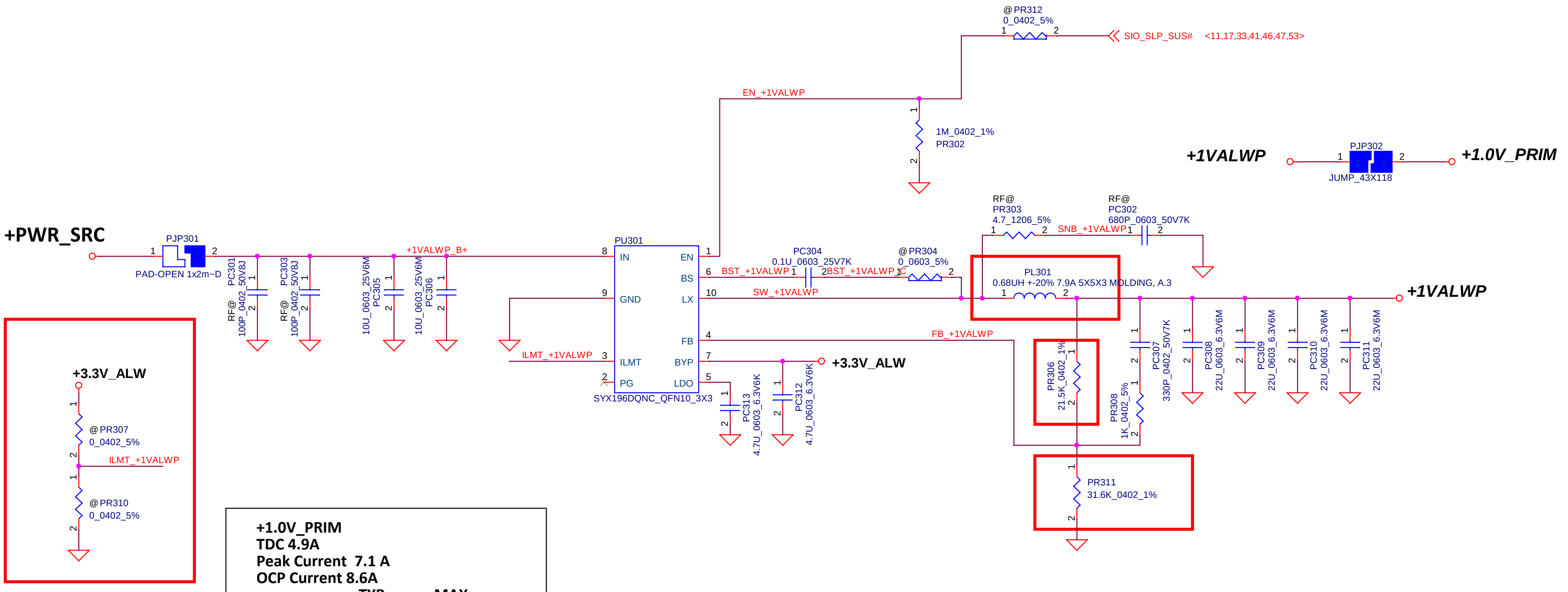
1.0
Date: Wednesday, November 09, 2016 Sheet 44 of 58



+1.0V_PRIM
TDC 4.9A
Peak Current 7.1 A
OCP Current 8.6A
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title
+1VALWP
Size
Document Number
LA-E131P
Rev
1.0
Date: Wednesday, November 09, 2016
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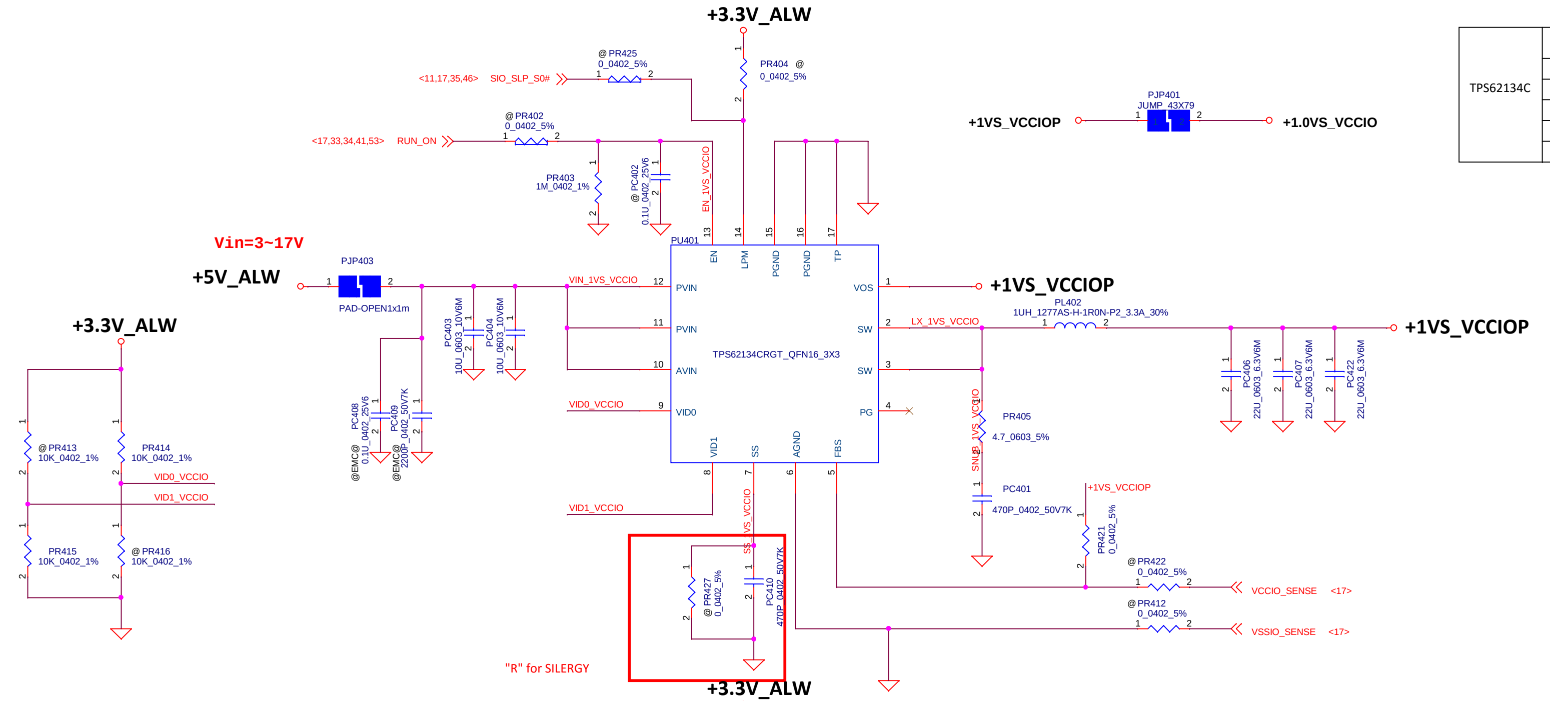
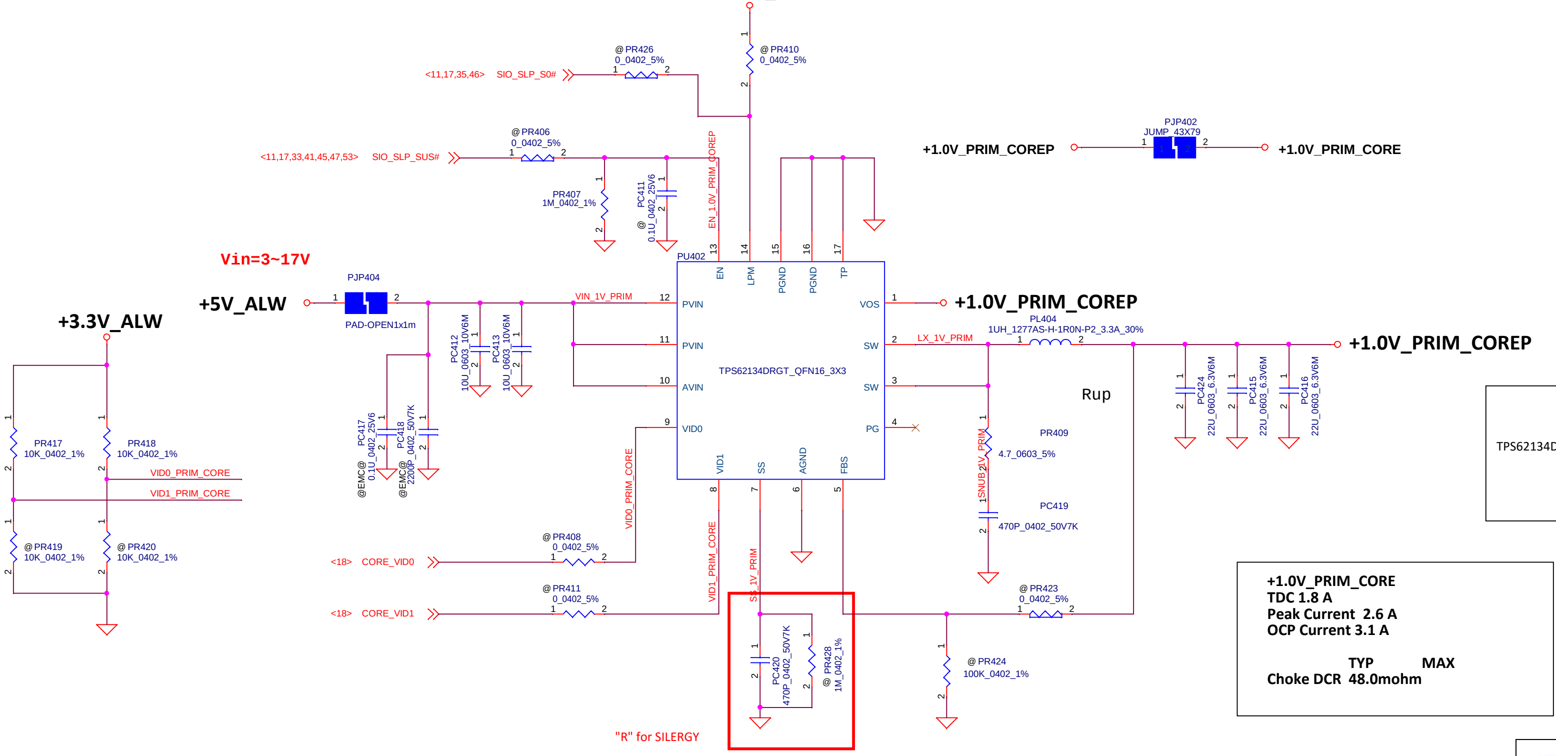




TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

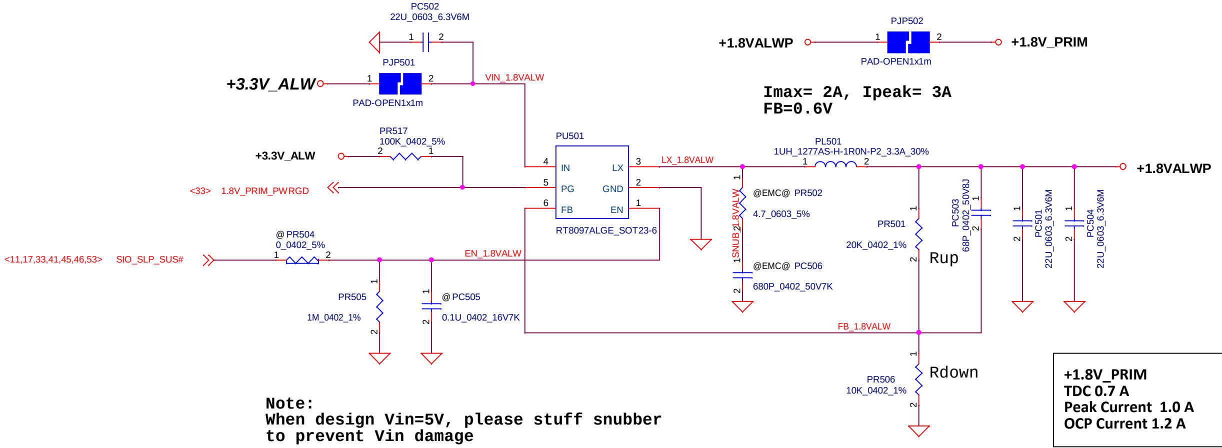
+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A
TYP MAX
Choke DCR 48.0mohm

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A
TYP MAX
Choke DCR 48.0mohm

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.
Title
+1VS_VCCIOP/+1.0V_PRIM_COREP
Size Document Number Rev
LA-E131P 1.0
Date: Wednesday, November 09, 2016 Sheet 46 of 58



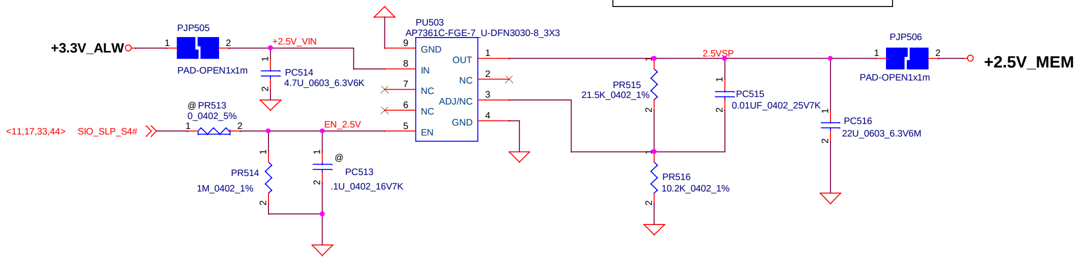
Imax= 2A, Ipeak= 3A
FB=0.6V

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

+1.8V_PRIM
TDC 0.7 A
Peak Current 1.0 A
OCP Current 1.2 A

+2.5V_MEN
TDC 0.3A by power budget
AP7361 U-DFN3030-8 Pd limit=1.7W
Peak loading=1.1A.
Pd=(3.3-2.5)*1.1=0.88W < 1.7W
OCP is 1.1~1.5A



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Title: **+1.8VALWP/+1.5VSP**		
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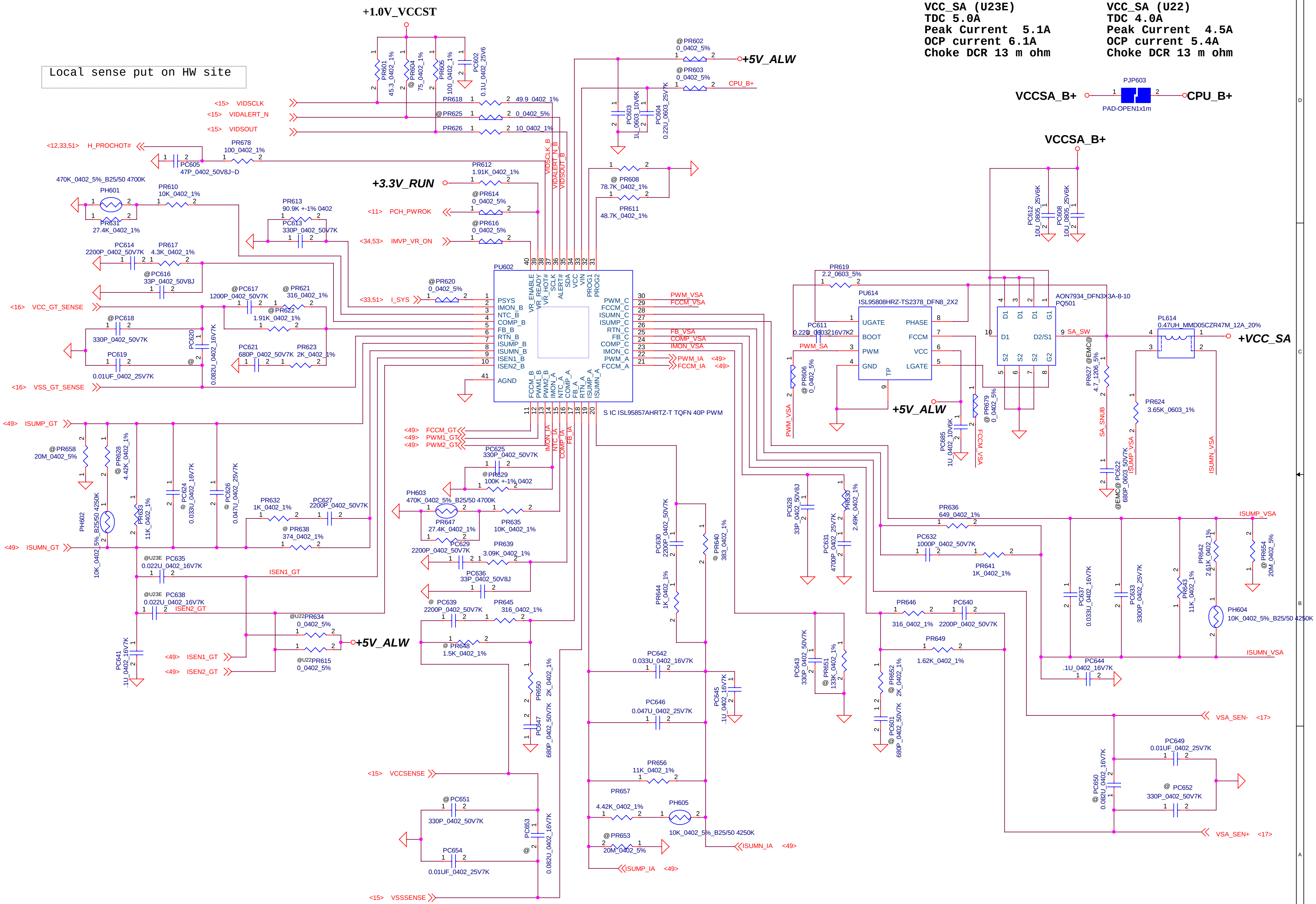
VCC_SA (U23E)
TDC 5.0A
Peak Current 5.1A
OCP current 6.1A
Choke DCR 13 m ohm

VCC_SA (U22)
TDC 4.0A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm

Local sense put on HW site



Local sense put on HW site

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Title **PWR_VCORE_ISL95857**		
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VCC_core (U22)
TDC 21A
Peak Current 32A
OCP current 38.4A
Choke DCR 0.9 +-7%m ohm

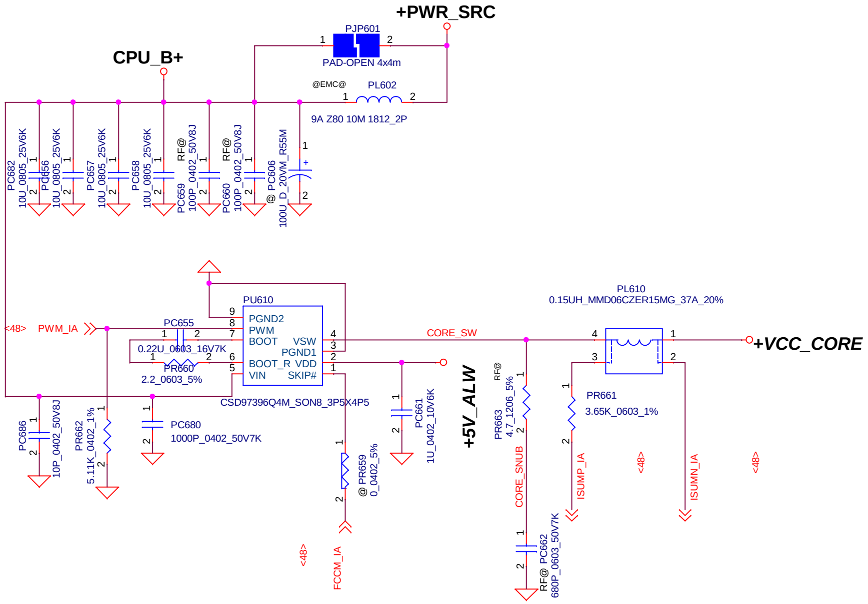
VCC_core (U23E)
TDC 22A
Peak Current 29A
OCP current 34.8A
Choke DCR 0.9 +-7%m ohm

U23E

PR628 @U23E	PR651 @U23E	PC626 @U23E	PR621 @U23E	PR608 @U23E	PR648 @U23E	PR622 @U23E
4.99K +-1% 0402	78.7K +-1% 0402	0.022U_0402_16V7K	1K +-1% 0402	100K +-1% 0402	1.5K +-1% 0402	2.55K_0402_1%
PR640 @U23E	PR638 @U23E	PR629 @U23E	PC624 @U23E	PC616 @U23E	PC617 @U23E	PC639 @U23E
383 +-1% 0402	470 +-1% 0402	86.6K +-1% 0402	0.1U 25V 0402	68P 50V J 0402	220P 50V 0402	2200P 50V 0402

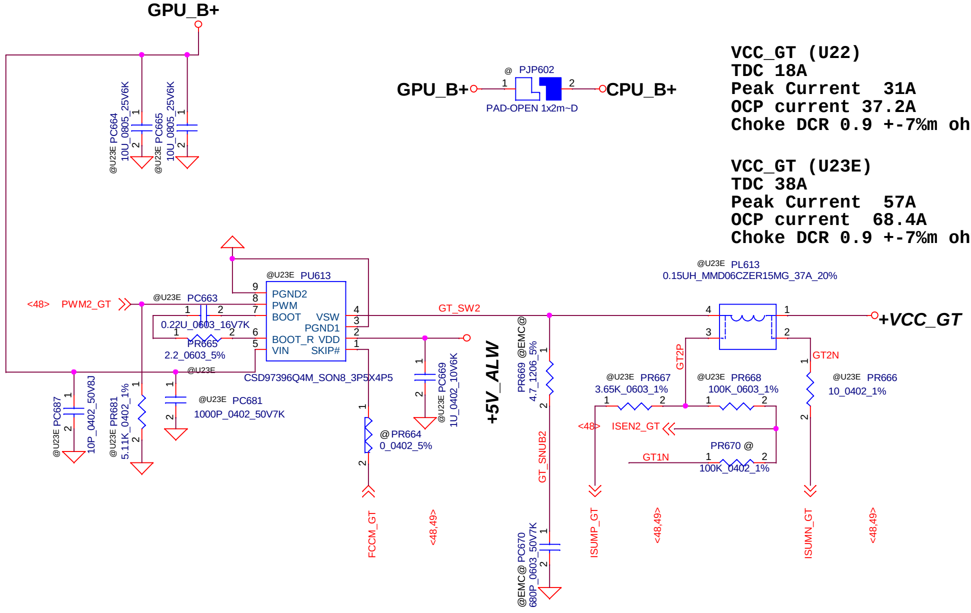
U22

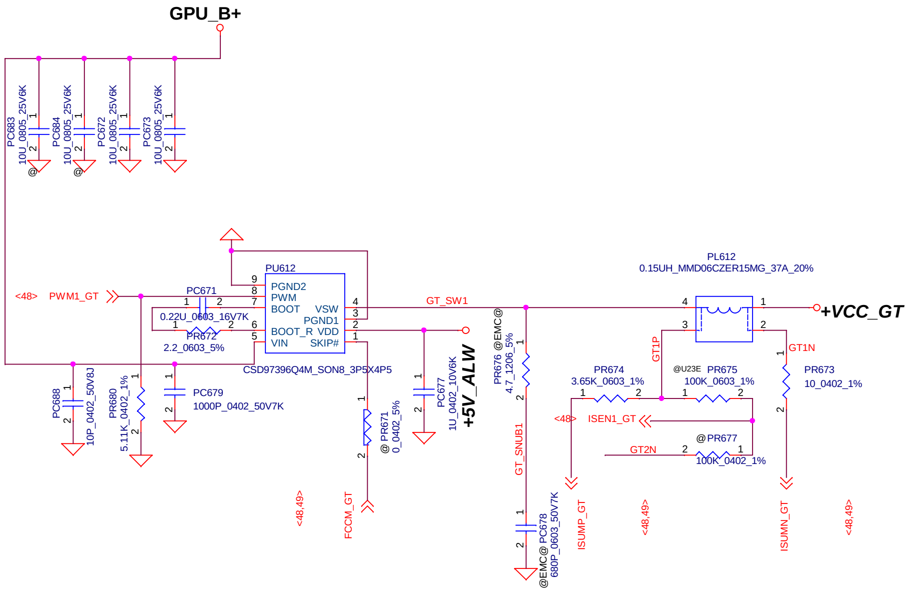
PR628 @U22	PR651 @U22	PC626 @U22	PR621 @U22	PR608 @U22	PR648 @U22	PR622 @U22
4.42K +-1% 0402	133K +-1% 0402	0.047U_0402_25V7K	316 +-1% 0402	78.7K +-1% 0402	1.5K +-1% 0402	1.91K +-1% 0402
PR640 @U22	PR638 @U22	PR629 @U22	PC624 @U22	PC616 @U22	PC617 @U22	PC639 @U22
383 +-1% 0402	374 +-1% 0402	100K +-1% 0402	.033U 16V 0402	33P 50V J 0402	1200P 50V 0402	1500P 50V K 0402



VCC_GT (U22)
TDC 18A
Peak Current 31A
OCP current 37.2A
Choke DCR 0.9 +-7%m ohm

VCC_GT (U23E)
TDC 38A
Peak Current 57A
OCP current 68.4A
Choke DCR 0.9 +-7%m ohm





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PWR_VCORE

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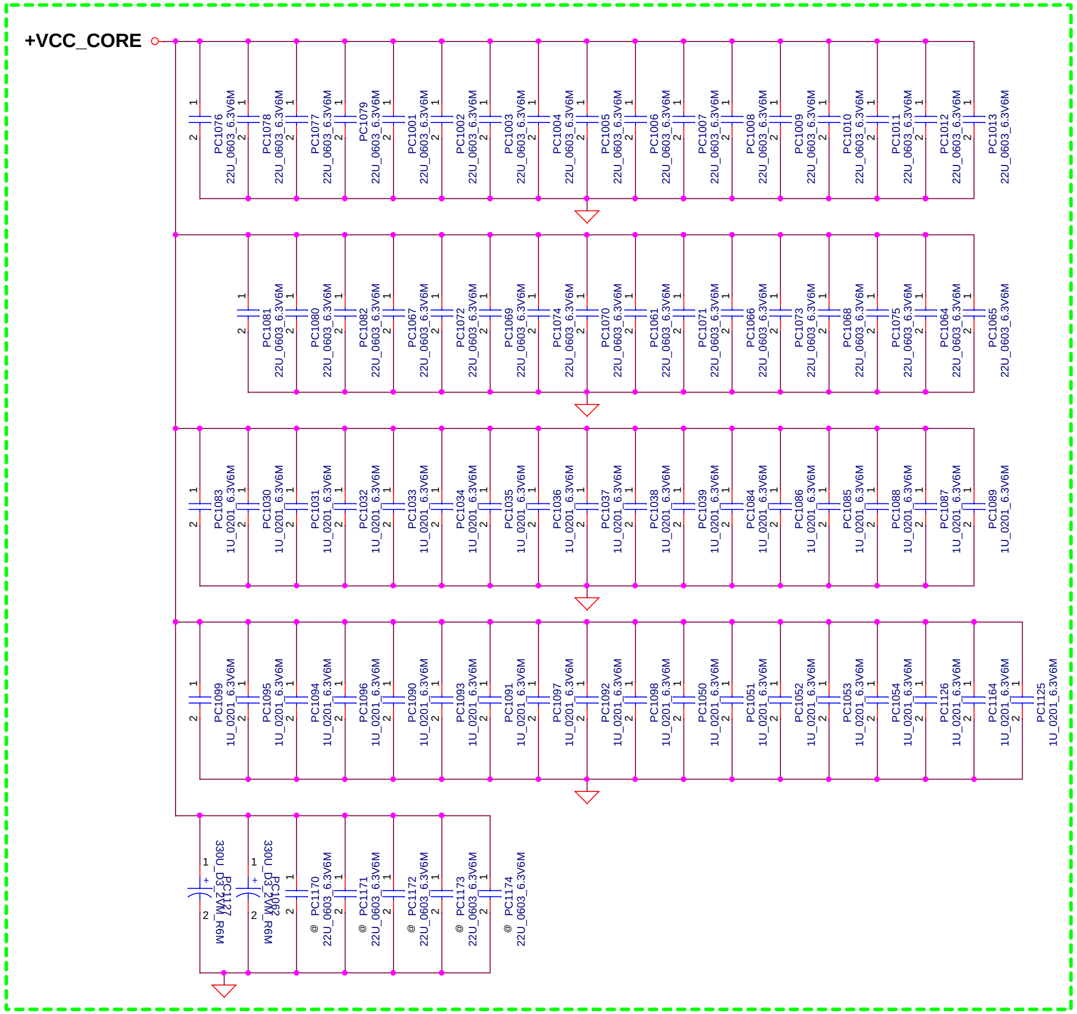
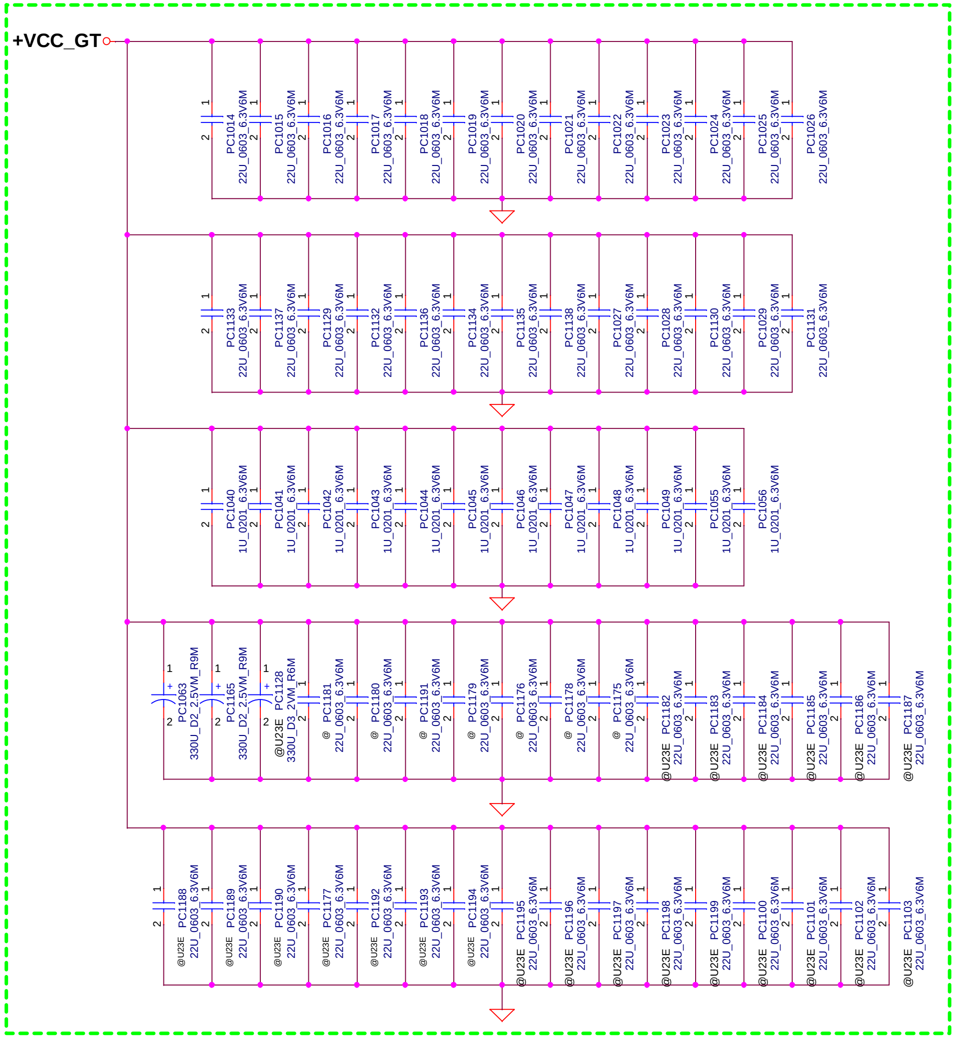
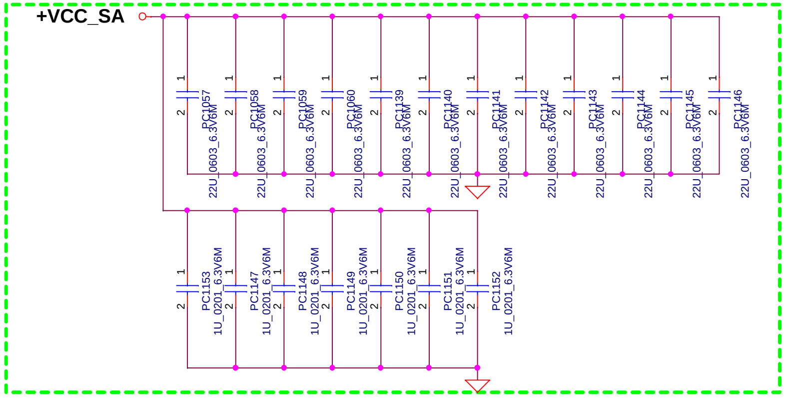
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs



VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs

VCC_GT Place on CPU (U23E)
22U_0603 * 48 pcs +1U_0201*12 pcs
+330u_D2*3 pcs





VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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PROCESSOR DECOUPLING

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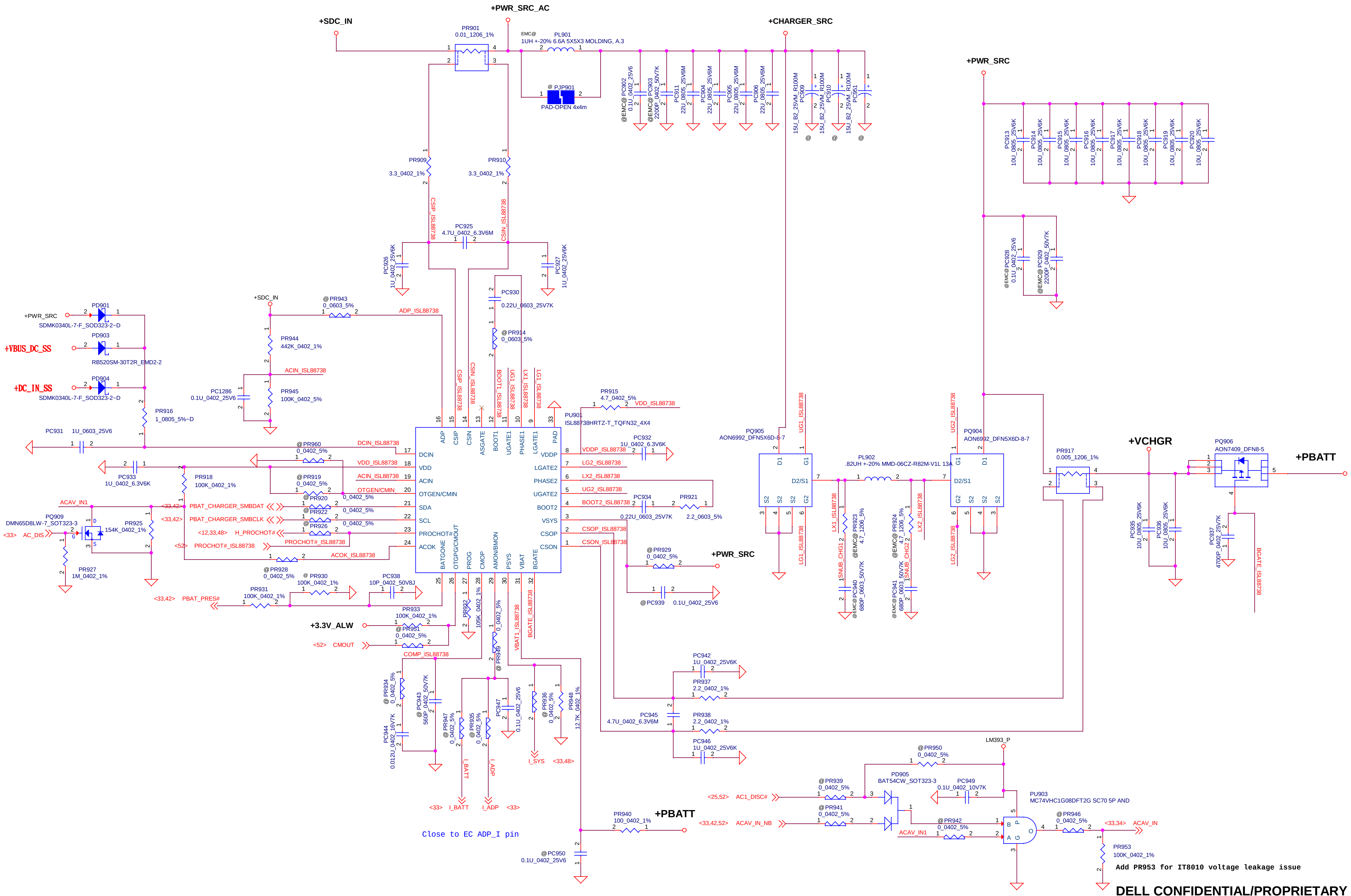

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Title	PWR CHGRGER ISL88738	
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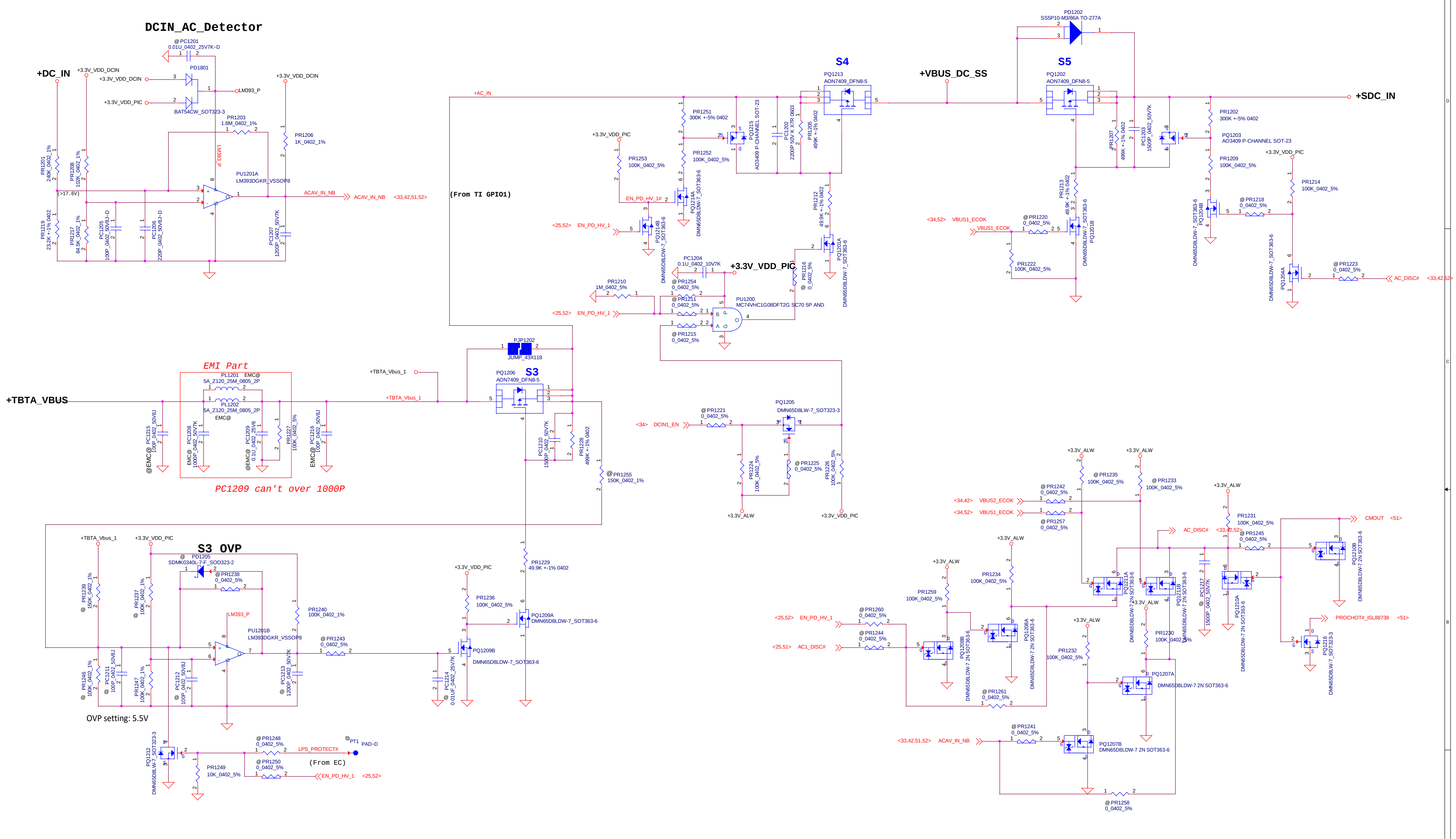

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Title
TypeC_PD
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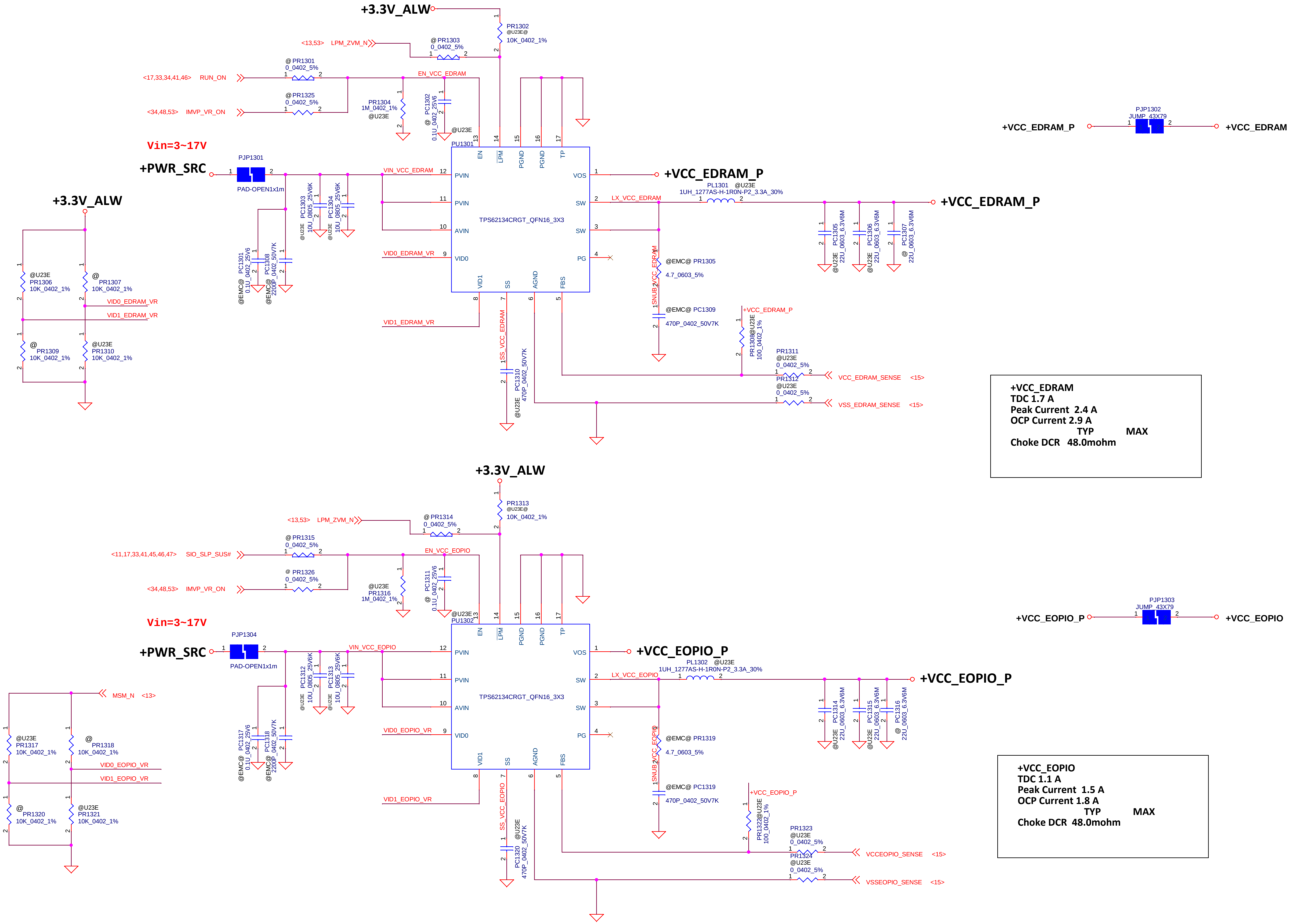

+VCC_EDRAM
TDC 1.7 A
Peak Current 2.4 A
OCP Current 2.9 A
TYP MAX
Choke DCR 48.0mohm

+VCC_EOPIO
TDC 1.1 A
Peak Current 1.5 A
OCP Current 1.8 A
TYP MAX
Choke DCR 48.0mohm

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PWR-VCCEDRAM/EOPIO

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	56	Change CPU VR version	2016 05/24	Compal	change solution version to fix PS4 funciton issue	change ISL95857HRTZ to ISL95857AHRTZ	X01
2	60	Change the S4 fast turn off circuit to avoid the leakage	2016 05/30	Compal	Change the S4 fast turn off circuit to avoid the leakage	Re-connect the PR1251.1 and PQ1215.3 from +VBUS_DC_SS to +AC_IN	X01
3	59	Add the Circuit for Multiple Input Detach detection & PROCHOT#	2016 05/30	Compal	Add the Circuit for Multiple Input Detach detection & PROCHOT#	Charger:Add PR960 and depop PR919 let the PU901.20 CMIN connect to GND. Add 1 net PROCHOT#_ISL88738 TypeC: Add PQ1216 to drive the PROCHOT# and PC1217 to do the reserve.	X01
4	50	MOS leakage problem	2016 05/30	Compal	To solve the MOS leakage problem to avoid the error active	PR12, PR11, PR1205, PR1207 and PR1228 change to 499K from 1M ohm PR16, PR18, PR1212, PR1213 and PR1229 change to 49.9K from 1M ohm PR10, PR1251 and PR1202 change to 300K from 100K ohm.	X01
5	60	Reserve the OVP function	2016 05/30	Compal	Reserve the OVP function to protect the typeC device.	Depop PJP1202, PR1255, PR1239, PR1246, PC1211, PR1237, PC1212, PD1205, PC1213, PC1214 and PR1248 Change the PR1247 from 200K_0402_1% to 100K_0402_5% ohm	X01
6	59	Decrease the charger input leakage voltage	2016 05/30	Compal	To decrease the charger input leakage voltage for TypeC AC	Change the PD903 from SCS0340L010 to SCS00006C00.	X01
7	51	Reduce footprint size for DFX request	2016 07/14	Compal	Reduce PC104 footprint size for DFX request	Change PC104 from 0805 change 0603 size for DFX request	X01
8	60	Fine tune the DC-IN detect voltage	2016 07/14	Compal	For Temp/Voltage test to fine tune the DC-IN detect voltage from 17.6V to 16.9V	PR1219 change from 22.6K to 23.2K. SD034232280	X02
9	59	Change Charger version	2016 07/14	Compal	Charger IC update version	1. Change the charger version to B version from A version 2. Change the PC926, PC927, PC942 and PC946 from @ to 1uF/0402_25V 3. Change the PC925 and PC945 from 1uF to 4.7uF/0402_10V. 4. Change the PR909 and PR910 from 1 Ohm to 3.3 Ohm. 5. Change the PR937 and PR938 from 1 Ohm to 2.2 Ohm. 6. Change the PC944 from 47nF to 12nF. 7. Change from PR932 from 118K to 105K 8. Change PD901 pull up source from +PBATT to +PWR_SRC 9. Add PC1286 0.1U_0402_25V	X02
10	57	Location Alignment	2016 07/20	Compal	Location Alignment	VCCSA change the PU606 to PU614 and PL601 to PL614 IA change the PU603 to PU610 and PL603 to PL610 GT change the PU604 to PU612 and PL604 to PL612	X02
11	56	SA OVP	2016 08/29	Compal	SA OVP when C status change	1. Change the PL614 from 1uH to 0.47uH 2. Change the PR651 from 124K to 133K 3. Change the PR636 from 1.24K to 649 4. Change the PC633 from 6800p to 3300p 5. Change the PR630 from 7.32K to 2.49K 6. Change the PC628 from 10p to 33p 7. Change the PC632 from 2200p to 1000p 8. Change the PC631 from 1200p to 4700p 9. Remove PC601 & PR652	X02
12	59	S5 power consumption	2016 08/29	Compal	S5 Power consumption fail because UE1 pin C7 has leakage	Add PR952 pull down 100K resistor to discharge UE1 pin C7 leakage	X02
13	54	Enable LPM mode	2016 08/29	Compal	Enable PRIM_CORE low power mode	Remove : PR410 Stuff : PR426	X02
14	51	For EMI request	2016 09/08	Compal	Add some parts for EMI request	stuff : PR106,PR202,PR303,PR663 stuff : PC112,PC204,PC302,PC662 stuff : PC100,PC103,PC202,PC203,PC216,PC217,PC301,PC303,PC659,PC660 stuff : PL901	X03
15	60	Modify symbol to 2nd source	2016 09/08	Compal	Modify PD1202,PD5 to 2nd source because vendor EOL	Modify PD1202,PD5 to 2nd source(SCS00005X00) because vendor EOL	X03
16	57	For U23e CPU modify	2016 09/23	Compal	Modify PR628 / PC626 value after Intel Validation test for U23e CPU	1. Change the PR628 from 2.61K to 4.99K for U23 CPU 2. Change the PC626 from 0.047u to 0.022u for U23 CPU 3. Change the PR622 from 2.49K to 2.55K for U23 CPU 4. Change the PR651 from 82K to 78.8K for U23 CPU	X03
17	51	Reserve symbol footprint	2016 09/26	Compal	Reserve symbol 3 pcs footprint	1. Reserve symbol PD100 footprint for 3V/5V enable 2. Reserve PR1325 / PR1326 footprint for sequence	X03
18	61	Enable LPM mode	2016 09/26	Compal	Enable EDRAM / EOPIO low power mode	1. Un-pop : PR1302 / PR1313 2. Stuff : PR1303 / PR1314	X03
19	59	Max. Power up to 125W	2016 09/26	Compal	Modify PR948 value for Max. Power 125W	1. Change the PR948 from 10.5K to 12.7K	X03
20	51	Type-C connector voltage droop	2016 10/05	Compal	Type-C connector voltage droop	Add PR121 0 ohm for Type-C connector voltage droop issue	X04
21	54	VCCIO design modify	2016 10/05	Compal	VCCIO design modify	1. VCCIO use local sense: PR421 change to 0 ohm, de-pop PR422,PR412 2. VCCIO change to 0.95V: De-pop PR413,PR416, pop PR415,PR414	X04
22	54		2016 11/02	Compal	Delete reserve resistor	Delete PR121	A00
23							

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Title: PWR P.I.R
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Version Change List (P. I. R. List)   *LA-E132P*

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	[Type C]PD Controller TI	2016/05/23	EE	UT5.D6 need to PD for TI suggestion	Pop RT101	0.2(X01)
2	24	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	TI TUSB546 sample change to ES3	Chagne UT9 from SA00009R700 to SA00009R710	0.2(X01)
3	25	[Type C]PD Controller TI	2016/05/23	EE	Schematic align	Add net name UT5.B2 : MUX1_FLIP_SEL_R UT5.C2 : EN_PD_HV_1_R UT5.D10 : PD1_GPIO2 UT5.G11 : AC1_DISC#_R UT5.C10 : SW2_DP1_HPD_R UT5.E10 : OTG_ID UT5.G10 : PD1_GPIO6 UT5.D7 : PD1_GPIO7	0.2(X01)
4	26	[Type C]PD Power	2016/05/23	EE	TypeC PD solution (dead battery mode)	RT111 change from 10K to 100K (SD028100380) CT90 change from 100P to 1U (SE00000QL10)	0.2(X01)
5	32	Codec ALC3246	2016/05/23	EMI	EMI request	CA2/CA3 change from 2200P to 330P (SE000006I80)	0.2(X01)
6	24	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	DP_AUX go through PD ,not TUSB546	Depop RT132, RT133, CT115, CT116	0.2(X01)
7	25	[Type C]PD Controller TI	2016/05/23	EE	DP_AUX go through PD ,not TUSB546	Pop RT108, RT109, CT80, CT81	0.2(X01)
8	40	PAD, LED	2016/05/23	EE	Remove HDD LED MUX feature	Add RZ361 and depop QZ3, QZ2, RZ25	0.2(X01)
9	24	DP/USB3 Repeater SW TUSB546	2016/05/23	EE	Disable AUX snoop feature	Pop RT308	0.2(X01)
10	33	EC MEC5105	2016/05/23	EE	Schematic align	Add net VCI_IN1# and add PU RE507 Add net VCI_IN2# and add PU RE508	0.2(X01)
11	35	USH & TPM	2016/05/23	EE	Atmel request for current TPM silicon	Add CZ74 (pop) and RZ72(depop) for UZ12.7	0.2(X01)
12	9	CPU (4/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Add net MEDIACARD_IRQ# to UC1.AN8	0.2(X01)
13	30	Card Reader	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Cardreader schematic change from RTS5330 (USB) to RTS5242 (PCIE)	0.2(X01)
14	10	CPU (5/14)	2016/05/23	EE	Cardreader change to RTS5242 (PCIE)	Change net from USB3.0 port 5 to PCIE port1 Delete USB2.0 port 6	0.2(X01)
15	10	CPU (5/14)	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Change net from PCIE port 10 to SATA port1	0.2(X01)
16	11	CPU (6/14)	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Assign CLKREQ_PCIE#0 to Cardreader	0.2(X01)
17	31	NGFF Card	2016/05/23	EE	No support M.2 3042 (HCA), but keep SATA cache for nonAR config	Change net from PCIE port 10 to SATA port1	0.2(X01)
18	36	M2 2280 Socket	2016/05/23	EE	Remove HDD LED MUX feature	Depop RN100	0.2(X01)
19	31	NGFF Card	2016/05/23	EE	Remove HDD LED MUX feature	Depop RN101	0.2(X01)
20	33	EC MEC5105	2016/05/23	EE	PORT80_DET#	Change location RE510 to RE512 Reserve RE513 100k (SD028100380) to GND	0.2(X01)
21	6	CPU (1/14)	2016/05/23	EE	Follow Intel PDG AUX topology	Delete RC179/RC180/RC181/RC182 Add test point T281/T282 for CPU_DP1_AUXN and CPU_DP1_AUXP	0.2(X01)
22	17	CPU (12/14)	2016/05/23	EE	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)

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Title
EE P.I.R (1/4)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	33	EC MEC5105	2016/05/24	EE	Schematic align	Delete RE506 and reserve PD 100K RE95 for TBT_RESET_N_EC_R	0.2(X01)
24	33	EC MEC5105	2016/05/25	EE	Symbol pin name change	UE1.C1 pin name change to GPIO024_nRESETI	0.2(X01)
25	25	[Type C]PD Controller TI	2016/05/25	EE	Symbol pin name change	UT5.A6/A7/A8/B7 pin name change to GND, UT5.D6 pin name change to HRESET	0.2(X01)
26	24	DP/USB3 Repeater SW TUSB546	2016/05/25	EE	Symbol pin name change	UT9.29 pin name change to SNK_CAD/DCI_DAT UT9.32 pin name change to HPDIN/DCI_CLK	0.2(X01)
27	35 39	USH & TPM Keyboard	2016/05/25	ME	Connector update	JUSH1 change to LTCX007Q600 JKBTP1 change to LTCX007Q500	0.2(X01)
28	40	PAD, LED	2016/05/25	ME	MB ME drawing change	Remove H11 and change H28 to H_5P0X4P0	0.2(X01)
29	6	CPU (1/14)	2016/05/31	EE	DP HPD base on INTEL PDG	Delete RC312/RC242	0.2(X01)
30	24	DP/USB3 Repeater SW TUSB546	2016/05/31	EE	Schematic align	SW2_DP1_HPD Add RT380 place near TUSB546	0.2(X01)
31	31	NGFF Card	2016/06/01	EE	Intel reviwe result	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603 CZ32/CZ31/CZ29 place near JNGFF1.2/JNGFF1.4 CZ27/CZ30/CZ28 place near JNGFF1.72/JNGFF1.74	0.2(X01)
32	29	LAN Clarkvillie & RJ45	2016/06/01	EE	EMI request	Change CL22 from 1500P to 150P (SE00000FA80)	0.2(X01)
33	32	Codec ALC3246	2016/06/01	EE	Audio EA modify (meet GS mark)	Change RA7, RA8 from 24.9ohm to 16.2ohm (SD00001U900)	0.2(X01)
34	11	CPU (6/14)	2016/06/01	EE	Crystal EA modify	Change CC21, CC22 from 15pf to 12pf	0.2(X01)
35	35	USH & TPM	2016/06/01	EE	TPM change to Nuvoton NPCT650JBAYX	All page	0.2(X01)
36	35	USH & TPM	2016/06/04	EE	Vendor schematic review	UZ12 change to NPCT650JB2YX (SA00008EL70) Add CZ75 4.7uF (SE00000SO00) for +UZ12_TPM	0.2(X01)
37	12	CPU (7/14)	2016/06/04	RF	Intel MOW request	Add CC331 2.2PF (SE07122AC80) for HDA_RST# Add CC332 2.2PF (SE07122AC80) for HDA_SDIN0 Add CC333 2.2PF (SE07122AC80) for HDA_SDOUT	0.2(X01)
38	31	NGFF Card	2016/06/04	RF	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
39	32	Codec ALC3246	2016/06/04	ESD	ESD request	Change LA10, LA11 to SM01000OZ00	0.2(X01)
40	28	eDP CONN& Touch screen	2016/06/04	EMI	EMI request	Change LV1 to SM01000NY00	0.2(X01)
41	31	NGFF Card	2016/06/06	EE	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
42	13 18	CPU (8/14) CPU (13/14)	2016/06/06	EE	For RF noise issue layout modify-SB14 only	Change CC213 to 0201 size (SE00000YB00) and remove T14	0.2(X01)
43	35	USH & TPM	2016/06/07	EE	Schematic align	Change loaction RZ90 to RZRZ362	0.2(X01)
44	23	USH & TPM	2016/06/14	EE	TPM pre-config	Reserve RZ363 ohm for GPIO2 and SIO_SLP_S3#	0.2(X01)
45	35	DP/USB3 Repeater SW TUSB546	2016/06/14	EE	Schematic align	Change net name from MUX1_LP_EN to AUX1_SNOOP_EN#	0.2(X01)
46	12	CPU (7/14)	2016/06/14	RF	RF request	Change CC27 from 22pf to 47pf (SE071470J80)	0.2(X01)

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Title: **EE P.I.R (2/4)**

Size | Document Number: **LA-E132P** | Rev 1.0

Version Change List (P. I. R. List)   LA-E132P

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
47	22	HDMI CONN	2016/06/14	EMI	EMI request	Change RV33,RV34 to 12nH (SHI0000PJ00) Change RV24,RV25,RV27,RV28,RV30,RV31 (SHI0000QS00) Change RV26,RV29,RV32,RV35 to SHI0000PJ00 to 300ohm (SD028300080)	0.2(X01)
48	20	DDR4	2016/06/14	EE	2nd source align	Change UD1 from SA00007WE00 to SA00007UR00	0.2(X01)
49	24	DP/USB3 Repeater SW TUSB546	2016/06/14	EE	2nd source align	Change LT11 from SM01000MS00 to SM01000MO00	0.2(X01)
50	33	EC MEC5105	2016/07/13	EE	For MEC5105K-D1-TN EC sample	Change UE1 to SA00009GL00 & Depop RE361,Pop RE360,RE362	0.3(X02)
51	35	USH & TPM	2016/07/13	EE	TPM pre-config	Pop RZ363 and depop (@) RZ111,RZ112, RZ113,QZ9	0.3(X02)
52	34	EC MEC5105 Support	2016/07/13	EE	Board ID	Change RE79 to 62Kohm (SD028620280)	0.3(X02)
53	33	EC MEC5105	2016/07/13	EE	GPIO map update	1.UE1.F11 add RTCRST_ON_GPIO122 & reserve RE515@ to QE12.2 2.UE1.B6 change to RTCRST_ON_GPIO141 and add RE514 to QE12.2	0.3(X02)
54	32	Codec ALC3246	2016/07/13	EE	ESD request (2nd source align)	Change LA10, LA11 back to SM01000NA00	0.3(X02)
55	35	USH & TPM	2016/07/13	EE	USH BOM modify	1.RZ10 changed to 100K -Let USH_PWR_STATE# keep low at S5 2.DZ7 depop and pop RZ87 - X8 have no difference JUSH1 pin define with X7	0.3(X02)
56	31	NGFF Card	2016/07/13	EE	Symbol error	Re-link JSIM1 symbol and change SIM_DET to JSIM1.2	0.3(X02)
57	25	[Type C]PD Controller TI	2016/07/13	EE	For PD sample	Change UT5 from SA00009W200 to SA00009W210	0.3(X02)
58	34	EC MEC5105 Support	2016/07/13	EE	Vendor schematic review	Add net WRST# to UE2.4 and CE500 1uf (SE000000K80)	0.3(X02)
59	22	HDMI CONN	2016/07/13	EMI	EMI request	1. Change RV24 to LV31, RV25 to LV32, RV27 to LV33, RV28 to LV34, RV30 to LV35, RV31 to LV36 and from SHI0000QS00 to SHI0000QT00 2. Change RV33 to LV37, RV34 to LV38 and from SHI0000PJ00 to SHI00006Q00	0.3(X02)
60	11	CPU (6/14)	2016/07/18	EE	Sync up schematic with AR	Add PU RC190 to CLKREQ_PCIE#5	0.3(X02)
61	40	PAD, LED	2016/07/20	EE	Intel suggestion	H5, H6 cnage from 1.1mm to 1.0mm	0.3(X02)
62	28	eDP CONN & Touch screen	2016/07/20	ME	Factory request	Change JIR1 to SP01001YO00 to avoid JTS1 and JIR1 assembly error	0.3(X02)
63	29	LAN Clarkvillie & RJ45	2016/07/21	EMI	EMI request	Change CL22 from 150P to 10P (SE167100J80)	0.3(X02)
64	34	EC MEC5105 Support	2016/07/21	EE	Vendor schematic review	Add RE523 0 ohm for UE2 power pin soft start	0.3(X02)
65	28	eDP CONN & Touch screen	2016/07/22	ESD	ESD request	Reserve the ESD diode DV7 on USB20_N5 and USB_P5 for system damage issue	0.3(X02)
66	28	eDP CONN & Touch screen	2016/07/25	ESD	ESD request (layout limit)	Change DV7 to DV7 and DV8 (SC40000AR00)	0.3(X02)
67	33	EC MEC5105	2016/07/25	EE	Vendor schematic review	Change RPE12.1 to RE524 (10Kohm) for EXPANDER_GPU_SMDAT Change RPE12.2 to RE524 (10Kohm) for EXPANDER_GPU_SMCLK	0.3(X02)
68	26	[Type C]PD Power	2016/07/25	EE	For UT7 2nd source issue	Add RT393 PD 100K ohm to +5V_PD_VDD for discharging instantly	0.3(X02)
69	34	EC MEC5105 Support	2016/08/01	EE	Vendor schematic review	Change RE14,RE15,RE18 from 100k ohm to 10k ohm	0.3(X02)
70	39	Keyboard	2016/08/01	EE	Touchpad I2C EA	Chagne RZ20, RZ21 from 4.7k ohm to 2.2k ohm Change CZ80, CZ81 from 330pf to 10pf	0.3(X02)
71	14	CPU (9/14)	2016/08/01	EE	Intel suggestion	Change RC137 from 1k ohm to 3k ohm	0.3(X02)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
72	11	CPU (6/14)	2016/08/01	EE	Intel suggestion	Depop RC190	0.3(X02)
73	35	USH & TPM	2016/09/06	EE	TPM change NPCT650VB2YX	Change UZ12 from to SA00008EL70 to SA00008EL80	0.4(X03)
74	34 33	EC MEC5105 Support EC MEC5105	2016/09/06	EE	Expander I/O change to Microchip MCP23008	Change UE2 from SA00009VL00 to SA0000ADQ00, remove RE523 Change RE524, RE525 from 10Kohm to 2.2Kohm	0.4(X03)
75	34	EC MEC5105 Support	2016/09/06	EE	Board ID	Change RE79 to 33kohm (SD028330280)	0.4(X03)
76	34	EC MEC5105 Support	2016/09/06	EE	EC watchdog reserve	Add QE13,RE530,RE531	0.4(X03)
77	33	EC MEC5105	2016/09/06	EE	Schematic align	Reserve RE526(10K) PU for USH_DET# to +3.3V_ALW	0.4(X03)
78	33	EC MEC5105	2016/09/08	EE	EC request for GPIO setting	Reserve RE505 PU for LOM_CABLE_DETECT# Add RE532 PU for BCM5882_ALERT#	0.4(X03)
79	35	USH & TPM	2016/09/13	EE	EC request for GPIO setting	Pop RZ8, RZ9 for USH_SMBCLK and USH_SMBDAT	0.4(X03)
80	34	EC MEC5105 Support	2016/09/13	EE	EC watchdog delete	Delete QE13,RE530,RE531	0.4(X03)
81	32	Codec ALC3246	2016/09/13	RF	RF request	Pop CA54 82pf for DMIC_CLK0	0.4(X03)
82	34	EC MEC5105 Support	2016/09/26	EE	Dell request	Reserve RE536/RE537 for resistors for PCH_DPWROK circuit	0.5(X04)
83	33	EC MEC5105	2016/09/26	EE	WDT schematic option 2	Use Option2: pop RE361 / depop RE362	0.5(X04)
84	24	DP/USB3 Repeater SW TUSB546	2016/09/26	EE	BITS296634/287982-Cannot wake on LAN via Type-C to LAN dongle	Add LT13 for +3.3V_VDD_PIC and depop LT11 Change +3.3V_RUN to +3.3V_CPS for this page	0.5(X04)
85	34	EC MEC5105 Support	2016/09/29	EE	WDT schematic	Add QE13, CE503, RE530	0.5(X04)
86	34	EC MEC5105 Support	2016/09/30	EE	Board ID	Change RE79 to 8.2kohm (SD028820180)	0.5(X04)
87	34	EC MEC5105 Support	2016/09/30	EE	BITS294007-Sometimes need to press power button twice to power on system	Change CE12 to 2.2uf and RE33 to 1Kohm	0.5(X04)
88	24	DP/USB3 Repeater SW TUSB546	2016/09/30	EE	Schematic align	Reserve RT399~RT402 (0ohm) for TBT RX	0.5(X04)
89	33	EC MEC5105	2016/10/05	EE	Prevent EOS issue on MEC5105	Add 100ohm serial resistor on CV2_ON close to UE1.H8	0.5(X04)
90	24	DP/USB3 Repeater SW TUSB546	2016/10/05	EE	Schematic align (BME)	Remove RT399~RT402 (0ohm) for TBT RX	0.5(X04)
91	34	EC MEC5105 Support	2016/11/04	EE	Board ID	Change RE79 to 4.3kohm (SD028820180)	1.0(A00)
92	33	EC MEC5105	2016/11/04	EE	MEC5105 change from revB to revC	Change MEC5105 CPN to SA00009GL30 Depop RE361,Pop RE362	1.0(A00)
93	34	EC MEC5105 Support	2016/11/04	EE	MEC5105 revC WDT schematic	Pop RE536, Depop QE13, CE503, RE530, UE7, CE5,CE6, RE348	1.0(A00)
94	All	All page	2016/11/04	EE	0 ohm short pad	Change 0 ohm to short pad	1.0(A00)
95	12	CPU (7/14)	2016/11/04	EE	Service Mode Switch remove	Depop SW1, RC222 and pop RC221	1.0(A00)
96	25	[Type C]PD Controller TI	2016/11/04	EE	TI PD CC1/CC2 CAP change	Change CT85,CT86 to 820pf (SE000003W00)	1.0(A00)

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