First International Computer,Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : VME40

Version : 0.3

Initial Date : 04/28/ 2009

Manager Sign by: AVERY/RICHARD

Drawing by : Chris

Total confirm by: RICHARD

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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: Title | Rev: 0.1

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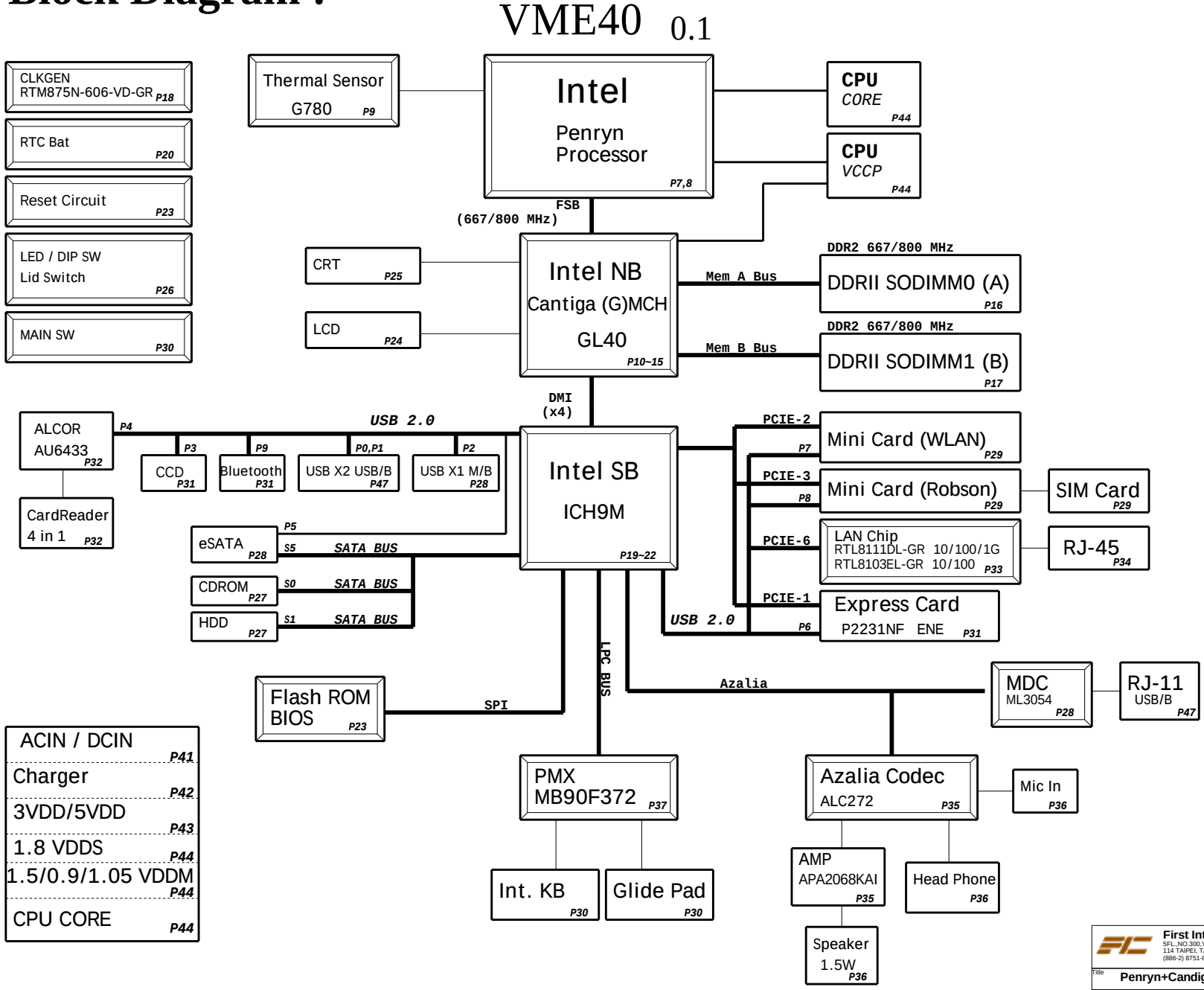
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	3.3V power rail by PSUSC#
3VDDA	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer(High Speed)
Layer 4	Stripline Layer(High Speed)
Layer 5	Power Plane
Layer 6	Solder Side,Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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8. Layout Guideline :

Crestline DDRII Layout Guidelines

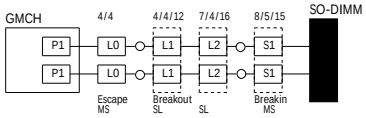
DDRII Signal Groups

Group	Signal Name
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SA_DQS#[7..0] SB_DQS[7..0]/SB_DQS#[7..0]
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#
Control	SM_CS#[3..0] SM_CKE[3..0] SM_ODT[3..0]
Clock	SM_CK[3..0] SM_CK#[3..0]
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : SM_CK[3..0],SM_CK#[3..0]

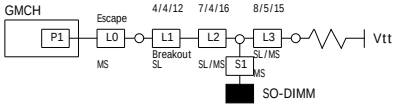


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 2 00 mils

Feedback group :
SA_RCVENIN#],SA_RCVENOUT#,SB_RCVENIN#],SB_RCVENOUT#

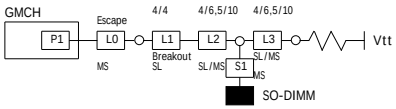
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



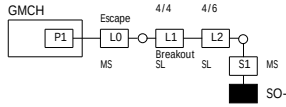
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Character istic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group :
SA_MA[13..0],SB_MA[13..0],SA_BS[2.0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



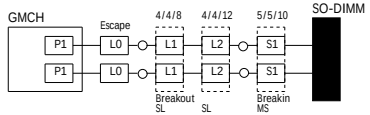
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Character istic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 2 00 mils

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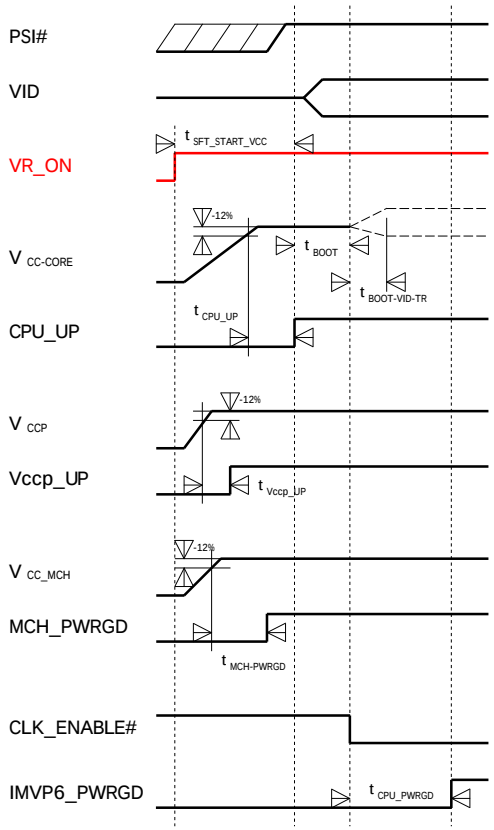
7. power on & off & S3 Sequence :

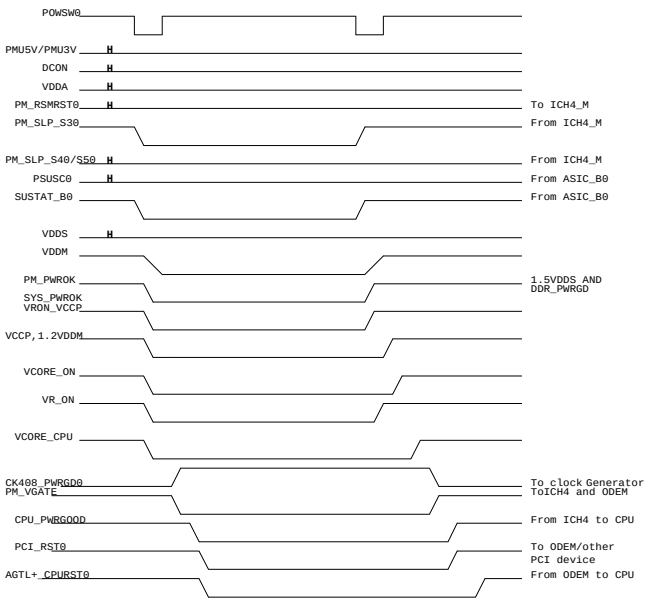
Power On Sequencing Timing Diag ram

20060117A - DATA FROM NO.16809

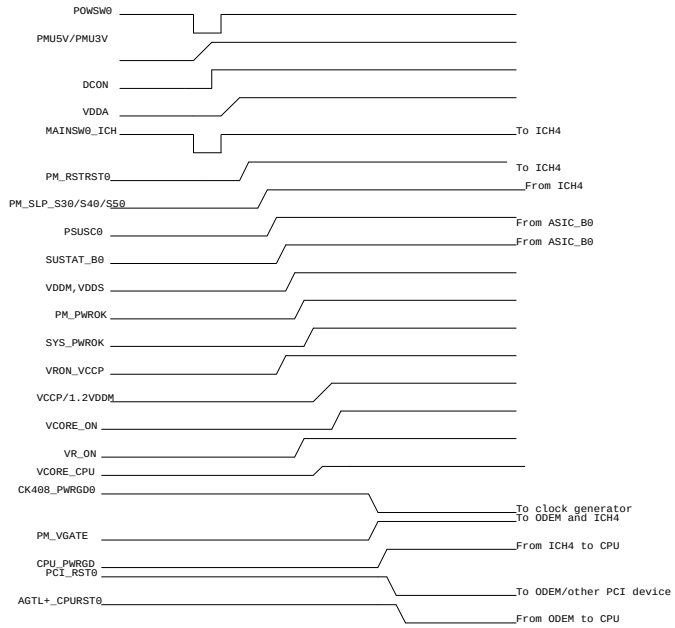


$t_{SFT\_START\_VCC}$	Max = 3 ms
t_{BOOT}	Min = 10 us , Max = 100 us
$t_{BOOT-VID-TR}$	Max = 100 us
t_{CPU_UP}	Min = 10 us , Max = 30 us
t_{Vccp_UP}	Min = 10 us , Max = 30 us
$t_{MCH-PWRGD}$	Min = 10 us , Max = 30 us
t_{CPU_PWRGD}	Min = 3 ms , Max = 20 ms

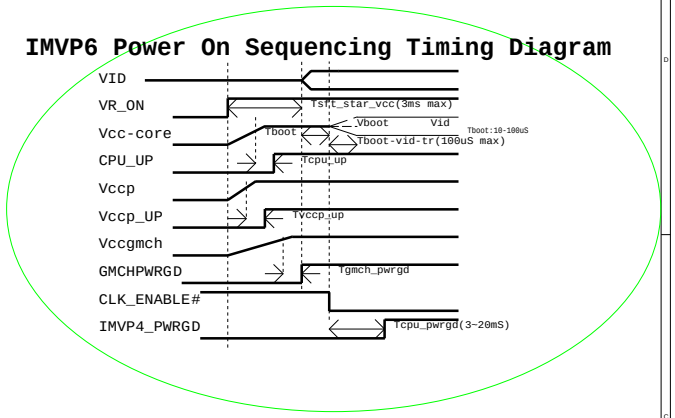
S3 SUSPEND AND RESUME TIMING



BATTERY ONLY POWER ON TIMING



IMVP6 Power On Sequencing Timing Diagram



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6.Schematic modify Item and History :

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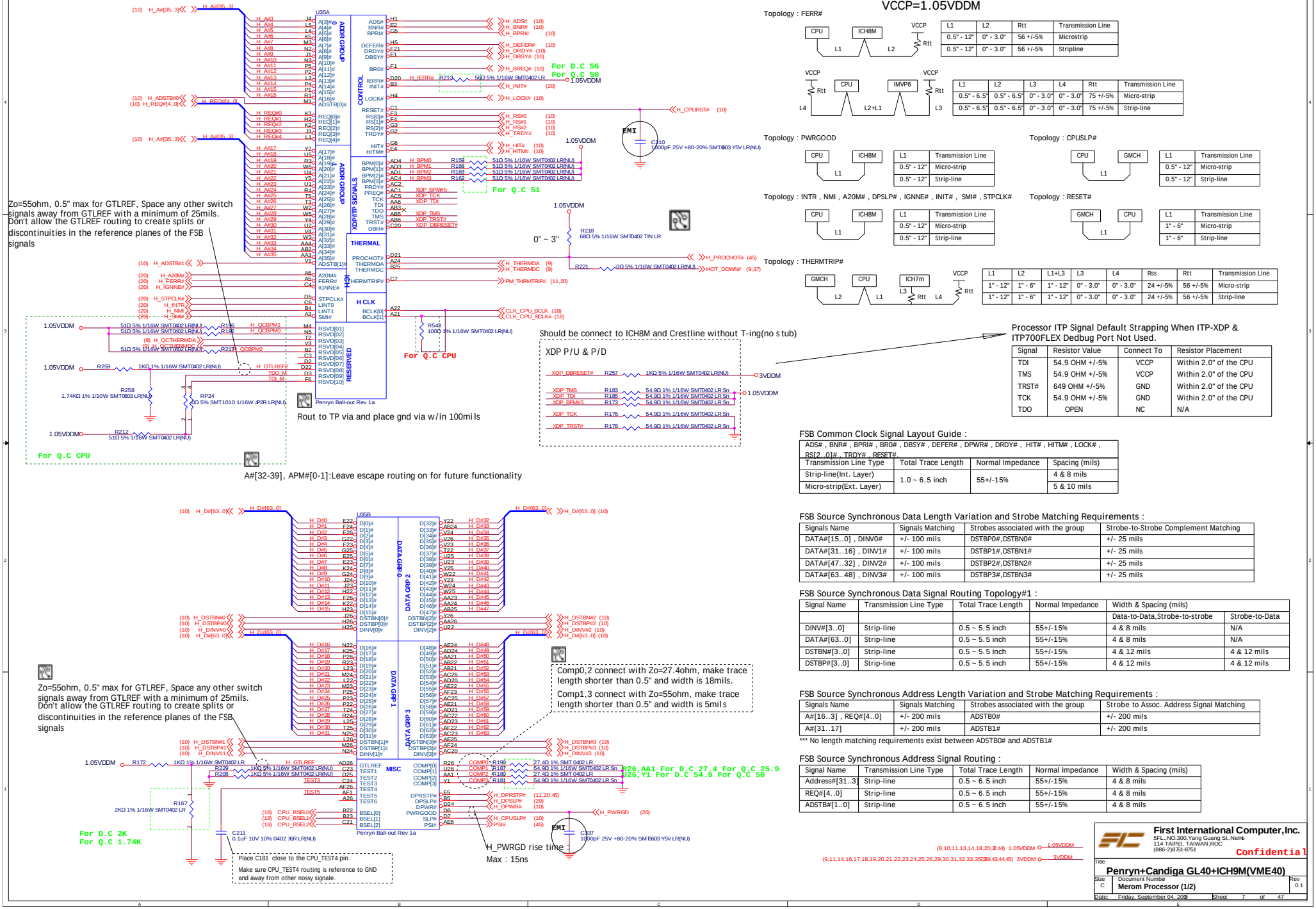

L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Microstrip
0.5" - 12"	0" - 3.0"	56 +/-5%	Stripline

L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	75 +/-5%	Strip-line

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils

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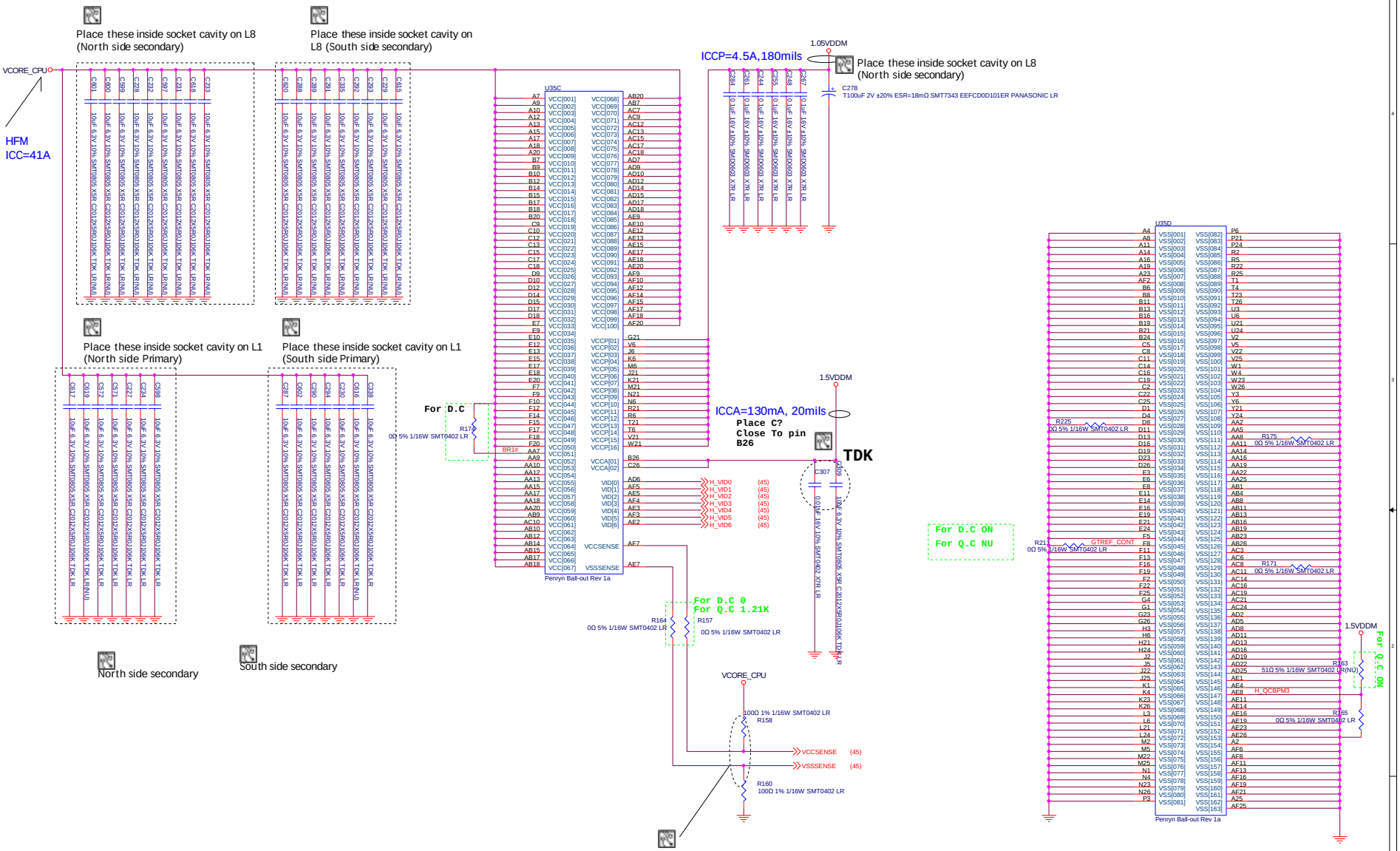

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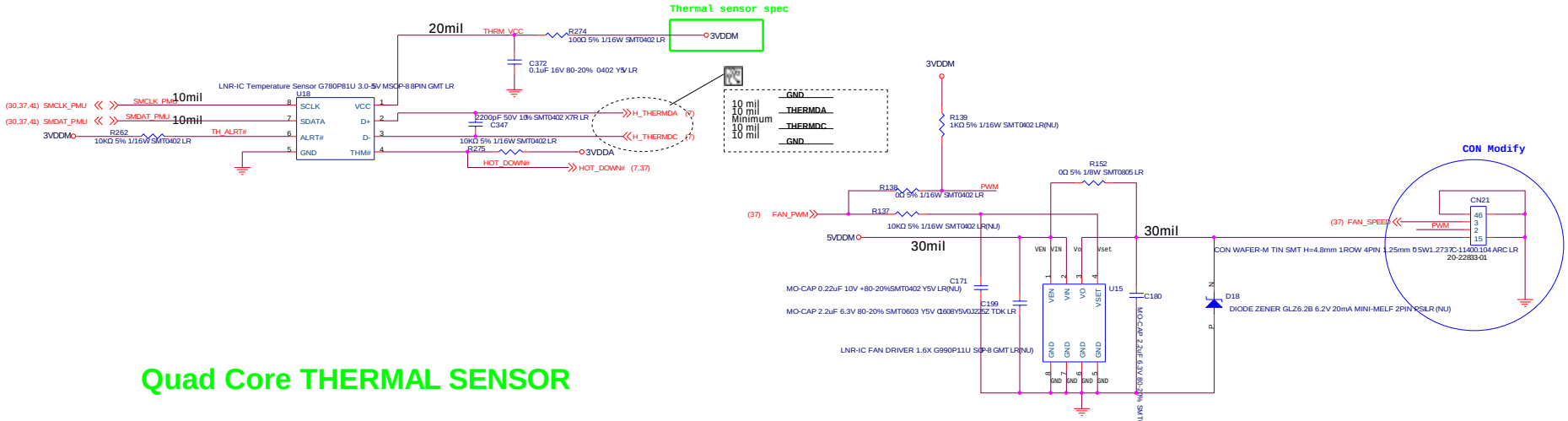
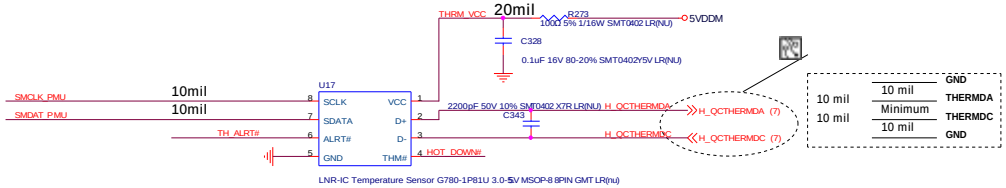
Dual Core THERMAL SENSOR



Quad Core THERMAL SENSOR



(7,11,14,16,17,18,19,20,21,22,23,24,25,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM — 3VDDM
(18,19,20,21,22,23,24,28,29,30,31,33,37,41,43,44) 3VDDA — 3VDDA
(22,25,27,30,35,39,43,44,45) 5VDDM — 5VDDM

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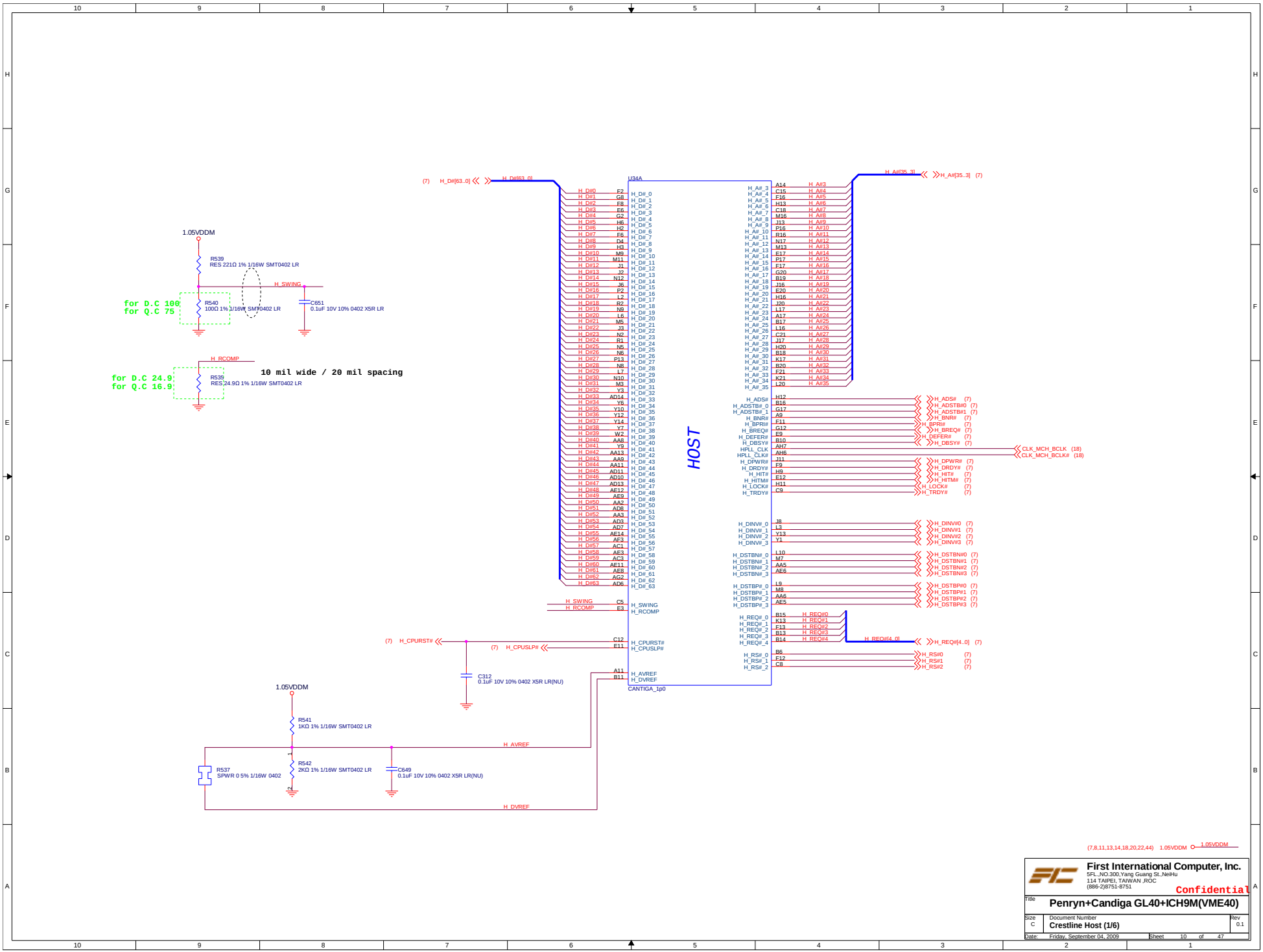

(7,8,11,13,14,18,20,22,44) 1.05VDDM 1.05VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)		
Size: C	Document Number: Crestline Host (1/6)	Rev: 0.1
Date: Friday, September 04, 2009	Sheet 10 of 47	

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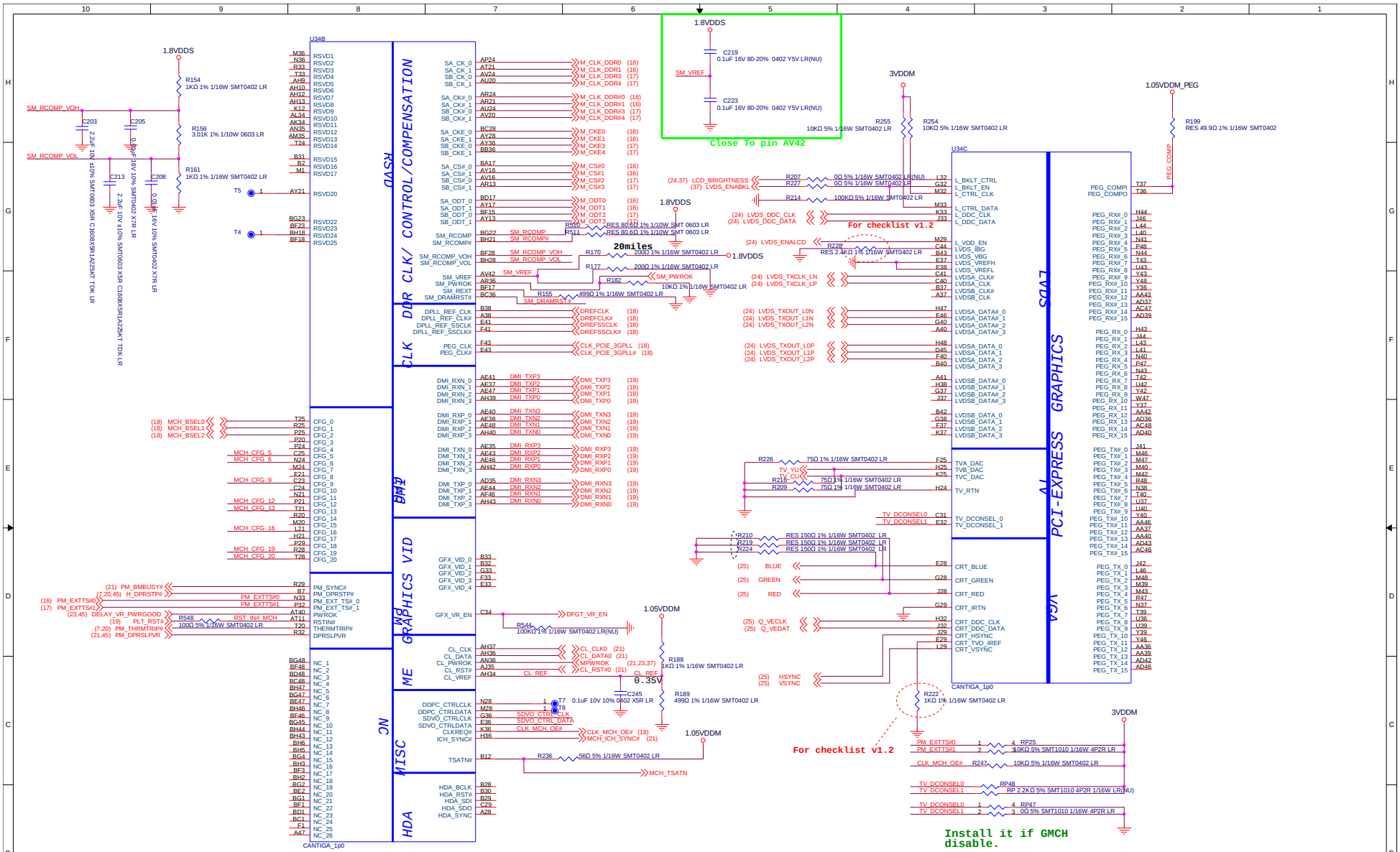

GMCH Strapping Requirements

CFG [2:0]	000=FSB1066 011=FSB667 010=FSB800	CFG7	0 = Isolators are bypassed 1= Isolators are active (Default)
CFG5	0 = DMI * 2 1 = DMI * 4 (Default)	CFG10	0 = PCIE loopback enable 1= PCIE loopback disable(Default)
CFG6	0 = ITPM is enabled 1 = ITPM is disabled (Default)	CFG16	0 = Dynamic ODT Disabled 1 = DMI Lane Reversal Enabled (Default)
CFG9	0 = Lane Reverse (PCIE) 1 = Normal Operation (Default)	CFG19	0 = Normal (Default) (DMI lane) 1 = Lanes Reversed
CFG [12:13]	00 = Clock Gating Disable 01 = XOR Mode Enabled 10 = All Z Mode Enable 11 = Normal Operation (Default)	CFG20	0 = Only SDVO or PCIE X1 is operationl (default) 1 = SDVO or PCIE X1 are operatingsimulaneously via the PEG port.

(14) 1.05VDDM_PEG 1.05VDDM_PEG
(7,8,10,13,14,18,20,22,44) 1.05VDDM 1.05VDDM
(13,14,16,17,44) 1.8VDDS 1.8VDDS
(7,9,14,16,17,18,19,20,21,22,23,24,25,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM 3VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: Crestline DMI/Graphic (2/6) | Rev: 0.1

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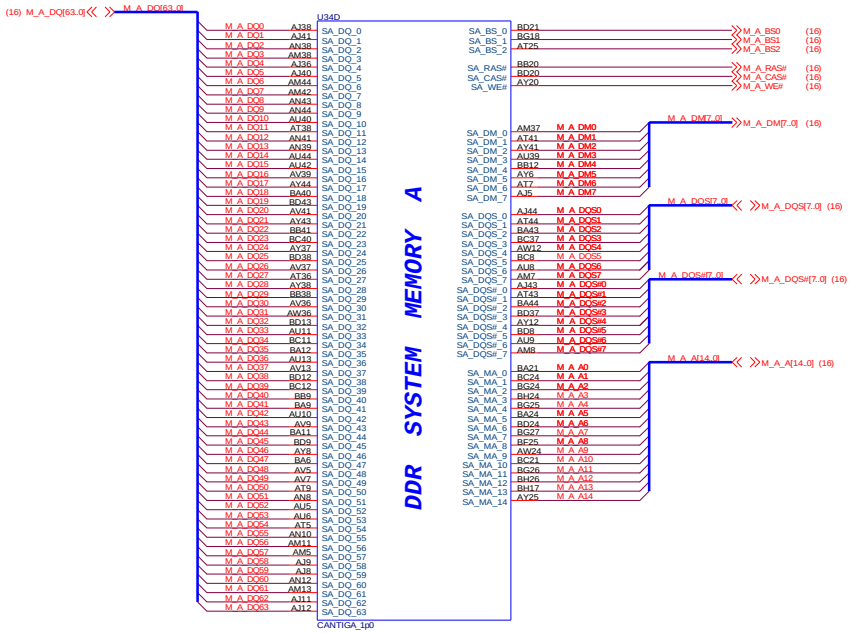
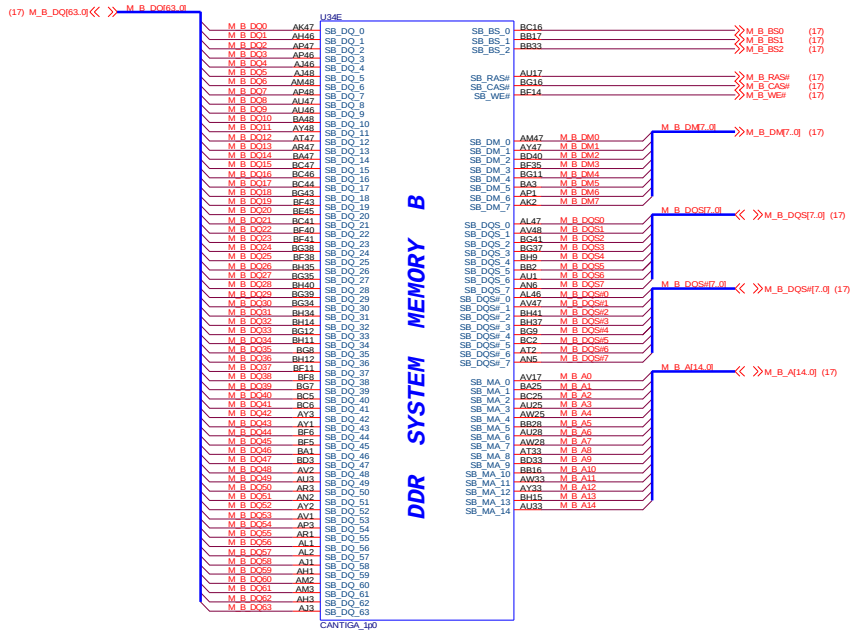
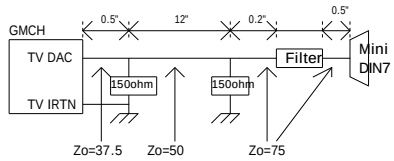




TV DAC Routing Guideline

1. The minimum spacing between each RGB is 40-mils while 50-mils is preferred
2. RGB signals should be routed on the same layer, have a similar number of bends, same number of vias
3. All routing should be done with ground referencing as well
4. TV DAC route lengths should be lenght match to within 200 mils



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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: Crestline DDR2 (3/6) | Rev: 0.1

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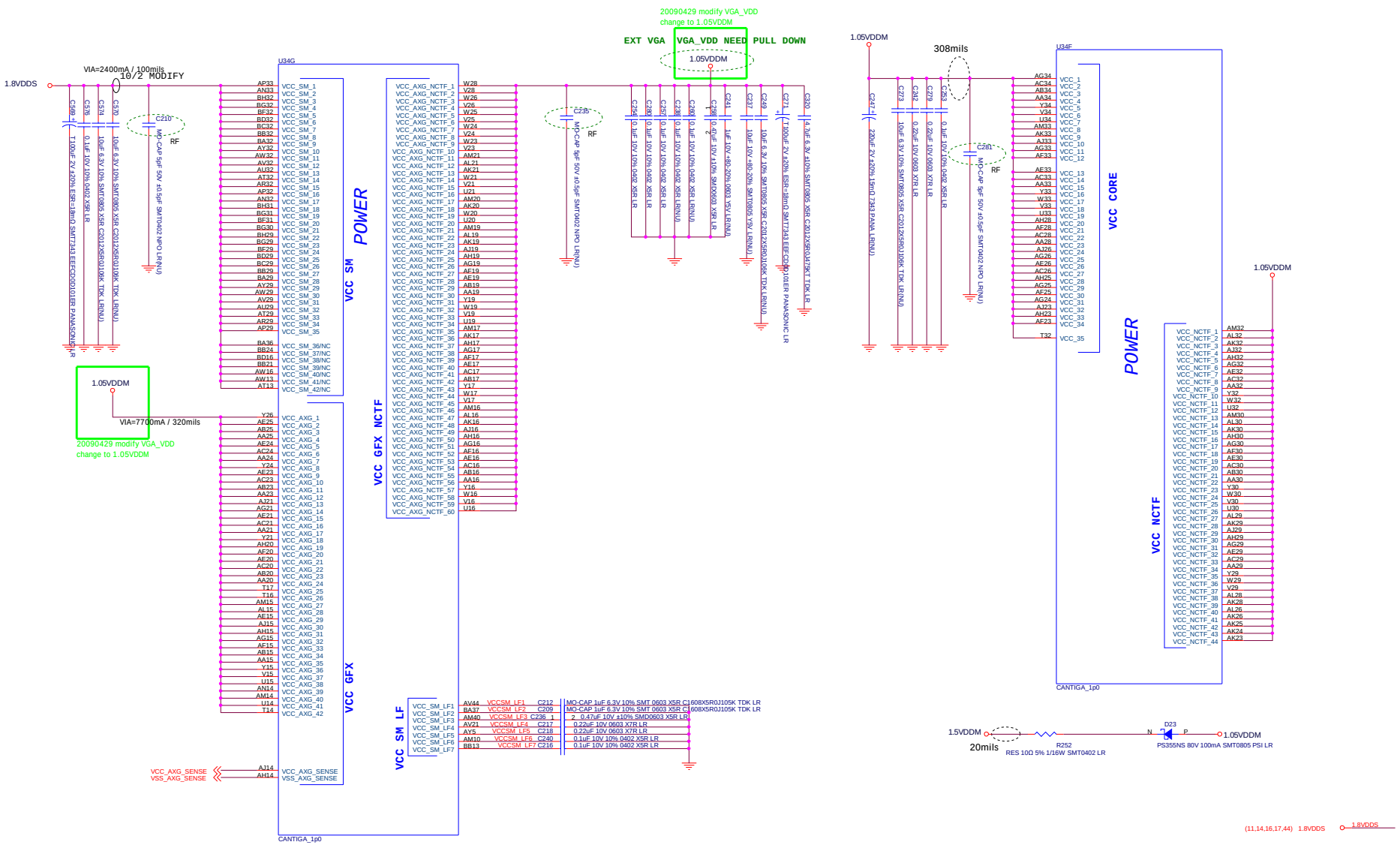

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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: Crestline Power (4/6) | Rev: 0.1

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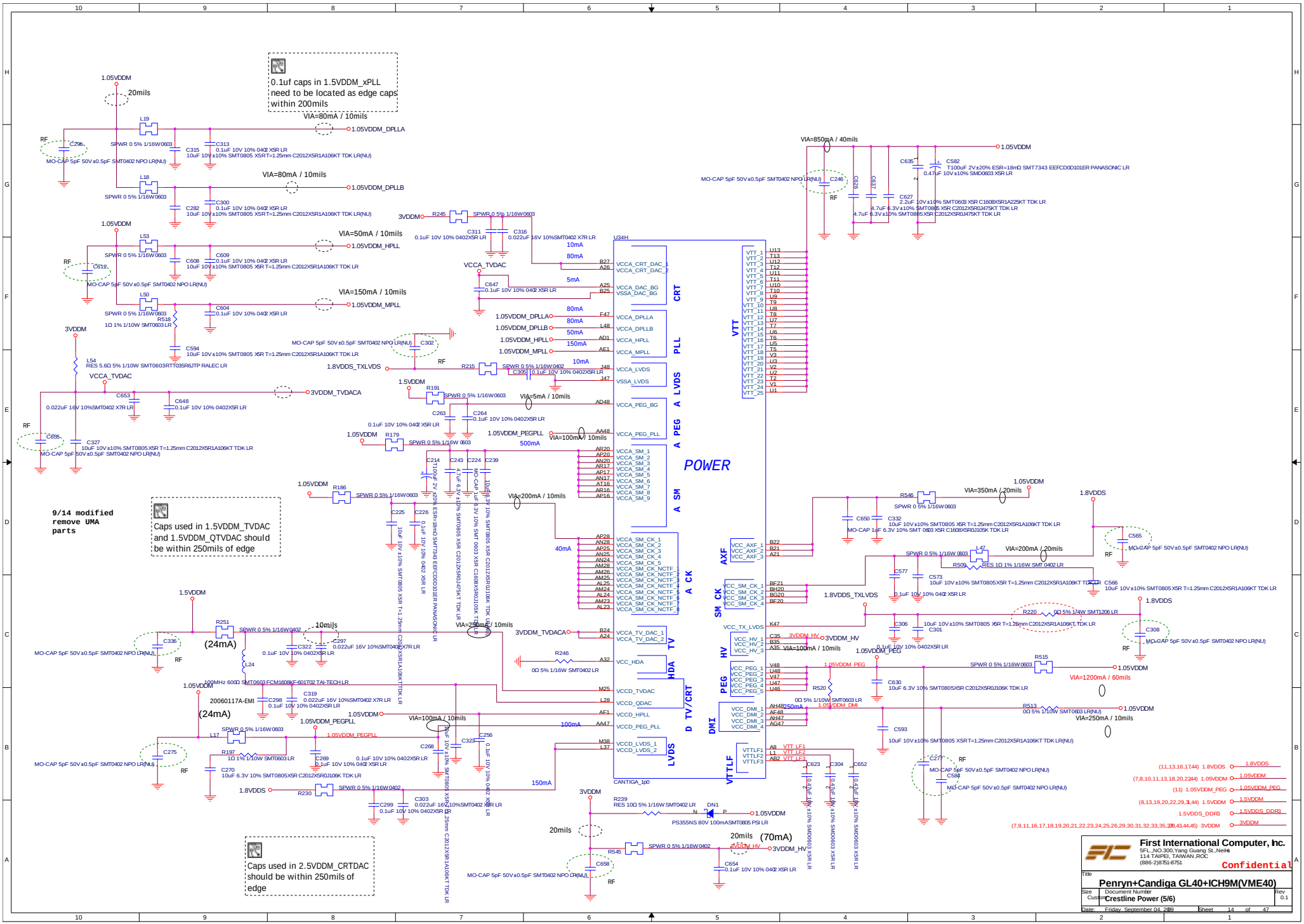
0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
9/14 modified remove UMA parts
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
Caps used in 2.5VDDM_CRTDAC should be within 250mils of edge
POWER
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
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Title
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Size
Custom
Document Number
Crestline Power (5/6)
Rev
0.1
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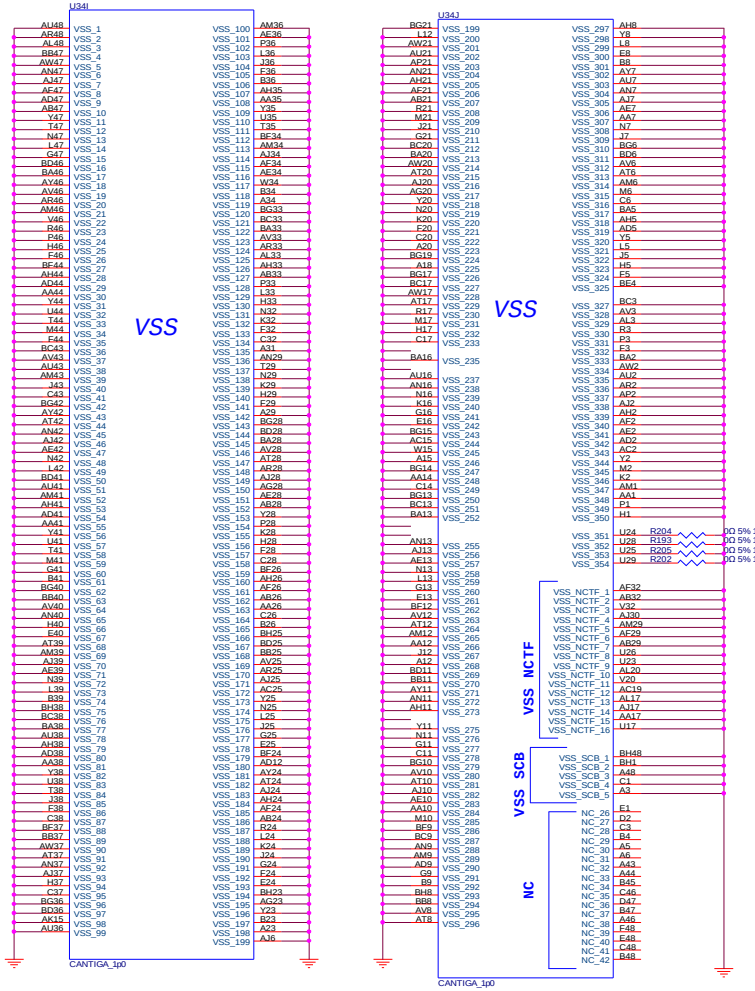
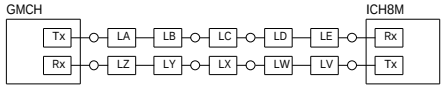


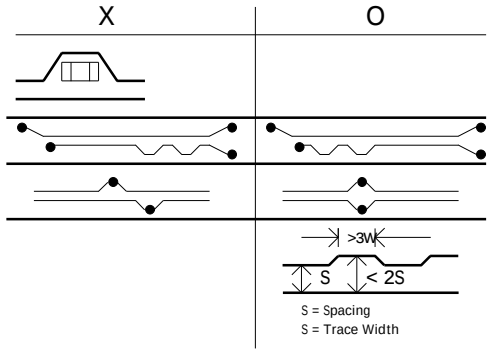
DMI Routing Guideline



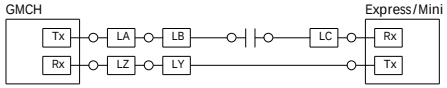
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Dididerential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+L C+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



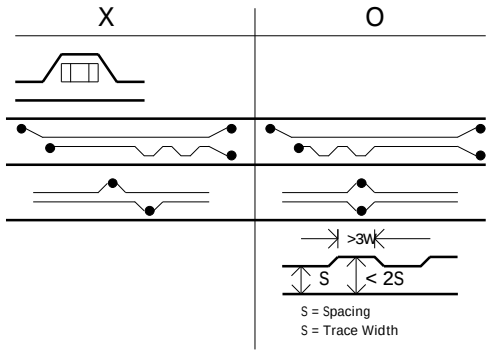
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane spli ts No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differenti al pair to +/- 5 mils



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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: Crestline Ground (6/6) | Rev: 0.1

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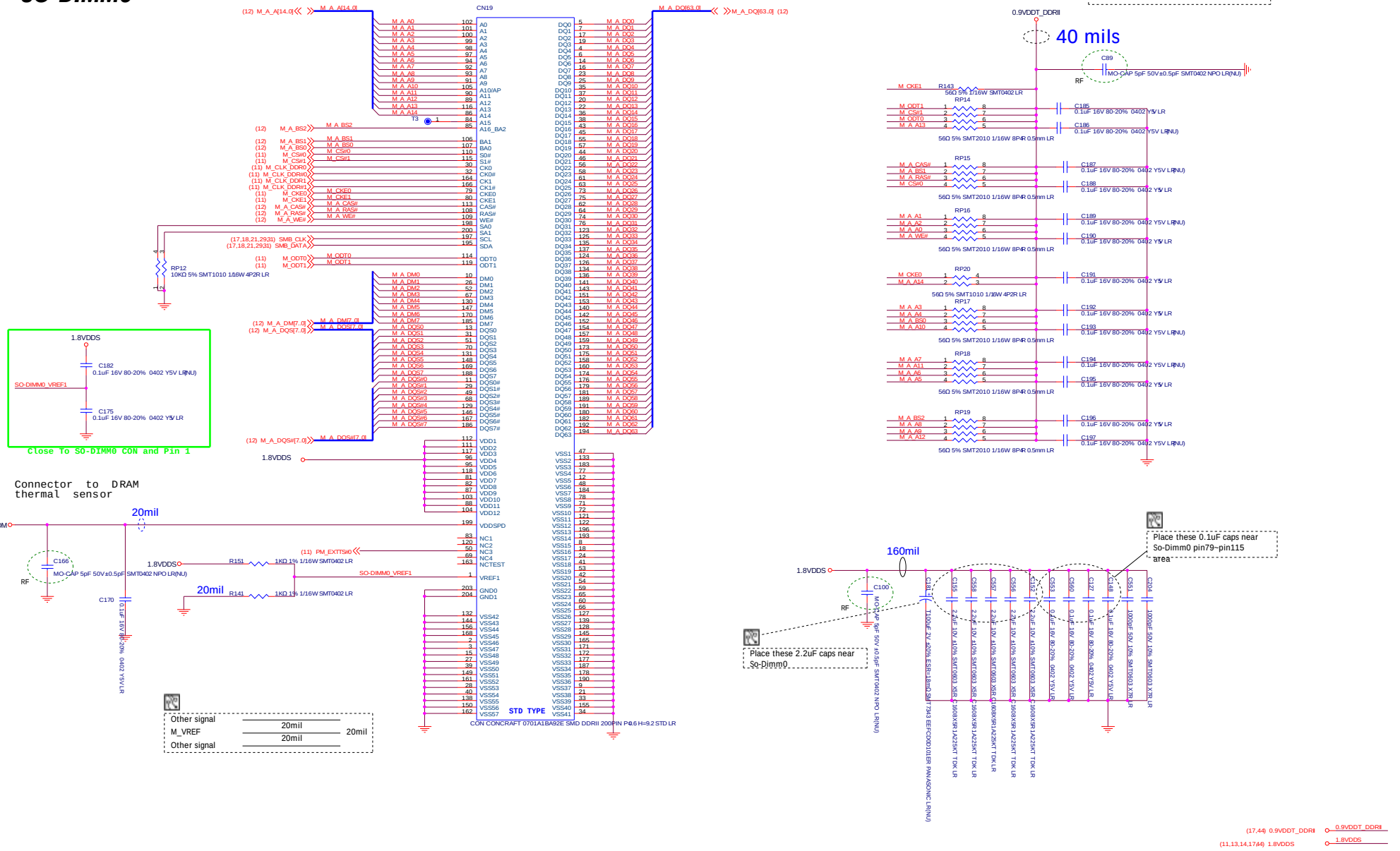
SO-DIMM0



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Title	Penryn+Candiga GL40+ICH9M(VME40)	
Size C	Document Number DDR2 SDRAM SO-DIMM0	Rev 0.1
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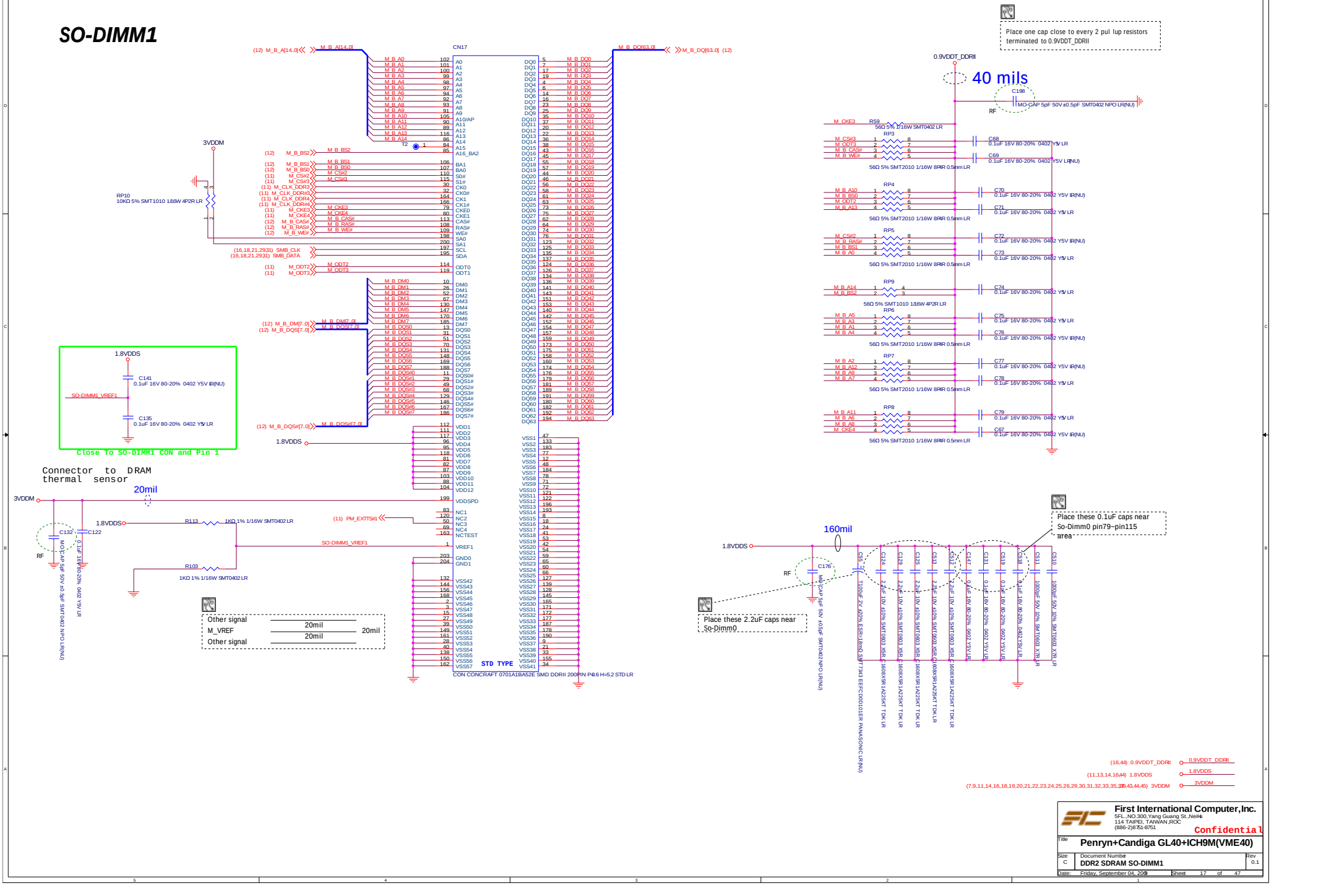
SO-DIMM1


CN17
STD TYPE
CON CONCRAFT 0701A1BA52E SMD DDRII 200PIN P0.6 H=5.2 STD LR
Close To SO-DIMM1 CON and Pin 1
Connector to DRAM thermal sensor
20mil
160mil
40 mils
Place one cap close to every 2 pul lup resistors terminated to 0.9VDDT_DDRII
Place these 0.1uF caps near So-Dimm0 pin79~pin115 area
Place these 2.2uF caps near So-Dimm0
Other signal
M_VREF
Other signal
20mil
20mil
0.9VDDT_DDRII
1.8VDDS
3VDDM
SO-DIMM1_VREF1
RP10 10KΩ 5% SMT1010 1/16W 4P2R LR
RP3 RP4 RP5 RP9 RP6 RP7 RP8
56Ω 5% SMT2010 1/16W 8P4R 0.5mm LR
56Ω 5% SMT1010 1/16W 4P2R LR
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DDR2 SDRAM SO-DIMM1
Rev 0.1
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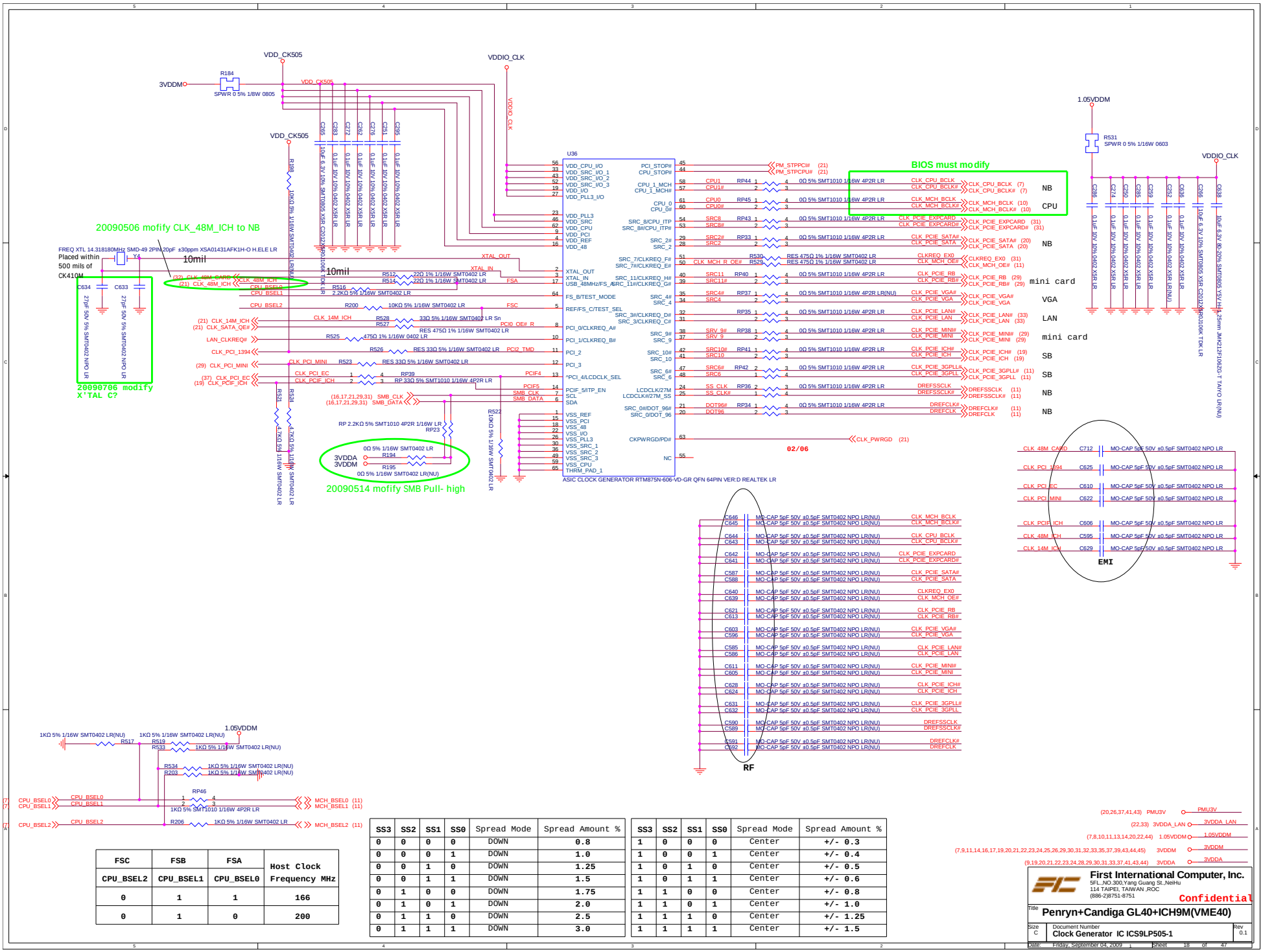

FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHz
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

(20,26,37,41,43) PMU3V — PMU3V
(22,33) 3VDDA_LAN — 3VDDA_LAN
(7,8,10,11,13,14,20,22,44) 1.05VDDM — 1.05VDDM
(7,9,11,14,16,17,19,20,21,22,23,24,25,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM — 3VDDM
(9,19,20,21,22,23,24,28,29,30,31,33,37,41,43,44) 3VDDA — 3VDDA

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Title: Penryn+Candiga GL40+ICH9M(VME40)
Size: C | Document Number: Clock Generator IC ICS9LP505-1 | Rev: 0.1
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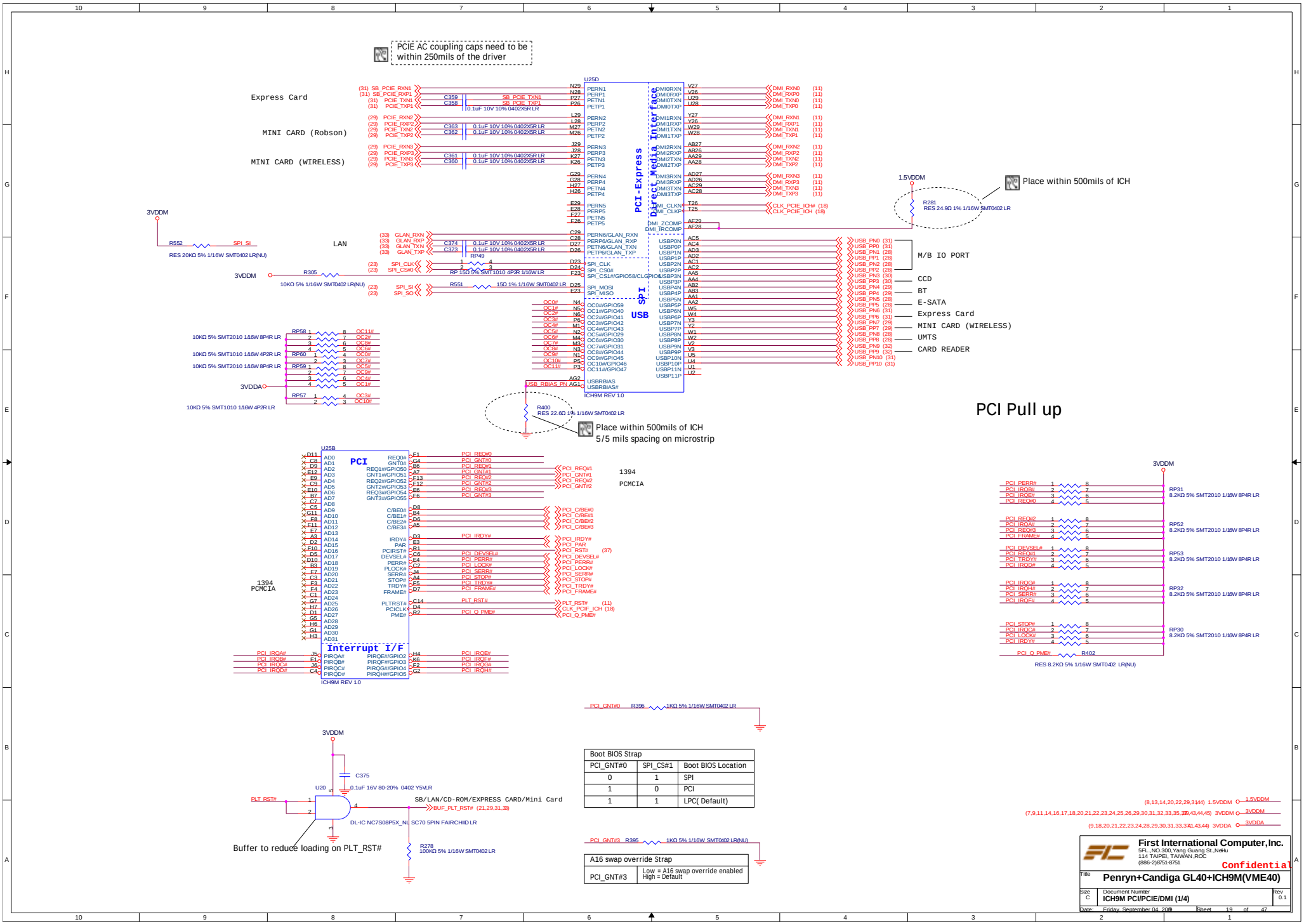
PCIE AC coupling caps need to be within 250mils of the driver
Express Card
MINI CARD (Robson)
MINI CARD (WIRELESS)
LAN
PCI-Express
Direct Media Interface
SPI
USB
ICH9M REV 1.0
M/B IO PORT
CCD
BT
E-SATA
Express Card
MINI CARD (WIRELESS)
UMTS
CARD READER
Place within 500mils of ICH
Place within 500mils of ICH
5/5 mils spacing on microstrip
PCI Pull up
PCI
Interrupt I/F
1394
PCMCIA
Buffer to reduce loading on PLT_RST#
SB/LAN/CD-ROM/EXPRESS CARD/Mini Card
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
Boot BIOS Strap
PCI_GNT#0 | SPI_CS#1 | Boot BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override Strap
PCI_GNT#3 | Low = A16 swap override enabled High = Default
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Penryn+Candiga GL40+ICH9M(VME40)
ICH9M PCI/PCIE/DMI (1/4)
Friday, September 04, 2009

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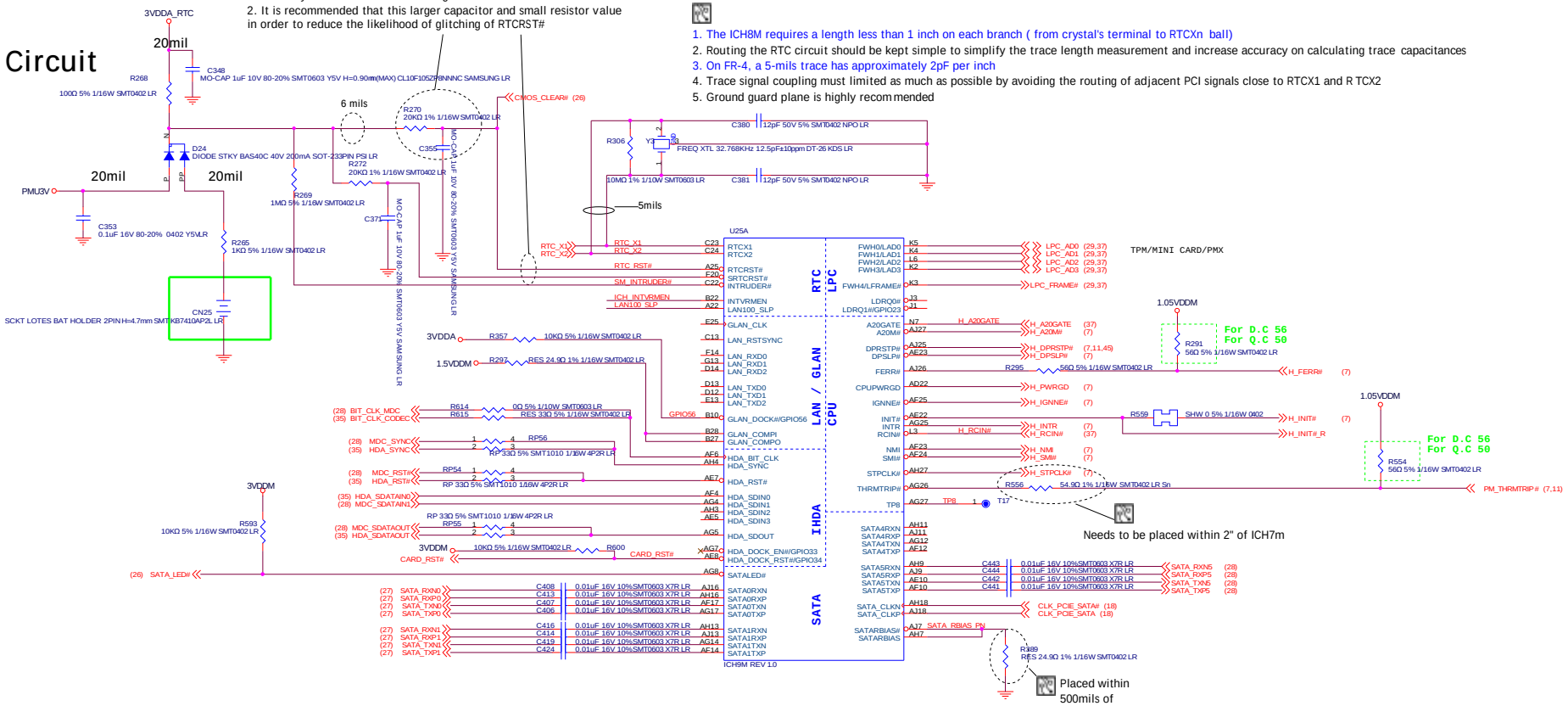
RTC Circuit

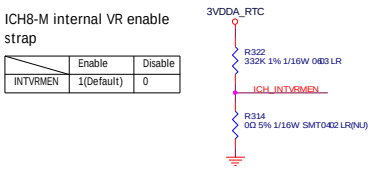
1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

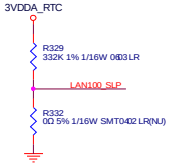
1. The ICH8M requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and R TCX2
5. Ground guard plane is highly recommended



ICH8-M internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0





ICH8-M LAN100 SLP Strap	
Internal VR for VccLAN1_05 and VccCL1_05)	
LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled (Default)

(22,33) 3VDDA_LAN — 3VDDA_LAN
(22) 3VDDA_RTC — 3VDDA_RTC
(26,37,41,43) PMU3V — PMU3V
(7,8,10,11,13,14,18,22,44) 1.05VDDM — 1.05VDDM
(8,13,14,19,22,29,31,44) 1.5VDDM — 1.5VDDM
(9,18,19,21,22,23,24,28,29,30,31,33,37,43,44) 3VDDA — 3VDDA
(7,9,11,14,16,17,18,19,21,22,23,24,25,26,29,30,31,32,33,35,39,43,44,45) 3VDDM — 3VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size	Document Number	Rev
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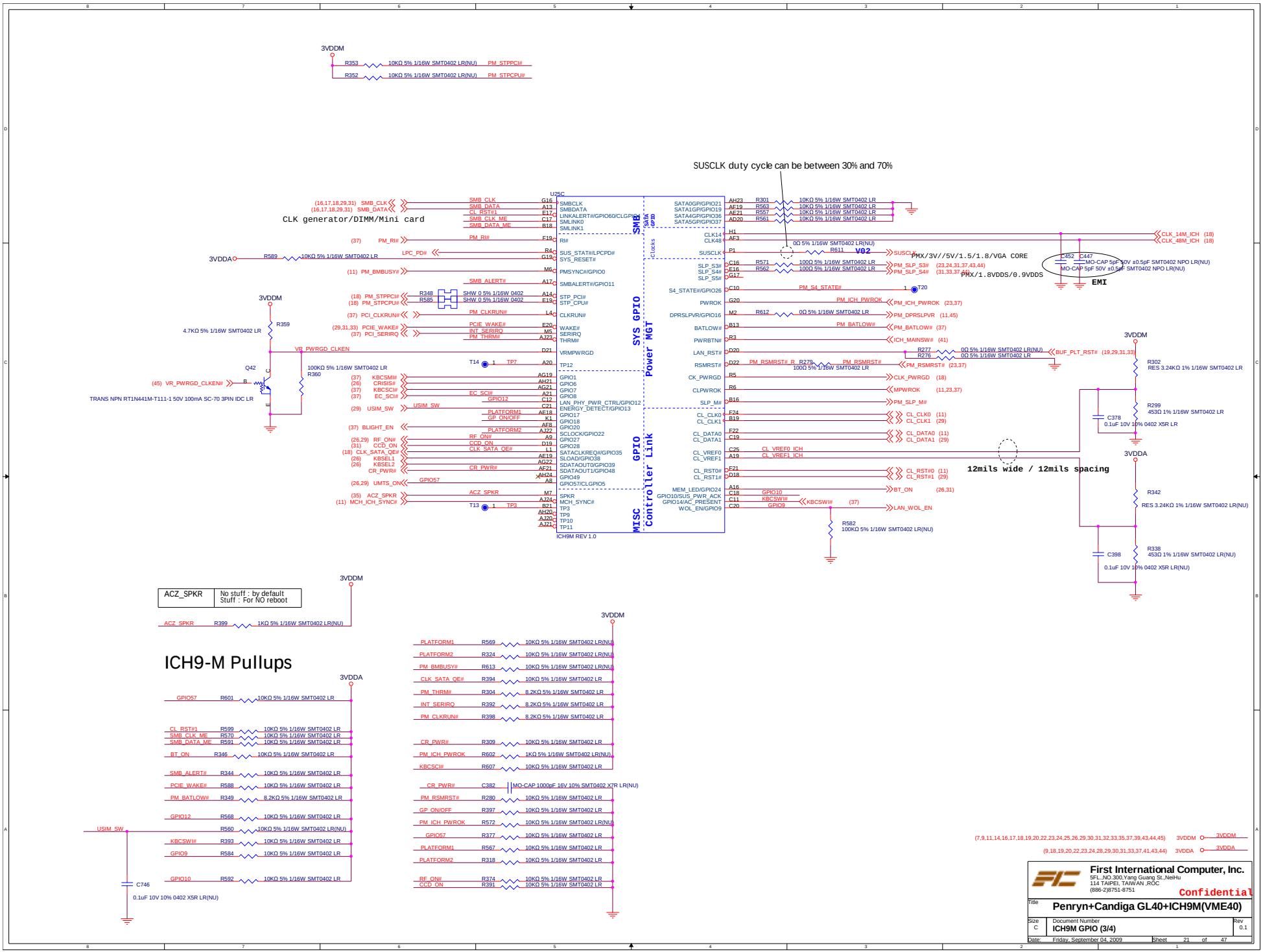
CLK generator/DIMM/Mini card
SUSCLK duty cycle can be between 30% and 70%
ICH9M REV 1.0
SMB
SATA GPIO
CLOCKS
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
PMX/3V//5V/1.5/1.8/VGA CORE
PMX/1.8VDDS/0.9VDDS
EMI
12mils wide / 12mils spacing
ACZ_SPKR
No stuff : by default
Stuff : For NO reboot
ICH9-M Pullups
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ICH9M GPIO (3/4)
Friday, September 04, 2009

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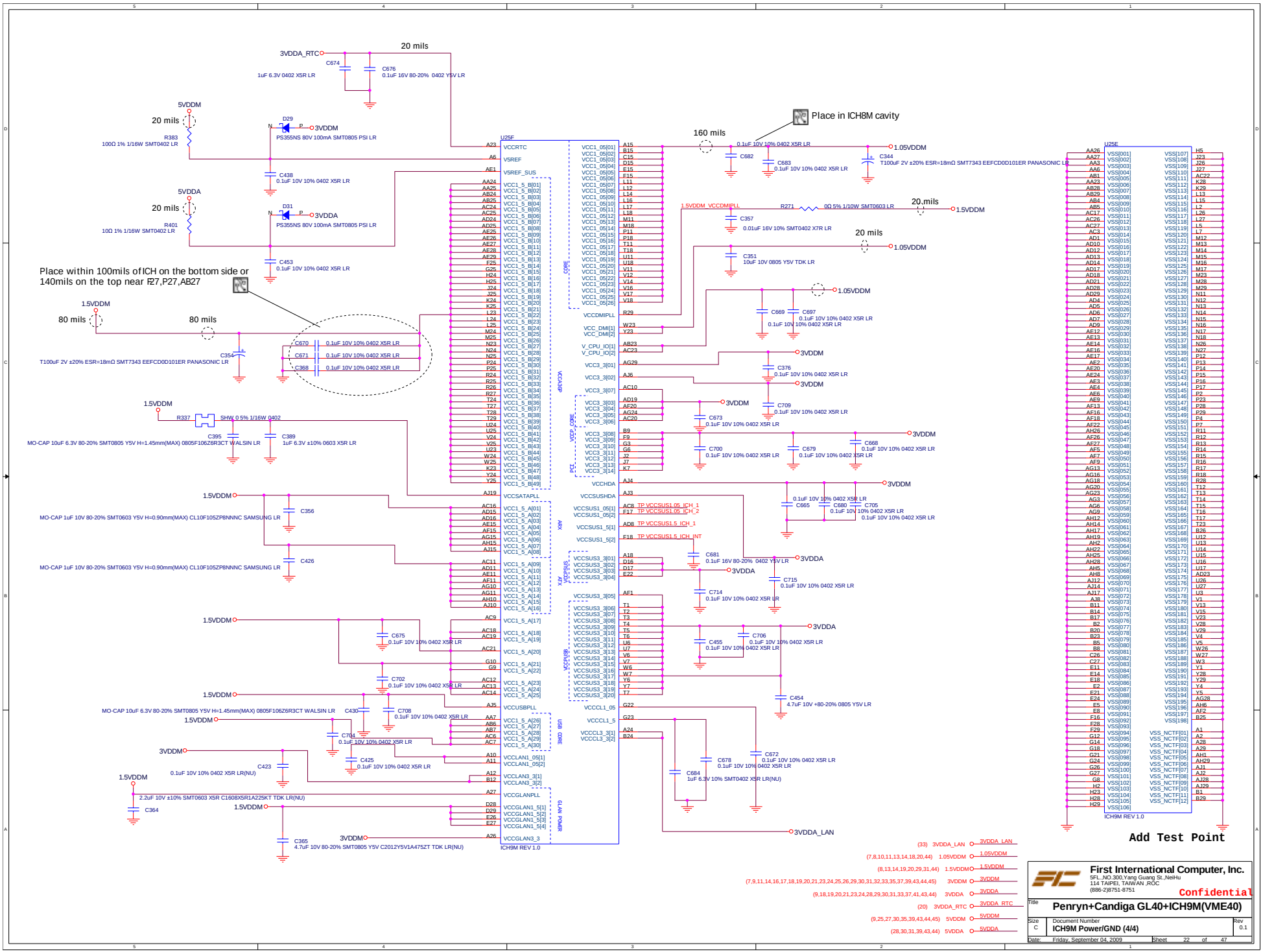
3VDDA_RTC
20 mils
C674
1uF 6.3V 0402 X5R LR
C676
0.1uF 16V 80-20% 0402 Y5V LR
5VDDM
20 mils
R383
100Ω 1% 1/16W SMT0402 LR
D29
PS355NS 80V 100mA SMT0805 PSI LR
3VDDM
C438
0.1uF 10V 10% 0402 X5R LR
5VDDA
20 mils
R401
10Ω 1% 1/16W SMT0402 LR
D31
PS355NS 80V 100mA SMT0805 PSI LR
3VDDA
C453
0.1uF 10V 10% 0402 X5R LR
Place within 100mils of ICH on the bottom side or
140mils on the top near R27,P27,AB27
1.5VDDM
80 mils
80 mils
C354
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR
C670
C671
C368
0.1uF 10V 10% 0402 X5R LR
1.5VDDM
R337
SHW 0.5% 1/16W 0402
C395
MO-CAP 10uF 6.3V 80-20% SMT0805 Y5V H=1.45mm(MAX) 0805F106Z6R3CT WALSIN LR
C389
1uF 6.3V ±10% 0603 X5R LR
1.5VDDM
C356
MO-CAP 1uF 10V 80-20% SMT0603 Y5V H=0.90mm(MAX) CL10F105ZP8NNNC SAMSUNG LR
C426
MO-CAP 1uF 10V 80-20% SMT0603 Y5V H=0.90mm(MAX) CL10F105ZP8NNNC SAMSUNG LR
1.5VDDM
C675
0.1uF 10V 10% 0402 X5R LR
C702
0.1uF 10V 10% 0402 X5R LR
1.5VDDM
MO-CAP 10uF 6.3V 80-20% SMT0805 Y5V H=1.45mm(MAX) 0805F106Z6R3CT WALSIN LR
C430
C708
0.1uF 10V 10% 0402 X5R LR
1.5VDDM
C704
0.1uF 10V 10% 0402 X5R LR
3VDDM
C423
0.1uF 10V 10% 0402 X5R LR(NU)
C425
0.1uF 10V 10% 0402 X5R LR
1.5VDDM
2.2uF 10V ±10% SMT0603 X5R C1608X5R1A225KT TDK LR(NU)
C364
1.5VDDM
C365
4.7uF 10V 80-20% SMT0805 Y5V C2012Y5V1A475ZT TDK LR(NU)
3VDDM
U25F
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
VCC1_5_B[09]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
VCC1_5_B[14]
VCC1_5_B[15]
VCC1_5_B[16]
VCC1_5_B[17]
VCC1_5_B[18]
VCC1_5_B[19]
VCC1_5_B[20]
VCC1_5_B[21]
VCC1_5_B[22]
VCC1_5_B[23]
VCC1_5_B[24]
VCC1_5_B[25]
VCC1_5_B[26]
VCC1_5_B[27]
VCC1_5_B[28]
VCC1_5_B[29]
VCC1_5_B[30]
VCC1_5_B[31]
VCC1_5_B[32]
VCC1_5_B[33]
VCC1_5_B[34]
VCC1_5_B[35]
VCC1_5_B[36]
VCC1_5_B[37]
VCC1_5_B[38]
VCC1_5_B[39]
VCC1_5_B[40]
VCC1_5_B[41]
VCC1_5_B[42]
VCC1_5_B[43]
VCC1_5_B[44]
VCC1_5_B[45]
VCC1_5_B[46]
VCC1_5_B[47]
VCC1_5_B[48]
VCC1_5_B[49]
VCCSATAPLL
VCCUSBPLL
VCCLANPLL
VCCGLANPLL1_5[1]
VCCGLANPLL1_5[2]
VCCGLANPLL1_5[3]
VCCGLANPLL1_5[4]
VCCGLAN3_3
ICH9M REV 1.0
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01]
VCC3_3[02]
VCC3_3[07]
VCC3_3[03]
VCC3_3[04]
VCC3_3[05]
VCC3_3[06]
VCC3_3[08]
VCC3_3[09]
VCC3_3[10]
VCC3_3[11]
VCC3_3[12]
VCC3_3[13]
VCC3_3[14]
VCCHDA
VCCSUSHDA
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
VCCSUS3_3[05]
VCCSUS3_3[06]
VCCSUS3_3[07]
VCCSUS3_3[08]
VCCSUS3_3[09]
VCCSUS3_3[10]
VCCSUS3_3[11]
VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
VCCSUS3_3[20]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
160 mils
Place in ICH8M cavity
0.1uF 10V 10% 0402 X5R LR
C682
C683
0.1uF 10V 10% 0402 X5R LR
C344
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR
1.05VDDM
1.5VDDM_VCCDMIPLL
R271
0Ω 5% 1/10W SMT0603 LR
20 mils
1.5VDDM
C357
0.01uF 16V 10% SMT0402 X7R LR
20 mils
1.05VDDM
C351
10uF 10V 0805 Y5V TDK LR
1.05VDDM
C669
C697
0.1uF 10V 10% 0402 X5R LR
0.1uF 10V 10% 0402 X5R LR
3VDDM
C376
0.1uF 10V 10% 0402 X5R LR
3VDDM
C709
0.1uF 10V 10% 0402 X5R LR
3VDDM
C673
0.1uF 10V 10% 0402 X5R LR
3VDDM
C700
C679
C668
0.1uF 10V 10% 0402 X5R LR
0.1uF 10V 10% 0402 X5R LR
0.1uF 10V 10% 0402 X5R LR
3VDDM
C665
C680
C705
0.1uF 10V 10% 0402 X5R LR
0.1uF 10V 10% 0402 X5R LR
0.1uF 10V 10% 0402 X5R LR
TP VCCSUS1.05_ICH_1
TP VCCSUS1.05_ICH_2
TP VCCSUS1.5_ICH_1
TP VCCSUS1.5_ICH_INT
C681
0.1uF 16V 80-20% 0402 Y5V LR
3VDDA
3VDDA
C715
0.1uF 10V 10% 0402 X5R LR
C714
0.1uF 10V 10% 0402 X5R LR
3VDDA
C455
0.1uF 10V 10% 0402 X5R LR
C706
0.1uF 10V 10% 0402 X5R LR
C454
4.7uF 10V +80-20% 0805 Y5V LR
C678
0.1uF 10V 10% 0402 X5R LR
C672
0.1uF 10V 10% 0402 X5R LR
C684
1uF 6.3V 10% SMT0402 X5R LR(NU)
3VDDA_LAN
U25E
VSS[001]
VSS[002]
VSS[003]
VSS[004]
VSS[005]
VSS[006]
VSS[007]
VSS[008]
VSS[009]
VSS[010]
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VSS[196]
VSS[197]
VSS[198]
VSS_NCTF[01]
VSS_NCTF[02]
VSS_NCTF[03]
VSS_NCTF[04]
VSS_NCTF[05]
VSS_NCTF[06]
VSS_NCTF[07]
VSS_NCTF[08]
VSS_NCTF[09]
VSS_NCTF[10]
VSS_NCTF[11]
VSS_NCTF[12]
ICH9M REV 1.0
Add Test Point
(33) 3VDDA_LAN
(7,8,10,11,13,14,18,20,44) 1.05VDDM
(8,13,14,19,20,29,31,44) 1.5VDDM
(7,9,11,14,16,17,18,19,20,21,23,24,25,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM
(9,18,19,20,21,23,24,28,29,30,31,33,37,41,43,44) 3VDDA
(20) 3VDDA_RTC
(9,25,27,30,35,39,43,44,45) 5VDDM
(28,30,31,39,43,44) 5VDDA
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Penryn+Candiga GL40+ICH9M(VME40)
ICH9M Power/GND (4/4)
Rev 0.1
Friday, September 04, 2009
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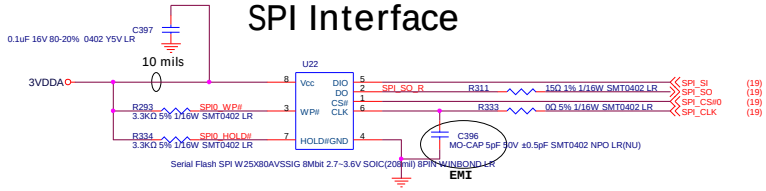
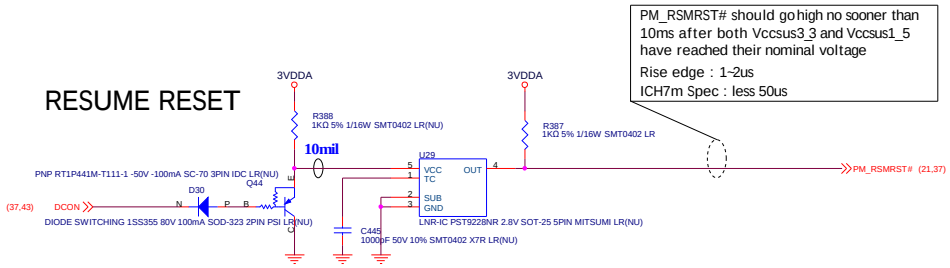
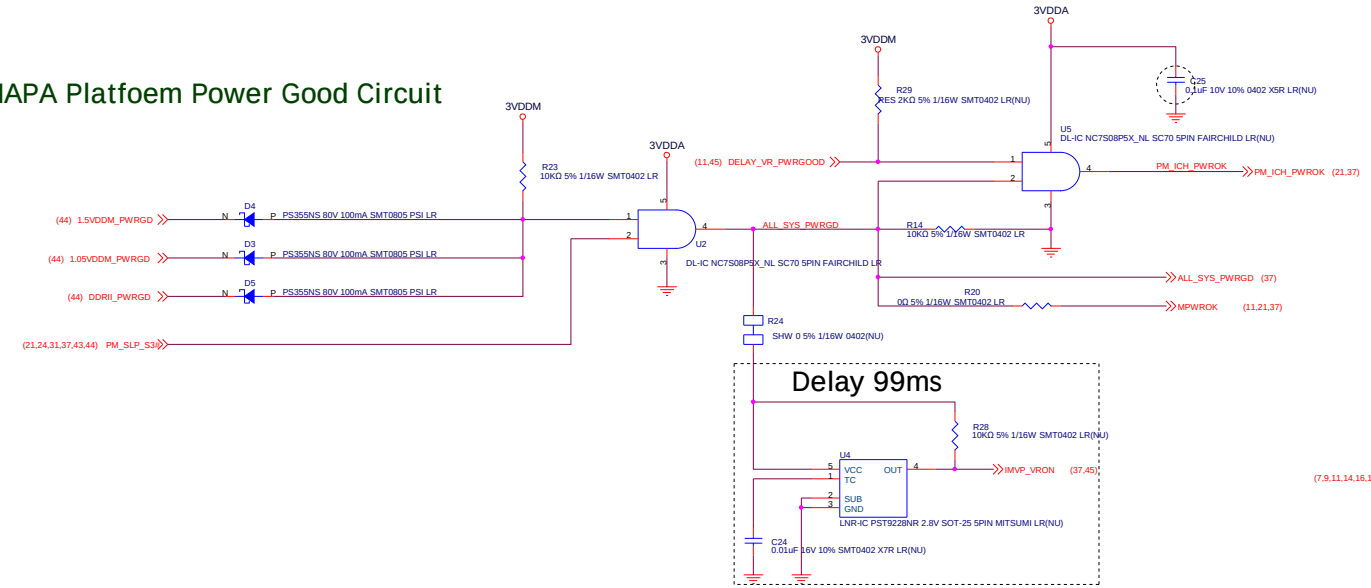
SPI Interface



RESUME RESET



NAPA Platfoem Power Good Circuit



(7,9,11,14,16,17,18,19,20,21,22,24,25,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM 3VDDM

(9,18,19,20,21,22,24,28,29,30,31,33,37,41,43,44) 3VDDA 3VDDA

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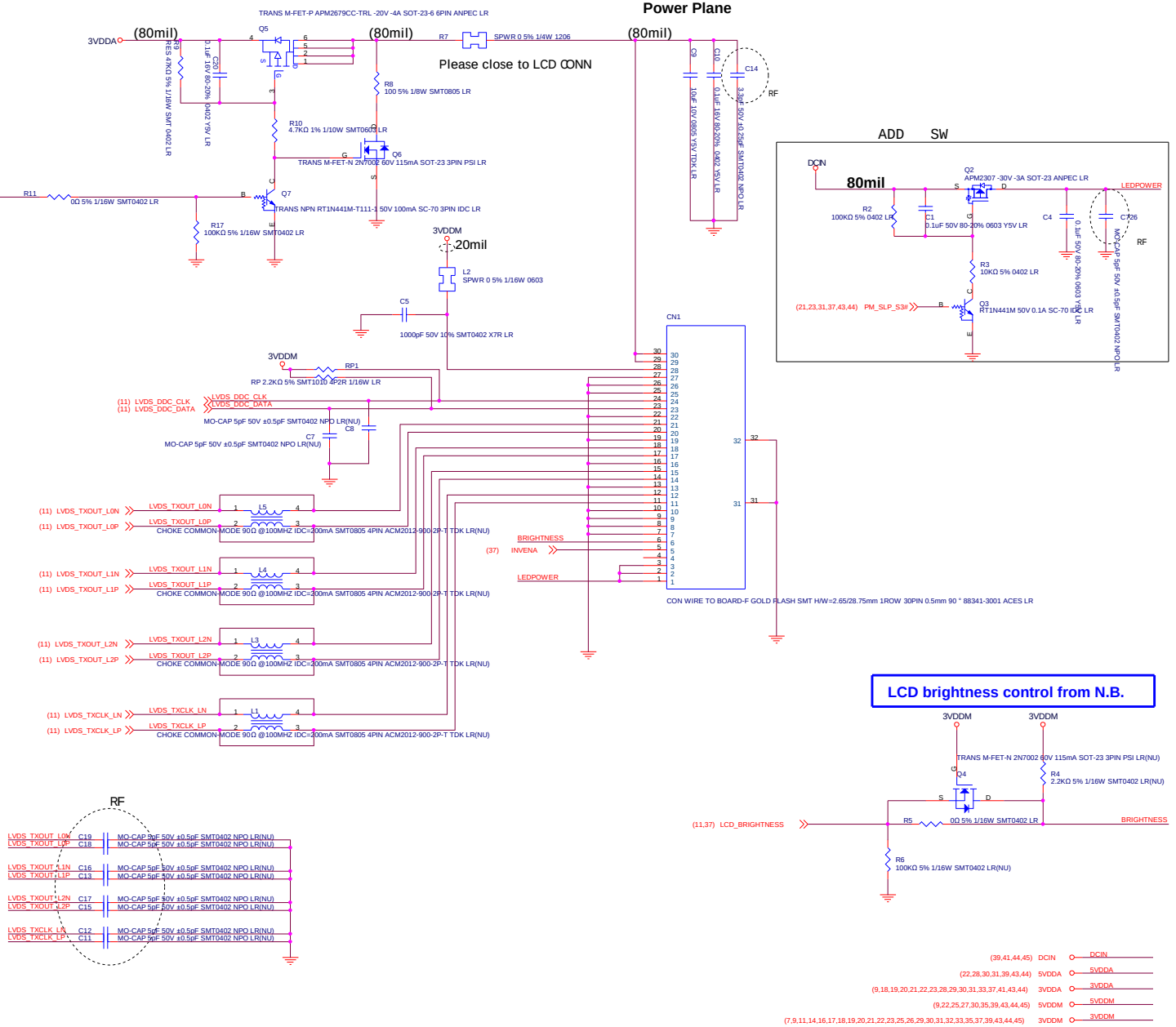
Min : 80 MIL or
Power Plane

Please close to LCD CONN

GMCH LVDS Signal Group Routing Guideline

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to non-LVDS	20 mils
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

***Cable Length must be less than 16"



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Layout Note:
RGB SIGNAL
Place 150 Ohm resistor near connector.
Use 37.5 Ohm traces from GMCH to 150 Ohm resistors
LENGTH MAX= 0.5" MATCHING = +/- 200mils

For VESA SPEC , R/G/B should be 665mV ~ 770mV

Place 150 Ohm resistor near connector.
Use 37.5 Ohm traces from GMCH to 150 Ohm resistors

Othrer Signal	
RED	20 mil
GREEN	20 mil
BLUE	20 mil
Other Signal	20 mil

D47 DIODE ESD RClamp0502B.TCT 5V SC-75(SOT523) 3PIN SEMTECH LR(NU)
D46 DIODE ESD RClamp0502B.TCT 5V SC-75(SOT523) 3PIN SEMTECH LR(NU)

20mil
20mil

5VDDM — F2 POLY-SWITCH 1.5A 8V SMT1812 SMD1812P150TF/8 PTC LR — D13 DIODE STKY SS1040 40V 1A SOD-123 2PIN PSI LR — L16 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR — CRT5VS — C149 0.1uF 16V 80-20% 0402 Y5V LR

(11) RED
(11) GREEN
(11) BLUE
VEDAT_CONN
CRT5VS — RP13 RP 2.2KΩ 5% SMT1010 4P2R 1/16W LR
VECLK_CONN

WIDTH= 8 MILS Z0=37.5 ohms
LENGTH MAX= 0.5" MATCHING = +/- 200mils
WIDTH= 8 MILS Z0=75 ohms

L14 56nH 5% 300mA SMT0603 FCI1608F-56NJ Tai-Tech LR
L13 56nH 5% 300mA SMT0603 FCI1608F-56NJ Tai-Tech LR
L12 56nH 5% 300mA SMT0603 FCI1608F-56NJ Tai-Tech LR

R108 0Ω 5% 1/10W SMT0603 LR
R92 0Ω 5% 1/10W SMT0603 LR
R81 0Ω 5% 1/10W SMT0603 LR

R479 RES 30Ω 5% 1/16W SMT0402 LR
R477 RES 30Ω 5% 1/16W SMT0402 LR

CNN_RED
CNN_GREEN
CNN_BLUE
CNN_HSYNC
CNN_VSYNC

CN18 — CON SUYIN DIP D-sub 15PIN reserved 070546FR015S211CU Lead-free & RoHS 20-25071-00

R110 RES 150Ω 1% 1/16W SMT0402 LR
R94 RES 150Ω 1% 1/16W SMT0402 LR
R77 RES 150Ω 1% 1/16W SMT0402 LR

C542 MO-CAP 8.2pF 50V ±0.5pF SMT0402 NPO C1005NP082B0GT DARFON LR(NU)
C538 MO-CAP 8.2pF 50V ±0.5pF SMT0402 NPO C1005NP082B0GT DARFON LR(NU)
C531 MO-CAP 8.2pF 50V ±0.5pF SMT0402 NPO C1005NP082B0GT DARFON LR(NU)

C538 330pF 16V 5% SMT0402 X7R LR(NU)
C532 330pF 16V 5% SMT0402 X7R LR(NU)

C119 22pF 50V 5% SMT0402 NPO LR(NU)
C123 22pF 50V 5% SMT0402 NPO LR(NU)
C144 22pF 50V 5% SMT0402 NPO LR(NU)

C118 15pF 50V 5% SMT0402 NPO LR
C126 15pF 50V 5% SMT0402 NPO LR
C143 15pF 50V 5% SMT0402 NPO LR

C532 MO-CAP 8.8pF 50V ±0.25pF SMT0402 NPO LR
C537 MO-CAP 8.8pF 50V ±0.25pF SMT0402 NPO LR

C90 220pF 50V 10% SMT0402 X7R LR(NU)
C540 220pF 50V 10% SMT0402 X7R LR(NU)

U10 — (11) HSYNC — WIDTH=4 MILS Z0=55 ohms — OL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR
3VDDM
U12 — (11) VSYNC — WIDTH=4 MILS Z0=55 ohms — OL-IC NC7SZ126P5X_NL SC-70 5PIN FAIRCHILD LR

Ckeck

3VDDM
Q23 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
(11) Q_VECLK — VECLK_CONN
RP 2.2KΩ 5% SMT1010 4P2R 1/16W LR — RP11
3VDDM — 3VDDM
(11) Q_VEDAT — VEDAT_CONN
Q27 TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR

(7,9,11,14,16,17,18,19,20,21,22,23,24,26,29,30,31,32,33,35,37,39,43,44,45) 3VDDM — 3VDDM
(9,22,27,30,35,39,43,44,45) 5VDDM — 5VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)
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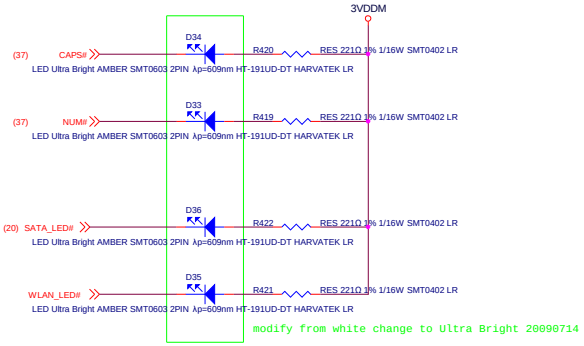
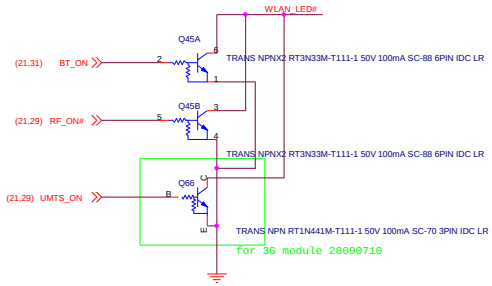
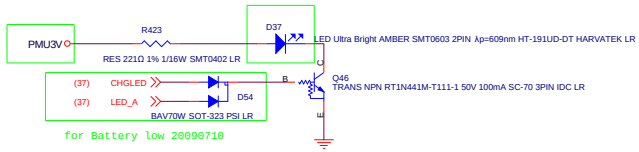
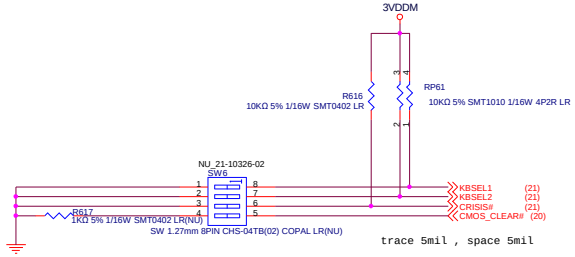
LED indicator control logic







DIP SWITCH



KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

CRISIS#	ON	CRISIS mode
	OFF	Normal
CMOS_CLEAR#	ON	Reset RTC
	OFF	NONE

CHARGER	HDD	CapsLock	NumLock	WIRELESS
		A	1	

Status Indicator SPEC:

Battery Status.
HDD / NAND Flash Status.
CAPS Lock.
NumLock
RF Status.

(20,37,41,43) PMU3V — PMU3V
(9,18,19,20,21,22,23,24,28,29,30,31,33,37,41,43,44) 3VDDA — 3VDDA
(7,9,11,14,16,17,18,19,20,21,22,23,24,25,29,30,31,32,33,35,37,39,43,44,45) 3VDDM — 3VDDM
(22,28,30,31,39,43,44) 5VDDA — 5VDDA
(37,43) PMU5V — PMU5V

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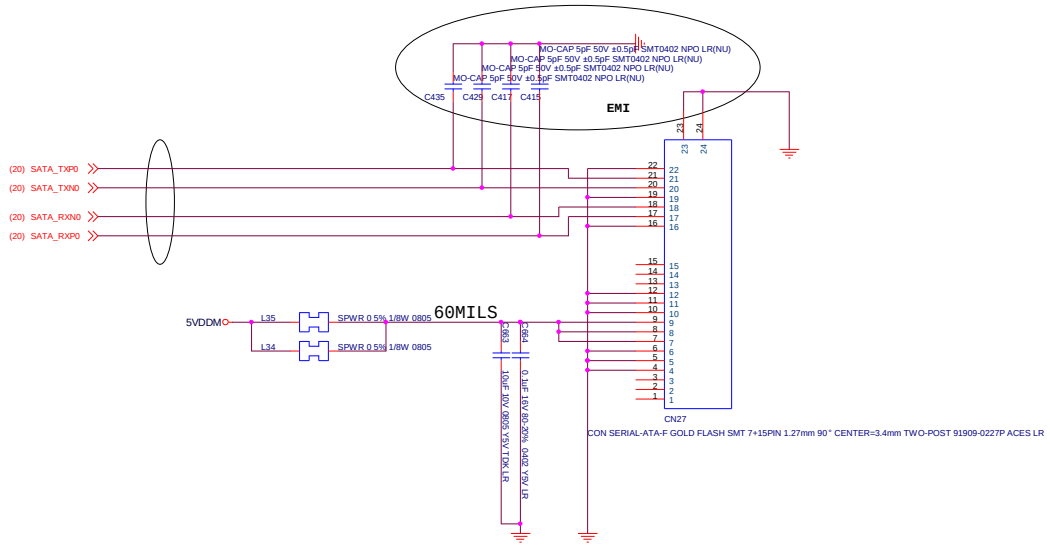
NOTE

SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

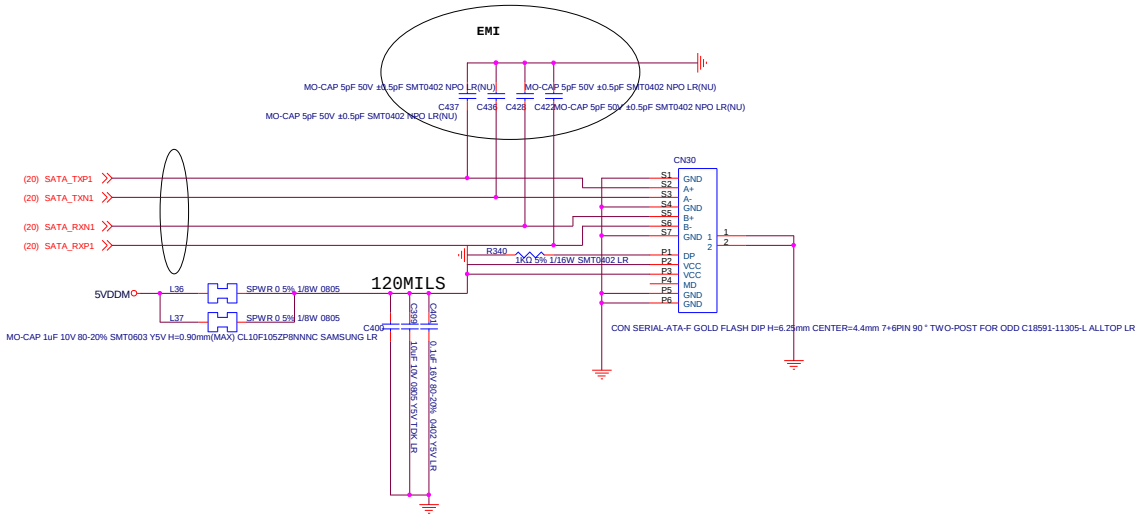
SATA Layout Note:

MS or SL:

* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.



CD-ROM CNN



(9,22,25,30,35,39,43,44,45) 5VDDM 5VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)

Size: C | Document Number: SATA HDD & ODD CON | Rev: 0.1

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檔

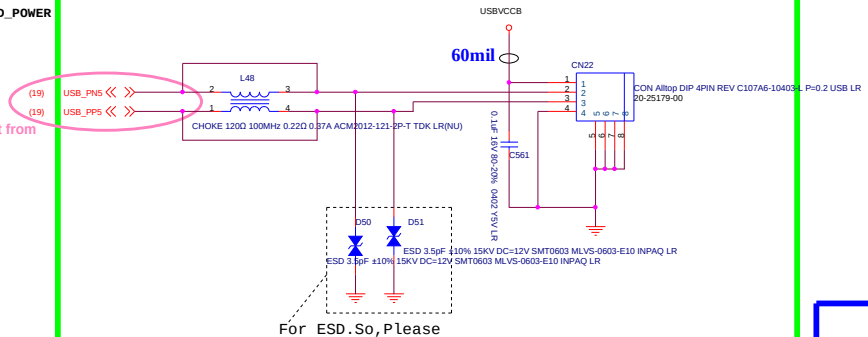
5 mil GND_POWER
10 mil
5 mil USB20_P+
5 mil
5 mil USB20_P-
10 mil
5 mil GND_POWER

20090514 USB Port CO-Lay

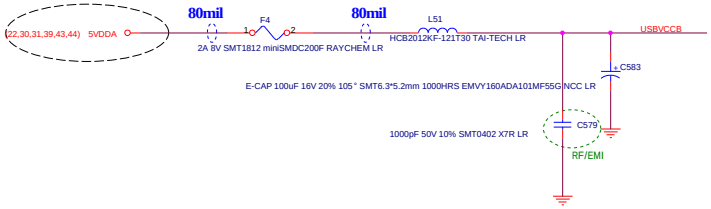
USB Port

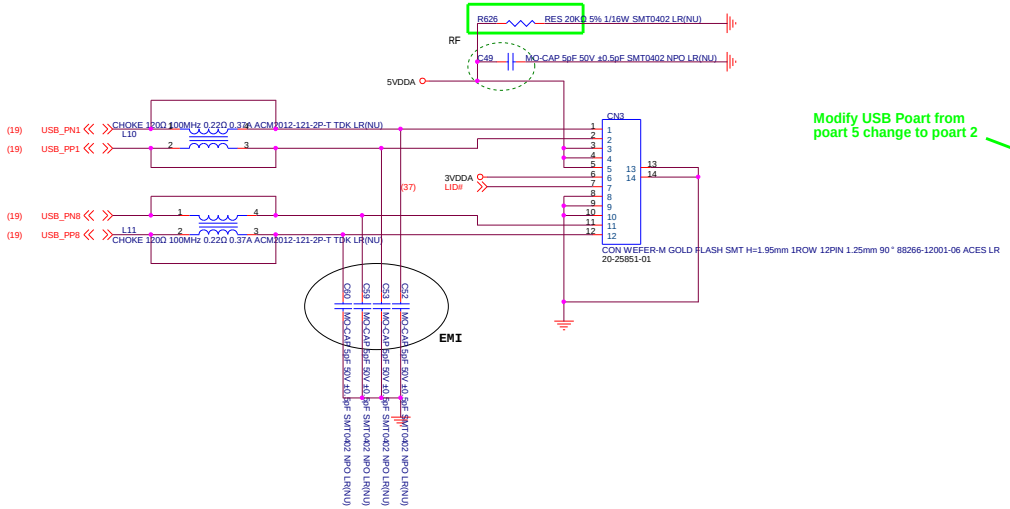
USBP+/- must same length

Modify USB Poart from poart 2 change to poart 5



USB CNN

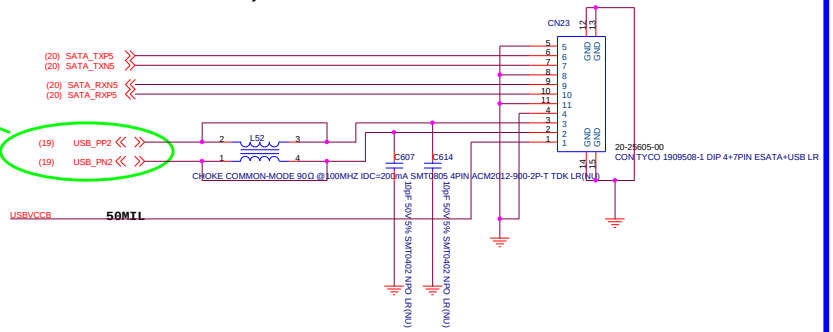




Modify USB Poart from poart 5 change to poart 2

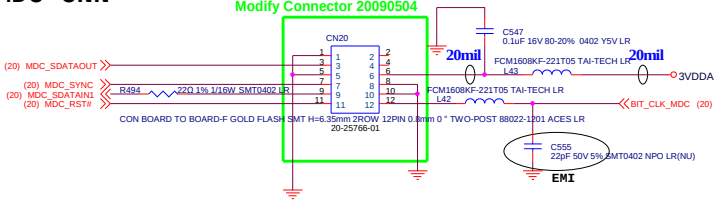
E-SATA Port

V0.2 Modify for BOM



MDC CNN

Modify Connector 20090504



(9,18,19,20,21,22,23,24,29,30,31,33,37,41,43,44) 3VDDA 3VDDA

(22,30,31,39,43,44) 5VDDA 5VDDA

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Size: C | Document Number: USB CNN / MDC CNN / E-SATA | Rev: 0.1

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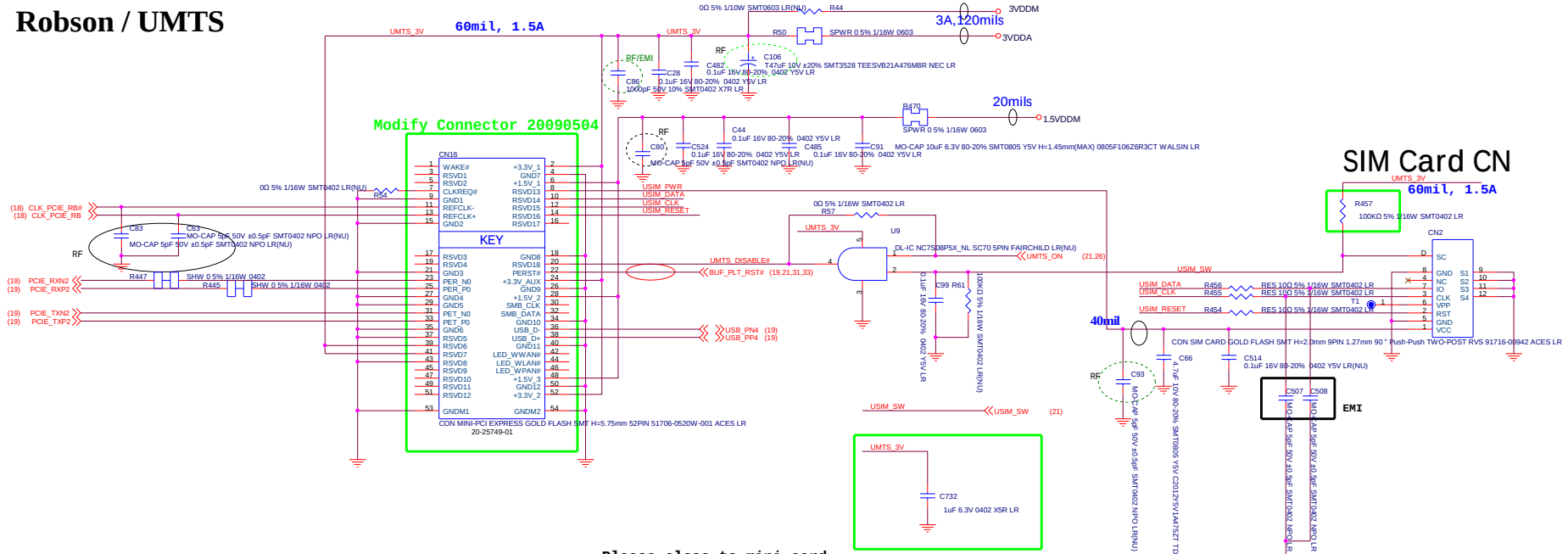
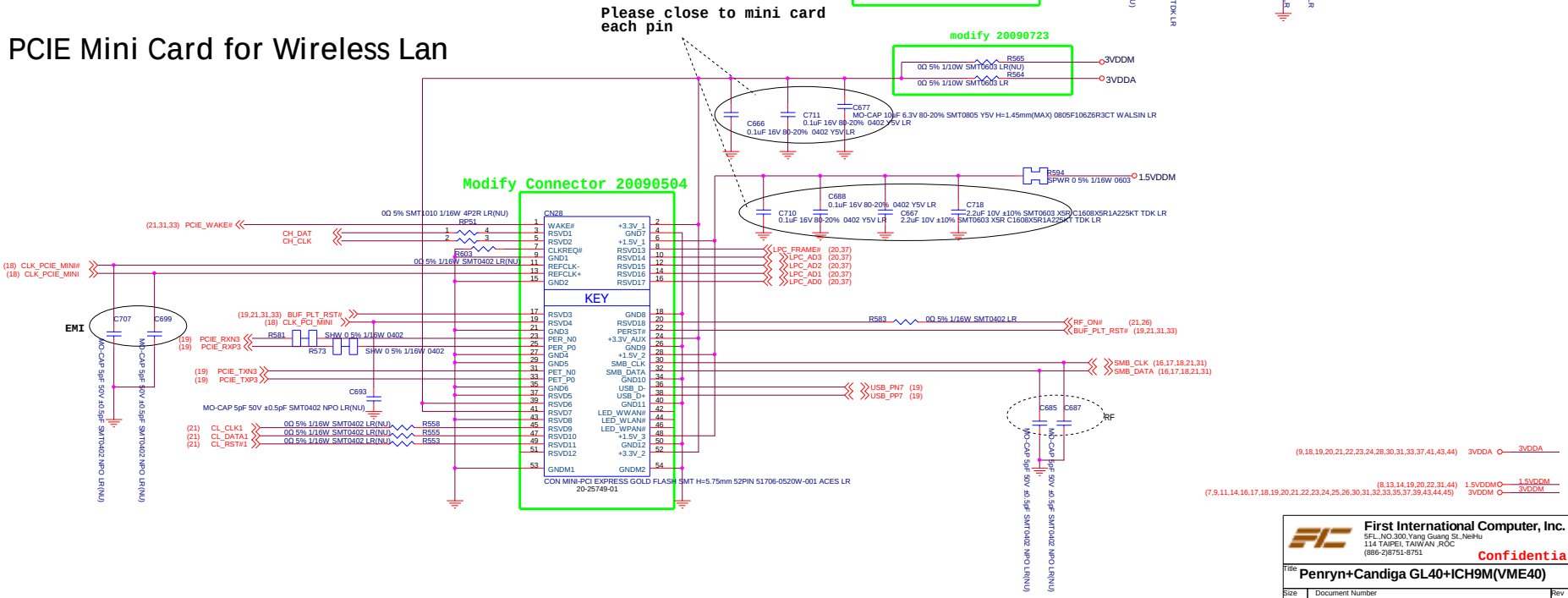
Robson / UMTS



SIM Card CN

PCIE Mini Card for Wireless Lan



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Size	C
Document Number	PCIE Mini / UMTS(3G)
Rev	0.1
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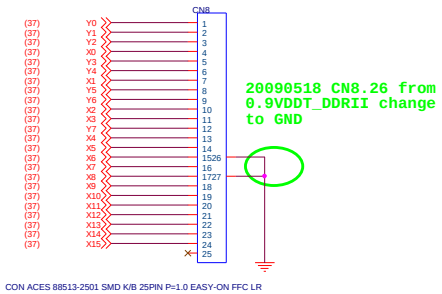
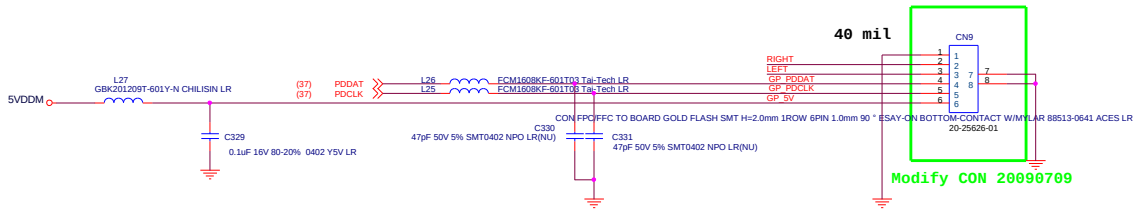
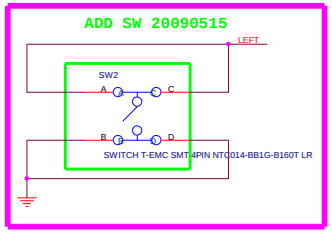
INT KB CNN

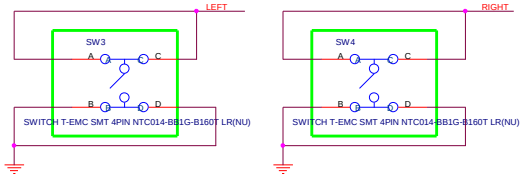


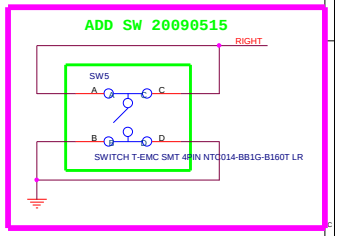
GLIDE PAD CONNECTOR



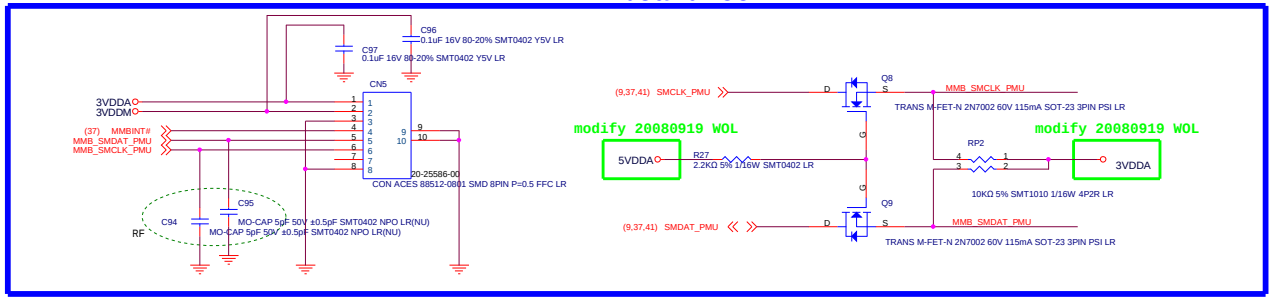
Modify SW 20090504



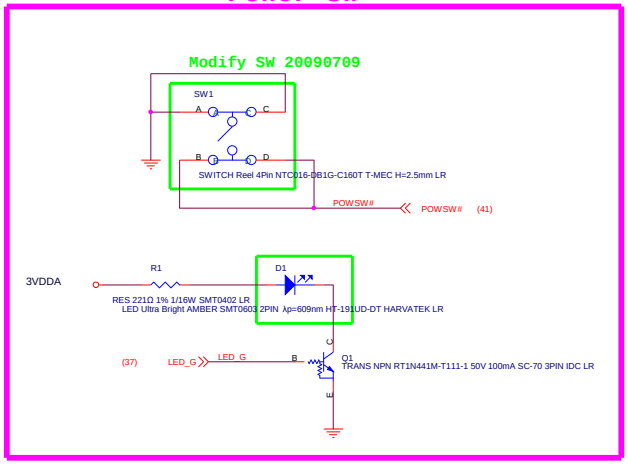




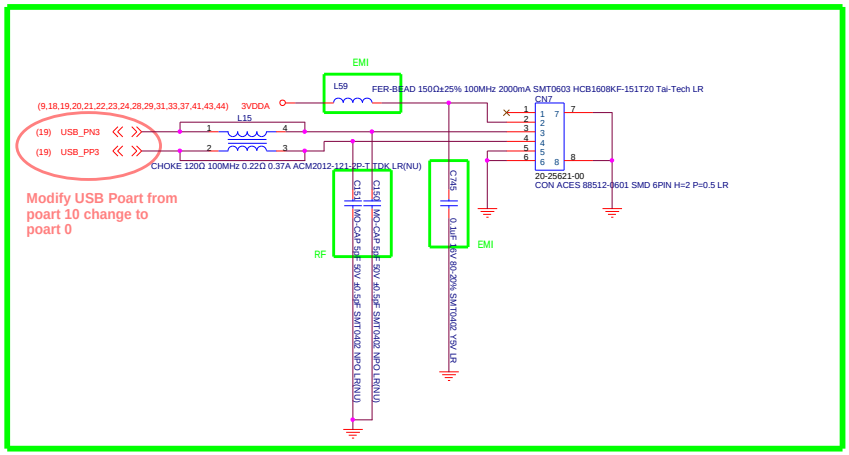
MMB board CON



Power SW



Finger Print CON



(16,17,44) 0.9VDDT_DDRII — 0.9VDDT_DDRII
(22,28,31,39,43,44) 5VDDA — 5VDDA
(7,9,11,14,16,17,18,19,20,21,22,23,24,25,26,29,31,32,33,35,37,39,43,44,45) 3VDDM — 3VDDM
(9,18,19,20,21,22,23,24,28,29,31,33,37,41,43,44) 3VDDA — 3VDDA
(9,22,25,27,35,39,43,44,45) 5VDDM — 5VDDM

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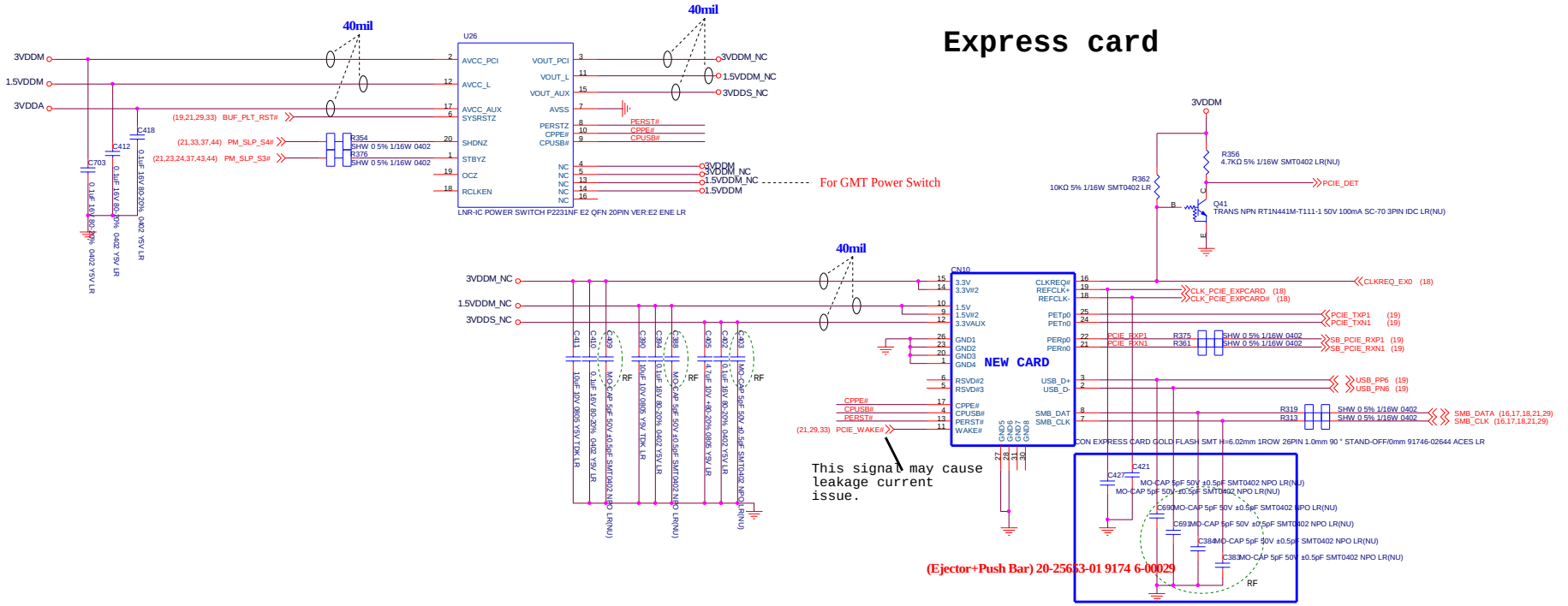
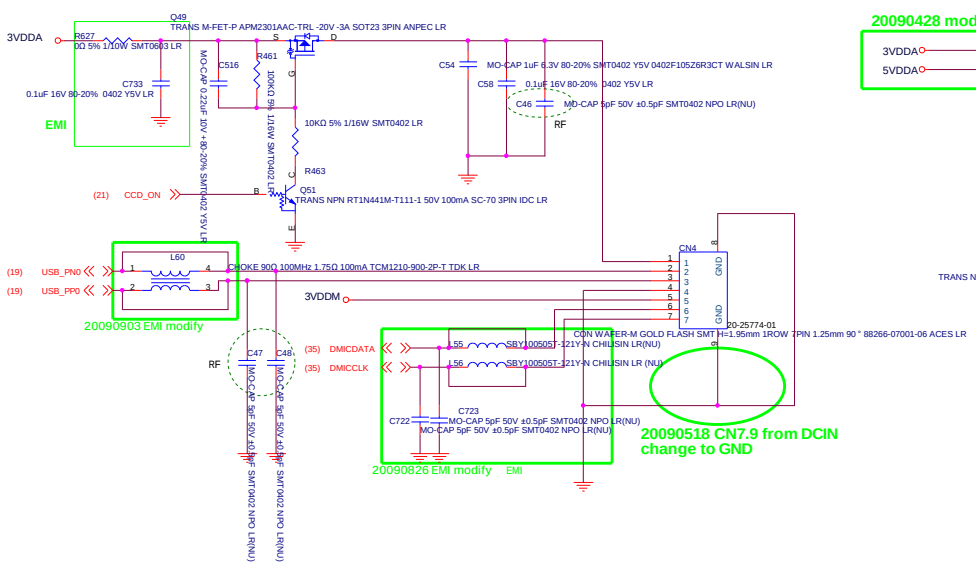
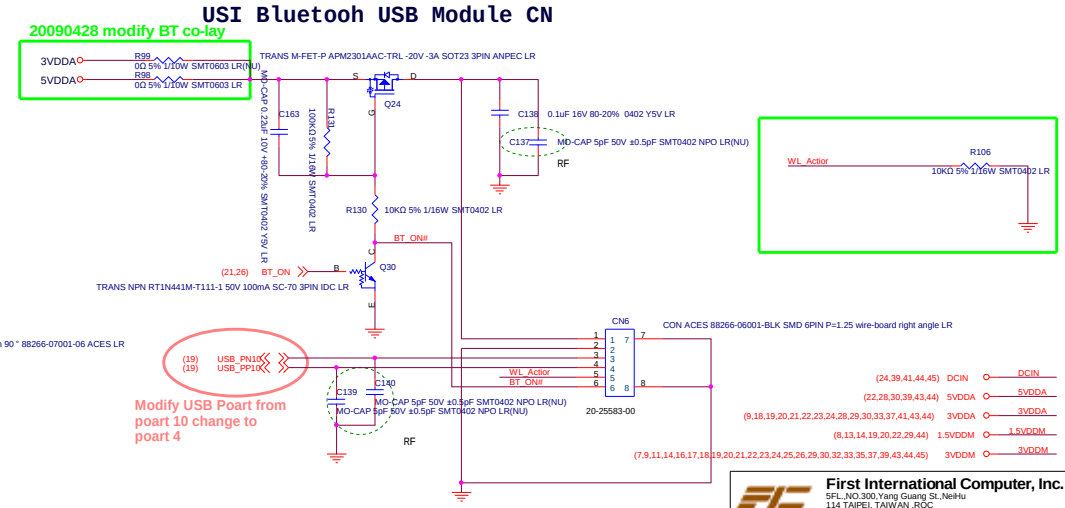
Express card



CCD Module CN



USI Bluetooh USB Module CN



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Express Card / CCD / BT

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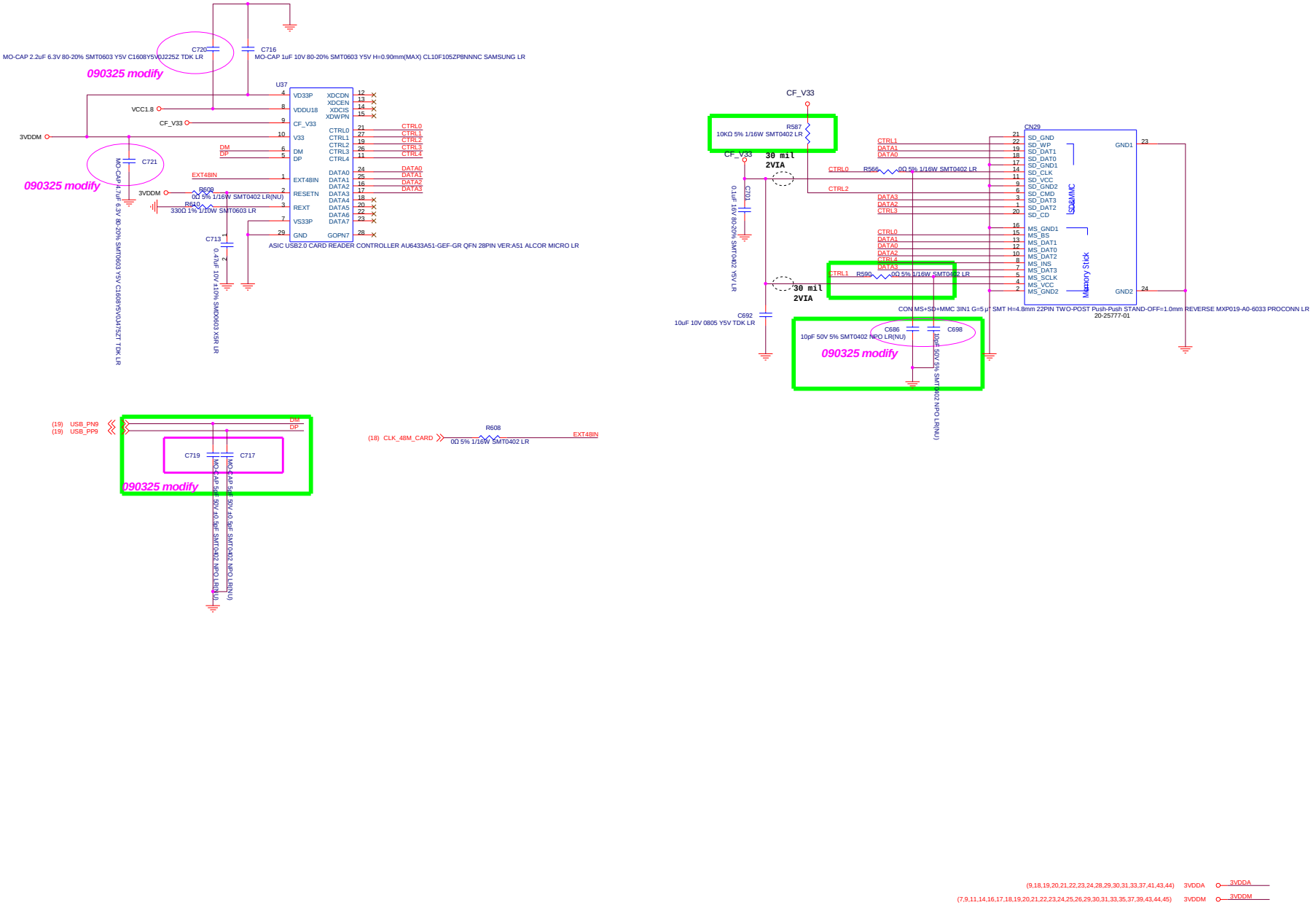
C720
MO-CAP 2.2uF 6.3V 80-20% SMT0603 Y5V C1608Y5VOJ225Z TDK LR
C716
MO-CAP 1uF 10V 80-20% SMT0603 Y5V H=0.90mm(MAX) CL10F105ZP8NNNC SAMSUNG LR
090325 modify
U37
VCC1.8
CF_V33
3VDDM
C721
MO-CAP 4.7uF 6.3V 80-20% SMT0603 Y5V C1608Y5VOJ475Z TDK LR
090325 modify
EXT48IN
R609
0Ω 5% 1/16W SMT0402 LR(NU)
R610
330Ω 1% 1/10W SMT0603 LR
C713
0.47uF 10V ±10% SMX0603 X5R LR
VD33P
VDDU18
CF_V33
V33
DM
DP
EXT48IN
RESETN
REXT
VS33P
GND
XDCDN
XDCEN
XDCIS
XDWPN
CTRL0
CTRL1
CTRL2
CTRL3
CTRL4
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
GOPN7
ASIC USB2.0 CARD READER CONTROLLER AU6433A51-GEF-GR QFN 28PIN VER:A51 ALCOR MICRO LR
(19) USB_PN9
(19) USB_PP9
C719
C717
MO-CAP 4.7uF 6.3V 80-20% SMT0603 Y5V C1608Y5VOJ475Z TDK LR
MO-CAP 4.7uF 6.3V 80-20% SMT0603 Y5V C1608Y5VOJ475Z TDK LR
090325 modify
(18) CLK_48M_CARD
R608
0Ω 5% 1/16W SMT0402 LR
EXT48IN
CF_V33
R587
10KΩ 5% 1/16W SMT0402 LR
30 mil
2VIA
C703
0.1uF 16V 80-20% SMT0402 Y5V LR
C692
10uF 10V 0805 Y5V TDK LR
CN29
CTRL1
DATA1
DATA0
CTRL0
R566
0Ω 5% 1/16W SMT0402 LR
CTRL2
DATA3
DATA2
CTRL3
CTRL0
DATA1
DATA0
DATA2
CTRL4
DATA3
CTRL1
R590
0Ω 5% 1/16W SMT0402 LR
SD_GND
SD_WP
SD_DAT1
SD_DAT0
SD_GND1
SD_CLK
SD_VCC
SD_GND2
SD_CMD
SD_DAT3
SD_DAT2
SD_CD
MS_GND1
MS_BS
MS_DAT1
MS_DAT0
MS_DAT2
MS_INS
MS_DAT3
MS_SCLK
MS_VCC
MS_GND2
GND1
GND2
SD/MMC
Memory Stick
CON MS+SD+MMC 3IN1 G=5 μ' SMT H=4.8mm 22PIN TWO-POST Push-Push STAND-OFF=1.0mm REVERSE MXP019-A0-6033 PROCONN LR
20-25777-01
C686
10pF 50V 5% SMT0402 NPO LR(NU)
C698
10pF 50V 5% SMT0402 NPO LR(NU)
090325 modify
(9,18,19,20,21,22,23,24,28,29,30,31,33,37,41,43,44) 3VDDA
3VDDA
(7,9,11,14,16,17,18,19,20,21,22,23,24,25,26,29,30,31,33,35,37,39,43,44,45) 3VDDM
3VDDM
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Size C
Document Number
AU6433 (Card Reader)
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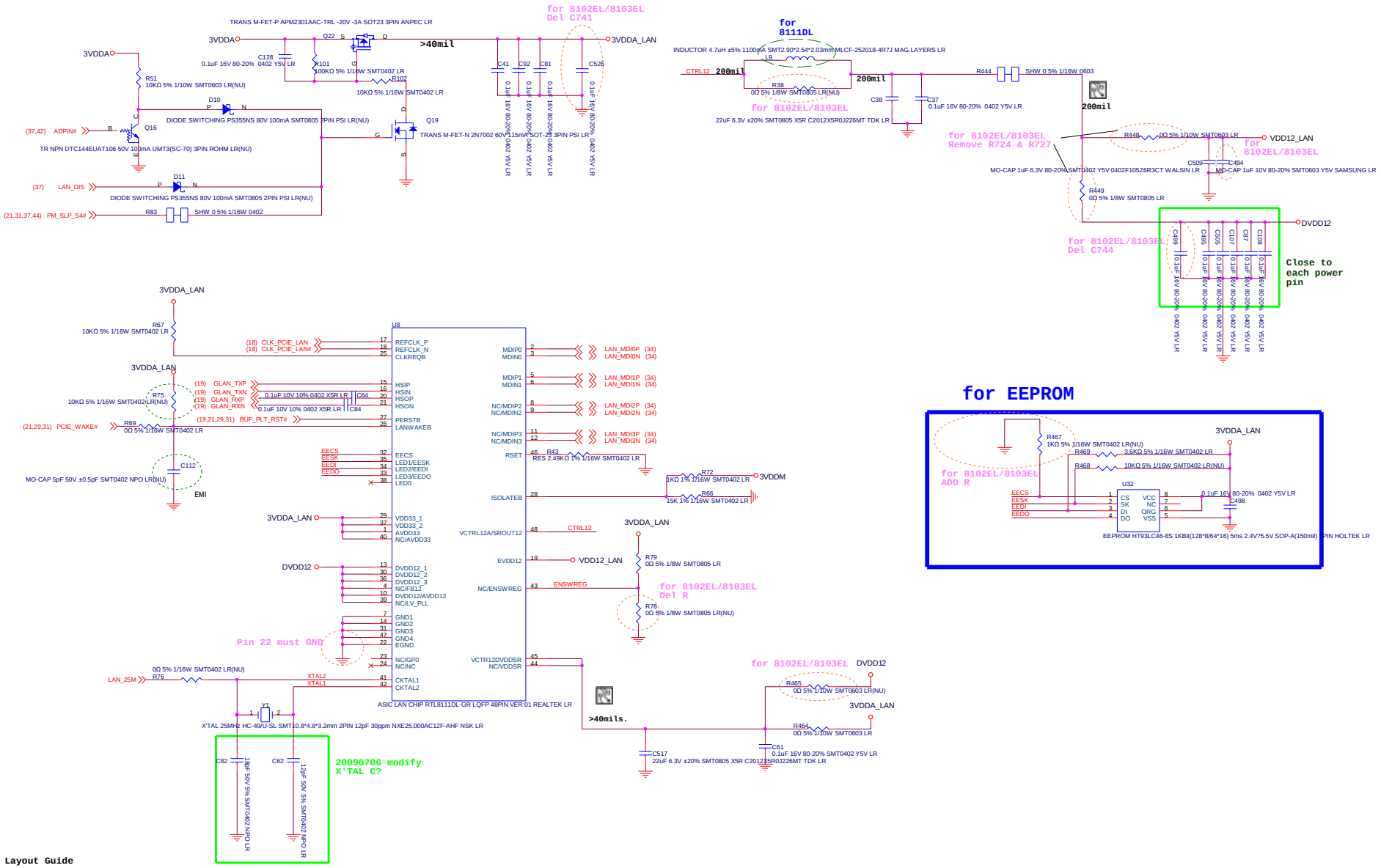
檔



Layout Guide

1.The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.
10.PLACE GND PLANE AS LARGE AS POSSIBLE
11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.
12.It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analong power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15.The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

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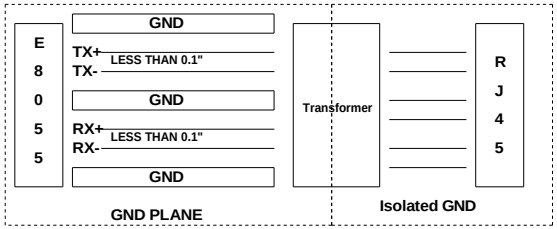
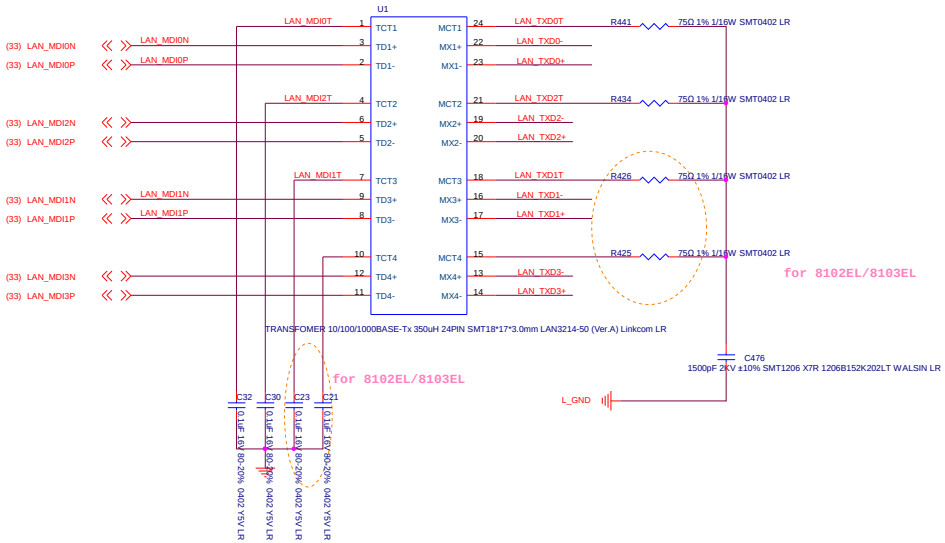
檔

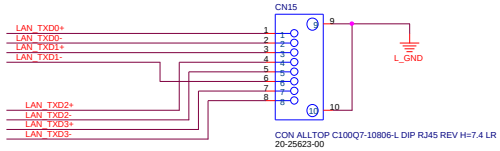
TX
RX

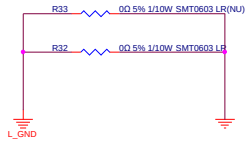
100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length



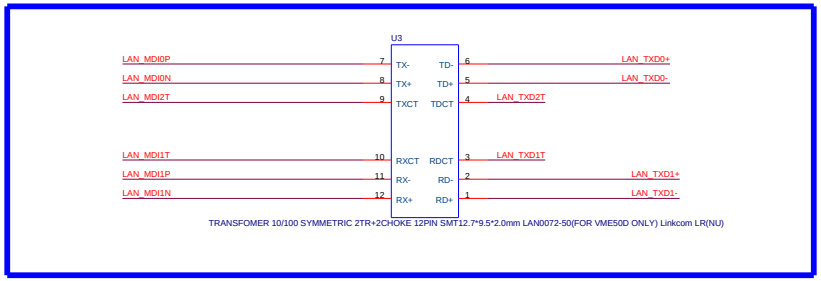
GIGA:Transformer use LAN3214-50(12-02109-02)







10/100:Transformer use LAN0072-50(12-02209-01)
10/100:Transformer use LAN0054-53(12-02150-03)



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10mil GND_POWER
10mil 10mil 14MCLK_AC97
10mil 10mil GND_POWER

AC97/HDA CODEC DUAL LAYOUT

AC97 USE VIA VT1708

A_GND 10mil
LINE_OUT_L 10mil
A_GND 10mil
LINE_OUT_R 10mil
A_GND 10mil

HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#

ICH7m L1 L2 39ohm L3 HD Audio
ICH7m L1 L2 39ohm L3 MDC CONN

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"~2.5" L2 <= 0.1" L3 = 1"~8"

*** L3 can be extened up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN

ICH7m L1 39ohm L2 HD Audio

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"~15" L2 <= 0.5"

*** Breakout can be routed 4 on 4 up to 500 mils

Place next to pin27
Place next to pin34
Place next to pin40
Place next to pin13
Please close to CODEC CHIP
Please close to AMP CHIP
Modify 0603 change to 0402
20090630 bo-sound issue
Modify Add Diode
Please close to CODEC CHIP
Please close to AMP CHIP
20 mils
20 mils
EMI
EMI
ASIC AUDIO CODEC (4CH) ALC272-GR LQFP 48PIN VER:A REALTEK LR
LNR-IC Audio-AMP APA2030RI-TRL(G) 2.6W SSOP 24PIN ANPEC LR
DL-IC NC7S08P5X_NL SC70 5PIN FAIRCHILD LR
DIODE STKY RB751V-40 40V 200mA SOD-323 2PIN PSI LR(NU)
MO-CAP 220pF 25V 5% SMT0402 NPO C1005NP0221JFT DARFON LR(NU)
SBY100505T-121Y-N CHILISIN LR(NU)

AUDIO_GND
EP PIN
Connect the exposed thermal pad to AUDIO_GND

60 mils 60 mils

CODEC POWER:

AVDD1	5V or 3.3V	Analog power for mixer and amplifier
AVDD2	5V or 3.3V	Analog power for DACs and ADCs
DVDD	3.3V	Digital core power for core logic
DVDD I/O	3.3V or 1.5V	Digital I/O power for HDA link.
PVDD1	5V	Power supply for full-bridge left channel
PVDD2	5V	Power supply for full-bridge right channel

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Size: Custom | Document Number: ALC272 CODEC | Rev: 0.1
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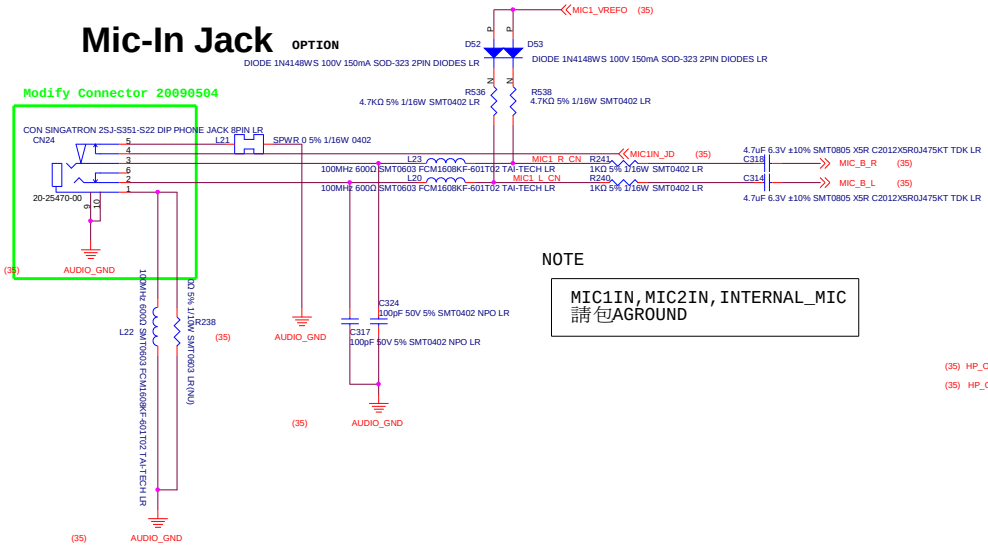
Mic-In Jack

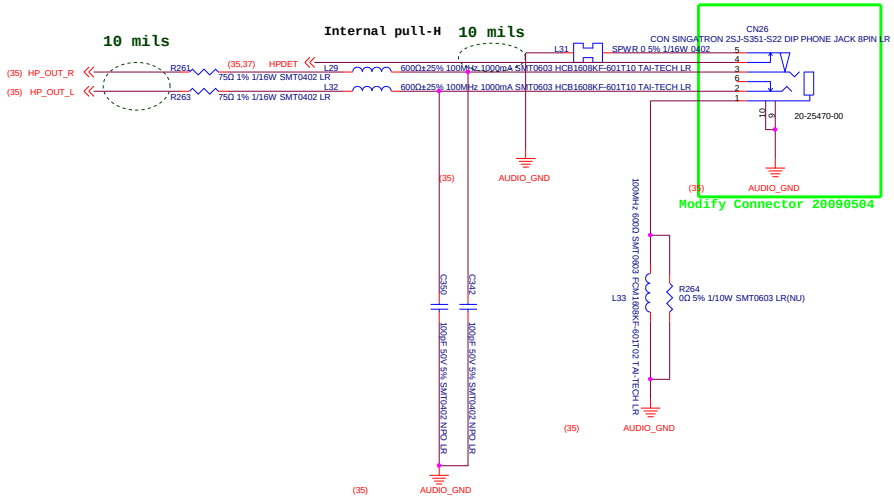
OPTION



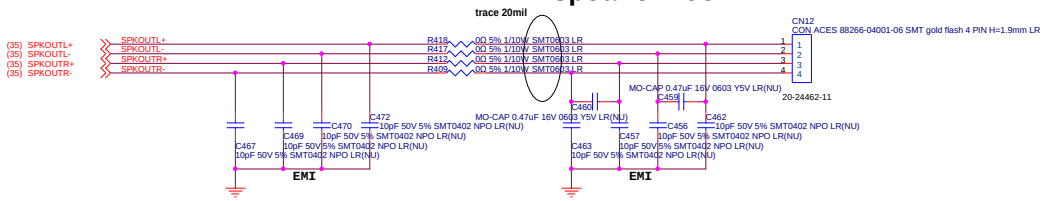
NOTE

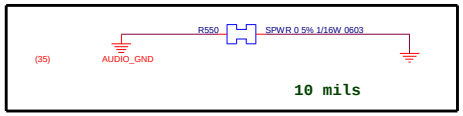
MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND

Head-Phone Jack



Speaker Conn





(9,22,25,27,30,35,39,43,44,45) 5VDDM

5VDDM

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Title: Penryn+Candiga GL40+ICH9M(VME40)

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C	HP OUT & MIC IN	0.1

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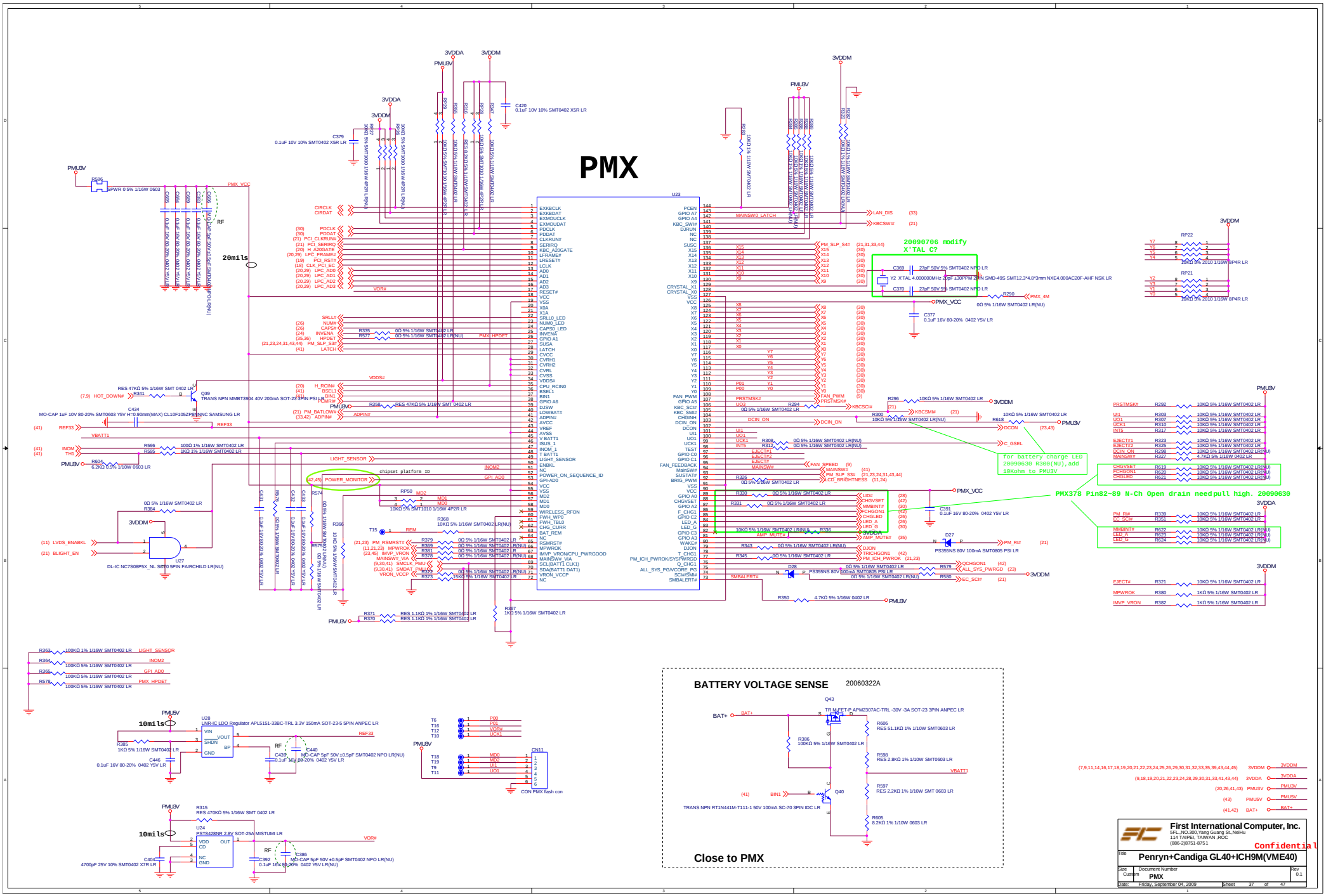
PMX
20090706 modify X'TAL C?
for battery charge LED 20090630 R309(NU),add 10Kohm to PMU3V
PMX378 Pin82~89 N-Ch Open drain needpull high. 20090630
BATTERY VOLTAGE SENSE 20060322A
Close to PMX
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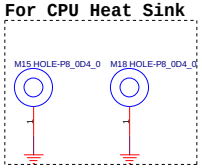
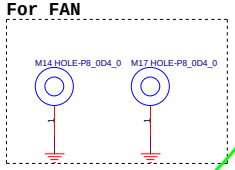
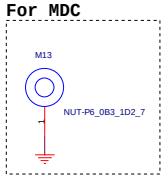
stuff
P/N:24-10966-51
For CPU Heat Sink



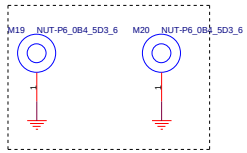
stuff
P/N:24-10966-51
For FAN



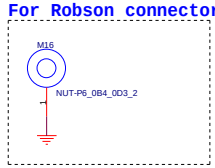
stuff
P/N:24-10732-21
For MDC



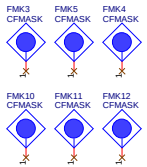
stuff
P/N:24-11743-50
For mini car

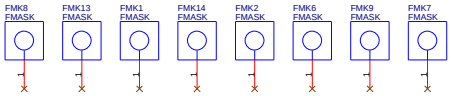


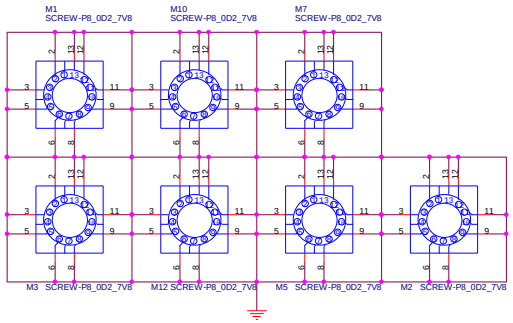
Not stuff 8/16 for Robson
P/N:24-11618-50
For Robson connector NUT

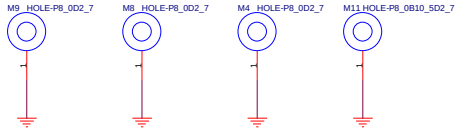


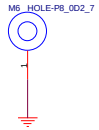
20080518 modify hole



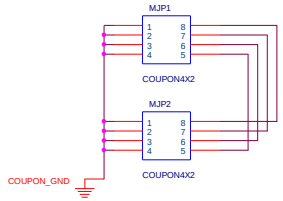








COUPON4X2



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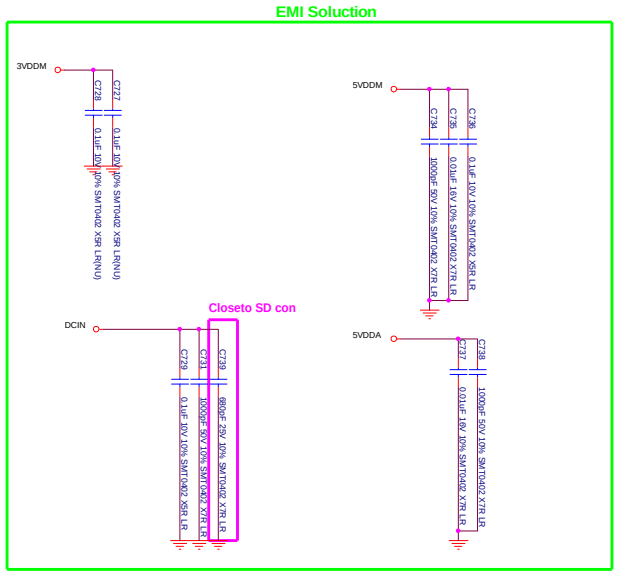

(22,28,30,31,43,44) 5VDDA 5VDDA

(7,9,11,14,16,17,18,19,20,21,22,23,24,25,26,29,30,31,32,33,35,37,43,44,45) 3VDDM 3VDDM

(9,22,25,27,30,35,43,44,45) 5VDDM 5VDDM

(24,41,44,45) DCIN DCIN

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Title
Penryn+Candiga GL40+ICH9M(VME40)

Size	Document Number	Rev
C	**BLOCK**	0.1

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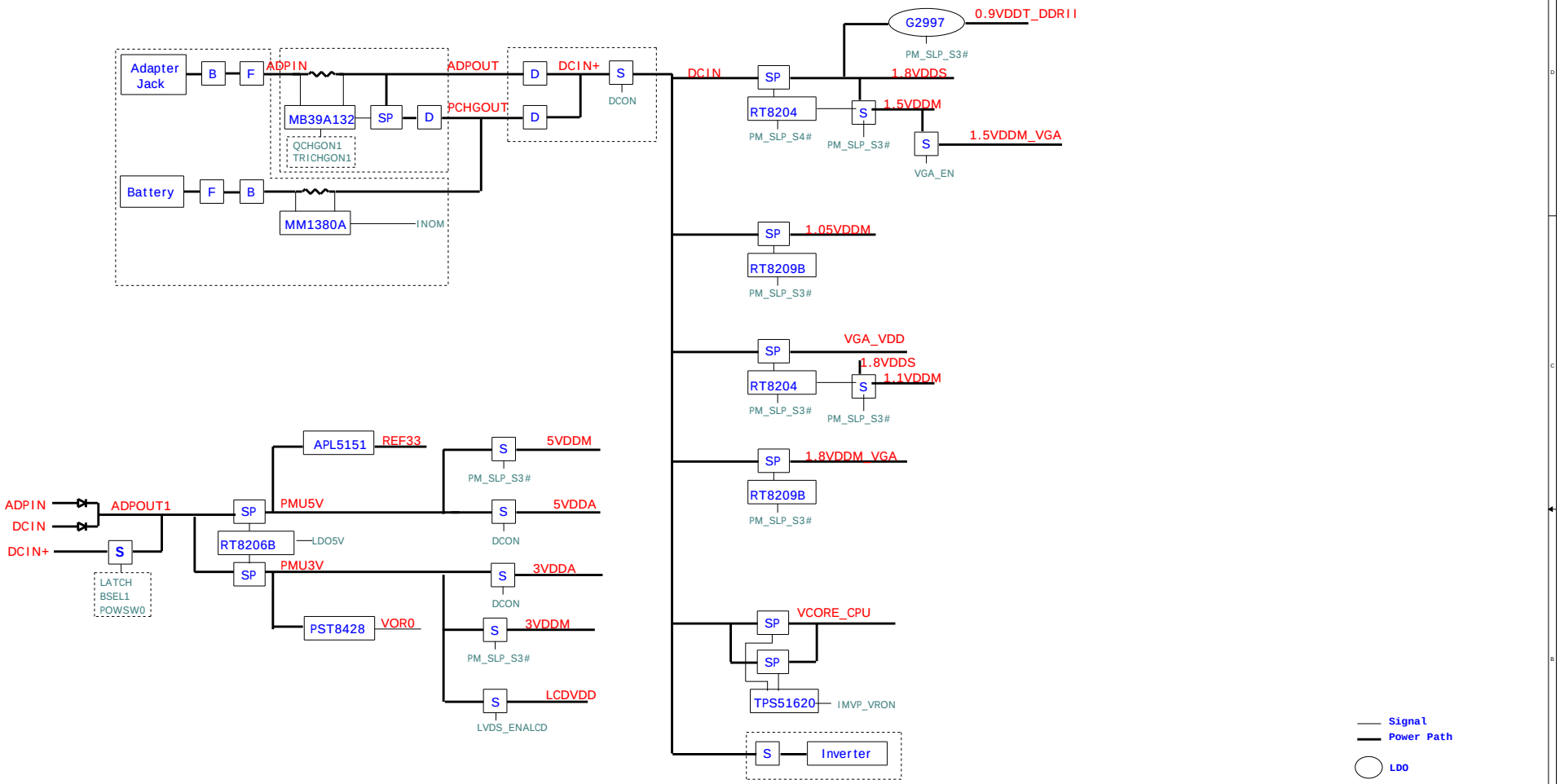
VME50 Power Block



Signal
Power Path
LDO
B Bead
D Diode
F Fuse
S Switch
SP Switching Power Converter

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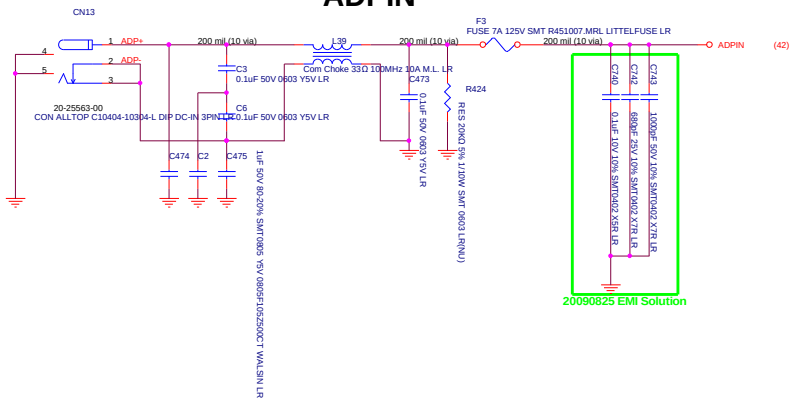
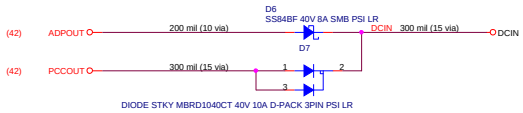
ADPIN, BATIN, DCIN, ADPOUT+

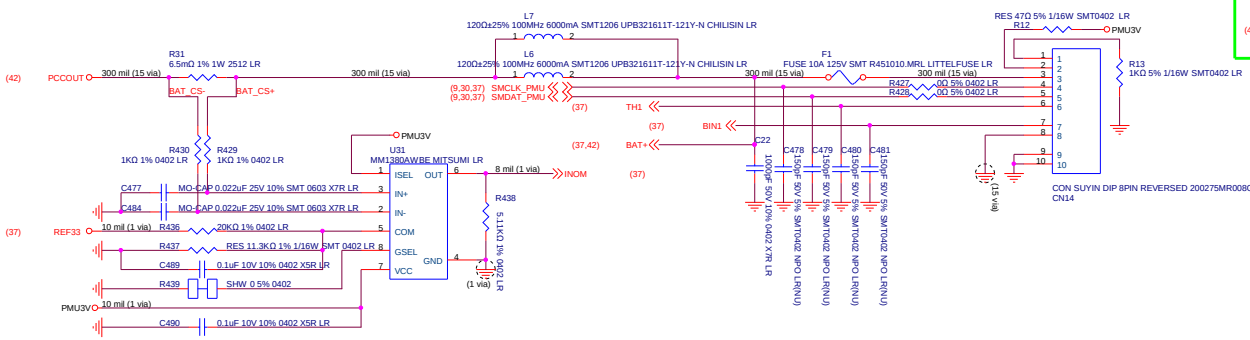
ADPIN



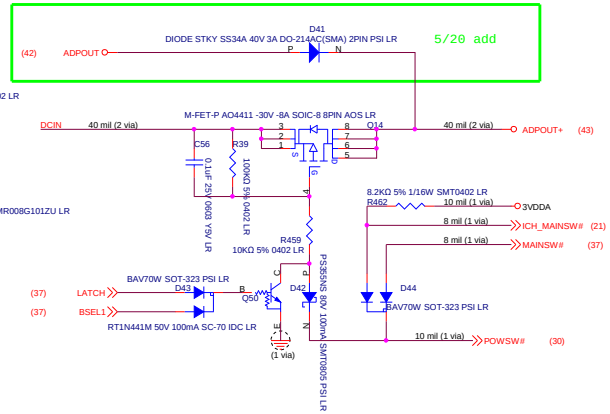
DCIN



BATIN



ADPOUT+



(24,39,44,45) DCIN — DCIN
(20,26,37,43) PMU3V — PMU3V
(9,18,19,20,21,22,23,24,28,29,30,31,33,37,43,44) 3VDDA — 3VDDA

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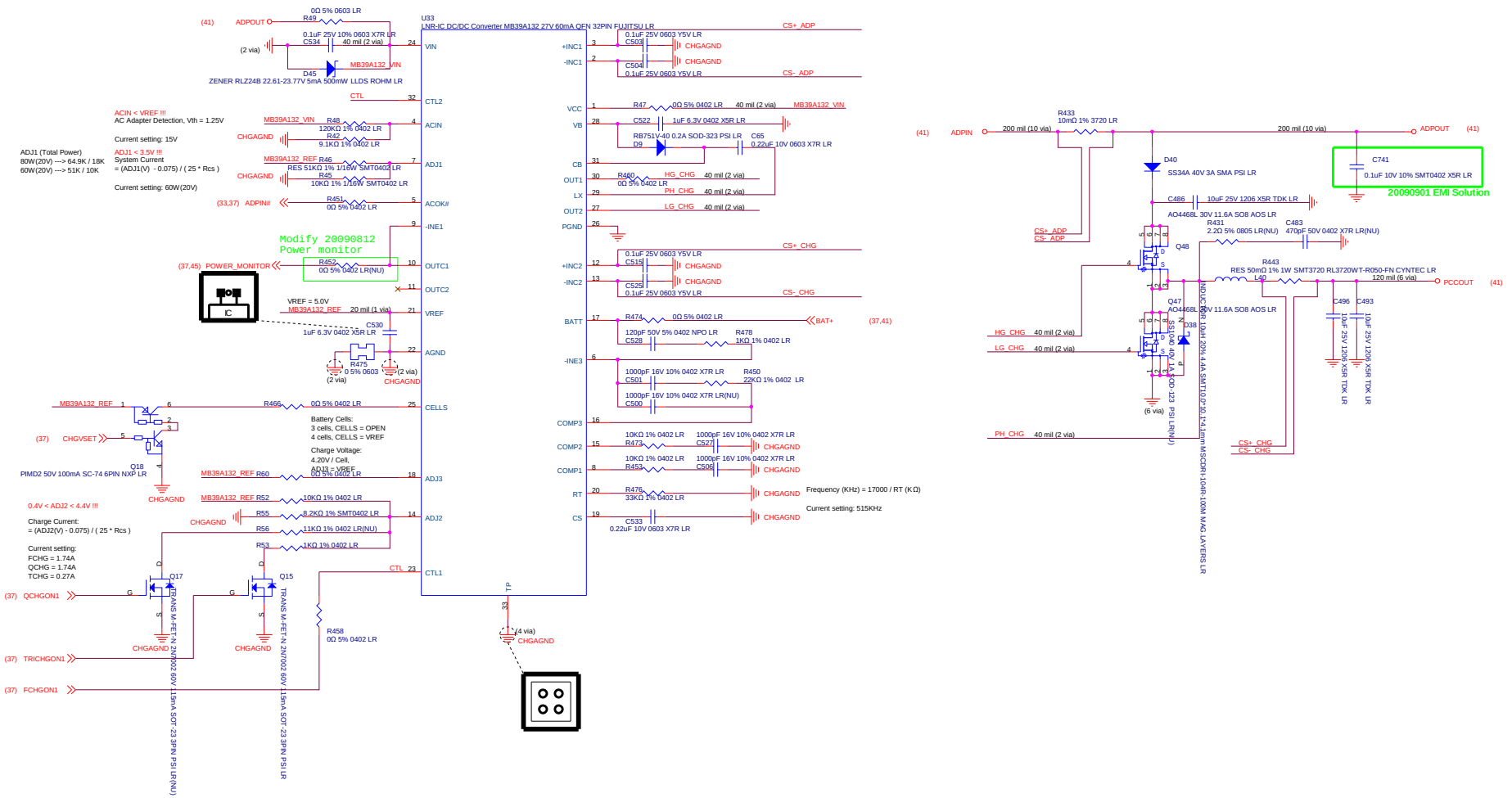
Charger



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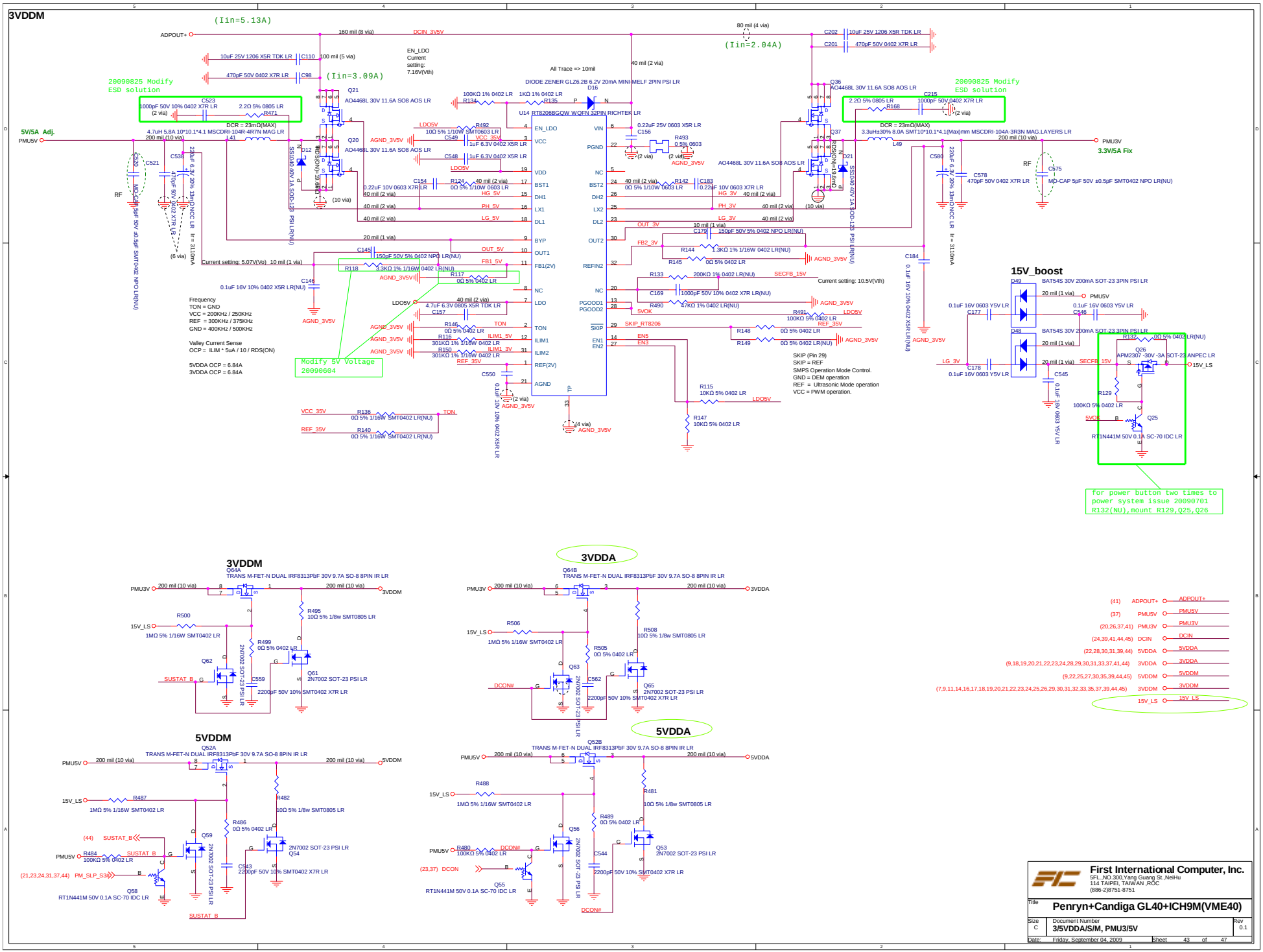
3VDDM
(Iin=5.13A)
ADPOUT+
160 mil (8 via)
DCIN_3V5V
EN_LDO
Current setting: 7.16V(Vth)
All Trace => 10mil
80 mil (4 via)
(Iin=2.04A)
C202 10uF 25V 1206 X5R TDK LR
C201 470pF 50V 0402 X7R LR
10uF 25V 1206 X5R TDK LR C110
100 mil (5 via)
470pF 50V 0402 X7R LR C98
(Iin=3.09A)
20090825 Modify ESD solution
Q21 AO4468L 30V 11.6A SO8 AOS LR
1000pF 50V 10% 0402 X7R LR (2 via) C523
2.2Ω 5% 0805 LR R471
DCR = 23mΩ(MAX)
5V/5A Adj.
PMU5V
4.7uH 5.8A 10*10.1*4.1 MSCDRI-104R-4R7N MAG LR L41
200 mil (10 via)
C521 MCD-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
C538 220uF 6.3V 20% 13mΩ NCC LR
470pF 50V 0402 X7R LR
(6 via)
Irt = 3110mA
RF
Q20 AO4468L 30V 11.6A SO8 AOS LR
SS1040-40V 1A SOD-123 PSI LR(NU)
D12
(10 via)
LDO5V
R492 10Ω 5% 1/10W SMT0603 LR
C549 1uF 6.3V 0402 X5R LR
VCC_35V
C548 1uF 6.3V 0402 X5R LR
C154 0.22uF 10V 0603 X7R LR
R124 0Ω 5% 1/10W 0603 LR
40 mil (2 via)
HG_5V
PH_5V
LG_5V
20 mil (1 via)
OUT_5V
FB1_5V
C145 150pF 50V 5% 0402 NPO LR(NU)
R118 3.3KΩ 1% 1/16W 0402 LR(NU)
R117 0Ω 5% 0402 LR
AGND_3V5V
C146 0.1uF 16V 10% 0402 X5R LR(NU)
Current setting: 5.07V(Vo) 10 mil (1 via)
Frequency
TON = GND
VCC = 200KHz / 250KHz
REF = 300KHz / 375KHz
GND = 400KHz / 500KHz
Valley Current Sense
OCP = ILIM * 5uA / 10 / RDS(ON)
5VDDA OCP = 6.84A
3VDDA OCP = 6.84A
Modify 5V Voltage 20090604
C157 4.7uF 6.3V 0805 X5R TDK LR
R146 0Ω 5% 0402 LR
TON
R116 301KΩ 1% 1/16W 0402 LR
ILIM1_5V
R150 301KΩ 1% 1/16W 0402 LR
ILIM1_3V
REF_35V
C550 0.1uF 10V 0402 X5R LR
VCC_35V
R136 0Ω 5% 1/16W SMT0402 LR(NU)
REF_35V
R140 0Ω 5% 1/16W SMT0402 LR(NU)
DIODE ZENER GLZ6.2B 6.2V 20mA MINI-MELF 2PIN PSI LR
D16
100KΩ 1% 0402 LR R134
1KΩ 1% 0402 LR R135
U14 RT8206BGQW WQFN 32PIN RICHTEK LR
EN_LDO
VCC
VDD
BST1
DH1
LX1
DL1
BYP
OUT1
FB1(2V)
NC
LDO
TON
ILIM1
ILIM2
REF(2V)
AGND
VIN
PGND
BST2
DH2
LX2
DL2
OUT2
FB2_3V
REFIN2
PGOOD1
PGOOD2
SKIP
EN1
EN2
C156 0.22uF 25V 0603 X5R LR
R493 0.5Ω 0603
C183 0.22uF 10V 0603 X7R LR
R142 0Ω 5% 1/10W 0603 LR
OUT_3V
C179 150pF 50V 5% 0402 NPO LR(NU)
R144 3.3KΩ 1% 1/16W 0402 LR(NU)
R145 0Ω 5% 0402 LR
R133 200KΩ 1% 0402 LR(NU)
SECFB_15V
C169 1000pF 50V 10% 0402 X7R LR(NU)
R490 47KΩ 1% 0402 LR(NU)
5VOK
SKIP_RT8206
EN5
EN3
R491 100KΩ 5% 0402 LR
R148 0Ω 5% 0402 LR
R149 0Ω 5% 0402 LR(NU)
R115 10KΩ 5% 0402 LR
R147 10KΩ 5% 0402 LR
Current setting: 10.5V(Vth)
SKIP (Pin 29)
SKIP = REF
SMPS Operation Mode Control.
GND = DEM operation
REF = Ultrasonic Mode operation
VCC = PWM operation.
Q36 AO4468L 30V 11.6A SO8 AOS LR
20090825 Modify ESD solution
2.2Ω 5% 0805 LR R168
1000pF 50V 0402 X7R LR C215
Q37 AO4468L 30V 11.6A SO8 AOS LR
D21 SS1040-40V 1A SOD-123 PSI LR(NU)
DCR = 23mΩ(MAX)
3.3uH±30% 8.0A SMT10*10.1*4.1(Max)mm MSCDRI-104A-3R3N MAG.LAYERS LR
L49
200 mil (10 via)
PMU3V
3.3V/5A Fix
C580 220uF 6.3V 20% 13mΩ NCC LR
C578 470pF 50V 0402 X7R LR
C575 MD-CAP 5pF 50V ±0.5pF SMT0402 NPO LR(NU)
C184 0.1uF 16V 10% 0402 X5R LR(NU)
15V_boost
D49 BAT54S 30V 200mA SOT-23 3PIN PSI LR
D48 BAT54S 30V 200mA SOT-23 3PIN PSI LR
20 mil (1 via)
PMU5V
0.1uF 16V 0603 Y5V LR
C177
C546
C178
C545
R132 0Ω 5% 0402 LR(NU)
Q26 APM2307 -30V -3A SOT-23 ANPEC LR
15V_LS
R129 100KΩ 5% 0402 LR
Q25 RT1N441M 50V 0.1A SC-70 IDC LR
for power button two times to power system issue 20090701 R132(NU),mount R129,Q25,Q26
3VDDM
Q64A TRANS M-FET-N DUAL IRF8313PbF 30V 9.7A SO-8 8PIN IR LR
PMU3V
200 mil (10 via)
3VDDM
R500 1MΩ 5% 1/16W SMT0402 LR
15V_LS
R495 10Ω 5% 1/8w SMT0805 LR
R499 0Ω 5% 0402 LR
Q62
Q61 2N7002 SOT-23 PSI LR
SUSTAT_B
C559 2200pF 50V 10% SMT0402 X7R LR
3VDDA
Q64B TRANS M-FET-N DUAL IRF8313PbF 30V 9.7A SO-8 8PIN IR LR
3VDDA
R506 1MΩ 5% 1/16W SMT0402 LR
R508 10Ω 5% 1/8w SMT0805 LR
R505 0Ω 5% 0402 LR
Q63
Q65 2N7002 SOT-23 PSI LR
DCON#
C562 2200pF 50V 10% SMT0402 X7R LR
5VDDM
Q52A TRANS M-FET-N DUAL IRF8313PbF 30V 9.7A SO-8 8PIN IR LR
5VDDM
R487 1MΩ 5% 1/16W SMT0402 LR
R482 10Ω 5% 1/8w SMT0805 LR
R486 0Ω 5% 0402 LR
(44) SUSTAT_B
Q59
2N7002 SOT-23 PSI LR Q54
R484 100KΩ 5% 0402 LR
(21,23,24,31,37,44) PM_SLP_S3#
Q58 RT1N441M 50V 0.1A SC-70 IDC LR
C543 2200pF 50V 10% SMT0402 X7R LR
5VDDA
Q52B TRANS M-FET-N DUAL IRF8313PbF 30V 9.7A SO-8 8PIN IR LR
5VDDA
R488 1MΩ 5% 1/16W SMT0402 LR
R481 10Ω 5% 1/8w SMT0805 LR
R489 0Ω 5% 0402 LR
Q56
Q53 2N7002 SOT-23 PSI LR
R480 100KΩ 5% 0402 LR
(23,37) DCON
Q55 RT1N441M 50V 0.1A SC-70 IDC LR
C544 2200pF 50V 10% SMT0402 X7R LR
(41) ADPOUT+
(37) PMU5V
(20,26,37,41) PMU3V
(24,39,41,44,45) DCIN
(22,28,30,31,39,44) 5VDDA
(9,18,19,20,21,22,23,24,28,29,30,31,33,37,41,44) 3VDDA
(9,22,25,27,30,35,39,44,45) 5VDDM
(7,9,11,14,16,17,18,19,20,21,22,23,24,25,26,29,30,31,32,33,35,37,39,44,45) 3VDDM
15V_LS
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Title
Penryn+Candiga GL40+ICH9M(VME40)
Size C
Document Number 3/5VDDA/S/M, PMU3/5V
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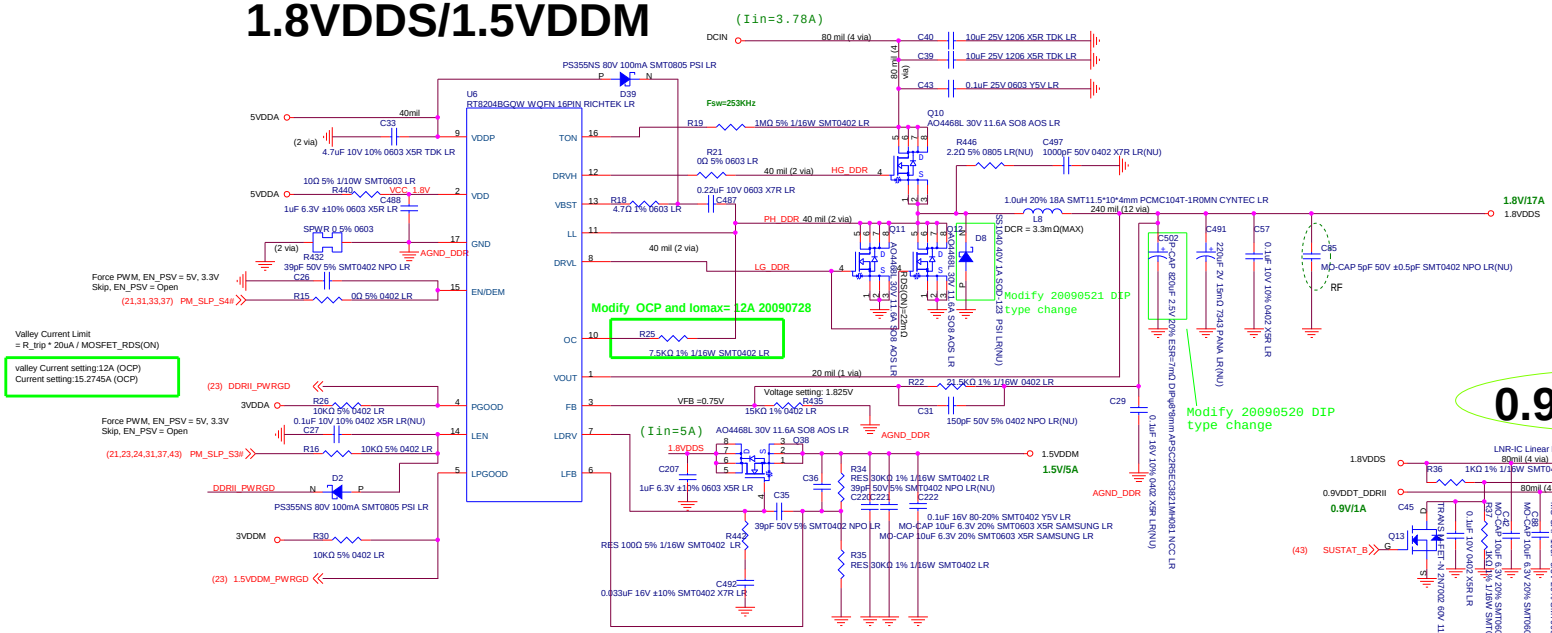
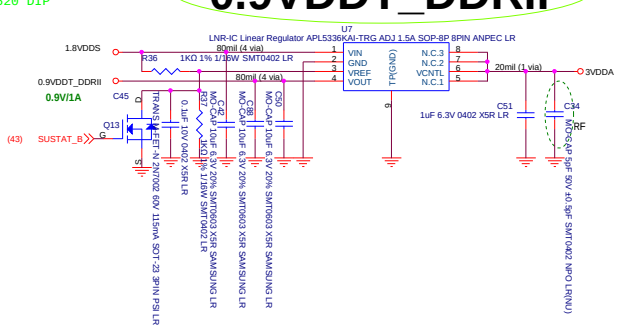
1.8VDDS / 1.5VDDM / 0.9VDDM/1.05VDDM

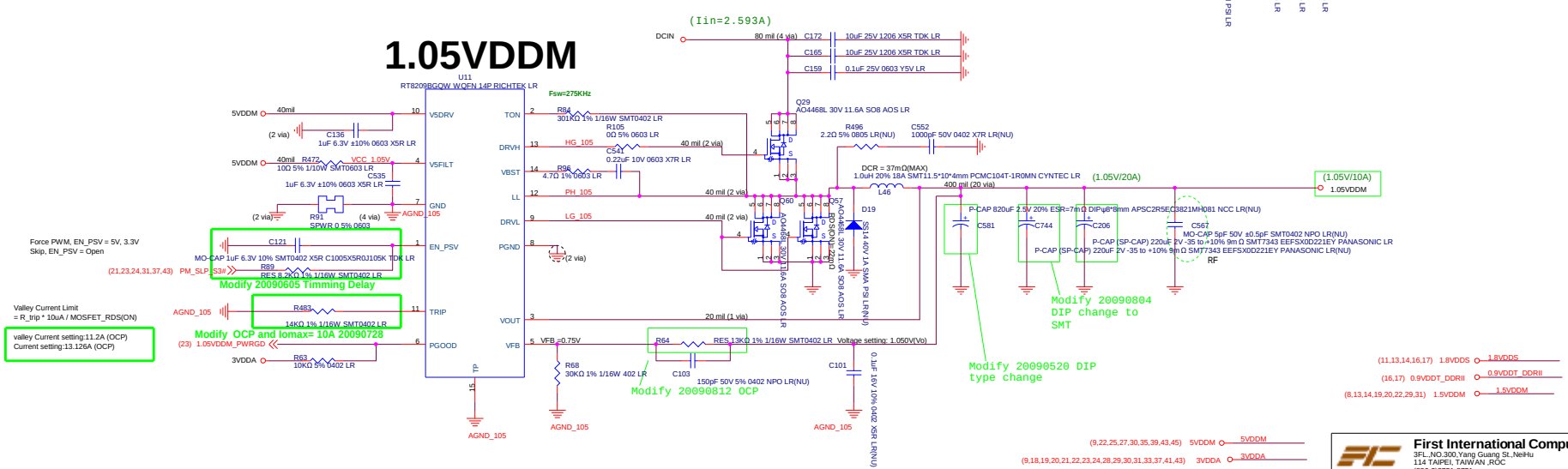
1.8VDDS/1.5VDDM



0.9VDDT_DDRII



1.05VDDM



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Title	Penryn+Candiga GL40+ICH9M(VME40)	
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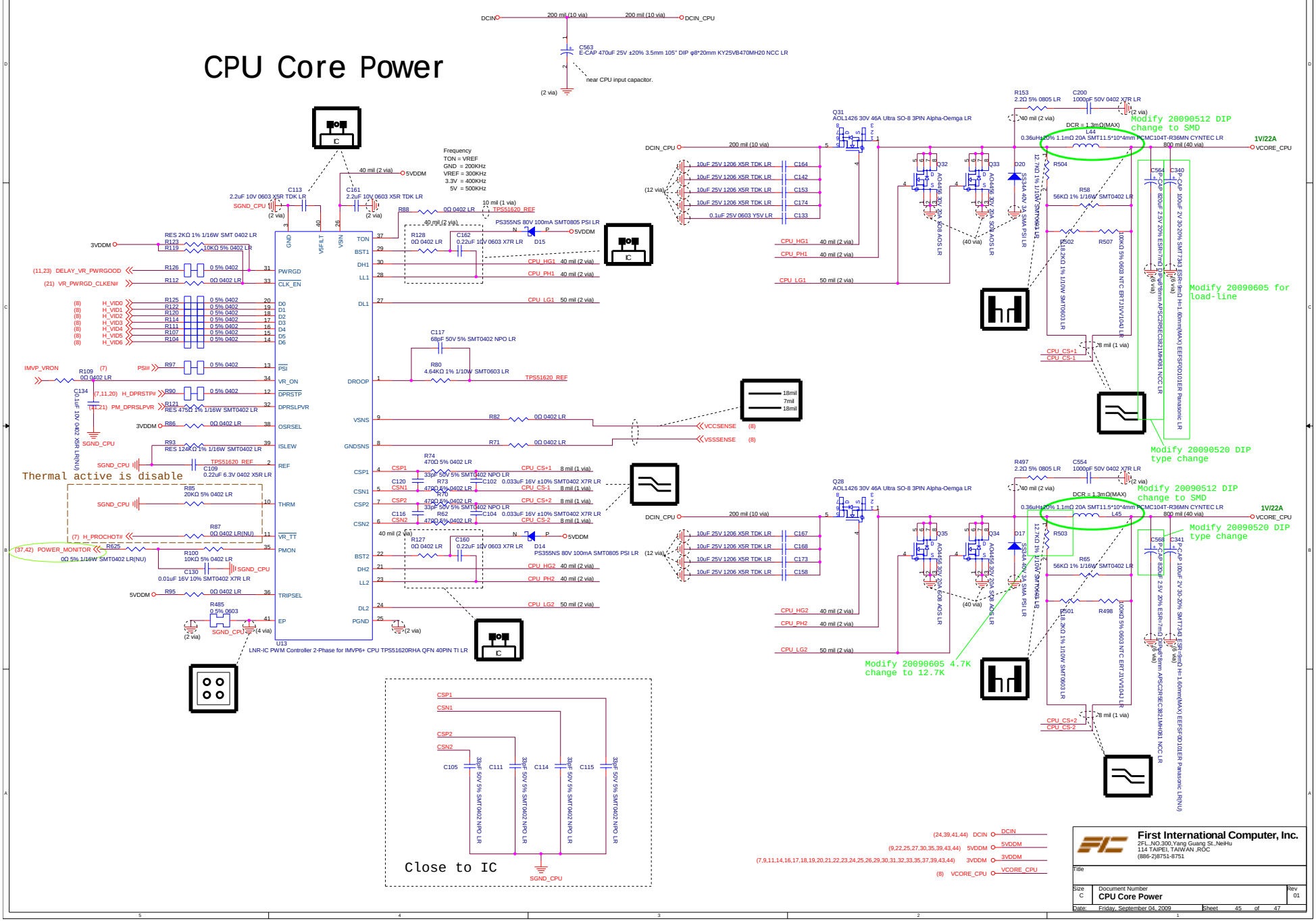
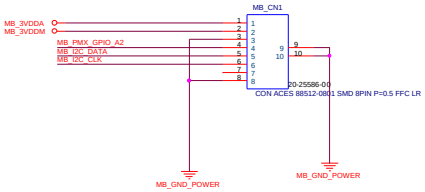
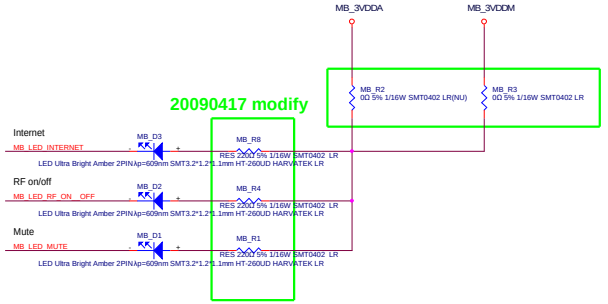
CPU Core Power

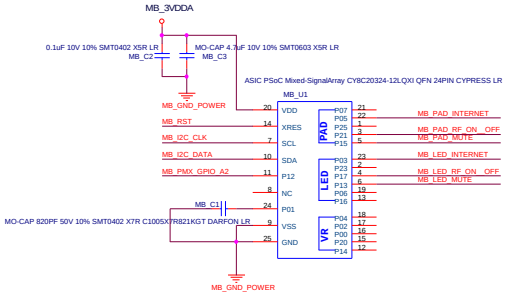


檔

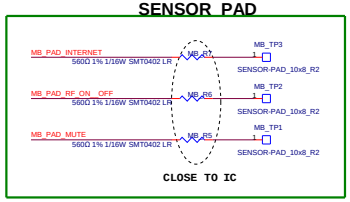
MMB Board con







SENSOR_PAD



左 TP1--TP2--TP3 右

trace:spacing=7:7
Button-GND spacing 0.5mm
Button-Button spacing 10mm
PAD Diameter 8~10mm ,rotundity or sq uareness
SMBUS trace and data can't pa rallel
GND plane Partial GND fill 60%

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For MDC modem

U_CN1
CON ACES 85204-02001 WIRE DIP 2PIN P=1.25 LR
20-20294-20

U_L3 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR
U_L4 600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TAI-TECH LR

U_CN3
CON ALLTOP C10140-102A4-L SMD RJ11 2 PIN H=8.6 LR
20-25681-00

U_M1
SCREW-P6_0D2_8V8

NOTE
USB WIDTH 5MILS,
SPACING 7MILS,
請包GROUND

U_5VDDS_USB
60mil
U_USB20_P0N
U_USB20_P0P
U_L1
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR(NU)
U_CN4
CON Alltop DIP 4PIN REV C107A6-10403-L P=0.2 USB LR
20-25179-00
U_C5 0.1uF 16V 80-20% 0402 Y5V LR
U_D2
U_D1
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR
For ESD.So,Please
close to USB CNN

U_CN2
CON WEFER-M GOLD FLASH SMT H=1.95mm 1ROW 12PIN 1.25mm 90 ° 88266-12001-06 ACES LR
20-25851-01
U_USB20_P1P
U_USB20_P1N
U_LID#
U_3VDDA
U_USB20_P0P
U_USB20_P0N

U_5VDDS_USB
80mil
U_L5
HCB2012KF-121T30 TAI-TECH LR
U_F1
POLY-SWITCH 1.5A 8V SMT1812 SMD1812P150TF/8 PTTC LR
80mil
U_C2 E-CAP 100uF 16V 20% 105° SMT6.3*5.2mm 100HRS EMVY160ADA101MF55G NCC LR
U_C3 0.1uF 16V 80-20% 0402 Y5V LR
0.1uF 16V 80-20% SMT0603 Y5V LR(NU)
U_C4

NOTE
USB WIDTH 5MILS,
SPACING 7MILS,
請包GROUND

U_5VDDS_USB
60mil
U_USB20_P1N
U_USB20_P1P
U_L2
CHOKE 120Ω 100MHz 0.22Ω 0.37A ACM2012-121-2P-T TDK LR(NU)
U_CN5
CON Alltop DIP 4PIN REV C107A6-10403-L P=0.2 USB LR
20-25179-00
U_C1 0.1uF 16V 80-20% 0402 Y5V LR
U_D4
U_D3
ESD 3.5pF ±10% 15KV DC=12V SMT0603 MLVS-0603-E10 INPAQ LR
For ESD.So,Please
close to USB CNN

LID Switch

U_3VDDA
U_R1 100KΩ 5% 1/16W SMT0402 LR
TO PMX
U_LID#
U_C6 100pF 50V 5% SMT0402 NPO LR
U_D5
LNR-IC HALL-EFFECT SWITCH EC2648-BL-F 2.7-3.3V SOT-23 3PIN E-CMOS LR
VDD
OUT
GND
U_C7 0.1uF 10V 10% SMT0402 X5R LR
U_GND_POWER

U_M2
SCREW-P8_0D2_8V8

U_FM3 CFMASK
U_FM4 CFMASK
U_FM2 CFMASK
U_FM1 CFMASK

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