UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled
UMA:UMA platform installed
OPS:Optimus
CR:Chief River
V: V-Series installed

<Variant Name>

緯創資通 Wistron Corporation
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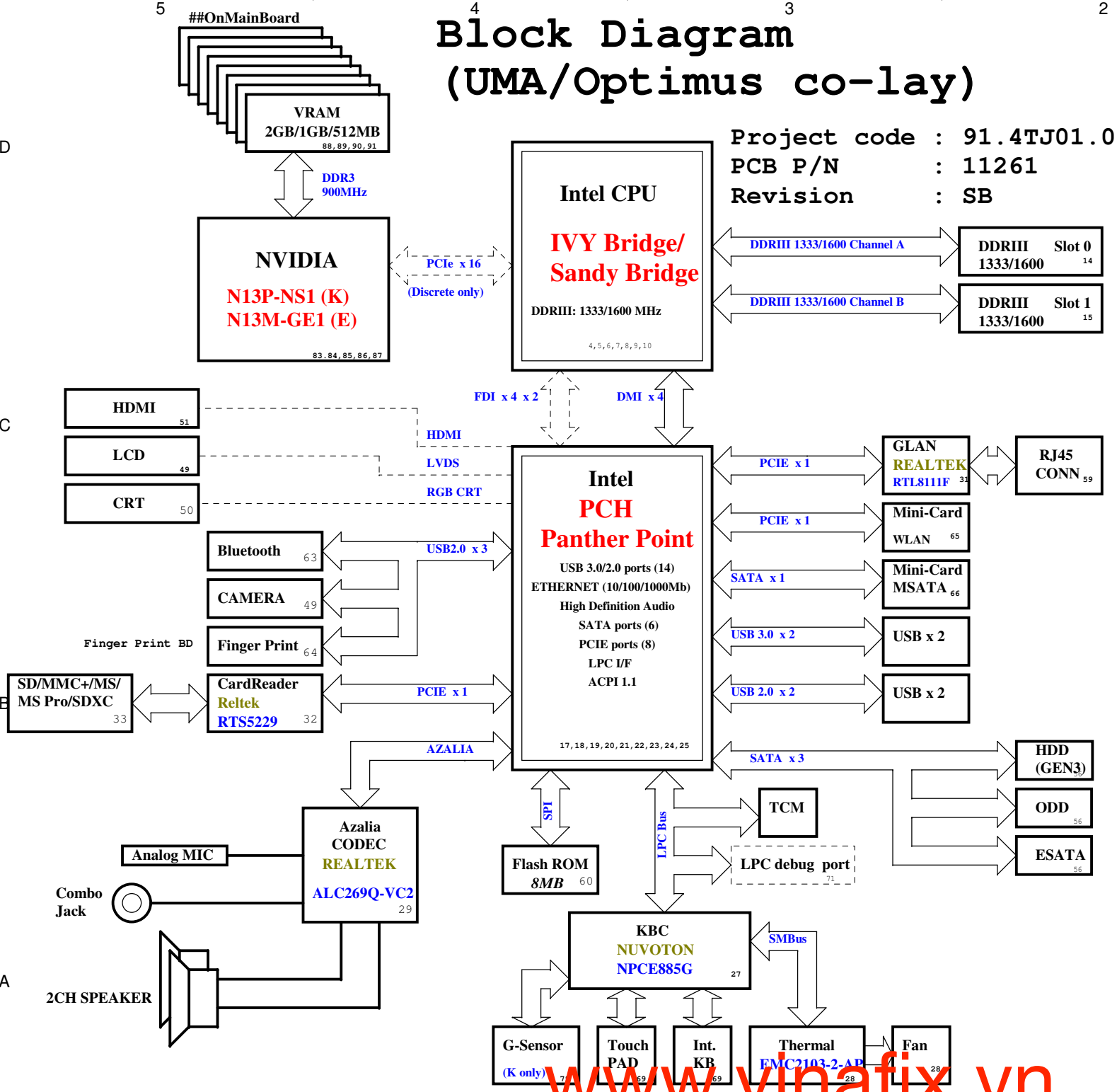
Block Diagram (UMA/Optimus co-lay)

Project code : 91.4TJ01.001
PCB P/N : 11261
Revision : SB



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA

CPU DC/DC TPS51640 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

INPUTS	OUTPUTS

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
AD_JK	BT+

SYSTEM DC/DC RT9018B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

INPUTS	OUTPUTS

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:GND
L2:VCC	L6:Bottom
L3:Signal	
L4:Signal	

<Variant Name>

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PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor TBNI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

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Title: Table of Content

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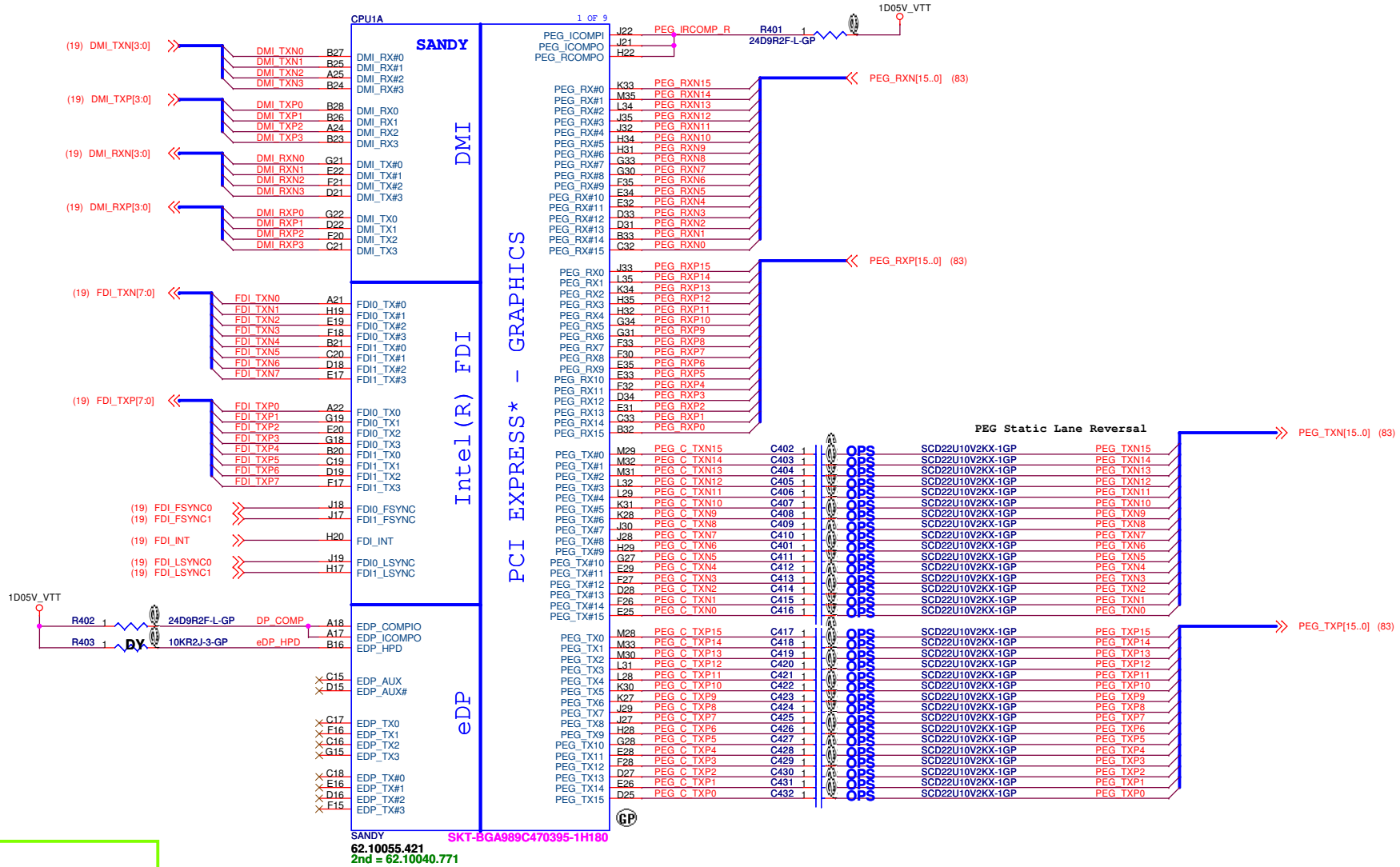
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

<Variant Name>

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Title: CPU (PCIE/DMI/FDI)
Size: A3 | Document Number: LLP-1 | Rev: SA
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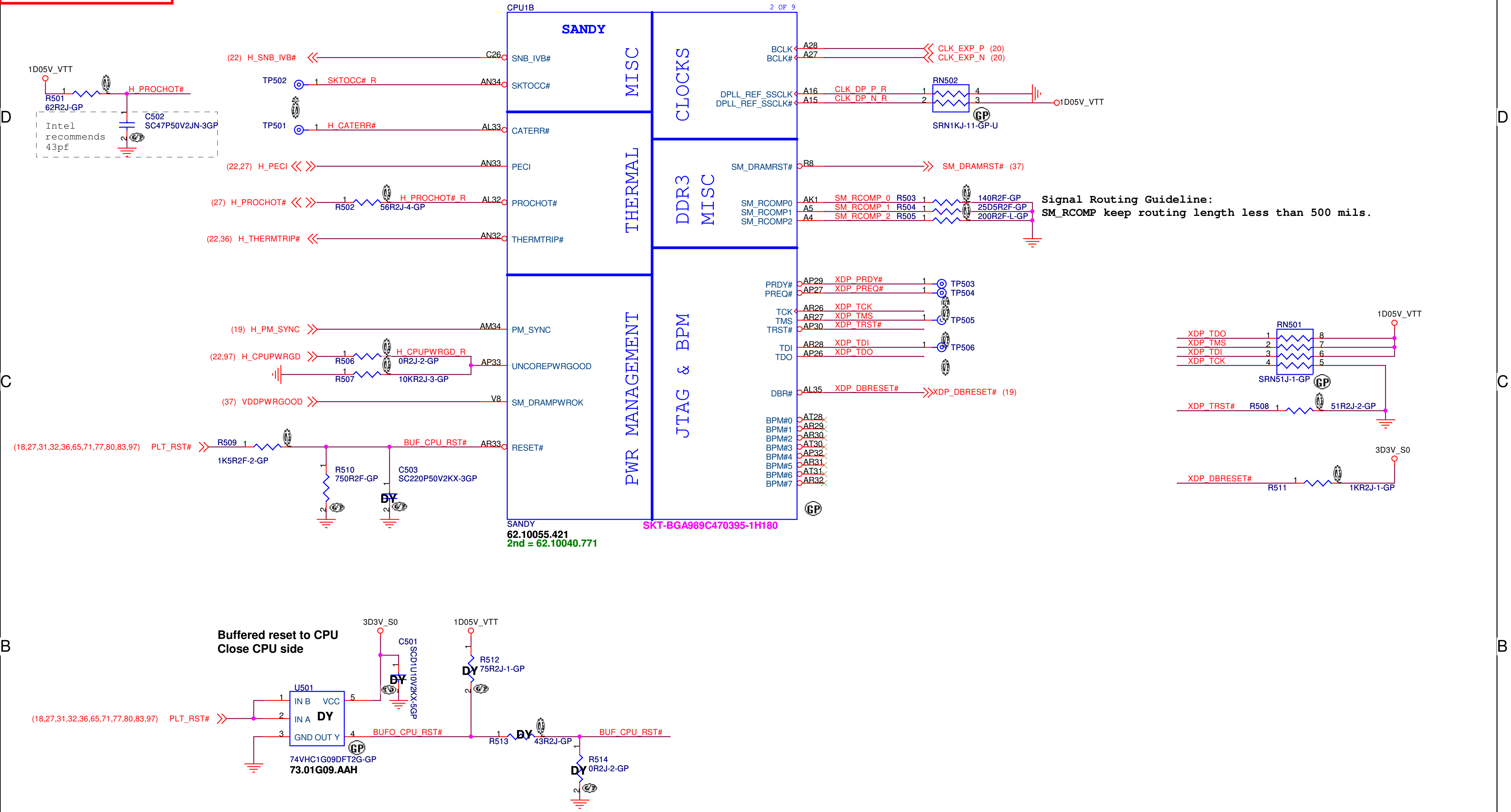
SSID = CPU



CPU1B
2 OF 9
SANDY
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#0
BPM#1
BPM#2
BPM#3
BPM#4
BPM#5
BPM#6
BPM#7
(22) H_SNB_IVB#
(22,27) H_PECI
(27) H_PROCHOT#
(22,36) H_THERMTRIP#
(19) H_PM_SYNC
(22,97) H_CPUPWRGD
(37) VDDPWRGOOD
(18,27,31,32,36,65,71,77,80,83,97) PLT_RST#
1D05V_VTT
R501
62R2J-GP
H_PROCHOT#
C502
SC47P50V2JN-3GP
Intel recommends 43pf
TP502
SKTOCC#_R
TP501
H_CATERR#
R502
56R2J-4-GP
H_PROCHOT#_R
R506
0R2J-2-GP
H_CPUPWRGD_R
R507
10KR2J-3-GP
R509
1K5R2F-2-GP
BUF_CPU_RST#
R510
750R2F-GP
C503
SC220P50V2KX-3GP
DY
CLK_EXP_P (20)
CLK_EXP_N (20)
CLK_DP_P_R
CLK_DP_N_R
RN502
SRN1KJ-11-GP-U
SM_DRAMRST# (37)
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
R503
R504
R505
140R2F-GP
25D5R2F-GP
200R2F-L-GP
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
XDP_PRDY#
XDP_PREQ#
XDP_TCK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
TP503
TP504
TP505
TP506
XDP_DBRESET#
XDP_DBRESET# (19)
SANDY
62.10055.421
2nd = 62.10040.771
SKT-BGA989C470395-1H180
RN501
SRN51J-1-GP
R508
51R2J-2-GP
3D3V_S0
R511
1KR2J-1-GP
Buffered reset to CPU
Close CPU side
C501
SCD1U10V2KX-5GP
R512
75R2J-1-GP
U501
IN B
IN A
GND
VCC
OUT Y
74VHC1G09DFT2G-GP
73.01G09.AAH
BUFO_CPU_RST#
R513
43R2J-GP
R514
0R2J-2-GP

<Variant Name>

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Title	CPU (THERMAL/CLOCK/PM)
Size	A3
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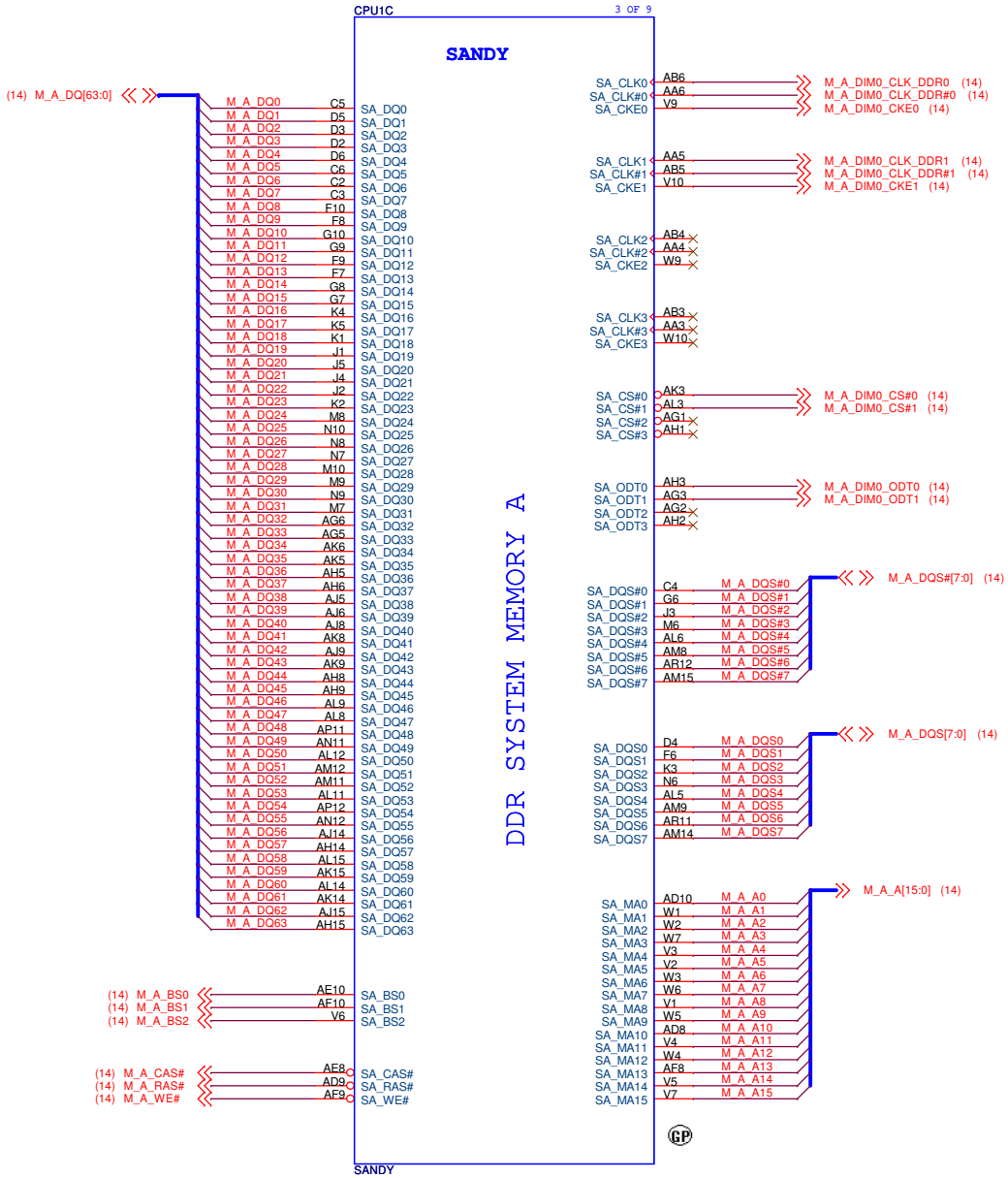
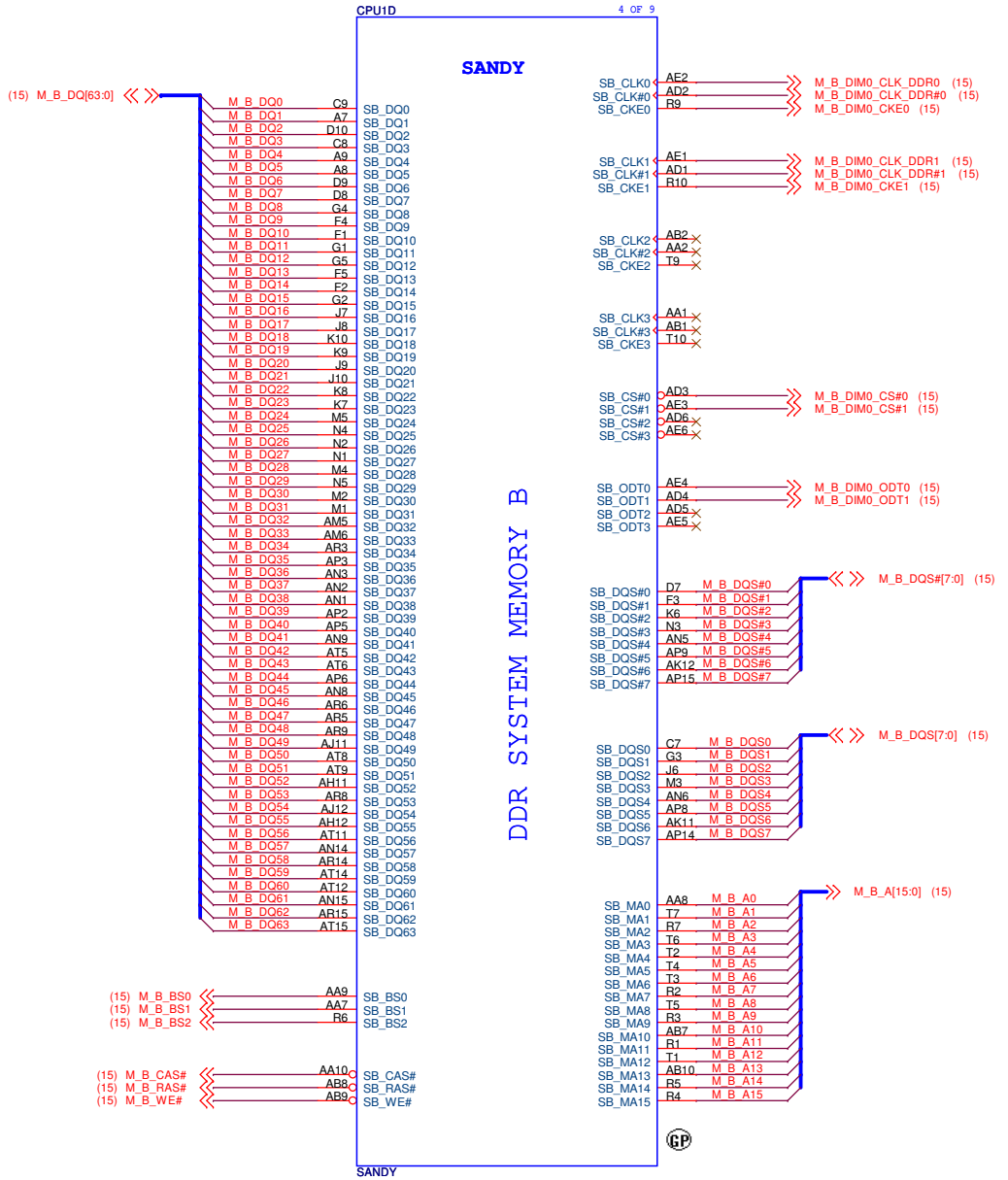
SSID = CPU





<Variant Name>

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Title: CPU (DDR)

Size	Document Number	Rev
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SSID = CPU

CFG2 — R702 1KR2J-1-GP — QPS

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4 — R703 1KR2J-1-GP — DY

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG0 — R706 1KR2J-1-GP — DY

CFG5 — R704 1KR2J-1-GP — DY

CFG6 — R705 1KR2J-1-GP — DY

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

CFG7 — R701 1KR2J-1-GP — DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU1E — 5 OF 9 — SANDY — RESERVED

TP702	CFG0	AK28	CFG0		
	CFG1	AK29	CFG1		
	CFG2	AL26	CFG2		
TP704	CFG3	AL27	CFG3		
	CFG4	AK26	CFG4		
	CFG5	AL29	CFG5		
	CFG6	AL30	CFG6		
	CFG7	AM31	CFG7		
		AM32	CFG8		
		AM30	CFG9		
		AM28	CFG10		
		AM26	CFG11		
		AN28	CFG12		
		AN31	CFG13		
		AN26	CFG14		
		AM27	CFG15		
TP705	CFG16	AK31	CFG16		
		AN29	CFG17		
		AJ31	RSVD#AJ31		
		AH31	RSVD#AH31		
		AJ33	RSVD#AJ33		
		AH33	RSVD#AH33		
		AJ26	RSVD#AJ26		
(12) DDR_WR_VREF01		B4	RSVD#B4		
(12) DDR_WR_VREF02		D1	RSVD#D1		
		F25	RSVD#F25		
		F24	RSVD#F24		
		F23	RSVD#F23		
		D24	RSVD#D24		
		G25	RSVD#G25		
		G24	RSVD#G24		
		F23	RSVD#E23		
		D23	RSVD#D23		
		C30	RSVD#C30		
		A31	RSVD#A31		
		B30	RSVD#B30		
		B29	RSVD#B29		
		D30	RSVD#D30		
		B31	RSVD#B31		
		A30	RSVD#A30		
		C29	RSVD#C29		
		J20	RSVD#J20		
TP708	H_VCCP_SEL	B18	RSVD#B18		
		A19	RSVD#A19		
		J15	RSVD#J15		
				RSVD#L7	L7
				RSVD#AG7	AG7
				RSVD#AE7	AE7
				RSVD#AK2	AK2
				RSVD#W8	W8
				RSVD#AT26	AT26
				RSVD#AM33	AM33
				RSVD#AJ27	AJ27
				RSVD#T8	T8
				RSVD#J16	J16
				RSVD#H16	H16
				RSVD#G16	G16
				RSVD#AR35	AR35
				RSVD#AT34	AT34
				RSVD#AT33	AT33
				RSVD#AP35	AP35
				RSVD#AR34	AR34
				RSVD#B34	B34
				RSVD#A33	A33
				RSVD#A34	A34
				RSVD#B35	B35
				RSVD#C35	C35
				RSVD#AJ32	AJ32
				RSVD#AK32	AK32
				RSVD#AH27	AH27 — TP705 — TP706
				RSVD#AN35	AN35 — TP706 — TP701
				RSVD#AM35	AM35 — TP707 — TP707
				RSVD#AT2	AT2
				RSVD#AT1	AT1
				RSVD#AR1	AR1

SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

<Variant Name>

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POWER

VCC CORE:53A

VCCIO:8.5A

CPU1F

SANDY

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PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC_CORE

1D05V_VTT

C802 C820 C803 C804 C805 C821 C816 C817 C818 C819 C822 C823 C824 C825 C826 C827 C828 C829 C838 C839 C840 C841 C842 C843 C844 C845 C806 C807 C808 C809 C810 C811 C812 C813 C814 C815 C830 C831 C832 C833 C834 C835 C801 C836 C837

SC10U6D3V5KX-1GP

DY

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

R810 130R2F-1-GP

R802 75R2F-2-GP

R803 43R2J-GP

VIDALERT# AJ29 H_CPU_SVIDALRT#

VIDSCLK AJ30 H_CPU_SVIDCLK

VIDSOUT AJ28 H_CPU_SVIDDAT

VR_SVID_ALERT# (42)

H_CPU_SVIDCLK (42)

H_CPU_SVIDDAT (42)

R804 10R2F-L-GP

R805 100R2F-L1-GP-U

R806 10R2F-L-GP

R807 100R2F-L1-GP-U

VCCIO_SENSE

VSSIO_SENSE

VCC_SENSE AJ35

VSS_SENSE AJ34

VCCSENSE (42)

VSSSENSE (42)

VCCIO_SENSE B10

VSSIO_SENSE A10

VCCIO_SENSE (45)

VSSIO_SENSE (45)

<Variant Name>

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Title: CPU (VCC_CORE)

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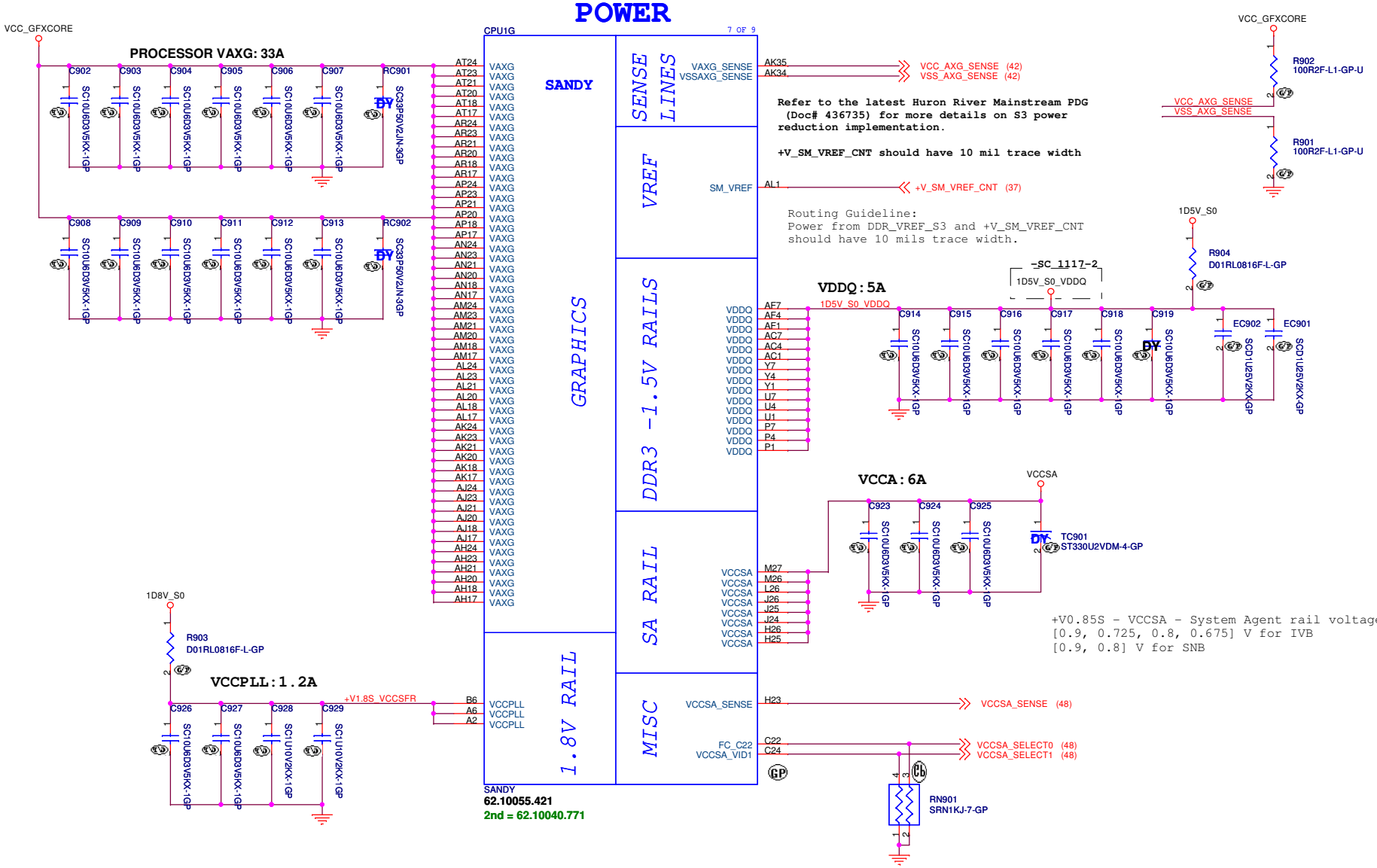
POWER



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Title: CPU (VCC_GFXCORE)

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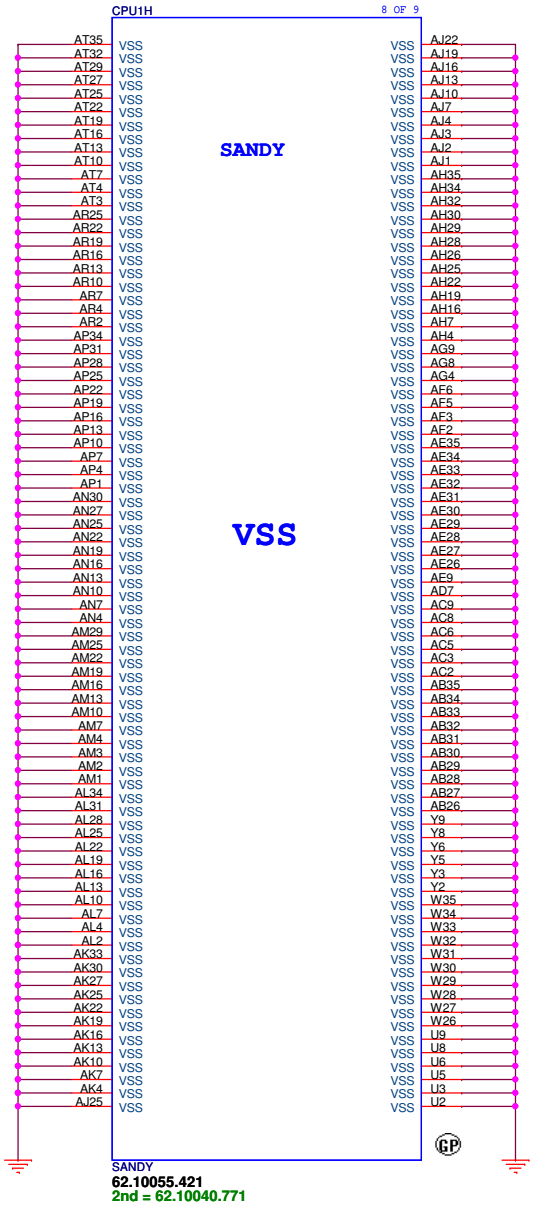
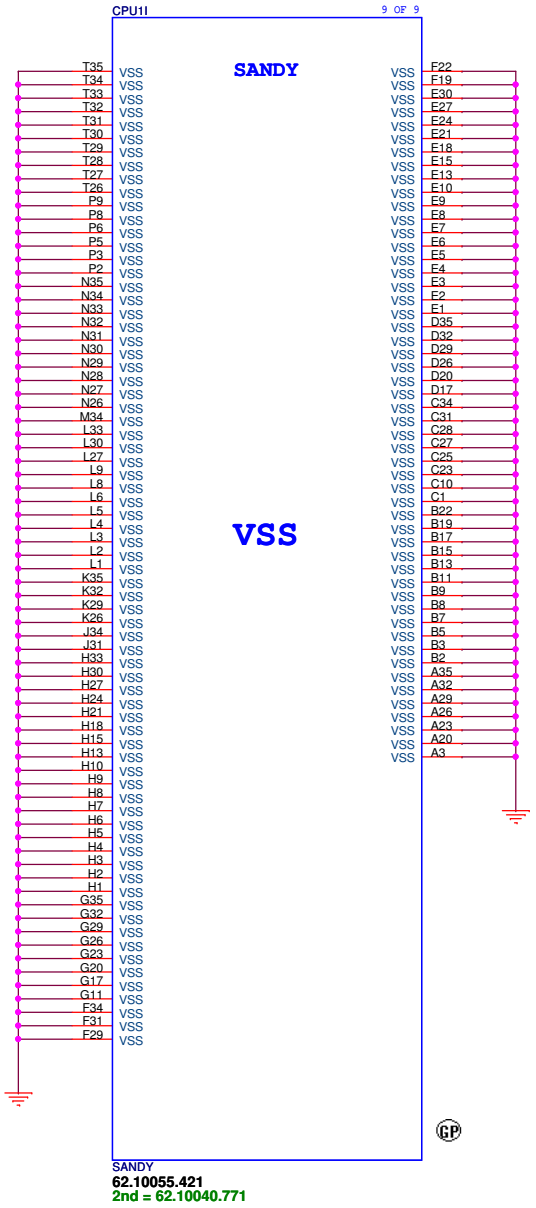
SSID = CPU





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緯創資通 Wistron Corporation
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Title: CPU (VSS)

Size	Document Number	Rev
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<Variant Name>

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Title: <Title>		
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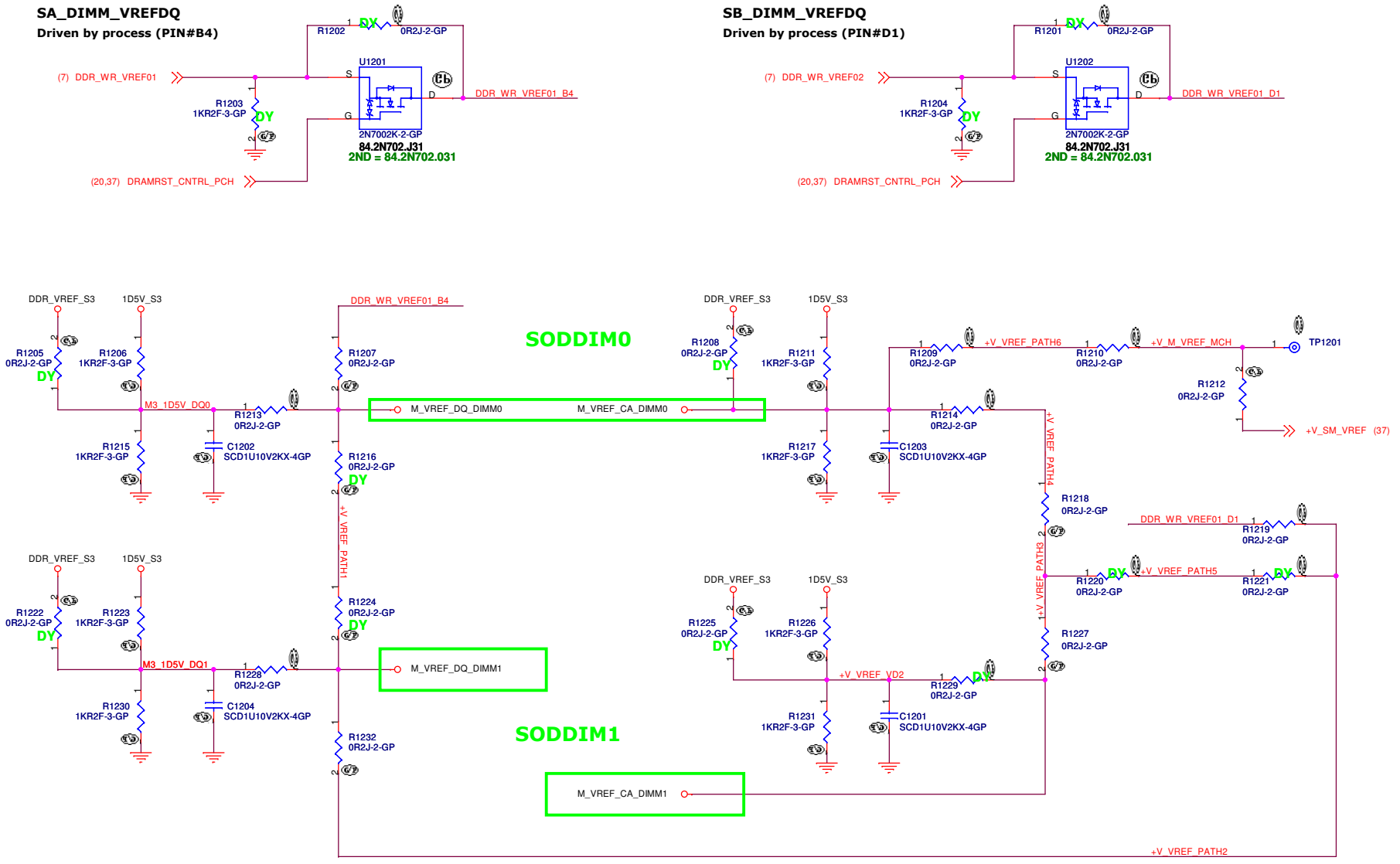
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry



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緯創資通 Wistron Corporation
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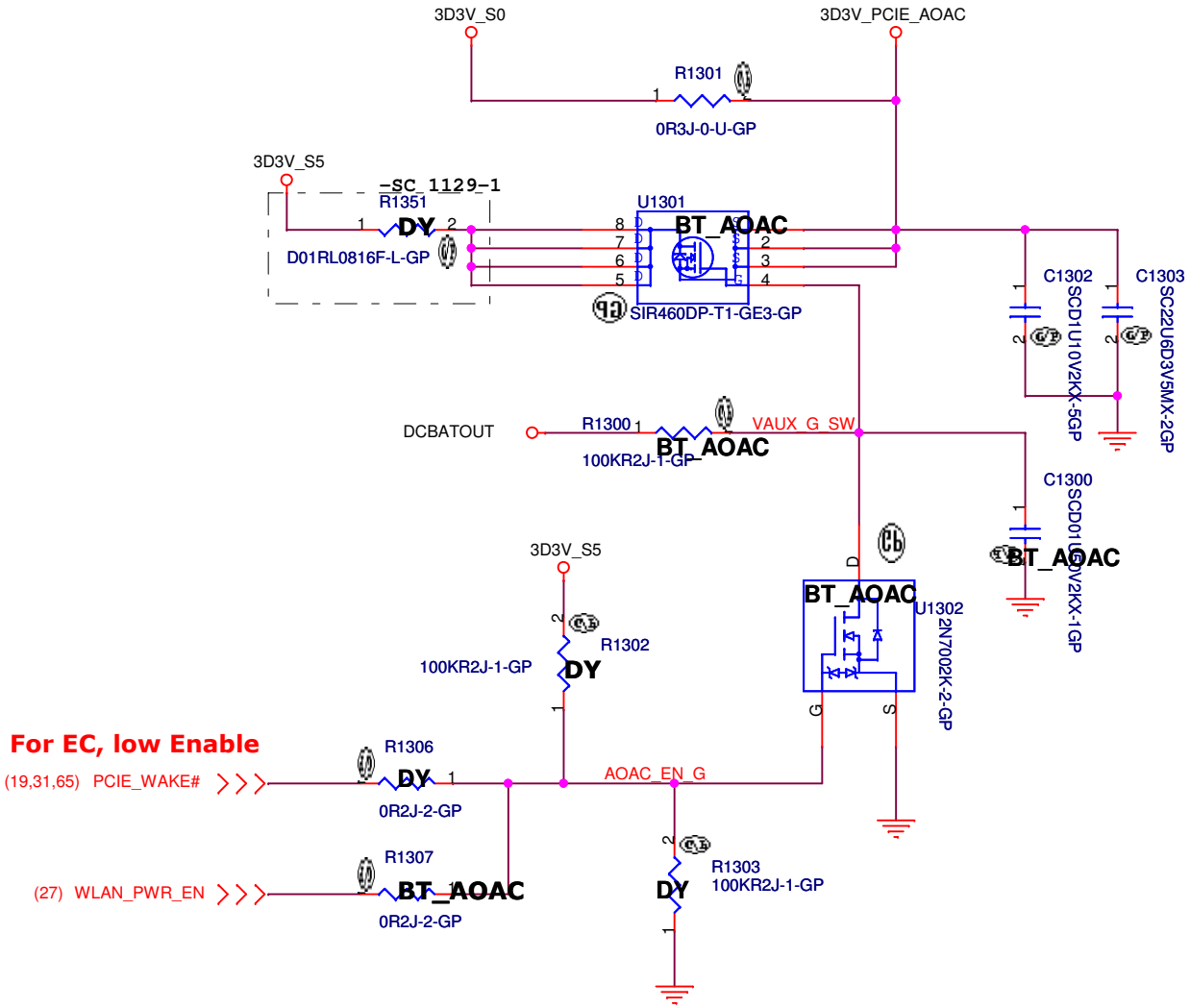
Taipei Hsien 221, Taiwan, R.O.C.

Title	M3	
Size A3	Document Number LLP-1	Rev SA
Date: Monday, December 05, 2011	Sheet 12 of 105	

3D3V_PCIE_AOAC tie to I/O board WLAN, WWAN

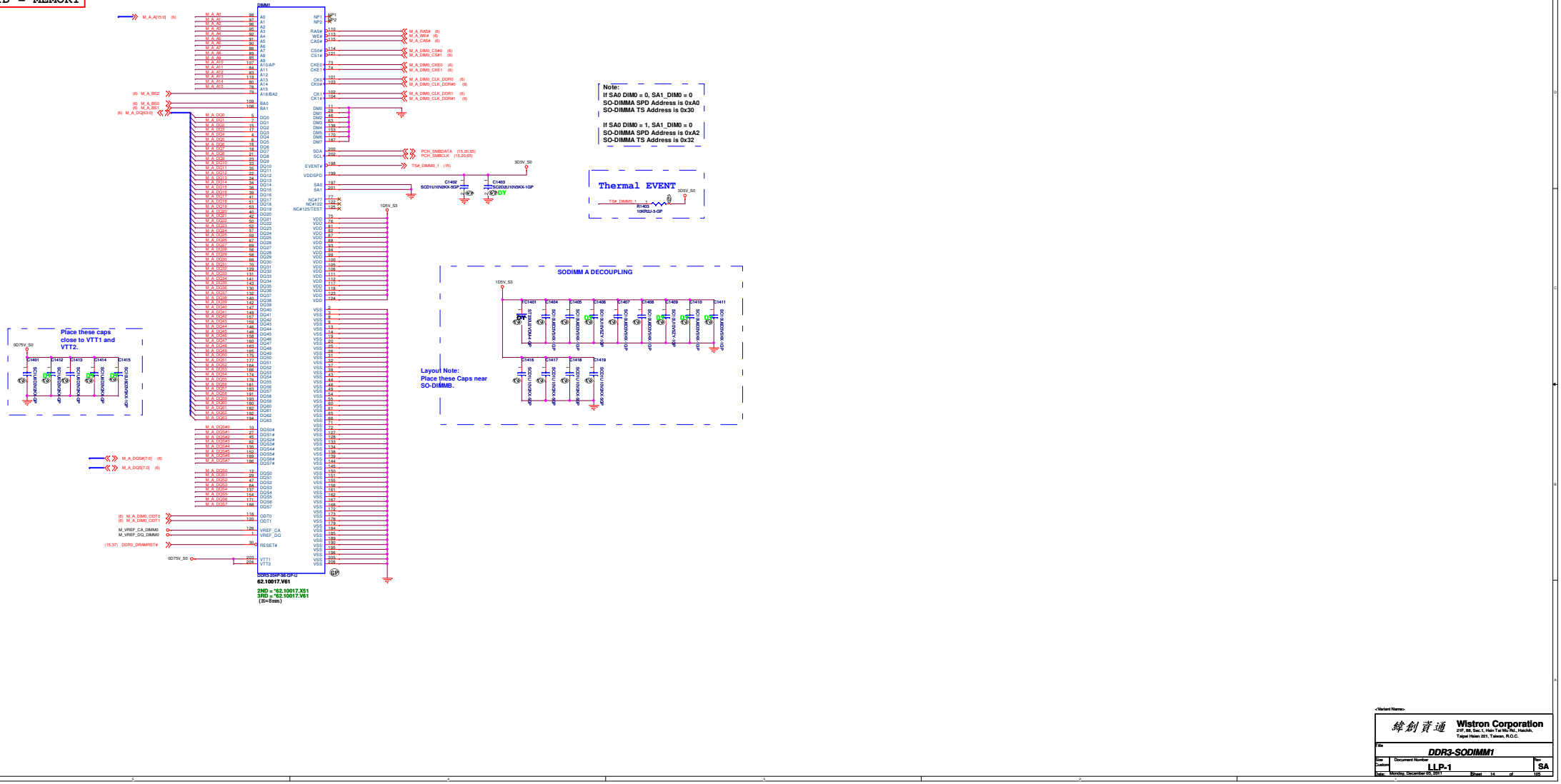


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**AOAC**	
Size A4	Document Number **LLP-1**	Rev **SA**
Date: Monday, December 05, 2011	Sheet 13 of 105	

SSID = MEMORY



<Variant Name>

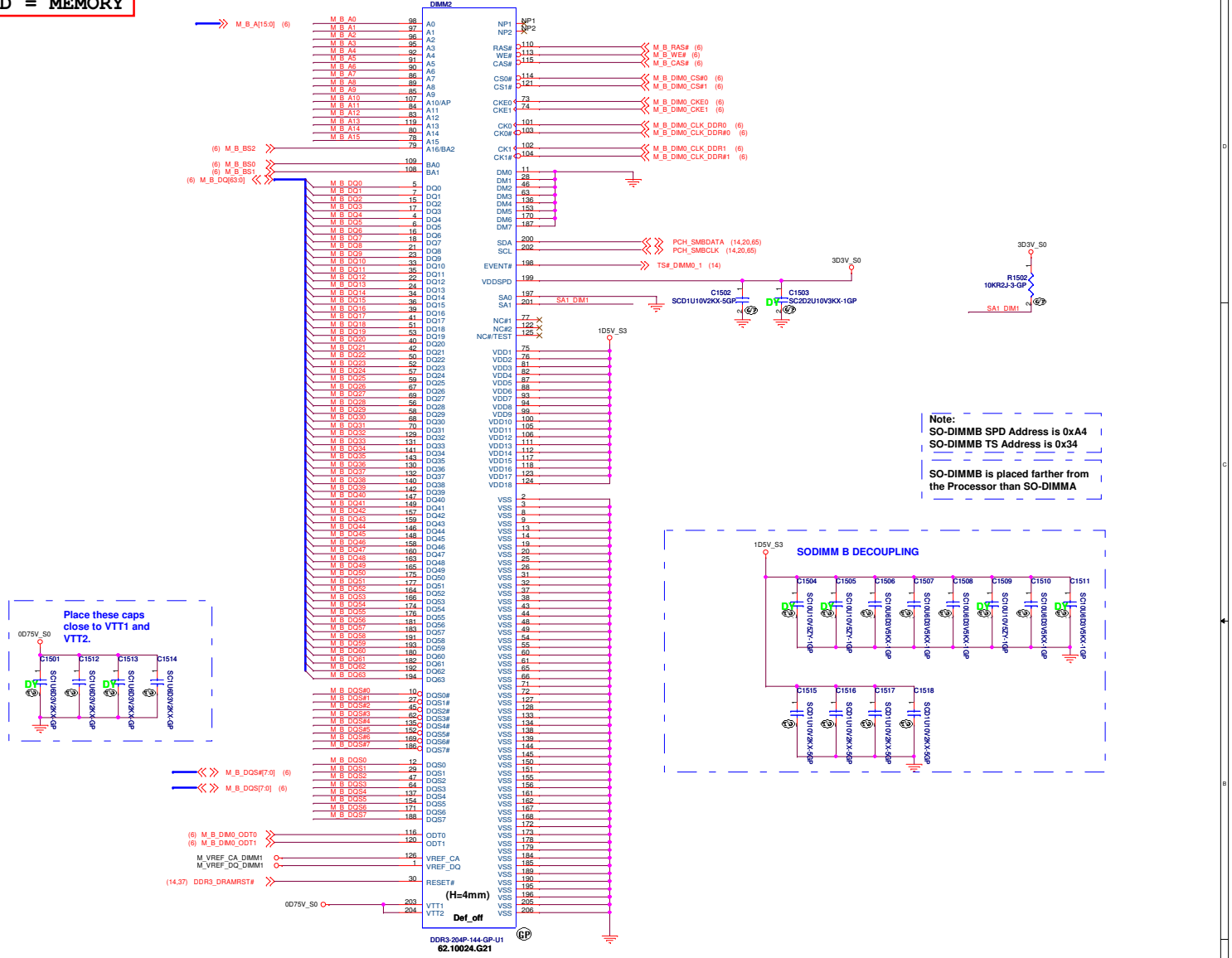
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: C-Custom | Document Number: LLP-1 | Rev: SA

Date: Monday, December 05, 2011 | Sheet 14 of 105

SSID = MEMORY



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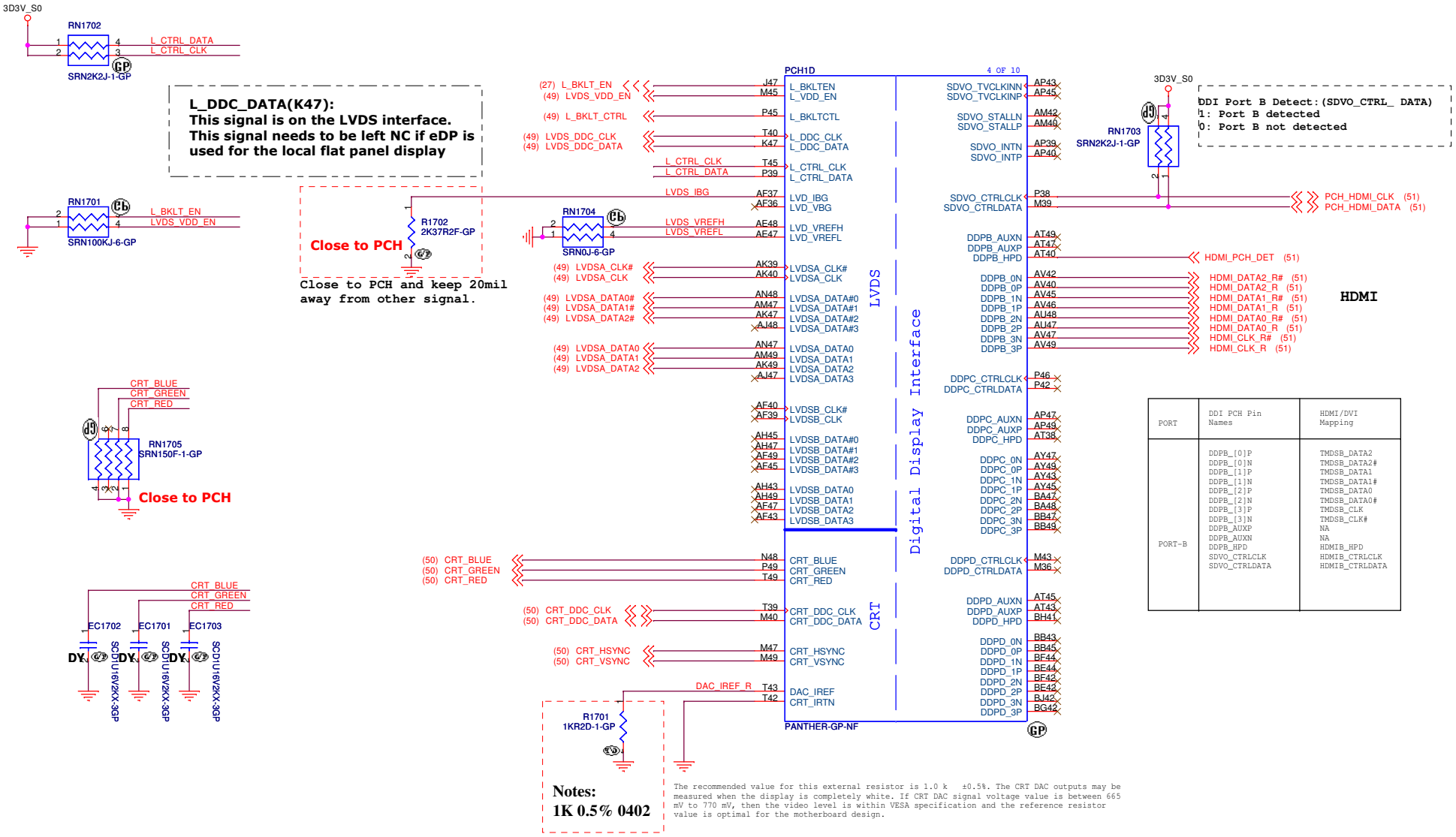
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 16 of 105



PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA
	DDPB_AUXN	NA
	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	HDMIB_CTRLCLK
	SDVO_CTRLDATA	HDMIB_CTRLDATA

<Variant Name>

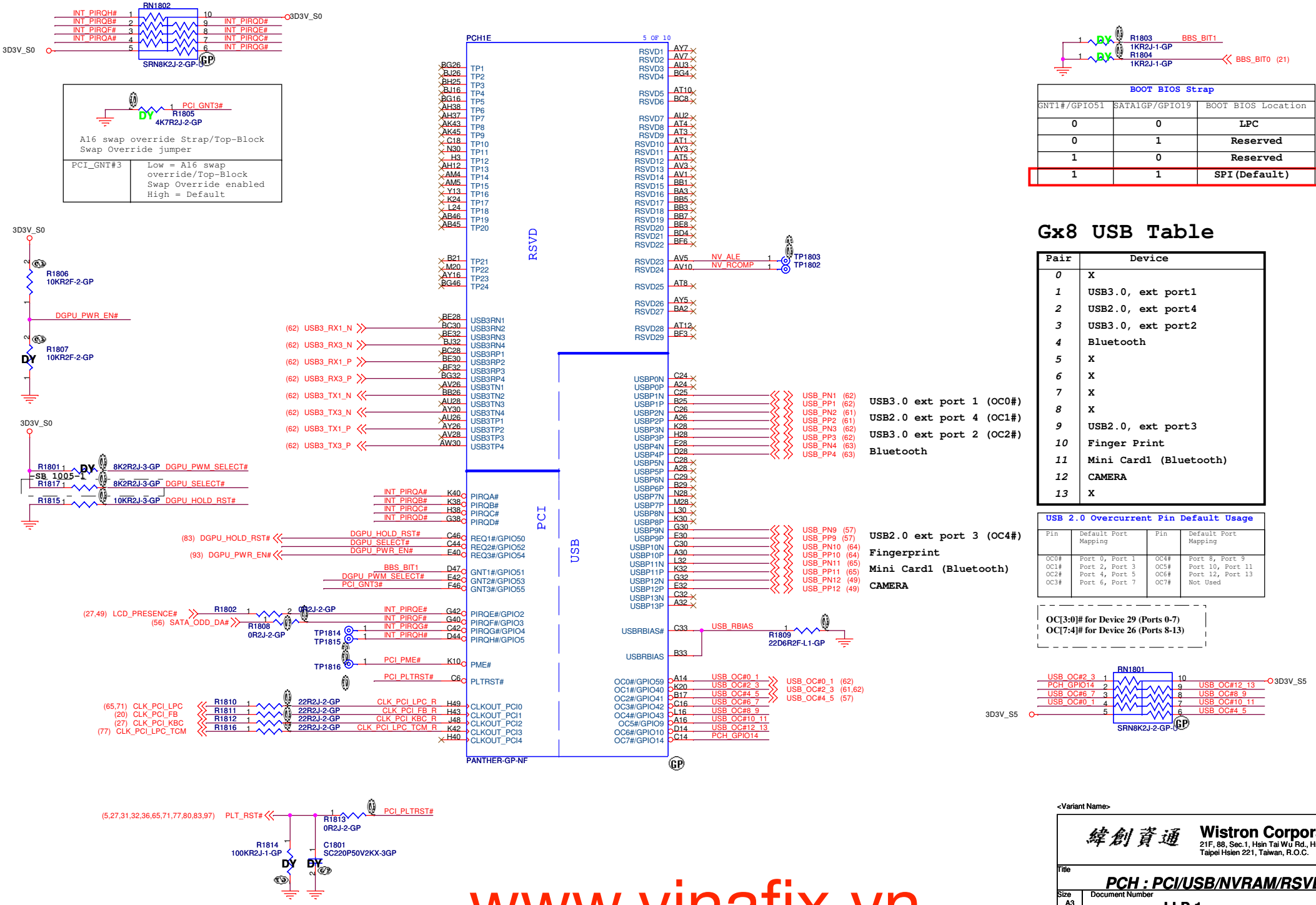
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : LVDS/CRT/DDI

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 17 of 105

SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	X
6	X
7	X
8	X
9	USB2.0, ext port3
10	Finger Print
11	Mini Card1 (Bluetooth)
12	CAMERA
13	X

USB3.0 ext port 1 (OC0#)
USB2.0 ext port 4 (OC1#)
USB3.0 ext port 2 (OC2#)
Bluetooth
USB2.0 ext port 3 (OC4#)
Fingerprint
Mini Card1 (Bluetooth)
CAMERA

USB 2.0 Overcurrent Pin Default Usage			
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

<Variant Name>

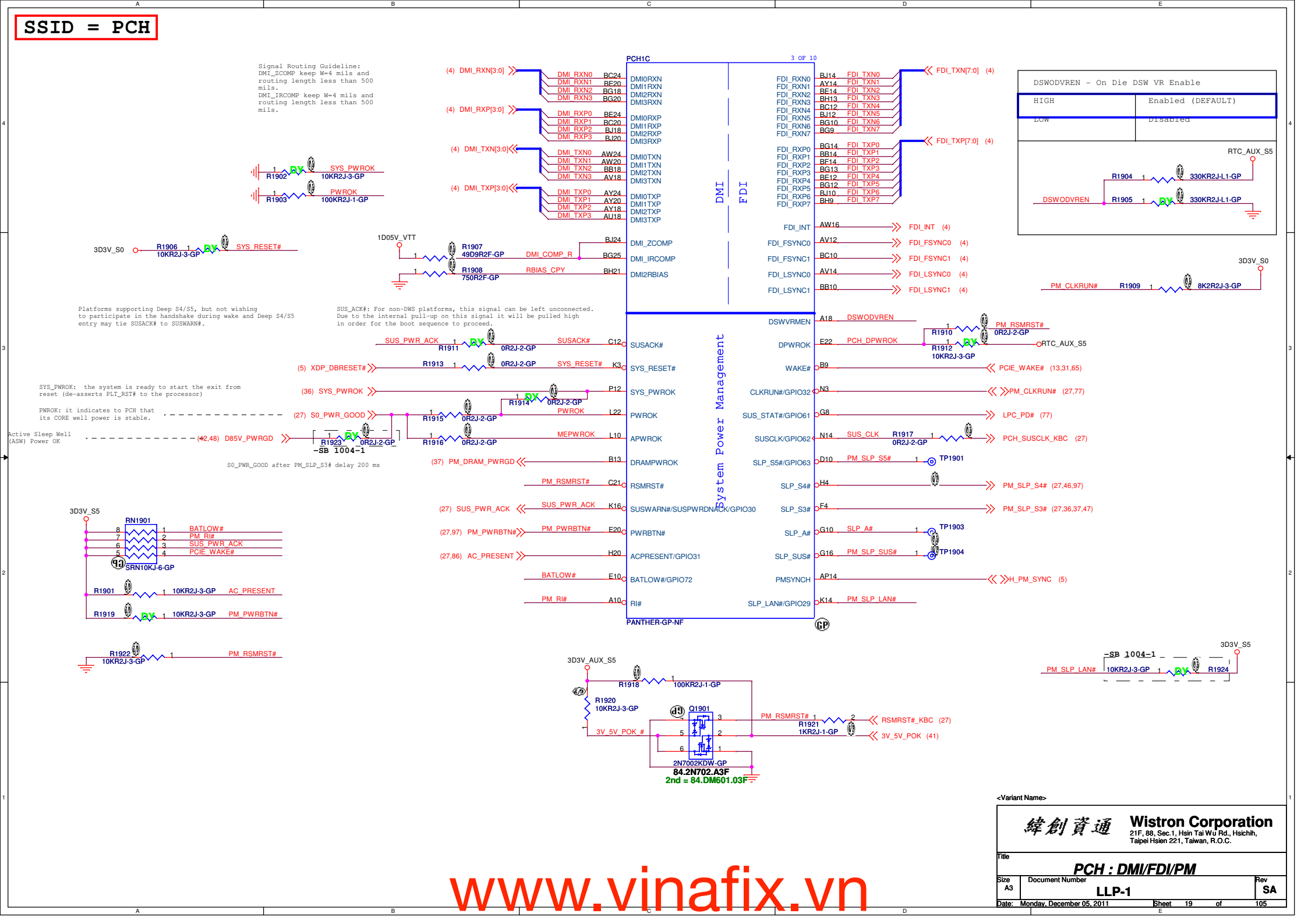
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : PCI/USB/NVRAM/RSVD

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 18 of 105

SSID = PCH



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : DMI/FDI/PM

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 19 of 105

SSID = PCH

If PCIE port 1 is disabled, it will cause all PCIE port disabled

PCH1B

WWAN

WLAN

Card Reader

LAN

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PANTHER-GP-NF

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

WLAN CLK

Card Reader CLK

LAN CLK

-SB 1013-3

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX Clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI_E looped be routed.

<Variant Name>

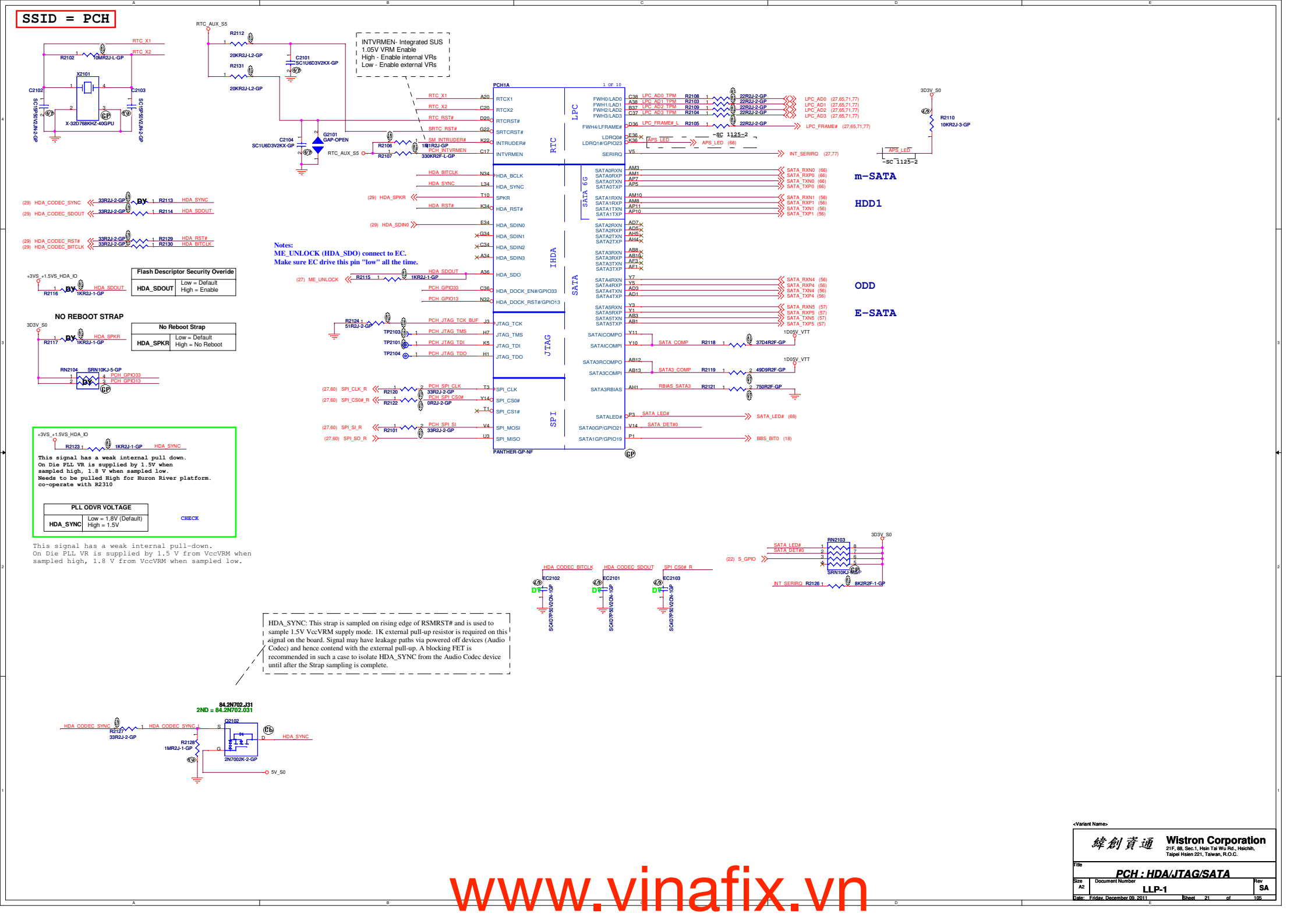
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : PCIE/SMBUS/CLK

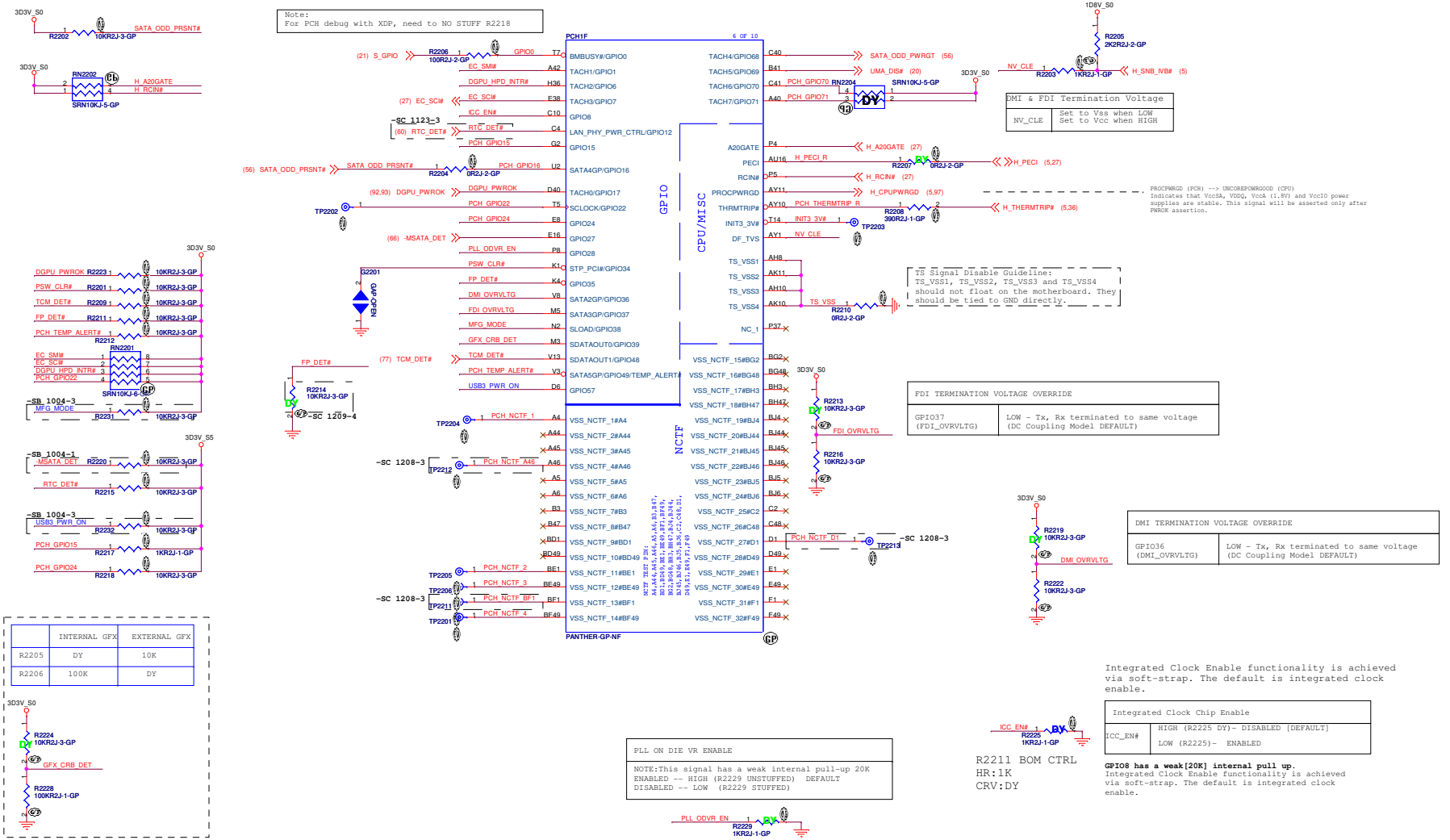
Size: A3 | Document Number: LLP-1 | Rev: SA

Date: Friday, December 09, 2011 | Sheet 20 of 105

SSID = PCH



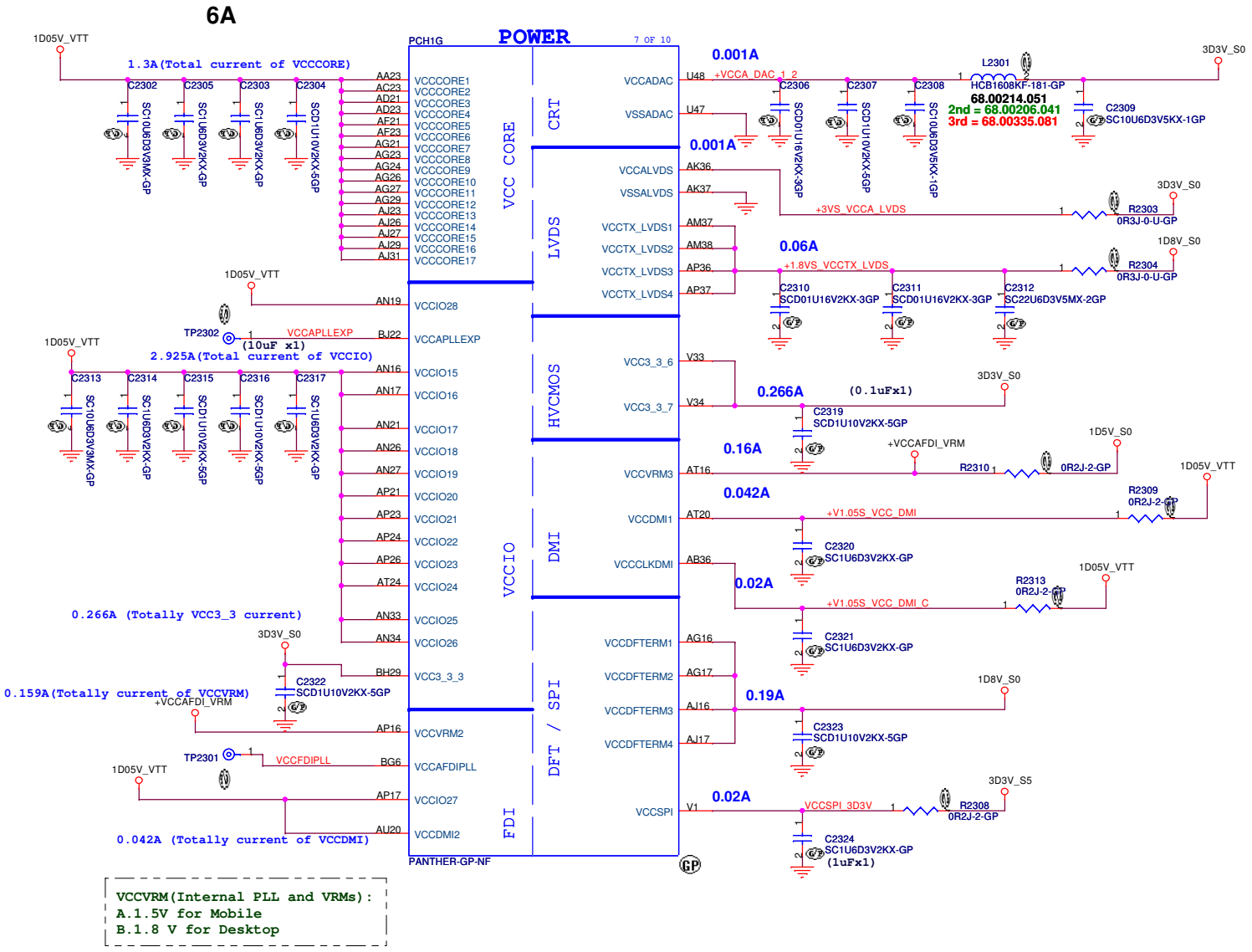
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: PCH : HDA/JTAG/SATA
Size: A2 | Document Number: LLP-1 | Rev: SA
Date: Friday, December 09, 2011 | Sheet 21 of 105



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : GPIO/NTCF/MISC
Size: A2 | Document Number: LLP-1 | Rev: SA
Date: Friday, December 09, 2011 | Sheet 22 of 105

SSID = PCH



<Variant Name>

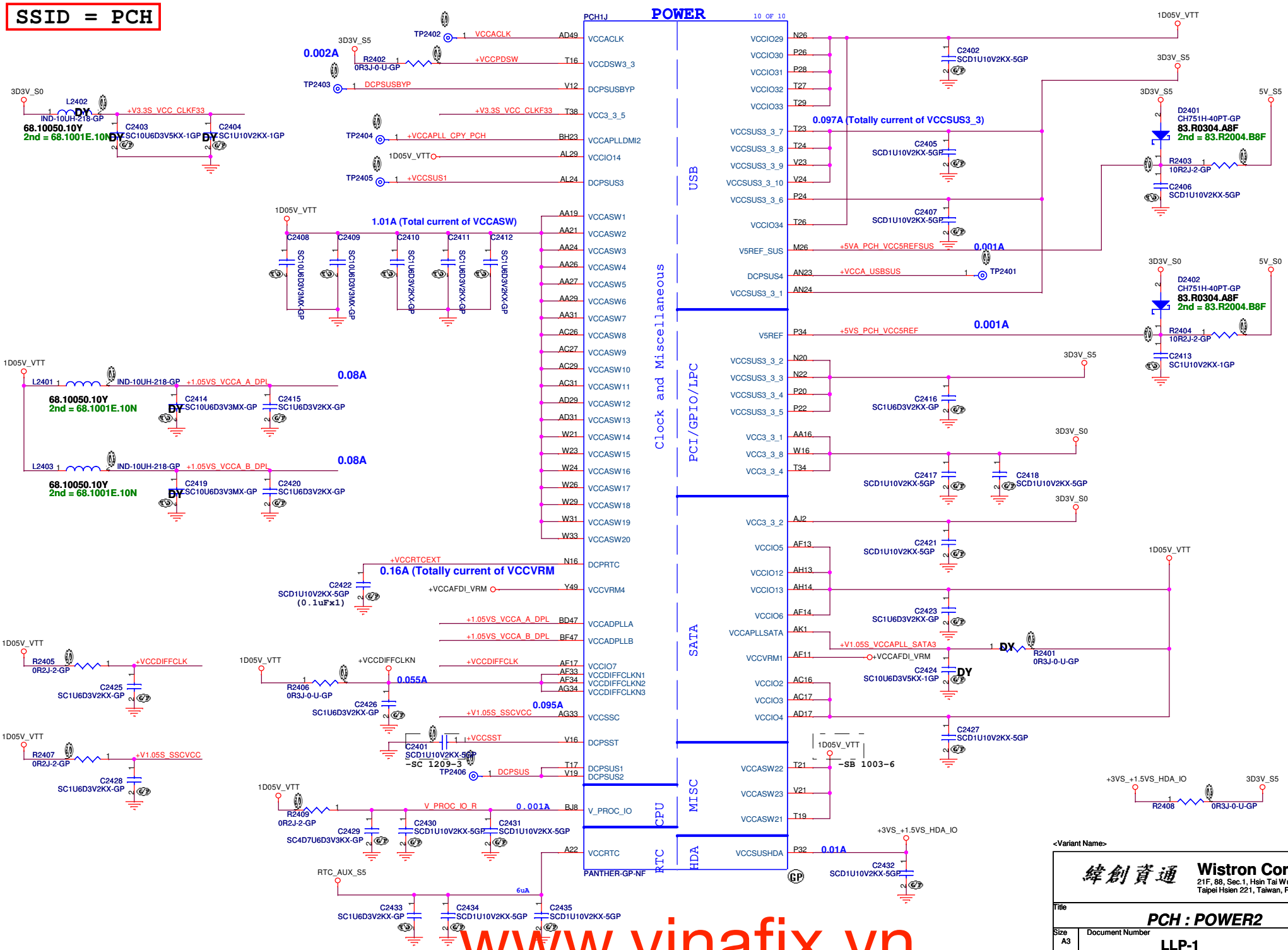
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : POWER1

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 23 of 105

SSID = PCH



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

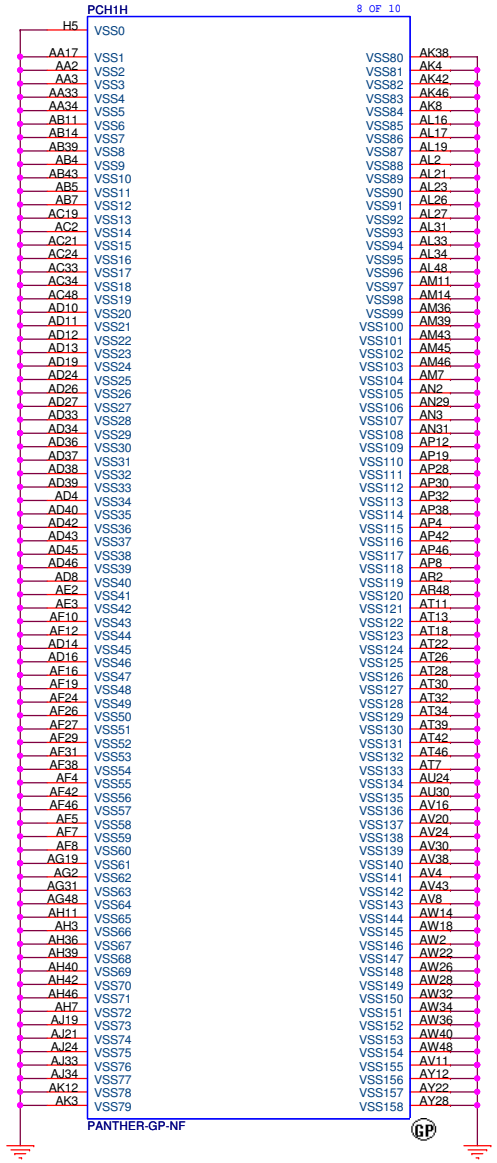
<Variant Name>

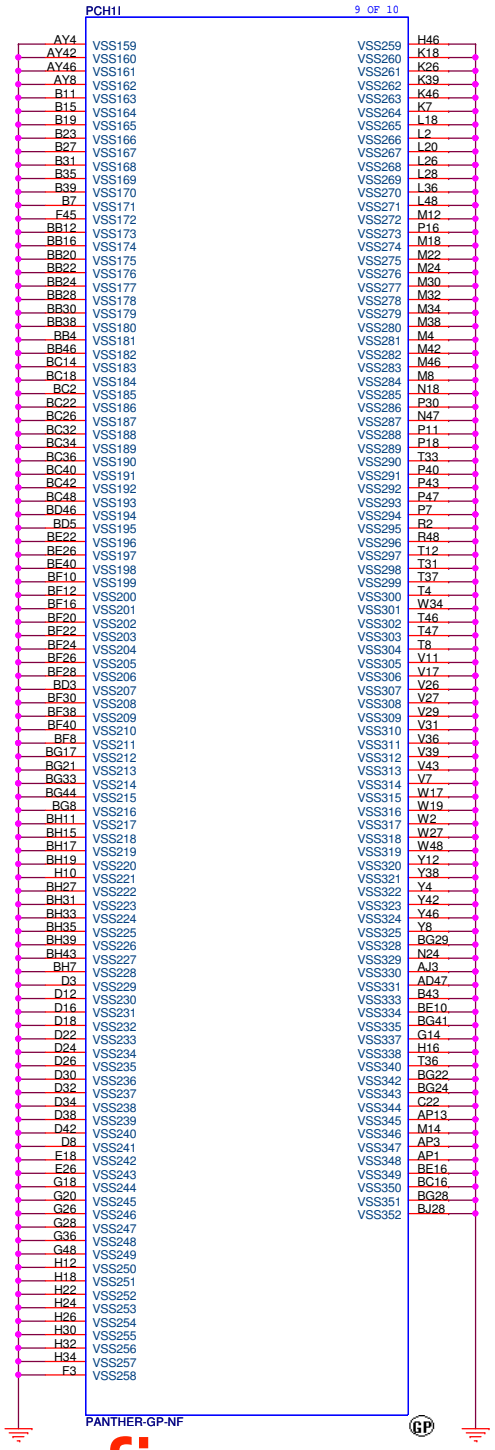
Title: PCH : POWER2

Size: A3 | Document Number: LLP-1 | Rev: SA

Date: Friday, December 09, 2011 | Sheet 24 of 105

SSID = PCH





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH : VSS

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 25 of 105

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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Date: Monday, December 05, 2011 Sheet 26 of 105

SSID = KBC

65W_90W#
High: 65W / Low 90W

For LED issue

For AD_OFF issue

EC_GPIO47 High Active

Reset IC: Prevent BIOS data loss solution

EC GPIO standard PH/PL

R2720 and C2716
Need very close to EC

MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA (LGN-1)	100.0K	10.0K	3.0V
UMA (LLP-1)	100.0K	20.0K	2.75V
OPTIMUS (LLP-1)	100.0K	33.0K	2.48V
UMA (LSS-1)	100.0K	47.0K	2.24V
OPTIMUS (LSS-1)	100.0K	64.9K	2.0V

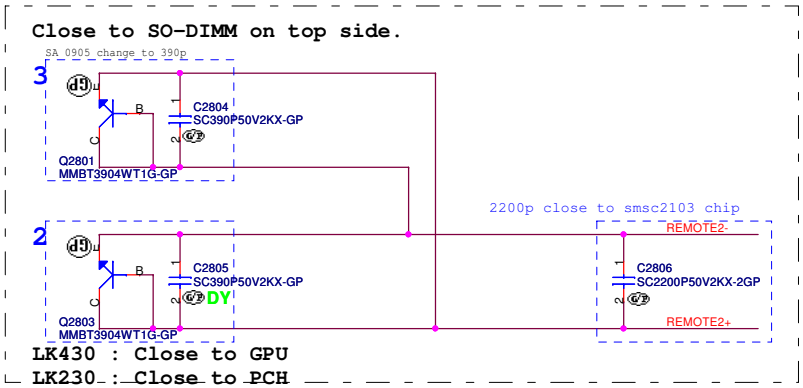
PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title: <Title>
Size: A1 Document Number: LLP-1 Rev: 5A
Date: Monday, December 05, 2011 Sheet 27 of 185

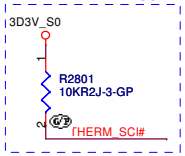
SSID = Thermal

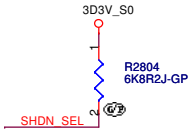
Thermal sensor



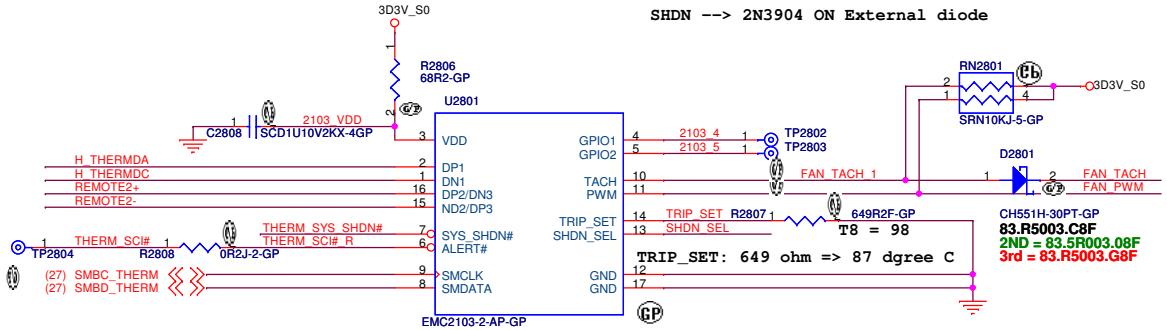
CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

20110718_Carrey:
For Vendor suggestion, add 10k pull high to 3D3V_S0



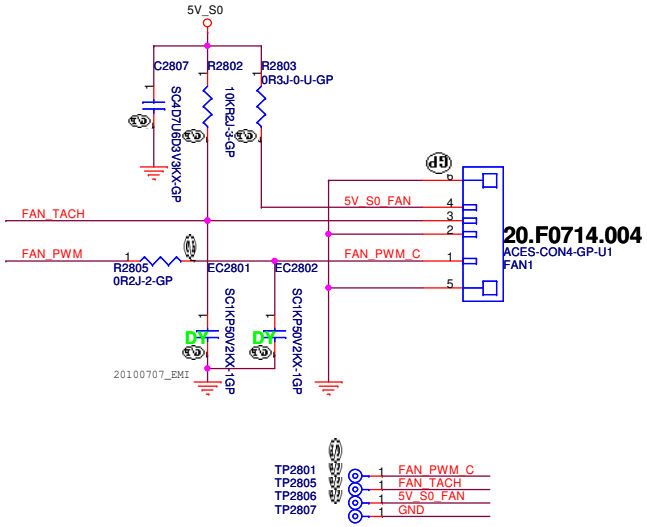


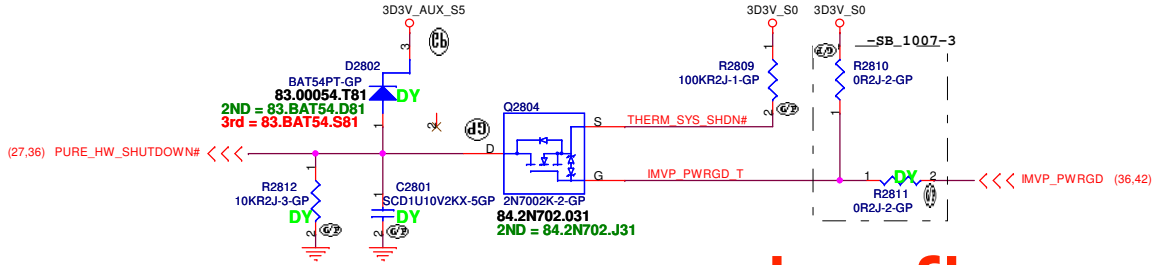
SHDN --> 2N3904 ON External diode



pin6, ALERT# OD
pin7, SYS_SHDN# OD

4 WIRE PWM Fan Control circuit





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103

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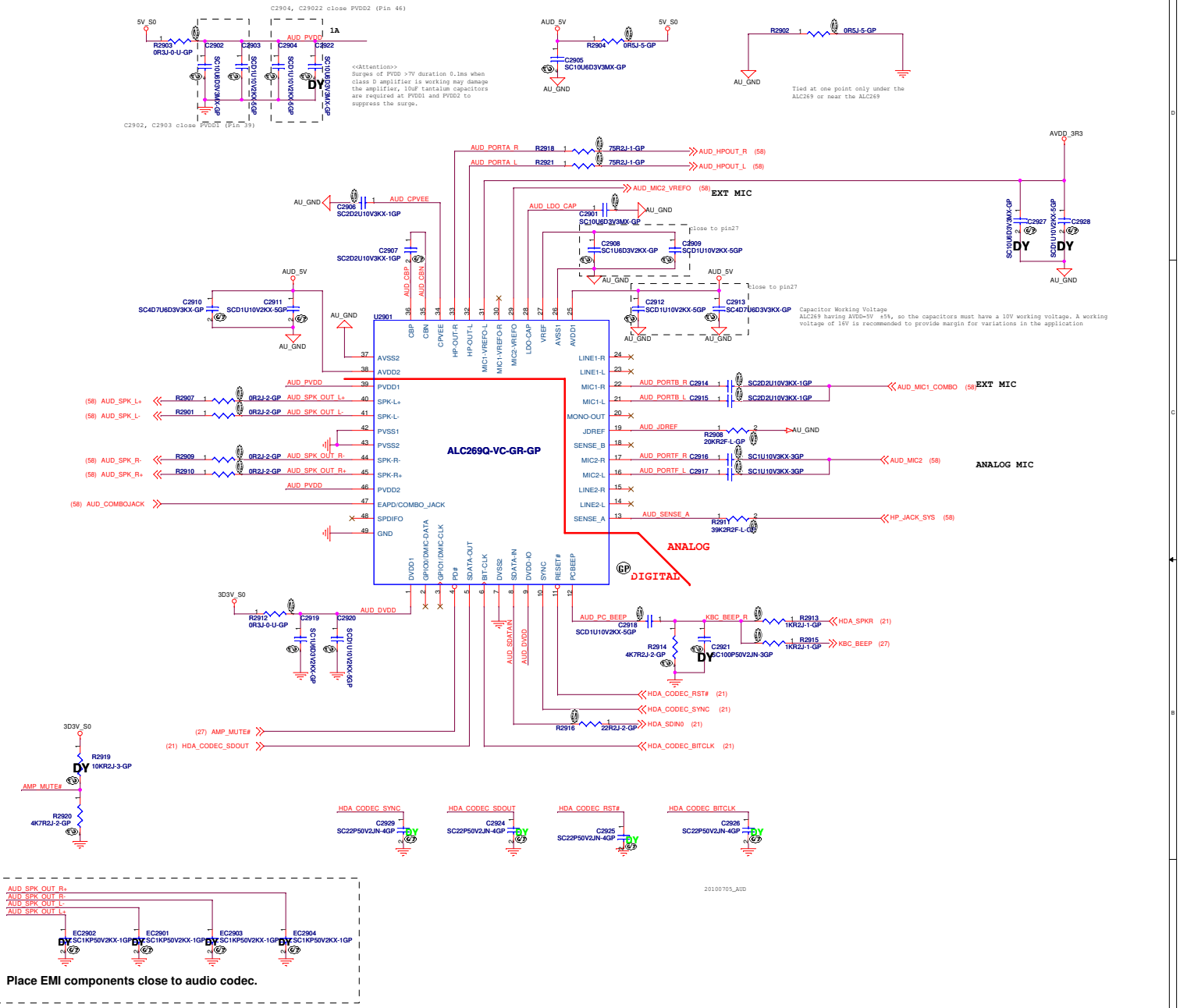

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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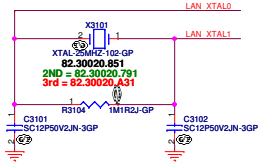
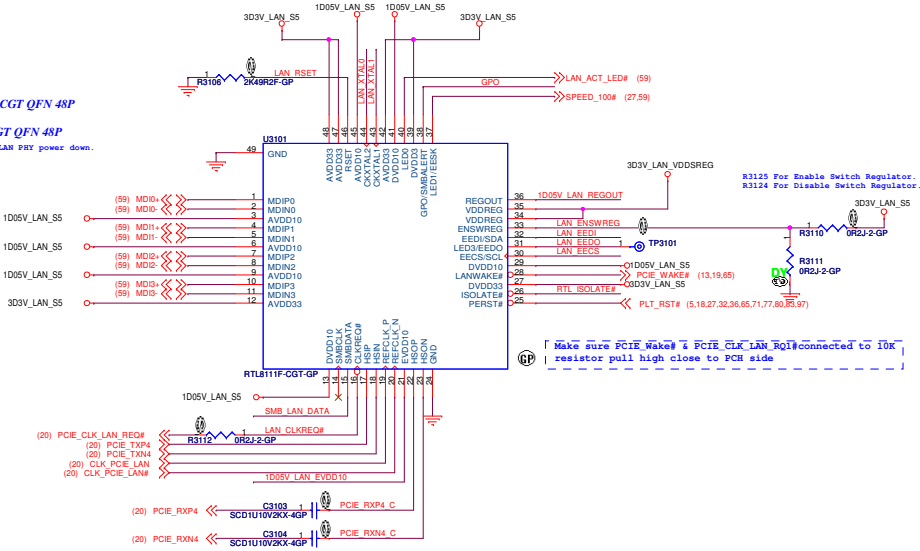
25MHz XTAL



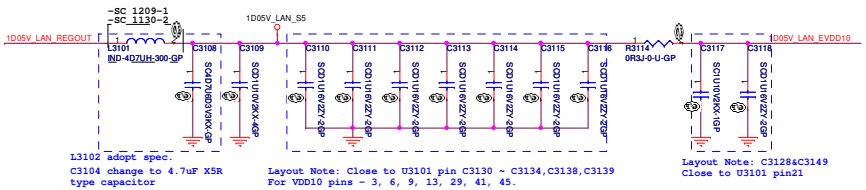
71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.



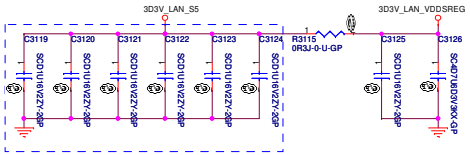
Make sure PCIE_Wake# & PCIE_CLK_LAN_RQI#connected to 10K resistor pull high close to PCH side



L3102 adopt spec.
C3104 change to 4.7uF X5R type capacitor

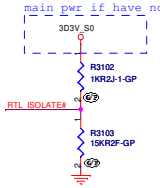
Layout Note: Close to U3101 pin C3130 ~ C3134,C3138,C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21

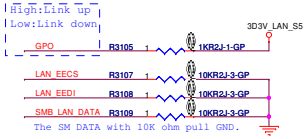


Layout Note: C3135, C3140~C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.

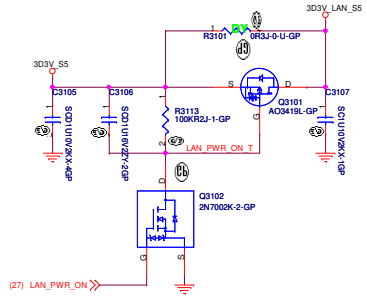
main pwr if have no ASF



High:Link up
Low:Link down



The SM DATA with 10K ohm pull GND.



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111F
Size: A2
Document Number: LLP-1
Rev: SA
Date: Friday, December 09, 2011
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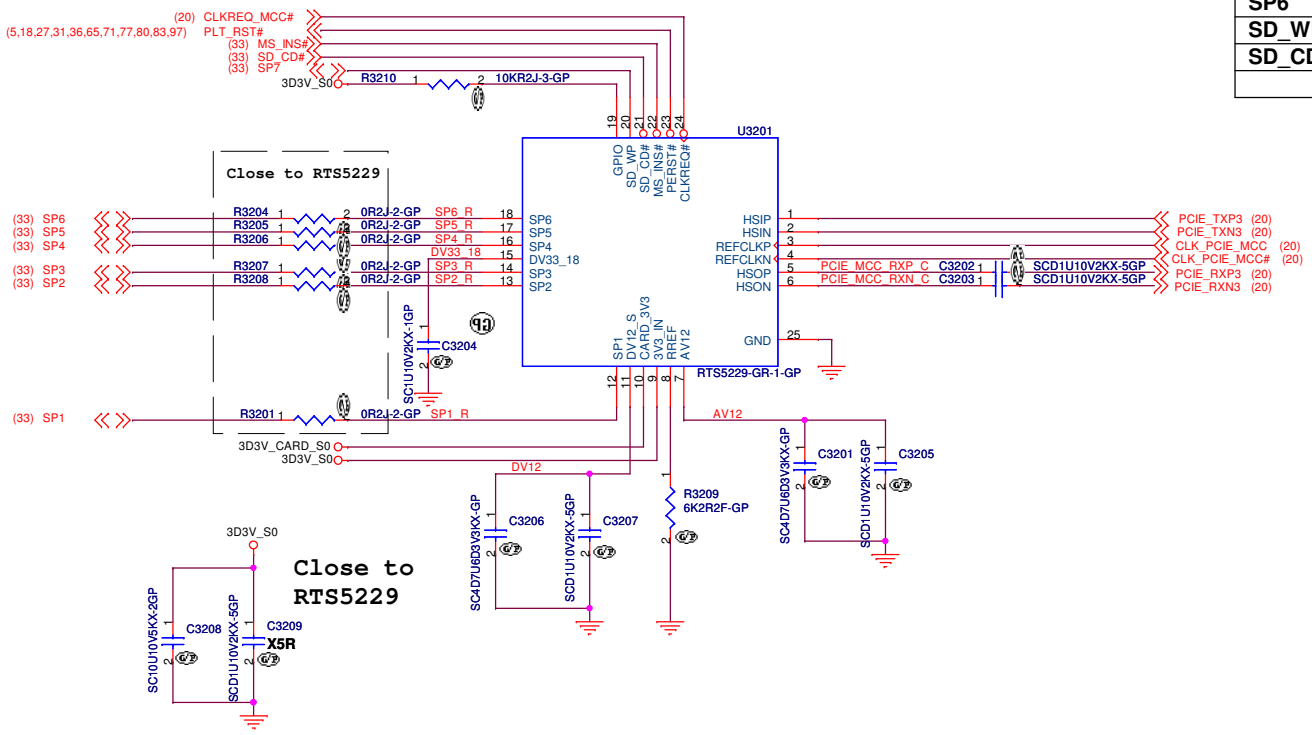
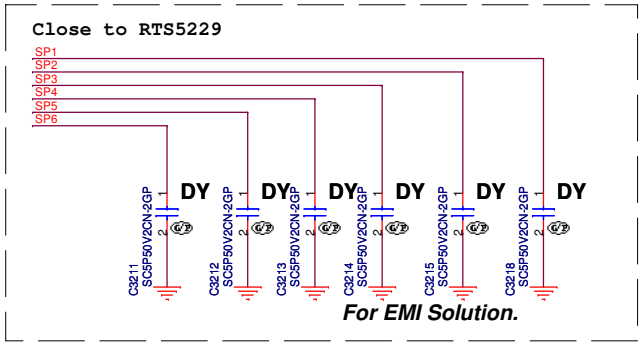
SP_IO	SD/MMC	MS
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SD_WP	SD_WP	MS_BS
SD_CD#		SD_CD#
	MS_INS#	MS_INS#





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5229

Size: A3 | Document Number: LGN-1 | Rev: SA

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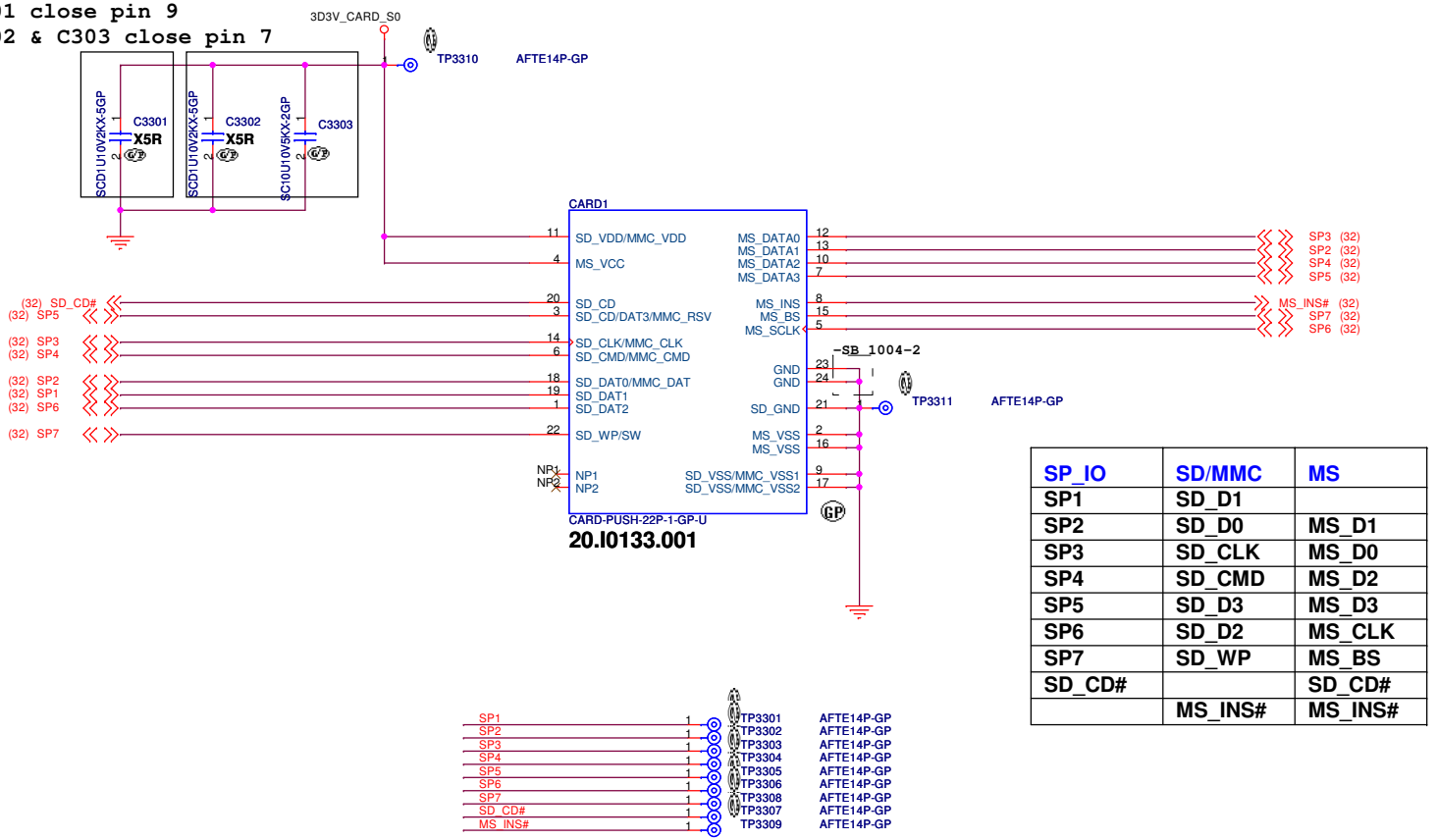
SD/MMC/MMC+ Card Reader

C3301 close pin 9
C3302 & C303 close pin 7



SP_IO	SD/MMC	MS
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS
SD_CD#		SD_CD#
	MS_INS#	MS_INS#

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SD/MMC/MMC+ Card CONN

Size: A3 | Document Number: LGN-1 | Rev: SA

Date: Monday, December 05, 2011 | Sheet 33 of 105

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LLP-1	SA

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<Variant Name>

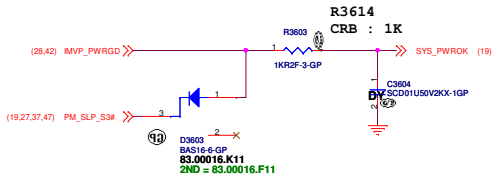
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

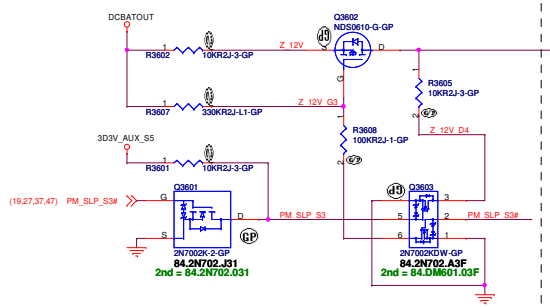
Size	Document Number	Rev
A4	LLP-1	SA

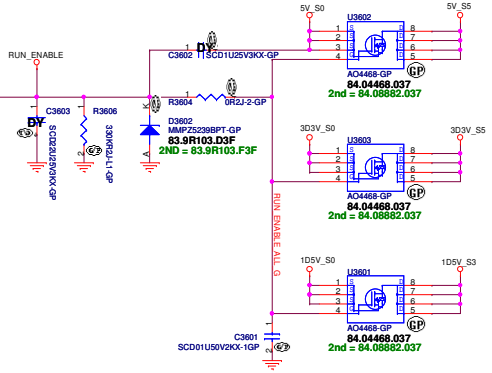
Date: Monday, December 05, 2011 Sheet 35 of 105

Power Sequence



Run Power

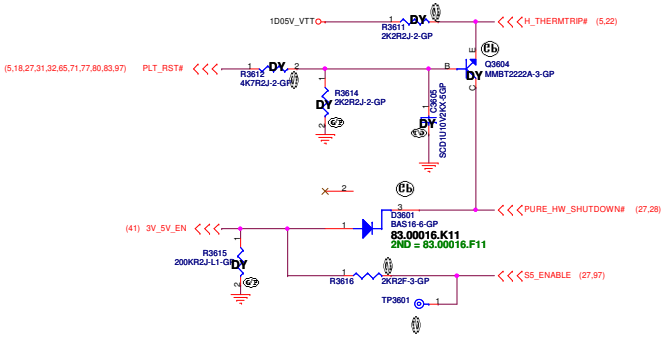


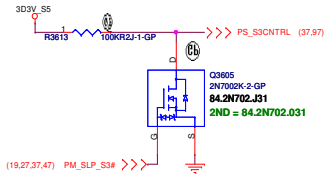


-SB 1003-2

1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A





<Variant Name>

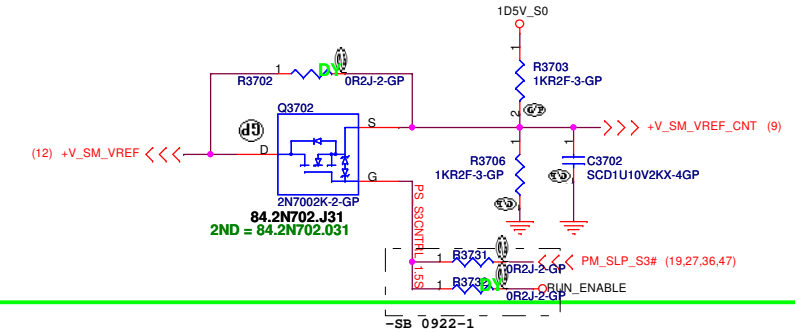
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

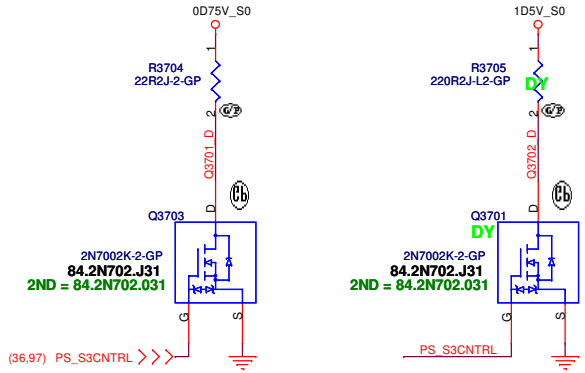
Size: A2 | Document Number: LLP-1 | Rev: SA

Date: Monday, December 05, 2011 | Sheet 36 of 105

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

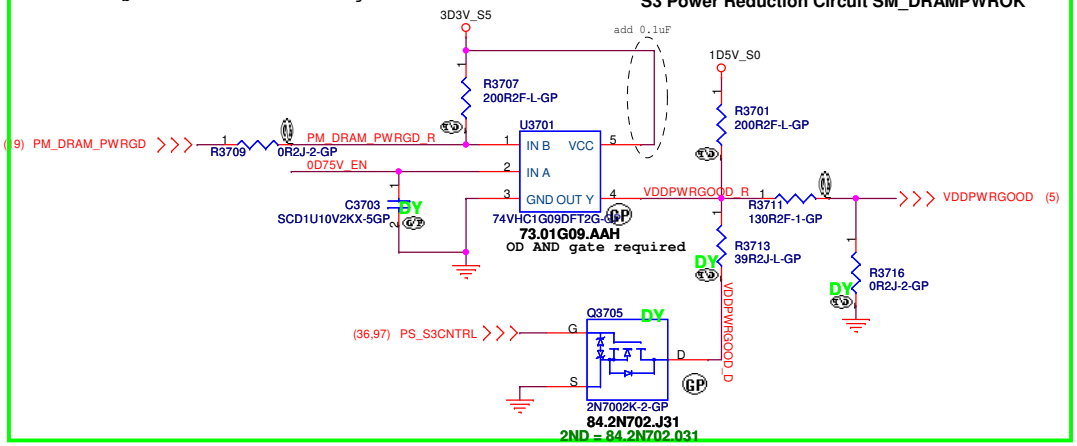


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

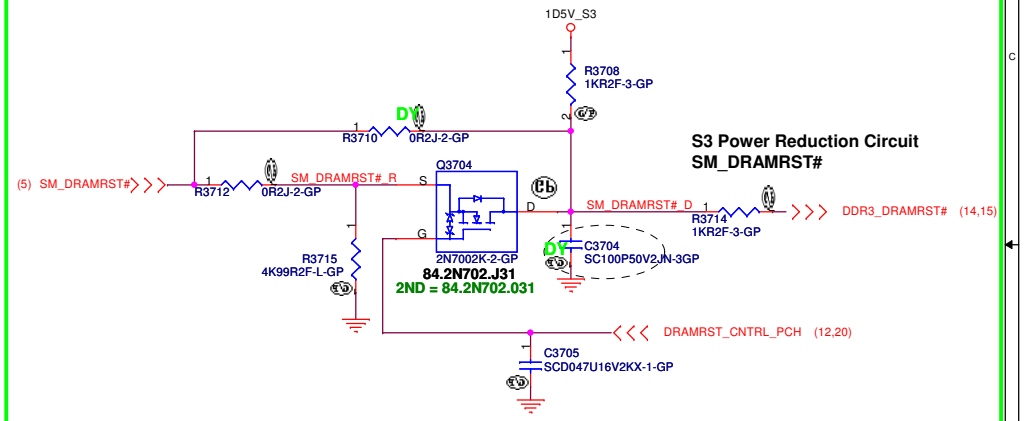


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

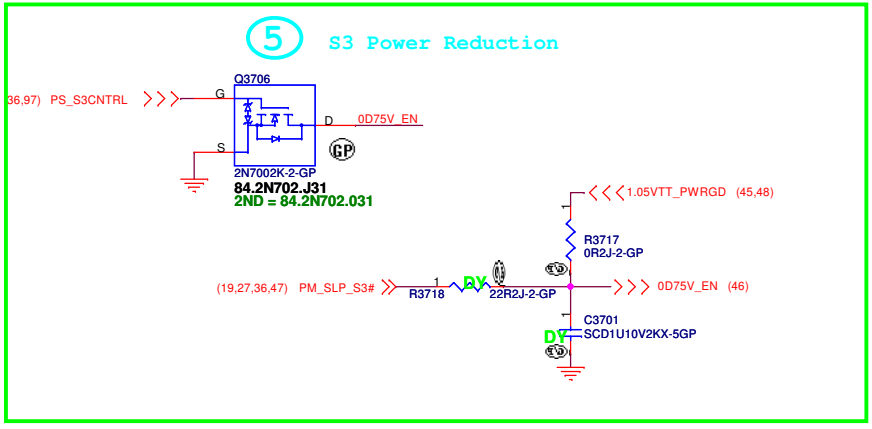
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



5 S3 Power Reduction



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

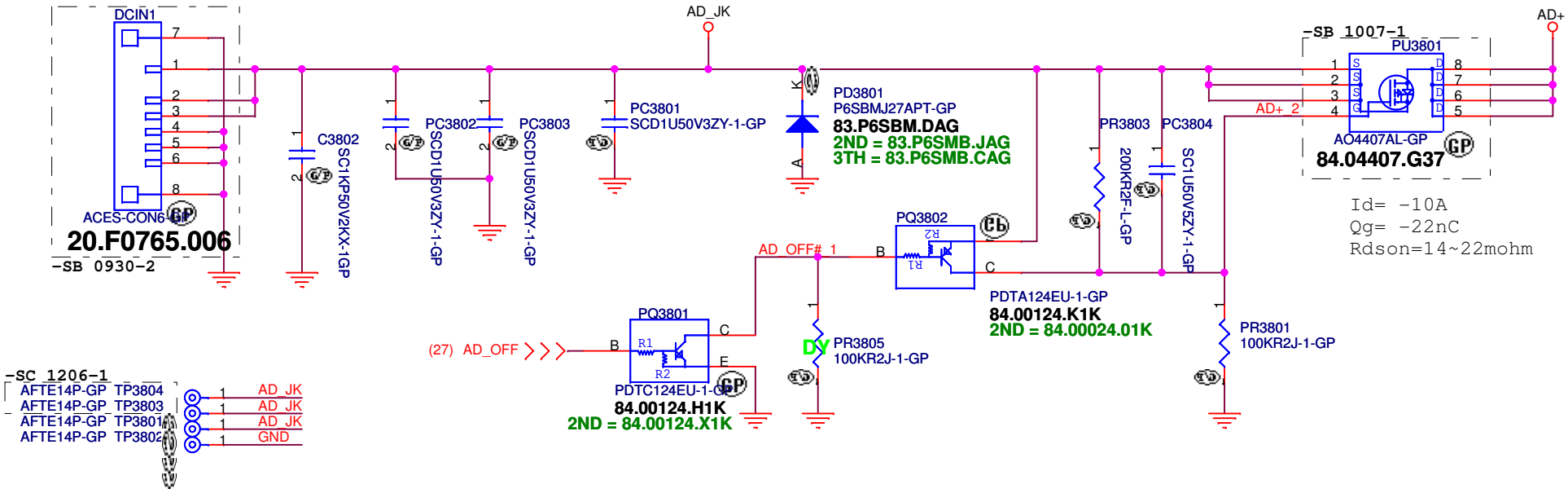
Title: ADAPTER

Size	Document Number	Rev
A3	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 37 of 105

CHECK Adaptor ID PIN

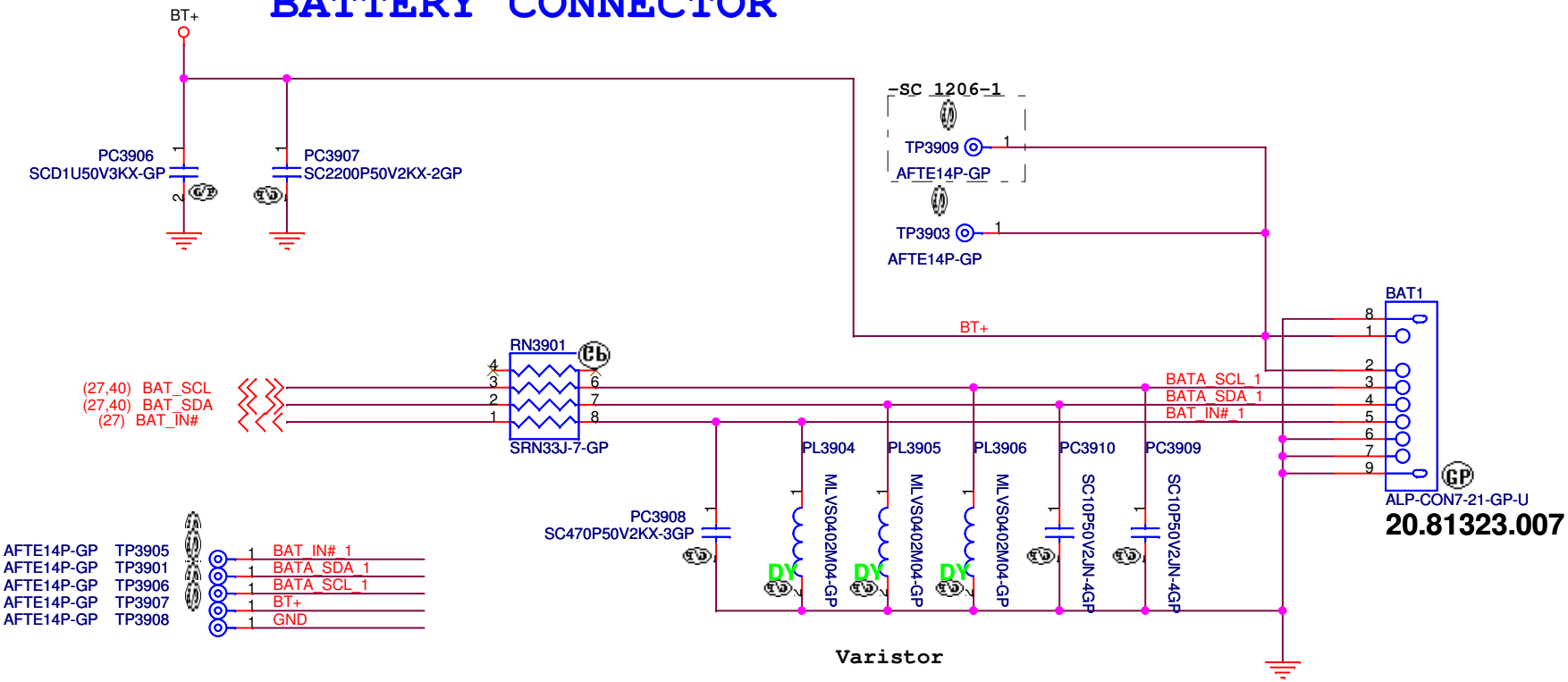
Adaptor in to generate DCBATOUT



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DCIN_JACK	
Size A4	Document Number LLP-1	Rev SA
Date: Tuesday, December 06, 2011	Sheet 38 of 105	

BATTERY CONNECTOR



JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BATT_CONN***	
Size	Document Number **LLP-1**	Rev **SA**
Date: Tuesday, December 06, 2011	Sheet 39 of 105	

SSID = Charger

A8 (ANNIE/ASTRO)
PR4007,PR4008 R1:
UMA:64.12425.6DL
DIS:64.60425.6DL

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118K	100K

STOP_CHG# connects to KBC

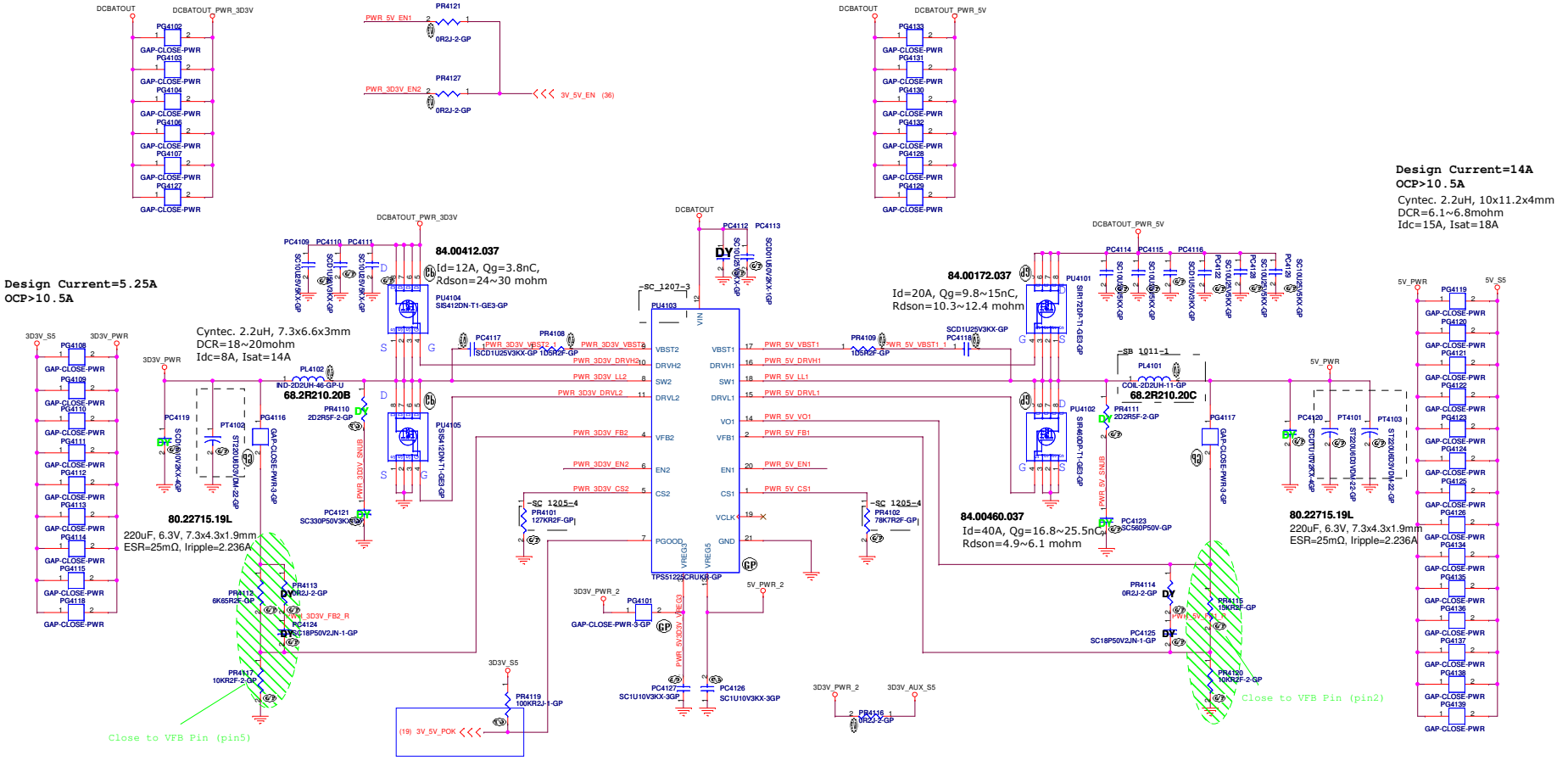
Cyntec.5.6uH 7*6.6*3mm
DCR=39~42mohm
Idc=5.5A, Isat=6.0A

Charger Current=1.4~3.6A

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: BQ24737_Charger
Size: Document Number: LLP-1 Rev: SA
Date: Wednesday, December 07, 2011 Sheet 40 of 105

SSID = PWR.Plane.Regulator_5v3p3v



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

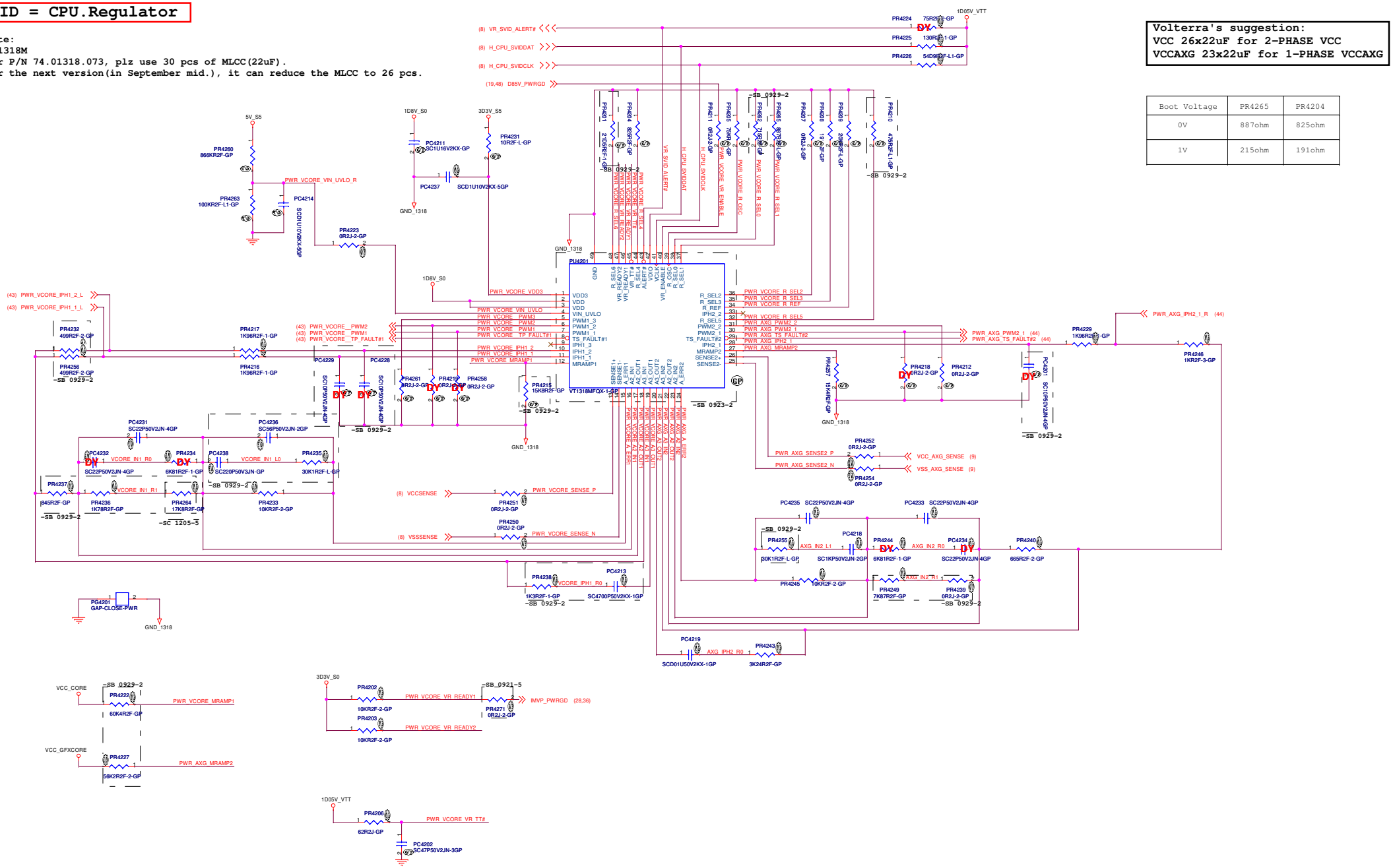
Title	TPS51225_5V_3D3V	
Size	Document Number	Rev
	LLP-1	SA
Date: Wednesday, December 07, 2011	Sheet 41 of 105	

SSID = CPU.Regulator

Note:
VT1318M
For P/N 74.01318.073, plz use 30 pcs of MLCC(22uF).
For the next version(in September mid.), it can reduce the MLCC to 26 pcs.

Volterra's suggestion:
VCC 26x22uF for 2-PHASE VCC
VCCAXG 23x22uF for 1-PHASE VCCAXG

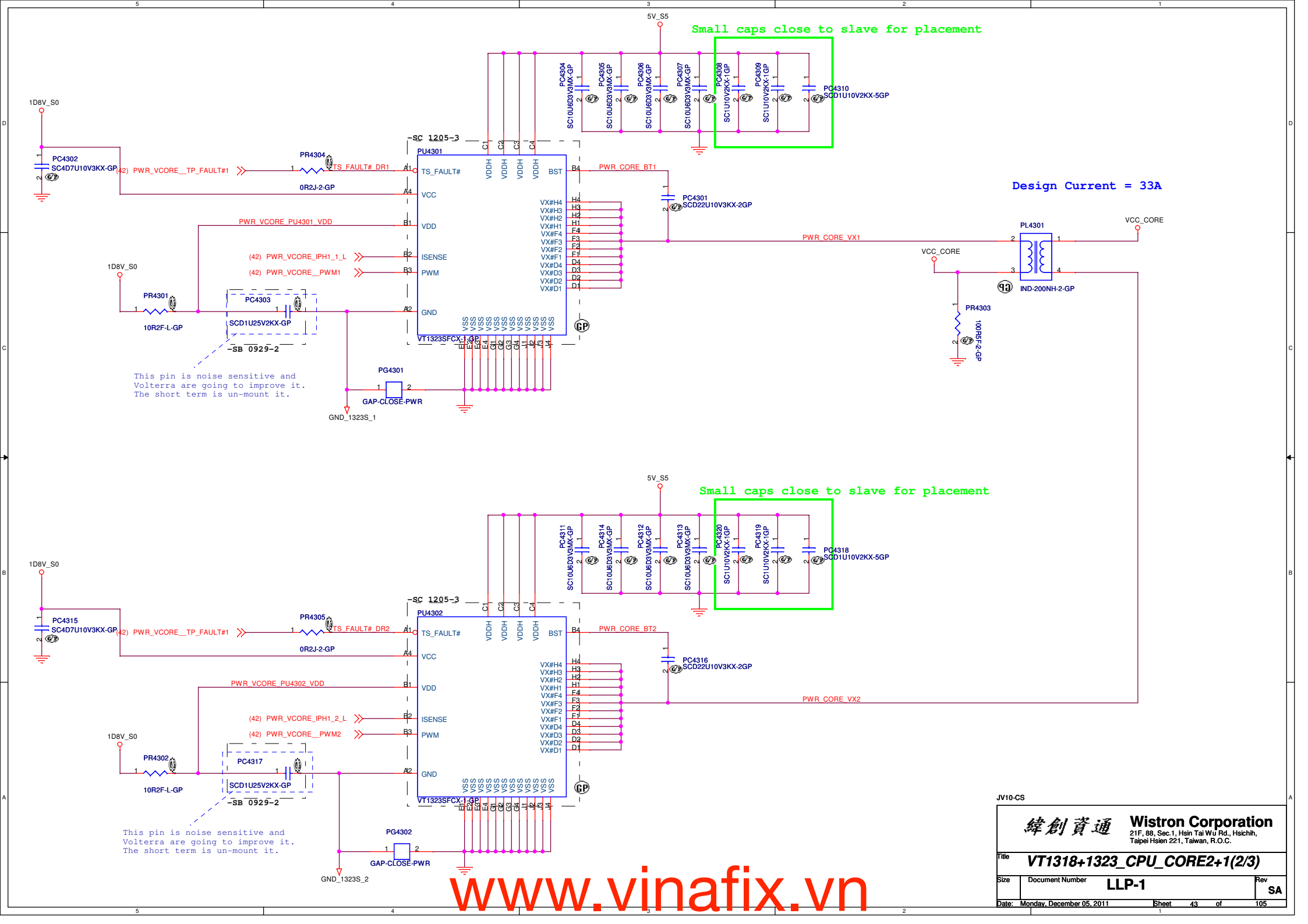
Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm

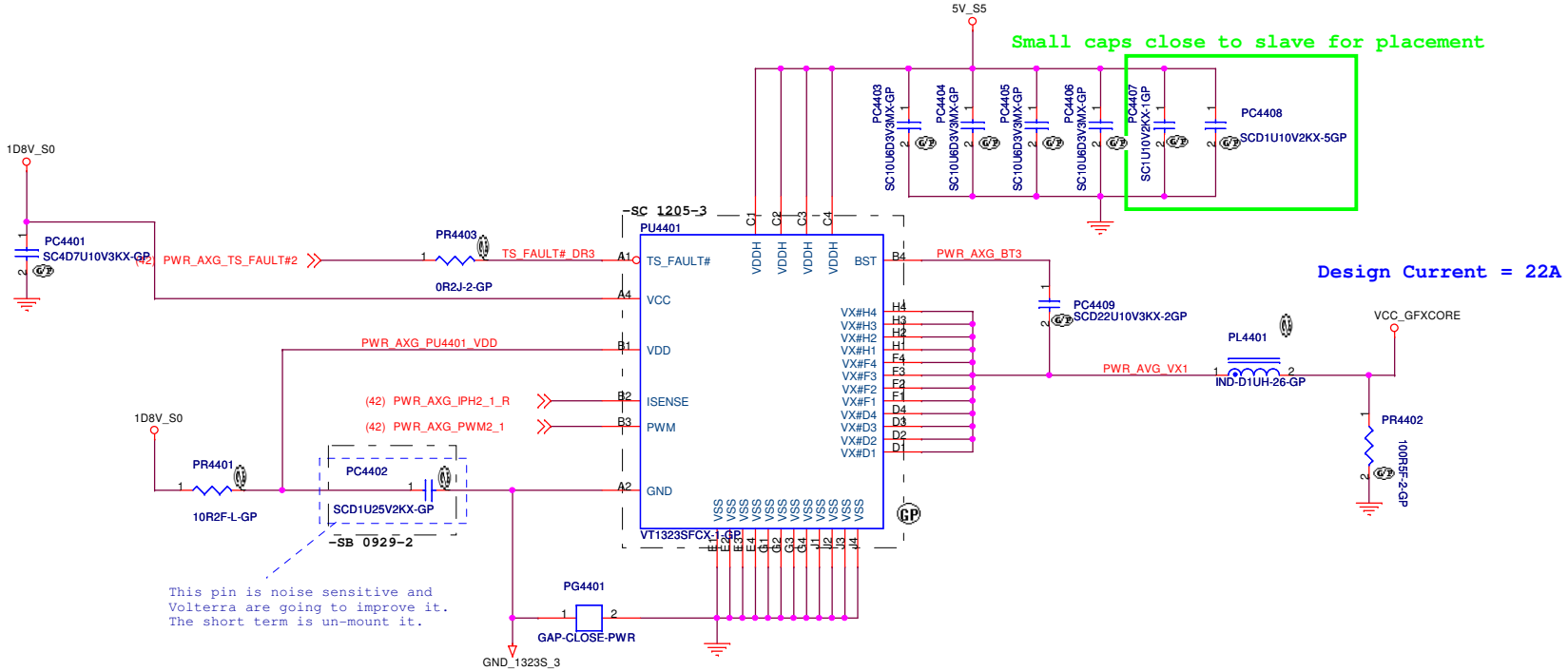


JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318+1323_CPU_CORE2+1(1/3)
Size: | Document Number: LLP-1 | Rev: SA
Date: Monday, December 05, 2011 | Sheet 42 of 105

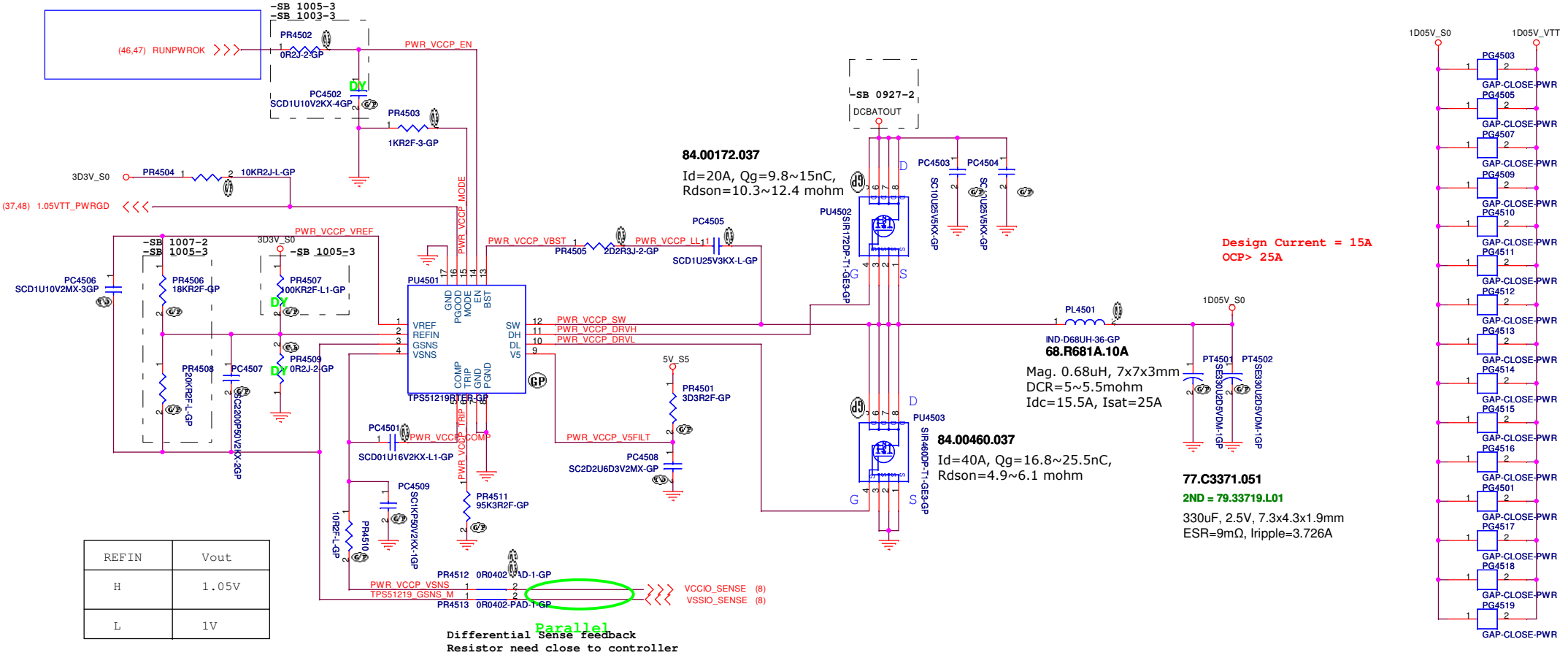




JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VT1318+1323_CPU_CORE2+1(3/3)	
Size	Document Number LLP-1	Rev SA
Date: Monday, December 05, 2011	Sheet 44 of 105	

TPS51219 for 1D05V



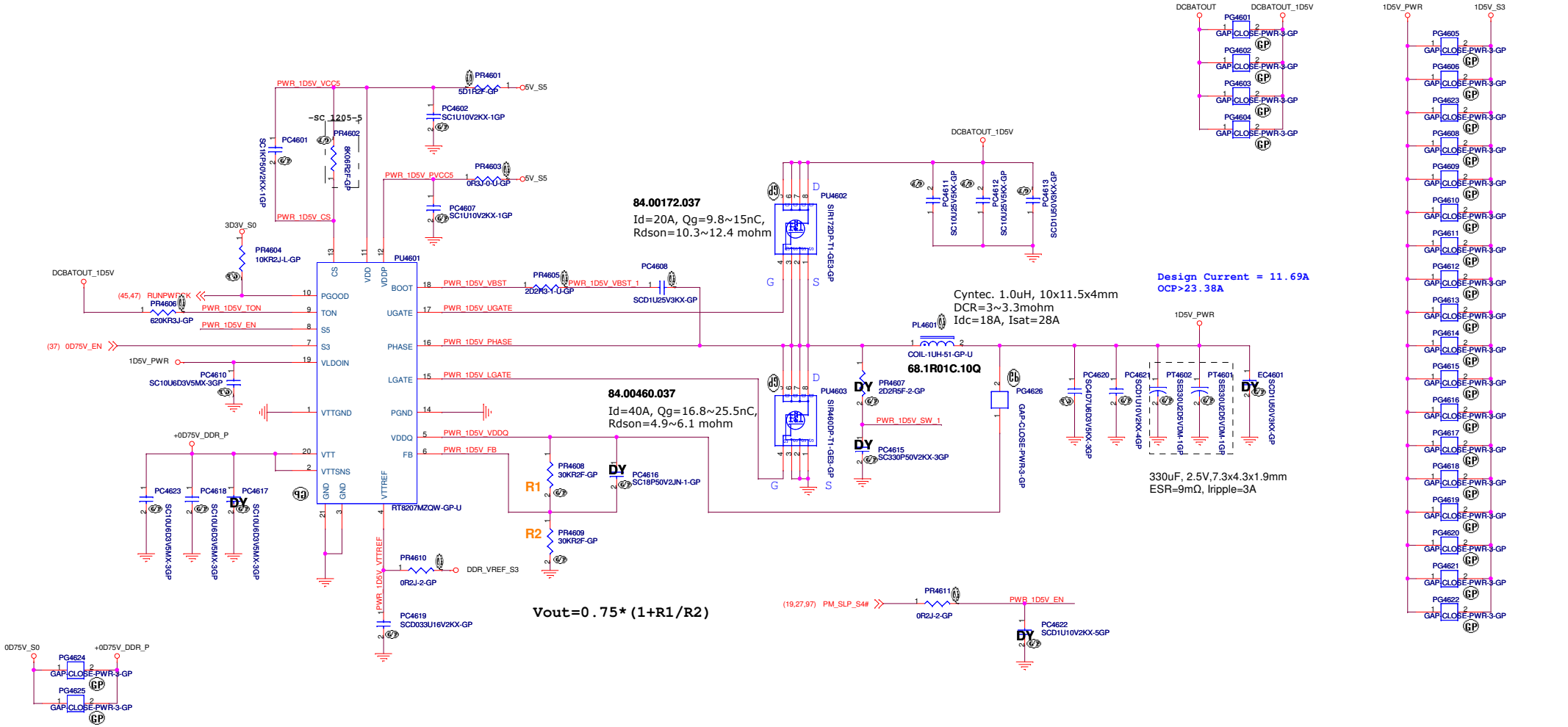
REFIN	Vout
H	1.05V
L	1V

JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51219_1D05V	
Size	Document Number: LLP-1	Rev: SA
Date: Monday, December 05, 2011	Sheet 45 of 105	

SSID = PWR.Plane.Regulator_1p5v0p75v

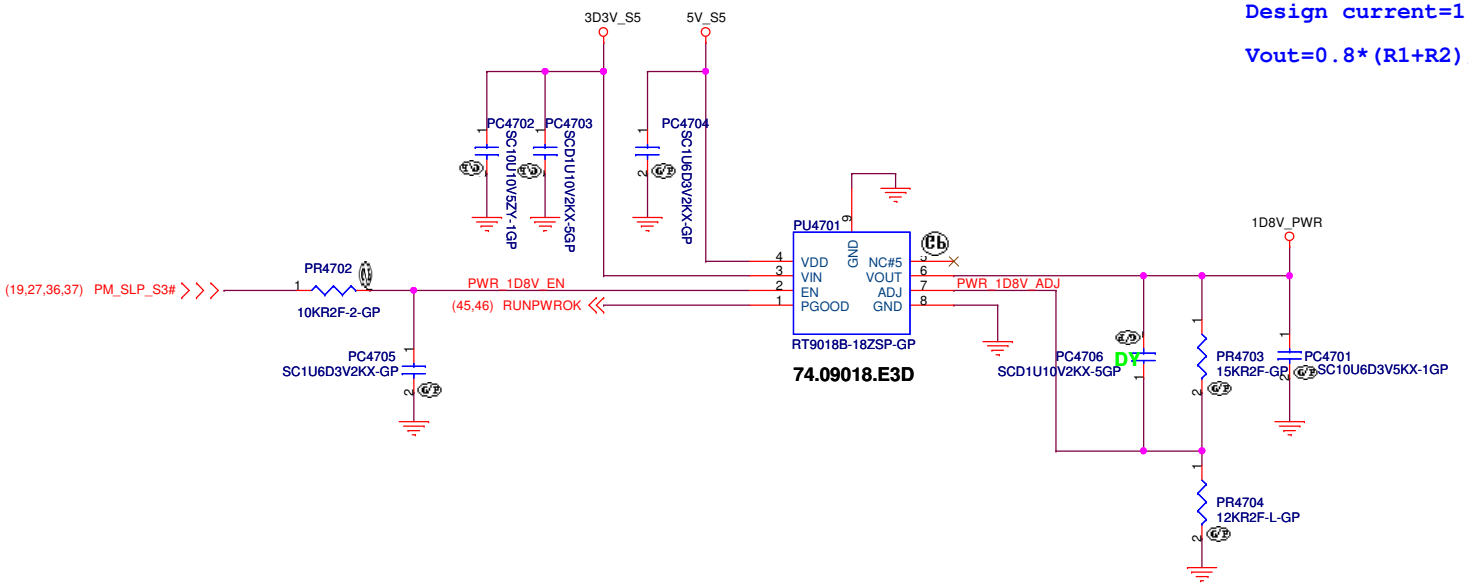


JV10-CS

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8207M_1D5V_0D75V		
Size	Document Number: LLP-1	Rev: SA
Date: Monday, December 05, 2011	Sheet 46 of 105	

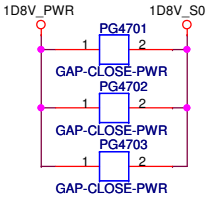
SSID = PWR.Plane.Regulator_1p8v

RT9018B-18ZSP for 1D8V_S0



Design current=1.05A

Vout=0.8*(R1+R2)/R2

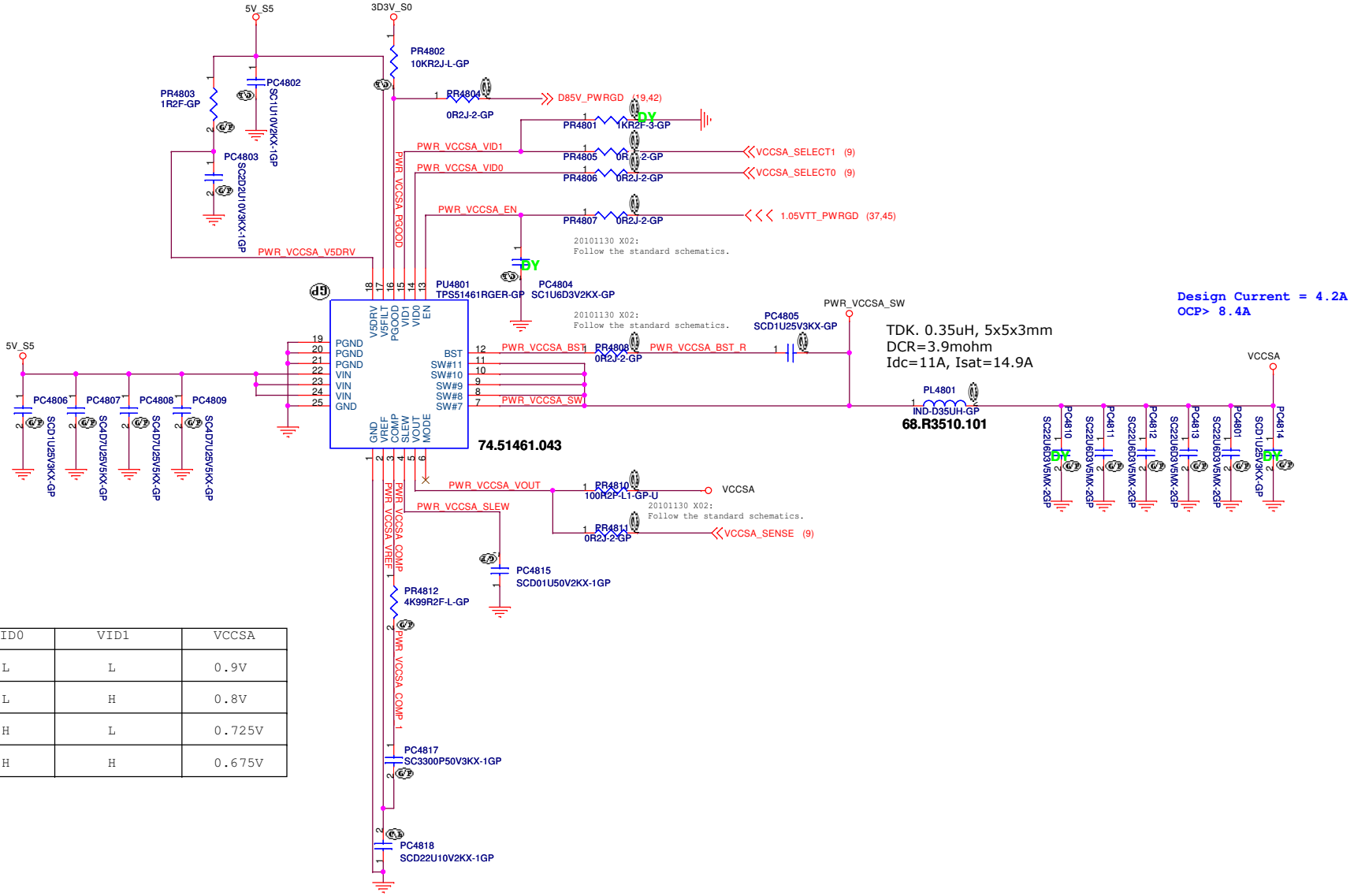


JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWM_1D8V_RT9018B-18ZSP	
Size	Document Number: LLP-1	Rev: SA
Date: Monday, December 05, 2011	Sheet 47 of 105	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

JV10-CS

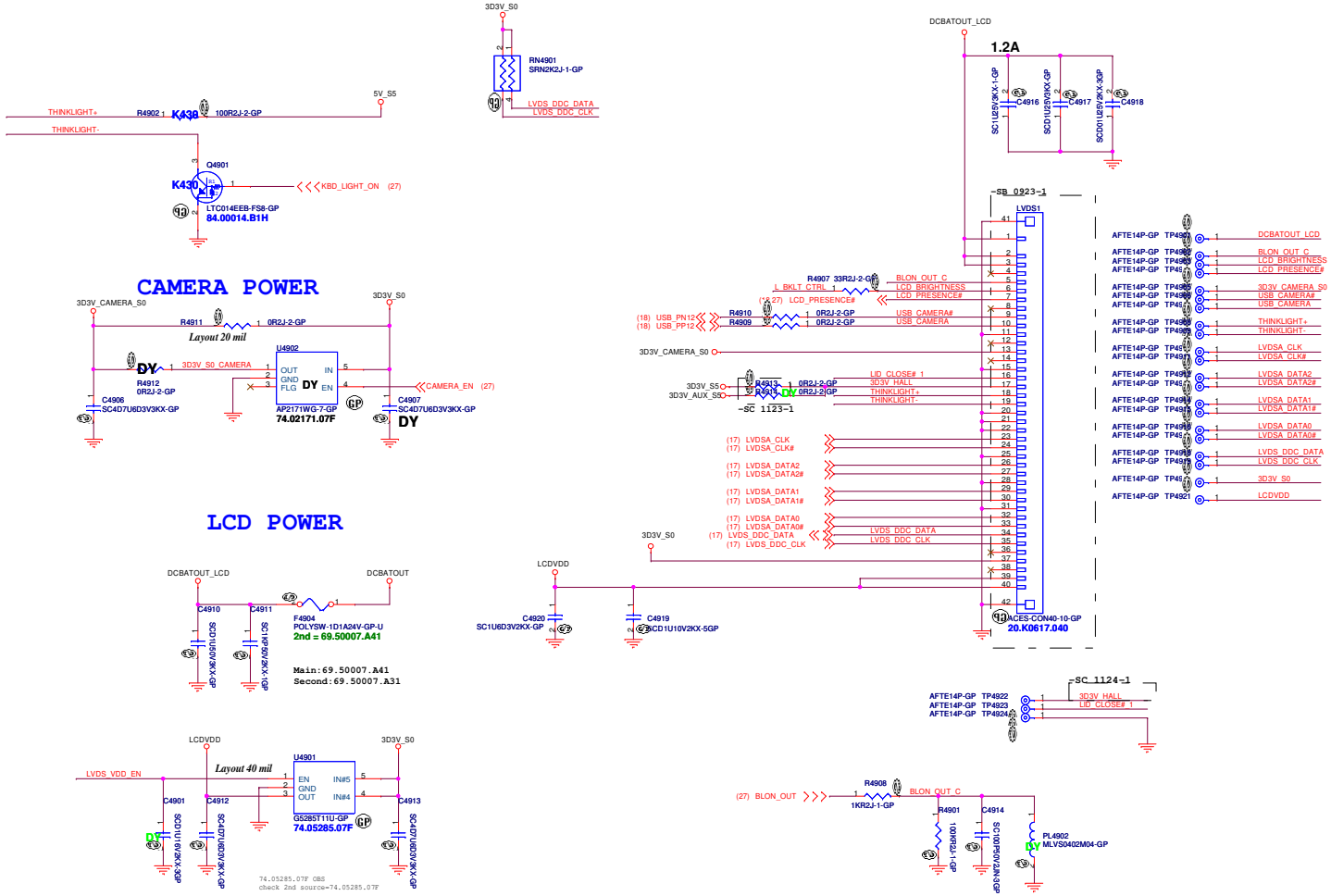
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA_TPS51461	
Size	Document Number LLP-1	Rev SA
Date: Monday, December 05, 2011	Sheet 48 of 105	

SSID = VIDEO

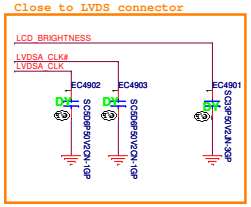
LVDS connector

LCD / Inverter Connector



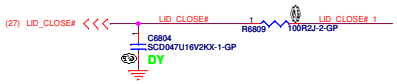
For EMI request

Close to LVDS connector



Panel BL brightness/Power En/BL En

HALL SENSE



<Variant Name>

緯創資通 Wistron Corporation

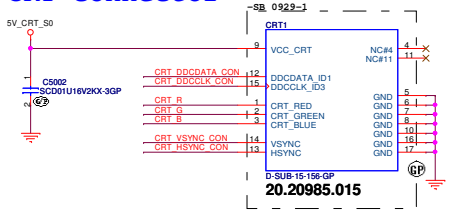
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

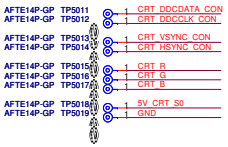
Title: LCD Connector

Size | Document Number | Rev: SA

Date: Wednesday, December 05, 20 | Sheet of 105

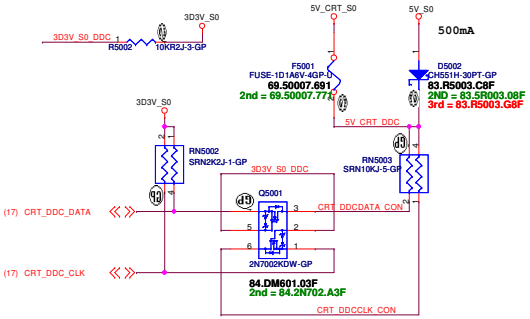
CRT connector



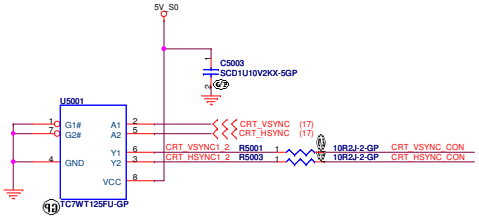


CRT DDCDATA & DDCCLK level shift

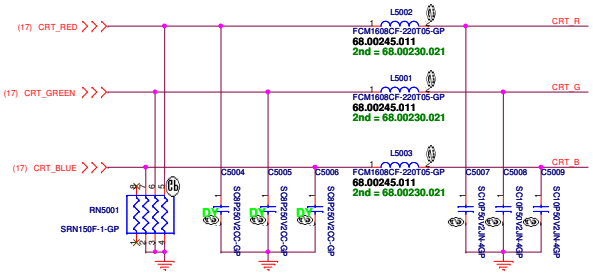
Pull High 5V Design on CRT Board

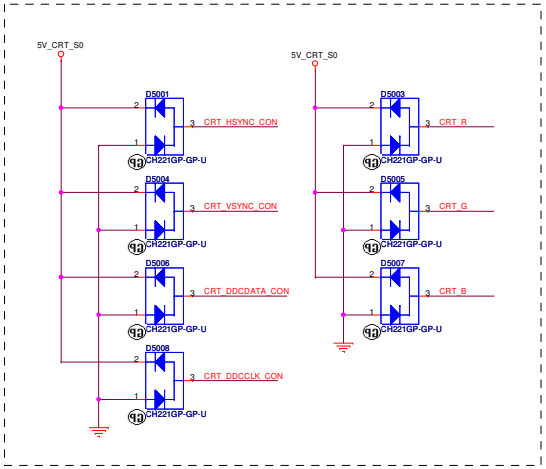


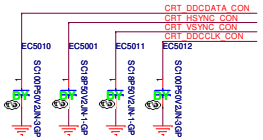
CRT Hsync & Vsync level shift



CRT RGB







<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size: A2 | Document Number: LLP-1 | Rev: SA

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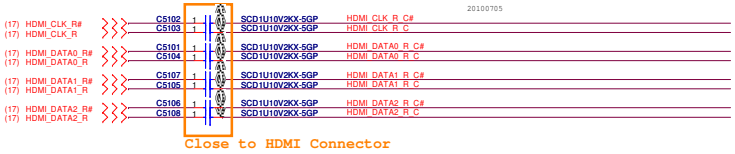
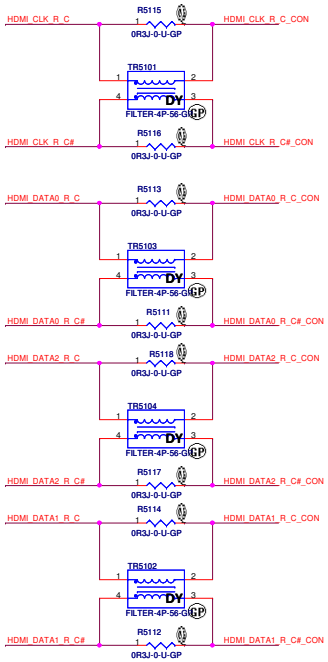
SSID = VIDEO

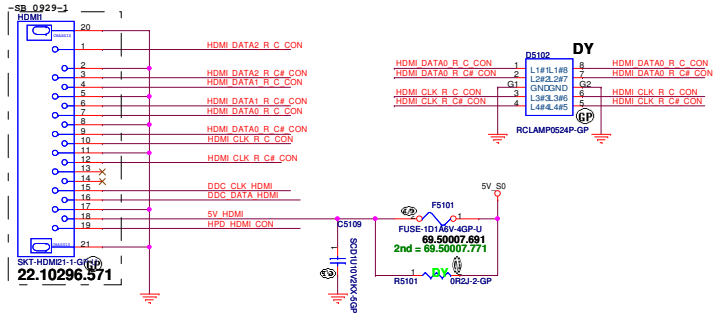
HDMI Passive Level Shifter

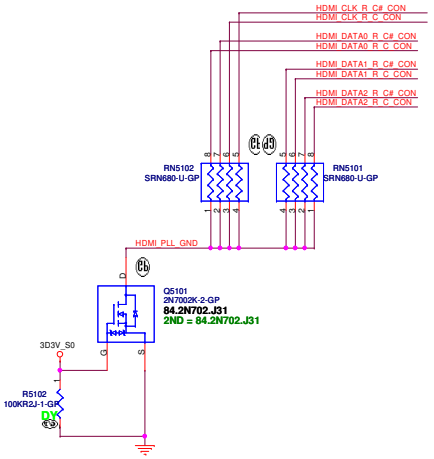
Close to HDMI Connector

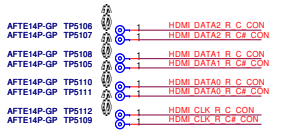


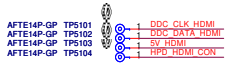


HDMI CONNECTOR

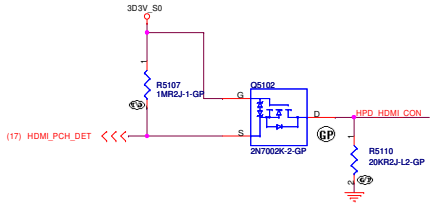


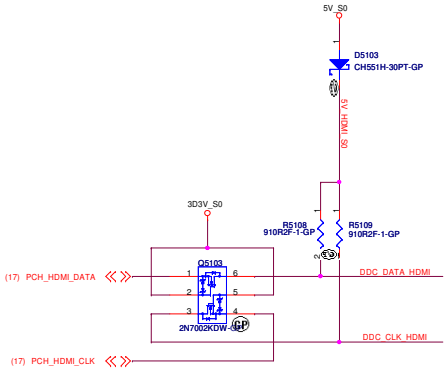






HDMI DDC Passive Level Shifter





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: LLP-1 | Rev: SA

Date: Monday, December 05, 2011 | Sheet 51 of 105

BLANK

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

Size	Document Number	Rev
A4	LLP-1	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	LLP-1	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LLP-1	SA

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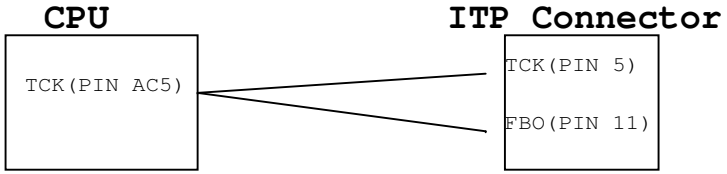
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

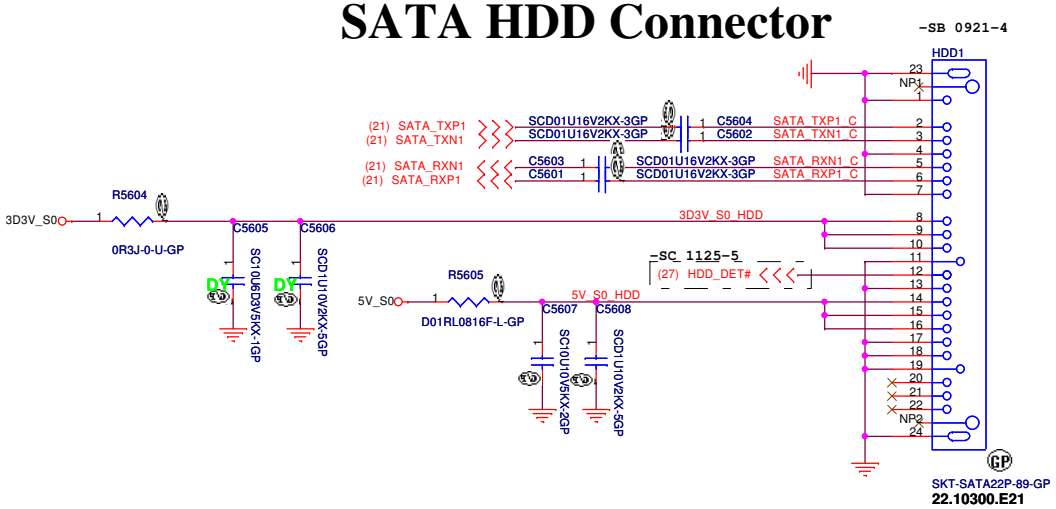


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LLP-1	Rev: SA
Date: Monday, December 05, 2011	Sheet 55 of 105	

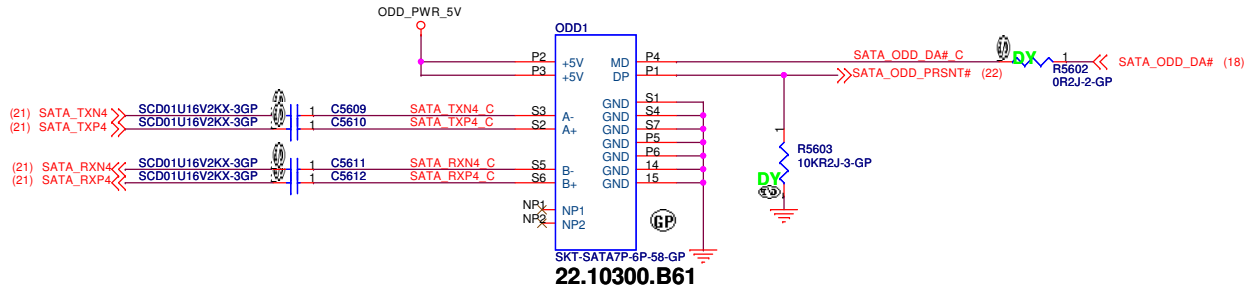
SATA HDD Connector



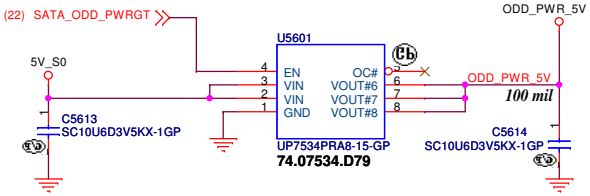
ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

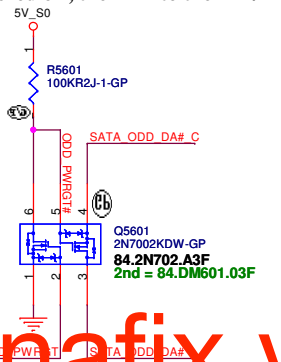


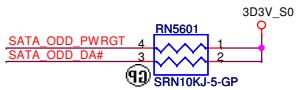
SATA Zero Power ODD



Current limit
Active High
typ =>2A

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON





SUPPORT ZERO SATA ODD

<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD**

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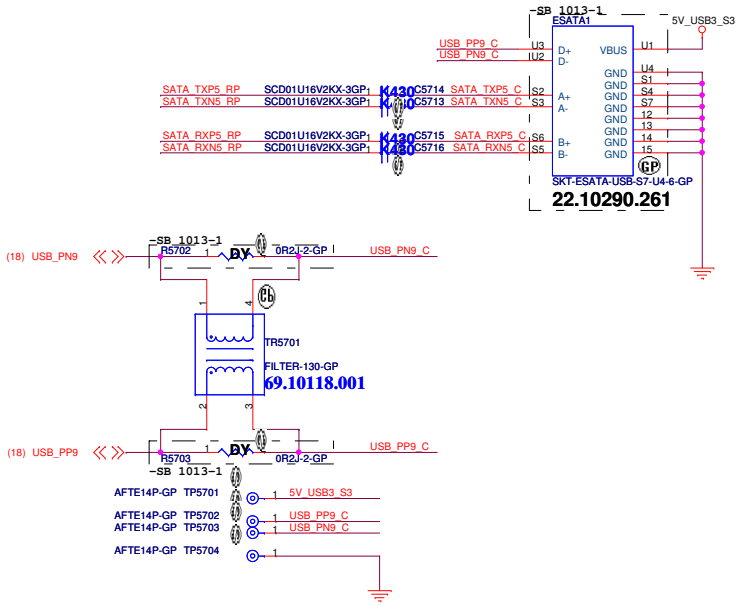
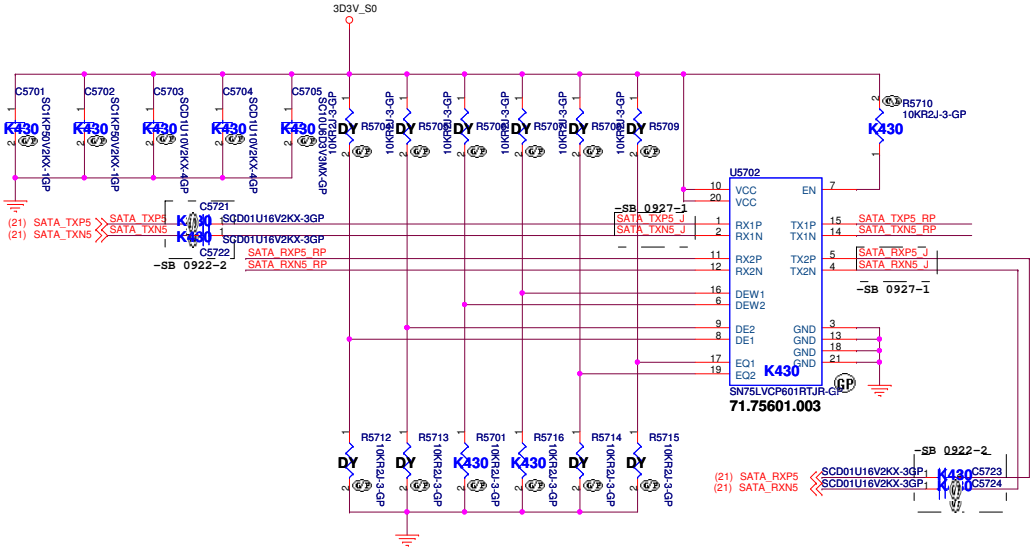


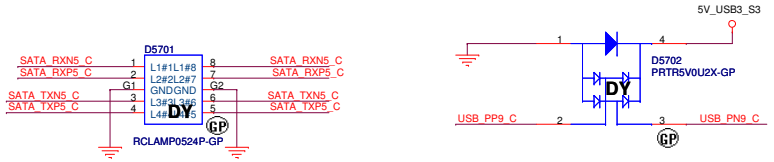
ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND

USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

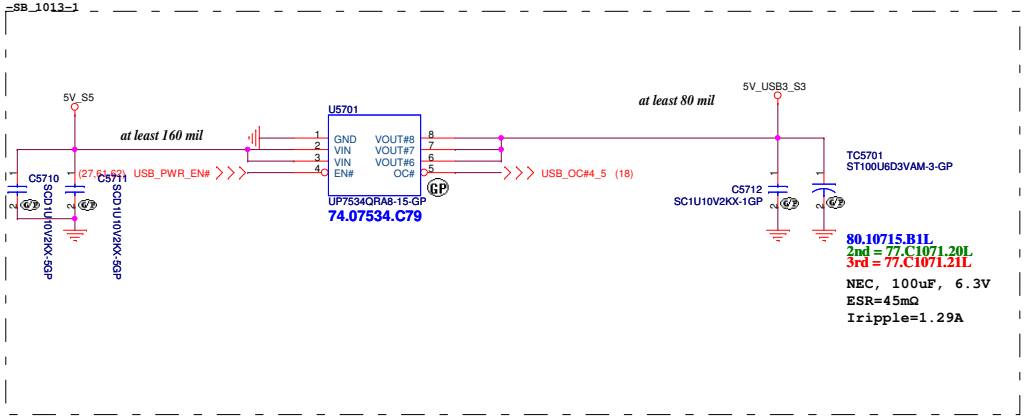


ESATA Repeater

ESD Protection



POWER



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA or USB20

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Custom	LLP-1	SA

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Int. Mono Analog MIC for B series

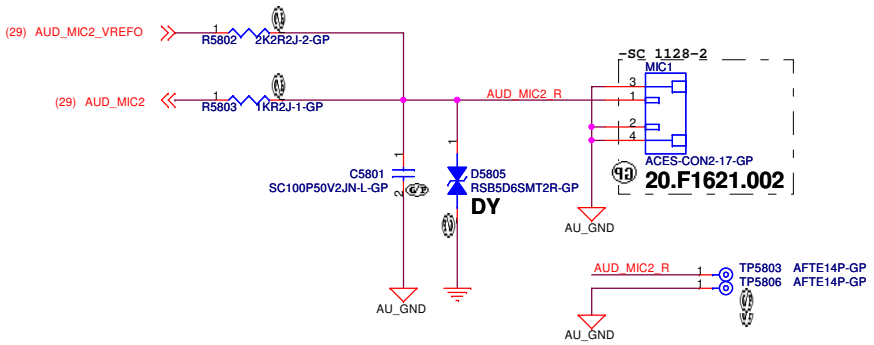
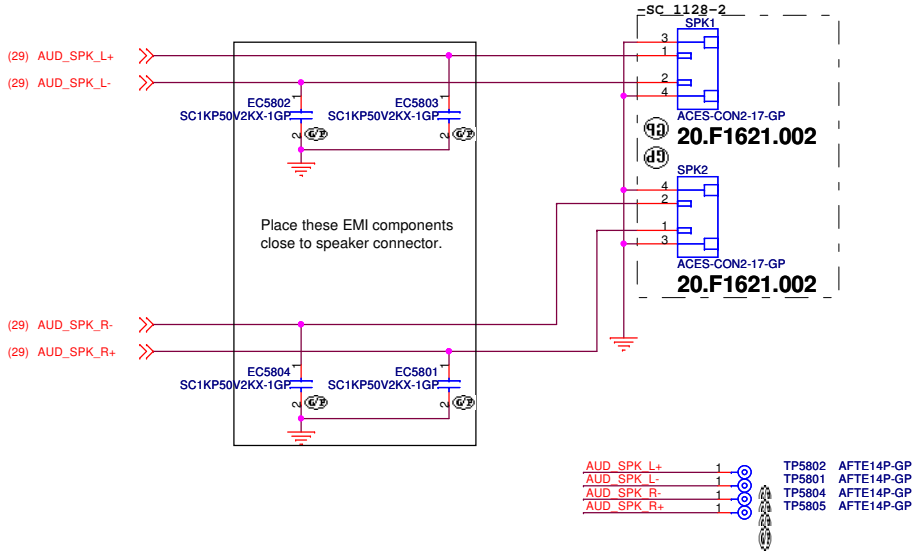
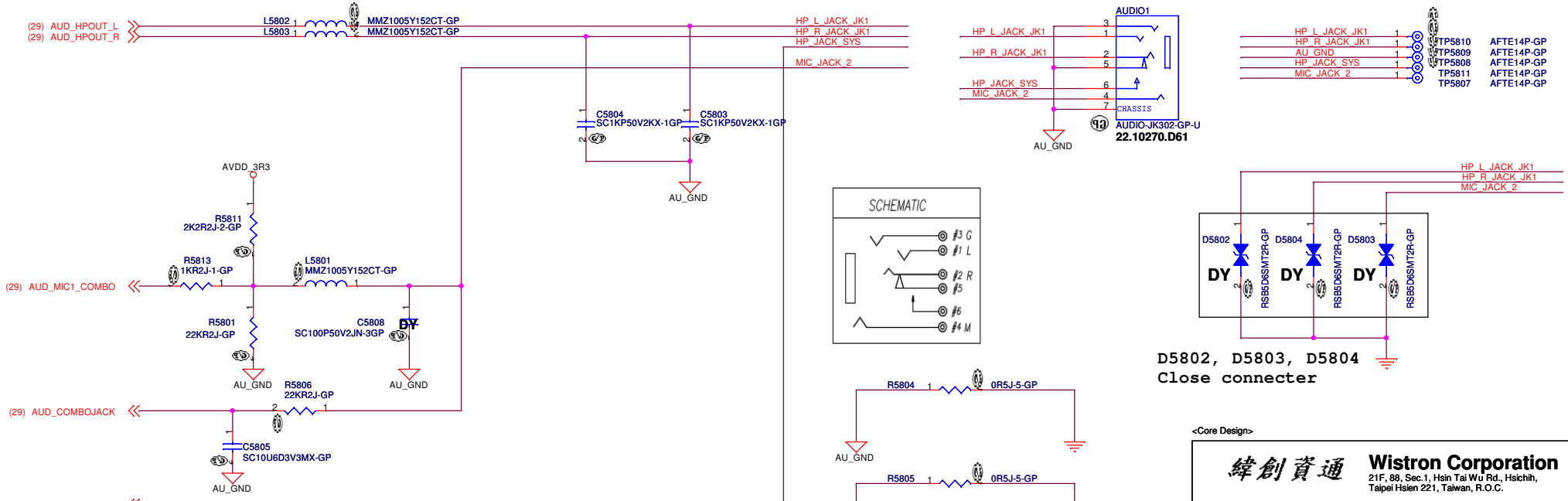


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

INTERNAL STEREO SPEAKERS





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

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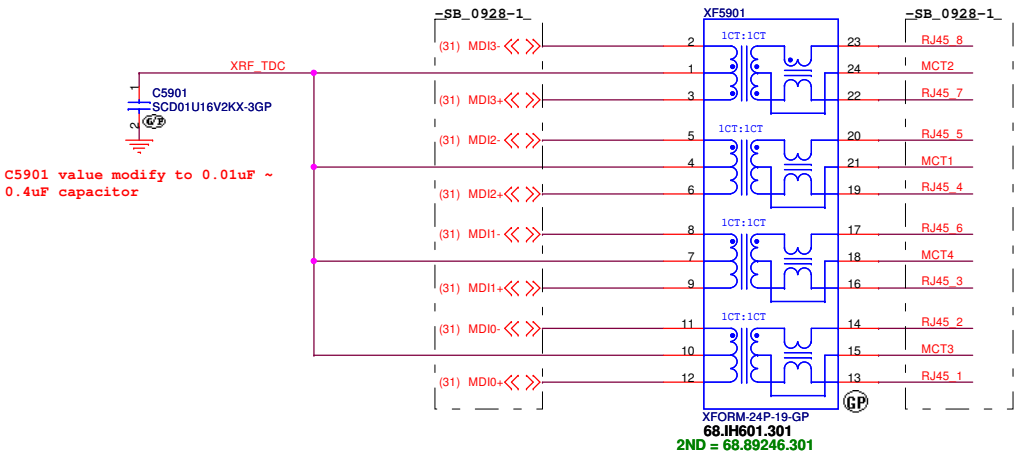
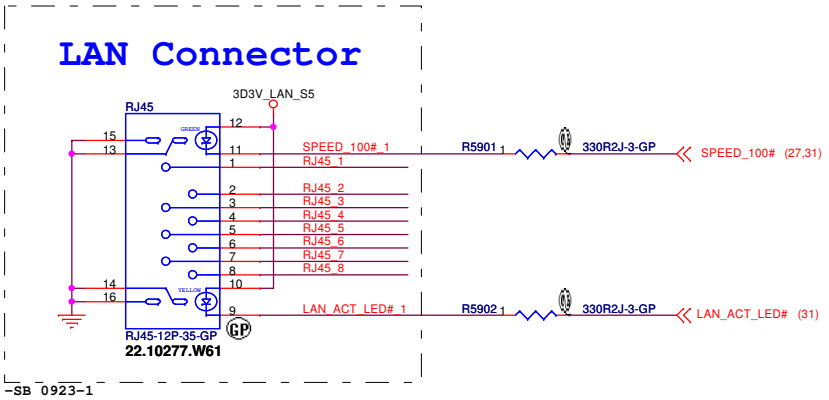
FOR CO-LAY

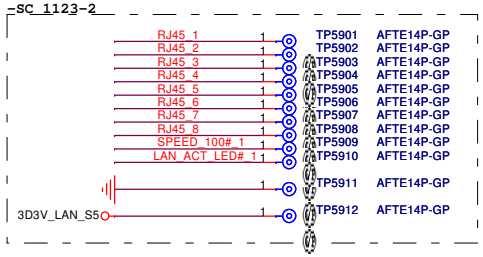
GIGA Lan Transformer

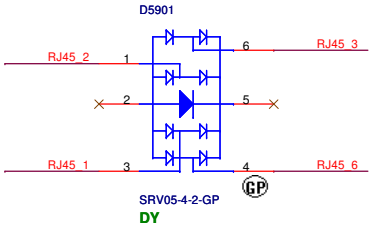


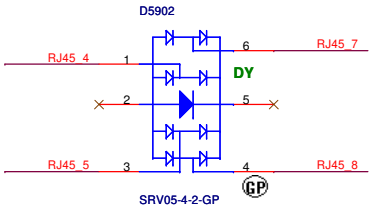
1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

LAN Connector



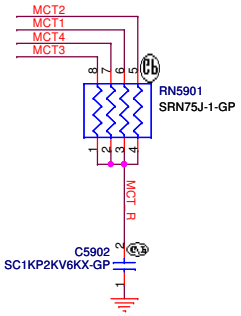






TVS
83.00005.BAE
DIODE ARR SRV05-4.TCT SOT-23-6

83.09904.AAE
DIODE ESD AZC099-04S SOT23-6L



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45 / Transformer

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A3	LLP-1	SA

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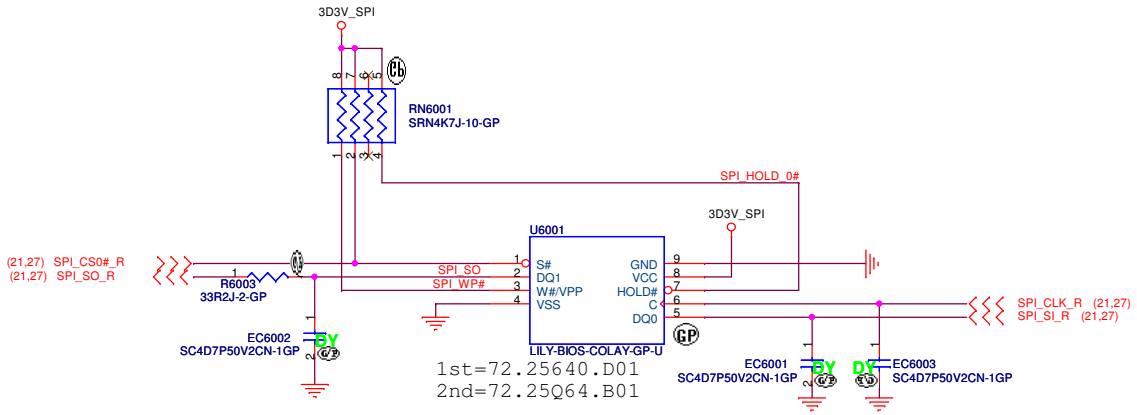
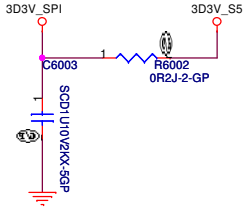
SSID = Flash.ROM

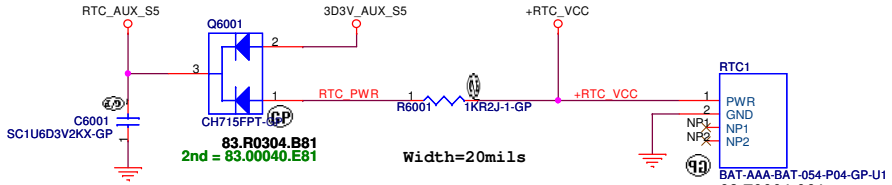
SPI FLASH ROM (8M byte) for PCH

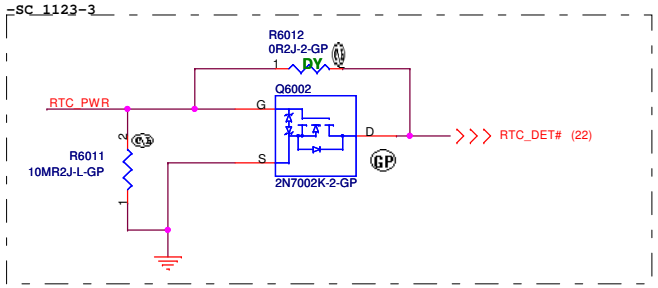


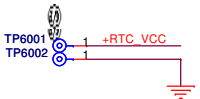


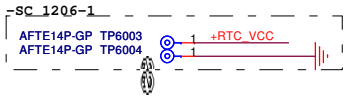
SPI FLASH ROM (8M byte) for PCH

SSID = RBATT









<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: LLP-1 | Rev: SA

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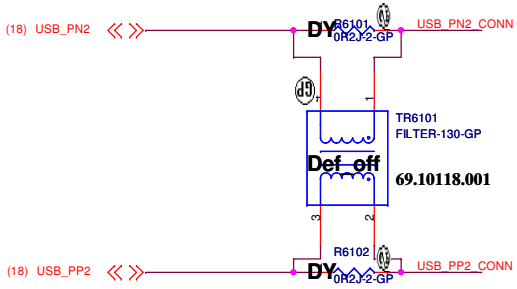
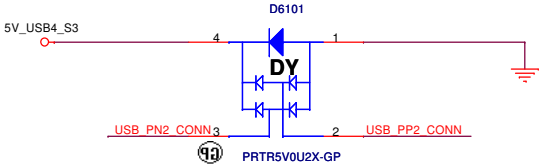
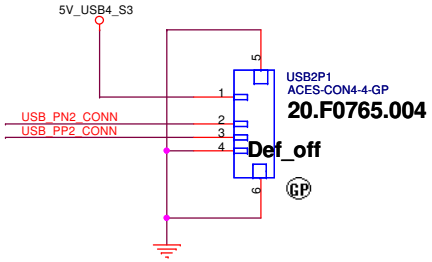
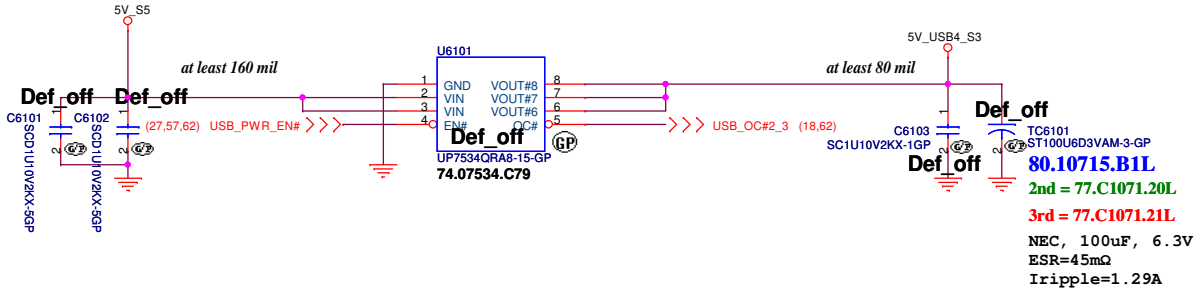






Only USB2.0

POWER



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Connector
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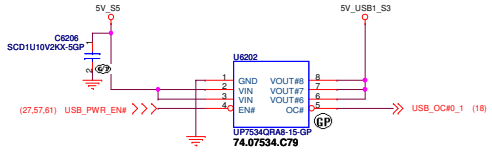
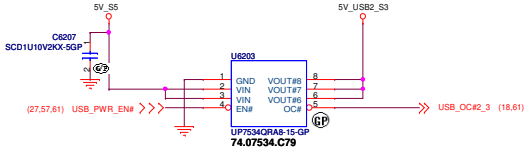
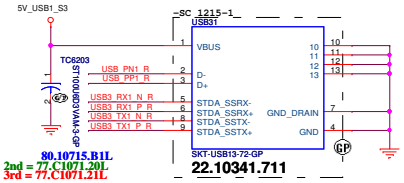
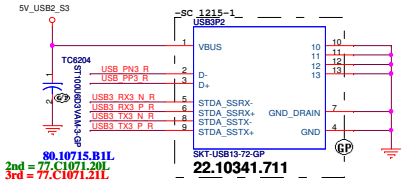
USB3.0 Port1

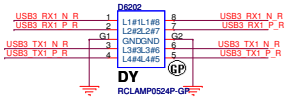


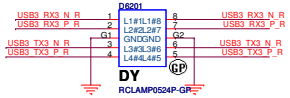
USB3.0 Port2

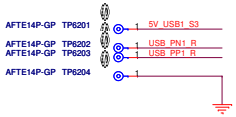


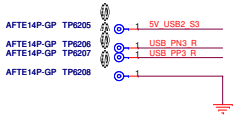


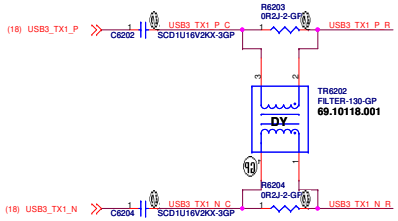


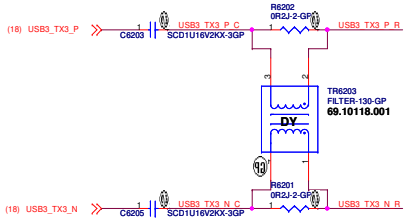


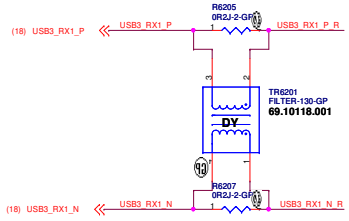


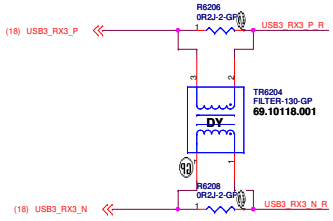


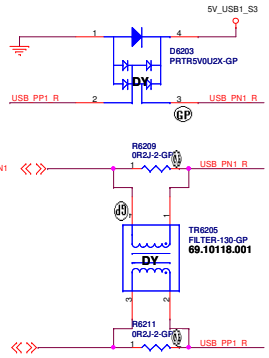


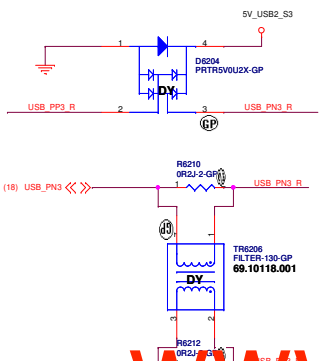












<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 3.0 Port*2

Size	Document Number	Rev
A2	LLP-1	SA

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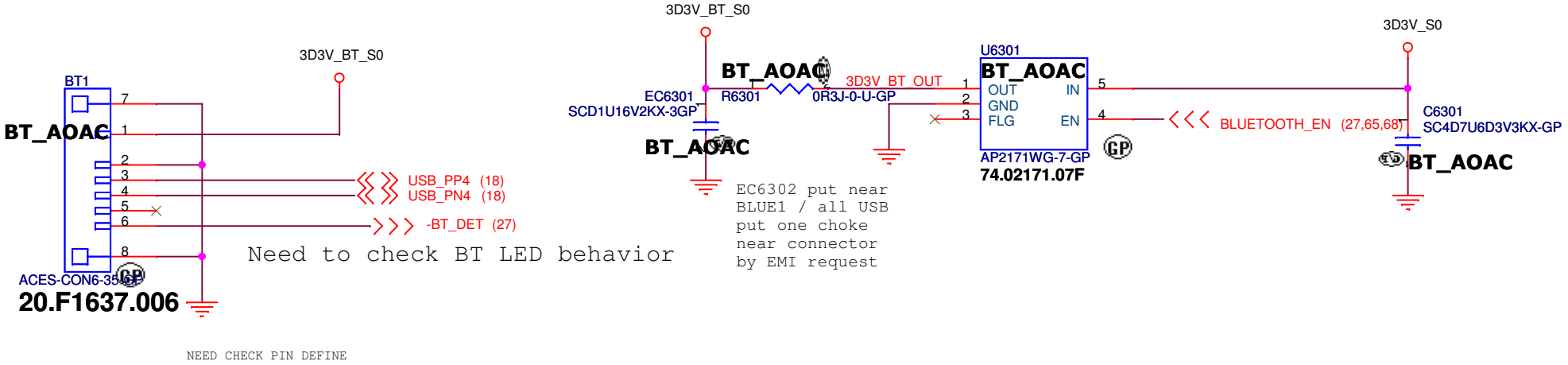
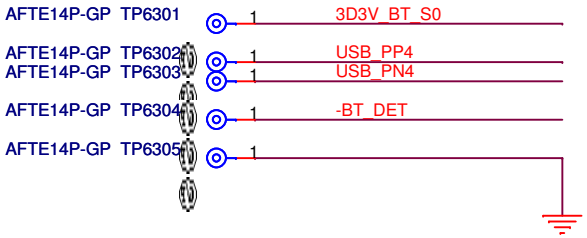
SSID = User.Interface

-SB 1013-2

Bluetooth conn.



	BT CONN.	WLAN CONN.
BT1	**ASM**	**DY**
R6301	**ASM**	**DY**
U6301	**ASM**	**DY**
C6301	**ASM**	**DY**
RN1803	**DY**	**ASM**
RN1804	**ASM**	**DY**



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

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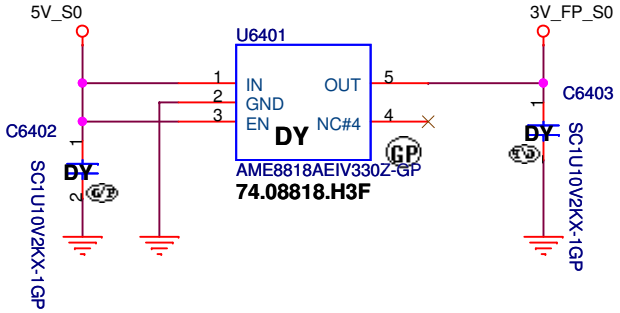
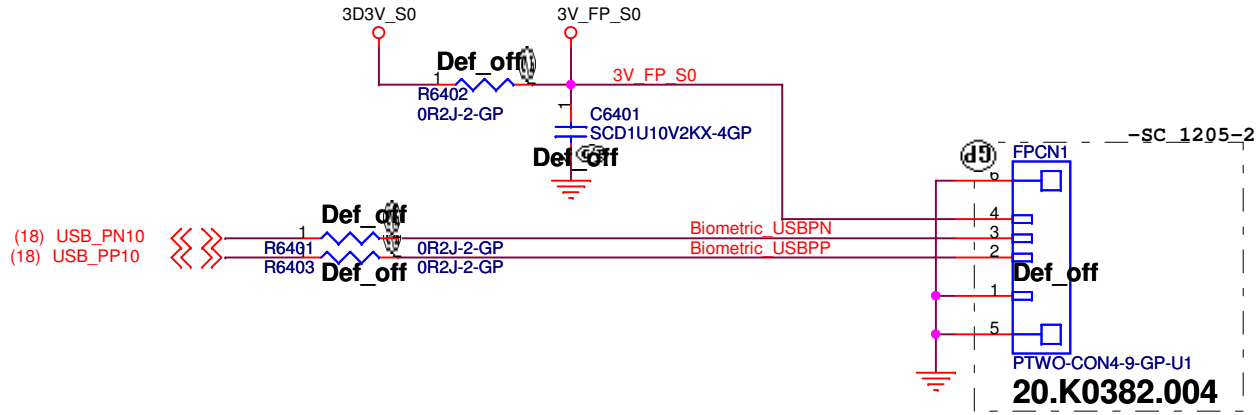
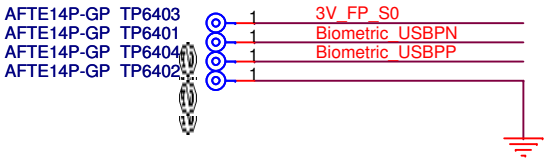
3.3V FP LDO



Finger Printer Connector





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Printer Connector*

Size	Document Number	Rev
A4	LLP-1	SA

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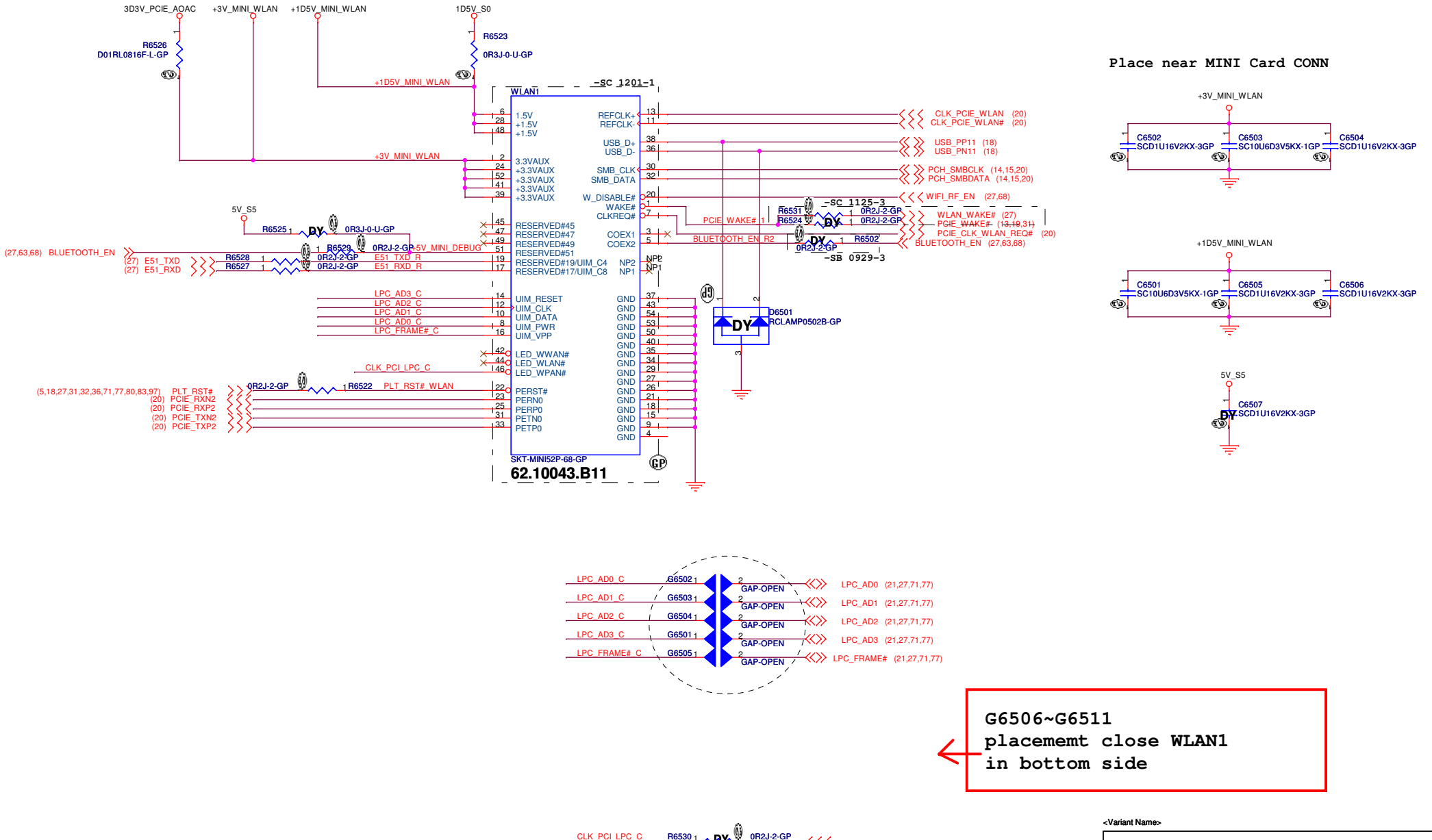
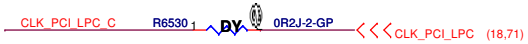
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN

G6506~G6511
placememt close WLAN1
in bottom side



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

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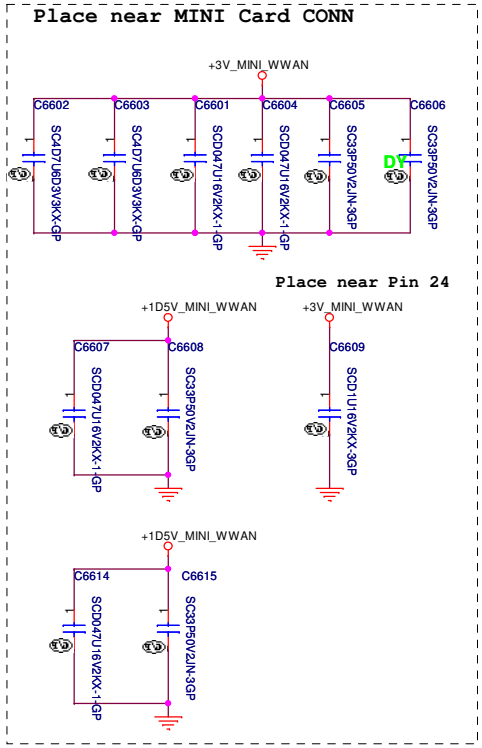
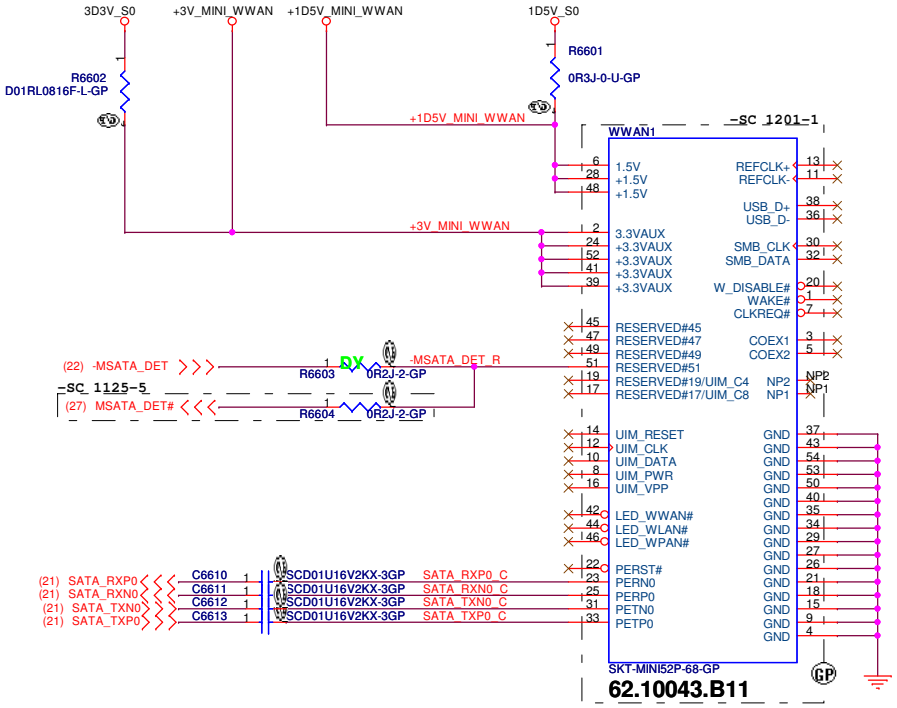
SSID = Wireless

Mini Card Connector(WWAN)





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size: A3 | Document Number: LLP-1 | Rev: SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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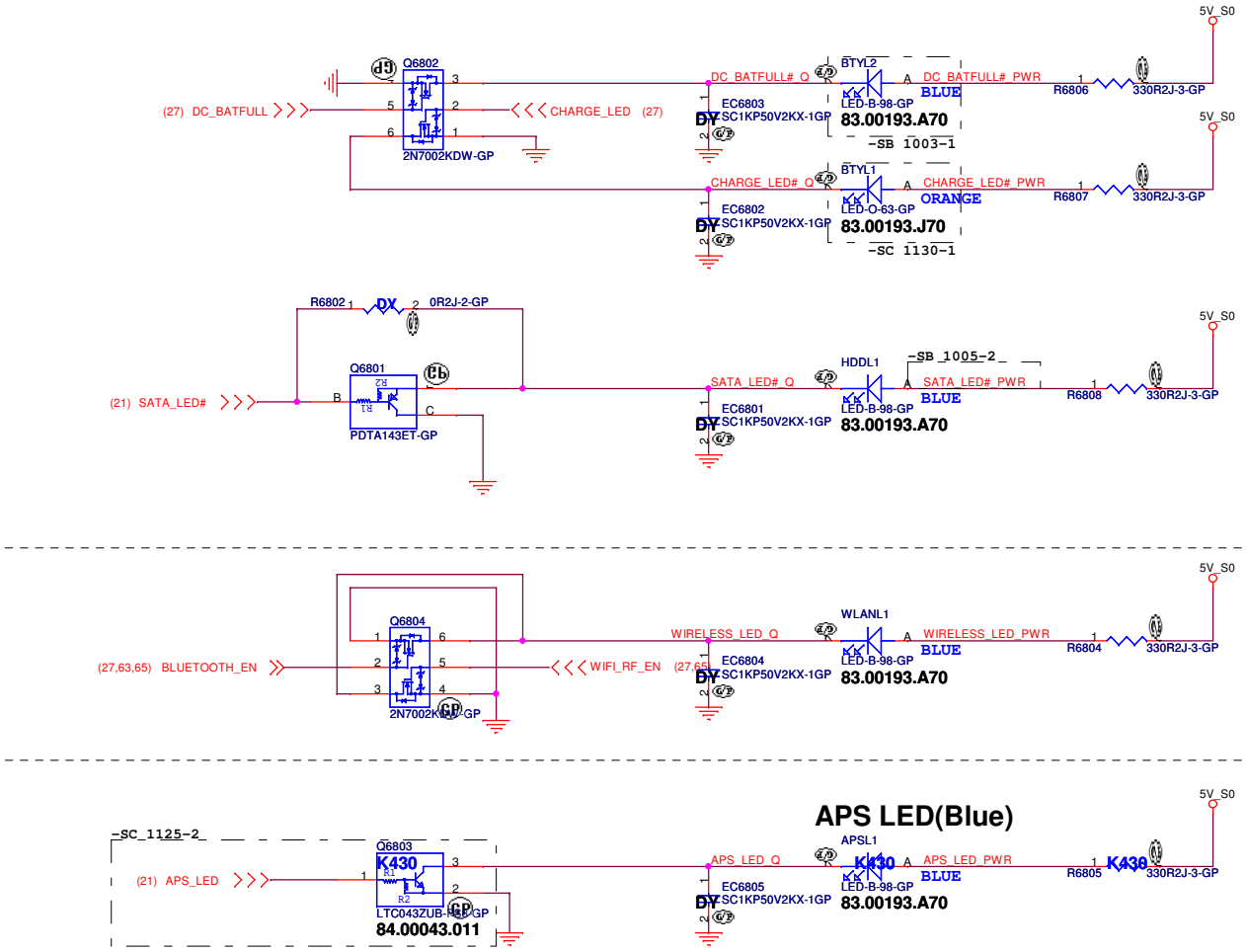
SSID = User.Interface



APS LED(Blue)

APS
LK430 : YES
LE430 : N/A
LK230 : YES

bom LA47

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LED Bard/Power Button***

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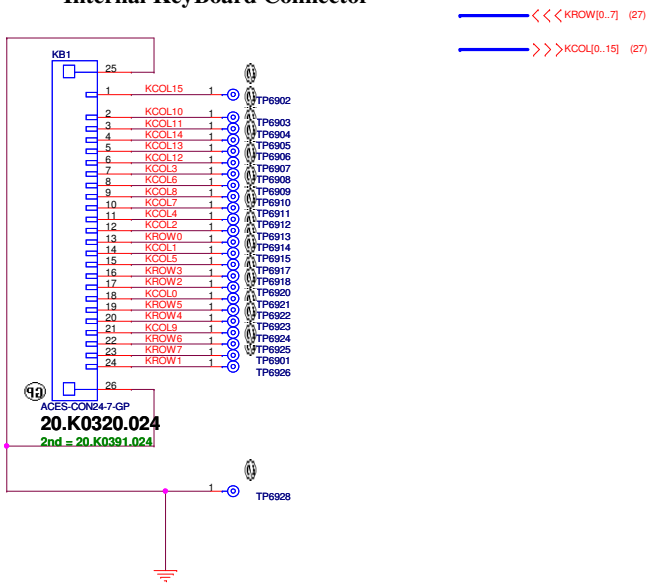
SSID = KBC

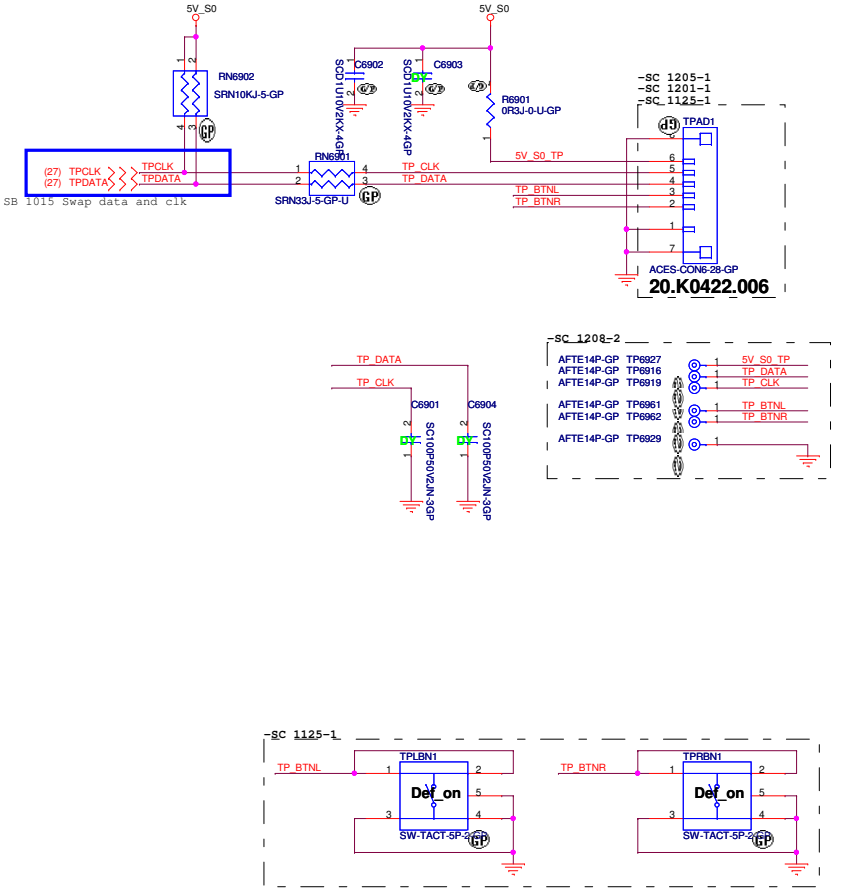
Internal KeyBoard Connector



* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	S1	S2	S3	S4	S5	S6	S7	S8

SSID = Touch.Pad



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TOUCH PAD CONNECTOR
Size: Custom	Document Number: LLP-1
Rev	SA
Date: Thursday, December 08, 2011	Sheet 69 of 105

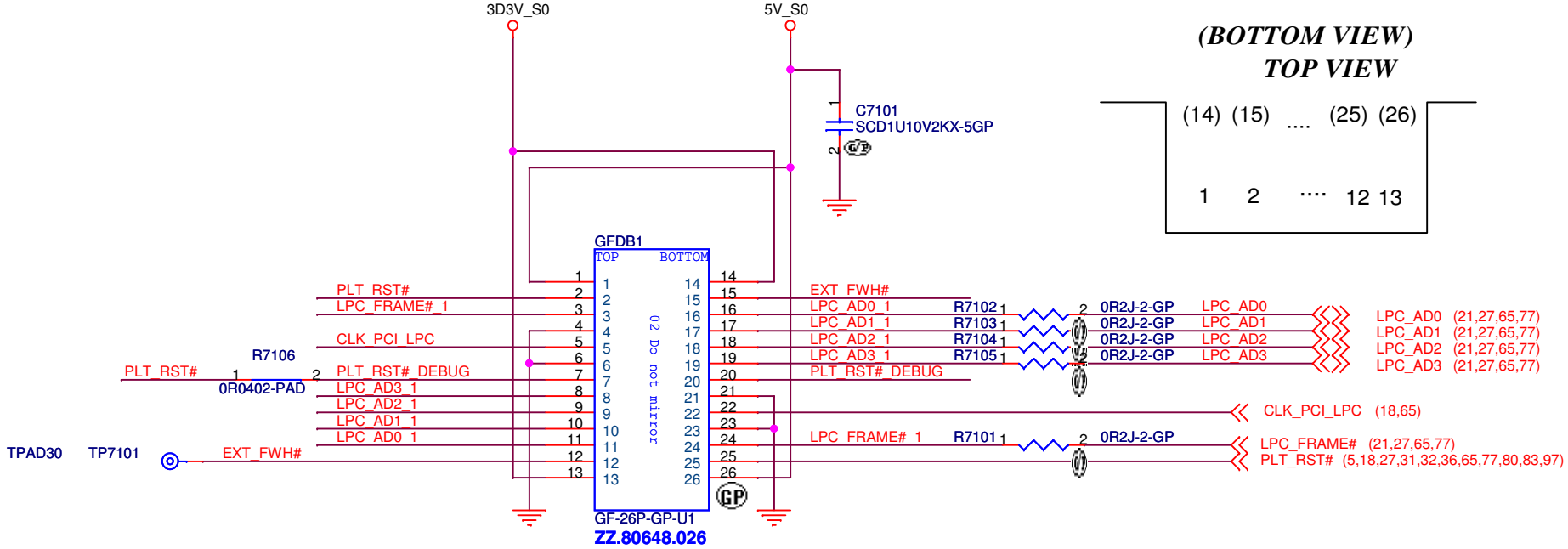
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Hall Sensor

Size	Document Number	Rev
A4	LLP-1	SA

Date: Monday, December 05, 2011 Sheet 70 of 105



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LLP-1	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A2	LLP-1	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A4	LLP-1	SA

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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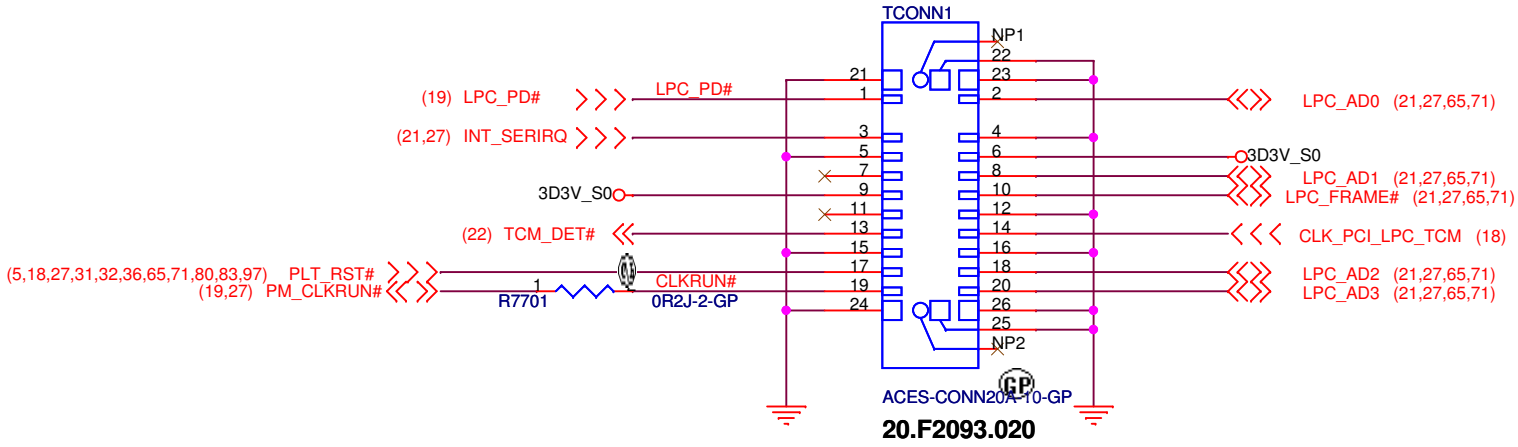
TCM
LK430 : YES
LE430 : N/A
LK230 : YES



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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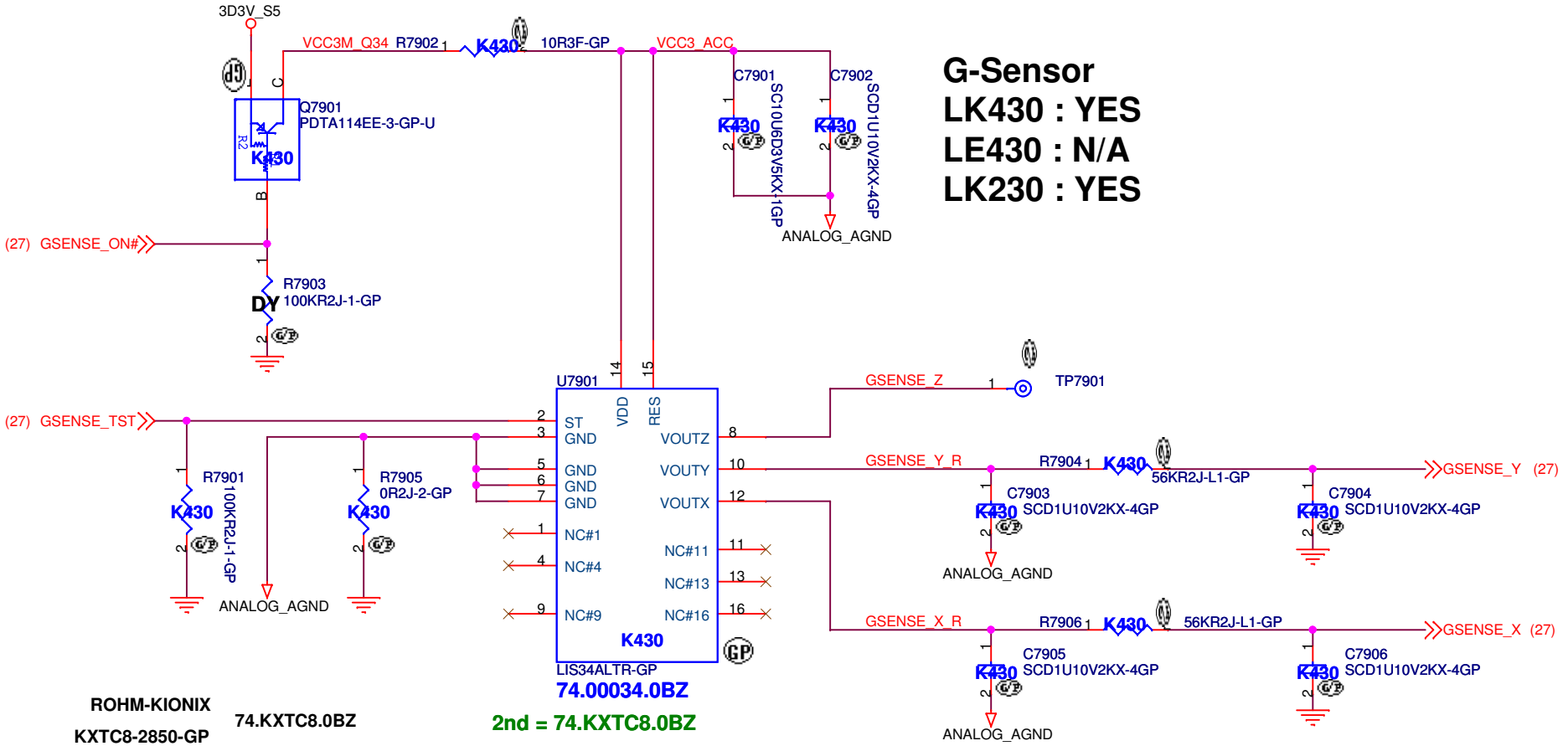
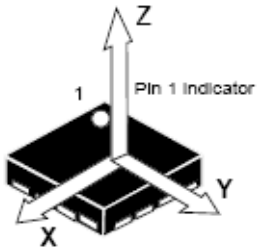


G-Sensor
LK430 : YES
LE430 : N/A
LK230 : YES

ROHM-KIONIX
KXTC8-2850-GP

74.KXTC8.0BZ

2nd = 74.KXTC8.0BZ



<Variant Name>

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G-Sensor**

Size	Document Number	Rev
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RFID

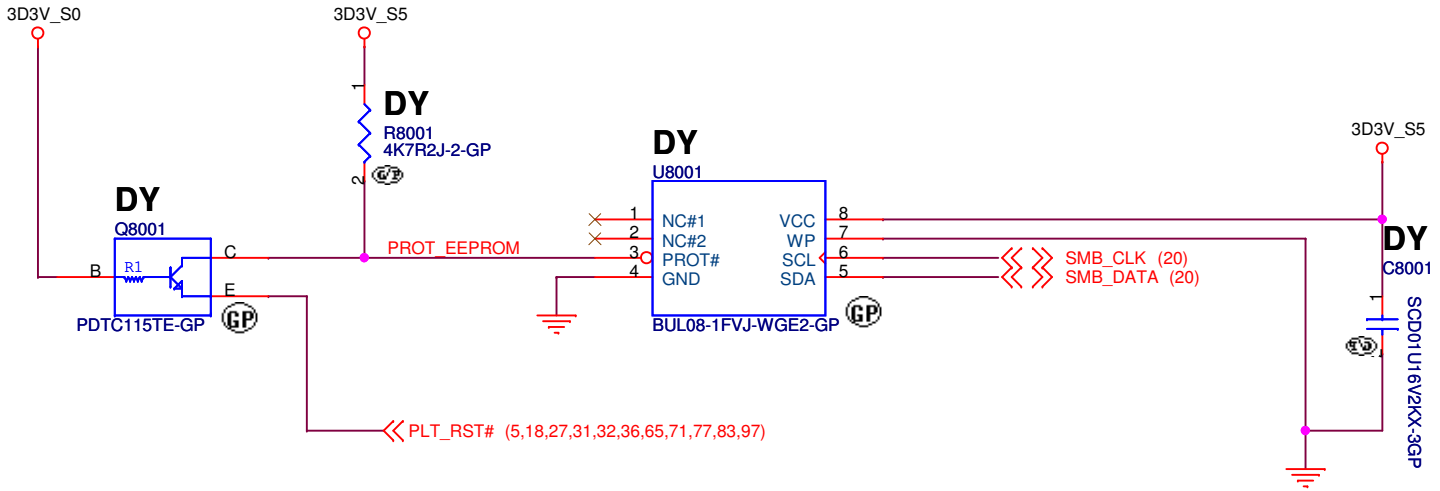

Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

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Date: Monday, December 05, 2011 Sheet 80 of 105

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<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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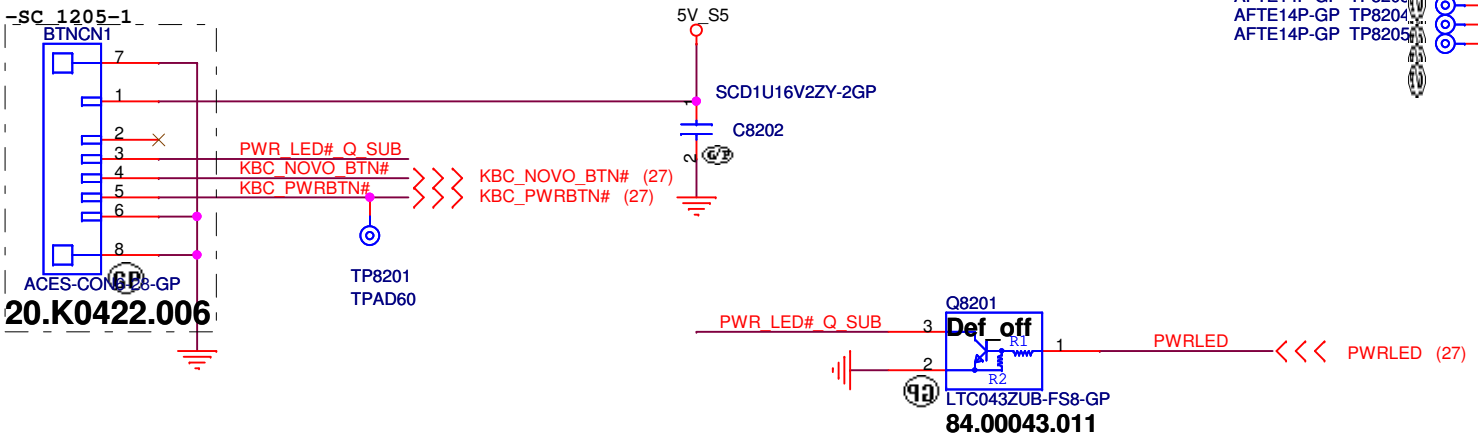
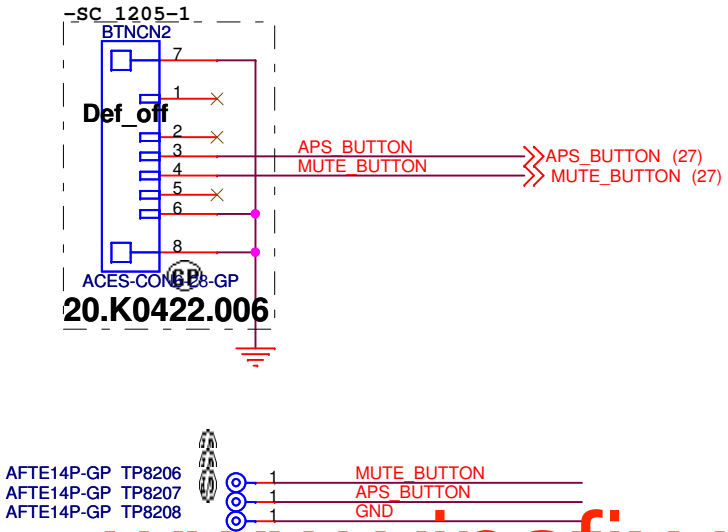
POWER BUTTON BOARD



BUTTON BOARD



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
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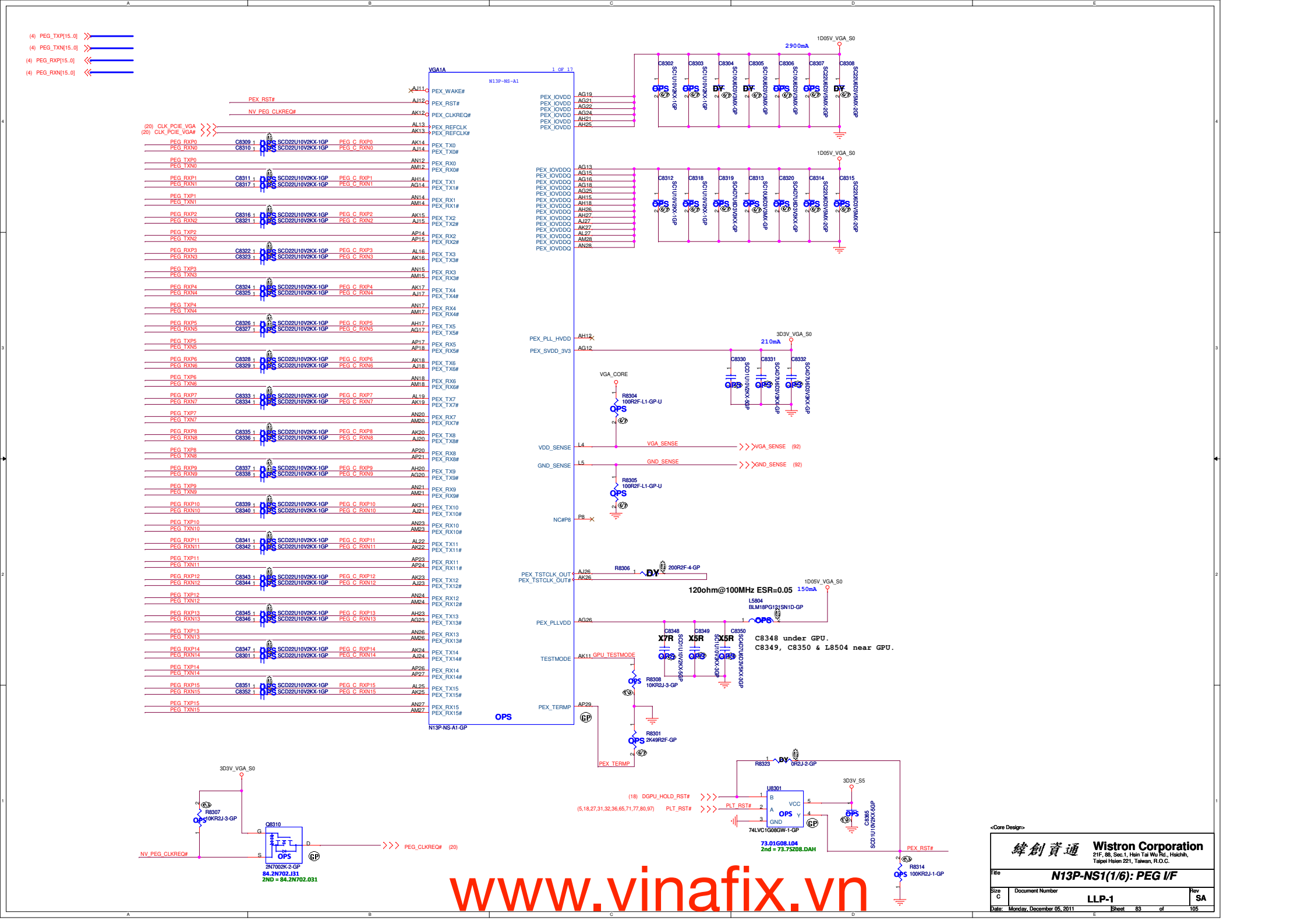

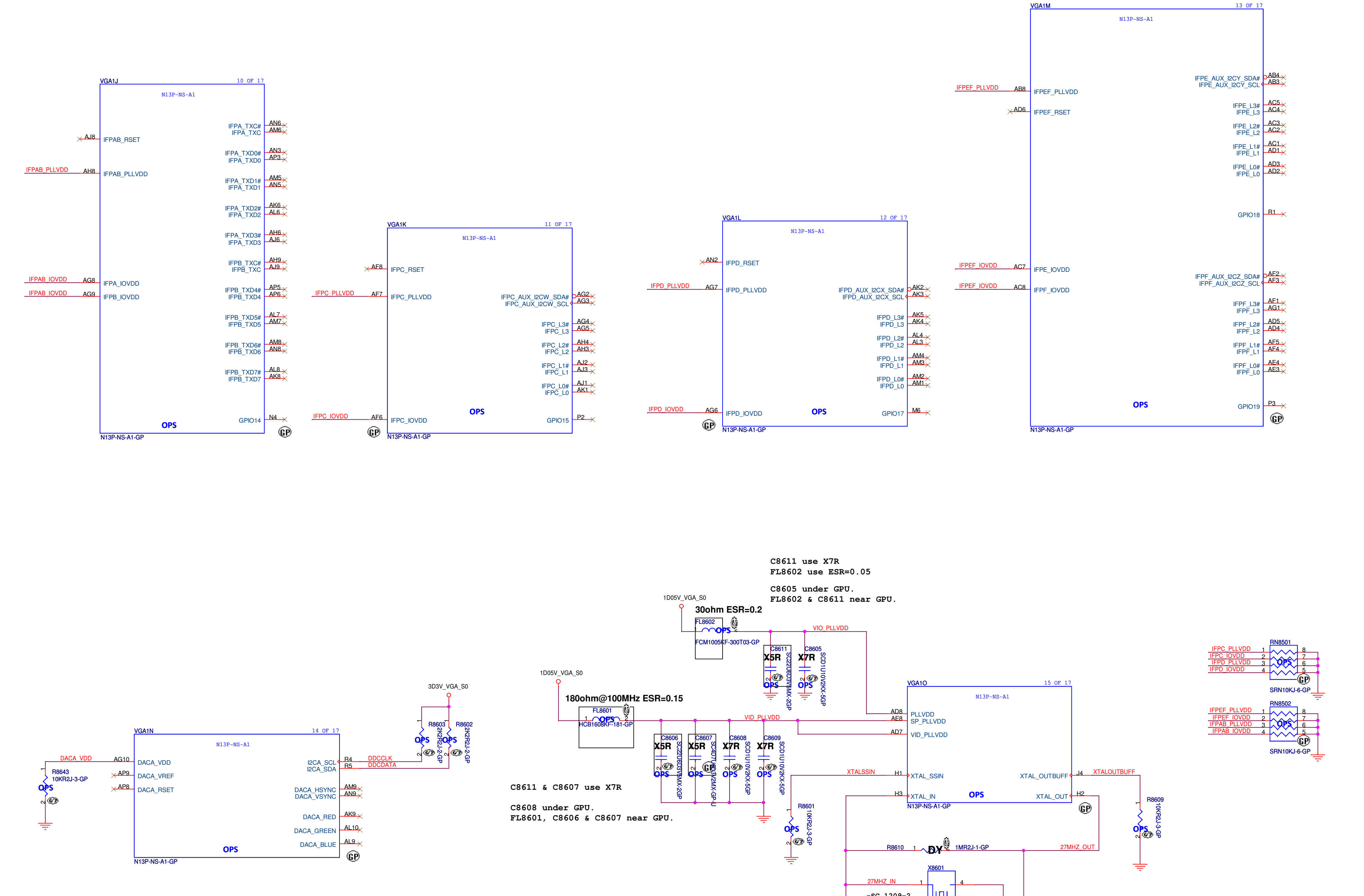

VGA1J 10 OF 17 N13P-NS-A1
VGA1K 11 OF 17 N13P-NS-A1
VGA1L 12 OF 17 N13P-NS-A1
VGA1M 13 OF 17 N13P-NS-A1
VGA1N 14 OF 17 N13P-NS-A1
VGA1O 15 OF 17 N13P-NS-A1
N13P-NS-A1-GP
IFPAB_RSET
IFPAB_PLLVDD
IFPA_IOVDD
IFPB_IOVDD
IFPC_RSET
IFPC_PLLVDD
IFPC_IOVDD
IFPD_RSET
IFPD_PLLVDD
IFPD_IOVDD
IFPEF_PLLVDD
IFPEF_RSET
IFPE_IOVDD
IFPF_IOVDD
DACA_VDD
DACA_VREF
DACA_RSET
I2CA_SCL
I2CA_SDA
DDCCLK
DDCDATA
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
PLLVDD
SP_PLLVDD
VID_PLLVDD
XTAL_SSIN
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
1D05V_VGA_S0
3D3V_VGA_S0
30ohm ESR=0.2
FL8602 FCM1005KF-300T03-GP
180ohm@100MHz ESR=0.15
FL8601 HCB1608KF-181-GP
VIO_PLLVDD
VID_PLLVDD
XTALSSIN
XTALOUTBUFF
27MHZ_IN
27MHZ_OUT
X8601 XTAL-27MHZ-122-GP
R8610 1MR2J-1-GP
C8612 SC15P50V2JN-2-GP
C8613 SC15P50V2JN-2-GP
-SC_1209-2
RN8501 SRN10KJ-6-GP
RN8502 SRN10KJ-6-GP
C8611 use X7R
FL8602 use ESR=0.05
C8605 under GPU.
FL8602 & C8611 near GPU.
C8611 & C8607 use X7R
C8608 under GPU.
FL8601, C8606 & C8607 near GPU.

Y1

TXC 7M27000149	27MHZ 8.5PF 30PPM 4P	61Y9503AA
RIVER FCX-04-27000J1421	27MHZ 8.5PF 50PPM FCX-04	61Y9503BA

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **N13P-NS1(2/6): DIGITAL OUT**

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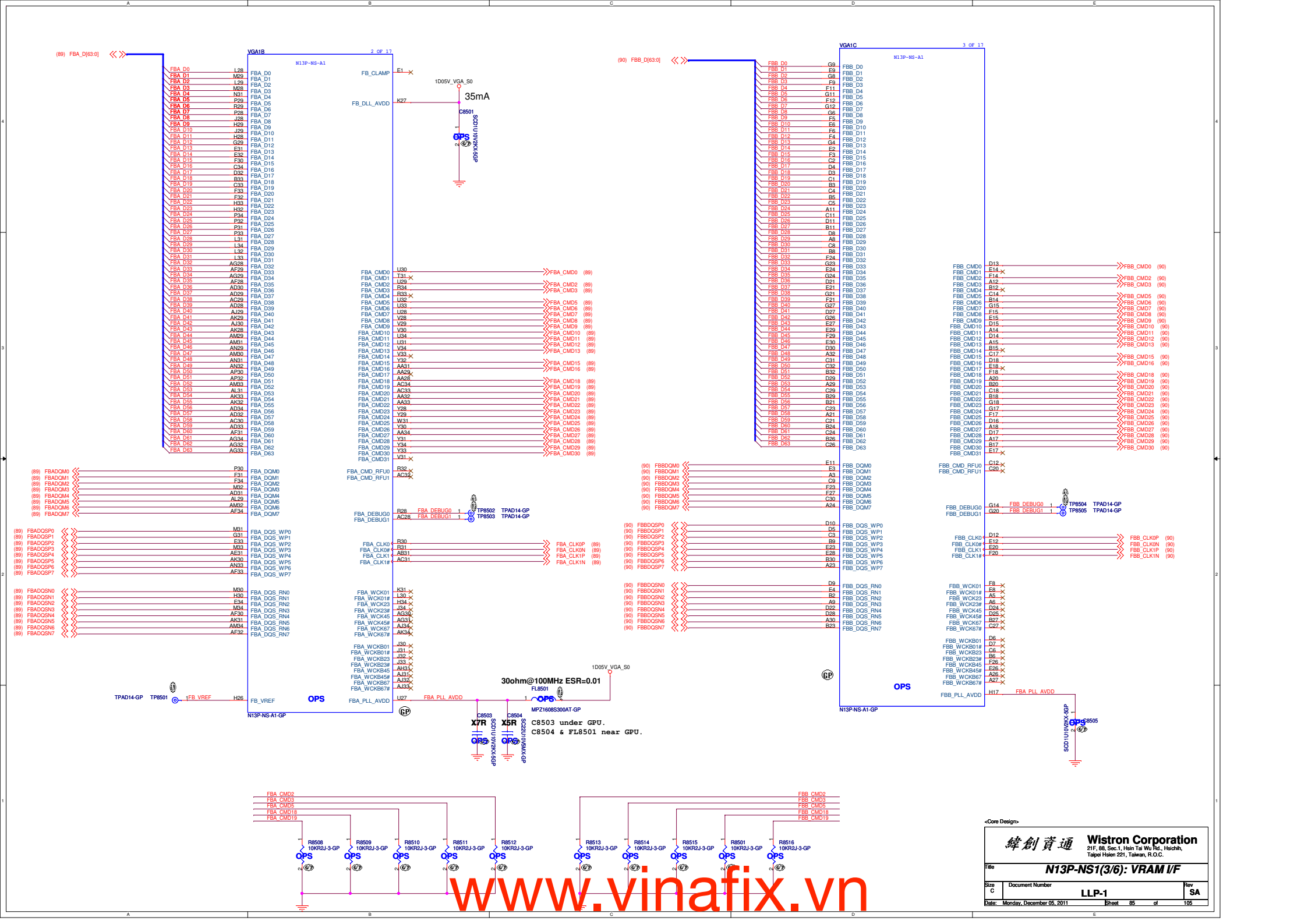

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>
Title: N13P-NS1(3/6): VRAM I/F
Size: C
Document Number: LLP-1
Rev: SA
Date: Monday, December 05, 2011
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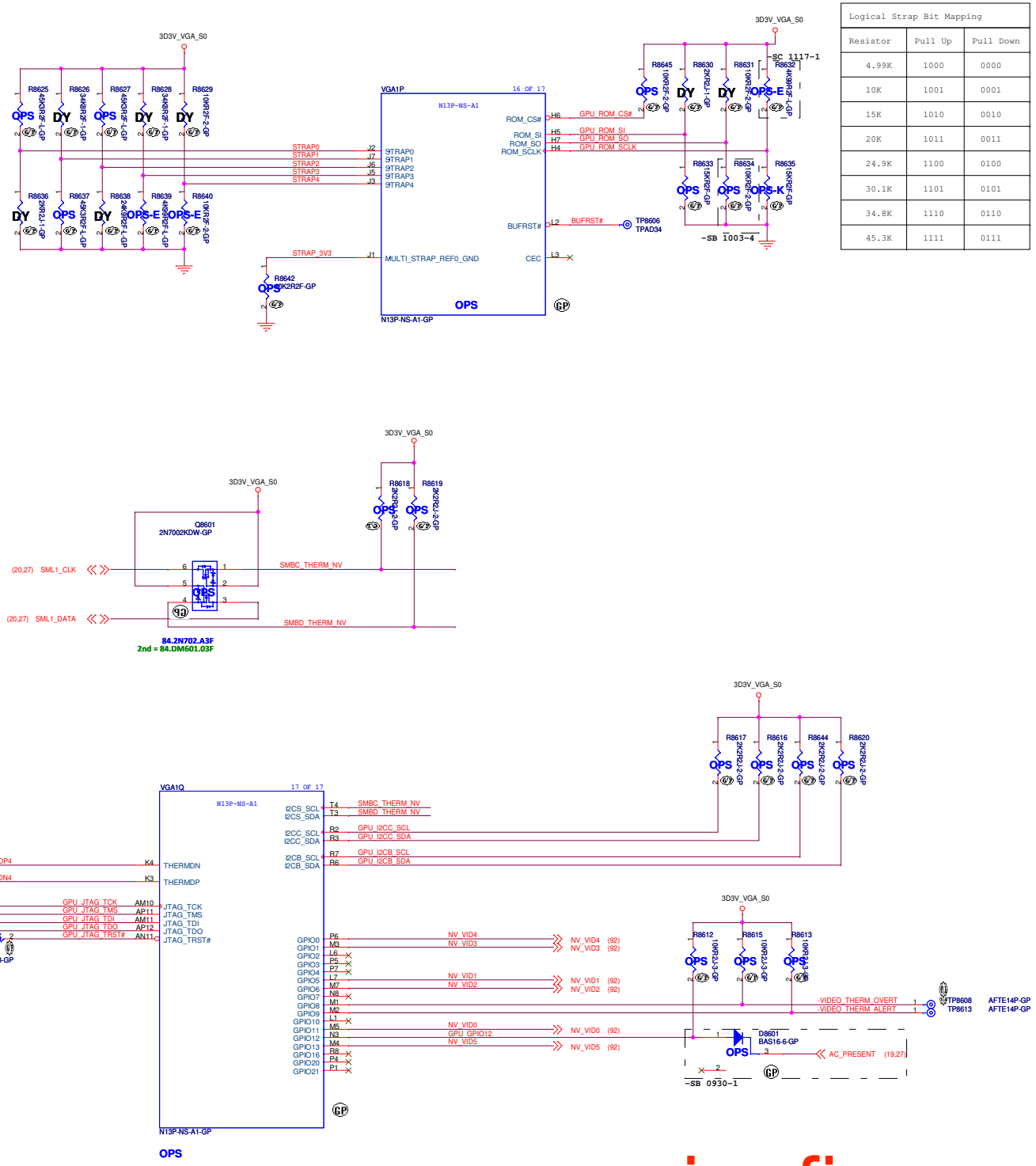

Logical Strap Bit Mapping		
Resistor	Pull Up	Pull Down
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

GPU_ROM_SI				
Type	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
Hynix (64x16) (0x2)	0	0	1	0
Samsung (64x16) (0x3)	0	0	1	1
Hynix (128x16) (0x6)	0	1	1	0
Samsung (128x16) (0x7)	0	1	1	1

GPU_ROM_SCLK				
Type	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
N13P-NS1	0	0	1	0
Type	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
N13M-GE1	1	0	0	0

GPU_ROM_SO				
Type	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
N13P-NS1	0	0	0	1
Type	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
N13M-GE1	0	1	0	1

STRAP0				
Type	USER[3]	USER[2]	USER[1]	USER[0]
EDID Panel	1	1	1	1

STRAP1				
Type	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
N13P-NS1	0	1	1	1
Type	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
N13M-GE1	0	1	1	0

STRAP2				
Type	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
N13P-NS1	1	1	1	1
Type	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
N13M-GE1	1	0	0	0

STRAP3_N13M-GE1 ONLY				
Type	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
EDID Panel	0	0	0	0

STRAP4_N13M-GE1 ONLY				
Type	Reserved	Reserved	PCIE_MAX_SPEED	DP_PLL_VDD33V
EDID Panel	0	0	0	1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(4/6): GPIO

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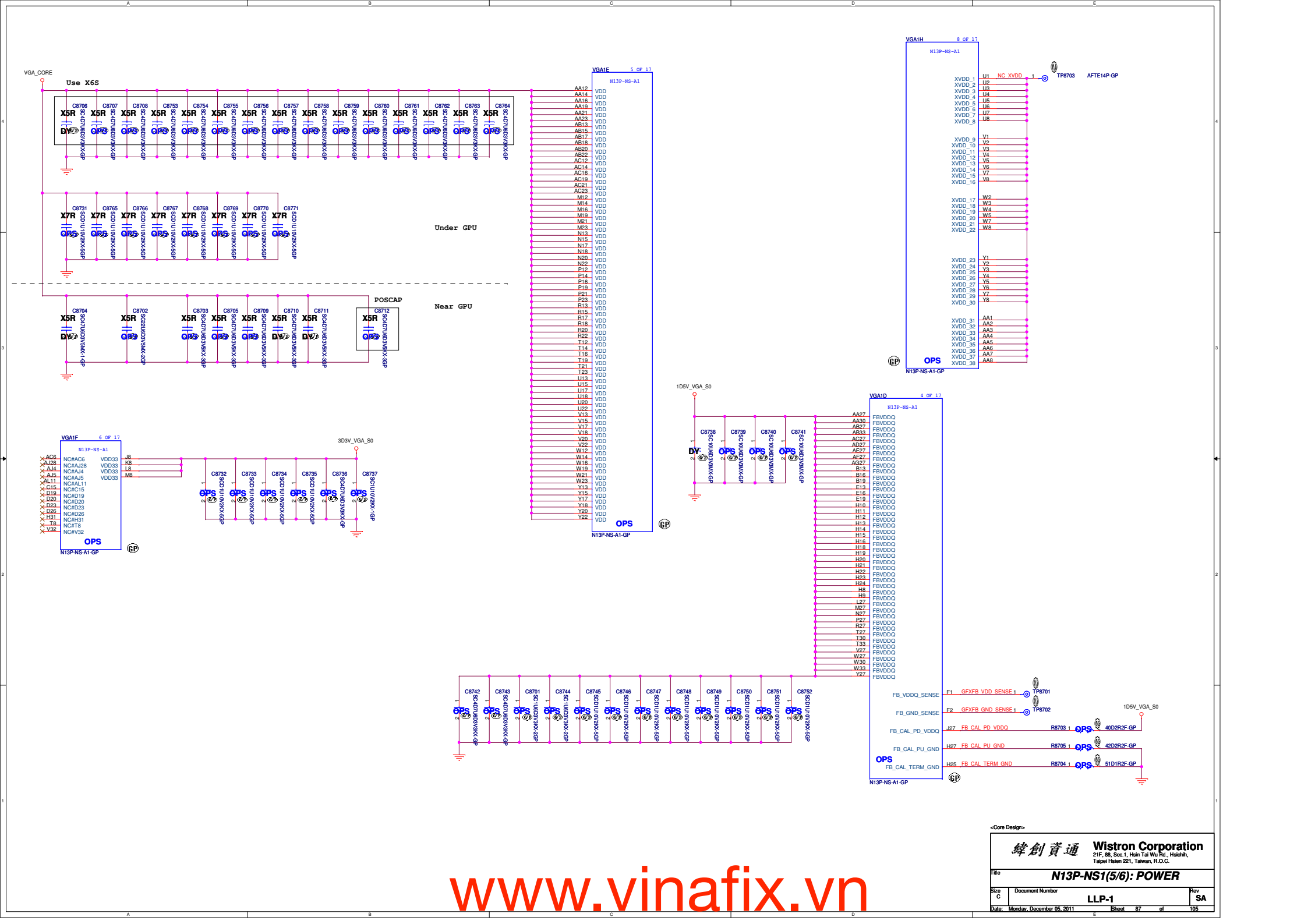

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N13P-NS1(5/6): POWER

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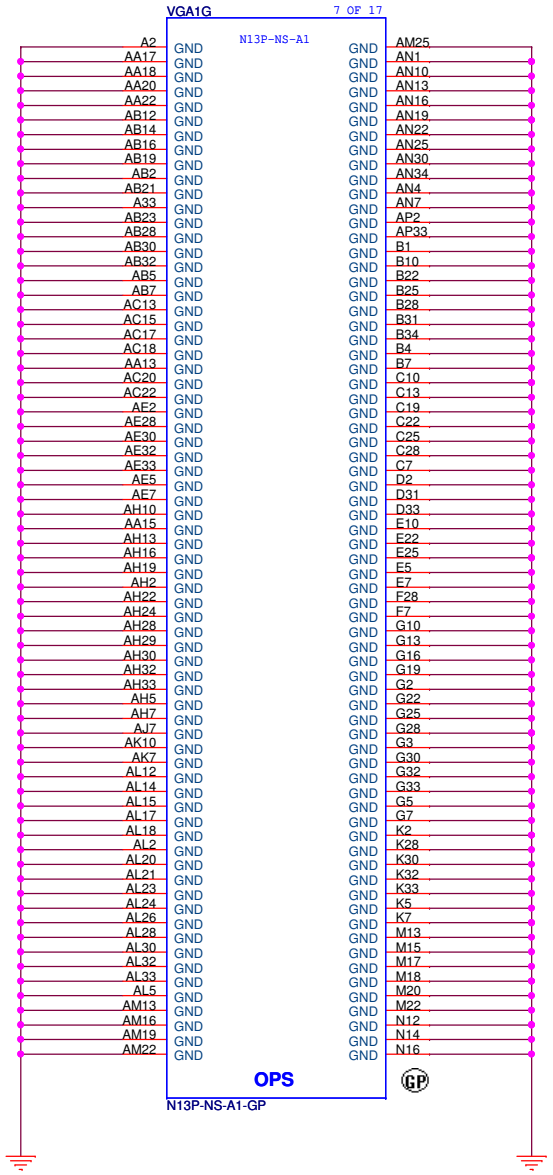

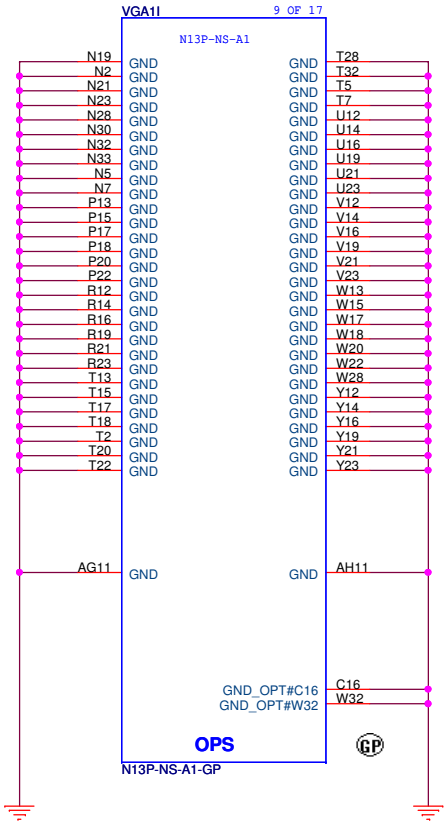

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***N13P-NS1(6/6): GND***	
Size B	Document Number **LLP-1**	Rev **SA**
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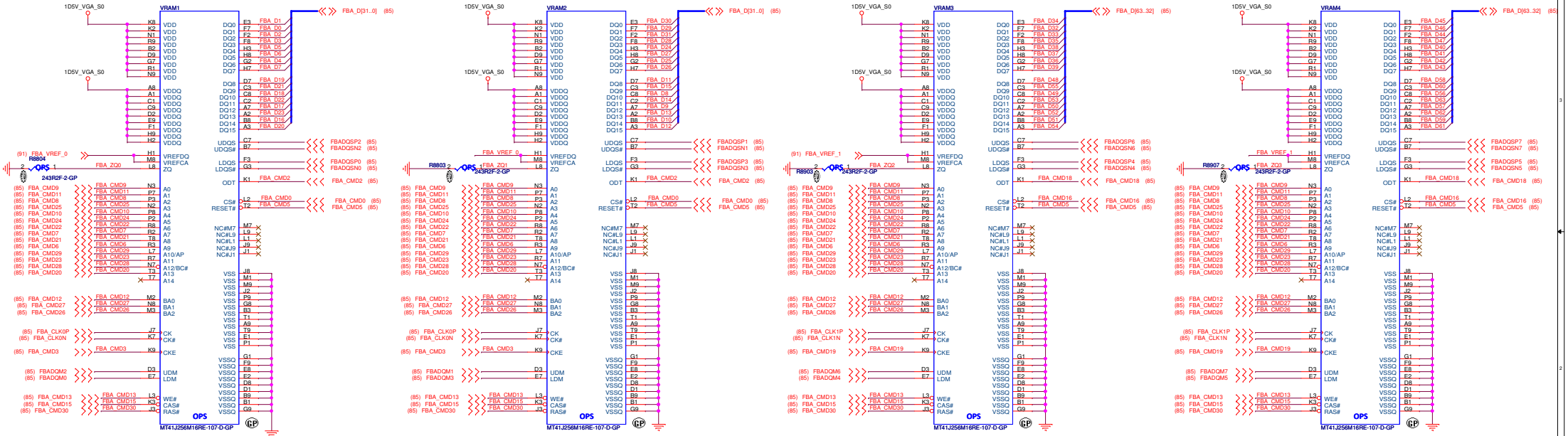
TABLE
DDR3 VIDEO MEMORY

	HYNIX 1GBITS (64Mx16)	SAMSUNG 1GBITS (64Mx16)
U100 U111 U99 U108 U107 U110 U105 U109	H5TQ1G63DFR-11C	K4W1G1646G-BC11

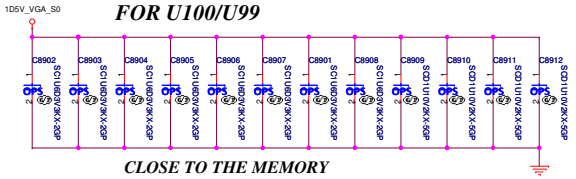
LOGIC

FB CMD mapping Mode D-N12x

Use Micron MT41J256M16RE-107-D for Layout placement

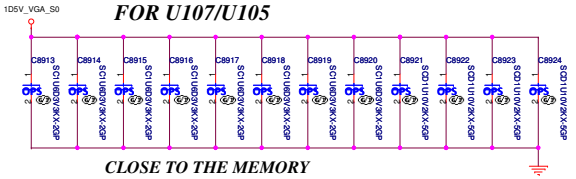


FOR U100/U99



CLOSE TO THE MEMORY

FOR U107/U105



CLOSE TO THE MEMORY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A

Size: Custom | Document Number: LLP-1 | Rev: SA

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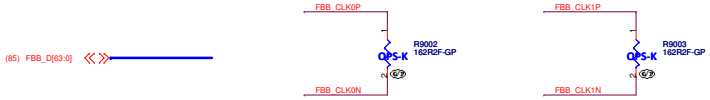
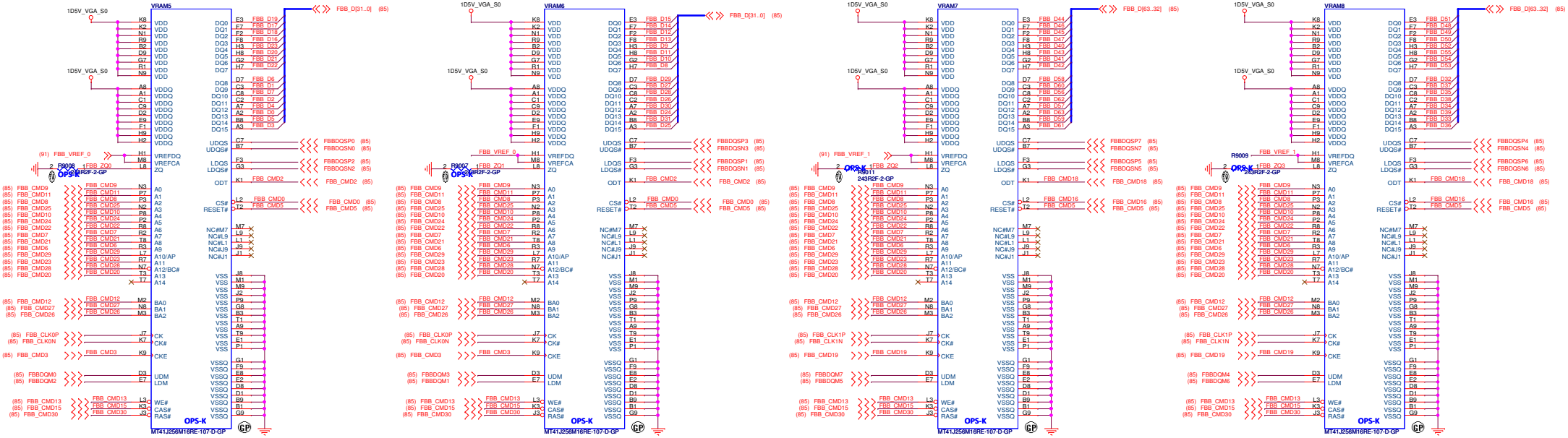
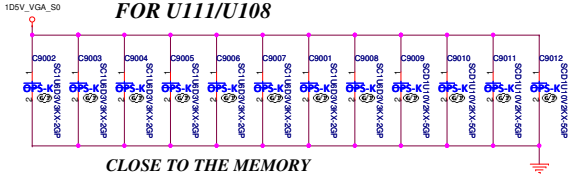


FB CMD mapping Mode D-N12x

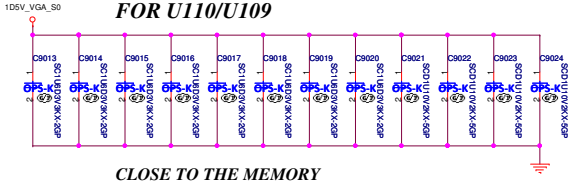


FOR U111/U108



CLOSE TO THE MEMORY

FOR U110/U109



CLOSE TO THE MEMORY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-B

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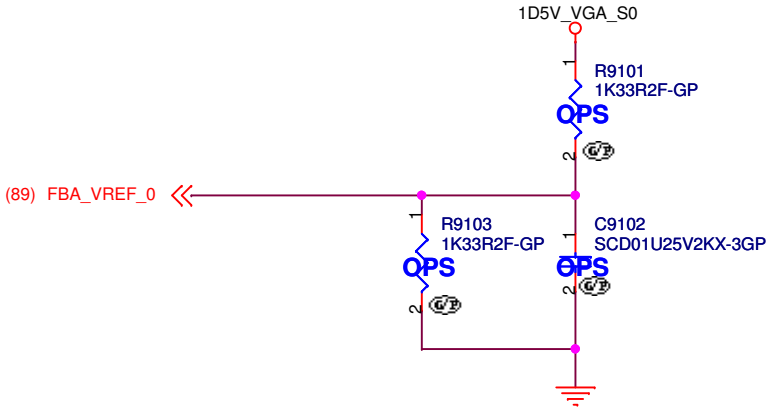

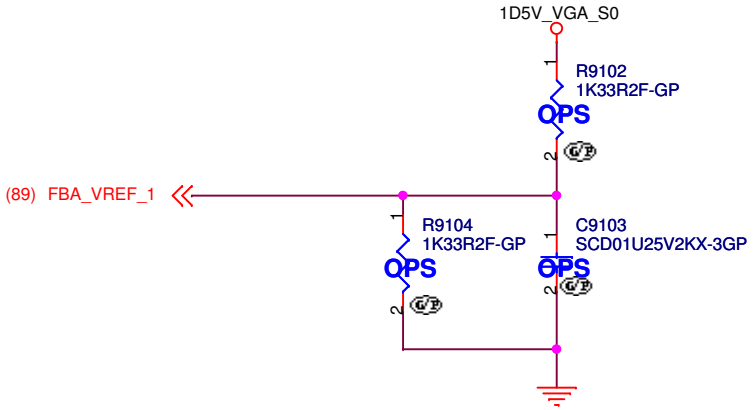

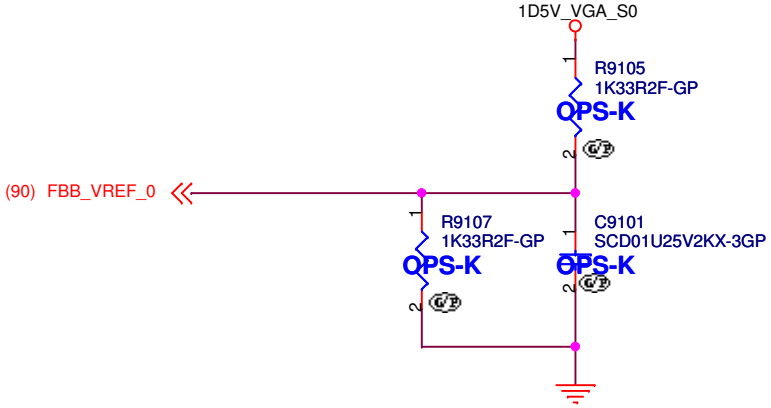

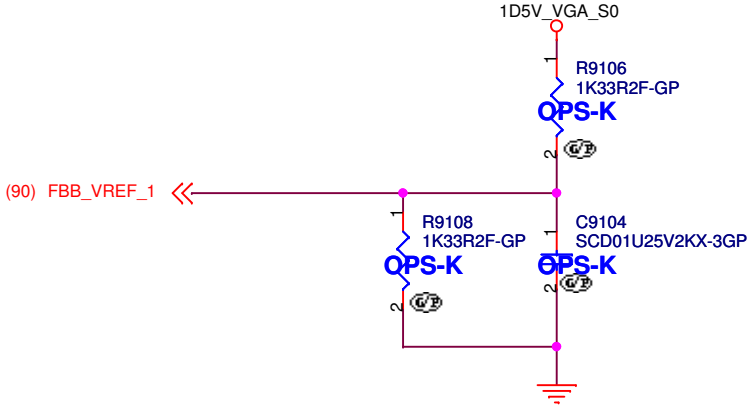

<Core Design>

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Title ***VIDEO MEMORY TERMINATION***

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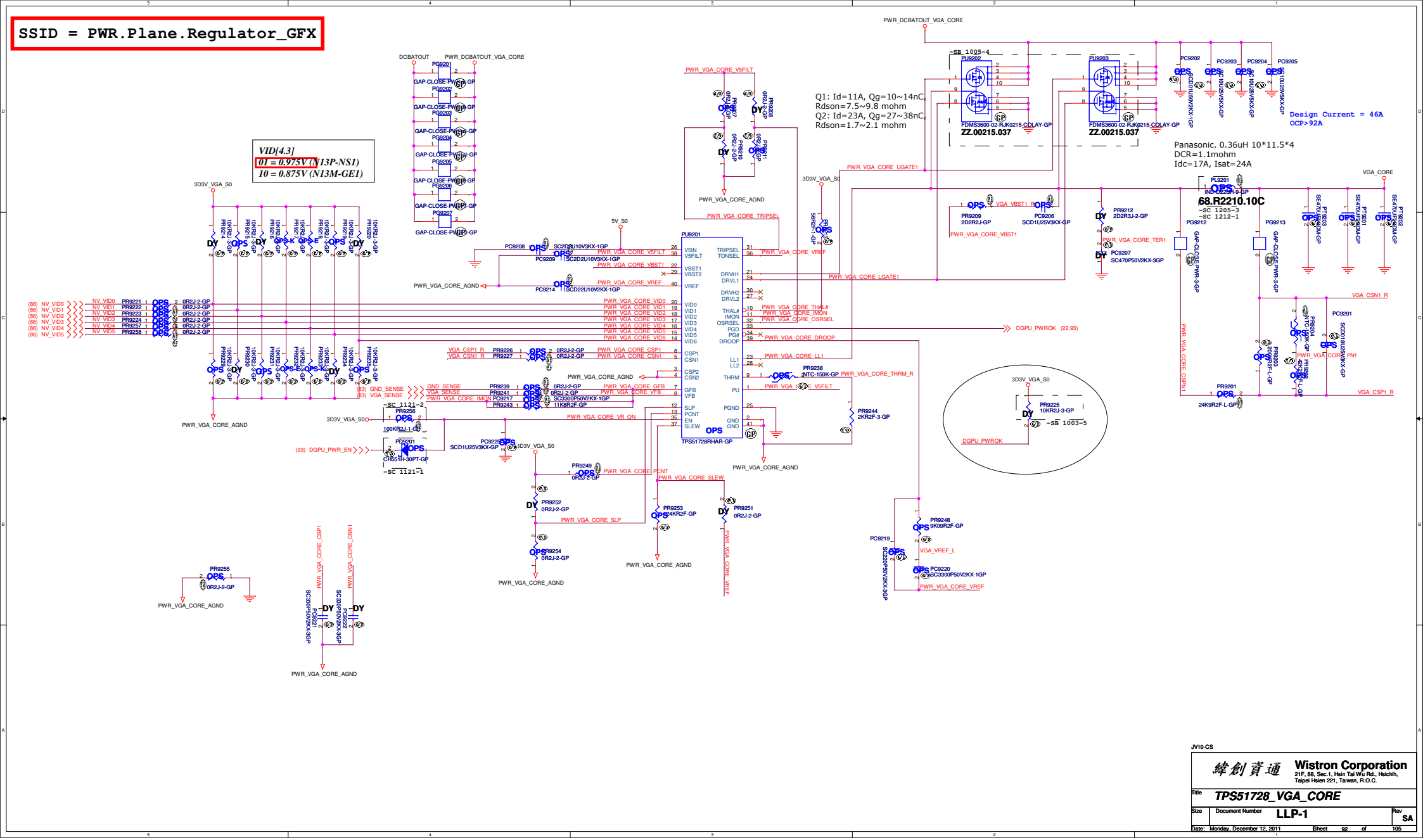
SSID = PWR.Plane.Regulator_GFX



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51728_VGA_CORE		
Size	Document Number: LLP-1	Rev: SA
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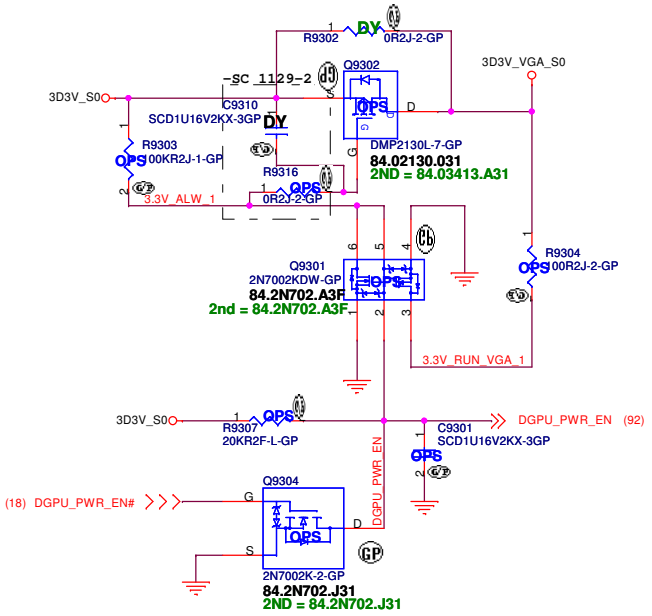
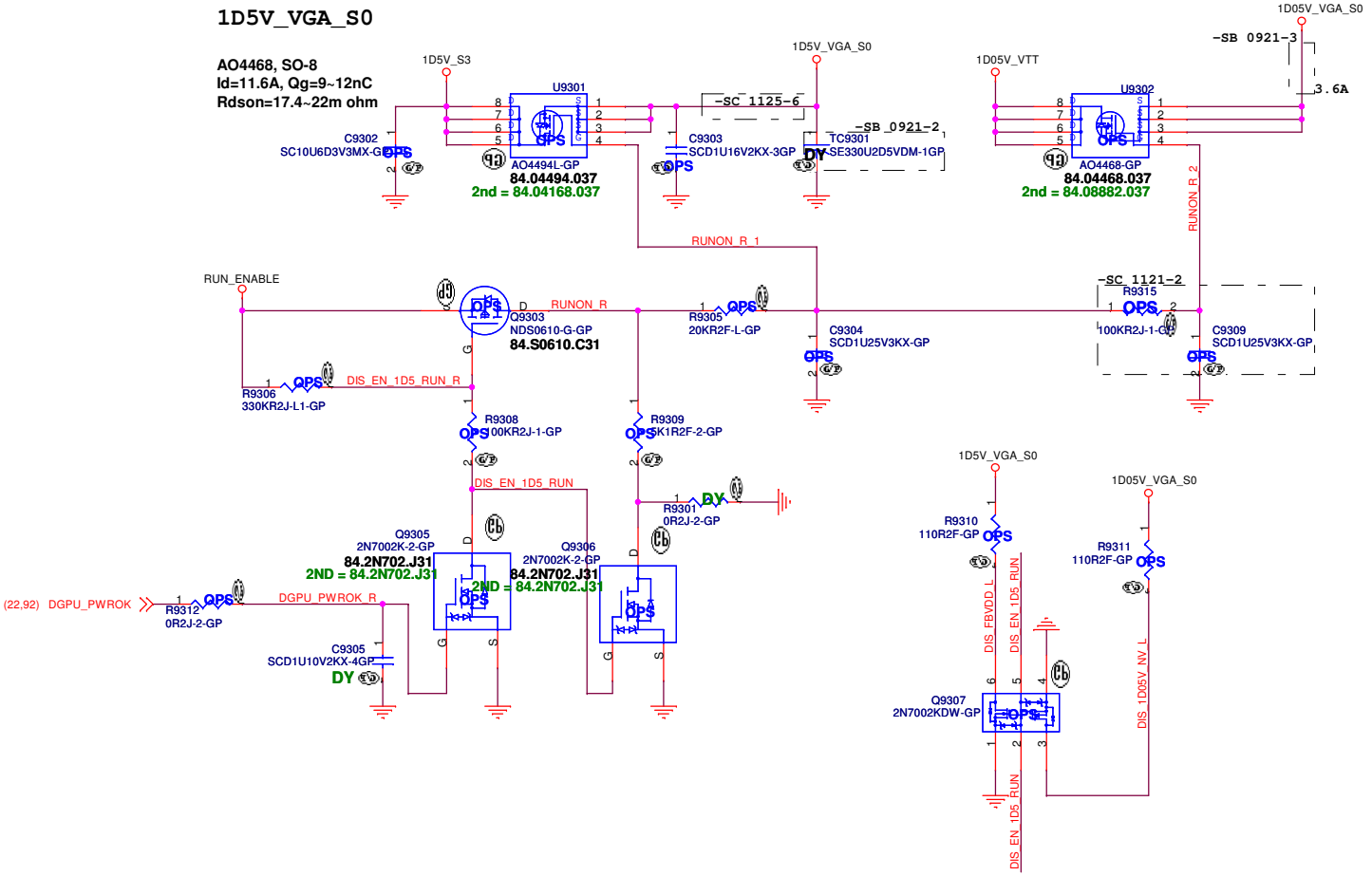
+3VS to 3.3V_DELAY Transfer

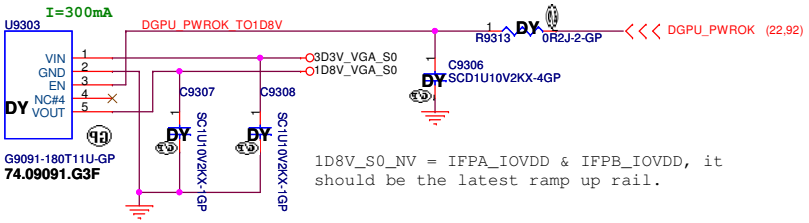


1D5V_VGA_S0

AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISCRETE VGA POWER		
Size: A3	Document Number: LLP-1	Rev: SA
Date: Tuesday, December 06, 2011	Sheet 93 of 105	

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<Variant Name>

緯創資通
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Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LLP-1	Rev: SA
Date: Monday, December 05, 2011	Sheet 94 of 105	

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<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***TOUCH PANEL***

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CPU boss

H4 HOLE256R142-GP ZZ.00PAD.801
H5 HOLE256R142-GP ZZ.00PAD.801
H6 HOLE256R142-GP ZZ.00PAD.801
H7 HOLE256R142-GP ZZ.00PAD.801

VGA boss

H1 HOLE256R142-GP ZZ.00PAD.801
H2 HOLE256R142-GP ZZ.00PAD.801
H3 HOLE256R142-GP ZZ.00PAD.801

TCM STD-OFF

H8 STF217R115H121-GP 34.4Y801.011
H9 STF217R115H121-GP 34.4Y801.011
-SC 1208-1

Mini PCI STD-OFF -SC 1128-1

H10 STF256R117H119-GP 34.4B502.001 HALF
H12 STF256R117H119-GP 34.4B502.001 LONG
H11 STF256R105H158-GP 34.4TJ01.001
H13 STF256R105H158-GP 34.4TJ01.001

Check test point

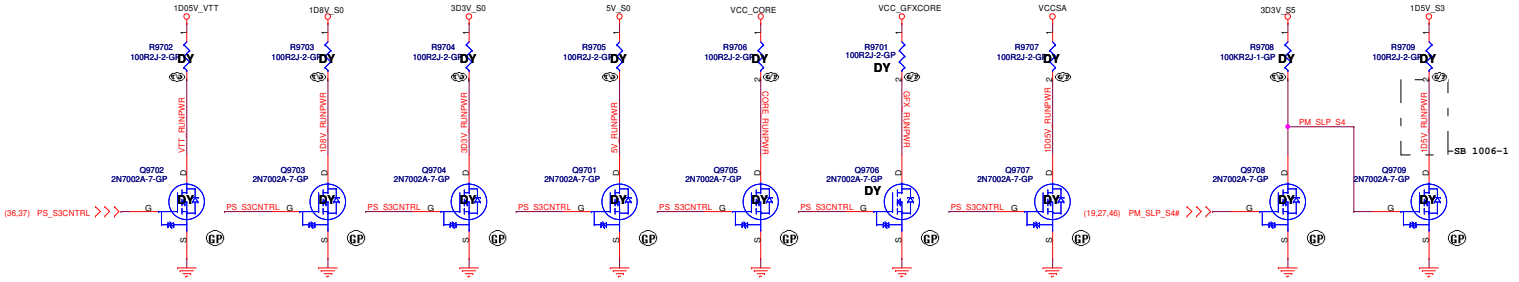
3D3V_S0		TP9702
3D3V_AUX_S5		TP9703
3D3V_S5		TP9704
5V_S5		TP9705
(19,27) PM_PWRBTN#		TP9706
(5,22) H_CPUPWRGD		TP9701
(27,36) S5_ENABLE		TP9707
(5,18,27,31,32,36,65,71,77,80,83) PLT_RST#		TP9708

Test Point放在Dimm Door打開可量測處

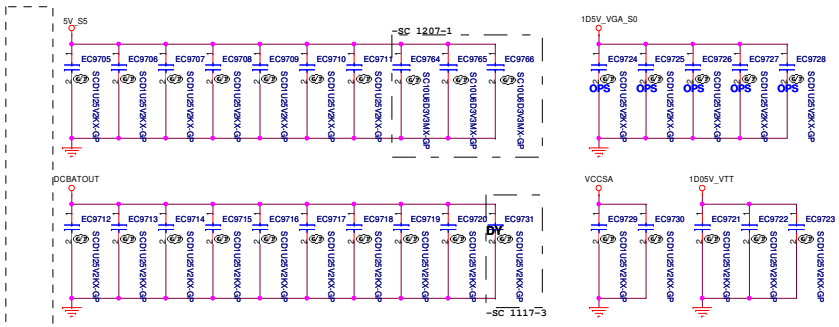
Structure boss

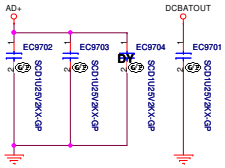
H14 HOLE315X315R91-S1-GP ZZ.00PAD.581
H15 HOLE315X315R91-S1-GP ZZ.00PAD.581
H16 HOLE315X315R91-S1-GP ZZ.00PAD.581
H17 HOLE315X315R91-S1-GP ZZ.00PAD.581
H18 HOLE315X315R91-S1-GP ZZ.00PAD.581
H19 HOLE237R95-GP ZZ.00PAD.921
H20 HOLE237R95-GP ZZ.00PAD.921
H21 HOLE237R95-GP ZZ.00PAD.921
H22 HOLE237R95-GP ZZ.00PAD.921
H23 HOLE237R95-GP ZZ.00PAD.921
H24 HOLE237R95-GP ZZ.00PAD.921

For Discharge

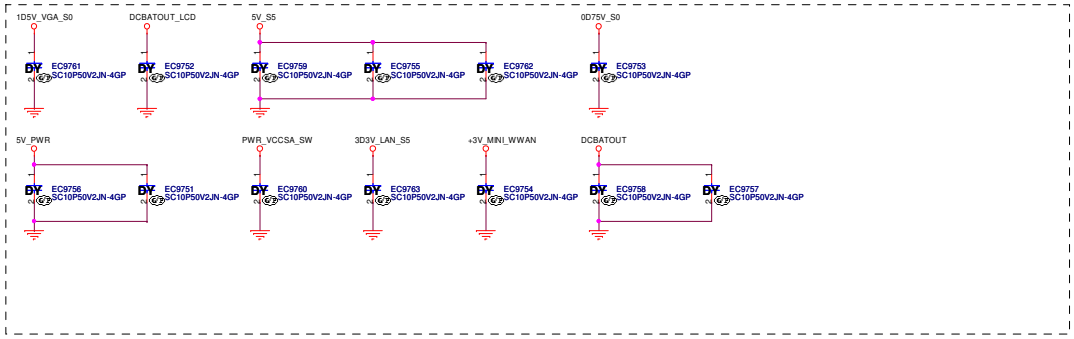


EMI





RF -SB 0928-2



<Variant Name>

緯創資通 Wistron Corporation
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Title: UNUSED PARTS/EMI Capacitors
Size: A2 | Document Number: LLP-1 | Rev: SA
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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Change History***

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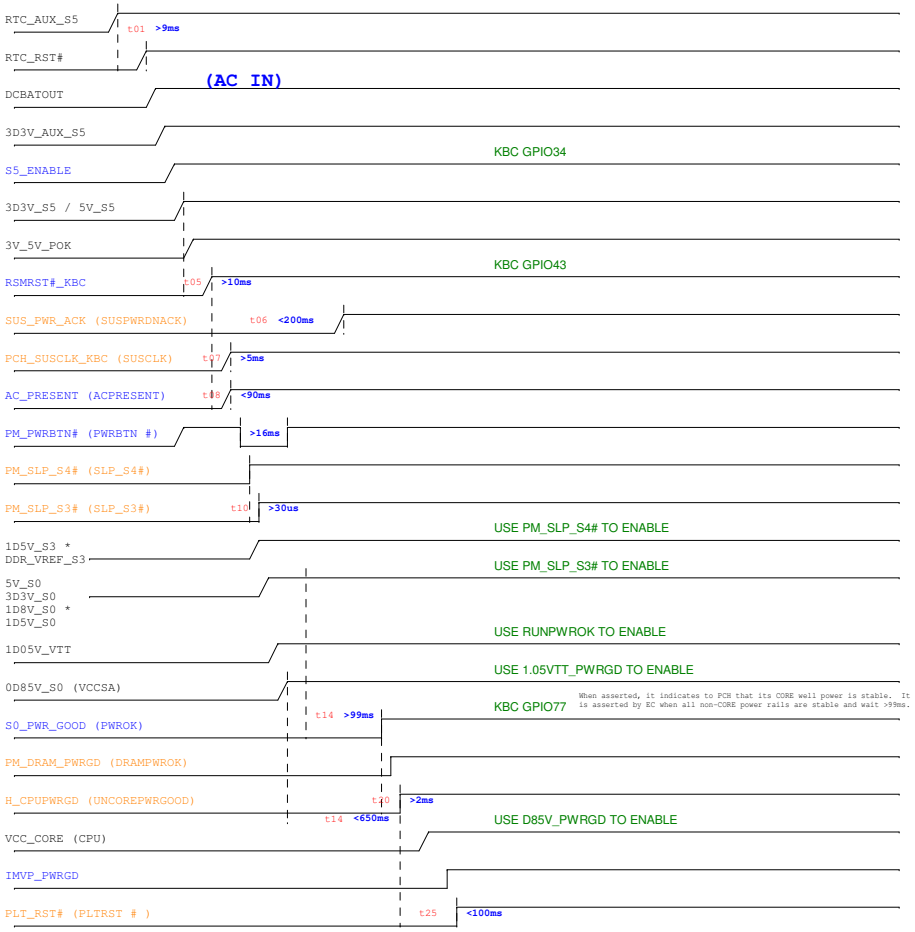
(AC mode)

red word: KBC GPIO
red word: PCH / CPU



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緯創資通	**Wistron Corporation** 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title	<Title>
Size: A2	Document Number: LLP-1
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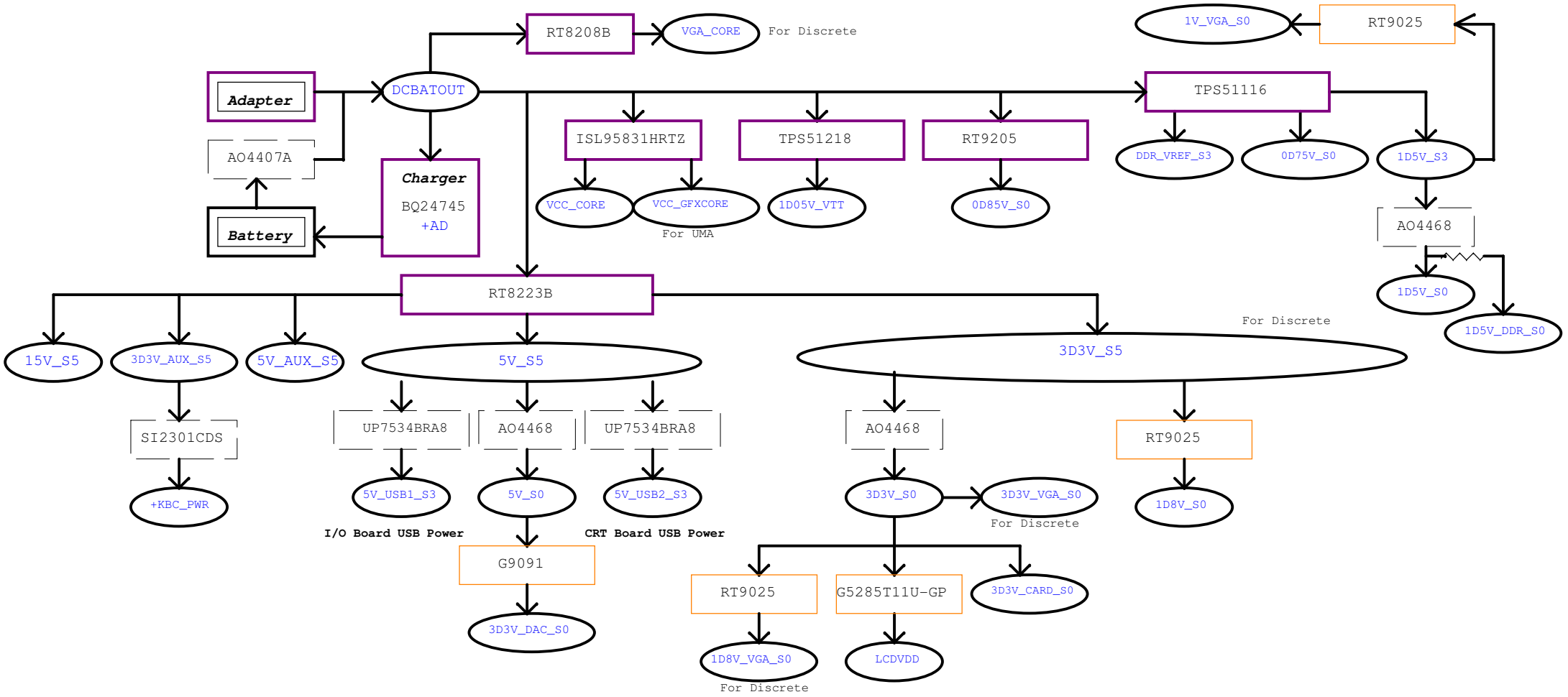

Power Shape

Regulator	LDO	Switch

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***Power Block Diagram***

Size	Document Number	Rev
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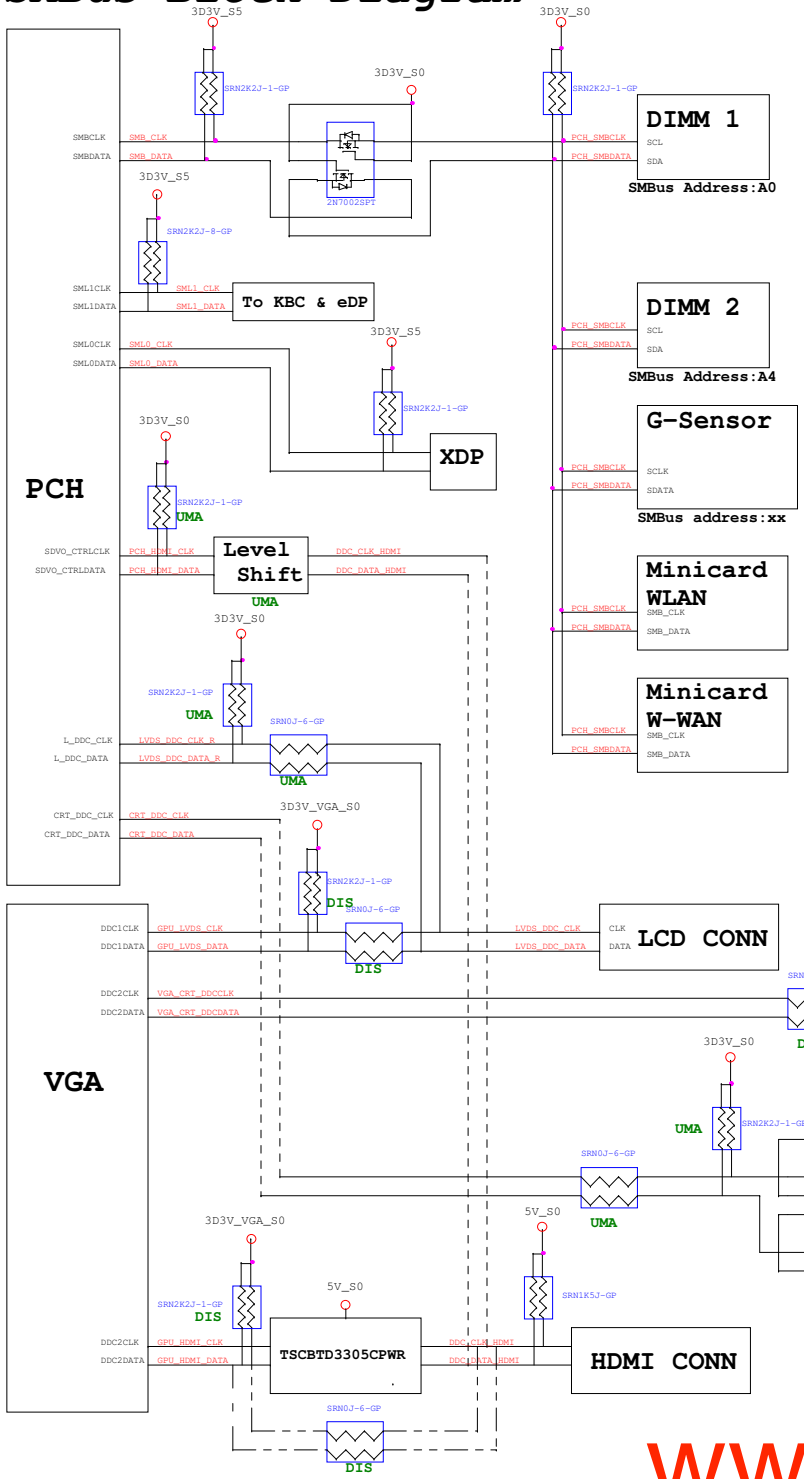
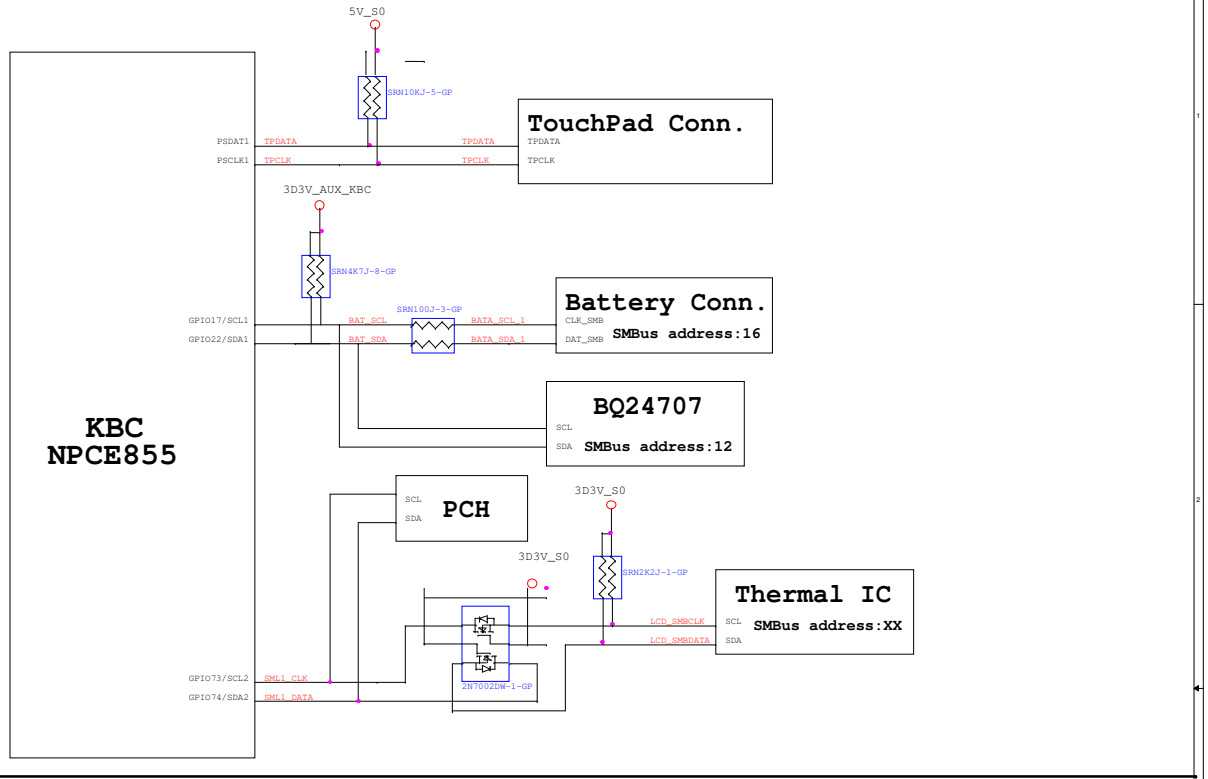
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

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Title: SMBUS Block Diagram

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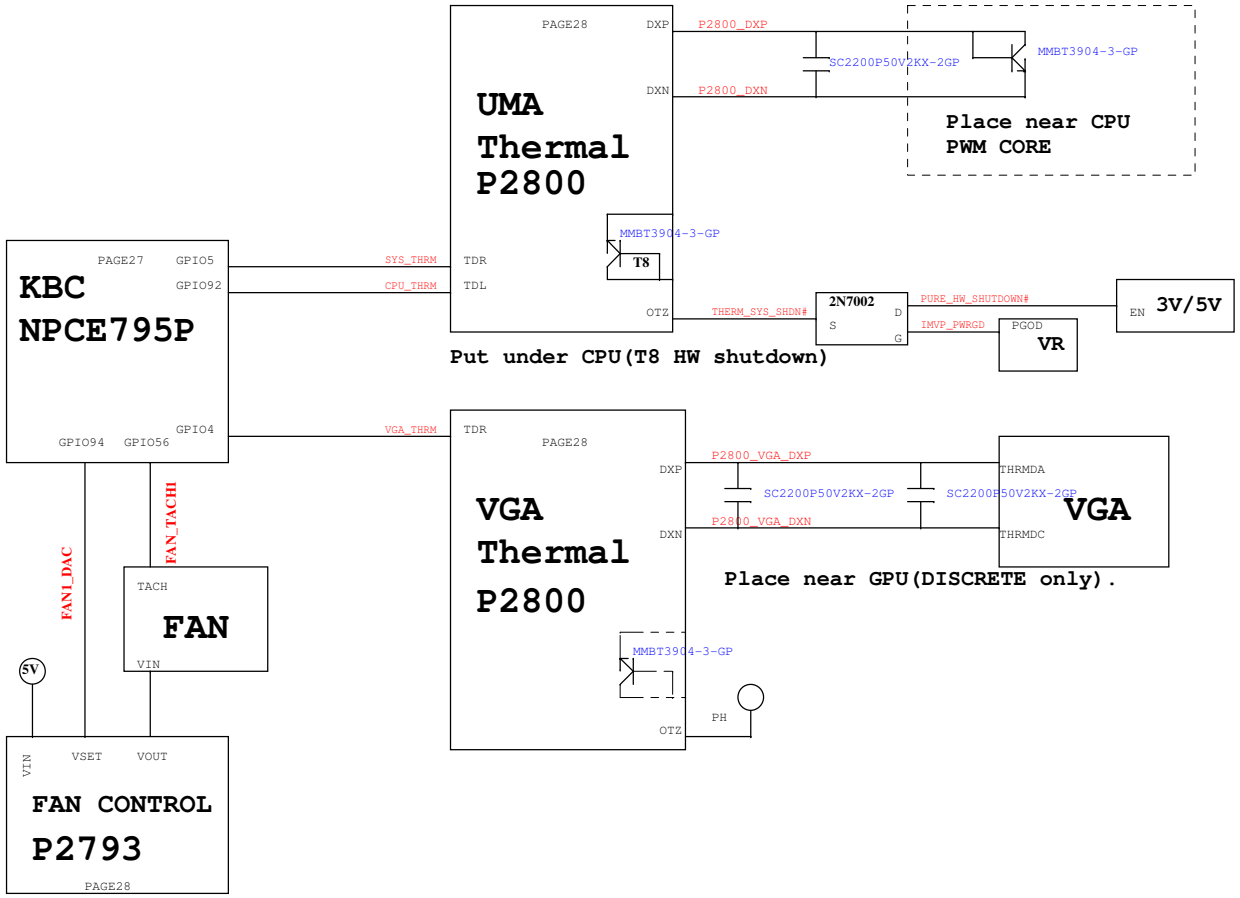
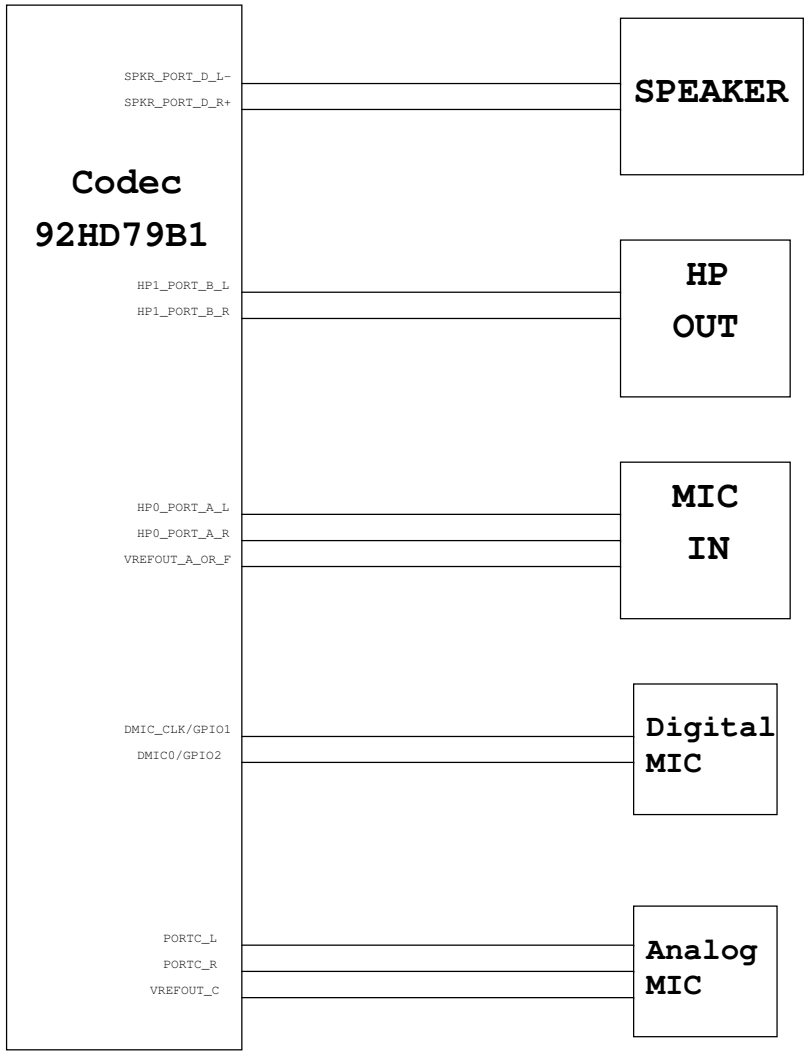
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
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Title: Thermal/Audio Block Diagram

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Change notes - Page 1

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SB	09/21	1	27	Change R2739 from 10KR to 20KR	PCB version goes into SB.	EE
		2	93	Move TC9301 to connect R9314 pin1 side	Place capacitor closer to electric load.	EE
		3	93	Delete R9315	Layout space constraint.	EE
		4	56	Delete TP5601 and connect HDD1 pin18 to GND	Remove unused test point.	EE
		5	42	Add PR4271 0-ohm resistor	Link power good signal of VCORE VRM.	EE
	09/22	1	37	Add R3731 and reserve R3732 0-ohm resistor	Follow Intel S3 power reduction circuit.	EE
		2	57	Add C5721~C5724 0.01uF 0402 capacitor	Follow Intel eSATA with repeater design guide.	EE
	09/23	1	49,59	Modify connector for LVDS1, RJ45	Drawing updated by ME.	ME
		2	42	Update PU4201 symbol	Revision change by vendor.	Power
	09/27	1	57	Rename duplicated net name	Existed net name suffix "_C", change to "_J".	EE
		2	45	Delete power gap between source and high-side MOS	Layout space constraint.	EE
	09/28	1	59	Swap net on transformer	Smoothen layout routing.	EE
		2	97	Reserve RF required capacitors	Request by RF team.	RF
	09/29	1	50,51	Change CRT1 and HDMI1 connector	ME drawing update.	ME
		2	42,43,44	Empty PC4201,PC4228,PC4229; stuff 0.1uF capacitor on PC4303,PC4317,PC4402; PC4236 change to 56pF; PC4238 change to 220pF; PR4201 to 21.5R; PR4210 to 475R; PR4215 to 15.8KR; PR4222 to 60.4KR; PR4227 to 56.2KR; PR4232,PR4256 to 499R; PR4235 to 30.1KR; PR4236 to 1.78KR; PR4237 to 845R; PR4238 to 1.3KR; PR4239 to 0R; PR4249 to 7.87KR; PR4255 to 30.1KR; PR4264 to 20KR; PR4246 to 715R; PC4213 to 4700pF	Request by Power Team.	Power
		3	65	Change R6502, short-pad to 0R-0402 and default empty	Reserve for future bluetooth module feature.	EE
	09/30	1	86	Add D8601 and connect net "AC_PRESENT"	Inform GPU about system power status.	EE
		2	38	Change connector "DCIN1"	ME design change.	ME
	10/3	1	68	Change part reference from "BTYL0" to "BTYL2"	To prevent OrCAD system bug on BOM creation.	EE
		2	36	Remove U3604 U3605 and related net	Remove defect power enable circuit.	EE
		3	45	Change PR4502 to 1KR, PC4502 to 0.1uF	Delay enable sequence for 1.05V power resume from S3.	Power
		4	86	Change R8634 from 30.1KR to 10KR	Set GPU strap following vendor debug result.	EE
		5	92	Set R9225 default empty	Double pull-up with R2223.	EE
		6	24	Change net name from 1D05V_VTT_VCCASW to 1D05V_VTT	Connect to 1D05V_VTT.	EE
	10/4	1	19,22	Empty R1923,R1924, move R2220 PU 3D3V_S5	Follow Intel design checklist and power sequence.	EE
		2	33	Remove TP3312 and connect chassis to GND	Better signal shielding.	EE
		3	22	Seperate RN2203, R2231 PU 3D3V_S0, R2232 PU 3D3V_S5	Follow Intel design checklist.	EE
	10/5	1	18	Stuff R1817, 8.2KR	Follow Intel design checklist.	EE
		2	68	Rename net "DC_BATFULL#_PWR" to "SATA_LED#_PWR"	Correct LED lighting behavior.	EE
		3	45	Empty PC4502 PR4507, stuff PR4506 as 8.87KR, PR4508 as 10KR, and PR4502 as 0R	Fine tuned 1.05V power sequence.	Power
		4	92	Change PU9202 PU9203 footprint	Change footprint for multiple component sources.	Power

<Variant Name>

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Title: Change History

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VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SB	10/6	1	97	Change net name from "3D3V_RUNPWR" to "1D5V_RUNPWR"	Duplicated net name.	EE
	10/7	1	38,40	Change PU3801 PU4001 PU4002 PU4004 PU4005	Change by Power Team request.	Power
		2	45	Change PR4506 to 18KR and PR4508 to 20KR	Change by Power Team request.	Power
		3	28	Empty R2811 and stuff R2810	Solve T8 shutdown can't be performed issue.	Power
	10/11	1	41	Change PL4101	Change by Power Team request.	Power
	10/13	1	57	Stuff selected parts	Stuff parts for E49 USB2.0 port function.	EE
		2	63	Stuff selected parts	Stuff parts for Bluetooth module function.	EE
		3	20	Stuff RN2016	dGPU can be acknowledged when RN2016 stuffed.	EE
SC	11/17	1	86	Change R8632 from 15KR to 4.99KR	nVidia specificaiton updates strap setting.	EE
		2	9	Rename net N11126255 to 1D5V_S0_VDDQ	Give regular name to power net.	EE
		3	97	Add EC9731 0.1uF, 25V	Request by EMC team.	EMC
	11/21	1	92	Add diode PD9201	For VGA_CORE enable signal discharge circuit.	EE
		2	92,93	Change PR9256 to 100KR, add R9315 100KR, C9309 0.1uF	Fine tune GPU power sequence.	EE
	11/23	1	49	Add R4913 R4914 0R power shunt	Reserved for hall effect sensor power source.	EE
		2	59	Add AFTP5901 - AFTP5912	Place AFTP for manufactory.	EE
		3	22,59	Add RTC battery detect circuit.	For factory manufacturing process.	EE
	11/24	1	49	Change TP4922 net name from 3D3V_S5 to 3D3V_HALL	Follow AFTP rule.	EE
	11/25	1	69	Add switch TPLBN1 and TPRBN1, and change TPAD1	Requested by ME.	ME
		2	21,68	Modify APS LED circuit	Modify design to follow VB480.	EE
		3	27,65	Add net "WLAN_WAKE#" and related circuit	To support wake on wireless LAN function.	EE
		4	27	Add net "RJ45_DET#" circuit	For EC to sense RJ45 cable stuff or not.	EE
		5	27,56,66	Add HDD and mSATA detect circuit	For EC to sense devices stuff or not.	EE
		6	93	Remove R9314 10mR	Reduce voltage drop on power rail 1D5V_VGA_S0.	EE
	11/28	1	97	Modify mini-card stand-off hole	Requested by ME.	ME
		2	58	Change SPK1 and MIC1, add SPK2	Requested by ME.	ME
	11/29	1	13	Reserve R1351	Reserved for AOAC power	EE
		2	93	Reserve C9310 and R9316 soft start circuit	Reserved for power tunning.	EE
	11/30	1	68	Change BTYL1	Downsize LED height for factory request.	EE
		2	31	Modify L3101	Downsize and follw project LGN-1.	EE
	12/01	1	65,66,69	Change TPAD1, WLAN1, and WWAN1	ME changed.	ME
	12/05	1	69,82	Change TPAD1, BTNCN1, and BTNCN2	ME changed.	ME
		2	64	Reverse FPCN1 pin define	Reverse pin define to match ME cable define.	EE
		3	43,44,92	Change PL9201, PU4301, PU4302, and PU4401	Changed by Power Team Request.	Power
		4	41	PR4102 110K to 78.7K,PR4101 150K to 127K	Adjust Over Current Protection parameter by Power Team.	Power
		5	42,46	PR4602 9.76K to 8.06K, PR4264 20K to 17.8K	Adjust 1.5V OCP, and fine tune VCORE load line.	Power

<Variant Name>

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Title: Change History

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Change notes - Page 3

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
SC	12/05	6	27	Reserve R2747 and R2748 pull-up resistors	Follow LGN-1 for LED issue.	EE
		7	27	Add R2731 (63.10034.1DL) & C2712 (78.10134.1FL)	Follow LGN-1 for AD_OFF issue.	EE
	12/06	1	39	Add AFTE,TP3909 TP3803 TP3804 TP6003 TP6004	Add by AFTE request to meet DFX	AFTE
	12/07	1	97	Add EC9764 EC9765 EC9766	Add by EMC team request.	EMC
		2	40	Change PU4003 pin 14 to connect to GND	Power team design change to ease noise coupling.	Power
		3	41	Change PU4103 from TPS51225 to TPS51225C	Power team changes to use new version IC.	Power
	12/08	1	97	Change H8, H9 part	Change by ME request.	ME
		2	69	Modify to use AFTE Test Point	Add by AFTE request to meet DFX.	AFTE
		3	22	Add more NCTF test points	For more NCTF test points.	EE
	12/09	1	31	Change L3101 part number	The same part with different feeding direction for SMT	EE
		2	20	Change C2007 C2008 C8612 C8613 to 15pF	Changed by vendor measurement report.	EE
		3	24	Stuff C2401	Occupy the location to follow CRB.	EE
		4	22	Empty R2214	Leave vacancy for nominal voltage level.	EE
	12/09	1	92	Change PL9201 part number	Change by Power Team request.	Power
	12/15	1	62	Change USB3P1 and USB3P2 part number	Change by ME request to use blue color USB connector.	ME

<Variant Name>

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Title: Change History

Size: A3 | Document Number: LLP-1 | Rev: SA

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