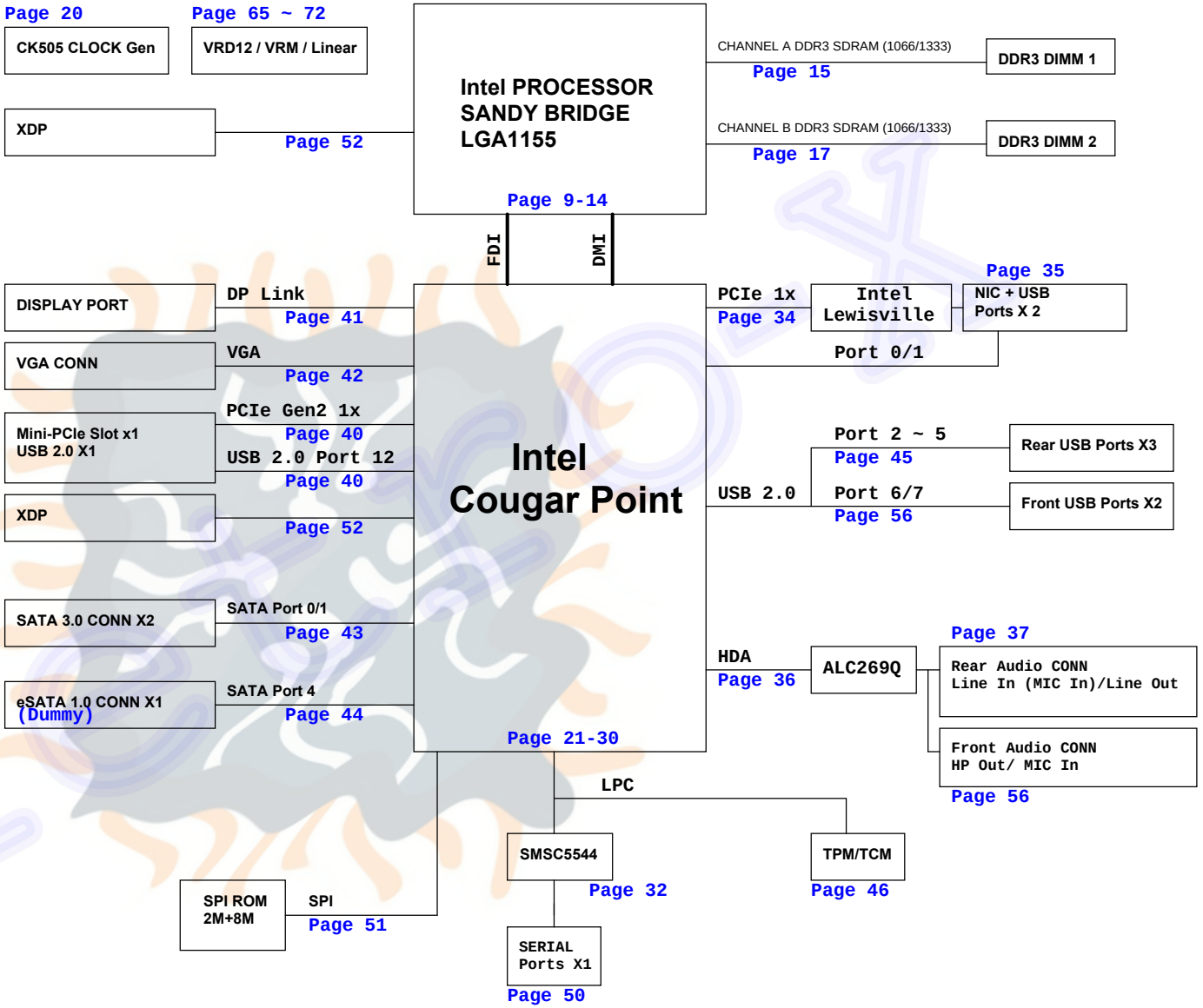
Katsiki-USFF



DESIGN	CHECK	APPROVE
Steven	Sam	Sdiu

DELL INC.

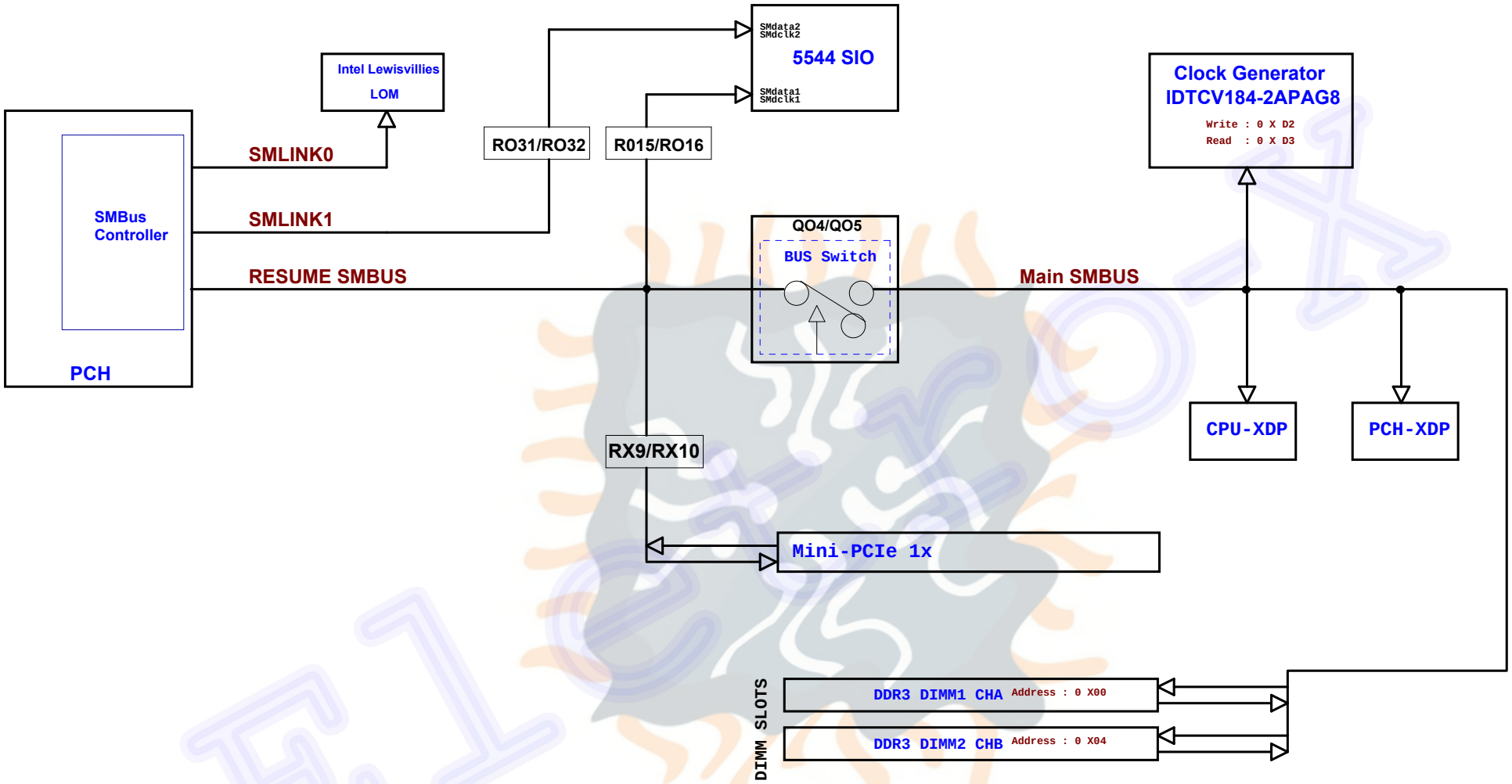
Title: Index / Block diagram

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 1 of 72

SMBUS DIAGRAM



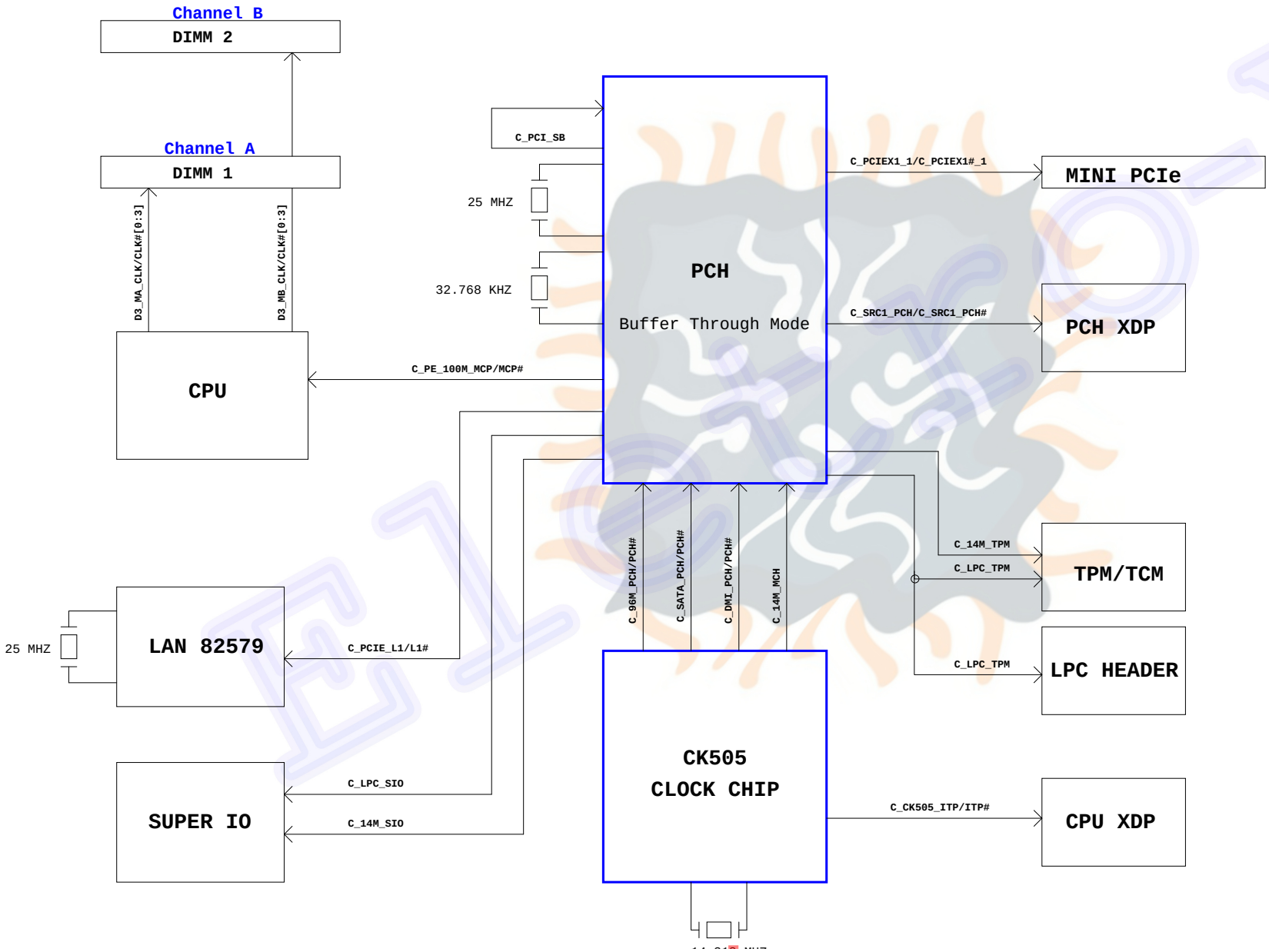
DELL INC.

Title: SMBus MAP

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 2 of 72



DELL INC.

Title: Clock Distribution

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 3 of 72

RESET / Power Good MAP

Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

Deep Sleep Exit MAP

Sequence Signal Name:

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#

CPU-Sandy Bridge

UNCOREPWRGOOD
SM_DRAMPWROK
RESET*
SM_DRAMRST*

PROCPWRGD
PWROK
> 1ms

(9) (10)

Buffer (UH2)

DDRIII Slots
D3_RESET# (8)

LAN
PE_RST_N (10)

TPM/TCM
LRESET# (10)

CPU-XDP (9) (1)

PCH-XDP
F_TP_XDP_RST (1)

Front Panel
O_PWRBTN#IN

(1)

Power On Botton
O_PWRBTN#IN (1)

(1) (D1)

PCH

PWRBTN#
PROCPWRGD
DRAMPWROK (8)
PLTRST# (10)
SYS_PWROK
AND
PWROK
SLP_S3# (2)
SLP_S4# (2)
SLP_A# (2)
SYS_RESET#
RSMRST#
HDA_RST#
APWROK
SUSACK#
SUSWARN#
SLP_SUS#

VRD 12
VR_RDY (6)

RESET BUTTON
FP_RST#

HD Audio
RESET# (12)

ME POWER-GOOD CIRCUIT
PCH_MEPWRGD (5)

PCH_MEPWRGD
+1P05V_ME
> 1ms

(D5) (D4) (D2)

Sequence Logic Circuit
Page.64 (D3)

+5VDUAL
SUSACK#

Sequence Logic Circuit
Page.64

+5V_S5/+3V_S5
SLP_SUS#

SIO-5544

PWRBTN#
LRESET#
PWR_GOOD_3V (7)
SLP_S3#
SLP_S4_S5#
IO_SMI#
PCI_RST_SYS# (11)
PS_ON# (3)
PWRGD_PS (4)

Mini-PCIe
PERST#

ATX Power
PSON
PWROK

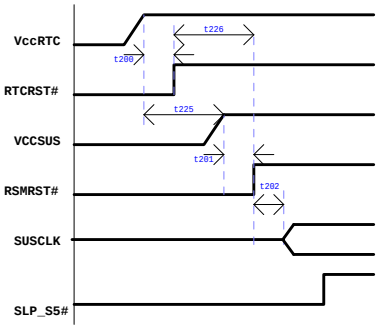
PWR_GOOD_3V
PWRGD_PS
100~120ms

DELL INC.

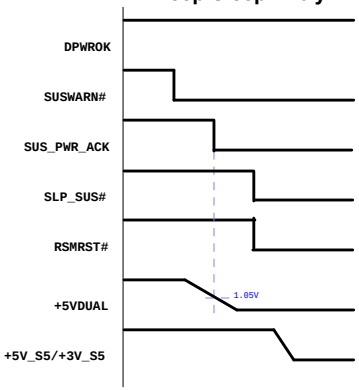
Title: Reset / Power Good Map
DWG NO: Katsiki_USFF
Rev: A00
Date: Monday, December 06, 2010 Sheet 6 of 72

POWER ON Timing Diagram

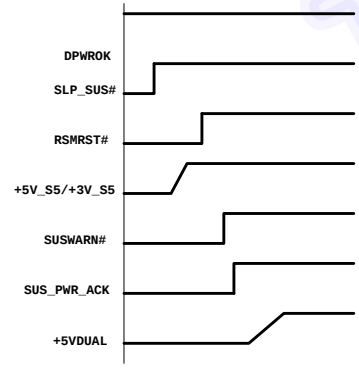
G3 to S4/S5 Timing Diagram

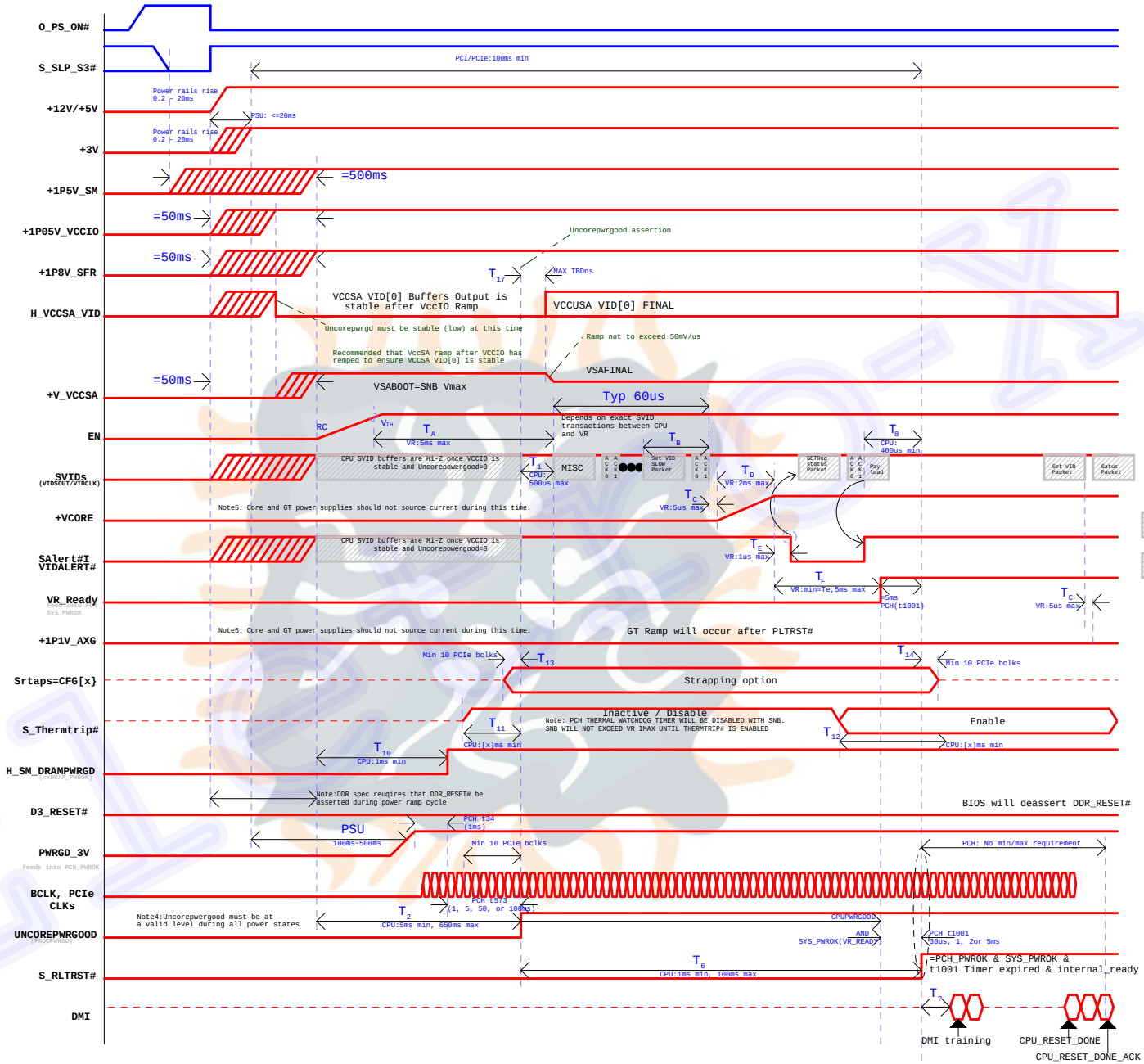


Deep Sleep Entry



Deep Sleep Exit





DELL INC.

Title: **Power On Sequence**

DWG NO: *Katsiki_USFF*

Rev: A00

Date: Monday, December 06, 2010 Sheet 5 of 72

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL1	C_CK_BSEL2
100	1	0	1
133	1	0	0

Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP
		0	SRC8 DEFAULT
PCI3/CFGP (PIN5)	C_CK505_33M_PCI3	Low	See CFG Table DEFAULT (Set SATA and SRC come from PLL4)
		Mid	See CFG Table
		High	See CFG Table

SIO SMSC5544

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description
High	1.5V
Low	1.8V DEFAULT

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description
High	Regulator is enabled. DEFAULT
Low	Regulator is disabled.

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable DEFAULT
Low	Topblock swap mode: Enable

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable DEFAULT

Integrated 1.05V VRM

INTVRMEN	Description
High	Integrated 1.05V VRM: Enable DEFAULT
Low	Integrated 1.05V VRM: Disable

TLS Confidentiality

GPIO15 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality DEFAULT

Flash Descriptor Override Strap

HDA_SDO	Description
High	Flash descriptor security will be override DEFAULT
Low	Disable ME in Manufacturing Mode

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description
Low	DMI Rx Termination Voltage DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description
High	DMI and FDI Tx/Rx Termination Voltage DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
Low	High	Flash cycle routed to NAND
High	High	Flash cycle routed to SPI DEFAULT

Integrated Clocking Strap

GPIO8 (IN-PU)	Description
High	Buffer Through Mode DEFAULT
Low	Enable Integrated Clock Chip

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description
High	Enable DEFAULT
Low	Disable

Digital Port C Strap

DDPC_CTRLDATA	Description
High	Configure Port C DEFAULT
Low	Disable

DELL INC.

Title: GPIO/IRQ/IDSEL Table

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 7 of 72

PCH GPIO Summary

GPIO	Type	Power Well	Default	IN-PU/PD	EX-PU/PD	Schematic usage
GPIO[0]	I/O	Core	GPI	--	10k pull-up to +3V	S_PECI_REQ#
GPIO[1]	I/O	Core	GPI	20K IN-PU (only on TACH1)	10k pull-up to +3V 1k pull-down to GND (dummy)	S_GPI_CHASSIS_ID0
GPIO[2]	I/OD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPUSB_DETECT
GPIO[3]	I/OD	Core	GPI	--	--	V_DDSP_C_HPD
GPIO[4]	I/OD	Core	GPI	--	8.2k pull-up to +3V	V_GPI_VGA_CBL_DET#
GPIO[5]	I/OD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPPE_DETECT#
GPIO[6]	I/O	Core	GPI	20K IN-PU (only on TACH2)	10k pull-up to +3V	S_GPI_PCH_HS_DET#
GPIO[7]	I/O	Core	GPI	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SKU2
GPIO[8]	I/O	Suspend	GPO	20K IN-PU	--	S_TP_GP8
GPIO[9]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5	U_USB_OC_R_#5
GPIO[10]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X_WLAN_WAKE#
GPIO[11]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	X4_WAKE#
GPIO[12]	I/O	Suspend	Native	--	10k pull-up to +3V_LAN 10k pull-down to GND	L_LAN_DISABLE#
GPIO[13]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5	X1_WAKE#
GPIO[14]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5	GPO_WLOM
GPIO[15]	I/O	Suspend	GPO	20K IN-PD	1k pull-up to +3V_S5	S_PCH_GP15
GPIO[16]	I/O	Core	GPI	--	10k pull-up to +3V 10k pull-down to GND	H_SKTOCC_R_#
GPIO[17]	I/O	Core	GPI	20K IN-PU (only on TACH0)	10k pull-up to +3V 1k pull-down to GND (dummy)	S_GPI_CHASSIS_ID1
GPIO[19]	I/O	Core	GPI	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND	S_SATA1GP
GPIO[20]	I/O	Core	Native	--	10k pull-up to +3V 10k pull-down to GND	S_PCH_GPIO20_PU
GPIO[21]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_GPI_BRD_REV0
GPIO[22]	I/O	Core	GPI	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	S_PCH_CONFIG_JUMPER
GPIO[23]	I/O	Core	Native	20K IN-PU	10k pull-up to +3V (dummy)	L_DRQ1#
GPIO[24]	I/O	Suspend	GPO	--	100k pull-up to +3V_S5	H_SKTOCC#
GPIO[27]	I/O	Deep Sleep	GPI	20K IN-PU	10k pull-up to +3V_DUAL 1k pull-down to GND	S_GP27_PD
GPIO[28]	I/O	Suspend	GPO	20K IN-PU	10k pull-up to +3V_S5 1k pull-down to GND	S_PCH_GP28_PU
GPIO[29]	I/O	Suspend	Native	--	1k pull-up to +3V_S5 (dumm	S_SLP_LAN#
GPIO[30]	I/O	Deep Sleep	Native	--	10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND	S_SUSWARN#
GPIO[31]	I/O	Deep Sleep	GPI	TBD IN-PD	8.2k pull-up to +3V_DUAL	S_PSWD_CLR
GPIO[32]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SKU0
GPIO[33]	I/O	Core	GPO	--	--	--
GPIO[34]	I/O	Core	GPI	--	10k pull-up to +3V	PCH_GPIO34
GPIO[35]	I/O	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_SKU1
GPIO[36]	I/O	Core	GPI	20K IN-PD	---	S_TP_GPIO36
GPIO[37]	I/O	Core	GPI	20K IN-PD	---	S_TP_GPIO37
GPIO[38]	I/O	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_GPI_CHASSIS_ID2
GPIO[39]	I/O	Core	GPI	--	10k pull-up to +3V	A_FP_PRES#
GPIO[40]	I/O	Suspend	Native	--	---	U_USB_OC_R_#1
GPIO[41]	I/O	Suspend	Native	--	---	U_USB_OC_R_#2
GPIO[42]	I/O	Suspend	Native	--	---	U_USB_OC_R_#3
GPIO[43]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5	U_USB_OC_R_#4
GPIO[44]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	S_INTRUD_CBL_DET#
GPIO[45]	I/O	Suspend	Native	--	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	O_COM_SER2_DET#
GPIO[46]	I/O	Suspend	Native	20K IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	S_GPI_BRD_REV1
GPIO[48]	I/O	Core	GPI	--	10k pull-up to +3V	S_GPIO48_PU
GPIO[49]	I/O	Core	GPI	--	8.2k pull-up to +3V	TMIN_SHIFT
GPIO[50]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#1
GPIO[51]	I/O	Core	Native	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	K_GNT#1
GPIO[52]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#2
GPIO[53]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dumm	K_GNT#2
GPIO[54]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#3
GPIO[55]	I/O	Core	Native	20K IN-PU	1k pull-down to GND (dumm	K_GNT#3
GPIO[57]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	S_GPIO57_PD
GPIO[58]	I/O	Suspend	Native		10k pull-up to +3V_S5	S_SMLINK1_CLK
GPIO[59]	I/O	Suspend	Native	--	---	U_USB_OC_R_#0
GPIO[60]	I/O	Suspend	Native	--	2.2k pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#
GPIO[61]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dum	S_LPCPD#
GPIO[62]	I/O	Suspend	Native	--	--	S_SUSCLK
GPIO[63]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_PCIAUX_GATE
GPIO[64]	I/O	Core	Native	20K IN-PD	---	S_TP_CLKOUTFLEX0
GPIO[65]	I/O	Core	Native	20K IN-PD	---	C_14M_SIO_R
GPIO[66]	I/O	Core	Native	20K IN-PD	---	S_TP_CLKOUTFLEX2
GPIO[67]	I/O	Core	Native	20K IN-PD	---	C_14M_TPM_R
GPIO[68]	I/O	Core	GPI	20K IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_GPI_BRD_REV2
GPIO[69]	I/O	Core	GPI	20K IN-PU (only on TACH5)	10k pull-up to +3V	O_PRT_DET#
GPIO[70]	I/O	Core	Native	20K IN-PU (only on TACH6)	8.2k pull-up to +3V	S_USB_HDR_DET#
GPIO[71]	I/O	Core	Native	20K IN-PU (only on TACH7)	10k pull-up to +3V	--
GPIO[72]	I/O	Suspend	Native (Mobile Only)	20K IN-PU	10k pull-up to +3V_S5	S_PCH_GP72_PU
GPIO[74]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_MFG_MODE_OR
GPIO[75]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_DATA

SIO_5544 GPIO Summary

GPIO	PIN NAME	Power well	Bufffer Type	EX-PU/PD	Schematic usage
GP000	(DIAG_LED3#) GP000	VTR	IO	NA	O_DIAG_LED3#
GP001	(DIAG_LED1#) GP001	VTR	IO	NA	O_DIAG_LED1#
GP002	(DIAG_LED2#) GP002	VTR	IO	NA	O_DIAG_LED2#
GP003	(DIAG_LED4#) GP003	VTR	IO	NA	O_DIAG_LED4#
GP004	GP004	VTR	IO	NA	NC
GP005	(H_CPURST#) GP005 / PECI_REQUEST#	VTR	IO/OD	10k pull-up to +3V	O_PECI_REQ#
GP006	YELLOW# / GP006	VTR	O/IO	NA	O_YELLOW#
GP007	GREEN# / GP007	VTR	O/IO	NA	O_GREEN#
GP010	SMBDAT2 / GP010	VTR	IOD/IO	8.2k pull-up to +3V_DUAL(dummy)	S_SMLINK1_DATA_R
GP011	SMBCLK2 / GP011	VTR	IOD/IO	8.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_CLK_R
GP012	GP012	VTR	IO	8.2k pull-up to +3V_DUAL	SPI_DI
GP013	GP013	VTR	IO	NA	NC
GP014	(TMIN_SHIFT) GP014	VTR	IO	8.2k pull-up to +3V	TMIN_SHIFT
GP015	PWRBTN# / GP015	VTR	I/IO	1k pull-up to +3V_DUAL	O_PWRBTN#IN
GP016	PROCHOT_IN#/PROCHOT_OUT#/GP016	VTR	I/OD/IOD	51ohm pull-up to +1P05V_VCCIO	H_PROCHOT#
GP017	TACH1 / GP017	VTR	I/IO	1k pull-up to +3V	O_SEN_CPUFAN
GP020	TACH2 / GP020	VTR	I/IO	1k pull-up to +3V	O_SEN_CHAFAN
GP021	TACH3 / GP021	VTR	I/IO	NA	NC
GP022	PWM1 / GP022	VTR	OD/IO	4.7k pull-up to +3V	O_CPUFAN_PWM
GP023	PWM2 / GP023	VTR	OD/IO	4.7k pull-up to +3V	O_CHAFAN_PWM
GP024	PWM3 / GP024	VTR	OD/IO	NA	NC
GP025	(FP_CBL_DET#) GP025	VTR	IO	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
GP026	PCI_RST_SYS# / GP026	VTR	O/IO	NA	X_PLTRST_PCIE_SLOT#
GP027	PCI_RST_SLOTS# / GP027	VTR	O/IO	NA	H_RESET#
GP030	PS_ON# / GP030	VTR	OD/IO	4.7k pull-up to +5VSB	O_PSON#
GP031	(PC_SPKR_DET) GP031	VTR	IO	8.2k pull-up to +3V_DUAL	O_AUD_PCSPKR_DET#
GP032	GP032	VTR	IO	NA	NC
GP033	PWR_GOOD_3V / GP033	VTR	O/IO	NA	PWRGD_3V
GP034	RSMRST#/ GP034	VTR	O/IO	10k pull-down to GND	O_RSMRST#
GP035	GP035	VTR	IO	8.2k pull-up to +3V_DUAL	O_BC_CLK
GP036	GP036 / SMB_CLK1	VTR	IO/IOD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCI_R
GP040	GP040 / SMB_DAT1	VTR	IO/IOD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCI_R
GP041	GP041 / IO_PME#	VTR	IO/OD	10k pull-up to +3V_S5	O_IO_PME#
GP042	GP042 / DRVDEN0	VTR	IO/O	100k pull-up to +3V_DUAL	T_ESATA_DET#
GP043	DCD1# / GP043 / MCDAT	VTR	I/IO/O	NA	O_DCD1#_R
GP044	DSR1# / GP044 / MCCLK	VTR	I/IO/O	NA	O_DSR1#_R
GP045	RXD1 / GP045	VTR	I/IO	NA	O_RXD1_R
GP046	RTS1# / GP046	VTR	O/IO	NA	O_RTS1#_R
GP047	(5V_PRSNT) GP047 / TXD1	VTR	IO/O	NA	O_TXD1_R
GP050	CTS1# / GP050	VTR	I/IO	NA	O_CTS1#_R
GP051	DTR1# [TEST_EN] / GP051	VTR	O/IO	8.2k pull-up to +3V_DUAL(dummy) 30k pull-down to GND	O_DTR1#_R
GP052	RI1# / GP052	VTR	I/IO	NA	O_RI1#_R
GP053	GP053 / DCD2#	VTR	IO/I	2.2k pull-up to +3V	O_DCD2#_R
GP054	GP054 / DSR2#	VTR	IO/I	2.2k pull-up to +3V	O_DSR2#_R
GP055	GP055 / RXD2	VTR	IO/I	2.2k pull-up to +3V	O_RXD2_R
GP056	(PWR2_PRSNT) GP056 / RTS2#	VTR	IO/O	30k pull-up to +3V	O_RTS2#_R
GP057	(MB_REG_PG) GP057 / TXD2	VTR	IO/O	30k pull-up to +3V	O_TXD2_R
GP060	GP060 / CTS2#	VTR	IO/I	2.2k pull-up to +3V	O_CTS2#_R
GP061	(MEM_REG_PG) GP061 / DTR2#	VTR	IO/O	30k pull-up to +3V	O_DTR2#_R
GP062	GP062 / RI2#	VTR	IO/I	2.2k pull-up to +3V	O_RI2#_R
GP063	GP063 / KBDRST#	VTR	IO/OD	10k pull-up to +3V	O_KB_RST#
GP064	GP064 / A20M	VTR	IO/OD	10k pull-up to +3V	O_GA20
GP065	SLP_S3# / GP065	VTR	I/IO	NA	S_SLP_S3#
GP066	SLP_S4_S5# / GP066	VTR	I/IO	NA	S_SLP_S4#
GP067	PWRGD_PS / GP067	VTR	I/IO	1k pull-up to +5V	B_ATX_PWROK
GP070	SPEAKER [DIAG_EN#] / GP070	VTR	O/IO	8.2k pull-up to +3V_DUAL(dummy) 8.25k pull-down to GND	O_SPEAKER
GP071	(SLP_M#) GP071 / IO_SMI#	VTR	IO/OD	NA	S_SLP_M#
GP072	PECI / LVSMB_CLK1 / GP072	VTR	PECI_IO/IOD/IO	1k pull-up to +1P05V_VCCIO (dummy)	H_PECI_R
GP073	PECI_READY / LVSMB_DAT1 / GP073	VTR	PECI_I/IOD/IO	1k pull-up to +1P05V_VCCIO	O_GP73_PU

DELL INC.

Title: **GPIO Table**

DWG NO: *Katsiki_USFF*

Date: Monday, December 06, 2010 Sheet 8

20100913: update CPU socket PN from M disk

UH1E

MISC

5/10

PE115527-4041-0DF

RH4 usage 1kOhm ; CRB 0.7-12/10/09
Removed RH3; CRB 0.7-12/29/09
Dummy RH6 ; CRB 0.7-12/28/09
Removed RH7; CRB 0.7-12/10/09
20100203: Dummy RH5; Intel update

RO40change reference to RH7 and move from SIO to CPU side ; CRB 0.7-12/29/09

RH2 change to 44.2 ; CRB0.7 12/07/09

Change net name to H_RESET#-12/28/09

Add off-page toXDP; CRB 0.7 12/27/09

20100308: Remove RH51,RH58

20100107: Remove test points

Add RH66 pull-up to +3V_DUAL; CRB 0.7-12/10/09

Close to XDP Conn

Close to CPU

20100104: add UH2 to prevent SIO can't use

20100709: Reserve RH58 connect H_PWRGD to GND
20100721: Mount RH58

RH17 change to 4.7k; CRB 0.7-11/30/09
20100709: Reserve CH11 connect H_PROC_SEL to GND

RH39 change to 110 ohm; CRB 0.7-11/30/09

Add H_VCCIO_SEL circuit; CRB 0.7-12/03/09

Remove CH1,CH2-12/29/09

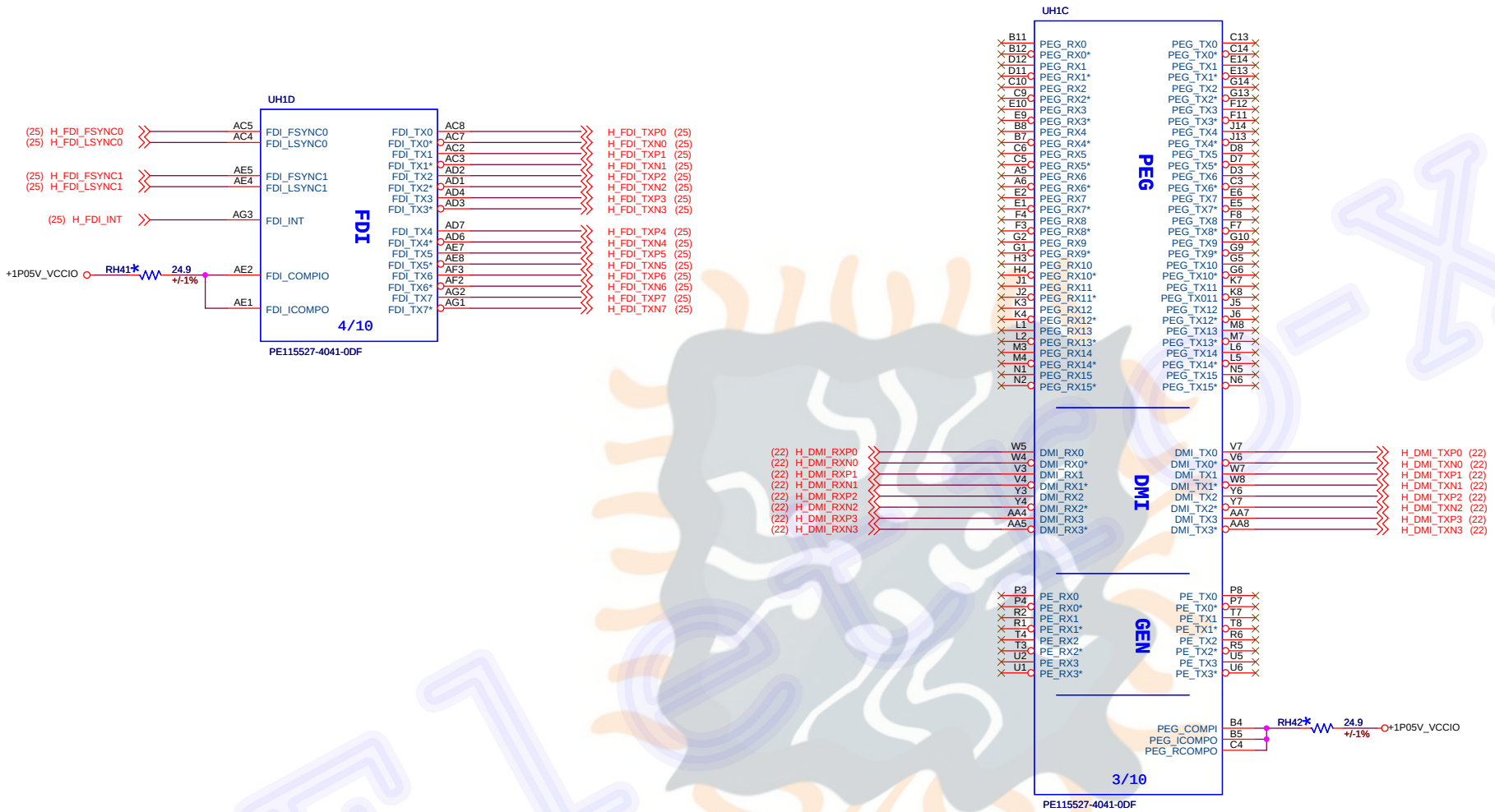
DELL INC.

Title: CPU-1: MISC

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 9 of 72



DELL INC.

Title

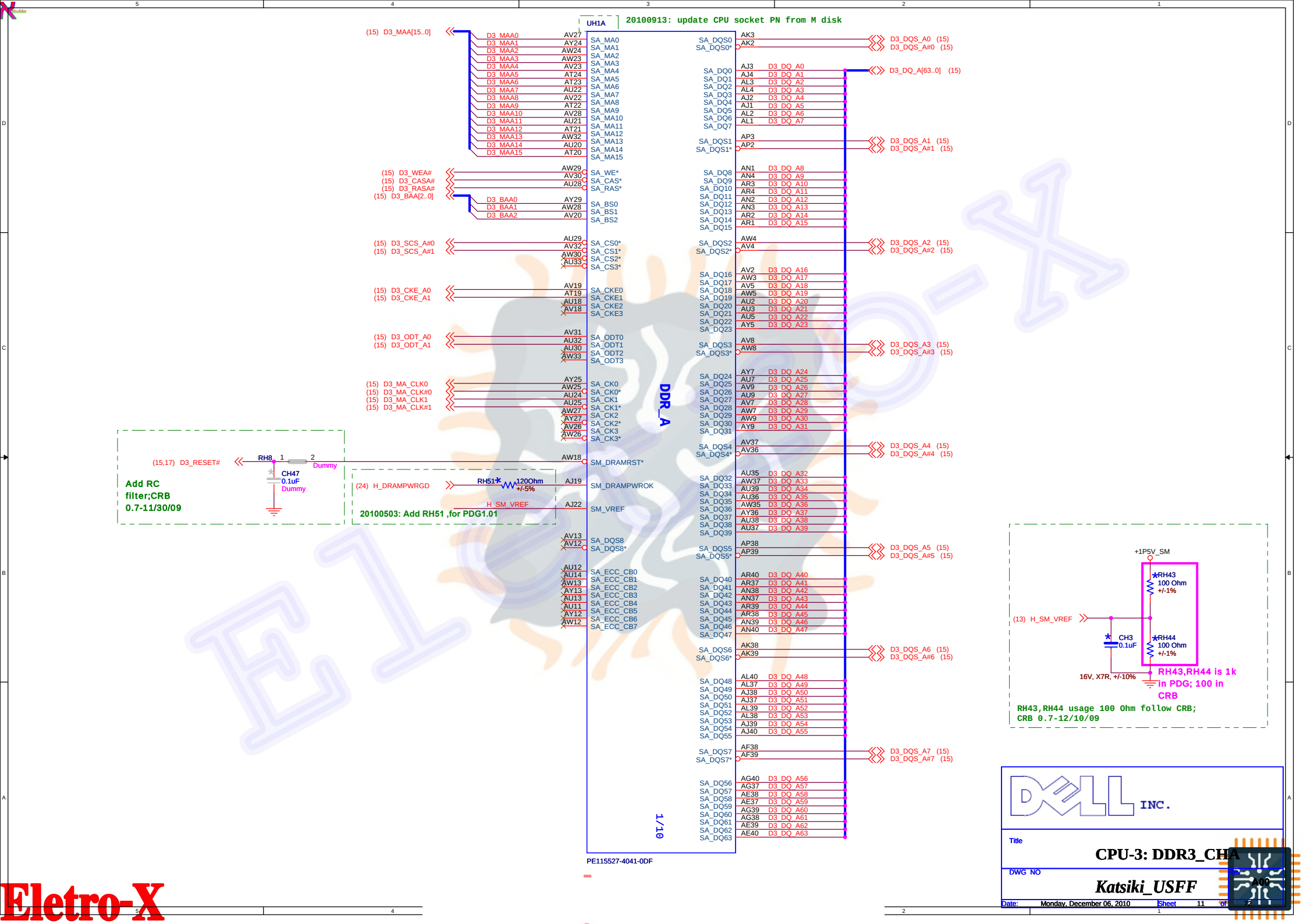
CPU-2: FDI/PCIe/DMI

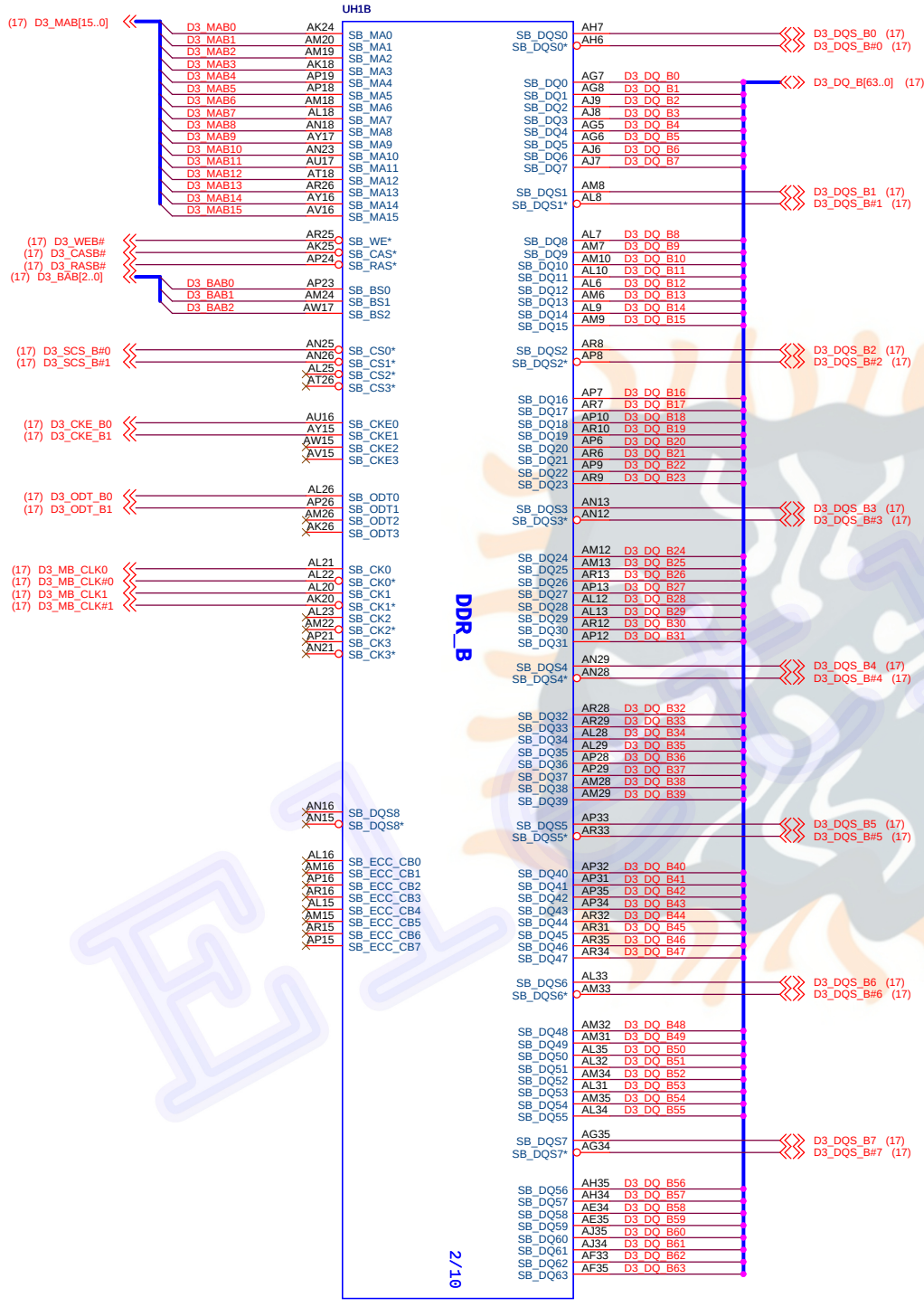
DWG NO

Katsiki_USFF

A00

Date: Monday, December 06, 2010 Sheet 10 of 72


20100913: update CPU socket PN from M disk
UH1A
DDR_A
1/10
PE115527-4041-0DF
(15) D3_MAA[15..0]
D3_MAA0 AV27
D3_MAA1 AY24
D3_MAA2 AW24
D3_MAA3 AW23
D3_MAA4 AV23
D3_MAA5 AT24
D3_MAA6 AT23
D3_MAA7 AU22
D3_MAA8 AV22
D3_MAA9 AT22
D3_MAA10 AV28
D3_MAA11 AU21
D3_MAA12 AT21
D3_MAA13 AW32
D3_MAA14 AU20
D3_MAA15 AT20
SA_MA0
SA_MA1
SA_MA2
SA_MA3
SA_MA4
SA_MA5
SA_MA6
SA_MA7
SA_MA8
SA_MA9
SA_MA10
SA_MA11
SA_MA12
SA_MA13
SA_MA14
SA_MA15
(15) D3_WEA# AW29 SA_WE*
(15) D3_CASA# AV30 SA_CAS*
(15) D3_RASA# AU28 SA_RAS*
(15) D3_BAA[2..0]
D3_BAA0 AY29 SA_BS0
D3_BAA1 AW28 SA_BS1
D3_BAA2 AV20 SA_BS2
(15) D3_SCS_A#0 AU29 SA_CS0*
(15) D3_SCS_A#1 AV32 SA_CS1*
AW30 SA_CS2*
AU33 SA_CS3*
(15) D3_CKE_A0 AV19 SA_CKE0
(15) D3_CKE_A1 AT19 SA_CKE1
AU18 SA_CKE2
AV18 SA_CKE3
(15) D3_ODT_A0 AV31 SA_ODT0
(15) D3_ODT_A1 AU32 SA_ODT1
AU30 SA_ODT2
AW33 SA_ODT3
(15) D3_MA_CLK0 AY25 SA_CK0
(15) D3_MA_CLK#0 AW25 SA_CK0*
(15) D3_MA_CLK1 AU24 SA_CK1
(15) D3_MA_CLK#1 AU25 SA_CK1*
AW27 SA_CK2
AY27 SA_CK2*
AV26 SA_CK3
AW26 SA_CK3*
(15,17) D3_RESET# AW18 SM_DRAMRST*
RH8 1 2 Dummy
CH47 0.1uF Dummy
Add RC filter;CRB 0.7-11/30/09
(24) H_DRAMPWRGD AJ19 SM_DRAMPWROK
RH51* 120Ohm +/-5%
H_SM_VREF AJ22 SM_VREF
20100503: Add RH51 ,for PDG1.01
AV13 SA_DQS8
AV12 SA_DQS8*
AU12 SA_ECC_CB0
AU14 SA_ECC_CB1
AW13 SA_ECC_CB2
AY13 SA_ECC_CB3
AU13 SA_ECC_CB4
AU11 SA_ECC_CB5
AY12 SA_ECC_CB6
AW12 SA_ECC_CB7
SA_DQS0 AK3
SA_DQS0* AK2
D3_DQS_A0 (15)
D3_DQS_A#0 (15)
SA_DQ0 AJ3 D3_DQ_A0
SA_DQ1 AJ4 D3_DQ_A1
SA_DQ2 AL3 D3_DQ_A2
SA_DQ3 AL4 D3_DQ_A3
SA_DQ4 AJ2 D3_DQ_A4
SA_DQ5 AJ1 D3_DQ_A5
SA_DQ6 AL2 D3_DQ_A6
SA_DQ7 AL1 D3_DQ_A7
D3_DQ_A[63..0] (15)
SA_DQS1 AP3
SA_DQS1* AP2
D3_DQS_A1 (15)
D3_DQS_A#1 (15)
SA_DQ8 AN1 D3_DQ_A8
SA_DQ9 AN4 D3_DQ_A9
SA_DQ10 AR3 D3_DQ_A10
SA_DQ11 AR4 D3_DQ_A11
SA_DQ12 AN2 D3_DQ_A12
SA_DQ13 AN3 D3_DQ_A13
SA_DQ14 AR2 D3_DQ_A14
SA_DQ15 AR1 D3_DQ_A15
SA_DQS2 AW4
SA_DQS2* AV4
D3_DQS_A2 (15)
D3_DQS_A#2 (15)
SA_DQ16 AV2 D3_DQ_A16
SA_DQ17 AW3 D3_DQ_A17
SA_DQ18 AV5 D3_DQ_A18
SA_DQ19 AW5 D3_DQ_A19
SA_DQ20 AU2 D3_DQ_A20
SA_DQ21 AU3 D3_DQ_A21
SA_DQ22 AU5 D3_DQ_A22
SA_DQ23 AY5 D3_DQ_A23
SA_DQS3 AV8
SA_DQS3* AW8
D3_DQS_A3 (15)
D3_DQS_A#3 (15)
SA_DQ24 AY7 D3_DQ_A24
SA_DQ25 AU7 D3_DQ_A25
SA_DQ26 AV9 D3_DQ_A26
SA_DQ27 AU9 D3_DQ_A27
SA_DQ28 AV7 D3_DQ_A28
SA_DQ29 AW7 D3_DQ_A29
SA_DQ30 AW9 D3_DQ_A30
SA_DQ31 AY9 D3_DQ_A31
SA_DQS4 AV37
SA_DQS4* AV36
D3_DQS_A4 (15)
D3_DQS_A#4 (15)
SA_DQ32 AU35 D3_DQ_A32
SA_DQ33 AW37 D3_DQ_A33
SA_DQ34 AU39 D3_DQ_A34
SA_DQ35 AU36 D3_DQ_A35
SA_DQ36 AW35 D3_DQ_A36
SA_DQ37 AY36 D3_DQ_A37
SA_DQ38 AU38 D3_DQ_A38
SA_DQ39 AU37 D3_DQ_A39
SA_DQS5 AP38
SA_DQS5* AP39
D3_DQS_A5 (15)
D3_DQS_A#5 (15)
SA_DQ40 AR40 D3_DQ_A40
SA_DQ41 AR37 D3_DQ_A41
SA_DQ42 AN38 D3_DQ_A42
SA_DQ43 AN37 D3_DQ_A43
SA_DQ44 AR39 D3_DQ_A44
SA_DQ45 AR38 D3_DQ_A45
SA_DQ46 AN39 D3_DQ_A46
SA_DQ47 AN40 D3_DQ_A47
SA_DQS6 AK38
SA_DQS6* AK39
D3_DQS_A6 (15)
D3_DQS_A#6 (15)
SA_DQ48 AL40 D3_DQ_A48
SA_DQ49 AL37 D3_DQ_A49
SA_DQ50 AJ38 D3_DQ_A50
SA_DQ51 AJ37 D3_DQ_A51
SA_DQ52 AL39 D3_DQ_A52
SA_DQ53 AL38 D3_DQ_A53
SA_DQ54 AJ39 D3_DQ_A54
SA_DQ55 AJ40 D3_DQ_A55
SA_DQS7 AF38
SA_DQS7* AF39
D3_DQS_A7 (15)
D3_DQS_A#7 (15)
SA_DQ56 AG40 D3_DQ_A56
SA_DQ57 AG37 D3_DQ_A57
SA_DQ58 AE38 D3_DQ_A58
SA_DQ59 AE37 D3_DQ_A59
SA_DQ60 AG39 D3_DQ_A60
SA_DQ61 AG38 D3_DQ_A61
SA_DQ62 AE39 D3_DQ_A62
SA_DQ63 AE40 D3_DQ_A63
+1P5V_SM
*RH43 100 Ohm +/-1%
(13) H_SM_VREF
* CH3 0.1uF
*RH44 100 Ohm +/-1%
16V, X7R, +/-10%
RH43,RH44 is 1k in PDG; 100 in CRB
RH43,RH44 usage 100 Ohm follow CRB; CRB 0.7-12/10/09
DELL INC.
Title
CPU-3: DDR3_CHA
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
Sheet 11 of 72
A00
Eletro-X



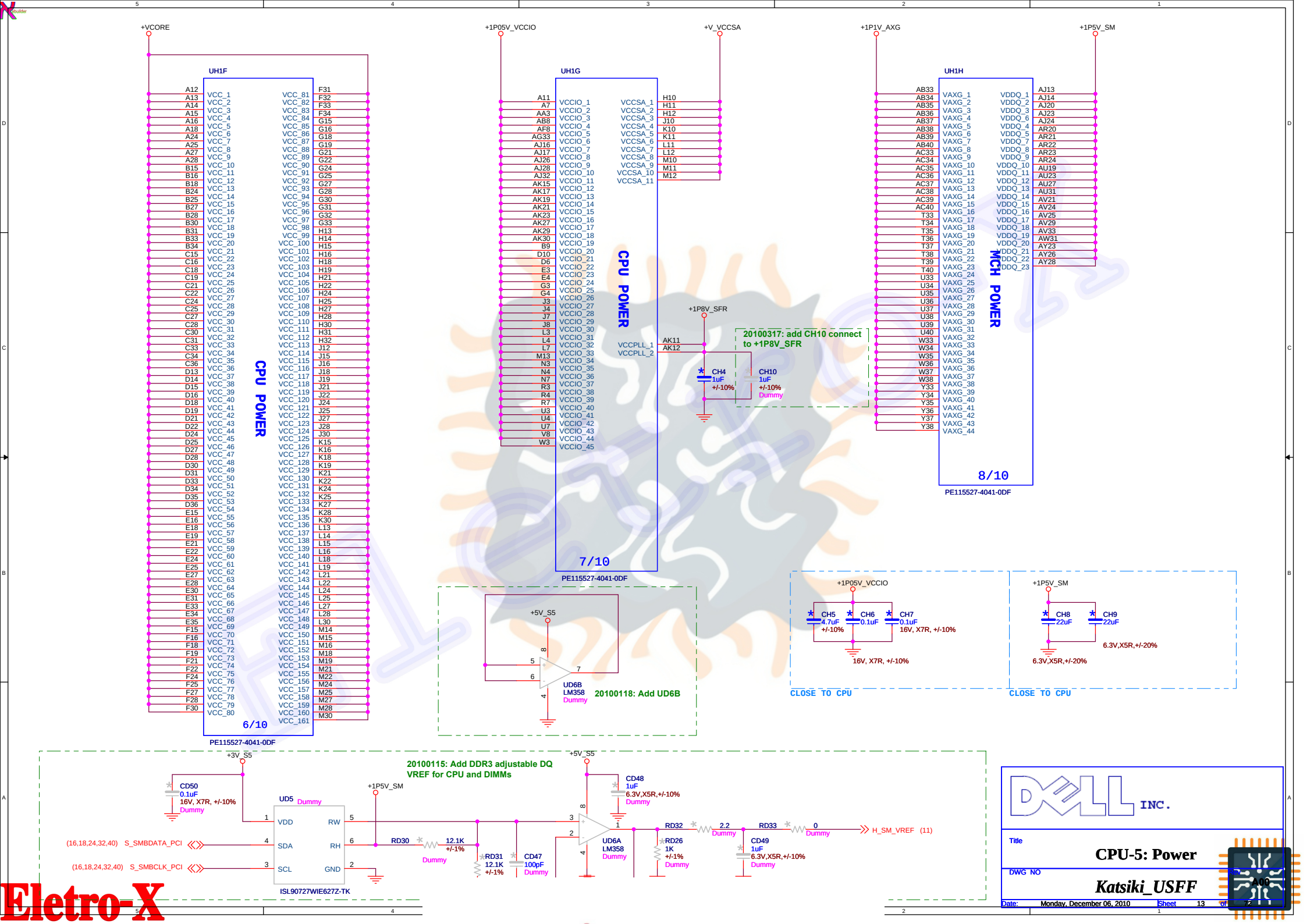
DELL INC.

Title: CPU-4: DDR3_CHB

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010 Sheet 12 of 12


+VCORE
UH1F
CPU POWER
6/10
PE115527-4041-0DF
+1P05V_VCCIO
+V_VCCSA
UH1G
CPU POWER
7/10
PE115527-4041-0DF
+1P8V_SFR
20100317: add CH10 connect to +1P8V_SFR
CH4 1uF +/-10%
CH10 1uF +/-10% Dummy
+5V_S5
UD6B LM358 Dummy
20100118: Add UD6B
+1P1V_AXG
+1P5V_SM
UH1H
MCH POWER
8/10
PE115527-4041-0DF
+1P05V_VCCIO
CH5 4.7uF +/-10%
CH6 0.1uF
CH7 0.1uF 16V, X7R, +/-10%
16V, X7R, +/-10%
CLOSE TO CPU
+1P5V_SM
CH8 22uF
CH9 22uF
6.3V,X5R,+/-20%
6.3V,X5R,+/-20%
CLOSE TO CPU
+3V_S5
CD50 0.1uF 16V, X7R, +/-10% Dummy
UD5 Dummy
ISL90727WIE627Z-TK
20100115: Add DDR3 adjustable DQ VREF for CPU and DIMMs
(16,18,24,32,40) S_SMBDATA_PCI
(16,18,24,32,40) S_SMBCLK_PCI
RD30 12.1K +/-1% Dummy
RD31 12.1K +/-1%
CD47 100pF Dummy
+5V_S5
CD48 1uF 6.3V,X5R,+/-10% Dummy
UD6A LM358 Dummy
RD32 2.2 Dummy
RD26 1K +/-1% Dummy
RD33 0 Dummy
CD49 1uF 6.3V,X5R,+/-10% Dummy
H_SM_VREF (11)
DELL INC.
Title
CPU-5: Power
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
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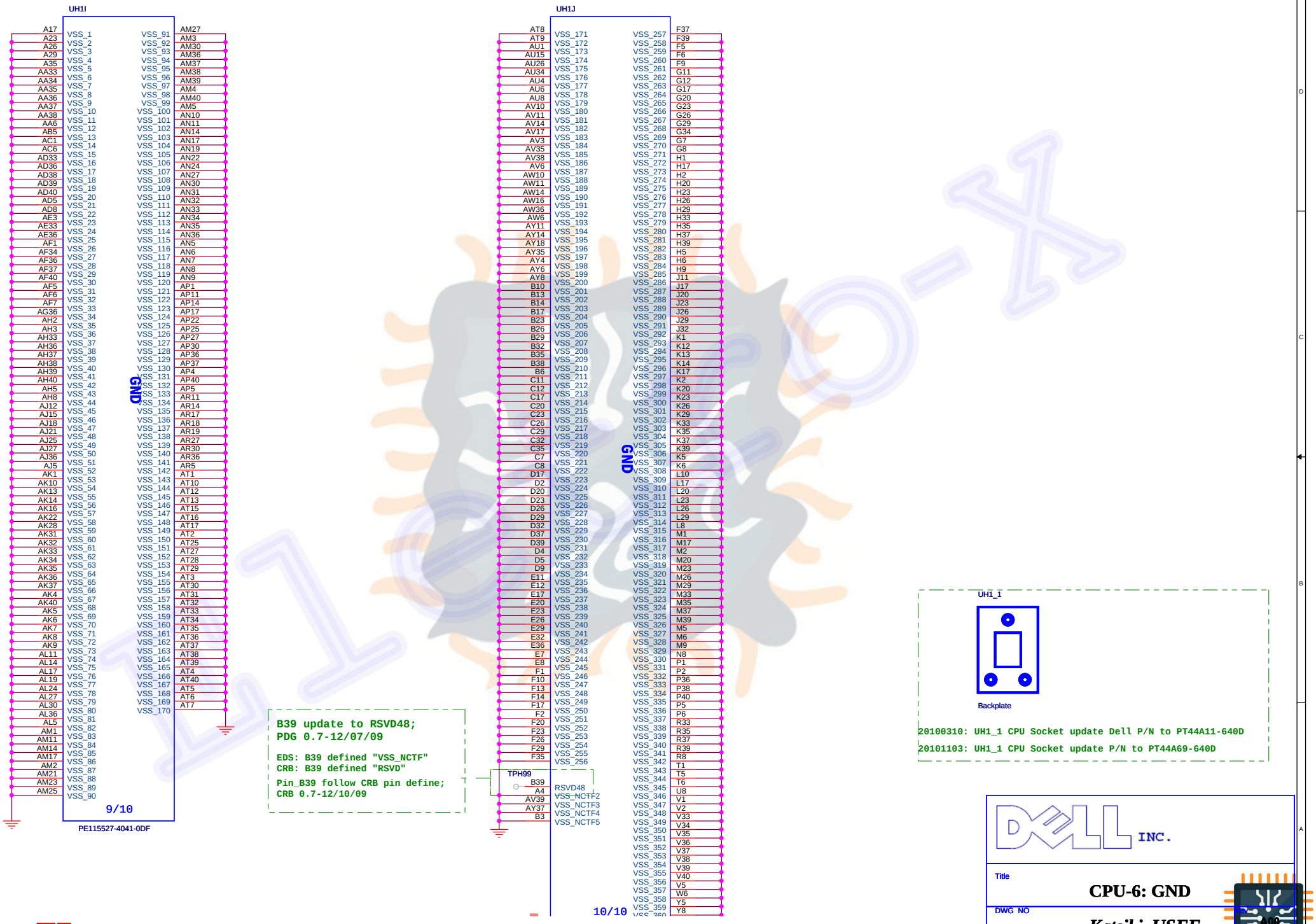
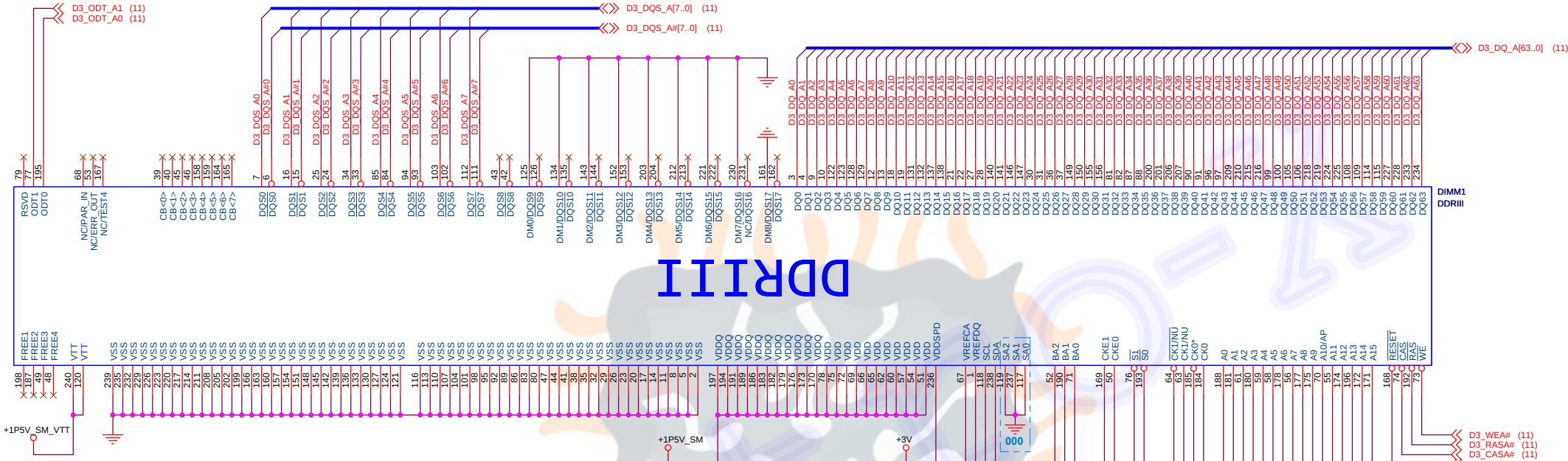
A00
Eletro-X


UH1I
A17 VSS_1
A23 VSS_2
A26 VSS_3
A29 VSS_4
A35 VSS_5
AA33 VSS_6
AA34 VSS_7
AA35 VSS_8
AA36 VSS_9
AA37 VSS_10
AA38 VSS_11
AA6 VSS_12
AB5 VSS_13
AC1 VSS_14
AC6 VSS_15
AD33 VSS_16
AD36 VSS_17
AD38 VSS_18
AD39 VSS_19
AD40 VSS_20
AD5 VSS_21
AD8 VSS_22
AE3 VSS_23
AE33 VSS_24
AE36 VSS_25
AF1 VSS_26
AF34 VSS_27
AF36 VSS_28
AF37 VSS_29
AF40 VSS_30
AF5 VSS_31
AF6 VSS_32
AF7 VSS_33
AG36 VSS_34
AH2 VSS_35
AH3 VSS_36
AH33 VSS_37
AH36 VSS_38
AH37 VSS_39
AH38 VSS_40
AH39 VSS_41
AH40 VSS_42
AH5 VSS_43
AH8 VSS_44
AJ12 VSS_45
AJ15 VSS_46
AJ18 VSS_47
AJ21 VSS_48
AJ25 VSS_49
AJ27 VSS_50
AJ36 VSS_51
AJ5 VSS_52
AK1 VSS_53
AK10 VSS_54
AK13 VSS_55
AK14 VSS_56
AK16 VSS_57
AK22 VSS_58
AK28 VSS_59
AK31 VSS_60
AK32 VSS_61
AK33 VSS_62
AK34 VSS_63
AK35 VSS_64
AK36 VSS_65
AK37 VSS_66
AK4 VSS_67
AK40 VSS_68
AK5 VSS_69
AK6 VSS_70
AK7 VSS_71
AK8 VSS_72
AK9 VSS_73
AL11 VSS_74
AL14 VSS_75
AL17 VSS_76
AL19 VSS_77
AL24 VSS_78
AL27 VSS_79
AL30 VSS_80
AL36 VSS_81
AL5 VSS_82
AM1 VSS_83
AM11 VSS_84
AM14 VSS_85
AM17 VSS_86
AM2 VSS_87
AM21 VSS_88
AM23 VSS_89
AM25 VSS_90
VSS_91 AM27
VSS_92 AM3
VSS_93 AM30
VSS_94 AM36
VSS_95 AM37
VSS_96 AM38
VSS_97 AM39
VSS_98 AM4
VSS_99 AM40
VSS_100 AM5
VSS_101 AN10
VSS_102 AN11
VSS_103 AN14
VSS_104 AN17
VSS_105 AN19
VSS_106 AN22
VSS_107 AN24
VSS_108 AN27
VSS_109 AN30
VSS_110 AN31
VSS_111 AN32
VSS_112 AN33
VSS_113 AN34
VSS_114 AN35
VSS_115 AN36
VSS_116 AN5
VSS_117 AN6
VSS_118 AN7
VSS_119 AN8
VSS_120 AN9
VSS_121 AP1
VSS_122 AP11
VSS_123 AP14
VSS_124 AP17
VSS_125 AP22
VSS_126 AP25
VSS_127 AP27
VSS_128 AP30
VSS_129 AP36
VSS_130 AP37
VSS_131 AP4
VSS_132 AP40
VSS_133 AP5
VSS_134 AR11
VSS_135 AR14
VSS_136 AR17
VSS_137 AR18
VSS_138 AR19
VSS_139 AR27
VSS_140 AR30
VSS_141 AR36
VSS_142 AR5
VSS_143 AT1
VSS_144 AT10
VSS_145 AT12
VSS_146 AT13
VSS_147 AT15
VSS_148 AT16
VSS_149 AT17
VSS_150 AT2
VSS_151 AT25
VSS_152 AT27
VSS_153 AT28
VSS_154 AT29
VSS_155 AT3
VSS_156 AT30
VSS_157 AT31
VSS_158 AT32
VSS_159 AT33
VSS_160 AT34
VSS_161 AT35
VSS_162 AT36
VSS_163 AT37
VSS_164 AT38
VSS_165 AT39
VSS_166 AT4
VSS_167 AT40
VSS_168 AT5
VSS_169 AT6
VSS_170 AT7
GND
9/10
PE115527-4041-0DF
B39 update to RSVD48;
PDG 0.7-12/07/09
EDS: B39 defined "VSS_NCTF"
CRB: B39 defined "RSVD"
Pin_B39 follow CRB pin define;
CRB 0.7-12/10/09
UH1J
AT8 VSS_171
AT9 VSS_172
AU1 VSS_173
AU15 VSS_174
AU26 VSS_175
AU34 VSS_176
AU4 VSS_177
AU6 VSS_178
AU8 VSS_179
AV10 VSS_180
AV11 VSS_181
AV14 VSS_182
AV17 VSS_183
AV3 VSS_184
AV35 VSS_185
AV38 VSS_186
AV6 VSS_187
AW10 VSS_188
AW11 VSS_189
AW14 VSS_190
AW16 VSS_191
AW36 VSS_192
AW6 VSS_193
AY11 VSS_194
AY14 VSS_195
AY18 VSS_196
AY35 VSS_197
AY4 VSS_198
AY6 VSS_199
AY8 VSS_200
B10 VSS_201
B13 VSS_202
B14 VSS_203
B17 VSS_204
B23 VSS_205
B26 VSS_206
B29 VSS_207
B32 VSS_208
B35 VSS_209
B38 VSS_210
B6 VSS_211
C11 VSS_212
C12 VSS_213
C17 VSS_214
C20 VSS_215
C23 VSS_216
C26 VSS_217
C29 VSS_218
C32 VSS_219
C35 VSS_220
C7 VSS_221
C8 VSS_222
D17 VSS_223
D2 VSS_224
D20 VSS_225
D23 VSS_226
D26 VSS_227
D29 VSS_228
D32 VSS_229
D37 VSS_230
D39 VSS_231
D4 VSS_232
D5 VSS_233
D9 VSS_234
E11 VSS_235
E12 VSS_236
E17 VSS_237
E20 VSS_238
E23 VSS_239
E26 VSS_240
E29 VSS_241
E32 VSS_242
E36 VSS_243
E7 VSS_244
E8 VSS_245
F1 VSS_246
F10 VSS_247
F13 VSS_248
F14 VSS_249
F17 VSS_250
F2 VSS_251
F20 VSS_252
F23 VSS_253
F26 VSS_254
F29 VSS_255
F35 VSS_256
VSS_257 F37
VSS_258 F39
VSS_259 F5
VSS_260 F6
VSS_261 F9
VSS_262 G11
VSS_263 G12
VSS_264 G17
VSS_265 G20
VSS_266 G23
VSS_267 G26
VSS_268 G29
VSS_269 G34
VSS_270 G7
VSS_271 G8
VSS_272 H1
VSS_273 H17
VSS_274 H2
VSS_275 H20
VSS_276 H23
VSS_277 H26
VSS_278 H29
VSS_279 H33
VSS_280 H35
VSS_281 H37
VSS_282 H39
VSS_283 H5
VSS_284 H6
VSS_285 H9
VSS_286 J11
VSS_287 J17
VSS_288 J20
VSS_289 J23
VSS_290 J26
VSS_291 J29
VSS_292 J32
VSS_293 K1
VSS_294 K12
VSS_295 K13
VSS_296 K14
VSS_297 K17
VSS_298 K2
VSS_299 K20
VSS_300 K23
VSS_301 K26
VSS_302 K29
VSS_303 K33
VSS_304 K35
VSS_305 K37
VSS_306 K39
VSS_307 K5
VSS_308 K6
VSS_309 L10
VSS_310 L17
VSS_311 L20
VSS_312 L23
VSS_313 L26
VSS_314 L29
VSS_315 L8
VSS_316 M1
VSS_317 M17
VSS_318 M2
VSS_319 M20
VSS_320 M23
VSS_321 M26
VSS_322 M29
VSS_323 M33
VSS_324 M35
VSS_325 M37
VSS_326 M39
VSS_327 M5
VSS_328 M6
VSS_329 M9
VSS_330 N8
VSS_331 P1
VSS_332 P2
VSS_333 P36
VSS_334 P38
VSS_335 P40
VSS_336 P5
VSS_337 P6
VSS_338 R33
VSS_339 R35
VSS_340 R37
VSS_341 R39
VSS_342 R8
VSS_343 T1
VSS_344 T5
VSS_345 T6
VSS_346 U8
VSS_347 V1
VSS_348 V2
VSS_349 V33
VSS_350 V34
VSS_351 V35
VSS_352 V36
VSS_353 V37
VSS_354 V38
VSS_355 V39
VSS_356 V40
VSS_357 V5
VSS_358 W6
VSS_359 Y5
VSS_360 Y8
GND
TPH99
B39 RSVD48
A4 VSS_NCTF2
AV39 VSS_NCTF3
AY37 VSS_NCTF4
B3 VSS_NCTF5
10/10
UH1_1
Backplate
20100310: UH1_1 CPU Socket update Dell P/N to PT44A11-640D
20101103: UH1_1 CPU Socket update P/N to PT44A69-640D
DELL INC.
Title
CPU-6: GND
DWG NO
Katsiki_USFF
A00
Date: Monday, December 06, 2010 Sheet 14 of 72

CHANNEL A BANK 1

SMB ADDRESS:000



CLOSE TO DIMM POWER PIN

+1P5V_SM

CD1 1uF 6.3V,X5R,+/-10%

CD2 1uF 6.3V,X5R,+/-10%

CD3 1uF 6.3V,X5R,+/-10%

CD4 1uF 6.3V,X5R,+/-10%

+1P5V_SM_VTT

CD8 4.7uF 6.3V, X5R, +/-10%

CD9 0.1uF 16V, X7R, +/-10%

CD10 0.1uF 16V, X7R, +/-10%

+3V

CD6 1uF +/-10%

CD7 1uF 6.3V,X5R,+/-10%

20100104: Remove CD5 10uF

PLAECE CLOSE TO CH-A DIMM

+1P5V_SM

RD1 1K +/-1%

Dummy

CD11 0.1uF 16V, X7R, +/-10%

RD2 1K +/-1%

CD12 0.1uF 16V, X7R, +/-10%

D3_DQ_VREF_A (16)

Add CD52,CD53; follow CRB 0.7-12/28/09

Change to 0.1uF; PDG 0.7-12/07/09

Del CD52,CD53-12/29/09

+1P5V_SM

RD3 1K +/-1%

CD13 0.1uF 16V, X7R, +/-10%

RD4 1K +/-1%

CD14 0.1uF 16V, X7R, +/-10%

CD51 2.2uF 6.3V, Y5V, +80%/-20%

D3_CA_VREF_A

Change to 0.1uF; PDG 0.7-12/07/09

20100317: add CD51, should be ne

20100512: CD51 change package s

20100519: CD51 change to 2.2uf ar

Add CD47 , CD48, CD49, CD50, CD51 and Dummy;
CRB 0.7-12/10/09

Del CD47 , CD48, CD49, CD50, CD51 and Dummy;
CRB 0.7-12/29/09

Add RD25; PDG 0.7-12/07/09

D3_DQ_VREF_A RD25 0 Dummy D3_DQ_VREF_B (17,18)

D3_CA_VREF_A RD27 0 Dummy D3_DQ_VREF_B_CA (17,18)

20100317: add RD27,should be near RD4, follow PDG1.0

DELL INC.

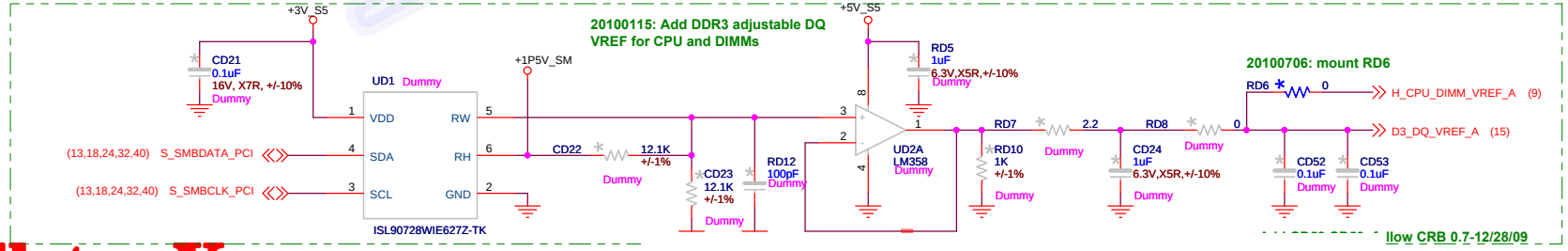
Title: DDR3 Conn: CHA_1 (DIMM1)

DWG NO: Katsiki_USFF

A00

Date: Monday, December 06, 2010 Sheet 15 of 72

Eletro-X



DELL INC.

Title

DDR3 Conn: CHA_DQ_VREF

DWG NO

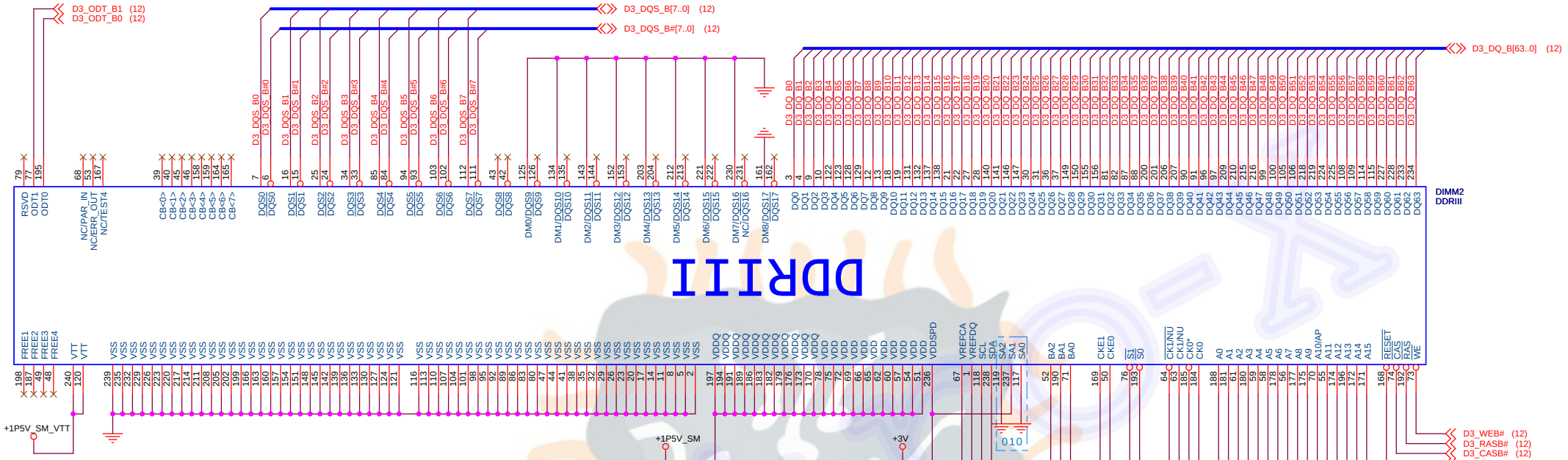
Katsiki_USFF

Date: Monday, December 06, 2010 Sheet 16 of 72

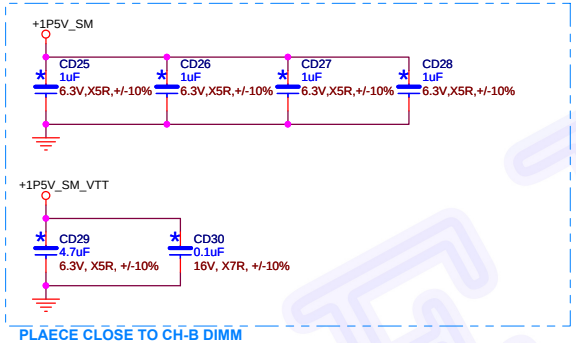
Eletro-X

CHANNEL B BANK 1

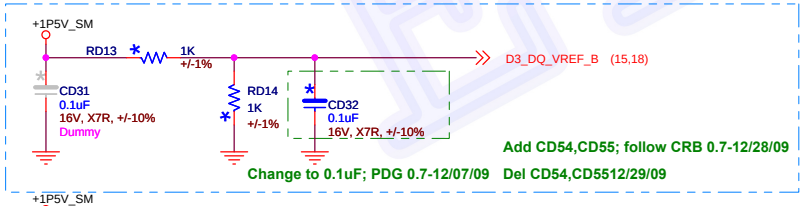
SMB ADDRESS:010

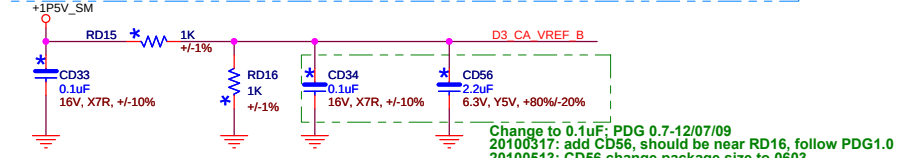


CLOSE TO DIMM POWER PIN



PLAECE CLOSE TO CH-B DIMM





SB_BS[0]-->Pin 71 (BA0)
SB_BS[1]-->Pin 190 (BA1)
SB_BS[2]-->Pin 52 (BA2)
; CRB 0.7-12/10/09

(15,20,32,52) S_SMBCLK_MAIN
(15,20,32,52) S_SMBDATA_MAIN
(12) D3_BAB[2..0]
D3_BAB2
D3_BAB1
D3_BAB0

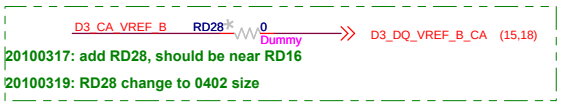
D3_CA_VREF_B
D3_DQ_VREF_B

(12) D3_CKE_B1
(12) D3_CKE_B0

(12) D3_SCS_B#1
(12) D3_SCS_B#0

(12) D3_MB_CLK#1
(12) D3_MB_CLK1
(12) D3_MB_CLK#0
(12) D3_MB_CLK0

(12) D3_MAB[15..0]
D3_MAB0
D3_MAB1
D3_MAB2
D3_MAB3
D3_MAB4
D3_MAB5
D3_MAB6
D3_MAB7
D3_MAB8
D3_MAB9
D3_MAB10
D3_MAB11
D3_MAB12
D3_MAB13
D3_MAB14
D3_MAB15



DELL INC.

Title: DDR3 Conn: CHB_1 (DIMM2)

DWG NO: Katsiki_USFF

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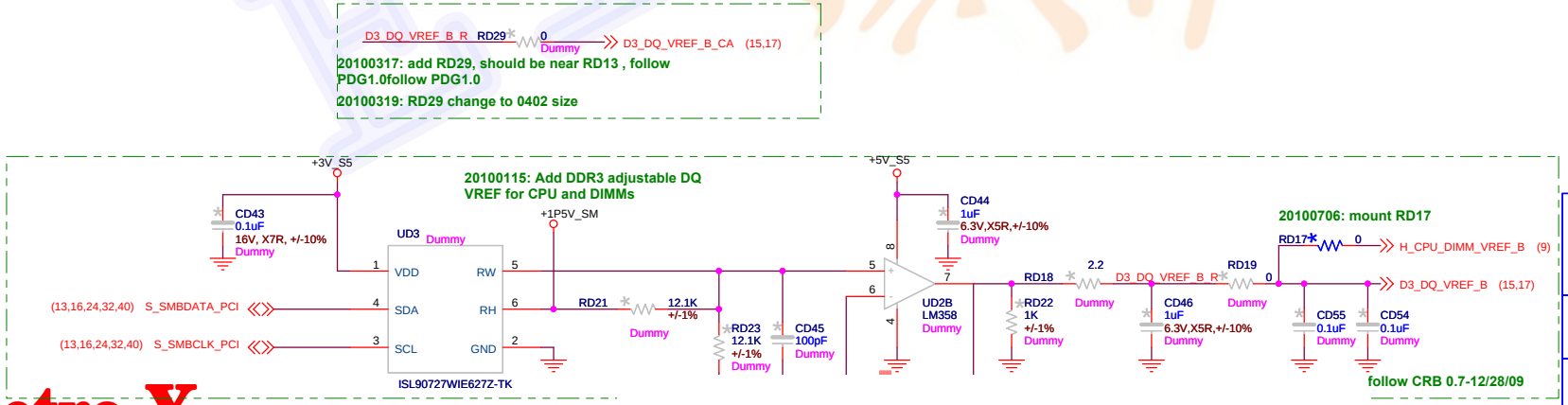
Date: Monday, December 06, 2010 Sheet 17 of 72



DELL INC.

Title

DDR3 Conn: CHB_DQ_VREF

DWG NO

Katsiki_USFF

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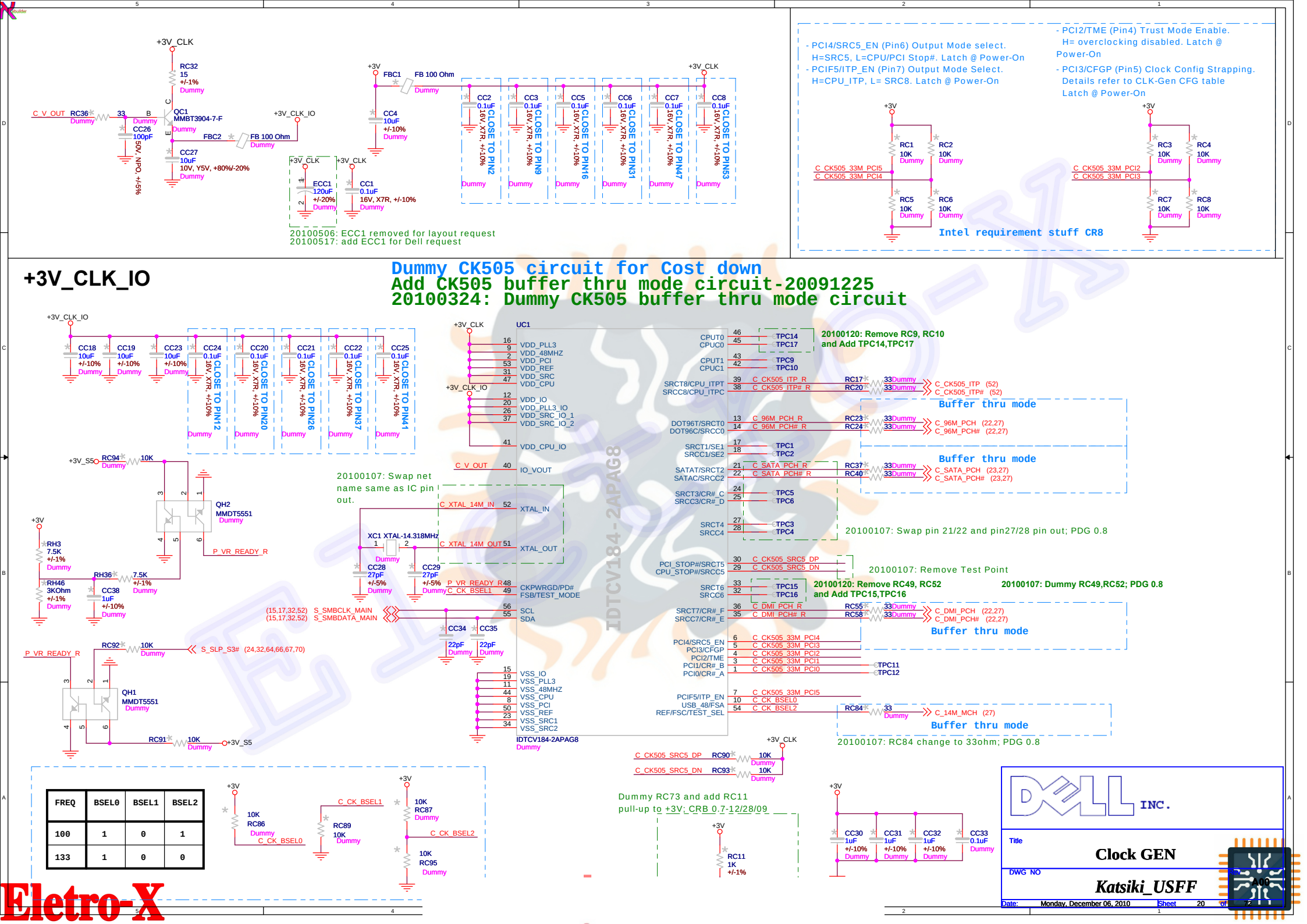
+3V_CLK
RC32 15 +/-1% Dummy
C_V_OUT RC36 33 Dummy
QC1 MMBT3904-7-F Dummy
CC26 100pF 50V, NPO, +/-5%
CC27 10uF 10V, Y5V, +80%/-20% Dummy
FB100 Ohm Dummy
+3V_CLK_IO
+3V
FBC1 FB 100 Ohm Dummy
CC4 10uF +/-10% Dummy
CC2 CC3 CC5 CC6 CC7 CC8 0.1uF 16V, X7R, +/-10% CLOSE TO PIN2 PIN9 PIN16 PIN31 PIN47 PIN53 Dummy
ECC1 120uF +/-20% Dummy
CC1 0.1uF 16V, X7R, +/-10% Dummy
20100506: ECC1 removed for layout request
20100517: add ECC1 for Dell request
- PCI4/SRC5_EN (Pin6) Output Mode select. H=SRC5, L=CPU/PCI Stop#. Latch @ Power-On
- PCIF5/ITP_EN (Pin7) Output Mode Select. H=CPU_ITP, L= SRC8. Latch @ Power-On
- PCI2/TME (Pin4) Trust Mode Enable. H= overclocking disabled. Latch @ Power-On
- PCI3/CFGP (Pin5) Clock Config Strapping. Details refer to CLK-Gen CFG table Latch @ Power-On
RC1 RC2 RC5 RC6 10K Dummy
C_CK505_33M_PCI5
C_CK505_33M_PCI4
Intel requirement stuff CR8
RC3 RC4 RC7 RC8 10K Dummy
C_CK505_33M_PCI2
C_CK505_33M_PCI3
+3V_CLK_IO
Dummy CK505 circuit for Cost down
Add CK505 buffer thru mode circuit-20091225
20100324: Dummy CK505 buffer thru mode circuit
CC18 CC19 CC23 10uF +/-10% Dummy
CC24 CC20 CC21 CC22 CC25 0.1uF 16V, X7R, +/-10% CLOSE TO PIN12 PIN20 PIN26 PIN37 PIN41 Dummy
+3V_S5
RC94 10K Dummy
QH2 MMDT5551 Dummy
P_VR_READY_R
RH3 7.5K +/-1% Dummy
RH36 7.5K +/-1% Dummy
RH46 3KOhm +/-1% Dummy
CC38 1uF +/-10% Dummy
RC92 10K Dummy
S_SLP_S3# (24,32,64,66,67,70)
QH1 MMDT5551 Dummy
RC91 10K Dummy
+3V_S5
UC1
+3V_CLK
VDD_PLL3
VDD_48MHZ
VDD_PCI
VDD_REF
VDD_SRC
VDD_CPU
+3V_CLK_IO
VDD_IO
VDD_PLL3_IO
VDD_SRC_IO_1
VDD_SRC_IO_2
VDD_CPU_IO
C_V_OUT IO_VOUT
20100107: Swap net name same as IC pin out.
C_XTAL_14M_IN XTAL_IN
XC1 XTAL-14.318MHz
C_XTAL_14M_OUT XTAL_OUT
CC28 CC29 27pF +/-5% Dummy
P_VR_READY_R CKPWRGD/PD#
C_CK_BSEL1 FSB/TEST_MODE
(15,17,32,52) S_SMBCLK_MAIN
(15,17,32,52) S_SMBDATA_MAIN
SCL
SDA
CC34 CC35 22pF Dummy
VSS_IO
VSS_PLL3
VSS_48MHZ
VSS_CPU
VSS_PCI
VSS_REF
VSS_SRC1
VSS_SRC2
IDTCV184-2APAG8 Dummy
IDTCV184-2APAG8
CPU0 CPUC0 TPC14 TPC17
20100120: Remove RC9, RC10 and Add TPC14,TPC17
CPU1 CPUC1 TPC9 TPC10
SRCT8/CPU_ITPT SRCC8/CPU_ITPC
C_CK505_ITP_R C_CK505_ITP# R
RC17 RC20 33 Dummy
C_CK505_ITP (52)
C_CK505_ITP# (52)
Buffer thru mode
DOT96T/SRCT0 DOT96C/SRCC0
C_96M_PCH_R C_96M_PCH# R
RC23 RC24 33 Dummy
C_96M_PCH (22,27)
C_96M_PCH# (22,27)
SRCT1/SE1 SRCC1/SE2 TPC1 TPC2
SATAT/SRCT2 SATAC/SRCC2
C_SATA_PCH_R C_SATA_PCH# R
RC37 RC40 33 Dummy
C_SATA_PCH (23,27)
C_SATA_PCH# (23,27)
Buffer thru mode
SRCT3/CR#_C SRCC3/CR#_D TPC5 TPC6
SRCT4 SRCC4 TPC3 TPC4
20100107: Swap pin 21/22 and pin27/28 pin out; PDG 0.8
PCI_STOP#/SRCT5 CPU_STOP#/SRCC5
C_CK505_SRC5_DP C_CK505_SRC5_DN
20100107: Remove Test Point
SRCT6 SRCC6 TPC15 TPC16
20100120: Remove RC49, RC52 and Add TPC15,TPC16
20100107: Dummy RC49,RC52; PDG 0.8
SRCT7/CR#_F SRCC7/CR#_E
C_DMI_PCH_R C_DMI_PCH# R
RC55 RC58 33 Dummy
C_DMI_PCH (22,27)
C_DMI_PCH# (22,27)
Buffer thru mode
PCI4/SRC5_EN PCI3/CFGP PCI2/TME PCI1/CR#_B PCI0/CR#_A
C_CK505_33M_PCI4 PCI3 PCI2 PCI1 PCI0
TPC11 TPC12
PCIF5/ITP_EN USB_48/FSA REF/FSC/TEST_SEL
C_CK505_33M_PCI5
C_CK_BSEL0
C_CK_BSEL2
RC84 33 Dummy
C_14M_MCH (27)
Buffer thru mode
20100107: RC84 change to 33ohm; PDG 0.8
C_CK505_SRC5_DP RC90 10K Dummy
C_CK505_SRC5_DN RC93 10K Dummy
Dummy RC73 and add RC11 pull-up to +3V; CRB 0.7-12/28/09
RC11 1K +/-1%
CC30 CC31 CC32 1uF +/-10% Dummy
CC33 0.1uF Dummy
FREQ BSEL0 BSEL1 BSEL2
100 1 0 1
133 1 0 0
RC86 10K Dummy
C_CK_BSEL0
RC89 10K Dummy
C_CK_BSEL1
RC87 10K Dummy
C_CK_BSEL2
RC95 10K Dummy
DELL INC.
Title
Clock GEN
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
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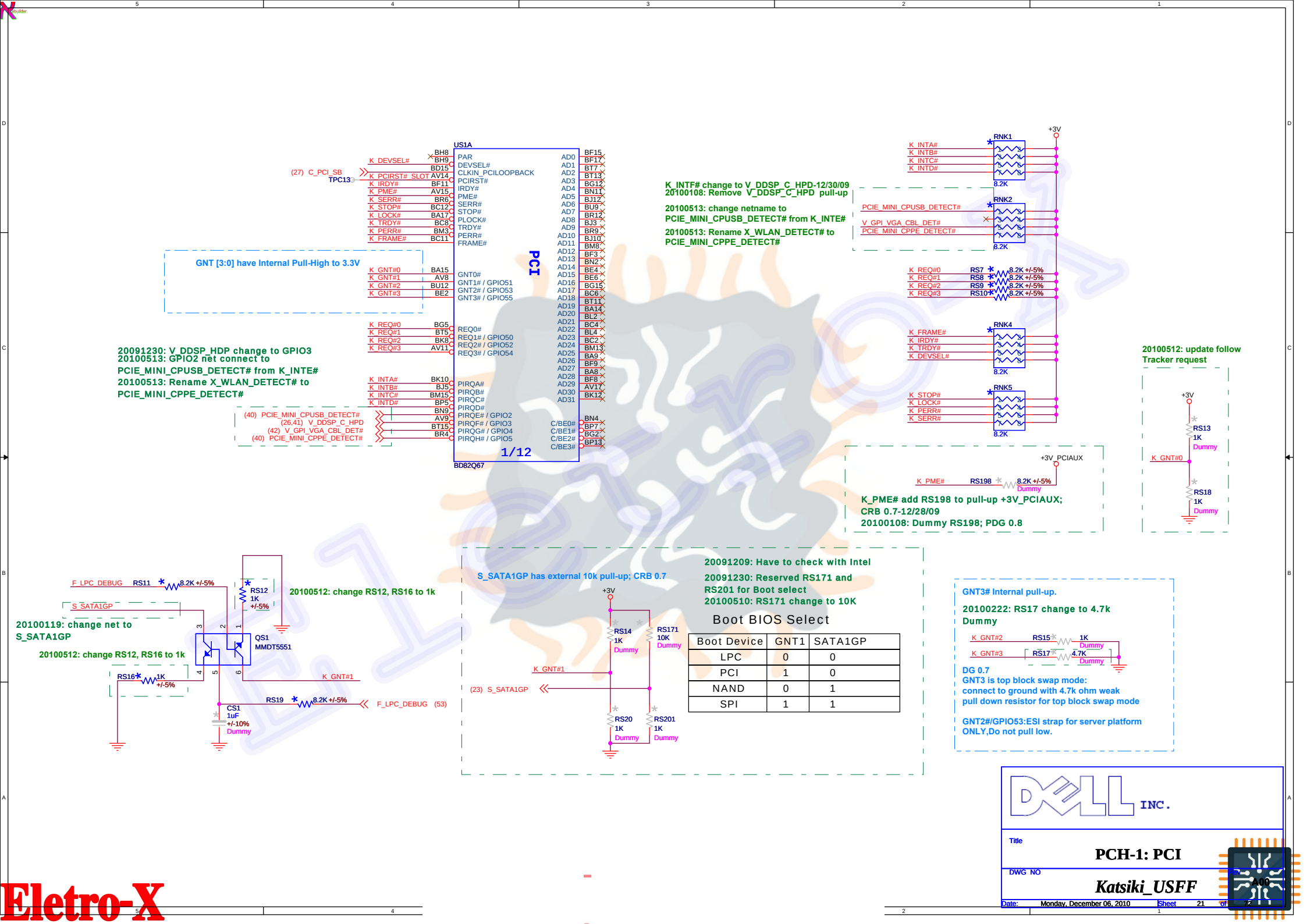
A00
Eletro-X


US1A
PCI
1/12
BD82Q67
(27) C_PCI_SB
TPC13
K_DEVSEL#
K_PCIRST#_SLOT
K_IRDY#
K_PME#
K_SERR#
K_STOP#
K_LOCK#
K_TRDY#
K_PERR#
K_FRAME#
PAR
DEVSEL#
CLKIN_PCILOOPBACK
PCIRST#
IRDY#
PME#
SERR#
STOP#
PLOCK#
TRDY#
PERR#
FRAME#
GNT [3:0] have Internal Pull-High to 3.3V
K_GNT#0
K_GNT#1
K_GNT#2
K_GNT#3
GNT0#
GNT1# / GPIO51
GNT2# / GPIO53
GNT3# / GPIO55
K_REQ#0
K_REQ#1
K_REQ#2
K_REQ#3
REQ0#
REQ1# / GPIO50
REQ2# / GPIO52
REQ3# / GPIO54
20091230: V_DDSP_HDP change to GPIO3
20100513: GPIO2 net connect to
PCIE_MINI_CPUSB_DETECT# from K_INTE#
20100513: Rename X_WLAN_DETECT# to
PCIE_MINI_CPPE_DETECT#
K_INTA#
K_INTB#
K_INTC#
K_INTD#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
(40) PCIE_MINI_CPUSB_DETECT#
(26,41) V_DDSP_C_HPD
(42) V_GPI_VGA_CBL_DET#
(40) PCIE_MINI_CPPE_DETECT#
PIRQE# / GPIO2
PIRQF# / GPIO3
PIRQG# / GPIO4
PIRQH# / GPIO5
C/BE0#
C/BE1#
C/BE2#
C/BE3#
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
K_INTF# change to V_DDSP_C_HPD-12/30/09
20100108: Remove V_DDSP_C_HPD pull-up
20100513: change netname to
PCIE_MINI_CPUSB_DETECT# from K_INTE#
20100513: Rename X_WLAN_DETECT# to
PCIE_MINI_CPPE_DETECT#
RNK1
RNK2
RNK4
RNK5
8.2K
PCIE_MINI_CPUSB_DETECT#
V_GPI_VGA_CBL_DET#
PCIE_MINI_CPPE_DETECT#
RS7
RS8
RS9
RS10
8.2K +/-5%
+3V
20100512: update follow
Tracker request
RS13
RS18
1K
Dummy
+3V_PCIAUX
K_PME#
RS198
K_PME# add RS198 to pull-up +3V_PCIAUX;
CRB 0.7-12/28/09
20100108: Dummy RS198; PDG 0.8
F_LPC_DEBUG
RS11
RS12
RS16
RS19
CS1
1uF
+/-10%
QS1
MMDT5551
20100512: change RS12, RS16 to 1k
20100119: change net to
S_SATA1GP
S_SATA1GP has external 10k pull-up; CRB 0.7
RS14
RS171
10K
RS20
RS201
(23) S_SATA1GP
20091209: Have to check with Intel
20091230: Reserved RS171 and
RS201 for Boot select
20100510: RS171 change to 10K
Boot BIOS Select
Boot Device | GNT1 | SATA1GP
LPC | 0 | 0
PCI | 1 | 0
NAND | 0 | 1
SPI | 1 | 1
GNT3# Internal pull-up.
20100222: RS17 change to 4.7k
Dummy
RS15
RS17
4.7K
DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode
GNT2#/GPIO53:ESI strap for server platform
ONLY,Do not pull low.
DELL INC.
Title
PCH-1: PCI
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
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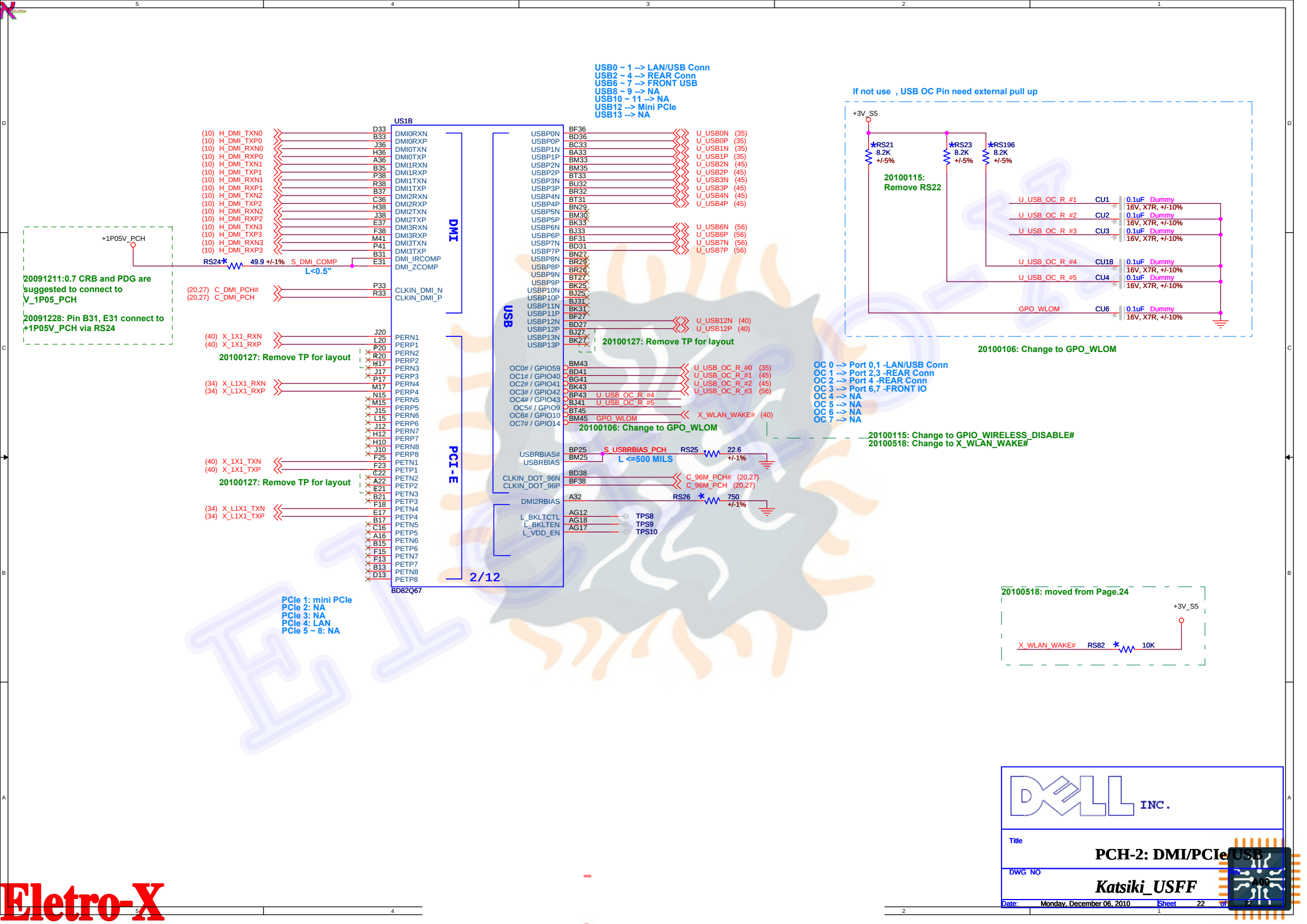
US1B
DMI
PCI-E
USB
2/12
BD82Q67
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_IRCOMP
DMI_ZCOMP
CLKIN_DMI_N
CLKIN_DMI_P
PERN1
PERP1
PERN2
PERP2
PERN3
PERP3
PERN4
PERP4
PERN5
PERP5
PERN6
PERP6
PERN7
PERP7
PERN8
PERP8
PETN1
PETP1
PETN2
PETP2
PETN3
PETP3
PETN4
PETP4
PETN5
PETP5
PETN6
PETP6
PETN7
PETP7
PETN8
PETP8
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
OC0# / GPIO59
OC1# / GPIO40
OC2# / GPIO41
OC3# / GPIO42
OC4# / GPIO43
OC5# / GPIO9
OC6# / GPIO10
OC7# / GPIO14
USBRBIAS#
USBRBIAS
CLKIN_DOT_96N
CLKIN_DOT_96P
DMI2RBIAS
L_BKLTCTL
L_BKLTEN
L_VDD_EN
USB0 ~ 1 --> LAN/USB Conn
USB2 ~ 4 --> REAR Conn
USB6 ~ 7 --> FRONT USB
USB8 ~ 9 --> NA
USB10 ~ 11 --> NA
USB12 --> Mini PCIe
USB13 --> NA
+1P05V_PCH
RS24 49.9 +/-1% S_DMI_COMP
L<0.5"
20091211:0.7 CRB and PDG are suggested to connect to V_1P05_PCH
20091228: Pin B31, E31 connect to +1P05V_PCH via RS24
20100127: Remove TP for layout
20100127: Remove TP for layout
20100127: Remove TP for layout
S_USBRBIAS_PCH
L <=500 MILS
RS25 22.6 +/-1%
RS26 750 +/-1%
20100106: Change to GPO_WLOM
20100127: Remove TP for layout
20100106: Change to GPO_WLOM
OC 0 --> Port 0,1 -LAN/USB Conn
OC 1 --> Port 2,3 -REAR Conn
OC 2 --> Port 4 -REAR Conn
OC 3 --> Port 6,7 -FRONT IO
OC 4 --> NA
OC 5 --> NA
OC 6 --> NA
OC 7 --> NA
20100115: Change to GPIO_WIRELESS_DISABLE#
20100518: Change to X_WLAN_WAKE#
If not use , USB OC Pin need external pull up
+3V_S5
RS21 8.2K +/-5%
RS23 8.2K +/-5%
RS196 8.2K +/-5%
20100115: Remove RS22
U_USB_OC_R_#1 CU1 0.1uF Dummy 16V, X7R, +/-10%
U_USB_OC_R_#2 CU2 0.1uF Dummy 16V, X7R, +/-10%
U_USB_OC_R_#3 CU3 0.1uF Dummy 16V, X7R, +/-10%
U_USB_OC_R_#4 CU18 0.1uF Dummy 16V, X7R, +/-10%
U_USB_OC_R_#5 CU4 0.1uF Dummy 16V, X7R, +/-10%
GPO_WLOM CU6 0.1uF Dummy 16V, X7R, +/-10%
20100518: moved from Page.24
+3V_S5
X_WLAN_WAKE# RS82 10K
PCIe 1: mini PCIe
PCIe 2: NA
PCIe 3: NA
PCIe 4: LAN
PCIe 5 ~ 8: NA
DELL INC.
Title
PCH-2: DMI/PCIe/USB
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
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(40) S_CLINK_CLK_WLAN
(40) S_CLINK_DATA_WLAN
(40) S_CLINK_RST_WLAN#
Dummy RH63 0 S_CLINK_CLK_LAN
Dummy RH64 0 S_CLINK_DATA_LAN
Dummy RH65 0 S_CLINK_RST_LAN#
Add CLINK to PCI-ex1; Follow CRB 0.7-12/03/09

20100121:
RH63,RH64,RH65
change to 0 ohm

S_INIT3_3VB RS27 1K Dummy

This signal should not be pulled low on EDS 0.5- Sherlock 10/27/09

20100107:Remove test points

20100107: Remove RS47, RS48 and connect S_PCH_MEPWROK_R to S_PCH_MEPWROK directly

20100104: Add TPS23,TPS25 and remove RS29,RS30,RS33, RS34 since useless this function

US1C

CLINK
SATA
FAN
GPIO
HOST

TP13
TP14
CL_CLK1
CL_DATA1
CL_RST1#
APWROK
PWM0
PWM1
PWM2
PWM3
TACH0 / GPIO17
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
TACH4 / GPIO68
TACH5/ GPIO69
TACH6 / GPIO70
TACH7 / GPIO71
SST
SCLOCK / GPIO22
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SLOAD / GPIO38
NC_1
NC_2
NC_3
NC_4
NC_5
3/12
BD82Q67

S_CLINK_CLK_LAN BA50
S_CLINK_DATA_LAN BF50
S_CLINK_RST_LAN# BF49
(66) PCH_MEPWRGD BC46

TPS23 S_TP_CPUFAN_PWM BN21
TPS25 S_TP_CHAFAN1_PWM BT21
TPS18 S_TP_CHAFAN2_PWM BM20
TPS19 S_TP_CHAFAN3_PWM BN19

(31) S_GPI_CHASSIS_ID1 BT17
(31) S_GPI_CHASSIS_ID0 BR19
(30) S_GPI_PCH_HS_DET# BA22
(31) S_GPI_SKU2 BR16

20100512: change net name to S_GPI_BRD_REV2

(31) S_GPI_BRD_REV2 BU16
TPS26 O_PRT_DET# BM18
(56) S_USB_HDR_DET# BN17
+3V RS144 10K BP15

Add RS 144 and pull-up to +3V; CRB 0.7-12/07/09

TPS28 BC43

FAN control from SMSC 5544 without using SST

S_PCH_CONFIG_JUMPER BA53
A_FP_PRES# BF55
(43) S_GPIO48_PU AW53
(31) S_GPI_CHASSIS_ID2 BE54

TPS30 A54
TPS31 A52
TPS32 F57
TPS33 D57
AY20

20100226: Remove TPS34 for layout

SATA0RXN AC56
SATA0RXP AB55
SATA0TXN AE46
SATA0TXP AE44
SATA1RXN AA53
SATA1RXP AA56
SATA1TXN AG49
SATA1TXP AG47
SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55
SATA4RXN AN49
SATA4RXP AN50
SATA4TXN AT50
SATA4TXP AT49
SATA5RXN AT46
SATA5RXP AT44
SATA5TXN AV50
SATA5TXP AV49
CLKIN_SATA_N / CKSSCD_N AF55
CLKIN_SATA_P / CKSSCD_P AG56
SATALED# BF57
SATAICOMPI AJ55
SATAICOMPO AJ53
SATA0GP / GPIO21 BC54
SATA1GP / GPIO19 AY52
SATA2GP / GPIO36 BB55
SATA3GP / GPIO37 BG53
SATA4GP / GPIO16 AU56
SATA5GP / GPIO49 BA56
SATA3COMPI AE54
SATA3RBIAS AC52
SATA3RCOMPO AE52
TP8 AB18
A20GATE BB57
INIT3_3V# BN56
RCIN# BG56
SERIRQ AV52
THRMTRIP# E56
PECI H48
PMSYNCH F55

T_SATA_RXN0 (43)
T_SATA_RXP0 (43)
T_SATA_TXN0 (43)
T_SATA_TXP0 (43)
T_SATA_RXN1 (43)
T_SATA_RXP1 (43)
T_SATA_TXN1 (43)
T_SATA_TXP1 (43)

T_ESATA_RXN4 (44)
T_ESATA_RXP4 (44)
T_ESATA_TXN4 (44)
T_ESATA_TXP4 (44)

20100127: Remove TP for layout

C_SATA_PCH# (20,27)
C_SATA_PCH (20,27)
T_SATALED# (56)
S_SATARBIAS_PCH RS36 37.4 Ohm +/-1%
+1P05V_PCH
check : using 37.4 ohm in DG , 49.9 ohm in CRB
20091209: CRB0.7 and PDG0.7 are suggested 37.4 ohm

S_GPI_BRD_REV0 (31)
S_SATA1GP (21)
S_TP_GPIO36 TPS27
S_TP_GPIO37 TPS39
H_SKTOCC_R_# TMIN_SHIFT (32)

20091209: CRB0.7 V_DDSP_C_HPD is connected to PCH pin N2 only , no connected to GPIO19,check whether RS35 need stuff for meet Intel PDG ?

20091230: Change to S_SATA1GP for Boot Select

20100503: S_GPI_CHASSIS_ID0/S_GPI_CHASSIS_ID1 change to GPIO1/GPIO17 from GPIO36/GPIO37, and add TPS27/TPS39 net name S_TP_GPIO36/S_TP_GPIO37

+1P05V_PCH
RS37 49.9 +/-1%
RS38 750 +/-1%

20100107:Remove test points

O_GA20 (32)
S_INIT3_3VB (53)
O_KB_RST# (32)
F_SERIRQ# (32,46)
H_THERMTRIP# (9)
RS39 0 Dummy
H_PECI (9,32)
H_PM_SYNC (9)

Dummy RS39; SMSC suggestion-12/08/09

+3V
O_KB_RST# RS28 10K
O_GA20 RS31 10K
F_SERIRQ# RS32 10K

20091221: RS35 stuffed for meet CRB0.7

20100503: Removed RS52, RS54

S_GPIO48_PU RS56 10K
S_GPI_PCH_HS_DET# RS58 10K
RS61 10K
(56) A_FP_PRES# O_PRT_DET# RS109 10K

20100119: Add RS109 for O_PRT_DET#

20100503: S_GPI_CHASSIS_ID0/S_GPI_CHASSIS_ID1 change to GPIO1/GPIO17 from GPIO36/GPIO37, and add TPS27/TPS39 net name S_TP_GPIO36/S_TP_GPIO37

PCH_CONFIG
+3V
RS55 1K
S_PCH_CONFIG_JUMPER
RS60 4.7K Dummy

20100107: Remove RS47, RS48 and connect S_PCH_MEPWROK_R to S_PCH_MEPWROK directly

+3V
RS53 10K
20100226: RS53 change to 10k
H_SKTOCC_R_#
RS57 0 Dummy
H_SKTOCC# (9,24)
RS59 10K Dummy
STUFF RS57 FOR ME ON CPU PRESENT DETECTION

DELL INC.

Title: PCH-3: SATA/HOST/FAN
DWG NO: Katsiki_USFF
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20100707: add RS124 connect A_Z_SDOUT_R to A_Z_SDO_R
20100709: Dummy RS124

20091223: signal rename to S_SUSWARN#

20100503: Pop RS72 , for intel request

CPT FLASH DESCRIPT OR OVERRIDE.HIGH FOR OVERRIDE

OD PLL VR SUPPLY SEL(internal pull down)
1.8V SUPPLY WHEN SAMPLED LOW
1.5V SUPPLY WHEB SAMPLED HIGH

20091223: Add RS151, RS197
DS mode:
20100104: Remove RS151, P.64 has same circuit

20100510: RS90 change to 10 Ohm
20100524: RS90 change to 10 Ohm
20100707: PCH Pin_BT23 net name rename to A_Z_SDO_R from A_Z_SDOUT_R
20100709: PCH Pin_BT23 net name rename back to A_Z_SDOUT_R

Internal pull-up

SPKR Control Option of SIO / PCH

S_SPKR
Pop To Enable No-Reboot
linternal pull-down.

US1D

LPC
AUDIO
RTC
SMB
SPI
4/12

20091209: Stuff for IGC function
20091225: Unstuff for disable IGC
20100505: X_WLAN_WAKE# change to GPIO8 ; Removed S_IGC_EN# and RS70
20100518: GPIO8 change to S_TP_GP8 and add TPS40

20091223: BU46 signal rename to S_SUSWARN#

20091223: BP53 signal name change to H_SKTOCC# .

20100127: change to TPS38, SERVICE_MODE circuit update

20091221: BD43 removed TPS38 and rename signal to S_SLP_SUS# ; BT37 rename S_RSMRST# to S_PCH_DPWROK_R ; BP45 rename to S_SUS_PWR_ACK

20100106: Add RS173

20091221: Dummy RS80 follow CRB0.7

20100106: Reserved RS151 for Disable 1.05V Regulator

High: Enable 1.05V Regulator
Low: Disable 1.05V Regulator
Has a weak Internal Pull-High
Reserved for CPU VR and TPM type

20091216: RS87 used 1k , PDG0.7
20100325: pop RS87

20091224: change to +3V

20100104: Dummy RS87; follow CRB 0.7

20091224: S_TP_SLP_S5# change to S_PEG_B_CLKREQ#

20091221: Add RS146, RS149
DS mode: RS146 pop, RS149 dis-pop
non-DS mode: RS146 dis-pop, RS149 pop

20100505: add RS124 pull-up to +3V_S5 for GPIO60
20100518: Delete RS124 and S_PCH_GPIO60

20091209:CRB0.7 is only 1.1 k ohm pull up, PDG0.7 is 4.75K ohm pull up
RS94 Dummy ; CRB 0.7-12/10/09
20100112: change RS93 to 4.75K ohm;PDG 0.8
20100503: RS93 change to 200 Ohm

20091223: BU49 signal name change to X_WLAN_WAKE#
20100504: GPIO60 change to S_PCH_GPIO60 and pull-up to +3V_S5 via 2.2k
20100518: GPIO60 change to GPIO_WIRELESS_DISABLE#

Integrated TPM
High to Enable
Low to Disable
Internal pull-down

SMSC recommend 01/13/11

Internal 1.1V and VCCME regulator enable(high)/disable(low)

RTC X'TAL

CLR_SRTC

20091214: CS4 stuffed

20100115: Remove RS109,RS110; vender suggestion

Near to Pch

FVS
TEST POINT

CLOSE TO PCH
0 OHM FOR DEFENSIVE DESIGN
66MHZ SPI TOPOLOGY,

Title: PCH-4: LPC/HDA/RTC/SMB/SPI
DWG NO: Katsiki_USFF
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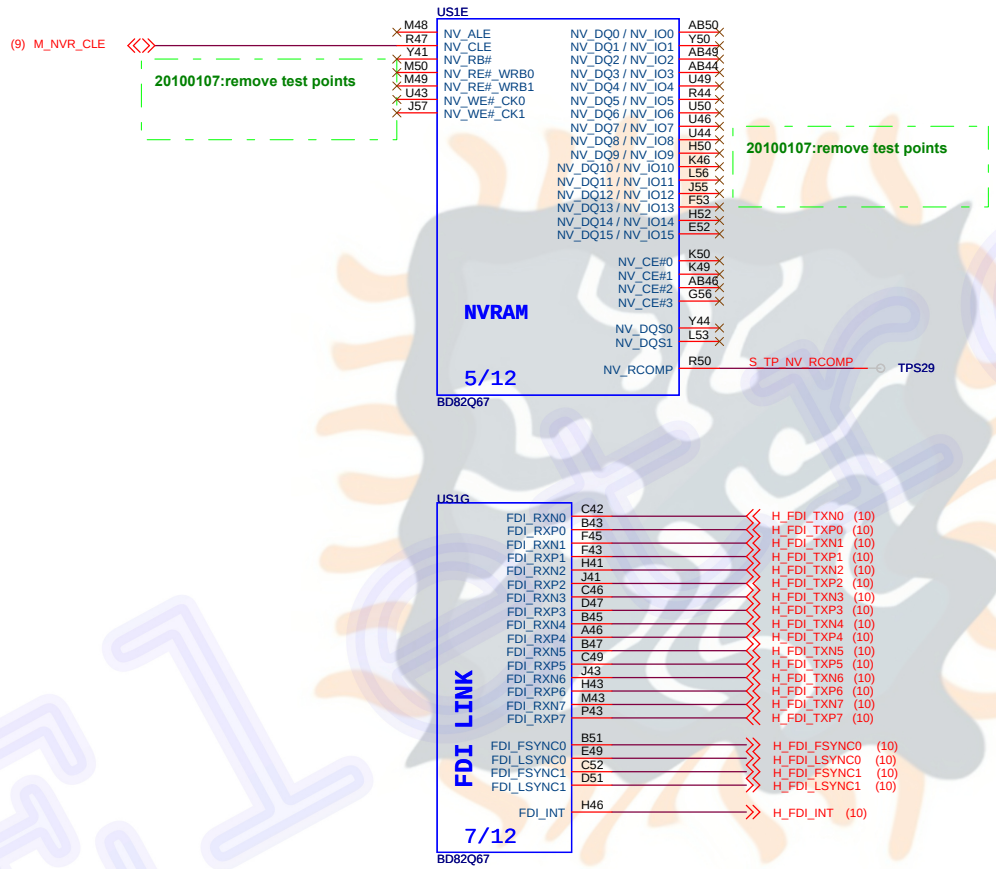
20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.

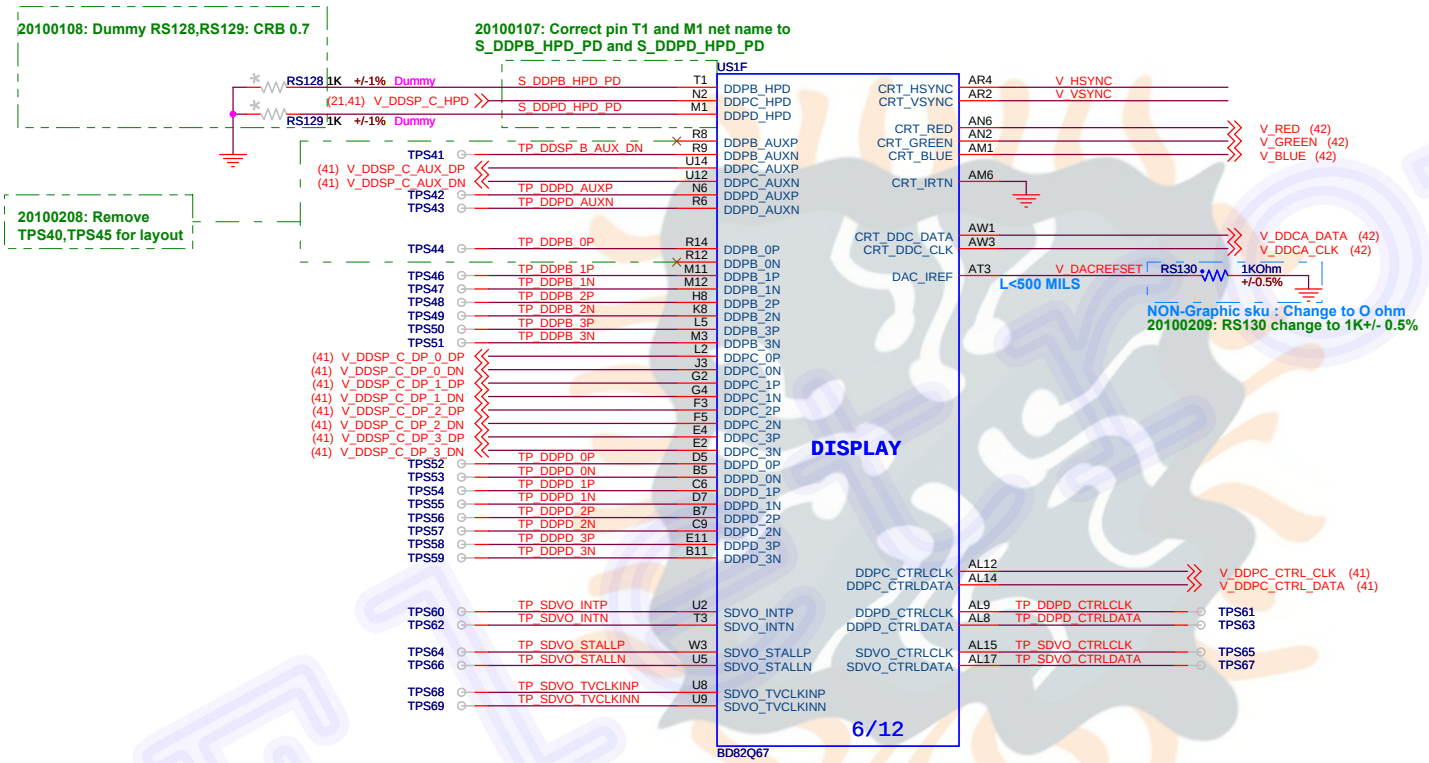


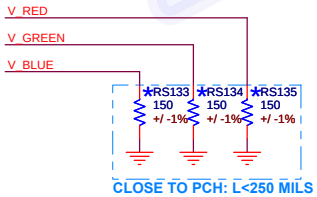
DELL INC.

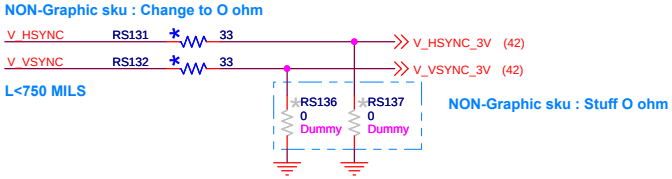
Title
PCH-5/7: NVRAM/FDI

DWG NO
Katsiki_USFF

Date: Monday, December 06, 2010 Sheet 25 of 72







DELL INC.

Title
PCH-6: Display

DWG NO
Katsiki_USFF

Rev A00

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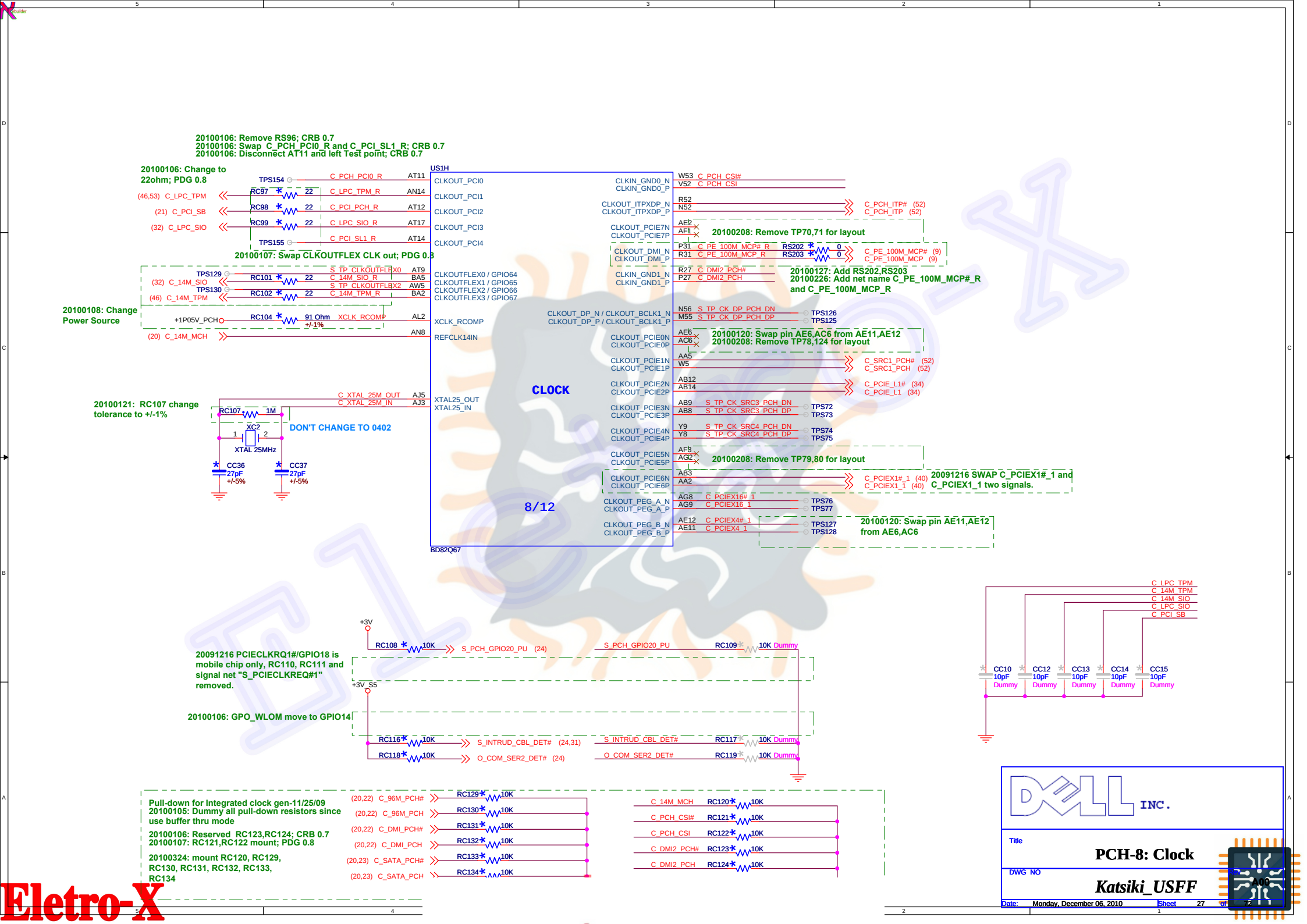
20100106: Remove RS96; CRB 0.7
20100106: Swap C_PCH_PCI0_R and C_PCI_SL1_R; CRB 0.7
20100106: Disconnect AT11 and left Test point; CRB 0.7
20100106: Change to 22ohm; PDG 0.8
20100107: Swap CLKOUTFLEX CLK out; PDG 0.8
20100108: Change Power Source
20100121: RC107 change tolerance to +/-1%
DON'T CHANGE TO 0402
US1H
CLOCK
8/12
BD82Q67
20100208: Remove TP70,71 for layout
20100127: Add RS202,RS203
20100226: Add net name C_PE_100M_MCP#_R and C_PE_100M_MCP_R
20100120: Swap pin AE6,AC6 from AE11,AE12
20100208: Remove TP78,124 for layout
20100208: Remove TP79,80 for layout
20091216 SWAP C_PCIEX1#_1 and C_PCIEX1_1 two signals.
20100120: Swap pin AE11,AE12 from AE6,AC6
20091216 PCIECLKRQ1#/GPIO18 is mobile chip only, RC110, RC111 and signal net "S_PCIECLKREQ#1" removed.
20100106: GPO_WLOM move to GPIO14
Pull-down for Integrated clock gen-11/25/09
20100105: Dummy all pull-down resistors since use buffer thru mode
20100106: Reserved RC123,RC124; CRB 0.7
20100107: RC121,RC122 mount; PDG 0.8
20100324: mount RC120, RC129, RC130, RC131, RC132, RC133, RC134
DELL INC.
Title
PCH-8: Clock
DWG NO
Katsiki_USFF
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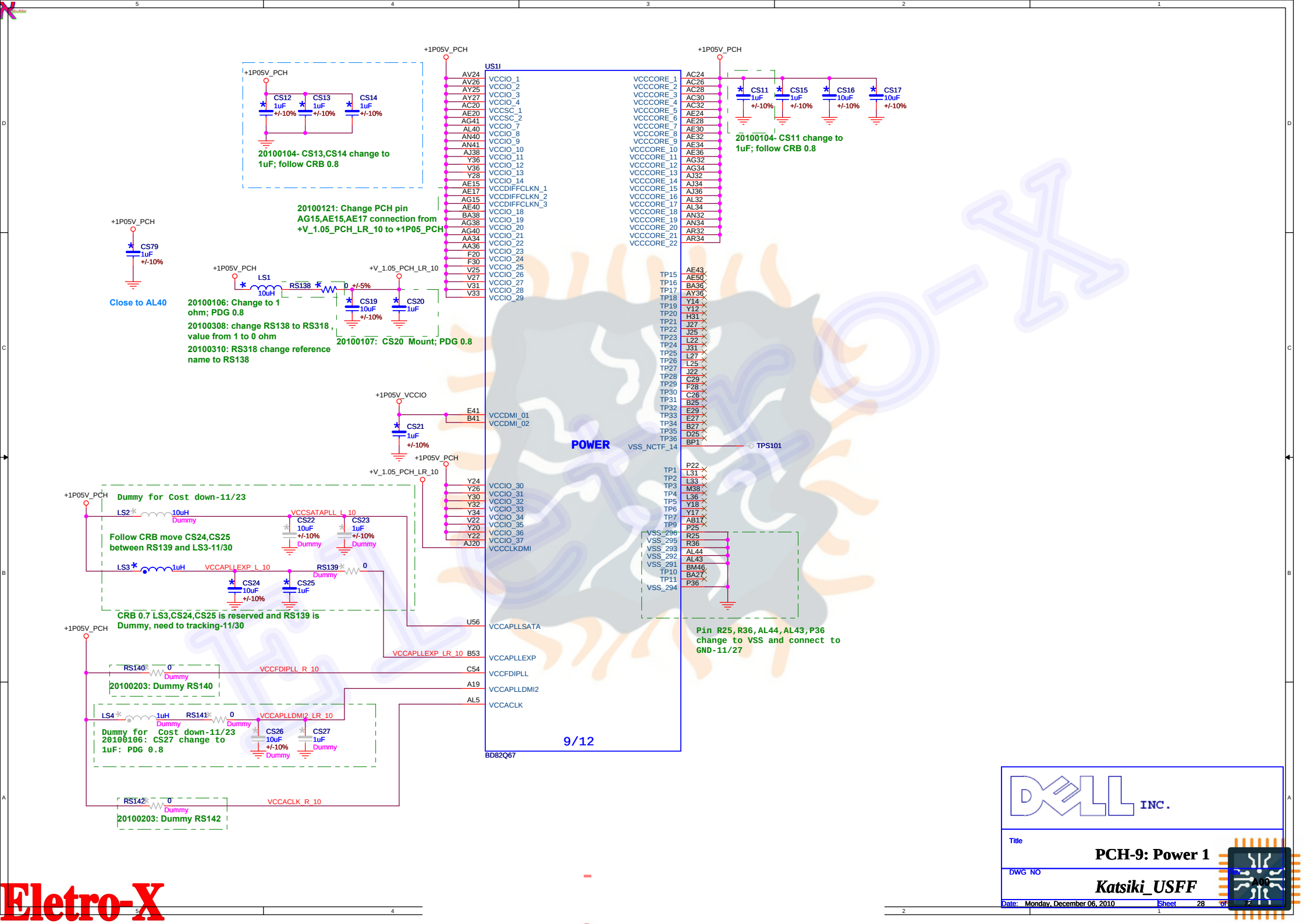

DELL INC.

Title: PCH-9: Power 1

DWG NO: Katsiki_USFF

Rev: A00

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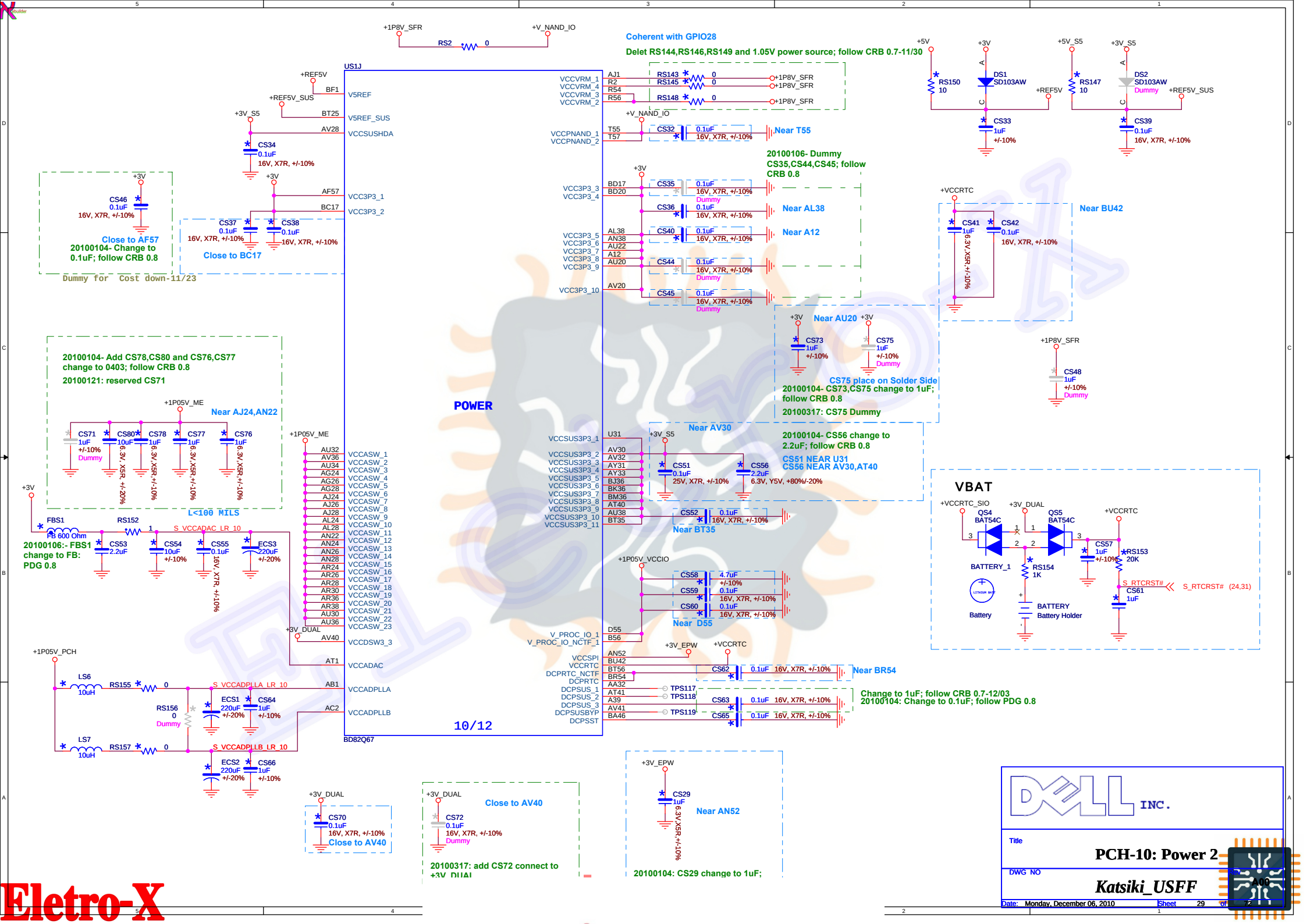
Eletro-X


POWER
US1J
BD82Q67
10/12
+1P8V_SFR
RS2
0
+V_NAND_IO
Coherent with GPIO28
Delet RS144,RS146,RS149 and 1.05V power source; follow CRB 0.7-11/30
+5V
+3V
+5V_S5
+3V_S5
RS150
10
DS1
SD103AW
RS147
DS2
Dummy
+REF5V_SUS
CS33
1uF
+/-10%
CS39
0.1uF
16V, X7R, +/-10%
+REF5V
+REF5V_SUS
BF1
V5REF
BT25
V5REF_SUS
AV28
VCCSUSHDA
CS34
0.1uF
16V, X7R, +/-10%
AF57
VCC3P3_1
BC17
VCC3P3_2
CS46
0.1uF
16V, X7R, +/-10%
Close to AF57
20100104- Change to 0.1uF; follow CRB 0.8
Dummy for Cost down-11/23
CS37
0.1uF
16V, X7R, +/-10%
CS38
0.1uF
16V, X7R, +/-10%
Close to BC17
VCCVRM_1
VCCVRM_4
VCCVRM_3
VCCVRM_2
AJ1
R2
R54
R56
RS143
RS145
RS148
0
+1P8V_SFR
VCCPNAND_1
VCCPNAND_2
T55
T57
CS32
0.1uF
16V, X7R, +/-10%
Near T55
20100106- Dummy CS35,CS44,CS45; follow CRB 0.8
VCC3P3_3
VCC3P3_4
BD17
BD20
CS35
CS36
Near AL38
VCC3P3_5
VCC3P3_6
VCC3P3_7
VCC3P3_8
VCC3P3_9
AL38
AN38
AU22
A12
AU20
CS40
Near A12
CS44
VCC3P3_10
AV20
CS45
Dummy
+VCCRTC
CS41
1uF
6.3V,X5R,+/-10%
CS42
0.1uF
16V, X7R, +/-10%
Near BU42
Near AU20
CS73
CS75
CS75 place on Solder Side
20100104- CS73,CS75 change to 1uF; follow CRB 0.8
20100317: CS75 Dummy
CS48
20100104- Add CS78,CS80 and CS76,CS77 change to 0403; follow CRB 0.8
20100121: reserved CS71
+1P05V_ME
Near AJ24,AN22
CS71
CS80
CS78
CS77
CS76
L<100 MILS
+1P05V_ME
AU32
AV36
AU34
AG24
AG26
AG28
AJ24
AJ26
AJ28
AL24
AL28
AN22
AN24
AN26
AN28
AR24
AR26
AR28
AR30
AR36
AR38
AU30
AU36
VCCASW_1
VCCASW_2
VCCASW_3
VCCASW_4
VCCASW_5
VCCASW_6
VCCASW_7
VCCASW_8
VCCASW_9
VCCASW_10
VCCASW_11
VCCASW_12
VCCASW_13
VCCASW_14
VCCASW_15
VCCASW_16
VCCASW_17
VCCASW_18
VCCASW_19
VCCASW_20
VCCASW_21
VCCASW_22
VCCASW_23
+3V_DUAL
AV40
VCCDSW3_3
AT1
VCCADAC
AB1
VCCADPLLA
AC2
VCCADPLLB
VCCSUS3P3_1
U31
VCCSUS3P3_2
VCCSUS3P3_3
VCCSUS3P3_4
VCCSUS3P3_5
VCCSUS3P3_6
VCCSUS3P3_7
VCCSUS3P3_8
VCCSUS3P3_9
VCCSUS3P3_10
VCCSUS3P3_11
AV30
AV32
AY31
AY33
BJ36
BK36
BM36
AT40
AU38
BT35
+3V_S5
Near AV30
CS51
0.1uF
25V, X7R, +/-10%
CS56
2.2uF
6.3V, Y5V, +80%/-20%
20100104- CS56 change to 2.2uF; follow CRB 0.8
CS51 NEAR U31
CS56 NEAR AV30,AT40
CS52
0.1uF
16V, X7R, +/-10%
Near BT35
VBAT
+VCCRTC_SIO
QS4
BAT54C
+3V_DUAL
QS5
BAT54C
+VCCRTC
CS57
1uF
+/-10%
RS153
20K
BATTERY_1
RS154
1K
S_RTCRST#
S_RTCRST# (24,31)
CS61
1uF
Battery
BATTERY
Battery Holder
+1P05V_VCCIO
CS58
4.7uF
+/-10%
CS59
0.1uF
16V, X7R, +/-10%
CS60
0.1uF
16V, X7R, +/-10%
Near D55
V_PROC_IO_1
V_PROC_IO_NCTF_1
D55
B56
+3V_EPW
+VCCRTC
VCCSPI
VCCRTC
DCPRTC_NCTF
DCPRTC
AN52
BU42
BT56
BR54
AA32
CS62
0.1uF
16V, X7R, +/-10%
Near BR54
DCPSUS_1
DCPSUS_2
DCPSUS_3
DCPSUSBYP
DCPSST
AT41
A39
AV41
BA46
TPS117
TPS118
TPS119
CS63
CS65
Change to 1uF; follow CRB 0.7-12/03
20100104: Change to 0.1uF; follow PDG 0.8
+1P05V_PCH
LS6
10uH
RS155
0
S_VCCADPLLA_LR_10
ECS1
220uF
+/-20%
CS64
1uF
+/-10%
RS156
0
Dummy
LS7
10uH
RS157
0
S_VCCADPLLB_LR_10
ECS2
220uF
+/-20%
CS66
1uF
+/-10%
FBS1
RS 600 Ohm
RS152
1
S_VCCADAC_LR_10
20100106:- FBS1 change to FB: PDG 0.8
CS53
2.2uF
CS54
10uF
+/-10%
CS55
0.1uF
16V, X7R, +/-10%
ECS3
220uF
+/-20%
+3V_DUAL
CS70
0.1uF
16V, X7R, +/-10%
Close to AV40
+3V_DUAL
CS72
0.1uF
16V, X7R, +/-10%
Dummy
Close to AV40
20100317: add CS72 connect to +3V_DUAL
+3V_EPW
CS29
1uF
6.3V,X5R,+/-10%
Near AN52
20100104: CS29 change to 1uF;
DELL INC.
Title
PCH-10: Power 2
DWG NO
Katsiki_USFF
Rev
A00
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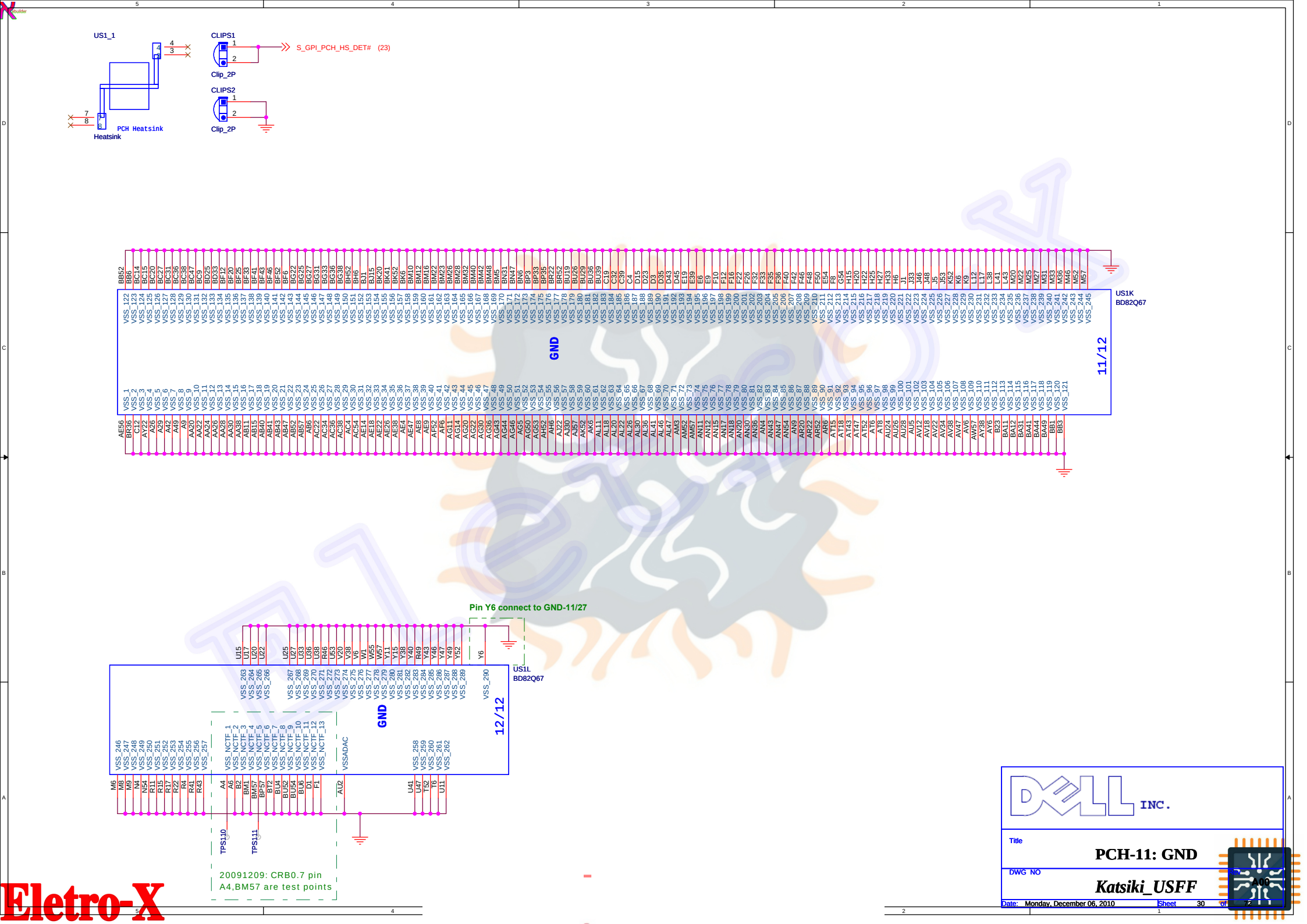
Eletro-X


US1_1
PCH Heatsink
Heatsink
CLIPS1
Clip_2P
S_GPI_PCH_HS_DET# (23)
CLIPS2
Clip_2P
US1K
BD82Q67
GND
11/12
US1L
BD82Q67
GND
12/12
Pin Y6 connect to GND-11/27
TPS110
TPS111
20091209: CRB0.7 pin
A4,BM57 are test points
DELL INC.
Title
PCH-11: GND
DWG NO
Katsiki_USFF
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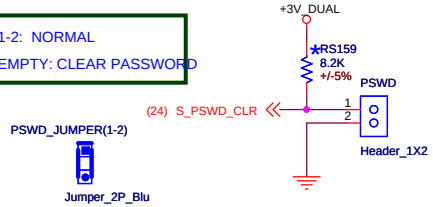
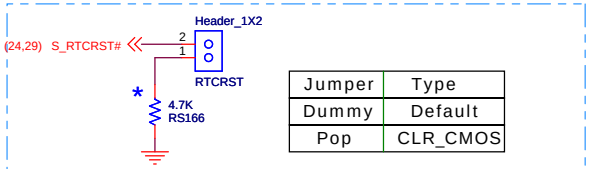
A00
Eletro-X

Clear Password

1-2: NORMAL
EMPTY: CLEAR PASSWORD

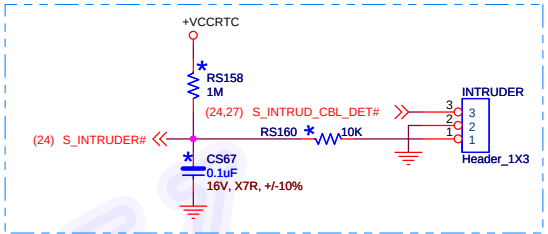


CLR_CMOS

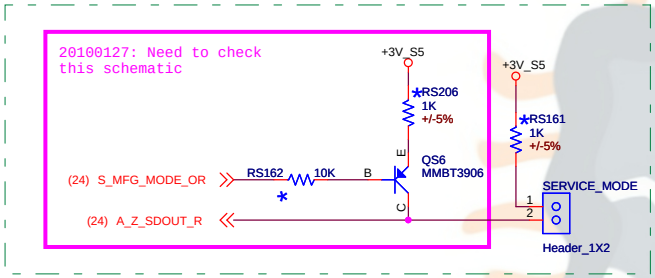


Jumper	Type
Dummy	Default
Pop	CLR_CMOS

Chassis Intruder



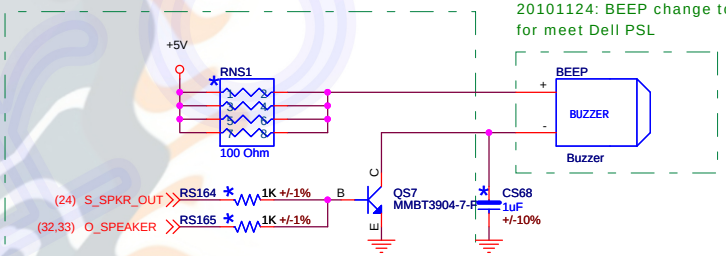
SERVICE_MODE



20100127: Update SERVICE_MODE circuit
20100316: RS206 and RS161 change pull-up to +3V_S5 ; Value change to 1k
20100503: QS6 change to MMBT3906

BEEP

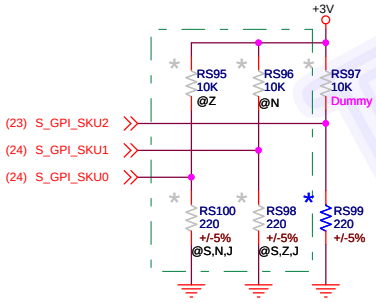
20100326: BEEP change to KPM-G1205A-3558, check link
20101124: BEEP change to AAC_HCM1206A-2.9mm-G for meet Dell PSL



20101012: RS165 stuffed, BEEP power change to +5V, QS7 change from MMDT5551 to MMBT3904

SKU ID

20100203: Dummy RS98 and RS96; TPM configuration update
20100525: RS95, RS96, RS100, RS98 add SKU pop option



SKU ID

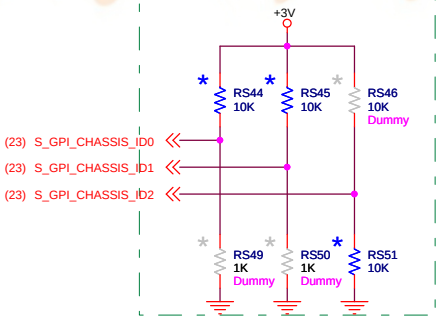
SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

Chassis ID

check : need to update table
20100324: Update Chassis ID Table

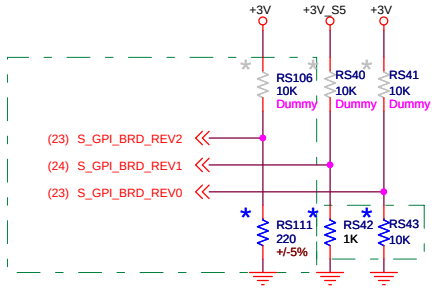
ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Tambor
0	0	0	MT/DT
0	1	1	USFF

20100106: change to 1k since have internal pull-up 10k
20100203: Dummy RS49,RS50,RS46 and Mount RS44,RS45,RS51; USFF configuration
20100503: RS44, RS45 change to 10kOhm ; RS49, RS50 change to 1kOhm



BOARD ID

20100512: change net name from S_GPI_SKU3 to S_GPI_BRD_REV2 ; dummy RS106 and mount RS111 ; update Board ID Table



20100106: change to 1k since have internal pull-up 10k

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

DELL INC.

Title: PCH MISC Conn/BUZ
DWG NO: Katsiki_USFF
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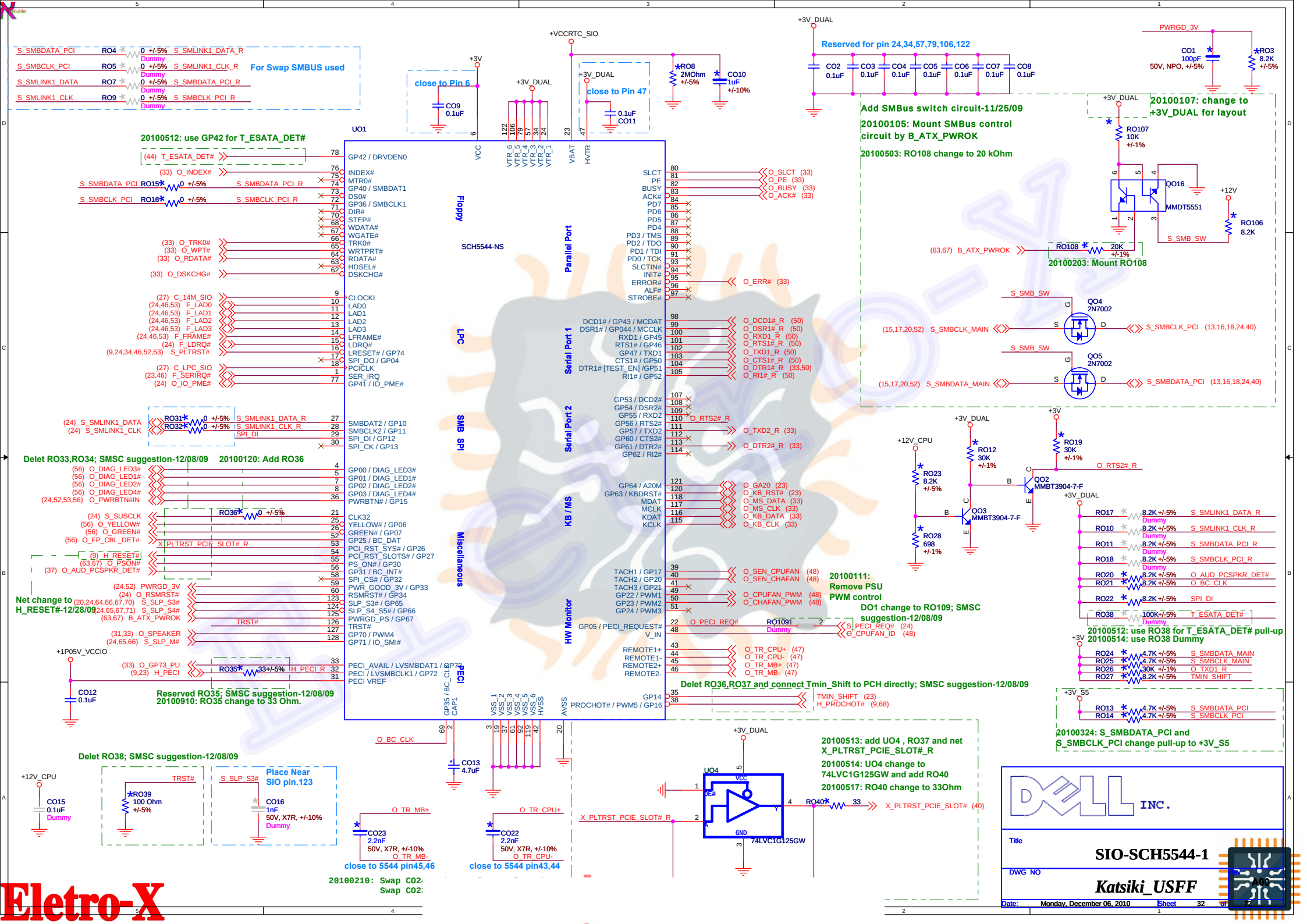
UO1
SCH5544-NS
Floppy
LPC
SMB SPI
PECI
Parallel Port
Serial Port 1
Serial Port 2
KB / MS
Miscellaneous
HW Monitor
GP42 / DRVDEN0
INDEX#
MTR0#
GP40 / SMBDAT1
DS0#
GP36 / SMBCLK1
DIR#
STEP#
WDATA#
WGATE#
TRK0#
WRTPRT#
RDATA#
HDSEL#
DSKCHG#
CLOCKI
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ#
LRESET# / GP74
SPI_DO / GP04
PCICLK
SER_IRQ
GP41 / IO_PME#
SMBDAT2 / GP10
SMBCLK2 / GP11
SPI_DI / GP12
SPI_CK / GP13
GP00 / DIAG_LED3#
GP01 / DIAG_LED1#
GP02 / DIAG_LED2#
GP03 / DIAG_LED4#
PWRBTN# / GP15
CLK32
YELLOW# / GP06
GREEN# / GP07
GP25 / BC_DAT
PCI_RST_SYS# / GP26
PCI_RST_SLOTS# / GP27
PS_ON# / GP30
GP31 / BC_INT#
SPI_CS# / GP32
PWR_GOOD_3V / GP33
RSMRST# / GP34
SLP_S3# / GP65
SLP_S4_S5# / GP66
PWRGD_PS / GP67
TRST#
GP70 / PWM4
GP71 / IO_SMI#
PECI_AVAIL / LVSMBDAT1 / GP72
PECI / LVSMBCLK1 / GP72
PECI VREF
SLCT
PE
BUSY
ACK#
PD7
PD6
PD5
PD4
PD3 / TMS
PD2 / TDO
PD1 / TDI
PD0 / TCK
SLCTIN#
INIT#
ERROR#
ALF#
STROBE#
DCD1# / GP43 / MCDAT
DSR1# / GP044 / MCCLK
RXD1 / GP45
RTS1# / GP46
GP47 / TXD1
CTS1# / GP50
DTR1# [TEST_EN] /GP51
RI1# / GP52
GP53 / DCD2#
GP54 / DSR2#
GP55 / RXD2
GP56 / RTS2#
GP57 / TXD2
GP60 / CTS2#
GP61 / DTR2#
GP62 / RI2#
GP64 / A20M
GP63 / KBDRST#
MDAT
MCLK
KDAT
KCLK
TACH1 / GP17
TACH2 / GP20
TACH3 / GP21
GP22 / PWM1
GP23 / PWM2
GP24 / PWM3
GP05 / PECI_REQUEST#
V_IN
REMOTE1+
REMOTE1-
REMOTE2+
REMOTE2-
GP14
PROCHOT# / PWM5 / GP16
VCC
VBAT
HVTR
AVSS
HVSS
GP35 / BC_CLK
CAP1
VTR_6
VTR_5
VTR_4
VTR_3
VTR_2
VTR_1
+3V_DUAL
+VCCRTC_SIO
+3V
close to Pin 6
close to Pin 47
CO9 0.1uF
CO11 0.1uF
RO8 2MOhm +/-5%
CO10 1uF +/-10%
Reserved for pin 24,34,57,79,106,122
CO2 0.1uF
CO3 0.1uF
CO4 0.1uF
CO5 0.1uF
CO6 0.1uF
CO7 0.1uF
CO8 0.1uF
PWRGD_3V
CO1 100pF 50V, NPO, +/-5%
RO3 8.2K +/-5%
For Swap SMBUS used
S_SMBDATA_PCI RO4 0 +/-5% Dummy S_SMLINK1_DATA_R
S_SMBCLK_PCI RO5 0 +/-5% Dummy S_SMLINK1_CLK_R
S_SMLINK1_DATA RO7 0 +/-5% Dummy S_SMBDATA_PCI_R
S_SMLINK1_CLK RO9 0 +/-5% Dummy S_SMBCLK_PCI_R
20100512: use GP42 for T_ESATA_DET#
(44) T_ESATA_DET#
(33) O_INDEX#
S_SMBDATA_PCI RO15 0 +/-5% S_SMBDATA_PCI_R
S_SMBCLK_PCI RO16 0 +/-5% S_SMBCLK_PCI_R
(33) O_TRK0#
(33) O_WPT#
(33) O_RDATA#
(33) O_DSKCHG#
(27) C_14M_SIO
(24,46,53) F_LAD0
(24,46,53) F_LAD1
(24,46,53) F_LAD2
(24,46,53) F_LAD3
(24,46,53) F_FRAME#
(24) F_LDRQ#
(9,24,34,46,52,53) S_PLTRST#
(27) C_LPC_SIO
(23,46) F_SERIRQ#
(24) O_IO_PME#
(24) S_SMLINK1_DATA
(24) S_SMLINK1_CLK
RO31 0 +/-5% S_SMLINK1_DATA_R
RO32 0 +/-5% S_SMLINK1_CLK_R
SPI_DI
Delet RO33,RO34; SMSC suggestion-12/08/09
20100120: Add RO36
(56) O_DIAG_LED3#
(56) O_DIAG_LED1#
(56) O_DIAG_LED2#
(56) O_DIAG_LED4#
(24,52,53,56) O_PWRBTN#IN
(24) S_SUSCLK
(56) O_YELLOW#
(56) O_GREEN#
(56) O_FP_CBL_DET#
RO36 0 +/-5%
X_PLTRST_PCIE_SLOT#_R
(9) H_RESET#
(63,67) O_PSON#
(37) O_AUD_PCSPKR_DET#
Net change to H_RESET#-12/28/09
(24,52) PWRGD_3V
(24) O_RSMRST#
(20,24,64,66,67,70) S_SLP_S3#
(24,65,67,71) S_SLP_S4#
(63,67) B_ATX_PWROK
TRST#
(31,33) O_SPEAKER
(24,65,66) S_SLP_M#
+1P05V_VCCIO
(33) O_GP73_PU
(9,23) H_PECI
RO35 33+/-5% H_PECI_R
CO12 0.1uF
Reserved RO35; SMSC suggestion-12/08/09
20100910: RO35 change to 33 Ohm.
Delet RO38; SMSC suggestion-12/08/09
+12V_CPU
CO15 0.1uF Dummy
TRST#
RO39 100 Ohm +/-5%
S_SLP_S3#
Place Near SIO pin.123
CO16 1nF 50V, X7R, +/-10% Dummy
O_BC_CLK
CO13 4.7uF
O_TR_MB+
CO23 2.2nF 50V, X7R, +/-10% O_TR_MB-
close to 5544 pin45,46
O_TR_CPU+
CO22 2.2nF 50V, X7R, +/-10% O_TR_CPU-
close to 5544 pin43,44
20100210: Swap CO2
Swap CO2
O_SLCT (33)
O_PE (33)
O_BUSY (33)
O_ACK# (33)
O_ERR# (33)
O_DCD1#_R (50)
O_DSR1#_R (50)
O_RXD1_R (50)
O_RTS1#_R (50)
O_TXD1_R (50)
O_CTS1#_R (50)
O_DTR1#_R (33,50)
O_RI1#_R (50)
O_RTS2# R
O_TXD2_R (33)
O_DTR2#_R (33)
O_GA20 (23)
O_KB_RST# (23)
O_MS_DATA (33)
O_MS_CLK (33)
O_KB_DATA (33)
O_KB_CLK (33)
O_SEN_CPUFAN (48)
O_SEN_CHAFAN (48)
O_CPUFAN_PWM (48)
O_CHAFAN_PWM (48)
O_PECI_REQ#
RO1091 Dummy
S_PECI_REQ# (24)
O_CPUFAN_ID (48)
O_TR_CPU+ (47)
O_TR_CPU- (47)
O_TR_MB+ (47)
O_TR_MB- (47)
Delet RO36,RO37 and connect Tmin_Shift to PCH directly; SMSC suggestion-12/08/09
TMIN_SHIFT (23)
H_PROCHOT# (9,68)
20100111: Remove PSU PWM control
DO1 change to RO109; SMSC suggestion-12/08/09
20100513: add UO4 , RO37 and net X_PLTRST_PCIE_SLOT#_R
20100514: UO4 change to 74LVC1G125GW and add RO40
20100517: RO40 change to 33Ohm
UO4
74LVC1G125GW
X_PLTRST_PCIE_SLOT# (40)
Add SMBus switch circuit-11/25/09
20100105: Mount SMBus control circuit by B_ATX_PWROK
20100503: RO108 change to 20 kOhm
20100107: change to +3V_DUAL for layout
RO107 10K +/-1%
QO16 MMDT5551
RO106 8.2K
(63,67) B_ATX_PWROK
RO108 20K +/-1%
20100203: Mount RO108
S_SMB_SW
QO4 2N7002
QO5 2N7002
(15,17,20,52) S_SMBCLK_MAIN
S_SMBCLK_PCI (13,16,18,24,40)
(15,17,20,52) S_SMBDATA_MAIN
S_SMBDATA_PCI (13,16,18,24,40)
+12V_CPU
RO23 8.2K +/-5%
RO28 698 +/-1%
RO12 30K +/-1%
RO19 30K +/-1%
QO2 MMBT3904-7-F
QO3 MMBT3904-7-F
RO17 8.2K +/-5% Dummy S_SMLINK1_DATA_R
RO10 8.2K +/-5% Dummy S_SMLINK1_CLK_R
RO11 8.2K +/-5% Dummy S_SMBDATA_PCI_R
RO18 8.2K +/-5% Dummy S_SMBCLK_PCI_R
RO20 8.2K +/-5% O_AUD_PCSPKR_DET#
RO21 8.2K +/-5% O_BC_CLK
RO22 8.2K +/-5% SPI_DI
RO38 100K+/-5% Dummy T_ESATA_DET#
20100512: use RO38 for T_ESATA_DET# pull-up
20100514: use RO38 Dummy
RO24 4.7K +/-5% S_SMBDATA_MAIN
RO25 4.7K +/-5% S_SMBCLK_MAIN
RO26 30K +/-1% O_TXD1_R
RO27 8.2K +/-5% TMIN_SHIFT
RO13 4.7K +/-5% S_SMBDATA_PCI
RO14 4.7K +/-5% S_SMBCLK_PCI
20100324: S_SMBDATA_PCI and S_SMBCLK_PCI change pull-up to +3V_S5
DELL INC.
Title
SIO-SCH5544-1
DWG NO
Katsiki_USFF
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Eletro-X

SCH5544 Decoupling

+3V_DUAL
CO18 0.1uF
CO19 0.1uF
+VCCRTC_SIO
CO20 0.1uF
+3V
CO21 0.1uF

+3V
RO43 30K +/-1%
O_TXD2_R

+3V
RO44 30K +/-1%
O_DTR2#_R

+1P05V_VCCIO
+3V
RO45 8.25K +/-1%
(32) O_TXD2_R
RO49 7.15K +/-1%
QO6 MMDT5551
RO51 2KOhm +/-1%
O_TXD2_R
RO55 33KOhm +/-1%
+3V_EPW

+3V_DUAL
RO46 8.2K +/-5% Dummy
O_SPEAKER (31,32)
RO52 8.25K +/-1%

20100107: Remove RO47, RO53 and O_RTS1#_R strapping, SMSC suggestion

+3V_DUAL
RO48 8.2K +/-5% Dummy
O_DTR1#_R (32,50)
RO54 30K +/-1%

	SPEAKER	DTR1#
	Diag_En	Flash_en
PULL HIGH	Disable	Flash Enable
PULL LOW	Enable	Parallel Enable

SIO STRAPING

+5V
RNO1 1K +/-5%
RO50 1K +/-5%
O_INDEX# (32)
O_RDATA# (32)
O_DSKCHG# (32)
O_WPT# (32)
O_TRK0# (32)

20100206: Swap net for routing

+1P05V_PCH
+3V
RO56 8.25K +/-1%
O_TXD2_R
QO7 MMDT5551
RO57 6.8K +/-1%
+1P05V_ME
O_TXD2_R

+5V
RNO4 1K +/-5%
RO98 1K
20100208: Swap net for routing
(32) O_ERR#
(32) O_ACK#
(32) O_BUSY
(32) O_PE
(32) O_SLCT

+5V_DUAL_USBKB
RNO3 2K +/-5%
(32) O_KB_DATA
(32) O_KB_CLK
(32) O_MS_CLK
(32) O_MS_DATA
20100513: swap pin1 and pin3

+1P5V_SM
+3V
RO58 8.25K +/-1%
O_TXD2_R
QO9 MMDT5551
RO61 10K +/-1%
+3V
RO62 30K +/-1%
(20,24,52,64,68) P_VR_READY
O_DTR2#_R (32)

20100104: Removed useless dummied components, and only left O_PECI_READY pull-up

+1P05V_VCCIO
RO60 1K
O_GP73_PU (32)

5544 PRE-POST DIAG PG GENERATION

DELL INC.

Title: SIO-SCH5544-2 (Miso)
DWG NO: Katsiki_USFF
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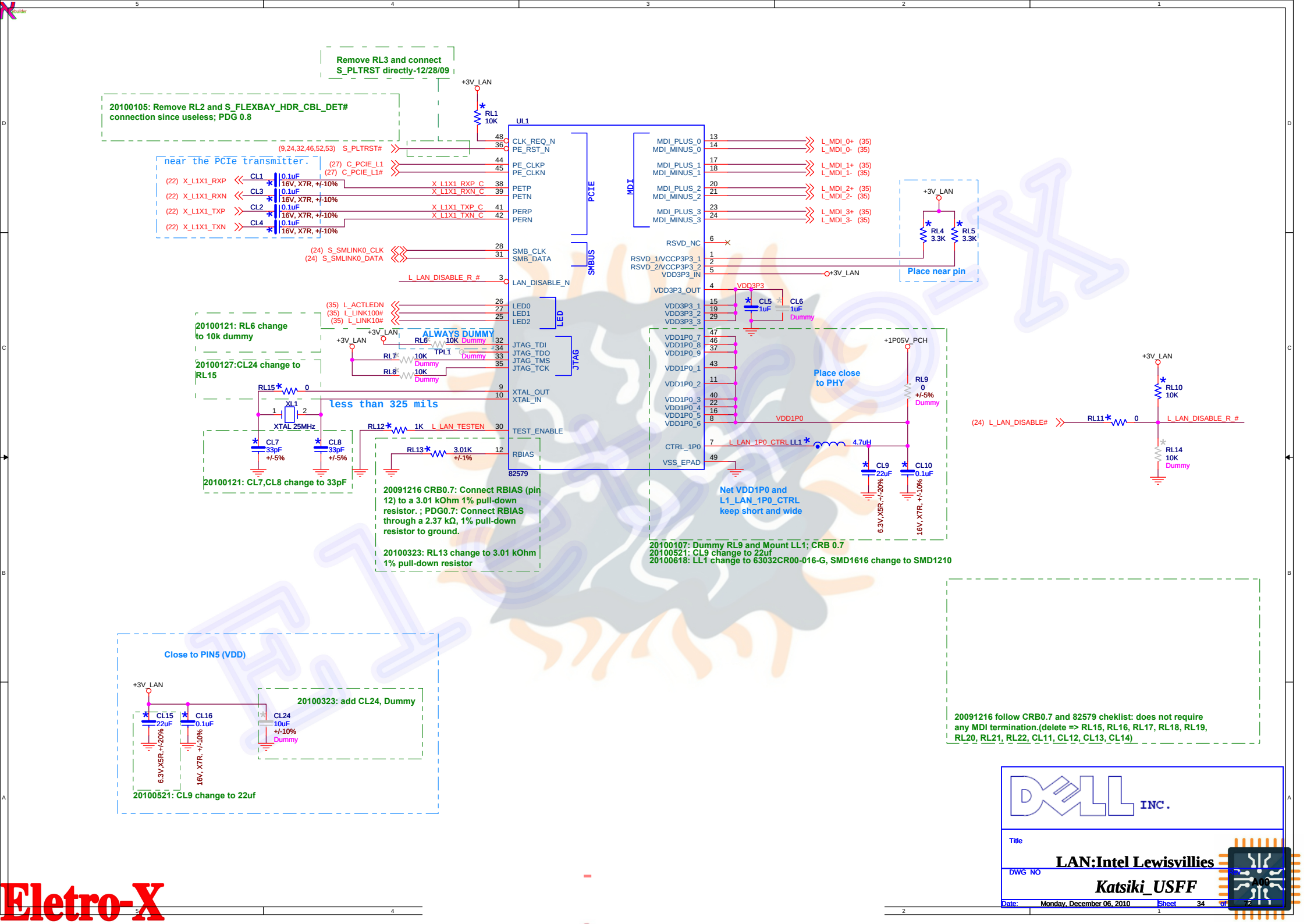
Remove RL3 and connect S_PLTRST directly-12/28/09
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET# connection since useless; PDG 0.8
near the PCIe transmitter.
+3V_LAN
RL1 10K
UL1
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETP
PETN
PERP
PERN
PCIE
SMB_CLK
SMB_DATA
SMBUS
LAN_DISABLE_N
LED0
LED1
LED2
LED
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
XTAL_OUT
XTAL_IN
TEST_ENABLE
RBIAS
82579
MDI_PLUS_0
MDI_MINUS_0
MDI_PLUS_1
MDI_MINUS_1
MDI_PLUS_2
MDI_MINUS_2
MDI_PLUS_3
MDI_MINUS_3
MDI
RSVD_NC
RSVD_1/VCCP3P3_1
RSVD_2/VCCP3P3_2
VDD3P3_IN
VDD3P3_OUT
VDD3P3_1
VDD3P3_2
VDD3P3_3
VDD1P0_7
VDD1P0_8
VDD1P0_9
VDD1P0_1
VDD1P0_2
VDD1P0_3
VDD1P0_4
VDD1P0_5
VDD1P0_6
VDD1P0
CTRL_1P0
VSS_EPAD
L_MDI_0+ (35)
L_MDI_0- (35)
L_MDI_1+ (35)
L_MDI_1- (35)
L_MDI_2+ (35)
L_MDI_2- (35)
L_MDI_3+ (35)
L_MDI_3- (35)
RL4 3.3K
RL5 3.3K
Place near pin
CL5 1uF
CL6 1uF Dummy
+1P05V_PCH
RL9 0 +/-5% Dummy
Place close to PHY
LL1 4.7uH
L_LAN_1P0_CTRL
CL9 22uF
CL10 0.1uF
6.3V,X5R,+/-20%
16V, X7R, +/-10%
Net VDD1P0 and L1_LAN_1P0_CTRL keep short and wide
20100107: Dummy RL9 and Mount LL1; CRB 0.7
20100521: CL9 change to 22uf
20100618: LL1 change to 63032CR00-016-G, SMD1616 change to SMD1210
(9,24,32,46,52,53) S_PLTRST#
(27) C_PCIE_L1
(27) C_PCIE_L1#
(22) X_L1X1_RXP
(22) X_L1X1_RXN
(22) X_L1X1_TXP
(22) X_L1X1_TXN
CL1 0.1uF 16V, X7R, +/-10%
CL3 0.1uF 16V, X7R, +/-10%
CL2 0.1uF 16V, X7R, +/-10%
CL4 0.1uF 16V, X7R, +/-10%
X_L1X1_RXP_C
X_L1X1_RXN_C
X_L1X1_TXP_C
X_L1X1_TXN_C
(24) S_SMLINK0_CLK
(24) S_SMLINK0_DATA
L_LAN_DISABLE_R_#
(35) L_ACTLEDN
(35) L_LINK100#
(35) L_LINK10#
20100121: RL6 change to 10k dummy
ALWAYS DUMMY
RL6 10K Dummy
RL7 10K Dummy
RL8 10K Dummy
TPL1
20100127:CL24 change to RL15
RL15 0
XL1
XTAL 25MHz
less than 325 mils
CL7 33pF +/-5%
CL8 33pF +/-5%
20100121: CL7,CL8 change to 33pF
RL12 1K L_LAN_TESTEN
RL13 3.01K +/-1%
20091216 CRB0.7: Connect RBIAS (pin 12) to a 3.01 kOhm 1% pull-down resistor. ; PDG0.7: Connect RBIAS through a 2.37 kΩ, 1% pull-down resistor to ground.
20100323: RL13 change to 3.01 kOhm 1% pull-down resistor
(24) L_LAN_DISABLE#
RL11 0
RL10 10K
RL14 10K Dummy
L_LAN_DISABLE_R_#
Close to PIN5 (VDD)
CL15 22uF
CL16 0.1uF
CL24 10uF +/-10% Dummy
20100323: add CL24, Dummy
20100521: CL9 change to 22uf
20091216 follow CRB0.7 and 82579 cheklist: does not require any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19, RL20, RL21, RL22, CL11, CL12, CL13, CL14)
DELL INC.
Title
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LAN CONNECTOR

NIC_USB

NIC
LAN CONN
USB Port-0
USB Port-1

1uF should be closed to the Connector -10/01/09-Sherlock

VCT
CL17 1uF +/-10%
CL18 0.1uF 16V, X7R, +/-10%
20100121: Change CL18 to 0.1uF
+3V_LAN
CL19 0.1uF 16V, X7R, +/-10%
NIC_USB
USB_PWR0_F_50
(34) L_LINK10#
(34) L_LINK100#
RL23 150 +/ -1%
RL24 150 +/ -1%
CL20 470pF 50V, X7R, +/-10%
CL21 470pF 50V, X7R, +/-10%
(34) L_MDI_0+
(34) L_MDI_0-
(34) L_MDI_1+
(34) L_MDI_1-
(34) L_MDI_2+
(34) L_MDI_2-
(34) L_MDI_3+
(34) L_MDI_3-
GRN_LED
ORG_LED
USB-2
USB-1
RJ45+MJ2
YLW_LED
U_USB1N_R
U_USB0N_R
U_USB1P_R
U_USB0P_R
+3V_LAN
20100121: Change RL25 position
(34) L_ACTLEDN
RL25 150 +/ -1%
CL22 470pF 50V, X7R, +/-10% Dummy
CL23 470pF 50V, X7R, +/-10%
20100317: Change CL22 to Dummy, tracker item#108
CONN - USBX2_RJ45

Change to BAT54A and remove CL24 for Cost down-11/23/09
DL1
(34) L_LINK100#
(34) L_LINK10#
L_FP_LAN_LED_GRN# (56)
BAT54A

+5V_DUAL_USBKB
USB_PWR0_F_50
FU11 Fuse 2A
20100728: FU1 change to 1812L200THPR
20100804: FU1 change to MINISMDC200F
ECU1 470uF +/-20%
CU7 0.1uF 16V, X7R, +/-10%
RU1 10K +/-1%
RU2 15K +/-1%
U_USB_OC_R_#0 (22)

LU1
U_USB0N_R
U_USB0P_R
Common Choke 90 Ohm
RU3 0 Dummy
RU4 0 Dummy
U_USB0N (22)
U_USB0P (22)
20100318: mount RU3, RU4,RU5,RU6 and dummy LU1,LU2
20100511: Mount LU1, LU2 ; Dummy RU3, RU4,RU5,RU6

LU2
U_USB1N_R
U_USB1P_R
Common Choke 90 Ohm
RU5 0 Dummy
RU6 0 Dummy
U_USB1N (22)
U_USB1P (22)
20100514: LU1, LU2 change to ACM2012E-900-2P-T000

USB_PWR0_F_50
UU1
U_USB0N_R
U_USB1N_R
U_USB0P_R
U_USB1P_R
IP4223CZ6
Dummy for Cost down-11/23/09
20100728: UU1 change to IP4223CZ6, mount

LAN POWER

20100721: QL1 change to SI4835DDY-T1-GE3 , check link
+3V_S5
QL1
SI4835DDY-T1-GE3
+3V
+3V_EPW
+3V_LAN
RL27 0 Dummy
RL28 0 Dummy
20100510: RL28 pop
20100618: RL28 Dummy
ECL1 120uF +/-20%
CL25 0.1uF 16V, X7R, +/-10%

+5V_S5
RL26 1K
L_VREG_LANDUAL_PCH
(24) S_SLP_LAN#
RL29 4.7K
QL2 MMBT3904-7-F
RL31 100K Dummy
20100519: RL30 change to 10 kOhm
20100726: RL30 change to 8.2 kOhm
20100803: RL30 change to 1 kOhm, +/-1%
RL30 1K +/-1%
L_VREG_Gate
CL26 1uF

+3V
CL27 1uF +/-10%
+3V_S5
CL28 1uF +/-10%

DELL INC.

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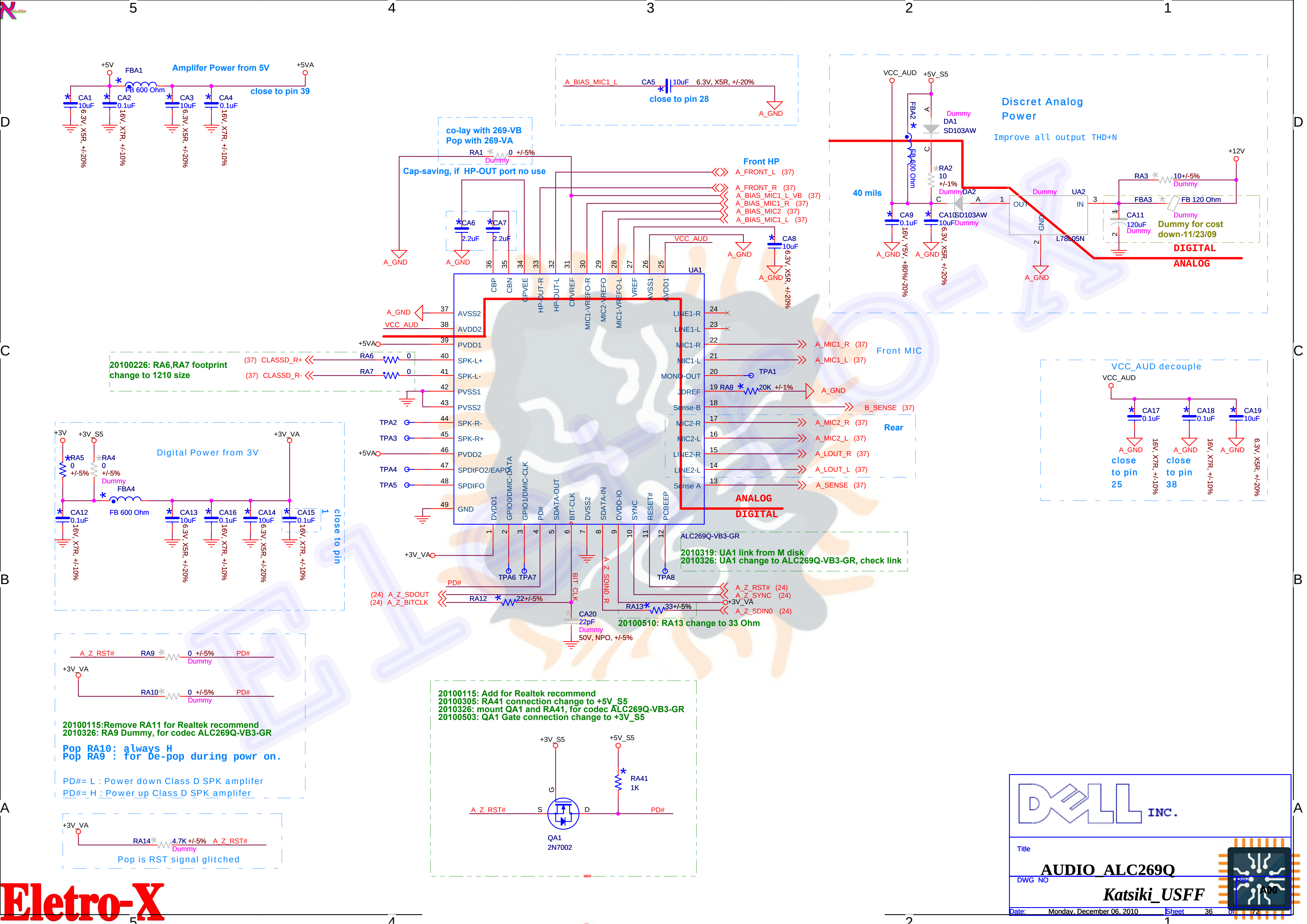

Amplifer Power from 5V
+5V
FBA1
FB 600 Ohm
+5VA
close to pin 39
CA1 10uF 6.3V, X5R, +/-20%
CA2 0.1uF 16V, X7R, +/-10%
CA3 10uF 6.3V, X5R, +/-20%
CA4 0.1uF 16V, X7R, +/-10%
A_BIAS_MIC1_L
CA5 10uF 6.3V, X5R, +/-20%
close to pin 28
A_GND
co-lay with 269-VB
Pop with 269-VA
RA1 0 +/-5% Dummy
Cap-saving, if HP-OUT port no use
Front HP
A_FRONT_L (37)
A_FRONT_R (37)
A_BIAS_MIC1_L_VB (37)
A_BIAS_MIC1_R (37)
A_BIAS_MIC2 (37)
A_BIAS_MIC1_L (37)
CA6 2.2uF
CA7 2.2uF
VCC_AUD
CA8 10uF 6.3V, X5R, +/-20%
UA1
CBP CBN CPVEE HP-OUT-R HP-OUT-L CPVREF MIC1-VREFO-R MIC2-VREFO MIC1-VREFO-L VREF AVSS1 AVDD1
AVSS2 AVDD2 PVDD1 SPK-L+ SPK-L- PVSS1 PVSS2 SPK-R- SPK-R+ PVDD2 SPDIFO2/EAPD SPDIFO GND
LINE1-R LINE1-L MIC1-R MIC1-L MONO-OUT JDREF Sense-B MIC2-R MIC2-L LINE2-R LINE2-L Sense A
DVDD1 GPIO0/DMIC-DATA GPIO1/DMIC-CLK PD# SDATA-OUT BIT-CLK DVSS2 SDATA-IN DVDD-IO SYNC RESET# PCBEEP
20100226: RA6,RA7 footprint change to 1210 size
(37) CLASSD_R+ RA6 0
(37) CLASSD_R- RA7 0
TPA1 TPA2 TPA3 TPA4 TPA5 TPA6 TPA7 TPA8
A_MIC1_R (37)
A_MIC1_L (37)
Front MIC
RA8 20K +/-1%
B_SENSE (37)
A_MIC2_R (37)
A_MIC2_L (37)
A_LOUT_R (37)
A_LOUT_L (37)
A_SENSE (37)
Rear
ANALOG
DIGITAL
ALC269Q-VB3-GR
2010319: UA1 link from M disk
2010326: UA1 change to ALC269Q-VB3-GR, check link
Digital Power from 3V
+3V +3V_S5 +3V_VA
RA5 0 +/-5%
RA4 0 +/-5% Dummy
FBA4 FB 600 Ohm
CA12 0.1uF 16V, X7R, +/-10%
CA13 10uF 6.3V, X5R, +/-20%
CA16 0.1uF 16V, X7R, +/-10%
CA14 10uF 6.3V, X5R, +/-20%
CA15 0.1uF 16V, X7R, +/-10%
close to pin 1
(24) A_Z_SDOUT
(24) A_Z_BITCLK
RA12 22+/-5%
CA20 22pF Dummy 50V, NPO, +/-5%
A_Z_RST# (24)
A_Z_SYNC (24)
A_Z_SDIN0 (24)
RA13 33+/-5%
20100510: RA13 change to 33 Ohm
Discret Analog Power
Improve all output THD+N
VCC_AUD +5V_S5
FBA2 FB 600 Ohm
DA1 SD103AW Dummy
RA2 10 +/-1%
DA2 SD103AW Dummy
40 mils
CA9 0.1uF 16V, Y5V, +80%/-20%
CA10 10uF Dummy 6.3V, X5R, +/-20%
UA2 L78L05N Dummy
+12V
RA3 10+/-5% Dummy
FBA3 FB 120 Ohm Dummy
CA11 120uF Dummy
Dummy for cost down-11/23/09
VCC_AUD decouple
CA17 0.1uF 16V, X7R, +/-10% close to pin 25
CA18 0.1uF 16V, X7R, +/-10% close to pin 38
CA19 10uF 6.3V, X5R, +/-20%
A_Z_RST# RA9 0 +/-5% Dummy PD#
RA10 0 +/-5% Dummy PD#
20100115:Remove RA11 for Realtek recommend
2010326: RA9 Dummy, for codec ALC269Q-VB3-GR
Pop RA10: always H
Pop RA9 : for De-pop during powr on.
PD#= L : Power down Class D SPK amplifer
PD#= H : Power up Class D SPK amplifer
RA14 4.7K +/-5% A_Z_RST# Dummy
Pop is RST signal glitched
20100115: Add for Realtek recommend
20100305: RA41 connection change to +5V_S5
2010326: mount QA1 and RA41, for codec ALC269Q-VB3-GR
20100503: QA1 Gate connection change to +3V_S5
RA41 1K
QA1 2N7002
DELL INC.
Title
AUDIO_ALC269Q
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Front Audio

(36) A_BIAS_MIC1_R
(36) A_BIAS_MIC1_L
(36) A_BIAS_MIC1_L_VB
close to codec
RA17 2.2KOhm +/-1%
RA18 2.2KOhm +/-1% Dummy
RA19 2.2KOhm +/-1%

Front MIC

(36) A_MIC1_R — CA23 2.4.7uF A_MIC1_R_C RA22 1K +/-1% — RA23 0 — A_MIC1_R_L (56)
(36) A_MIC1_L — CA24 2.4.7uF A_MIC1_L_C RA24 1K +/-1% — RA25 0 — A_MIC1_L_L (56)

CA25 470pF 50V, X7R, +/-10% — A_GND
CA26 470pF 50V, X7R, +/-10% — A_GND

Improve HP-OUT 32-Ohm's Cross-Talk and THD+N

It can be reserved if output de-coupled cap used SMD type.

Front HP

(36) A_FRONT_R — RA32 22 Ohm +/-1% — RA33 0 — A_FRONT_R_L (56)
(36) A_FRONT_L — RA34 22 Ohm +/-1% — RA35 0 — A_FRONT_L_L (56)

Port A Support Capless HP

Change to 22ohm; follow Wembley-12/25/09

CA33 470pF 50V, X7R, +/-10% — A_GND
CA34 470pF 50V, X7R, +/-10% — A_GND

(36) A_SENSE
RA36 39.2K +/-1% — A_JD_FRONT (56) — Front HP
RA37 20K +/-1% — A_JD_MIC1 (56) — Front MIC

Close to Pin 33

A_MIC1_R_L
A_MIC1_L_L
DA6 PESD5V0L2BT Dummy — A_GND

A_FRONT_R_L
A_FRONT_L_L
DA7 PESD5V0L2BT Dummy — A_GND

Rear Audio Jack

Change to 22uF; follow Wembley-12/25/09
20100326: CA21 and CA22 change to 22uF,+/-20%,X7R,10V,G,SMD1206
20100330: CA21 and CA22 change to 22uF,+/-10%,X5R,10V,G,SMD1206
20100512: CA21 and CA22 change to 22uF,+/-10%,X5R,16V,G,SMD1206
20100712: CA21 and CA22 change to 22uF,+/-10%,X5R,16V,G,SMD1210, check with CE
20100716: CA21 and CA22 22uF,+/-10%,X5R,16V,G,SMD1210 Link from CIS

(36) A_LOUT_L — CA21 22uF +/-10% — A_LOUT_L_C — RA15 75+/-1% — RA16 0 — A_LOUT_L_L
(36) A_LOUT_R — CA22 22uF +/-10% — A_LOUT_R_C — RA20 75+/-1% — RA21 0 — A_LOUT_R_L

Audio Jack
D — LINE_OUT
C — LINE_IN / MIC_IN

Rear Line In / Mic

(36) A_BIAS_MIC2
close to codec
DA3 BAT54A

AUDIO_LINE_OUT
A_JD_LOUT
RA26 4.7KOhm +/-1%
RA27 4.7KOhm +/-1%

(36) A_MIC2_L — CA27 2.4.7uF A_MIC2_L_C RA28 1K +/-1% — RA29 0 — A_MIC2_L_L
(36) A_MIC2_R — CA28 2.4.7uF A_MIC2_R_C RA30 1K +/-1% — RA31 0 — A_MIC2_R_L

CONN-Audio Jack AUDIO_LINE_IN
A_JD_MIC2
CONN-Audio Jack

CA29 470pF 50V, X7R, +/-10% — A_GNDA_GND
CA30 470pF 50V, X7R, +/-10% — A_GNDA_GND
CA31 470pF 50V, X7R, +/-10% — A_GNDA_GND
CA32 470pF 50V, X7R, +/-10% — A_GNDA_GND

CA35 10nF 25V, X7R, +/-10% — A_GND
CA36 10nF 25V, X7R, +/-10% — A_GND
CA37 10nF 25V, X7R, +/-10% — A_GND
CA38 10nF 25V, X7R, +/-10% — A_GND
CA39 10nF 25V, X7R, +/-10% — A_GND

CPA1 COPPER Dummy
CPA2 COPPER Dummy
CPA3 COPPER Dummy
CPA4 COPPER Dummy
A_GND

20100119: Add for Realtek recommend and change Audion signal GND to A_GND
20100512: CPA5 removed

A_LOUT_L_L — A_LOUT_R_L — DA5 PESD5V0L2BT Dummy — A_GND
A_MIC2_L_L — A_MIC2_R_L — DA4 PESD5V0L2BT Dummy — A_GND

(36) B_SENSE
RA38 20K +/-1% — A_JD_MIC2 — Rear MIC In/LINE IN
RA39 39.2K +/-1% — A_JD_LOUT — Rear Line out

Close to Pin 33

Place near Audio Chip
CA41 1nF 50V, X7R, +/-10%
(36) CLASSD_R-
(36) CLASSD_R+
CA43 1uF Dummy 10V, X5R, +/-10%
CA45 1nF 50V, X7R, +/-10%
close to AR12, AR13

Place connector
CA42 100pF 50V, NPO, +/-5% Dummy
CA44 100pF 50V, NPO, +/-5%
CLASSD_R-
CLASSD_R+
(32) O_AUD_PCSPKR_DET#
INT_SPKR
Header_1X5_K2

CHASSIS SPEAKER

Header 1x5 cut2

Pin.1--> Left-
Pin.2--> NC key
Pin.3--> GND
Pin.4--> SPK det#
Pin.5--> Left+

DELL INC.

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Mini PCIe

20100121: Add RX17
20100127: Mount RX17
20100128: Dummy RX17 and Mount RX8
20100226: Add RX18 and Modify
schematic as MT/DT
20100518: RX8 change to 2.2k Ohm
20100721: Dummy RX18 and Mount RX17

+3V_S5 +3V_PCIAUX +3V_PCIAUX +V_1.5V_PCIE

RX8 2.2K
RX18 10K Dummy
RX17 0

(24) GPIO_WIRELESS_DISABLE#
(32) X_PLTRST_PCIE_SLOT#

20100518: RX9, RX10 Dummy

(13,16,18,24,32) S_SMBCLK_PCI
(13,16,18,24,32) S_SMBDATA_PCI
RX9 0 Dummy
RX10 0 Dummy

U_USB12N_R
U_USB12P_R

(21) PCIE_MINI_CPUSB_DETECT#
RX11 0 Dummy
RX12 0
RX13 0 Dummy
(56) X_WIRELESS_LED#

20100513: PCIE_MINI_CPUSB_DETECT#
connect to pin 40 of mini-PCIe

PCIE_MINICARD

2	3D3VAUX_3	WAKE#	1
4	GND0	Reserved0	3
6	1D5V_0	Reserved1	5
8	Reserved/UIMPWR	CLKREQ#	7
10	Reserved/UIMDATA	GND11	9
12	Reserved/UIMCLK	REFCLK-	11
14	Reserved/UIMRESET	REFCLK+	13
16	Reserved/UIMVPP	GND10	15
18	GND1	Reserved/UIM C8	17
20	Reserved/WDISABLE#	Reserved/UIM C4	19
22	PERST#	GND9	21
24	3D3VAUX_4	PERn0	23
26	GND2	PERp0	25
28	1D5V_1	GND8	27
30	SMBCLK	GND7	29
32	SMBDATA	PETn0	31
34	GND3	PETp0	33
36	USB_D-	GND6	35
38	USB_D+	GND12	37
40	GND4	3D3VAUX_1	39
42	LED_WWAN#	3D3VAUX_2	41
44	LED_WLAN#	GND13	43
46	LED_WPAN#	Reserved6	45
48	1D5V_2	Reserved7	47
50	GND5	Reserved8	49
52	3D3VAUX_5	Reserved9	51
53	A1		
54	A2		

Memory Module Socket
minipcie52half_con
Half size

+3V_PCIAUX
Peak(MAX) 2,750 mA
Normal = 1,100 mA

RX16 10K
X_WLAN_WAKE# (22)

C_PCIEX1#_1 (27)
C_PCIEX1_1 (27)

X_1X1_RXN (22)
X_1X1_RXP (22)

X_1X1_TXN_C
X_1X1_TXP_C
CX56 0.1uF 16V, X7R, +/-10%
CX57 0.1uF 16V, X7R, +/-10%
X_1X1_TXN (22)
X_1X1_TXP (22)

PCIE_MINI_CPPE_DETECT# (21)
20100513: Rename X_WLAN_DETECT# to PCIE_MINI_CPPE_DETECT#

Close to PCH

S_CLINK_CLK_WLAN (23)
S_CLINK_DATA_WLAN (23)
S_CLINK_RST_WLAN# (23)

Add net; CRB 0.7-12/03/09

Dummy for cost down 11/23/09

(22) U_USB12N
(22) U_USB12P
LU13 Dummy
Common Choke 90 Ohm
U_USB12N_R
U_USB12P_R
RU44 0
RU43 0

+3V_PCIAUX
CX61 0.1uF 16V, X7R, +/-10% Pin2
CX62 0.1uF 16V, X7R, +/-10% Pin52
CX63 0.1uF 16V, X7R, +/-10% Pin24
CX64 0.1uF 16V, X7R, +/-10% Pin41

+3V_PCIAUX
Close to slot
CX58 22uF 6.3V,X5R,+/-20% Dummy
CX59 22uF 6.3V,X5R,+/-20% Dummy
CX60 22uF 6.3V,X5R,+/-20% Dummy

+V_1.5V_PCIE

+V_1.5V_PCIE
20100316: CX66 and CX67 Dummy
Close to slot
CX65 0.1uF 16V, X7R, +/-10%
CX66 0.1uF 16V, X7R, +/-10% Dummy
CX67 0.1uF 16V, X7R, +/-10% Dummy

Latch

PCIE_MINICARD_1
GND1 GND2 GND3 GND4 GND5 GND6
MiniCard_Latch
minipcie52half_lat

+3V
UX1
ADJ Vout Vin
NCP1117STAT3G
+V_1.5V_PCIE
Peak(MAX) 500 mA
Normal = 375 mA
CX68 10uF +/-10%
CX69 0.1uF 16V, X7R, +/-10%
V_1D5V_PCIEADJ
RX14 124 +/-1%
RX15 24.9 +/-1%
CX70 22uF 6.3V,X5R,+/-20%

DELL INC.

Title: Mini PCIe
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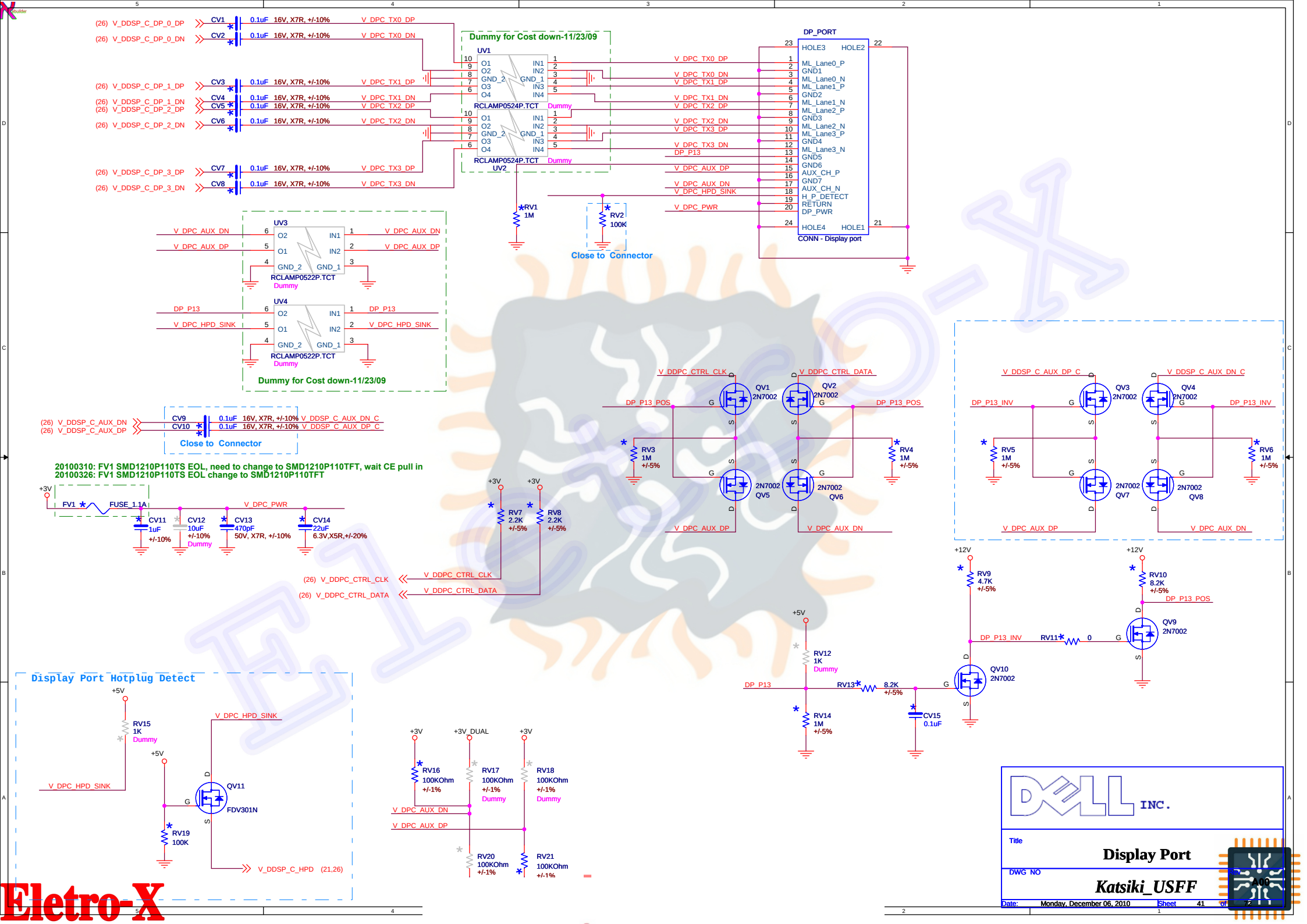
(26) V_DDSP_C_DP_0_DP
(26) V_DDSP_C_DP_0_DN
(26) V_DDSP_C_DP_1_DP
(26) V_DDSP_C_DP_1_DN
(26) V_DDSP_C_DP_2_DP
(26) V_DDSP_C_DP_2_DN
(26) V_DDSP_C_DP_3_DP
(26) V_DDSP_C_DP_3_DN
CV1 CV2 CV3 CV4 CV5 CV6 CV7 CV8
0.1uF 16V, X7R, +/-10%
V_DPC_TX0_DP
V_DPC_TX0_DN
V_DPC_TX1_DP
V_DPC_TX1_DN
V_DPC_TX2_DP
V_DPC_TX2_DN
V_DPC_TX3_DP
V_DPC_TX3_DN
Dummy for Cost down-11/23/09
UV1
UV2
RCLAMP0524P.TCT
Dummy
DP_PORT
HOLE3
HOLE2
HOLE4
HOLE1
ML_Lane0_P
ML_Lane0_N
ML_Lane1_P
ML_Lane1_N
ML_Lane2_P
ML_Lane2_N
ML_Lane3_P
ML_Lane3_N
GND1
GND2
GND3
GND4
GND5
GND6
GND7
AUX_CH_P
AUX_CH_N
H_P_DETECT
RETURN
DP_PWR
DP_P13
V_DPC_AUX_DP
V_DPC_AUX_DN
V_DPC_HPD_SINK
V_DPC_PWR
CONN - Display port
RV1 1M
RV2 100K
Close to Connector
UV3
UV4
RCLAMP0522P.TCT
Dummy for Cost down-11/23/09
(26) V_DDSP_C_AUX_DN
(26) V_DDSP_C_AUX_DP
CV9 CV10
V_DDSP_C_AUX_DN_C
V_DDSP_C_AUX_DP_C
20100310: FV1 SMD1210P110TS EOL, need to change to SMD1210P110TFT, wait CE pull in
20100326: FV1 SMD1210P110TS EOL change to SMD1210P110TFT
+3V
FV1 FUSE_1.1A
V_DPC_PWR
CV11 1uF +/-10%
CV12 10uF +/-10% Dummy
CV13 470pF 50V, X7R, +/-10%
CV14 22uF 6.3V,X5R,+/-20%
RV7 2.2K +/-5%
RV8 2.2K +/-5%
(26) V_DDPC_CTRL_CLK
(26) V_DDPC_CTRL_DATA
V_DDPC_CTRL_CLK
V_DDPC_CTRL_DATA
QV1 2N7002
QV2 2N7002
QV3 2N7002
QV4 2N7002
QV5 2N7002
QV6 2N7002
QV7 2N7002
QV8 2N7002
RV3 1M +/-5%
RV4 1M +/-5%
RV5 1M +/-5%
RV6 1M +/-5%
DP_P13_POS
DP_P13_INV
V_DDSP_C_AUX_DP_C
V_DDSP_C_AUX_DN_C
+12V
RV9 4.7K +/-5%
RV10 8.2K +/-5%
RV11 0
RV12 1K Dummy
RV13 8.2K +/-5%
RV14 1M +/-5%
CV15 0.1uF
QV9 2N7002
QV10 2N7002
Display Port Hotplug Detect
RV15 1K Dummy
RV19 100K
QV11 FDV301N
V_DPC_HPD_SINK
V_DDSP_C_HPD (21,26)
+3V_DUAL
RV16 100KOhm +/-1%
RV17 100KOhm +/-1% Dummy
RV18 100KOhm +/-1% Dummy
RV20 100KOhm +/-1%
RV21 100KOhm +/-1%
DELL INC.
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Display Port
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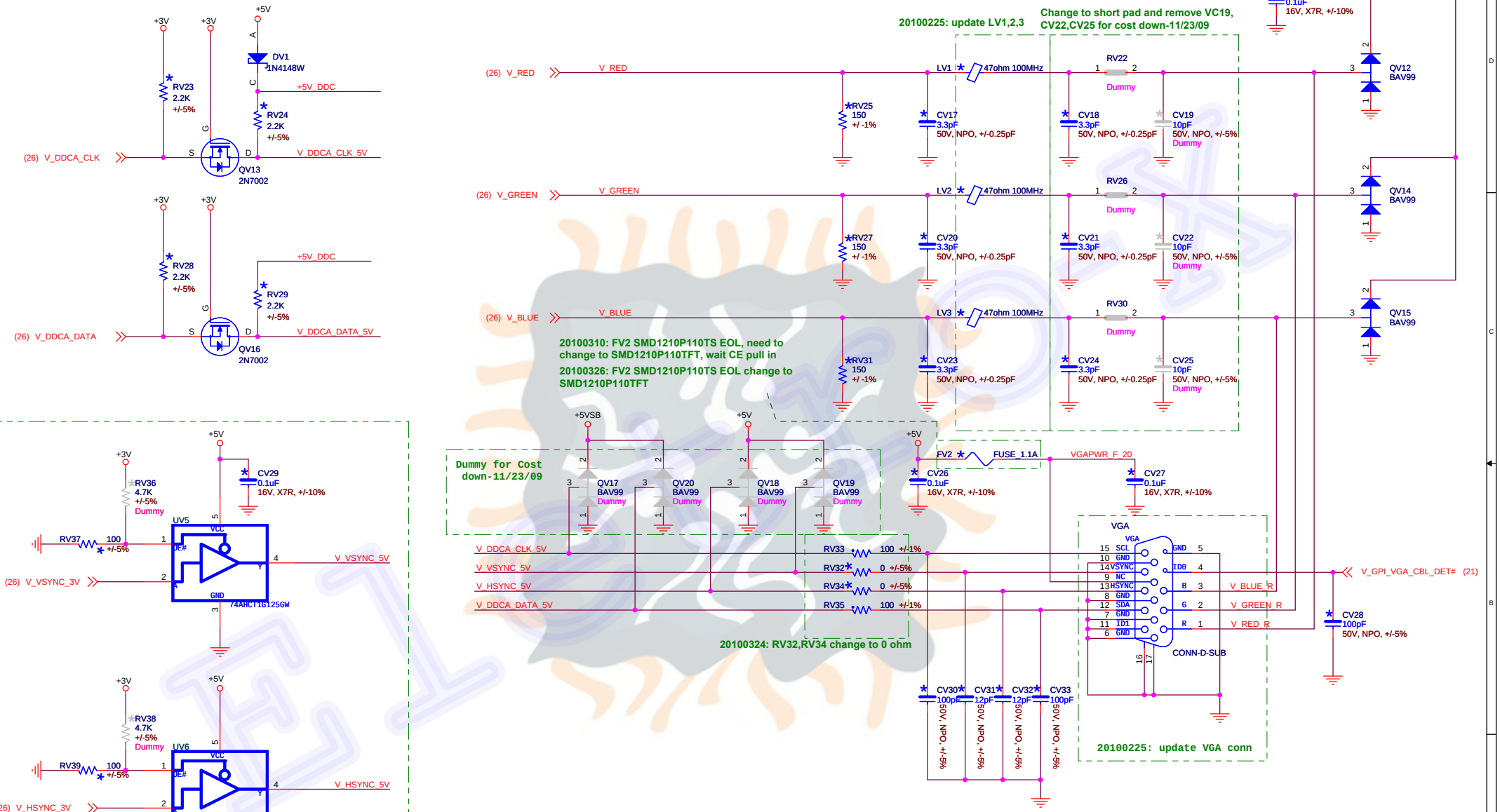
VGA Connector



DELL INC.

Title: VGA Conn

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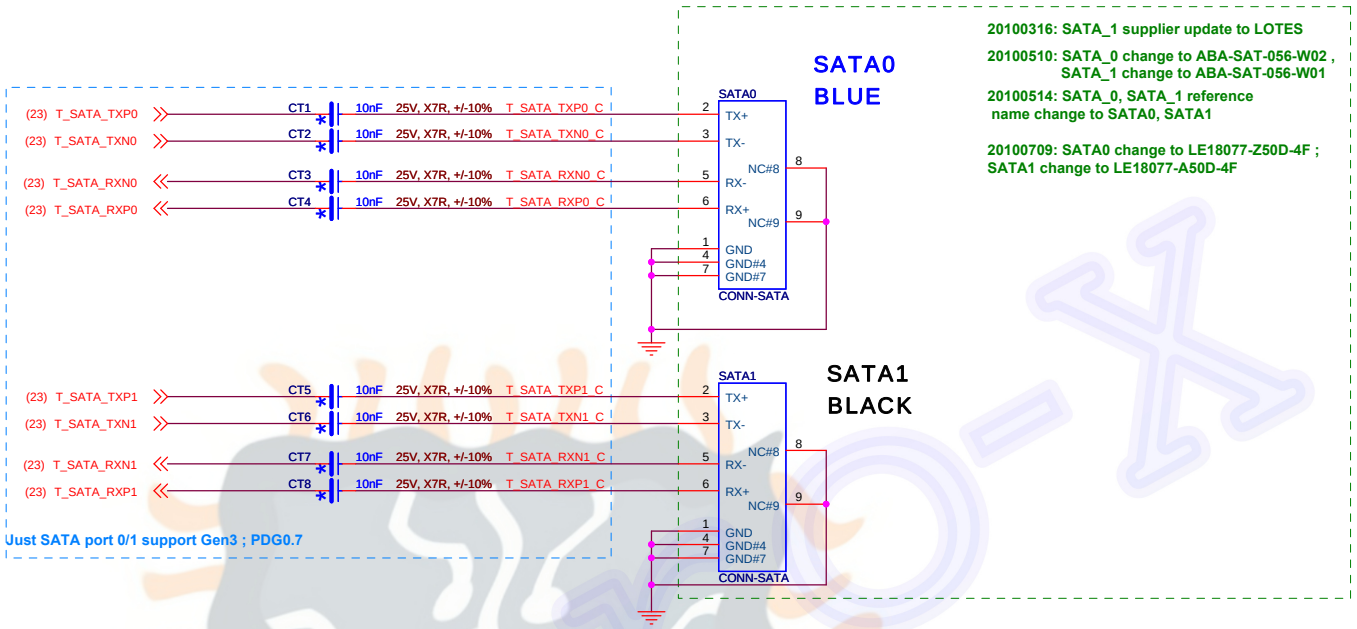
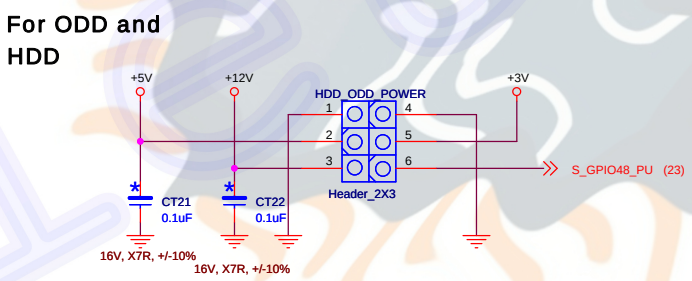
Eletro-X





DELL INC.

Title: SATA Conn

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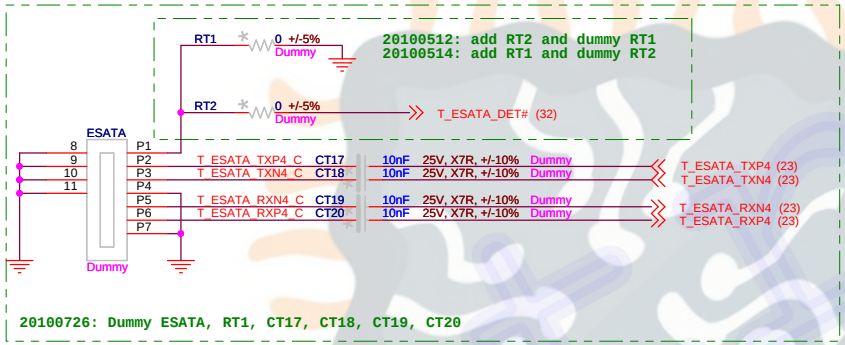
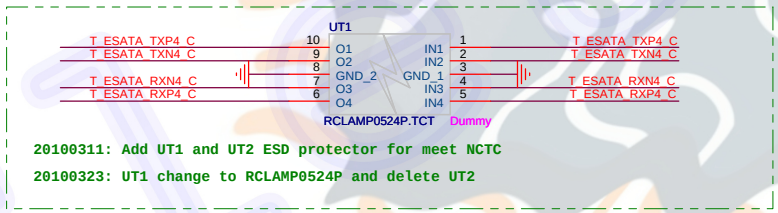
eSATA





DELL INC.

Title: eSATA Conn

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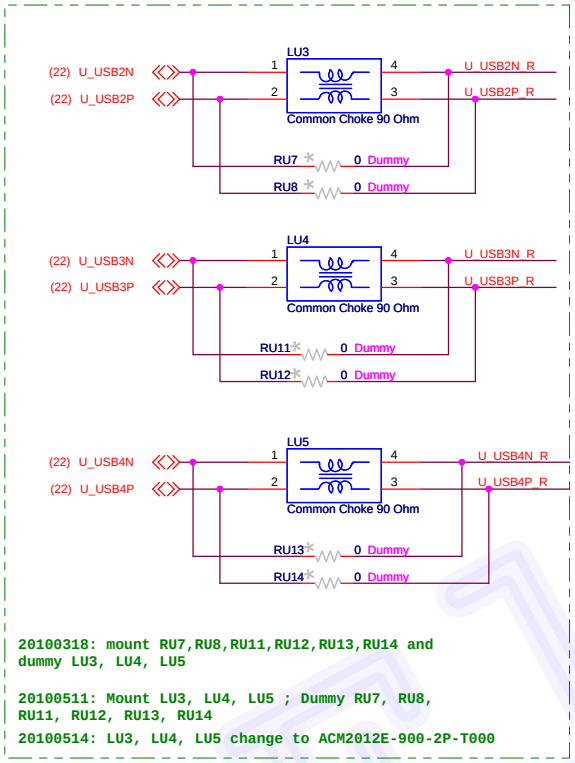
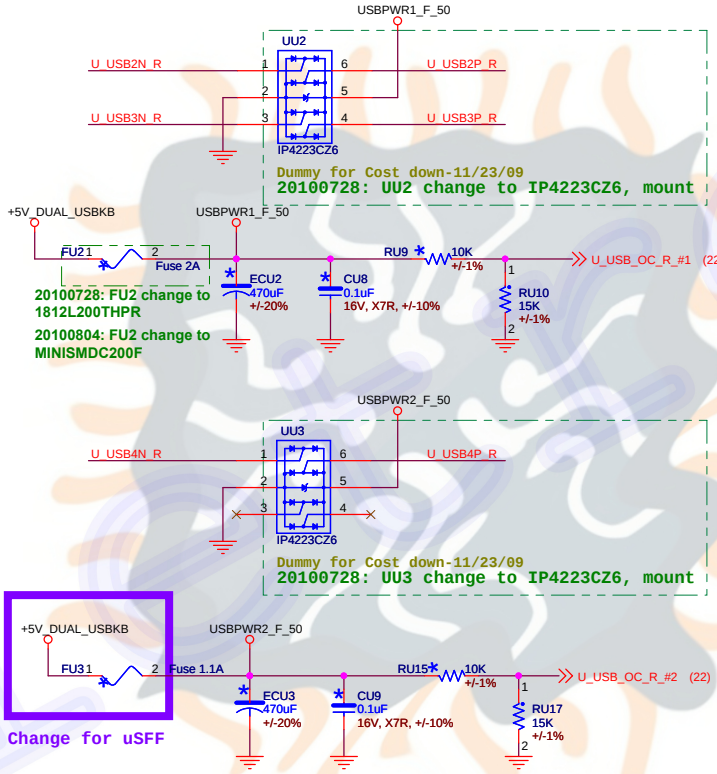
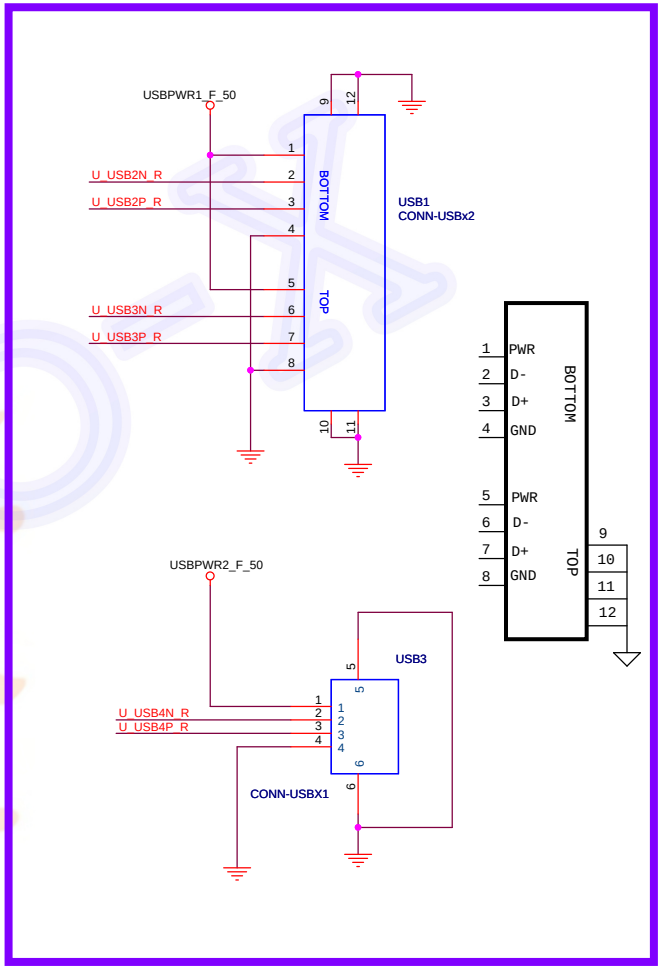
Rear USB CONNECTOR







Rear USB CONN MAP

USB1

USB Port-2	
USB Port-3	USB Port-4

USB3

DELL INC.

Title: Rear USB

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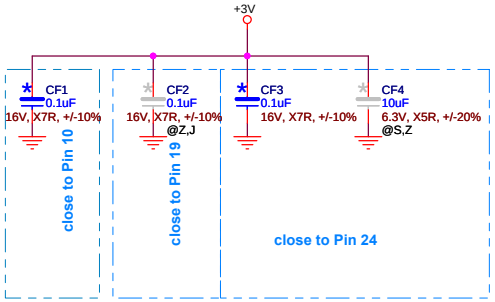
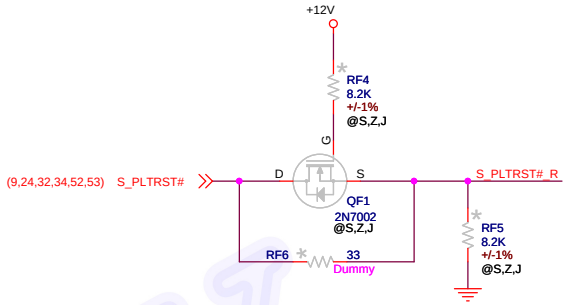
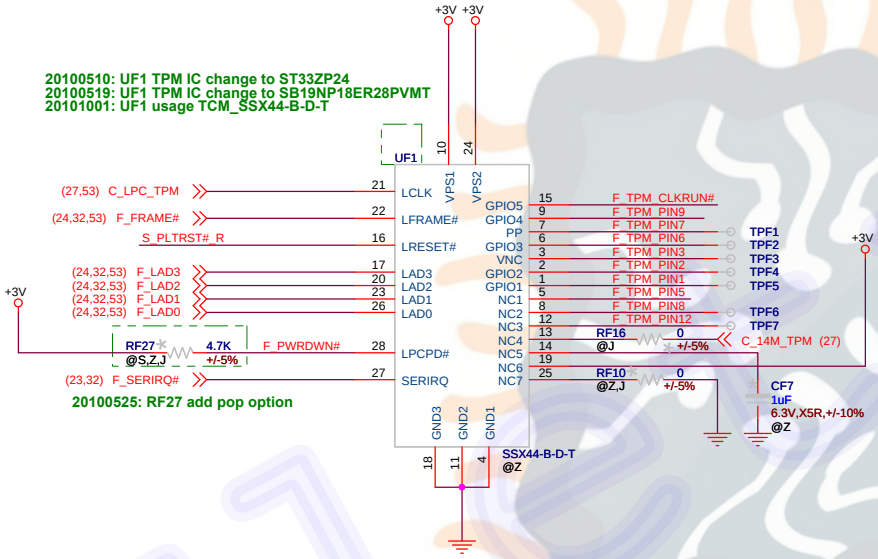
TPM, TCM

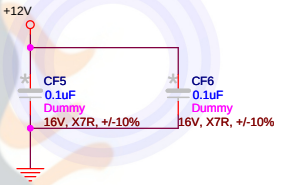
(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21

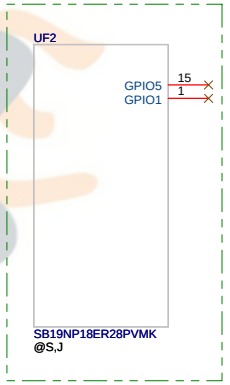
(TCM is just reserved because MRD has removed TCM requirement)











DELL INC.

Title: TPM & TCM

DWG NO: Katsiki_USFF

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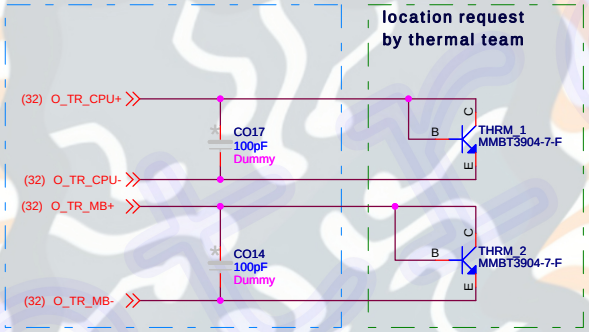

20100210: Swap CO24 and CO14 layout location
Swap CO23 and CO17 layout location

20100309: Dummy CO17,CO14

20100311: THRM2 reference name rename to THRM_1 , THRM3 reference name rename to THRM_2 , follow Dell PIG1.2

DELL INC.

Title: Thermal Sensor

DWG NO: Katsiki_USFF

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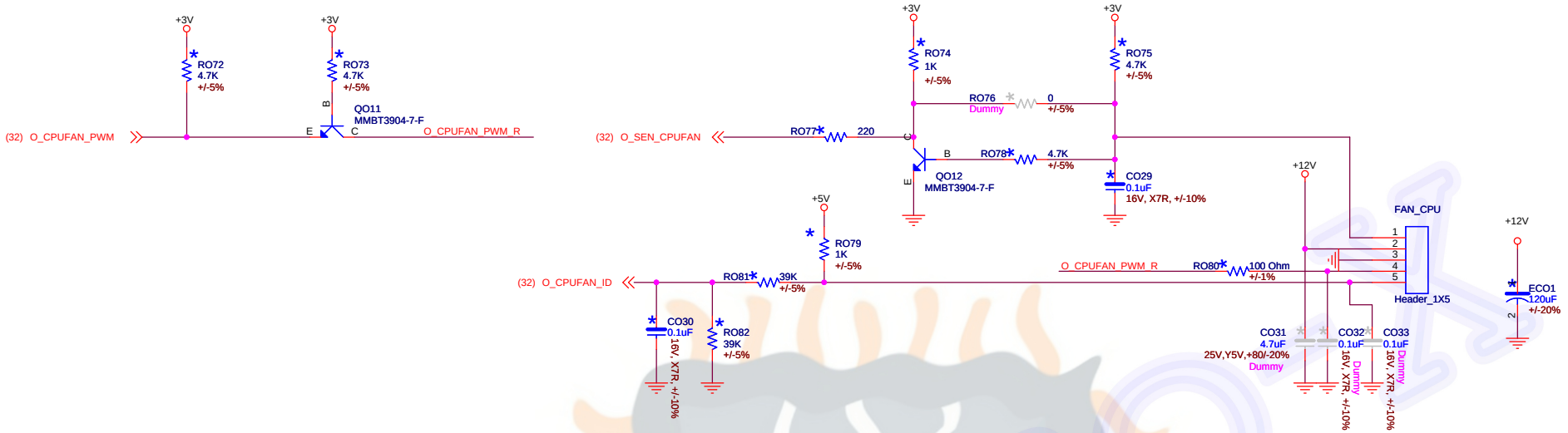
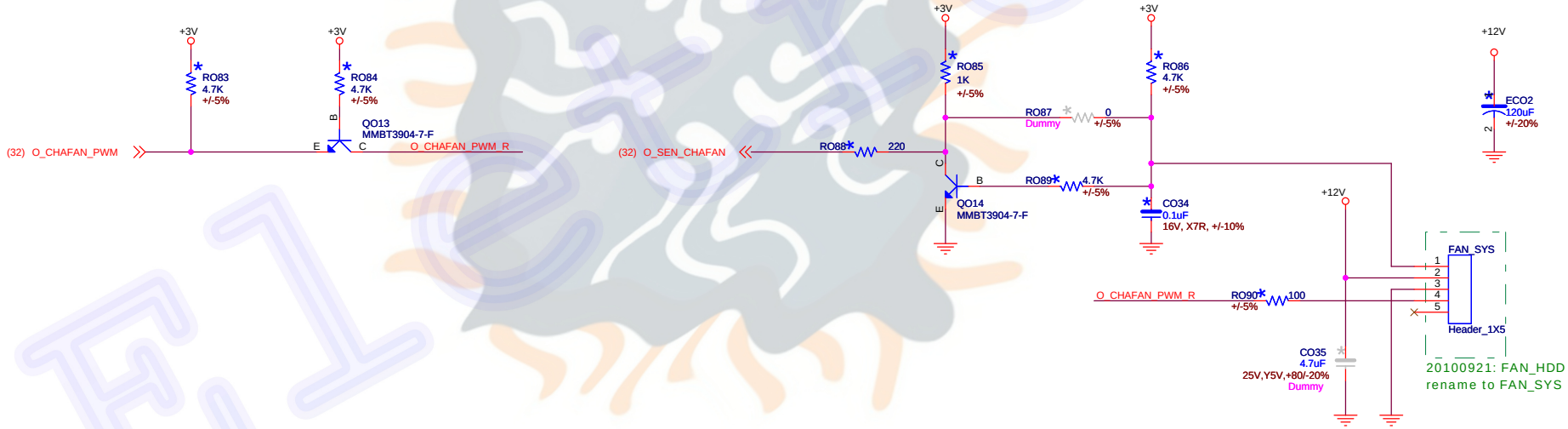
CPU Fan



SYS Fan



PSU Fan

20100111: Remove PSU PWM control

DELL INC.

Title: FAN

DWG NO: Katsiki_USFF

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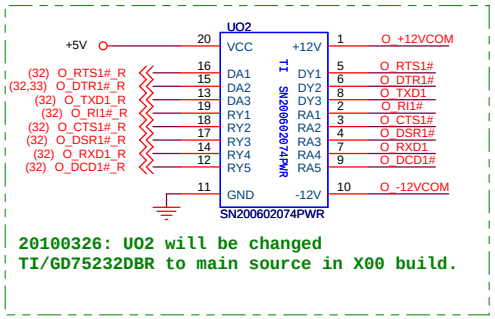
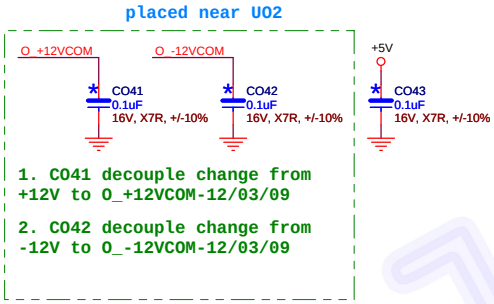
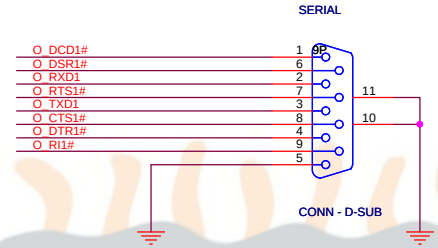
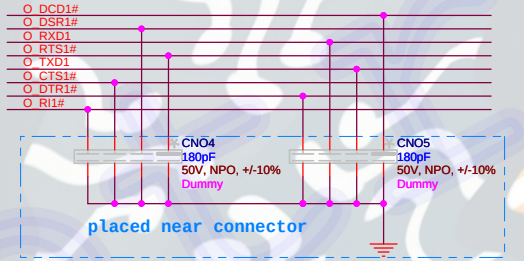
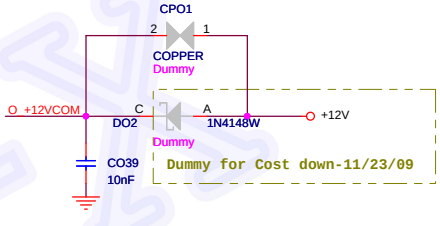
Serial Port 1

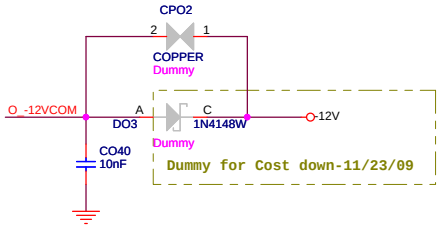












DELL INC.

Title
COM1

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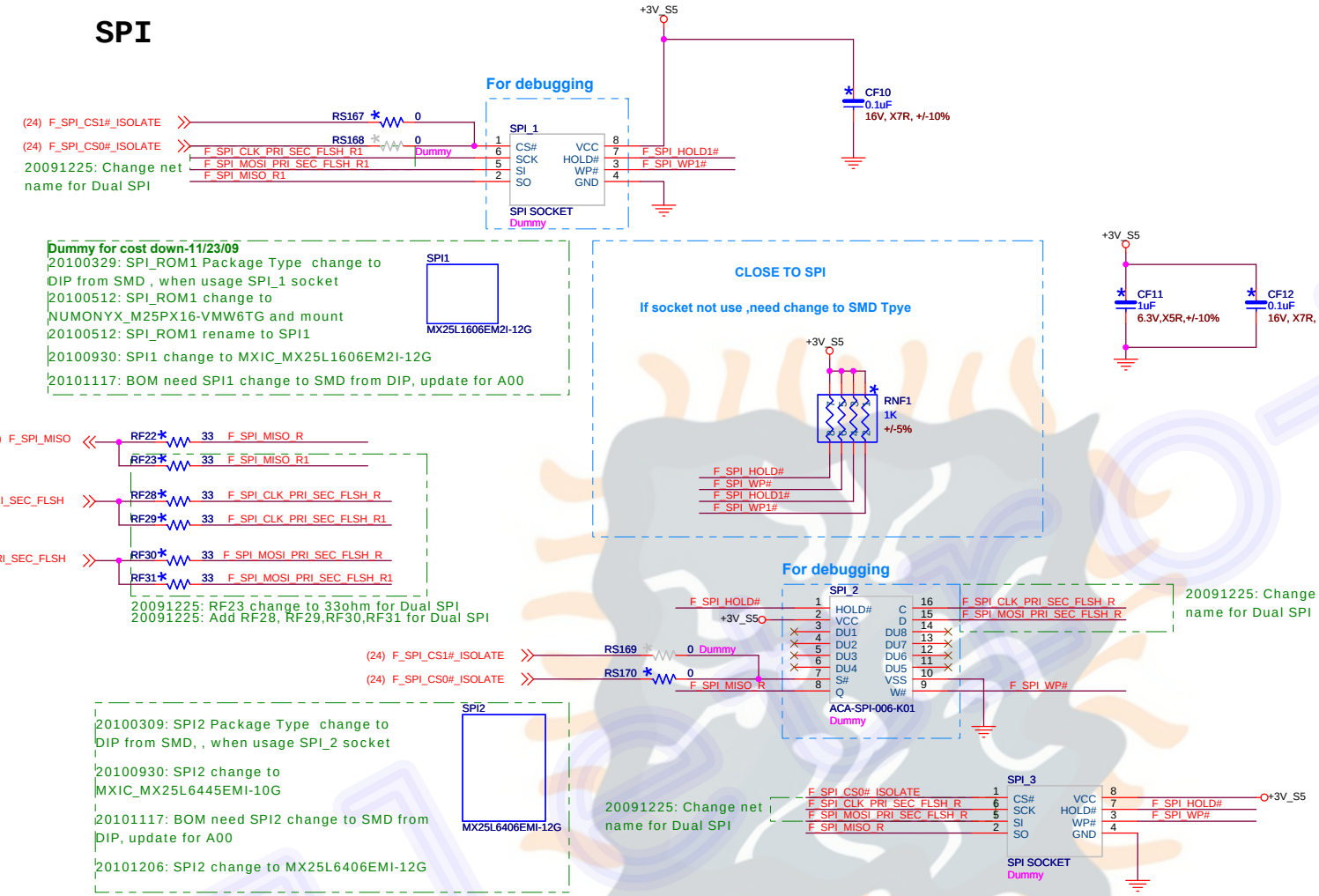
SPI



DELL INC.

Title: SPI

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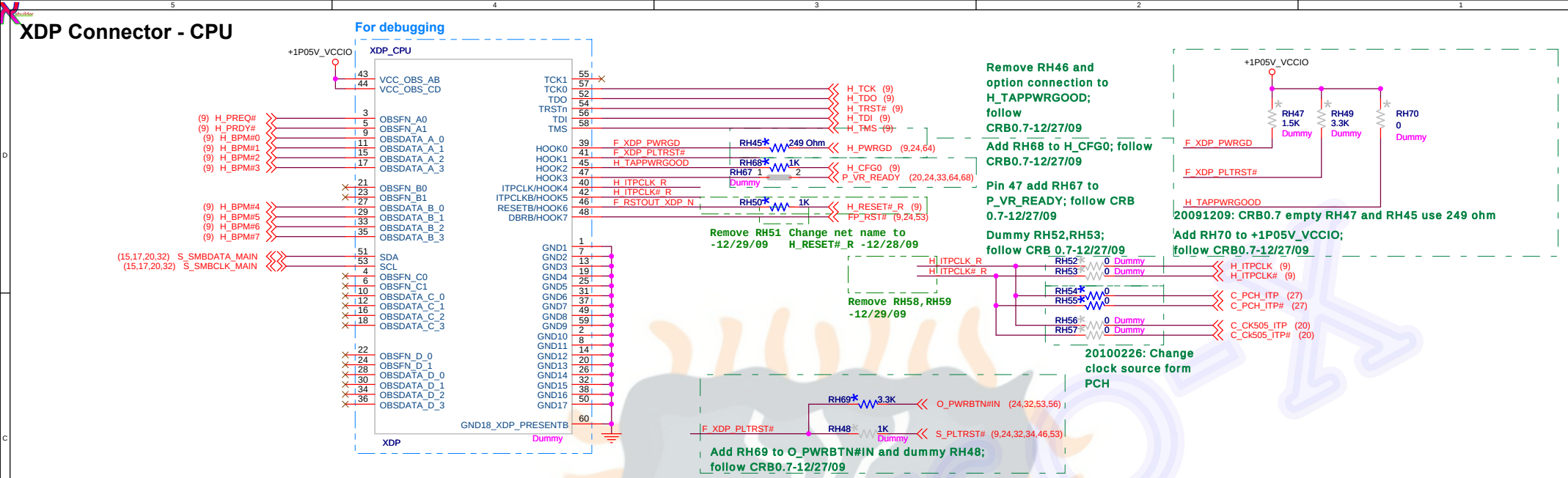
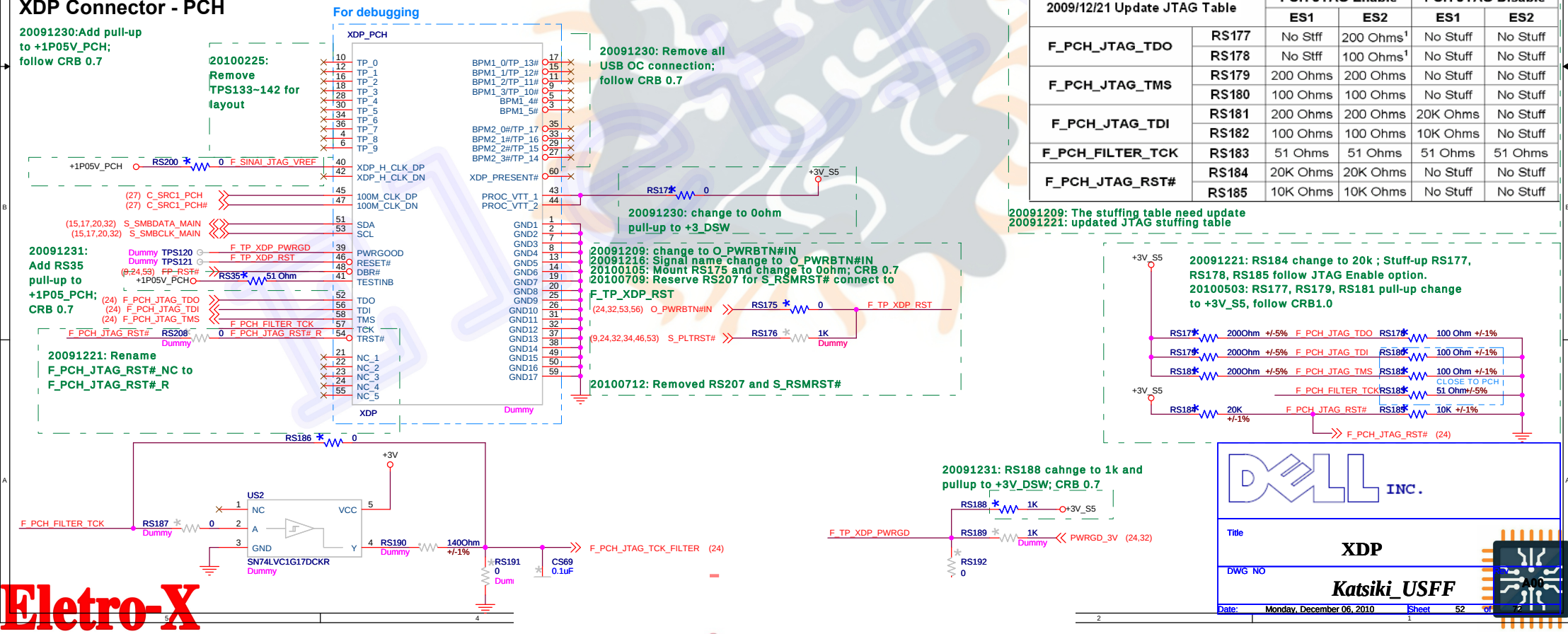
XDP Connector - CPU



XDP Connector - PCH



2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms[1]	No Stuff	No Stuff
	RS178	No Stff	100 Ohms[1]	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

20091209: The stuffing table need update
20091221: updated JTAG stuffing table

DELL INC.

Title: XDP

DWG NO: A00

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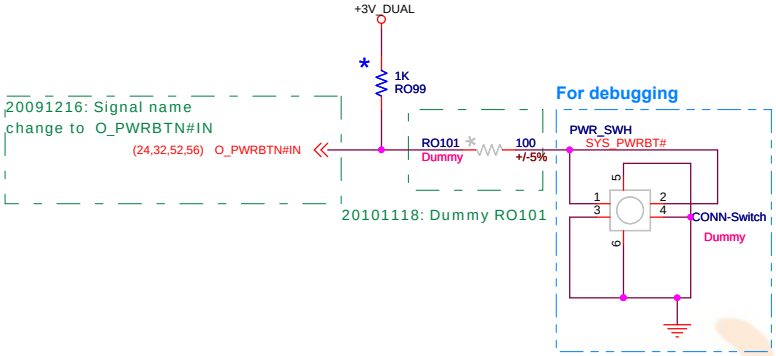
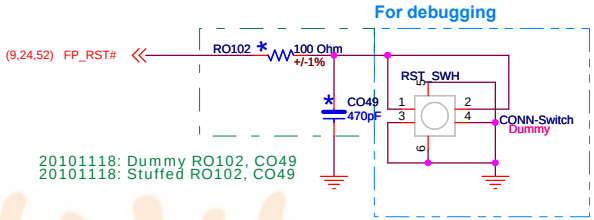
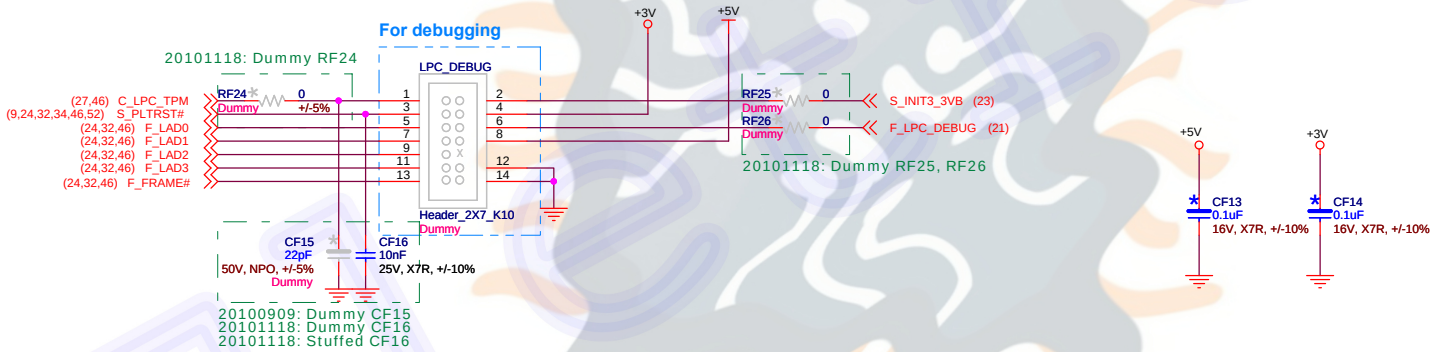
Power Bottom



Reset Bottom



LPC DEBUG



DELL INC.

Title
Pilot Run Conn

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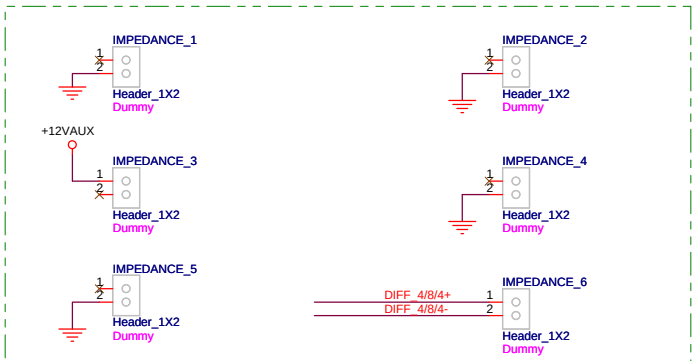
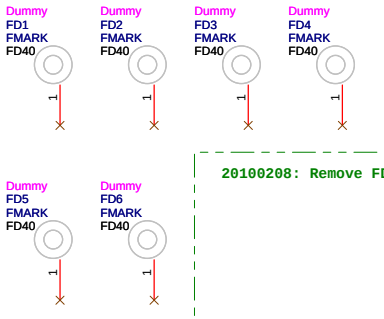
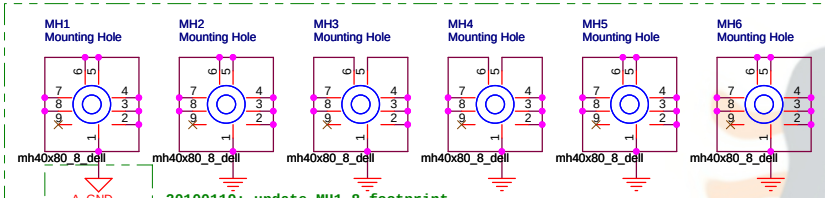


20100224: change IMPEDANCE1~6 size for layout
20100322: Update IMPEDANCE_3 and IMPEDANCE_5 connection
20100325: Update IMPEDANCE_5 connection one pin is empty, another is GND



20100208: Remove FD7~FD12 for routing

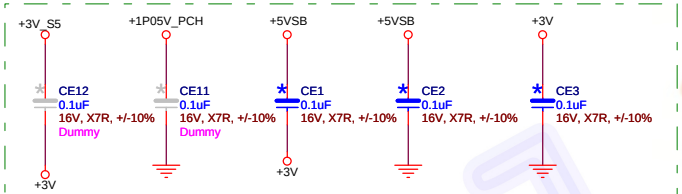


20100204: Remove MH7, MH8

20100505: MH1~MH6 footprint change to mh40x80_8_dell

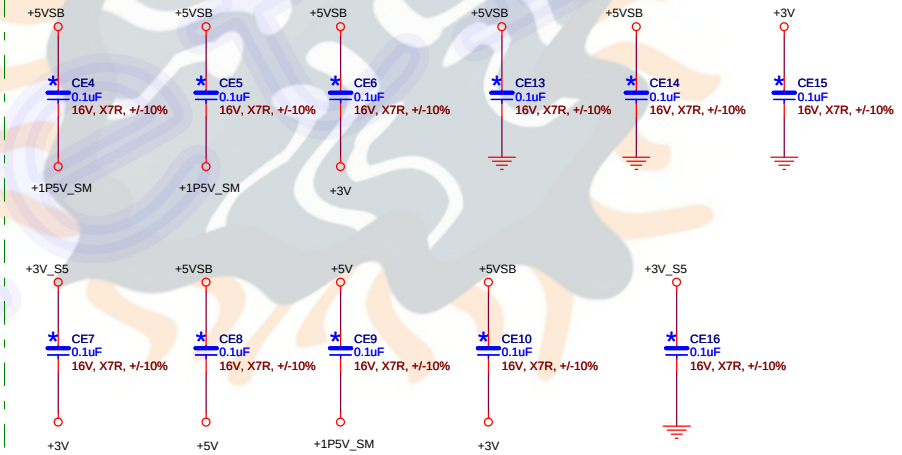
20100119: update MH1~8 footprint

20100204: Change to A_GND for layout



20100202: add Stitching cap 3.3V to 5V for clock signal pair H_Tpclk .
20100208: 1. CE1 change connection from 5V to 5VSB
2. Add CE2,CE3 for EMI

20100309: Add CE11,CE12 for Layout request



20100302: Add CE4~CE10 for EMI

20100304: +3V via CE10 connecte to +5VSB from +5V

20100319: add CE13 , CE14, CE15 for layout request.

20100323: aadd CE16 (+3V_S5->GND) for USB signals layer transitions

DELL INC.

Title: EMI

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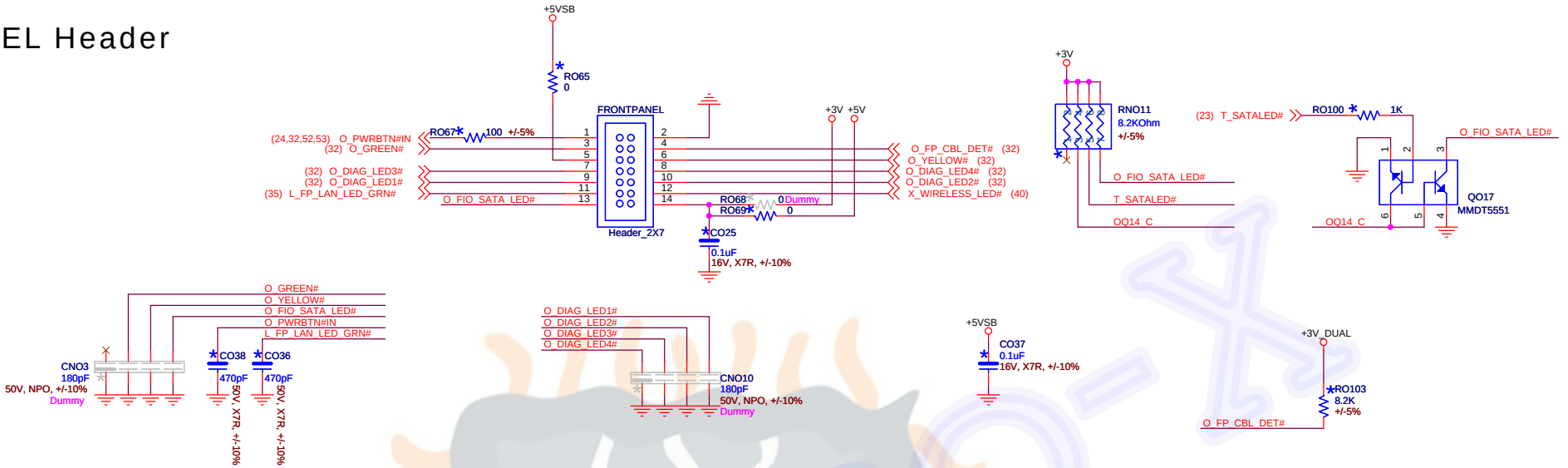
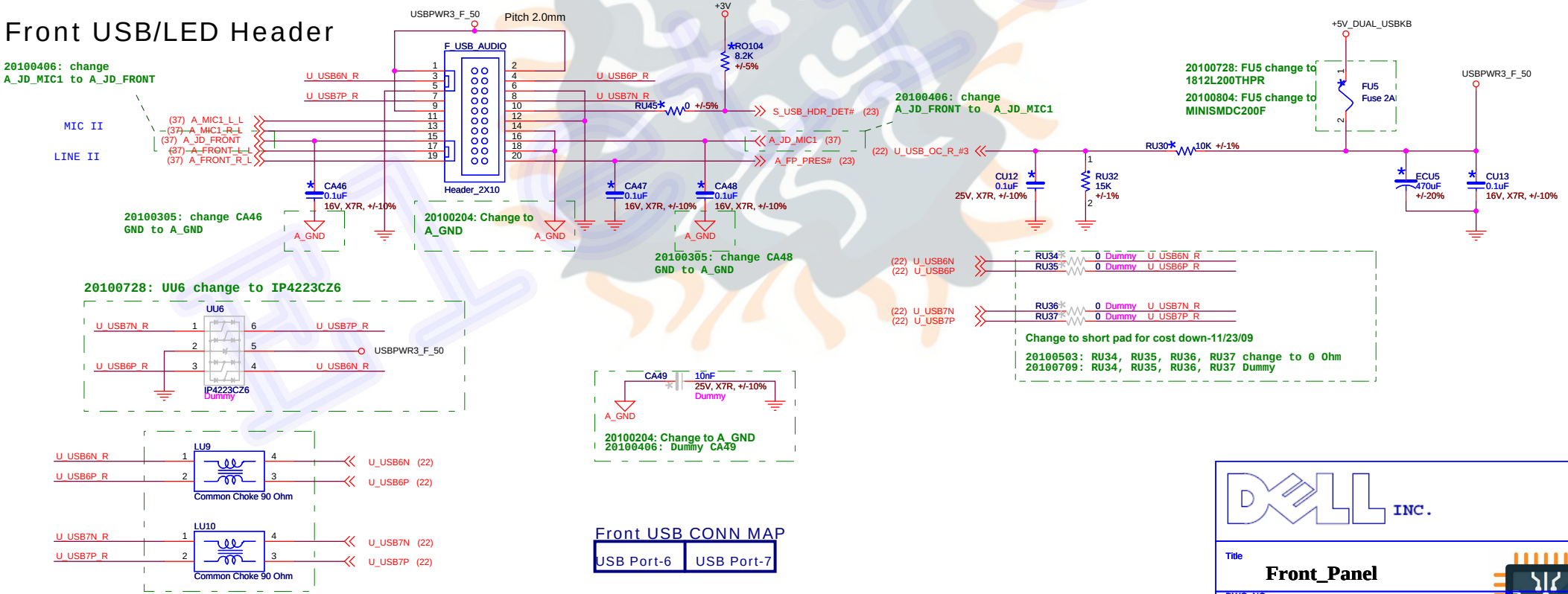
FRONTPANEL Header



Front USB/LED Header



Front USB CONN MAP

USB Port-6	USB Port-7

DELL INC.

Title: **Front_Panel**

DWG NO: **Katsiki_USFF**

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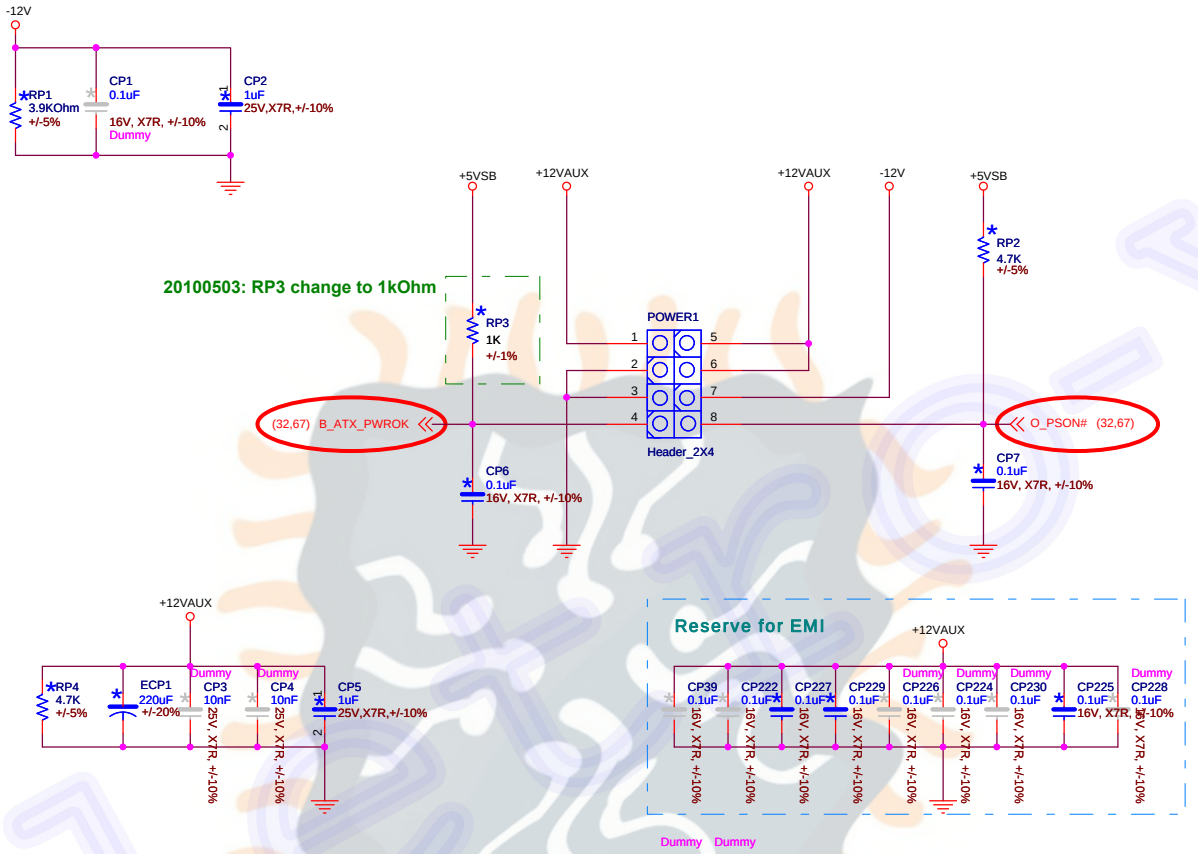
ATX POWER CONNECTOR



DELL INC.

Title: Power Conn

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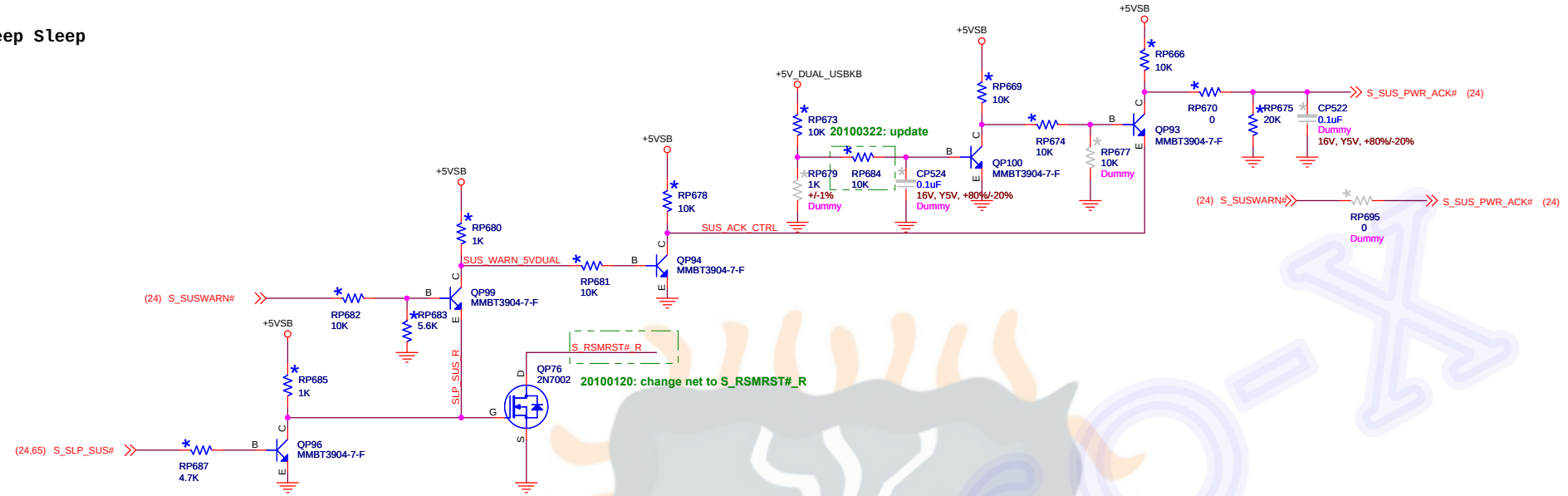
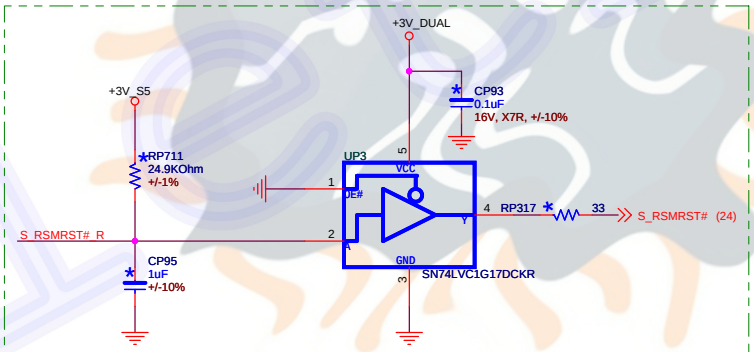
For Deep Sleep

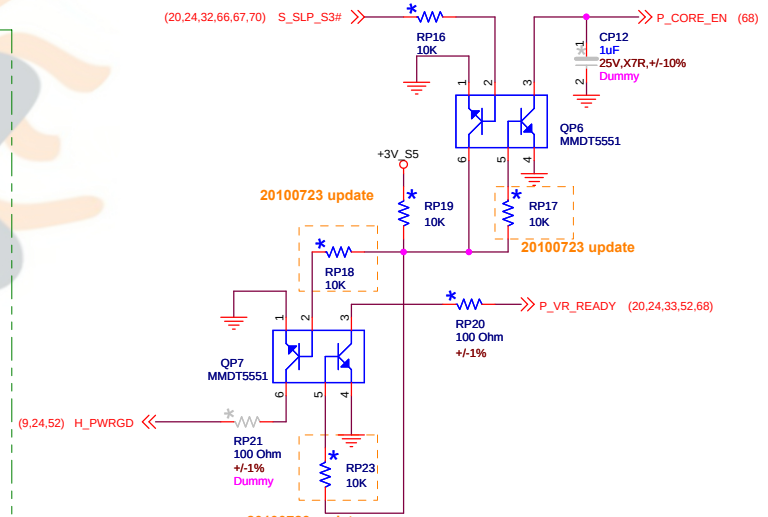


RESUME RESET Logic

Remove QP20 circuit; the same circuit (QS2) in page 24-01/13/10
20100308: CP528 change to 2.2uF; QP57,QP58 change to 3904; RP709 change to 10k
20100406: CP528 change to 1.0uF; RP708 change to 68k
20100505: RP708 change to 71.5k
20100510: RP708 , CP528, QP57, RP709, QP58, RP710 Dummy
20100511: CP528 change size to 0402
20100517: RP708 , CP528, QP57, RP709, QP58, RP710 removed



VR_READY DEFENSIVE



DELL INC.

Title: Power Sequence

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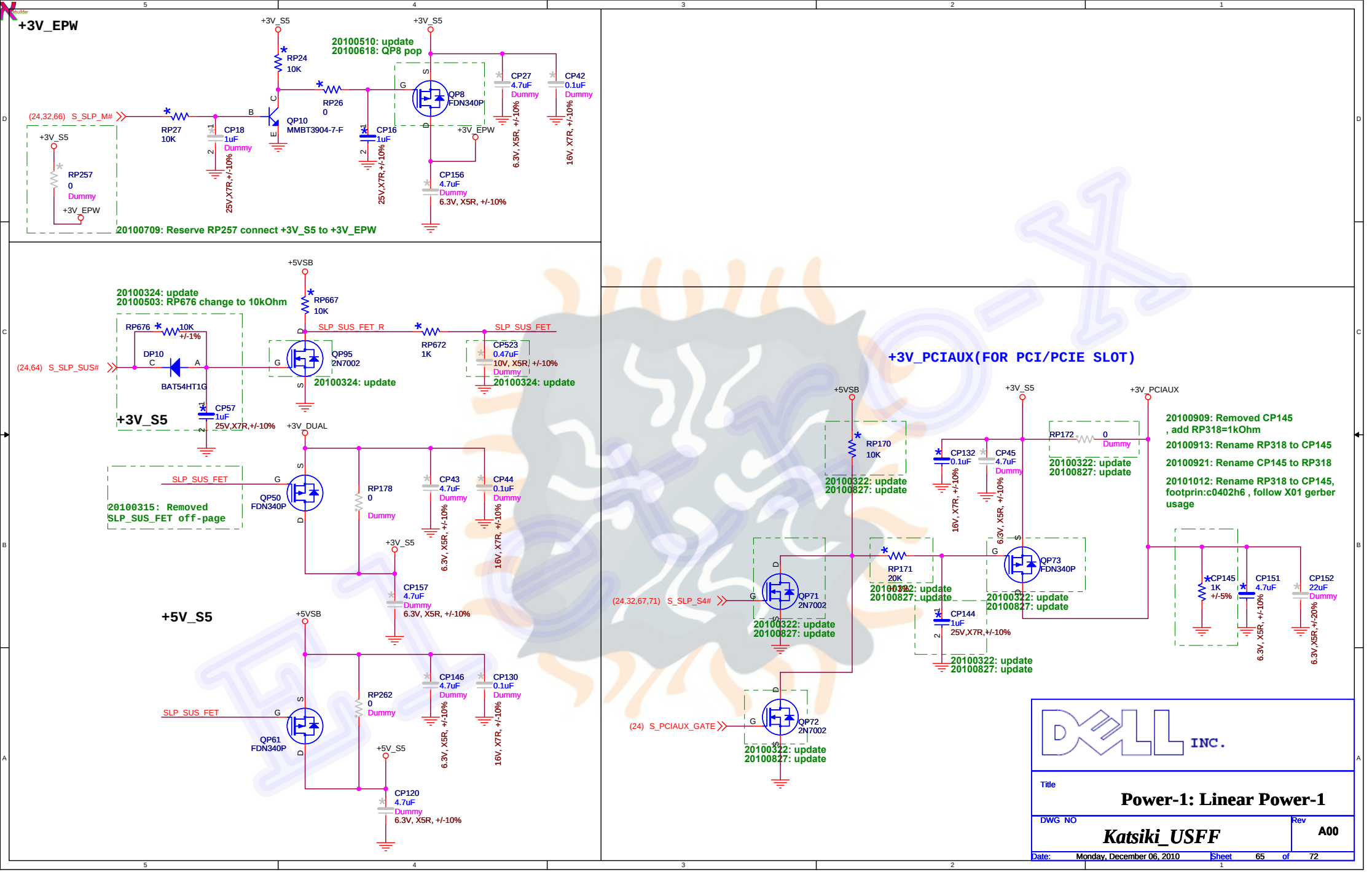
+3V_EPW
20100510: update
20100618: QP8 pop
RP24 10K
RP26 0
QP8 FDN340P
CP27 4.7uF Dummy
CP42 0.1uF Dummy
(24,32,66) S_SLP_M#
RP27 10K
QP10 MMBT3904-7-F
CP18 1uF Dummy 25V,X7R,+/-10%
CP16 1uF 25V,X7R,+/-10%
RP257 0 Dummy
CP156 4.7uF Dummy 6.3V, X5R, +/-10%
20100709: Reserve RP257 connect +3V_S5 to +3V_EPW
20100324: update
20100503: RP676 change to 10kOhm
RP667 10K
RP676 10K +/-1%
DP10 BAT54HT1G
(24,64) S_SLP_SUS#
QP95 2N7002
SLP_SUS_FET_R
RP672 1K
CP523 0.47uF 10V, X5R, +/-10% Dummy
CP57 1uF 25V,X7R,+/-10%
+3V_S5
+3V_DUAL
SLP_SUS_FET
QP50 FDN340P
20100315: Removed SLP_SUS_FET off-page
RP178 0 Dummy
CP43 4.7uF Dummy 6.3V, X5R, +/-10%
CP44 0.1uF Dummy 16V, X7R, +/-10%
CP157 4.7uF Dummy 6.3V, X5R, +/-10%
+5V_S5
+5VSB
RP262 0 Dummy
QP61 FDN340P
CP146 4.7uF Dummy 6.3V, X5R, +/-10%
CP130 0.1uF Dummy 16V, X7R, +/-10%
CP120 4.7uF Dummy 6.3V, X5R, +/-10%
+3V_PCIAUX(FOR PCI/PCIE SLOT)
RP170 10K
20100322: update
20100827: update
(24,32,67,71) S_SLP_S4#
QP71 2N7002
RP171 20K
CP132 0.1uF 16V, X7R, +/-10%
CP45 4.7uF Dummy 6.3V, X5R, +/-10%
QP73 FDN340P
CP144 1uF 25V,X7R,+/-10%
RP172 0 Dummy
20100909: Removed CP145 , add RP318=1kOhm
20100913: Rename RP318 to CP145
20100921: Rename CP145 to RP318
20101012: Rename RP318 to CP145, footprin:c0402h6 , follow X01 gerber usage
CP145 1K +/-5%
CP151 4.7uF 6.3V, X5R, +/-10%
CP152 22uF Dummy 6.3V, X5R, +/-20%
(24) S_PCIAUX_GATE
QP72 2N7002
DELL INC.
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Power-1: Linear Power-1
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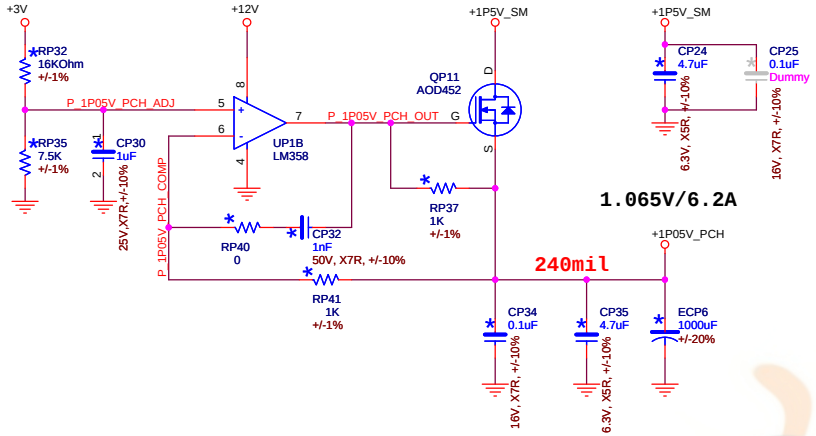
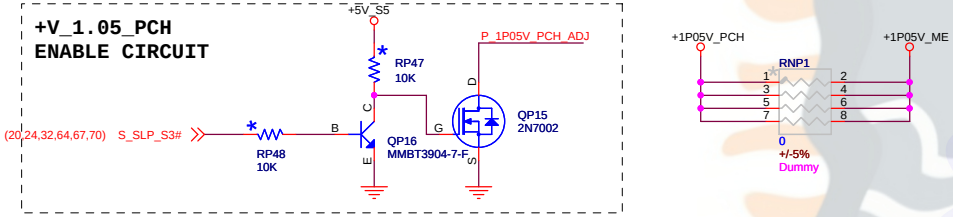
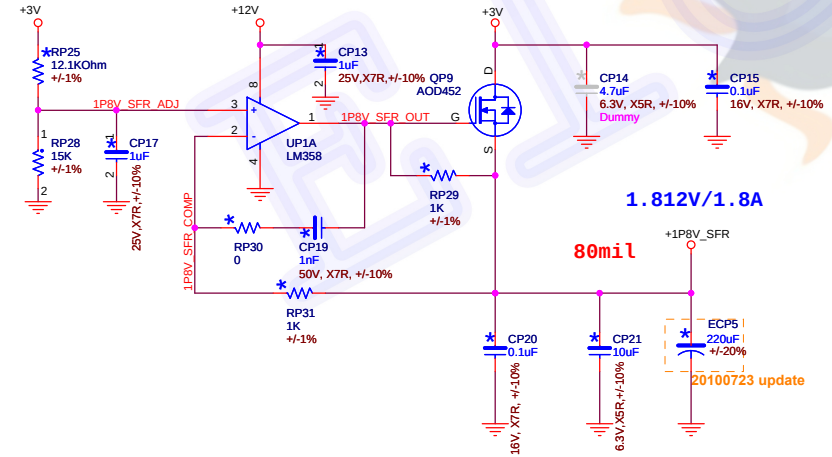
+V_1.05_PCH



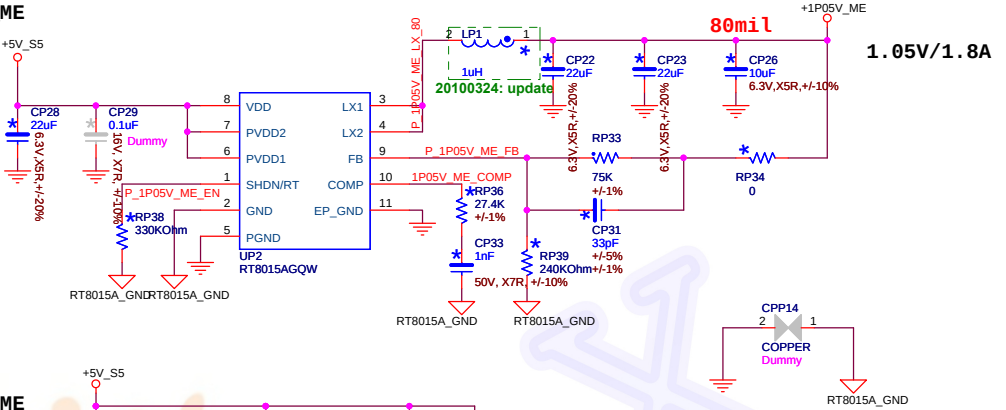
+V_1.05_PCH ENABLE CIRCUIT



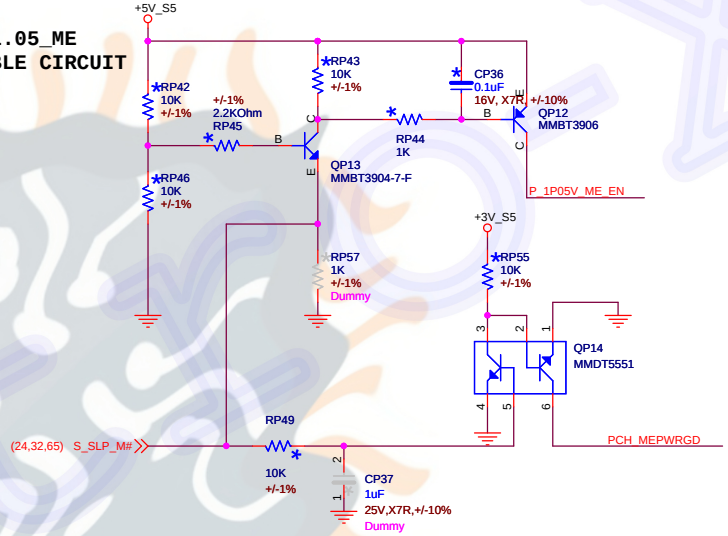
+V_1P8_SFR

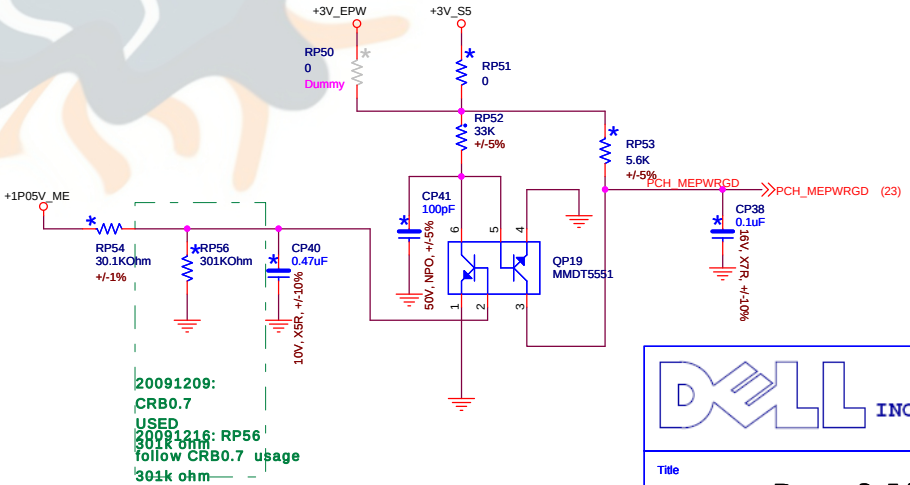


+V_1.05_ME



+V_1.05_ME ENABLE CIRCUIT





DELL INC.

Title: **Power-2: Linear Power 2**

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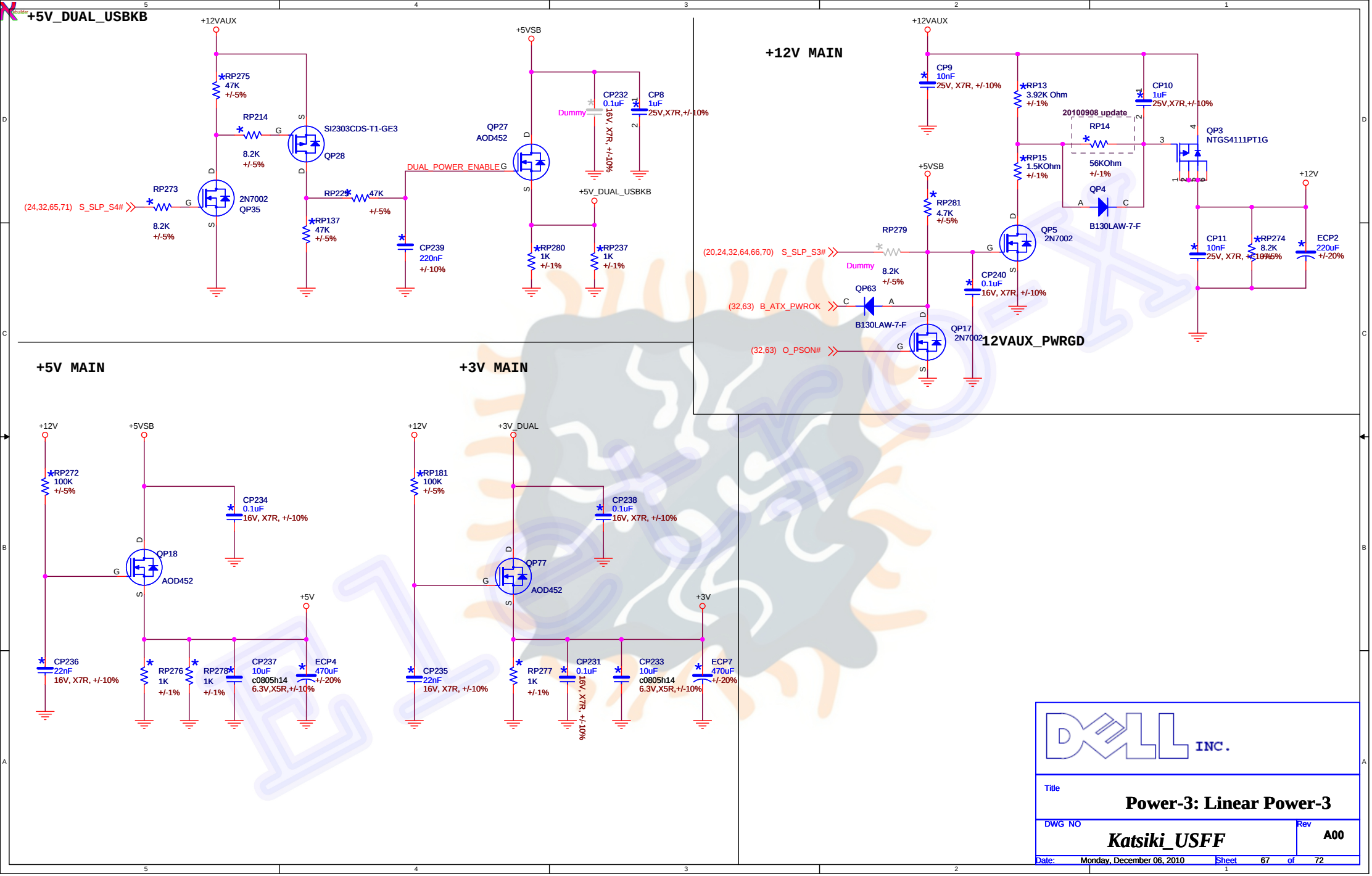
+5V_DUAL_USBKB
+12VAUX
RP275 47K +/-5%
RP214
8.2K +/-5%
SI2303CDS-T1-GE3
QP28
RP273
8.2K +/-5%
2N7002
QP35
(24,32,65,71) S_SLP_S4#
RP225 47K +/-5%
RP137 47K +/-5%
CP239 220nF +/-10%
DUAL_POWER_ENABLE
+5VSB
QP27 AOD452
CP232 0.1uF 16V, X7R, +/-10%
Dummy
CP8 1uF 25V,X7R,+/-10%
+5V_DUAL_USBKB
RP280 1K +/-1%
RP237 1K +/-1%
+12V MAIN
+12VAUX
CP9 10nF 25V, X7R, +/-10%
RP13 3.92K Ohm +/-1%
CP10 1uF 25V,X7R,+/-10%
20100908 update
RP14 56KOhm +/-1%
QP3 NTGS4111PT1G
RP15 1.5KOhm +/-1%
QP4 B130LAW-7-F
+5VSB
RP281 4.7K +/-5%
RP279 Dummy 8.2K +/-5%
(20,24,32,64,66,70) S_SLP_S3#
QP5 2N7002
CP240 0.1uF 16V, X7R, +/-10%
QP63 B130LAW-7-F
(32,63) B_ATX_PWROK
QP17 2N7002
(32,63) O_PSON#
12VAUX_PWRGD
CP11 10nF 25V, X7R, +/-10%
RP274 8.2K +/-5%
ECP2 220uF +/-20%
+12V
+5V MAIN
+12V
+5VSB
RP272 100K +/-5%
CP234 0.1uF 16V, X7R, +/-10%
QP18 AOD452
+5V
CP236 22nF 16V, X7R, +/-10%
RP276 1K +/-1%
RP278 1K +/-1%
CP237 10uF c0805h14 6.3V,X5R,+/-10%
ECP4 470uF +/-20%
+3V MAIN
+12V
+3V_DUAL
RP181 100K +/-5%
CP238 0.1uF 16V, X7R, +/-10%
QP77 AOD452
+3V
CP235 22nF 16V, X7R, +/-10%
RP277 1K +/-1%
CP231 0.1uF 16V, X7R, +/-10%
CP233 10uF c0805h14 6.3V,X5R,+/-10%
ECP7 470uF +/-20%
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Sugar Bay VR12 POWER - 3+1 PHASE

VCC_CORE

VCC_AXG

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

VCORE PORTION

V_GT PORTION

OPTION: DISALBE V_GT

PUT COLSE TO V_GT HOT SPOT

PUT COLSE TO VCORE HOT SPOT

BOTTOM PAD CONNECT TO GND Through 4 VIAs

VCORE VBOOT SET AT 0V

V_GT IMAX SET AT 35A

PWM ADDRESS

VCORE IMAX SET AT 73A

DELL INC.

Title: Power-4: Vcore

DWG NO: Katsiki_USFF

Rev: A00

Date: Monday, December 06, 2010

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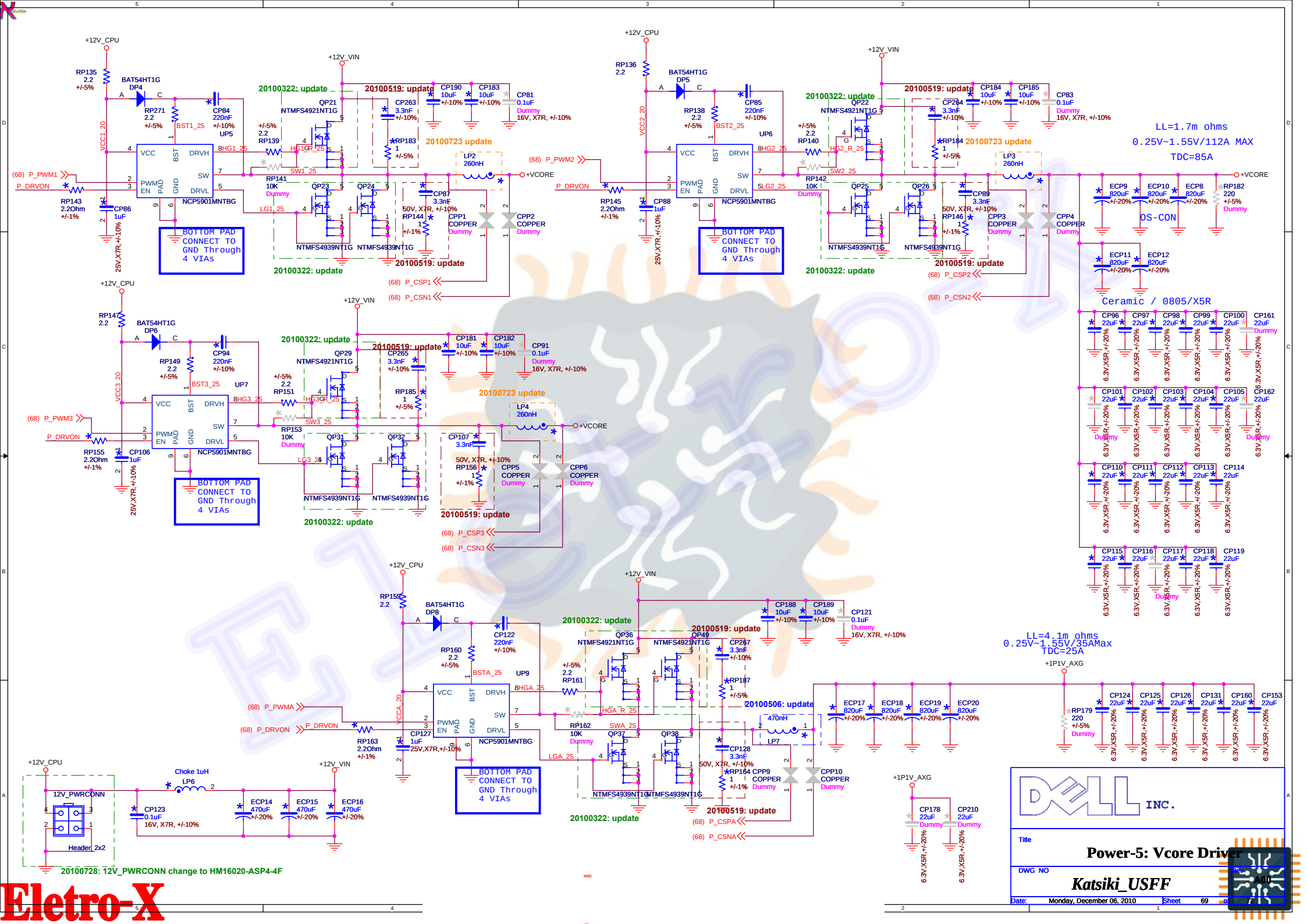
+12V_CPU
+12V_VIN
RP135 2.2 +/-5%
BAT54HT1G DP4
RP271 2.2 +/-5%
CP84 220nF +/-10%
UP5
VCC1_20
VCC
BST
DRVH
8HG1_25
PWM EN
PAD
GND
SW
DRVL
NCP5901MNTBG
BST1_25
HG1_R_25
SW1_25
LG1_25
RP139 2.2 +/-5%
RP141 10K Dummy
RP143 2.2Ohm +/-1%
CP86 1uF
25V,X7R,+/-10%
BOTTOM PAD CONNECT TO GND Through 4 VIAs
QP21 NTMFS4921NT1G
QP23
QP24
NTMFS4939NT1G
CP263 3.3nF +/-10%
RP183 1 +/-5%
CP190 10uF +/-10%
CP183 10uF +/-10%
CP81 0.1uF Dummy 16V, X7R, +/-10%
20100322: update
20100519: update
20100723 update
LP2 260nH
CP87 3.3nF 50V, X7R, +/-10%
RP144 1 +/-1%
CPP1 COPPER Dummy
CPP2 COPPER Dummy
(68) P_PWM1
P_DRVON
(68) P_CSP1
(68) P_CSN1
+VCORE
RP136 2.2
RP138 2.2 +/-5%
RP145 2.2Ohm +/-1%
CP88 1uF
UP6
BST2_25
HG2_R_25
SW2_25
LG2_25
RP140 2.2 +/-5%
RP142 10K Dummy
QP22
QP25
QP26
CP85 220nF +/-10%
CP264 3.3nF +/-10%
RP184 1 +/-5%
CP89 3.3nF 50V, X7R, +/-10%
RP146 1 +/-1%
CPP3 COPPER Dummy
CPP4 COPPER Dummy
CP184 10uF +/-10%
CP185 10uF +/-10%
CP83 0.1uF Dummy 16V, X7R, +/-10%
(68) P_PWM2
(68) P_CSP2
(68) P_CSN2
LP3 260nH
LL=1.7m ohms
0.25V~1.55V/112A MAX
TDC=85A
ECP9 820uF +/-20%
ECP10 820uF +/-20%
ECP8 820uF +/-20%
RP182 220 +/-5% Dummy
OS-CON
ECP11 820uF +/-20%
ECP12 820uF +/-20%
Ceramic / 0805/X5R
CP96 22uF
CP97 22uF
CP98 22uF
CP99 22uF
CP100 22uF
CP161 22uF Dummy
CP101 22uF
CP102 22uF
CP103 22uF
CP104 22uF
CP105 22uF
CP162 22uF Dummy
CP110 22uF
CP111 22uF
CP112 22uF
CP113 22uF
CP114 22uF
CP115 22uF
CP116 22uF
CP117 22uF Dummy
CP118 22uF
CP119 22uF
6.3V,X5R,+/-20%
RP147 2.2
RP149 2.2 +/-5%
CP94 220nF +/-10%
UP7
VCC3_20
BST3_25
HG3_25
SW3_25
LG3_25
RP151 2.2 +/-5%
RP153 10K Dummy
RP155 2.2Ohm +/-1%
CP106 1uF
QP29 NTMFS4921NT1G
QP31
QP32
CP265 3.3nF +/-10%
RP185 1 +/-5%
CP181 10uF +/-10%
CP182 10uF +/-10%
CP91 0.1uF Dummy 16V, X7R, +/-10%
LP4 260nH
CP107 3.3nF 50V, X7R, +/-10%
RP156 1 +/-1%
CPP5 COPPER Dummy
CPP6 COPPER Dummy
(68) P_PWM3
(68) P_CSP3
(68) P_CSN3
RP159 2.2
CP122 220nF +/-10%
UP9
VCCA_20
BSTA_25
HGA_25
SWA_25
LGA_25
RP160 2.2 +/-5%
RP161 2.2 +/-5%
RP162 10K Dummy
RP163 2.2Ohm +/-1%
CP127 1uF 25V,X7R,+/-10%
QP36 NTMFS4921NT1G
QP37
QP38
NTMFS4939NT1G
CP267 3.3nF +/-10%
RP187 1 +/-5%
CP128 3.3nF 50V, X7R, +/-10%
RP164 1 +/-1%
CPP9 COPPER Dummy
CPP10 COPPER Dummy
CP188 10uF +/-10%
CP189 10uF +/-10%
CP121 0.1uF Dummy 16V, X7R, +/-10%
20100506: update
470nH
LP7
(68) P_PWMA
(68) P_CSPA
(68) P_CSNA
LL=4.1m ohms
0.25V~1.55V/35AMax
TDC=25A
+1P1V_AXG
ECP17 820uF +/-20%
ECP18 820uF +/-20%
ECP19 820uF +/-20%
ECP20 820uF +/-20%
RP179 220 +/-5% Dummy
CP124 22uF
CP125 22uF
CP126 22uF
CP131 22uF
CP160 22uF
CP153 22uF
CP178 22uF Dummy
CP210 22uF Dummy
Choke 1uH
LP6
12V_PWRCONN
Header_2x2
CP123 0.1uF 16V, X7R, +/-10%
ECP14 470uF +/-20%
ECP15 470uF +/-20%
ECP16 470uF +/-20%
20100728: 12V_PWRCONN change to HM16020-ASP4-4F
DELL INC.
Title
Power-5: Vcore Driver
DWG NO
Katsiki_USFF
Rev
A00
Date: Monday, December 06, 2010
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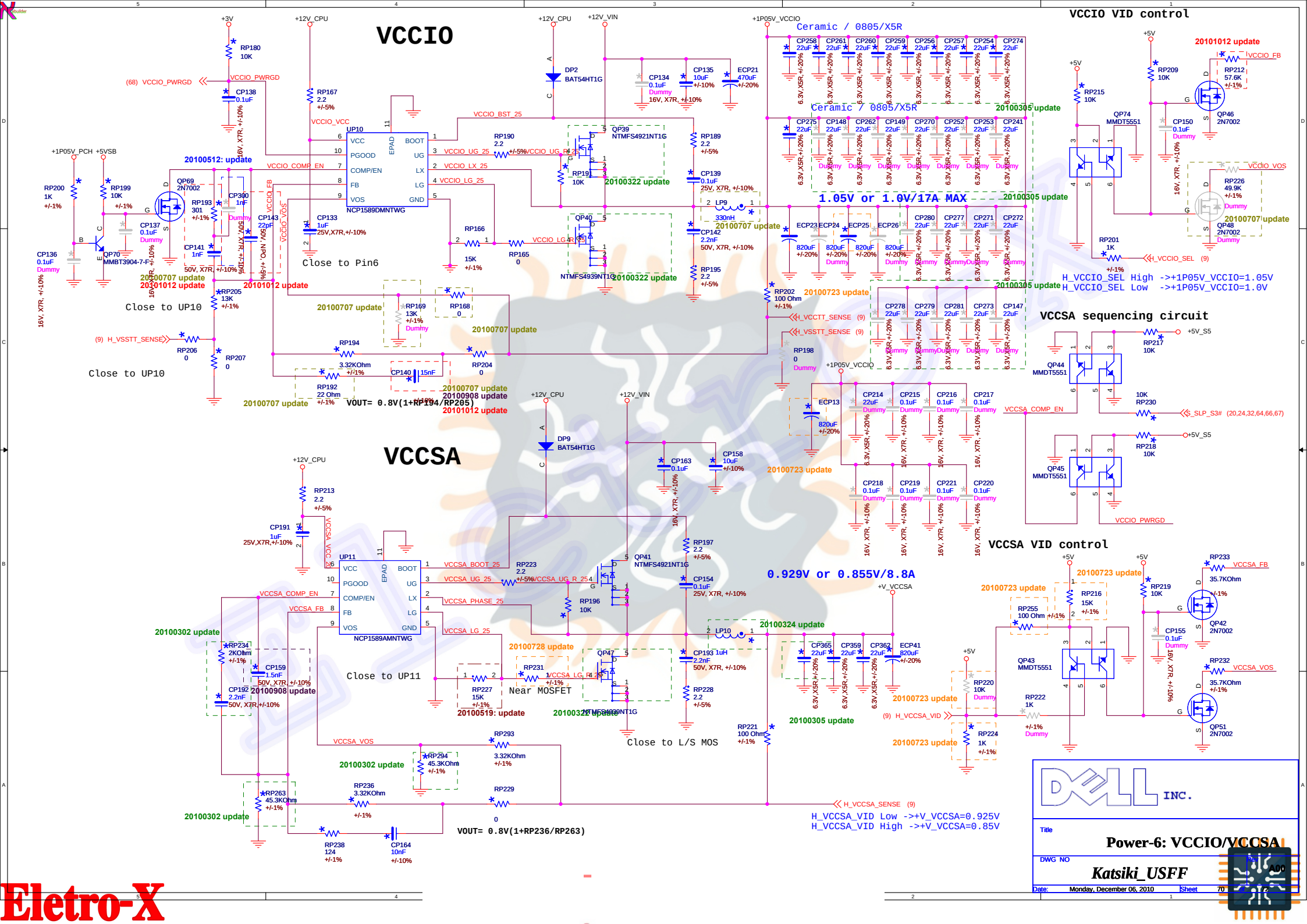
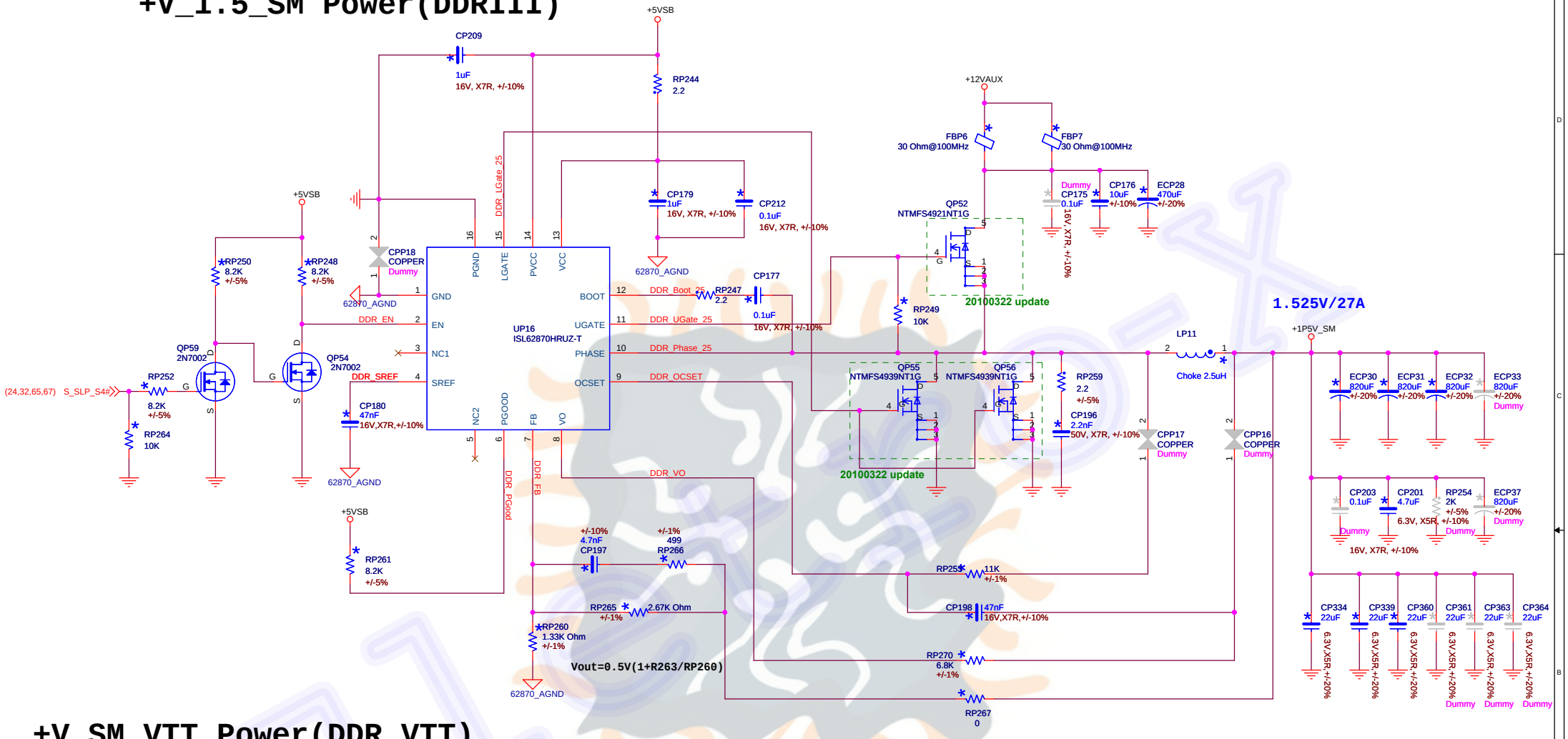
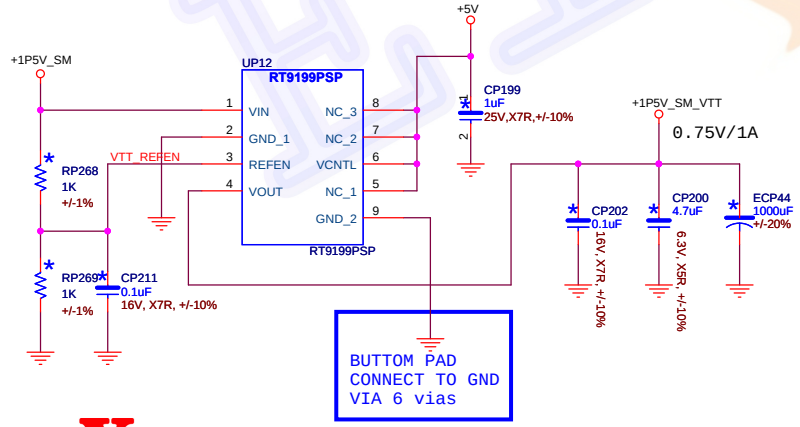
Eletro-X


VCCIO
VCCSA
VCCIO VID control
VCCSA sequencing circuit
VCCSA VID control
Ceramic / 0805/X5R
1.05V or 1.0V/17A MAX
0.929V or 0.855V/8.8A
20101012 update
20100305 update
20100707 update
20100322 update
20100723 update
20100908 update
20100519: update
20100302 update
20100324 update
20100728 update
Close to Pin6
Close to UP10
Close to UP11
Near MOSFET
Close to L/S MOS
VOUT= 0.8V(1+RP194/RP205)
VOUT= 0.8V(1+RP236/RP263)
H_VCCIO_SEL High ->+1P05V_VCCIO=1.05V
H_VCCIO_SEL Low ->+1P05V_VCCIO=1.0V
H_VCCSA_VID Low ->+V_VCCSA=0.925V
H_VCCSA_VID High ->+V_VCCSA=0.85V
NCP1589DMNTWG
NCP1589AMNTWG
Title
Power-6: VCCIO/VCCSA
DWG NO
Katsiki_USFF
Date: Monday, December 06, 2010
Sheet 70

+V_1.5_SM Power(DDRIII)



+V_SM_VTT Power(DDR VTT)

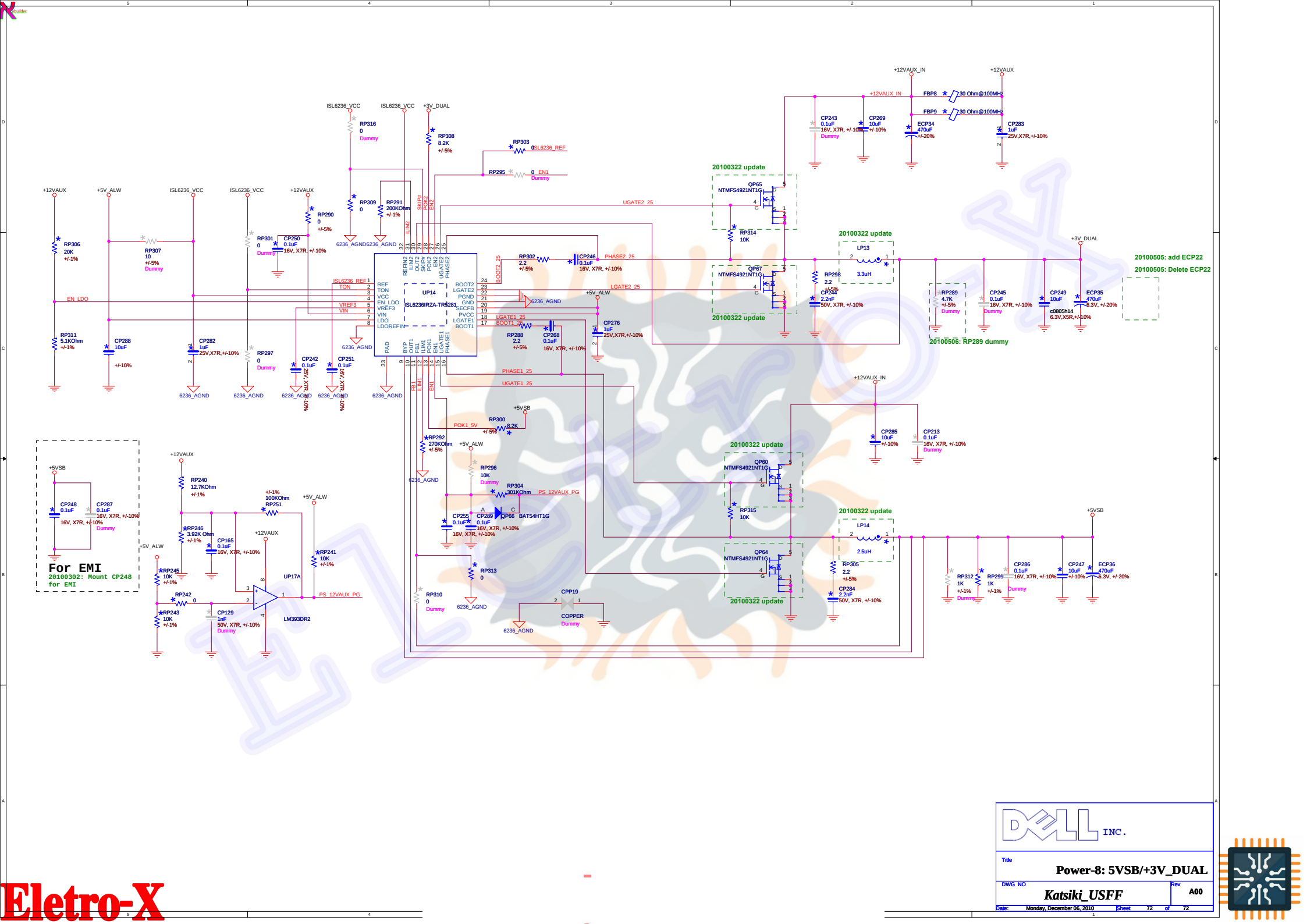


DELL INC.

Title: Power-7: DD3

DWG NO: Katsiki_USFF

Date: Monday, December 06, 2010 Sheet 71 of 72


+12VAUX
+5V_ALW
ISL6236_VCC
+3V_DUAL
+12VAUX_IN
+5VSB
6236_AGND
UP14
ISL6236IRZA-TR5281
UP17A
LM393DR2
EN_LDO
UGATE2_25
LGATE2_25
PHASE2_25
BOOT2_25
UGATE1_25
LGATE1_25
PHASE1_25
BOOT1_25
PS_12VAUX_PG
POK1_5V
20100322 update
20100505: add ECP22
20100505: Delete ECP22
20100506: RP289 dummy
For EMI
20100302: Mount CP248 for EMI
DELL INC.
Power-8: 5VSB/+3V_DUAL
Katsiki_USFF
A00
Monday, December 06, 2010
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