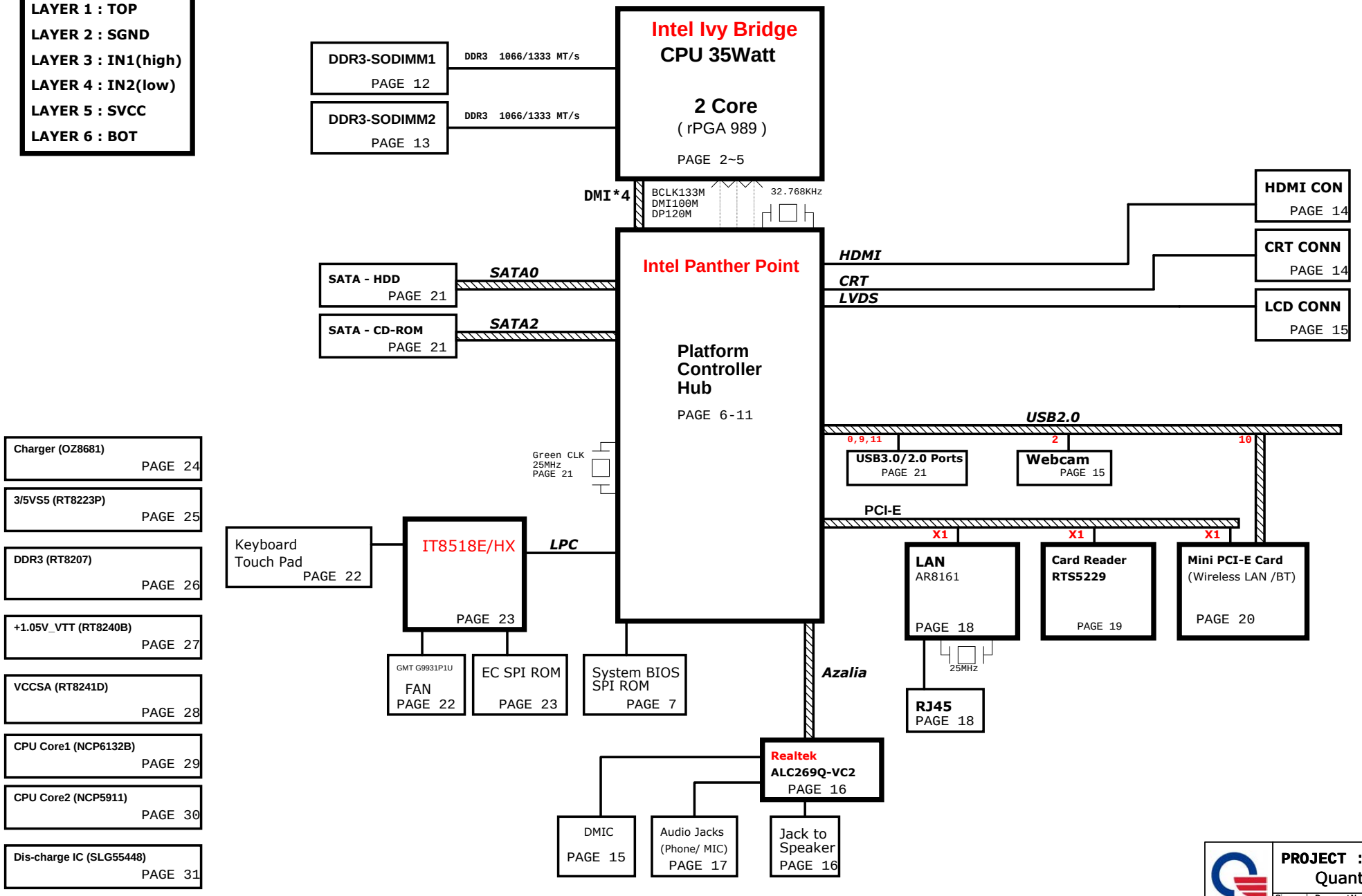
SW6C UMA (14") BLOCK DIAGRAM

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(high)
LAYER 4 : IN2(low)
LAYER 5 : SVCC
LAYER 6 : BOT

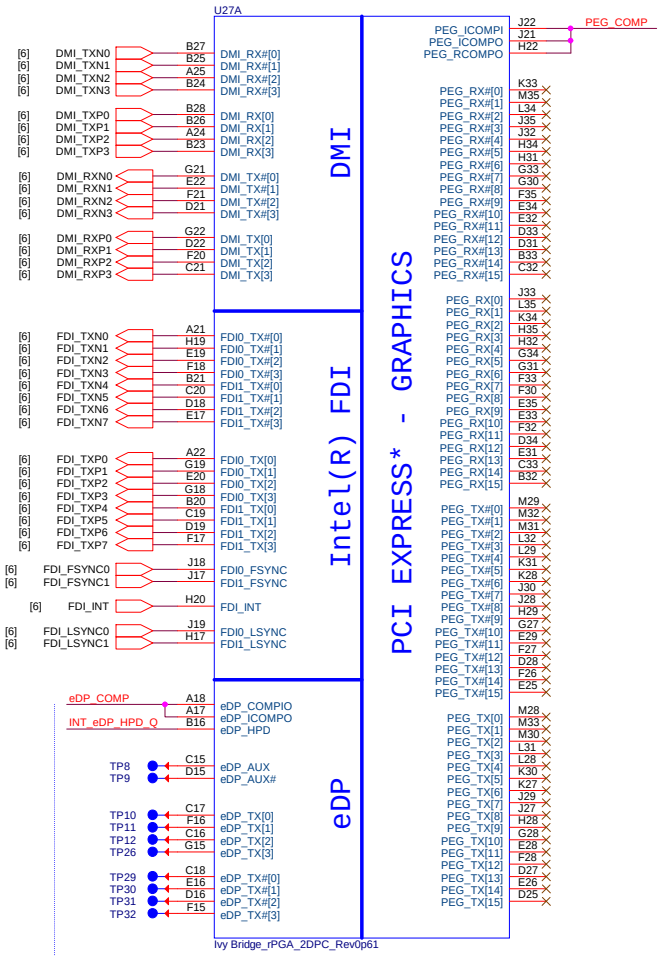


NB5	PROJECT : SW6C Quanta Computer Inc.	
Size	Document Number Block Diagram	Rev 1A
Date: Tuesday, November 20, 2012	Sheet 1 of 34	

Ivy Bridge Processor (DMI,PEG,FDI)

Ivy Bridge Processor (CLK,MISC,JTAG)

02



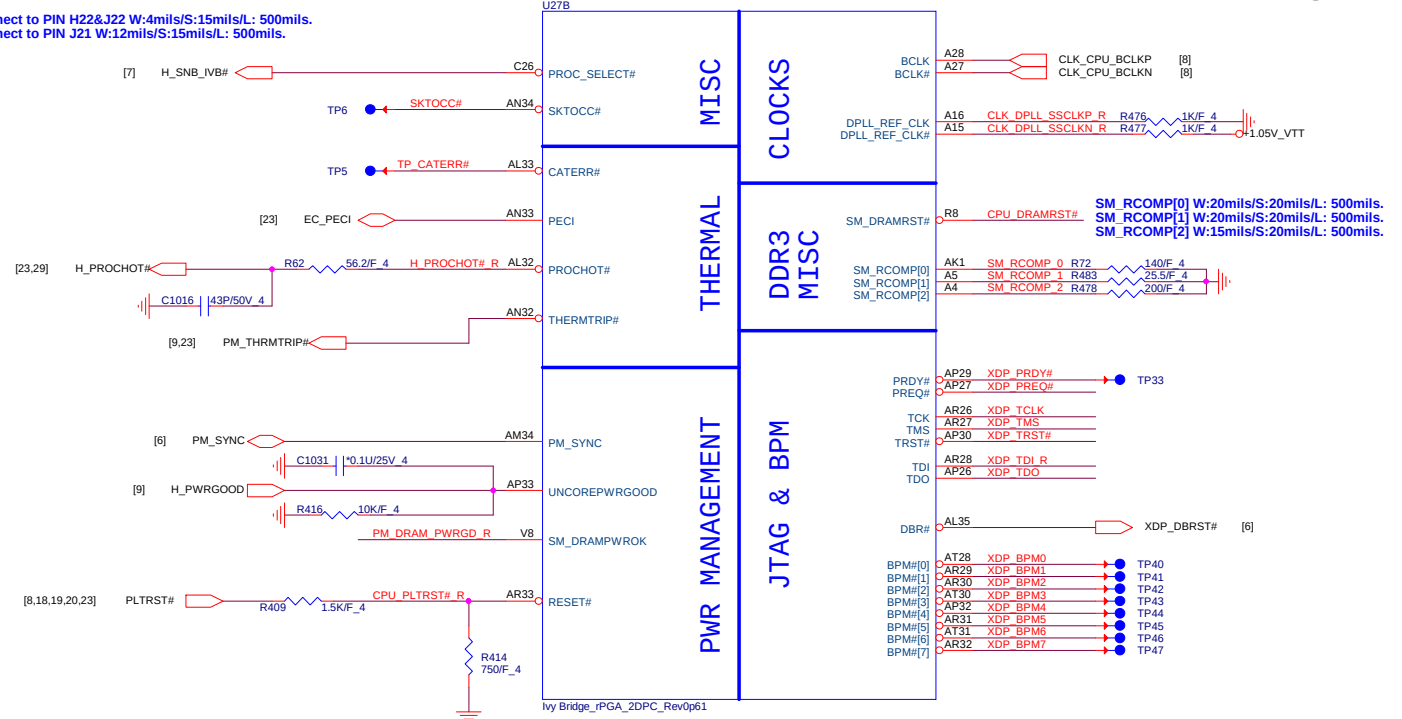
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

+1.05V_VTT R481 24.9/F_4 eDP_COMP
+1.05V_VTT R81 24.9/F_4 PEG_COMP

eDP_HPD can be left as no connect if entire eDP is disabled.

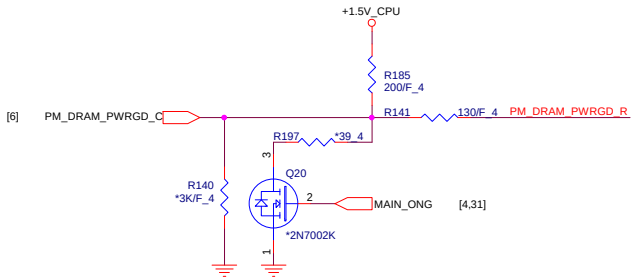
+1.05V_VTT R482 *10K/F_4 INT_eDP_HPD_Q

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

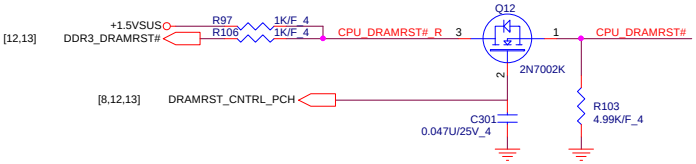


SM_RCOMP[0] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils.
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils.

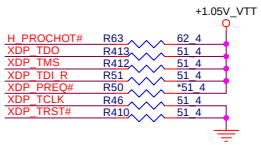
SM_DRAMPWROK Processor Input.



DDR3 DRAM RESET



Processor pull-up (CPU)



NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
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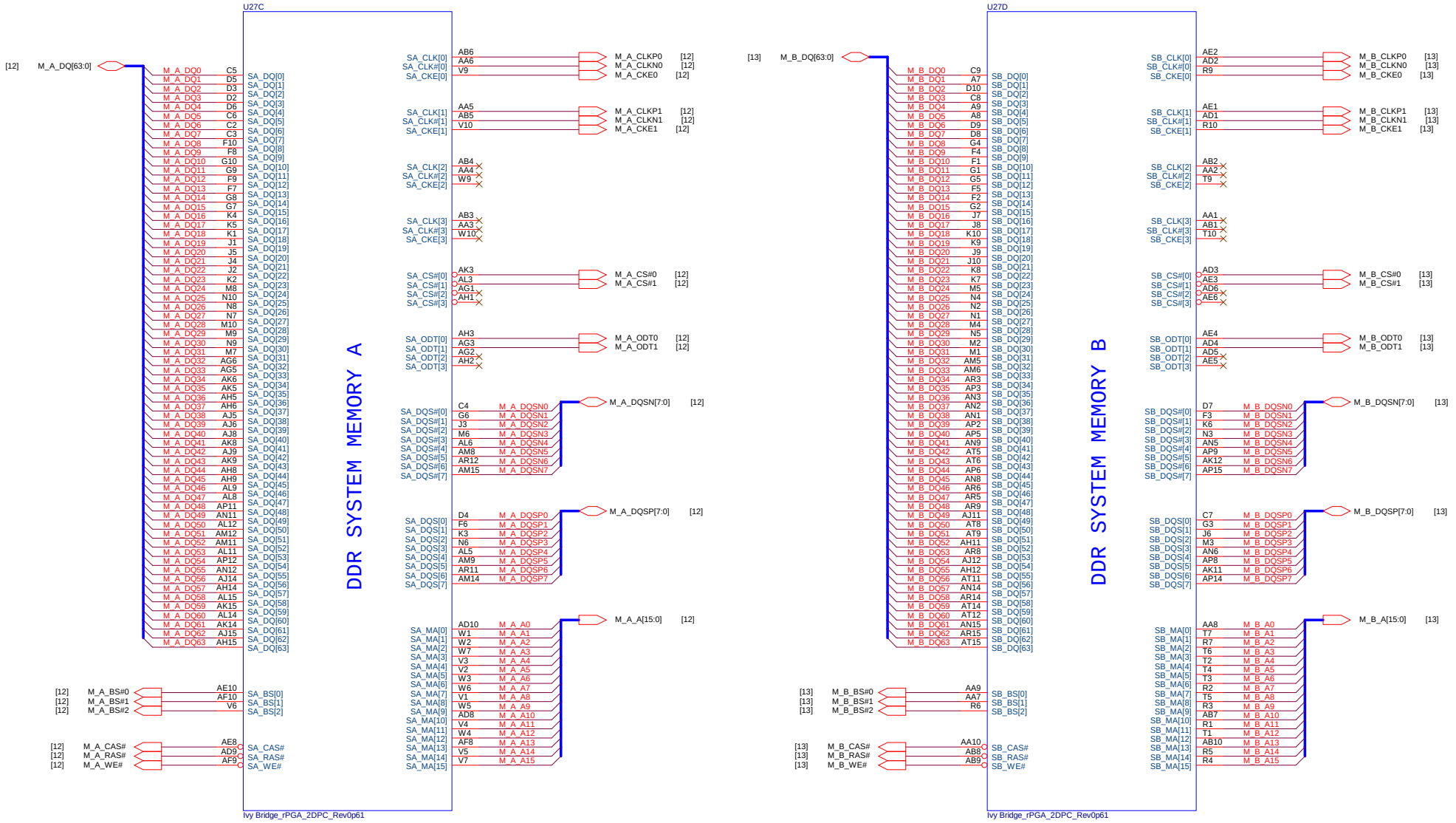
Ivy Bridge Processor (DDR3)



NB5

PROJECT : SW6C

Quanta Computer Inc.

Size	Document Number	Rev
	SNB 2/4 (DDR3 I/F)	1A

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Ivy Bridge Processor (POWER)

Ivy Bridge Processor (GRAPHIC POWER)

04

POWER

U27F

U27G

CORE SUPPLY

SNB: 55A
IVY: 55A

+VCC_CORE

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

C609 22U/6.3VS_6 C607 22U/6.3VS_6 C79 22U/6.3VS_6
C36 22U/6.3VS_6 C83 22U/6.3VS_6 C39 22U/6.3VS_6
C616 22U/6.3VS_6 C599 22U/6.3VS_6 C132 22U/6.3VS_6
C108 22U/6.3VS_6 C166 22U/6.3VS_6 C613 22U/6.3VS_6
C230 22U/6.3VS_6 C608 22U/6.3VS_6 C165 22U/6.3VS_6
C190 22U/6.3VS_6 C167 22U/6.3VS_6 C117 22U/6.3VS_6
C141 22U/6.3VS_6 C123 22U/6.3VS_6 C206 22U/6.3VS_6
C600 22U/6.3VS_6 C602 22U/6.3VS_6 C573 22U/6.3VS_6
C604 22U/6.3VS_6 C606 22U/6.3VS_6 C113 22U/6.3VS_6
C598 22U/6.3VS_6 C605 22U/6.3VS_6 C601 22U/6.3VS_6

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

PEG AND DDR

SNB: 8.5A
IVY: 8.5A

+1.05V_VTT

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C203 22U/6.3VS_6 C235 22U/6.3VS_6 C666 22U/6.3VS_6
C131 22U/6.3VS_6 C204 22U/6.3VS_6 C105 22U/6.3VS_6
C218 *22U/6.3VS_6 C150 22U/6.3VS_6 C614 22U/6.3VS_6
C610 *22U/6.3VS_6 C173 *22U/6.3VS_6 C189 *22U/6.3VS_6
C652 22U/6.3VS_6 C111 *22U/6.3VS_6 C116 *22U/6.3VS_6
C236 *22U/6.3VS_6 C625 22U/6.3VS_6 C139 *22U/6.3VS_6
C619 *22U/6.3VS_6 C636 22U/6.3VS_6 C217 22U/6.3VS_6

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

SVID

+1.05V_VTT

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VR_SVID_CLK
VIDSOUT AJ28 VR_SVID_DATA

SENSE LINES

VCC_SENSE AJ35 R65 100/F_4 +VCC_CORE
VSS_SENSE AJ34 R67 100/F_4

VCCIO_SENSE B10 R1001 10/F_4 +1.05V_VTT
VSS_SENSE_VCCIO A10 R1002 10/F_4

VCCP_SENSE [27]
VSSP_SENSE [27]

GRAPHICS

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

SNB: 21.5A
IVY: 38A

+VCC_GFX

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

C581 22U/6.3VS_6 C133 22U/6.3VS_6
C118 22U/6.3VS_6 C106 22U/6.3VS_6
C119 22U/6.3VS_6 C580 22U/6.3VS_6
C107 22U/6.3VS_6 C138 22U/6.3VS_6
C612 22U/6.3VS_6 C140 22U/6.3VS_6
C130 22U/6.3VS_6 C611 22U/6.3VS_6

1.8V RAIL

SNB: 1.5A
IVY: 1.5A

+1.8V

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

C708 10U/6.3V_6 C712 1U/16V_4 C713 1U/16V_4 C709 330U/2V_7343

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R68 100/F_4 +VCC_GFX
R66 100/F_4

VCC_AXG_SENSE [29]
VSS_AXG_SENSE [29]

+VDDR_REF_CPU & DDR_VTTREF must use 10mils width

VREF

+VDDR_REF_CPU

Q8 2N7002K
DDR_VTTREF [12,13,26]

SM_VREF AL1
C3001 0.1U/25V_4
R3002 3.3K_4
C3002 470P/50V_4
MAIND [31]

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

SMDDR_VREF_DQ0_M3 [12]
SMDDR_VREF_DQ1_M3 [13]

R88 *1K/F_4
R121 *1K/F_4

DDR3 -1.5V RAILS

SNB: 5A
IVY: 5A

+1.5V_CPU

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

C187 10U/6.3V_6 C146 10U/6.3V_6 C109 10U/6.3V_6 C145 10U/6.3V_6
C134 10U/6.3V_6 C114 10U/6.3V_6 C1001 *330U/2.5V_3528

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

SNB: 6A
IVY: 6A

+VCCSA

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C234 10U/6.3V_6 C707 10U/6.3V_6 C667 10U/6.3V_6 C711 10U/6.3V_6

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23
R3001 *100/F_4 +VCCSA
VCCSUSA_SENSE [28]

VCCSA_VID[0] C22
VCCSA_VID[1] C24
R480 10K/F_4
R479 10K/F_4
VCCSA_VID0 [28]
VCCSA_VID1 [28]

VCCIO_SEL A19

Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5VSUS

Q10 AON7410
Check
MAIND

R83 220_8

C164 0.1U/25V_4
C172 0.1U/25V_4
C186 0.1U/25V_4
C147 0.1U/25V_4

C229 *470P/50V_4

Q11 2N7002K
MAIN_ONG [2,31]

+1.5V_CPU +1.5V

VR_SVID_CLK VR_SVID_CLK [29]
+1.05V_VTT R74 130/F_4 VR_SVID_DATA [29]
+1.05V_VTT C1002 0.1U/25V_4 R71 75/F_4
H_CPU_SVIDALRT# R73 43_4 VR_SVID_ALERT# [29]

NB5

PROJECT : SW6C
Quanta Computer Inc.

Size	Document Number	Rev
	SNB 3/4 (POWER)	1A

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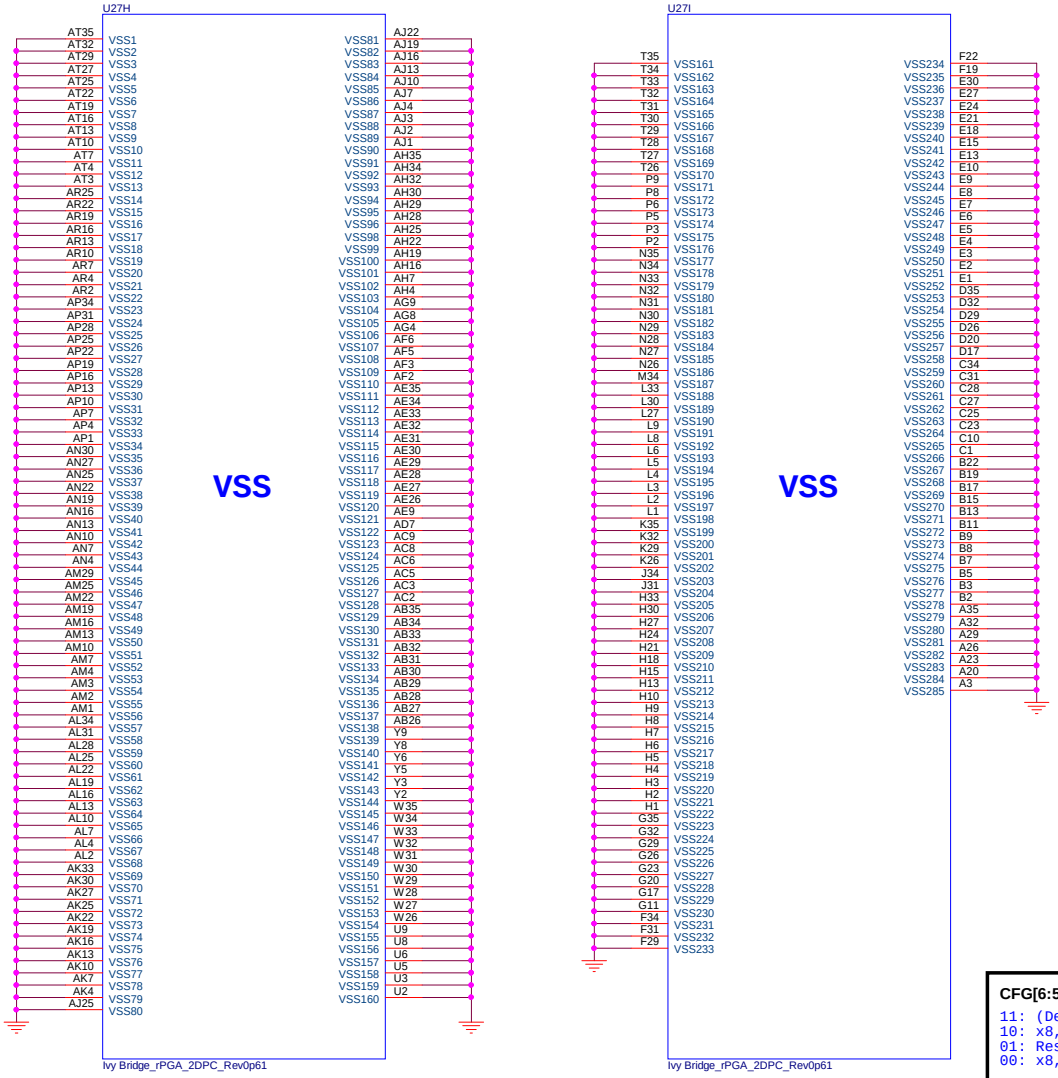
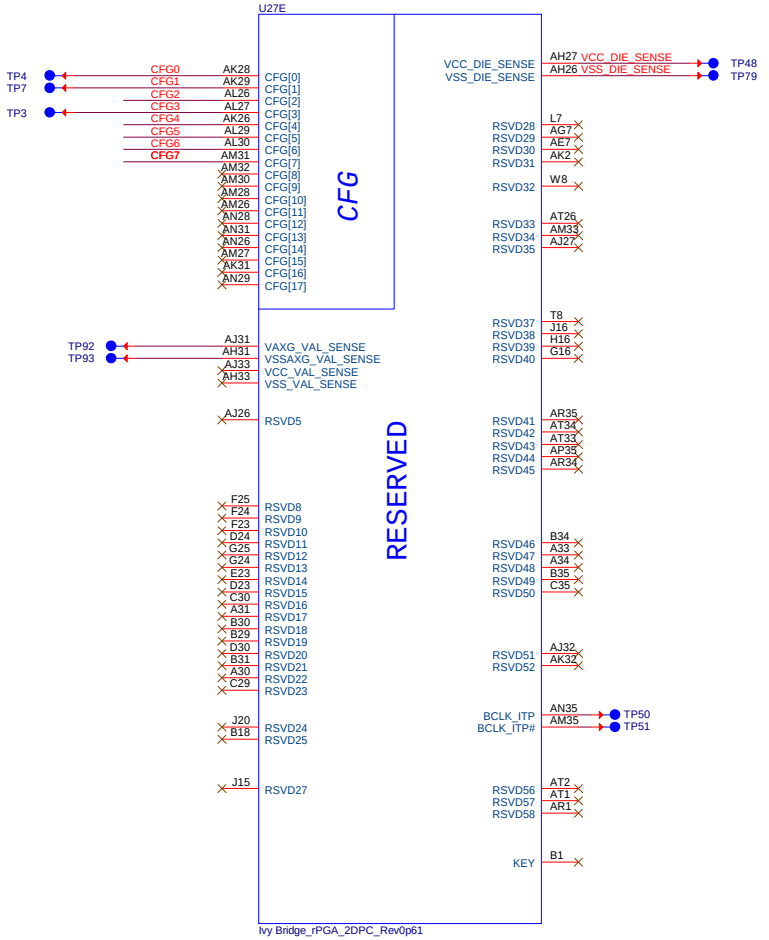
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)



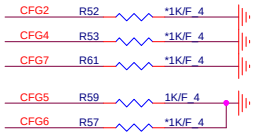
CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



need check GPU(JW3 used x8 lane)
eDP Enable

PROJECT : SW6C
Quanta Computer Inc.

Size	Document Number	Rev
NB5	SNB 4/4 (GND)	1A

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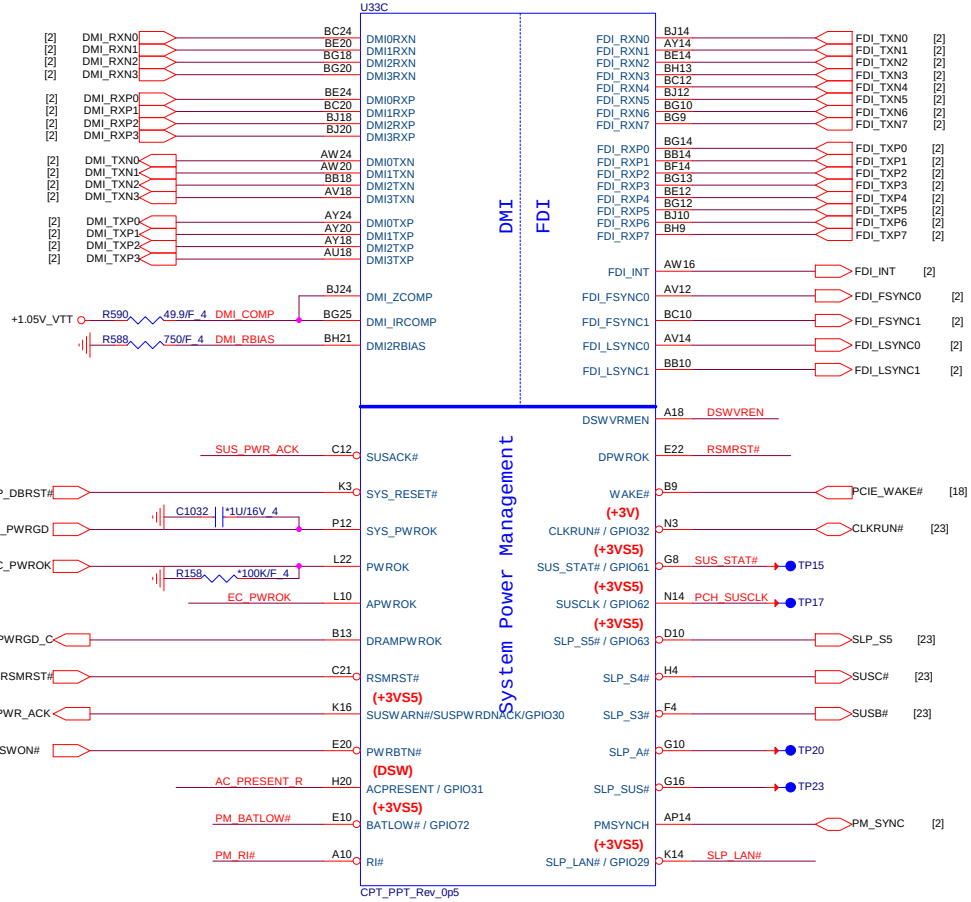
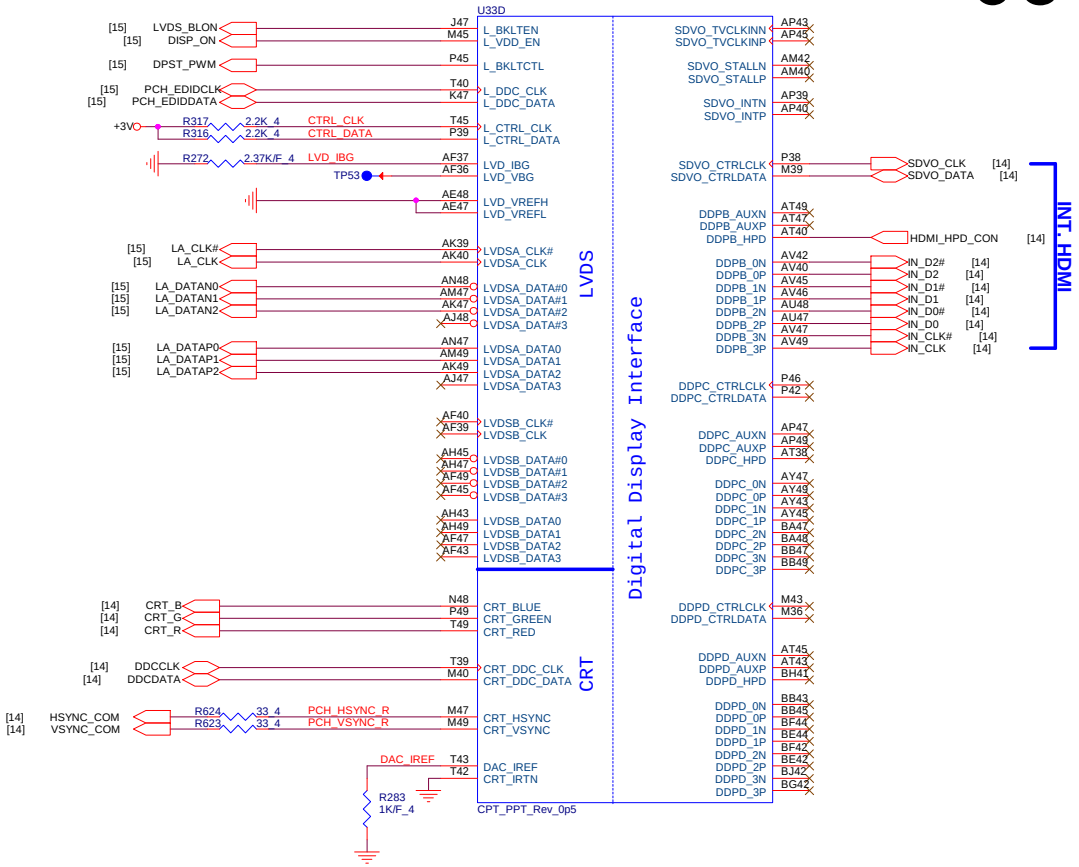
Panther Point(DMI,FDI,PM)

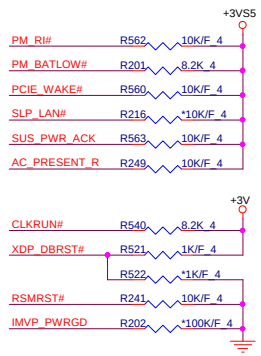


Panther Point(LVDS,DDI,CRT)



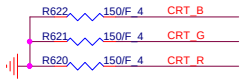
06

PCH Pull-high/low(CLG)



PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



System PWR_OK(CLG)

On Die DSW VR Enable
High = Enable (Default) Low = Disable

NB5

PROJECT : SW6C

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 1/6 (DMI/FDI/VIDEO)	1A

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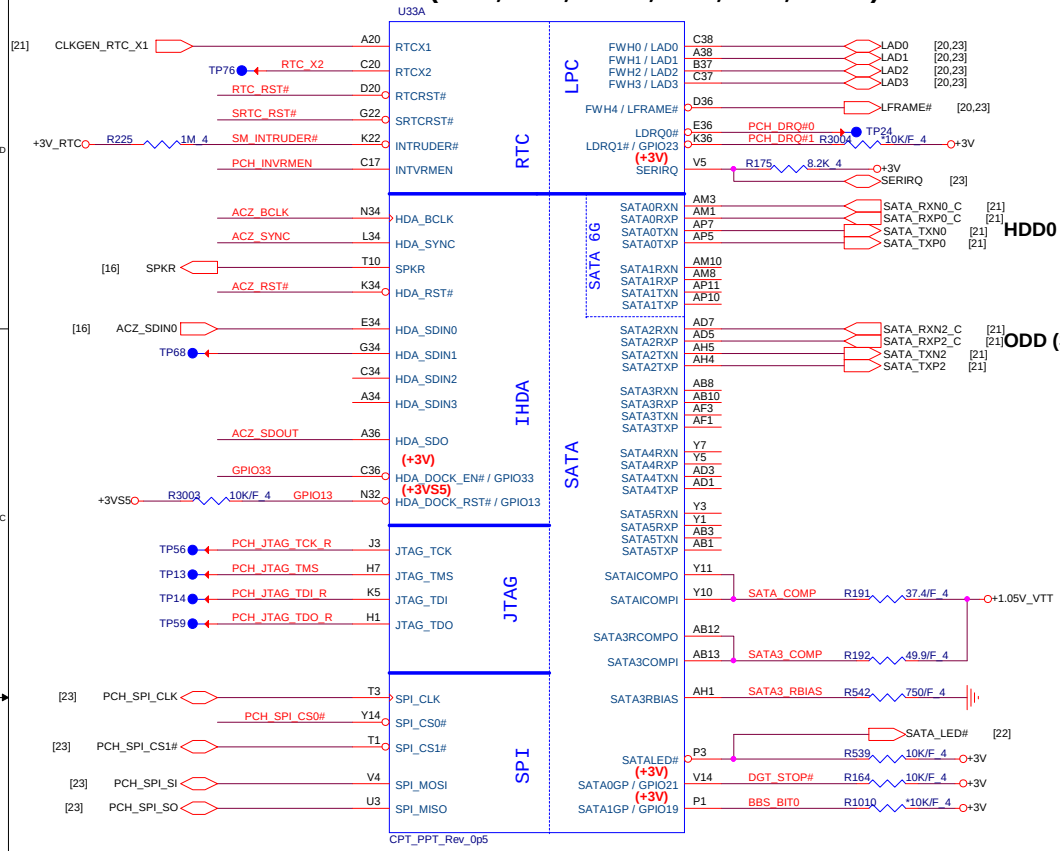
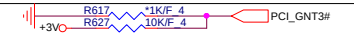
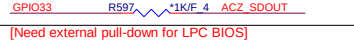
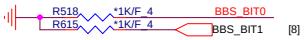
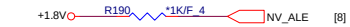
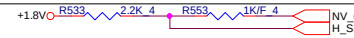
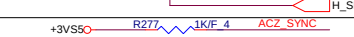
Panther Point(RTC,HDA,JTAG,SPI,LPC,SATA)



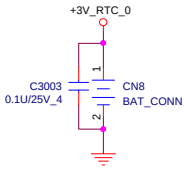
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI 1 / 0 / LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

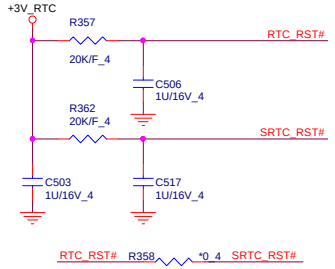
07

RTC Circuitry(RTC)

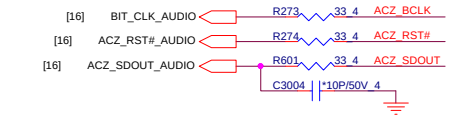


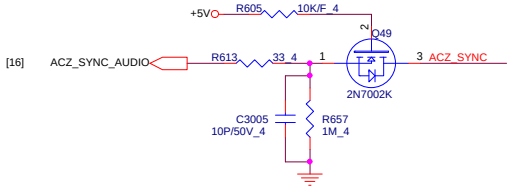
RTC Power trace width 20mils.

30mils



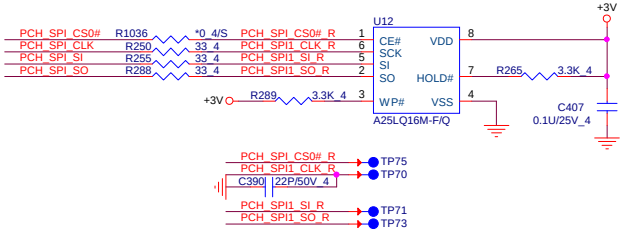
HDA Bus(CLG)





Vender	Size	P/N
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
GGD	2MB	AKE38GN0Q00 (GD25Q16BSIGR)

PCH SPI ROM(CLG)



Panther Point(PCI,USB)

Panther Point(PCI-E,SMBUS,CLK,CL)

08

PCI/USBOC# Pull-up(CLG)

RP3001 10P8R-8.2K
RP20 10K_10P8R_6
RP19 10K_10P8R_6

PLTRST#(CLG)

SMBus/Pull-up(CLG)

Q2001 Q2002 2N7002DW

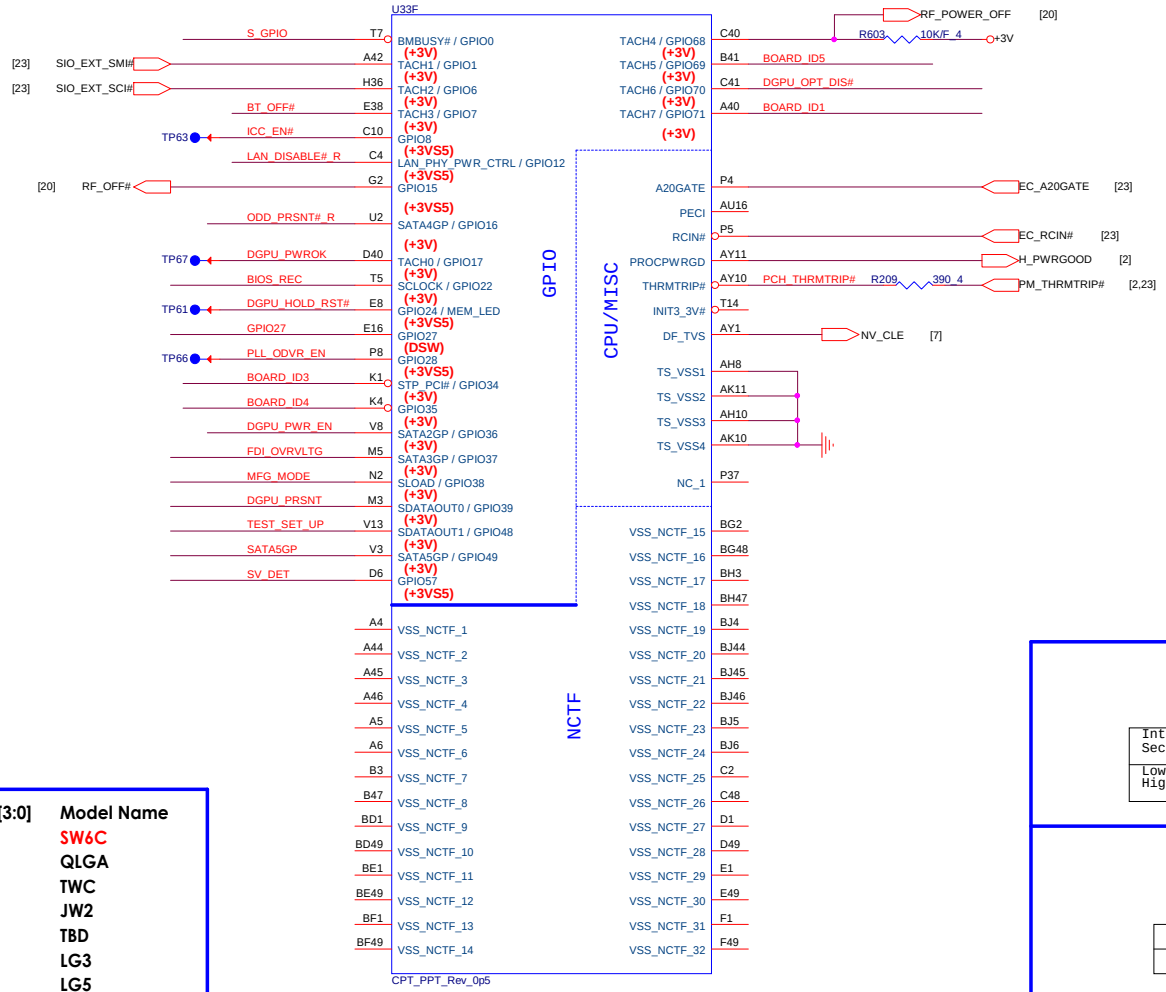
CLK_REQ/Strap Pin(CLG)

CLOCK TERMINATION for FCIM

SMBus/Pull-up(CLG)

PROJECT :	SW6C
	Quanta Computer Inc.
Size	NB5
Document Number	PCH 3/6 (PCIE/USB/CLK)
Rev	1A
Date: Tuesday, November 20, 2012	Sheet 8 of 34

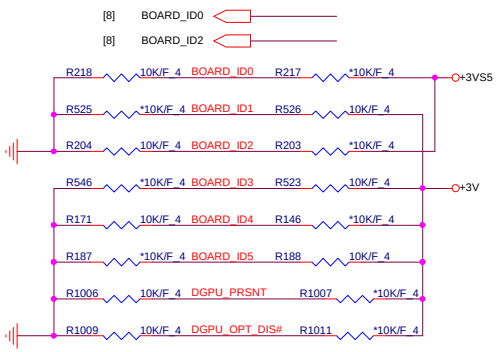
Panther Point(GPIO,VSS_NCTF,MISC)



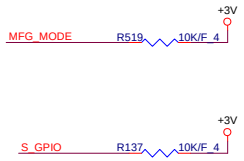
GPIO49	BOARD_ID[3:0]	Model Name
0	1010	SW6C
	0000	QLGA
	0001	TWC
	0010	JW2
	0011	TBD
	0100	LG3
	0101	LG5
	0110	LG2C
	0111	LG4C
	1000	TBD
	1001	JW6/JW7
	1010	JW3

Chief River BOARD ID SETTING

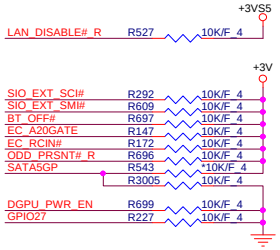
BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	Full Feature=0 Default Feature=1
BOARD_ID5	GPIO69	HM76=0,HM70=1
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

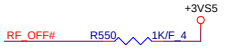


MFG-TEST



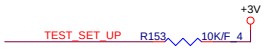
GPIO Pull-up/Pull-down(CLG)



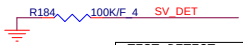


Intel ME Crypto Transport Layer Security (TLS) cipher suite	
Low = Disable (Default) High = Enable	

BIOS RECOVERY	High = Disable (Default) Low = Enable

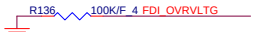


SV_SET_UP	
High = Strong (Default)	



TEST DETECT	
Low = Default	

20110926 Reserved only



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

NB5

PROJECT : SW6C

Quanta Computer Inc.

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A

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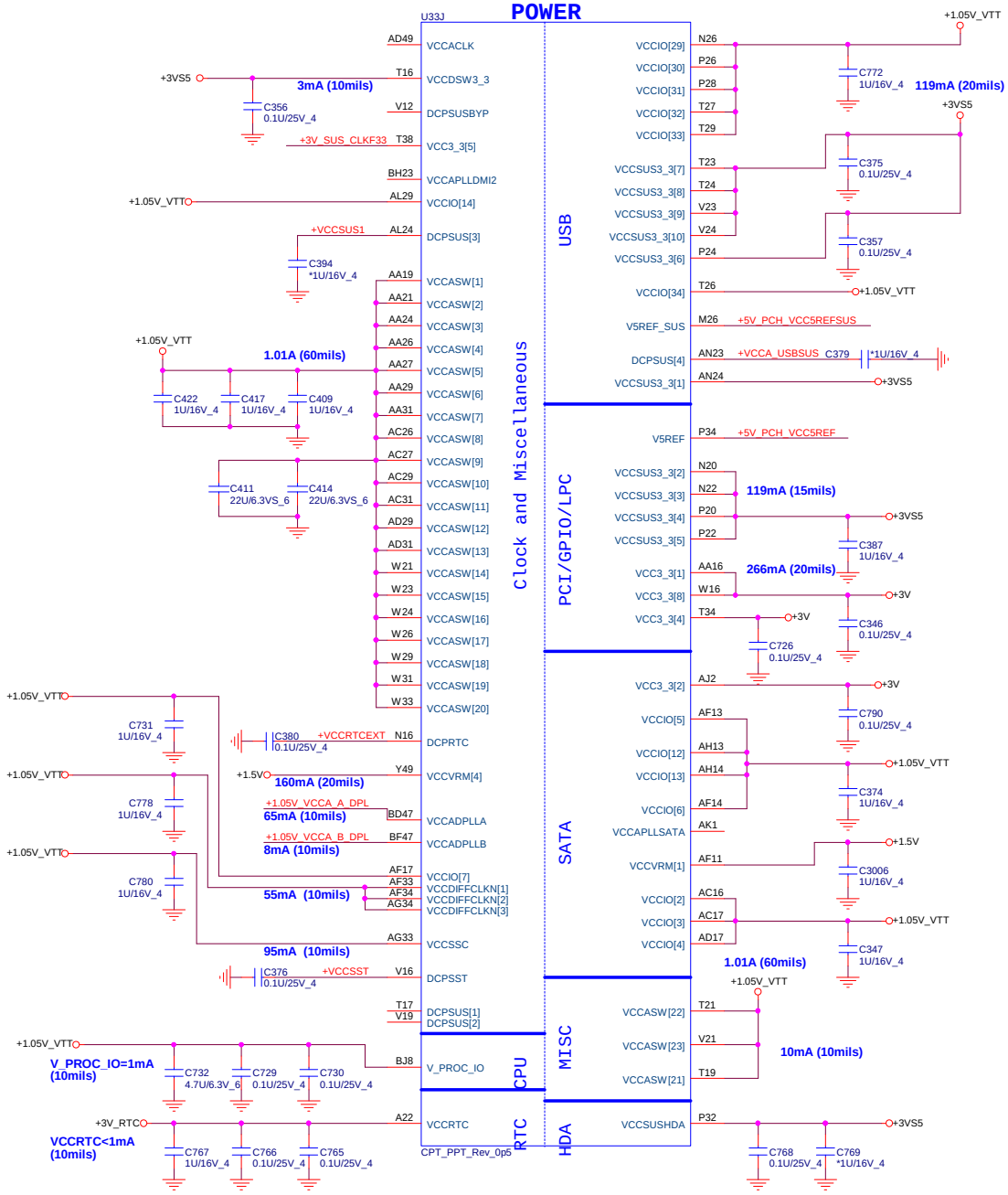
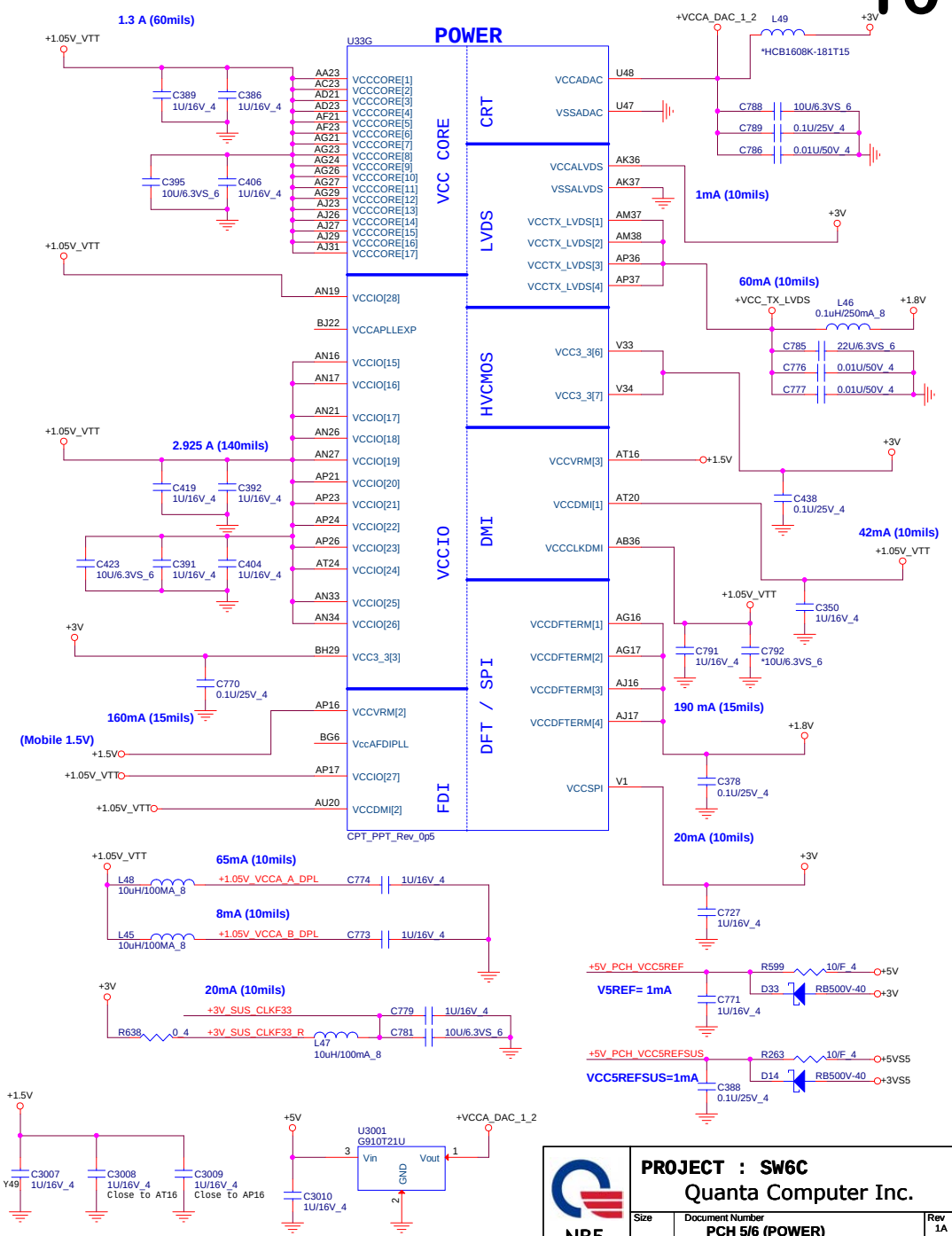
Panther Point(POWER)

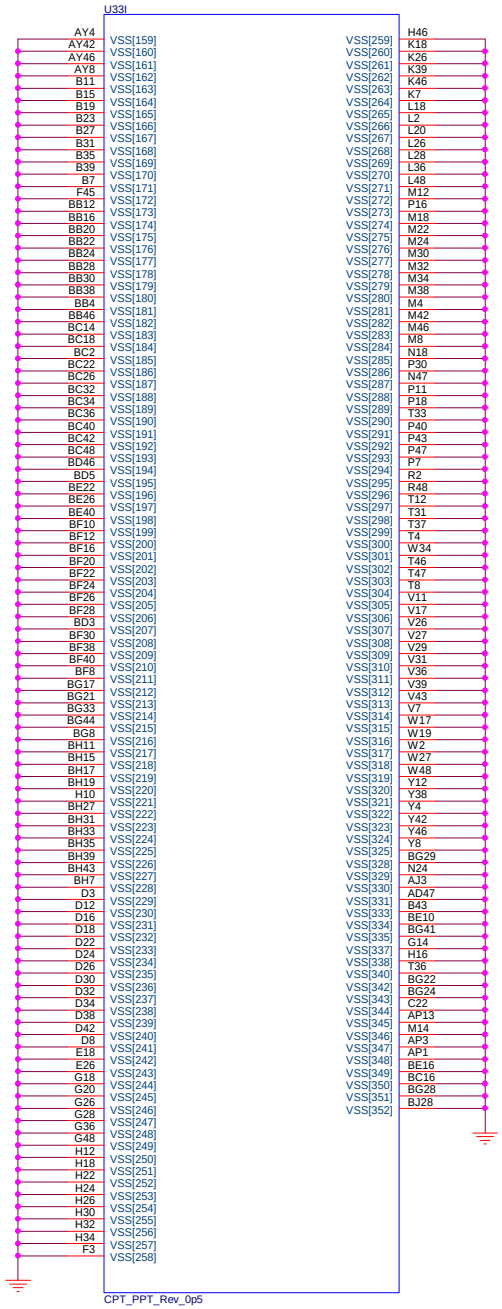
Panther Point(POWER)



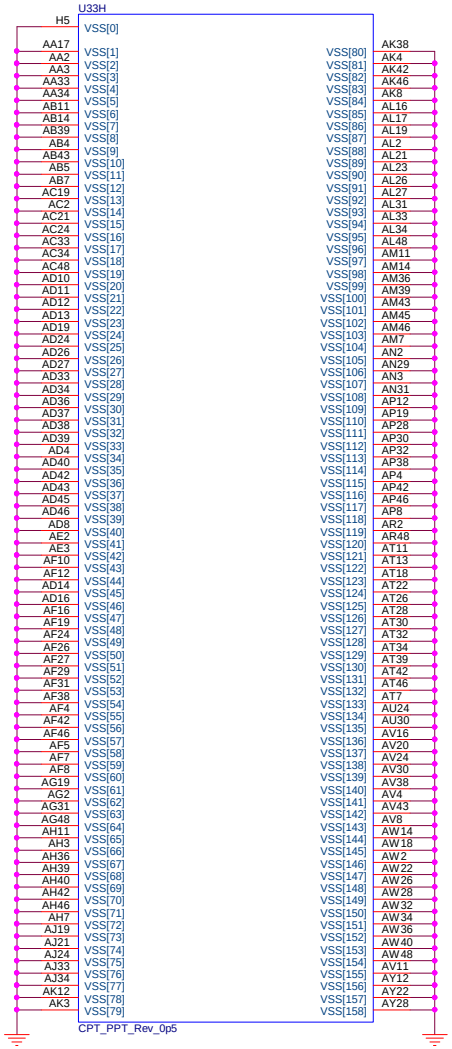


NB5	PROJECT : SW6C Quanta Computer Inc.	
Size	Document Number PCH 5/6 (POWER)	Rev 1A
Date: Tuesday, November 20, 2012	Sheet 10 of 34	

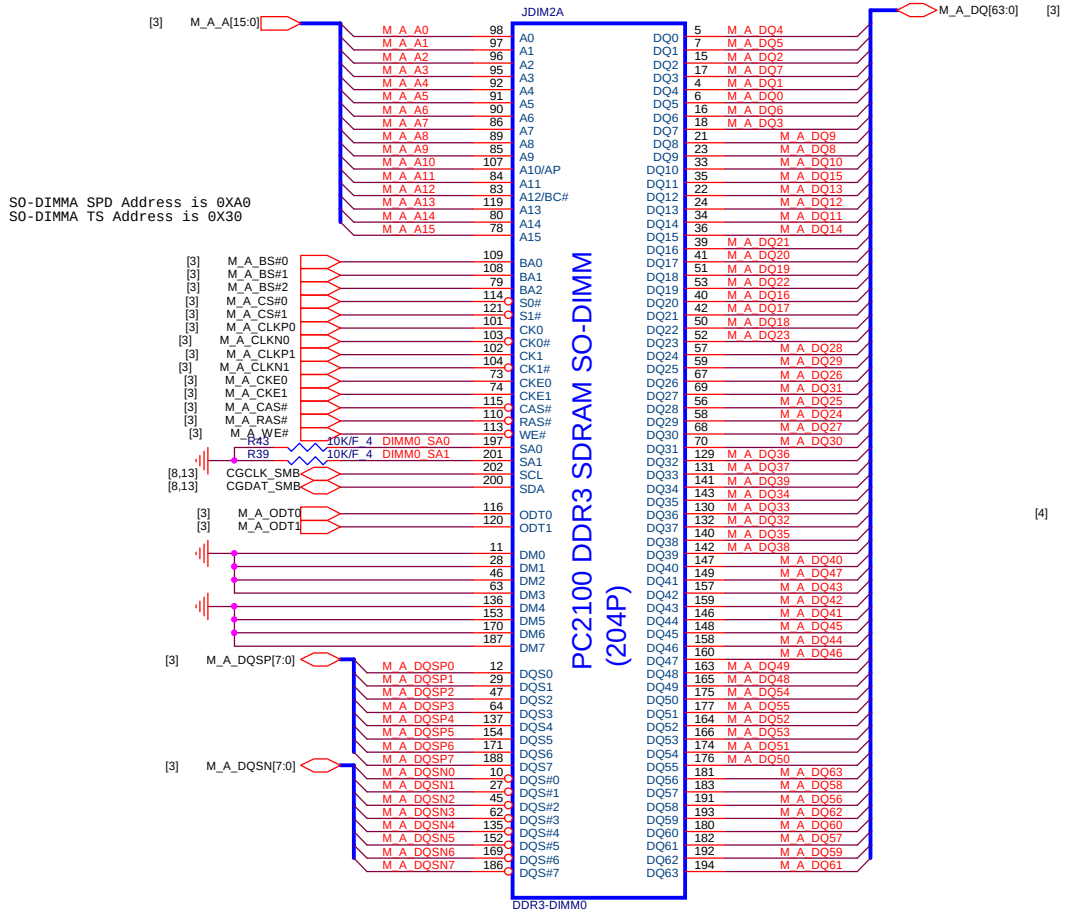
Panther Point(GND)

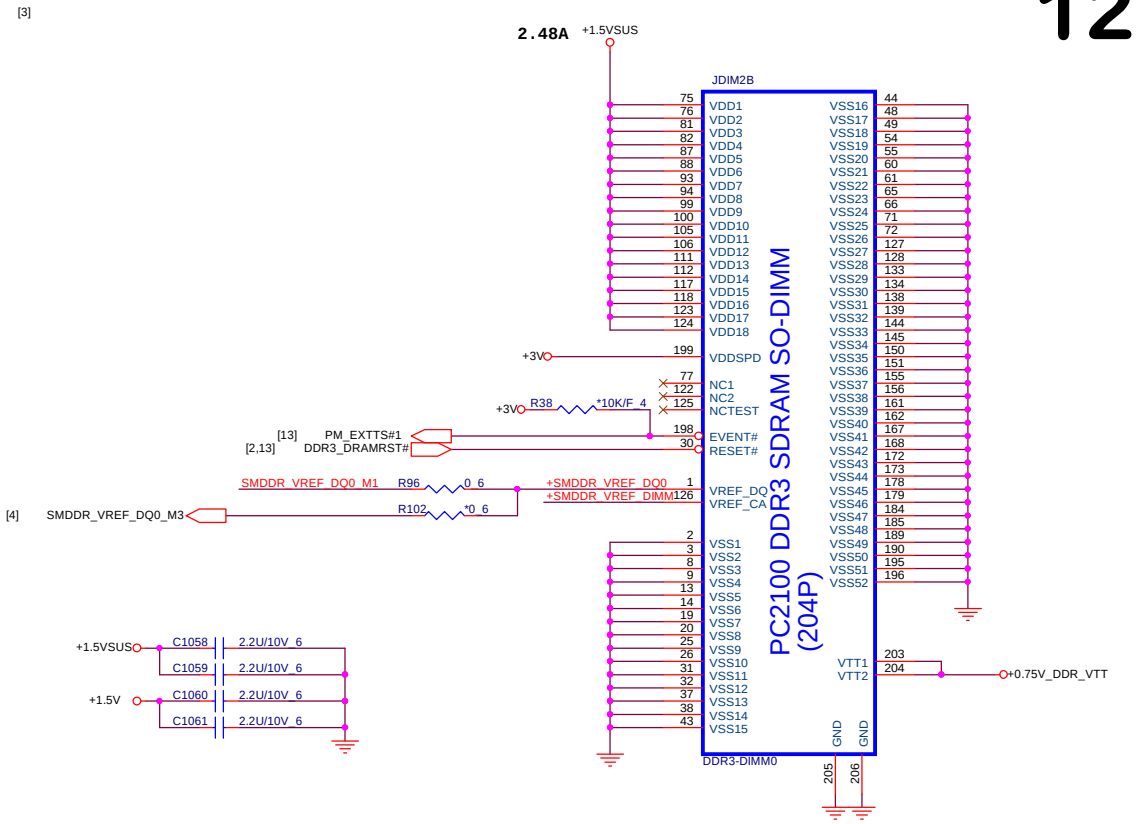


Panther Point(GND)

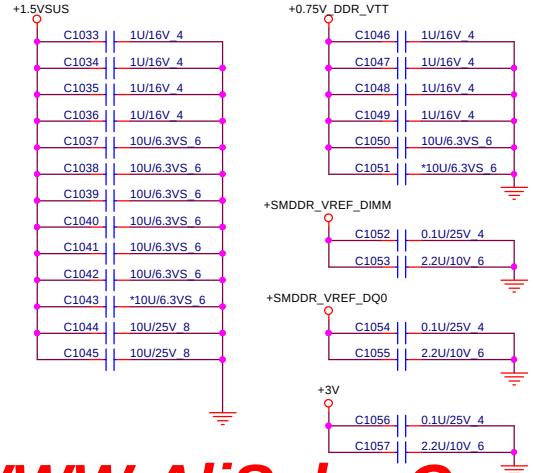


NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size: Document Number: PCH 6/6 (GND)	Rev: 1A
	Date: Tuesday, November 20, 2012	Sheet 11 of 34



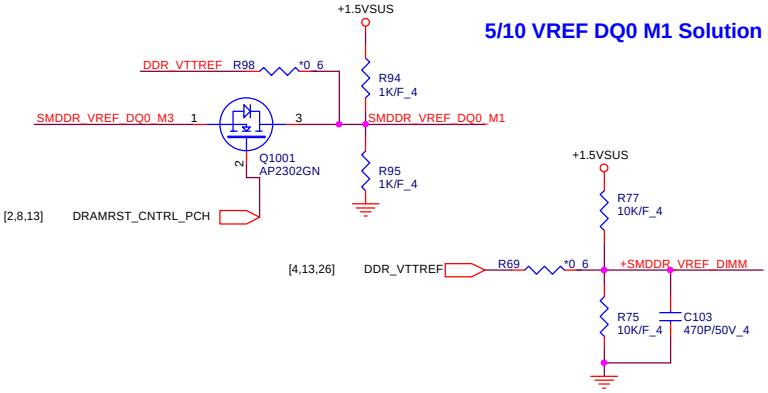


Place these Caps near So-Dimm0.



6/22:Document Number: 436996 **VREF DQ0 M2 Solution**
Intel remove the DDR3 verf M2 circuitry

5/10 VREF DQ0 M1 Solution



PROJECT : SW6C
Quanta Computer Inc.

Size	Document Number	Rev
NB5	DDR3 DIMM-0	1A

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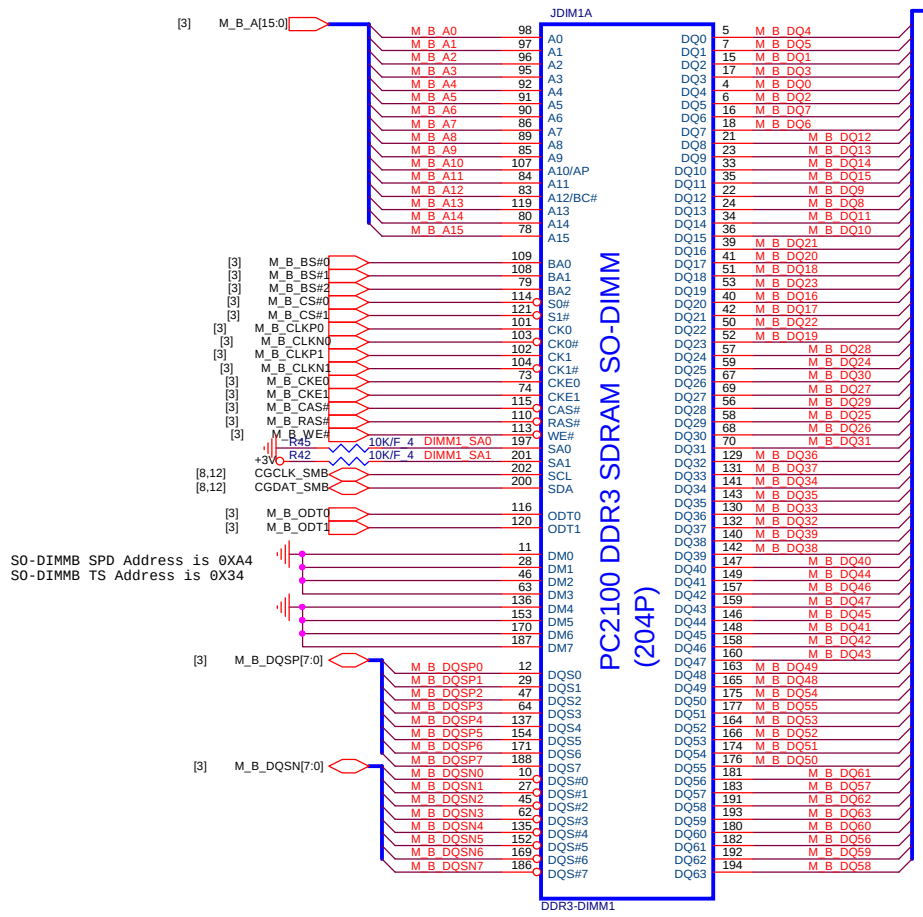
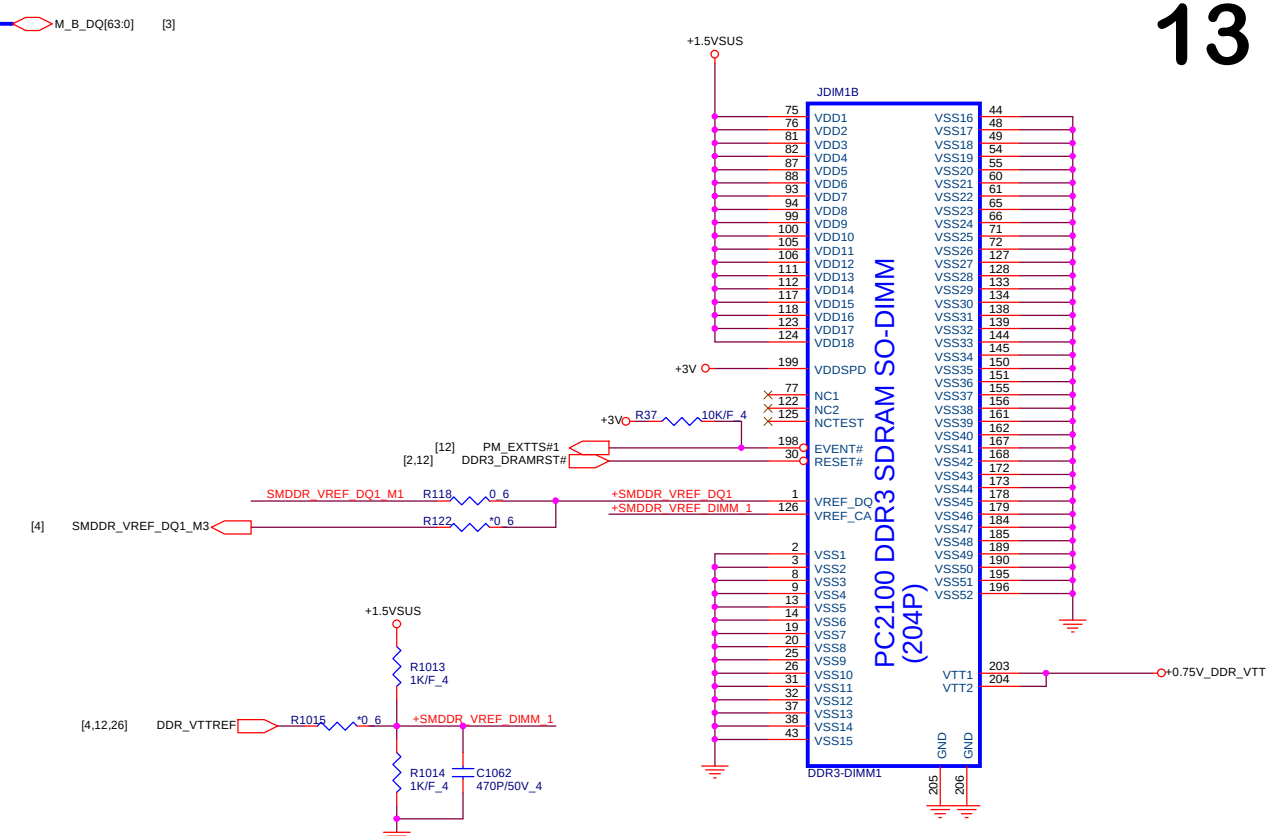
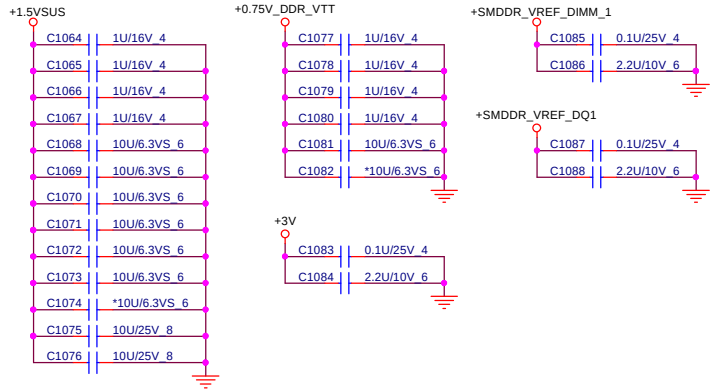
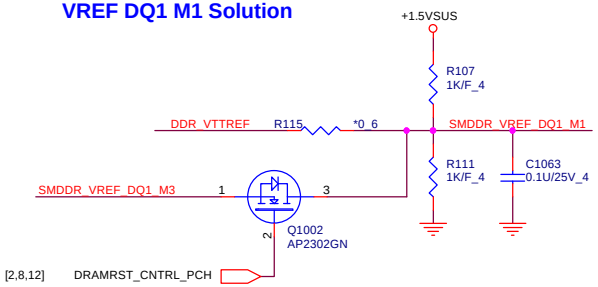






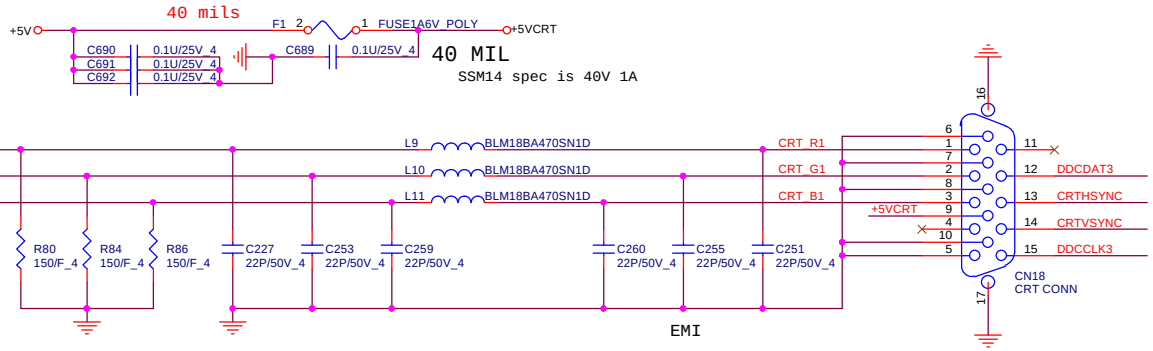
6/22:Document Number: 436996
Intel remove the DDR3 verf M2 circuitry

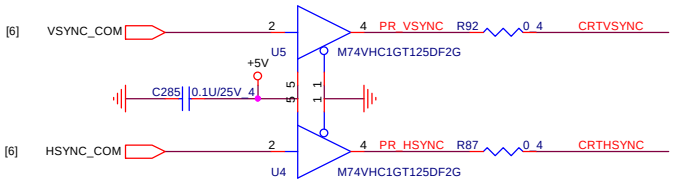
VREF DQ1 M2 Solution

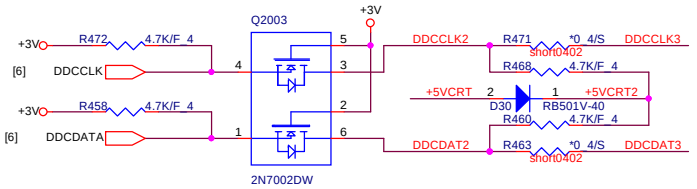


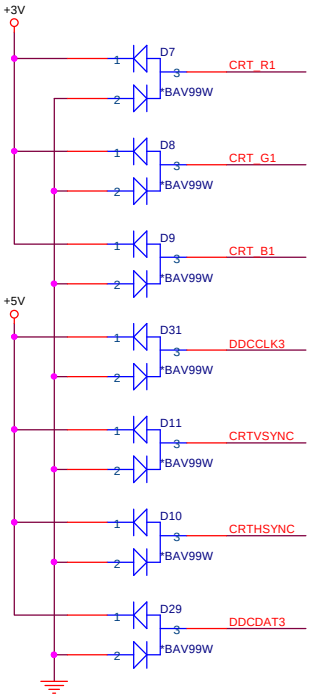
NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number DDR3 DIMM-1	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 13 of 34

CRT PORT

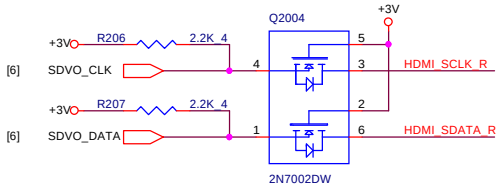


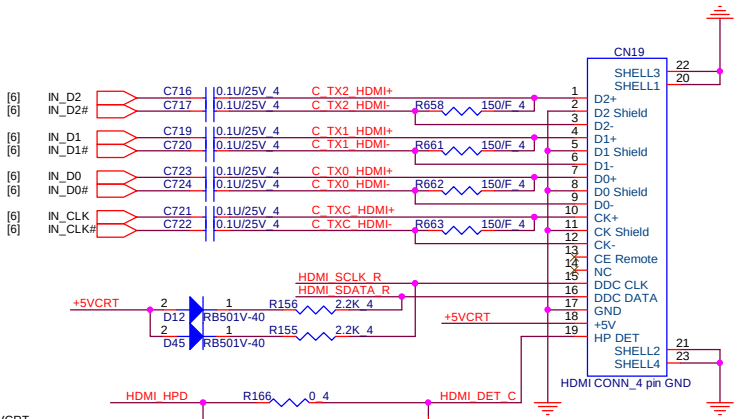


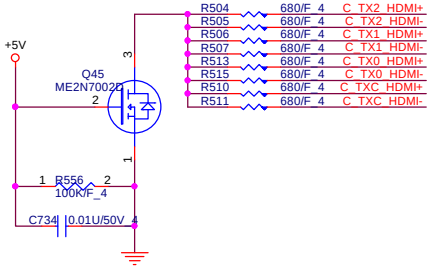


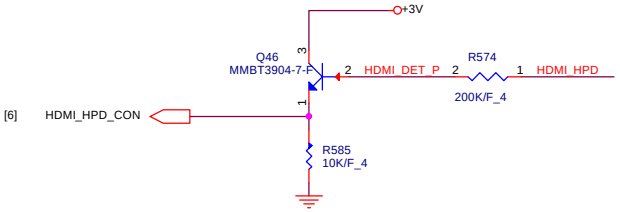


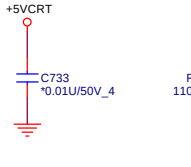
HDMI PORT



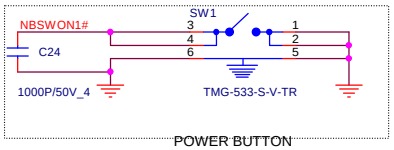




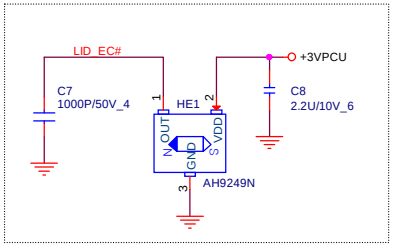


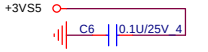


NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number CRT/HDMI Conn	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 14 of 34



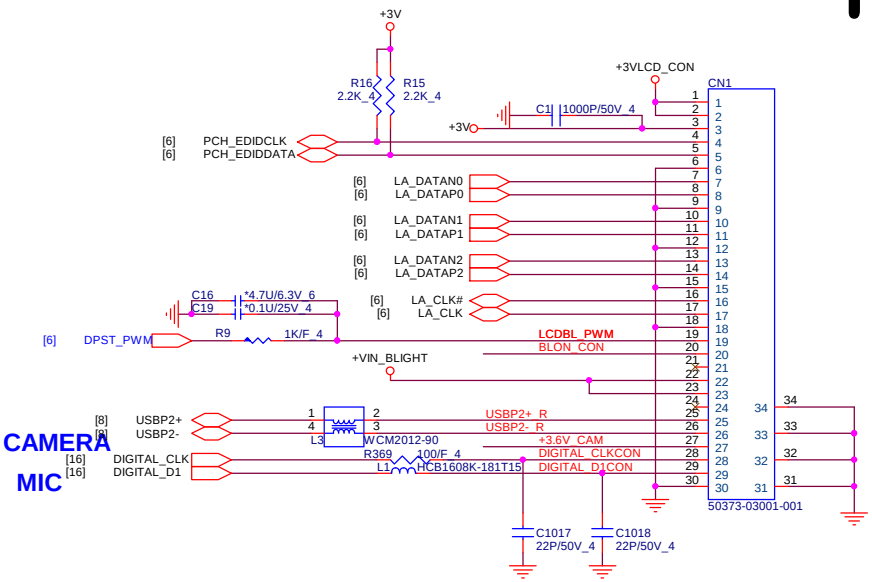
POWER BUTTON





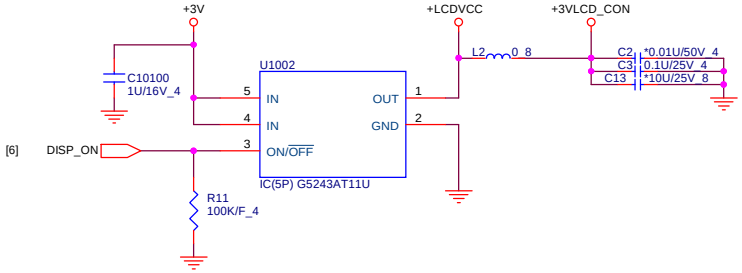
1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

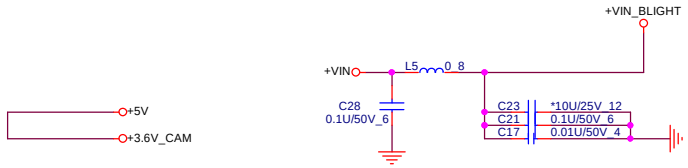
[23] NBSWON1#

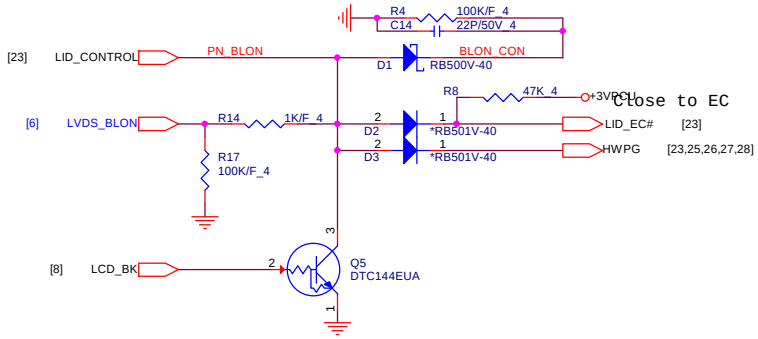


CAMERA

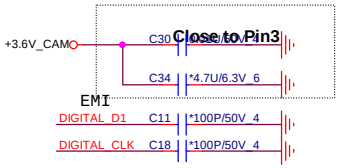
MIC





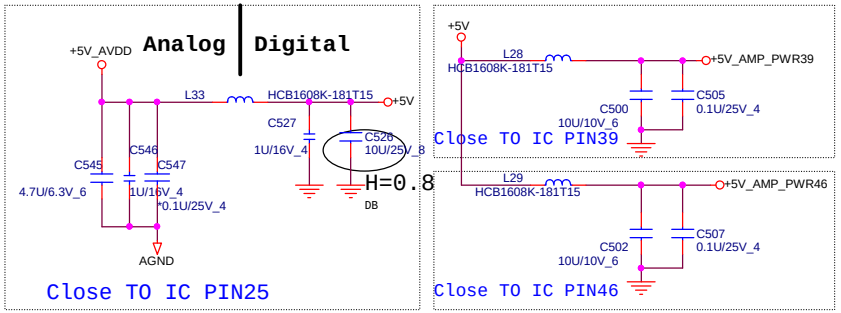


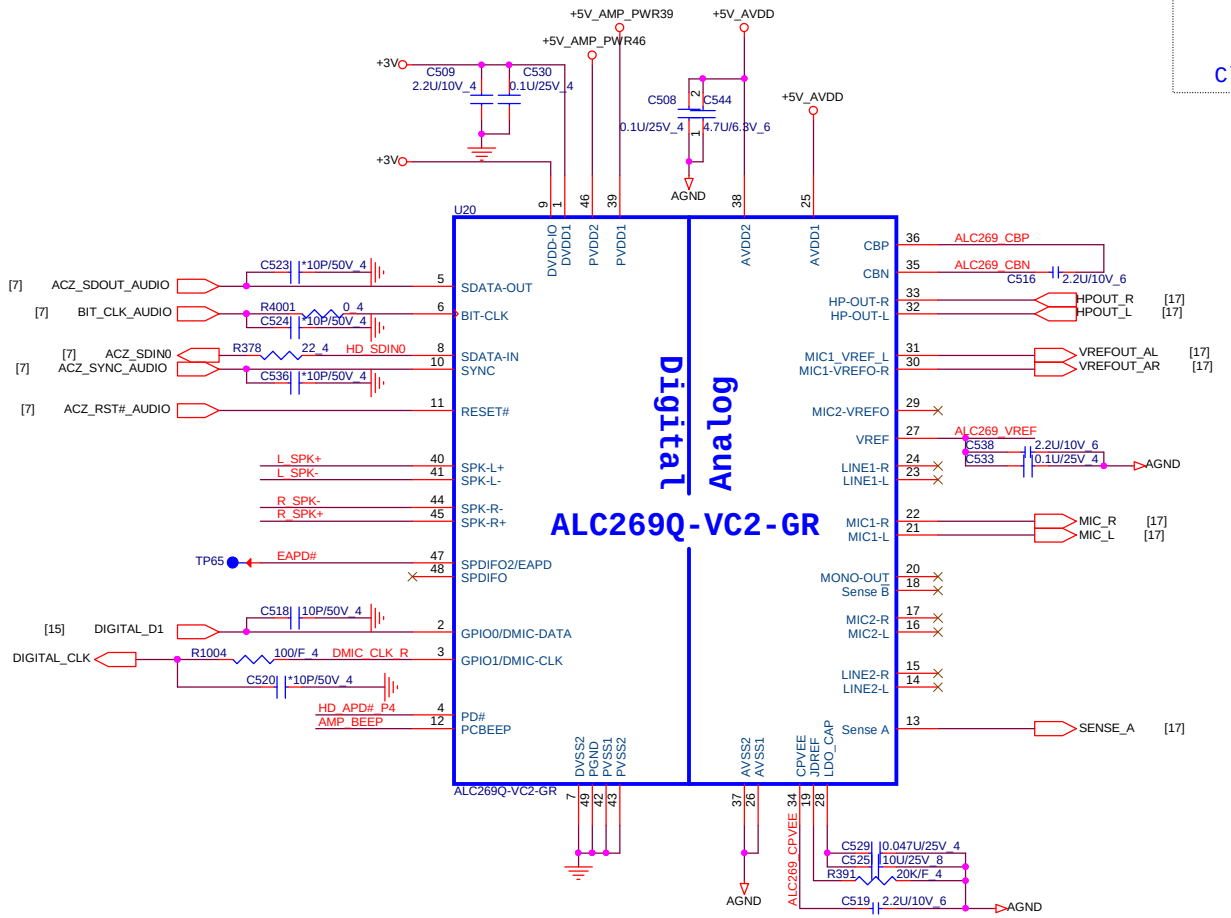
Close to EC



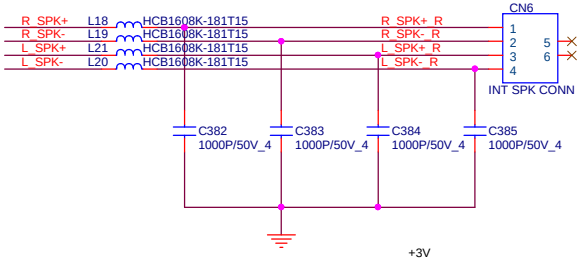
Close to Pin3

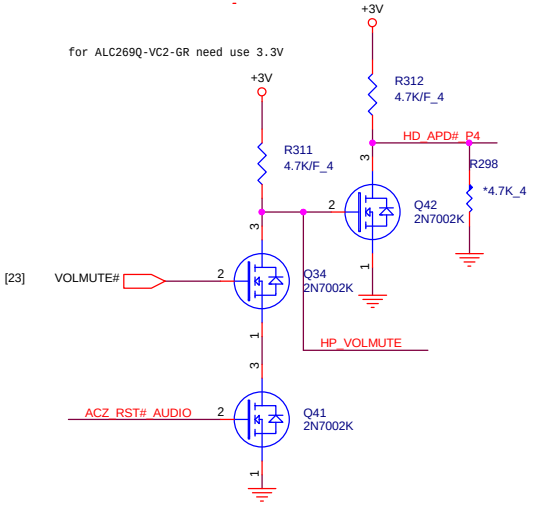
NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number LCD CONN	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 15 of 34

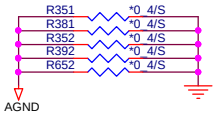


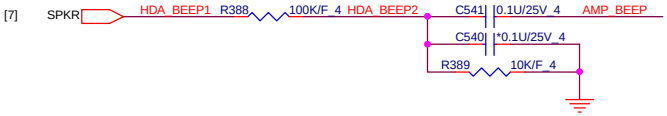


INT. SPEAKER



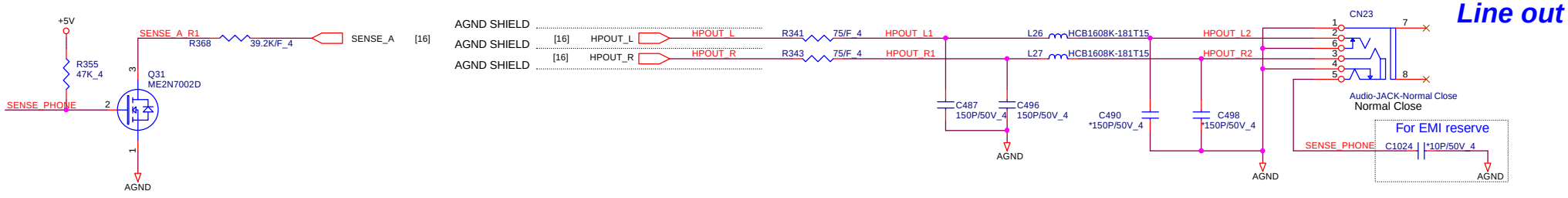




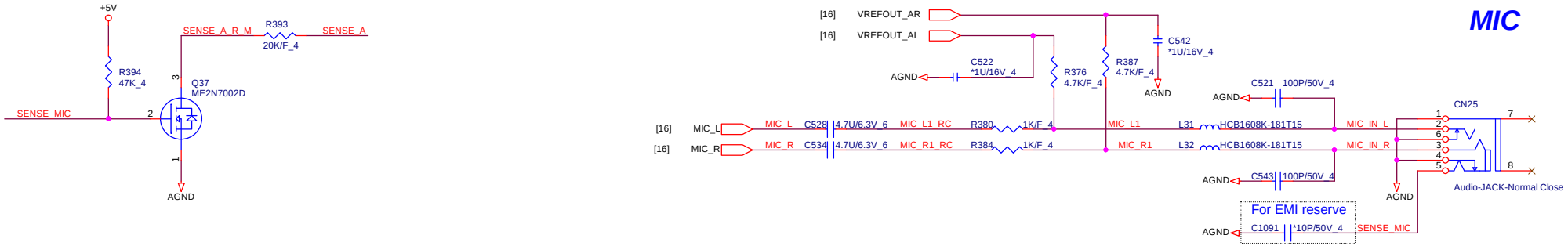


NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number ALC269Q-VC-GR	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 16 of 34

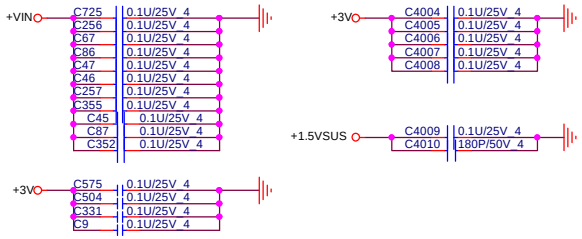
Line out



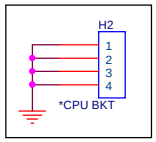
MIC



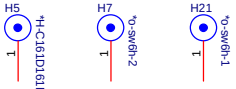
EMI

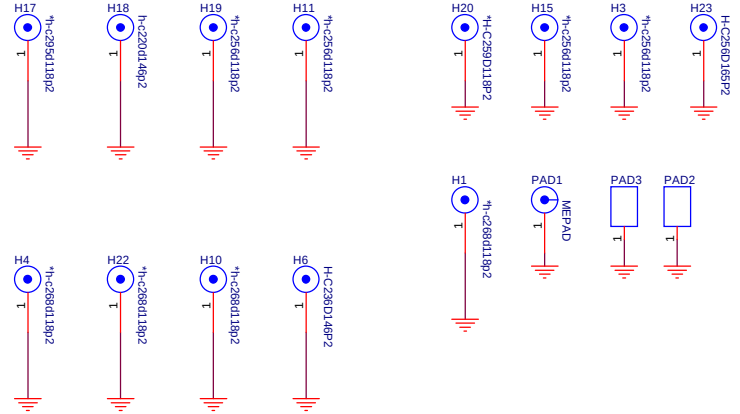


CPU

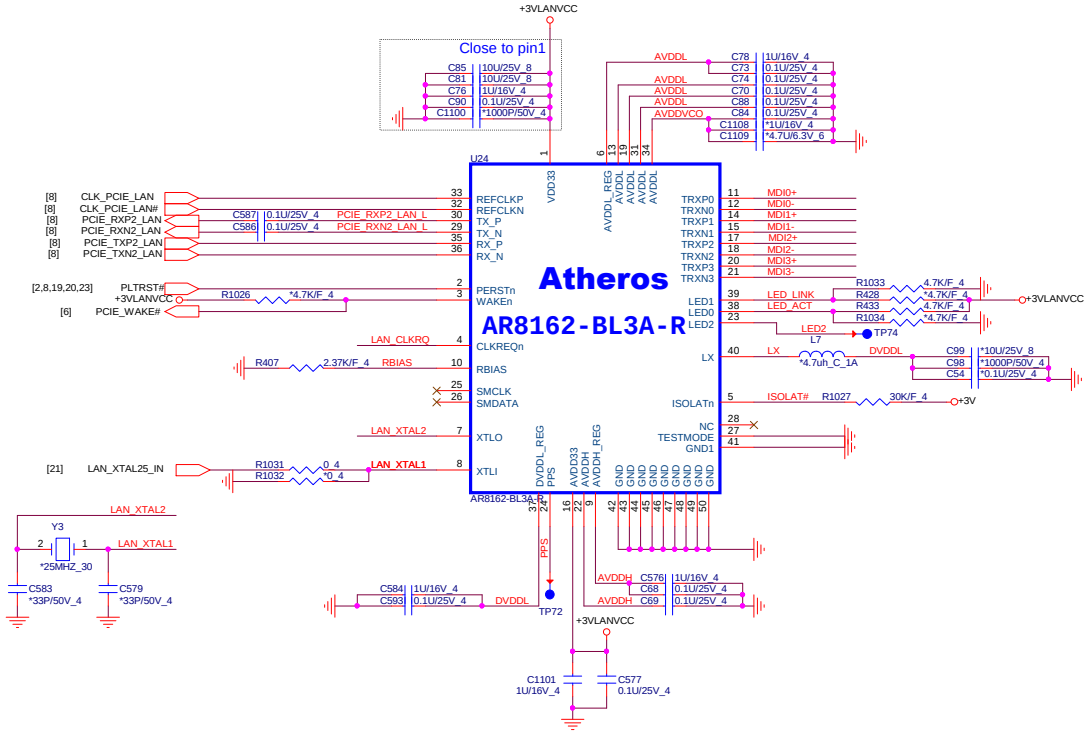


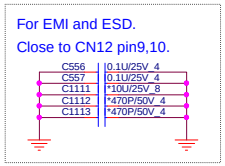
NPTH

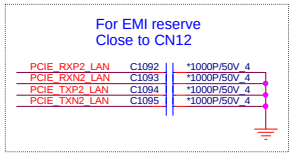


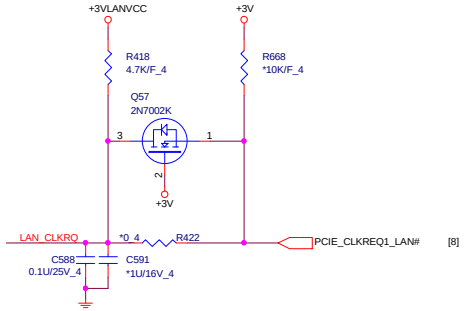


NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number AUDIO JACK/HOLES/EMI	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 17 of 34

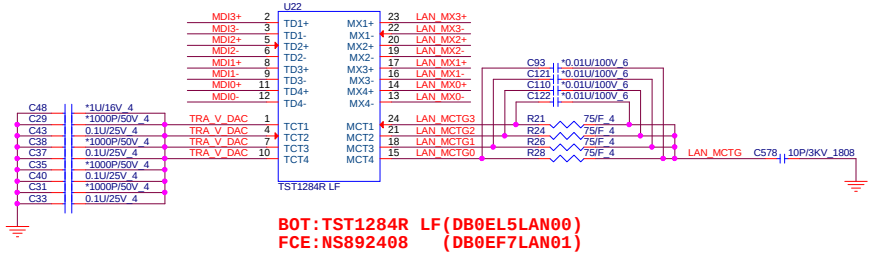








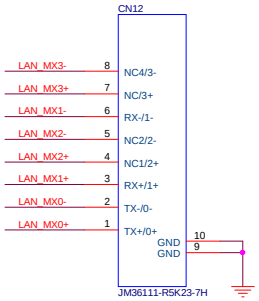
Transformer for 10/100/1000



BOT:TST1284R LF(DB0EL5LAN00)
FCE:NS892408 (DB0EF7LAN01)

Lan Connector

RJ45



PROJECT : SW6C
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	LAN AR8161	1A

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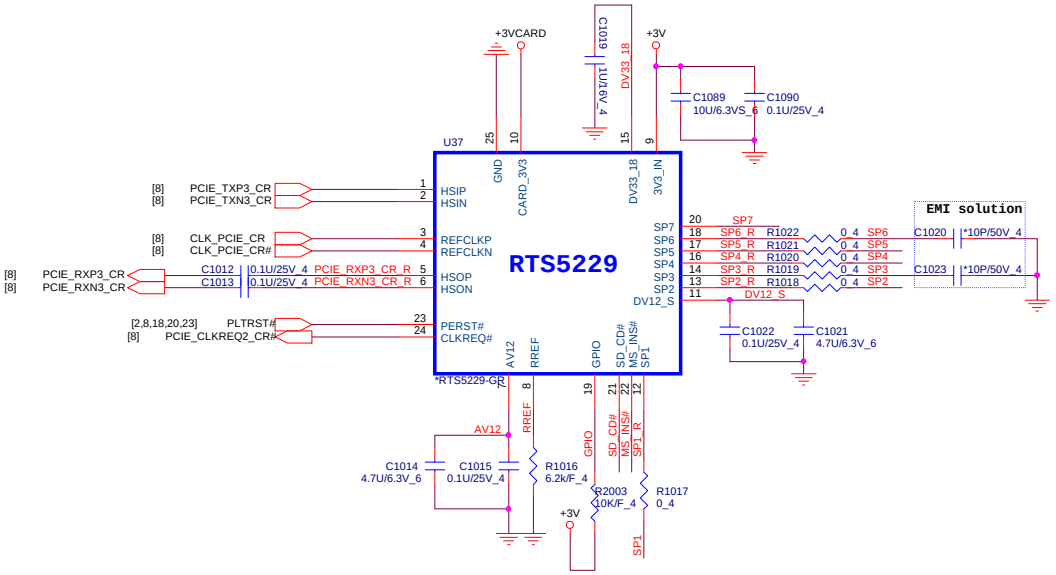
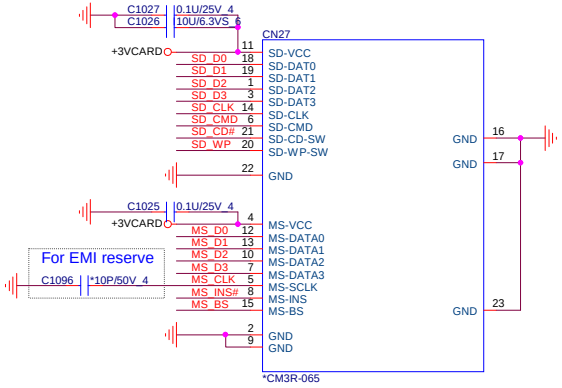
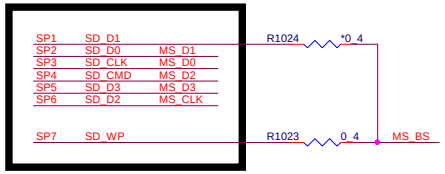
3 IN1 CARD READER SD/MMC/MS







Share Pin

Note:

1. **R1017~R1022,C1020,C1023 close to U37 pin**
2. **C1014, C1015 close to U37 pin7**
3. **C1021, C1022 close to U37 pin11**
4. **C1089, C1090 close to U37 pin9**
5. **C1019 close to U37 pin15**
6. **C1026, C1027 close to CN27 pin11**
7. **C1025 close to CN27 pin4**

NB5	**PROJECT : SW6C** Quanta Computer Inc.	
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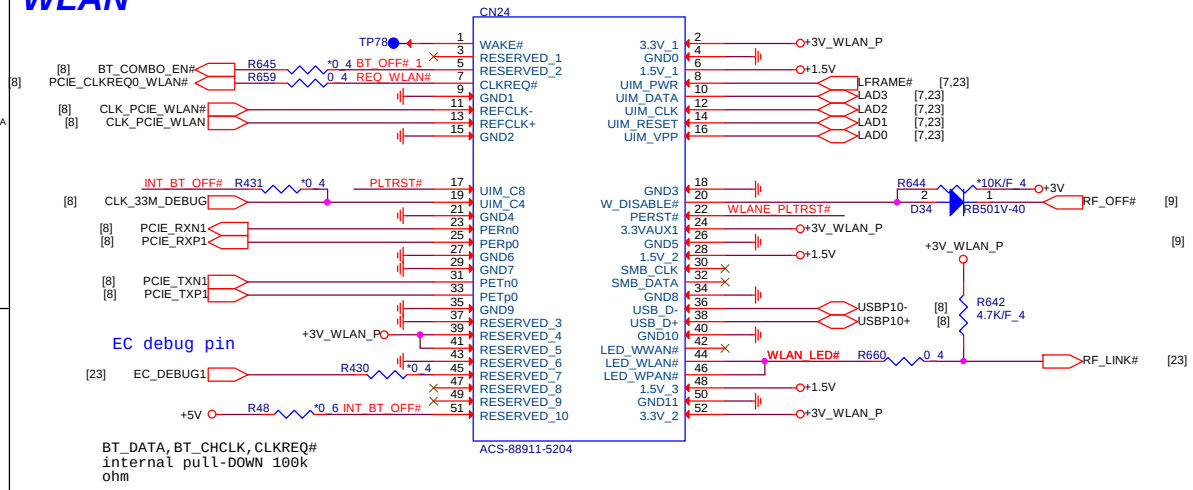
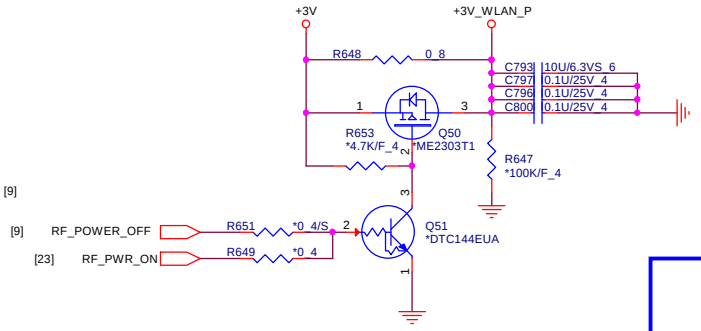
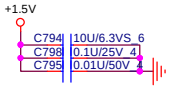
Mini PCI-E Card 1
WLAN

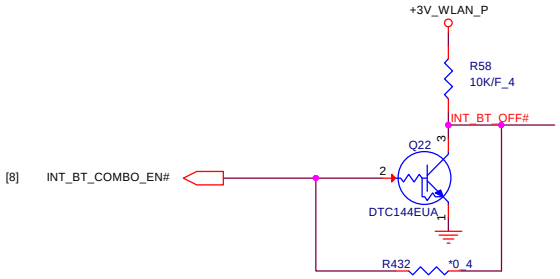


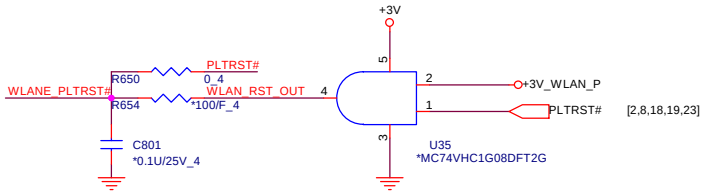
EC debug pin

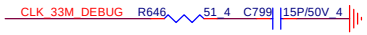
BT_DATA, BT_CHCLK, CLKREQ#
internal pull-DOWN 100k
ohm





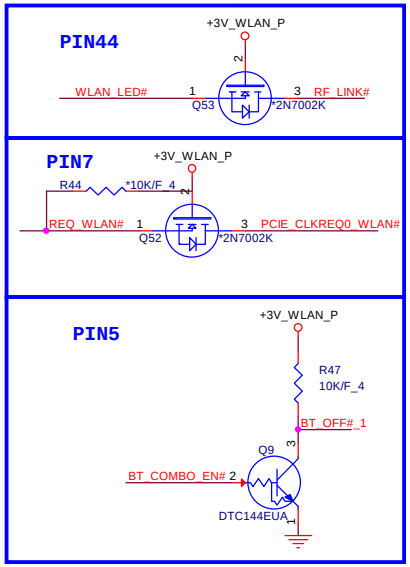






LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

Avoid leakage issue



NB5

PROJECT : SW6C
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCIE CONN X2	1A

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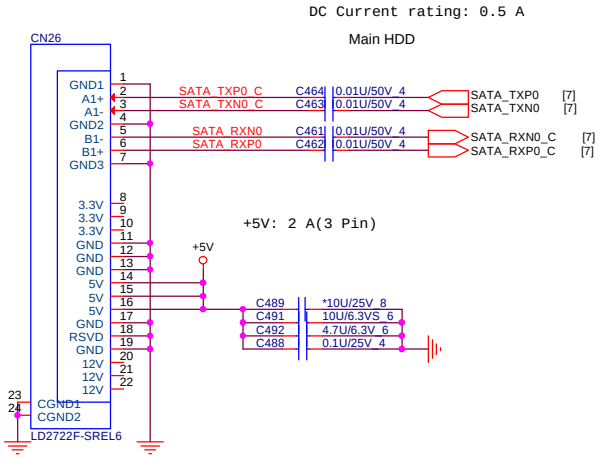
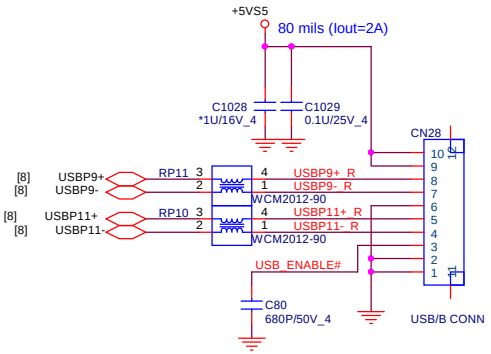
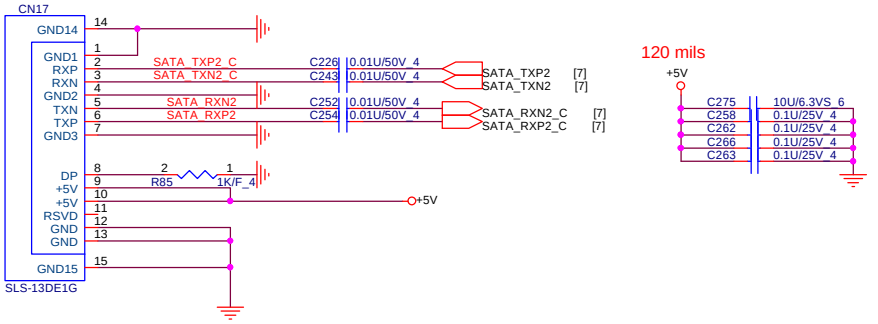
SATA HDD



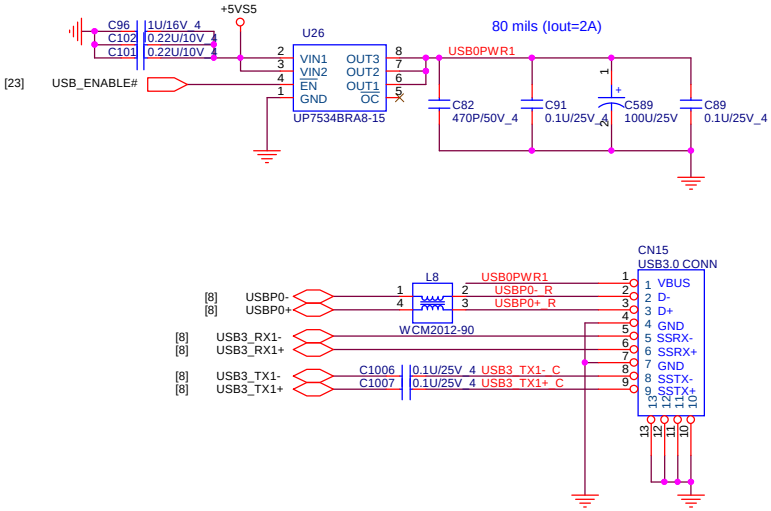
USB2.0X2



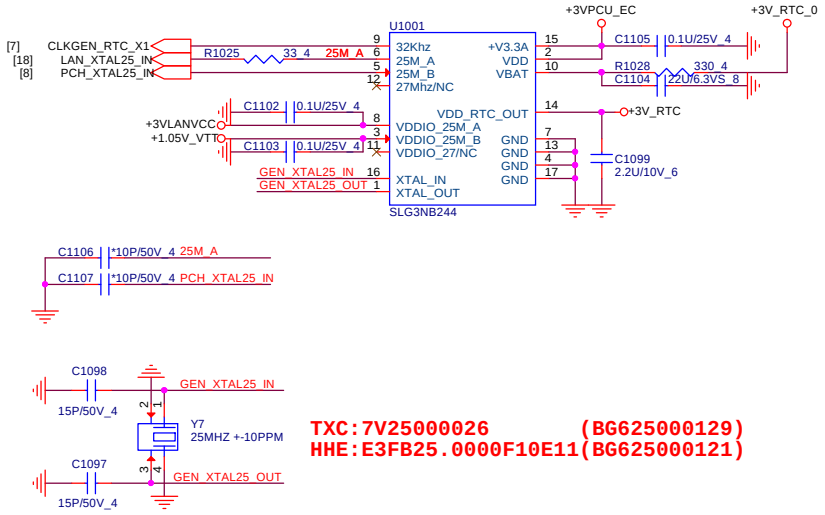
SATA ODD



USB3.0

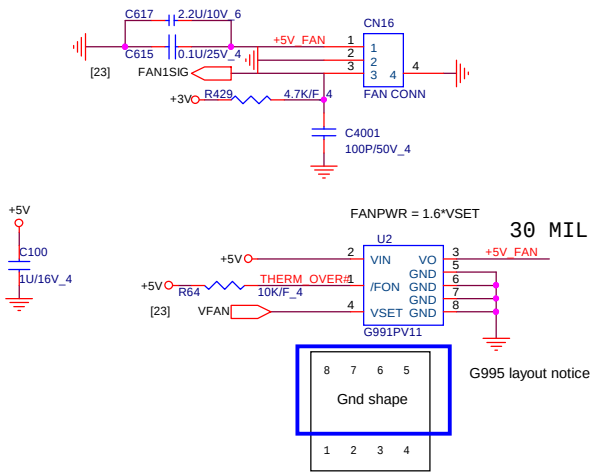


Green CLK

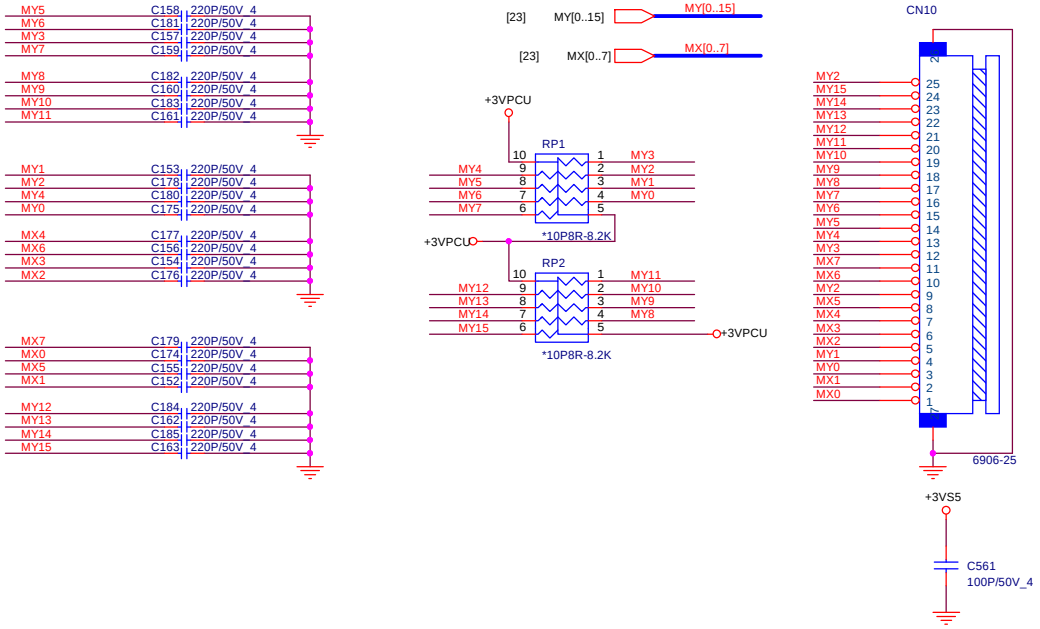


NB5	PROJECT : SW6C Quanta Computer Inc.	
	Size Document Number ODD/HDD/NEW CARD/TP	Rev 1A
	Date: Tuesday, November 20, 2012	Sheet 21 of 34

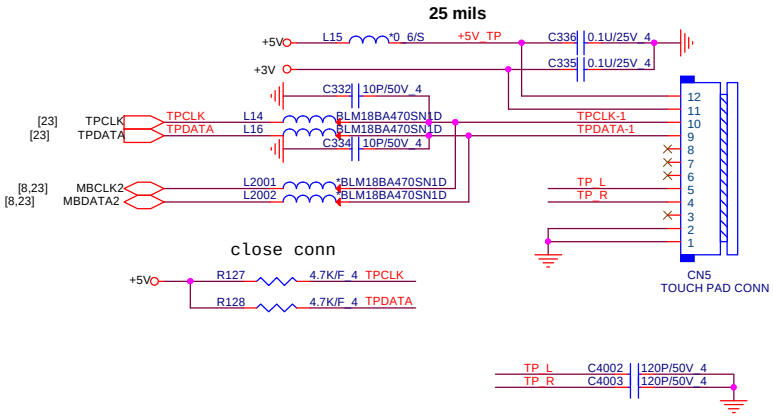
CPU FAN



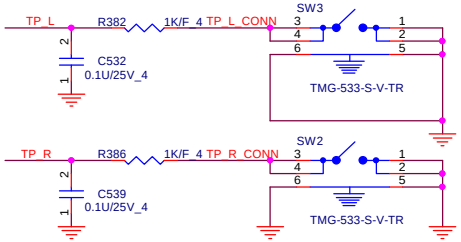
KEYBOARD



TOUCH PAD

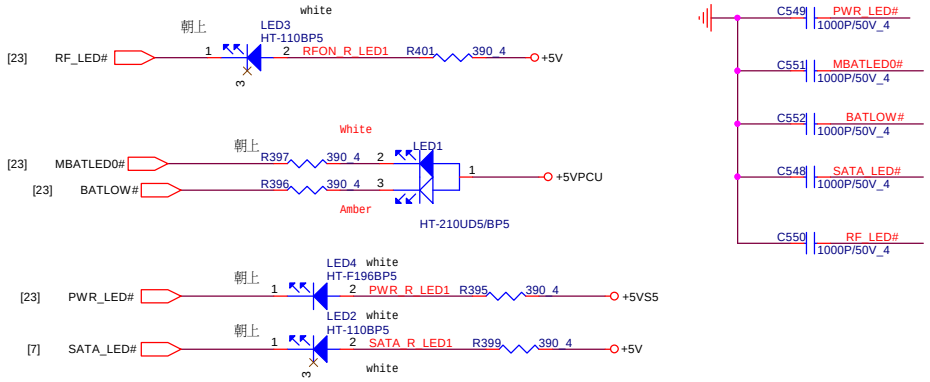


TOUCH PAD L/R



LED

Close to U21 For EMI



NB5

PROJECT : SW6C

Quanta Computer Inc.

Size	Document Number	Rev
	KB/PWR/FAN/CAM/MIC	1A

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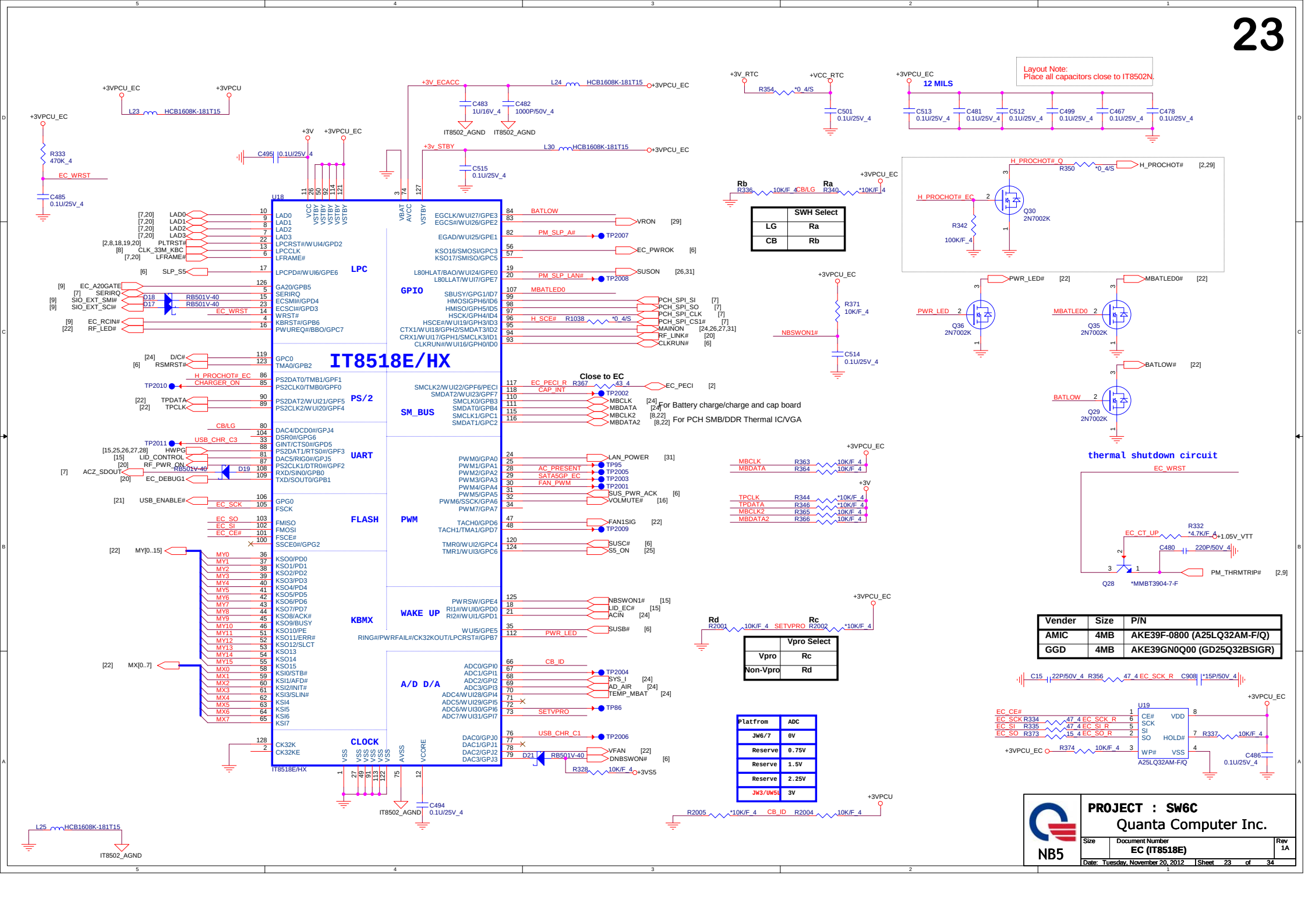
IT8518E/HX
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Close to EC
For Battery charge/charge and cap board
For PCH SMB/DDR Thermal IC/VGA
Layout Note:
Place all capacitors close to IT8502N.
12 MILS
SWH Select
LG Ra
CB Rb
Vpro Select
Vpro Rc
Non-Vpro Rd
Platfrom ADC
JW6/7 0V
Reserve 0.75V
Reserve 1.5V
Reserve 2.25V
JW3/UW5U 3V
thermal shutdown circuit
Vender Size P/N
AMIC 4MB AKE39F-0800 (A25LQ32AM-F/Q)
GGD 4MB AKE39GN0Q00 (GD25Q32BSIGR)
PROJECT : SW6C
Quanta Computer Inc.
NB5
EC (IT8518E)
Date: Tuesday, November 20, 2012
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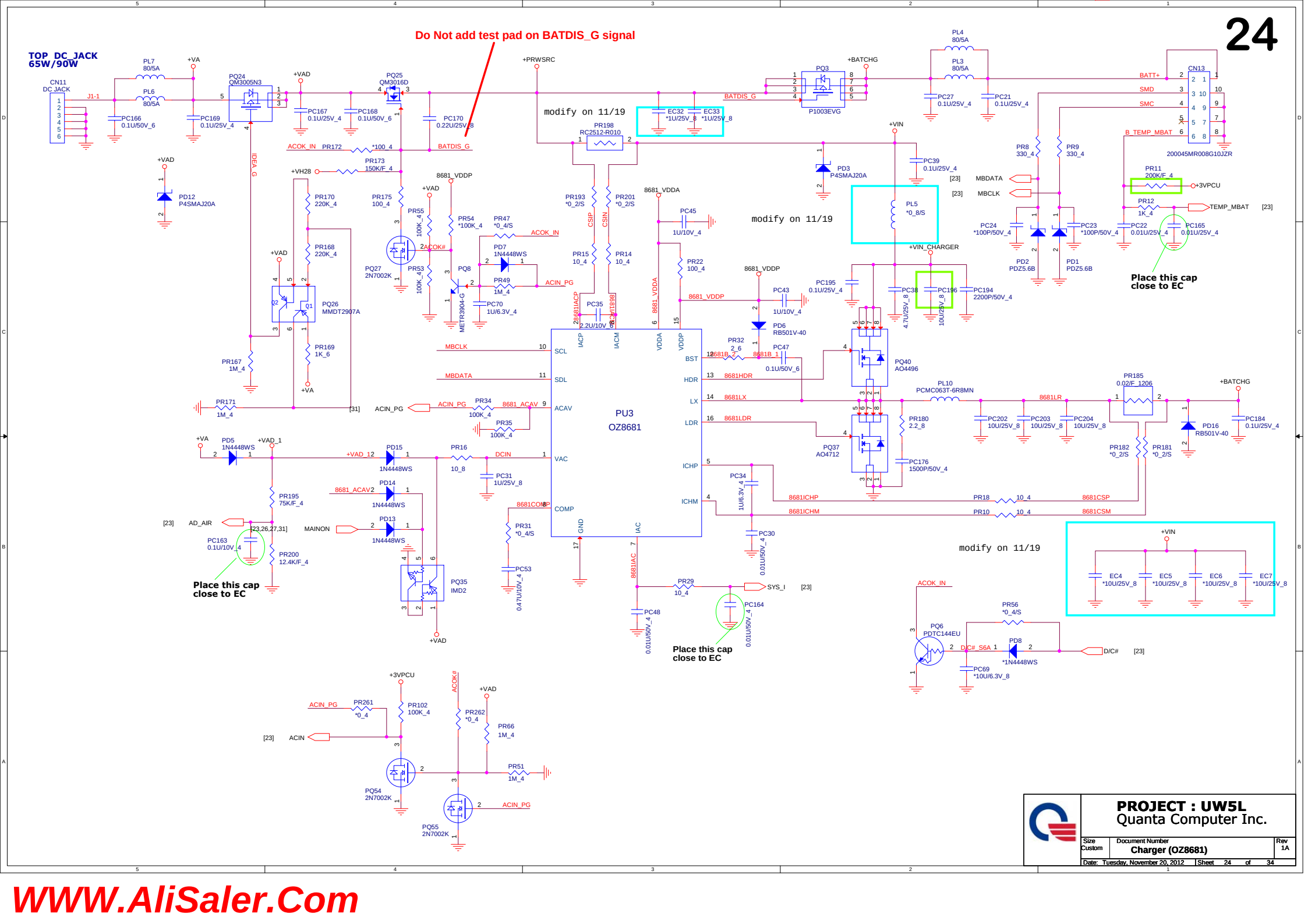
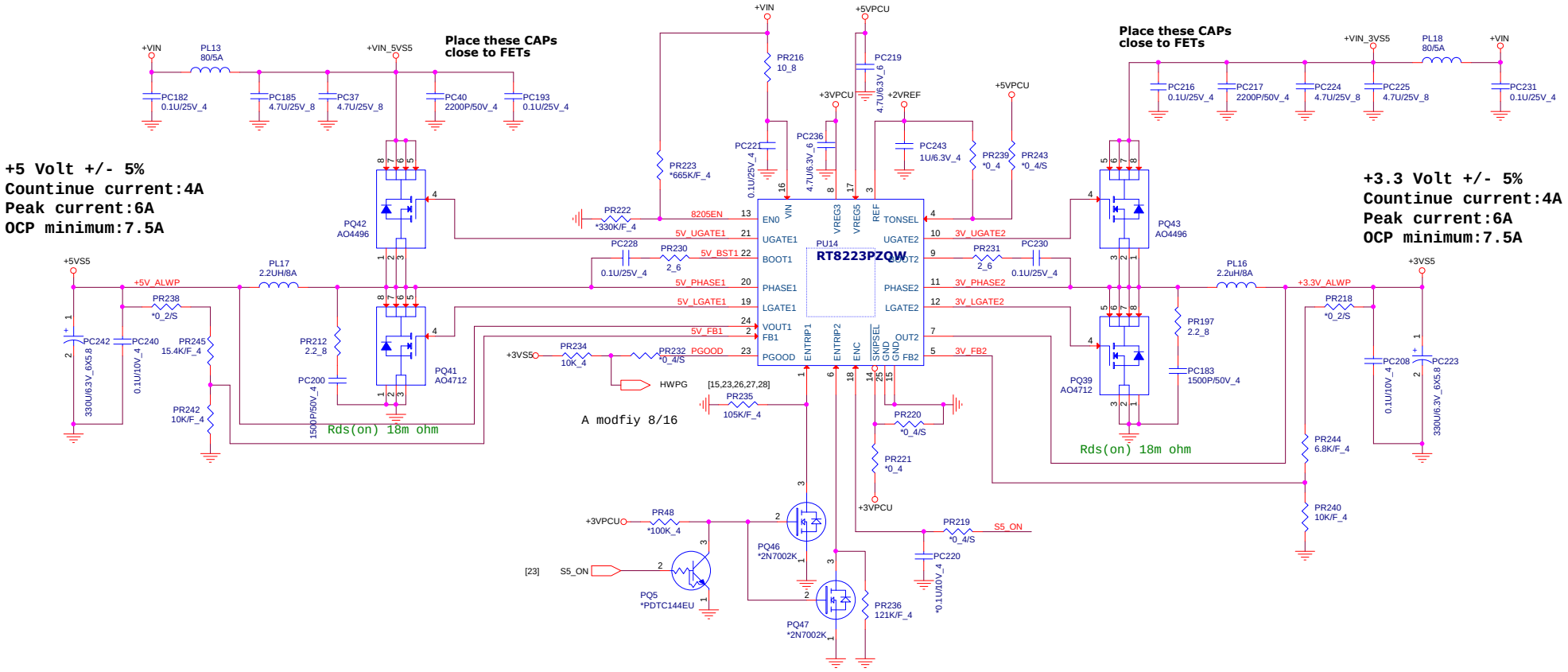
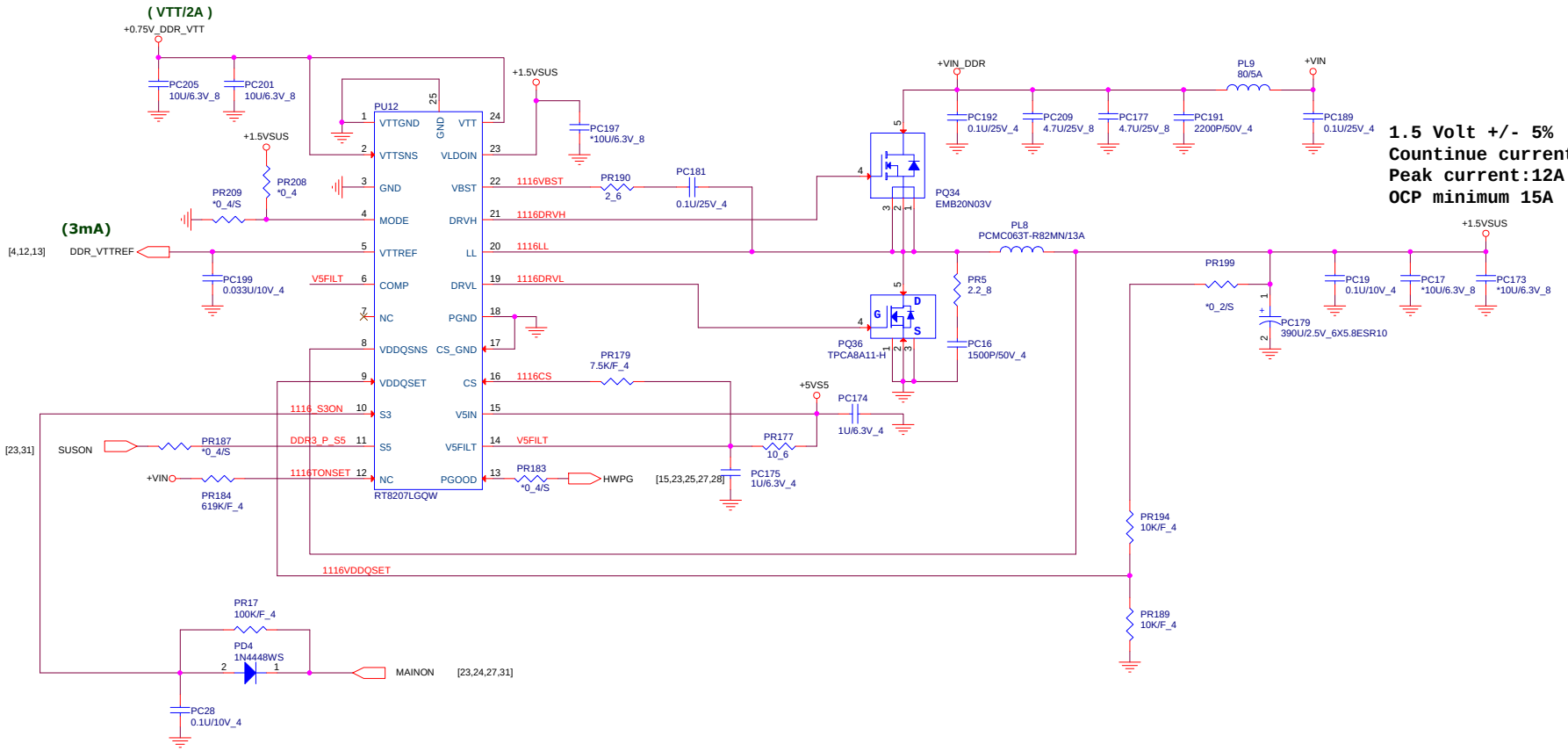


DC/DC +3VS5/+5VS5



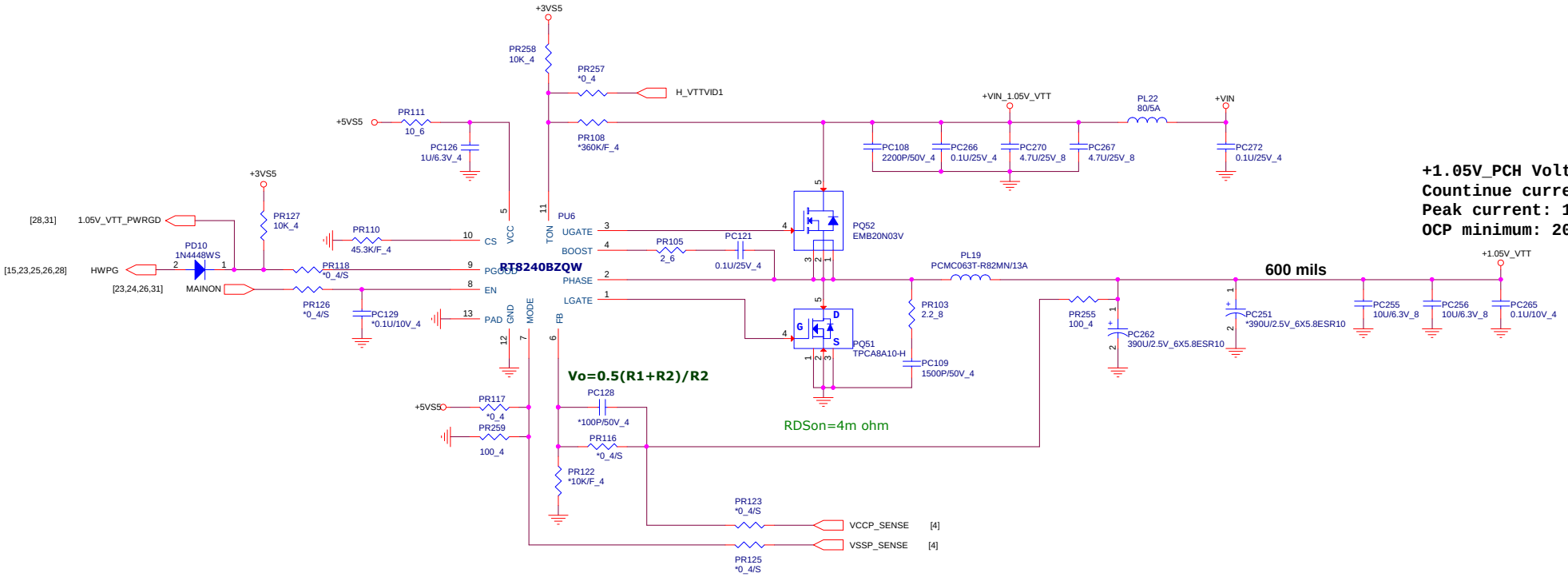
	PROJECT : UW5L Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VS5 (RT8223P)	Rev: 1A
Date: Tuesday, November 20, 2012	Sheet 25 of 34	

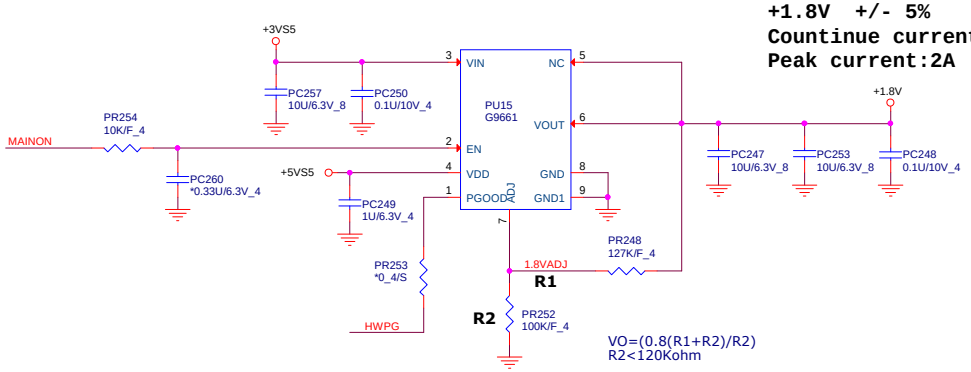


PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

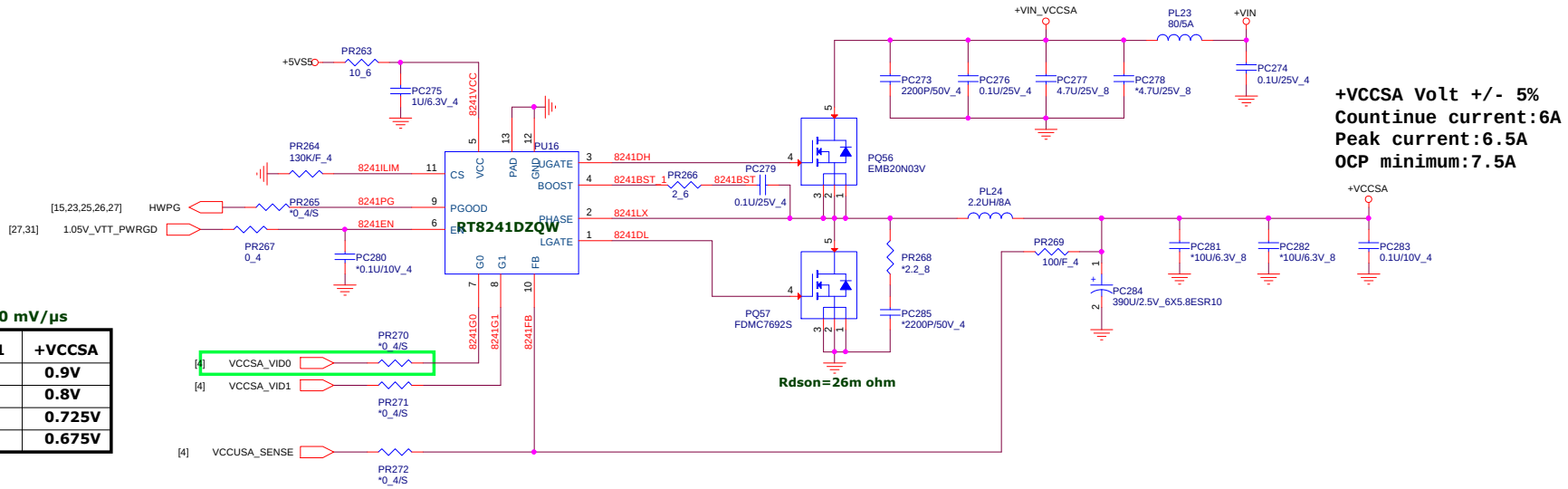
Date: Tuesday, November 20, 2012 Sheet 26 of 34





PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V_VTT (RT8238A)	1A
Date: Tuesday, November 20, 2012	Sheet 27 of 34	



+VCCSA Volt +/- 5%
Countinue current:6A
Peak current:6.5A
OCP minimum:7.5A

slew rate = 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCCSA (RT8241A)	1A

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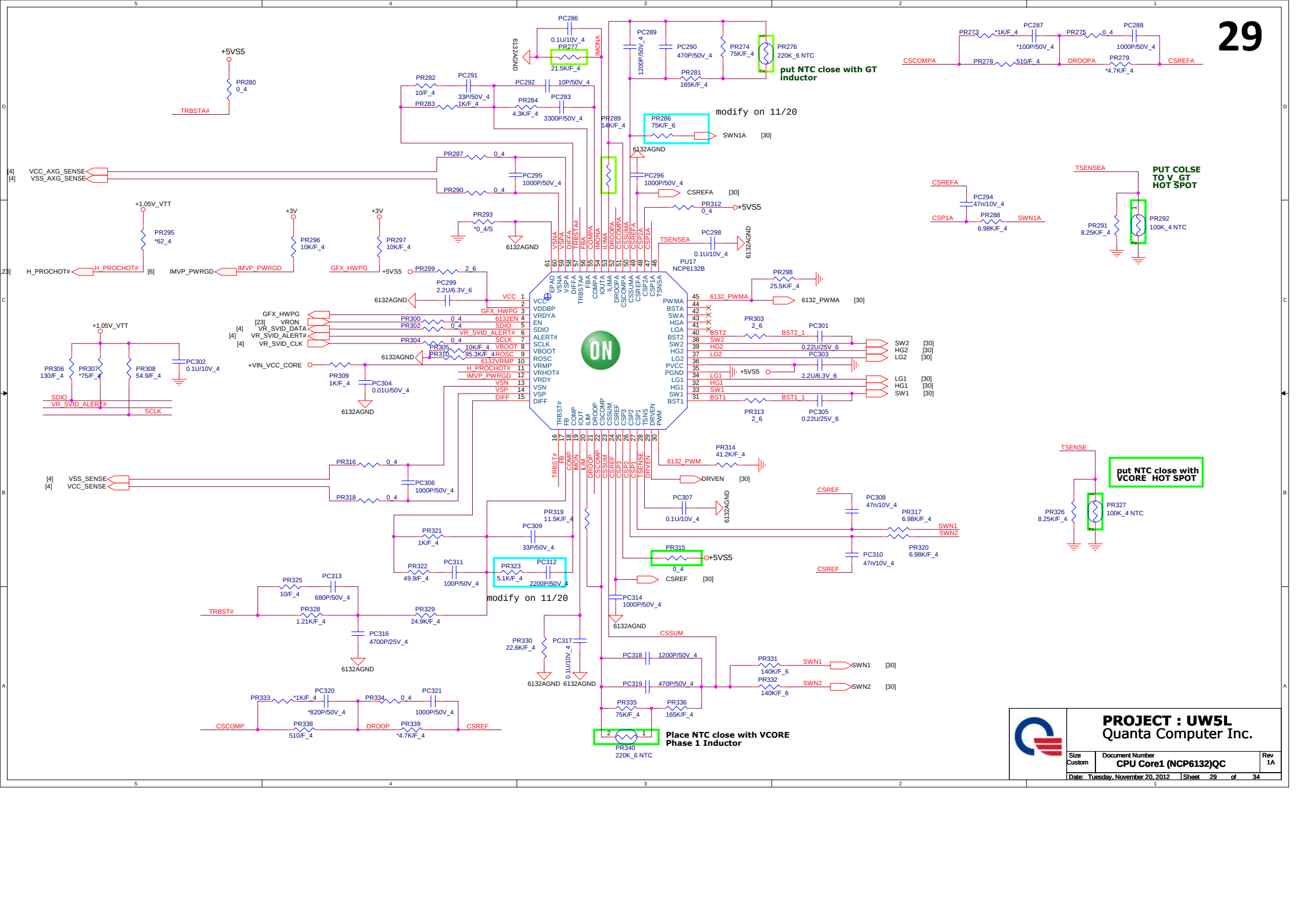

PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core1 (NCP6132)QC	1A

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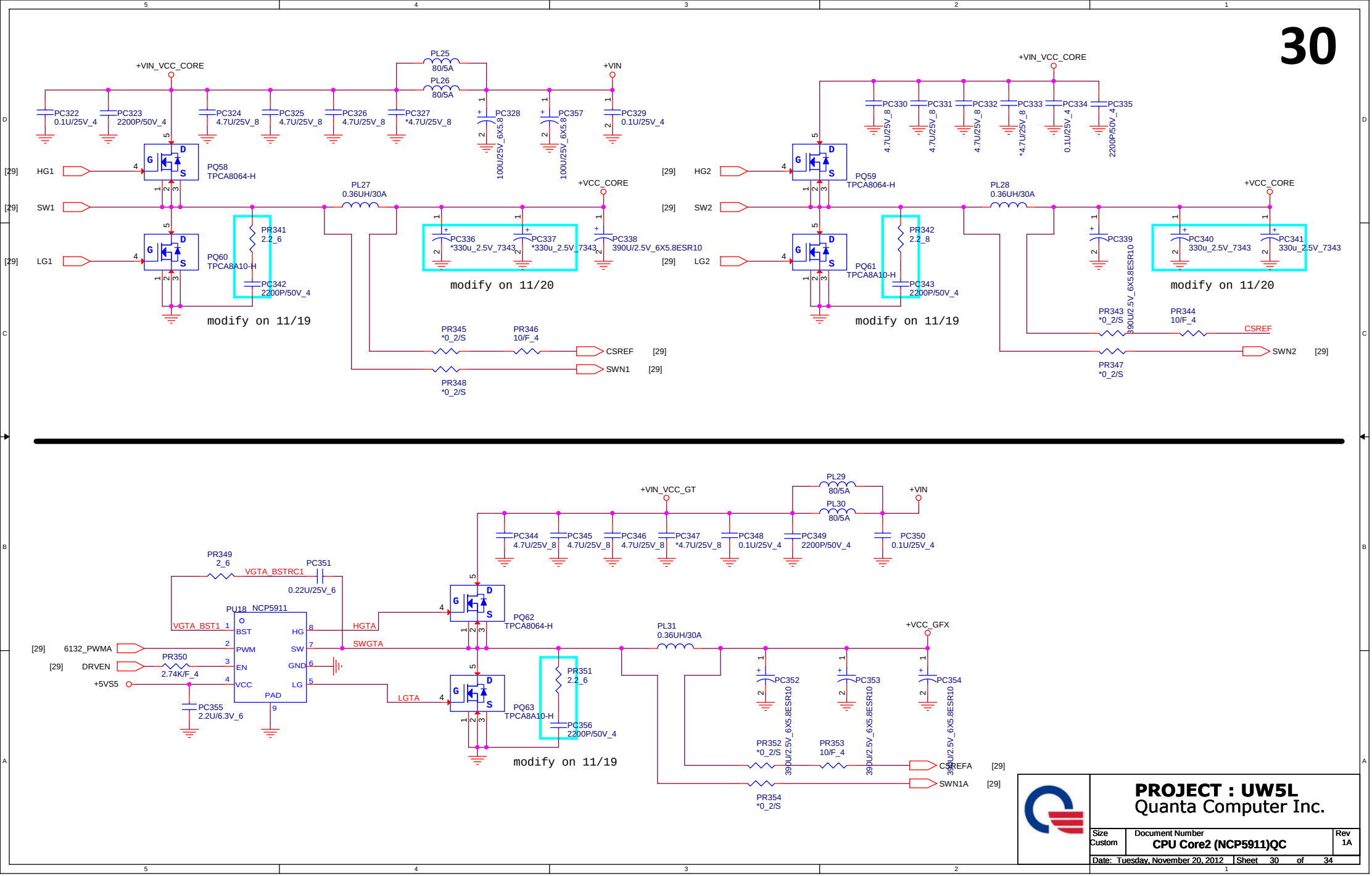

PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core2 (NCP5911)QC	1A

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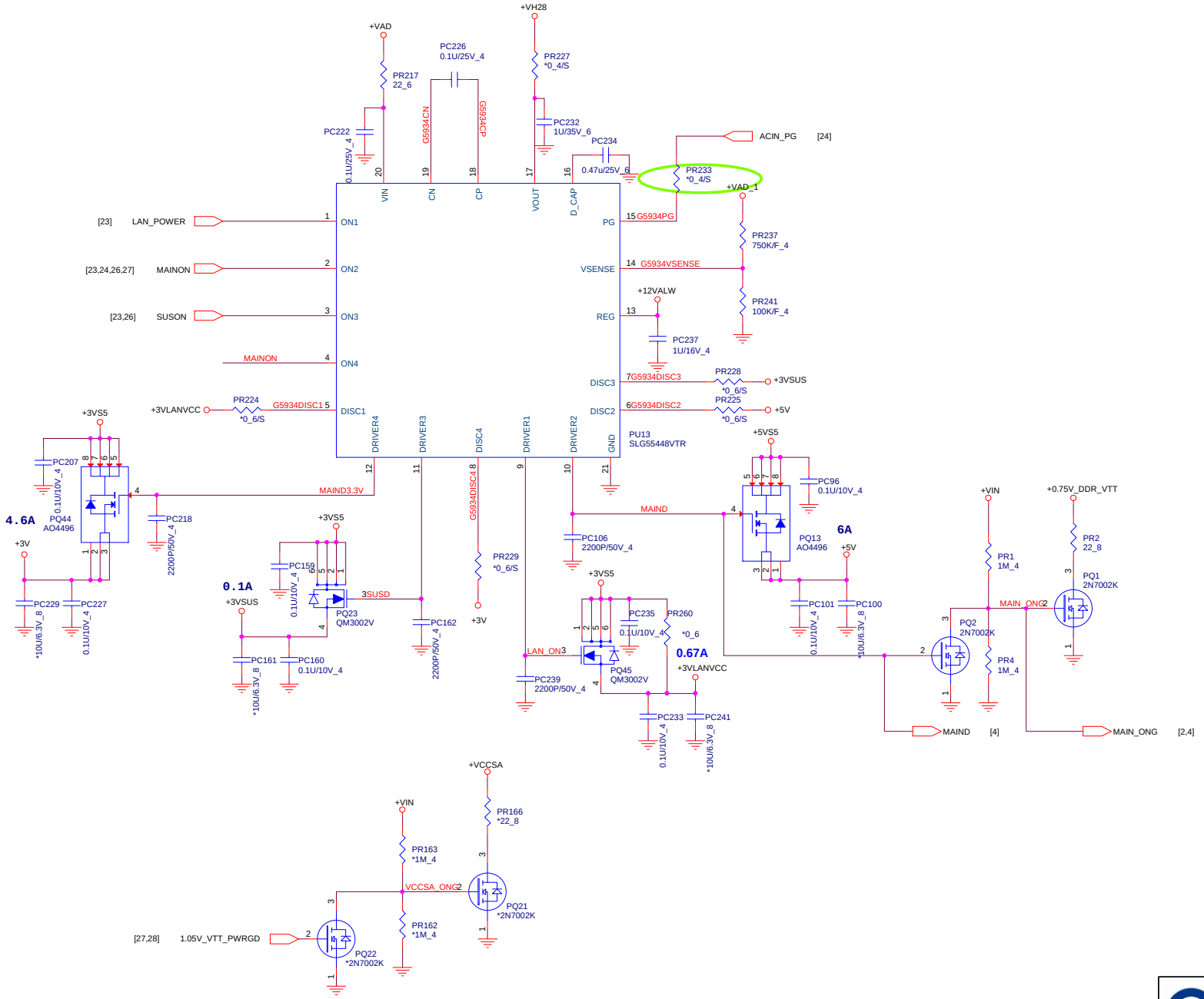

PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (GS7502)	1A
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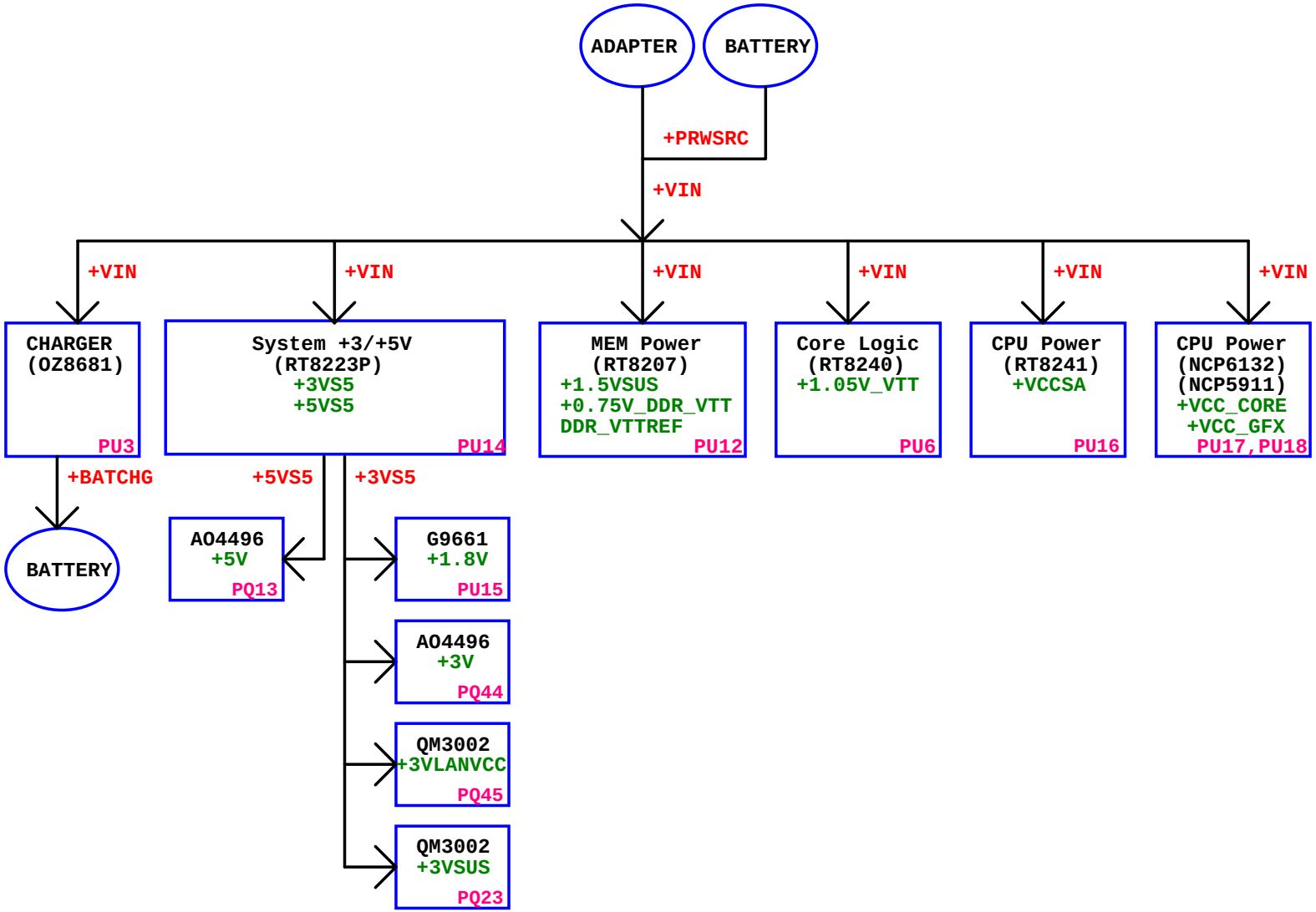
Main Power Tree



PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Main Power Tree	1A

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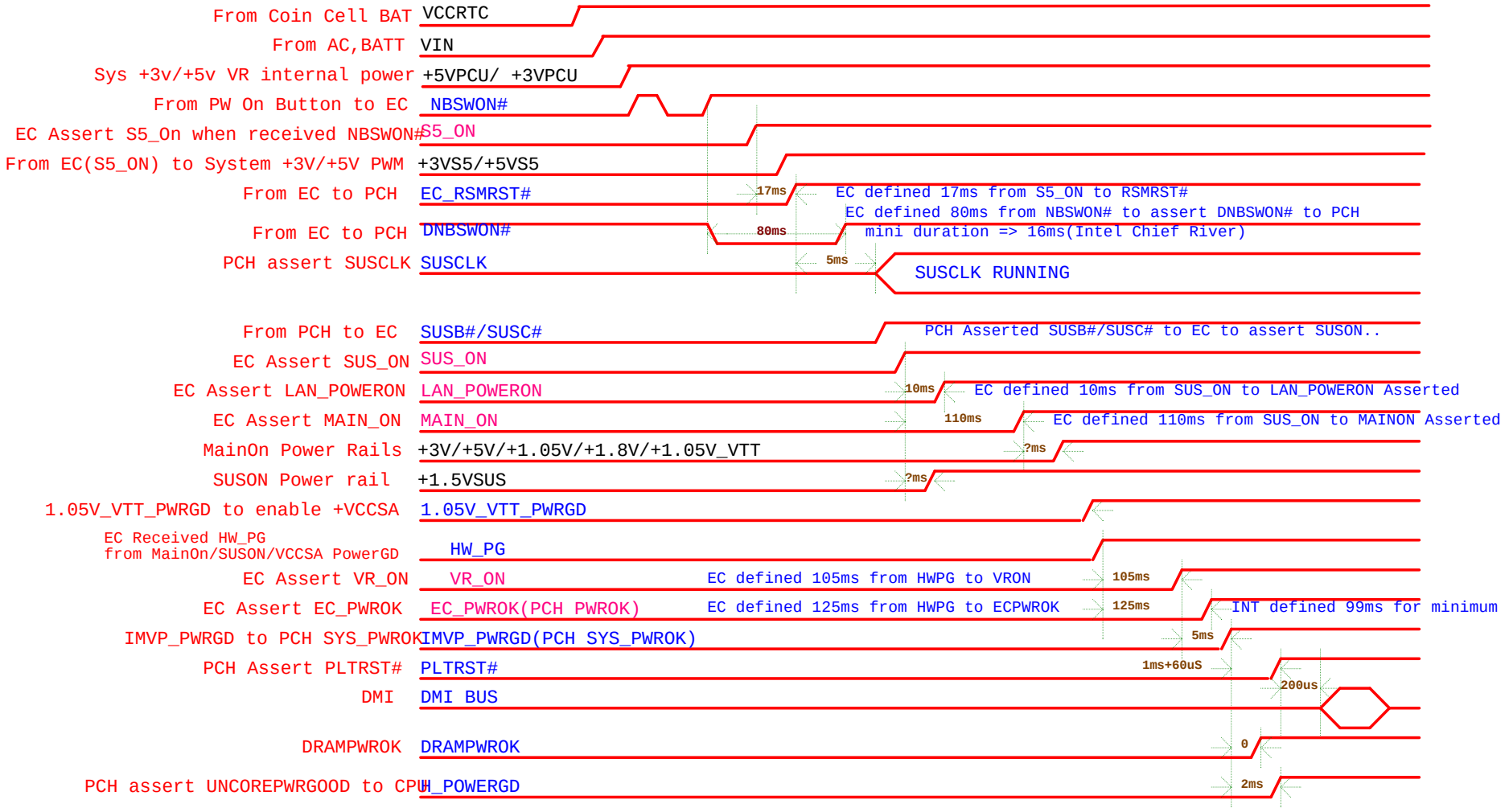
Chief River mainly Power On Sequence(G3 to S0)



PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power On Sequence	1A

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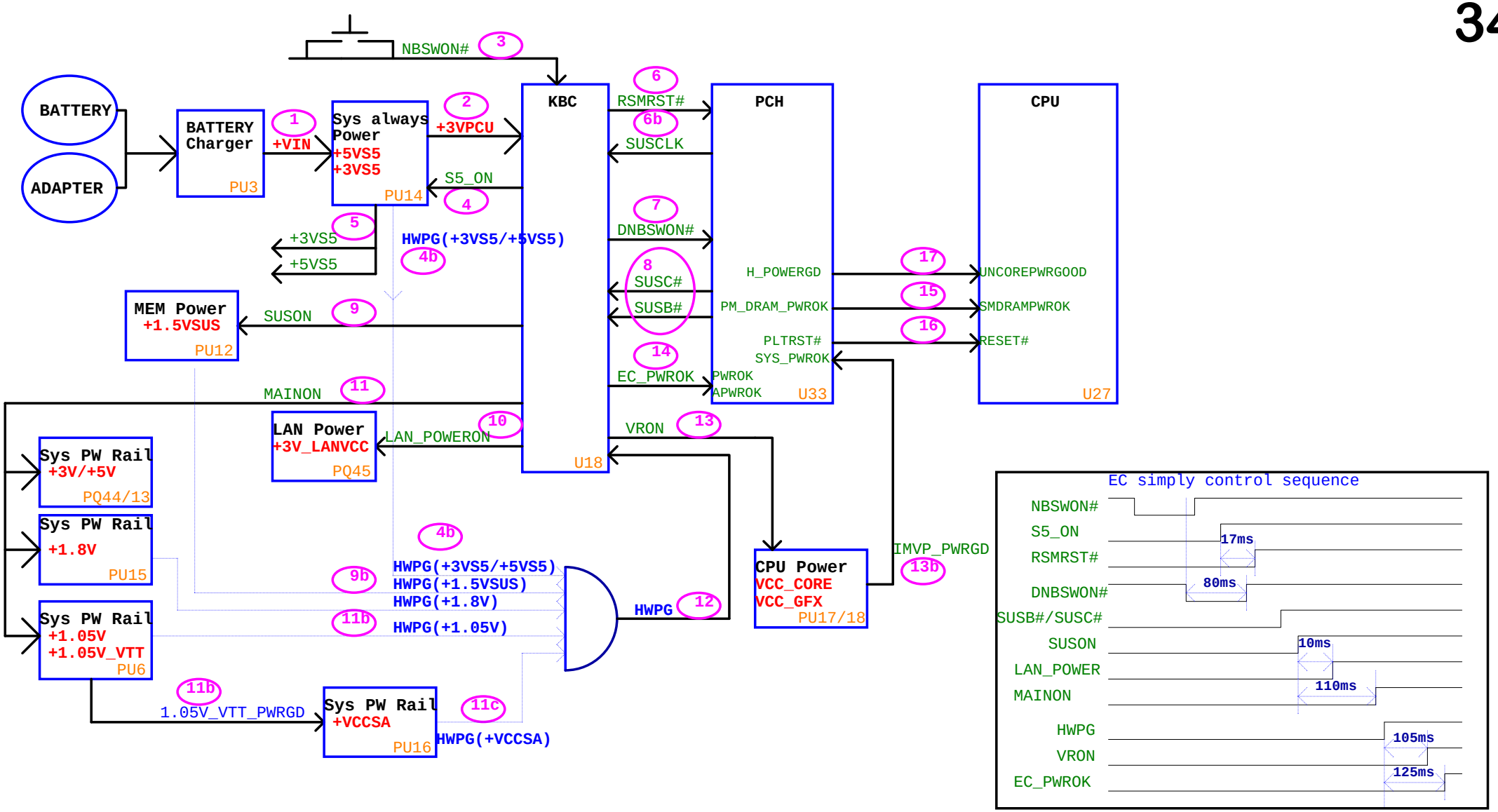

PROJECT : UW5L
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Control Procedure	1A

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