Tesla
Schematics Document

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***

Size	Document Number	Rev
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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Title: **Table of Content**

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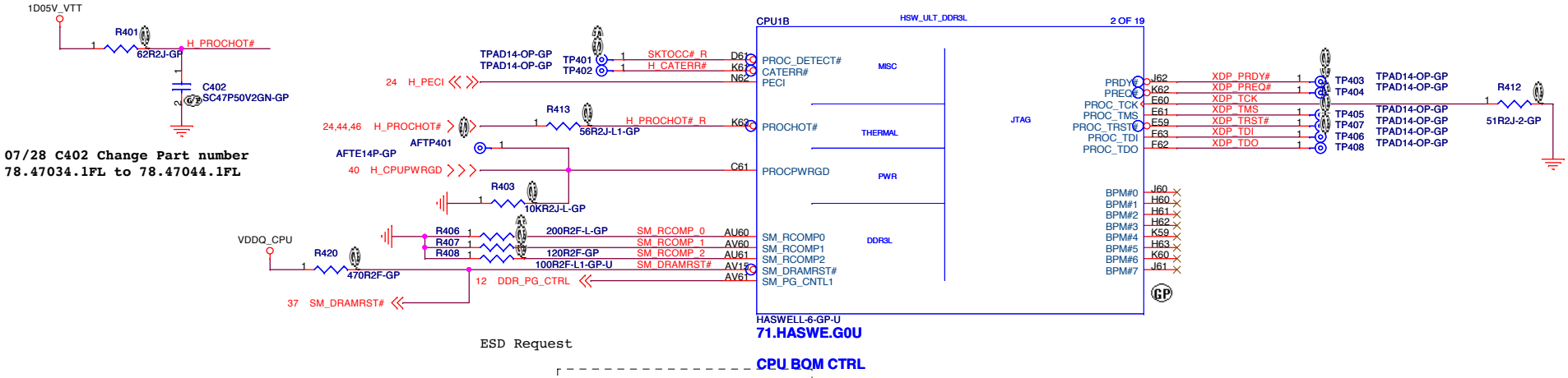
SSID = CPU

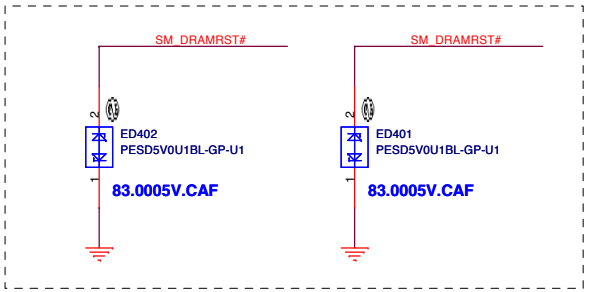
SC

071.BROAD.0M0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.6GHz 15W 1333DDR ES-2	934843 QGHA
071.BROAD.0N0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.6GHz 15W 1600DDR ES-2	934844 QGHB
071.BROAD.0P0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.8GHz 15W 1600DDR ES-2	934842 QGH9



ESD Request

CPU BOM CTRL



12/18 add ED4003, ED4004 83.0005V.CAF
一個放前端,一個放後端

06/19 Delete ESD

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
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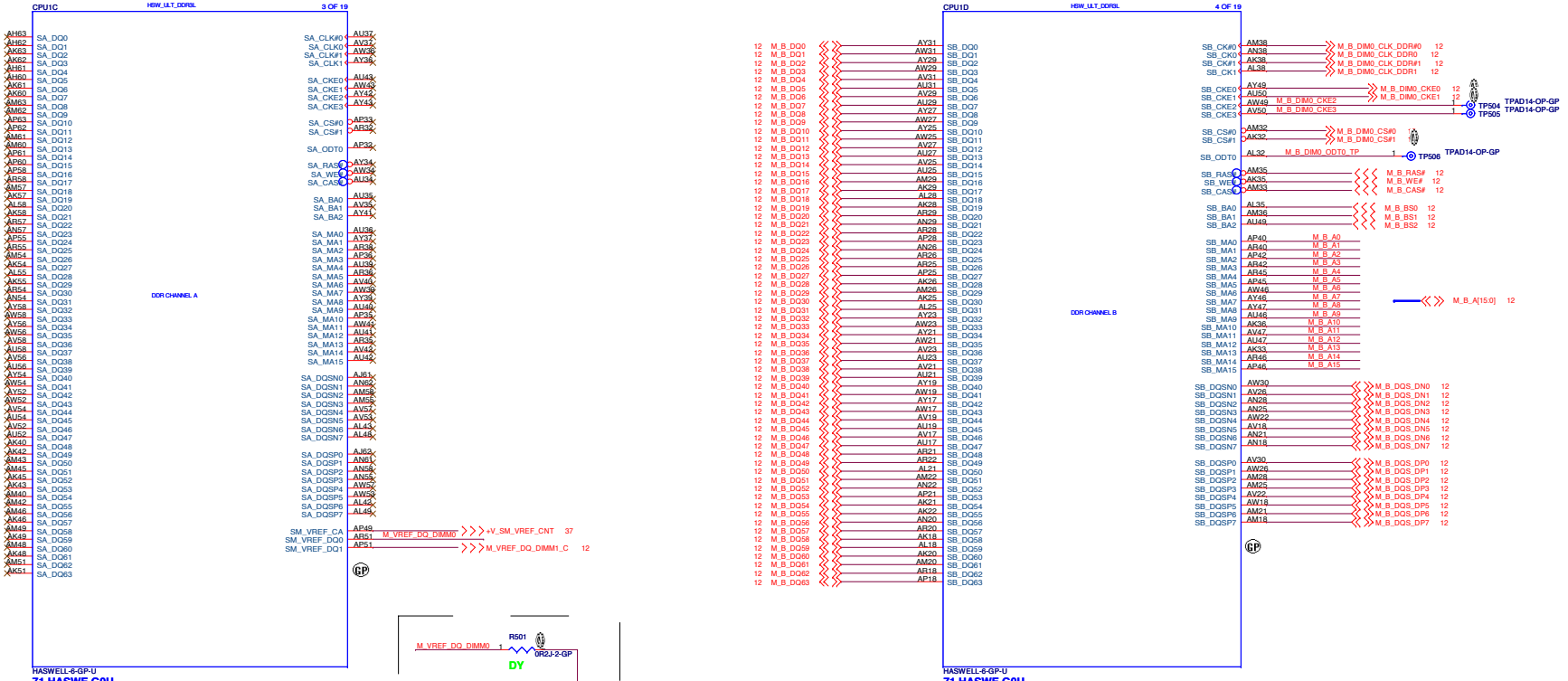
SSID = CPU



06/19 add R501 M_VREF_DQ_DIMM0 接 M_VREF_DQ_DIMM1_C

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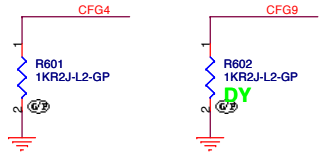
Title: CPU (DDR)

Size	Document Number	Rev
A2	LT41	-1

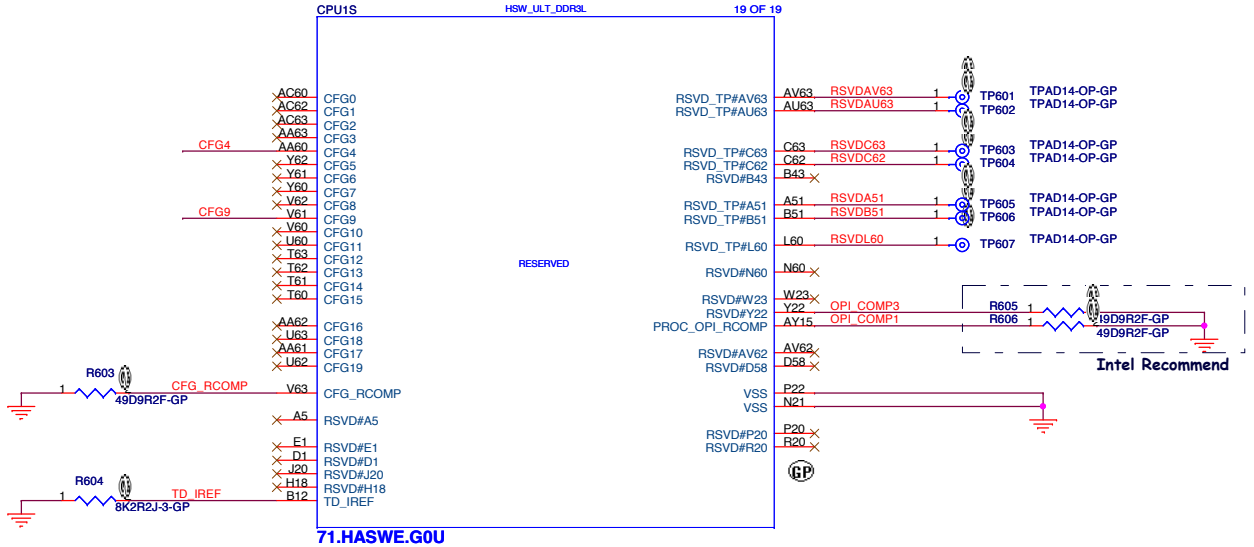
Date: Tuesday, January 20, 2015 Sheet 5 of 102

SSID = CPU

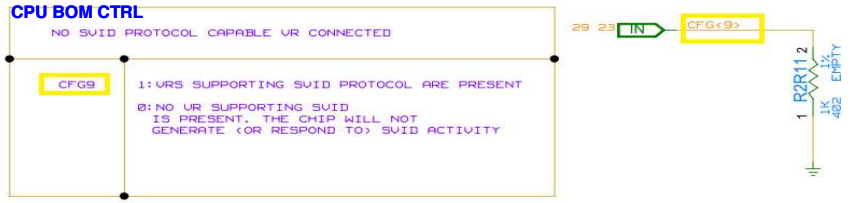
eDP Enable	
CFG4	1:Disable 0:Enable



Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[3:0]:** Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express* Static x16 Lane Numbering Reversal. — — • • **CFG[4]: eDP enable** — 1 = Disabled — 0 = Enabled • **[19:5]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
		continued...



CFG9:



7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

HARRIS_BEACH_REFRESH
REV 0.7
PBA:G62502-004

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Title: **CPU (CFG)**

Size	Document Number	Rev
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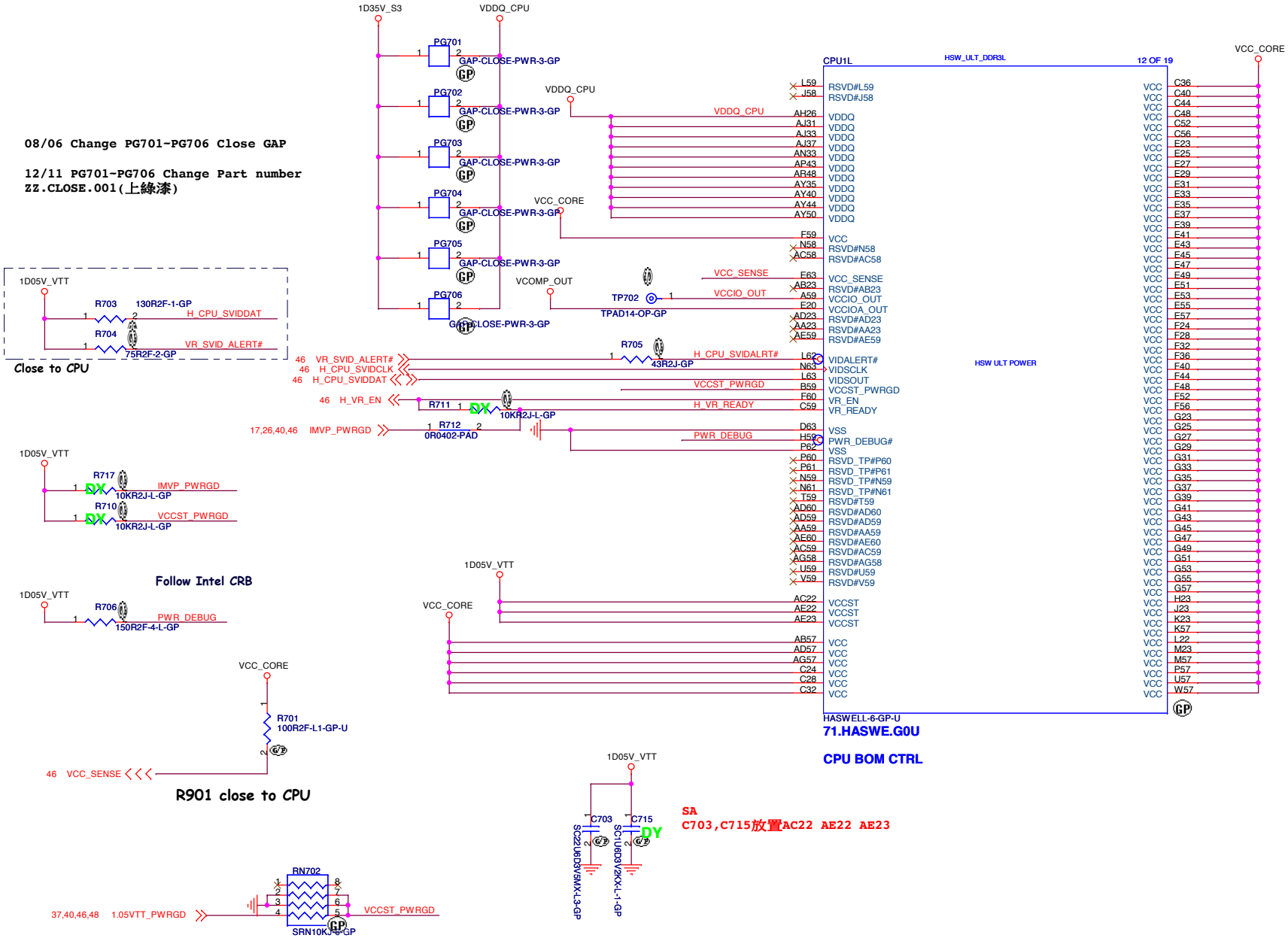
SSID = CPU

08/06 Change PG701~PG706 Close GAP

12/11 PG701~PG706 Change Part number
ZZ.CLOSE.001(上綠漆)



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Title	CPU (VCC_CORE)
Size A3	Document Number LT41
Rev	-1
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SSID = CPU

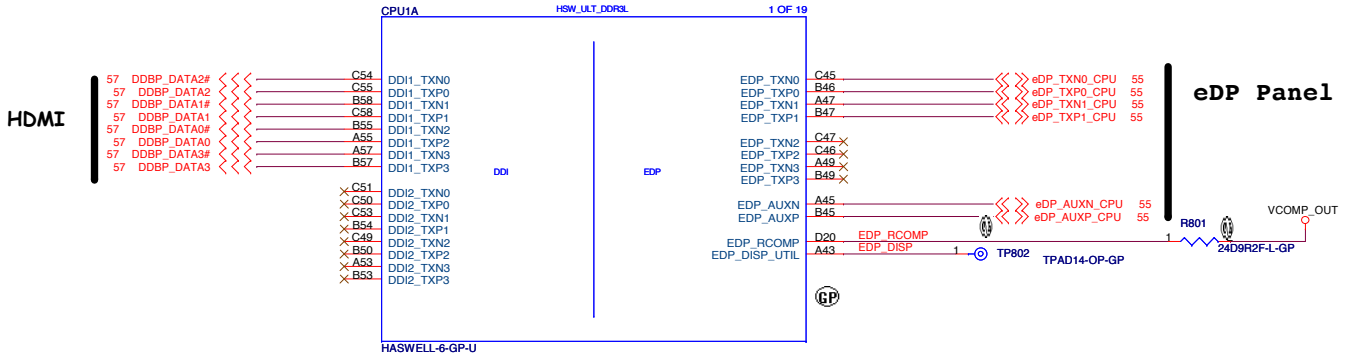

Table 19-1. Mapping of HDMI* signals for DDI ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA
Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CK
		DDPC_CTRLDATA	DDI2_CTRL_DATA

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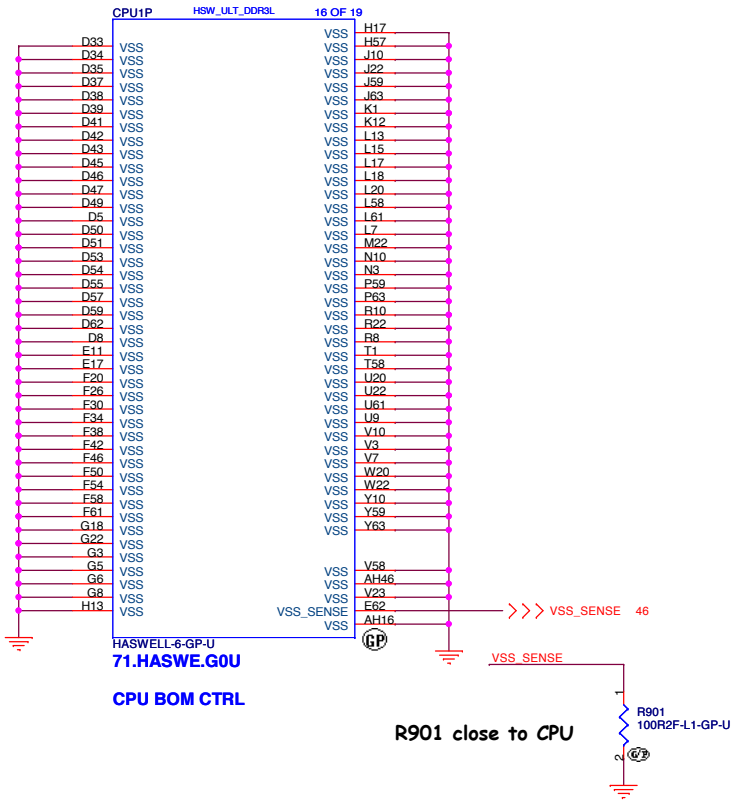
Title: CPU (DDI/EDP)

Size: Custom | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 8 of 102

SSID = CPU



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Title: ***CPU (VSS)***		
Size: A3	Document Number: **LT41**	Rev: **-1**
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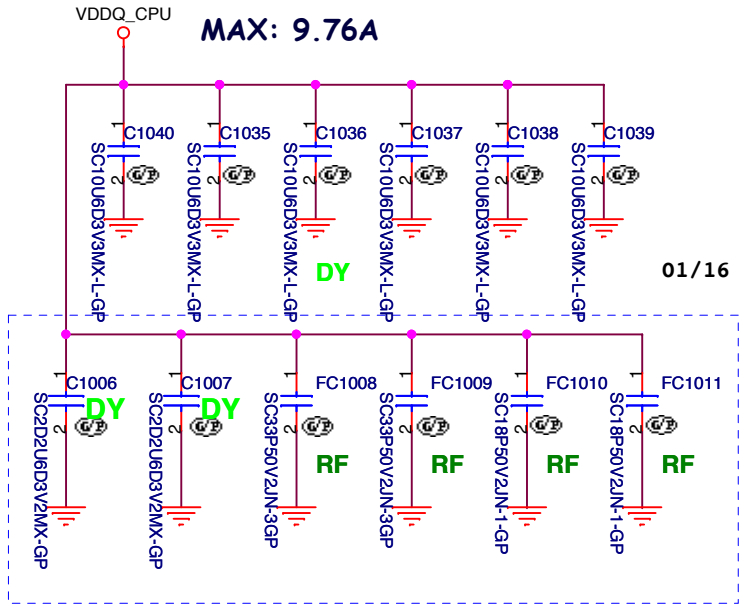
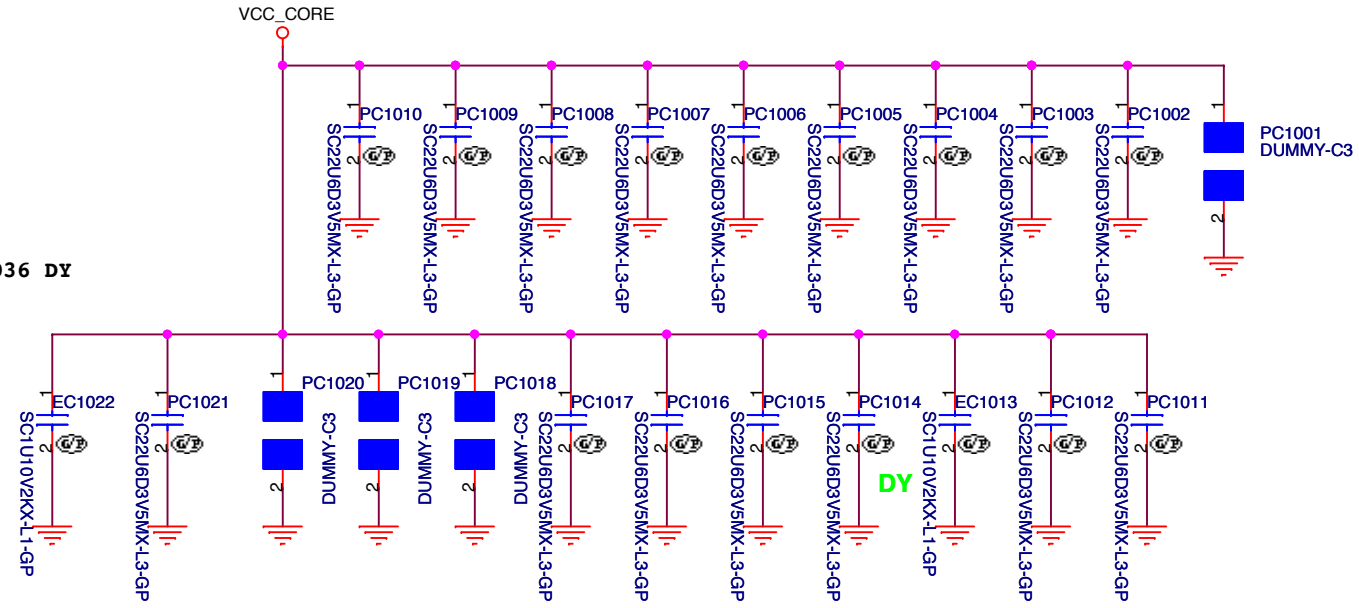


01/16 C1036 DY

For Intel Recommend EE Part

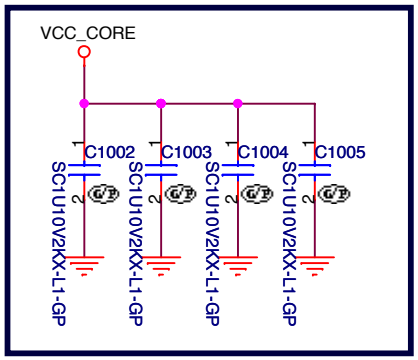
10/19 Change C1008, C1009 to RC1008,RC1009 (2.2uF to 33pF)

10/19 add RC1010, RC1011 18pF

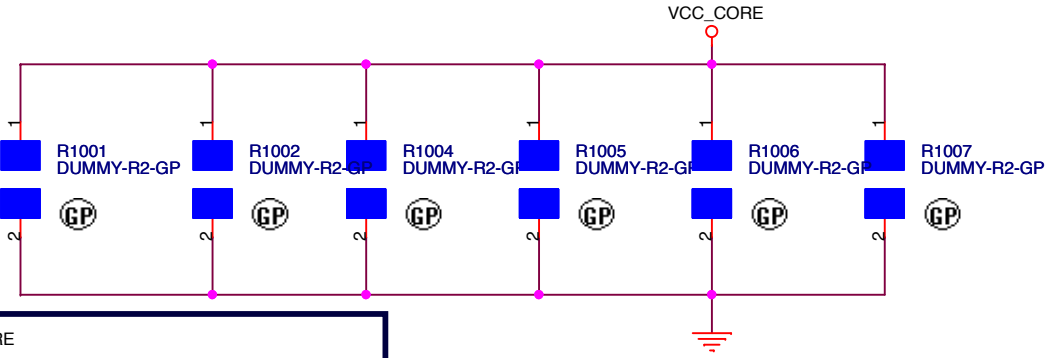


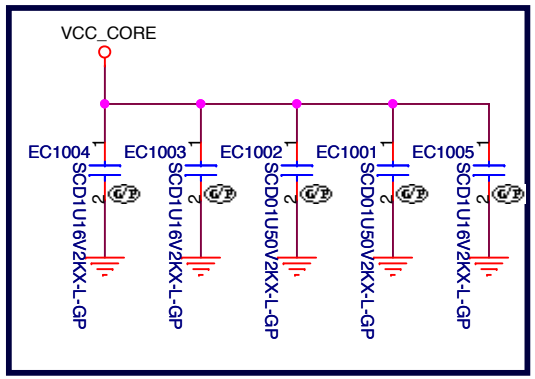
12/18 PC1013 改為EC1013 FOR EMI, 1uF 上件

12/18 PC1022 改為EC1022 FOR EMI, 1uF 上件



For Intel Recommend EE Part





For EMC Recommend

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Title: CPU (Power CAP1)

Size	Document Number	Rev
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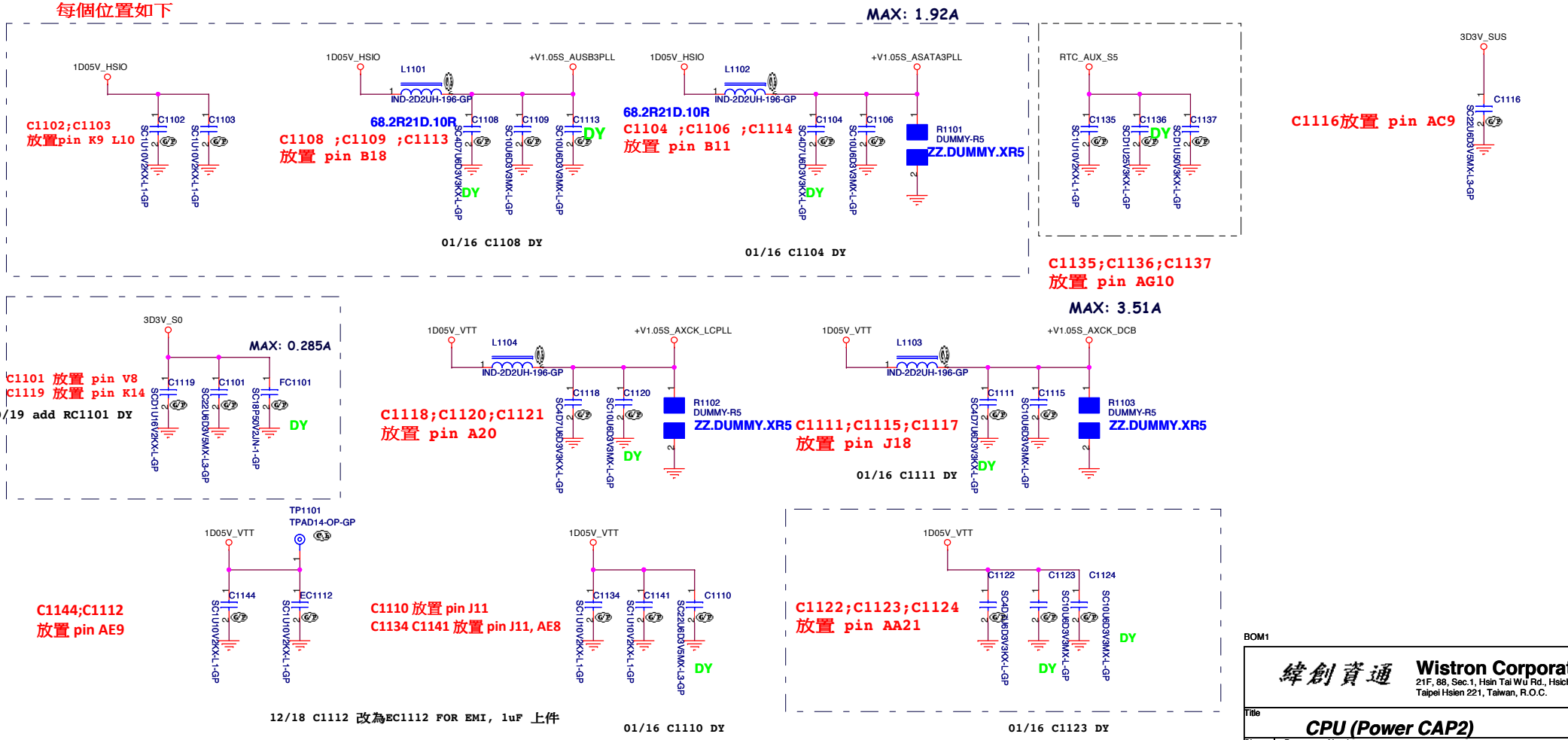
擺放電容的位置請參考Page 21
每個位置如下



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Title: CPU (Power CAP2)

Size	Document Number	Rev
Custom	LT41	-1

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SSID = MEMORY

DIMM1

DDR3-204P-262-GP-U

H = 4mm

62.10024.S21

2nd = 62.10024.M31

3rd = 62.10024.Q61

12/23 增加 3rd 62.10024.Q61

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

R1201 10KR2J-L-GP

ODT resistor must be 66.5 ohm

Q1201 DMN5L06K-7-GP
84.05067.031
2nd = 084.00138.0A31

Q1202 DMN5L06K-7-GP
84.05067.031
2nd = 084.00138.0A31

Q1202 Q1203限用於84.05067.031
因為此刻Vth為1V

Layout Note:
Place these Caps near
SO-DIMMA.

SODIMM A DECOUPLING

For Intel Recommend Close to DIMM

Close RAM1 CA & DQ pin

10/19 add FC1202 DY

Place these caps close to VTT1 and VTT2.

12/22 增加AFTP1201 測點

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Title: DDR3L-SODIMM1

Size: A2 | Document Number: LT41 | Rev: -1

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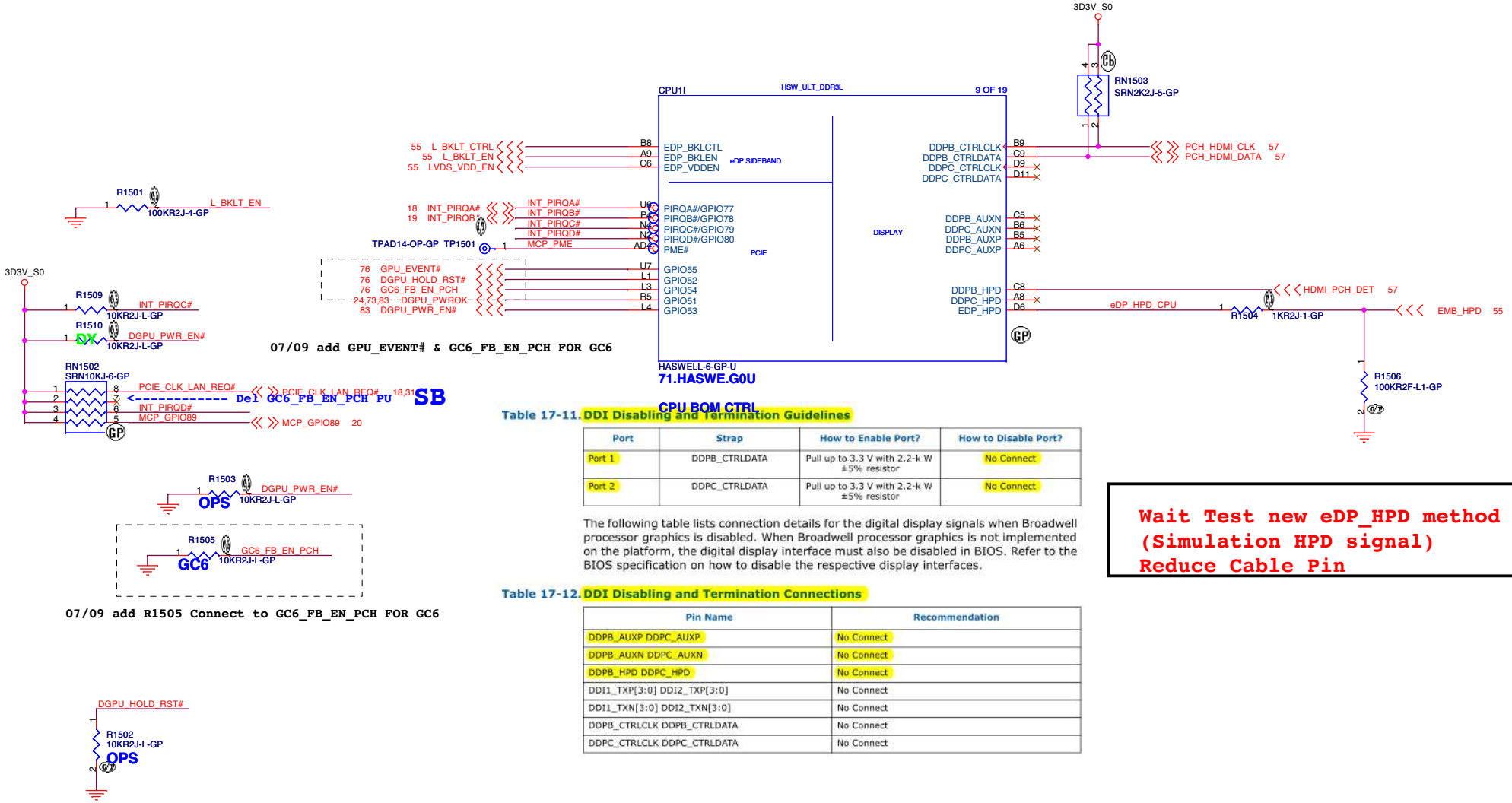

Table 17-11. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W ±5% resistor	No Connect

The following table lists connection details for the digital display signals when Broadwell processor graphics is disabled. When Broadwell processor graphics is not implemented on the platform, the digital display interface must also be disabled in BIOS. Refer to the BIOS specification on how to disable the respective display interfaces.

Table 17-12. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP DDPC_AUXP	No Connect
DDPB_AUXN DDPC_AUXN	No Connect
DDPB_HPD DDPC_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPB_CTRLDATA	No Connect
DDPC_CTRLCLK DDPC_CTRLDATA	No Connect

Wait Test new eDP_HPD method (Simulation HPD signal) Reduce Cable Pin

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緯創資通 Wistron Corporation
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Title: CPU(EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
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SSID = PCH

USB2.0 Table

Pair	Device
0	USB3.0 Port 1 (USB_OC#0)
1	USB3.0 Port 2 (with Debug Function) (USB_OC#1)
2	NC
3	Camera
4	USB2.0 Port 4 (USB_OC#2)
5	WLAN(Bluetooth)
6	NC
7	Panel Touch

USB3.0 Table

Pair	Device
1	USB3.0 Charger Port 1
2	USB3.0 Port 2
3	Reserved
4	USB3.0 Card Reader Port 2

PCIE Table

Pair	Device
1	Reserved
2	Reserved
3	WLAN
4	LAN
5	GPU
6	Reserved

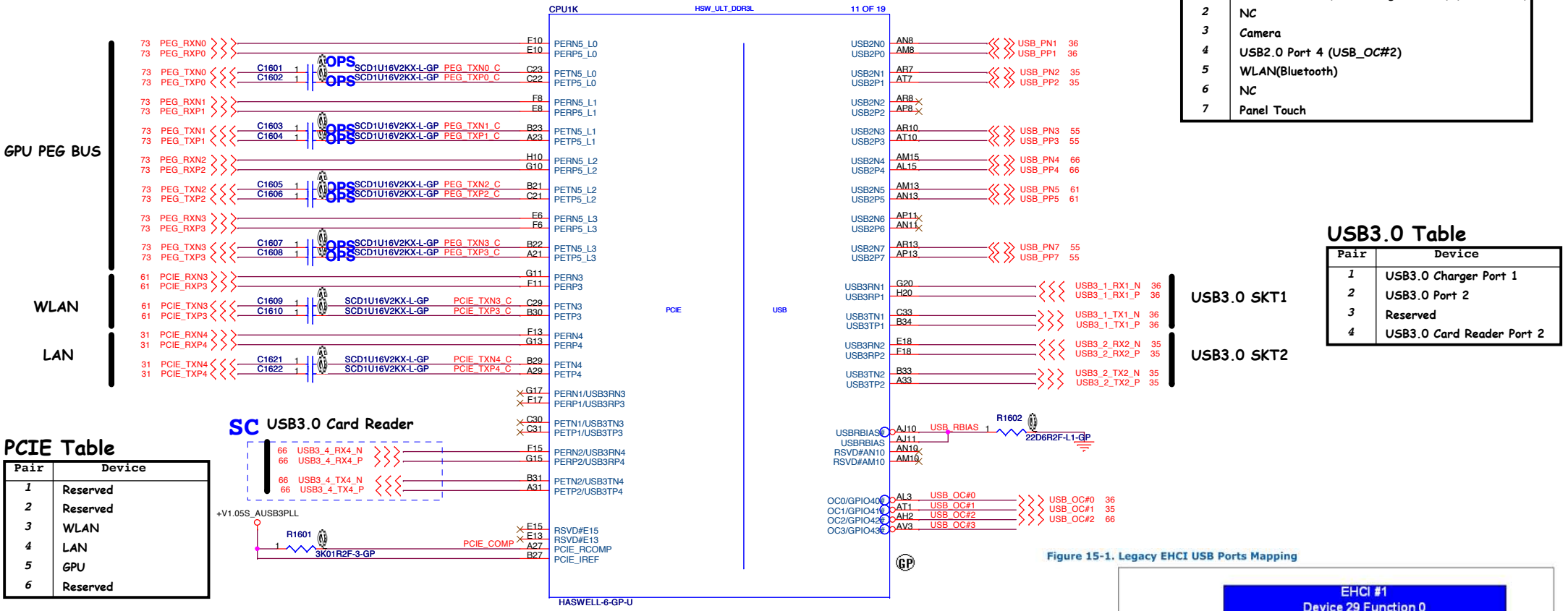
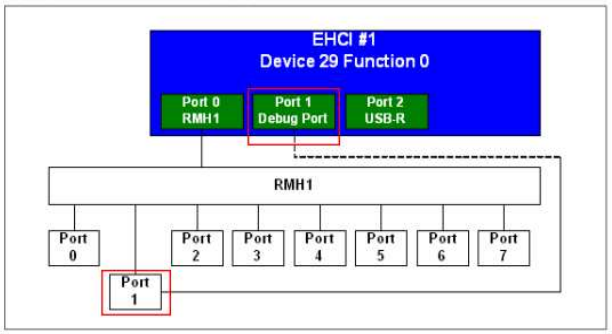


Figure 15-1. Legacy EHCI USB Ports Mapping



71.HASWE.G0U

CPU BOM CTRL

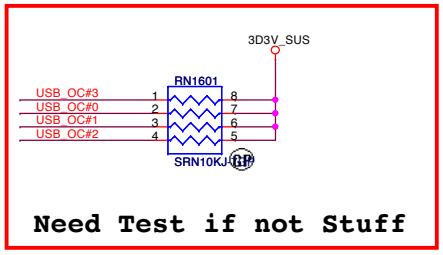


Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD							PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										

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Title: **CPU (PCI/USB)**

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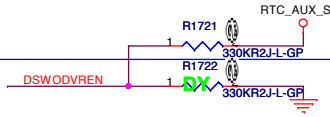
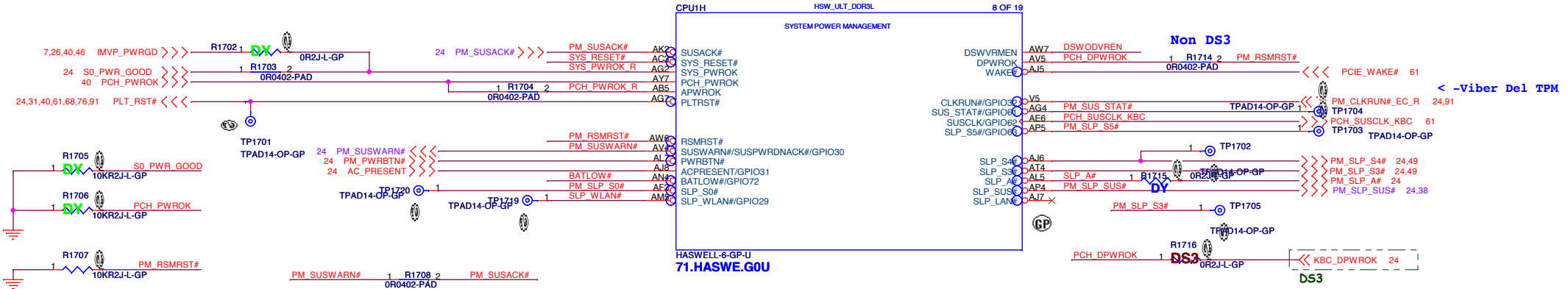
SSID = PCH

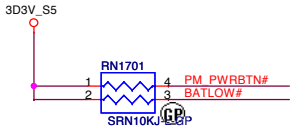
Bit	Description
31:3	Reserved
2	**WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN)** - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': • Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. • Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. **NOTE:** Deep Sx disabled configuration must leave this bit at '0'.

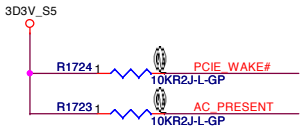
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

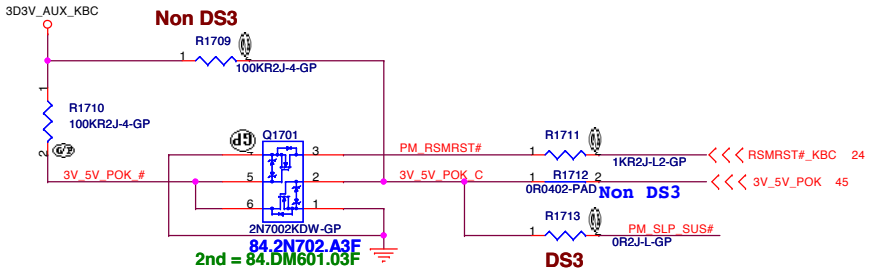


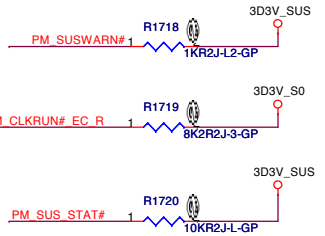
Follow Intel CRB



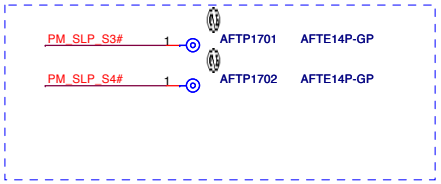








SC

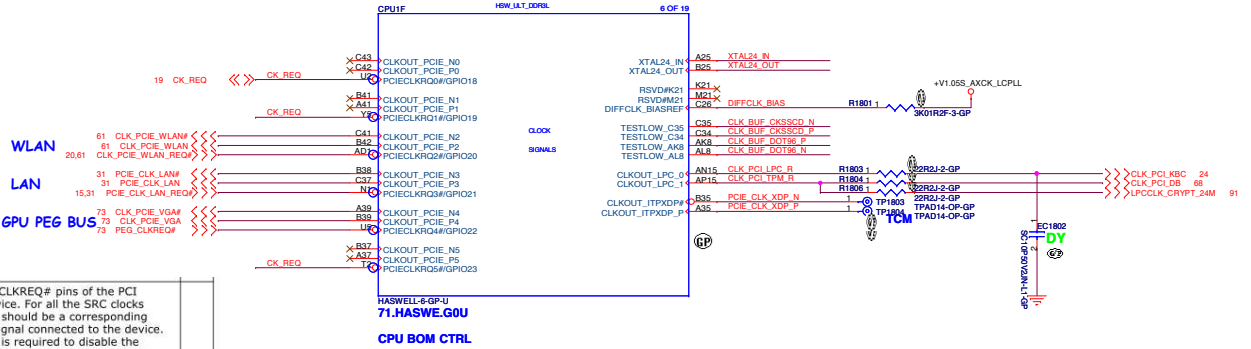


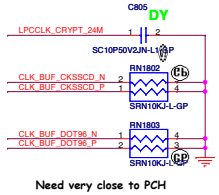
BOM1

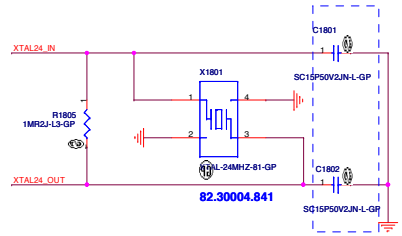
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DMI/FDI/PM)
Size: A3 | Document Number: LT41 | Rev: -1
Date: Tuesday, January 20, 2015 | Sheet 17 of 102

SSID = PCH



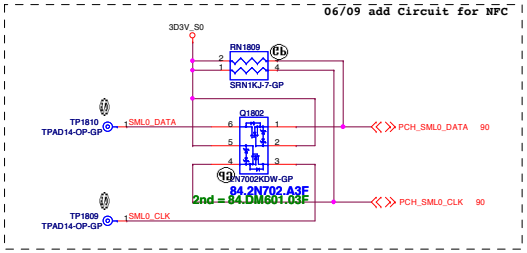


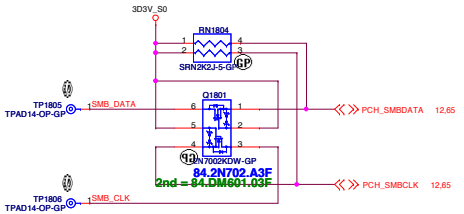


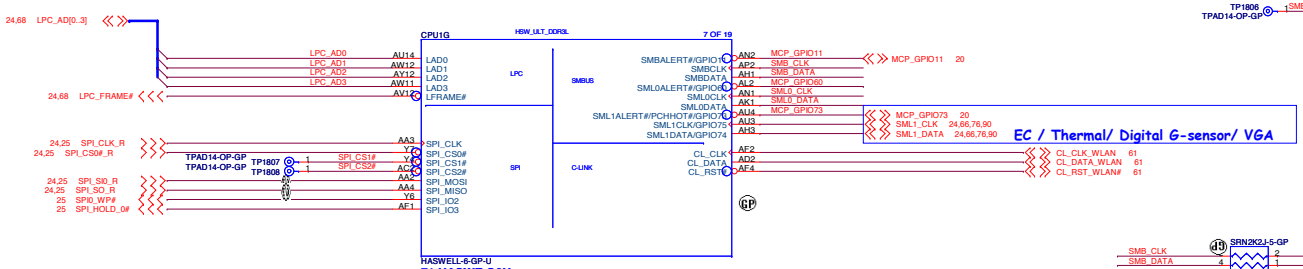
PCIECLKRQ[5:0]#	Clock request signals. 10 KΩ ±5% external pull-up resistors required to core rail. PCIECLKRQ[7:0]#	Connect to CLKREQ# pins of the PCI Express device. For all the SRC clocks used, there should be a corresponding CLKREQ# signal connected to the device. The pull-up is required to disable the functionality in the absence of actively driven by device. **Note:** If the pin is not used as PCIECLKRQ# or as GPIO, refer to an un-used GPIO for termination guidance. **Note:** PCIECLKRQn# assignment is fixed to the PCIe* Root Port (n+1), it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIe* Root Port n via FITC tool. A 10 KΩ ±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled by means of the Intel® Management Engine (Intel® ME) FW. Please refer to *Intel® ME FW Bring Up Guide* for configuring/ disabling CLKREQ#.

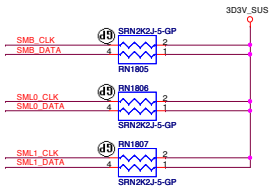
PCIE Table

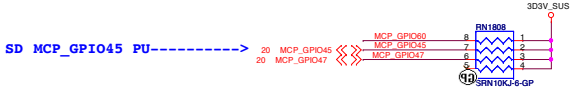
Pair	Device
1	Reserved
2	Reserved
3	WLAN(RQ2#)
4	LAN(RQ3#)
5	GPU(RQ4#)
6	Reserved











08/05 add SENSOR_HUB_INT#

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 18 of 102

SSID = PCH

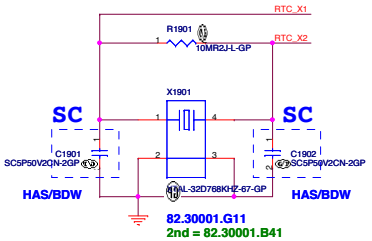
X1901 32D768KHZ BDW U SPEC:

32 Real Time Clock (RTC) Design Guidelines

Note: Unless otherwise indicated, this content pertains to Broadwell U, Broadwell Y and Broadwell H 1-chip platforms. Information relating specifically to one platform only (Broadwell U, Broadwell Y or Broadwell H) will be marked with "BDW U" "BDW Y" or "BDW H" in paragraph margins as appropriate.

Note: Max Crystal ESR = 50k Ohm.

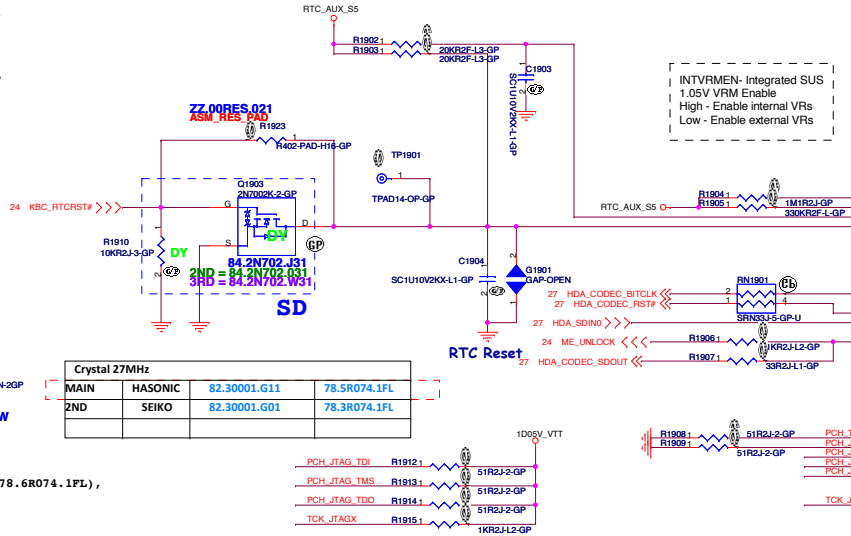
The PCH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

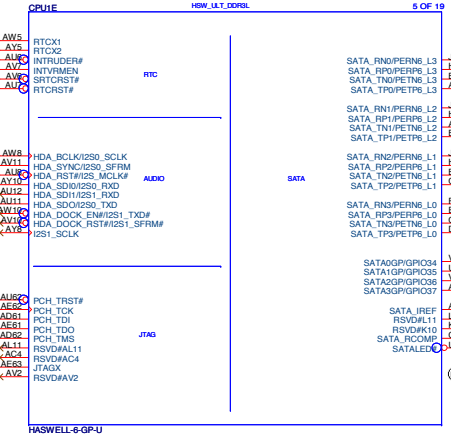


82.30001.G11
2nd = 82.30001.B41

10/22 C1902, C1901 Haswell 用6pF (78.6R074.1FL), Broadwell 5pF

Crystal 27MHz			
MAIN	HASONIC	82.30001.G11	78.5R074.1FL
2ND	SEIKO	82.30001.G01	78.3R074.1FL



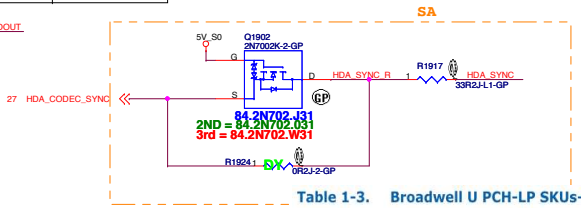


HDD

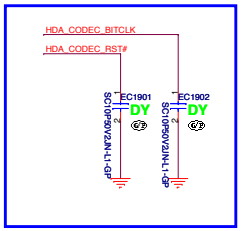
SATA Table	
Pair	Device
0	HDD/SSD
1	NGFF SATA
2	Reserved
3	Reserved

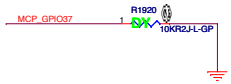
INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

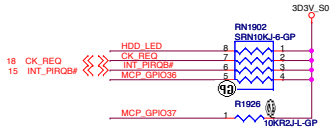
Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable



For EMC Recommend







EMC HDD TVS need to close CPU

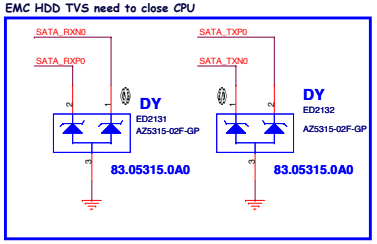


Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1 SSD	USB 3.0 Port 4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3 / PCIe* Port 6 Lane 0 SSD	SATA 6Gb/s Port 2 / PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1 / PCIe* Port 6 Lane 2	SATA 6Gb/s Port 0 / PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3 / PCIe* Port 1 SSD	USB 3.0 Port 4 / PCIe* Port 2 SSD	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0

2.1 PCIe SSD

PCIe SSD is one of the new features in Broadwell (2014) platform. In Haswell (2013) platform, only SATA-based SSD is supported. Moving SSD to PCIe gives better SSD performance over previous generation. M.2 Socket 2 supports both SATA and PCIe based SSDs. Figure below shows the configuration of High Speed I/Os in 2013/2014 PCH. The Haswell board can be made ready for both, the optional PCIe SSD and SATA SSD, by routing PCIe Port 6 Lane 0 and Lane 1 to the M.2 Socket 2 connector. For details on M.2 signals and pins for SATA and PCIe, please refer to Documentation Table below, M.2 row.

Configuration of High Speed I/Os in 2013/2014

	USB3 P1	USB3 P2	PCIe P1 NAND / USB3 P3	PCIe P2 NAND / USB3 P4	PCIe P3	PCIe P4	PCIe P5 L0 NAND	PCIe P5 L1 NAND	PCIe P5 L2	PCIe P5 L3	PCIe P6 L0 NAND / SATA P3	PCIe P6 L1 NAND / SATA P2	PCIe P6 L2 / SATA P1	PCIe P6 L3 / SATA P0
	GbE	GbE	GbE	GbE	GbE	GbE	GbE	GbE	GbE	GbE				
	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/LPC/SATA/HDA)

Size: Custom | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 19 of 102

SSID = PCH

Thermal

Thermal
NCT7718: 1
Thermal VD : 0

NCT7718&TV

SKU	Fun./Location	7718/TV
SKU1,2	R2037	ASM
SKU3	R2036	ASM

01/20 RN2002 SWAP,走線較好

SB

08/06 add SENSOR_HUB_INT#

08/14 add NFC Detect pin

08/05 add SENSOR_HUB_INT#

CPU1J
HSW_ULT_DDR3L
10 OF 19
HASWELL-6-GP-U
71.HASWE.G0U

<-----Default:Low

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

CPU BOM CTRL

	GSPI0_MOSI_BBS0_R(SSD_PWR)
PU	RESERVED
PD	SPI BUS

TOUCH&VRAM

TOUCH

Fun./Location	TOUCH	NON TOUCH
R2019	ASM	DY
R2020	DY	ASM

VRAM 900MHZ&1000MHZ

Fun./Location	900MHZ	1000MHZ
R2032	ASM	DY
R2033	DY	ASM

VRAM SINGLE&DUAL

SKU2, SKU3 SKU4, SKU5

Fun./Location	SINGLE	DUAL
R2021	ASM	DY
R2022	DY	ASM

UMA&OPS

DGPU_PRSNT#
UMA: 1
Optimus(Muxless) : 0

UMA&OPS

SKU	Fun./Location	UMA/DIS
SKU1	R2013	ASM
SKU2~5	R2014	ASM

08/13 add NFC Detect Pin

<-Viber Del TPM

<-----------LS41 NO ODD

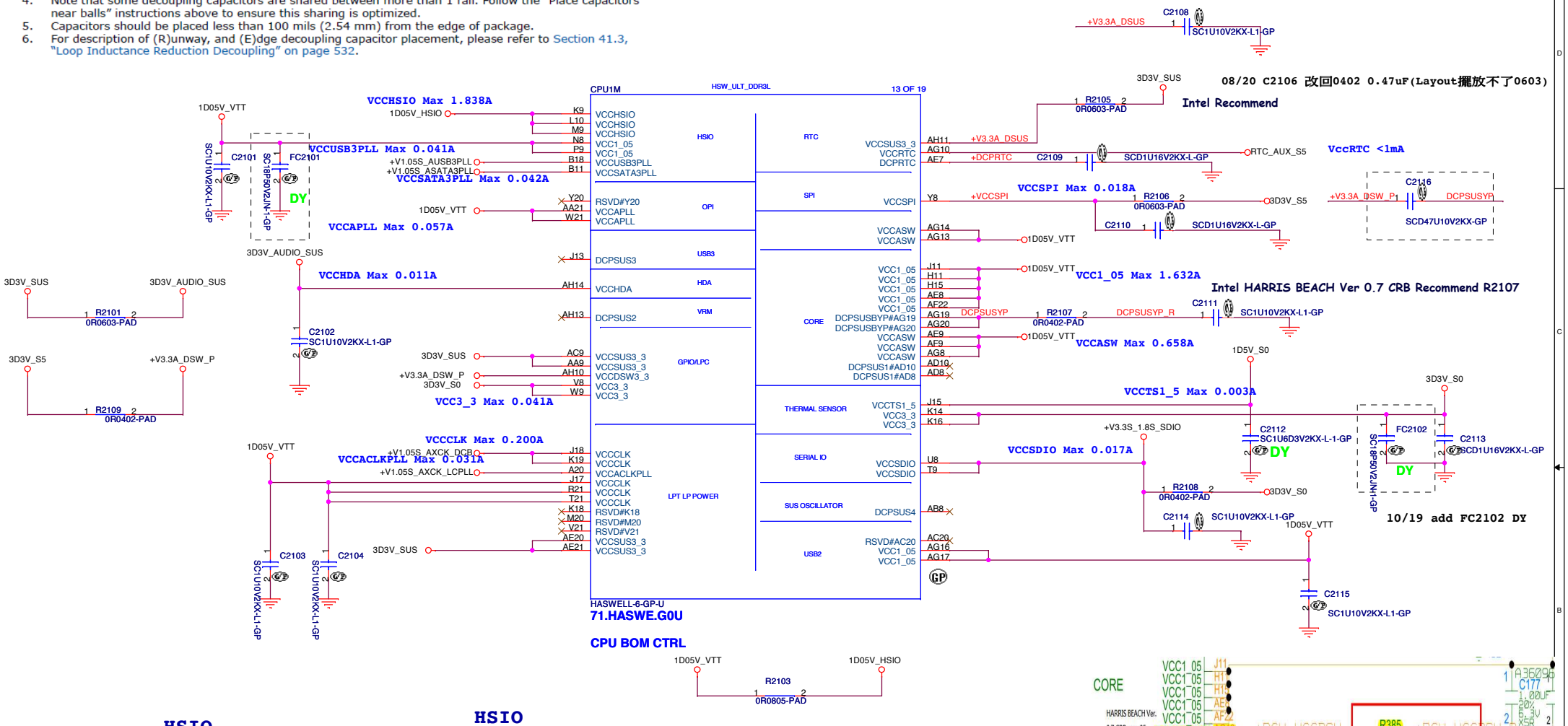
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/MISC)
Size: Custom
Document Number: LT41
Rev: -1
Date: Tuesday, January 20, 2015
Sheet 20 of 102

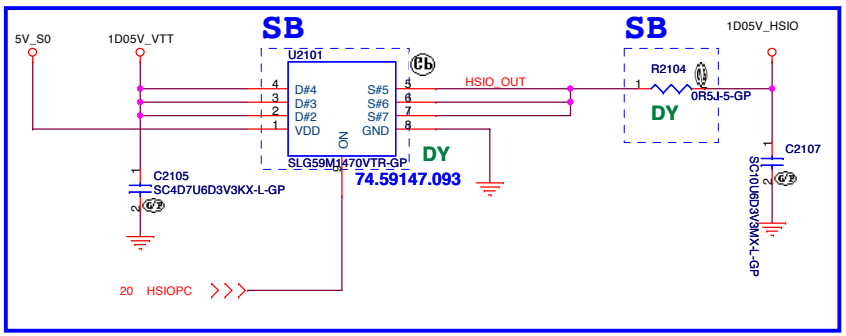
Notes:

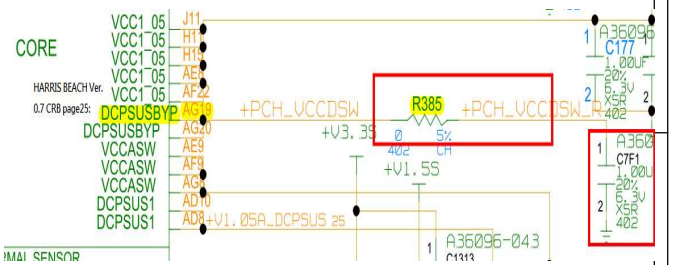
1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.



HSIO

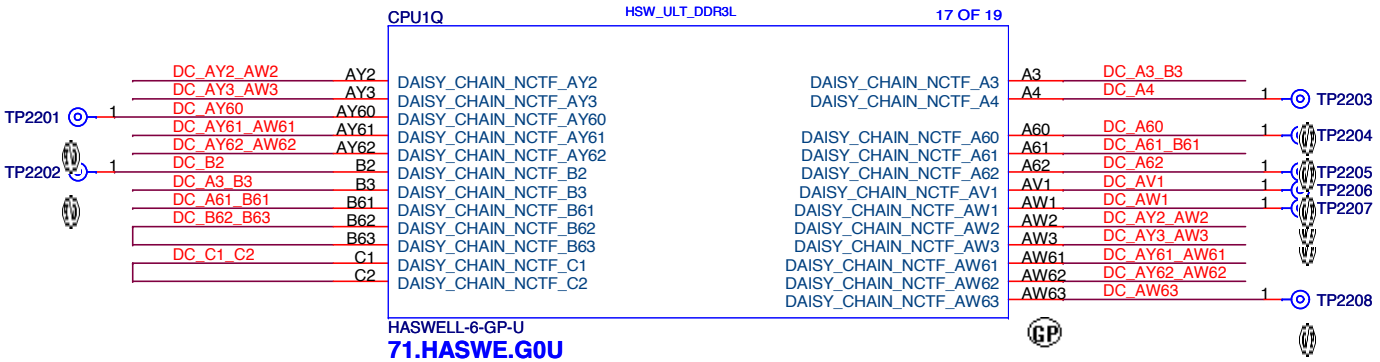
Function LOCATION	HSIO	NON HSIO
U2101	ASM	DY
R2104	ASM	DY
R2103	DY	ASM

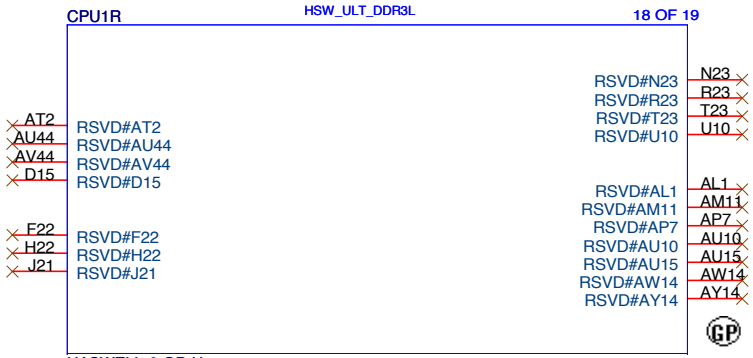




BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU (POWER1)	
Size A3	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 21 of 102	





BOM1

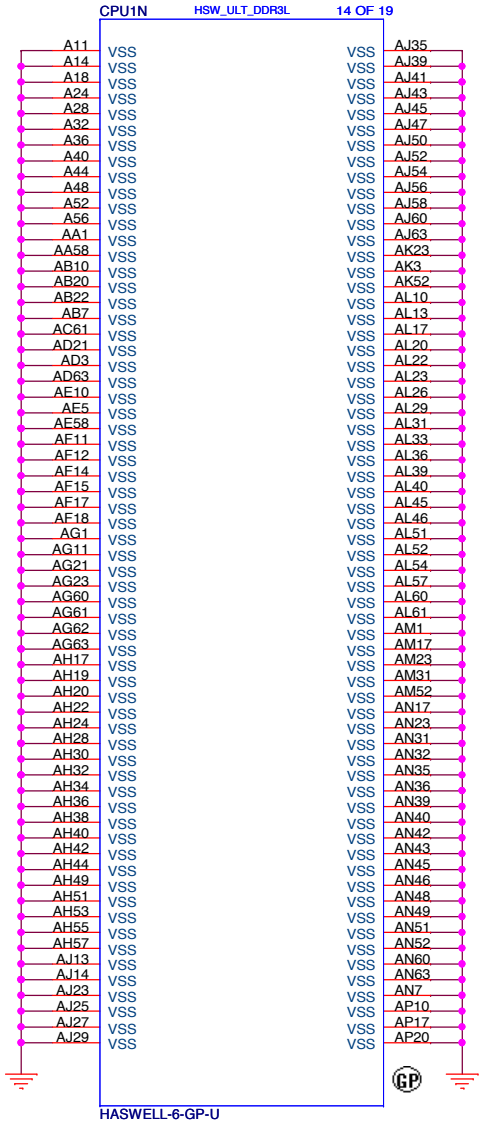
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

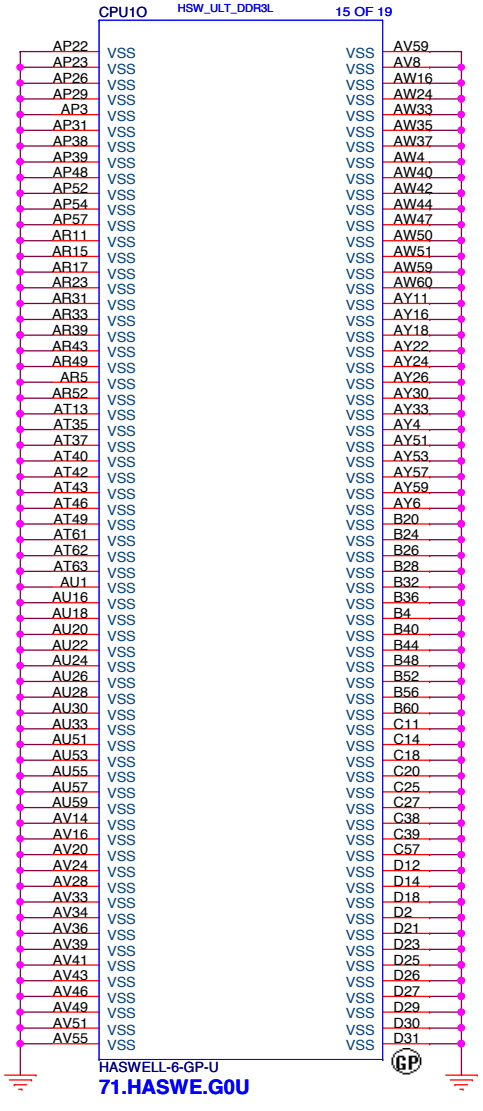
Title: ***CPU (RSVD)***

Size	Document Number	Rev
Custom	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 22 of 102

SSID = PCH





BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
Custom	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 23 of 102

SSID = KBC

Model_ID_BOM Ctrl

MODEL ID

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LT41 Intel Broadwell	100.0K	10.0K	64.10025.6DL	3.0V
LC41 Intel Broadwell	100.0K	20.0K	64.20025.L0L	2.75V
LC51 Intel Broadwell	100.0K	33.0K	64.33025.L0L	2.48V
LT41 Intel Haswell	100.0K	47.0K	64.47025.6DL	2.24V
LC41 Intel Haswell	100.0K	64.9K	64.64925.6DL	2.0V
LC51 Intel Haswell	100.0K	76.8K	64.76825.6DL	1.87V
NA	100.0K	215.0K	64.21535.6DL	1.048V

SPEC: ADT PWR Detection Function V1 3

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

DELTA Model:ADP65FD BB-PD03 ADP

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.663V < ID <= 2.102V	90W
90W	1.172V < ID <= 1.618V	90W
65W	0.693V < ID <= 1.134V	65W
45W	0.214V < ID <= 0.663V	45W

SA

Prevent BIOS data loss solution

84.T3906.A11
2nd = 84.T3906.E11

NPCE285G

01/16 R2449,R2454,R2455,R2456,R2498 Change to Short PAD

NOTE: Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

NOTE: Locate resistors R2415 and R2417 close to the U2401.

06/26 LT41 USB_CHAR_SEL

KBC PWR supply at PSL mode.

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

06/24 add D2401, 將Novo button 與 Power button 接一起,因KBC PSL 只有4Pin ,所以要讓1 Pin給AOU_IFLG#

12/25 D2401 add 2nd & 3rd Source
2nd = 75.00054.K7D
3rd = 075.00054.0B7D

6/18 U2403 Change Part Number to 71.00285.0A0G (285P)

2013/9/12
GPIO83/SOUT_CR & GPIO87/SIN_CR Need reserved TP for Debug

Reserved AOAC

071.00285.0A0G

R2472 close to Pin103

08/20 Change I2C_GSENSE_INT to 5V_EN ----->
08/12 Change LAN_PWR_ON to GPIO10 ----->
08/12 Change Lid_CLOSE# to GPIO93 ----->
08/05 Sensor Hub ----->
Thermal VD
BATTERY / CHARGER ----->
PCH / GPU N15S / Gsensor /MCT7718
08/05 Sensor Hub ----->
08/05 Sensor Hub ----->
10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN# , not name 互換
06/24 NOVO Button----->
TP----->
06/16 MAX R1717 DY

Nuvoton KBC PSL Power Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):

EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

84.02130.031
2nd = 084.03413.0031
84.2N702.J31

EC_GPIO47 High Active
84.2N702.J31
2nd = 84.2N702.031

EC GPIO PH

08/21 R2430 先DY, 待確認5V_EN, OK,再上件

08/12 R2439 VOL_DOWN_BTN# Change to 3D3V_S0
R2443 VOL_UP_BTN# Change to 3D3V_S0
R2447 SCREEN_ROTATE_LOCK# Change to 3D3V_S0
06/05 add R2447 Pull High for SCREEN_ROTATE_LOCK#

08/20 5V_EN Change to pull high 3D3V_AUX_KBC

06/24 R2464 KBC_NOVO_BTN#_EC Change Net Name to KBC_NOVO_BTN#_EC
06/25 KBC_NOVO_BTN#_EC 種3D3V_AUX_S5, 要改成 3D3V_AUX_KBC
06/05 Delete R2460(DG)
06/25 add R2465 Pull high 3D3V_AUX_S5 to KBC_NOVO_BTN#

EC GPIO PL

(Debug Card Side)
(Main Board Side)
3.3V
KBC
GND
TX
RX
3.3V_S5
(RX) reserved
(RX)
(TX)
(TX) reserved

LF15V Note:
(1) R21= DY R2458(E51_TXD)
(2) R13= DY R2451(E51_RXD)

Nuvoton KBC PSL Logic

Table 11. PSL Operation States

Inputs			Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

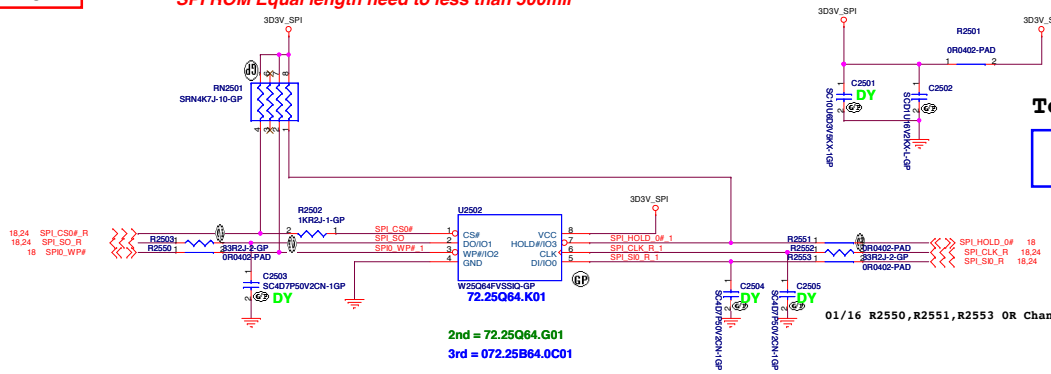
Micrel P/N:74.02782.072

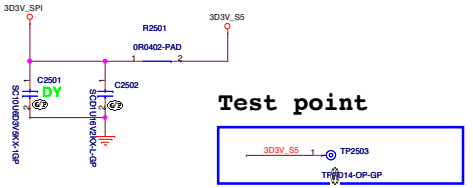
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_NPCE285P
Size: N
Document Number: LT41
Rev: -1
Date: Tuesday, January 08, 2013
Sheet 24 of 102

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil





Test point

01/16 R2550,R2551,R2553 0R Change to Short PAD

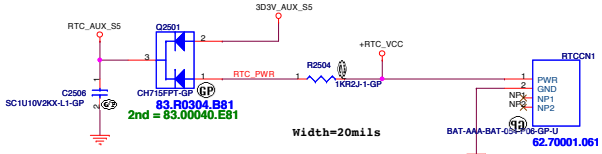
12/24 U2502 3rd Change to 072.25B64.0C01

U2502			
Main	Winbond	W25Q64FV	72.25Q64.K01
SC	GIGADEVICE	GD25B64BSIGR	072.25B64.0001
SD	MICRON	N25Q064A13ESEC0F	72.25Q64.G01

Don't use MXIC 72.25647.00A

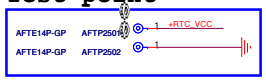
SSID = RBATT

SSID = RBATT

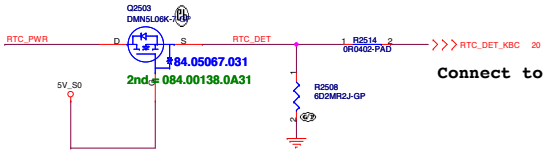


12/22 3rd 62.70001.061 有問題,SVT拿掉

Test point



High Detect
Need to Check whether to PD in PCH Side



Connect to CPU GPIO57

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Flash(KBC+PCH)/RTC***

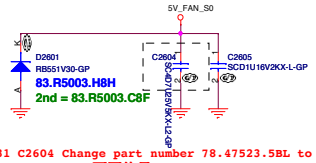
Size: A2 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 25 of 102

SSID = Thermal

Thermal sensor NCT 7718W

Layout 15 mil



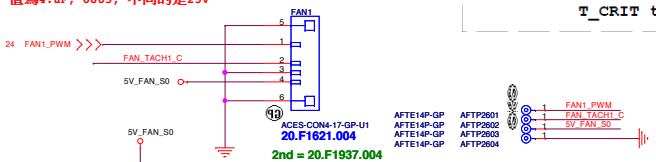
07/31 C2604 Change part number 78.47523.5BL to 78.47522.L4L, 值為4.uF, 0805, 不同的是25V

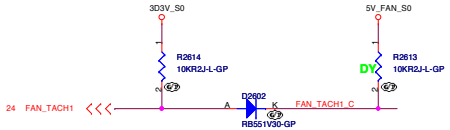
ALERT# /T_CRIT# Pull-up Resistor

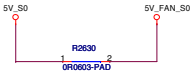
R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

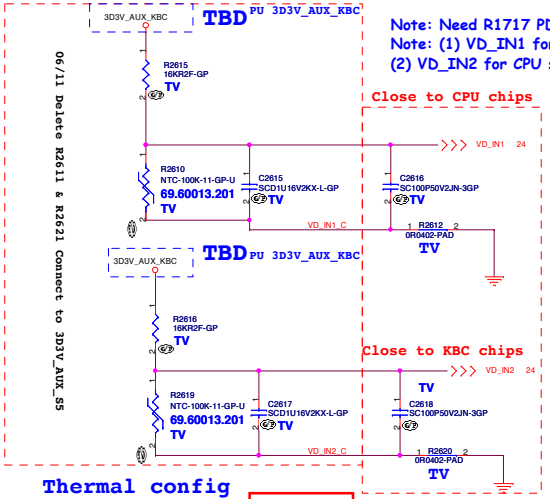






2.System Sensor, Put on palm rest

Close to Thermal sensor



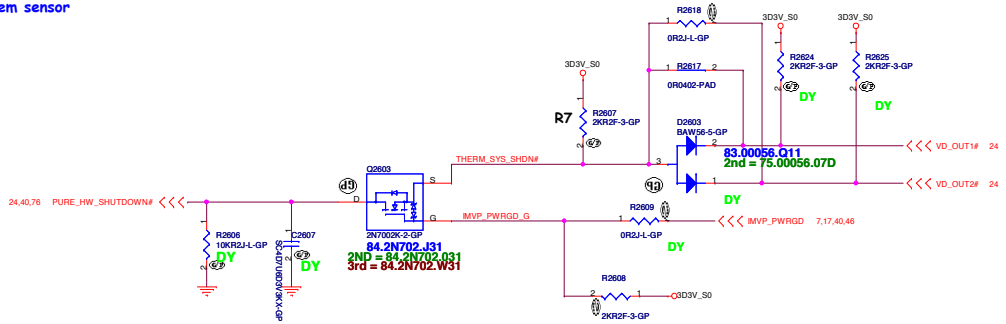
Close to CPU chips

Close to KBC chips

Note: Need R1717 PD: Enable Thermal VD Fun.
Note: (1) VD_IN1 for System sensor
(2) VD_IN2 for CPU sensor

T8=85 degree

10/27 R2617 DY改上件
DY 12/18 R2617 Change to Short PAD



Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
R1717	ASM	DY

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

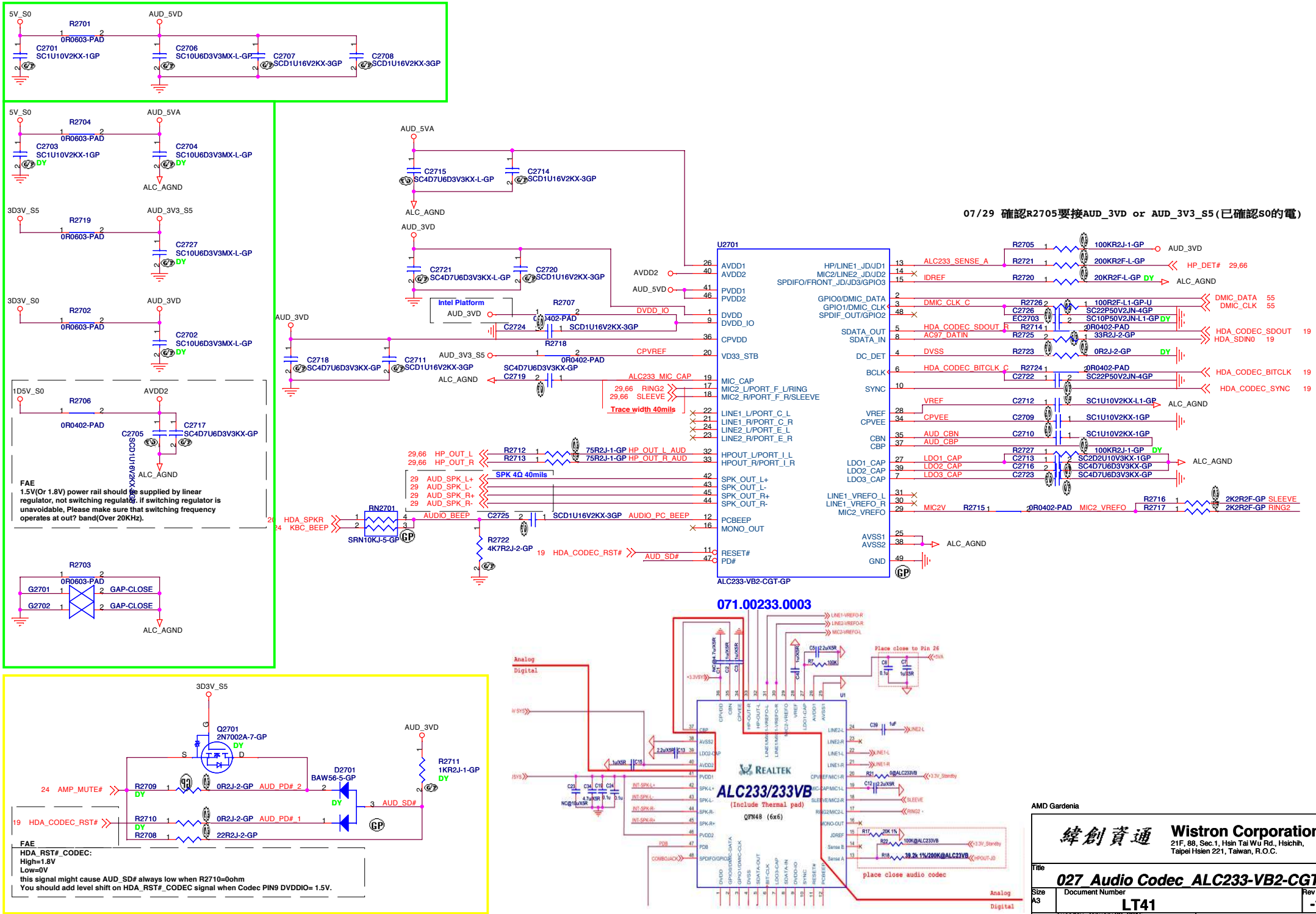
Size: A2 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 26 of 102

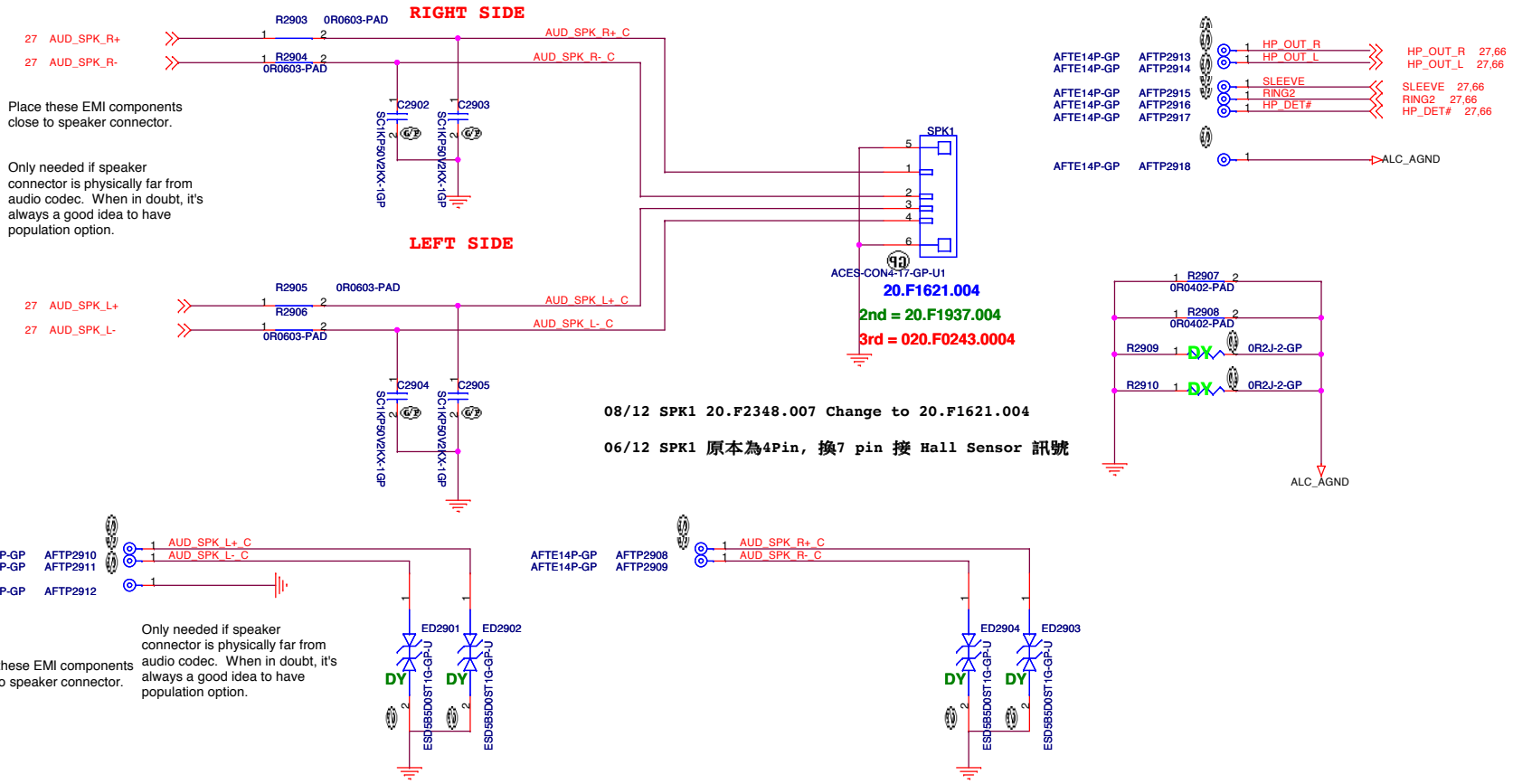
ALC233-VB2-CGT

07/29 確認R2705要接AUD_3VD or AUD_3V3_S5(已確認S0的電)

071.00233.0003

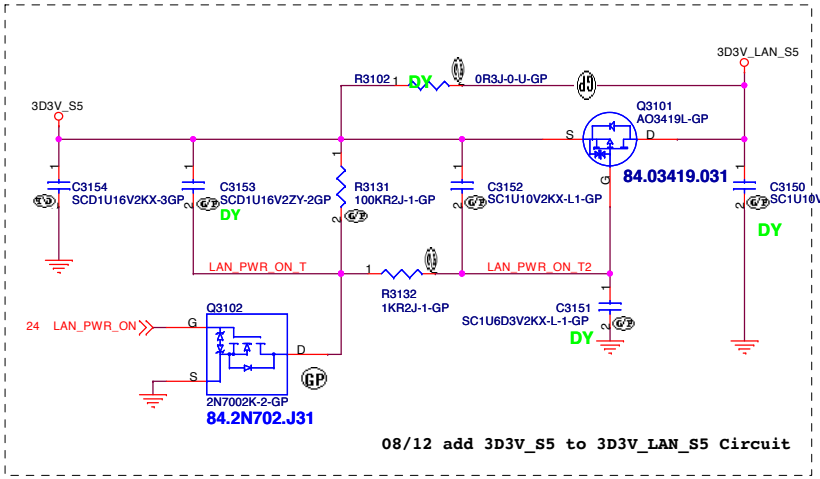


INTERNAL STEREO SPEAKERS

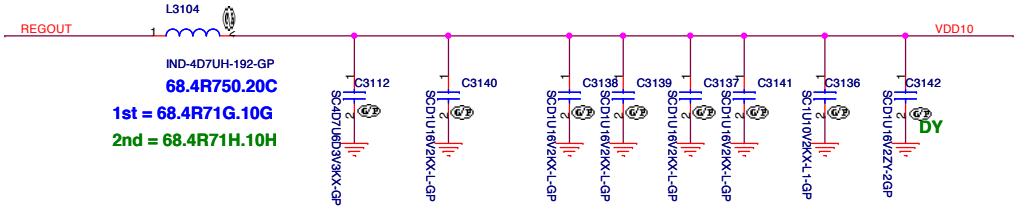


BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MIC/SPEAKER/AUDIO JACK		
Size: Custom	Document Number: LT41	Rev: -1
Date: Tuesday, January 20, 2015	Sheet 29 of 102	

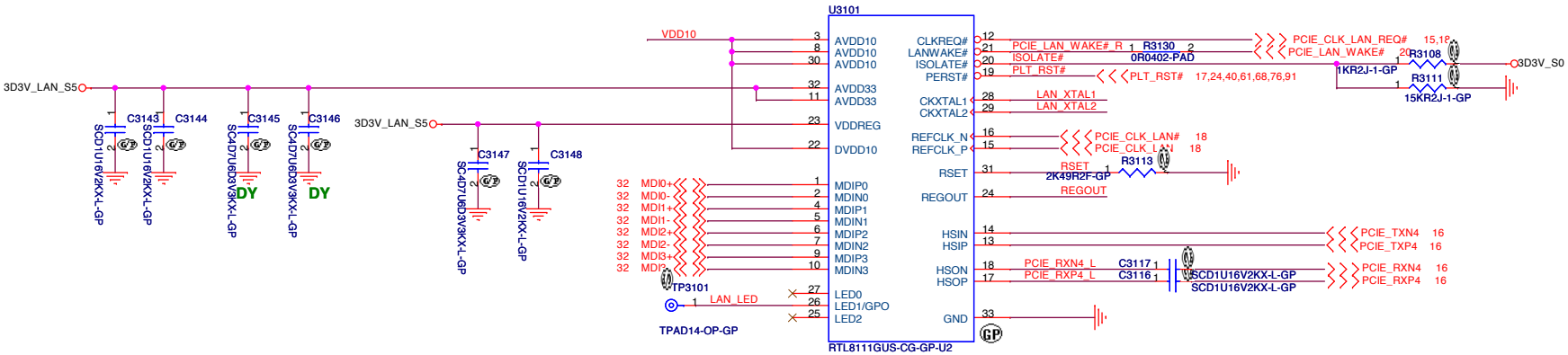


12/22 L3104 add 2nd& 3rd Source, 1st 已為禁用,但之前沒有其他Source,所以先導,量產拿掉



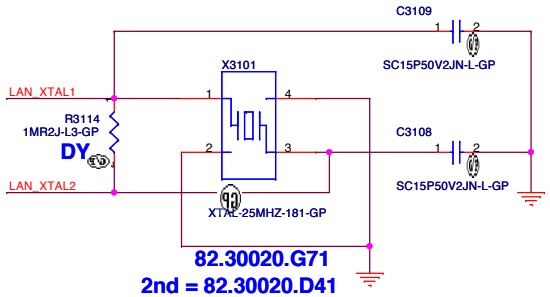
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3138 to C3141 close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C20 and C21 close to each VDD10 pin-- 22 (Reserved)



Change LAN PN to 20200540

25MHz XTAL



Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

LAN and Transformer Config:

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8111GUL

Size	Document Number	Rev
A3	LT41	-1

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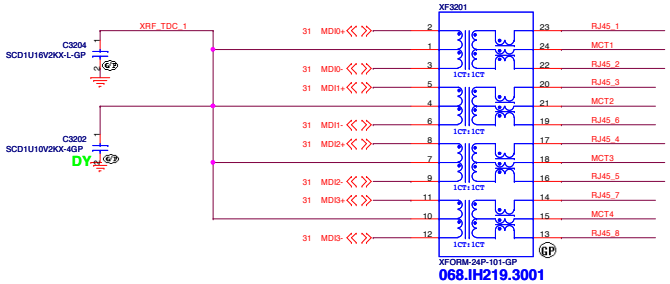
10/100M/1000M Lan Transformer



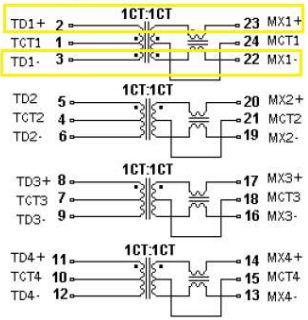
068.IH219.3001
2nd = 68.89240.30D

1000M Lan Transformer pin define

Part Number	Insertion Loss (dB Max) 1-100MHz	Return lo (dB MIN @1
		1-30 40 50 60
IH-106-A	-1.0	-18 -14.4 -13.1

SCHEMATICS :

Pin Define



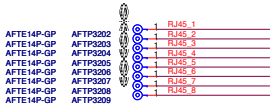
LAN and Transformer Config:

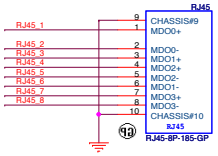
12/18 3rd 068.24101.3041 是Wendell的料,EMI測試不過,所以拿掉
12/18 2nd 68.89240.30D 為要成料,新導入,(原本為68.89246.301)

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

1000M Transformer PN:
068.01010.3001 (AZ chip)

LAN Connector





022.10001.00A1
2nd = 022.10001.0E71

06/13 Delete LAN_AGND

08/13 RJ45 22.10019.141 Change to 022.10001.00A1

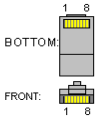
AZ&NON AZ

Function LOCATION	AZ	NON AZ
ED3102	DY	ASM
R3114	DY	ASM
ED3103	ASM	DY
ED3104	ASM	DY
ED3105	ASM	DY
ED3106	ASM	DY
ED3107	ASM	DY
ED3108	ASM	DY
R3112	ASM	DY
R3115	ASM	DY
R3116	ASM	DY
R3117	ASM	DY
R3118	ASM	DY
R3119	ASM	DY
R3120	ASM	DY

RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

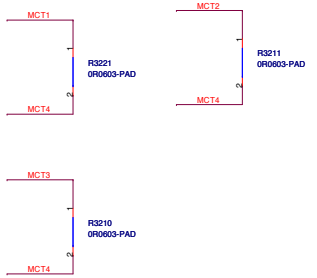
The connector is 8 pin RJ45 (8P8C) male

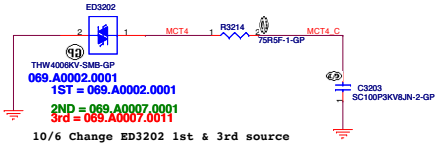


The associated connector is 8 pin RJ45 (8P8C) female

10/100/1000 LAN surge circuit

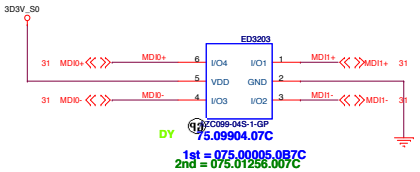
For test stuff

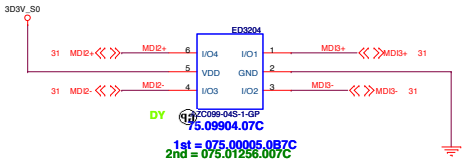




069.A0002.0001
1ST = 069.A0002.0001
2ND = 069.A0007.0001
3rd = 069.A0007.0011

10/6 Change ED3202 1st & 3rd source





8/25 將ED3203,ED3204 屬性ESD STUFF OPTION 改成DY, 上件會無法Wake on Lan

10/13 ED3203,ED3204 改成跟ED3501一樣, 增加三個Source

10/23 將3rd Source拿掉 75.09904.07C, 因為已有案子50米網線測不過(Part number跟ED3501一樣,BOM別帶錯)

10/23 ED3203, ED3204 ESD STUFF OPTION改 DY,不上件

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONNECTOR

Size	Document Number	Rev
A2	LT41	-1

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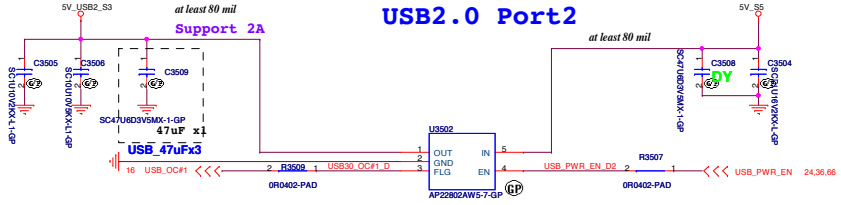
USB2.0 Port2

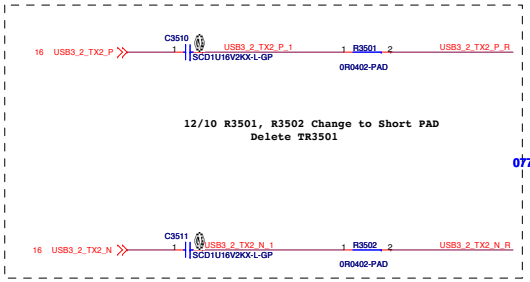


074.22802.009F
1st = 074.00524.0B9F
2nd = 74.06288.07F

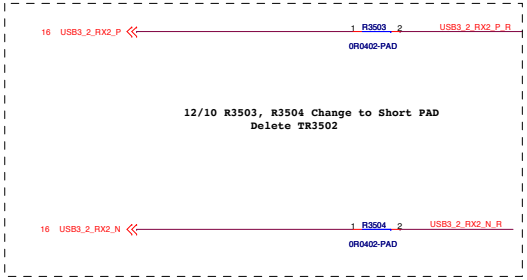
08/05 U3502 add 2nd & 3rd Source
12/18 074.22802.009F 被禁用

12/22 增加AFTP3506 測點

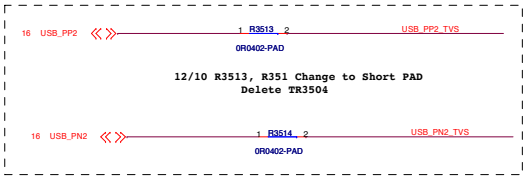
12/24 C3513, C3514 SVT階段,因為EMI問題,先上件1uF 0805,
待測試後,決定是否換回47uF



12/10 R3501, R3502 Change to Short PAD
Delete TR3501

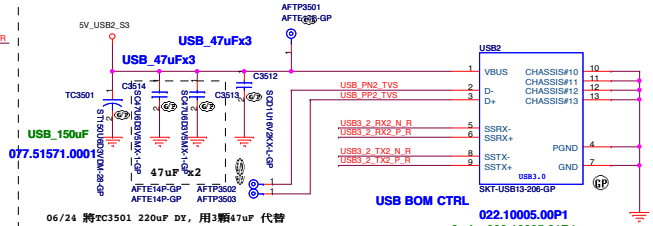


12/10 R3503, R3504 Change to Short PAD
Delete TR3502



12/10 R3513, R351 Change to Short PAD
Delete TR3504

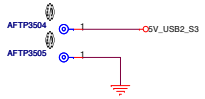
WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



06/24 將TC3501 220uF DY, 用3顆47uF 代替
10/13 220uF Change to 150uF(077.51571.0001)

USB BOM CTRL
022.10005.00P1
2nd = 022.10005.01B1
3rd = 022.10005.00Z1

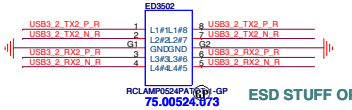
10/23 USB2 改接GND(原本USB3_AGND)
08/12 USB2 Change to 022.10005.00P1



12/23 增加LC41& LC51 USB CONN, 沒附型的CONN
1st 022.10005.01U1
2nd 022.10005.01W1
3rd 022.10005.01V1

EMI Request

12/18 ED3502 Change to DY
12/24 ED3502 Change to ESD STUFF OPTION

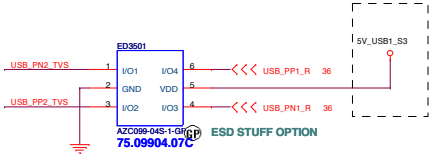


75.00524.073
1st = 075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

ESD STUFF OPTION

06/25 ED3501 VDD change Net Name to 5V_USB1_S3

12/24 ED3501 只導1st 075.00005.0B7C, 其他2nd & 3rd 不導入,會有Wake up 不起來的風險



ESD STUFF OPTION
75.09904.07C
1st = 075.00005.0B7C
2nd = 075.01256.007C
3rd = 075.09904.0A7C

10/28 1st 75.00005.C7C改為 075.00005.0B7C
6/17 ED3501 Change Part Number to 75.09904.07C
與 ED3602 合併,共用一顆ESD

12/18 ED3501 EMI說075.00005.0B7C 測試不過,要用075.01256.007C,
但2nd & 3rd Source 會有S3 Wake UP 不起來的風險,待討論

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 CONN

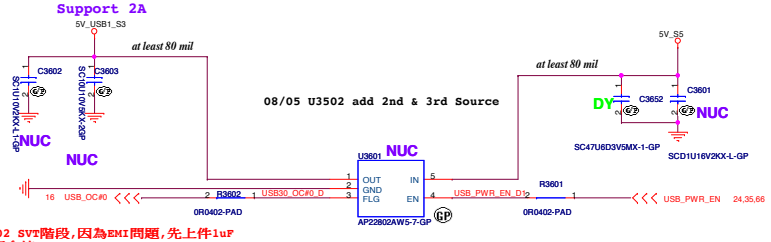
Size	Document Number	Rev
A2	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 35 of 102

UC, UC_ST, DY_UC_TI不上件

USB3.0 Port1

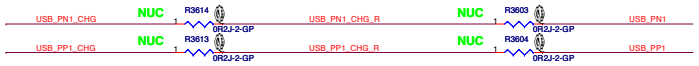
Support 2A



12/24 C3603, C3602 SVT階段,因為EMI問題,先上件1uF
待測試後,決定是否拿掉

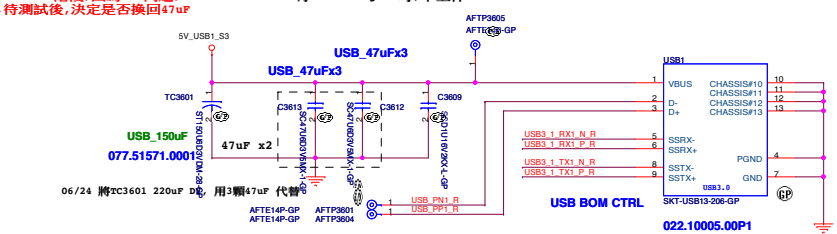
074.22802.009F

1st = 074.00524.0B9F
2nd = 74.06288.07F



12/24 C3612, C3613 SVT階段,因為EMI問題,
先上件1uF 0805,待測試後,決定是否換回47uF

06/12 NUC 有USB Charger 時,不上件



06/24 將TC3601 220uF D值, 用3顆47uF 代替

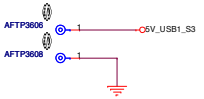
10/23 USB1 改接GND(原本USB3_AGND)

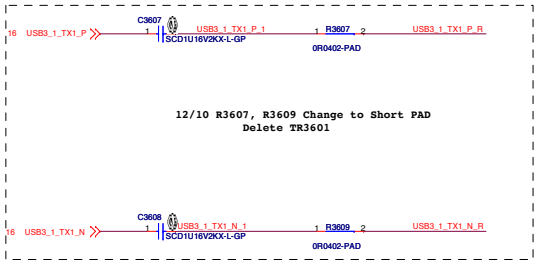
022.10005.00P1
2nd = 022.10005.01B1
3rd = 022.10005.00Z1

10/13 220uF Change to 150uF(077.51571.0001)

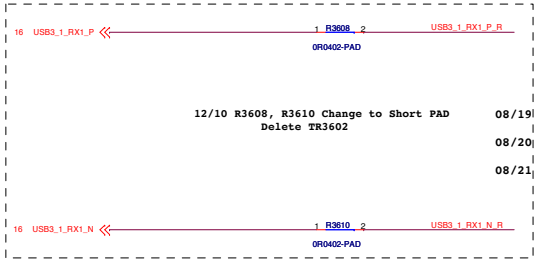
12/23 增加LC41& LC51 USB CONN, 沒附型的CONN
1st 022.10005.01U1
2nd 022.10005.01W1
3rd 022.10005.01V1

08/12 USB1 Change to 022.10005.00P1





12/10 R3607, R3609 Change to Short PAD
Delete TR3601



12/10 R3608, R3610 Change to Short PAD
Delete TR3602

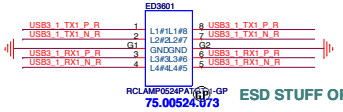
12/10 R3611, R3612 Change to Short PAD
Delete TR3603

08/19 TR3602 Change to ZZ.00CMC.006

08/20 add Pin5,6 USB3_1_RX1_P_R & USB3_1_RX1_N_R

08/21 Change to 69.10171.001(不用ZZ.00CMC.006)

EMI Request



75.00524.073

ESD STUFF OPTION

1st = 075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

12/18 ED3601 Change to DY

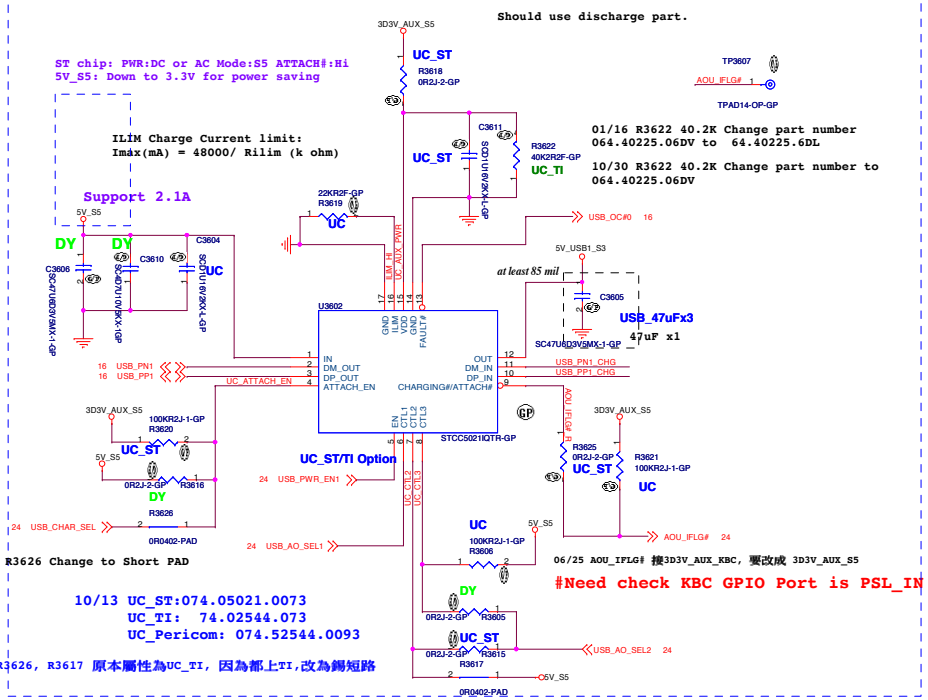
12/24 ED3601 Change to ESD STUFF OPTION

EMI Request

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB charger

Should use discharge part.



STCC5021 Truth Table

12/18 R3617 Change to Short PAD

Table 5. Truth table control pins CTLx

Host state	CTL1	CTL2	CTL3	Mode description
S0, S1	1	1	1	CDP BC1.2 with charging detection.
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

Table 3 can be used as an *aid* to program the TPS2544 per system states however not restricted to below settings only.

Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2544 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

M40

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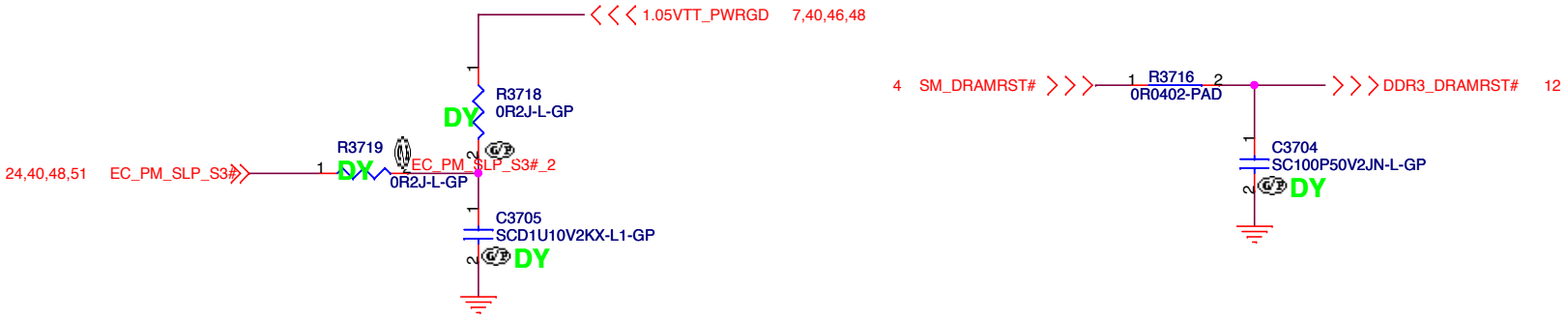
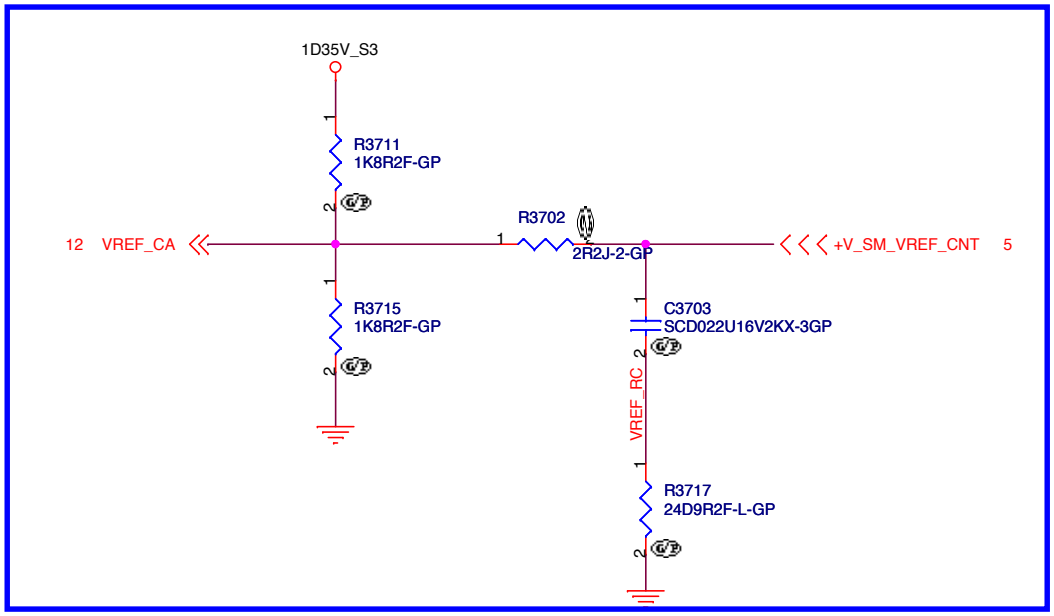
Title: USB 2.0 / 3.0 Port

Size: A2 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 36 of 102





For Intel Recommend Close to DIMM

BOM1

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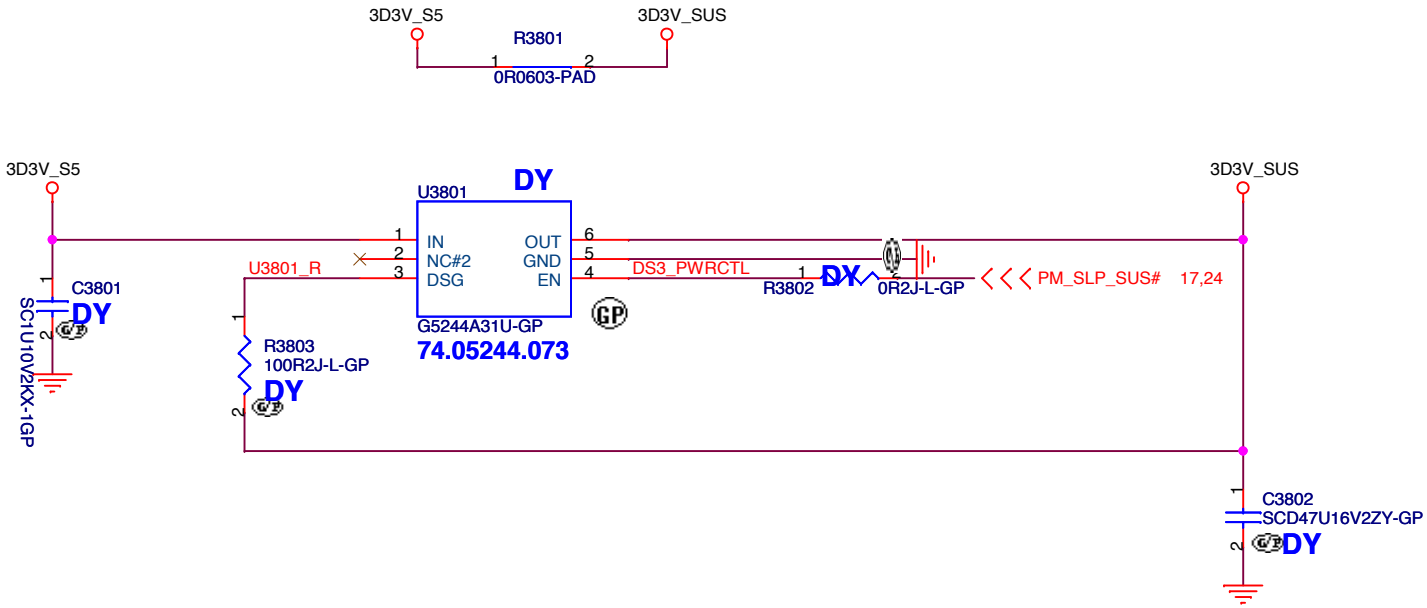
Title
ADAPTER OCP / S3 reduction

Size	Document Number	Rev
Custom	LT41	-1
Date: Tuesday, January 20, 2015	Sheet 37 of 102	

DS3

Function LOCATION	DS3	NON DS3
R3801	DY	ASM
R1712	DY	ASM
R1709	DY	ASM
R1714	DY	ASM
C3802	ASM	DY
R1713	ASM	DY
R1716	ASM	DY
R2444	ASM	DY
R2446	ASM	DY
R2487	ASM	DY
R3802	ASM	DY
R3803	ASM	DY
U3801	ASM	DY
C3801	ASM	DY



BOM1

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Title: ***(Reserved)***

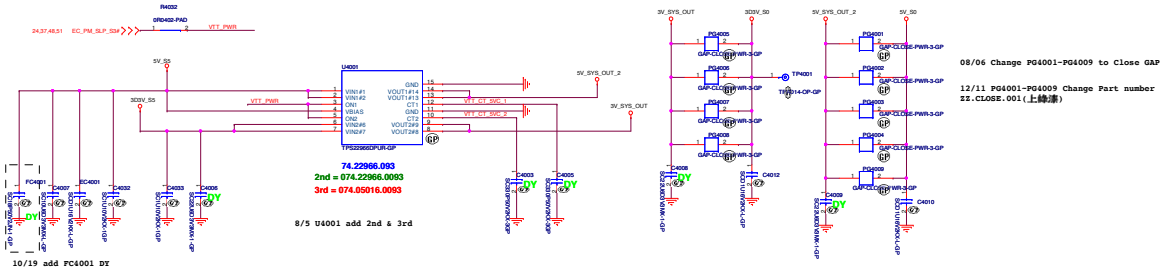
Size	Document Number	Rev
A4	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 38 of 102

Power Sequence

12/18 R4001 Change to Short PAD

Run Power



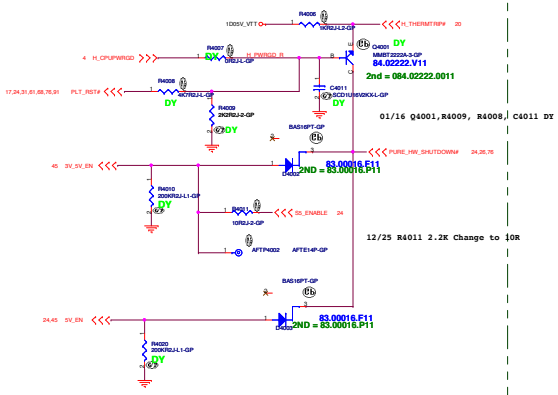
8/5 U4001 add 2nd & 3rd

10/19 add FC4001 DY

08/06 Change PG4001-PG4009 to Close GAP

12/11 PG4001-PG4009 Change Part number
ZZ.CLOSE.001(上錦凍)

Discharge circuit

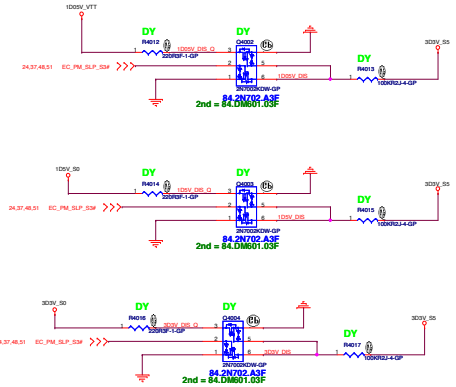


01/16 Q4001,R4009, R4008, C4011 DY

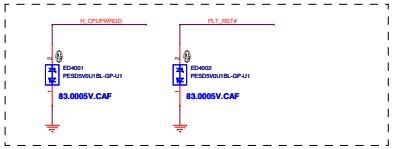
12/25 R4011 2.2K Change to 10R

08/21 add R4020, D4003 For 5V_EN,待驗證

10/15 D4003 改為上件



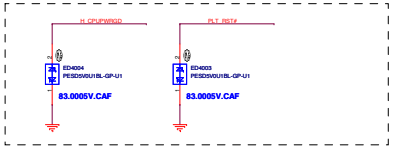
10/17 Delete 放電線路



10/16 add ED4001, ED4002

10/27 EMI上錯料,(083.00105.00AF)才是對的, 先把原來的DY

12/18 ED4001, ED4002 change Part Number to 83.0005V.CAF



12/18 add ED4003, ED4004 83.0005V.CAF

BOM#

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

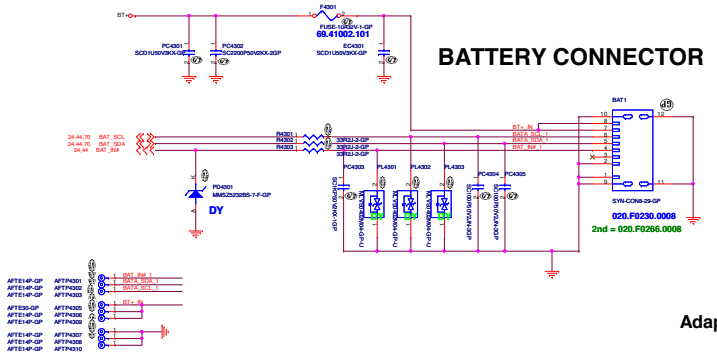
Title: Power Plane Enable & SEQUENCE

Size: A3 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 26, 2010 | Sheet 45 of 50

12/25 F4301 change Part Number 69.41002.101(原本69.42002.031)

BATTERY CONNECTOR



Connector Pin Alignment(Vendor：Suyin,Aces)

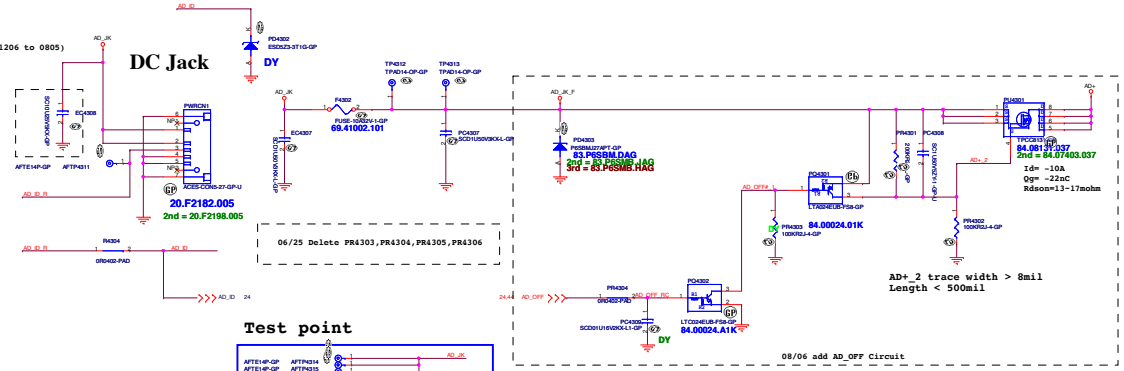
Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

Adaptor in to generate DCBATOUT

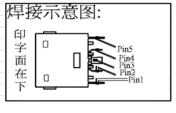
08/01 EC4308 Change part number 78.10622.L5L to 78.10622.51L(1206 to 0805)

DC Jack

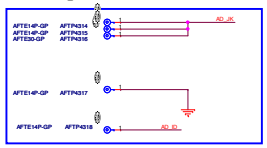


MB_Side		Cable
		Max. Current
Pin 1	AD_JK_F	UL10064AWG28# (3A)
Pin 2	AD_JK_F	UL10064AWG28# (3A)
Pin 3	AD_ID	UL10064AWG28# (3A)
Pin 4	GND	UL10064AWG26# (3.8A)
Pin 5	GND	UL10064AWG26# (3.8A)

焊接示意图:



Test point



BOM1

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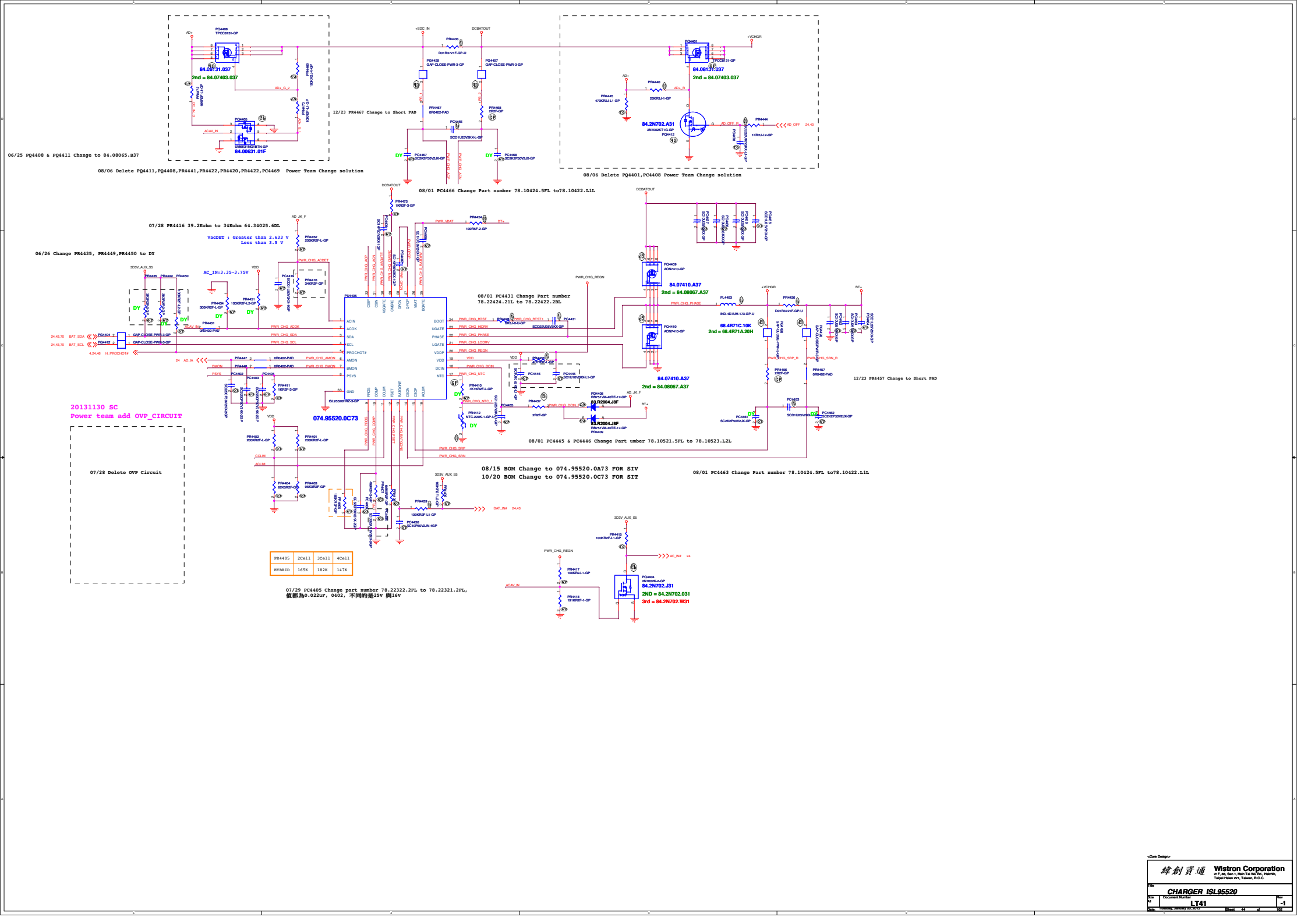
Title: **DCIN JACK & BATT Conn**

Size: D | Document Number: LT41 | Rev: -1

Date: Tuesday, January 08, 2013 | Sheet 48 of 102



<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL95520

Size	Document Number	Rev
A3	LT41	-1

Date: Tuesday, January 26, 2010 Sheet 44 of 102

08/20 add 5V_EN

08/20 PR4501 Change to DY,待實驗確認是否沒問題後,再決定是否3D3V, 5V_EN可分開

10/15 PR4501 原本為0R,改為錫短路ZZ.00RES.021
PR4507 原本為錫短路ZZ.00RES.021,改為0R

12/18 PR4501,PR4502 Change to Short PAD

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(上綠漆)

08/06 Change to Close GAP

12/11 Change Part number ZZ.CLOSE.001(上綠漆)

08/06 Change to Close GAP

10/17 Delete Close GAP

Design Current=3.1A
OCP <6.2A

Design Current=6.4A
OCP < 12.8A

84.07410.A37
2nd = 84.08067.A37

68.3R310.20V
2nd = 68.3R31A.10V

68.2R21A.20B
2nd = 68.2R21B.10J

77.52271.09L
2nd = 77.92271.03L

074.51275.0073

SC BOT
ASM_RES_PAD_DY

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

12/22 增加AFTP4501 測點

06/16 PU4501 Change Part Number from TPS51275 to RT6575B (074.06575.0043).
06/17 PU4501 Change Part Number from RT6575B to TPS51275 (074.51275.0073)

<Core Design>

緯創資通 Wistron Corporation
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Title: TPS51275 5V/3D3V

Size: A2 | Document Number: LT41 | Rev: -1

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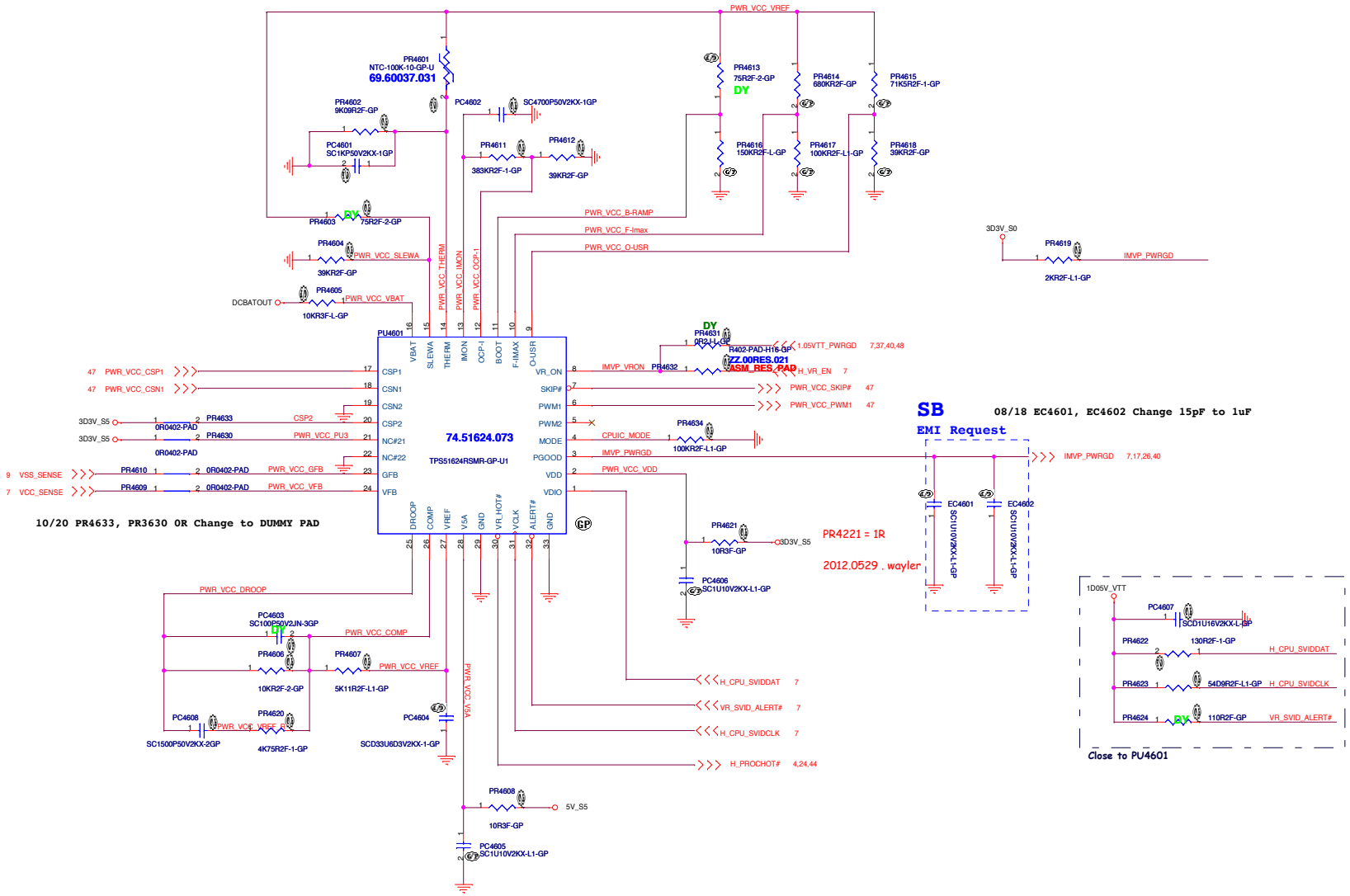
SSID = CPU.Regulator



<Core Design>

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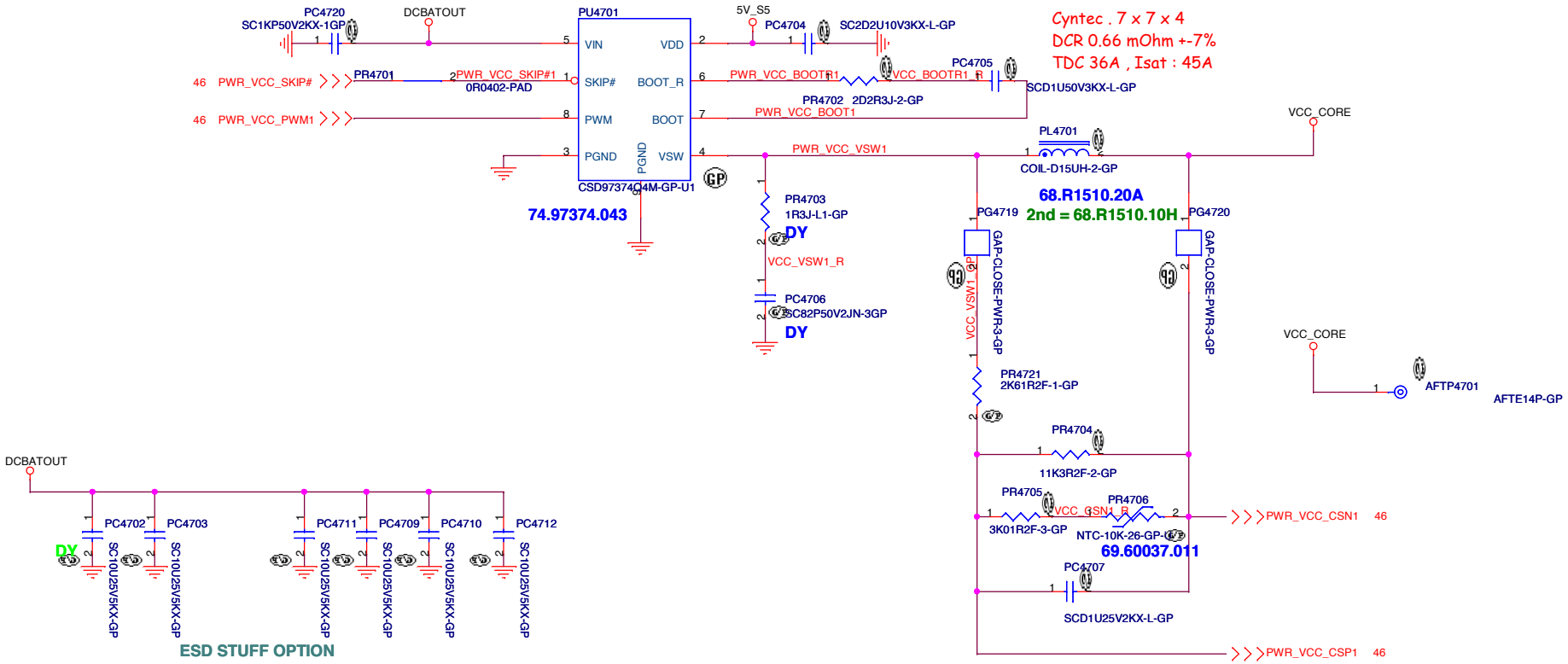
Title: TPS51624_CPUCORE(1/2)

Size	Document Number	Rev
C	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 46 of 102



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51624_CPUCORE(2/2)***

Size	Document Number	Rev
B	LT41	-1

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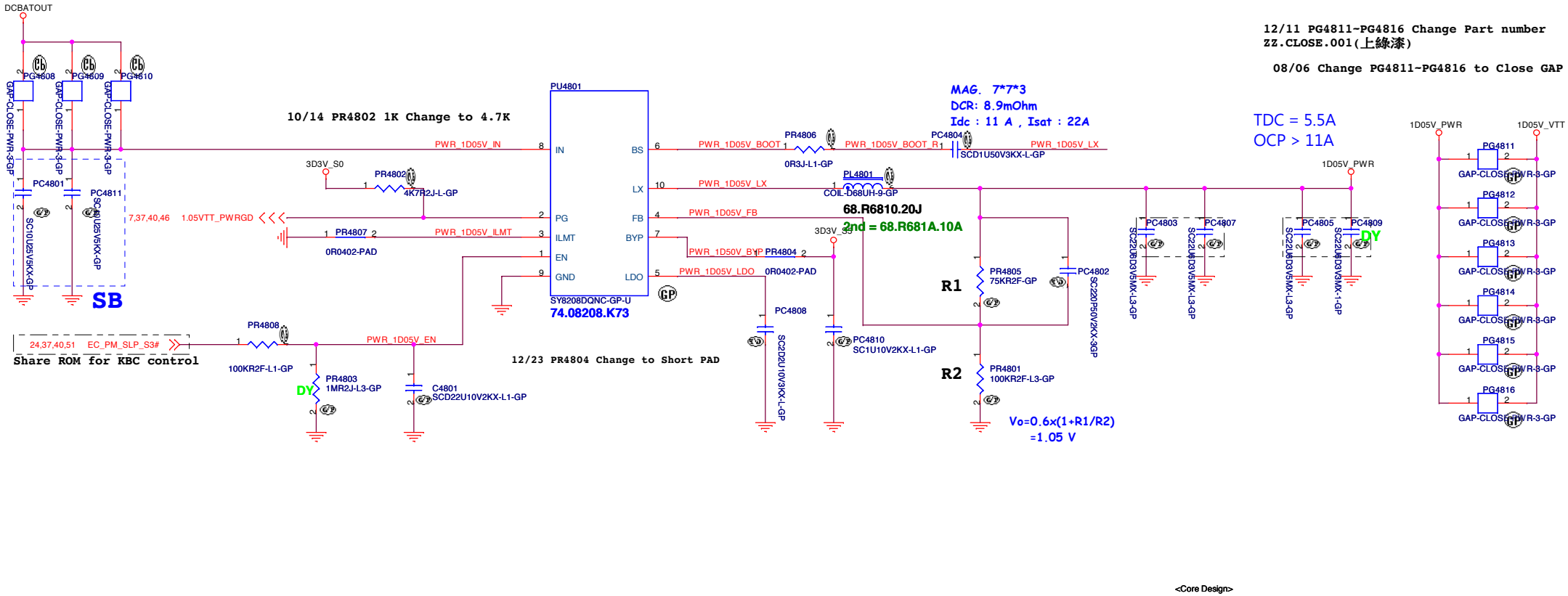
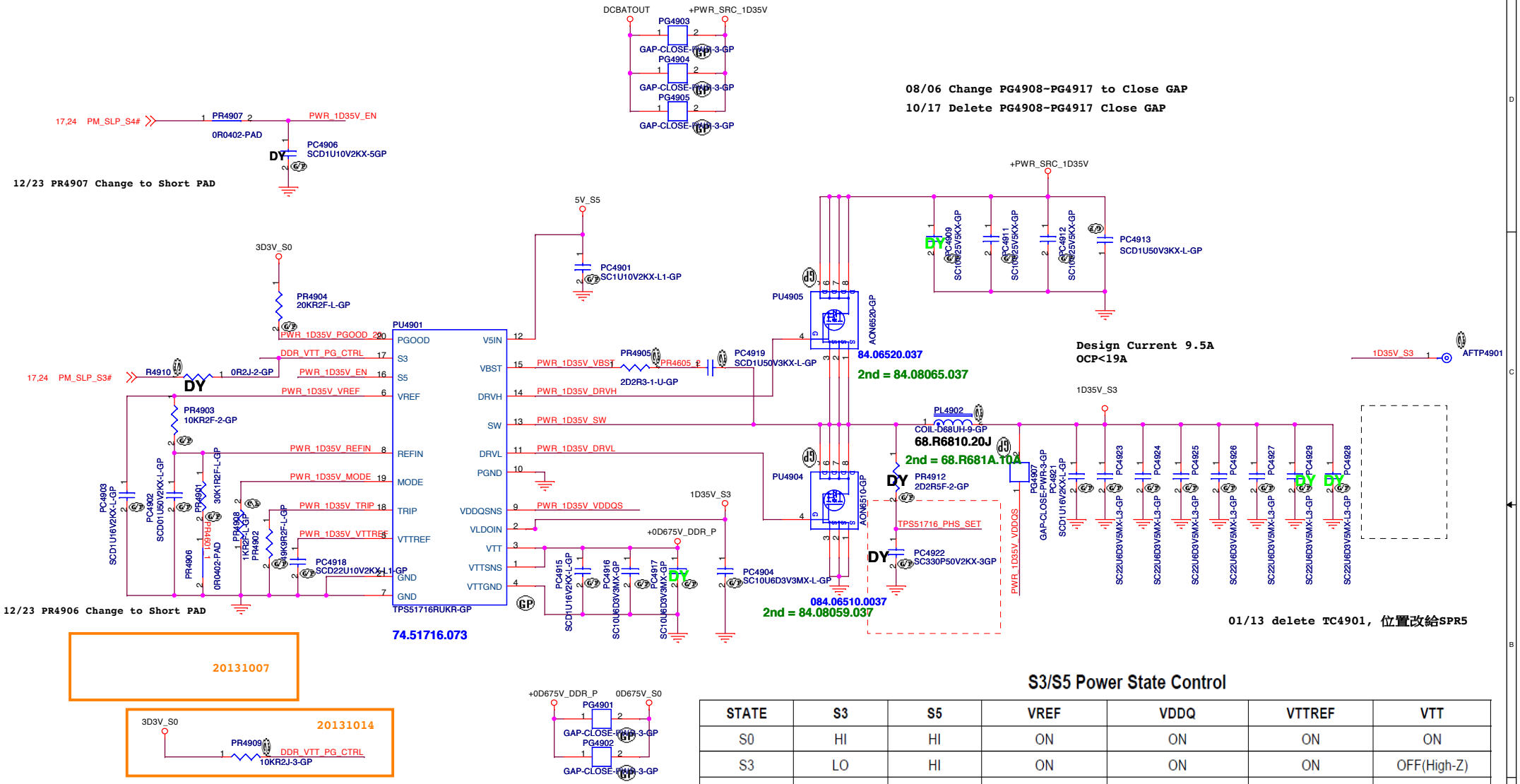
SY8208D for 1D05V



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC to DC_1D05V(SY8208)		
Size: A3	Document Number: LT41	Rev: -1
Date: Tuesday, January 20, 2015	Sheet 48 of 102	

SSID = PWR.Plane.Regulator_1p35v0p675v



S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	33	D-CAP2	500	Non-Tracking
2	22		670	
1	12		670	Tracking
0	1		500	

<Core Design>

緯創資通 Wistron Corporation
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Title: TPS51716(VDDQ_VTT)

Size	Document Number	Rev
A3	LT41	-1

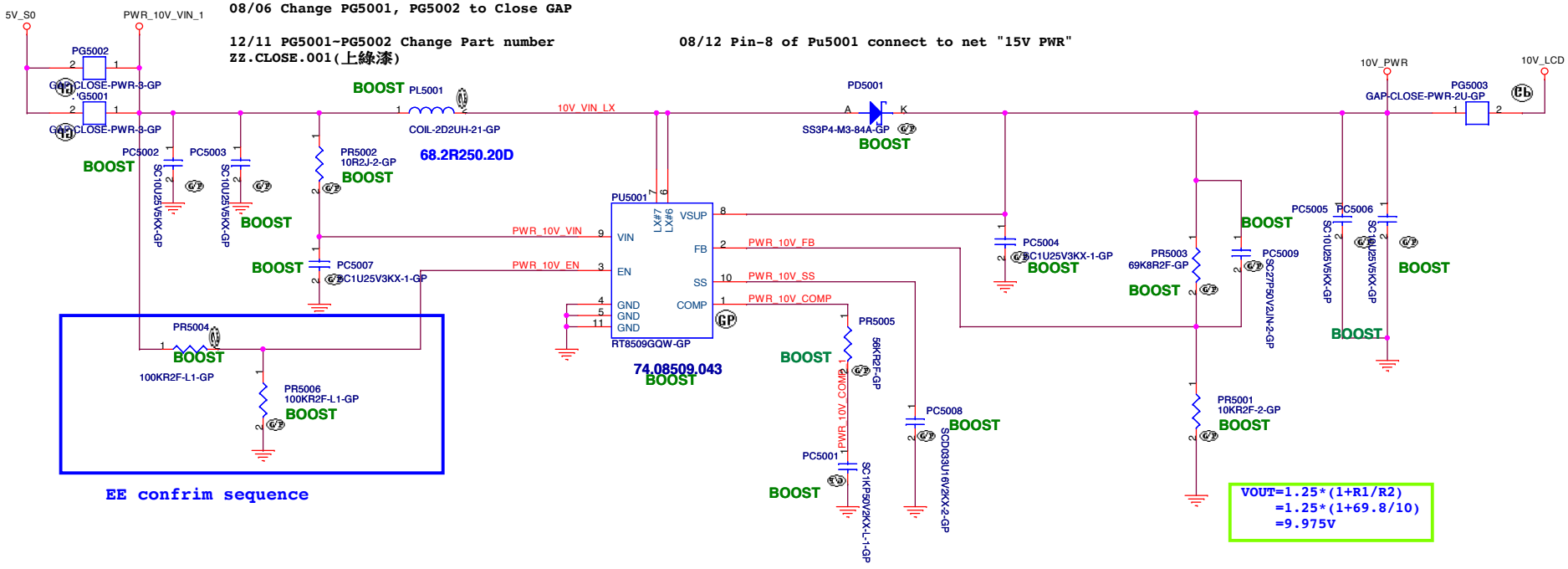
Date: Tuesday, January 20, 2015 Sheet 49 of 102

08/19 Change PL5001 4.7uH to 2.2uH

08/06 Change PG5001, PG5002 to Close GAP

12/11 PG5001-PG5002 Change Part number
ZZ.CLOSE.001(上綠漆)

08/12 Pin-8 of Pu5001 connect to net "15V PWR"



EE confrim sequence

08/19 PR5003 Change 110K to 69.8K

BOM1

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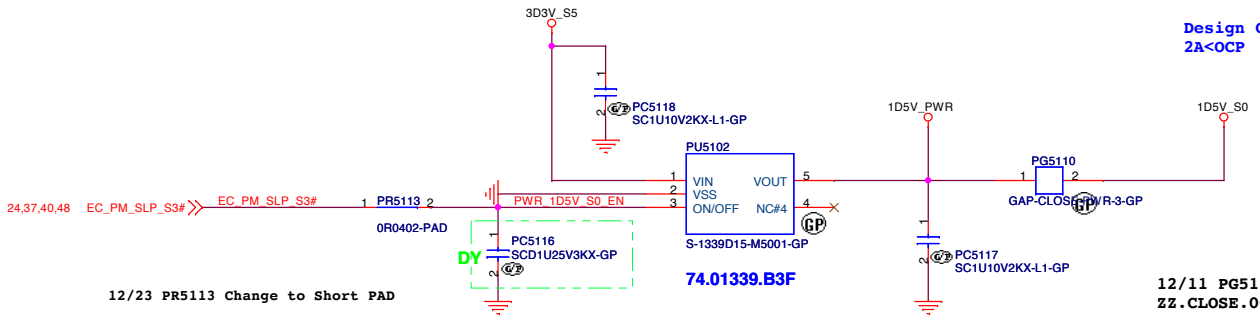
Title: 10V RT8509

Size: A3 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 50 of 102

RT9198 for 1D5V_S0



Design Current = 20mA
2A<OCP

12/23 PR5113 Change to Short PAD

12/11 PG5110 Change Part number
ZZ.CLOSE.001(上綠漆)

10/28 74.09198.B7F(鎖料) 改 74.01339.B3F

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	1D5V_S0 RT9198	
Size A3	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 51 of 102	

BOM1

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Title

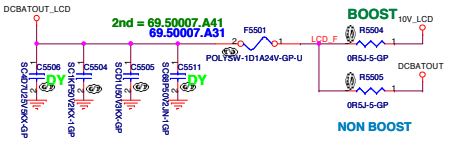
CRT Board Connector

Size	Document Number	Rev
Custom	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 53 of 102

SSID = VIDEO

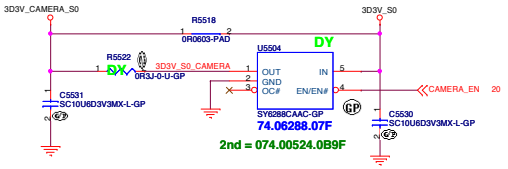
INVERTER POWER



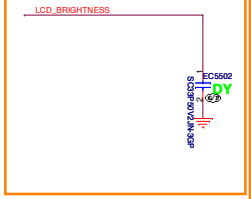
07/04 R5504 BOOST, R5504 NON BOOST

CAMERA POWER

Layout 40 mil

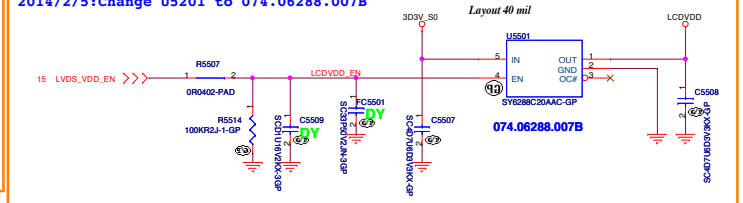


Close to eDP connector

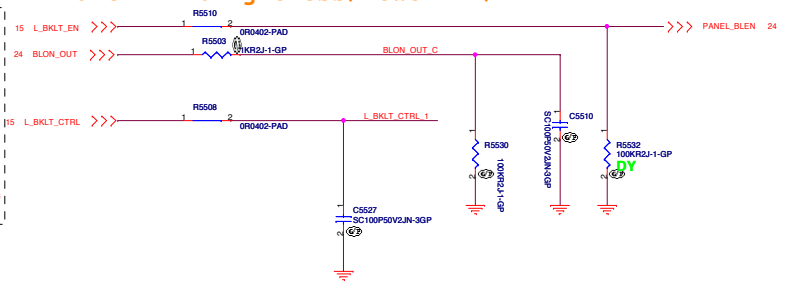


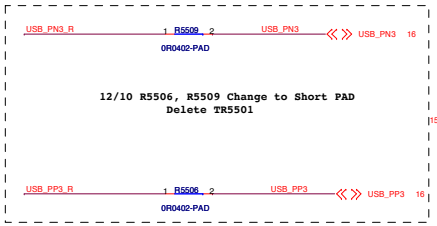
SSID = VIDEO LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

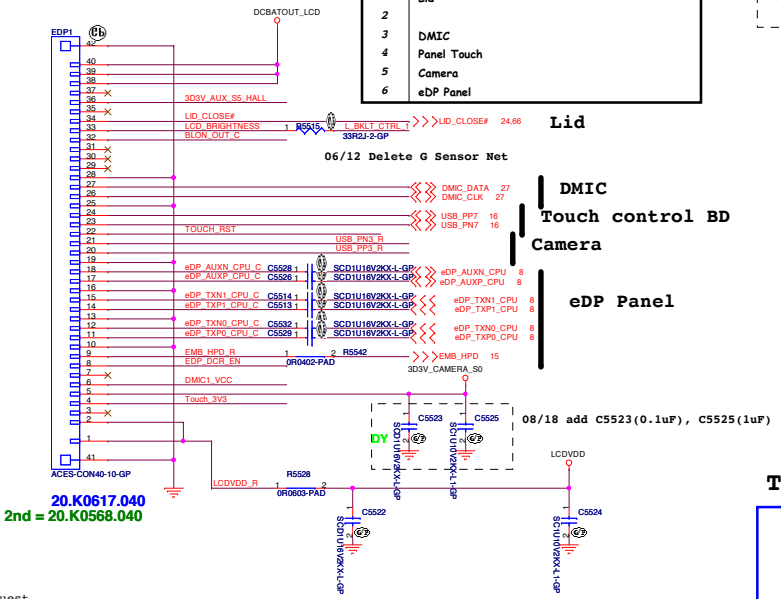


Panel BL brightness/Power En/BL En





eDP connector



eDP Device

Item	Device
1	Lid
2	
3	DMIC
4	Panel Touch
5	Camera
6	eDP Panel

Lid

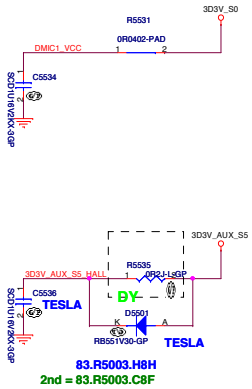
06/12 Delete G Sensor Net

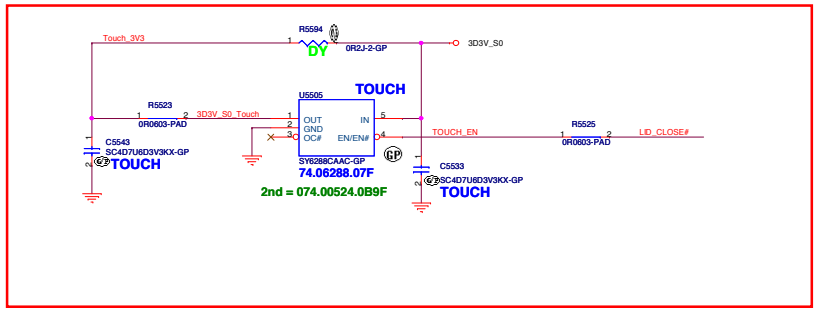
DMIC

Touch control BD

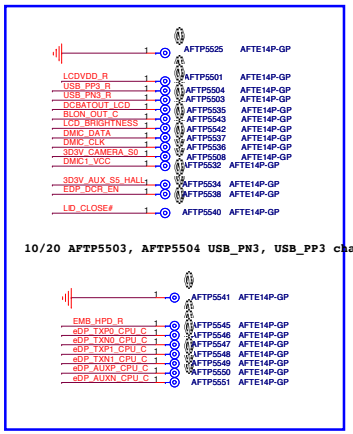
Camera

eDP Panel





Test point



10/20 AFTP5503, AFTP5504 USB_PN3, USB_PP3 change to USB_PN3_R, USB_PP3_R

ESD Request

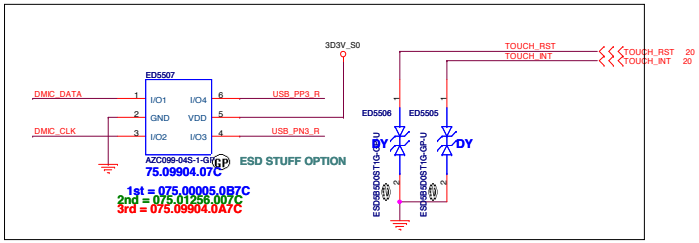
10/16 add ED5507

10/17 change ED5507 從6pin 改為10 pin(EMI要求)

10/20 change ED5507 從10pin 改為6 pin(EMI要求)

12/18 ED5507 Change to DY

12/24 ED5507 Change to ESD STUFF OPTION,
重點: 1st 075.00005.0B7C 在ED5507不導入,
只導 075.01256.007C 及 075.09904.0A7C



M40

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size	Document Number	Rev
A2	LT41	-1

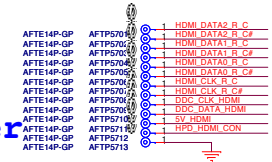
Date: Tuesday, January 20, 2015 Sheet 55 of 102

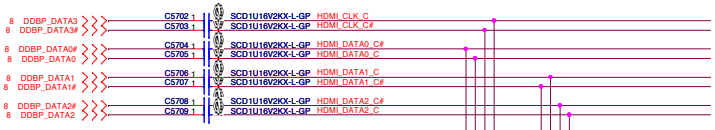
SSID = VIDEO

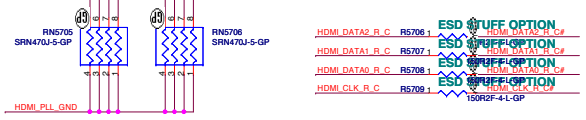
HDMI CONNECTOR

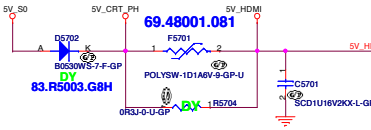
HDMI Passive Level Shifter

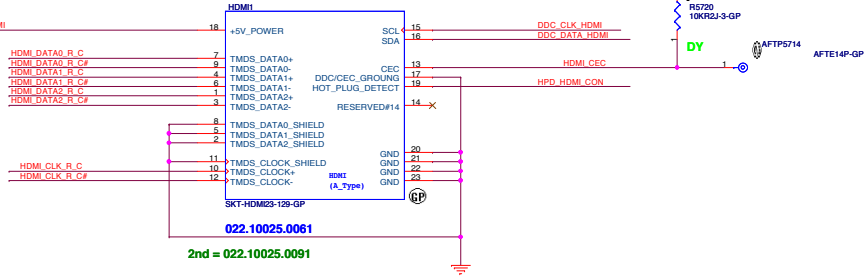
Close to HDMI Connector





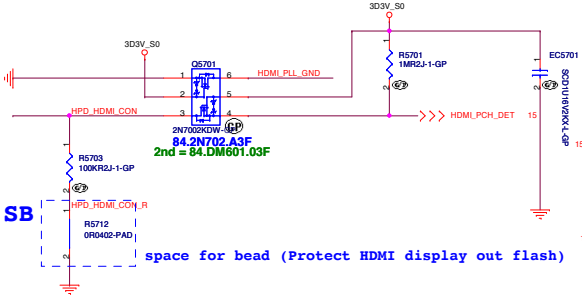


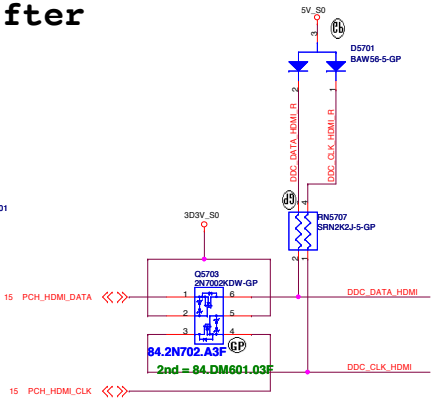


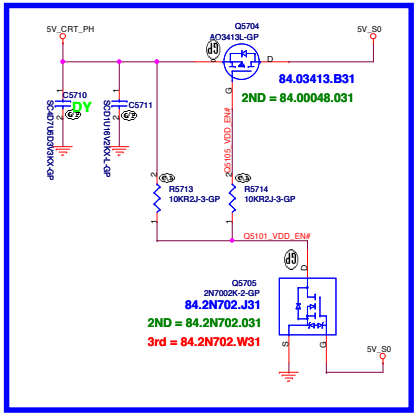


08/12 HDMI1 22.10296.B41 Change to 022.10025.0061

HDMI DDC Passive Level Shifter



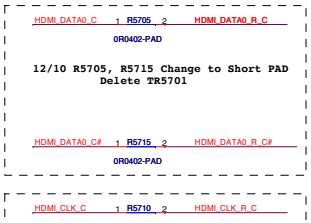


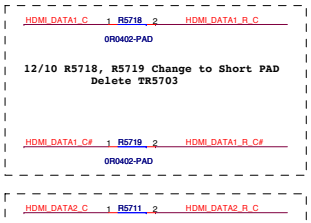


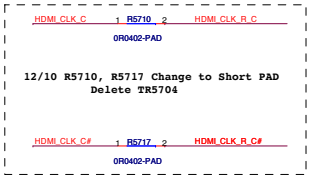
07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31

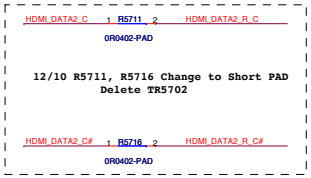
HDMI A type pin define (Total: 19pin)

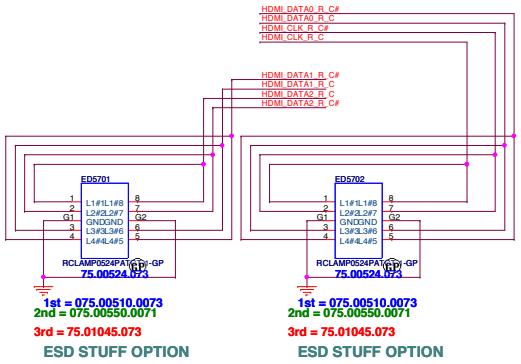
Pin	Pin定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2–
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1–
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0–
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock–
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

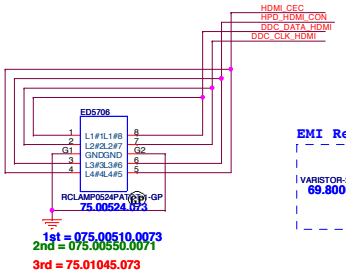




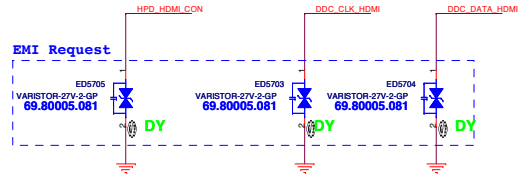








08/18 add ED5706



08/19 HPD_HDMI_CON & DDC_CLK_HDMI SWAP

10/15 ED5701,ED5702,ED5706 Change Part number to 75.00524.073
12/18 ED5701,ED5702,ED5706 Change to DY
12/24 ED5701,ED5702,ED5706 Change to ESD STUFF OPTION

BOM1

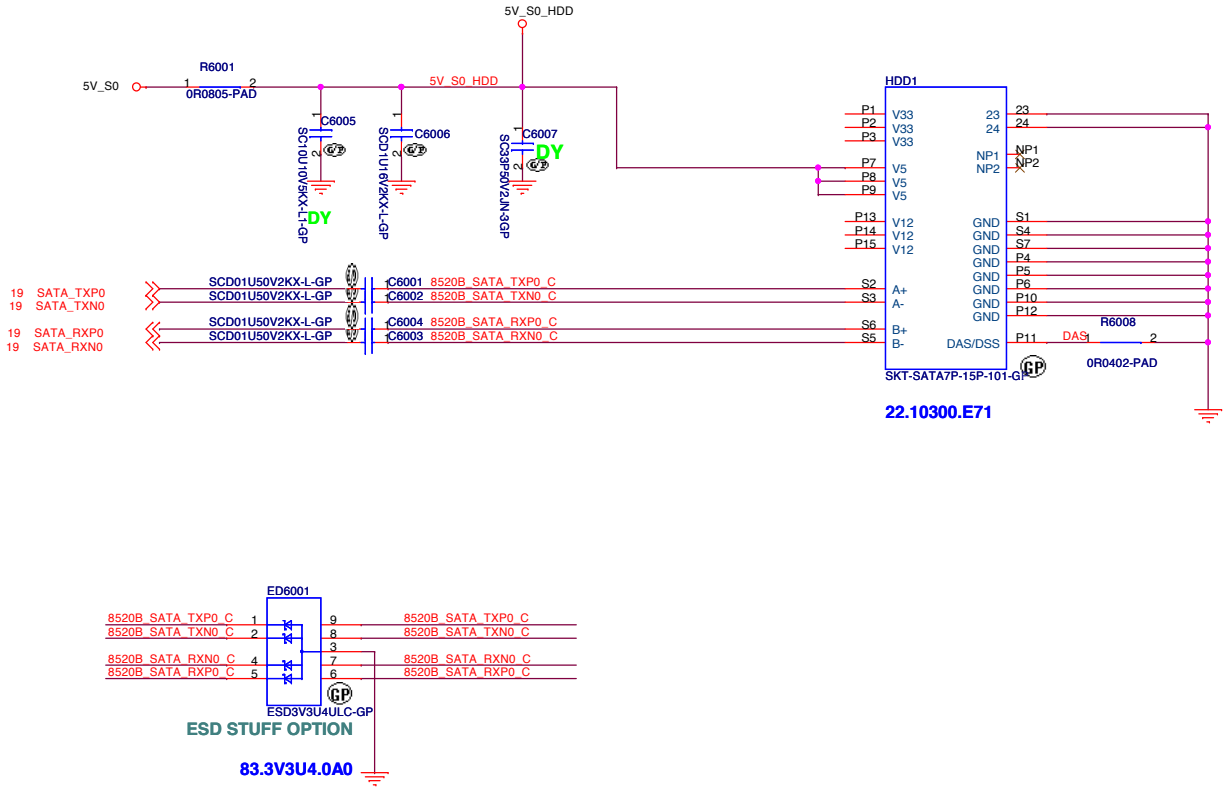
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A2	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 57 of 102

SSID = SATA



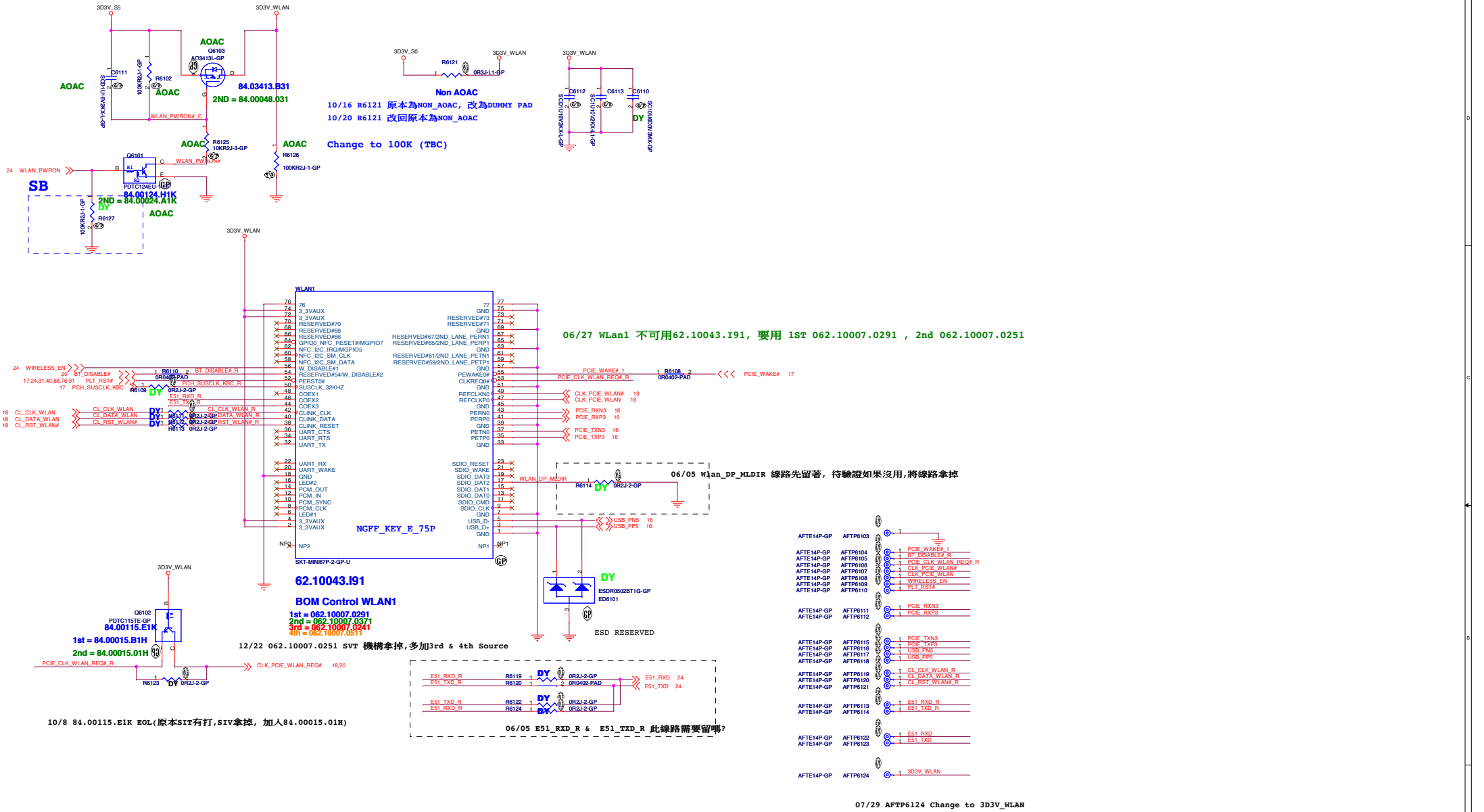
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD / NGFF_SSD***

Size	Document Number	Rev
A3	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 60 of 102



BOM1

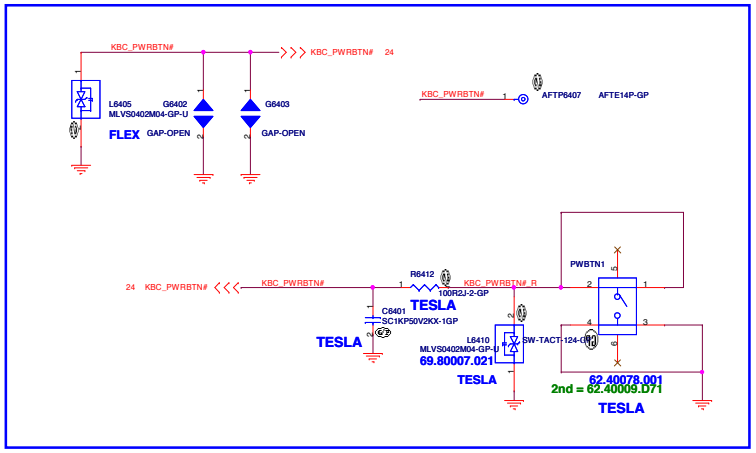
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN

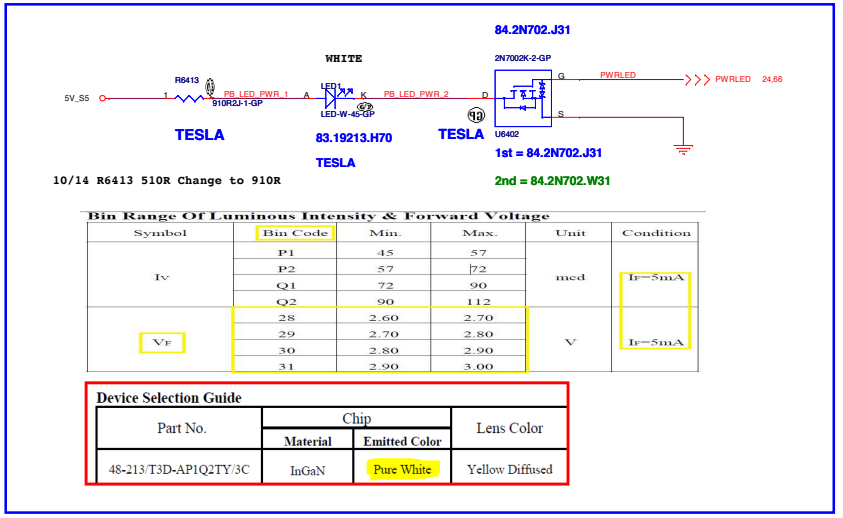
Size	Document Number	Rev
A2	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 61 of 102

Power Button



POWER BTN LED



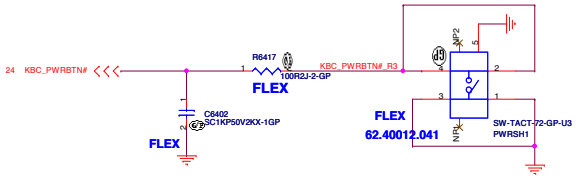
Bin Range Of Luminous Intensity & Forward Voltage

Symbol	Bin Code	Min.	Max.	Unit	Condition
Iv	P1	45	57	mcd	IF=5mA
	P2	57	72		
	Q1	72	90		
	Q2	90	112		
VF	28	2.60	2.70	V	IF=5mA
	29	2.70	2.80		
	30	2.80	2.90		
	31	2.90	3.00		

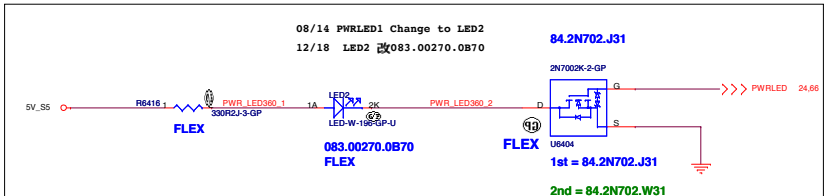
Device Selection Guide

Part No.	Chip		Lens Color
	Material	Emitted Color	
48-213/T3D-AP1Q2TY/3C	InGaN	Pure White	Yellow Diffused

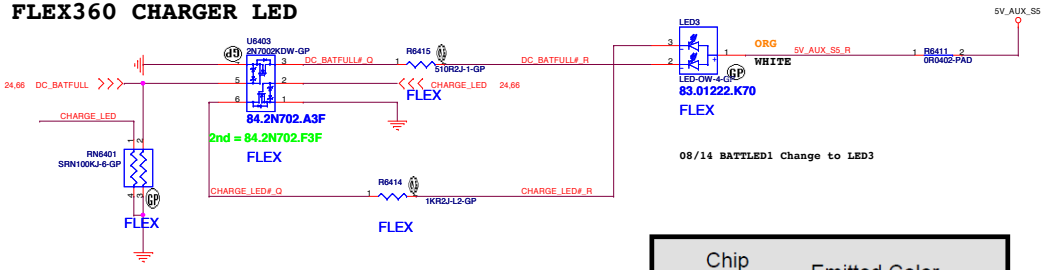
FLEX360 Power Button



FLEX360 POWER BTN LED



FLEX360 CHARGER LED

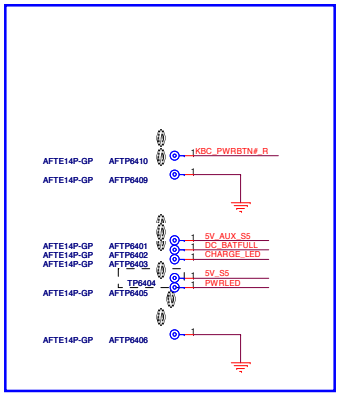


Electro-Optical Characteristics (Ta=25℃)

Parameter	Symbol		Min.	Typ.	Max.	Unit	Condition
		2 Different Bin Code type					
Forward Voltage	V_F	S2S	1.7	-----	2.3	V	I_F=5mA
		T3	2.7	-----	3.3		

Chip Materials	Emitted Color
AlGaInP	Brilliant Orange
InGaN	Pure White

Test point



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

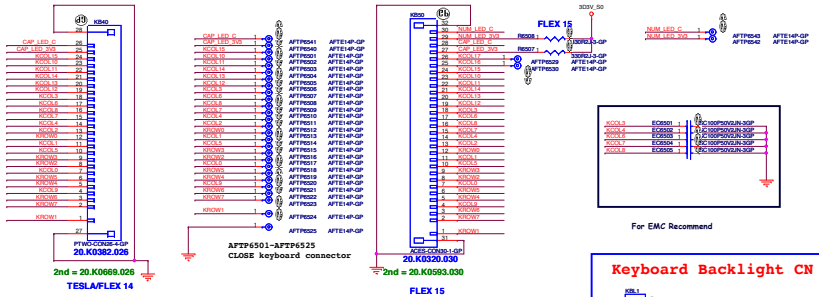
Title: LED Bard/Power Button

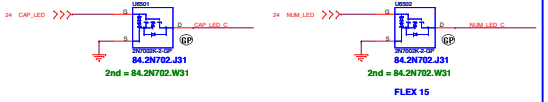
Size	Document Number	Rev
A2	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 64 of 102

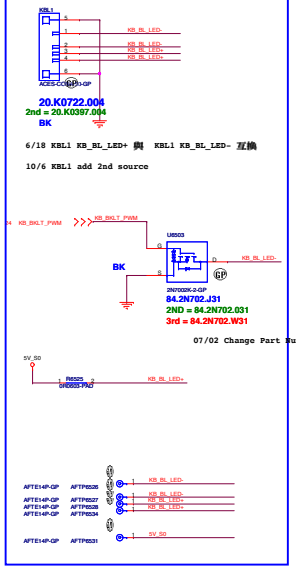
SSID = KBC

Internal KeyBoard Connector

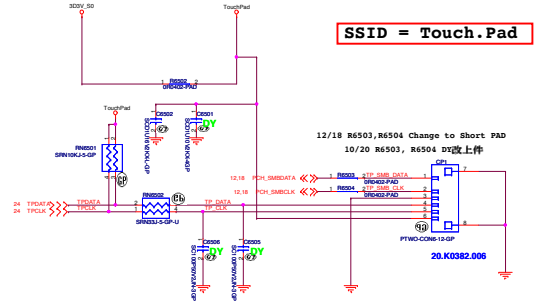


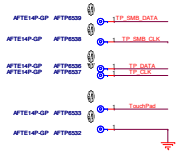


Keyboard Backlight CN

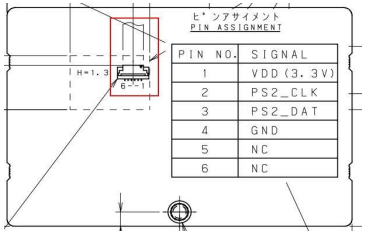


SSID = Touch.Pad





Ref. SPEC:KGDFF0106A11B0 31A
SA469D-22H1_v1.0
VCC=3.3V



PIN NO.	SIGNAL
1	VDD(3.3V)
2	PS2_CLK
3	PS2_DAT
4	GND
5	NC
6	NC

U6203 Keyboard Backlight U6203&BLKB1:

目前spec所看到
14和15的keyboard spec最大為300 mA

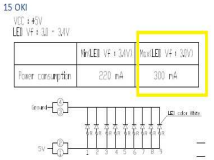
84.07002.I31

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_{amb} = 25 °C	-	-	60	V
V_{GS}	gate-source voltage	T_{amb} = 25 °C	-	-	±20	V
I_D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V	[1] -	-	350	mA
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 10 V; I_D = 500 mA	-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

15 OKI



BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

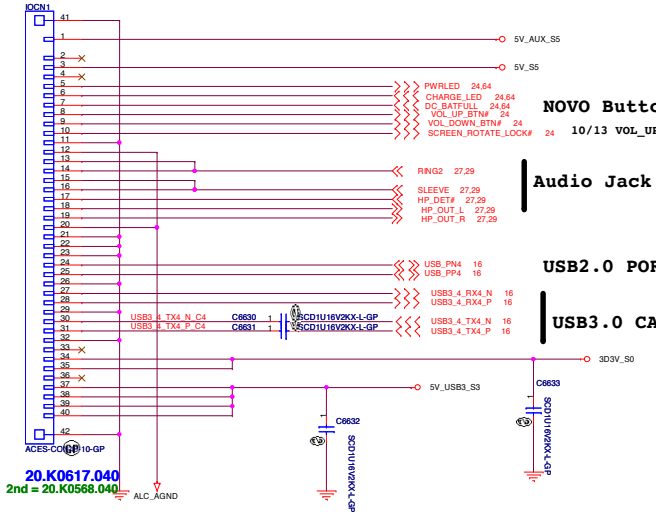
Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	LT41	-1

Date: Tuesday, January 29, 2013 Sheet 65 of 102

IO BD Device

Item	Device
1	NOVO Button
2	Audio Jack
3	USB Card Reader
4	USB2.0 Port4



NOVO Button

10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN# , net name 互換

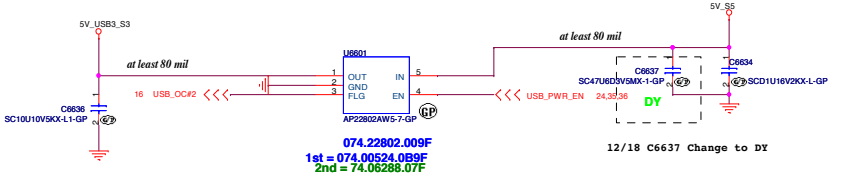
Audio Jack

USB2.0 PORT4

08/18 USB2.0 Port4 & USB3.0 Card Reader 有換PIN

USB3.0 CARD READER

USB 2.0 Power SW



12/18 C6636 Change to 10uF

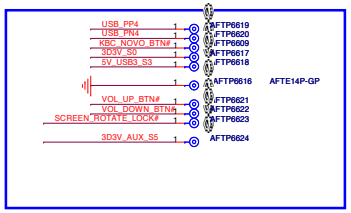
12/18 C6637 Change to DY

U6301 place near to IOCN1

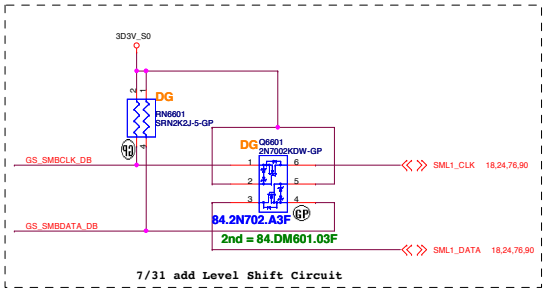
12/18 074.22802.009F 被禁用

08/05 U6601 add 2nd & 3rd Source

Test point

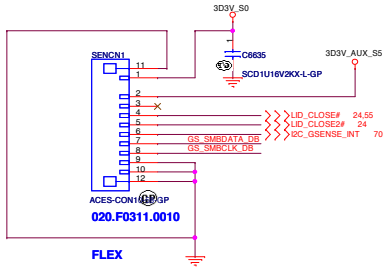


10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN# , net name 互換



7/31 add Level Shift Circuit

Flex360 SENSOR BD

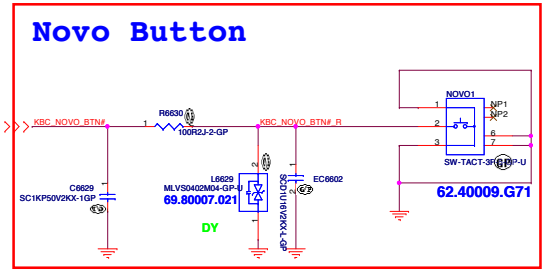


12/25 Sencn1 change Part Number 020.F0311.0010,
(原本20.F1897.010)

Hall sensor

06/12 Delete Hall Sensor CONN, 換7 pin 與SPK 訊號接同一CONN, SPK1

Novo Button



BOM1

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Title: IO Board Connector

Size	Document Number	Rev
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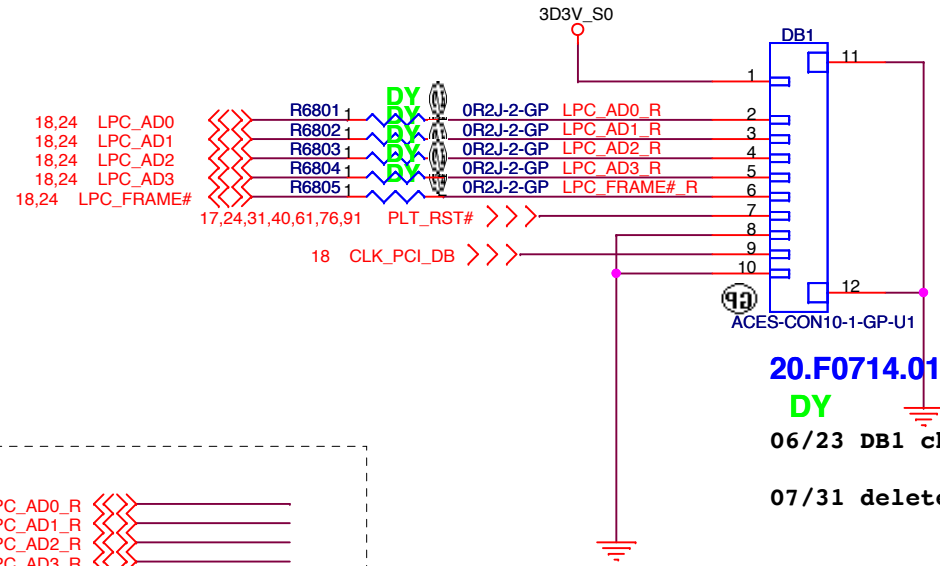
Date: Tuesday, January 20, 2015 Sheet 66 of 102

Debug Connector

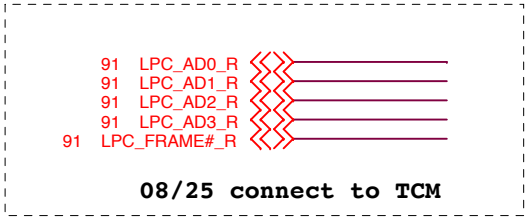


20.F0714.010

DY

06/23 DB1 change to Test point

07/31 delete Test point, add Debug CONN



BOM1

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Title: *Dubug connector*		
Size: A4	Document Number: LT41	Rev: -1
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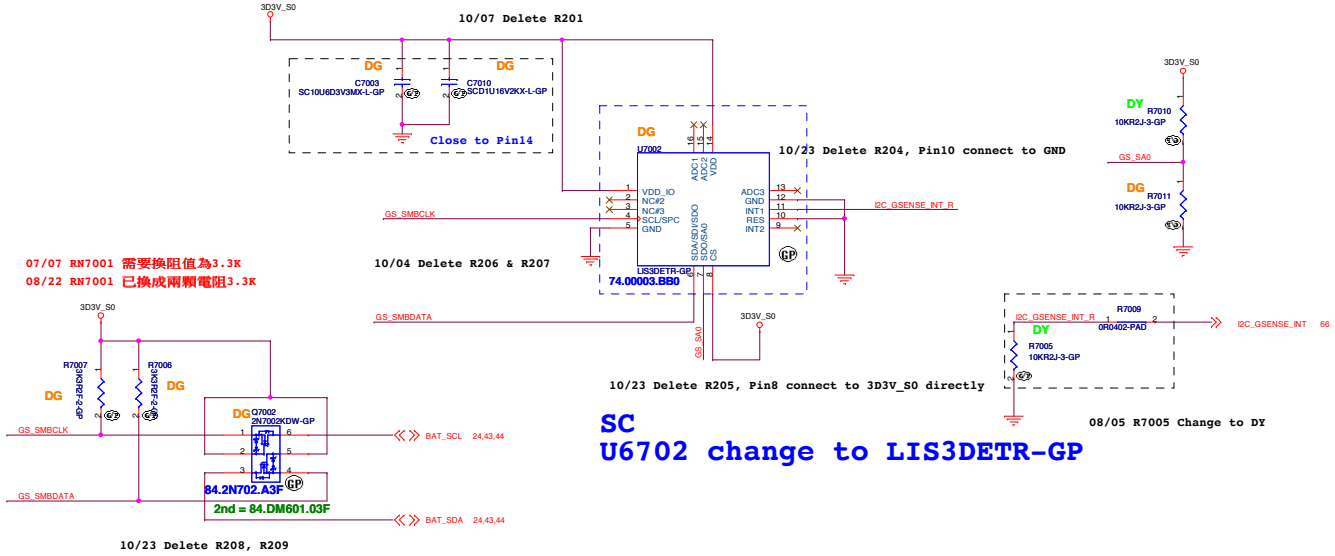
SC Digital_G-sensor

The Slave ADdress (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



SC U6702 change to LIS3DETR-GP

M40

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Title: G Sensor

Size	Document Number	Rev
A2	LT41	-1

Date: Tuesday, January 20, 2015 Sheet 70 of 102

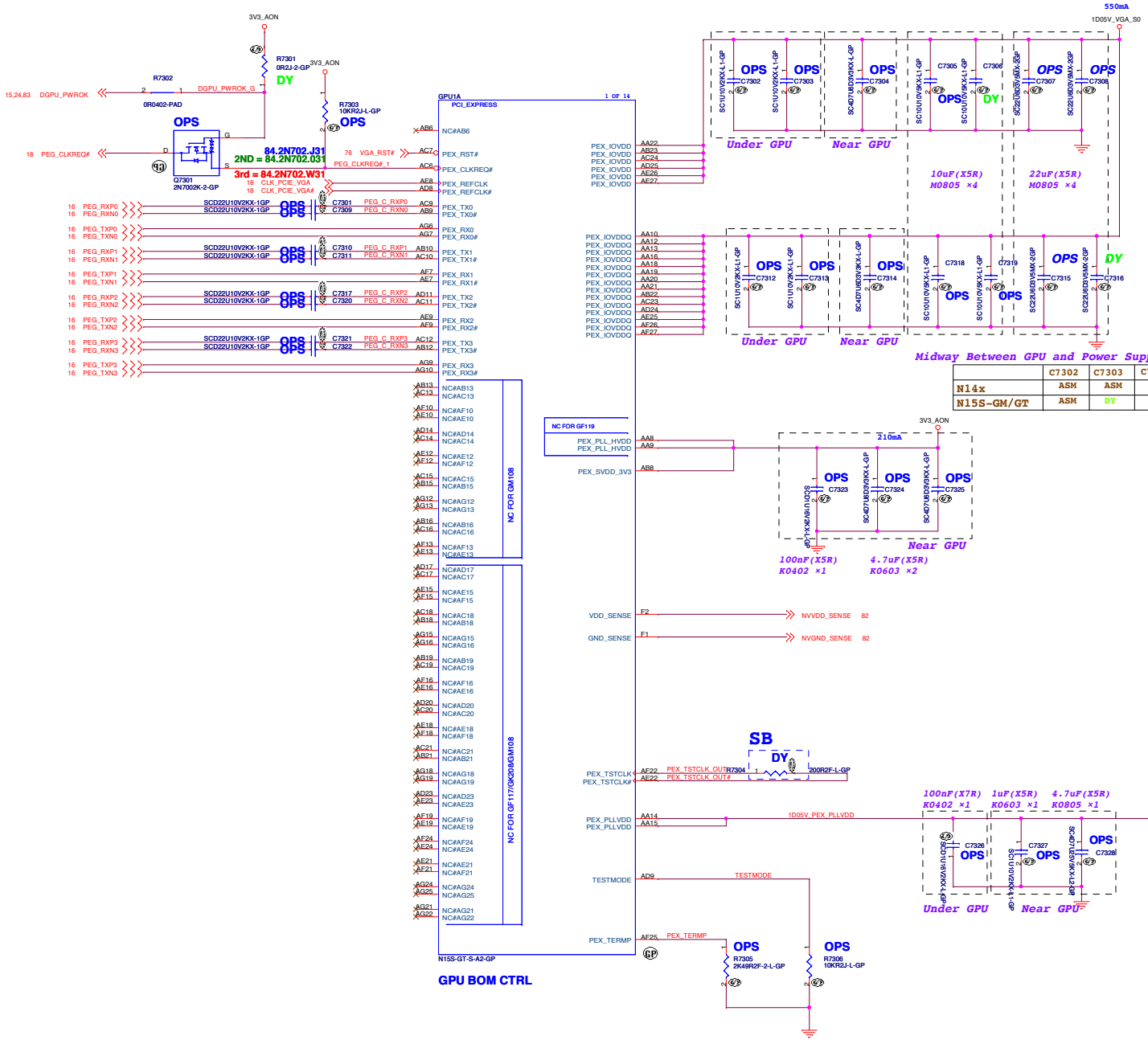

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
10uF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N15S-GM/GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY

M40

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Title: GPU(PEG)

Size: A2 | Document Number: LT41 | Rev: -1

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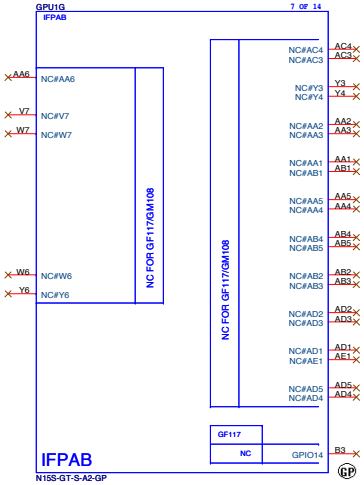
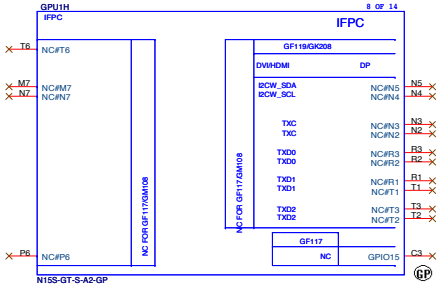
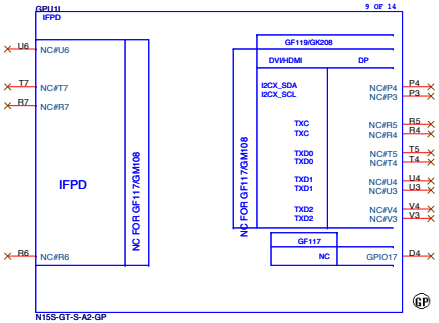


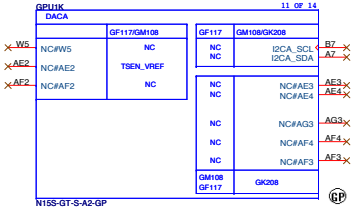
GPU BOM CTRL



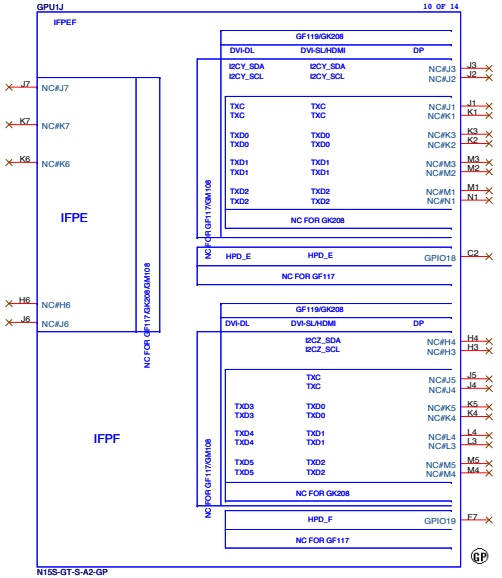
GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL



GPU BOM CTRL

M40

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Title: ***GPU (DIGITALOUT)***

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GPU Strap change Res. To Parallel Res.

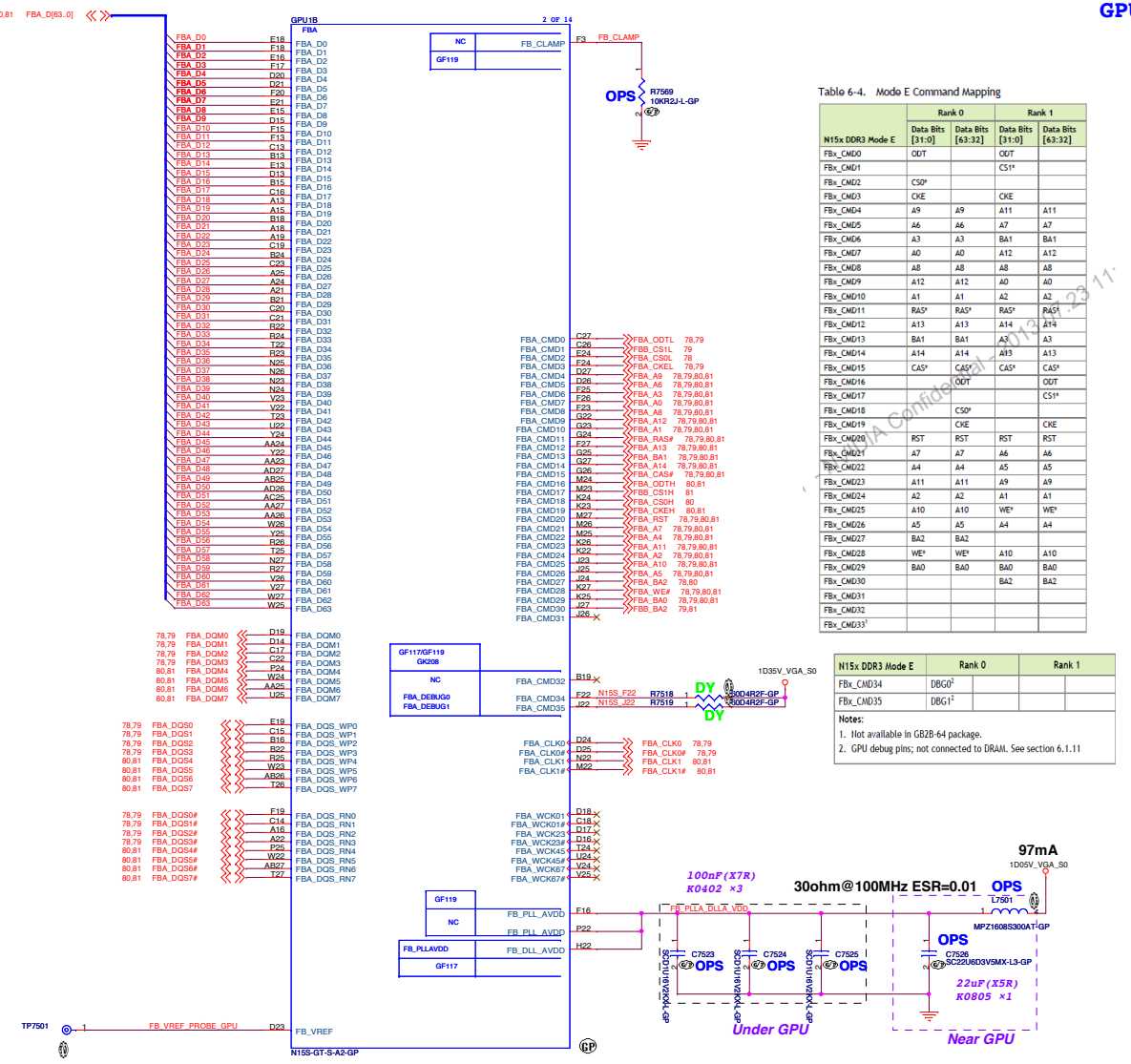
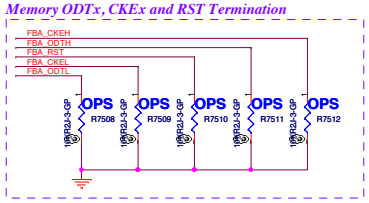


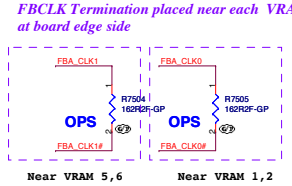
Table 6-4. Mode E Command Mapping

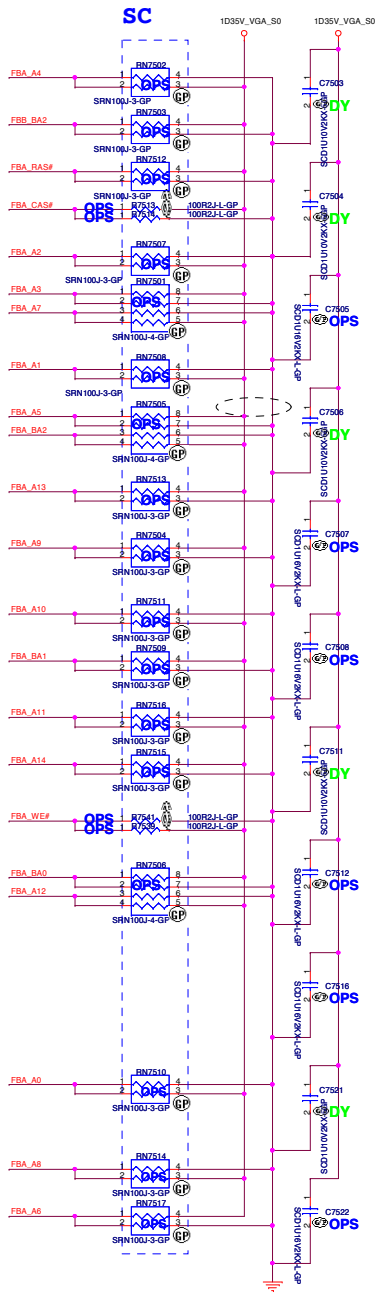
N15x DDR3 Mode E	Rank 0		Rank 1	
	Data Bits [31:0]	Data Bits [63:32]	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT		ODT	
FBx_CMD1			CS1*	
FBx_CMD2	CS0*			
FBx_CMD3	CKE		CKE	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS*	RAS*	RAS*	RAS*
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS*	CAS*	CAS*	CAS*
FBx_CMD16		ODT		ODT
FBx_CMD17				CS1*
FBx_CMD18		CS0*		
FBx_CMD19		CKE		CKE
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE*	WE*
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE*	WE*	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2
FBx_CMD31				
FBx_CMD32				
FBx_CMD33[1]				

N15x DDR3 Mode E	Rank 0	Rank 1
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11







M40

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Title: GPU (VRAM I/F)

Size	Document Number	Rev
Custom	LT41	-1

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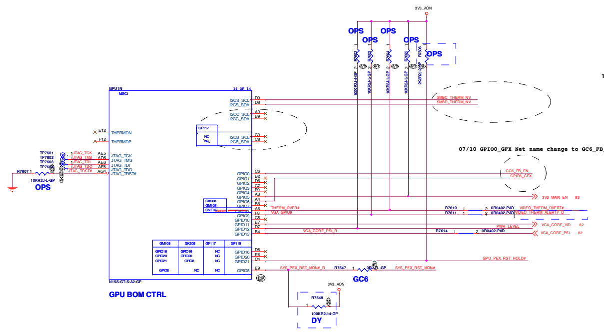

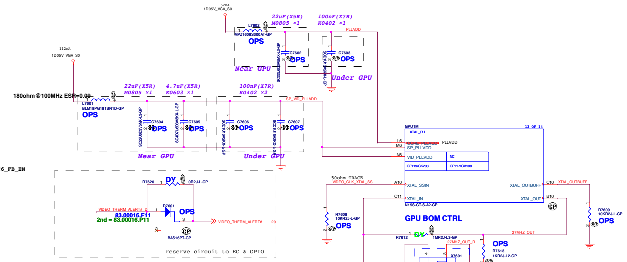

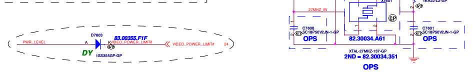

Crystal 27MHz

Crystal 27MHz			
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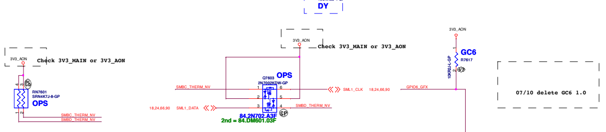
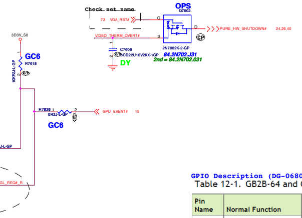
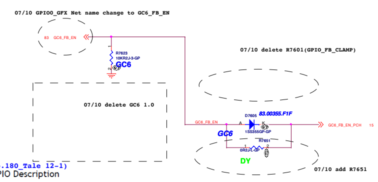
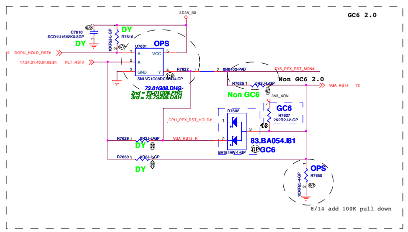
2ND	HARMONY	82.30034.351	78.18034.1FL









07/10 delete GC6 1.0

07/10 add R7651

GPIO Description (DG-06803-001_v04_p.180_Tale 12-1)

Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	10K pull-up to 3V3_AON unless actively driven.
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IPFB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

GPU (Dual Rank) VRAM Config:

Table 4. N15V-GM DDR3L Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3L	Hynix	0x4	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Production ready
	Micron	0xD	1.35 V/ 1.35 V	MT41K256M16HA-107G:E	900	N/A	Production ready

N15S-GT(GB2-64/GT840M)-->SB SKU2,3,4,5

Table 20. N15S-GT/GM DDR3L Dual-Rank Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3L	Hynix	0x3	1.35 V/ 1.35 V	H5TC4G63AFR-11C	900	N/A	Preliminary
	Micron	0x4	1.35 V/ 1.35 V	MT41J256M16HA-093G:E	900	1322	Preliminary
	Samsung	0x5	1.35V/ 1.35V	K4W4G1646D-HC1A	900	N/A	Preliminary

< - SA SKU2,3,4,5

Note: For N15S-GT/-GM, the maximum allowable memory case temperature is 85 °C.

Table 1. N15E-GX / -GT GC6 pin assignment

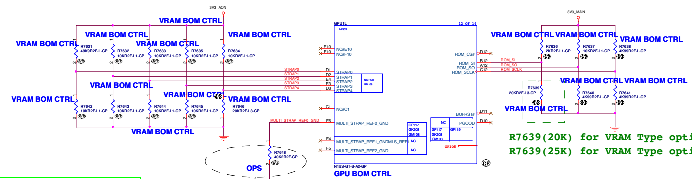
GPIO	GC6 1.0 Control Signal	GC6 2.0 Control Signal
GPIO1	FB_CLAMP_MON	GC6_FB_EN
GPIO2	FBCLAMP_TGL_REQ#	GPU_EVENT#
GPIO4	Reserve	PWR_EN
GPIO23	Reserve	GPU_PEX_RST_HOLD#
CEC	NC	SYS_PEX_RST_MON#

< - SA SKU2,3,4,5

GC6 1.0/2.0 GPU Support List

GPU	GC6 feature
N15V-GM-S[GF117]	No
N15V-GM-B[GF117]	No
N15S-GV[GK208]	GC6 1.0 only
N15S-GM[GM108]	GC6 2.0 only
N15S-GT[GM108]	GC6 2.0 only
N15S-GS[GM107]	GC6 2.0 only
N15P-GT[GM107]	GC6 2.0 only
N15P-GX[GM107]	GC6 2.0 only
N15E-GX[GK104]	GC6 1.0 only
N15E-GT[GK104]	GC6 1.0 only

< - SA SKU2,3,4,5



R7639(20K) for VRAM Type option (Default: Hynix)

R7639(25K) for VRAM Type option (Micron)

N15S-GT
Device ID: 0X1290(TBC)

07/29 Before "N15V-GM:DY Other:Stuff", 改為OPS 屬性, N16X 都要上件

NOTE: "N15V-GM" with Binary mode support, left Multi_Strap_Ref0_GND pin "NC";
All other N15x GPUs, connect Multi_Strap_Ref0_GND pin to GND per 40.2K resister

NVIDIA TABLE		N15S-GT Hynix 256Mx16 H5TC4G63AFR-11C Device ID 0X1140(TBC)	N15S-GT Micron 256Mx16 MT41J256M16HA-093G:E Device ID 0X1140(TBC)
ROM_SI(Depend on VRAM type)	R7636	DY	DY
	R7639	20Kohm	25Kohm
ROM_SO	R7637	DY	DY
	R7640	4.99Kohm	4.99Kohm
ROM_CLK	R7638	DY	DY
	R7641	4.99Kohm	4.99Kohm
STRAP0	R7631	50Kohm	50Kohm
	R7642	DY	DY
STRAP1	R7632	DY	DY
	R7643	DY	DY
STRAP2	R7633	DY	DY
	R7644	DY	DY
STRAP3	R7635	DY	DY
	R7645	DY	DY
STRAP4	R7634	DY	DY
	R7646	DY	DY

NVVDD Boot Voltage 0.9V

SKU4, SKU5------> 4GB (VRAM*8)

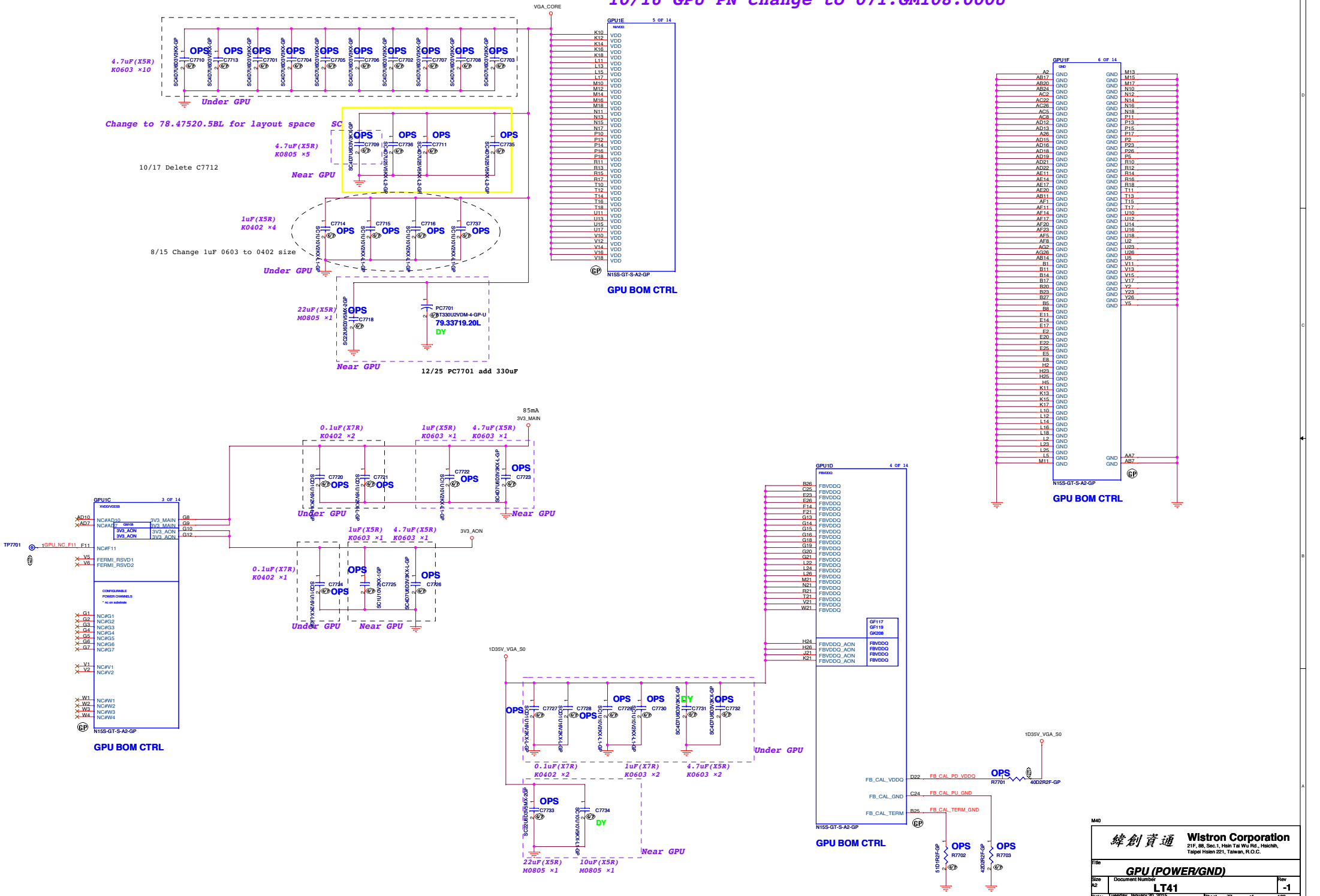
SKU2, SKU3------> 2GB(VRAM*4)(VRAM1,2,5,6 ASM)

1D35V Compatible VRAM P/N List			
Vendor	Vendor P/N	Lenovo P/N	1 chip VRAM Size
Hynix	H5TC4G63AFR-11C	1100897	512MB
Micron	MT41J256M16HA-093G:E	1101018	512MB

GPU Config:

GPU	SKU1 UMA	SKU2	SKU3	SKU4	SKU5
N15S-GT 071.0N15S.0C0U	NA	STUFF	STUFF	STUFF	STUFF

10/16 GPU PN change to 071.GM108.000U



M40

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (POWER/GND)

Size: A2 | Document Number: LT41 | Rev: -1

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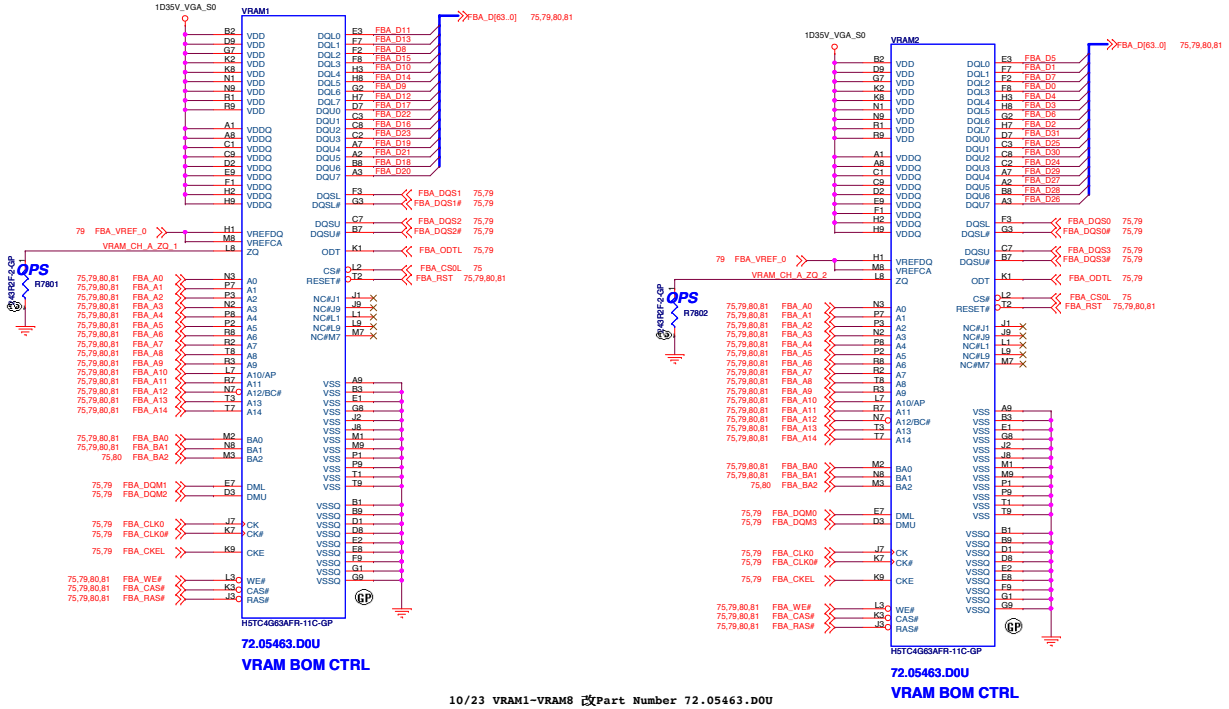
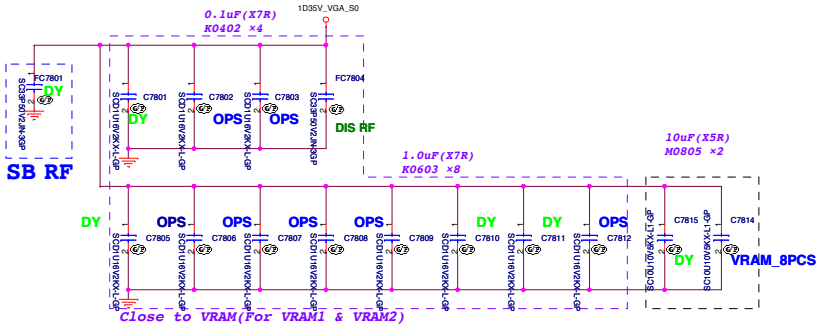
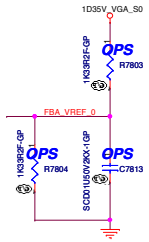
Data Bits 31:0 RANK 0



10/23 VRAM1~VRAM8 改Part Number 72.05463.D0U





08/18 C7801, C7804, C7805,C7810, C7811 Change to DY

08/18 C7814 Change to VRAM_8PCS

BOM1

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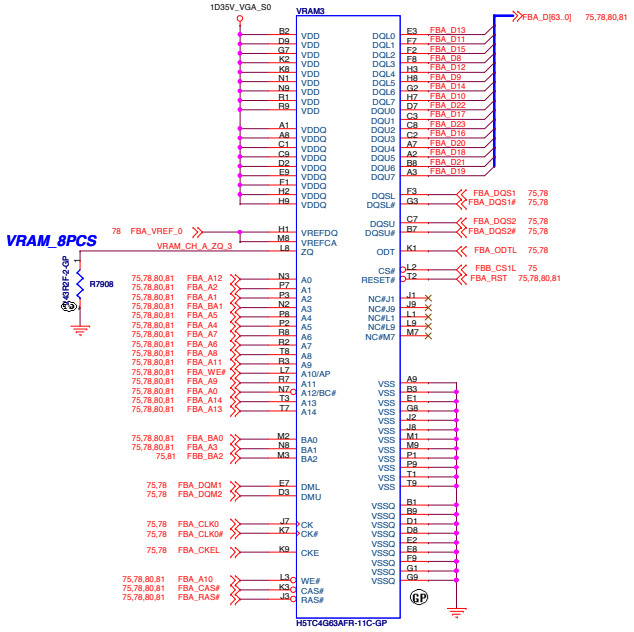
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

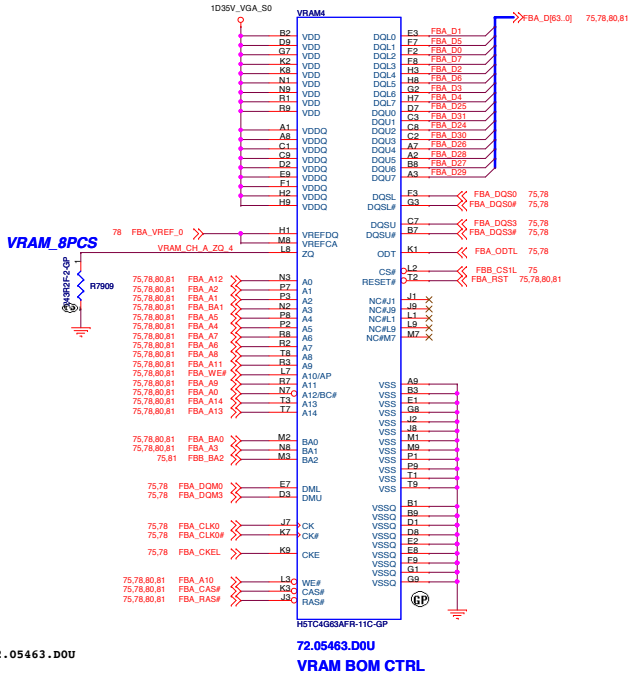
Size	Document Number	Rev
A2	LT41	-1

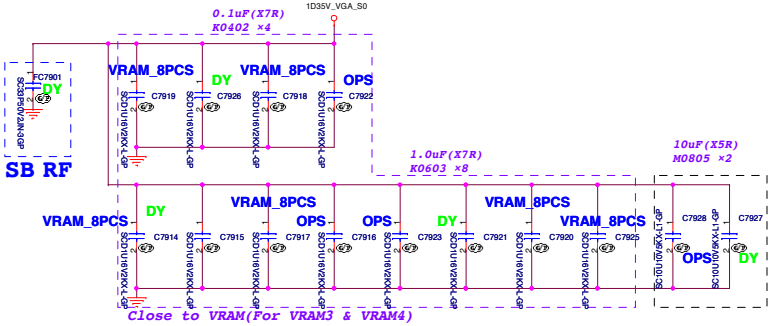
Date: Tuesday, January 20, 2015 Sheet 78 of 102

Data Bits 31:0 RANK 1



10/23 VRAM1-VRAM8 改Part Number 72.05463.D0U





08/18 C7915, C7921, C7926 Change to DY

08/18 C7914, C7917, C7918, C7919 ,C7920, C7925 Change to VRAM_8PCS

BOM1

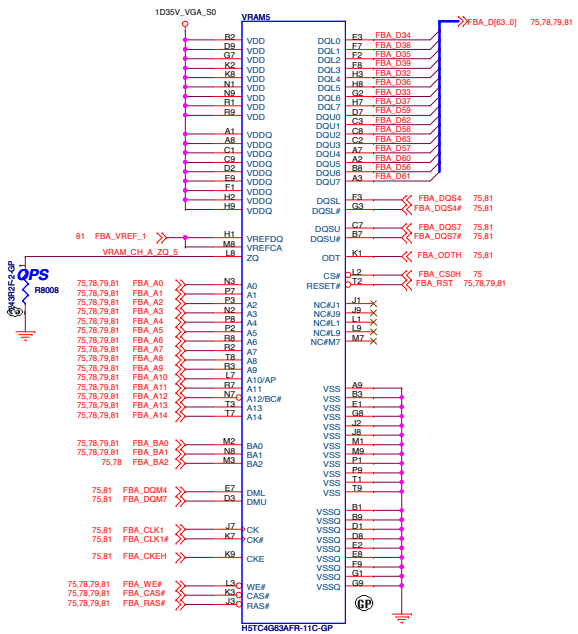
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM3,4 (2/4)***

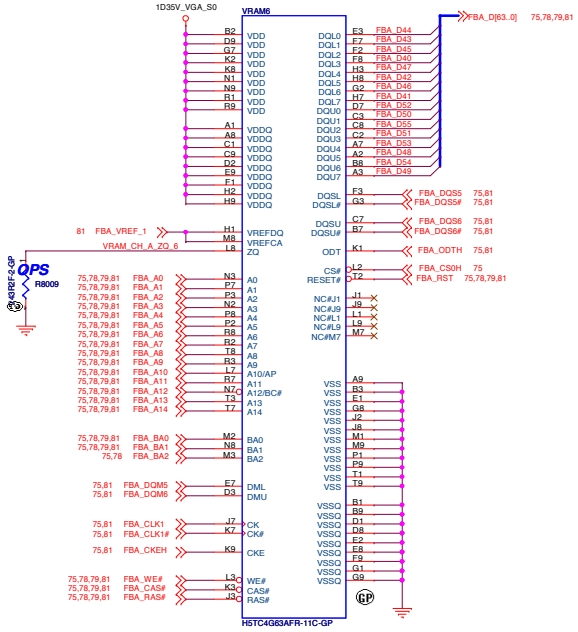
Size	Document Number	Rev
A2	LT41	-1

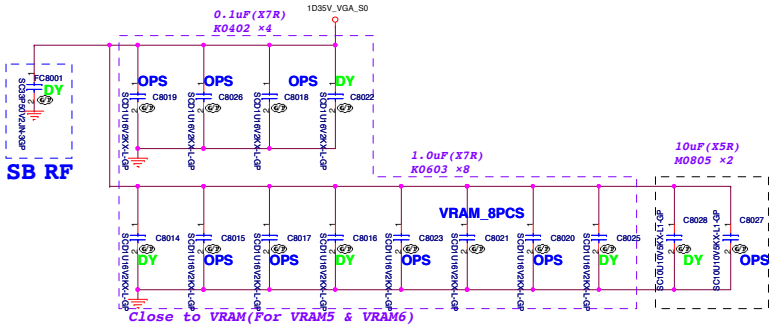
Date: Tuesday, January 20, 2015 Sheet 79 of 102

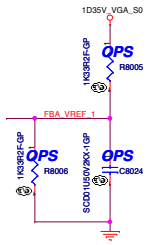
Data Bits 63:32 RANK 0



10/23 VRAM1-VRAM8 改Part Number 72.05463.D0U







08/18 C8014, C8016, C8022, C8025 Change to DY

08/18 C8021 Change to VRAM_8PCS

BOM1

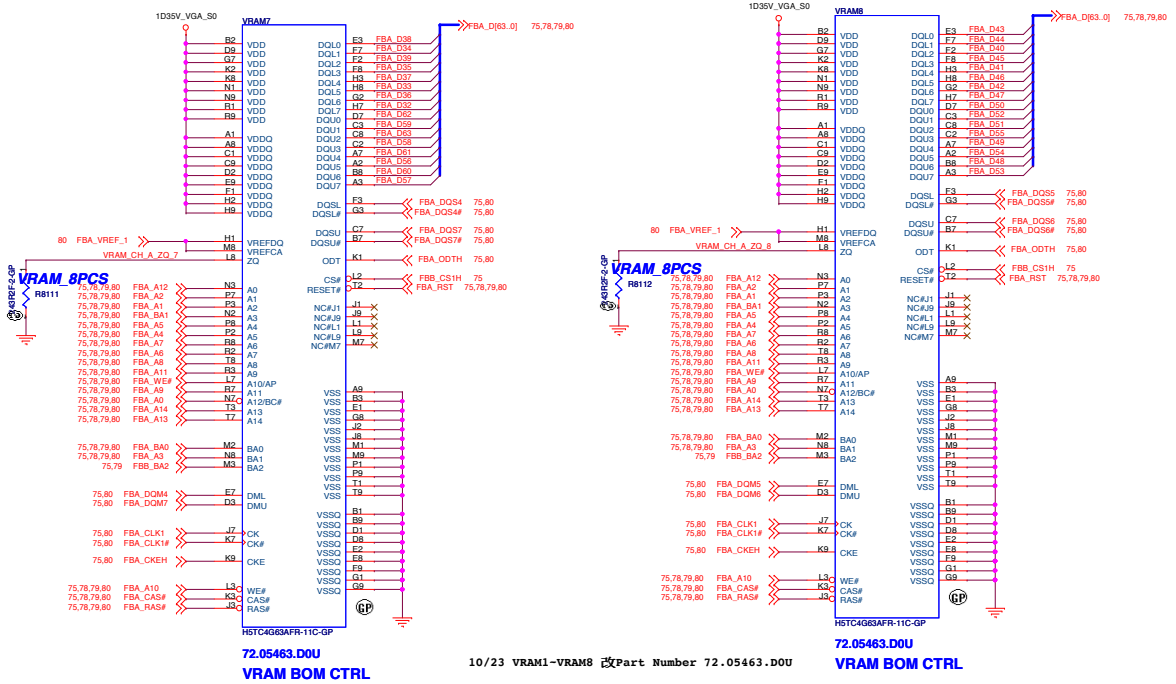
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

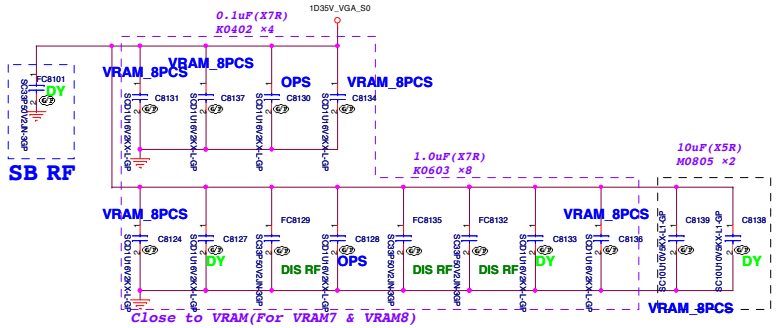
Size: A2 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 80 of 102

Data Bits 63:32 RANK 1



10/23 VRAM1~VRAM8 改Part Number 72.05463.D0U



08/18 C8127, C8129, C8132, C8133, C8135 Change to DY

08/18 C8124, C8131, C8134, C8136, C8137, C8139 Change to VRAM_8PCS

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM7,8 (4/4)**

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	Main source	2nd source
PU8202 PU8204	084.06970.0037	84.03660.037
PU8203 PU8205	084.06970.0037	84.03660.037

06/30 Change PU8202~PU8205 Main Source & 2nd Source

12/17 Change back

12/17 Change back

12/17 Change back

12/17 Change back

12/11 PG8201~PG8206 Change Part number
ZZ.CLOSE.001(上綠漆)

07/09 3V3_AON Change to 3V3_MAIN

Design Current
= 33.5 A
OCP< 67A

PU8201 RT8812AGQW-GP OPS 74.08812.073

PU8202 PU8204 FDMS3600-02-RJK0215-COLAY-GP OPS Change to 084.06970.0037 2nd = 84.03660.037

PU8203 PU8205 FDMS3600-02-RJK0215-COLAY-GP OPS Change to 084.06970.0037 2nd = 84.03660.037

Cyntec. 0.36uH 10*10*4
DCR=1.05mohm
Idc=30A, Isat=60A
PL8201 COIL-D36UH-6-GP OPS
68.R3610.20X
2ND = 068.R3610.1001

Cyntec. 0.36uH 10*10*4
DCR=1.05mohm
Idc=30A, Isat=60A
PL8202 COIL-D36UH-6-GP OPS
68.R3610.20X
2ND = 068.R3610.1001

GPU BOM CTRL
R1 PR8222 20KR2F-L3-GP
R2 PR8206 20KR2F-L3-GP
R3 PR8208 2KR2F-3-GP
R4 PR8209 18KR2F-GP
R5 PR8204 0R2J-2-GP

08/07 N16S-GT & N16V-GM 都為Config B 0.9V

Nvidia GPU Vreg Strap Table & P/N:

Nvidia GPU Vreg Strap	Table & P/N	
GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222)	64.27025.6DL	64.20025.L0L
R2(PR8206)	64.75015.6DL	64.20025.L0L
R3(PR8208)	63.R0034.1DL	64.20015.6DL
R4(PR8209)	64.62015.6DL	64.18025.6DL
R5(PR8204)	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL

GM108 SKU

Item	N16S-GT-B/S
Device ID	0x1347
Package	GB4B-128/GB2B-64
Internal P/N	GM108-755/655,28nm
ROM_SI	Refer to GM108 RAM Straps
ROM_SO	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
Strap2	
Strap3	
Strap4	
Open_VRG SKU	B
NVVDD Boot Voltage	0.9V

GK208s SKU

Item	N16V-GM-S
Device ID	0X1299
Package	GB2-64
Internal P/N	GK208-620,28nm
ROM_SI	Refer to GK208s RAM Straps
ROM_SO	0x8, 5K pull up for Optimus/0x9 ,10K Pull Up for Discrete SKU
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xF, 45kohm pull up
Strap1	3GIO_PAD_Config, 0x7, 45kohm pull down
Strap2	Device_ID, 0x1001_ 10Kohm pull UP
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down (PCIE_SPEED_CHANGE=1)
Open_VRG SKU	Config B[PSI not supported]
NVVDD Boot Voltage	0.9V

07/09 3V3_AON Change to 3V3_MAIN

BOM1

緯創資通 Wistron Corporation
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Title: RT8812A_VGA_CORE

Size: Custom | Document Number: LT41 | Rev: -1

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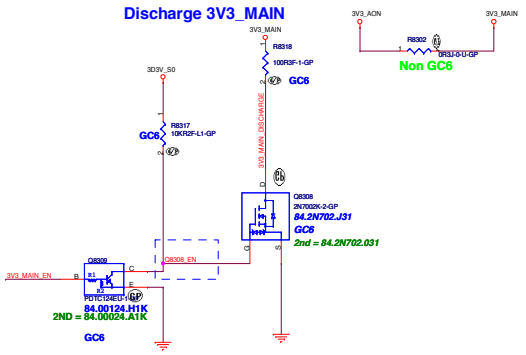
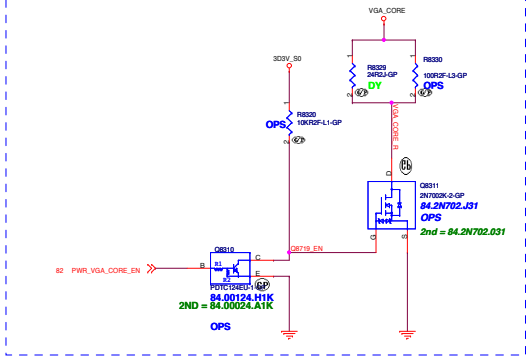
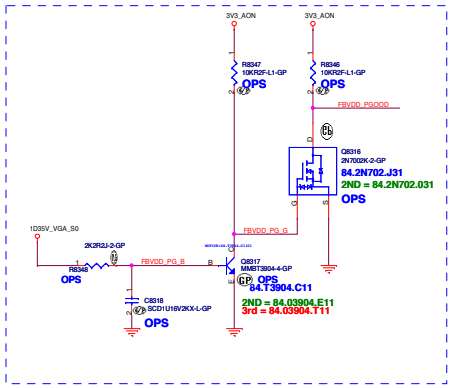
1D35V_VGA_S0

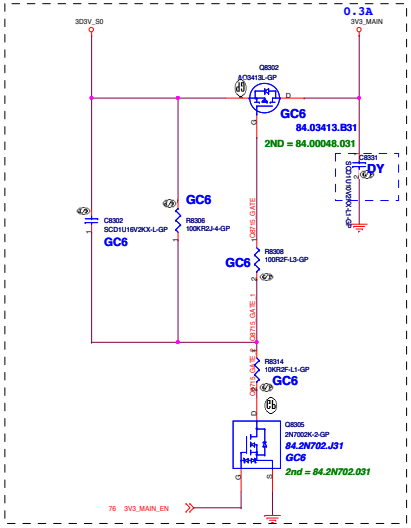
Discharge 3V3_MAIN



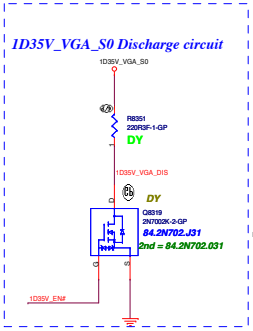
Discharge VGA_CORE

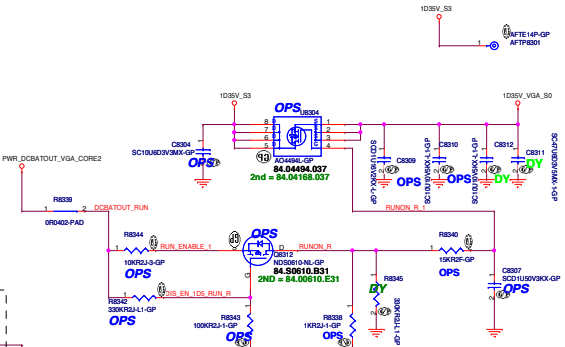


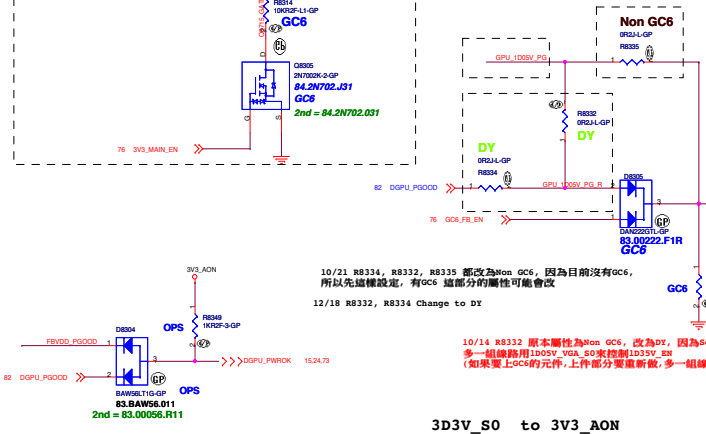


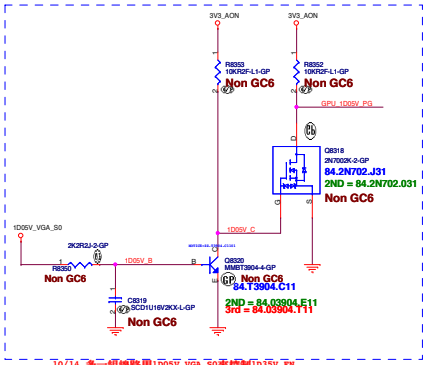


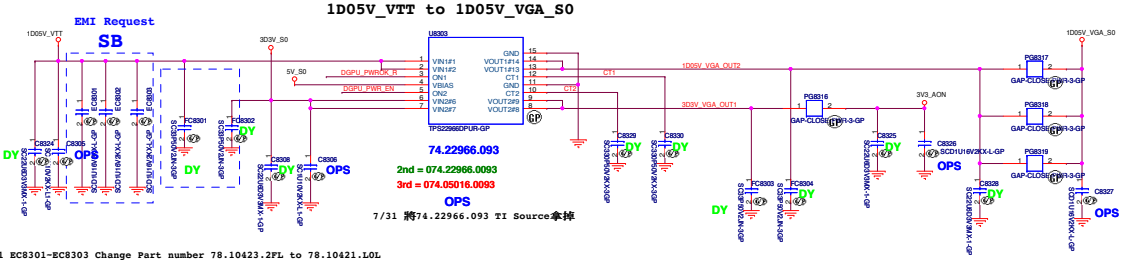
1D35V_VGA_S0 Discharge circuit

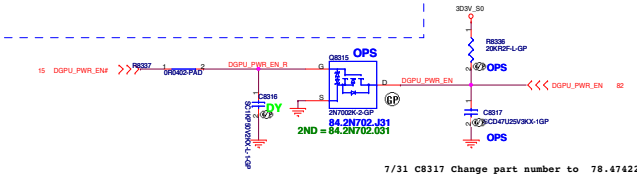


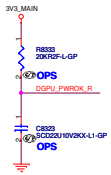












3D3V_S0 to 3V3_AON
1D05V_VTT to 1D05V_VGA_S0

10/21 R8334, R8332, R8335 都改為Non GC6，因為目前沒有GC6，所以先這樣設定，有GC6 這部分的屬性可能會改

12/18 R8332, R8334 Change to DY

10/14 R8332 原本屬性為Non GC6，改為DY，因為Sequence有問題，多一組線路用1D05V_VGA_S0來控制1D35V_EN（如果要上GC6的元件，上件部分要重新做，多一組線路是FOR Non GC6的）

12/09 R8313 Change to Short PAD

10/14 多一組線路用1D05V_VGA_S0來控制1D35V_EN（如果要上GC6的元件，上件部分要重新做，多一組線路是FOR Non GC6的）

10/21 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to DY (原本為Non GC6)

12/18 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to STUFF

12/11 PG8316~PG8319 Change Part number ZZ.CLOSE.001(上錄漆)

7/31 EC8301~EC8303 Change Part number 78.10423.2FL to 78.10421.LOL

7/31 將74.22966.093 TI Source拿掉

10/14 R8333 20K Change to 10K

10/27 R8333 10K Change to 20K

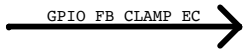
7/31 C8317 Change part number to 78.47422.5BL(0402 to 0603)

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

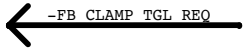
Title: DISCRETE VGA POWER
Size: Custom | Document Number: LT41 | Rev: -1
Date: Tuesday, January 20, 2015 | Sheet 83 of 102

Undefined Sys <-> GPU IO

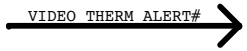
KBC <-> GPU



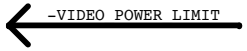
KBC output



KBC input

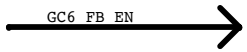


KBC GPIO (Reserved)

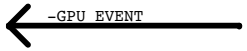


KBC output (Reserved)

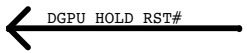
PCH <-> GPU



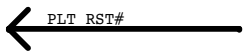
PCH input



PCH output

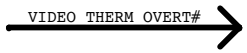


PCH output

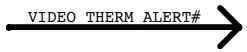


PCH output

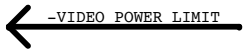
Thermal IC <-> GPU



Thermal IC input(Reserved)



Thermal IC GPIO(Reserved)



Thermal IC output(Reserved)

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Switchable GFX LCD(1/2)***

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08/14 H6, H8 ZZ.00PAD.591 Change to ZZ.SCREW.H21

Structure boss

H6 HOLET315B315X315R237-S-1-GP — ZZ.SCREW.H21 — GP

H8 HOLET315B315X315R237-S-1-GP — ZZ.SCREW.H21 — GP

H9 HOLET237B315X315R91-S-GP-U2 — ZZ.00PAD.591 — CB

Stand off

H14 STF236R128H88-GP — 34.4LY03.001 — 2nd = 34.4LY03.201

07/29 H3 Change to OPS

CPU

H1 STF237R128H42-GP — 34.4GD01.101 — 1ST = 34.4WZ01.001 — 2nd = 34.4WZ01.101

H2 STF237R128H42-GP — 34.4GD01.101 — 1ST = 34.4WZ01.001 — 2nd = 34.4WZ01.101

H4 STF237R128H42-GP — 34.4GD01.101 — 1ST = 34.4WZ01.001 — 2nd = 34.4WZ01.101

GPU

H3 STF237R128H42-GP — OPS — 34.4GD01.101 — 1st = 34.4WZ01.001 — 2nd = 34.4WZ01.101

H5 STF237R128H42-GP — OPS — 34.4GD01.101 — 1st = 34.4WZ01.001 — 2nd = 34.4WZ01.101

H12 HOLE237R95-GP — ZZ.00PAD.921 — GP

H13 HOLE237R158-GP — ZZ.0HOLE.011 — GP

H18 HOLE237R158-GP — ZZ.0HOLE.011 — GP

H19 HOLE237R95-GP — ZZ.00PAD.921 — GP

CLP1 SPRING-112-GP — 34.44401.001 — DY

CLP3 SPRING-112-GP — 34.44401.001

CLP5 SPRING-112-GP — 34.44401.001

CLP6 SPRING-112-GP — 34.44401.001

SPR5 SPRING-157-GP — 34.4YW17.001

SPR2 SPRING-157-GP — 34.4YW17.001

SPR4 SPRING-157-GP — 34.4YW17.001

CLP8 SPRING-112-GP — 34.44401.001 — DY

06/06 Delete Clp3 記得SB版要將CLP 上件

10/22 CLP1, CLP4, CLP7, CLP8 上件(原本為ZZ)

10/22 SPR1 上件(原本為ZZ)

12/18 CLP1 Change to DY

12/18 Delete CLP4, 因為那位置要放SPR4

01/13 add SPR5

08/22 add SPR2

12/11 SPR2 改上件

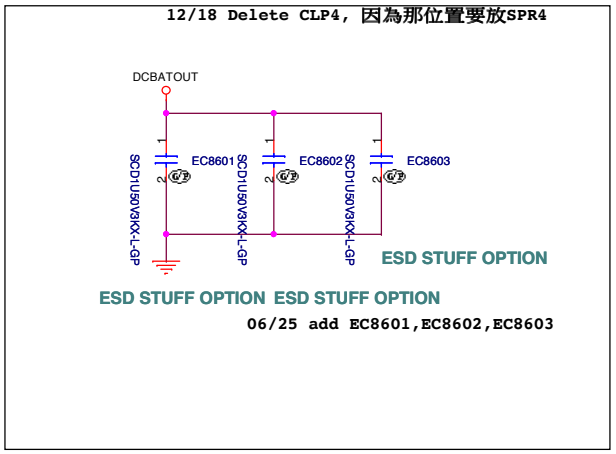
06/18 add SPR1

12/23 Delete SPR1 10/17 add EC8604-EC8611 for EMI

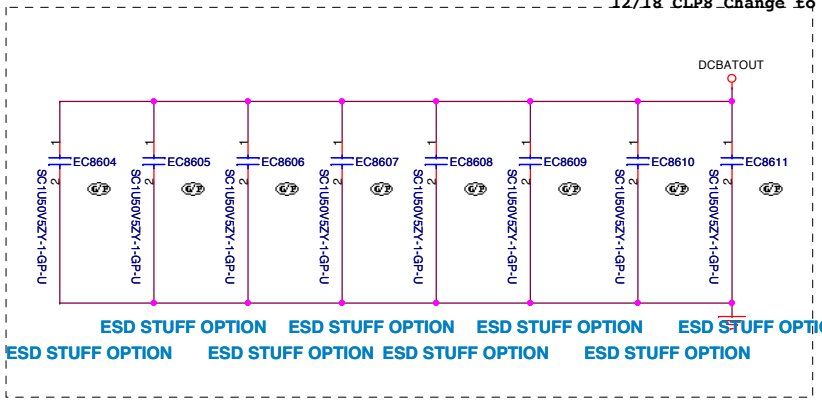
10/20 add CLP7, CLP8

10/23 Delete CLP7

12/18 CLP8 Change to DY



06/25 add EC8601,EC8602,EC8603



BOM1

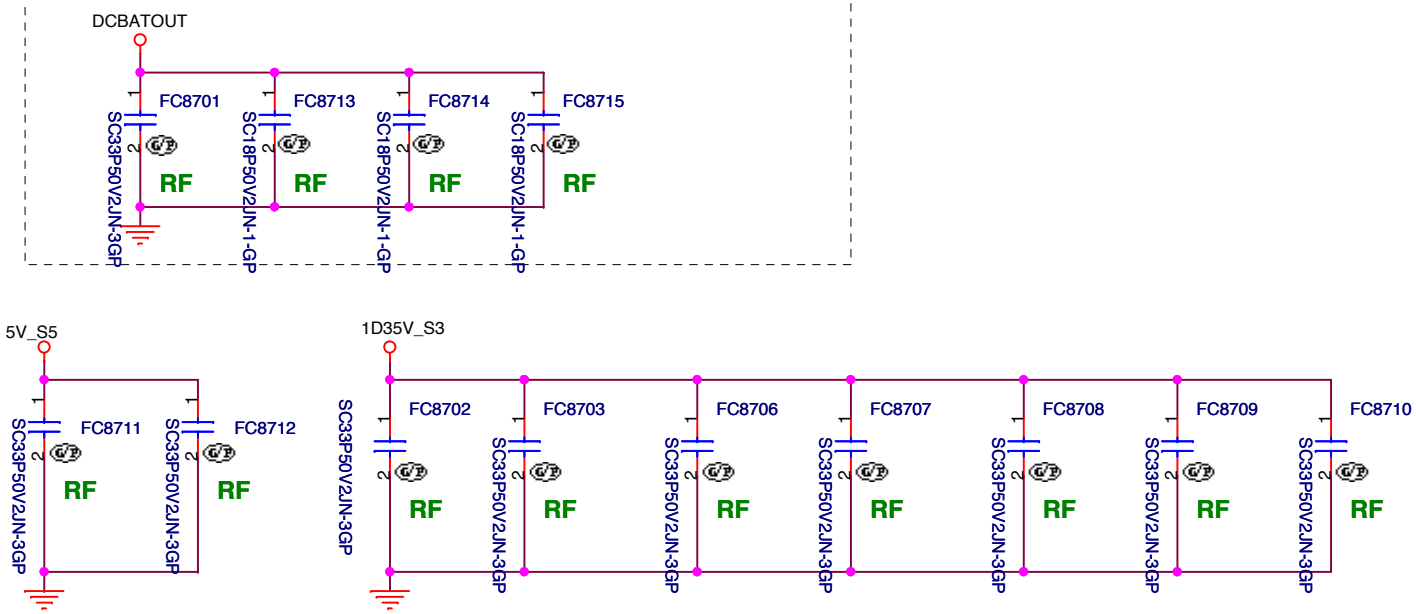
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: LT41 | Rev: -1

Date: Tuesday, January 20, 2015 | Sheet 86 of 102

10/19 add for RF



10/23 Delete FC8704,FC8705

BOM1

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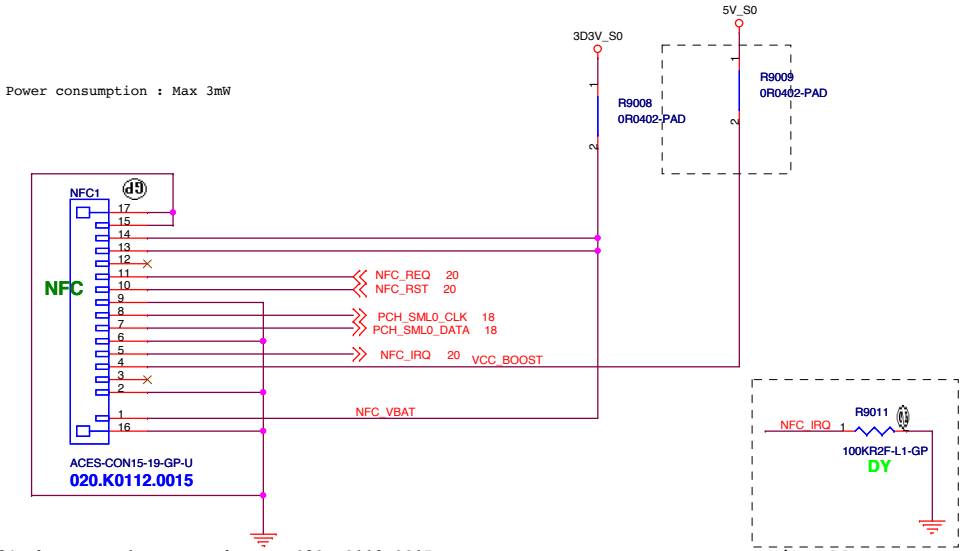
07/03 add R9009 5V_S0 Connect to NFC CONN Pin12 (SA板 未接)

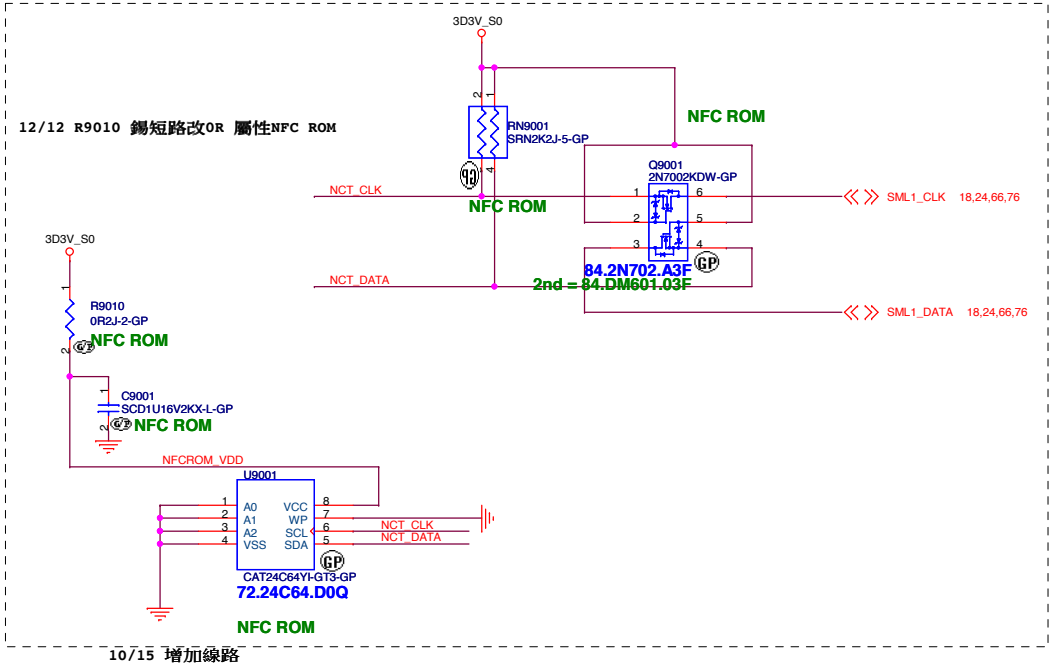


08/24 change NFC1 Part number to 020.K0112.0015

08/25 020.K0112.0015 新CONN, Pin腳整個反過來

12/3 add R9011 DY

12/12 R9010 錫短路改0R 屬性NFC ROM



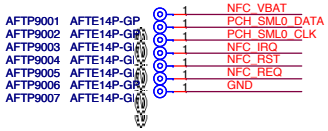
10/15 增加線路

10/15 U9001 料號記得要帶對,目前的不是要用的

10/16 NFC ROM都不上件,待驗證

07/07 add R9010 Connect to GND

07/21 Delete R9010 Connect to GND



NFC Module Pin Define

Suggestion Host Pin define (Use Sinbon FFC A9152420)

Pin#	Pin Name	Type	Refer	Description
1	VBAT	power	3.3V	Power supply voltage
2	GND	Power	GND	Ground
3	SWP	IO	-	SIM Card data
4	VCC_BOOST	Power	5V	Booster supply
5	IRQ	O	PVDD	Interrupt
6	PMUVCC	Power	connect to outside SE power or GND (no SE)	UICC power input from external PMU
7	I2C_SDA	I/O	PVDD	I2C Serial Data Line
8	I2C_SCL	I/O	PVDD	I2C Serial Clock Line
9	GND	Power	GND	Ground
10	VEN	I	GPIO Control (Normal 3.3V)	Enable/ disable LDO regulator / Reset
11	DWL_REQ	I	GPIO Control (Normal 0V)	Firmware download control pin
12	SIMVCC	Power	1.8V or N.C	Power output to supply the UICC
13	VBAT	Power	3.3V	Power supply voltage
14	PVDD	Power	3.3V	Pad supply voltage
15	GND	Power	GND	Ground

Pin#	Pin Name
15	VBAT
14	GND
13	SWP
12	VCC_BOOST
11	IRQ
10	PMUVCC
9	I2C_SDA
8	I2C_SCL
7	GND
6	VEN
5	DWL_REQ
4	SIMVCC
3	VBAT
2	PVDD
1	GND

BOM1

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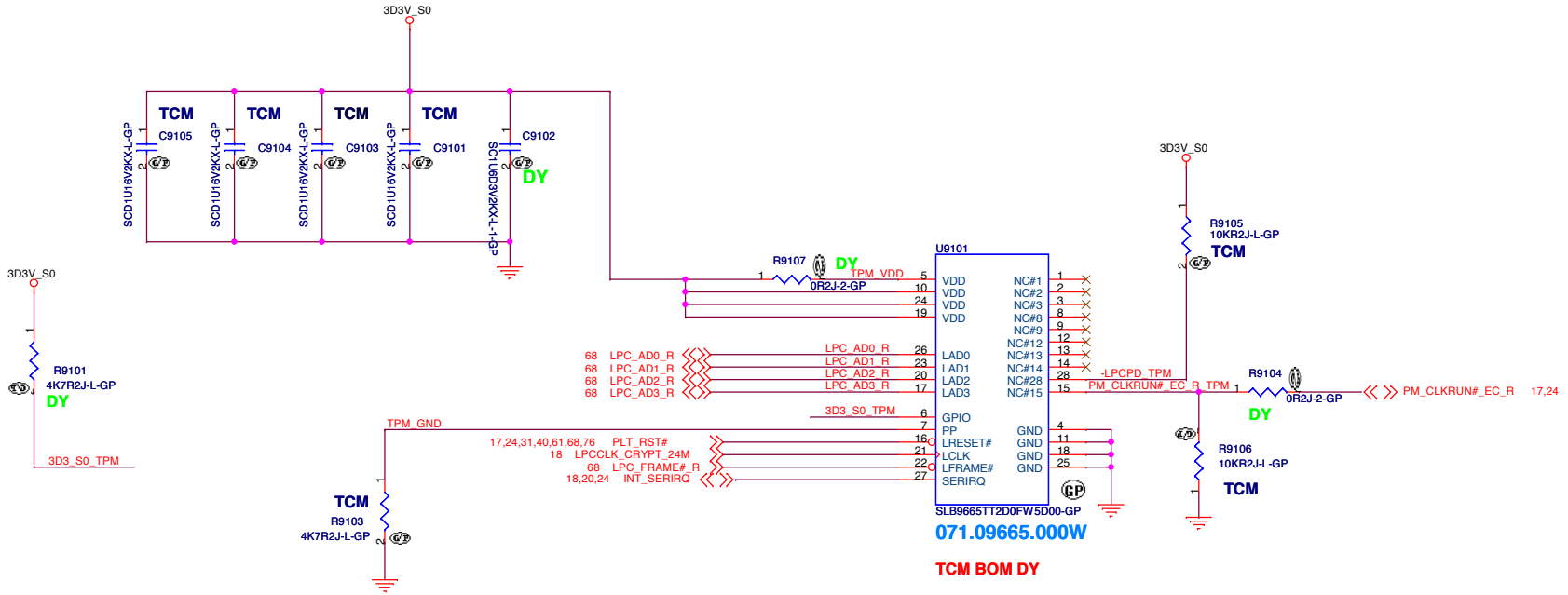

06/10 國民IC Pin5, Pin6 NC
Pin 15 GND

06/25 因國民的IC, 還未有料號,所以先要SAMPLO,回來自己上件

M40

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GPU BOM CTRL		For Detail see P82
GPU	N16V-GM	N16S-GT
Lenovo P/N	071.0N16V.000U	071.0N16S.000U
OPS (UMA:DY)	V	V
PR8222	64.20025.L0L	64.20025.L0L
PR8206	64.20025.L0L	64.20025.L0L
PR8208	64.20015.6DL	64.20015.6DL
PR8209	64.18025.6DL	64.18025.6DL
PR8204	63.R0034.1DL	63.R0034.1DL
PC8223	78.27224.2FL	78.27224.2FL

VRAM BOM CTRL	(Default Setting:900MHZ)								
Lenovo P/N		1101018	1100788	1100897	1101028	1101019	1100661	1100677	
IC Vendor		Micron	Hynix	Hynix	Samsung	Samsung	Micron	Micron	
IC Vendor P/N		MT41J256M16HA-093G:E N15S-GT only	H5TC2G63FFR-11C N15V-GM/N15S-GT	H5TC4G63AFR-11C N15V-GM/N15S-GT	K4W2G1646Q-BC1A N15V-GM/N15S-GT	K4W4G1646D-BC1A N15V-GM/N15S-GT	MT41J128M16JT-093G:K N15S-GT only	MT41K256M16HA-107G:E N15V-GM only	
RANK0 VRAM1,VRAM2,VRAM5,VRAM6		Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB		
RANK1 VRAM3,VRAM4,VRAM7,VRAM8		Stuff with Discrete 4GB		Stuff with Discrete 4GB		Stuff with Discrete 4GB			
R7642(Strap0-L)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L				
R7631(Strap0-H)		N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N16S-GT:64.49925.6DL N16V-GM:064.45325.06DV	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	
R7643(Strap1-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DV		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7632(Strap1-H)					N15V-GM:64.10025.L0L				
R7644(Strap2-L)						N15V-GM:64.10025.L0L			
R7633(Strap2-H)			N15V-GM:64.10025.L0L	N16V-GM:64.10025.L0L	N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L	
R7645(Strap3-L)				N16V-GM:64.49915.6DL					
R7635(Strap3-H)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7646(Strap4-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DV	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7634(Strap4-H)									
R7639(ROM_SI-L)		N15S-GT:64.24925.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.20025.L0L	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L N15S-GT:64.30025.6DL		N15V-GM:64.10025.L0L	
R7636(ROM_SI-H)			N15S-GT:64.10025.L0L		N15S-GT:64.20025.L0L		N15S-GT:64.15025.6DL		
R7640(ROM_SO-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N16S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	
R7637(ROM_SO-H)				N16V-GM:64.49915.6DL					
R7641(ROM_SCLK-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N16S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L N15S-GT:64.49915.6DL	N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	
R7638(ROM_SCLK-H)				N16V-GM:64.49915.6DL					

BOM1

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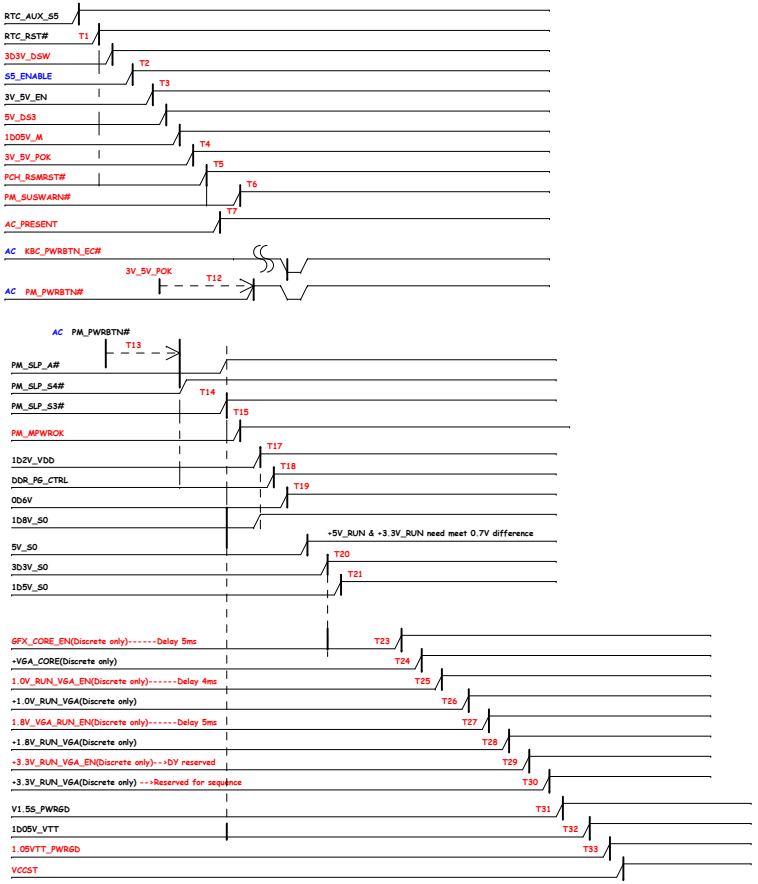
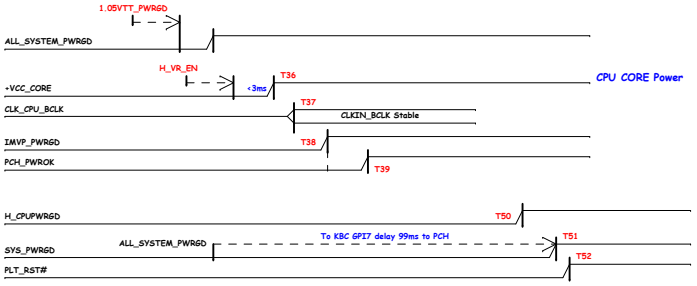
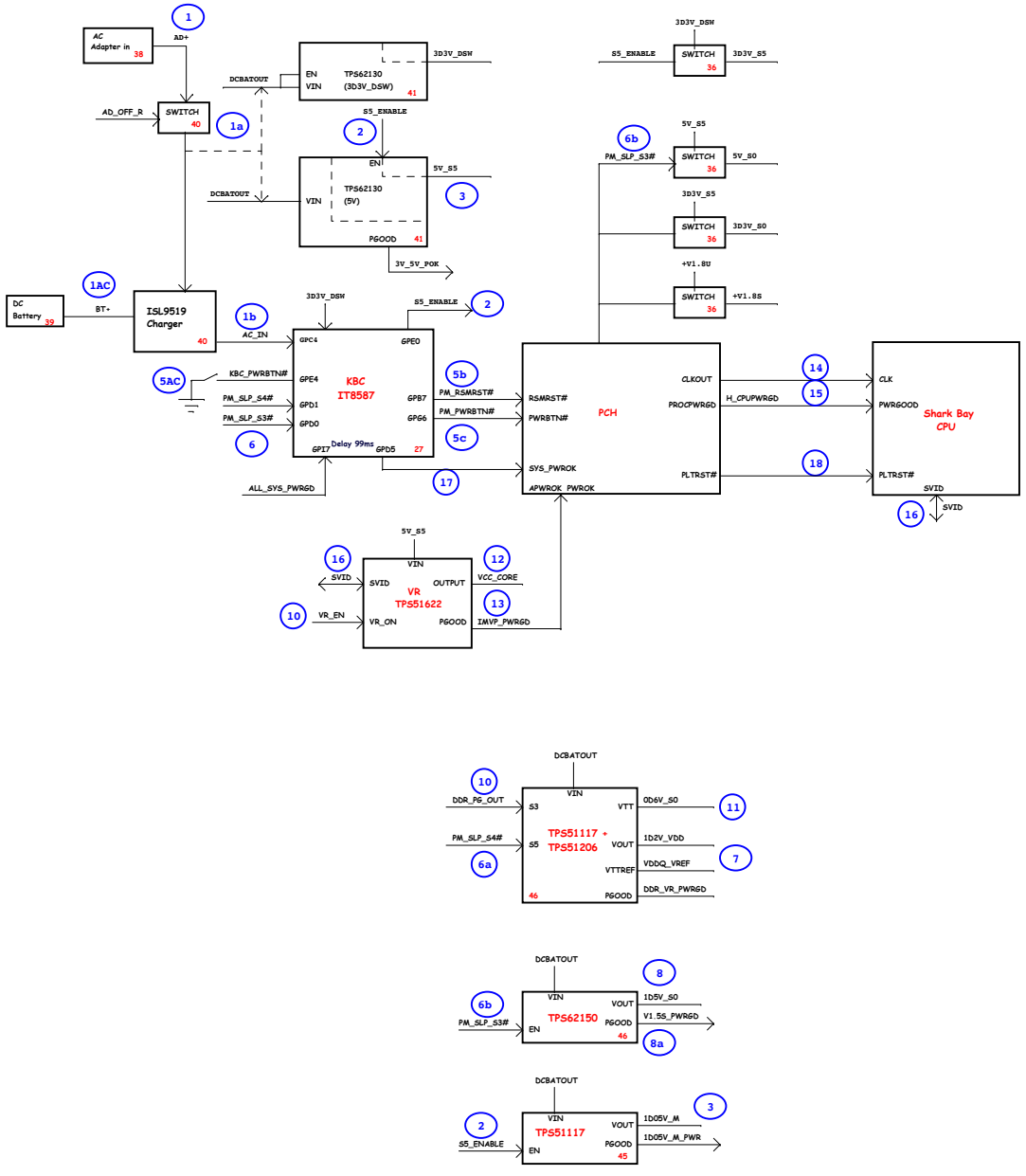
Intel-Power Up Sequence

(AC mode)





SHARK BAY POWER UP SEQUENCE DIAGRAM



Power Sequence

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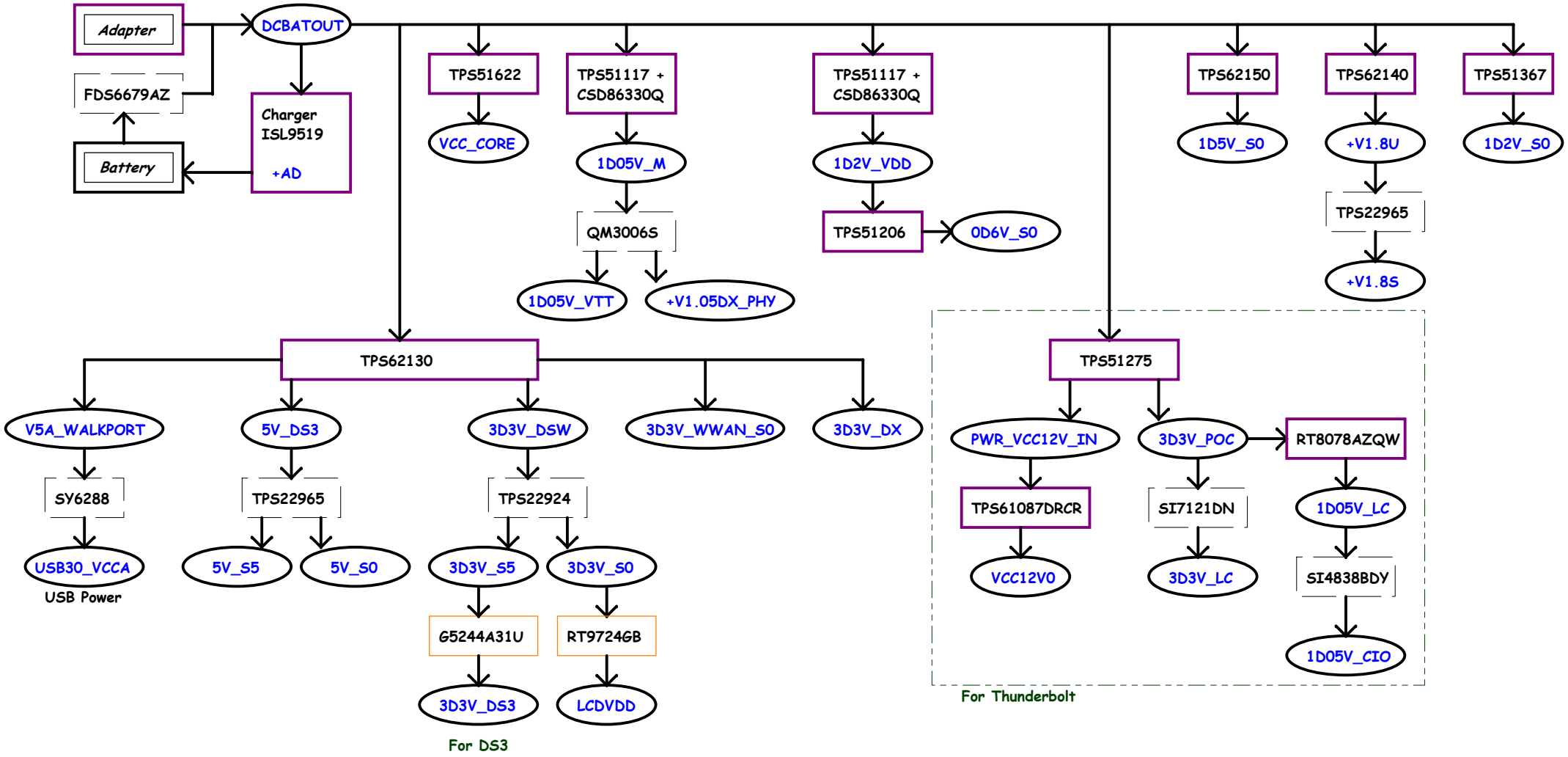

Power Shape

Regulator | LDO | Switch

BOM1

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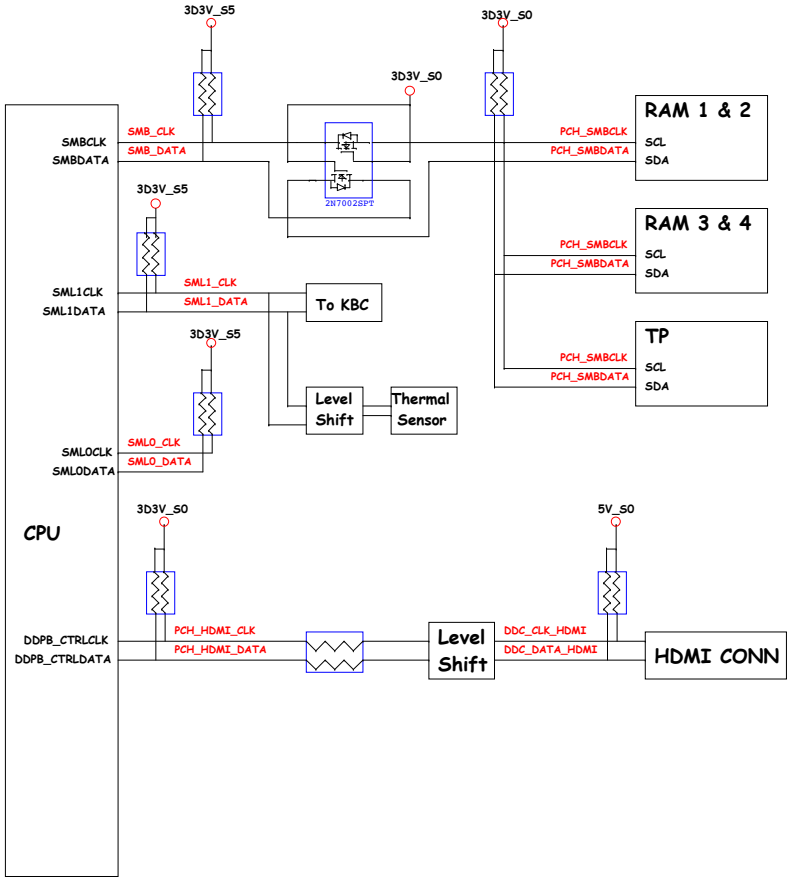
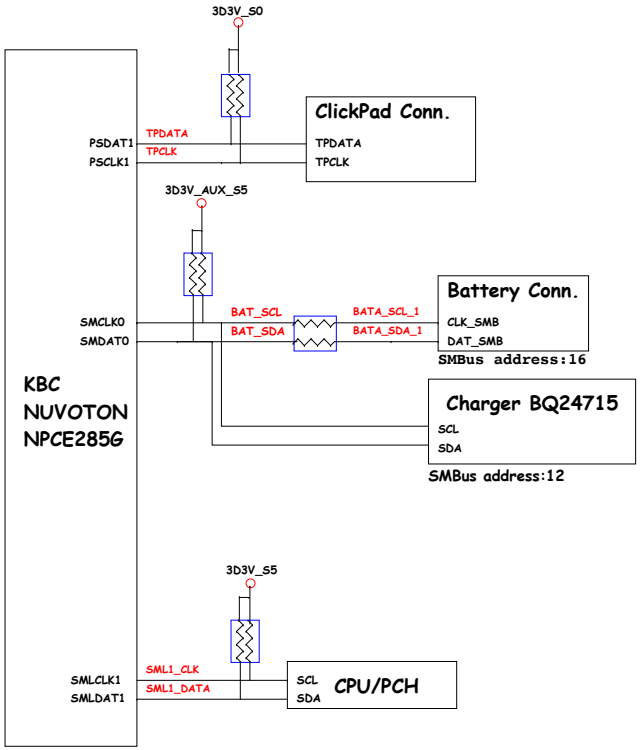
CPU/PCH SMBus Block Diagram



KBC SMBus Block Diagram



BOM1

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Title: SMBUS BLOCK DIAGRAM

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