Round Rock MLK 13.3" Schematics Document
Broadwell ULT

2015-08-19
REV : A00

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

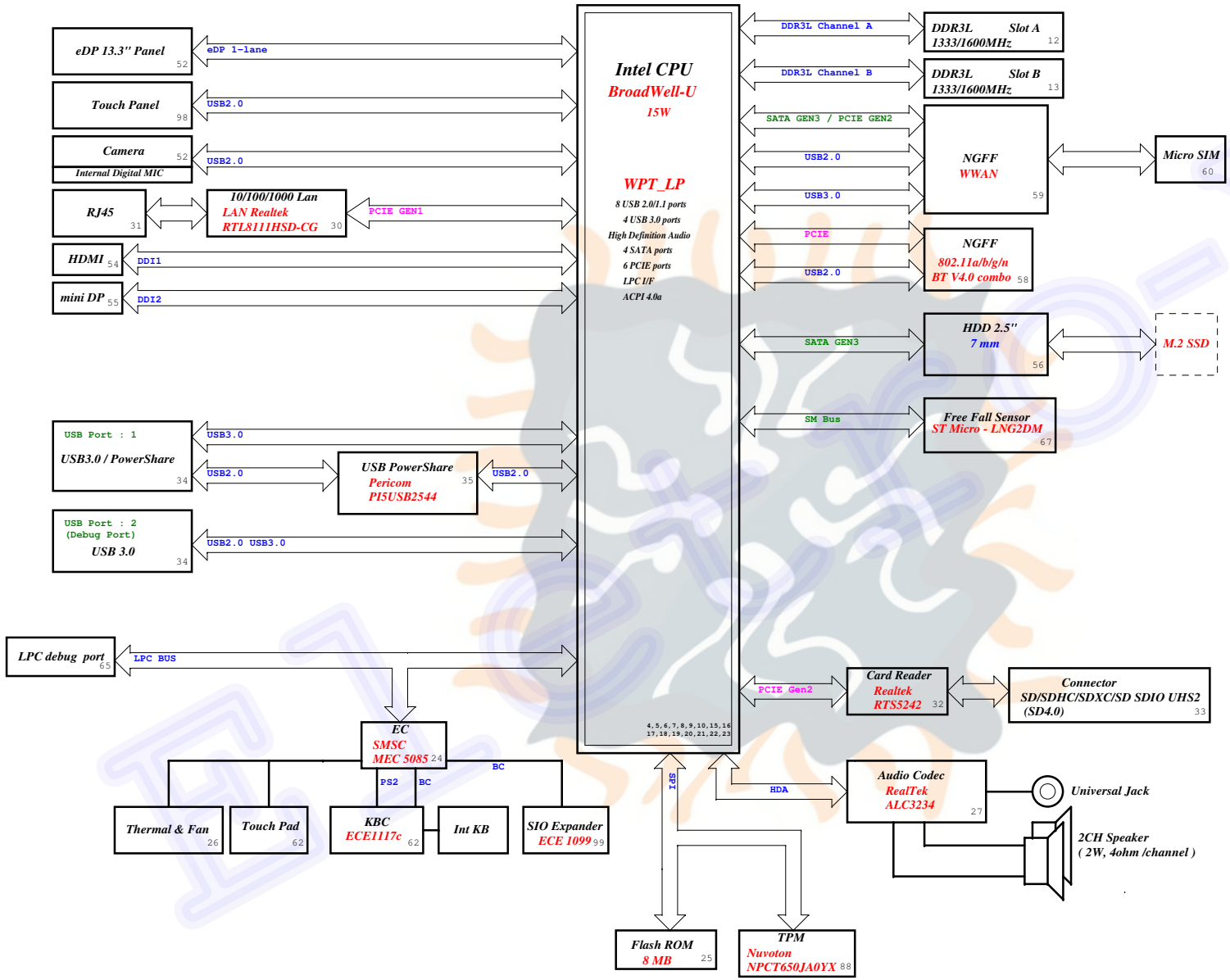
Title: Cover Page

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Wednesday, August 19, 2015 | Sheet 1 of

Round Rock MLK 13.3" Block Diagram

Project code : 4PD06F010001
PCB P/N : 15203
Revision : A00



CHARGER BQ24777 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5

CPU DC/DC TPS51624 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC SY8206DQNC 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M

SYSTEM DC/DC SY8206DQNC & APL5338 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

Load Switches 36	
INPUTS	OUTPUTS
5V_S5 3D3V_S5 1D05V_M	5V_S0 3D3V_S0 3D3V_S5_PCH 3D3V_M 3D3V_LAN 1D05V_MODPHY 1D05V_S0

PCB LAYER(FR4-6 Layer)	
L1:Top L2:PWR/GND L3:Signal L4:Signal L5:PWR/GND	L6:Bottom

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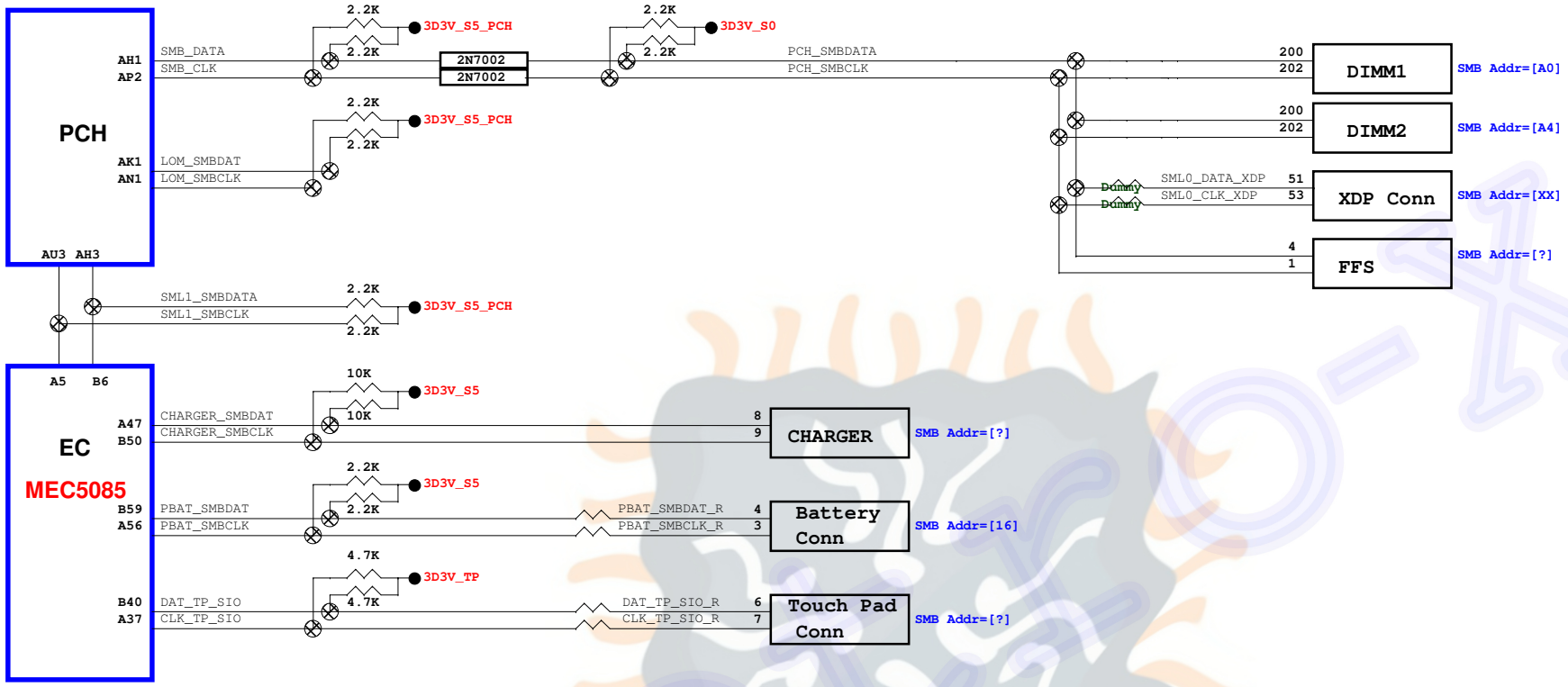
Title: Block Diagram
Size: A2
Document Number: Round Rock MLK 13.3"
Rev: A00
Date: Monday, August 17, 2015
Sheet 2



<Core Design>

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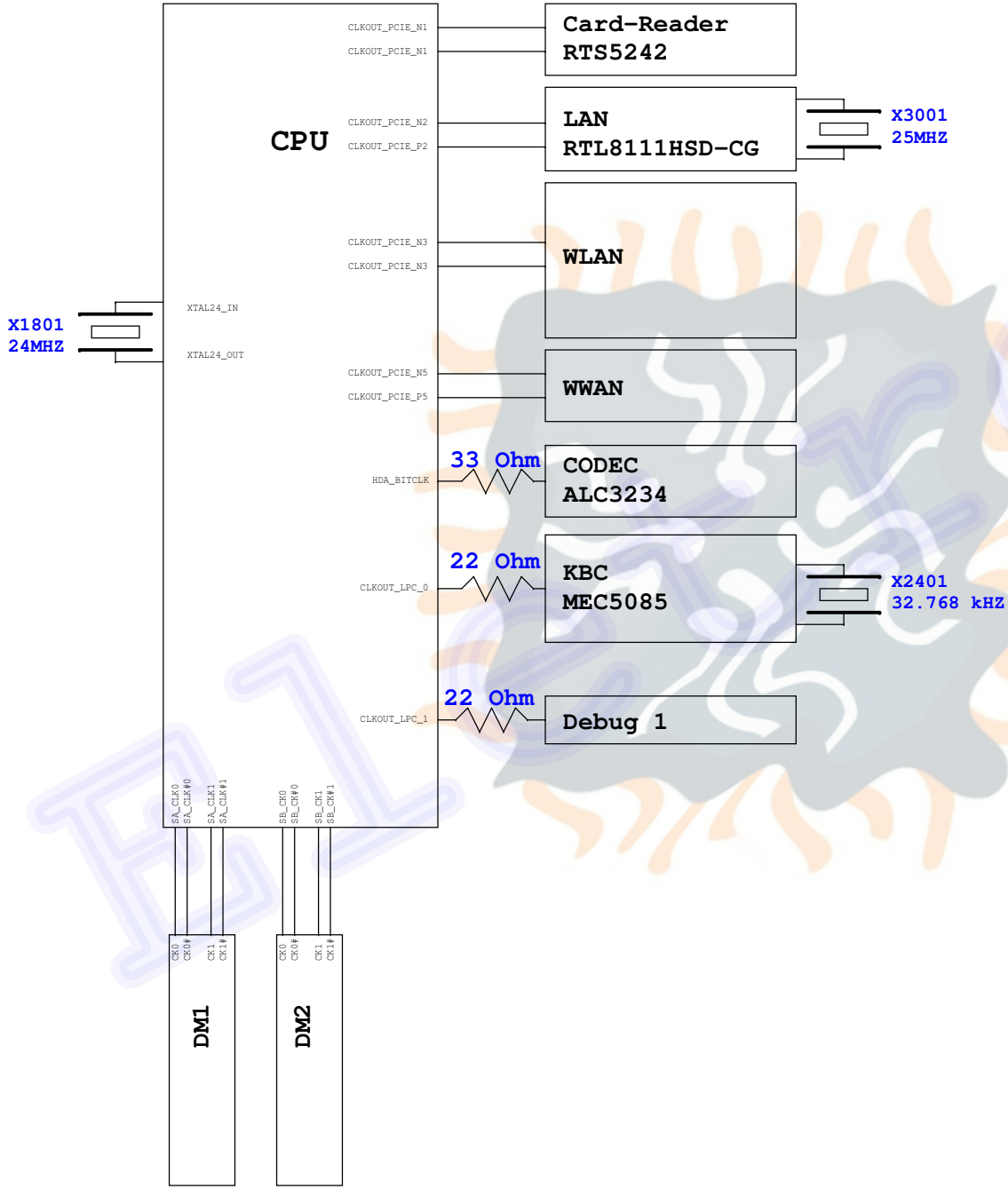
Title: SMBUS Block Diagram
Size: Document Number: Rev: A02
Round Rock MLK 13.3"
Date: Monday, August 17, 2015 Sheet 104

SSID = User.Interface

Regulatory model:P47G
Regulatory Type:P47G002;Latitude 3350



<Core Design>

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Title: CLK Block
Size: A3
Document Number: Round Rock MLK 13.3"
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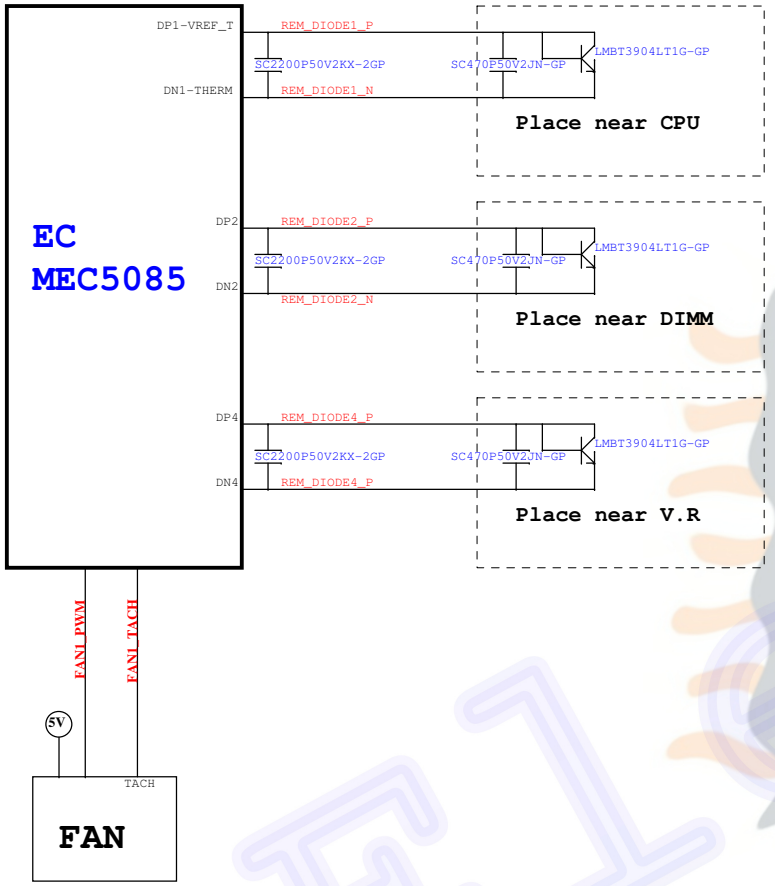
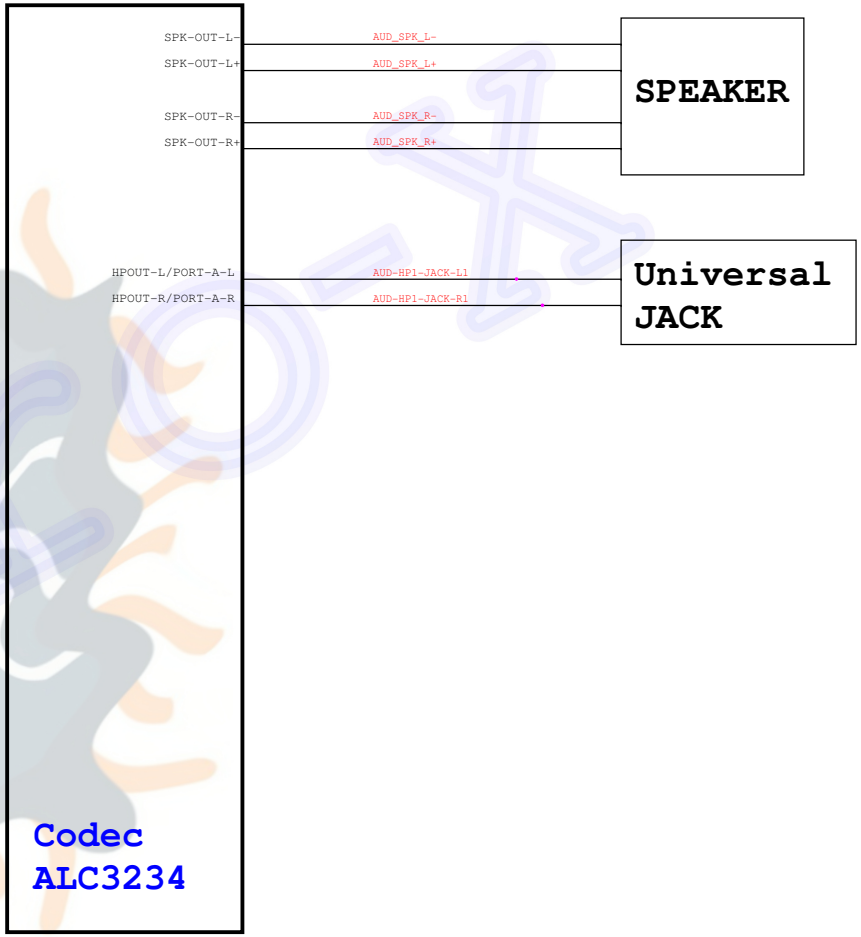
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title	Thermal/Audio Block Diagram	
Size	Document Number: Round Rock MLK 13.3"	Rev: A00
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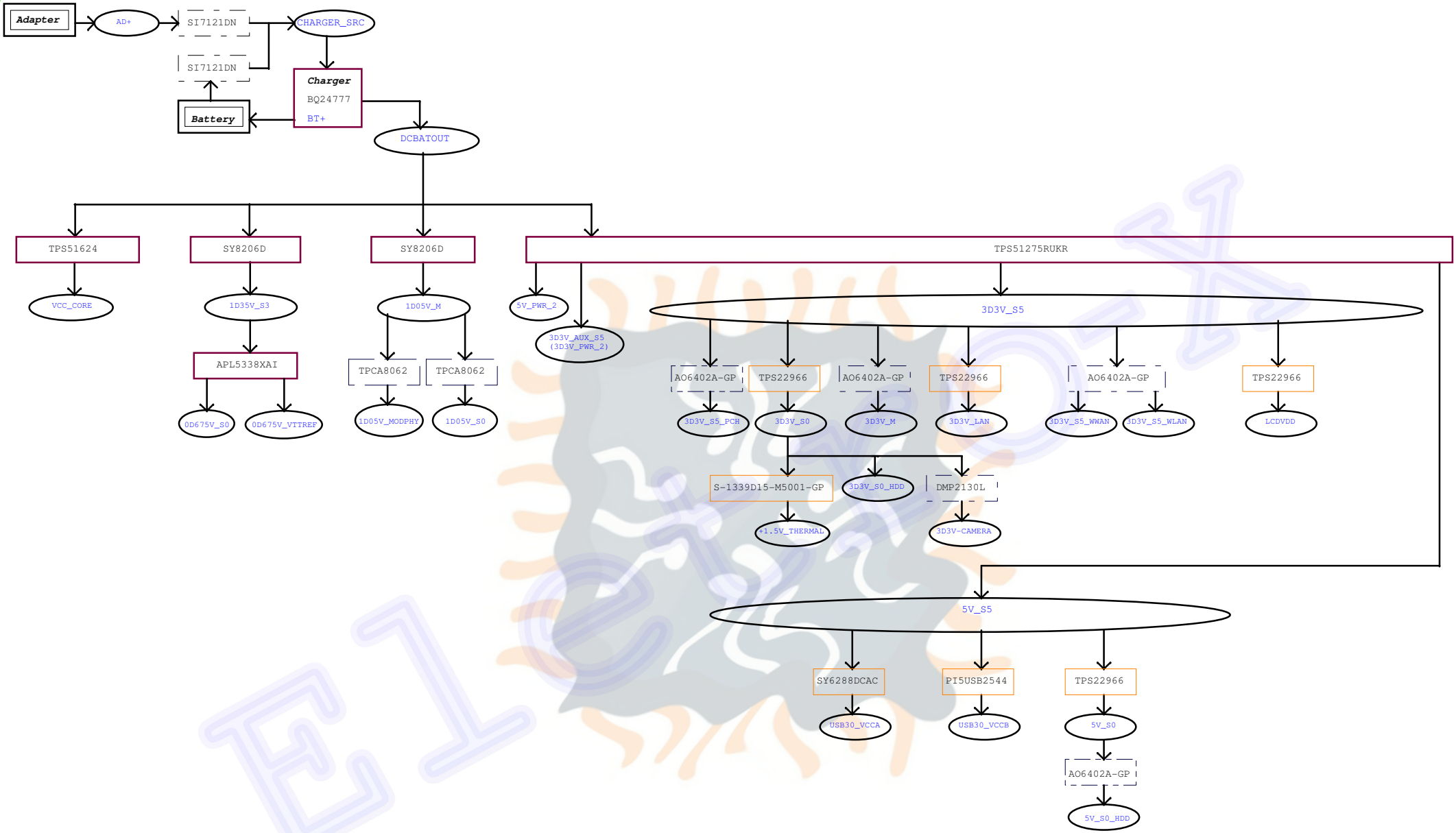

<Core Design>

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Title: Power Block Diagram

Size | Document Number: Round Rock MLK 13.3" | Rev: A02

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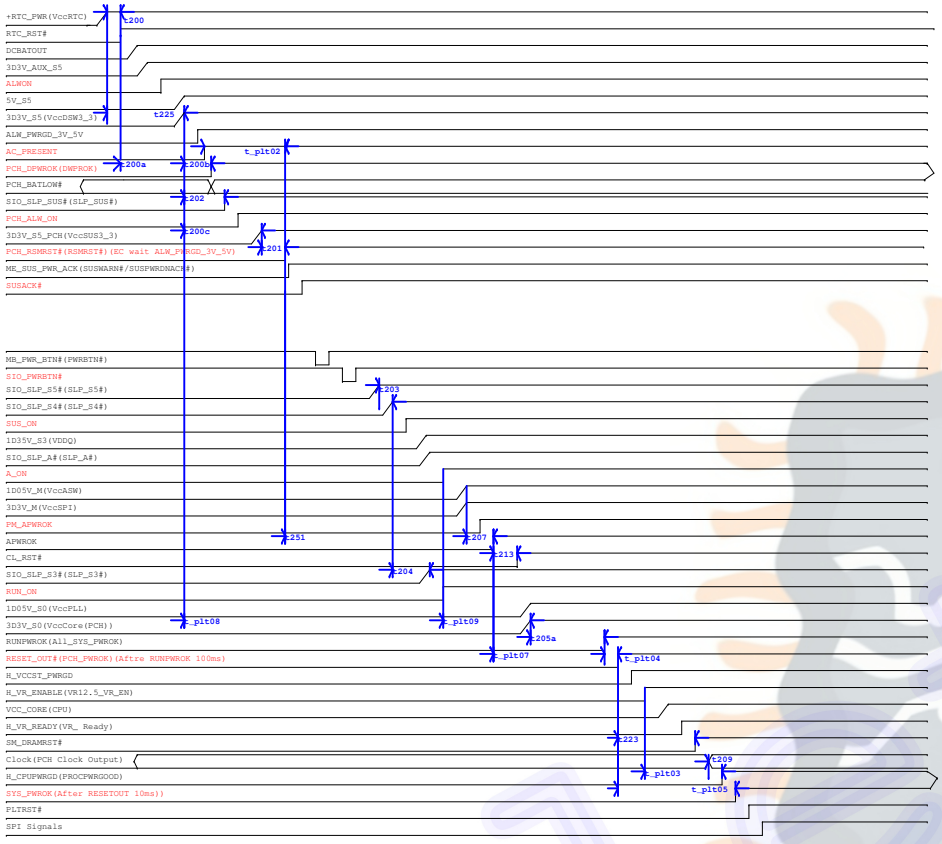
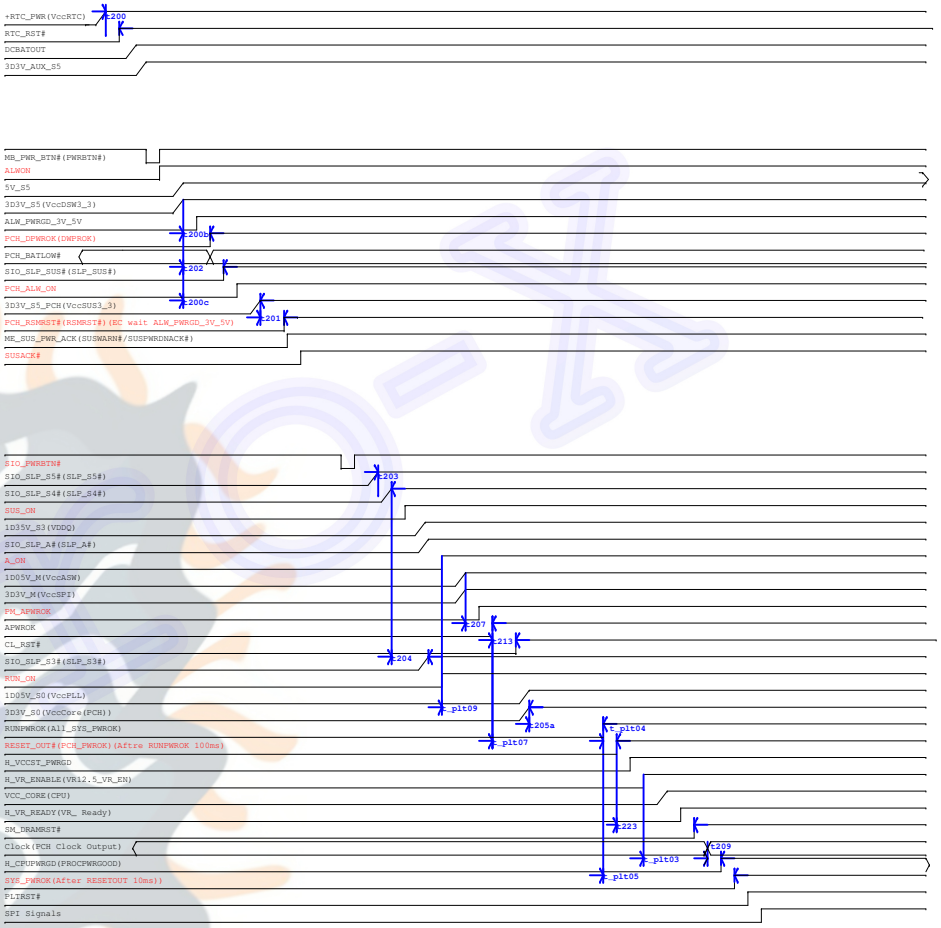
Intel-Power Up Sequence

(AC mode) Red word: KBC GPIO

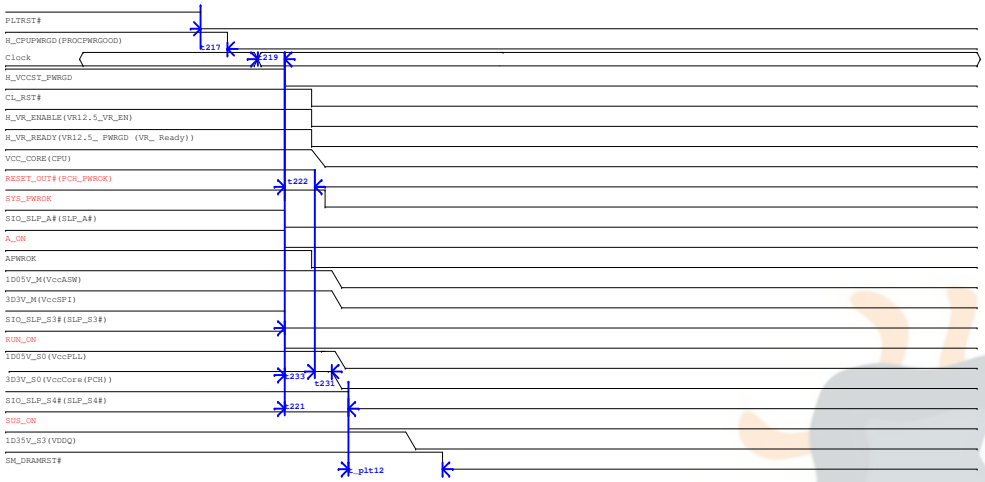


(DC mode) Red word: KBC GPIO

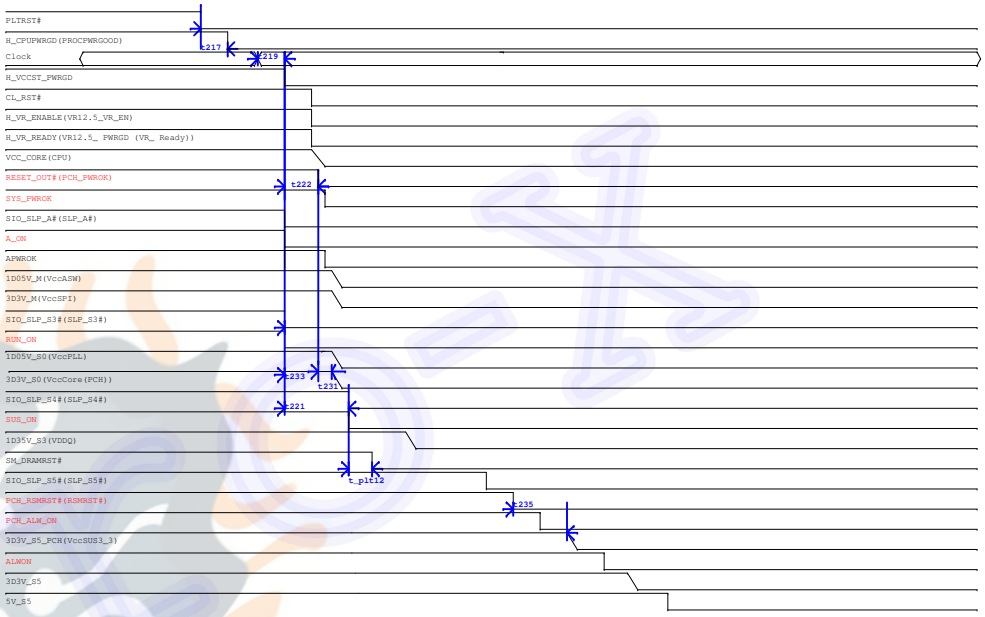


Intel-Power Down Sequence

(AC mode) red word: KBC GPIO



(DC mode) red word: KBC GPIO



SSID = CPU

+V1.05S_VCCST

R401 1 2 62R2J-GP H_PROCHOT#

CPU1B HSW_ULT_DDR3L 2 OF 19

24 H_PECI R402 1 2 0R0402-PAD-2-GP TP402 1 H_CATERR# H_PECI_R

D61 PROC_DETECT#
K62 CATERR#
N62 PECI
MISC

24,44,46 H_PROCHOT# R404 1 2 56R2J-4-GP H_PROCHOT#_R K63

PROCHOT#
THERMAL

SM_DRAMRST#

R405 1 2 10KR2J-3-GP H_CPUPWRGD C61

PROCPWRGD
PWR

ED401 AZ5725-01FDR7G-GP DY EV EMC

EC401 SC1KP50V2KX-1GP DY

SM_RCOMP_0 AU60
SM_RCOMP_1 AV60
SM_RCOMP_2 AU61
SM_DRAMRST# AV15
AV61

SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST#
SM_PG_CNTL1
DDR3L

14 DDR_PG_CTRL

PRDY# J62 XDP_PRDY# 96
PREQ# K62 XDP_PREQ# 96
PROC_TCK E60 XDP_TCK 96
PROC_TMS E61 XDP_TMS 96
PROC_TRST# E59 XDP_TRST# 19,96
PROC_TDI F63 XDP_TDI 96
PROC_TDO F62 XDP_TDO 96
JTAG

BPM#0 J60 XDP_BPM0 XDP_BPM0 96
BPM#1 H60 XDP_BPM1 XDP_BPM1 96
BPM#2 H61 XDP_BPM2 TP401
BPM#3 H62 XDP_BPM3 TP403
BPM#4 K59 XDP_BPM4 TP404
BPM#5 H63 XDP_BPM5 TP405
BPM#6 K60 XDP_BPM6 TP406
BPM#7 J61 XDP_BPM7 TP407

GP

HASWELL-6-GP-U

71.HASWE.G0U

+V1.05S_VCCST

XDP_TMS R406 1 XDP 2 51R2J-GP
XDP_TDI R407 1 XDP 2 51R2J-GP
XDP_TDO R409 1 2 51R2J-GP

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

R408 1 200R2F-L-GP SM_RCOMP_0
R410 1 121R2F-GP SM_RCOMP_1
R411 1 2 100R2F-L1-GP-U SM_RCOMP_2

EV follow PDG

XDP_TCK R412 1 XDP 2 51R2J-GP
XDP_TRST# R413 1 2 51R2J-GP

EC402 SC1KP50V2KX-1GP DY EV EMC

XDP_BPM0 R414 1 DY 2 0R2J-GP XDP_BPM1

Layout Note: Colse to DIMM

1D35V_S3

R415 470R2J-2-GP

SM_DRAMRST# R416 1 0R0402-PAD-2-GP DDR3_DRAMRST#_1 12
R417 1 0R0402-PAD-2-GP DDR3_DRAMRST#_2 13

<Core Design>

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Title: CPU (THERMAL/CLOCK/PM)

Size: A4 | Document Number: Round Rock MLK 13.3" | Rev: A00

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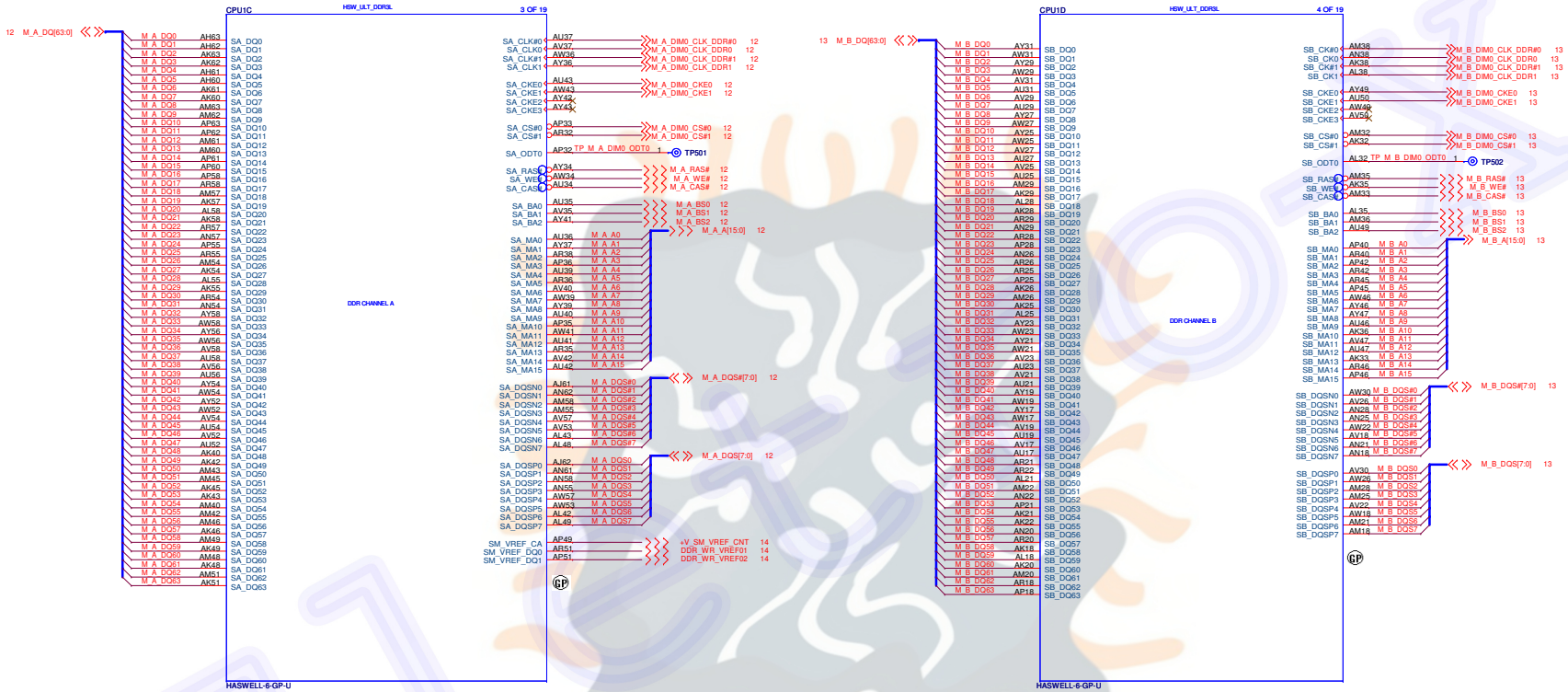
SSID = CPU



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Title: CPU (DDR)

Size: A2 | Document Number: Round Rock MLK 13" | Rev: 1.00

Date: Monday, August 17, 2015 | Sheet 5 of 40

SSID = CPU

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0:Lane Reversed 1:(Default) Normal Operation; No stall

CFG0 — R601 1KR2J-1-GP (DY)

PCH/PCH LESS MODE SELECTION	
CFG1	0:Lane Reversed 1:(Default) Normal Operation

CFG1 — R602 1KR2J-1-GP (DY)

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 — R606 1KR2J-1-GP

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

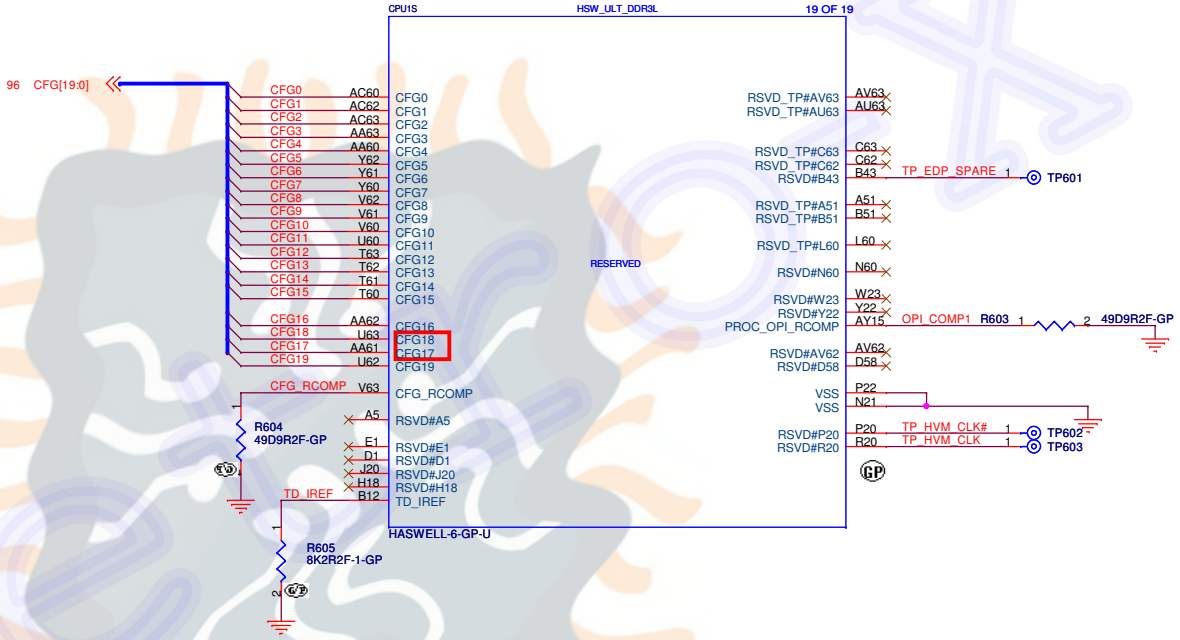
CFG8 — R607 1KR2J-1-GP (DY)

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

CFG9 — R608 1KR2J-1-GP (DY)

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

CFG10 — R609 1KR2J-1-GP (DY)



<Core Design>

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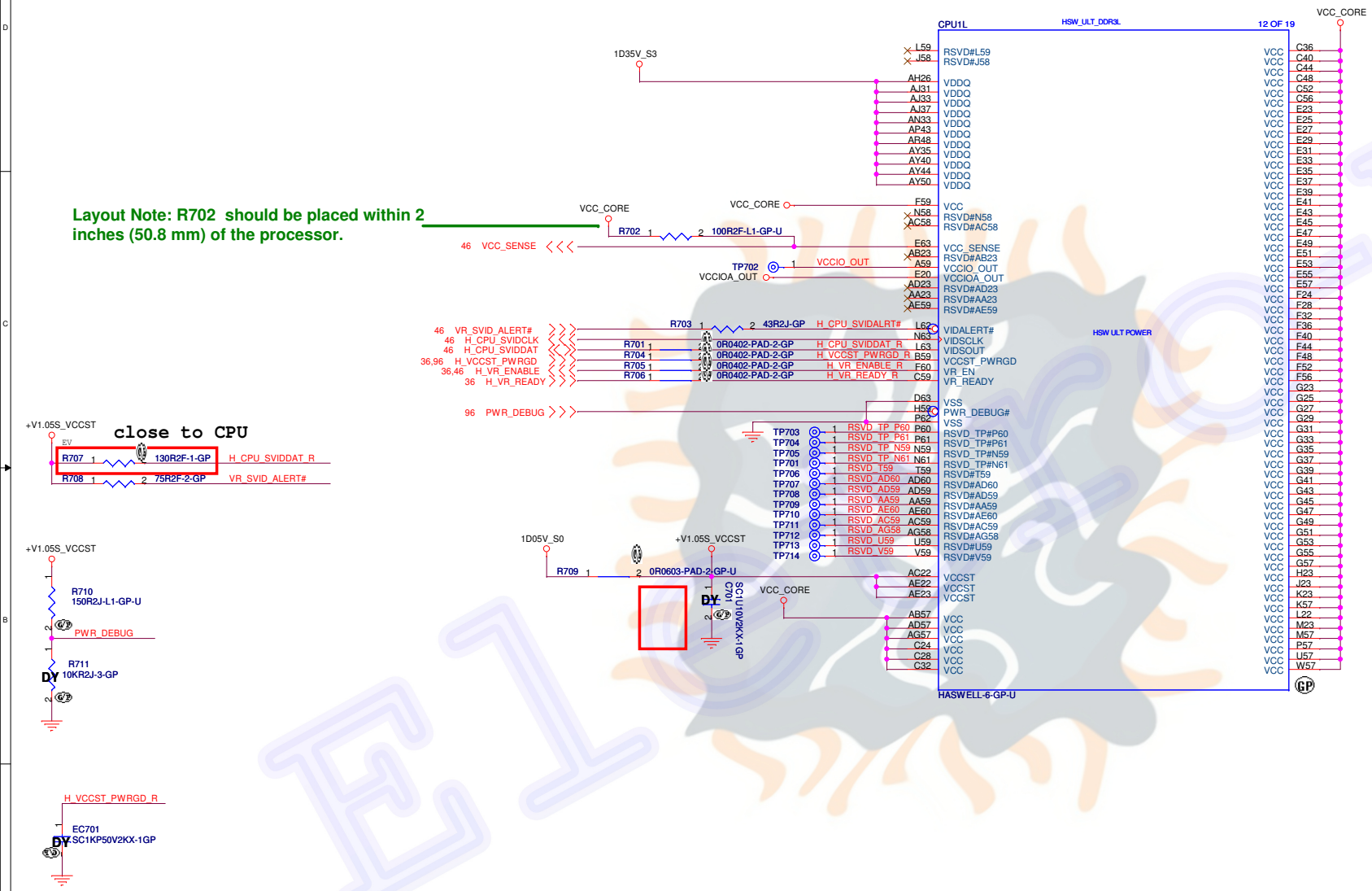
Title: CPU (XDP)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 6 of

SSID = CPU



<Core Design>

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Round Rock MLK 13.3" | Rev: A00

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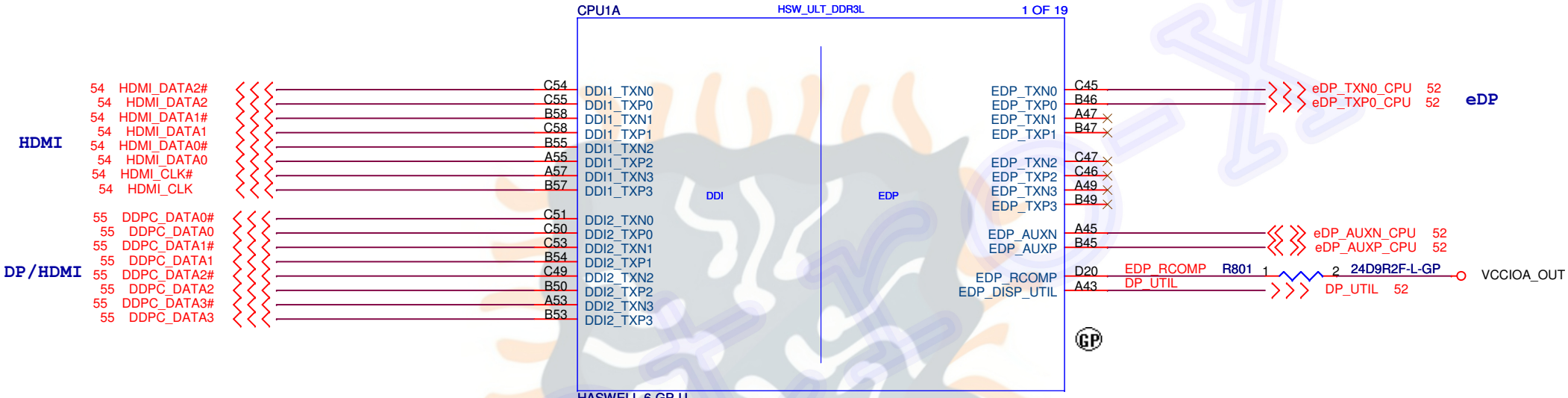
SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CK_N	DP_LANE3_N
DDI_TXP3	HDMI_CK_P	DP_LANE3_P

<Core Design>

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Title: CPU (DDI/EDP)

Size: A4 | Document Number: Round Rock MLK 13.3" | Rev: A00

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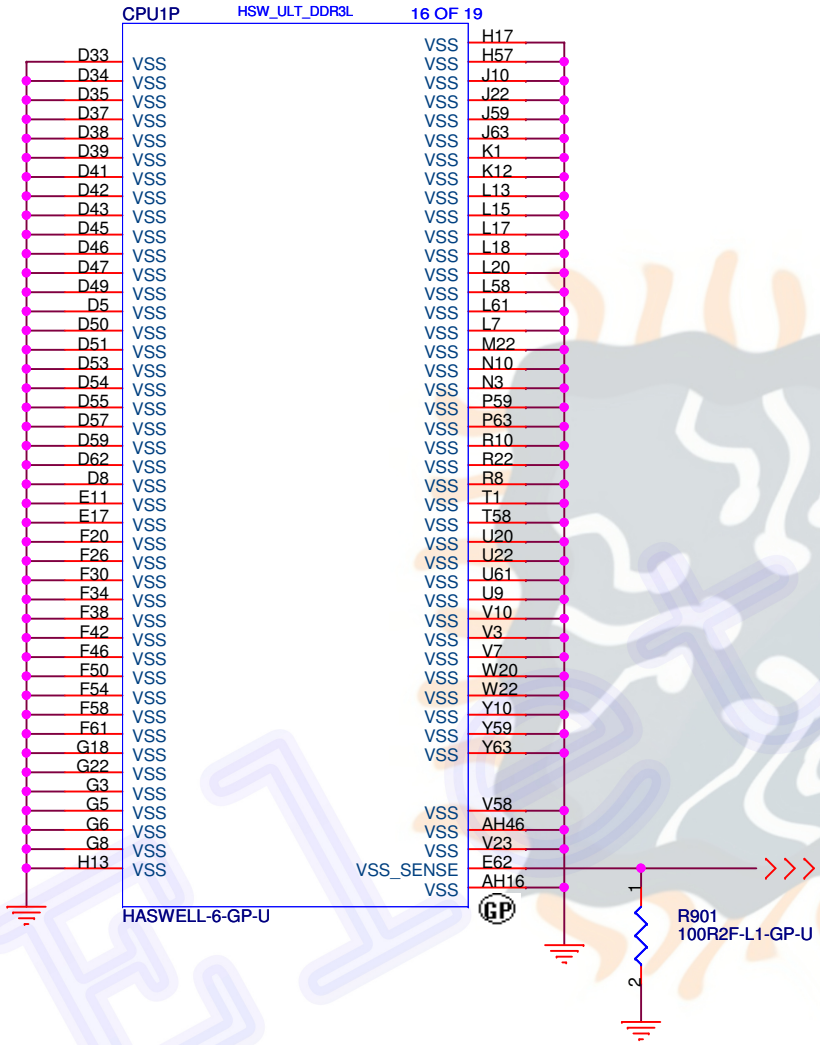
SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

<Core Design>

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Title: CPU (VSS)

Size	Document Number	Rev
A4	Round Rock MLK 13.3"	A00

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SSID = MEMORY

Layout Note:
Place these caps close to VREF_CA

M_VREF_CA_DIMMA

C1201 SCD1U16V2KX-3GP (DY) EC1 SCD1U16V2KX-3GP C1202 SCD1U16V2KX-3GP

Layout Note:
Place these caps close to VREF_DQ

M_VREF_DQ_DIMMA

C1204 SCD1U16V2KX-3GP (DY) C1205 SC2R2U10V3KX-1GP C1206 SCD1U16V2KX-3GP

0D675V_S0

Place these caps close to VTT1 and VTT2.

C1217 SCU1U10V2KX-1GP (DY) C1218 SCU1U10V2KX-1GP C1219 SCU1U10V2KX-1GP

DQS1	DQ0 M_A_DQ13 DQ1 M_A_DQ8 DQ2 M_A_DQ14 DQ3 M_A_DQ10 DQ4 M_A_DQ9 DQ5 M_A_DQ12 DQ6 M_A_DQ15 DQ7 M_A_DQ11
DQS3	DQ8 M_A_DQ29 DQ9 M_A_DQ28 DQ10 M_A_DQ30 DQ11 M_A_DQ31 DQ12 M_A_DQ25 DQ13 M_A_DQ24 DQ14 M_A_DQ27 DQ15 M_A_DQ26
DQS5	DQ16 M_A_DQ44 DQ17 M_A_DQ41 DQ18 M_A_DQ43 DQ19 M_A_DQ47 DQ20 M_A_DQ45 DQ21 M_A_DQ40 DQ22 M_A_DQ42 DQ23 M_A_DQ46
DQS6	DQ24 M_A_DQ51 DQ25 M_A_DQ50 DQ26 M_A_DQ49 DQ27 M_A_DQ48 DQ28 M_A_DQ52 DQ29 M_A_DQ53 DQ30 M_A_DQ54 DQ31 M_A_DQ55
DQS0	DQ32 M_A_DQ0 DQ33 M_A_DQ1 DQ34 M_A_DQ2 DQ35 M_A_DQ6 DQ36 M_A_DQ5 DQ37 M_A_DQ4 DQ38 M_A_DQ3 DQ39 M_A_DQ7
DQS2	DQ40 M_A_DQ21 DQ41 M_A_DQ20 DQ42 M_A_DQ17 DQ43 M_A_DQ16 DQ44 M_A_DQ18 DQ45 M_A_DQ19 DQ46 M_A_DQ22 DQ47 M_A_DQ23
DQS4	DQ48 M_A_DQ36 DQ49 M_A_DQ33 DQ50 M_A_DQ34 DQ51 M_A_DQ38 DQ52 M_A_DQ37 DQ53 M_A_DQ32 DQ54 M_A_DQ35 DQ55 M_A_DQ39
DQS7	DQ56 M_A_DQ62 DQ57 M_A_DQ58 DQ58 M_A_DQ60 DQ59 M_A_DQ61 DQ60 M_A_DQ63 DQ61 M_A_DQ59 DQ62 M_A_DQ56 DQ63 M_A_DQ57

DM1

5 M_A_A[15:0] — M_A_A0..M_A_A15 — A0..A16/BA2

5 M_A_BS2 — BA0, BA1

5 M_A_BS0, 5 M_A_BS1

5 M_A_DQ[63:0] — M_A_DQ13, M_A_DQ8, M_A_DQ14, M_A_DQ10, M_A_DQ9, M_A_DQ12, M_A_DQ15, M_A_DQ11, M_A_DQ29, M_A_DQ28, M_A_DQ30, M_A_DQ31, M_A_DQ25, M_A_DQ24, M_A_DQ27, M_A_DQ26, M_A_DQ44, M_A_DQ41, M_A_DQ43, M_A_DQ47, M_A_DQ45, M_A_DQ40, M_A_DQ42, M_A_DQ46, M_A_DQ51, M_A_DQ50, M_A_DQ49, M_A_DQ48, M_A_DQ52, M_A_DQ53, M_A_DQ54, M_A_DQ55, M_A_DQ0, M_A_DQ1, M_A_DQ2, M_A_DQ6, M_A_DQ5, M_A_DQ4, M_A_DQ3, M_A_DQ7, M_A_DQ21, M_A_DQ20, M_A_DQ17, M_A_DQ16, M_A_DQ18, M_A_DQ19, M_A_DQ22, M_A_DQ23, M_A_DQ36, M_A_DQ33, M_A_DQ34, M_A_DQ38, M_A_DQ37, M_A_DQ32, M_A_DQ35, M_A_DQ39, M_A_DQ62, M_A_DQ58, M_A_DQ60, M_A_DQ61, M_A_DQ63, M_A_DQ59, M_A_DQ56, M_A_DQ57 — DQ0..DQ63

5 M_A_DQS#[7:0] — M_A_DQS#1, M_A_DQS#3, M_A_DQS#5, M_A_DQS#6, M_A_DQS#0, M_A_DQS#2, M_A_DQS#4, M_A_DQS#7 — DQS0#..DQS7#

5 M_A_DQS[7:0] — M_A_DQS1, M_A_DQS3, M_A_DQS5, M_A_DQS6, M_A_DQS0, M_A_DQS2, M_A_DQS4, M_A_DQS7 — DQS0..DQS7

14 M_A_DIM0_ODT0, 14 M_A_DIM0_ODT1 — ODT0, ODT1

M_VREF_CA_DIMMA — VREF_CA

M_VREF_DQ_DIMMA — VREF_DQ

4 DDR3_DRAMRST#_1 — RESET#

SCD1U16V2KX-3GP (DY) C1220 — 0D675V_S0 — VTT1, VTT2

H =4mm

DDR3-204P-106-GP-U
62.10017.X31
2nd = 62.10024.M51

NP1, NP2

RAS# M_A_RAS# 5
WE# M_A_WE# 5
CAS# M_A_CAS# 5

CS0# M_A_DIM0_CS#0 5
CS1# M_A_DIM0_CS#1 5

CKE0 M_A_DIM0_CKE0 5
CKE1 M_A_DIM0_CKE1 5

CK0 M_A_DIM0_CLK_DDR0 5
CK0# M_A_DIM0_CLK_DDR#0 5

CK1 M_A_DIM0_CLK_DDR1 5
CK1# M_A_DIM0_CLK_DDR#1 5

DM0, DM1, DM2, DM3, DM4, DM5, DM6, DM7

SDA PCH_SMBDATA 13,18,67,96
SCL PCH_SMBCLK 13,18,67,96

EVENT#

VDDSPD — 3D3V_S0 — C1203 SCD1U16V2KX-3GP

SA0, SA1

NC#1, NC#2, NC#/TEST

1D35V_S3

VDD1..VDD18

VSS

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

1D35V_S3

DM1 DECOUPLING

C1208 C1209 C1210 C1211 C1212 C1213 C1214 C1222 — SC10U6D3V5MX-GP (DY)

Layout Note:
Place these Caps near DM1.

C1215 SCD1U16V2KX-3GP (DY) C1216 SCD1U16V2KX-3GP

<Core Design>

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Title: DDR3L-SODIMM1

Size: A2 | Document Number: Round Rock MLK 15.3" | Rev: 0A

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SSID = MEMORY

Layout Note:
Place these caps close to VREF_CA

M_VREF_CA_DIMMB

C1301 SCD1U16V2KX-3GP
EC2 SCD1U16V2KX-3GP
C1302 SCD1U16V2KX-3GP

Layout Note:
Place these caps close to VREF_DQ

M_VREF_DQ_DIMMB

C1305 SCD1U16V2KX-3GP
C1306 SCD1U16V2KX-3GP

0D675V_S0

Place these caps close to VTT1 and VTT2.

DY C1314 SC1U10V2KX-1GP
C1315 SC1U10V2KX-1GP
C1317 SC1U10V2KX-1GP

DQS1	DQ0 M_B_DQ8 DQ1 M_B_DQ14 DQ2 M_B_DQ10 DQ3 M_B_DQ11 DQ4 M_B_DQ12 DQ5 M_B_DQ9 DQ6 M_B_DQ13 DQ7 M_B_DQ15
DQS3	DQ8 M_B_DQ28 DQ9 M_B_DQ29 DQ10 M_B_DQ26 DQ11 M_B_DQ27 DQ12 M_B_DQ25 DQ13 M_B_DQ24 DQ14 M_B_DQ30 DQ15 M_B_DQ31
DQS5	DQ16 M_A_DQ40 DQ17 M_A_DQ41 DQ18 M_A_DQ46 DQ19 M_A_DQ42 DQ20 M_A_DQ45 DQ21 M_A_DQ44 DQ22 M_A_DQ47 DQ23 M_A_DQ43
DQS7	DQ24 M_A_DQ56 DQ25 M_A_DQ57 DQ26 M_A_DQ59 DQ27 M_A_DQ58 DQ28 M_A_DQ61 DQ29 M_A_DQ60 DQ30 M_A_DQ63 DQ31 M_A_DQ62
DQS0	DQ32 M_A_DQ4 DQ33 M_A_DQ1 DQ34 M_A_DQ3 DQ35 M_A_DQ7 DQ36 M_A_DQ5 DQ37 M_A_DQ0 DQ38 M_A_DQ2 DQ39 M_A_DQ6
DQS2	DQ40 M_A_DQ21 DQ41 M_A_DQ20 DQ42 M_A_DQ22 DQ43 M_A_DQ23 DQ44 M_A_DQ16 DQ45 M_A_DQ17 DQ46 M_A_DQ19 DQ47 M_A_DQ18
DQS4	DQ48 M_A_DQ36 DQ49 M_A_DQ33 DQ50 M_A_DQ35 DQ51 M_A_DQ39 DQ52 M_A_DQ37 DQ53 M_A_DQ32 DQ54 M_A_DQ34 DQ55 M_A_DQ38
DQS6	DQ56 M_A_DQ52 DQ57 M_A_DQ49 DQ58 M_A_DQ48 DQ59 M_A_DQ53 DQ60 M_A_DQ51 DQ61 M_A_DQ55 DQ62 M_A_DQ54 DQ63 M_A_DQ50

M_B_A[15:0] 5

5 M_B_BS2
5 M_B_BS0
5 M_B_BS1
5 M_B_DQ[63:0]

M_B_DQS#[7:0] 5
M_B_DQS[7:0] 5

14 M_B_DIM0_ODT0
14 M_B_DIM0_ODT1

M_VREF_CA_DIMMB
M_VREF_DQ_DIMMB

4 DDR3_DRAMRST#_2

DY C1323 SCD1U16V2KX-3GP
0D675V_S0

DM2

M_B_A0 98 … M_B_A15 79
M_B_DQ8 5 … M_B_DQ63 206
M_B_DQS#1 10 … M_B_DQS#8 186
M_B_DQS1 12 … M_B_DQS8 188

NP1 NP2
RAS# 110 — M_B_RAS# 5 — M_B_WE# 5
WE# 113 — M_B_CAS# 5
CAS# 115
CS0# 114 — M_B_DIM0_CS#0 5
CS1# 121 — M_B_DIM0_CS#1 5
CKE0 73 — M_B_DIM0_CKE0 5
CKE1 74 — M_B_DIM0_CKE1 5
CK0 101 — M_B_DIM0_CLK_DDR0 5
CK0# 103 — M_B_DIM0_CLK_DDR#0 5
CK1 102 — M_B_DIM0_CLK_DDR1 5
CK1# 104 — M_B_DIM0_CLK_DDR#1 5
BA0 109
BA1 108
DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187
SDA 200 — PCH_SMBDATA 12,18,67,96
SCL 202 — PCH_SMBCLK 12,18,67,96
EVENT# 198
VDDSPD 199 — 3D3V_S0
SA0 197
SA1 201 — SA1_DIM1 — R1301 1 10KR2J-3-GP — 2
NC#1 77
NC#2 122
NC#TEST 125
VDD1 75 … VDD18 124 — 1D35V_S3
VSS 2 … 206
VREF_CA 126
VREF_DQ 1
RESET# 30
VTT1 203
VTT2 204 — 0D675V_S0

DDR3-204P-106-GP-U
62.10017.X31
2nd = 62.10024.M51
H = 4mm

C1303 SCD1U16V2KX-3GP

1D35V_S3

DM2 DECOUPLING

DY C1307 SC10U6D3V3MX-GP
DY C1308 SC10U6D3V3MX-GP
C1309 SC10U6D3V3MX-GP
DY C1310 SC10U6D3V3MX-GP
C1311 SC10U6D3V3MX-GP
DY C1312 SC10U6D3V3MX-GP
C1313 SC10U6D3V3MX-GP
DY C1314 SC10U6D3V3MX-GP
DY TC1 ST330U2V0M-4-GP-U
C1321 SCD1U16V2KX-3GP

Layout Note:
Place these Caps near DM2

C1318 SCD1U16V2KX-3GP
C1319 SCD1U16V2KX-3GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

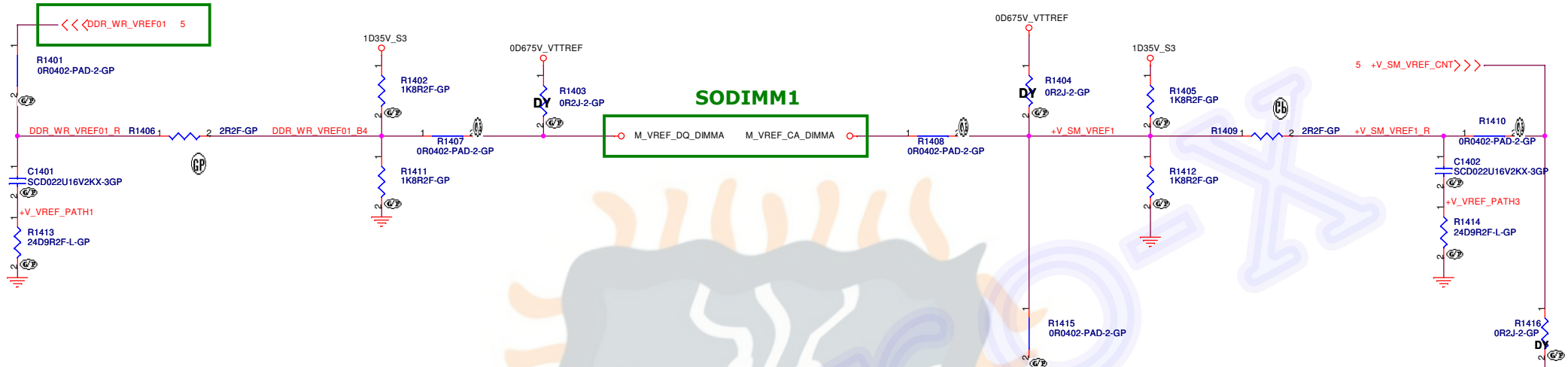
Title: DDR3L-SODIMM1
Size: A2 | Document Number: Round Rock MLK 13.3" | Rev: 0A
Date: Monday, August 17, 2015 | Sheet 13 of 40

SSID = MEMORY

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

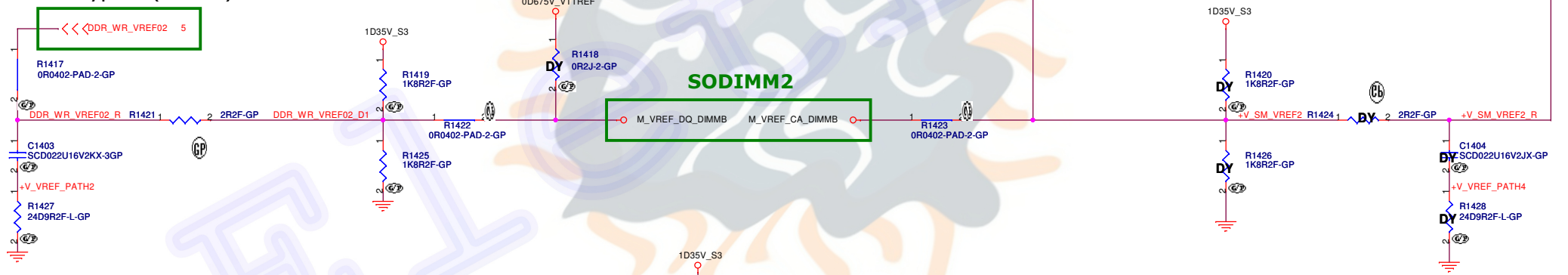
SA_DIMM_VREFDQ

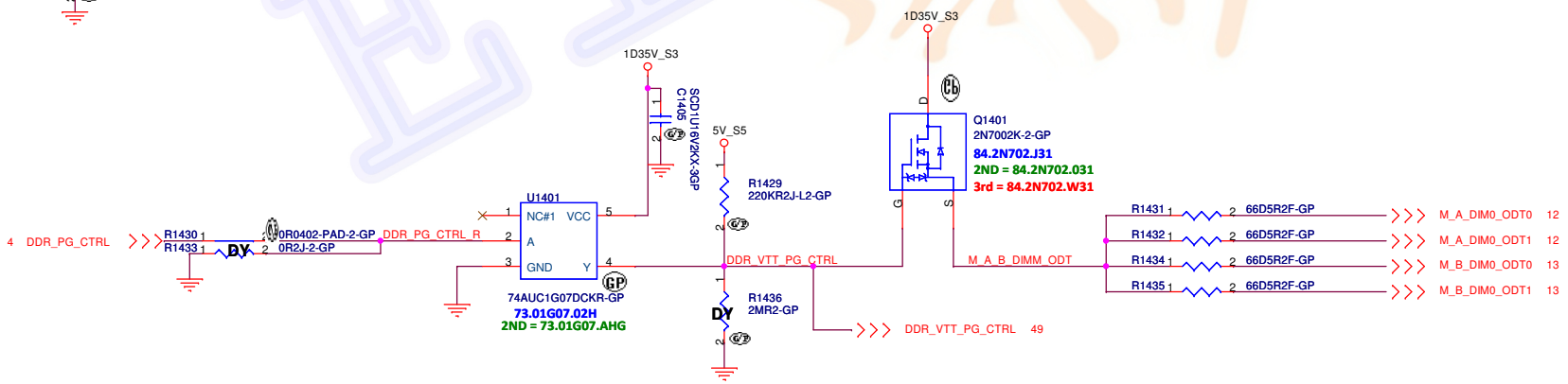
Driven by process (PIN#AR51)



SB_DIMM_VREFDQ

Driven by process (PIN#AP51)





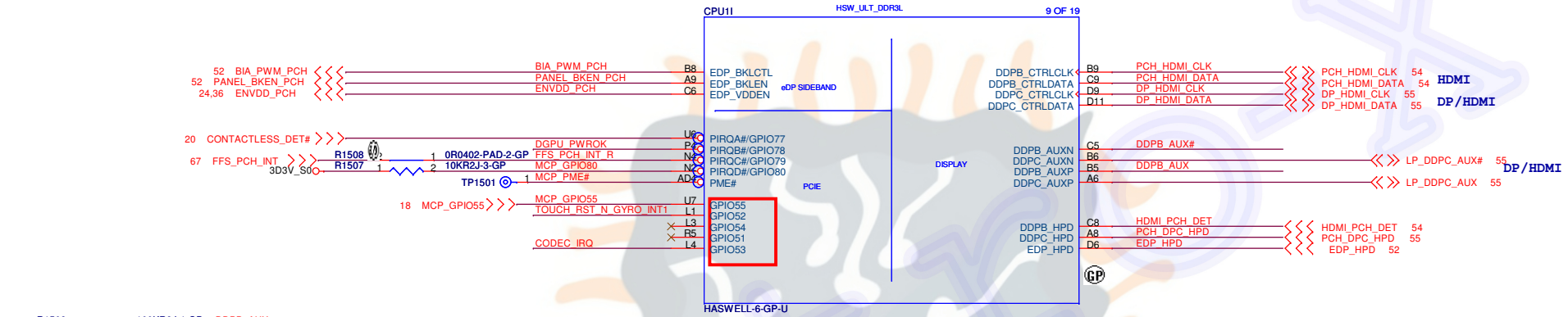
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M1 & M3 Implementation

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 14 of



R1502 100KR2J-1-GP DDPB_AUX
R1503 DY 1KR2F-5-GP CODEC_IRQ
R1504 DY 100KR2J-1-GP ENVDD_PCH
Schematic check list no need pull-low
R1505 100KR2J-1-GP PCH_DPC_HPD
R1506 DY 20KR2J-L2-GP HDMI_PCH_DET

3D3V_S0

RN1501
PCH_HDMI_DATA
PCH_HDMI_CLK
SRN2K2J-1-GP
RN1502
DP_HDMI_CLK
DP_HDMI_DATA
SRN2K2J-1-GP

3D3V_S0

RN1503
3.3V_TS_EN
3.3V_TP_EN
3.3V_TS_EN 20,98
3.3V_TP_EN 20,62
MCP_GPIO84 20
SRN10KJ-6-GP

RN1504
DGPU_PWROK
MINI2CLK_REQ#
MINI2CLK_REQ# 18,59
SRN10KJ-5-GP

R1513 10KR2J-3-GP TOUCH_RST_N_GYRO_INT1
R1514 100KR2J-1-GP DDPB_AUX#
R1515 DY 10KR2J-3-GP MCP_PME#
Schematic check list required pull-up 10k
R1517 10KR2J-3-GP FFS_PCH_INT_R

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (/DDI/PCI)
Size: A3
Document Number: Round Rock MLK 13.3" 400
Rev:
Date: Monday, August 17, 2015
Sheet 15 of

SSID = PCH

Broadwell ULT:
USB Ext. port 1
External debug port use on Broadwell ULT

USB2.0 Table

Pair	Device
0	USB port 1 (USB Charger)
1	USB port 2 (Win Debug)
2	WWAN
3	WLAN (BT)
4	N/A
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 Table

Pair	Device
1	USB port 1
2	USB port 2
3	WWAN
4	N/A

LAN

WLAN

EV follow ARD

WWAN

Card Reader

CPU1K HSW_ULT_DDR3L 11 OF 19

PCIE

USB

EV follow ARD

HASWELL-6-GP-U

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/USB)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 16 of 100

SSID = PCH

CPU1H
HSW_ULT_DDR3L
8 OF 19
SYSTEM POWER MANAGEMENT
HASWELL-6-GP-U

ME_SUS_PWR_ACK_R R1703 DY 0R2J-2-GP
R1704 0R0402-PAD-2-GP SUSACK# R
R1705 0R0402-PAD-2-GP SYS_PWROK_R
R1706 0R0402-PAD-2-GP PCH_PWROK
R1708 0R0402-PAD-2-GP APWROK_R
PCH_PLTRST#
24 SUSACK#
96 SYS_RESET#
24,96 SYS_PWROK
24,36 RESET_OUT#
36 APWROK
SUSACK# AK2
SYS_RESET# AC2
SYS_PWROK AG2
PCH_PWROK AY7
APWROK AB5
PLTRST# AG7

EV 18 PM_RSMRST#
PM_RSMRST#
R1710 0R0402-PAD-2-GP ME_SUS_PWR_ACK_R
R1711 0R0402-PAD-2-GP PM_PWRBTN# R
AC_PRESENT
PCH_BATLOW#
SIO_SLP_S0#
24 ME_SUS_PWR_ACK
96 PM_PWRBTN#_R
24 SIO_PWRBTN#
24 AC_PRESENT
88 SIO_SLP_S0#
99 SIO_SLP_WLAN#
RSMRST# AW6
SUSWARN#/SUSPWRDNACK#/GPIO30 AV4
PWRBTN# AL7
ACPRESENT/GPIO31 AJ8
BATLOW#/GPIO72 AN4
SLP_S0# AF2
SLP_WLAN#/GPIO29 AM2

NOTE:
PWRBTN# Integrated Pull-Up.

RTC_AUX_S5
R1707 DY 10KR2J-3-GP
PCH_DPWROK R1702 DY 0R2J-2-GP PM_RSMRST#
Reserve for NON DS3

DSWVRMEN AW7 DSWODVREN
DPWROK AV5 PCH_DPWROK
WAKE# AJ5
PCH_DPWROK 24
PCH_PCIE_WAKE# 24

CLKRUN#/GPIO32 V5 CLKRUN#
SUS_STAT#/GPIO61 AG4 SUS_STAT#/LPCPD# EV Remove LPC TPM
SUSCLK/GPIO62 AE6 SUSCLK R1709 DY 0R2J-2-GP
SLP_S5#/GPIO63 AP5 SIO_SLP_S5#
CLKRUN# 24
SUSCLK_NGFF 58,59
SIO_SLP_S5# 24

SLP_S4# AJ6
SLP_S3# AT4
SLP_A# AL5
SLP_SUS# AP4
SLP_LAN# AJ7
R1712 DY 0R2J-2-GP
SLP_A# R1713 DY 0R2J-2-GP
SIO_SLP_SUS# 0R0402-PAD-2-GP
SIO_SLP_LAN# TP1701
EV Remove Intel LAN
SIO_SLP_S4# 24,36,49
SIO_SLP_S3# 24,36,49
SIO_SLP_A# 24,36,48
SIO_SLP_SUS# 24

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
R1721 330KR2J-L1-GP
DSWODVREN R1723 DY 330KR2J-L1-GP

3D3V_S0
R1716 8K2R2J-3-GP CLKRUN#
R1719 DY 10KR2J-3-GP SYS_RESET#

3D3V_S5_PCH
EV follow Huston, pull high on XDP side
R1724 10KR2J-3-GP ME_SUS_PWR_ACK
R1726 10KR2J-3-GP SUSACK#
R1729 DY 10KR2J-3-GP SUS_STAT#/LPCPD#

+V3.3A_DSW_P
R1728 10KR2J-3-GP PCH_BATLOW#
RN1701 SRN10KJ-5-GP
PCH_PCIE_WAKE#
AC_PRESENT
R1722 DY 10KR2J-3-GP SIO_SLP_LAN#

R1733 DY 10KR2J-3-GP AC_PRESENT
R1734 DY 100KR2J-1-GP PCH_DPWROK
R1735 DY 10KR2J-3-GP SYS_PWROK
R1736 DY 10KR2J-3-GP PCH_PWROK
R1730 10KR2J-3-GP PM_RSMRST#
Schematic check list required pull-low 100k

3D3V_S0
C1701 SCD1U16V2KX-3GP
U1701
A VCC
B
GND Y
U74LVC1G08G-AL5-R-GP-U
73.01G08.EHG
2ND = 73.7SZ08.DAH
PCH_PLTRST#
PLTRST#
R1727 100KR2J-1-GP
R1725 0R0402-PAD-2-GP
R1717 0R0402-PAD-2-GP
R1718 0R0402-PAD-2-GP
R1720 0R0402-PAD-2-GP
PCH_PLTRST#_EC 24,65,88
PLTRST_MM# 32,58,59
PLTRST_XDP# 96
PLTRST_LAN# 30

APS1
3D3V_S5_PCH
+V3.3A_DSW_P
+V3.3A_DSW_P
19 RTC_RST#
24,61 MB_PWR_BTN#
SIO_SLP_S3#
SIO_SLP_S5#
SIO_SLP_S4#
SIO_SLP_A#
SYS_RESET#
SIO_SLP_S0#
APS
ETY-CON18-2-GP
20.K0493.018

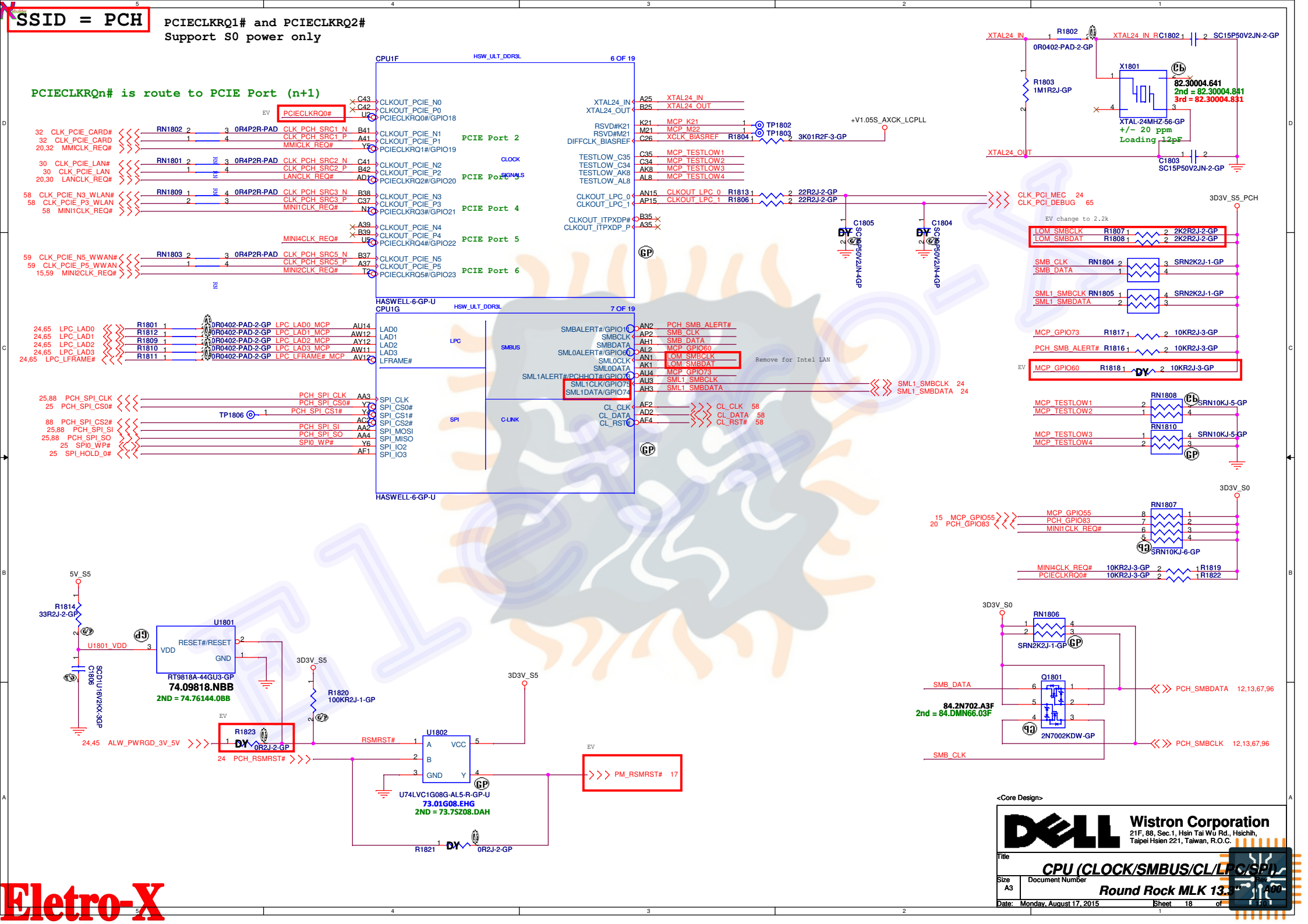
SYS_PWROK_R
PCH_PWROK
APWROK_R
PCH_DPWROK
SYS_RESET#
PCH_PLTRST#
PM_RSMRST#
EC1701 SC1KP50V2KX-1GP
EC1702 SC1KP50V2KX-1GP
EC1703 SC1KP50V2KX-1GP
EC1704 SC1KP50V2KX-1GP
EC1705 SC1KP50V2KX-1GP
EC1706 SC1KP50V2KX-1GP
EC1707 SC1KP50V2KX-1GP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CPU (PM)
Size: A3
Document Number: Round Rock MLK 13.3" 400
Rev:
Date: Monday, August 17, 2015
Sheet 17 of

SSID = PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLOCK/SMBUS/CL/LPC/SPI)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 18 of

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

CPU1E HSW_ULT_DDR3L 5 OF 19

HASWELL-6-GP-U

RTC_AUX_S5

RN1901 SRN20KJ-GP-U

G1902 GAP-OPEN

C1902 SC1U10V2KX-1GP

G1901 GAP-OPEN

C1903 SC1U10V2KX-1GP

EV_EMC

DY ED1901 AZ5725-01FDR7G-GP

R1901 1M1R2J-GP

R1903 330KR2F-L-GP

RTC_X1 AW5
RTC_X2 AY5
SM_INTRUDER# AU6
PCH_INTVRMEN AV7
SRTC_RST# AV6
RTC_RST# AU7

17 RTC_RST#

RTCX1
RTCX2
INTRUDER#
INTVRMEN
SRTCRST#
RTCRST#

RTC

HDA_BITCLK AW8
HDA_SYNC AV11
HDA_RST# AU8

27 HDA_SDIN0 AY10
98 ME_FWP AU12

R1904 1KR2J-1-GP

HDA_SDOUT AU11
AW10
AV10
AY8

HDA_BCLK/I2S0_SCLK
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S_MCLK#
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_SDO/I2S0_TXD
HDA_DOCK_EN#/I2S1_TXD#
HDA_DOCK_RST#/I2S1_SFRM#
I2S1_SCLK

AUDIO

RTC_X1
R1905 10MR2J-L-GP
RTC_X2
R1906 0R0402-PAD-2-GP
X1901
X1_R
C1901 SC2P50V2CN-GP
C1904 SC2P50V2CN-GP
XTAL-32.768KHZ-6-GP
+/- 20 ppm
CL=7 pF

82.30001.B21
2nd = 82.30001.661
3rd = 82.30001.B41
X02

4,96 XDP_TRST#
96 PCH_JTAG_TCK

R1907 0R2J-2-GP
R1908 0R2J-2-GP

XDP_TRST#_R AU62
PCH_JTAG_TCK_BUF AE62
PCH_JTAG_TDI AD61
PCH_JTAG_TDO AE61
PCH_JTAG_TMS AD62
AL11
AC4
AE63
AV2

PCH_TRST#
PCH_TCK
PCH_TDI
PCH_TDO
PCH_TMS
RSVD#AL11
RSVD#AC4
JTAGX
RSVD#AV2

JTAG

96 PCH_JTAGX

PCH_JTAGX

27 HDA_CODEC_SYNC
27 HDA_CODEC_SDOUT
27 HDA_CODEC_RST#
27 HDA_CODEC_BITCLK

R1911 33R2J-2-GP HDA_SYNC
R1912 33R2J-2-GP HDA_SDOUT
R1913 33R2J-2-GP HDA_RST#
R1914 33R2J-2-GP HDA_BITCLK

DY C1905 SC27P50V2JN-2-GP

SATA_RN0/PERN6_L3 J5
SATA_RP0/PERP6_L3 H5
SATA_TN0/PETN6_L3 B15
SATA_TP0/PETP6_L3 A15

SATA_RXN0 56
SATA_RXP0 56
SATA_TXN0 56
SATA_TXP0 56

HDD

SATA_RN1/PERN6_L2 J8
SATA_RP1/PERP6_L2 H8
SATA_TN1/PETN6_L2 A17
SATA_TP1/PETP6_L2 B17

SATA_RN2/PERN6_L1 J6
SATA_RP2/PERP6_L1 H6
SATA_TN2/PETN6_L1 B14
SATA_TP2/PETP6_L1 C15

SATA_RN3/PERN6_L0 F5
SATA_RP3/PERP6_L0 E5
SATA_TN3/PETN6_L0 C17
SATA_TP3/PETP6_L0 D17

SATA_RN3/PERN6_L0 59
SATA_RP3/PERP6_L0 59
SATA_TN3/PETN6_L0 59
SATA_TP3/PETP6_L0 59

WWAN

SATA

SATA0GP/GPIO34 V1
SATA1GP/GPIO35 U1
SATA2GP/GPIO36 V6
SATA3GP/GPIO37 AC1

MPCIE_RST#
HDD_DET#
MCP_GPIO36

HDD_DET# 56
NGFF_PCIE#_SATA 24

SATA_IREF A12
RSVD#L11 L11
RSVD#K10 K10
SATA_RCOMP C12
SATALED# U3

R1909 0R0402-PAD-2-GP
TP1901
TP1902
R1910 3K01R2F-3-GP
SATA_LED# 61

+V1.05S_ASATA3PLL

3D3V_S0

HDD_DET# R1931 10KR2J-3-GP
MPCIE_RST# R1925 10KR2J-3-GP
MCP_GPIO36 R1920 10KR2J-3-GP

1D05V_M

PCH_JTAGX R1919 PCH XDP 51R2J-2-GP
PCH_JTAG_TMS R1921 PCH XDP 51R2J-2-GP
PCH_JTAG_TDI R1922 PCH XDP 51R2J-2-GP
PCH_JTAG_TDO R1923 PCH XDP 51R2J-2-GP
PCH_JTAG_TCK_BUF R1924 PCH XDP 51R2J-2-GP

PCH_JTAG_TDO R1928 PCH XDP 0R2J-2-GP CPU_XDP_TDO_PCH 96
PCH_JTAG_TDI R1929 PCH XDP 0R2J-2-GP CPU_XDP_TDI_PCH 96
PCH_JTAG_TMS R1930 PCH XDP 0R2J-2-GP CPU_XDP_TMS_PCH 96

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

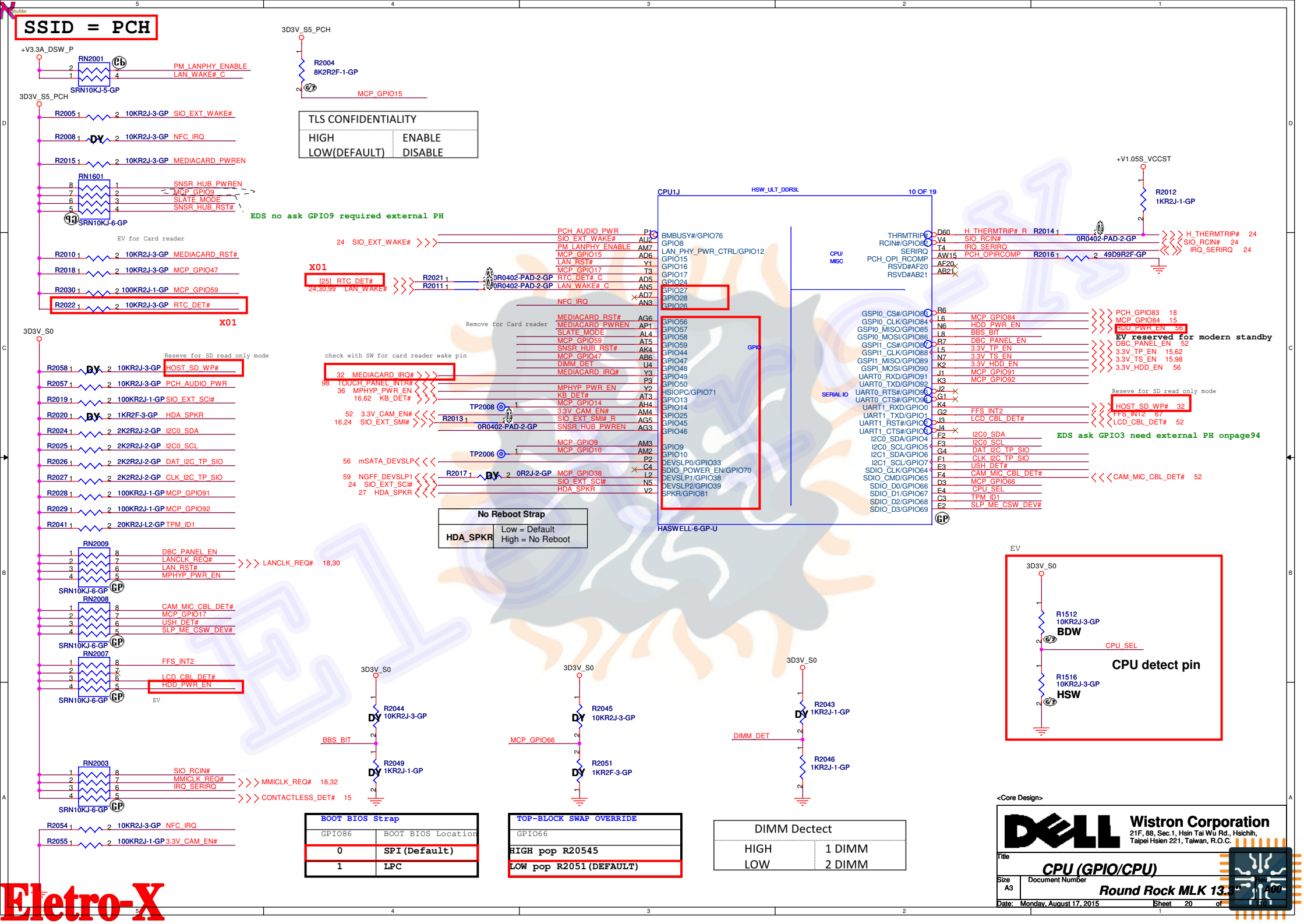
Title: CPU (RTC/SATA/HDA/JTAG)

Size: A3 Document Number: Round Rock MLK 13.3" Rev: A00

Date: Monday, August 17, 2015 Sheet 19 of

Eletro-X

SSID = PCH



<Core Design>

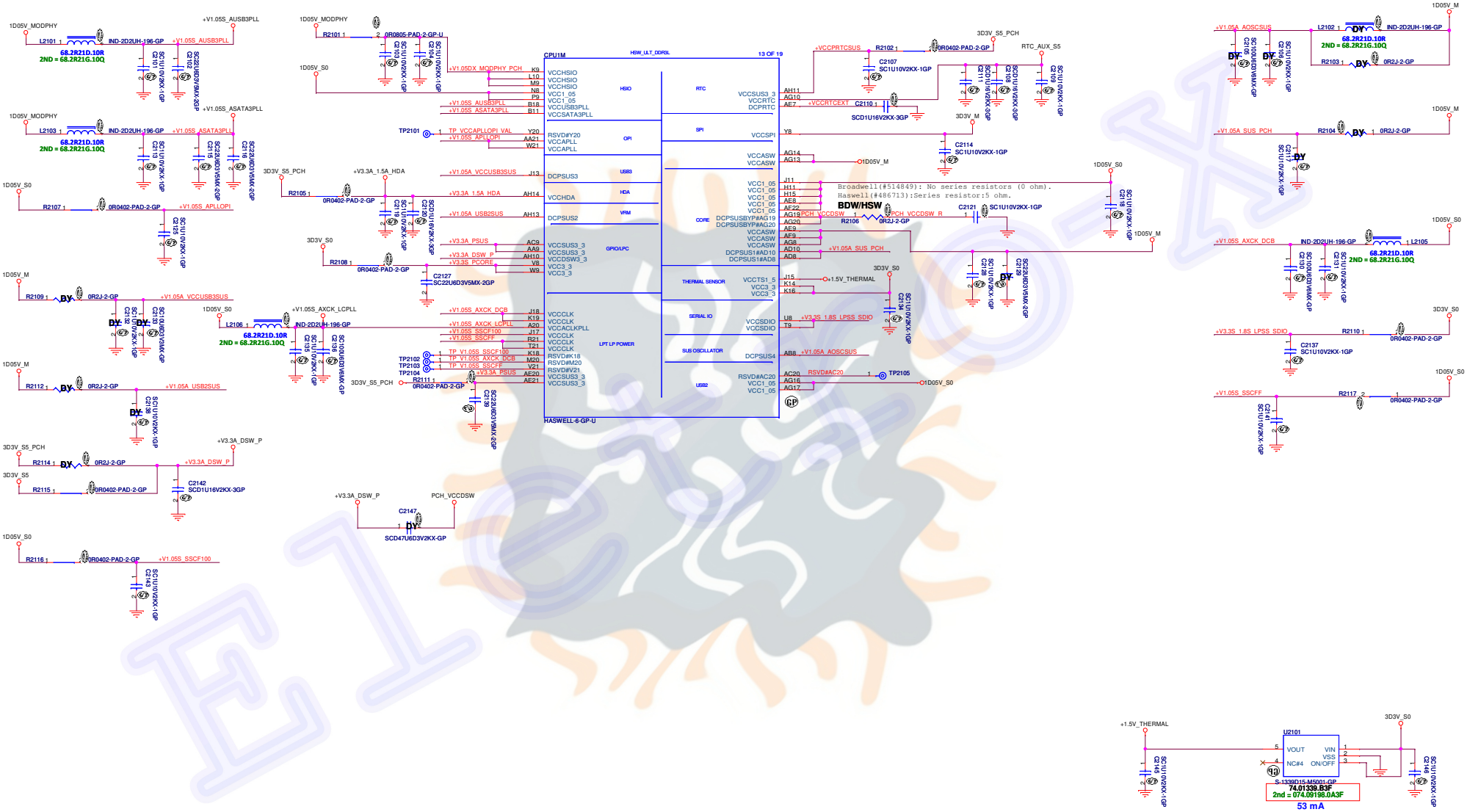
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

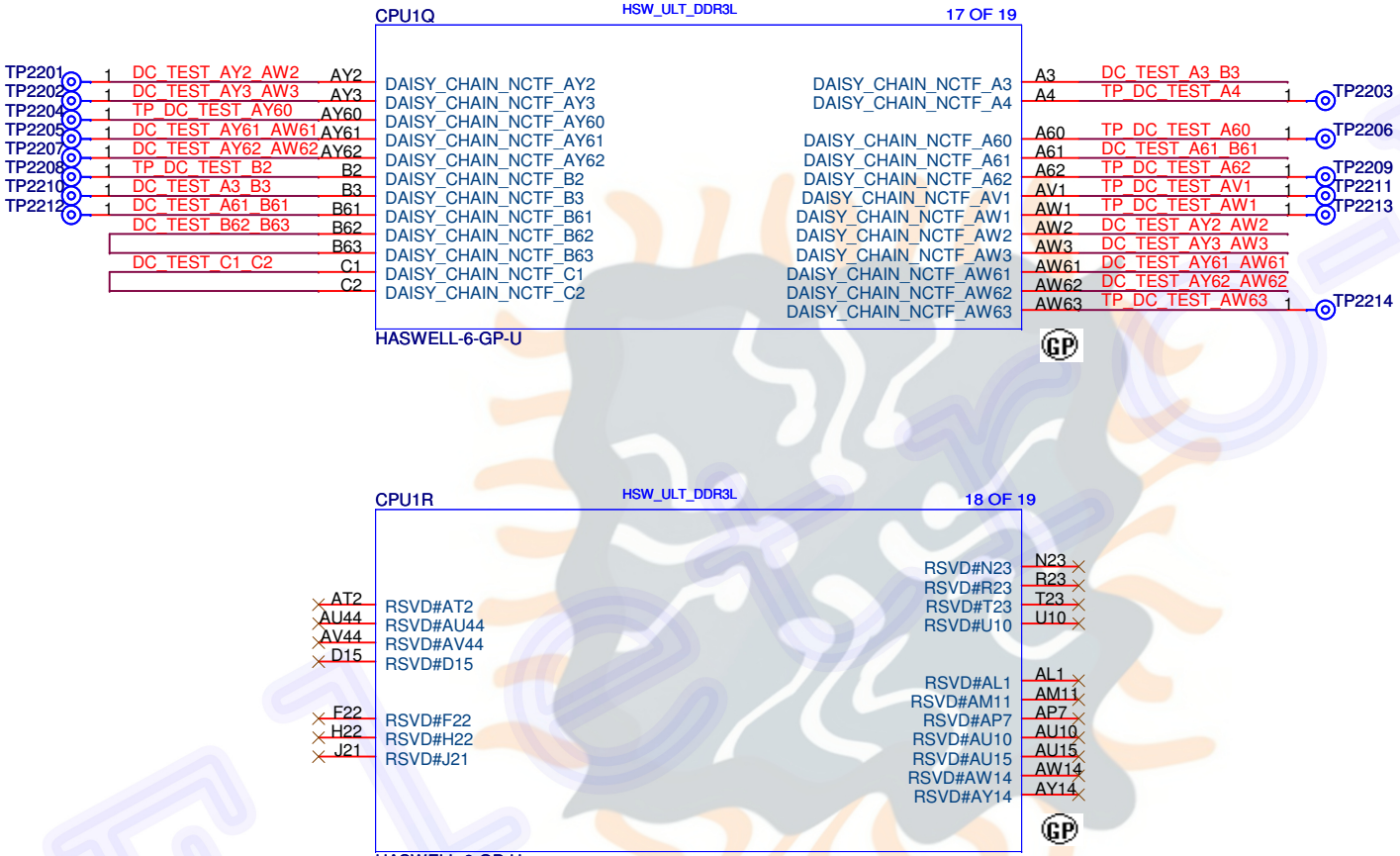
Title: CPU (GPIO/CPU)

Size: A3 | Document Number: Round Rock MLK 13.3" UMA 400 | Rev:

Date: Monday, August 17, 2015 | Sheet 20 of

SSID = PCH





<Core Design>

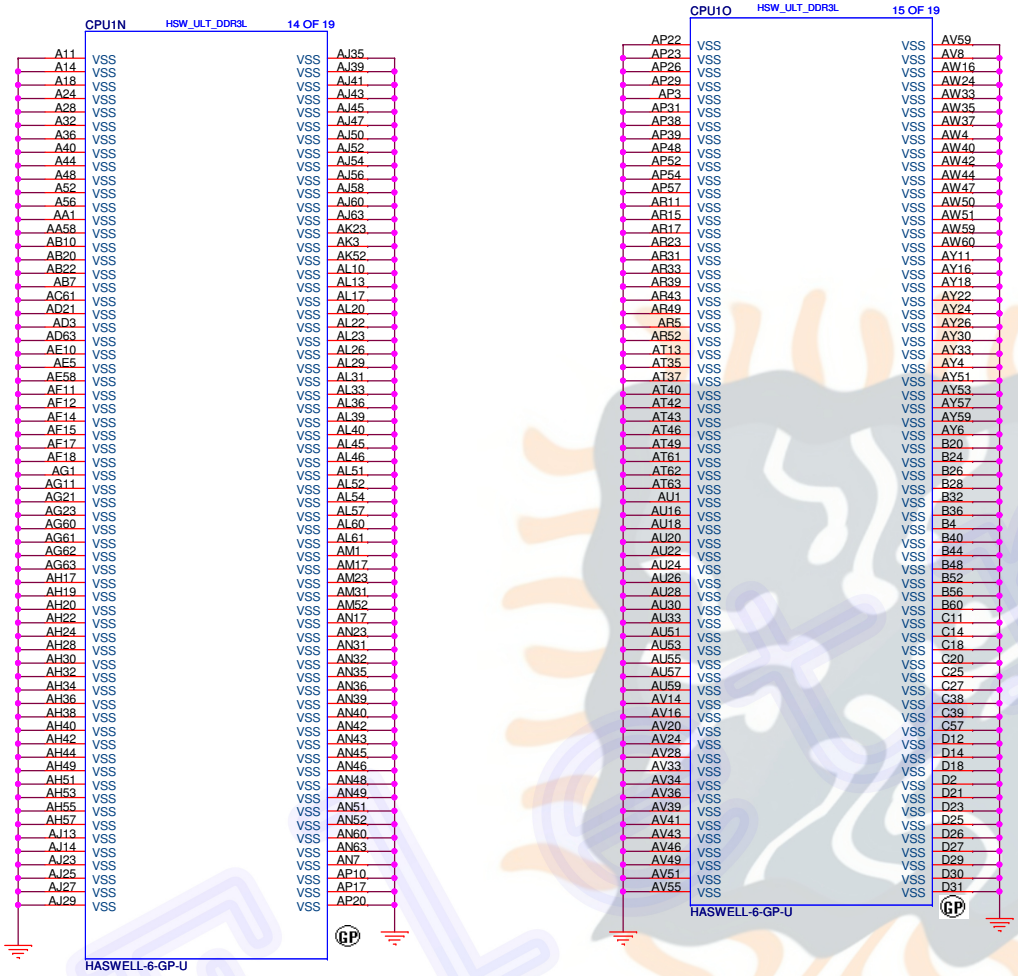
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (RSVD)**

Size	Document Number	Rev
A4	Round Rock MLK 13.3"	A00

Date: Monday, August 17, 2015 Sheet 22 of 110

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 23 of

SSID = KBC

EV reverve for factory test

0 = Reset JTAG I/F
1 = Disable

Place close to Pin58

Round Rock MLK 13.3" BOARD_ID		
Cap. Value	Res. Value	REV
4700pF	240k ohm	EV
	130k ohm	X01
	33k ohm	X02
	1k ohm	A00

EV follow Houston

R2463 pull DN, Enable JTAG debug mode

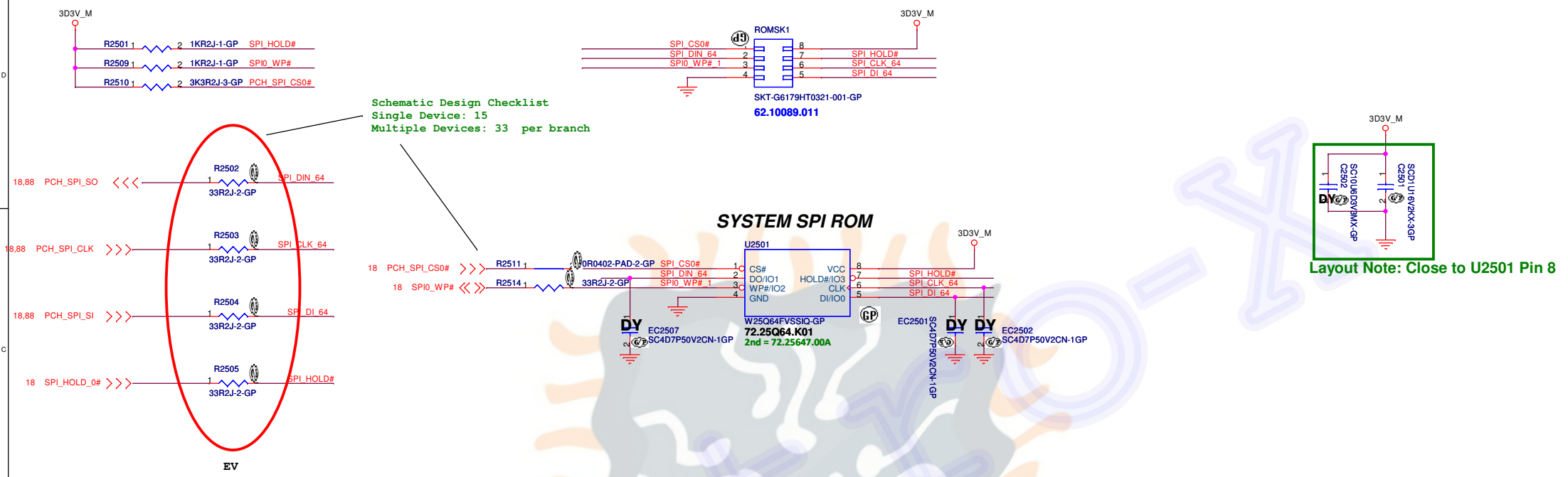
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

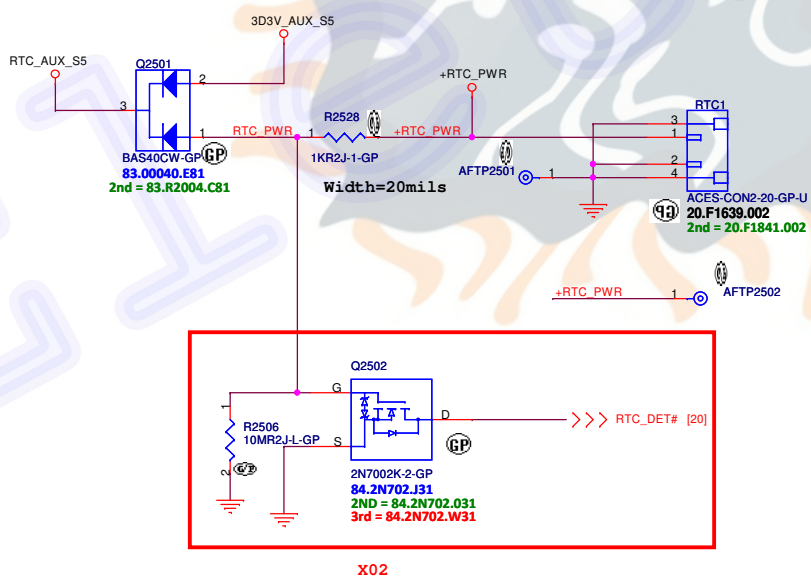
Title: EC - MEC5085
Size: A2 | Document Number: Round Rock MLK 13.3" | Rev: A00
Date: Tuesday, August 18, 2015 | Sheet 24

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil



SSID = RTC



<Variant Name>

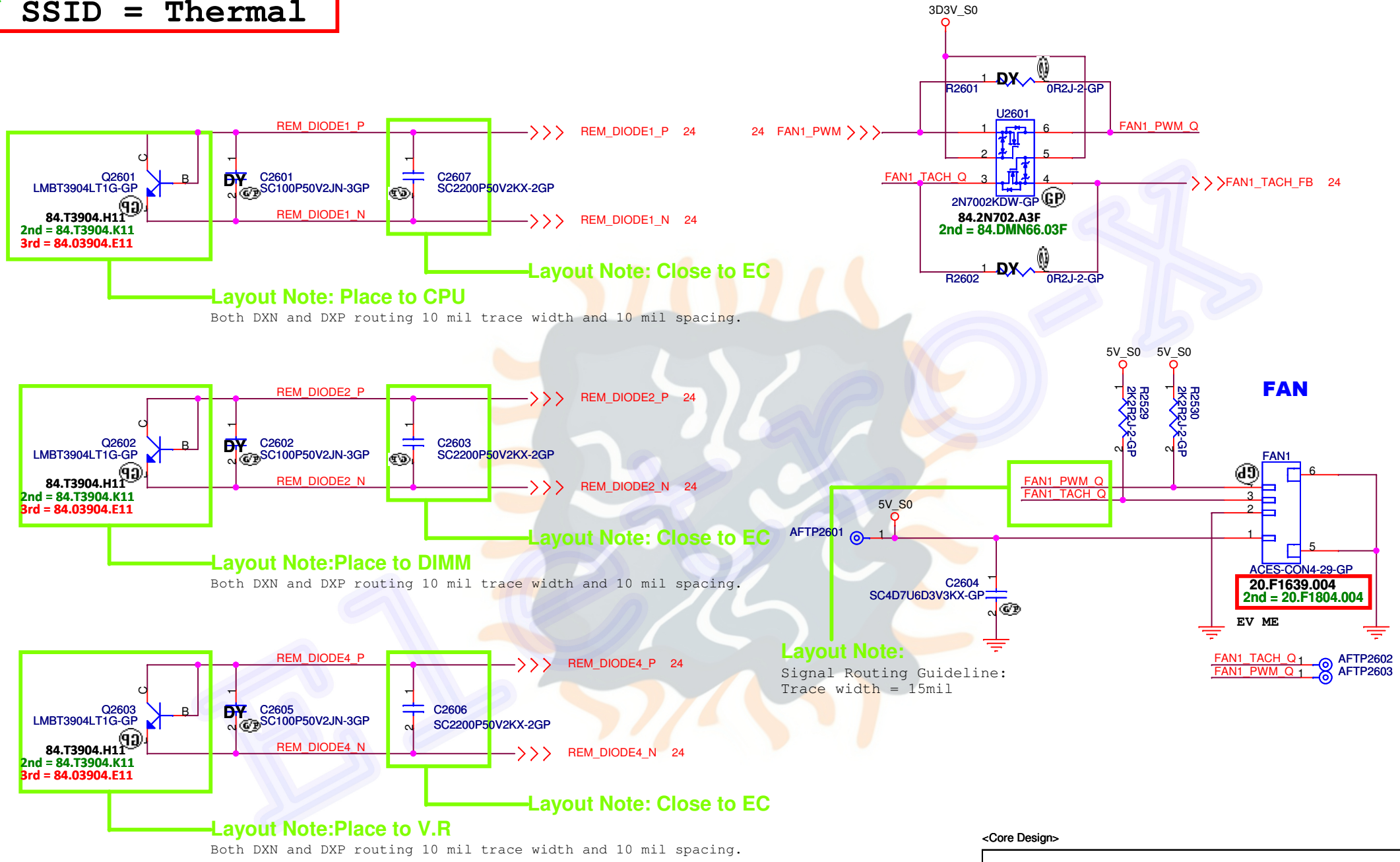
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size: A3 | Document Number: Round Rock MLK 13.3" A00 | Rev: X02

Date: Monday, August 17, 2015 | Sheet 25 of

SSID = Thermal

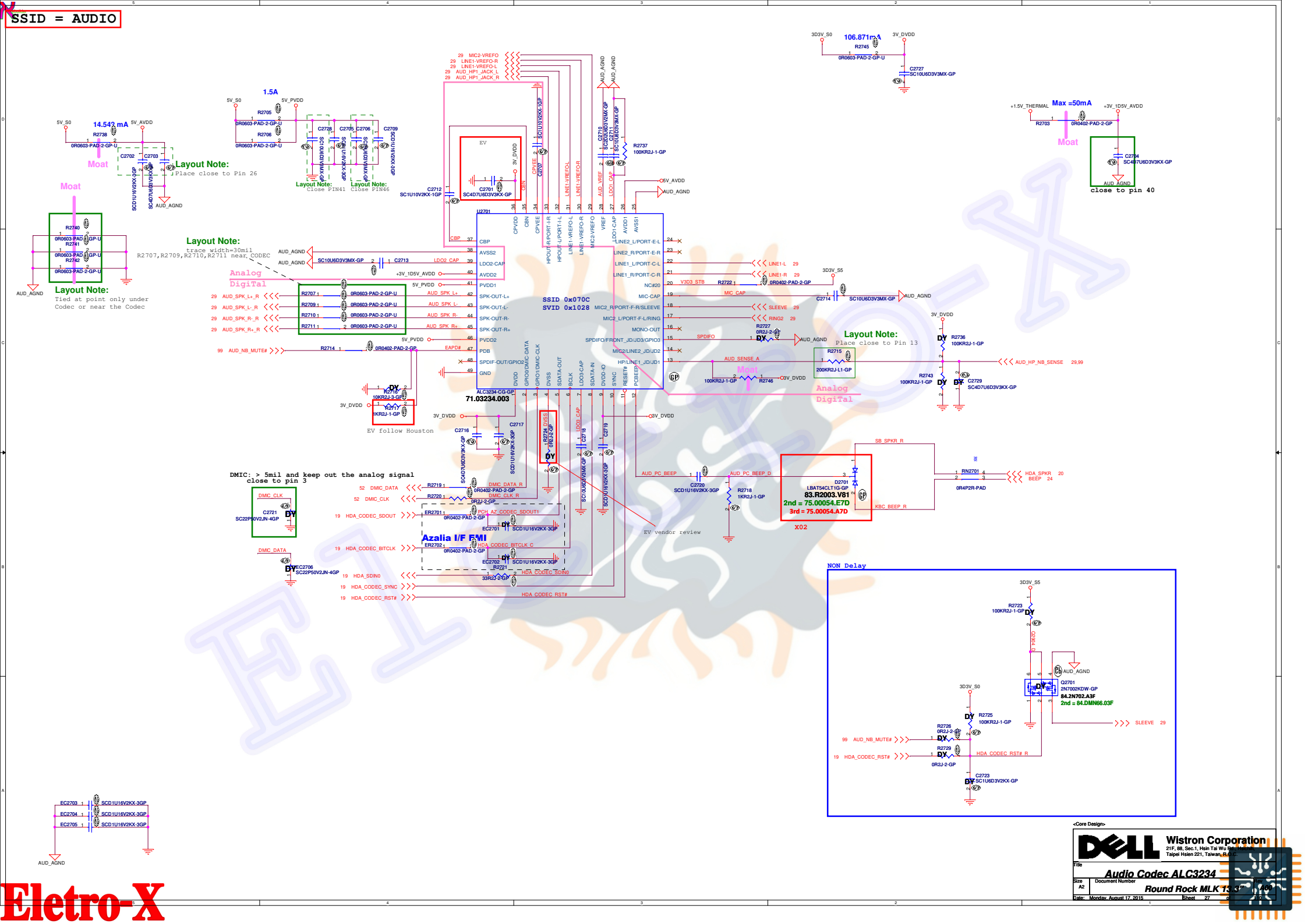


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal/Fan	
Size A4	Document Number: Round Rock MLK 13.3"	Rev: A00
Date: Monday, August 17, 2015	Sheet 26 of 110	

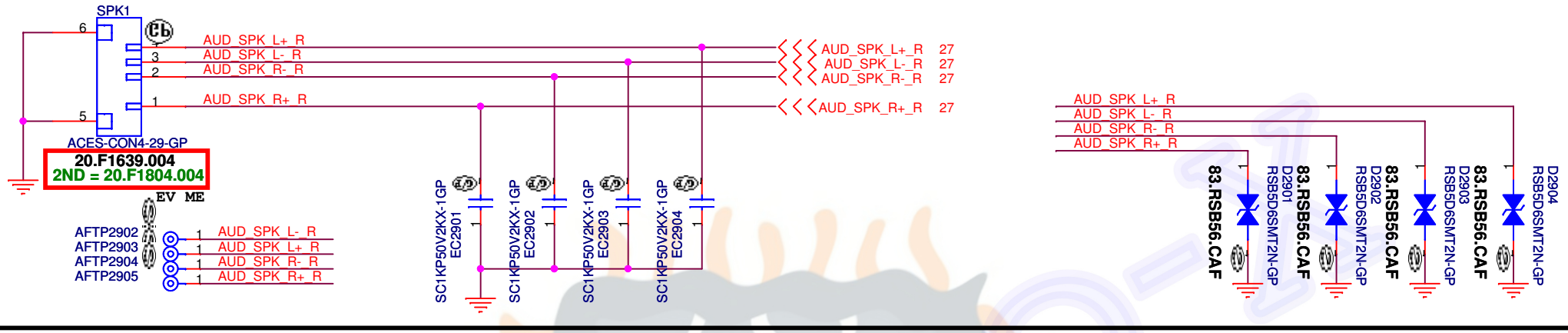
SSID = AUDIO



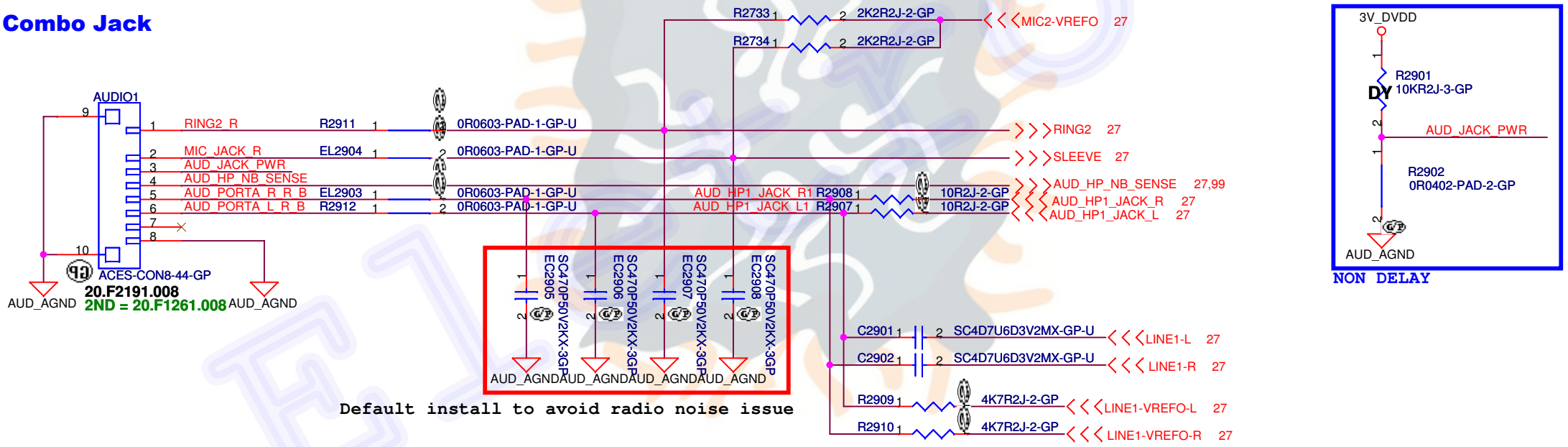
SSID = AUDIO

Speaker

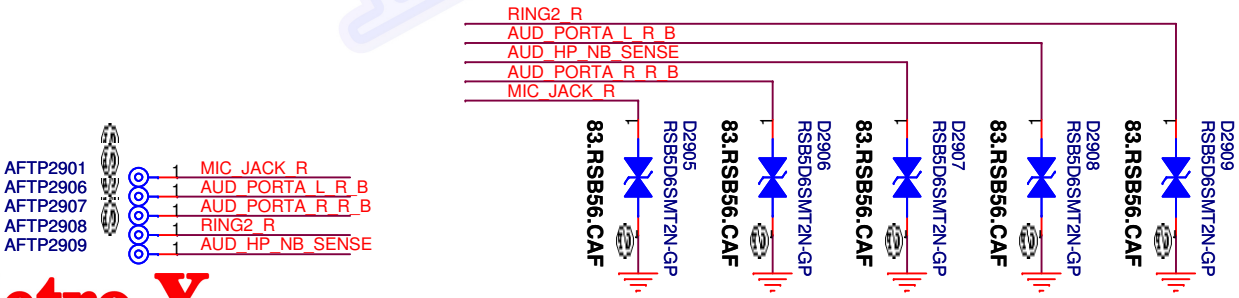
2W/ch



Combo Jack



Default install to avoid radio noise issue



<core_design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

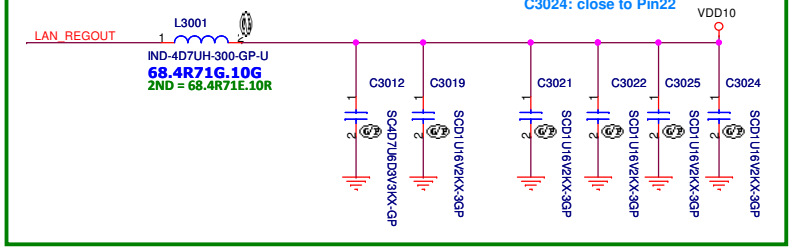
Size: A4 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 29 of 46

SSID = LAN

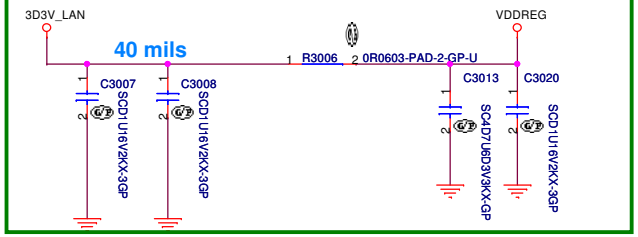
Layout:
* Place C3021 to C3024 close to each VDD10 pin--3, 8, 22, 30

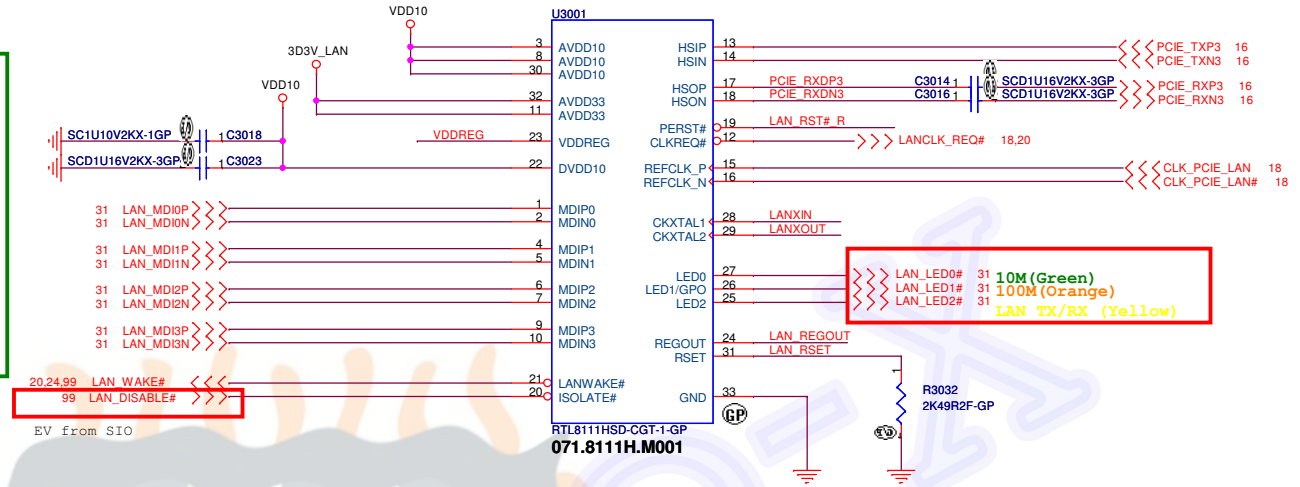
C3021: colse to Pin8
C3022 close to Pin3
C3025: close to Pin30
C3024: close to Pin22

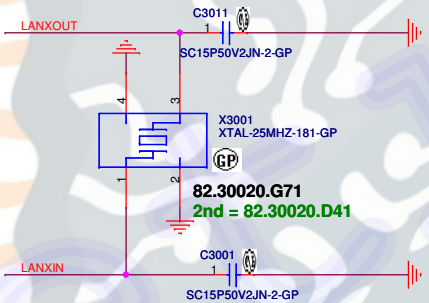


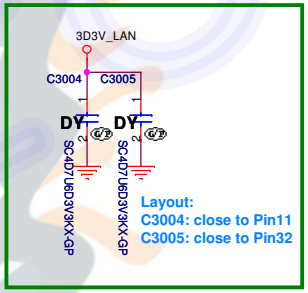
Layout:
* Place C3007 and C3008 close to each VDD33 pin-- 11, 32

C3008: close to Pin32
C3007: close to Pin11

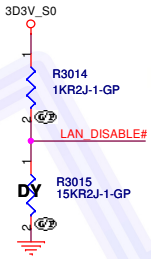


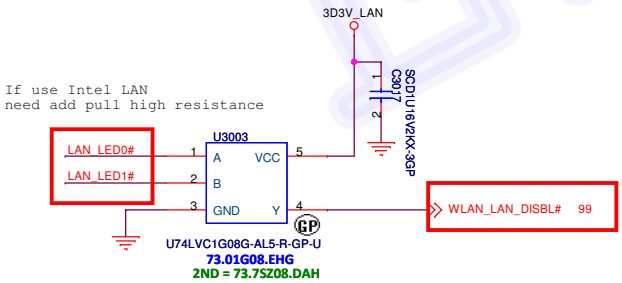


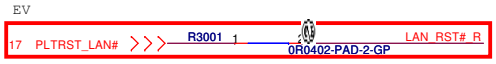




RTL8111HSD-CGT
071.8111H.M001
SWR mode
10/100/1000M







<Core Design>

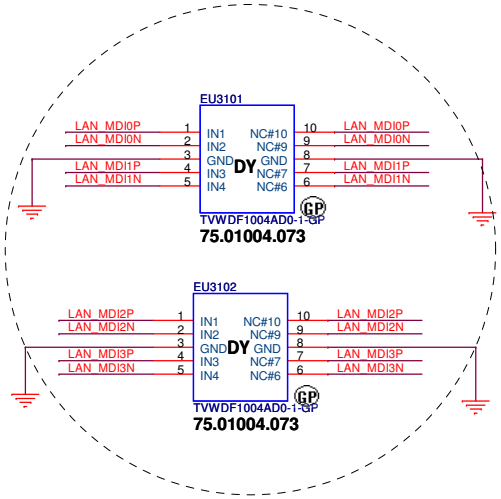
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

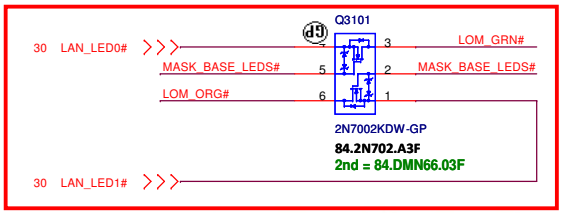
Date: Monday, August 17, 2015 | Sheet 30 of

SSID = LOM

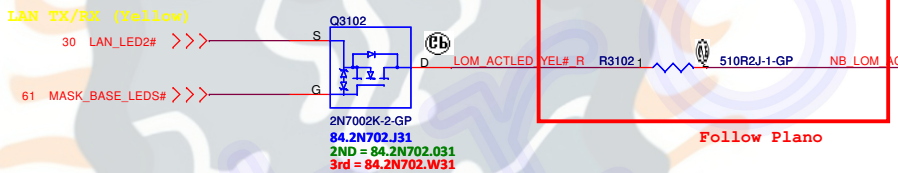


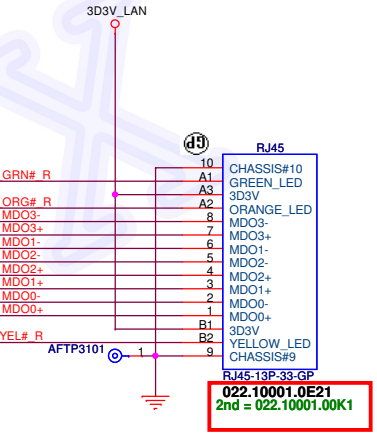
EV EMC

EV

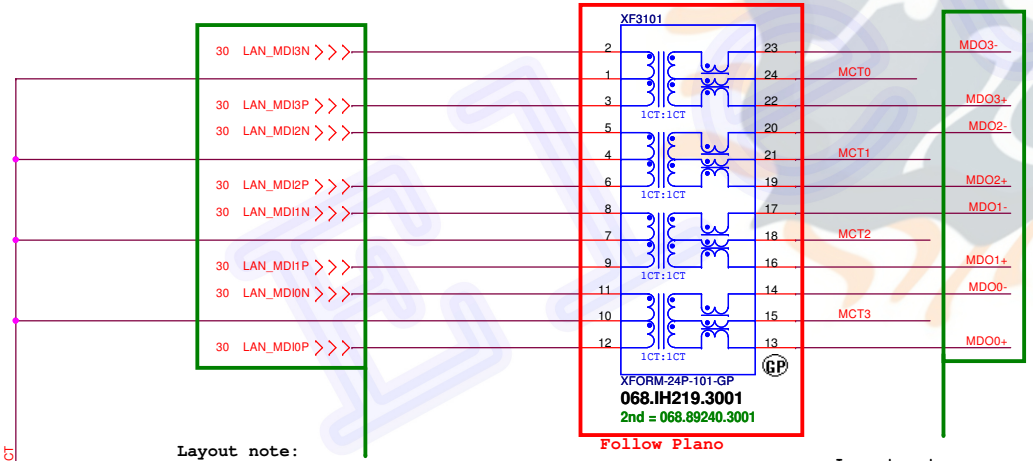


10M(Green)
100M(Orange)
1000M(Green+Orange)

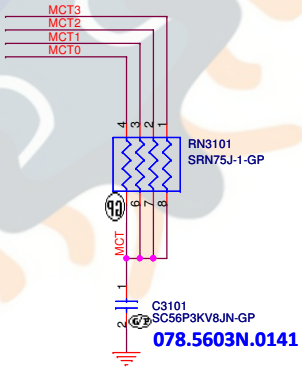


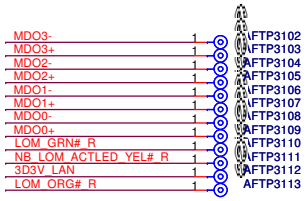


EV ME

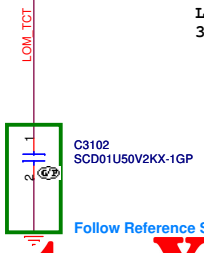


Layout note:
30 mil spacing between MDI differential pairs.





Layout note:
30 mil spacing between MDI differential pairs.



Follow Reference Schematic 0.01uF~0.4uF

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45/Transformer

Size: A3 | Document Number: Round Rock MLK 13.3 AMD | Rev: A00

Date: Monday, August 17, 2015 | Sheet 31 of

SSID =Card Reader

EV for card reader

17,58,59 PLTRST_MM# → R3201 1 2 0R0402-PAD-2-GP → PCIE_CARD_PLT_RST#

3D3V_S0_CARD

3D3V_S0 → R3206 1200 mA → 3D3V_S0_CARD

R3206 0R0805-PAD-2-GP-U

R3217 0R0805-PAD-2-GP-U

3D3V_S0_CARD → R3202 0R0603-PAD-2-GP-U → 3D3V_AUX_CARD

3D3V_S0_CARD: C3203 SC10U6D3V2MX-GP, C3205 SCD1U16V2KX-3GP

3D3V_AUX_CARD: C3204 SC10U6D3V2MX-GP, C3236 SCD1U16V2KX-3GP

Close to pin11 Close to pin27

SD_CLK → EC3201 SC6D8P50V2CN-GP DY

1D2V_LDO: C3227 SC4D7U6D3V2MX-GP-U, C3226 SCD1U16V2KX-3GP, C3231 SCD1U16V2KX-3GP

Layout Note:

Close to pin14 Close to pin10

SD_VDD2 SD_VDD1

U3201

1D2V_LDO, 3D3V_S0_CARD → AV12, 3V3_IN

CARD_3V3, SD_VDD2, DV12S, DV33_18, 3V3AUX

1D2V_LDO, DV33_18, 3D3V_AUX_CARD

SC1U10V2KX-1GP C3202

SP1 SD_D1_RCLK_M_R R3204 0R0402-PAD-2-GP → SD_D1_RCLK_M 33

SP2 SD_D0_RCLK_P_R R3207 0R0402-PAD-2-GP → SD_D0_RCLK_P 33

SP3 SD_CLK_R R3209 0R0402-PAD-2-GP → SD_CLK 33

SP4 SD_CMD_R R3210 0R0402-PAD-2-GP → SD_CMD 33

SP5 SD_D3_R R3211 0R0402-PAD-2-GP → SD_D3 33

SP6 SD_D2_R R3213 0R0402-PAD-2-GP → SD_D2 33

SP7 SD_WPI

SD_CD# MS_INS# → SD_CD# 33

PERST# → PCIE_CARD_PLT_RST#

CLK_REQ# → MMICLK_REQ# 18,20

WAKE# DEV_WAKE# → R3212 0R0402-PAD-2-GP → MEDIACARD_IRQ# 20

3D3V_AUX_CARD → R3205 10KR2J-3-GP → MEDIACARD_IRQ#

16 PCIE_TXP2, 16 PCIE_TXN2 → HSIP, HSIN

SCD1U16V2KX-3GP: C3230 PCIE_RXP2_C, C3229 PCIE_RXN2_C

16 PCIE_RXP2, 16 PCIE_RXN2 → HSOP, HSON

SCD1U16V2KX-3GP

18 CLK_PCIE_CARD, 18 CLK_PCIE_CARD# → REFCLKP, REFCLKN

RREF → CARD_RREF

SDREG2 → CARD_SDREG2

GPIO → CARD_GPIO → R3203 10KR2J-3-GP → 3D3V_AUX_CARD

C3205 SC1U10V2KX-1GP, R3208 6K2R2F-GP

For UHS-II

33 SD_D0P, 33 SD_D0N, 33 SD_D1P, 33 SD_D1N → SD_LN0_P, SD_LN0_M, SD_LN1_P, SD_LN1_M

GND

RTS5242-GR-GP-U

071.05242.0003

HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

R3214 DY 0R2J-2-GP

Q3201 2N7002K-2-GP

SD_WPI → D

S → SD_WPI_Q 33

G → HOST_SD_WP# 20

84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31

EV reseve for SD read only mode

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: 4.00

Date: Monday, August 17, 2015 | Sheet 32 of

SSID =Card Reader

SD_VDD1

SCD1U16V2KX-3GP C3302

SC4D7U6D3V3KX-GP C3304

Layout Note:Close to Card Reader CONN

SD_VDD2

SCD1U16V2KX-3GP C3306

SC4D7U6D3V9KX-GP C3307

SD 4.0 Card Connector

SD_VDD2 SD_VDD1

CARD1

SKT-SDCARD-44-GP-U

62.10051.I01

2nd = 062.10002.0051

EV ME

32 SD_CLK — R3301 0R0402-PAD-2-GP — SD_CLK_C

32 SD_CMD

EC3314 SC6D8P50V2CN-GP DY

VDD/VDD1 VDD2 CLK CMD FG1 FG2 FG3 FG4 FG5 FG6 FG7 NP1 NP2

D0+ D0- D1+ D1- DAT0/RCLK+ DAT1/RCLK- DAT2 CD/DAT3 CARD_DETECT WRITE_PROTECT CD WP

VSS1 VSS2 VSS3 VSS4 VSS5

SD_D0P 32 SD_D0N 32 SD_D1P 32 SD_D1N 32 SD_D0_RCLK_P 32 SD_D1_RCLK_M 32 SD_D2 32 SD_D3 32 SD_CD# 32 SD_WPI_Q 32

EV

SD_CD# SD_D3 SD_CLK_C SD_CMD SD_D0_RCLK_P SD_D1_RCLK_M SD_D2 SD_WPI_Q SD_VDD1 SD_D0P SD_D0N SD_D1P SD_D1N

AFTP3301 AFTP3302 AFTP3303 AFTP3304 AFTP3305 AFTP3306 AFTP3307 AFTP3308 AFTP3309 AFTP3311 AFTP3312 AFTP3313 AFTP3310

SD_D3 SD_CMD SD_D2 SD_D1_RCLK_M SD_D0_RCLK_P SD_D1N SD_D1P SD_D0N SD_D0P

EC3304 EC3305 EC3306 EC3309 EC3310 EC3311 EC3303 EC3307 EC3308 SC6D8P50V2CN-GP DY

<Core Design>

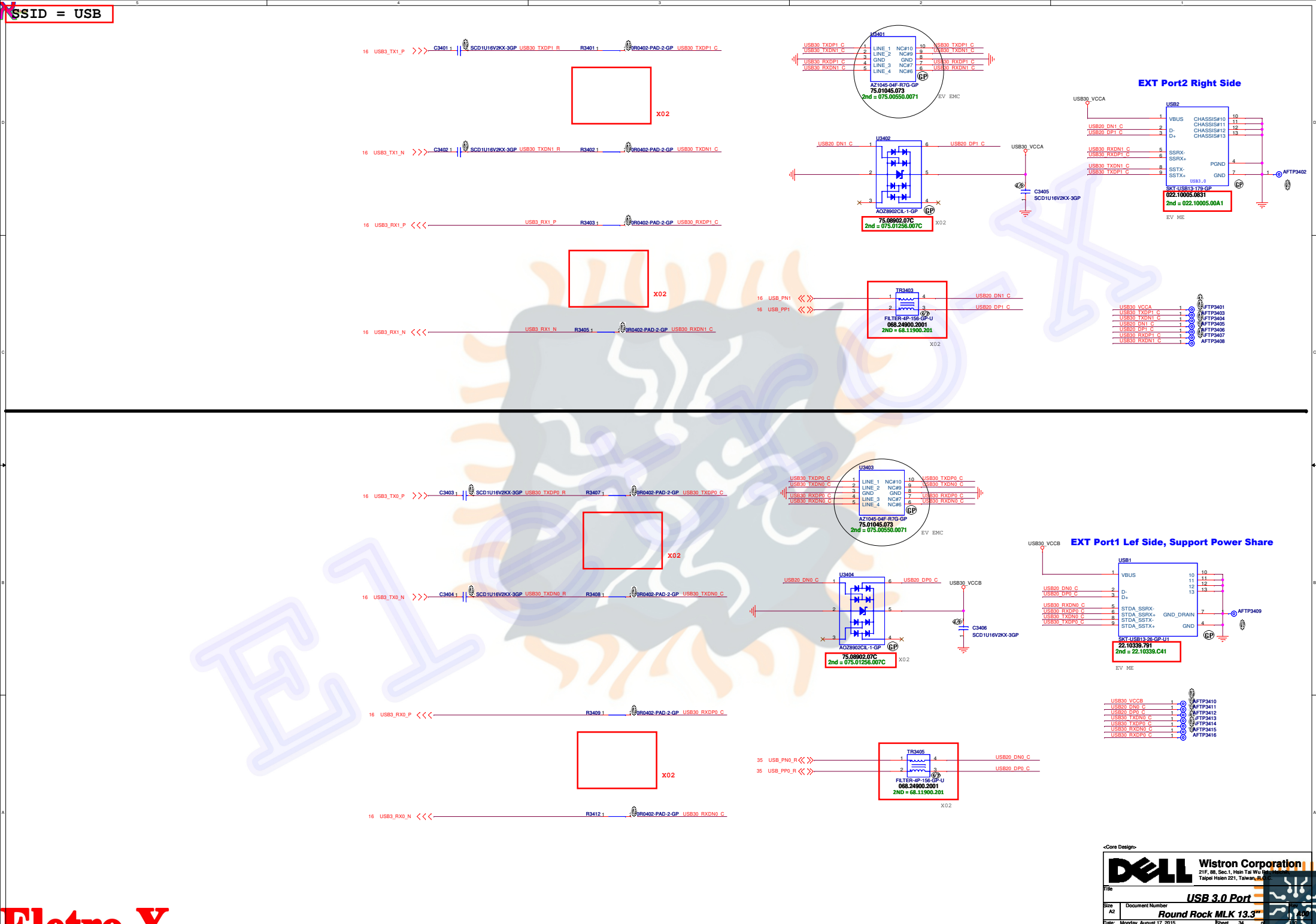
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader CONN

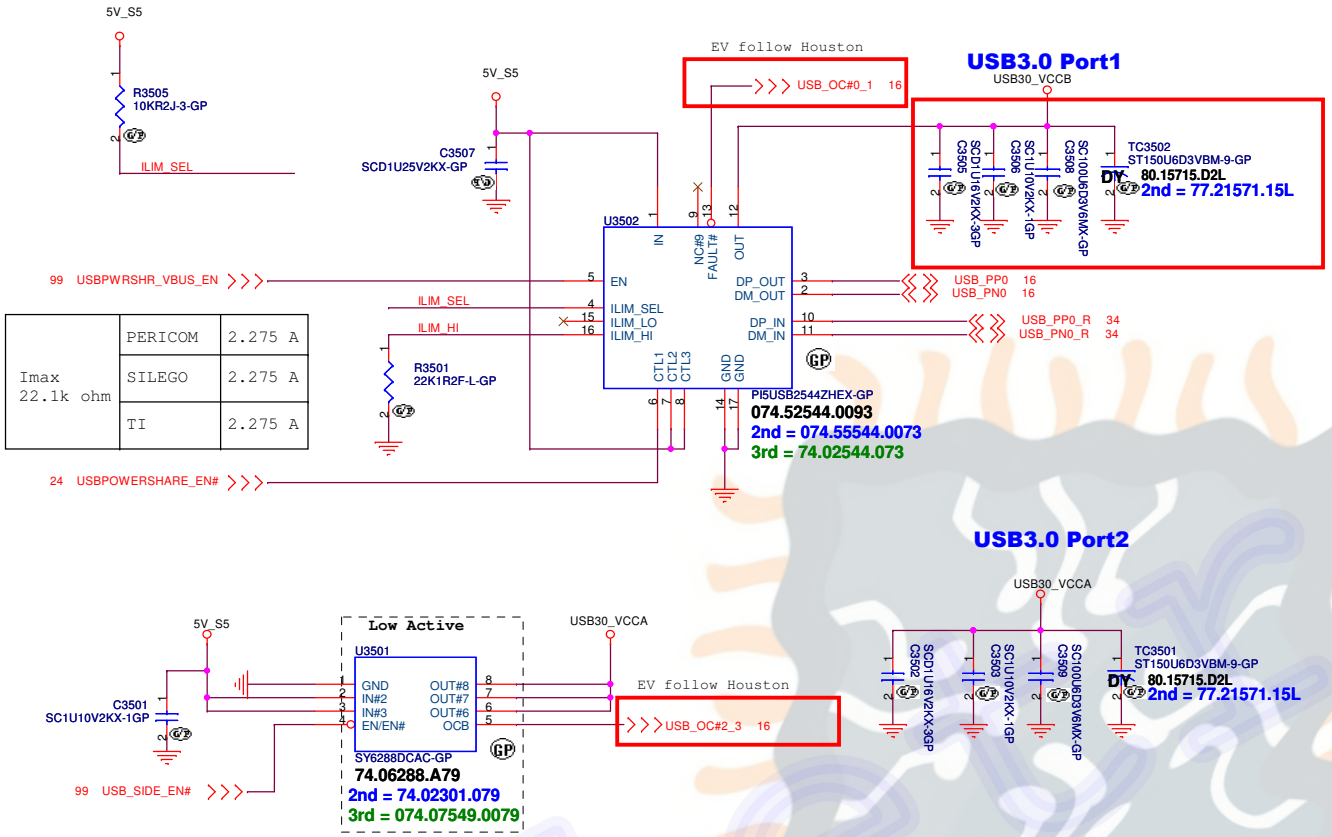
Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Tuesday, August 18, 2015 | Sheet 33 of 100

SSID = USB


EXT Port2 Right Side
EXT Port1 Lef Side, Support Power Share
USB 3.0 Port
Round Rock MLK 13.3**
Wistron Corporation
Eletro-X

SSID = USB



Imax 22.1k ohm		
	PERICOM	2.275 A
	SILEGO	2.275 A
	TI	2.275 A

PI5USB2544 Device Control Pins Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	x	1	x	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	0	0	SDP1	ILIM_LO	Data lines connected
0	1	0	1	SDP1	ILIM_HI	
0	1	1	0	DCP_Auto	ILIM_HI	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	Data lines disconnected
1	0	0	0	DCP_Shorted	ILIM_LO	Device forced to stay in DCP BC1.2 charging mode
1	0	0	1	DCP_Shorted	ILIM_HI	
1	0	1	0	Divider-1A	ILIM_LO	Device forced to stay in Divider-1A charging mode
1	0	1	1	Divider-1A	ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data lines connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2(1)	ILIM_LO	
1	1	1	1	CDP(1)	ILIM_HI	Data lines connected

Note:
(1) No OUT discharge when changing between 1111 and 1110.

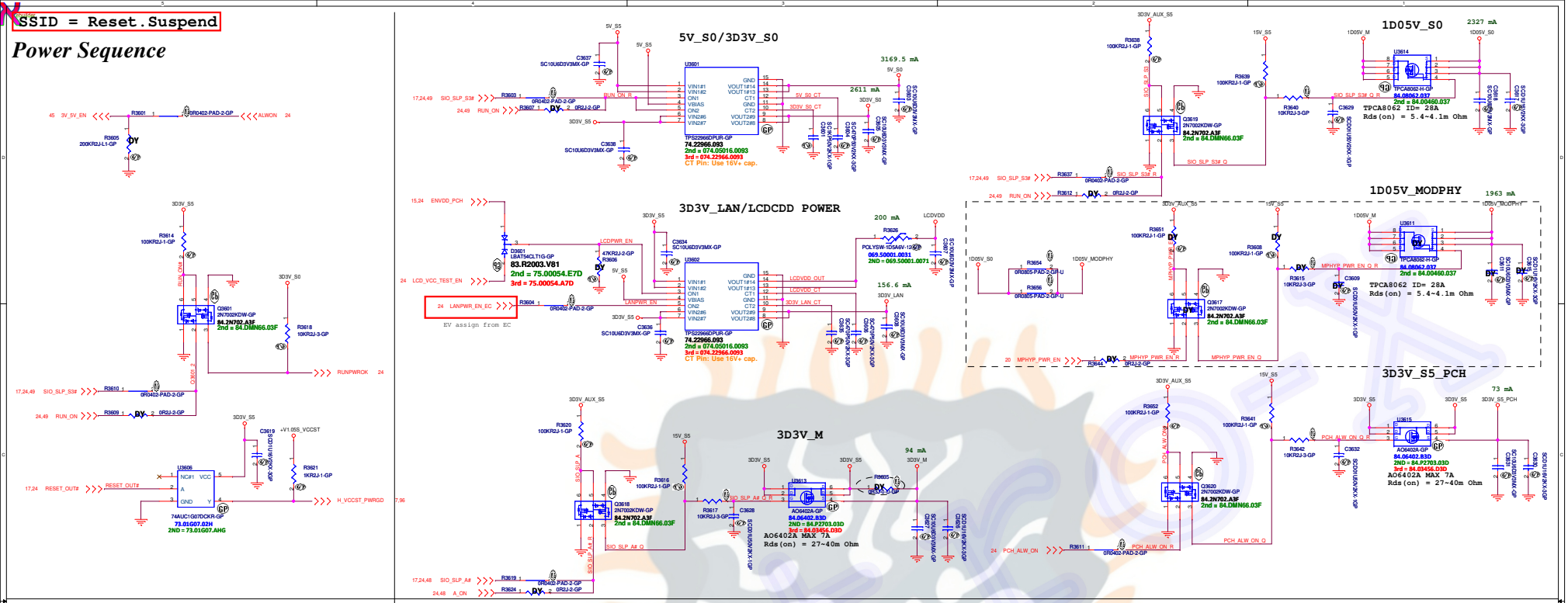
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 Power SW
Size: Document Number: Round Rock MLK 13.3" Rev: A00
Date: Monday, August 17, 2015 Sheet 35 of

SSID = Reset.Suspend

Power Sequence



Intel Power Sequence

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size: Custom | Document Number: Round Rock MLK 13.3" | Rev: A00

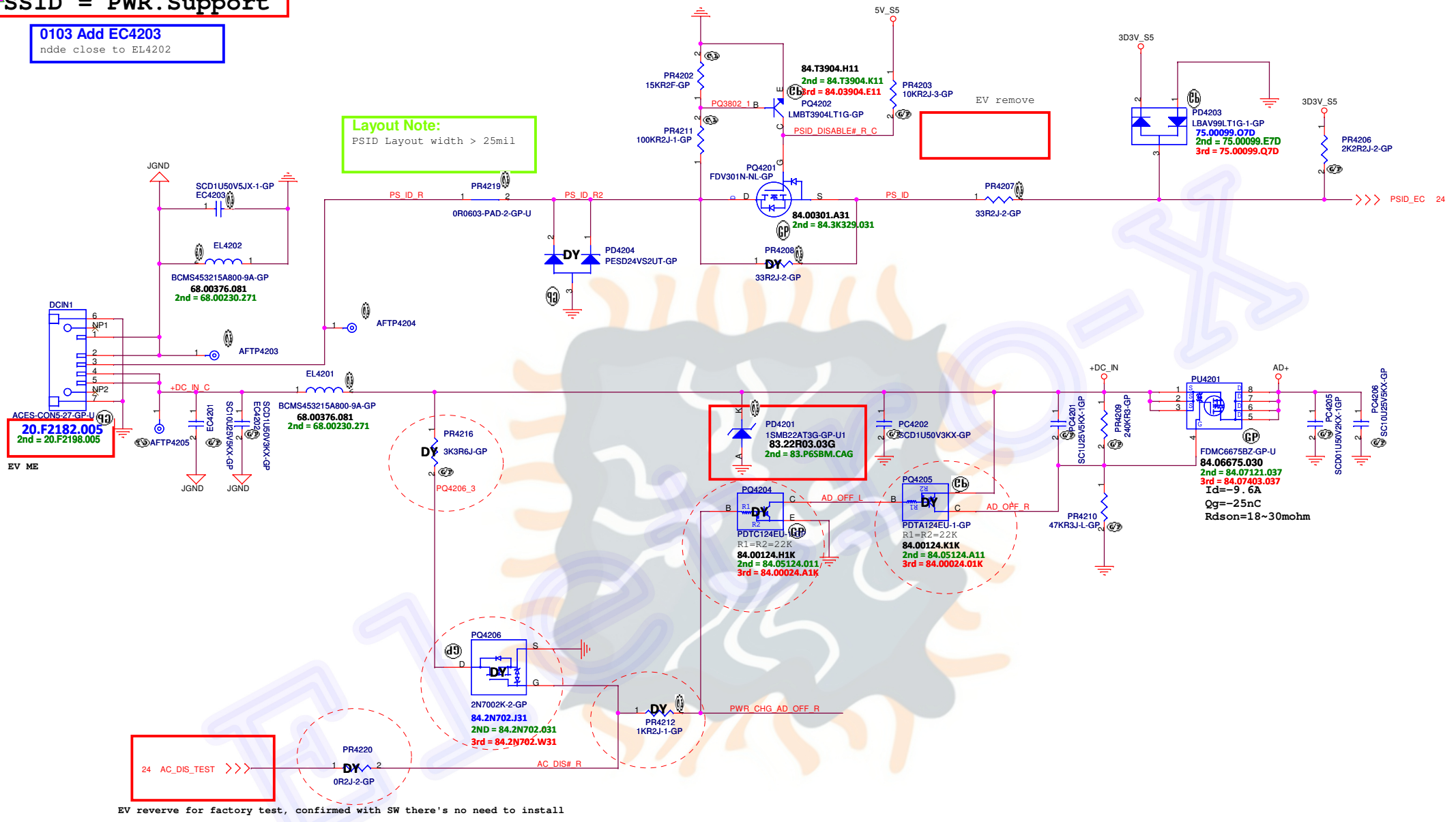
Date: Monday, August 17, 2015 | Sheet 36 of 110

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil

EV remove



EV reverve for factory test, confirmed with SW there's no need to install

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

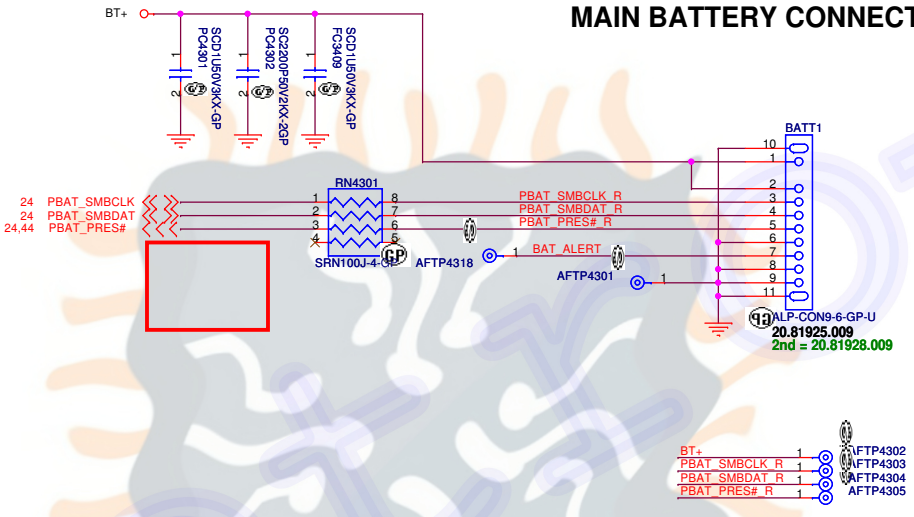
Title: DCIN JACK

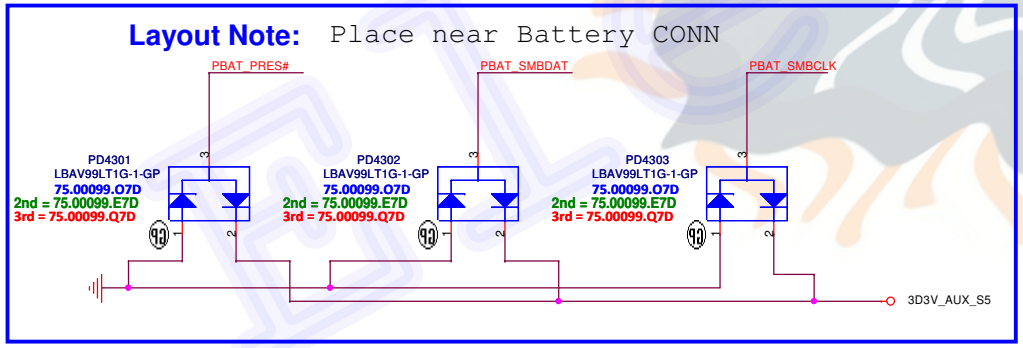
Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 42 of

SSID = PWR.Support

MAIN BATTERY CONNECTOR





<Variant Name>

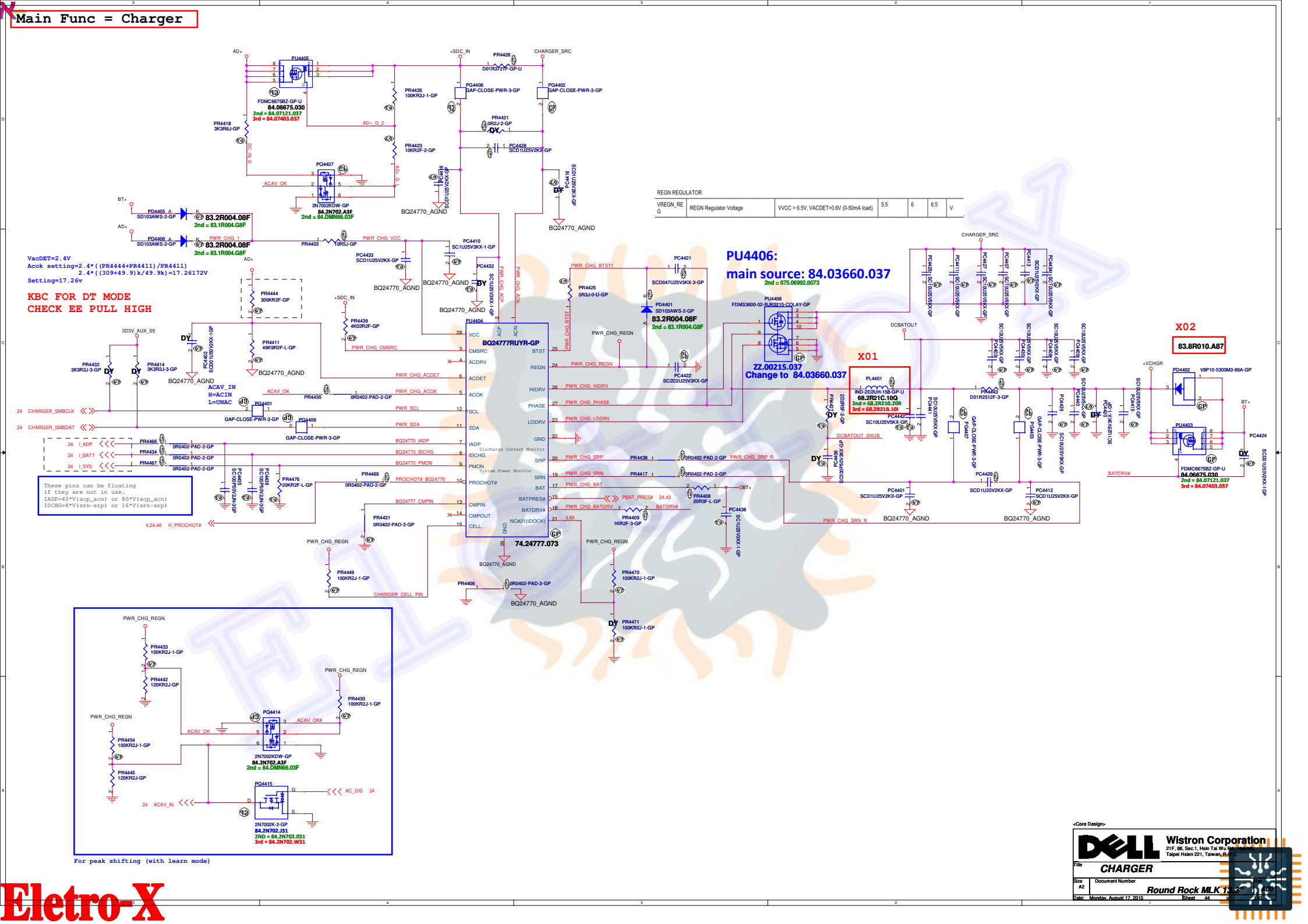
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY CONN

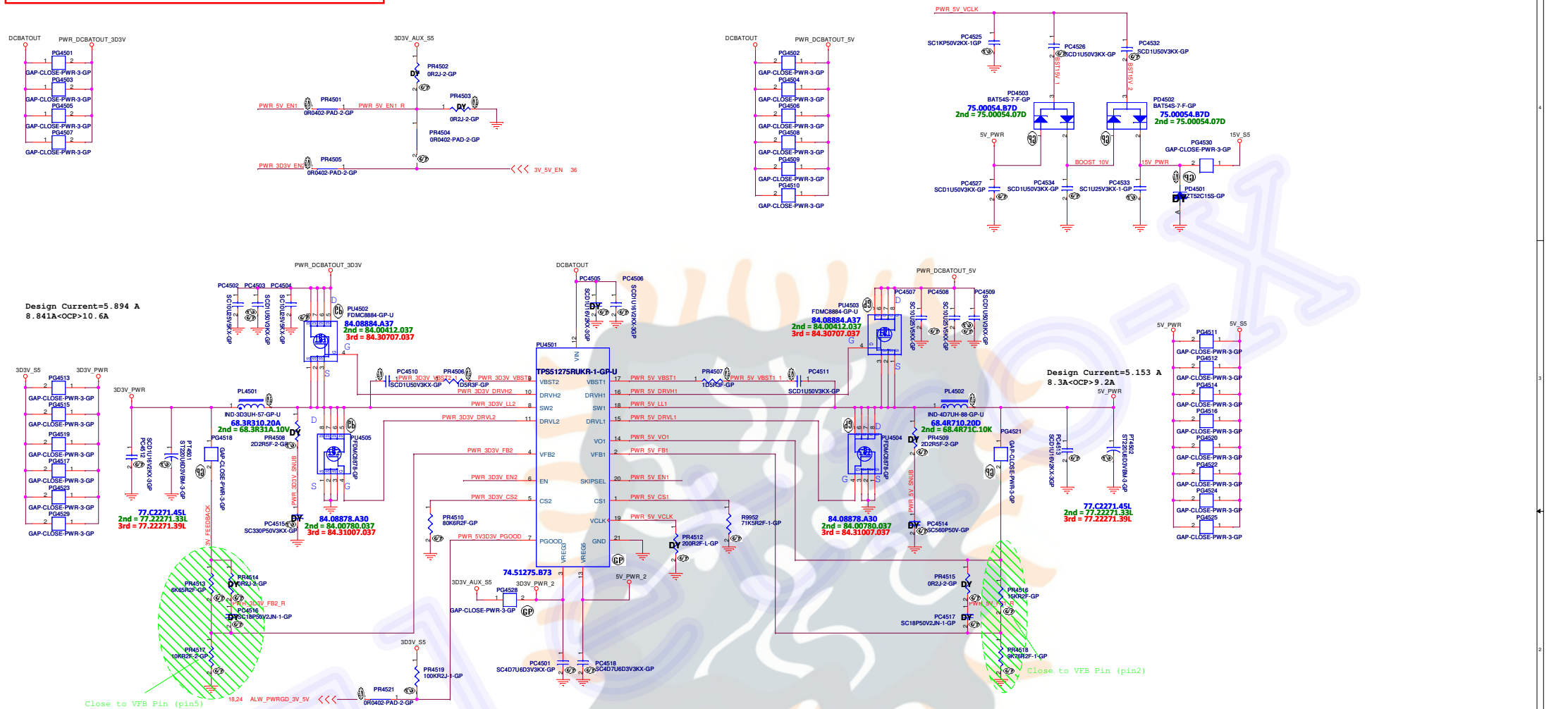
Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 43 of 70

Main Func = Charger



SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

<Core Design>

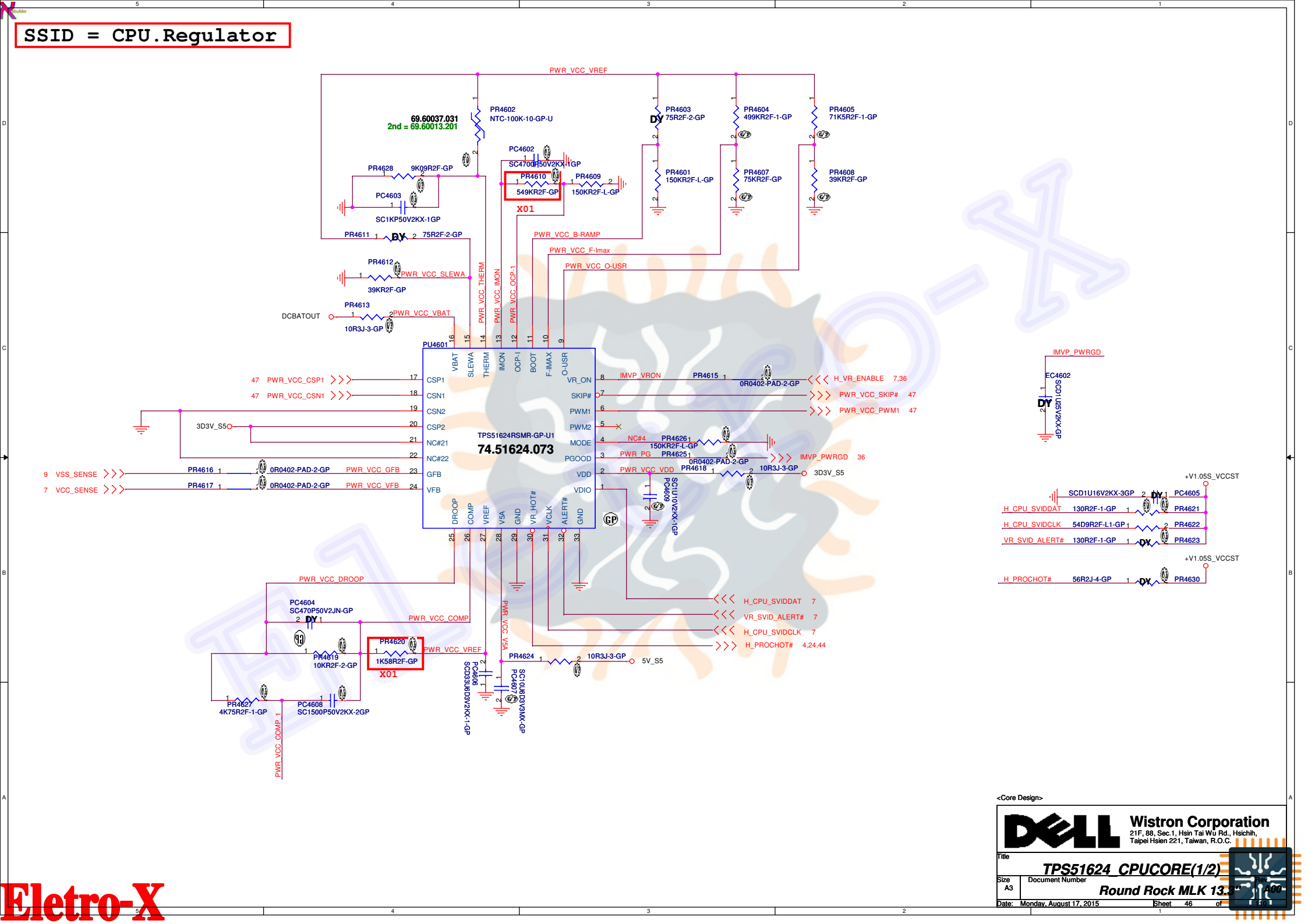
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51275

Size: A2 | Document Number: Round Rock MLK 13.3" | Rev: 1.00

Date: Monday, August 17, 2015 | Sheet 45 of 51

SSID = CPU.Regulator



<Core Design>

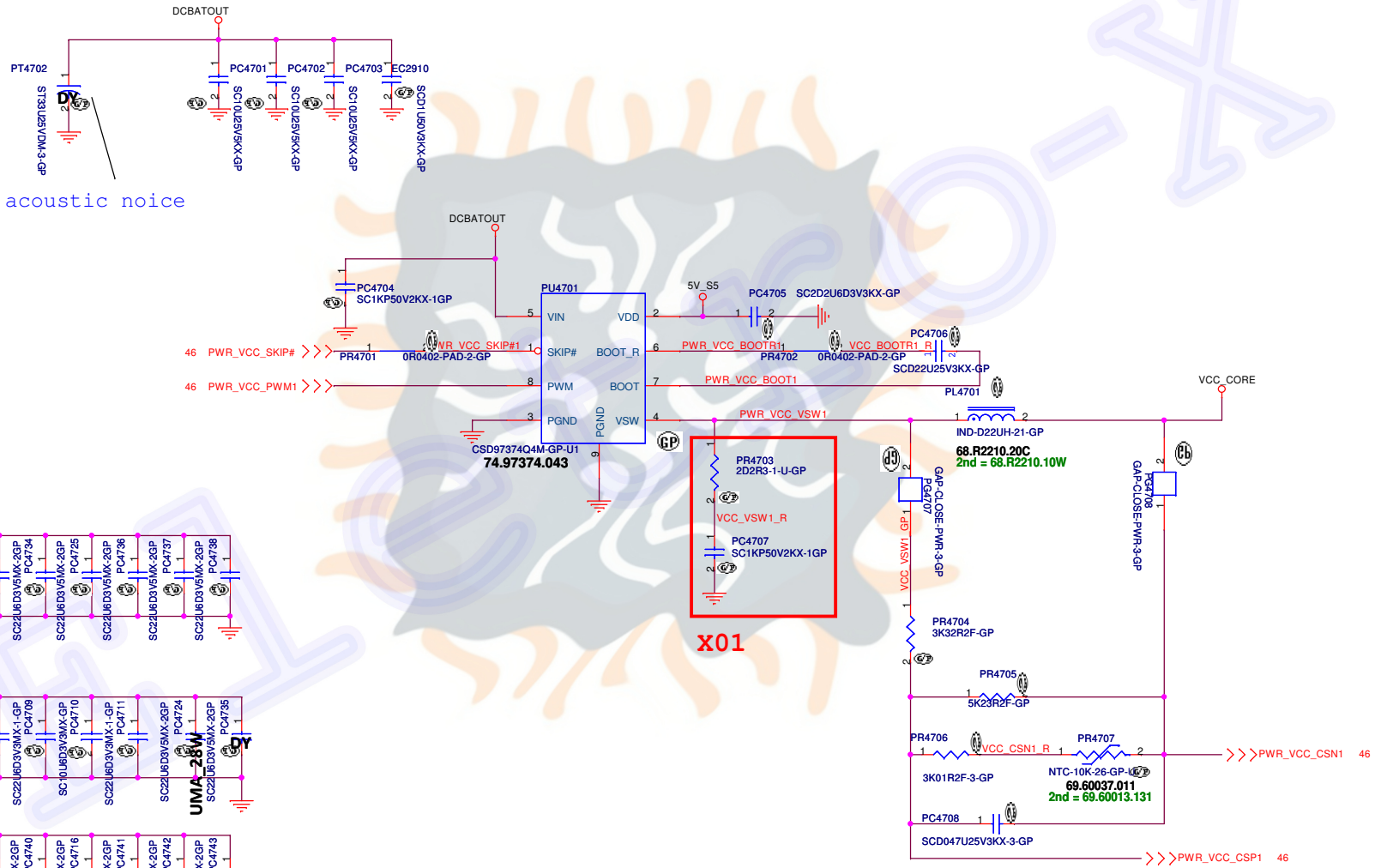
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51624_CPUCORE(1/2)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: 1A00

Date: Monday, August 17, 2015 | Sheet 46 of

SSID = CPU.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

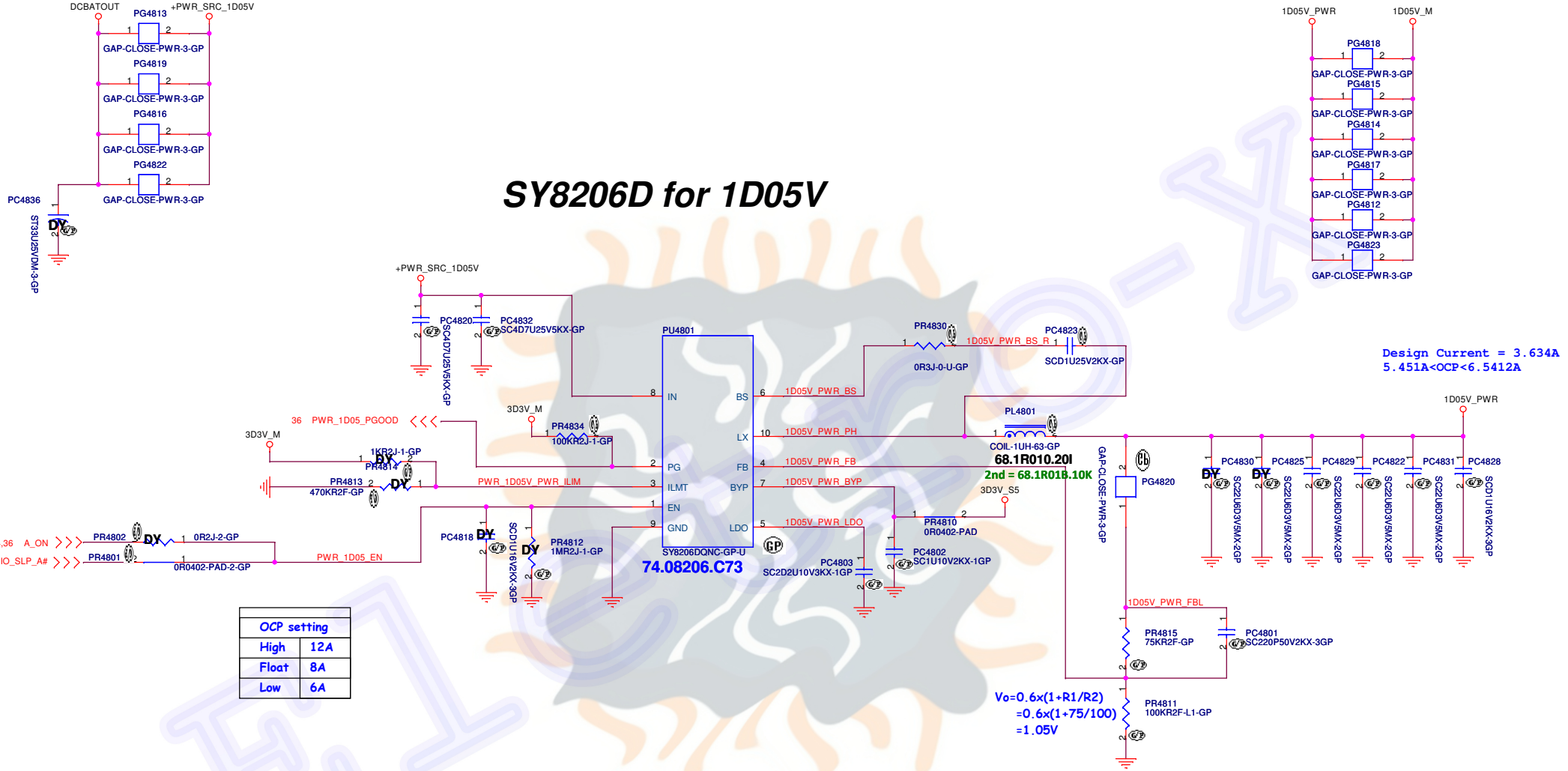
Title: TPS51624_CPUCORE(2/2)

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 47 of

SSID = PWR.Plane.Regulator_1p05v

SY8206D for 1D05V



OCP setting	
High	12A
Float	8A
Low	6A

<Core Design>

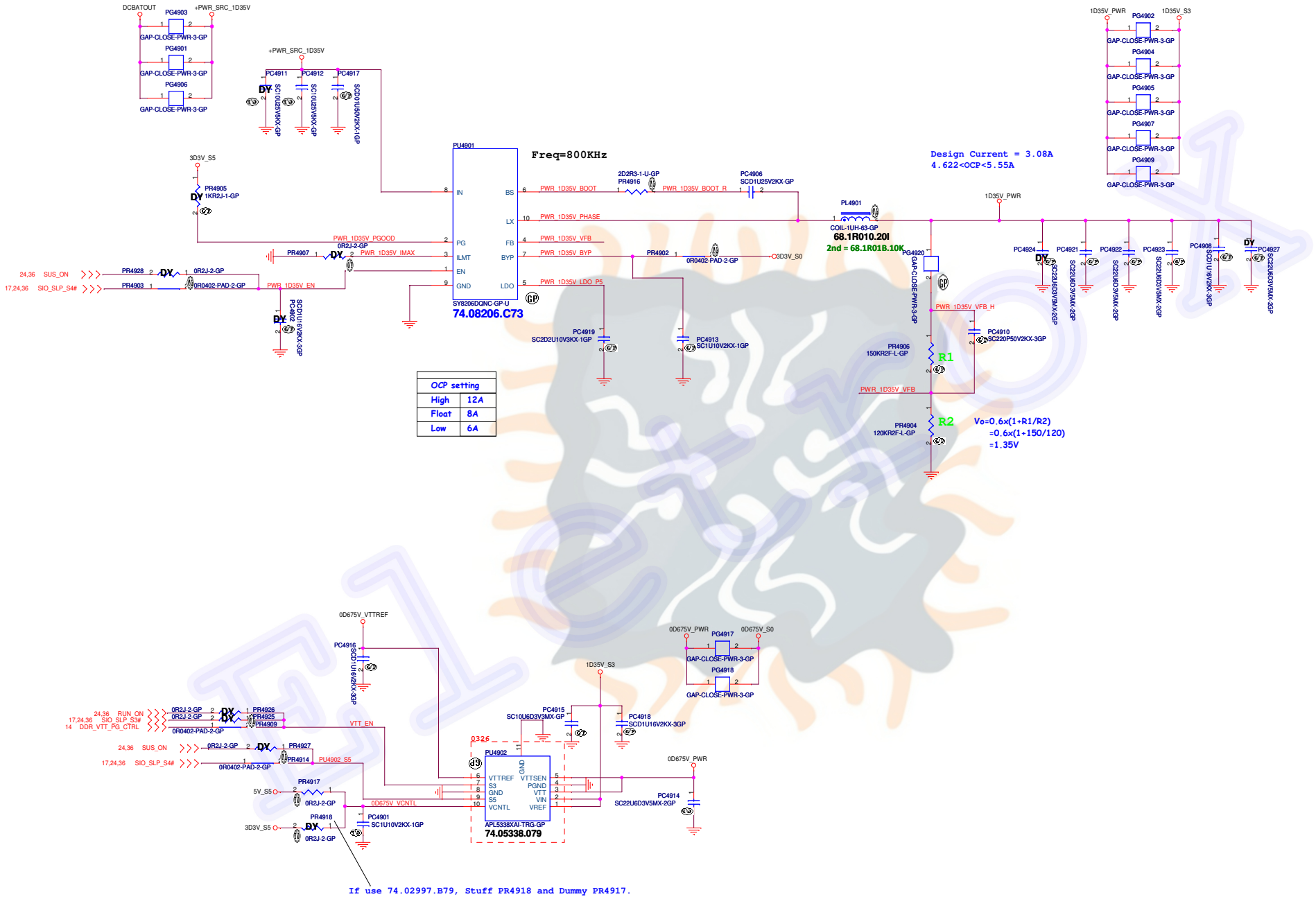
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8206_1D05V_M

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: 400

Date: Monday, August 17, 2015 | Sheet 48 of

SSID = PWR.Plane.Regulator_1p35v0p675v



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

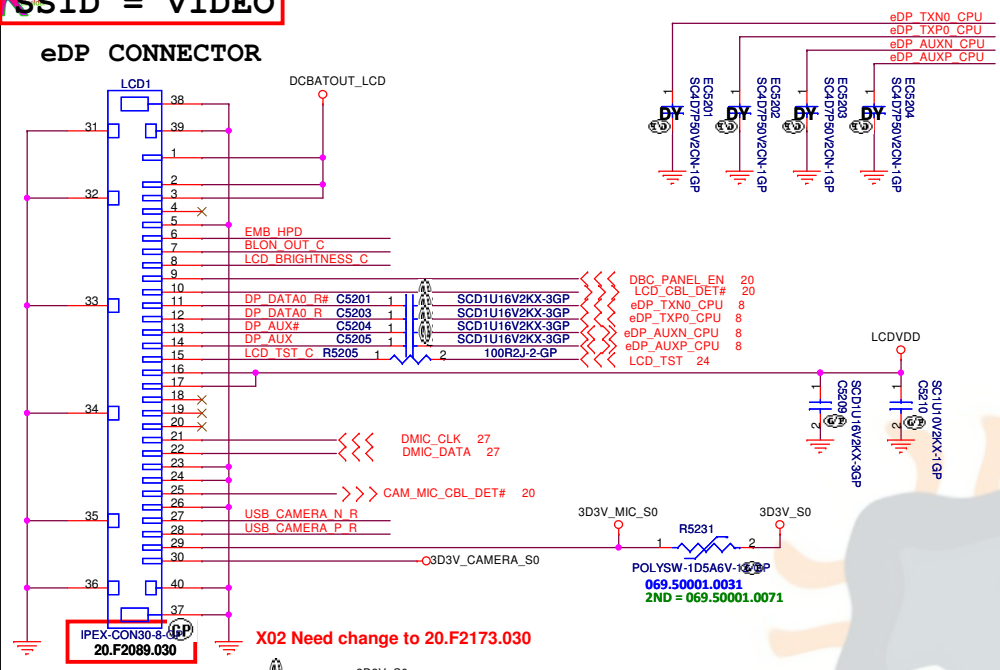
Title: SY8206_1D35V & 0D675V

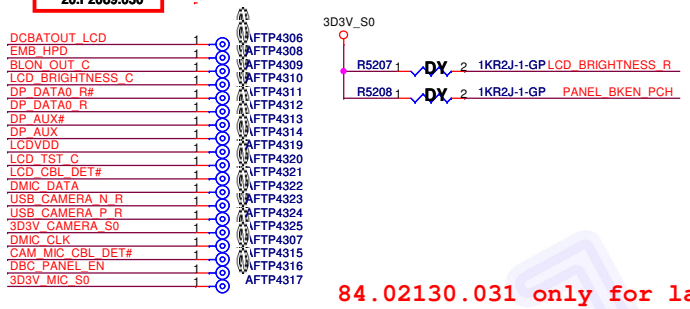
Size	Document Number	Rev
C	Round Rock MLK 13.3"	A00

Date: Monday, August 17, 2015 Sheet 49 of 110

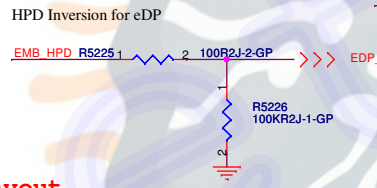
SSID = VIDEO

eDP CONNECTOR

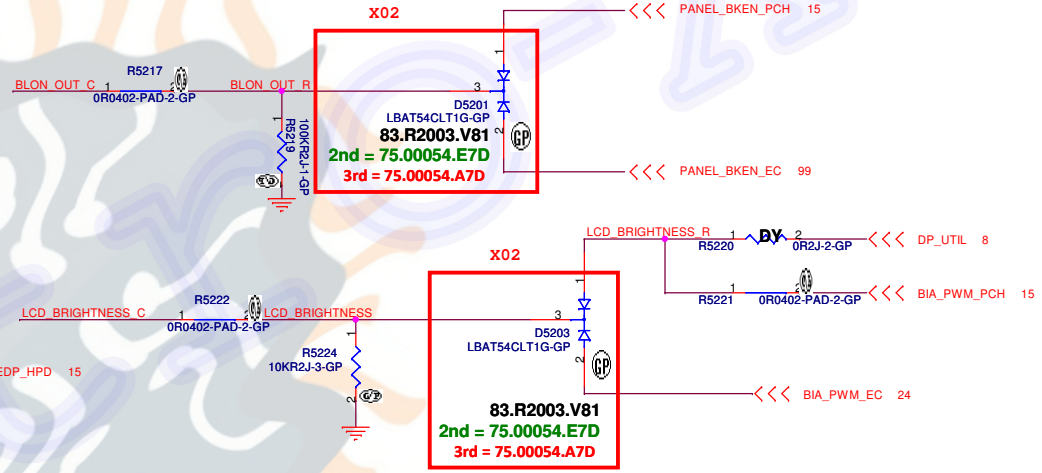




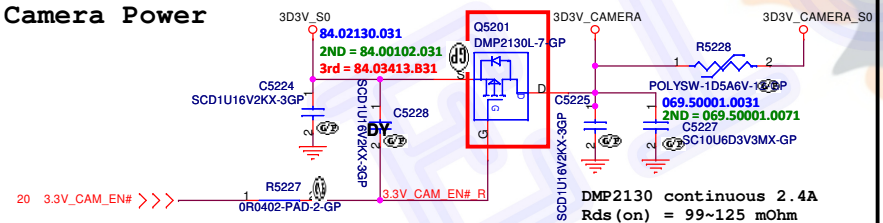
84.02130.031 only for layout

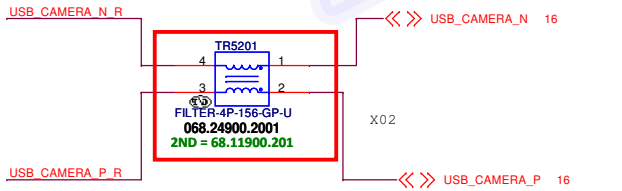


NOTE: EN has an internal pull down resistor to GND.



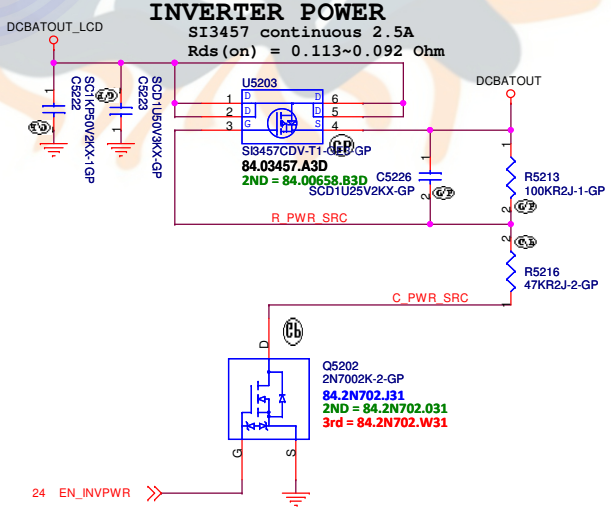
Camera Power





INVERTER POWER

SI3457 continuous 2.5A
Rds(on) = 0.113~0.092 Ohm



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: eDP Connector

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 52 of

SSID = VIDEO

HDMI CONNECTOR

Close to HDMI Connector

8 HDMI_CLK#
8 HDMI_CLK
C5401 1 SCD1U16V2KX-3GP HDMI_CLK_R_C#
C5402 1 SCD1U16V2KX-3GP HDMI_CLK_R_C

8 HDMI_DATA0#
8 HDMI_DATA0
C5403 1 SCD1U16V2KX-3GP HDMI_DATA0_R_C#
C5404 1 SCD1U16V2KX-3GP HDMI_DATA0_R_C

8 HDMI_DATA1#
8 HDMI_DATA1
C5405 1 SCD1U16V2KX-3GP HDMI_DATA1_R_C#
C5406 1 SCD1U16V2KX-3GP HDMI_DATA1_R_C

8 HDMI_DATA2#
8 HDMI_DATA2
C5407 1 SCD1U16V2KX-3GP HDMI_DATA2_R_C#
C5408 1 SCD1U16V2KX-3GP HDMI_DATA2_R_C

RN5401 SRN470J-5-GP
RN5402 SRN470J-5-GP

5V_S0
R5401 100KR2J-1-GP DY
Q5403 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
HDMI_PLL_GND
R5402 0R2J-2-GP DY

HDMI_CLK_R_C# R5404 0R0402-PAD-2-GP HDMI_CLK_R_C#_CON
HDMI_DATA1_R_C# R5405 0R0402-PAD-2-GP HDMI_DATA1_R_C#_CON
HDMI_CLK_R_C R5410 0R0402-PAD-2-GP HDMI_CLK_R_C_CON
HDMI_DATA1_R_C R5409 0R0402-PAD-2-GP HDMI_DATA1_R_C_CON
HDMI_DATA0_R_C# R5411 0R0402-PAD-2-GP HDMI_DATA0_R_C#_CON
HDMI_DATA2_R_C# R5412 0R0402-PAD-2-GP HDMI_DATA2_R_C#_CON
HDMI_DATA0_R_C R5413 0R0402-PAD-2-GP HDMI_DATA0_R_C_CON
HDMI_DATA2_R_C R5414 0R0402-PAD-2-GP HDMI_DATA2_R_C_CON

EV
HDMI_CLK_R_C#_CON R5415 150R2J-L1-GP-U HDMI_CLK_R_C_CON
HDMI_DATA0_R_C#_CON R5416 150R2J-L1-GP-U HDMI_DATA0_R_C_CON
HDMI_DATA1_R_C#_CON R5417 150R2J-L1-GP-U HDMI_DATA1_R_C_CON
HDMI_DATA2_R_C#_CON R5418 150R2J-L1-GP-U HDMI_DATA2_R_C_CON

5V_S0
D5401 AP2331SA-7-GP
074.02331.009B
2ND = 74.03517.07B
SCD1U16V2KX-3GP C5410
SCD1U16V2KX-3GP C5409
5V_HDMI
AFTP5414
AFTP5401

HDMI1 SKT-HDMI21-6-GP
22.10296.751
2ND = 22.10296.711
EV ME

HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
HDMI_CEC
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON

3D3V_S0
R5403 1MR2J-1-GP
Q5404 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
15 HDMI_PCH_DET
R5406 0R0402-PAD-2-GP
HDMI_HPD_S
HDMI_HPD_D
R5407 0R0402-PAD-2-GP
HPD_HDMI_CON
R5408 20KR2J-L2-GP

5V_S0
D5402 LBAW56LT1G-GP
83.00056.Y11
2nd = 75.00056.I7D
3rd = 75.00056.07D
5V_S0_D2
5V_S0_D1
RN5403 SRN2K2J-1-GP

3D3V_S0
Q5401 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DMN66.03F
15 PCH_HDMI_CLK
15 PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI

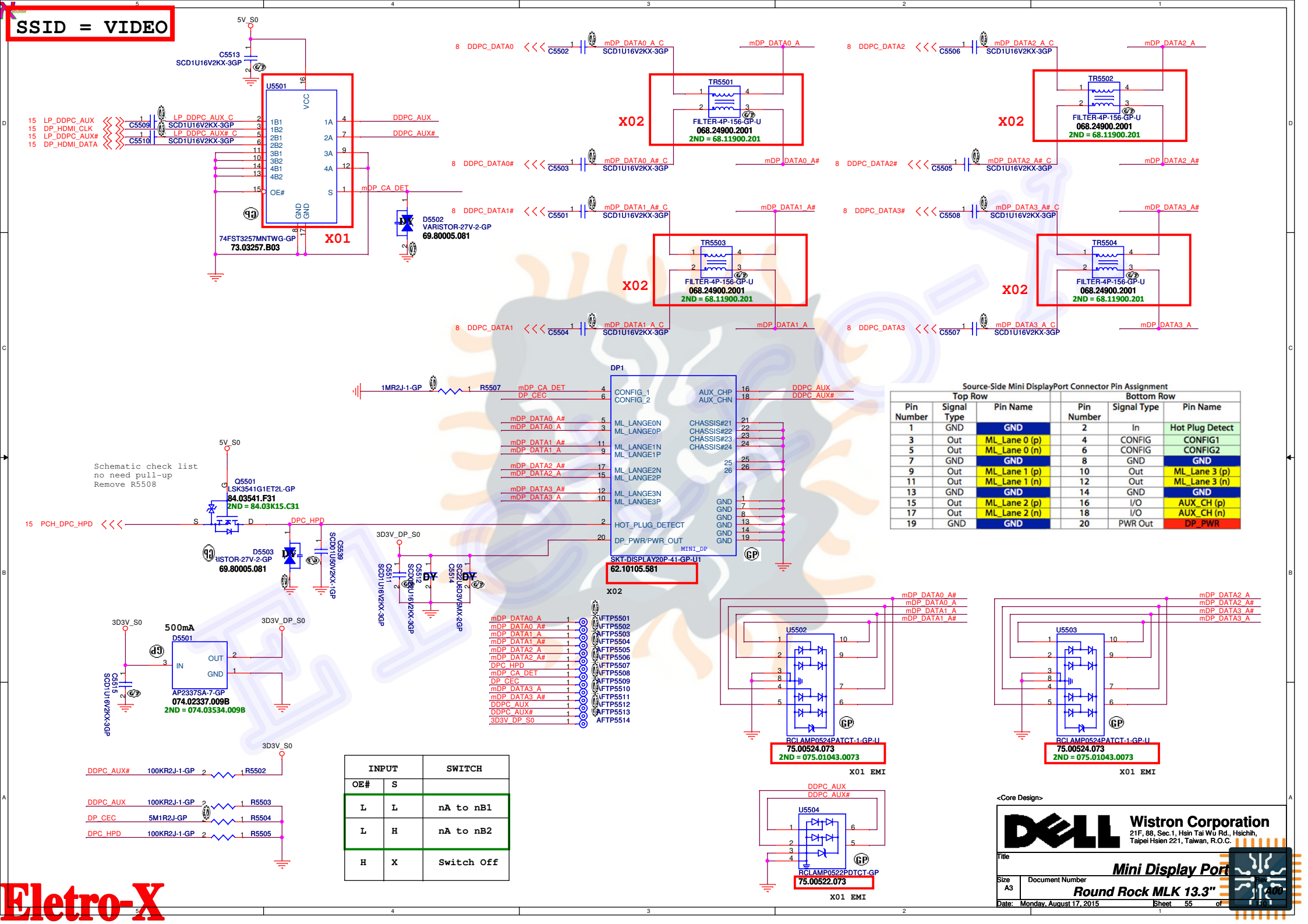
HDMI_DATA2_R_C_CON AFTP5402
HDMI_DATA2_R_C#_CON AFTP5403
HDMI_DATA1_R_C_CON AFTP5404
HDMI_DATA1_R_C#_CON AFTP5405
HDMI_DATA0_R_C_CON AFTP5406
HDMI_DATA0_R_C#_CON AFTP5407
HDMI_CLK_R_C_CON AFTP5408
HDMI_CLK_R_C#_CON AFTP5409
DDC_CLK_HDMI AFTP5410
DDC_DATA_HDMI AFTP5411
HPD_HDMI_CON AFTP5412
5V_HDMI AFTP5413

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Round Rock MLK 13.3"
Rev: A00
Date: Monday, August 17, 2015
Sheet 54 of

SSID = VIDEO



Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out	DP_PWR

INPUT		SWITCH
OE#	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	Switch Off

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Display Port
Size: A3
Document Number: Round Rock MLK 13.3"
Rev: A00
Date: Monday, August 17, 2015
Sheet 55 of

Eletro-X

SSID = SATA

R5601 0R0603-PAD-2-GP-U
3D3V_S0
3D3V_S0_HDD
C5601 SC68P-GP
C5602 SC3D3P50V2CN-GP
R5605 0R2J-2-GP
5V_S0_HDD
20 mSATA_DEVSLP
mSATA_DEVSLP_R
R5604 0R0402-PAD-2-GP
R5602 0R0603-PAD-2-GP-U
5V_S0
R5603 0R0603-PAD-2-GP-U
C5603 SC10U6D3MX-GP
C5604 SCD1U16V2KX-3GP
HDD1
SKT-SATA7P-15P-85-GP-U
20.81599.022
2nd = 22.10300.C51
3D3V_AUX_S5
R5607 100KR2J-1-GP
5V_HDD_ENABLE#
15V_S5
R5606 100KR2J-1-GP
Q5601 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DMN66.03F
EV reserved for modern stanby
19 SATA_TXP0
19 SATA_TXN0
19 SATA_RXP0
19 SATA_RXN0
C5605 SCD01U50V2KX-1GP
C5606 SCD01U50V2KX-1GP
C5608 SCD01U50V2KX-1GP
C5607 SCD01U50V2KX-1GP
SATA_TXP0_C
SATA_TXN0_C
SATA_RXP0_C
SATA_RXN0_C
HDD_DET# 19
EC5601 SC1KP50V2KX-1GP
FFS_INT2_Q 67
5V_S0
5V_S0_HDD
U5603 AO6402A-GP
84.06402.B3D
2ND = 84.P2703.03D
3rd = 84.03456.D3D
AO6402A MAX 7A
Rds(on) = 27~40m Ohm
5V_HDD_ENABLE
C5909 SC470P50V2KX-1GP
20 HDD_PWR_EN
R5608 0R2J-2-GP
HDD_PWR_EN_R
99 HDD_PWR_EN_SIO
R5610 0R2J-2-GP
R5609 100KR2J-1-GP
U5602 AZ1045-04F-R7G-GP
75.01045.073
2nd = 75.01004.073
EV EMC
550 mA
3D3V_S0
3D3V_S0_HDD
U5601 TPS22965DSGR-GP-U
74.22965.093
2nd = 74.03526.093
20 3.3V_HDD_EN
5V_S5
3D3V_S0_HDD_CT
C5612 SC10U10V5KX-2GP
C5611 SC470P50V2KX-3GP

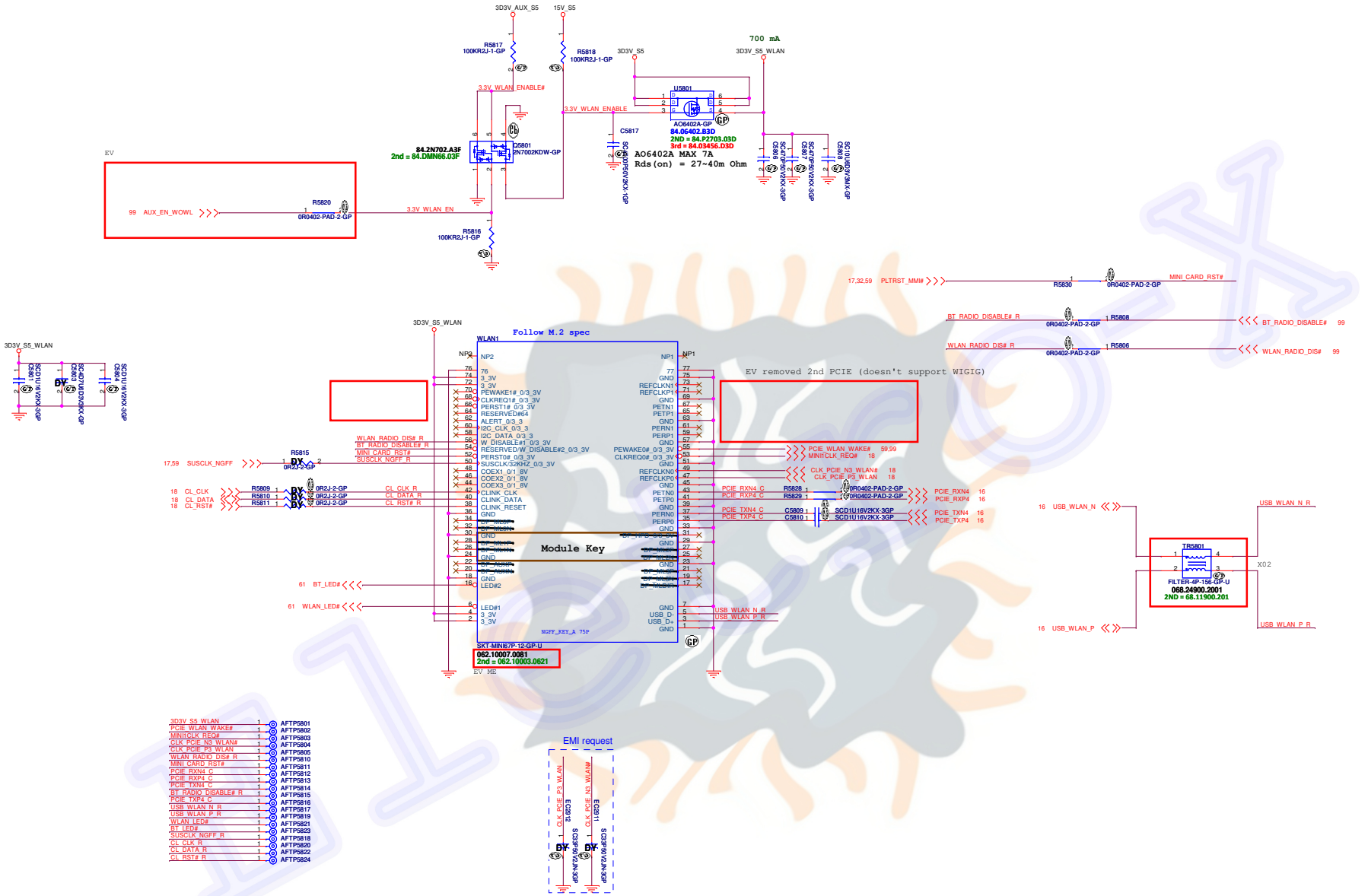
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD
Size: A4
Document Number: Round Rock MLK 13.3"
Rev: A00
Date: Monday, August 17, 2015
Sheet 56 of 110

Eletro-X

SSID = WIRELESS

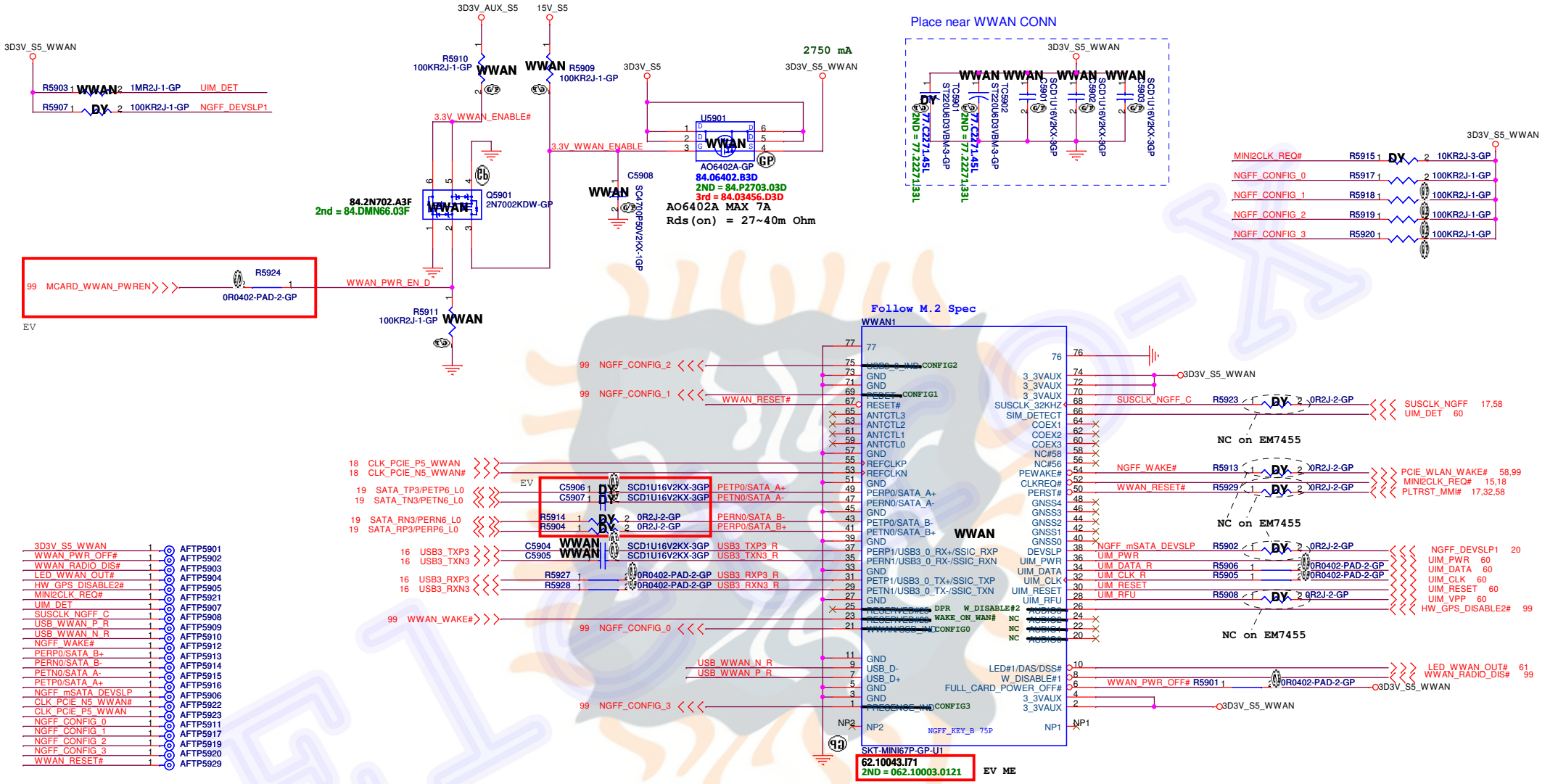


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)
Size: Document Number: Round Rock MLK 13.3"
Date: Monday, August 17, 2015 Sheet 58

SSID = WIRELESS NGFF(WWAN/SSD)



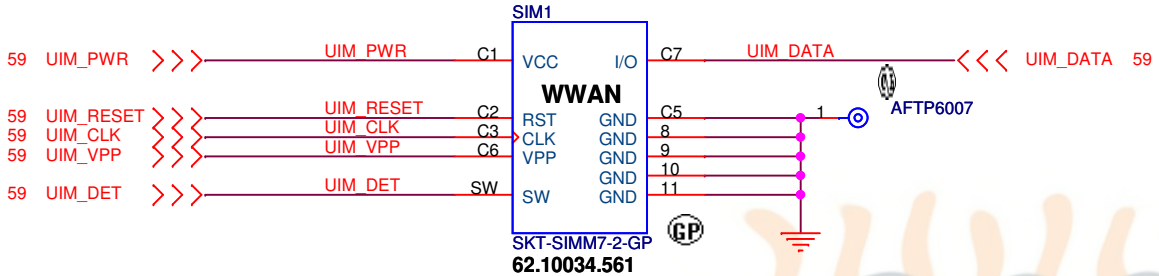
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD – SATA
1	GND	NC	GND	GND	SSD - PCIe
8	NC	GND	GND	GND	WWAN
14	NC	GND	NC	NC	HCA - PCIe
15	NC	NC	NC	NC	No Module Present

<Core Design>

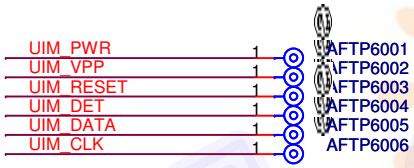
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

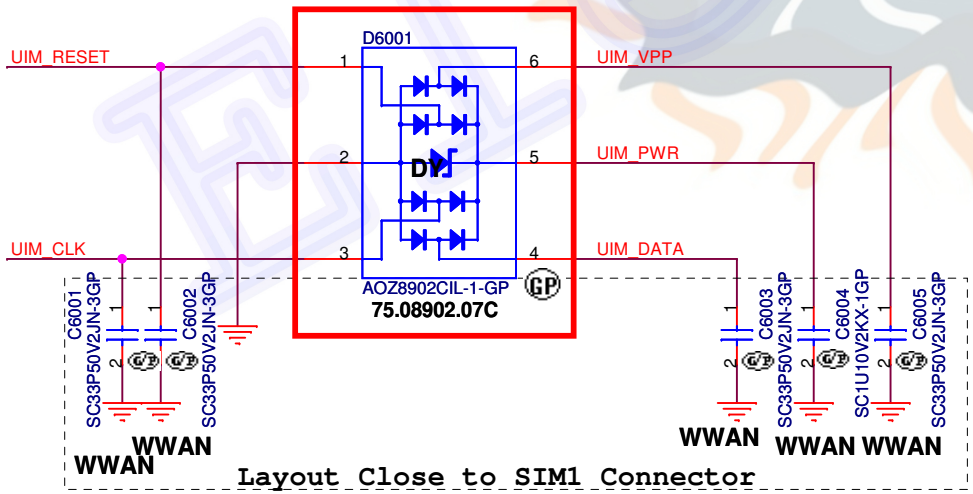
Title: NGFF-WWAN/SSD
Size: Document Number: Round Rock MLK 13.3"
Rev: A00
Date: Monday, August 17, 2015 Sheet 59 of

SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND





<Core Design>

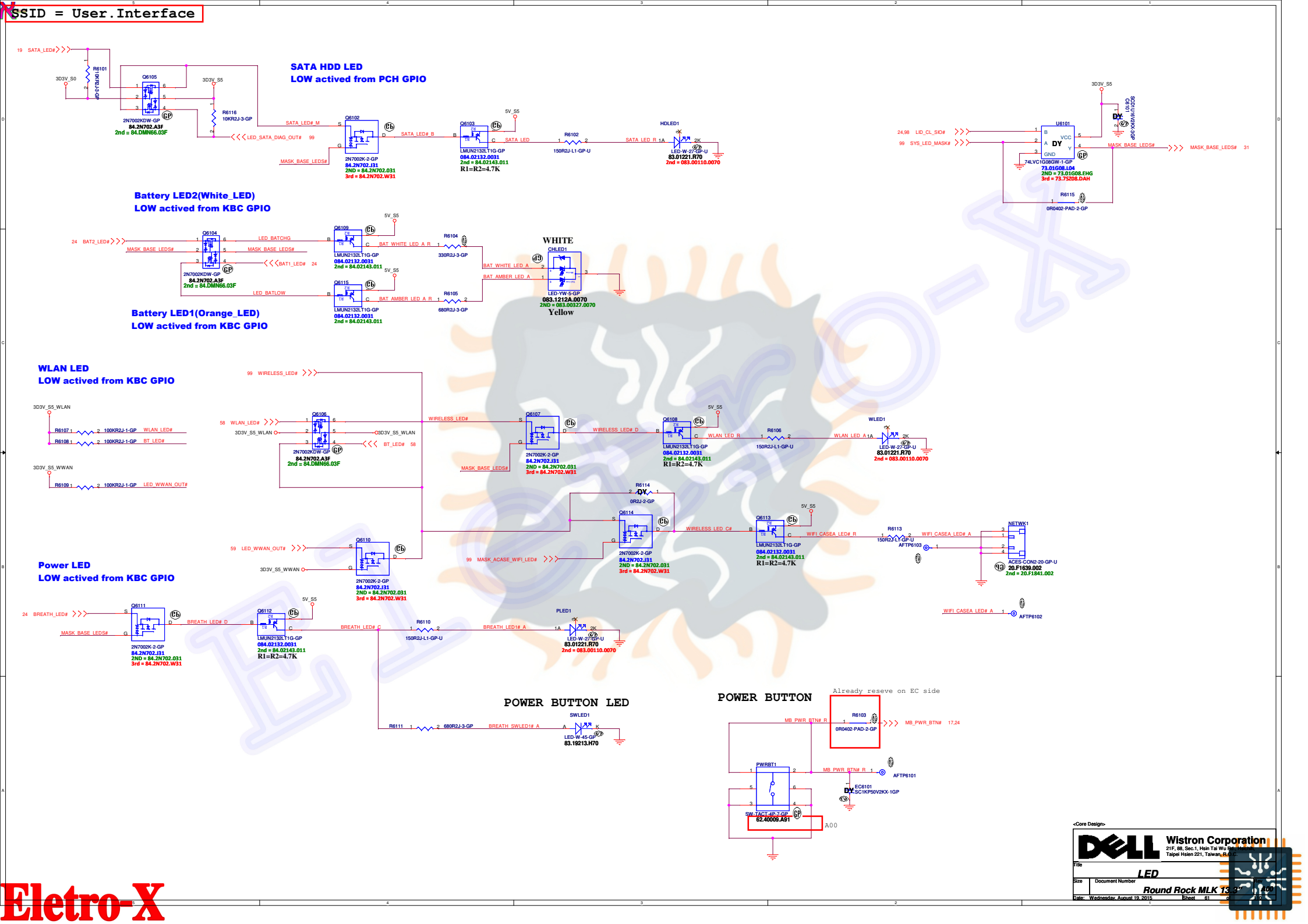
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: uSIM

Size | Document Number: Round Rock MLK 13.3" | Rev: A00

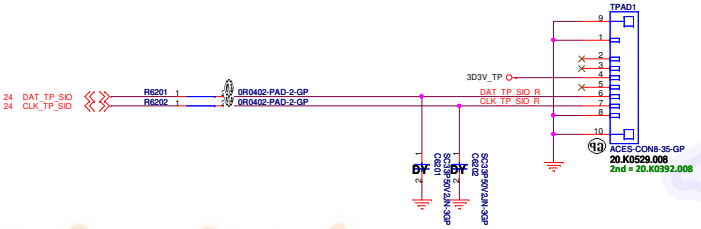
Date: Monday, August 17, 2015 | Sheet 60 of 110

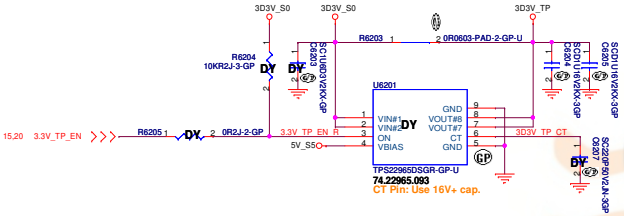
SSID = User.Interface



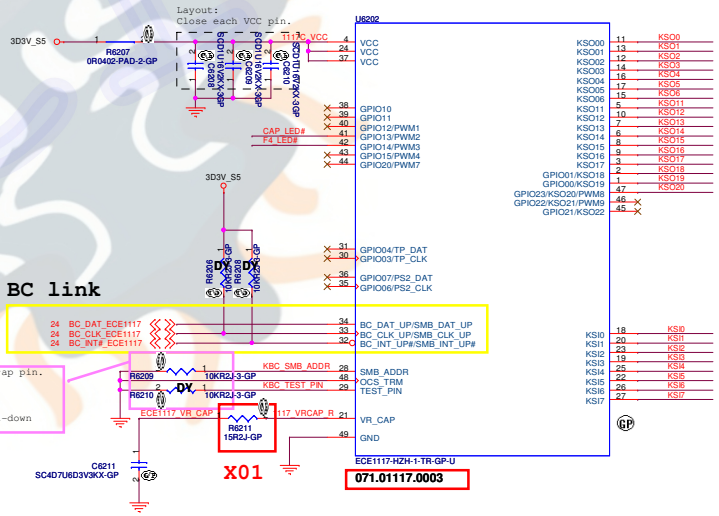
SSID = KBC | SSID = Touch.Pad

TouchPad Connector

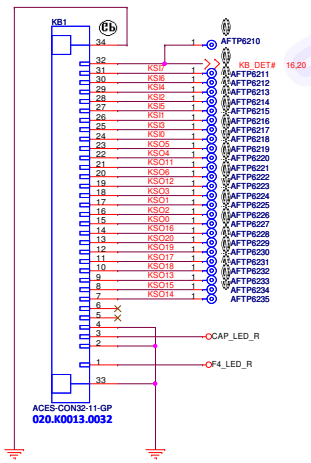




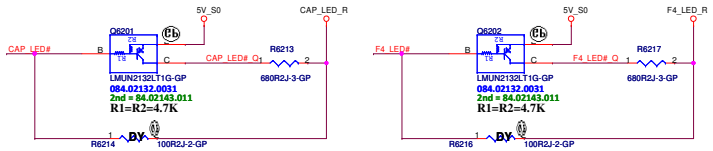
KBC SMSC ECE1117c



Internal KeyBoard Connector



MB Pin NO.	Description	Module Pin NO.
32	Diagnostic	1
31	KSI[7]:S8	2
30	KSI[6]:S7	3
29	KSI[4]:S5	4
28	KSI[2]:S3	5
27	KSI[5]:S6	6
26	KSI[1]:S2	7
25	KSI[3]:S4	8
24	KSI[0]:S1	9
23	KSO[5]:D6	10
22	KSO[4]:D5	11
21	KSO[11]:D8	12
20	KSO[6]:D7	13
19	KSO[12]:D9	14
18	KSO[3]:D4	15
17	KSO[1]:D2	16
16	KSO[2]:D3	17
15	KSO[0]:D1	18
14	KSO[16]:D13	19
13	KSO[20]:D17	20
12	KSO[19]:D16	21
11	KSO[17]:D14	22
10	KSO[18]:D15	23
9	KSO[13]:D10	24
8	KSO[15]:D12	25
7	KSO[14]:D11	26
6	NC	27
5	NC	28
4	GND	29
3	Caps Lock LED	30
2	GND	31
1	F4 LED	32



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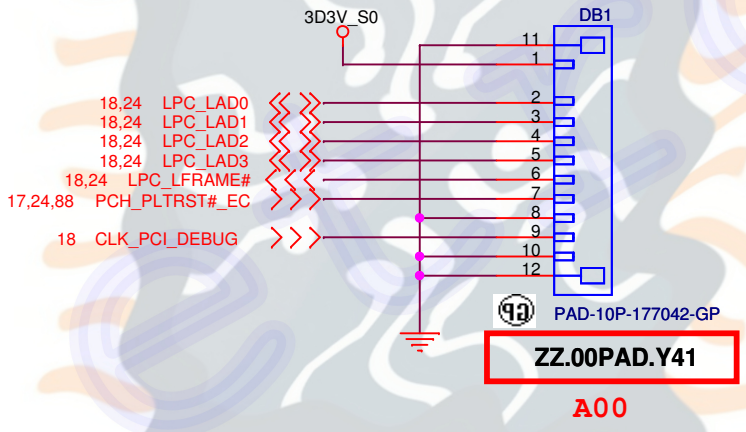
Title: Key Board/Touch Pad
Size: Document Number
Round Rock MLK 13.3"
Date: Monday, August 17, 2015 Sheet 62

SSID = DEBUG PORT



<Core Design>

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Title: Debug connector

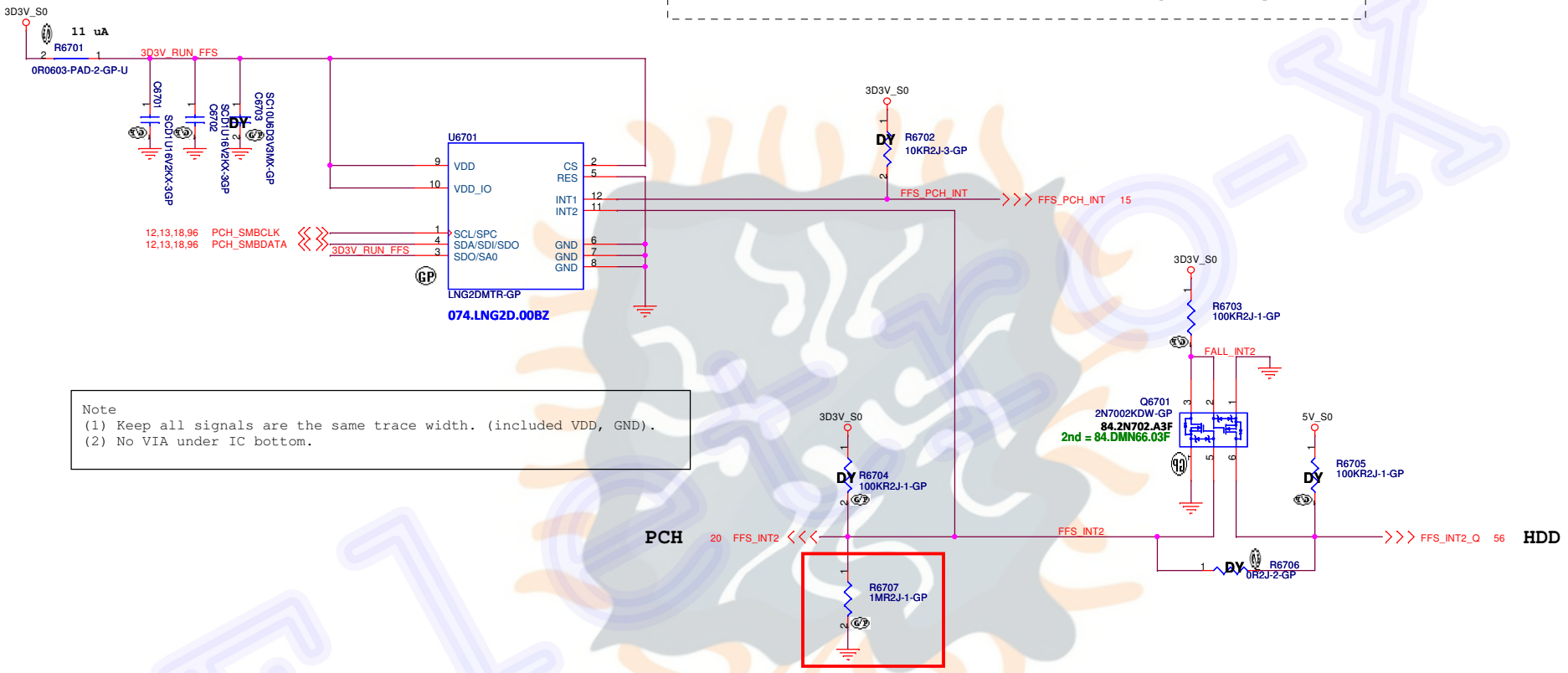
Size | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 65 of 116

SSID = User.interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Vender suggest,reserve to prevent error trigger

<Core Design>

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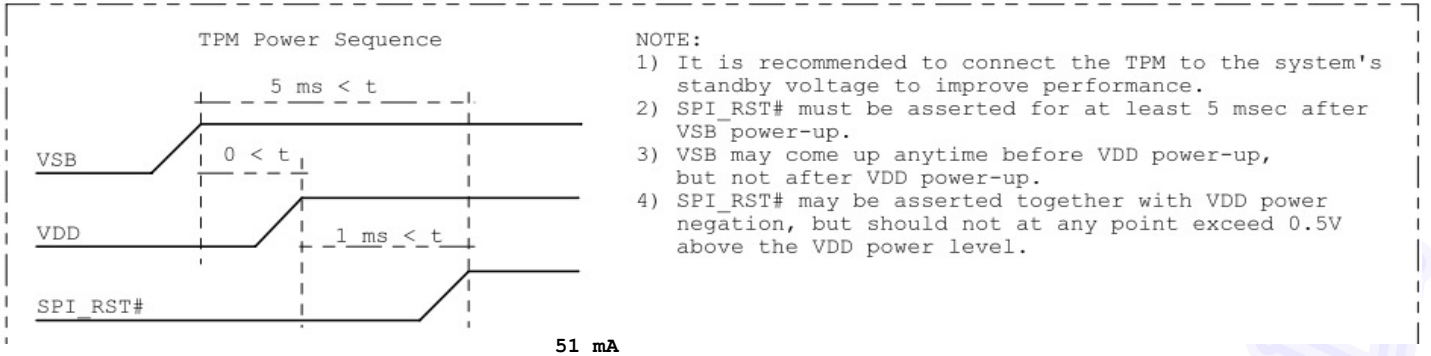
Title: Free Fall Sensor

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 67 of

SSID = TPM



NOTE:
1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
2) SPI_RST# must be asserted for at least 5 msec after VSB power-up.
3) VSB may come up anytime before VDD power-up, but not after VDD power-up.
4) SPI_RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

51 mA

EV Reseved for modern stanby

Measure power consumption on EV board

X02

84.02130.031 only for layout

84.02130.031
2ND = 84.00102.031
3rd = 84.03413.B31

U8801
NPCT650JA0YX-GP
071.00650.0B03

<Core Design>

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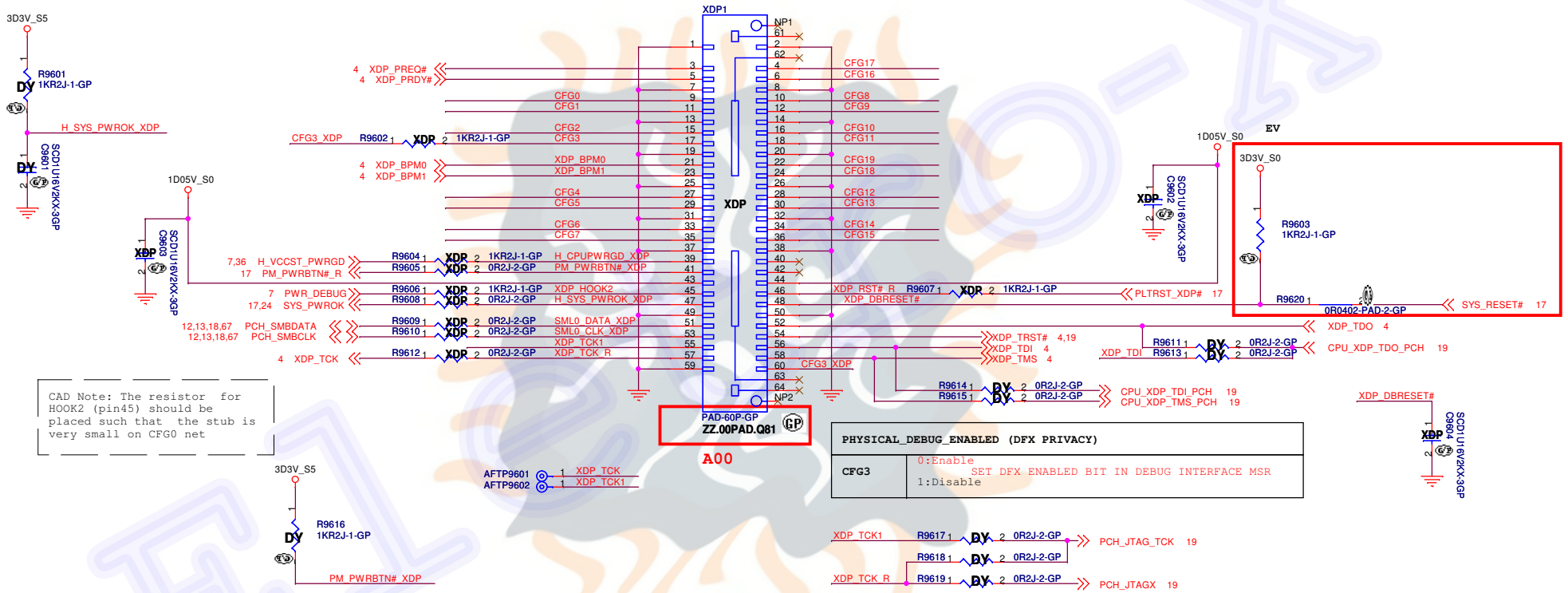
Title: TPM
Size: Document Number: Round Rock MLK 13.3" Rev: A00
Date: Monday, August 17, 2015 Sheet 88 of 110

SSID = CPU_XDP

CPU_XDP



<Core Design>

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Title: CPU_XDP

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 96 of

SSID = User.Interface

TOUCH PANEL POWER

84.02130.031 only for layout

3D3V_S0 — R9809 1 — 2 TOUCH_PANEL_INTR# — 10KR2J-3-GP

5V_S0 — 84.02130.031 / 2ND = 84.00102.031 / 3rd = 84.03413.B31

C9810 SC10U6D3V3MX-GP

Q9801 DMP2130L-7-GP

5V_TSP — R9806 PCSSW-1D5A6V-12-GP — 069.50001.0031 / 2ND = 069.50001.0071 — 5V_TSP_S0

C9812 SC10U10V5KX-2GP

C9811 SCD1U16V2KX-3GP DY

R9808 100KR2J-1-GP

TOUCH PANEL CONNECTOR

TOUCH1 — 5V_TSP_S0

TOUCHLCD_N

TOUCHLCD_P

TOUCH_PANEL_INTR# 20

AFTP9805

ACES-CONN20-GP-U — 20.F1639.006 / 2ND = 20.F1804.006 / EV ME

AFTP9801 5V_TSP_S0

AFTP9802 TOUCH_PANEL_INTR#

AFTP9803 TOUCHLCD_N

AFTP9804 TOUCHLCD_P

15,20 3.3V_TS_EN — R9807 — 0R0402-PAD-2-GP — 3.3V_TS_EN_R

Q9802 2N7002K-2-GP — 84.2N702.J31 / 2ND = 84.2N702.031 / 3rd = 84.2N702.W31

3.3V_TS_EN#

5V_TSP_S0 — U9802 AZC002-02N-GP DY

TOUCHLCD_N — TOUCHLCD_P

TR9801 FILTER-4P-156-GP-U — 068.24900.2001 / 2ND = 68.11900.201

TOUCHLCD_N — TOUCHPANEL_N 16

TOUCHLCD_P — TOUCHPANEL_P 16

X02

EV follow ARD

ME_FWP_EC R9802 0R2J-2-GP ME_FWP

Install after MP

Firmware SW

MESW1 SW-SLIDE6P-6-GP — 62.40018.691

24 ME_FWP_EC

19 ME_FWP

3D3V_S5_PCH — R9812 1KR2J-1-GP DY — MESW1_B

	A	B
ME_FWP	Low	High
	Normal Operation (Default)	Override

EV DY for LIDSW1 is PP

Lid Close

3D3V_S5

LIDSW1 S-5712ACDL1-M3T1U-GP — 74.05712.0BB / 2ND = 74.01810.0BB

VSS VDD OUT

LID_CL#

R9804 100KR2J-1-GP DY

SCD1U16V2KX-3GP C2314 DY

R9805 10R2J-2-GP

LID_CL_SIO# 24,61

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Title: Function Button

Size | Document Number: Round Rock MLK 13.3 | Rev: A00

Date: Tuesday, August 18, 2015 | Sheet 98 of

Eletro-X

SSID = SIO

59 NGFF_CONFIG_0
59 NGFF_CONFIG_1
59 NGFF_CONFIG_2
61 MASK_ACASE_WIFI_LED#

VGA_ID
PCIE_WAKE#
R9903 1 — 0R0402-PAD-2-GP
WIRELESS_LED#

PCIE_WLAN_WAKE# 58,59
WLAN_RADIO_DIS# 58
WIRELESS_LED# 61

3D3V_S5 — R9906 1 — 0R0402-PAD-2-GP — 1099_VCC

C9804 SCD1U16V2KX-3GP
C9805 SC10U6D3V3MX-GP DY
C9806 SCD1U16V2KX-3GP

20,24,30 LAN_WAKE# — R9905 1 — DY — 2 0R2J-2-GP — PCIE_WLAN_WAKE#

U9901

VCC 8
VCC 28

GPIO37/KSO15 23
GPIO36/KSO14 22
GPIO35/KSO13 21
GPIO34/KSO12 20
GPIO33/KSO11 19
GPIO32/KSO10 18
GPIO31/KSO09 17
GPIO30/KSO08 16

59 NGFF_CONFIG_3 — NGFF_CONFIG_3 — GPIO00/KSO16 24
35 USBPWRSHR_VBUS_EN — USBPWRSHR_VBUS_EN — GPIO01/KSO17 25
PROCHOT_GATE — GPIO02/KSO18 26
59 MCARD_WWAN_PWREN — MCARD_WWAN_PWREN — GPIO03/KSO19 27
59 HW_GPS_DISABLE2# — HW_GPS_DISABLE2# — GPIO04/KSO20 29
35 USB_SIDE_EN# — USB_SIDE_EN# — GPIO05/KSO21 30
GPIO06/KSO22 31
56 HDD_PWR_EN_SIO — HDD_PWR_EN_SIO — GPIO07 36

EV reserved for modern standby

R9949 1 — 2 10KR2J-3-GP — TEST_PIN — RESERVED#37 37 — TEST_PIN 38
R9950 1 — 2 10KR2J-3-GP — SMB_ADDR — SMB_ADDR 35

GPIO27/KSO07 15 — LED_SATA_DIAG_OUT# 61
GPIO26/KSO06 14 — SYS_LED_MASK# 61
GPIO25/KSO05 13 — WLAN_LAN_DISBL# 30
GPIO24/KSO04 12 — BT_RADIO_DISABLE# 58
GPIO23/KSO03 11 — WWAN_WAKE# 59
GPIO22/KSO02 10
GPIO21/KSO01 9
GPIO20/KSO00 7

BC_DAT/SMB_DATA 32 — BC_DAT_ECE1099 24
BC_CLK/SMB_CLK 33 — BC_CLK_ECE1099 24
BC_INT#/SMB_INT# 34 — BC_INT#_ECE1099 24

GPIO10/KSI0 39
GPIO11/KSI1 40
GPIO12/KSI2 1
GPIO13/KSI3 2
GPIO14/KSI4 3
GPIO15/KSI5 4
GPIO16/KSI6 5
GPIO17/KSI7 6

GND 41

ECE1099-FZG-GP
71.01099.003

3D3V_S5

R9913 1 — 2 100KR2J-1-GP — WWAN_RADIO_DIS#
R9926 1 — 2 10KR2J-3-GP — MASK_ACASE_WIFI_LED#
R9912 1 — 2 100KR2J-1-GP — WLAN_RADIO_DIS#
R9911 1 — 2 100KR2J-1-GP — WLAN_LAN_DISBL#
R9910 1 — 2 100KR2J-1-GP — BT_RADIO_DISABLE#
R9924 1 — 2 10KR2J-3-GP — WWAN_WAKE#
R9907 1 — 2 100KR2J-1-GP — WIRELESS_LED#
R9908 1 — DY — 2 100KR2J-1-GP — PROCHOT_GATE
R9917 1 — 2 100KR2J-1-GP — HW_GPS_DISABLE2#
R9902 1 — 2 100KR2J-1-GP — USBPWRSHR_VBUS_EN
R9901 1 — 2 10KR2J-3-GP — PCIE_WAKE#
R9904 1 — 2 100KR2J-1-GP — USB_SIDE_EN#
R9923 1 — 2 100KR2J-1-GP — VGA_ID

17 SIO_SLP_WLAN#
30 LAN_DISABLE#
27,29 AUD_HP_NB_SENSE
27 AUD_NB_MUTE#
59 WWAN_RADIO_DIS#
52 PANEL_BKEN_EC
58 AUX_EN_WOWL

	VGA_ID0
Discrete	0
UMA	1

R9936 1 — 2 100KR2J-1-GP — AUX_EN_WOWL
R9944 1 — 2 10KR2J-3-GP — SYS_LED_MASK#

<Core Design>

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Title: SIO - ECE1099

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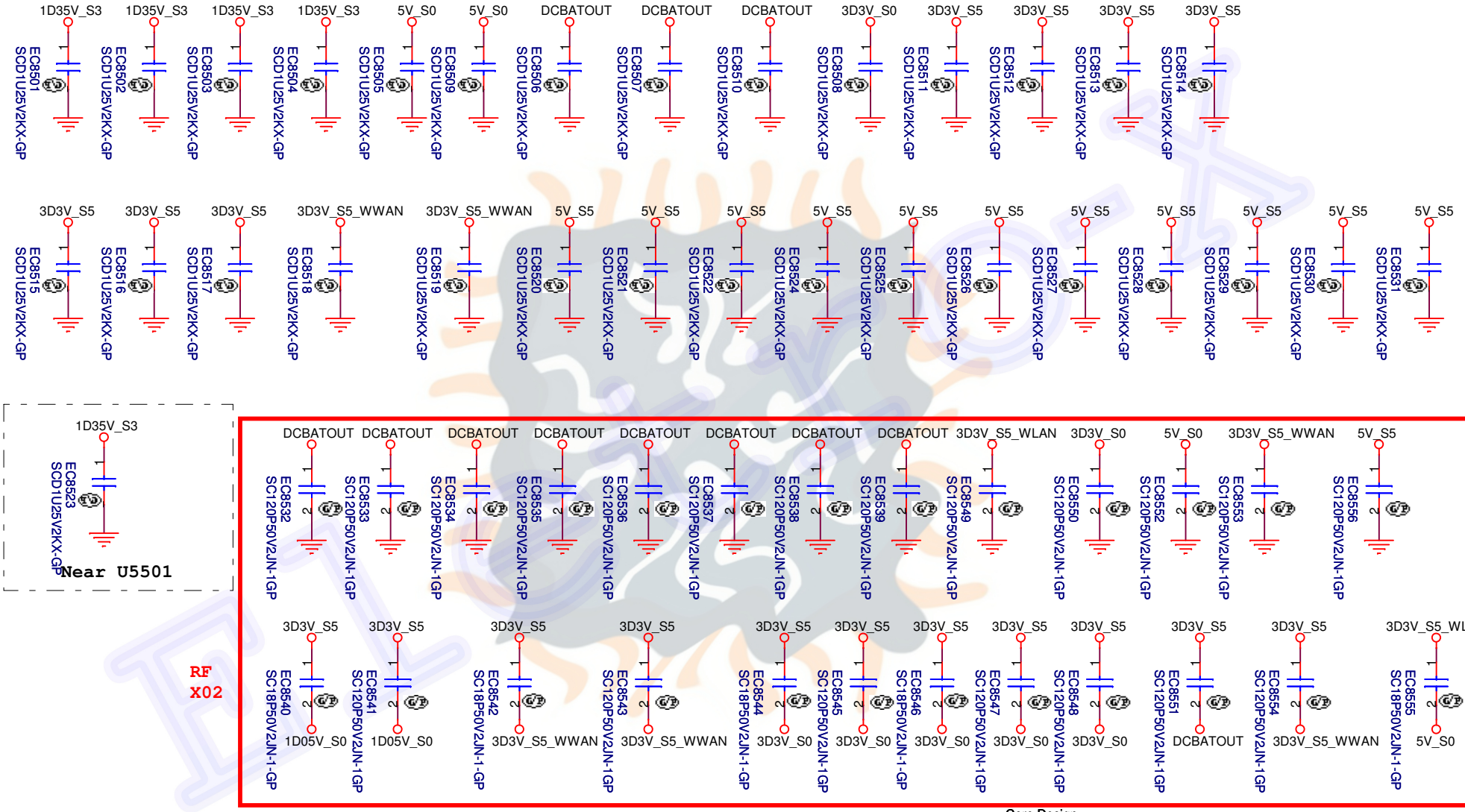

RF
X02

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI Capacitors1***

Size	Document Number	Rev
A4	***Round Rock MLK 13.3"***	A00

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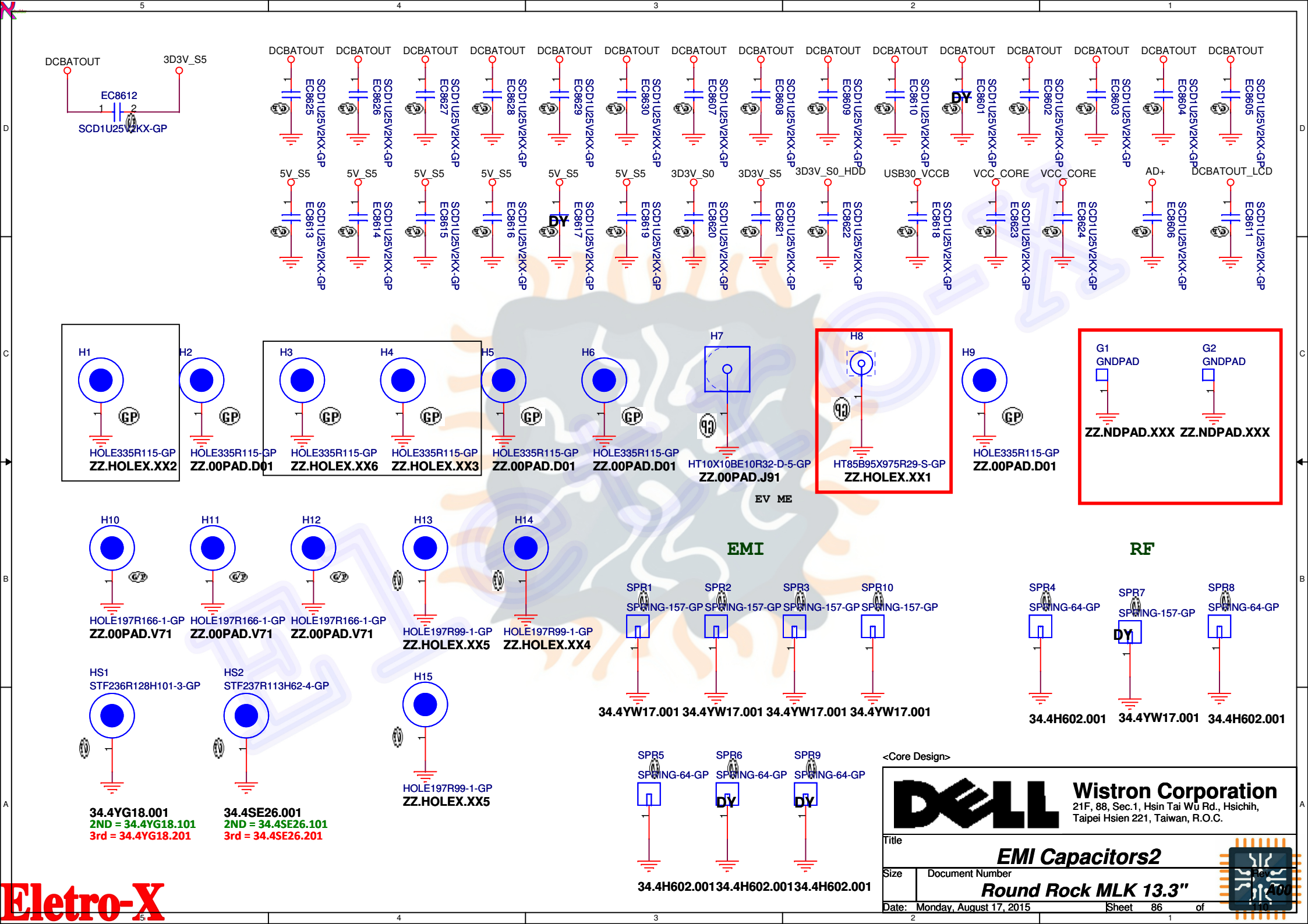
DCBATOUT
3D3V_S5
EC8612
SCD1U25V2KX-GP
5V_S5
3D3V_S0
3D3V_S5
3D3V_S0_HDD
USB30_VCCB
VCC_CORE
AD+
DCBATOUT_LCD
DY
H1
H2
H3
H4
H5
H6
H7
H8
H9
HOLE335R115-GP
ZZ.HOLEX.XX2
ZZ.00PAD.D01
ZZ.HOLEX.XX6
ZZ.HOLEX.XX3
HT10X10BE10R32-D-5-GP
ZZ.00PAD.J91
EV ME
HT85B95X975R29-S-GP
ZZ.HOLEX.XX1
G1
GNDPAD
G2
GNDPAD
ZZ.NDPAD.XXX
H10
H11
H12
H13
H14
HOLE197R166-1-GP
ZZ.00PAD.V71
HOLE197R99-1-GP
ZZ.HOLEX.XX5
ZZ.HOLEX.XX4
EMI
RF
SPR1
SPR2
SPR3
SPR10
SPRING-157-GP
34.4YW17.001
SPR4
SPR7
SPR8
SPRING-64-GP
34.4H602.001
HS1
STF236R128H101-3-GP
34.4YG18.001
2ND = 34.4YG18.101
3rd = 34.4YG18.201
HS2
STF237R113H62-4-GP
34.4SE26.001
2ND = 34.4SE26.101
3rd = 34.4SE26.201
H15
SPR5
SPR6
SPR9
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI Capacitors2
Size
Document Number
Round Rock MLK 13.3"
Rev
A00
Date: Monday, August 17, 2015
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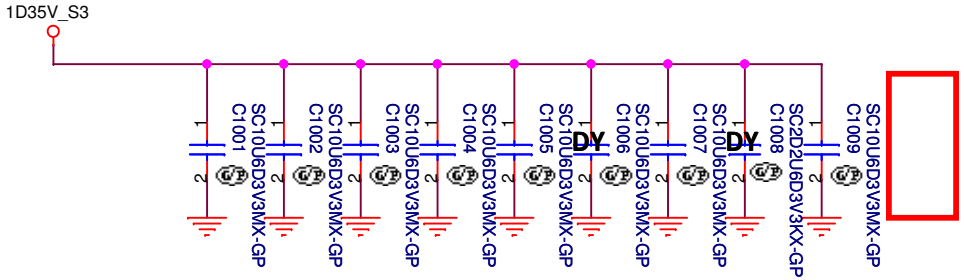
Eletro-X



<Core Design>

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Title: ***CPU (Power CAP1)***

Size	Document Number	Rev
A4	***Round Rock MLK 13.3"***	***A00***

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Processor Strapping

Broadwell ULT Processor Platform Design Guide Rev2.0

Name	Strap Description	Schematics Notes
CFG[0]		Connect a series 1 k resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.
CFG[4]	Display Port Presence strap	1:Disabled – No Physical Display Port attached to Embedded DisplayPort. No connect for disable. 0:Enabled – An external Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1KΩ ± 5% resistor to enable port.
SPKR/GPIO81	No Reboot on TCO Timer expiration	This signal has an integrated weak pull-down (20KΩ nominal) to enable reboot on TCO Timer expiration. Pull up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor to disable this capability.
SDIO_D0/GPIO66	Top-Block Swap Override	This signal has an integrated weak pull-down (20KΩ nominal) resistor to disable Top-Block Swap mode. To enable Top-Block Swap, this signal should be pulled up to VCCSDIO through a 1K to 4.7KΩ ± 5% resistor. The reference voltage for this strap is VCCSDIO.
INTVRMEN	Integrated VRM Enable/Disable	This signal has no integrated pull-up/pull-down resistor. To enable the integrated voltage regulator for DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 this signal must be pulled to VCCRTC through a weak resistor (e.g.330KΩ ± 5%). To disable the integrated voltage regulator, this signal must be pulled down through a weak resistor (e.g. 330KΩ ± 5%) and the DCPSUS rails must be powered externally.
GSPI0_MOSI/GPIO86	Boot BIOS Strap Bit (BBS)	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable boot from SPI. To enable boot to LPC this signal must be pulled up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor.
HDA_SDO/I2S0_TXD	Flash Descriptor Security Override	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable security measures in the flash descriptor. To enable Flash Descriptor Security Override this signal must be pulled up to VCCHDA through a 1K to 4.7KΩ ± 5% resistor.
GPIO15	TLS Confidentiality	This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. To enable Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality this signal must be pulled up to VCCSUS3_3 through a 1K to 8.2KΩ ± 5% resistor.
DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1K to 3.6KΩ ± 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1K to 3.6KΩ ± 5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	This signal has no integrated pull-up/pull-down. This signal must always be pulled to VCCRTC through a weak resistor (e.g. 330KΩ ± 5%).

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2 (win debug)
2	WWAN
3	WLAN (BT)
4	N/A
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	USB port 2
3	WWAN
4	N/A

PCIE Table

PCIE	
Lane	Device
1	NA
2	Card Reader
3	LOM
4	WLAN
5	NA
6	NA

SATA Table

SATA	
Pair	Device
0	HDD
1	NA
2	NA
3	NGFF WWAN

<Core Design>

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Title: Table of Content

Size: A3 | Document Number: Round Rock MLK 13.3" | Rev: A00

Date: Monday, August 17, 2015 | Sheet 100 of 110

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	62	2015/5/12	EE	Vendor suggest increase ECE1117C ESD protection.	Add R6211	X01
2	47	2015/5/12	Power	This request by EMI . Because EMI test result is fail. So we msut add snubber to solve EMI issue .	1. Change PR4703 from 2.2R 0402 to 2.2R 0603 (64.2R205.55L) and stuff 2. Change PC4707 from 1500P to 1000P (78.10224.2FL) and stuff	X01
3	44	2015/5/13	Power	PL4401 after heat & vibration test will be broken. Change to a part with glue	Change PL4401 to 68.2R21C.10Q	X01
4	48/49	2015/5/13	Power	PL4801, PL4901 main source no share	PL4801, PL4901 change to 68.1R010.20I	X01
5	55	2015/5/25	EMC	To solve Broadwell ESD issue	Stuff U5502, U5503, U5504	X01
6	20/25	2015/6/2	EE	Add RTC circuit for factory request	Add RTC detect circuit : Q2502, R2506, R2021, R2022	X01
7	25	2015/7/1	EE	Change RTC circuit for RTC leakage	Mirror Q2502 vertically	X02
8	88	2015/7/1	EE	Fix TPM resume from DS3 will be lost issue	Change U8801 VSB form 3D3V_S5_PCH to 3D3V_S5	X02
9	24	2015/7/1	EE	Change board ID version	Change R2457 to 33K	X02
10	19/24	2015/7/9	EE	Fix alternative parts loop issue	Change both X1901 & X2401 to same 3 sources	X02
11	All	2015/7/17	EE	Change to short pad	R402, R416, R417, R701, R704, R705, R706, R709, R1401, R1407, R1408, R1410 R1415, R1417, R1422, R1423, R1430, R1508, R1607, R1704, R1705, R1706, R1708 R1710, R1711, R1713, R1717, R1718, R1720, R1725, RN1801, RN1802, RN1803 RN1809, R1801, R1802, R1809, R1810, R1811, R1812, R1906, R1909, R2011, R2013 R2014, R2021, R2101, R2102, R2105, R2107, R2108, R2110, R2111, R2115, R2116 R2117, R2401, R2402, R2403, R2424, R2432, R2464, R2461, R2467, R2468, R2471 R2511, R2703, R2705, R2706, R2707, R2709, R2710, R2711, R2714, R2719, R2722 ER2701, ER2702, RN2701, R2738, R2740, R2741, R2742, R2745, R2911, EL2904 EL2903, R2912, R2902, R3006, R3001, R3201, R3206, R3217, R3202, R3204, R3207 R3209, R3210, R3211, R3213, R3212, R3301, R3401, R3402, R3403, R3405, R3407 R3408, R3409, R3412, R3601, R3610, R3603, R3604, R3637, R3654, R3656, R3619 R3611, R3655, R3625, R3657, PR4466, PR4434, PR4467, PR4430, PR4469 PR4501, PR4505, PR4521, PR4615, PR4625, PR4801, PR4903, R5217, R5222, R5221 R5227, R5406, R5407, R5601, R5602, R5603, R5604, R5820, R5830, R5808, R5806 R5828, R5829, R5924, R5927, R5928, R5901, R5906, R5905, R6115, R6103, R6201 R6202, R6203, R6207, R6701, R9620, R9807, R9906, R9903	X02
12	All	2015/7/17	Power	Change to short pad	PR4406, PR4417, PR4430, PR4431, PR4434, PR4438, PR4466, PR4467, PR4469 PR4501, PR4505, PR4521, PR4615, PR4616, PR4617, PR4625, PR4801, PR4902 PR4903	X02
13	55	2015/7/17	EMC	Change for source reason	Change TR5501, TR5502, TR5503, TR5504 form 69.10118.001 to 068.24900.2001	X02
14	42	2015/7/20	Power	Change for source reason	Remove PD4402 2ND 083.10100.008R	X02
15	52	2015/7/21	ME	Change for source reason	Remove LCD1 main 20.F2089.030	X02
16	55	2015/7/21	ME	Change for source reason	Remove DP1 2nd 62.10105.431	X02
17	61	2015/7/21	ME	Change for source reason	Remove PWRBT1 2nd 62.40009.A81	X02

<Core Design>

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Title: Change History-01

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
18	85	2015/7/21	RF	Add Caps for RF solution	EC8532~EC8556	X02
19	45	2015/8/17	EE	Remove parts with halogen	Remove PD4502, PD4503 2nd source 75.00054.C7D	A00
20	25	2015/8/17	EE	Remove parts with halogen	Change Q2501 main source from 83.R0304.B81 to 83.00040.E81	A00
21	44	2015/8/17	EE	Remove parts with halogen	Chagne PD4401 PD4405 PD4406 main source from 83.1R504.B8F to 83.2R004.08F	A00
22	24	2015/8/17	EE	Change EC to MP P/N	Change U2401 to 071.05085.0B03	A00
23	24	2015/8/17	EE	Change board ID version	Change R2457 to 1K	A00
24	96	2015/8/18	EE	Change XDP conn to P/N with solder mask	Change XDP1 to ZZ.00PAD.Q81	A00
25	65	2015/8/18	EE	Change DB conn to P/N with solder mask	Change DB1 to ZZ.00PAD.Y41	A00
26	61	2015/8/19	ME		Remove PWRBT1 2nd 062.40001.0211	A00
27	61	2015/8/19	ME		Remove SWLED1 2nd 83.00191.F70	A00

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