H55M01 Fab1.0

H55MXV-6KS3H GTI

CPU:

Intel Lynnfield/Havendale processors in LGA1156 Package

System Chipset:

PCH(Ibex Peck)

Main Memory:

Dual Channel / DDR-III * 2 (Max 8GB)

On Board Device:

Clock Generator :ICS9LRS4105

LAN1:RealTek 8111DL

HDA Codec:ALC88S/ALC662

BIOS:SPI Flash ROM 8M

Expansion Slots:

PCI EXPRESS 16X SLOT *1
PCI EXPRESS 4X SLOT * 1

PCI SLOT * 2

Version	Function	SKU	BOM
Fab.A			
Fab.B			
Fab.C			

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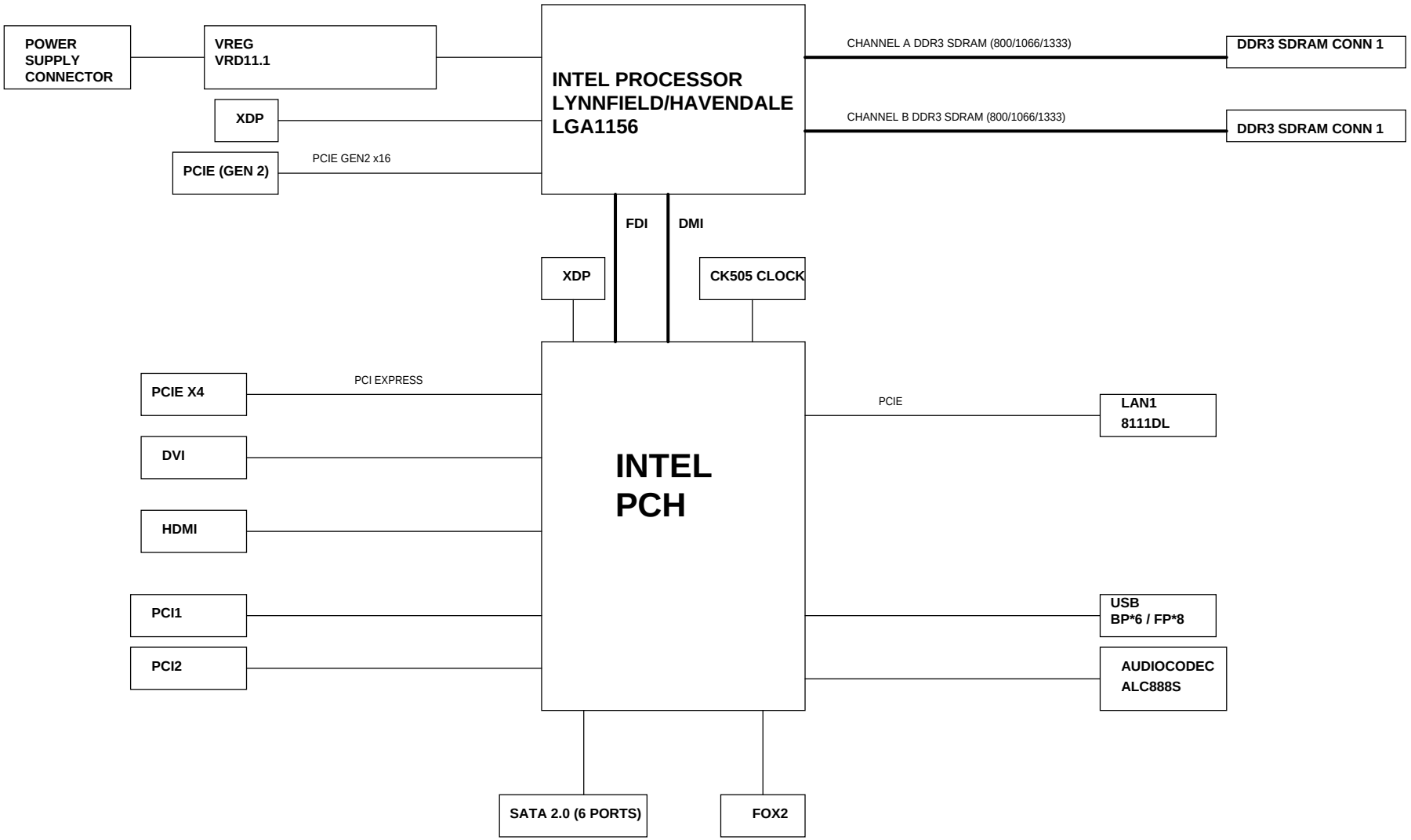
FOXCONN PCEG

Title: Cover Sheet			
Size: A3	Document Number: H55MXV		Rev: A
Date: Tuesday, December 29, 2009	Sheet 1 of 50		

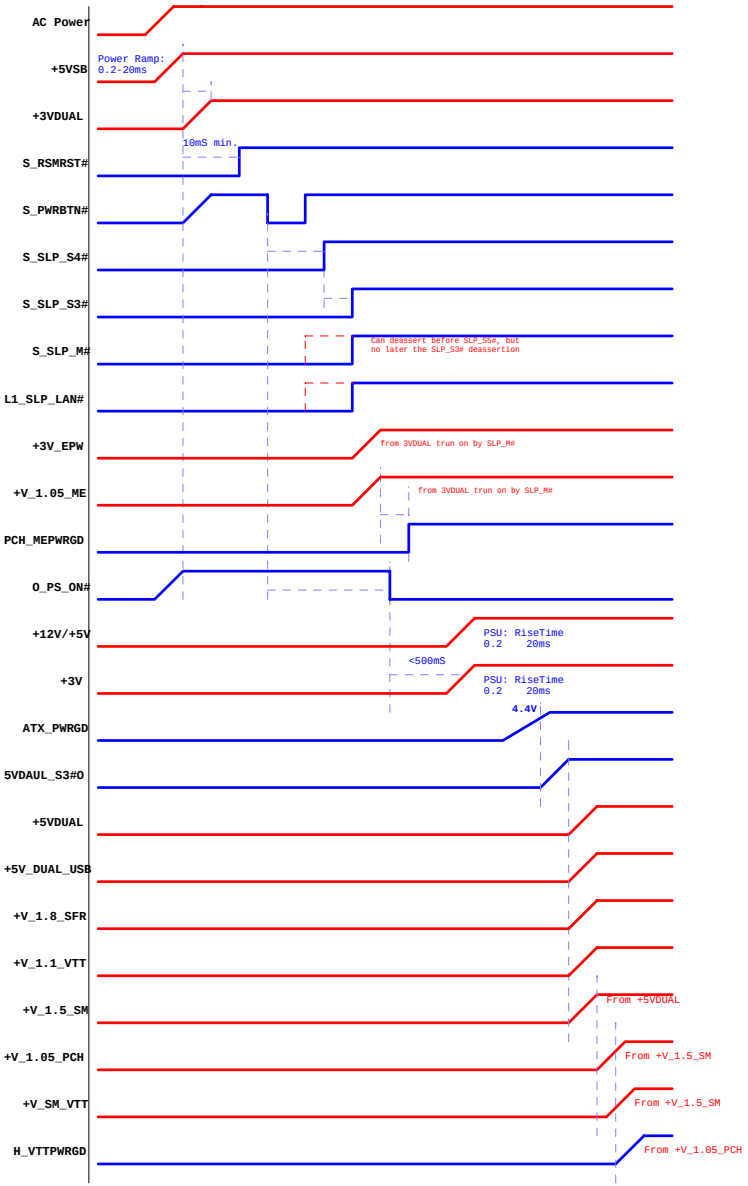
BLOCK DIAGRAM

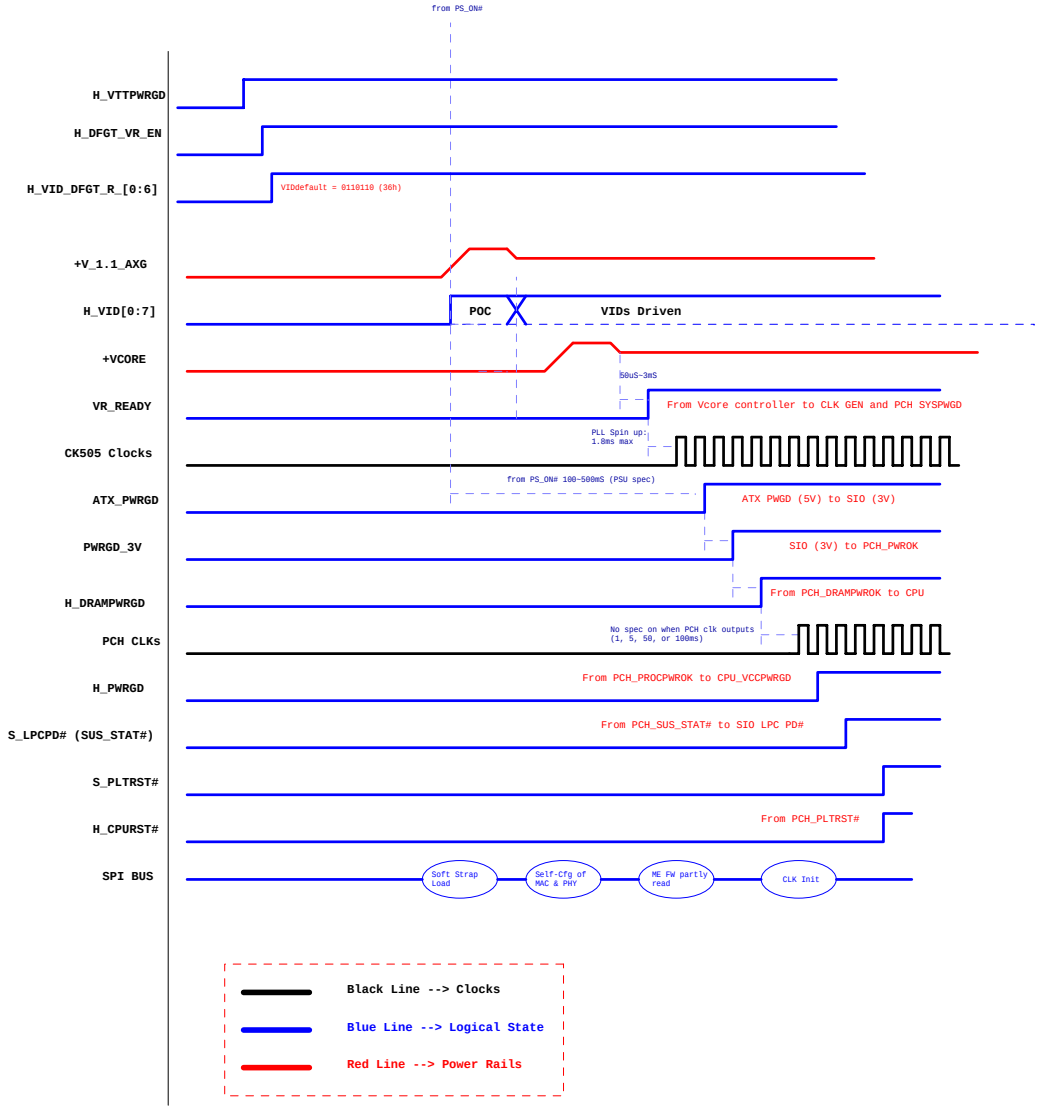


FOXCONN PCEG

Title: Block Diagram		
Size: A3	Document Number: H55MXV	Rev: A
Date: Wednesday, April 21, 2010	Sheet 2 of 50	

POWER ON SEQUENCE

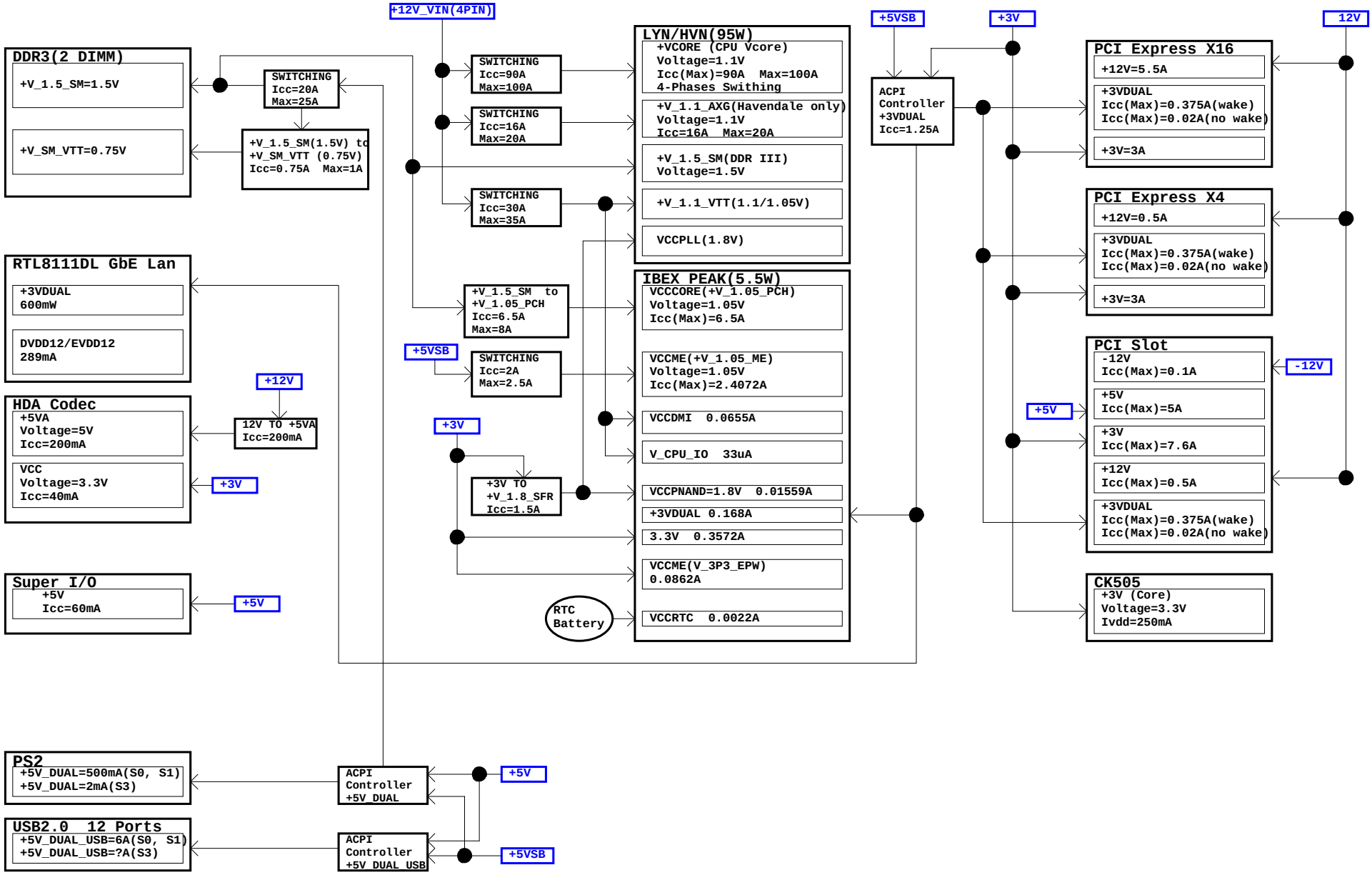




FOXCONN PCEG

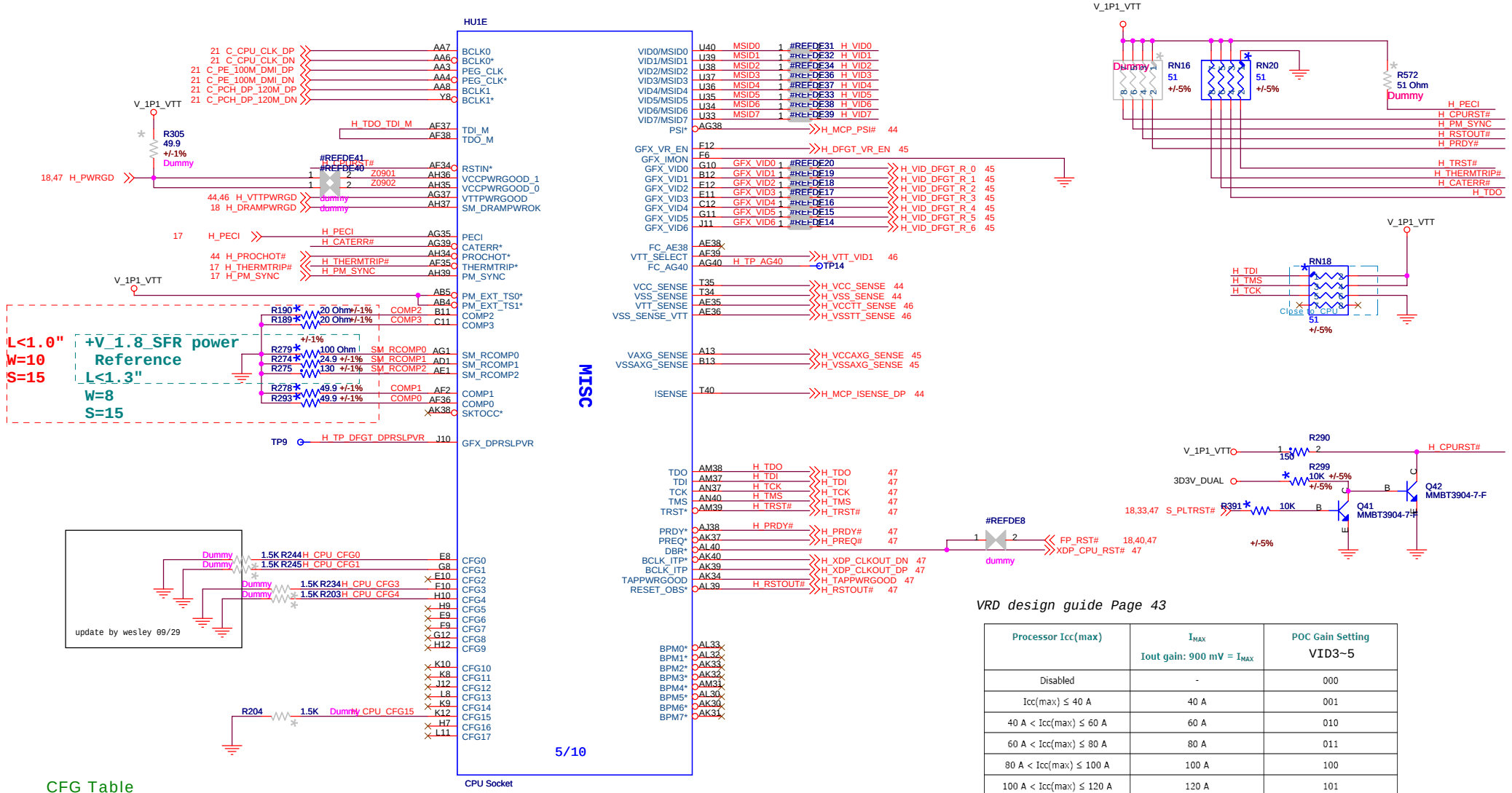
Title: Power On Sequence		
Size: A2	Document Number: H55MXV	Rev: B00
Date: Wednesday, April 21, 2010	Sheet 3 of 50	

POWER DELIVERY MAP



FOXCONN PCEG

Title: Power Delivery Map		
Size: C	Document Number: H55MXV	Rev: B00
Date: Wednesday, April 21, 2010	Sheet 4 of 50	



CFG Table

CFG	H / L	Description
0	PEG Config Table	PEG SEL0
1	PEG Config Table	PEG SEL1
2	PEG Config Table	PEG SEL2
3	Normal / Reverse	Lane Normal
4	Disable / Enable	DP Presence
5		RESERVED
6		RESERVED
7	ENGINEERING EXPERIMENT	
15	ENGINEERING EXPERIMENT	

CFG[0..5] HAVE INTERNAL PULL-UP

PEG Config Table

SEL2	SEL1	SEL0	PCI-E Config
1	1	1	1 x 16
1	1	0	2 x 8

Power On Config

	Function	Default
VID0	MSI0	Low
VID1	MSI1	High
VID2	MSI2	High
VID3	IMON CONFIG0	Low
VID4	IMON CONFIG1	Low
VID5	IMON CONFIG2	High
VID6	RESERVED	Low
VID7	VRD SELECT	Low
PSI#	RESERVED	Low

VRD design guide Page 43

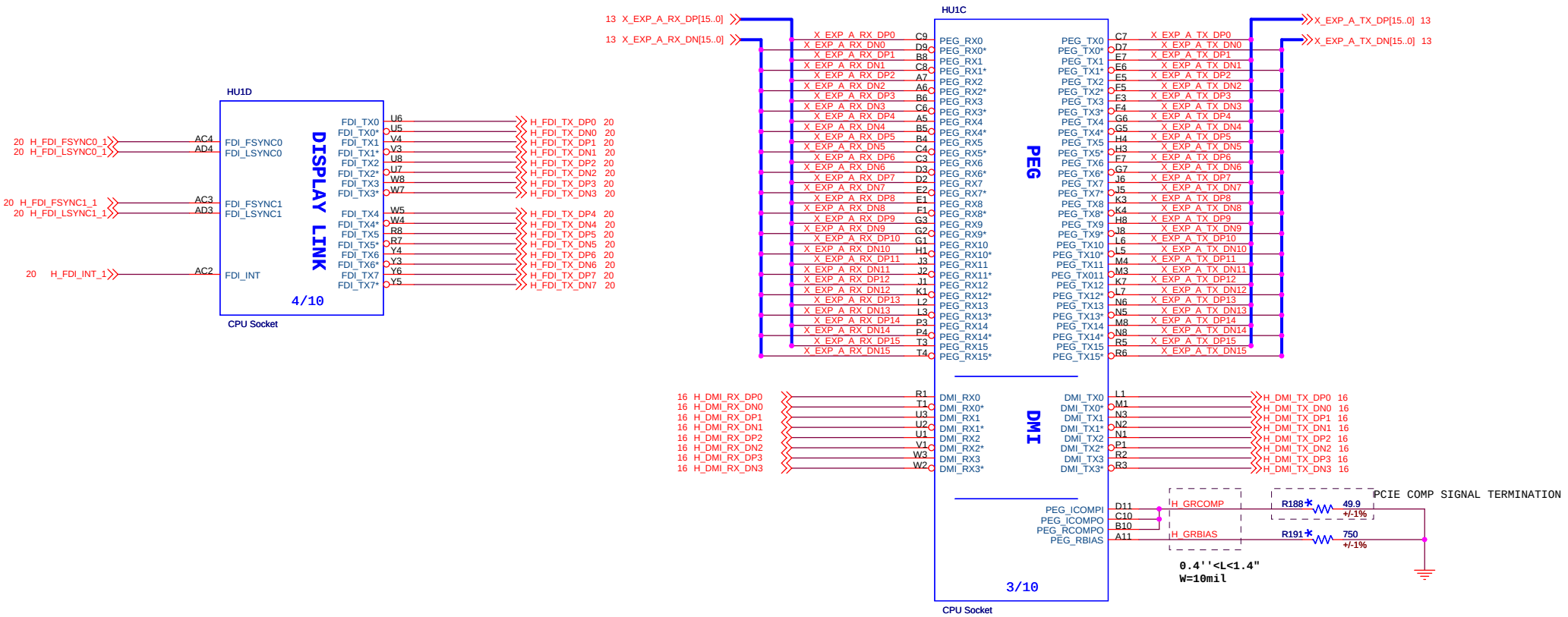
Processor Icc(max)	I_{MAX} Iout gain: 900 mV = I_{MAX}	POC Gain Setting VID3~5
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111

FOXCONN PCEG

Title: CPU-1:MISC

Size: A3 | Document Number: H55MXV | Rev: B00

Date: Wednesday, April 21, 2010 | Sheet 5 of 50

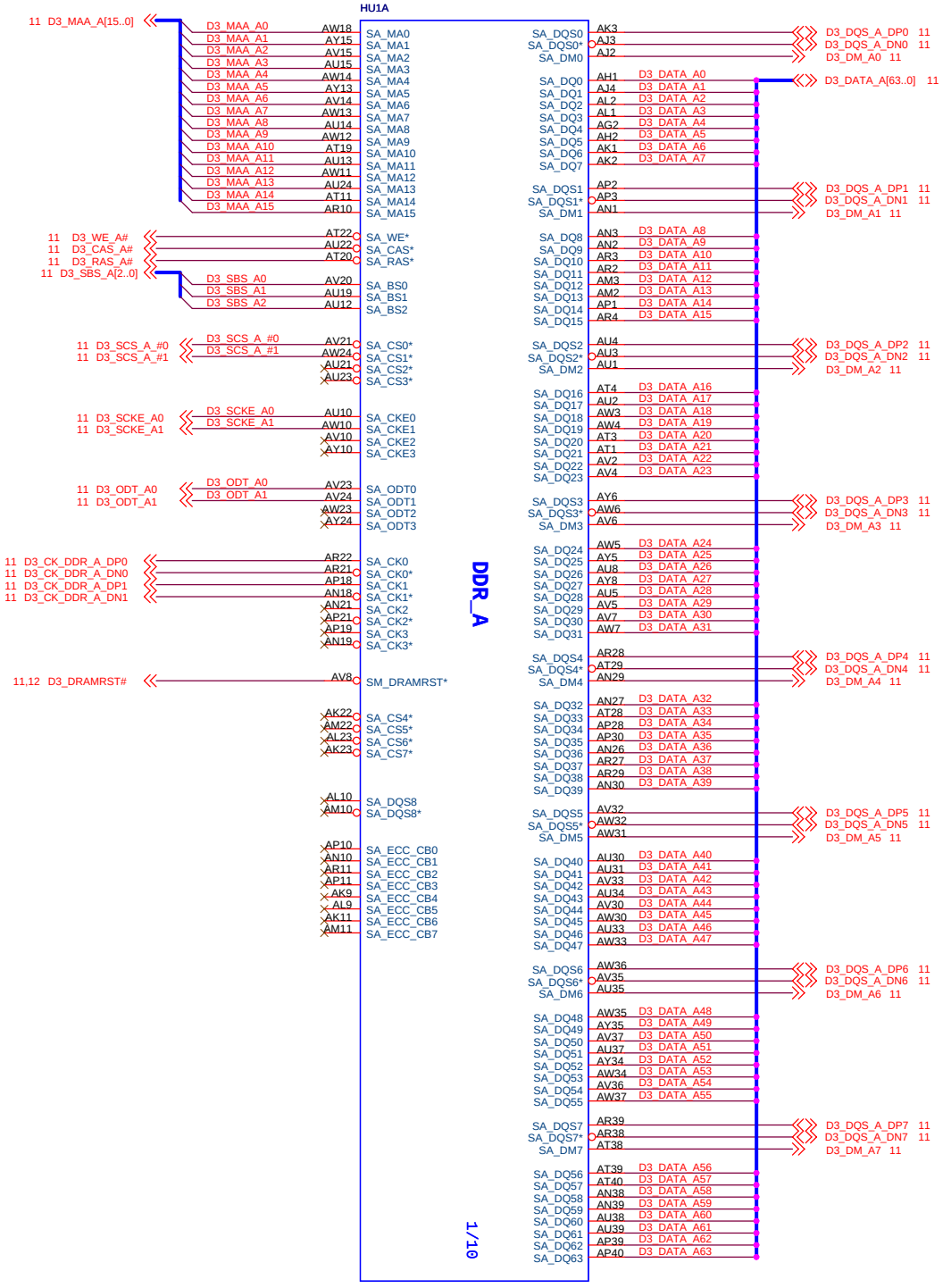


FOXCONN PCEG

Title: CPU-3:FDI/PCIE/DMI

Size	Document Number	Rev
A3	H55MXV	B00

Date: Wednesday, April 21, 2010 Sheet 6 of 50

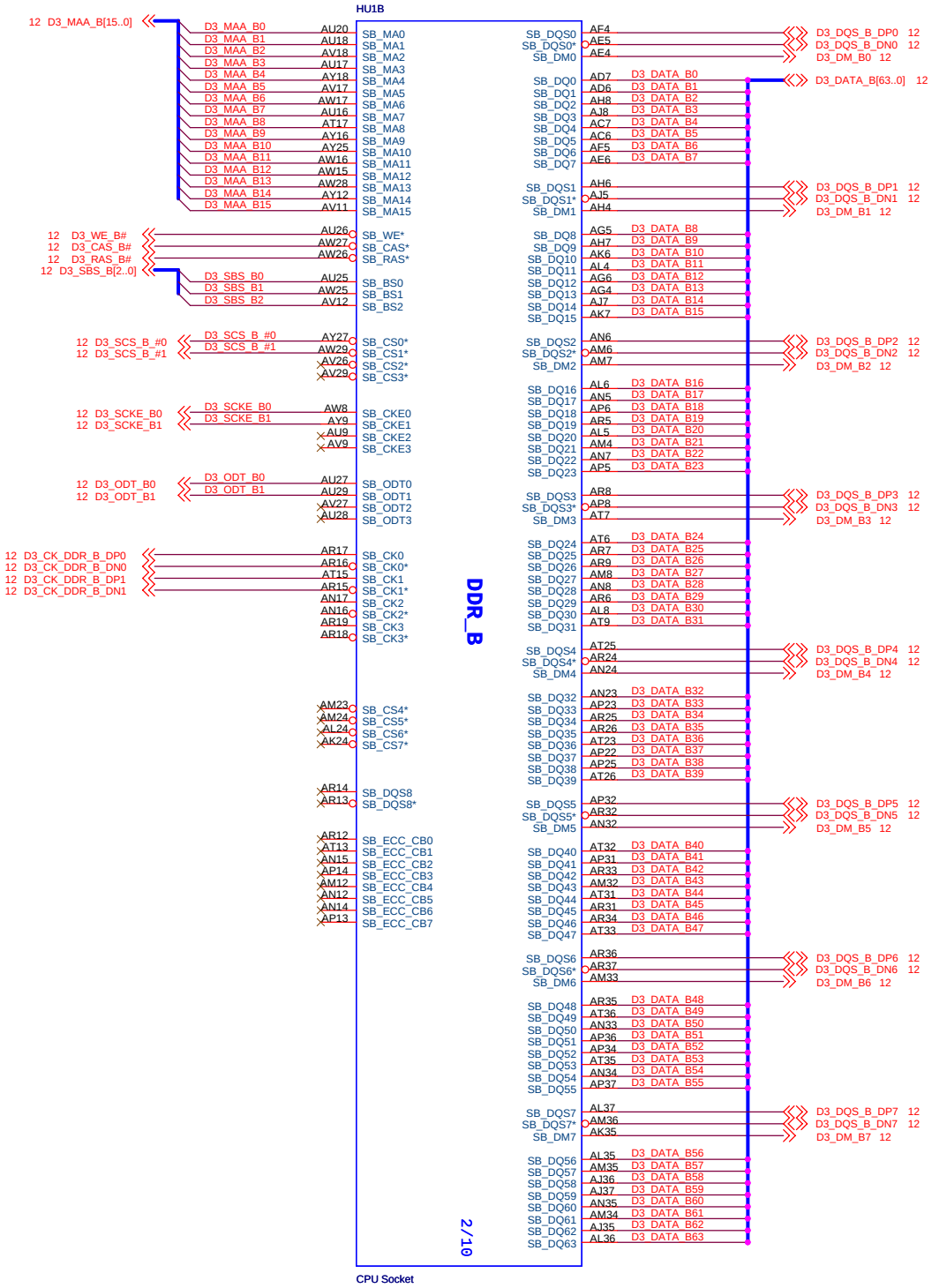


FOXCONN PCEG

Title: CPU-4:DDR3_CHA

Size: A3 | Document Number: H55MXV | Rev: B00

Date: Wednesday, April 21, 2010 | Sheet 7 of 50



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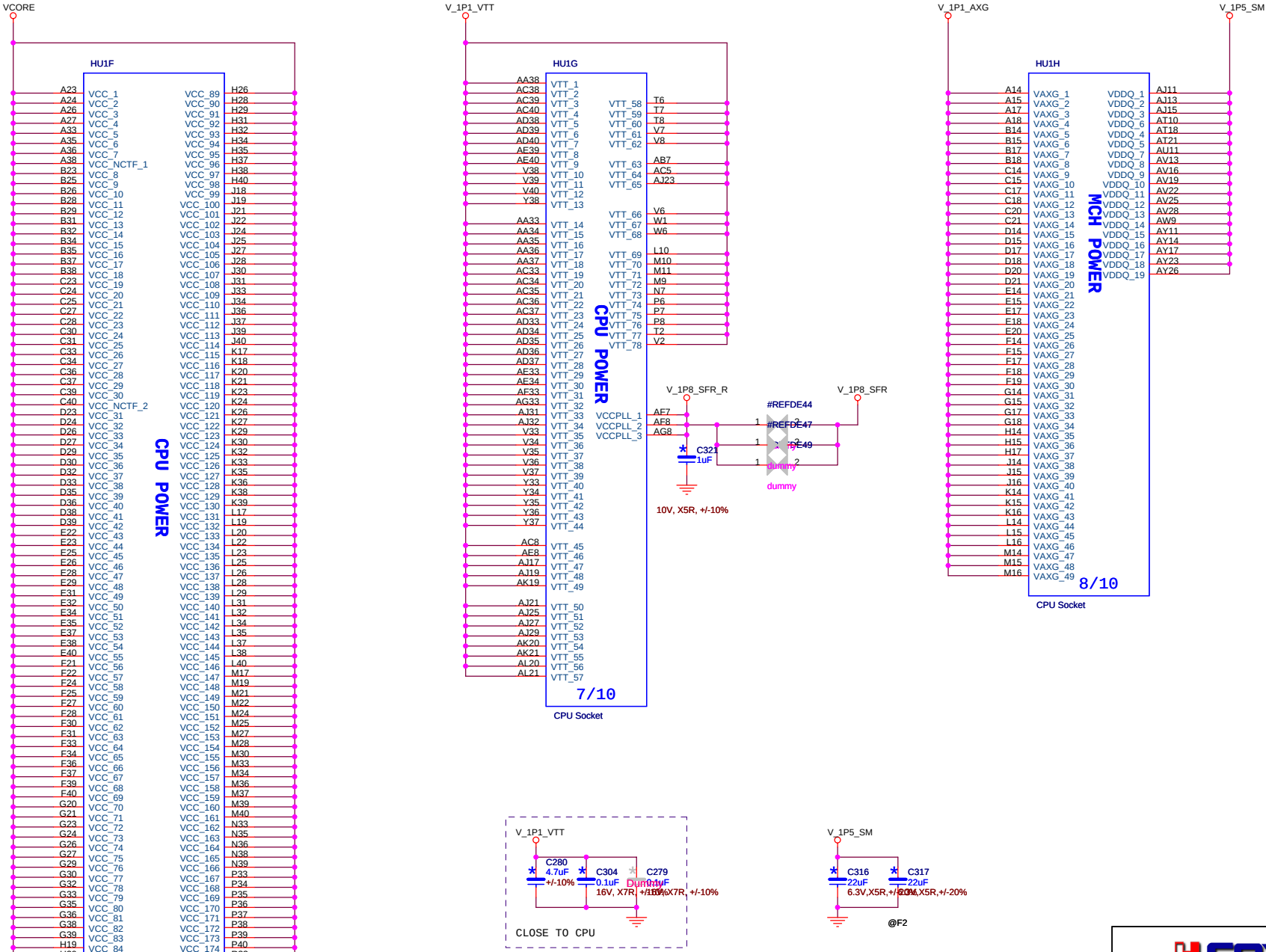
Title: CPU-5:DDR3_CHB

Size: A3 | Document Number: H55MXV | Rev: B00

Date: Wednesday, April 21, 2010 | Sheet 8 of 50



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Title	CPU-6:POWER	
Size A3	Document Number H55MXV	Rev B00
Date: Wednesday, April 21, 2010	Sheet 9 of 50	

HU1I

A16	VSS_1	VSS_282	AP35
A25	VSS_2	VSS_92	AP38
A28	VSS_3	VSS_283	AP4
A34	VSS_4	VSS_94	AP7
A37	VSS_5	VSS_95	AP9
AA5	VSS_6	VSS_96	AR1
AB3	VSS_7	VSS_97	AR20
AB33	VSS_8	VSS_98	AR23
AB34	VSS_9	VSS_284	AR30
AB35	VSS_10	VSS_99	AR40
AB36	VSS_11	VSS_100	AT12
AB37	VSS_12	VSS_101	AT14
AB38	VSS_13	VSS_102	AT16
AB39	VSS_14	VSS_103	AT2
AB40	VSS_15	VSS_104	AT24
AB6	VSS_16	VSS_105	AT27
AB8	VSS_17	VSS_106	AT30
AC1	VSS_18	VSS_285	AT34
AD5	VSS_19	VSS_286	AT37
AD8	VSS_20	VSS_110	AT5
AE3	VSS_21	VSS_287	AT8
AE37	VSS_22	VSS_111	AU32
AE7	VSS_23	VSS_288	AU36
AF1	VSS_24	VSS_289	AU6
AF40	VSS_25	VSS_290	AU7
AF6	VSS_26	VSS_113	AV3
AG34	VSS_27	VSS_114	AV31
AG36	VSS_28	VSS_115	AV34
AG7	VSS_30	VSS_291	AV38
AH3	VSS_31	VSS_118	AY33
AH33	VSS_32	VSS_119	AY36
AH38	VSS_33	VSS_120	AY4
AH5	VSS_276	VSS_121	AY7
AJ1	VSS_34	VSS_122	B16
AJ12	VSS_35	VSS_123	B24
AJ14	VSS_36	VSS_124	B27
AJ16	VSS_37	VSS_125	B30
AJ18	VSS_38	VSS_126	B33
AJ20	VSS_39	VSS_127	B36
AJ22	VSS_40	VSS_128	B7
AJ24	VSS_41	VSS_129	B9
AJ26	VSS_42	VSS_130	C13
AJ28	VSS_43	VSS_131	C16
AJ30	VSS_44	VSS_132	C19
AJ33	VSS_45	VSS_133	C22
AJ34	VSS_46	VSS_134	C26
AJ40	VSS_47	VSS_135	C29
AJ6	VSS_48	VSS_136	C32
AJ9	VSS_49	VSS_137	C35
AK10	VSS_50	VSS_138	C38
AK17	VSS_51	VSS_139	C5
AK36	VSS_52	VSS_140	D10
AK4	VSS_277	VSS_141	D12
AK5	VSS_53	VSS_142	D13
AK8	VSS_54	VSS_143	D16
AL11	VSS_55	VSS_144	D19
AL13	VSS_56	VSS_145	D22
AL16	VSS_57	VSS_146	D25
AL19	VSS_58	VSS_147	D28
AL22	VSS_59	VSS_148	D31
AL25	VSS_60	VSS_149	D34
AL28	VSS_61	VSS_150	D37
AL3	VSS_62	VSS_151	D4
AL31	VSS_63	VSS_152	D40
AL34	VSS_64	VSS_153	D5
AL38	VSS_65	VSS_154	D6
AL7	VSS_66	VSS_155	D8
AM1	VSS_67	VSS_156	E13
AM40	VSS_68	VSS_157	E16
AM5	VSS_278	VSS_158	E19
AM9	VSS_279	VSS_159	E21
AN13	VSS_70	VSS_160	E24
AN20	VSS_71	VSS_161	E27
AN22	VSS_72	VSS_162	E3
AN25	VSS_73	VSS_163	E30
AN28	VSS_74	VSS_164	E33
AN31	VSS_75	VSS_165	E36
AN36	VSS_77	VSS_166	E39
AN4	VSS_280	VSS_167	E4
AN9	VSS_281	VSS_168	F11
AP12	VSS_80	VSS_169	F13
AP15	VSS_81	VSS_170	F16
AP16	VSS_82	VSS_171	F2
AP17	VSS_83	VSS_172	F20
AP20	VSS_84	VSS_173	F23
AP24	VSS_85	VSS_174	F26
AP26	VSS_86	VSS_175	F29
AP27	VSS_87	VSS_176	F32
AP29	VSS_88	VSS_177	F35
AP33	VSS_91	VSS_178	F38

GND

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CPU Socket

HU1J

F8	VSS_179	VSS_269	W33	
G13	VSS_180	VSS_270	W34	
G16	VSS_181	VSS_271	W35	
G19	VSS_182	VSS_272	W36	
G22	VSS_183	VSS_273	W37	
G25	VSS_184	VSS_274	W38	
G28	VSS_185	VSS_275	Y7	
G31	VSS_186	CGC_TP_NCTF	B39	H_TP_CGC → TP6
G34	VSS_187			
G37	VSS_188	SA_DIMM_VREFDQ	AF3	D3_DQ_VREF_A 11
G4	VSS_189	SB_DIMM_VREFDQ	AG3	D3_DQ_VREF_B 12
G40	VSS_190			
G9	VSS_191	RSVD_1	A12	HTP2 → TP3
H11	VSS_192	RSVD_4	AD2	HTP9 → TP11
H13	VSS_193	RSVD_5	AE2	HTP10 → TP12
H16	VSS_194	RSVD_9	AH40	HTP11 → TP13
H18	VSS_195	RSVD_10	AJ39	HTP13 → TP15
H2	VSS_196			
H21	VSS_197			
H24	VSS_198			
H27	VSS_199			
H30	VSS_200			
H33	VSS_201			
H36	VSS_202			
H39	VSS_203	RSVD_13	AM14	
H5	VSS_204	RSVD_14	AM13	
H6	VSS_205	RSVD_15	AK15	
J13	VSS_206	RSVD_16	AK16	
J17	VSS_207			
J20	VSS_208	RSVD_17	AM25	
J23	VSS_209	RSVD_18	AL29	
J26	VSS_210	RSVD_19	AM30	
J29	VSS_211	RSVD_20	AK29	
J32	VSS_212	RSVD_21	AK28	
J35	VSS_213	RSVD_22	AM29	
J38	VSS_214	RSVD_23	AM28	
J4	VSS_215	RSVD_24	AL27	
J7	VSS_216	RSVD_25	AK27	
J9	VSS_217	RSVD_26	AM26	
K11	VSS_218	RSVD_27	AM27	
K13	VSS_219	RSVD_28	AL26	
K19	VSS_220	RSVD_29	AK26	
K2	VSS_221			
K22	VSS_222			
K25	VSS_223	RSVD_30	AK25	
K28	VSS_224	RSVD_TP	AN11	
K31	VSS_225			
K34	VSS_226	RSVD_32	L12	HTP7 → TP8
K37	VSS_227	RSVD_33	M12	HTP8 → TP10
K40	VSS_228			
K5	VSS_229	RSVD_34	AM21	
K6	VSS_230	RSVD_35	AM20	
L13	VSS_231	RSVD_36	AM19	
L18	VSS_232	RSVD_37	AM18	
L21	VSS_233	VSS_292	T39	H_INSENSE_DN → #REFDE35 1 2 dummy
L24	VSS_234			
L27	VSS_235	RSVD_39	AL18	
L30	VSS_236	RSVD_40	AK18	
L33	VSS_237			
L36	VSS_238	RSVD_41	AM15	
L39	VSS_239	RSVD_42	AM16	
L4	VSS_240	RSVD_43	AL15	
L9	VSS_241	RSVD_44	AL14	
M13	VSS_242			
M18	VSS_243	RSVD_45	AL17	
M2	VSS_244	RSVD_46	AM17	
M20	VSS_245	RSVD_47	AK14	
M23	VSS_246	RSVD_48	AK13	
M26	VSS_247	RSVD_49	AL12	HTP12 → TP16
M29	VSS_248	RSVD_50	AK12	
M32	VSS_249			
M35	VSS_250			
M38	VSS_251			
M5	VSS_252	RSVD_NCTF_1	AY3	
M6	VSS_253			
M7	VSS_254			
N34	VSS_255	RSVD_NCTF_2	C2	HTP5 → TP5
N37	VSS_256	RSVD_NCTF_3	D1	HTP6 → TP7
N4	VSS_257	RSVD_NCTF_4	AY37	HTP16 → TP19
N40	VSS_258	RSVD_NCTF_5	AW38	HTP17 → TP20
P2	VSS_259	RSVD_NCTF_6	AV1	
P5	VSS_260	RSVD_NCTF_7	AW2	
R4	VSS_261	RSVD_NCTF_8	AV39	HTP14 → TP17
T33	VSS_262	RSVD_NCTF_9	AU40	HTP15 → TP18
T36	VSS_263			
T37	VSS_264			
T38	VSS_265			
T5	VSS_266	RSVD_NCTF_10	A4	HTP1 → TP2
U4	VSS_267	RSVD_NCTF_11	B3	HTP3 → TP4
V5	VSS_268			

GND

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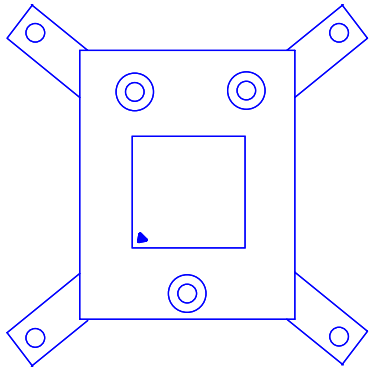
CPU Socket

update by wesley 0715



HU1_1

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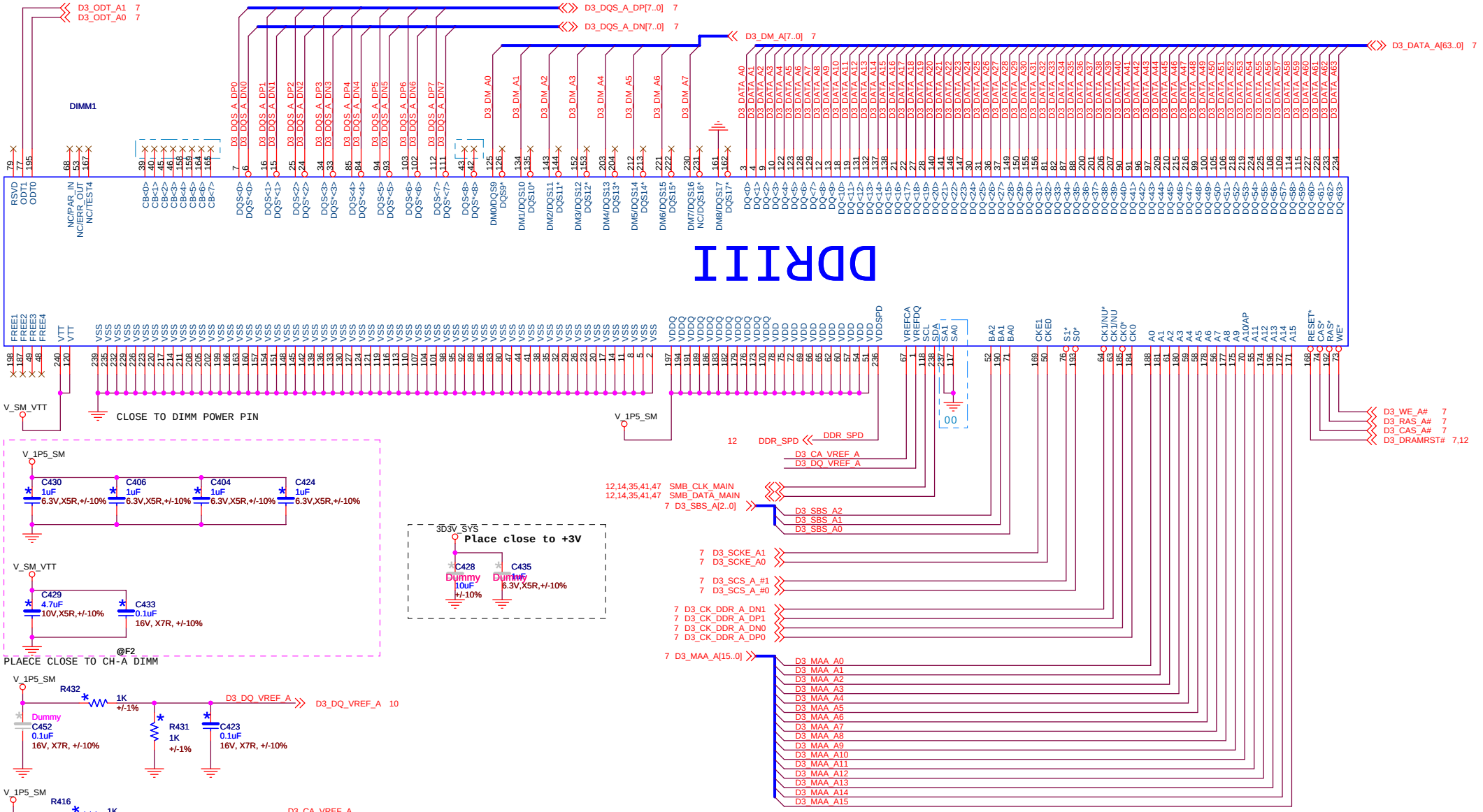
Title	CPU-7:GND		
Size A3	Document Number H55MXV		Rev B00
Date: Wednesday, April 21, 2010	Sheet 10 of 50		

CHANNEL A BANK 1
SMB ADDRESS:00



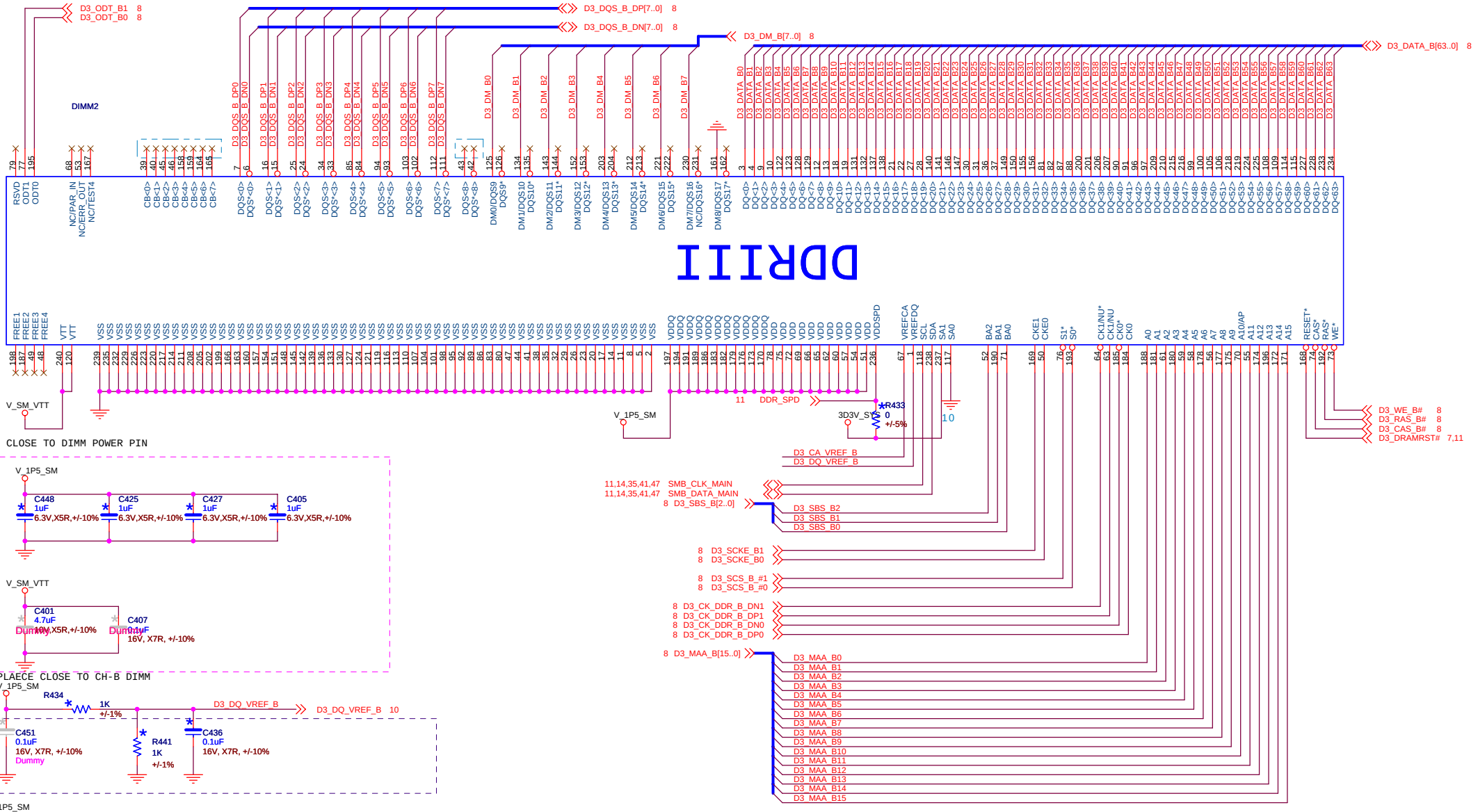
FOXCONN PCEG

Title: DDR3 CONN:CHA_1

Size	Document Number	Rev
A3	H55MXV	B00

Date: Wednesday, April 21, 2010 Sheet 11 of 50

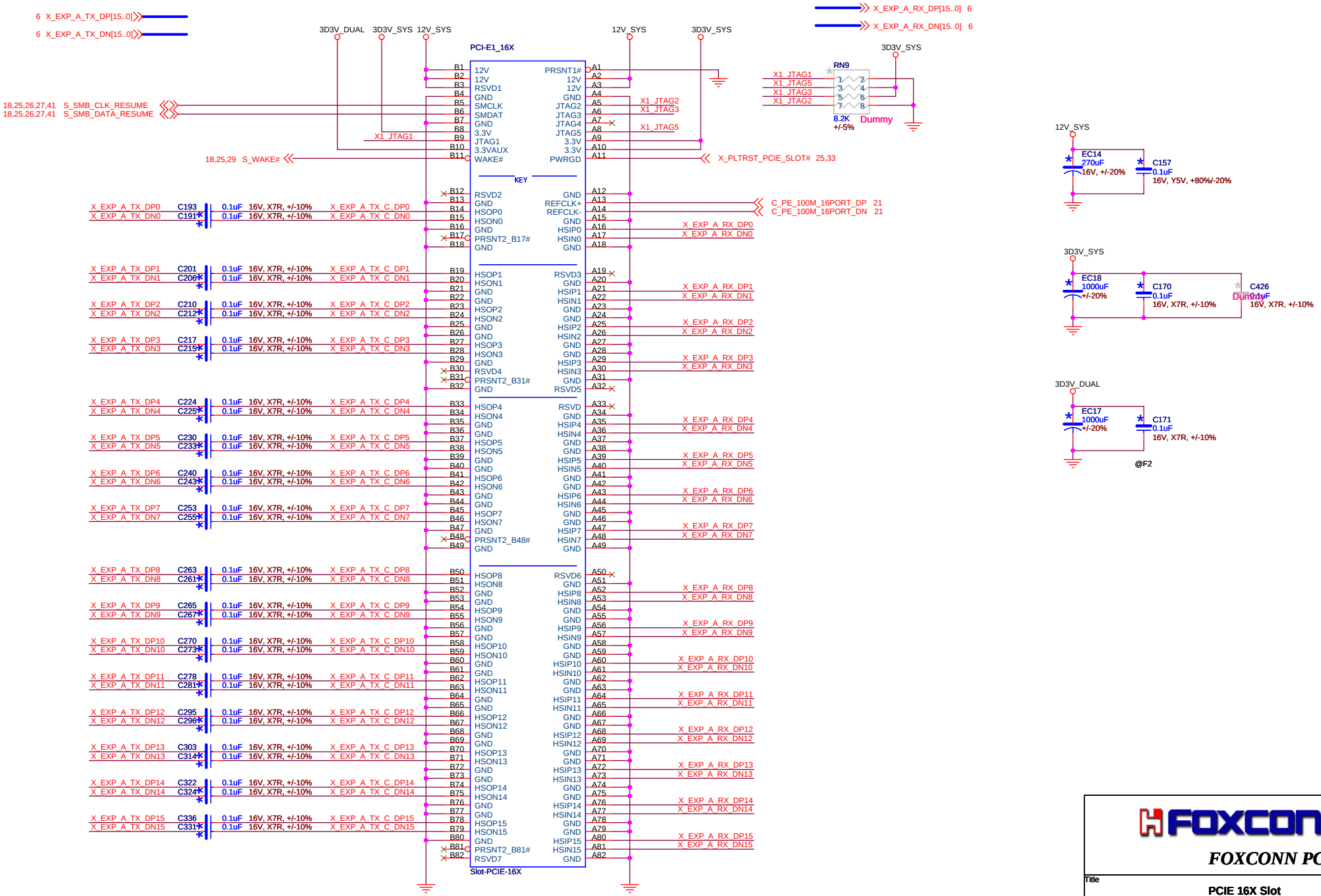
CHANNEL B BANK 1
SMB ADDRESS:010



FOXCONN PCEG

Title	DDR3 CONN:CHB_1	
Size A3	Document Number H55MXV	Rev B00
Date: Wednesday, April 21, 2010	Sheet 12 of 50	

PCIEX16

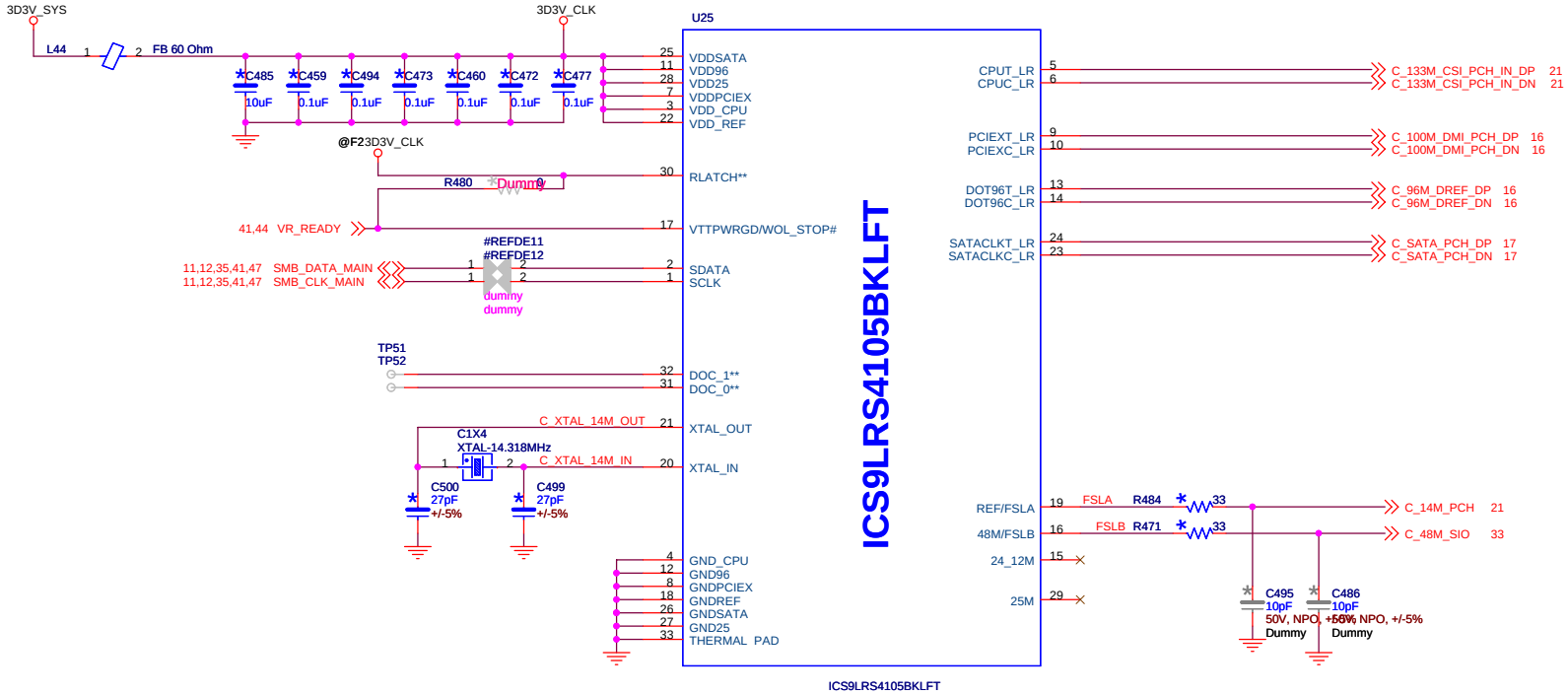


FOXCONN PCEG

Title: PCIE 16X Slot

Size	Document Number	Rev
A3	H55MXV	B00

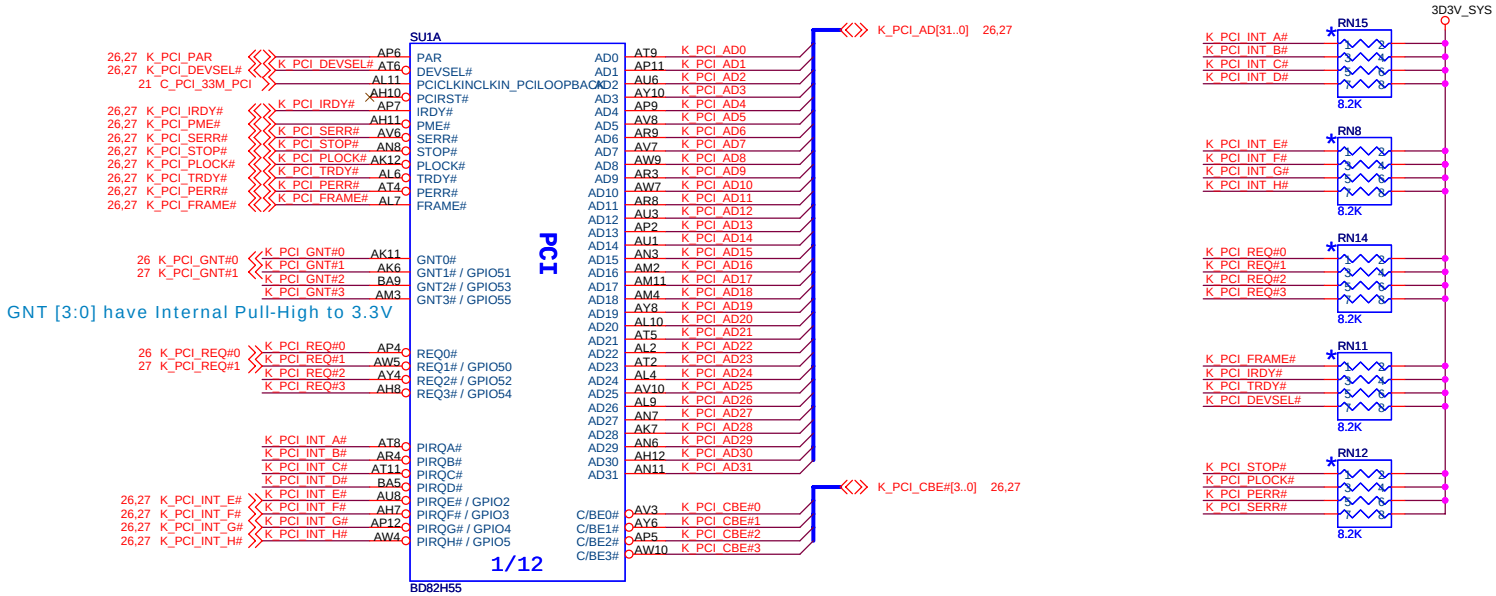
Date: Wednesday, April 21, 2010 Sheet 13 of 50



ICS9LRS4105BKLFT

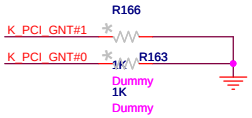
FOXCONN PCEG

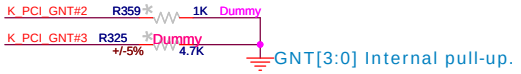
Title	CLOCK GEN	
Size A3	Document Number H55MXV	Rev B00
Date: Wednesday, April 21, 2010	Sheet 14 of 50	



Boot BIOS Select

Boot Device	GNT1	GNT0
LPC	0	0
PCI	1	0
Reserved	0	1
SPI *	1	1





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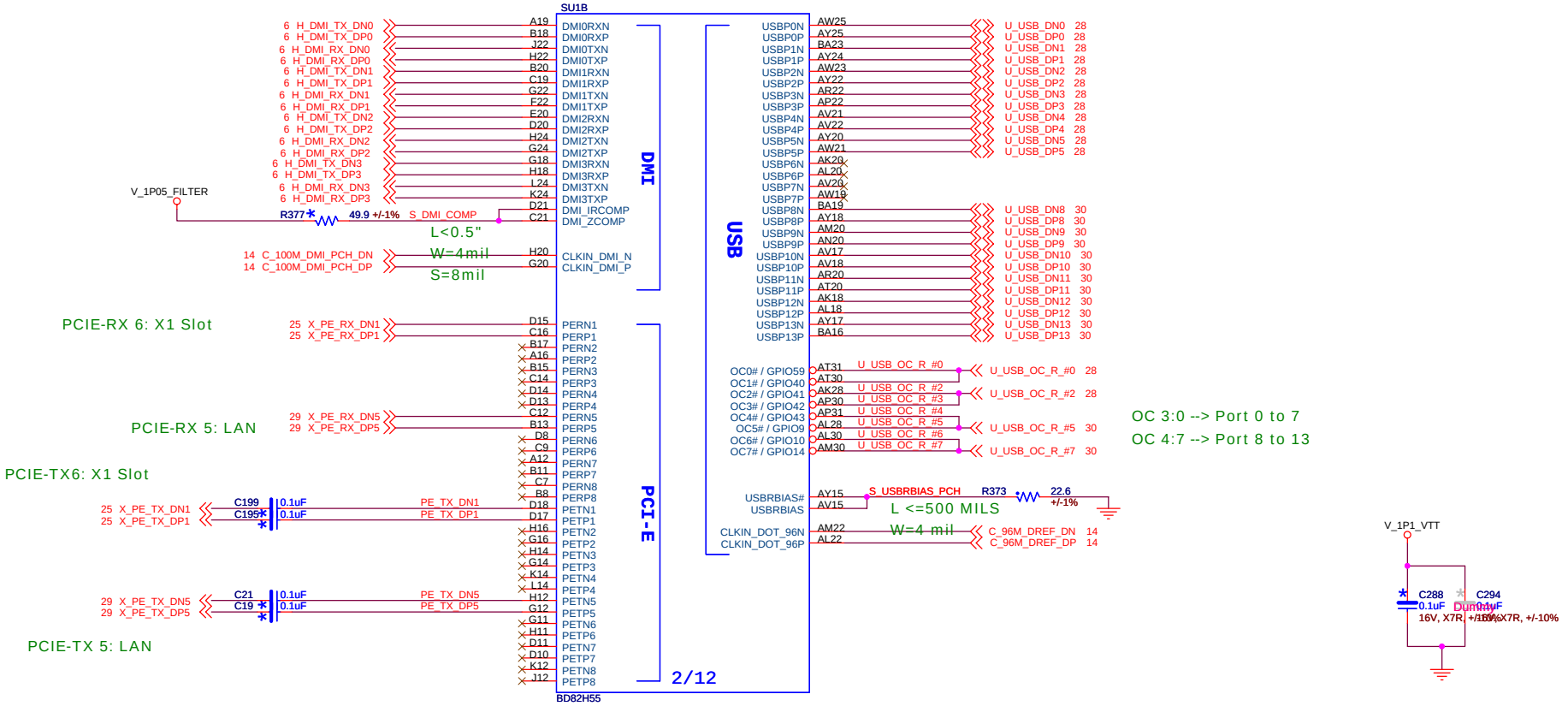
Title: PCH-1:PCI		
Size: A3	Document Number: H55MXV	Rev: B00
Date: Wednesday, April 21, 2010	Sheet 15 of 50	



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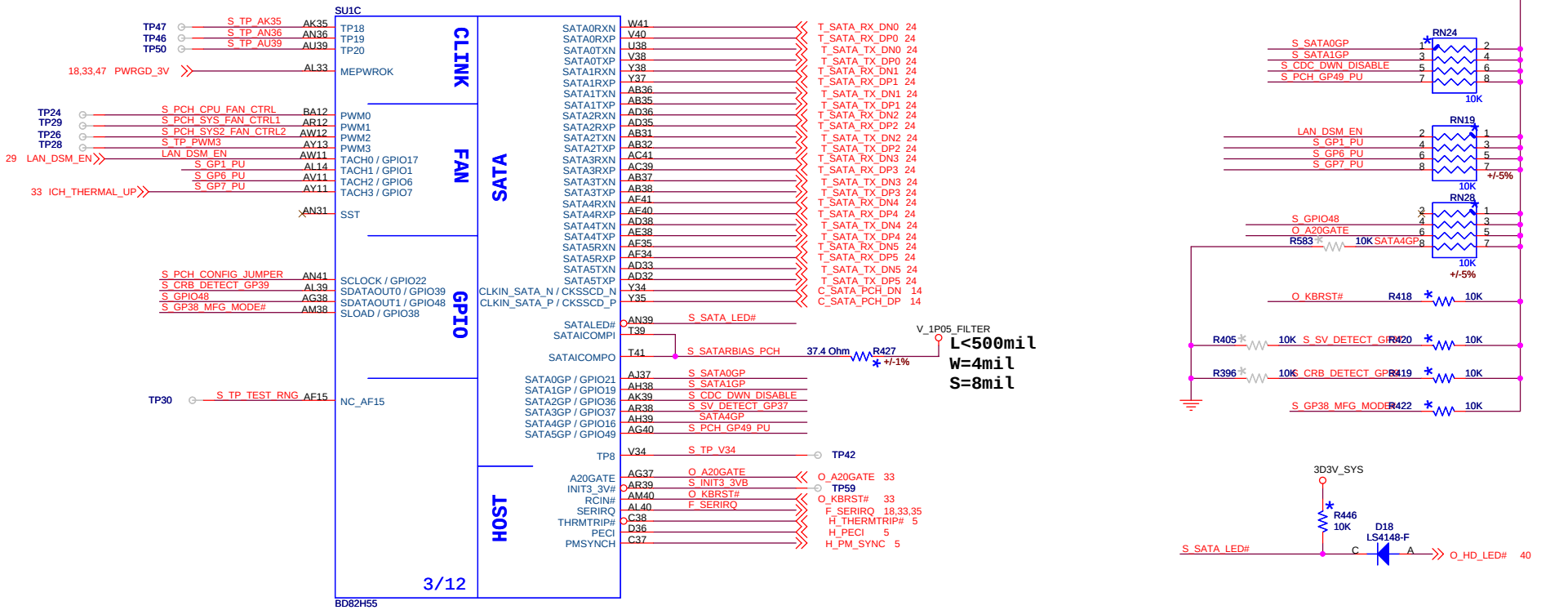
Title: PCH-2:DMI/PCIE/USB

Size: A3 | Document Number: H55MXV | Rev: B00

Date: Wednesday, April 21, 2010 | Sheet 16 of 50



BOARD ID TABLE		
GP37	GP39	BOARD STYLE
1	1	6K
1	0	8K

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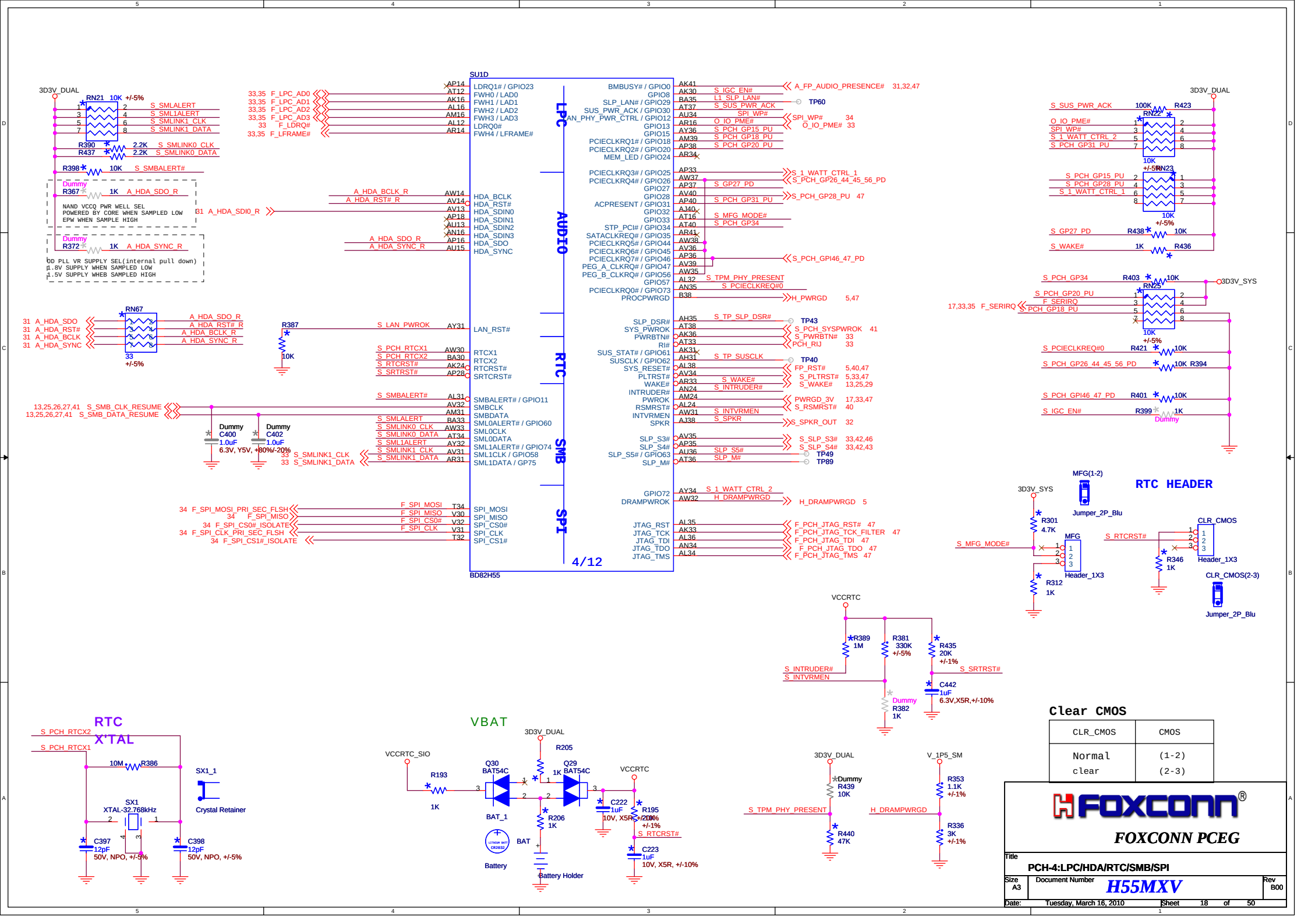
Title: PCH-3:SATA/HOST/FAN		
Size: A3	Document Number: H55MXV	Rev: B00
Date: Thursday, December 24, 2009	Sheet 17 of 50	


SU1D
LPC
AUDIO
RTC
SMB
SPI
4/12
BD82H55
LDRQ1# / GPIO23
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
LDRQ0#
FWH4 / LFRAME#
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC
LAN_RST#
RTCX1
RTCX2
RTCRST#
SRTCRST#
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SMLOALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GP75
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1#
3D3V_DUAL
RN21 10K +/-5%
S_SMLALERT
S_SML1ALERT
S_SMLINK1_CLK
S_SMLINK1_DATA
R390 2.2K S_SMLINK0_CLK
R437 2.2K S_SMLINK0_DATA
R398 10K S_SMBALERT#
Dummy
R367 1K A_HDA_SDO_R
NAND VCCQ PWR WELL SEL
POWERED BY CORE WHEN SAMPLED LOW
EPW WHEN SAMPLE HIGH
Dummy
R372 1K A_HDA_SYNC_R
DD PLL VR SUPPLY SEL(internal pull down)
.8V SUPPLY WHEN SAMPLED LOW
1.5V SUPPLY WHEB SAMPLED HIGH
RN67
33 +/-5%
R387 10K
Dummy C400 1.0uF 6.3V, Y5V, +80%/-20%
Dummy C402 1.0uF
RTC HEADER
MFG(1-2)
Jumper_2P_Blu
R301 4.7K
MFG
Header_1X3
R312 1K
CLR_CMOS
R346 1K
CLR_CMOS(2-3)
Jumper_2P_Blu
RTC X'TAL
SX1
XTAL-32.768kHz
SX1_1
Crystal Retainer
10M R386
C397 12pF 50V, NPO, +/-5%
C398 12pF 50V, NPO, +/-5%
VBAT
Q30 BAT54C
Q29 BAT54C
R205 1K
R206 1K
R193 1K
BAT_1
BAT
Battery
Battery Holder
C222 1uF 10V, X5R, +/-10%
R195 +/-1%
C223 1uF 10V, X5R, +/-10%
VCCRTC
R389 1M
R381 330K +/-5%
R435 20K +/-1%
C442 1uF 6.3V,X5R,+/-10%
Dummy R382 1K
V_1P5_SM
Dummy R439 10K
R440 47K
R353 1.1K +/-1%
R336 3K +/-1%
Clear CMOS
CLR_CMOS | CMOS
Normal | (1-2)
clear | (2-3)
FOXCONN PCEG
Title
PCH-4:LPC/HDA/RTC/SMB/SPI
Size A3
Document Number H55MXV
Rev B00
Date: Tuesday, March 16, 2010
Sheet 18 of 50

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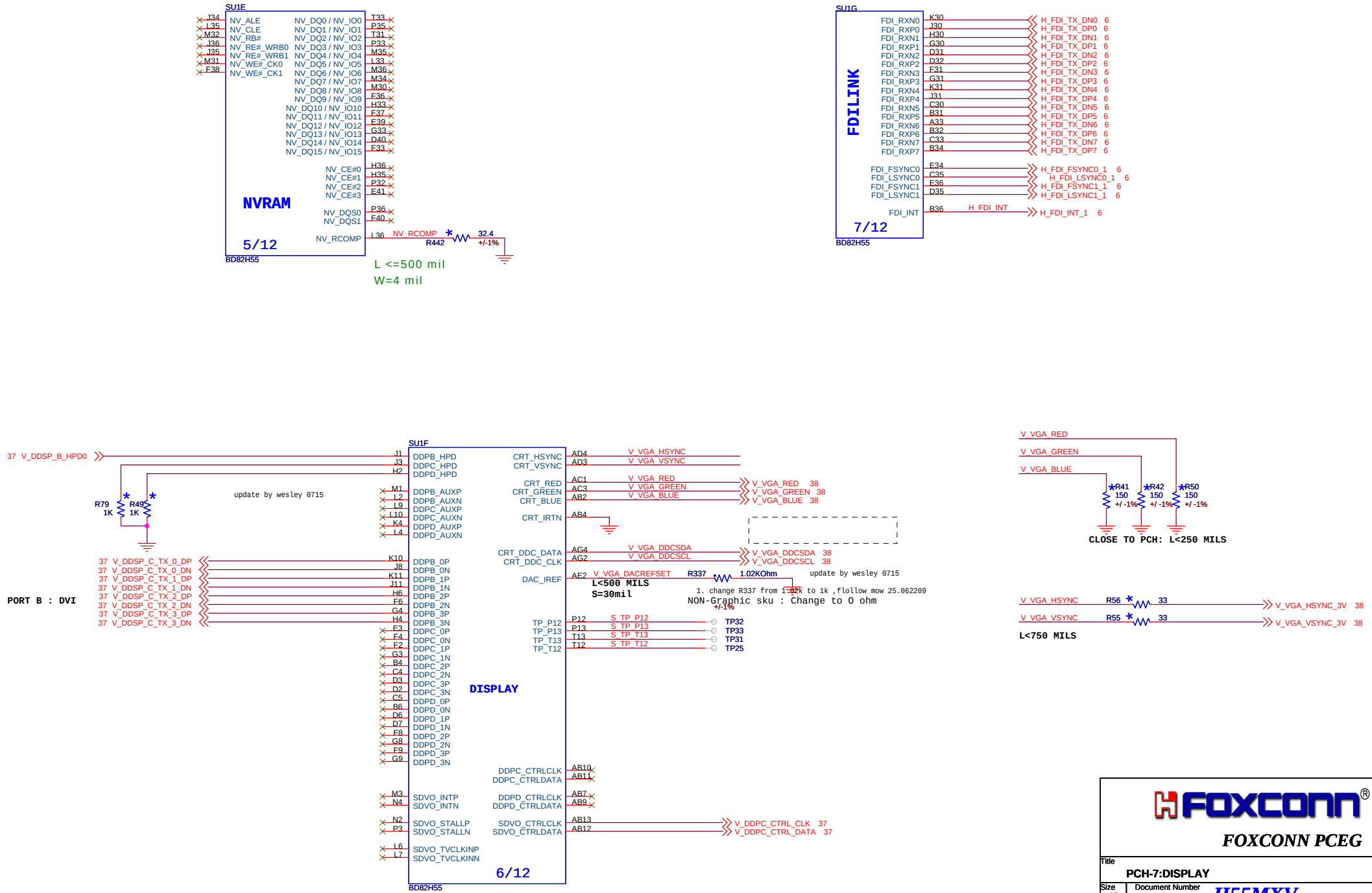
Title: PCH-5:NVRAM/ONFI Conn

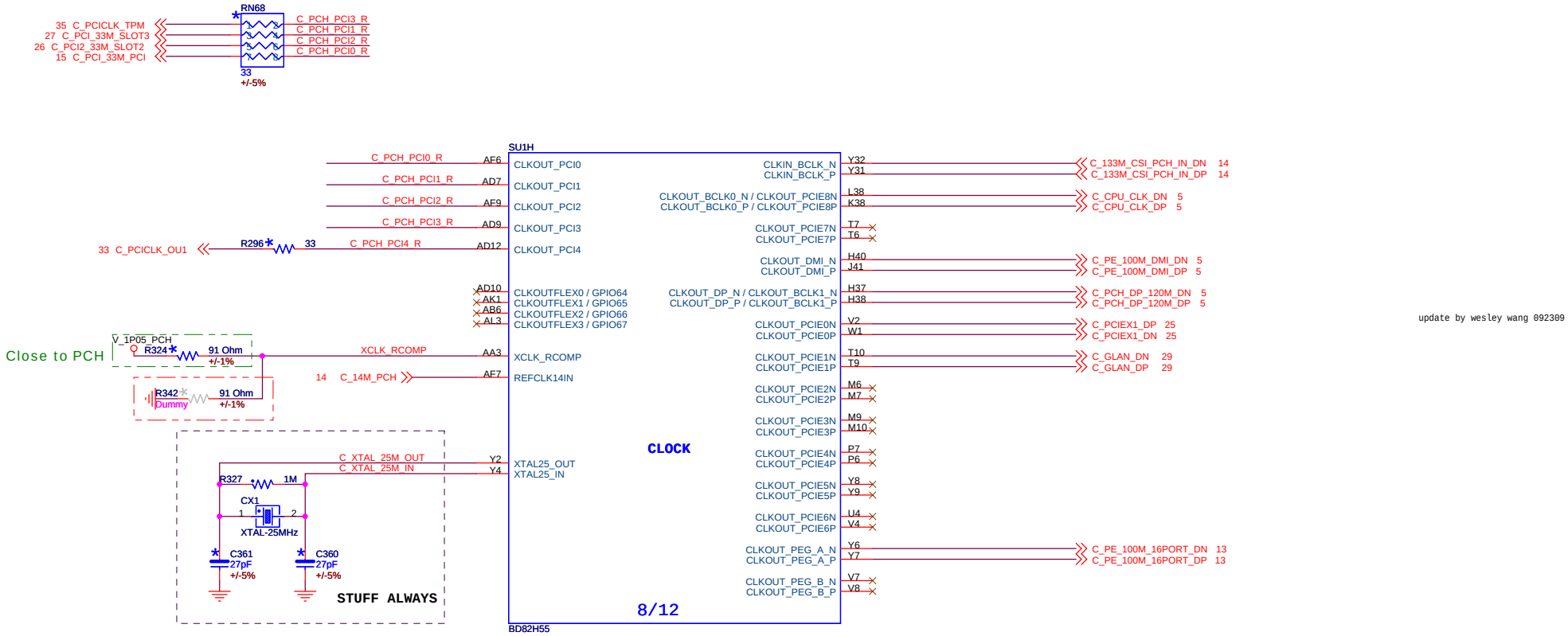
Size: A3 | Document Number: H55MXV | Rev: B00

Date: Wednesday, April 21, 2010 | Sheet 19 of 50



FOXCONN PCEG

Title	PCH-7:DISPLAY	
Size A3	Document Number H55MXV	Rev B00
Date: Wednesday, April 21, 2010	Sheet 20 of 50	



update by wesley wang 092309

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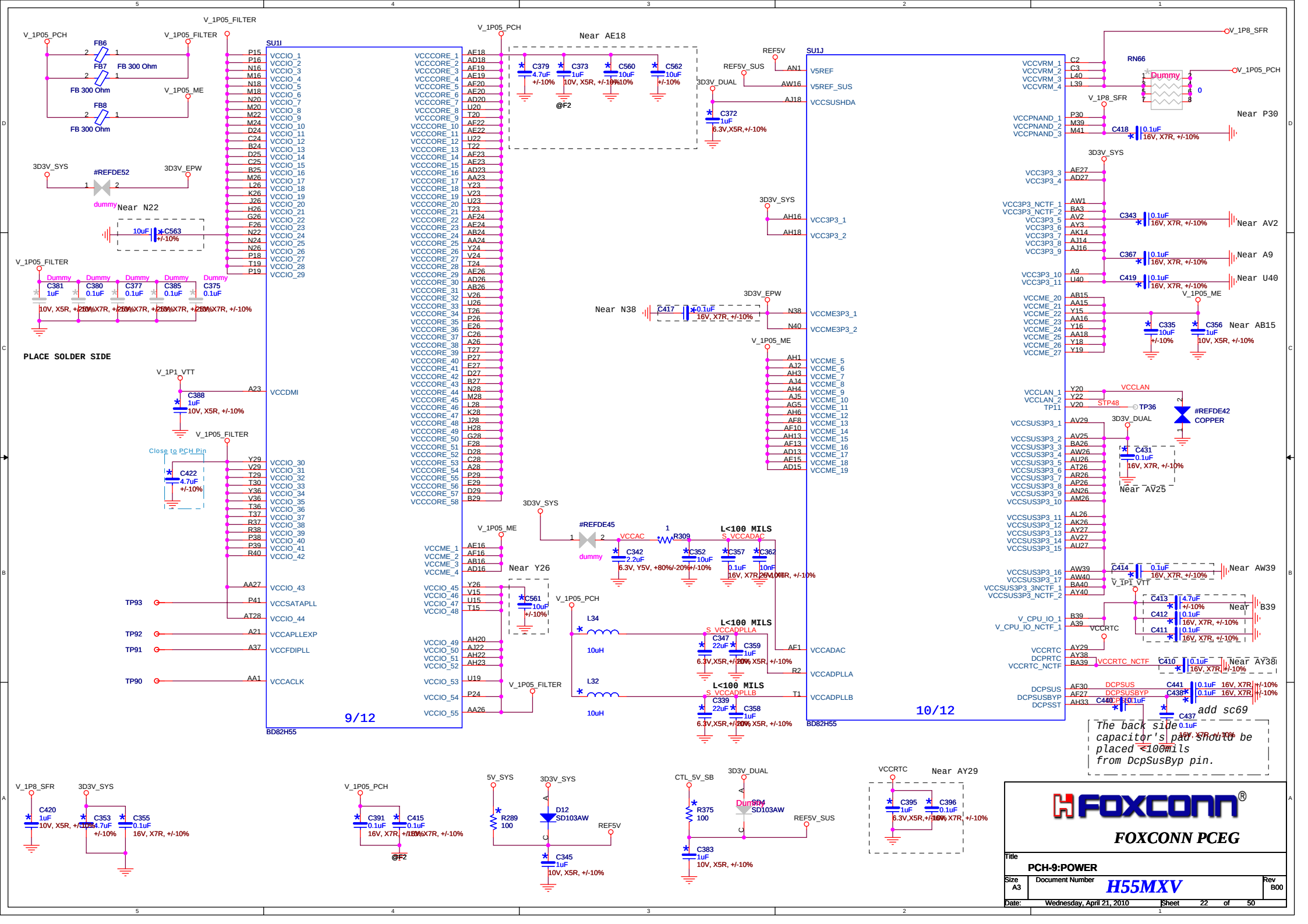
Title	PCH-8:CLOCK	
Size A3	Document Number *H55MXV*	Rev B00
Date: Thursday, December 24, 2009	Sheet 21 of 50	


V_1P05_FILTER
V_1P05_PCH
FB6
FB7
FB 300 Ohm
FB 300 Ohm
V_1P05_ME
FB8
FB 300 Ohm
SU1I
VCCIO_1
VCCIO_2
VCCIO_3
VCCIO_4
VCCIO_5
VCCIO_6
VCCIO_7
VCCIO_8
VCCIO_9
VCCIO_10
VCCIO_11
VCCIO_12
VCCIO_13
VCCIO_14
VCCIO_15
VCCIO_16
VCCIO_17
VCCIO_18
VCCIO_19
VCCIO_20
VCCIO_21
VCCIO_22
VCCIO_23
VCCIO_24
VCCIO_25
VCCIO_26
VCCIO_27
VCCIO_28
VCCIO_29
3D3V_SYS
#REFDE52
3D3V_EPW
dummy
Near N22
10uF
C563
+/-10%
V_1P05_FILTER
Dummy
C381
1uF
Dummy
C380
0.1uF
Dummy
C377
0.1uF
Dummy
C385
0.1uF
Dummy
C375
0.1uF
10V, X5R, +/-10%
PLACE SOLDER SIDE
V_1P1_VTT
C388
1uF
10V, X5R, +/-10%
VCCDMI
V_1P05_FILTER
Close to PCH Pin
C422
4.7uF
+/-10%
VCCIO_30
VCCIO_31
VCCIO_32
VCCIO_33
VCCIO_34
VCCIO_35
VCCIO_36
VCCIO_37
VCCIO_38
VCCIO_39
VCCIO_40
VCCIO_41
VCCIO_42
VCCIO_43
VCCSATAPLL
VCCIO_44
VCCAPLLEXP
VCCFDIPLL
VCCACLK
TP93
TP92
TP91
TP90
VCCCORE_1
VCCCORE_2
VCCCORE_3
VCCCORE_4
VCCCORE_5
VCCCORE_6
VCCCORE_7
VCCCORE_8
VCCCORE_9
VCCCORE_10
VCCCORE_11
VCCCORE_12
VCCCORE_13
VCCCORE_14
VCCCORE_15
VCCCORE_16
VCCCORE_17
VCCCORE_18
VCCCORE_19
VCCCORE_20
VCCCORE_21
VCCCORE_22
VCCCORE_23
VCCCORE_24
VCCCORE_25
VCCCORE_26
VCCCORE_27
VCCCORE_28
VCCCORE_29
VCCCORE_30
VCCCORE_31
VCCCORE_32
VCCCORE_33
VCCCORE_34
VCCCORE_35
VCCCORE_36
VCCCORE_37
VCCCORE_38
VCCCORE_39
VCCCORE_40
VCCCORE_41
VCCCORE_42
VCCCORE_43
VCCCORE_44
VCCCORE_45
VCCCORE_46
VCCCORE_47
VCCCORE_48
VCCCORE_49
VCCCORE_50
VCCCORE_51
VCCCORE_52
VCCCORE_53
VCCCORE_54
VCCCORE_55
VCCCORE_56
VCCCORE_57
VCCCORE_58
V_1P05_PCH
Near AE18
C379
4.7uF
+/-10%
C373
1uF
10V, X5R, +/-10%
C560
10uF
+/-10%
C562
10uF
+/-10%
@F2
REF5V
REF5V_SUS
3D3V_DUAL
C372
1uF
6.3V,X5R,+/-10%
SU1J
V5REF
V5REF_SUS
VCCSUSHDA
3D3V_SYS
VCC3P3_1
VCC3P3_2
3D3V_EPW
Near N38
C417
0.1uF
16V, X7R, +/-10%
VCCME3P3_1
VCCME3P3_2
V_1P05_ME
VCCME_5
VCCME_6
VCCME_7
VCCME_8
VCCME_9
VCCME_10
VCCME_11
VCCME_12
VCCME_13
VCCME_14
VCCME_15
VCCME_16
VCCME_17
VCCME_18
VCCME_19
VCCME_1
VCCME_2
VCCME_3
VCCME_4
3D3V_SYS
#REFDE45
dummy
VCCAC
R309
L<100 MILS
S_VCCADAC
C342
2.2uF
6.3V, Y5V, +80%/-20%
C352
10uF
+/-10%
C357
0.1uF
16V, X7R, +/-10%
C362
10nF
16V, X7R, +/-10%
Near Y26
C561
10uF
+/-10%
V_1P05_PCH
L34
10uH
L32
10uH
L<100 MILS
S_VCCADPLLA
C347
22uF
6.3V,X5R,+/-20%
C359
1uF
10V, X5R, +/-10%
L<100 MILS
S_VCCADPLLB
C339
22uF
6.3V,X5R,+/-20%
C358
1uF
10V, X5R, +/-10%
V_1P05_FILTER
VCCIO_45
VCCIO_46
VCCIO_47
VCCIO_48
VCCIO_49
VCCIO_50
VCCIO_51
VCCIO_52
VCCIO_53
VCCIO_54
VCCIO_55
AF1
VCCADAC
R2
VCCADPLLA
T1
VCCADPLLB
9/12
BD82H55
10/12
BD82H55
V_1P8_SFR
RN66
Dummy
V_1P05_PCH
Near P30
C418
0.1uF
16V, X7R, +/-10%
VCCVRM_1
VCCVRM_2
VCCVRM_3
VCCVRM_4
VCCPNAND_1
VCCPNAND_2
VCCPNAND_3
VCC3P3_3
VCC3P3_4
VCC3P3_NCTF_1
VCC3P3_NCTF_2
VCC3P3_5
VCC3P3_6
VCC3P3_7
VCC3P3_8
VCC3P3_9
VCC3P3_10
VCC3P3_11
C343
0.1uF
16V, X7R, +/-10%
Near AV2
C367
0.1uF
16V, X7R, +/-10%
Near A9
C419
0.1uF
16V, X7R, +/-10%
Near U40
V_1P05_ME
C335
10uF
+/-10%
C356
1uF
10V, X5R, +/-10%
Near AB15
VCCME_20
VCCME_21
VCCME_22
VCCME_23
VCCME_24
VCCME_25
VCCME_26
VCCME_27
VCCLAN
STP48
TP36
#REFDE42
COPPER
VCCLAN_1
VCCLAN_2
TP11
3D3V_DUAL
C431
0.1uF
16V, X7R, +/-10%
Near AV25
VCCSUS3P3_1
VCCSUS3P3_2
VCCSUS3P3_3
VCCSUS3P3_4
VCCSUS3P3_5
VCCSUS3P3_6
VCCSUS3P3_7
VCCSUS3P3_8
VCCSUS3P3_9
VCCSUS3P3_10
VCCSUS3P3_11
VCCSUS3P3_12
VCCSUS3P3_13
VCCSUS3P3_14
VCCSUS3P3_15
VCCSUS3P3_16
VCCSUS3P3_17
VCCSUS3P3_3NCTF_1
VCCSUS3P3_NCTF_2
C414
0.1uF
16V, X7R, +/-10%
Near AW39
V_1P1_VTT
C413
4.7uF
+/-10%
C412
0.1uF
16V, X7R, +/-10%
C411
0.1uF
16V, X7R, +/-10%
Near B39
V_CPU_IO_1
V_CPU_IO_NCTF_1
VCCRTC
VCCRTC
DCPRTC
VCCRTC_NCTF
VCCRTC_NCTF
C410
0.1uF
16V, X7R, +/-10%
Near AY38
DCPSUS
DCPSUSBYP
DCPSST
DCPSUS
DCPSUSBYP
C441
0.1uF
16V, X7R, +/-10%
C438
0.1uF
16V, X7R, +/-10%
C440
0.1uF
C437
0.1uF
16V, X7R, +/-10%
add sc69
The back side capacitor's pad should be placed <100mils from DcpSusByp pin.
V_1P8_SFR
3D3V_SYS
C420
1uF
10V, X5R, +/-10%
C353
4.7uF
+/-10%
C355
0.1uF
16V, X7R, +/-10%
V_1P05_PCH
C391
0.1uF
16V, X7R, +/-10%
C415
0.1uF
16V, X7R, +/-10%
@F2
5V_SYS
3D3V_SYS
R289
100
D12
SD103AW
REF5V
C345
1uF
10V, X5R, +/-10%
CTL_5V_SB
3D3V_DUAL
R375
100
Dummy
SD103AW
REF5V_SUS
C383
1uF
10V, X5R, +/-10%
VCCRTC
Near AY29
C395
1uF
6.3V,X5R,+/-10%
C396
0.1uF
16V, X7R, +/-10%
FOXCONN®
FOXCONN PCEG
Title
PCH-9:POWER
Size
A3
Document Number
H55MXV
Rev
B00
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22
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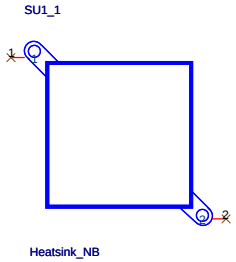
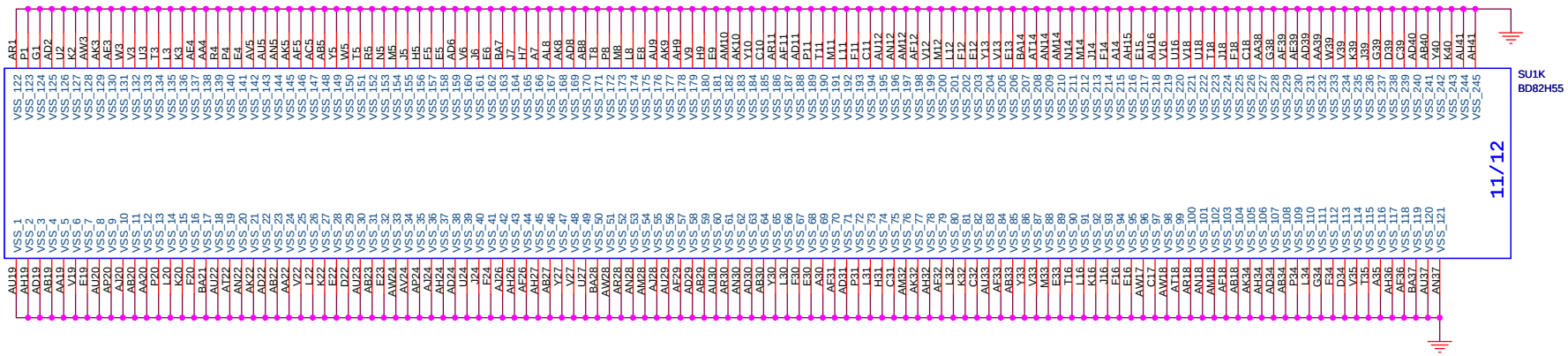
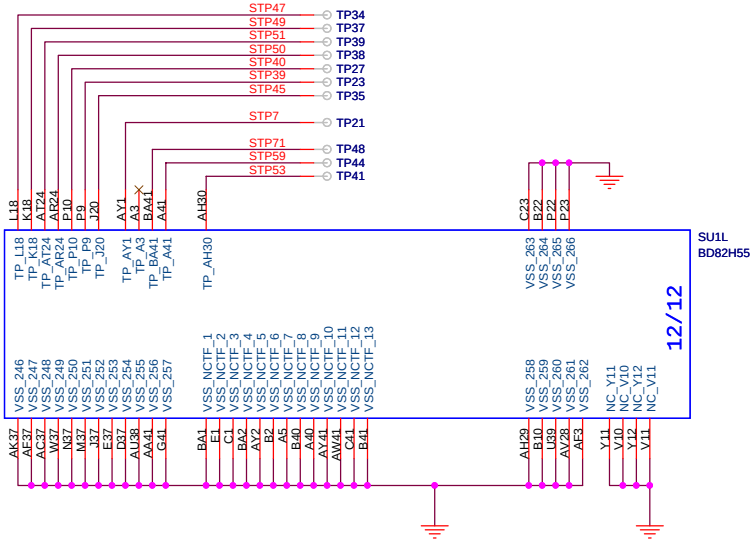
50







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Title: PCH-10:GND		
Size: A3	Document Number: H55MXV	Rev: B00
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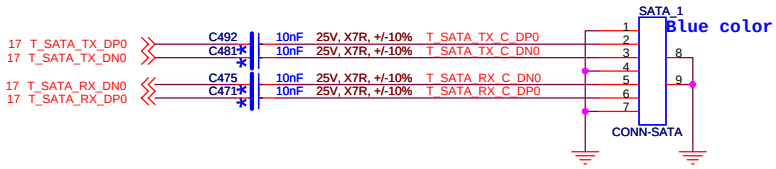
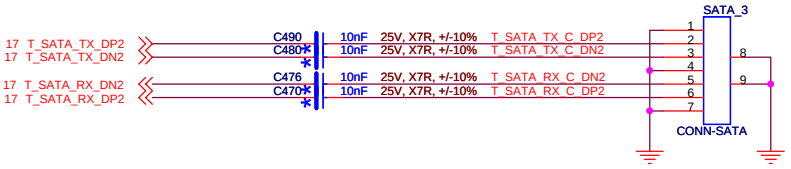
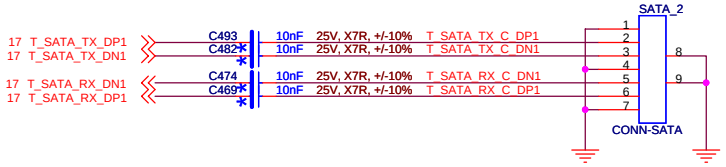
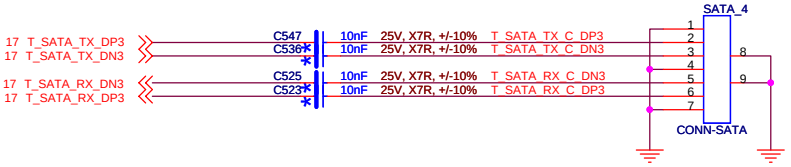
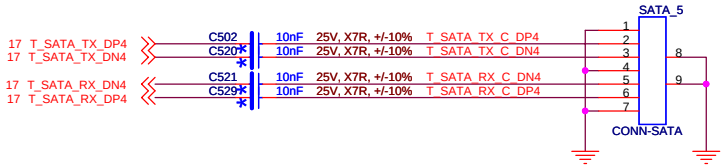
SATA x 6

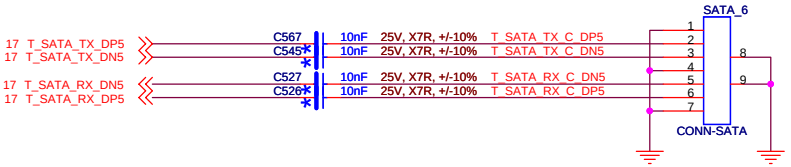












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Title	SATAx4/ESATA Buffer	
Size A3	Document Number *H55MXV*	Rev B00
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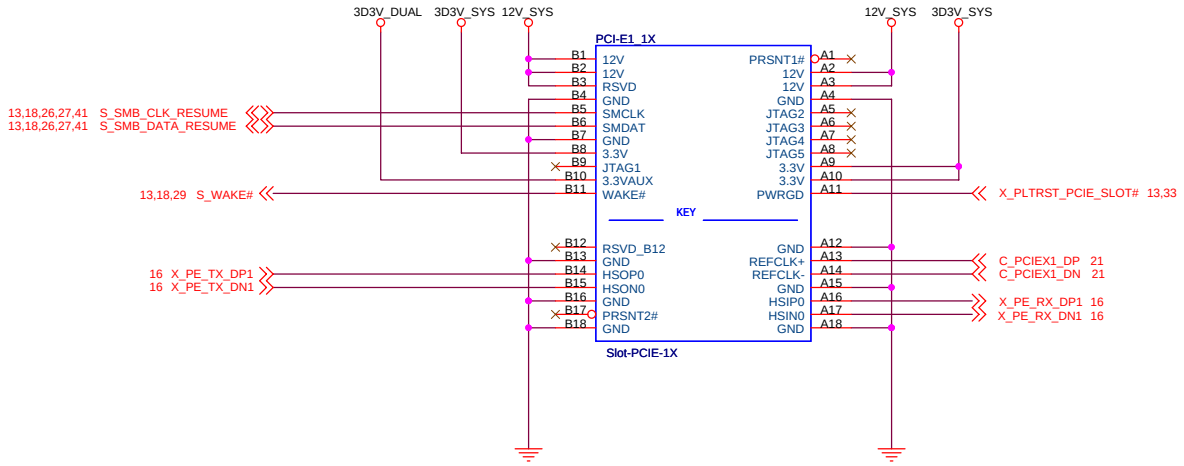
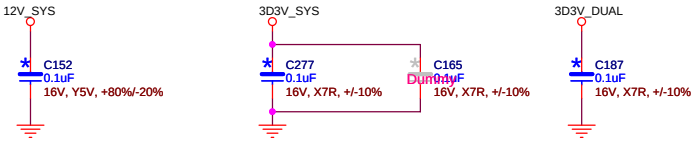
PCIE X1 SLOT





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Title: PCIE X1 Slot

Size	Document Number	Rev
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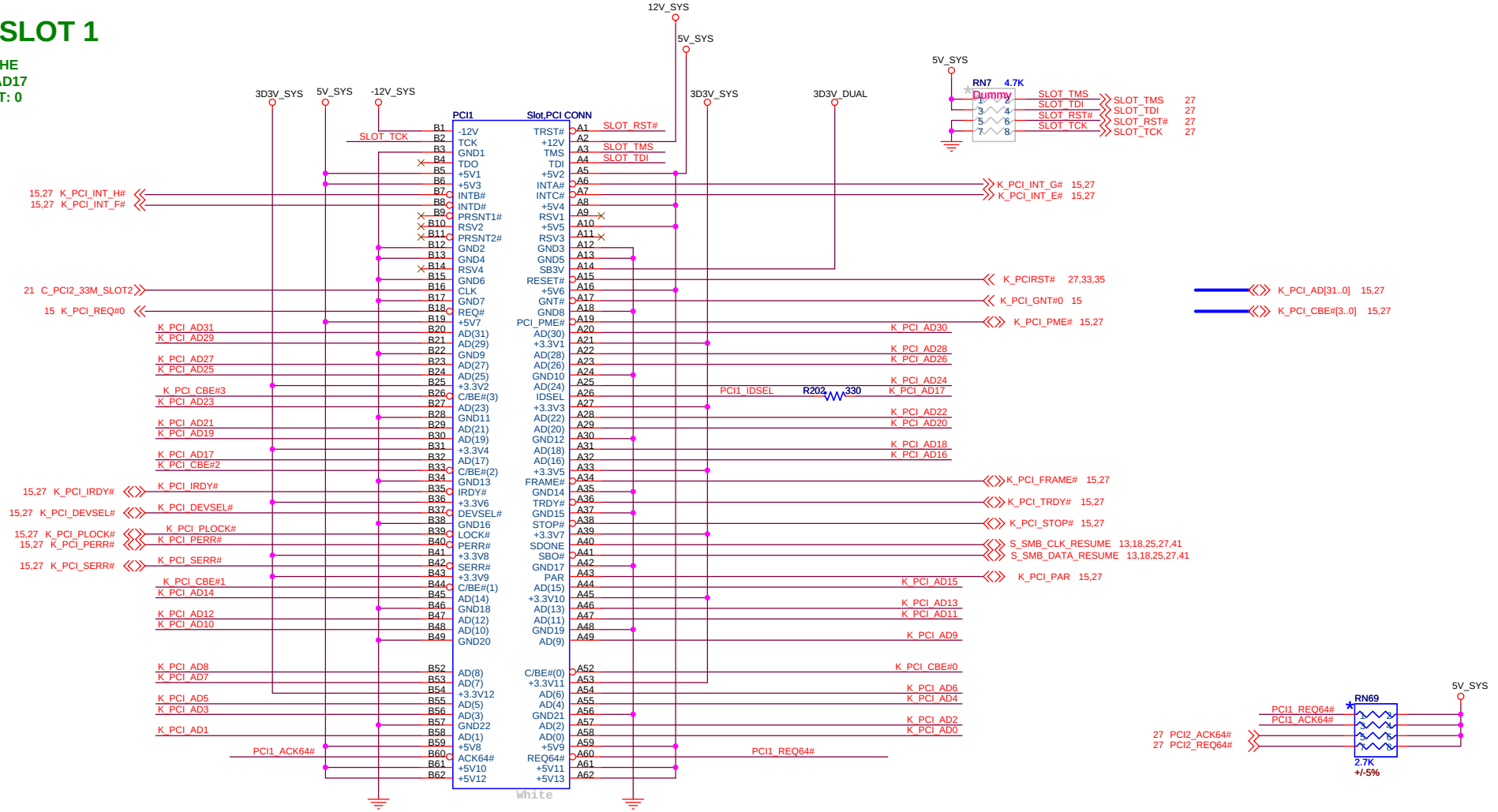
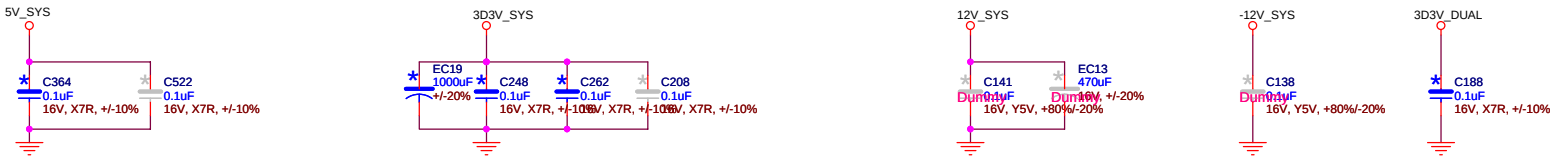
PCI SLOT 1

IRQ: FGHE
IDSEL: AD17
REQ/GNT: 0





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Title	PCI SLOT 1	
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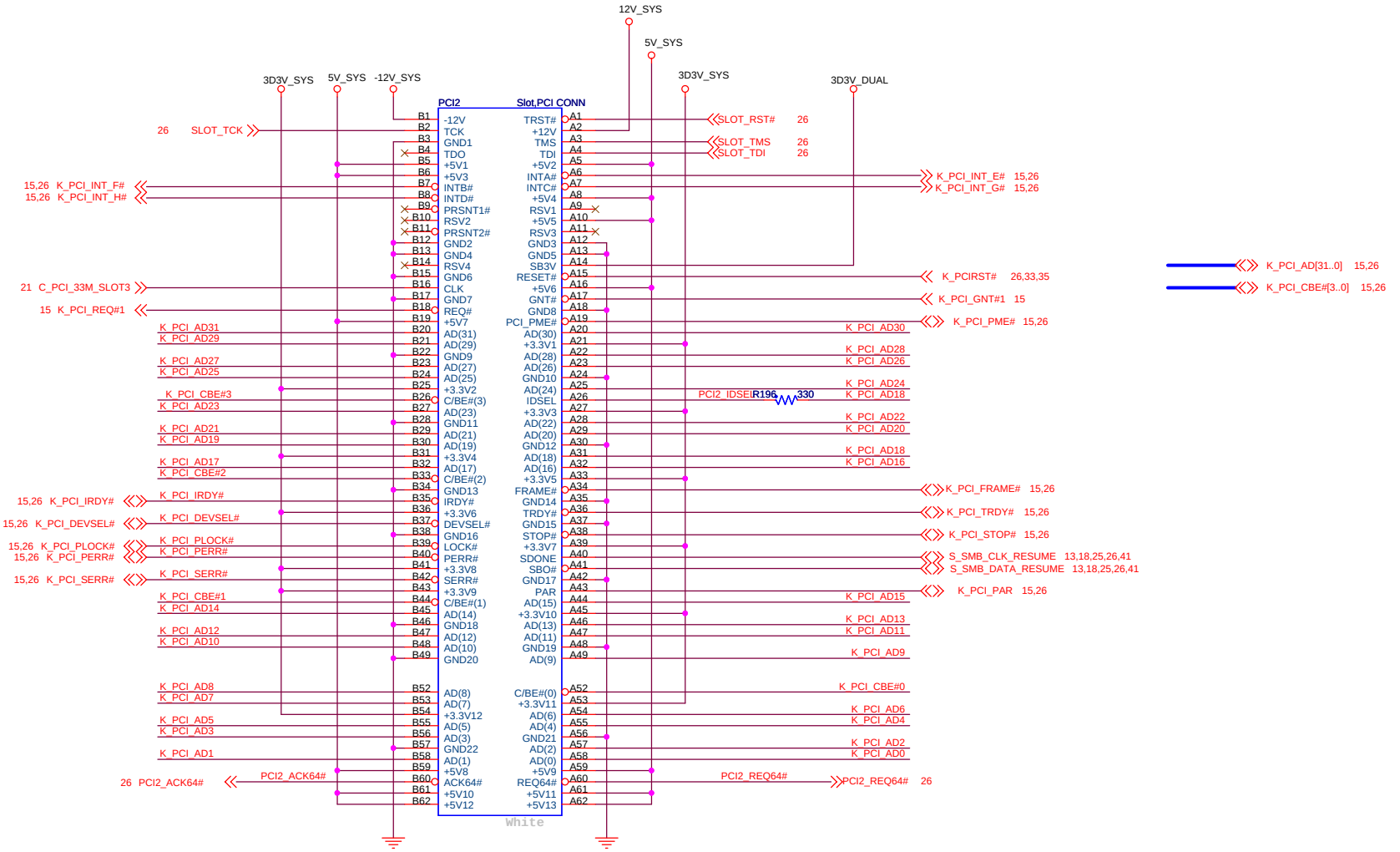
PCI SLOT 2

IRQ: GFEH
IDSEL: AD18
REQ/GNT: 1



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Title	PCI SLOT 2	
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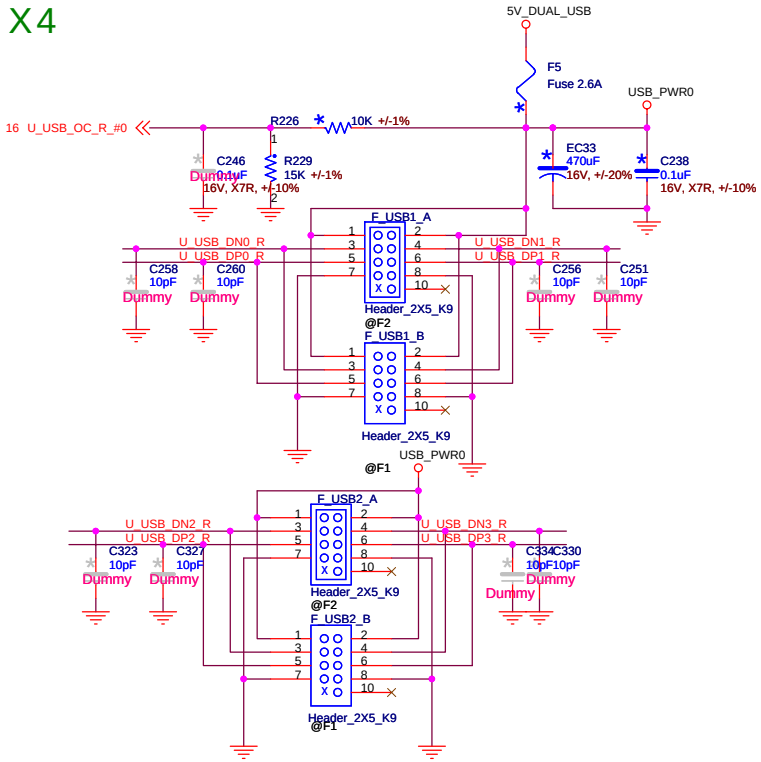
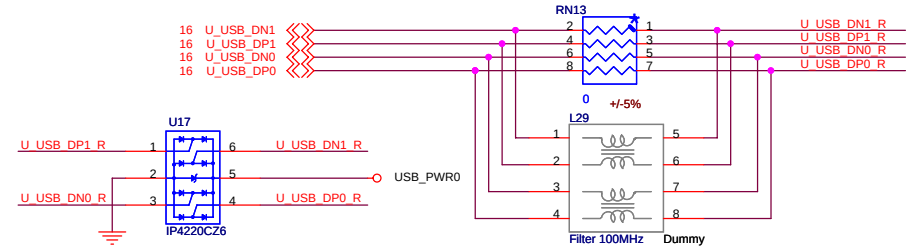
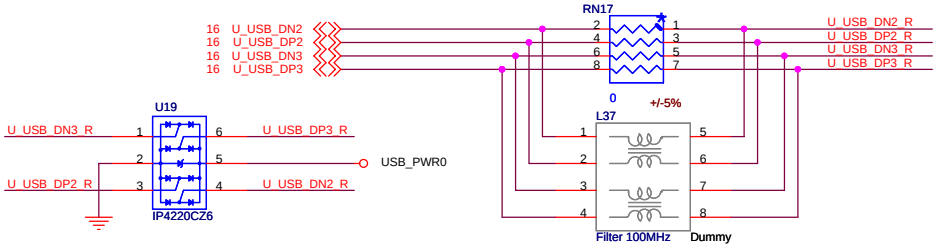
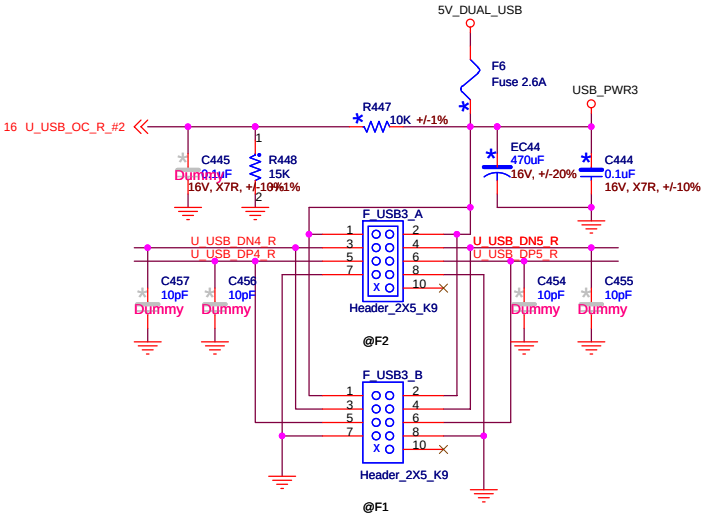
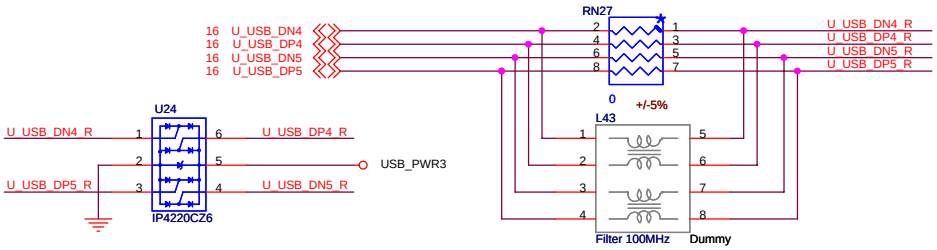
Front USB Header X4











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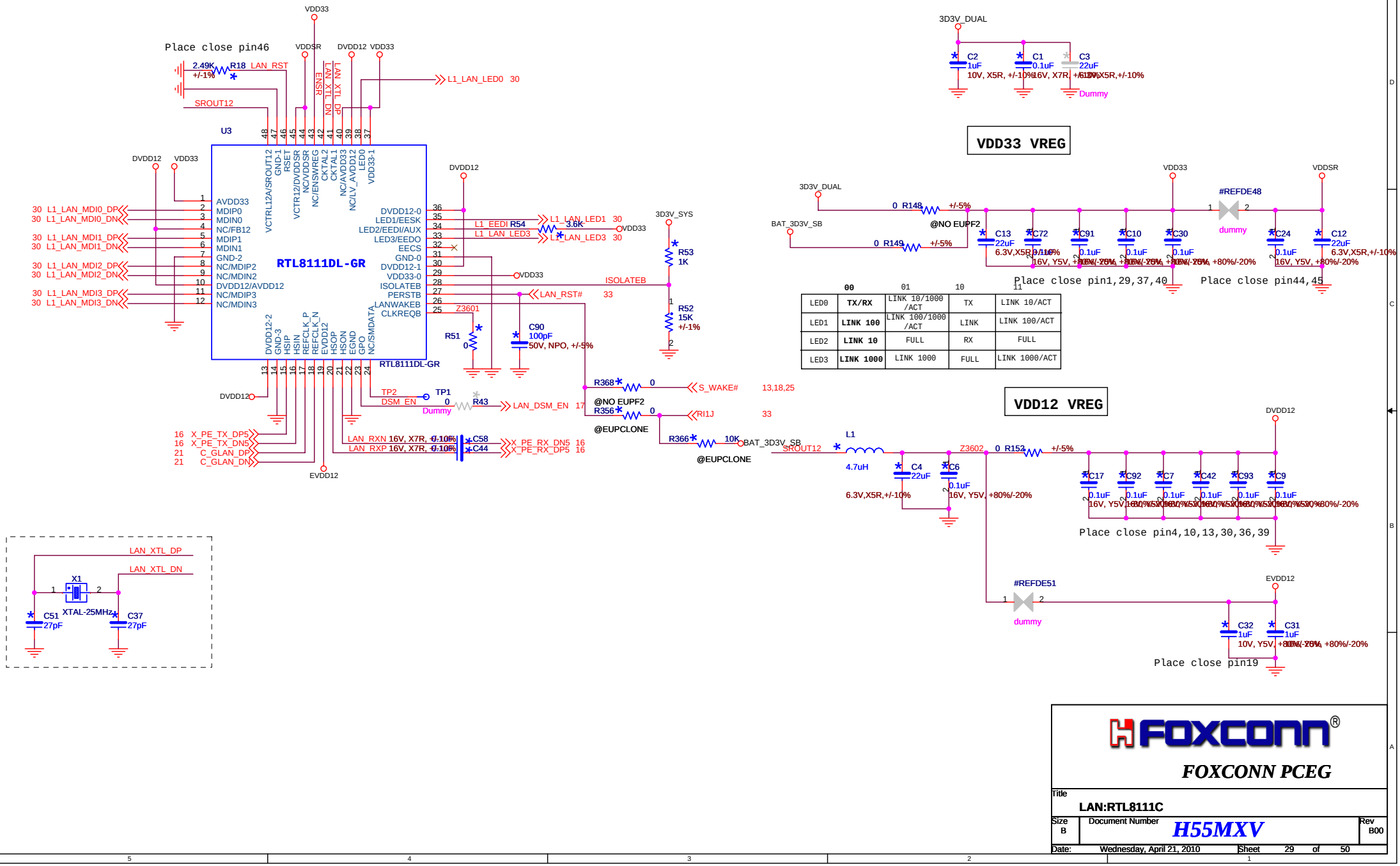
Title: **Front USB Header**		
Size: A3	Document Number: ***H55MXV***	Rev: B00
Date: Wednesday, April 21, 2010	Sheet 28 of 50	



	00	01	10	11
LED0	TX/RX	LINK 10/1000 /ACT	TX	LINK 10/ACT
LED1	LINK 100	LINK 100/1000 /ACT	LINK	LINK 100/ACT
LED2	LINK 10	FULL	RX	FULL
LED3	LINK 1000	LINK 1000	FULL	LINK 1000/ACT

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FOXCONN PCEG

Title: LAN:RTL8111C

Size: B | Document Number: H55MXV | Rev: B00

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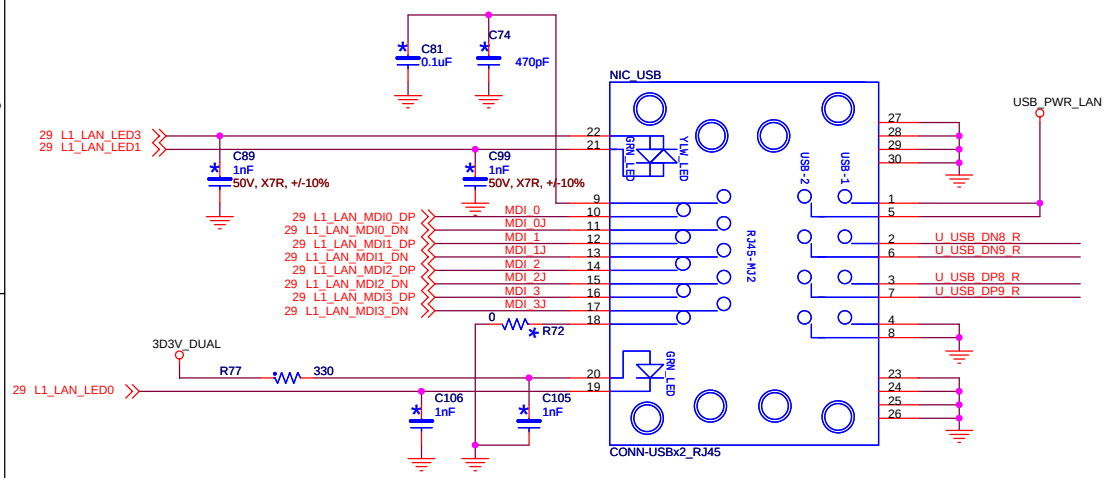
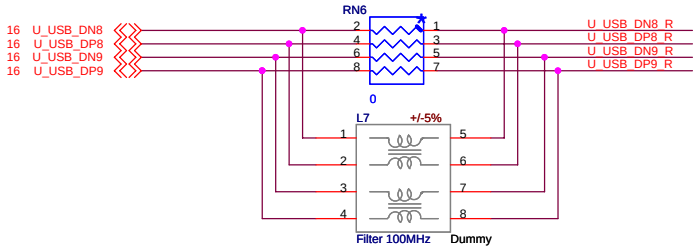
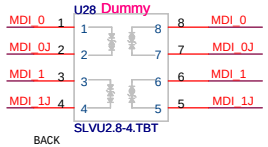
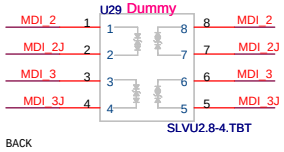
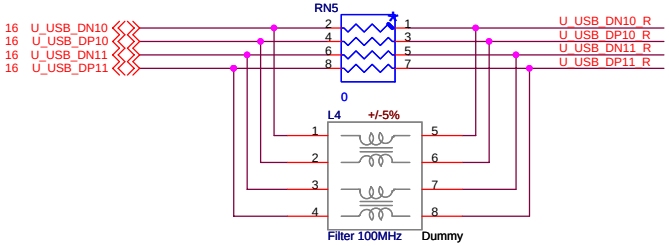
LAN/USB CONNECTOR

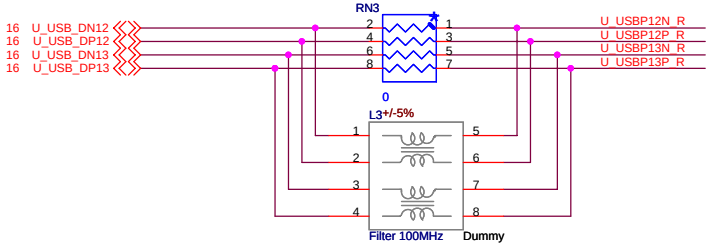


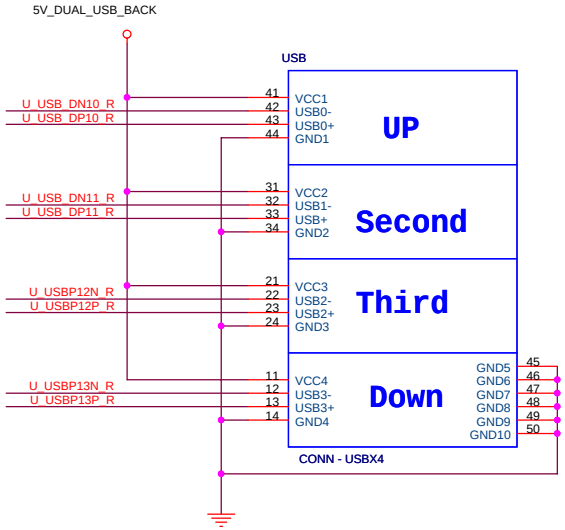


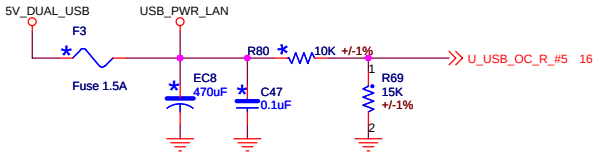


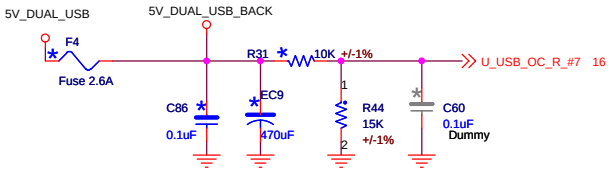


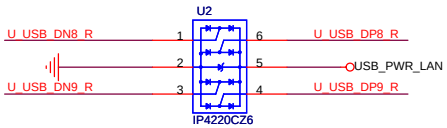


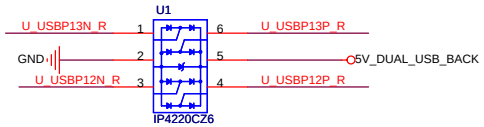


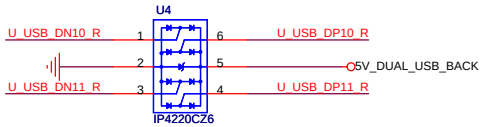












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FOXCONN PCEG

Title	LAN/USB CONN	
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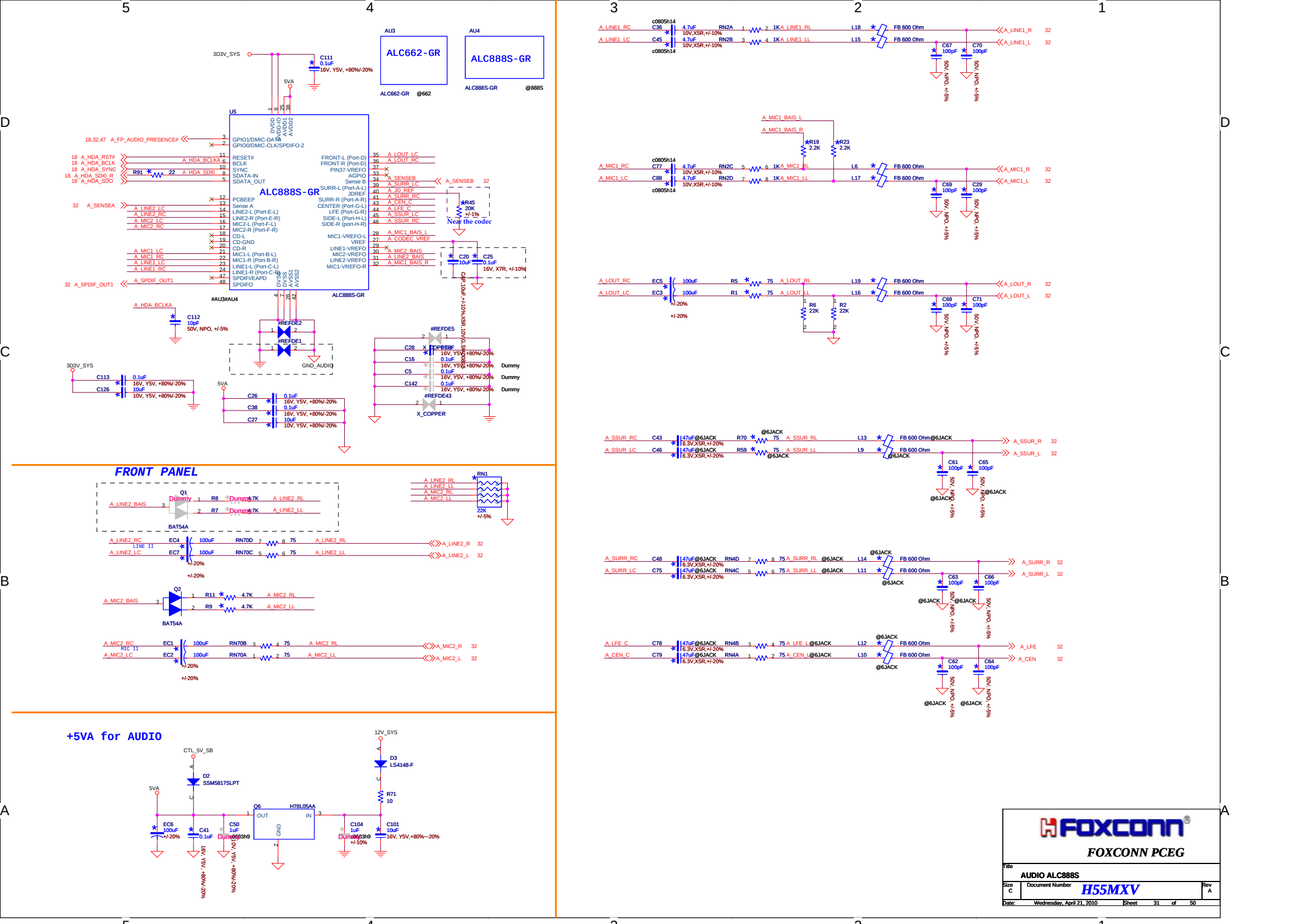
AU3
ALC662-GR
ALC662-GR @662
AU4
ALC888S-GR
ALC888S-GR @888S
U5
ALC888S-GR
#AU3#AU4
Near the codec
FRONT PANEL
+5VA for AUDIO
FOXCONN PCEG
AUDIO ALC888S
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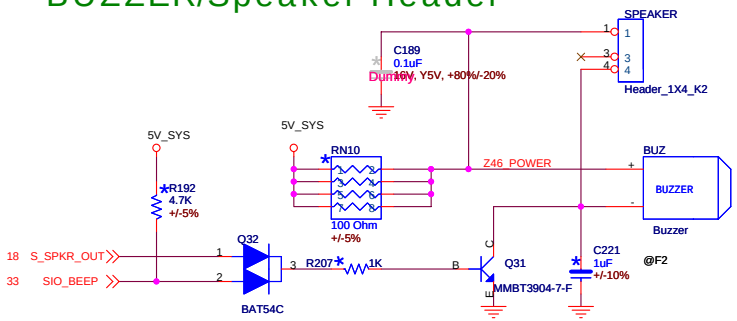
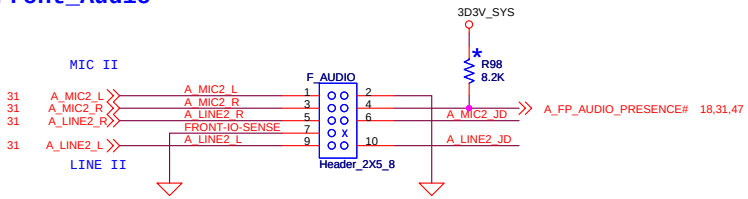
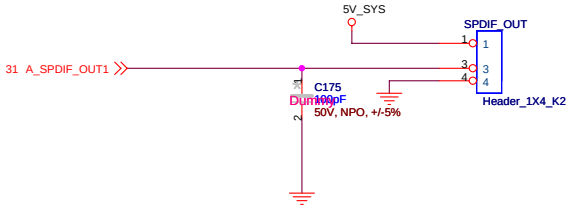
BUZZER/Speaker Header



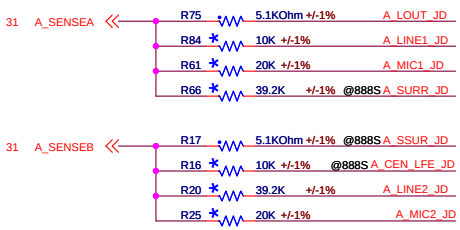
Front_Audio

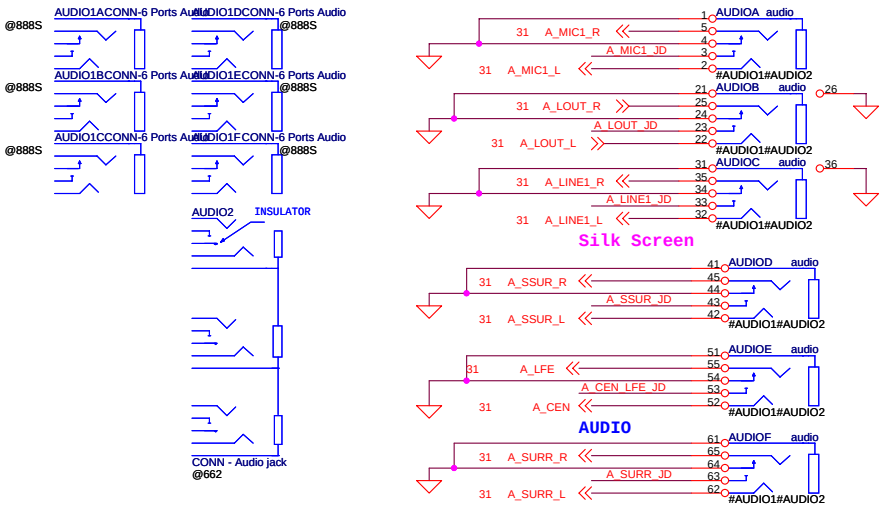


SPDIF OUT Header

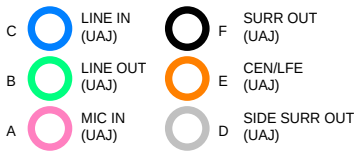


JACK SENSE





Audio Jack



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FOXCONN PCEG

Title: AUDIO JACK /BUZZER			
Size: Custom	Document Number: H55MXV		Rev: A
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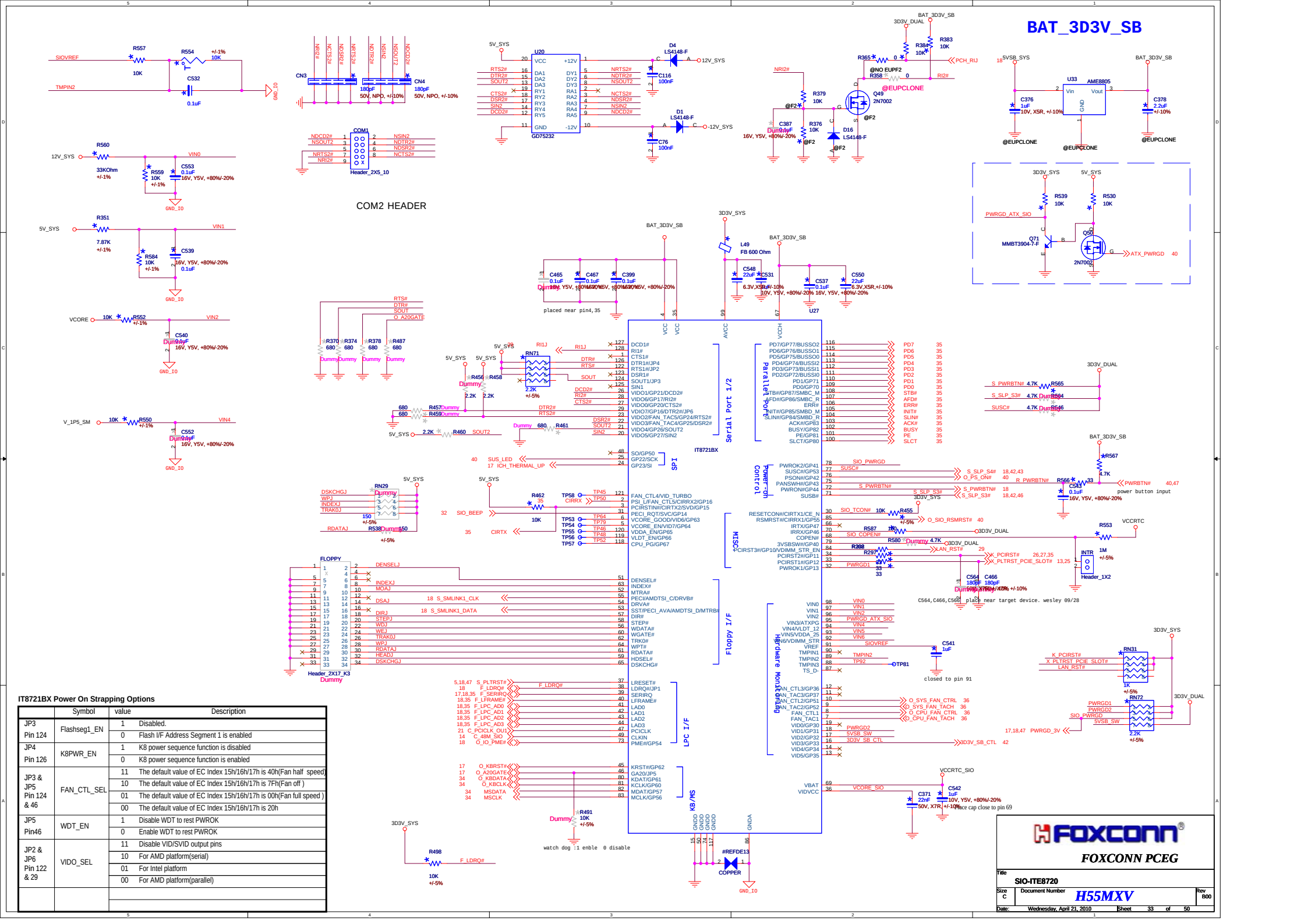
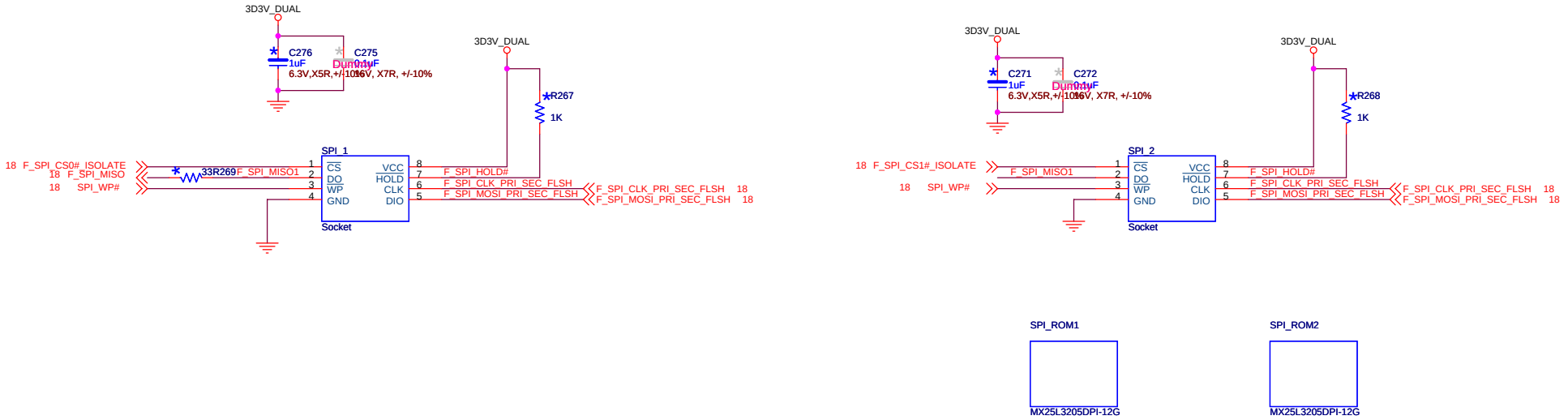


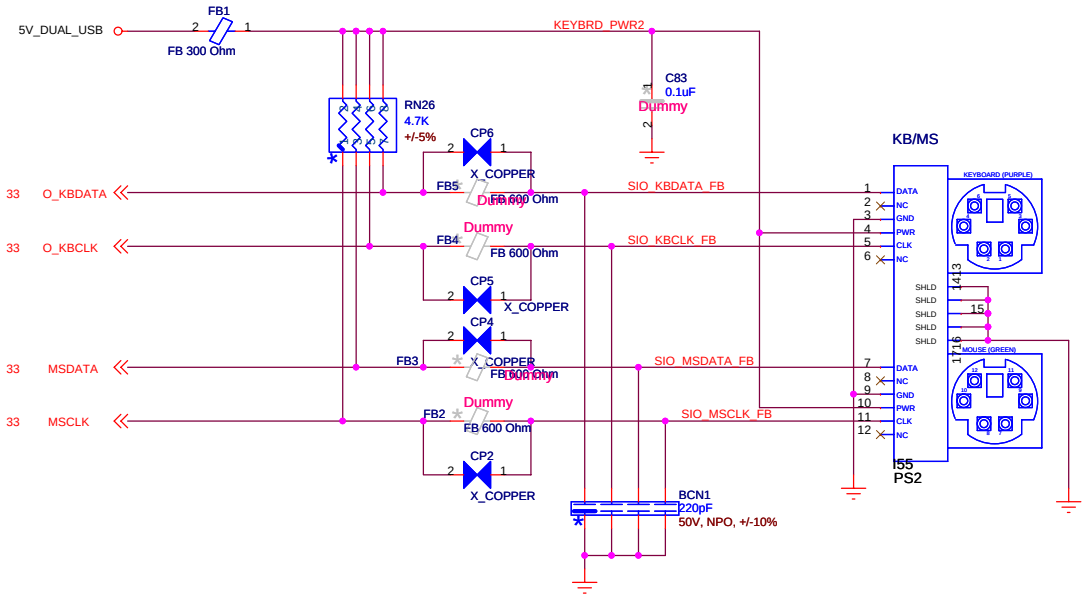
IT8721BX Power On Strapping Options

	Symbol	value	Description
JP3 Pin 124	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP2 & JP6 Pin 122 & 29	VIDO_SEL	11	Disable VID/SVID output pins
		10	For AMD platform(serial)
		01	For Intel platform
		00	For AMD platform(parallel)

SPI



PS2 KB / MS



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Title	SPI/KBUSB	
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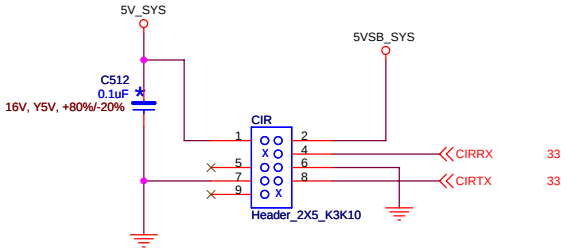
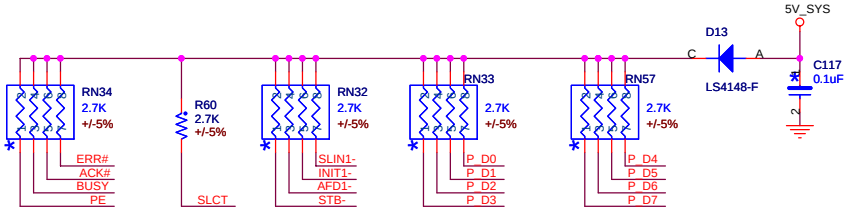
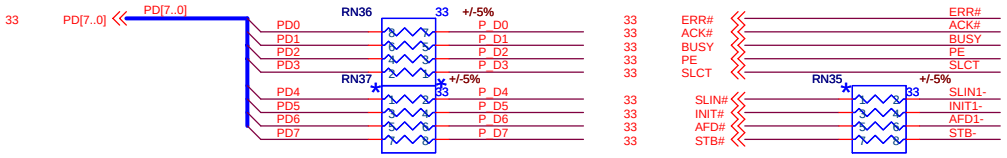
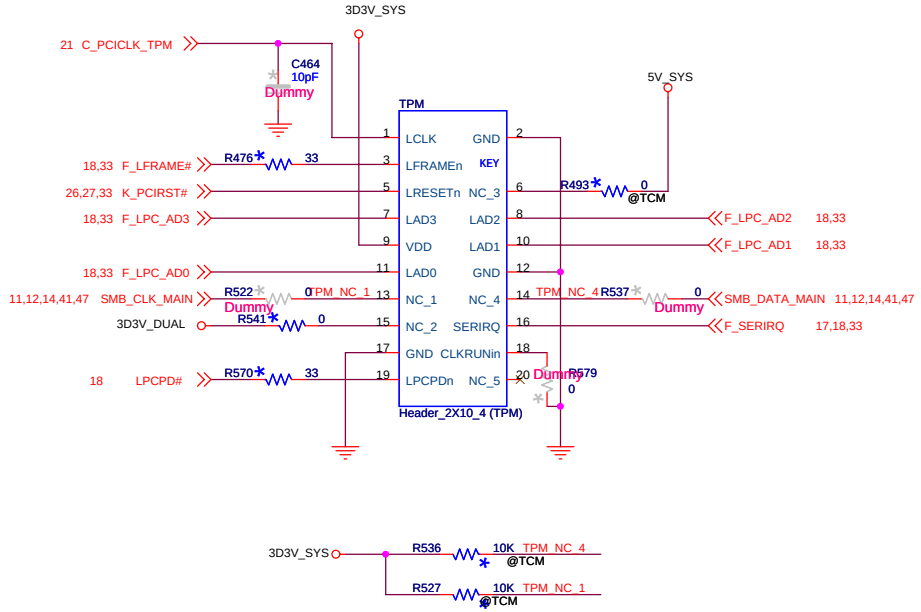
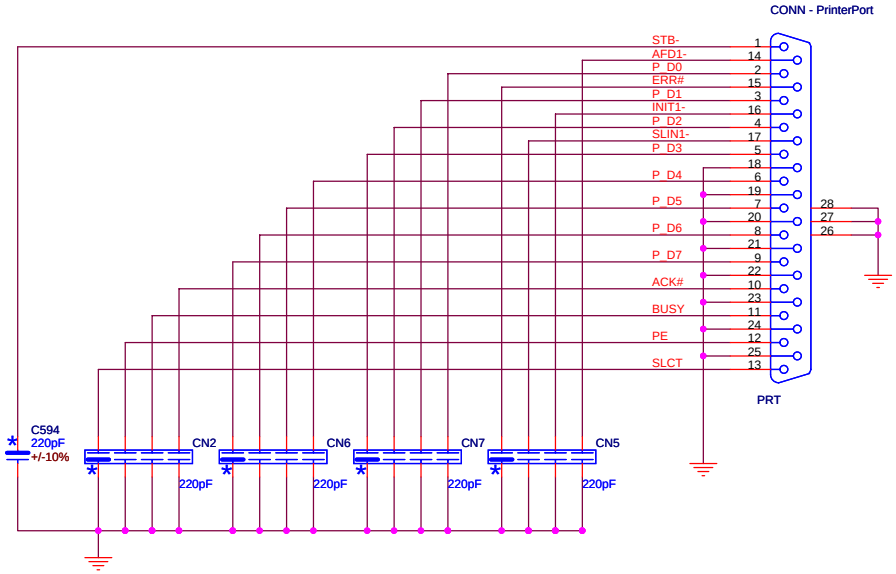






TPM/TCM Connector





LPT PORT

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Title	PCI SLOT	
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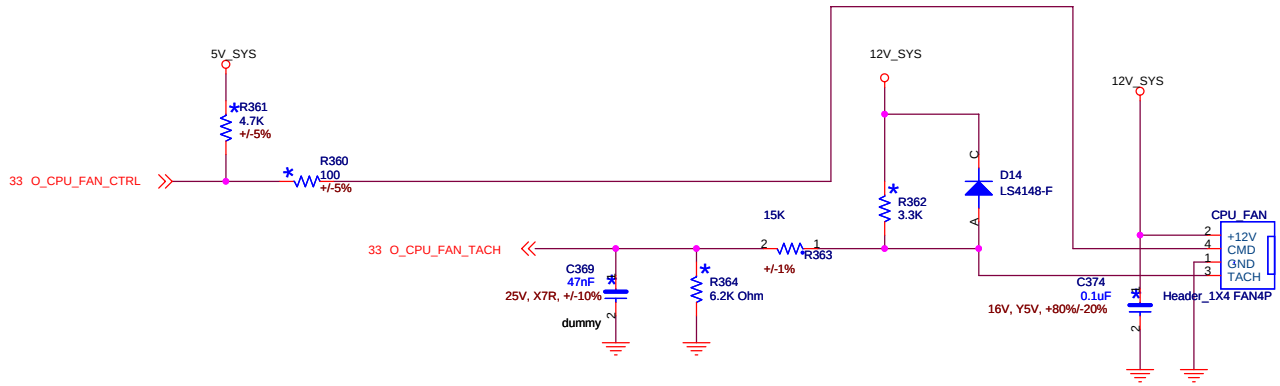
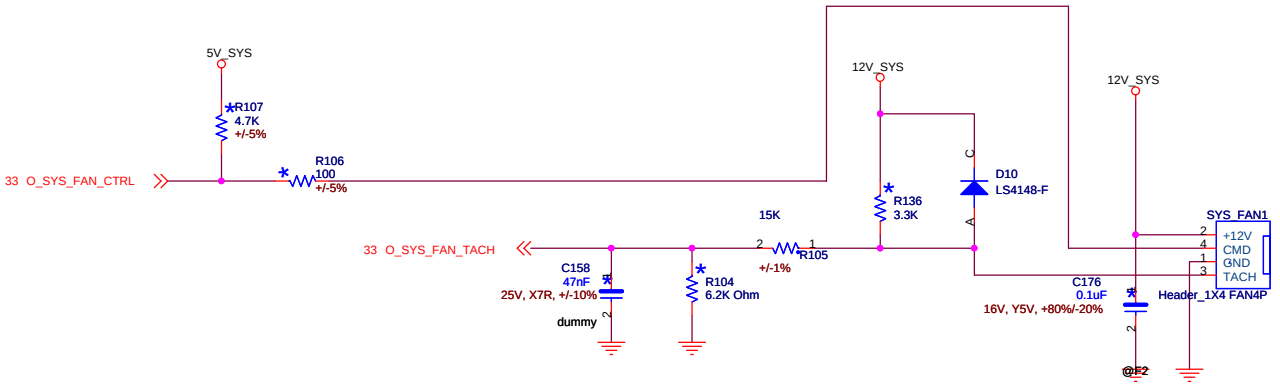
CPU FAN



SYSTEM FAN



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Title	CPU & System FAN	
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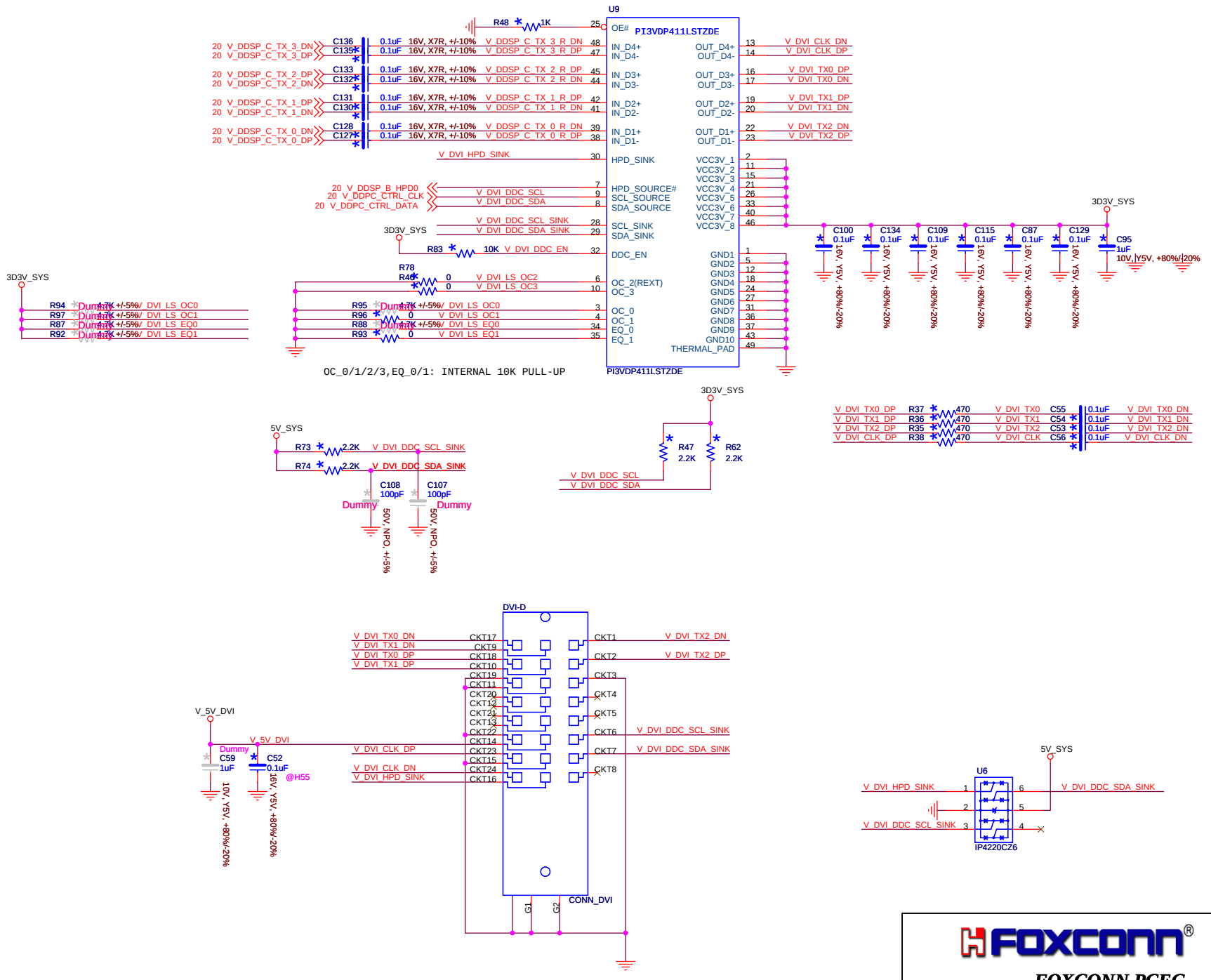

FOXCONN PCEG

Title: DVI-I Connector

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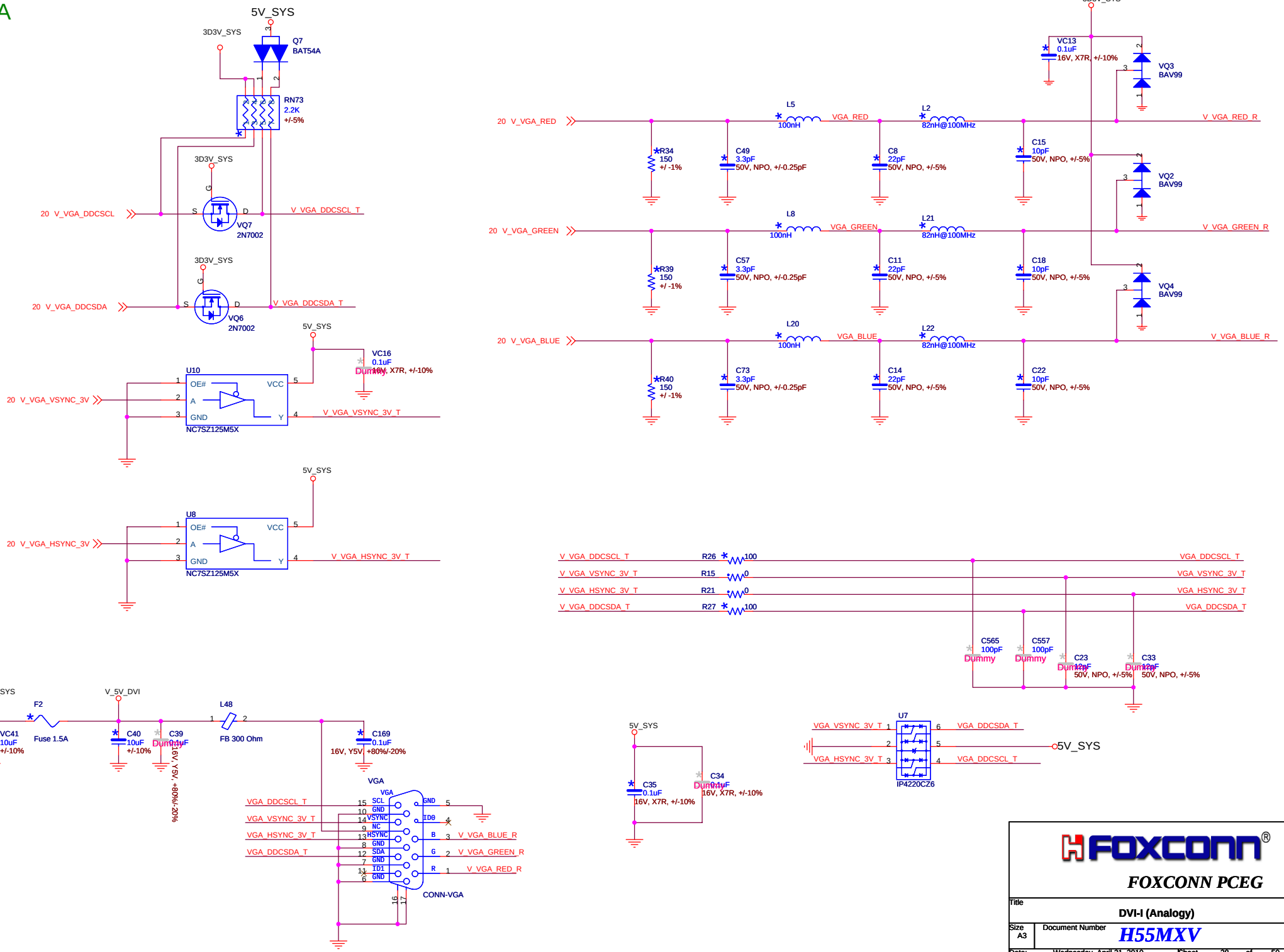
VGA



FOXCONN PCEG

Title	DVI-I (Analogy)	
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Title

BUZZER

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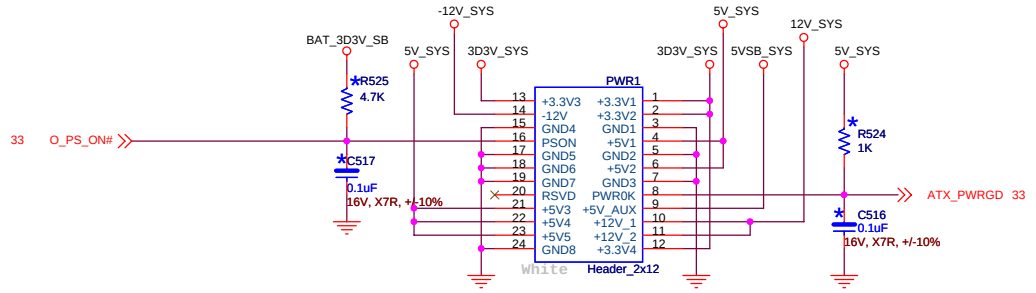
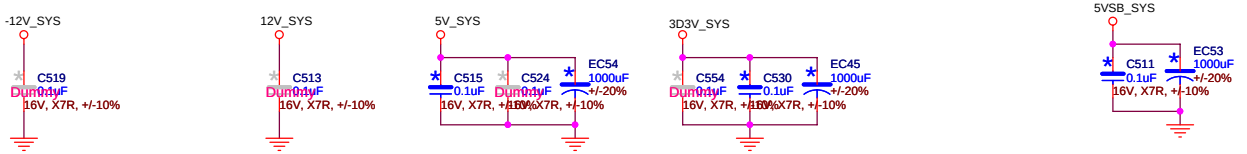
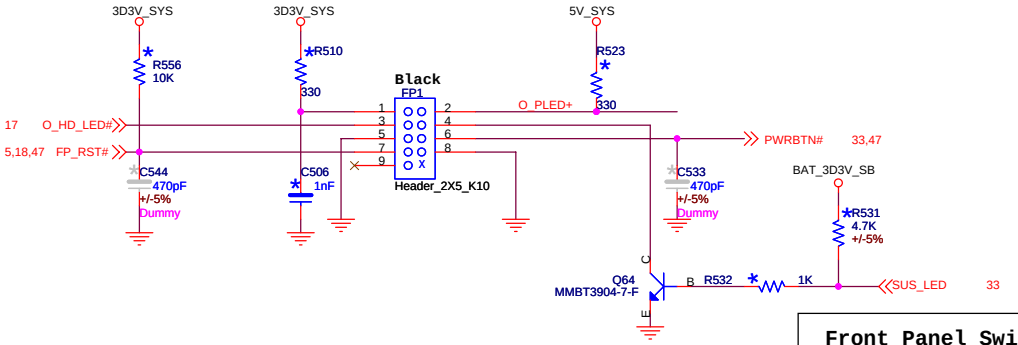
ATX POWER CONNECTOR





Front I/O Header

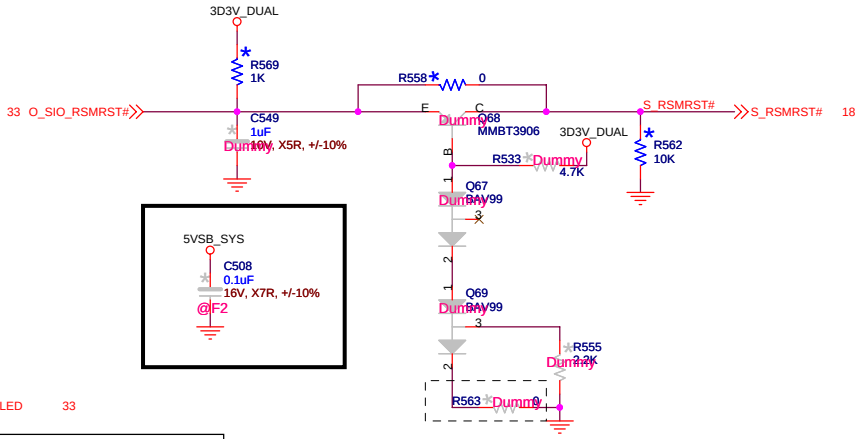


S0 : Power LED is on;
S1 : Power LED is blinking;
S3~S5: Power LED is off.

Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Detect pin
Detect pin	9	10	Key

RESUME RESET LOGIC



Title: ATX CONN/RESUME RESET

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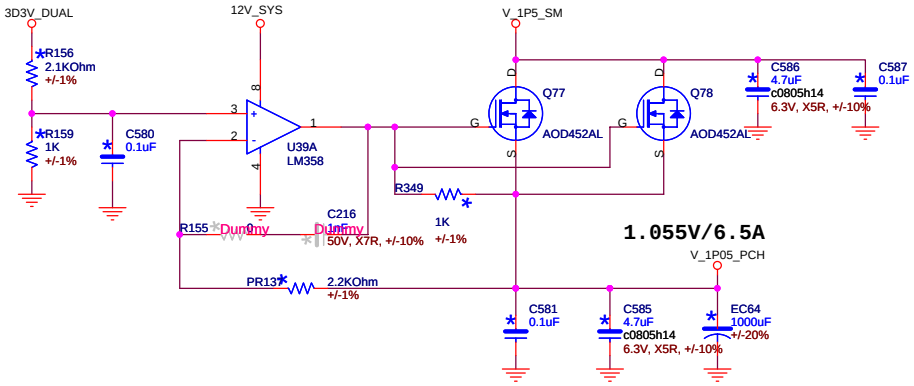
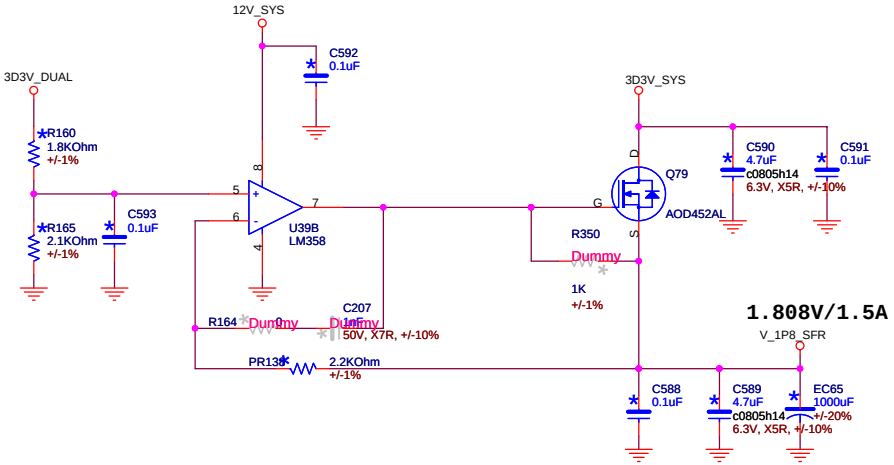
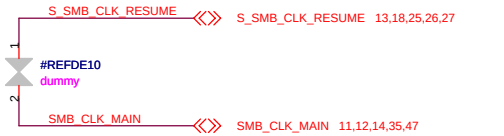
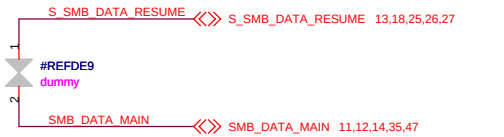
+V_1.05_PCH

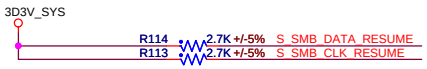




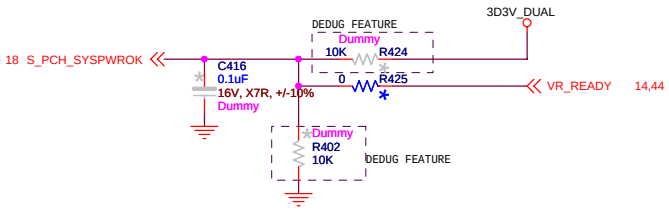
SMB ISOLATE







VR_READY DEFENSIVE (PCH POWEROK)



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Title	POWER-1:LINEAR POWER-1	
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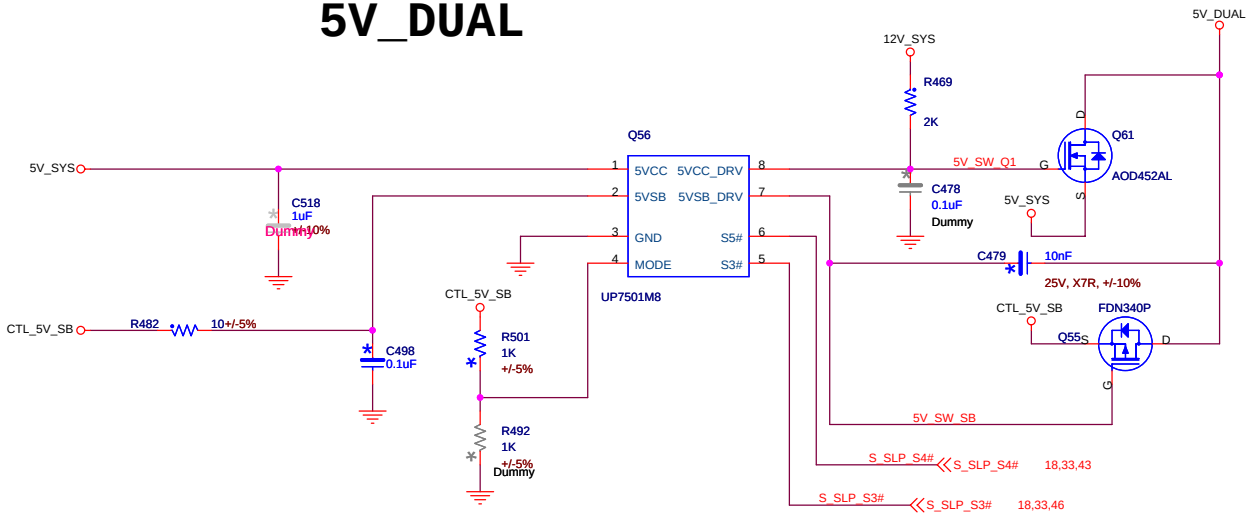
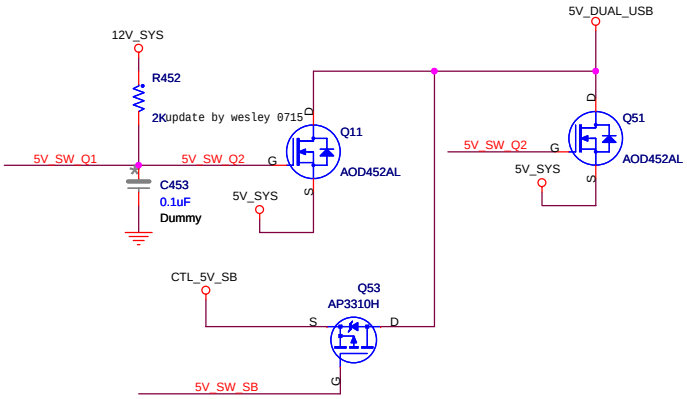
5V_DUAL



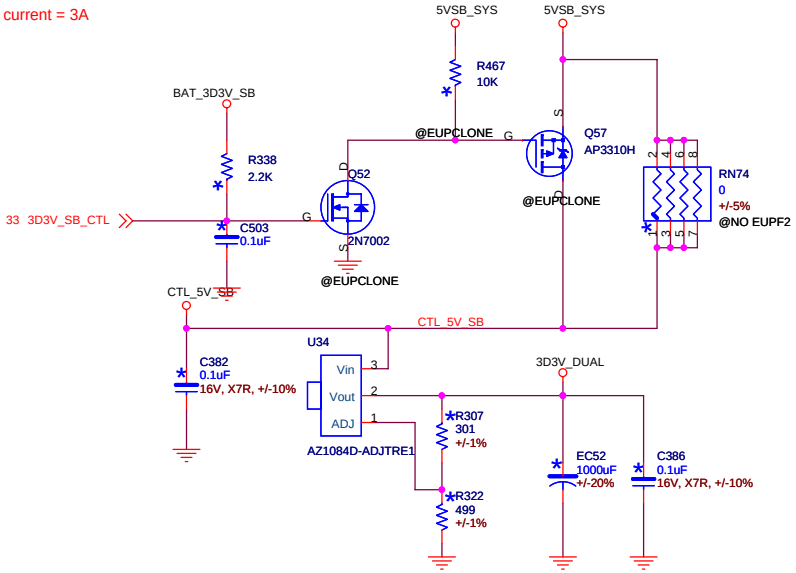


HI= S4/S5 5VDUAL FORM 5VSB
Low= S4/S5 5VDUAL TURN OFF

S5	S3	NODE	5VDUAL
H	H	X	5VCC
H	L	X	5VSB
L	X	H	5VSB
L	X	L	Shutdown

3D3V_SB

Max. output current = 3A



Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

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FOXCONN PCEG

Title
POWER-2:LINEAR POWER-2

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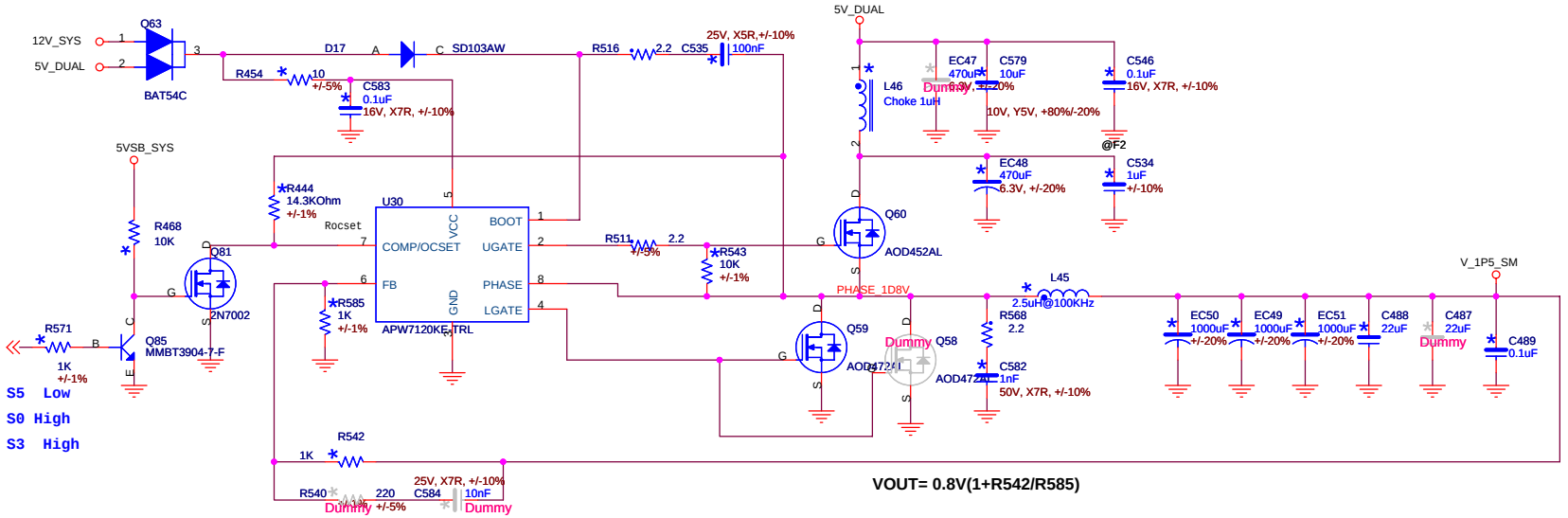
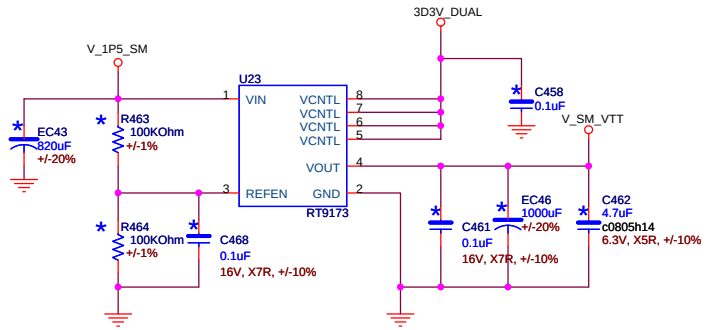


VOUT= 0.8V(1+R542/R585)

ROCPSET= (40uA*R10-0.4V)/Q8 RdsON



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FOXCONN PCEG

Title: POWER-5:V_SM/V_SM_VTT		
Size: A3	Document Number: H55MXV	Rev: X00
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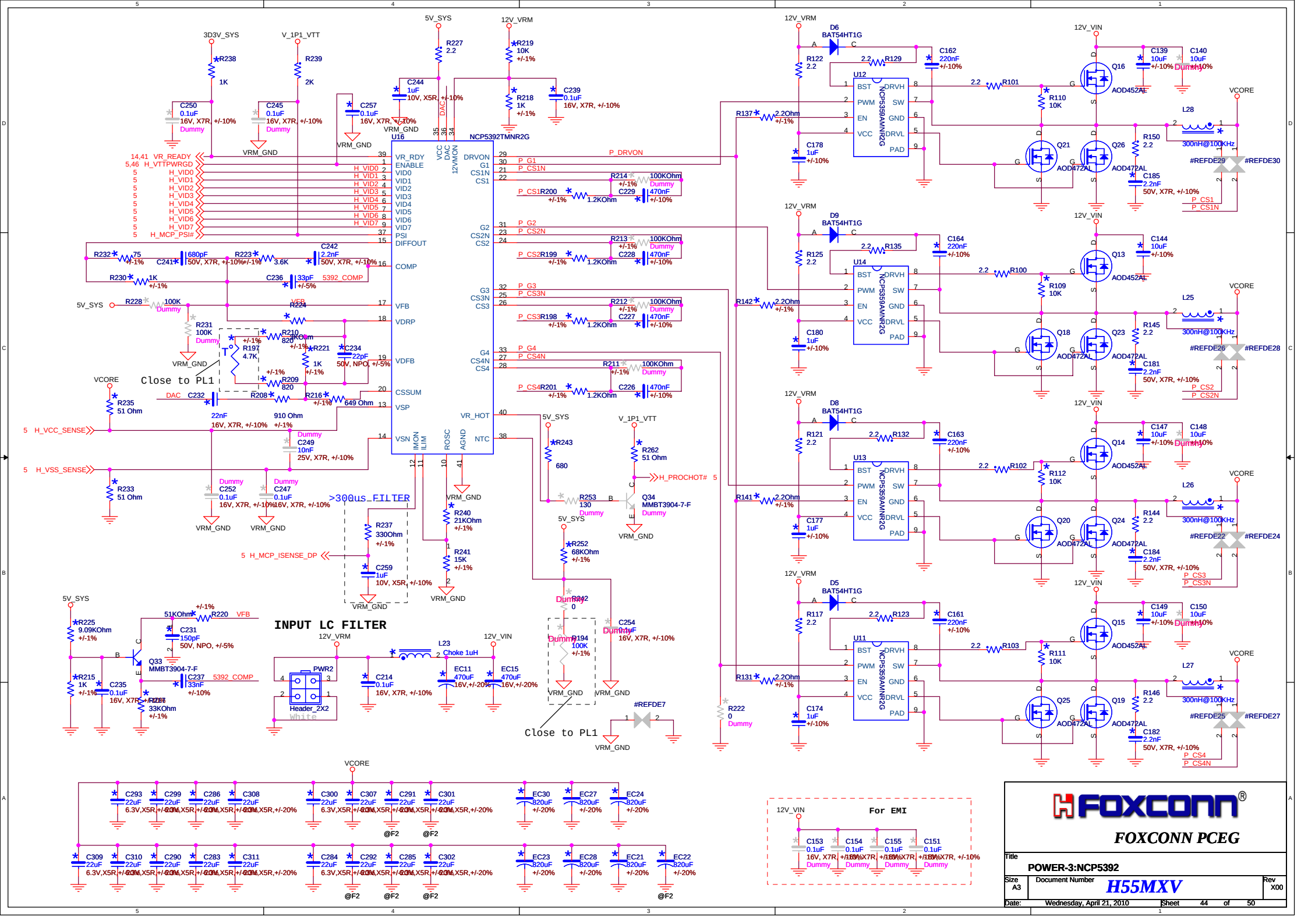
U16
NCP5392TMNR2G
INPUT LC FILTER
Close to PL1
>300us_FILTER
For EMI
FOXCONN PCEG
POWER-3:NCP5392
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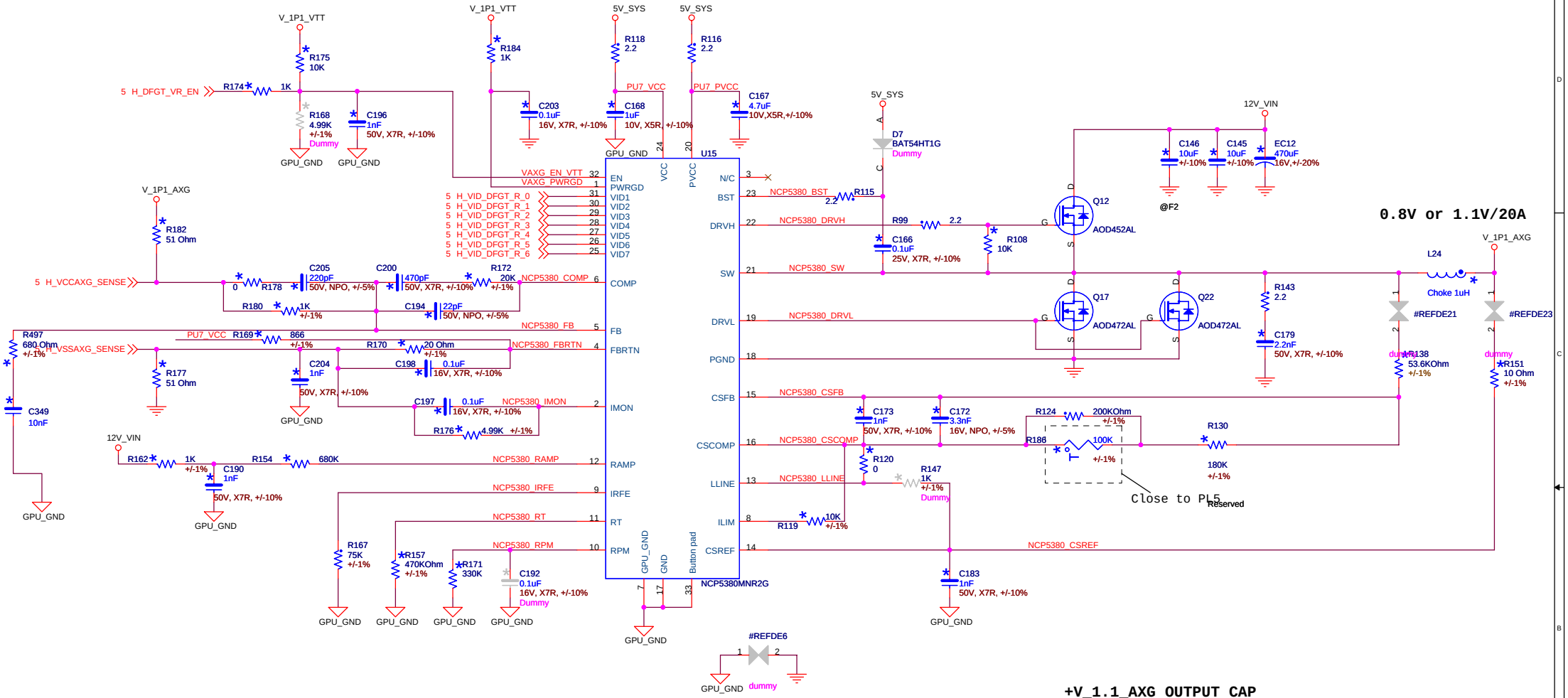
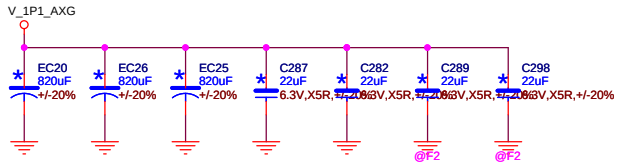
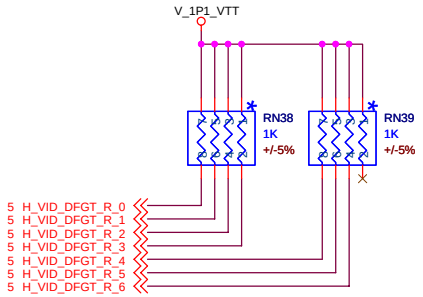
+V_1.1_AXG



+V_1.1_AXG OUTPUT CAP



Intel Demo board 1.0	
H_VID_DFGT_R_0	L
H_VID_DFGT_R_1	Floating
H_VID_DFGT_R_2	Floating
H_VID_DFGT_R_3	Floating
H_VID_DFGT_R_4	Floating
H_VID_DFGT_R_5	Floating
H_VID_DFGT_R_6	H
H_VID_DFGT_R_7	Floating



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FOXCONN PCEG

Title: POWER-4:VAXG NCP5380		
Size: A3	Document Number: H55MXV	Rev: X00
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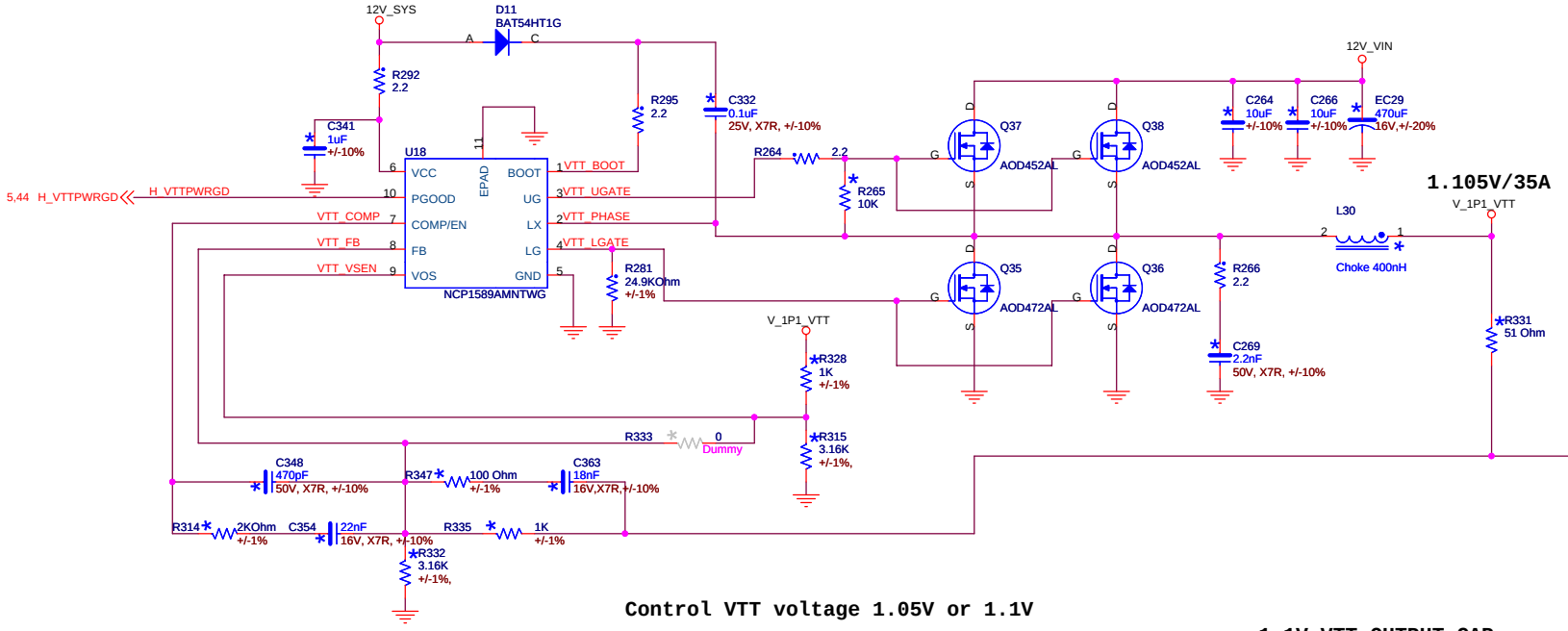
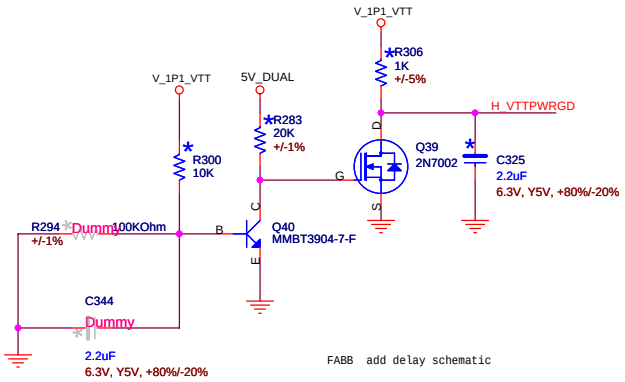
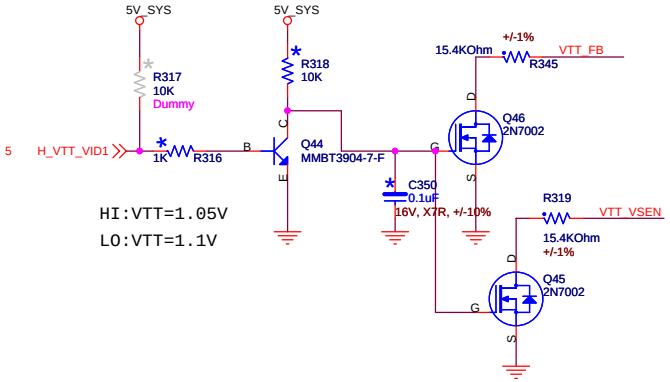
+V_1.1_VTT

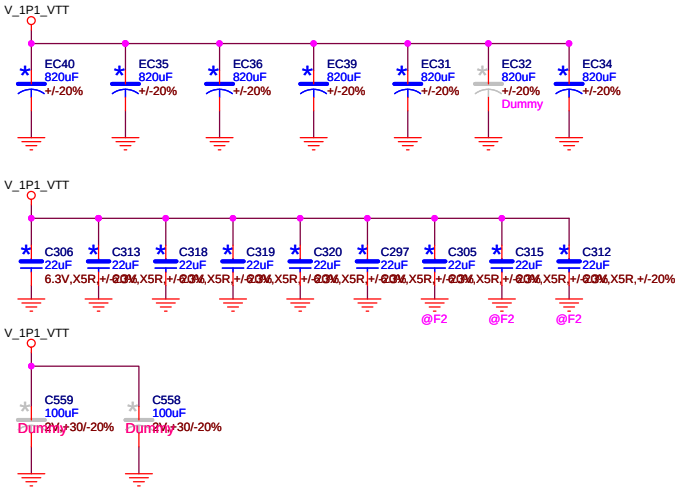


Control VTT voltage 1.05V or 1.1V



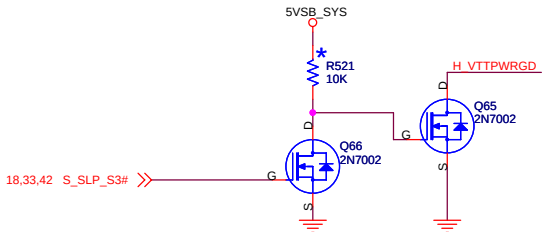


1.1V VTT OUTPUT CAP



+V_1.1_VTT Enable Circuit

+V_1.1_VTT Enable Circuit



Enable Circuit for turn on/off Vcore

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Title	POWER-5:VTT	
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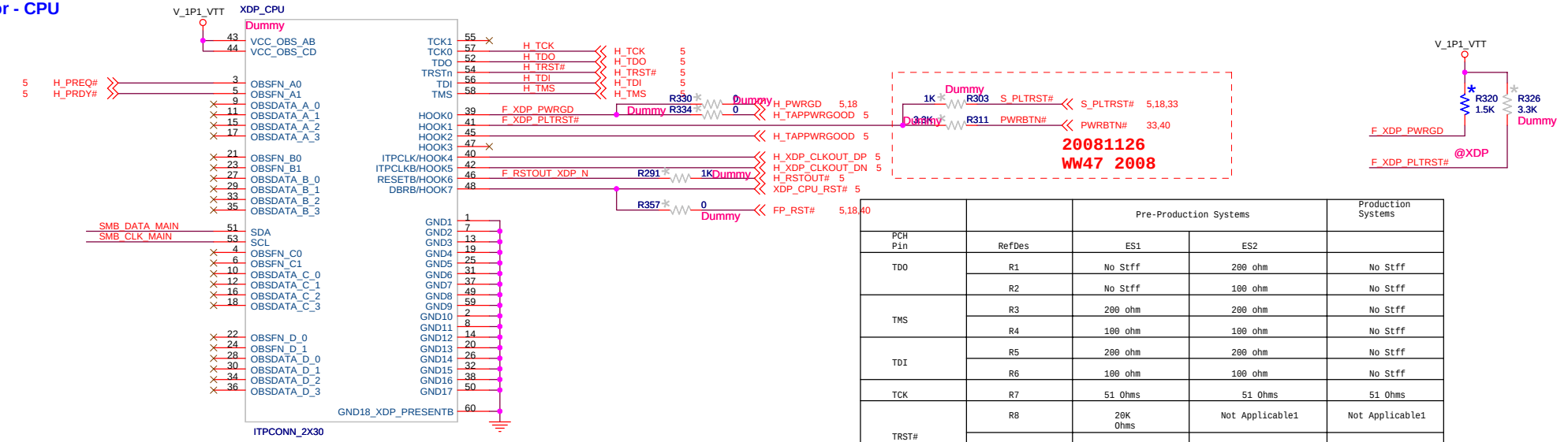
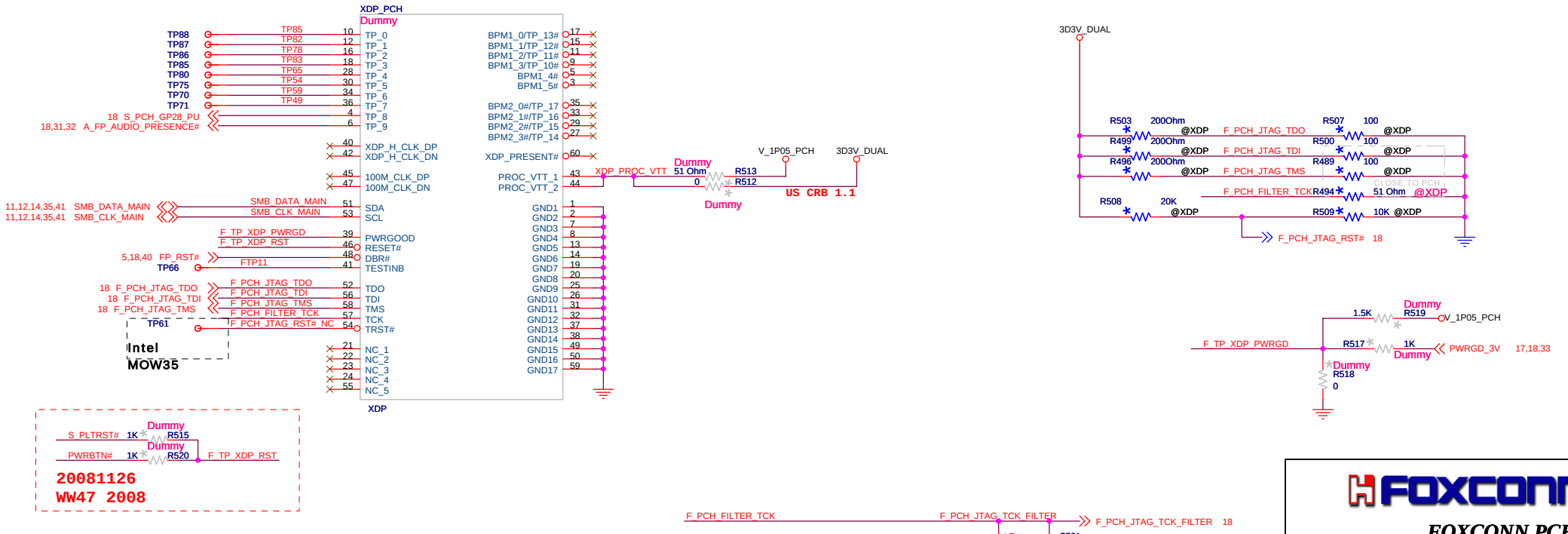
XDP Connector - CPU



PCH Pin	RefDes	Pre-Production Systems ES1	Pre-Production Systems ES2	Production Systems
TDO	R1	No Stff	200 ohm	No Stff
	R2	No Stff	100 ohm	No Stff
TMS	R3	200 ohm	200 ohm	No Stff
	R4	100 ohm	100 ohm	No Stff
TDI	R5	200 ohm	200 ohm	No Stff
	R6	100 ohm	100 ohm	No Stff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable1	Not Applicable1
	R9	10K Ohms	Not Applicable1	Not Applicable1

XDP Connector - PCH



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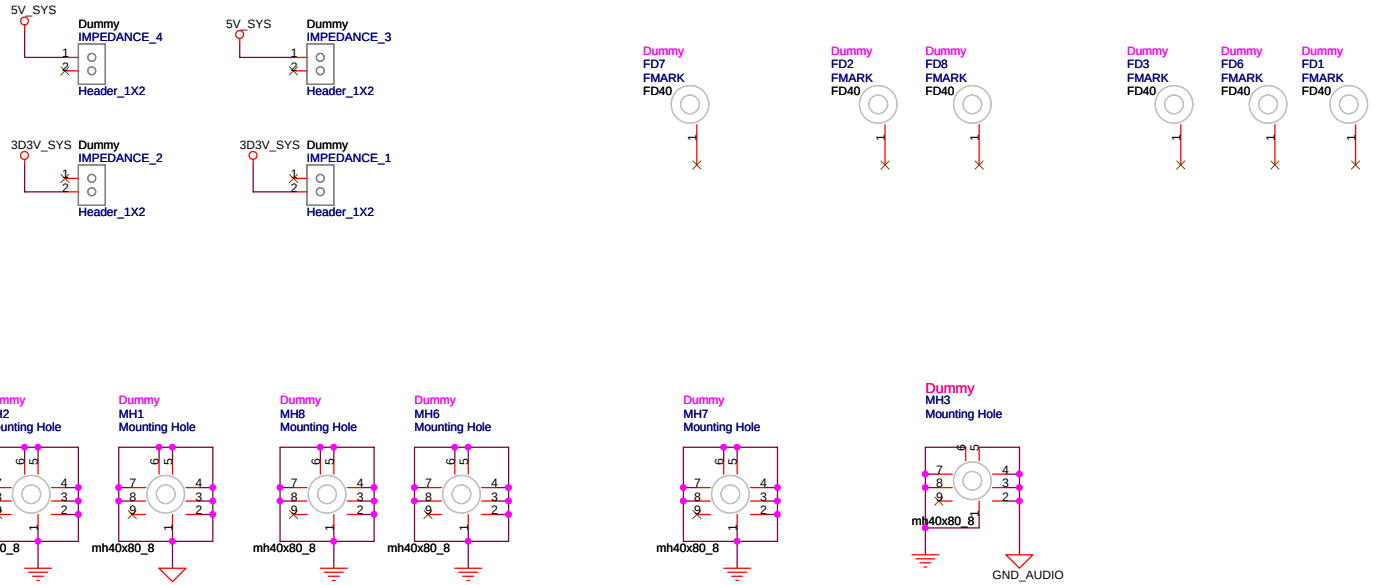

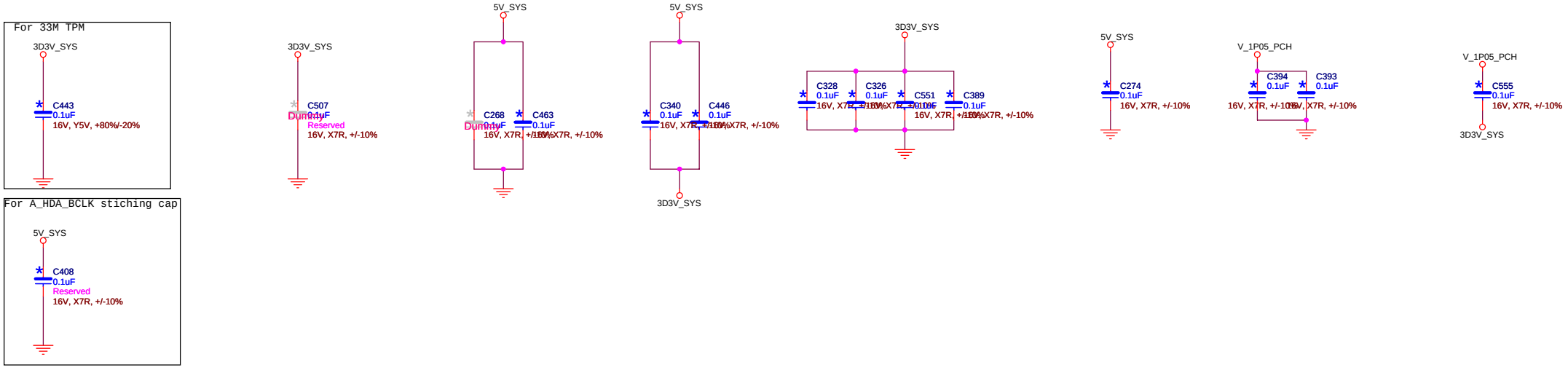

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Title: EMI		
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Ibex peak EDS 1.0

Name	Type	Recommendations	Tolerance	Power Well	Default	Blink Capability	Default	Power Plane	During Reset4	Immediately after Reset4	S0/S1	S3	S4/S5
GPIO0	I/O	Multiplexed with BMBUSY#.	3.3 V	Core	GPI	Yes	TBD						
GPIO1	I/O	Multiplexed with TACH1.	3.3 V	Core	GPI	Yes	TBD						
GPIO2	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GPI	Yes	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO3	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GPI	Yes	TBD						
GPIO4	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GPI	Yes	TBD						
GPIO5	I/OD	Multiplexed with PIRQ[H:E]#	5 V	Core	GPI	Yes	TBD						
GPIO6	I/O	Multiplexed with TACH[3:2].	3.3 V	Core	GPI	Yes	TBD						
GPIO7	I/O	Multiplexed with TACH[3:2].	3.3 V	Core	GPI	Yes	TBD						
GPIO8 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	High	High	Defined	Defined	Defined
GPIO9	I/O	Multiplexed with OC5#	3.3 V	Suspend	Native	Yes	TBD						
GPIO10	I/O	Multiplexed with OC6#	3.3 V	Suspend	Native	Yes	TBD						
GPIO11	I/O	Multiplexed with SMBALERT#.	3.3 V	Suspend	Native	Yes	TBD						
GPIO12	I/O	Multiplexed with LAN_PHY_PWR_CTRL. GPIO / Native functionality controlled via soft strap	3.3 V	Suspend	GPI	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO13	I/O	Multiplexed with HDA_DOCK_RST# (Mobile Only)	3.3 V	Suspend	GPI	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO14	I/O	Multiplexed with OC7#	3.3 V	Suspend	Native	Yes	TBD						
GPIO15 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO16	I/O	Multiplexed with SATA4GP.	3.3 V	Core	GPI	Yes	TBD						
GPIO17	I/O	Multiplexed with TACH0.	3.3 V	Core	GPI	Yes	TBD						
GPIO18	I/O	Multiplexed with PCIECLKRQ1#	3.3 V	Core	Native	Yes	TBD						
GPIO19	I/O	Multiplexed with SATA1GP	3.3 V	Core	GPI	Yes	TBD						
GPIO20	I/O	Multiplexed with PCIECLKRQ2#	3.3 V	Core	Native	Yes	TBD						
GPIO21	I/O	Multiplexed with SATA0GP	3.3 V	Core	GPI	Yes	TBD						
GPIO22	I/O	Multiplexed with SCLOCK	3.3 V	Core	GPI	Yes	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO23	I/O	Multiplexed with LDRQ1#.	3.3 V	Core	Native	Yes	TBD						
GPIO24	I/O	Unmultiplexed NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO25	I/O	Multiplexed with PCIECLKRQ3#	3.3 V	Suspend	Native	Yes	TBD						
GPIO26	I/O	Multiplexed with PCIECLKRQ4#	3.3 V	Suspend	Native	Yes	TBD						
GPIO27 (Strapping)	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO28	I/O	Unmultiplexed	3.3 V	Suspend	GPO	Yes	TBD	Suspend	Low	Low	Defined	Defined	Defined
GPIO29	I/O	Multiplexed with SLP_LAN#	3.3 V	Suspend	GPI	No	TBD	Suspend	High-Z	High-Z	High	Defined	Defined
GPIO30	I/O	Multiplexed with SUS_PWR_DN_ACK Desktop: Cannot be used for native function. Used as GPIO30 only. Mobile: Used as SUS_PWR_DN_ACK or GPIO30	3.3 V	Suspend	GPI	Yes	TBD	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined
GPIO31	I/O	Multiplexed with ACPRESENT	3.3 V	Suspend	GPI	Yes	TBD	Suspend	High-Z (Input)	High-Z (Input)	Defined	Defined	Defined

Ibex peak EDS 1.0

Name	Type	Recommendations	Tolerance	Power Well	Default	Blink Capability	Default	Power Plane	During Reset4	Immediately after Reset4	S0/S1	S3	S4/S5
GPIO32	I/O	Unmultiplexed	3.3 V	Core	GPO	No	TBD	Core	High	High	Defined	Off	Off
GPIO33 (Strapping)	I/O	Multiplexed with HDA_DOCK_EN# (Mobile Only)	3.3 V	Core	GPO	No	TBD	Core	High	High	Defined	Off	Off
GPIO34	I/O	Multiplexed with STP_PCI#	3.3 V	Core	GPI	No	TBD	Core	High-Z (Input)	High-Z (Input)	Defined	Off	Off
GPIO35	I/O	Multiplexed with SATACLKREQ#.	3.3 V	Core	GPO	No	TBD	Core	Low	Low	Defined	Off	Off
GPIO 36	I/O	Multiplexed with SATA2GP.	3.3 V	Core	GPI	No	TBD						
GPIO 37	I/O	Multiplexed with SATA3GP.	3.3 V	Core	GPI	No	TBD						
GPIO38	I/O	Multiplexed with SLOAD.	3.3 V	Core	GPI	No	TBD	Core	High-Z (Input)	High-Z (Input)	Blinking	Off	Off
GPIO39	I/O	Multiplexed with SDATAOUT0.	3.3 V	Core	GPI	No	TBD	Core	High-Z	High-Z	High-Z	Off	Off
GPIO40	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO41	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO42	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO43	I/O	Multiplexed with OC[4:1]#.	3.3 V	Suspend	Native	No	TBD						
GPIO44	I/O	Multiplexed with PCIECLKRQ5#	3.3V	Suspend	Native	No	TBD						
GPIO45	I/O	Multiplexed with PCIECLKRQ6#	3.3V	Suspend	Native	No	TBD						
GPIO46	I/O	Multiplexed with PCIECLKRQ7#	3.3V	Suspend	Native	No	TBD						
GPIO47	I/O	Multiplexed with PEG_A_CLKRQ#	3.3V	Suspend	Native	No	TBD						
GPIO48	I/O	Multiplexed with SDATAOUT1.	3.3 V	Core	GPI	No	TBD	Core	High-Z	High-Z	High-Z	Off	Off
GPIO49	I/O	Multiplexed with SATA5GP	3.3V	Core	GPI	No	TBD						
GPIO50	I/O	Multiplexed with REQ1#.	5.0 V	Core	Native	No	TBD						
GPIO51 (Strapping)	I/O	Multiplexed with GNT1#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO52	I/O	Multiplexed with REQ2#.	5.0 V	Core	Native	No	TBD						
GPIO53	I/O	Multiplexed with GNT2#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO54	I/O	Multiplexed with REQ3#.	5.0 V	Core	Native	No	TBD						
GPIO55	I/O	Multiplexed with GNT3#	3.3 V	Core	Native	No	TBD	Core	High	High	High	Off	Off
GPIO56	I/O	Multiplexed with PEG_B_CLKRQ#	3.3 V	Suspend	Native	No	TBD						
GPIO57	I/O	Unmultiplexed	3.3 V	Suspend	GPI	No	TBD	Suspend	High-Z (Input)	High-Z (Input)	Driven	Driven	Driven
GPIO58	I/O	Multiplexed with SML1CLK	3.3 V	Suspend	Native	No	TBD	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO59	I/O	Multiplexed with OC[0]#	3.3 V	Suspend	Native	No	TBD						
GPIO60	I/O	Multiplexed with SML0ALERT#	3.3 V	Suspend	Native	No	TBD	Suspend	High-Z	High-Z12	Defined	Defined	Defined
GPIO61	I/O	Multiplexed with SUS_STAT#	3.3 V	Suspend	Native	No	TBD	Suspend	Low	High	High	Low	Low
GPIO62	I/O	Multiplexed with SUSCLK	3.3 V	Suspend	Native	No	TBD	Suspend	Low	Running			
GPIO63	I/O	Multiplexed with SLP_S5#	3.3 V	Suspend	Native	No	TBD	Suspend	Low	High	High	High	Low3
GPIO64	I/O	Multiplexed with CLKOUTFLEX0	3.3 V	Core	Native	No	H	Core	Running	Running	Running	Off	Off
GPIO65 (Strapping)	I/O	Multiplexed with CLKOUTFLEX1	3.3 V	Core	Native	No	H	Core	Running	Running	Running	Off	Off
GPIO66	I/O	Multiplexed with CLKOUTFLEX2	3.3 V	Core	Native	No	L	Core	Running	Running	Running	Off	Off
GPIO67	I/O	Multiplexed with CLKOUTFLEX3	3.3 V	Core	Native	No	L	Core	Running	Running	Running	Off	Off
GPIO72	I/O	Mobile: Multiplexed with BATLOW#. Desktop: Unmultiplexed	3.3 V	Suspend	Native	No	H	Suspend	High-Z (Input)	High-Z (Input)	Driven	Driven	Driven
GPIO73	I/O	Multiplexed with PCIECLKRQ0#	3.3 V	Suspend	Native	No	H						
GPIO74	I/O	Multiplexed with SML1ALERT#	3.3 V	Suspend	Native	No	H	Suspend	High-Z	High-Z	Defined	Defined	Defined
GPIO75	I/O	Multiplexed with SML1DATA	3.3 V	Suspend	Native	No	H	Suspend	High-Z	High-Z	Defined	Defined	Defined

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Title	GPIO PIN		
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Changelist:

1. LAN Power
2. change VGA HYSN and VYSN's buffer package type
3.change clr header/s pin definition
4. change IR/CIR to CIR/change PCIE_1X and COM2 'S Sybol name
5. change EC64 , EC65 and C371'S footprint
6. add C503 near Q52
7.connect SIO susc pin to SLP_S4#

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Title: DDR3 CONN:CHB_2		
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