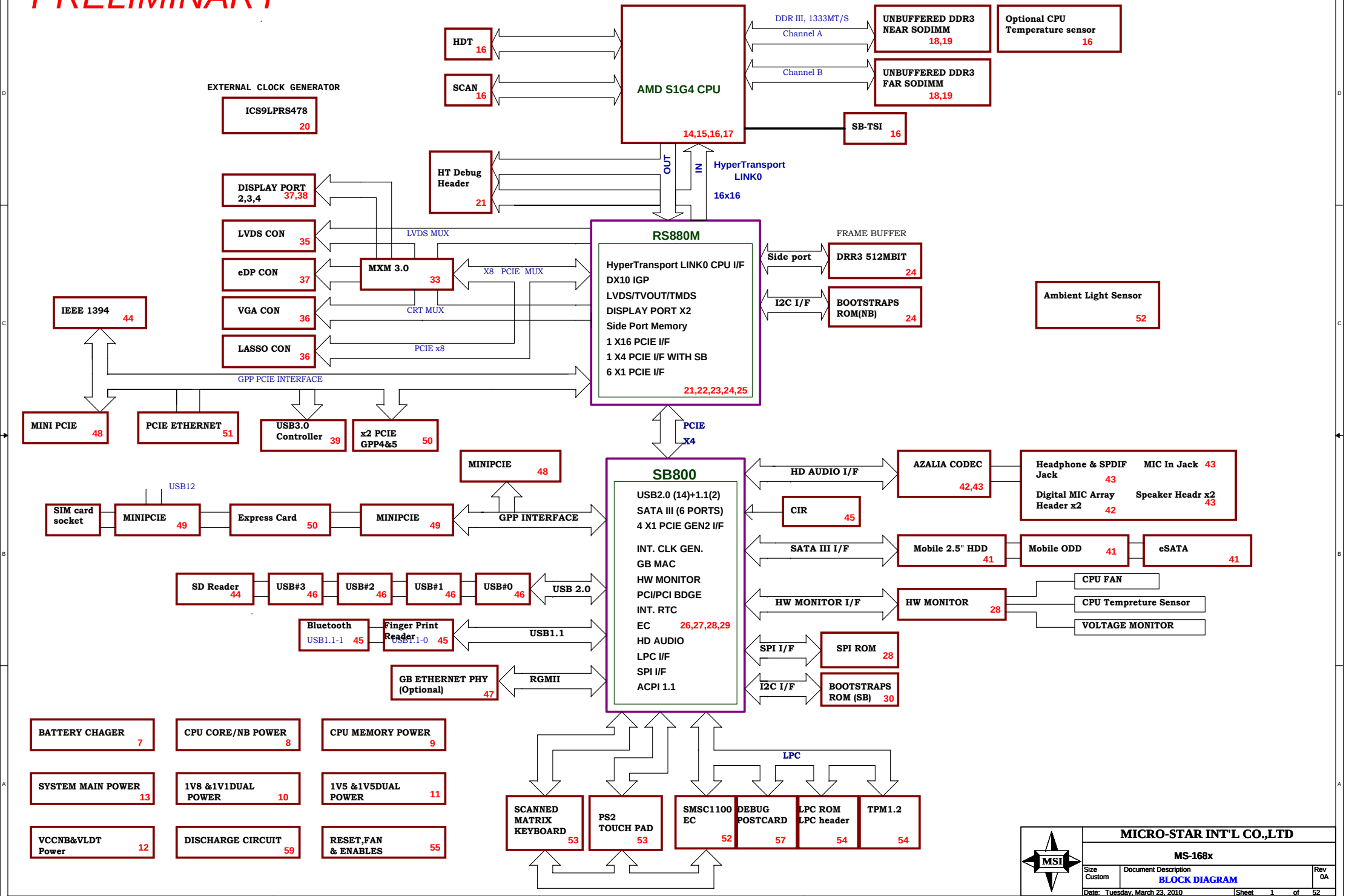
PRELIMINARY

# GUAM S1G4 SCHEMATIC DESIGN




MICRO-STAR INT'L CO.,LTD

MS-168x

| Size | Document Description | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 0A |

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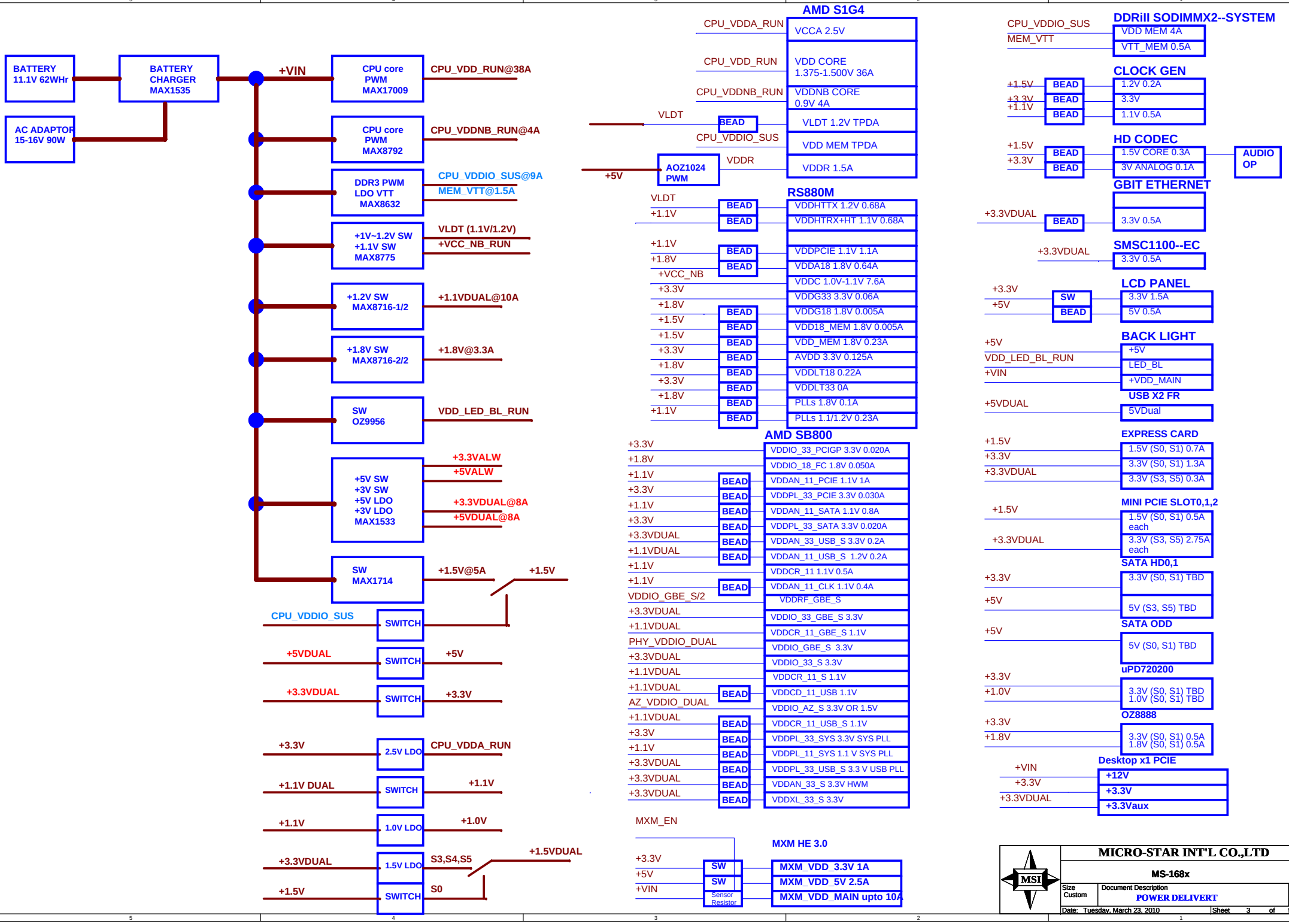
BATTERY 11.1V 62WHr
BATTERY CHARGER MAX1535
AC ADAPTOR 15-16V 90W
+VIN
CPU core PWM MAX17009
CPU_VDD_RUN@38A
CPU core PWM MAX8792
CPU_VDDNB_RUN@4A
DDR3 PWM LDO VTT MAX8632
CPU_VDDIO_SUS@9A
MEM_VTT@1.5A
+1V~1.2V SW +1.1V SW MAX8775
VLDT (1.1V/1.2V)
+VCC_NB_RUN
+1.2V SW MAX8716-1/2
+1.1VDUAL@10A
+1.8V SW MAX8716-2/2
+1.8V@3.3A
SW OZ9956
VDD_LED_BL_RUN
+5V SW +3V SW +5V LDO +3V LDO MAX1533
+3.3VALW
+5VALW
+3.3VDUAL@8A
+5VDUAL@8A
SW MAX1714
+1.5V@5A
+1.5V
CPU_VDDIO_SUS
SWITCH
+5VDUAL
SWITCH
+5V
+3.3VDUAL
SWITCH
+3.3V
+3.3V
2.5V LDO
CPU_VDDA_RUN
+1.1V DUAL
SWITCH
+1.1V
+1.1V
1.0V LDO
+1.0V
+3.3VDUAL
1.5V LDO
S3,S4,S5
+1.5VDUAL
+1.5V
SWITCH
S0
AMD S1G4
CPU_VDDA_RUN
VCCA 2.5V
CPU_VDD_RUN
VDD CORE 1.375-1.500V 36A
CPU_VDDNB_RUN
VDDNB CORE 0.9V 4A
VLDT
BEAD
VLDT 1.2V TPDA
CPU_VDDIO_SUS
VDD MEM TPDA
+5V
AOZ1024 PWM
VDDR
VDDR 1.5A
RS880M
VLDT
+1.1V
BEAD
BEAD
VDDHTTX 1.2V 0.68A
VDDHTRX+HT 1.1V 0.68A
+1.1V
+1.8V
+VCC_NB
+3.3V
+1.8V
+1.5V
+1.5V
+3.3V
+1.8V
+3.3V
+1.8V
+1.1V
BEAD
VDDPCIE 1.1V 1.1A
VDDA18 1.8V 0.64A
VDDC 1.0V-1.1V 7.6A
VDDG33 3.3V 0.06A
VDDG18 1.8V 0.005A
VDD18_MEM 1.8V 0.005A
VDD_MEM 1.8V 0.23A
AVDD 3.3V 0.125A
VDDLT18 0.22A
VDDLT33 0A
PLLs 1.8V 0.1A
PLLs 1.1/1.2V 0.23A
AMD SB800
+3.3V
+1.8V
+1.1V
+3.3V
+1.1V
+3.3V
+3.3VDUAL
+1.1VDUAL
+1.1V
+1.1V
VDDIO_GBE_S/2
+3.3VDUAL
+1.1VDUAL
PHY_VDDIO_DUAL
+3.3VDUAL
+1.1VDUAL
+1.1VDUAL
AZ_VDDIO_DUAL
+1.1VDUAL
+3.3V
+1.1V
+3.3VDUAL
+3.3VDUAL
+3.3VDUAL
BEAD
VDDIO_33_PCIGP 3.3V 0.020A
VDDIO_18_FC 1.8V 0.050A
VDDAN_11_PCIE 1.1V 1A
VDDPL_33_PCIE 3.3V 0.030A
VDDAN_11_SATA 1.1V 0.8A
VDDPL_33_SATA 3.3V 0.020A
VDDAN_33_USB_S 3.3V 0.2A
VDDAN_11_USB_S 1.2V 0.2A
VDDCR_11 1.1V 0.5A
VDDAN_11_CLK 1.1V 0.4A
VDDRF_GBE_S
VDDIO_33_GBE_S 3.3V
VDDCR_11_GBE_S 1.1V
VDDIO_GBE_S 3.3V
VDDIO_33_S 3.3V
VDDCR_11_S 1.1V
VDDCD_11_USB 1.1V
VDDIO_AZ_S 3.3V OR 1.5V
VDDCR_11_USB_S 1.1V
VDDPL_33_SYS 3.3V SYS PLL
VDDPL_11_SYS 1.1 V SYS PLL
VDDPL_33_USB_S 3.3 V USB PLL
VDDAN_33_S 3.3V HWM
VDDXL_33_S 3.3V
MXM_EN
MXM HE 3.0
+3.3V
+5V
+VIN
SW
SW
Sensor Resistor
MXM_VDD_3.3V 1A
MXM_VDD_5V 2.5A
MXM_VDD_MAIN upto 10A
CPU_VDDIO_SUS
MEM_VTT
DDRill SODIMMX2--SYSTEM
VDD MEM 4A
VTT_MEM 0.5A
CLOCK GEN
+1.5V
+3.3V
+1.1V
BEAD
BEAD
BEAD
1.2V 0.2A
3.3V
1.1V 0.5A
HD CODEC
+1.5V
+3.3V
BEAD
BEAD
1.5V CORE 0.3A
3V ANALOG 0.1A
AUDIO OP
GBIT ETHERNET
+3.3VDUAL
BEAD
3.3V 0.5A
SMSC1100--EC
+3.3VDUAL
3.3V 0.5A
LCD PANEL
+3.3V
+5V
SW
BEAD
3.3V 1.5A
5V 0.5A
BACK LIGHT
+5V
VDD_LED_BL_RUN
+VIN
+5V
LED_BL
+VDD_MAIN
USB X2 FR
+5VDUAL
5VDual
EXPRESS CARD
+1.5V
+3.3V
+3.3VDUAL
1.5V (S0, S1) 0.7A
3.3V (S0, S1) 1.3A
3.3V (S3, S5) 0.3A
MINI PCIE SLOT0,1,2
+1.5V
+3.3VDUAL
1.5V (S0, S1) 0.5A each
3.3V (S3, S5) 2.75A each
SATA HD0,1
+3.3V
+5V
3.3V (S0, S1) TBD
5V (S3, S5) TBD
SATA ODD
+5V
5V (S0, S1) TBD
uPD720200
+3.3V
+1.0V
3.3V (S0, S1) TBD
1.0V (S0, S1) TBD
OZ8888
+3.3V
+1.8V
3.3V (S0, S1) 0.5A
1.8V (S0, S1) 0.5A
Desktop x1 PCIE
+VIN
+3.3V
+3.3VDUAL
+12V
+3.3V
+3.3Vaux
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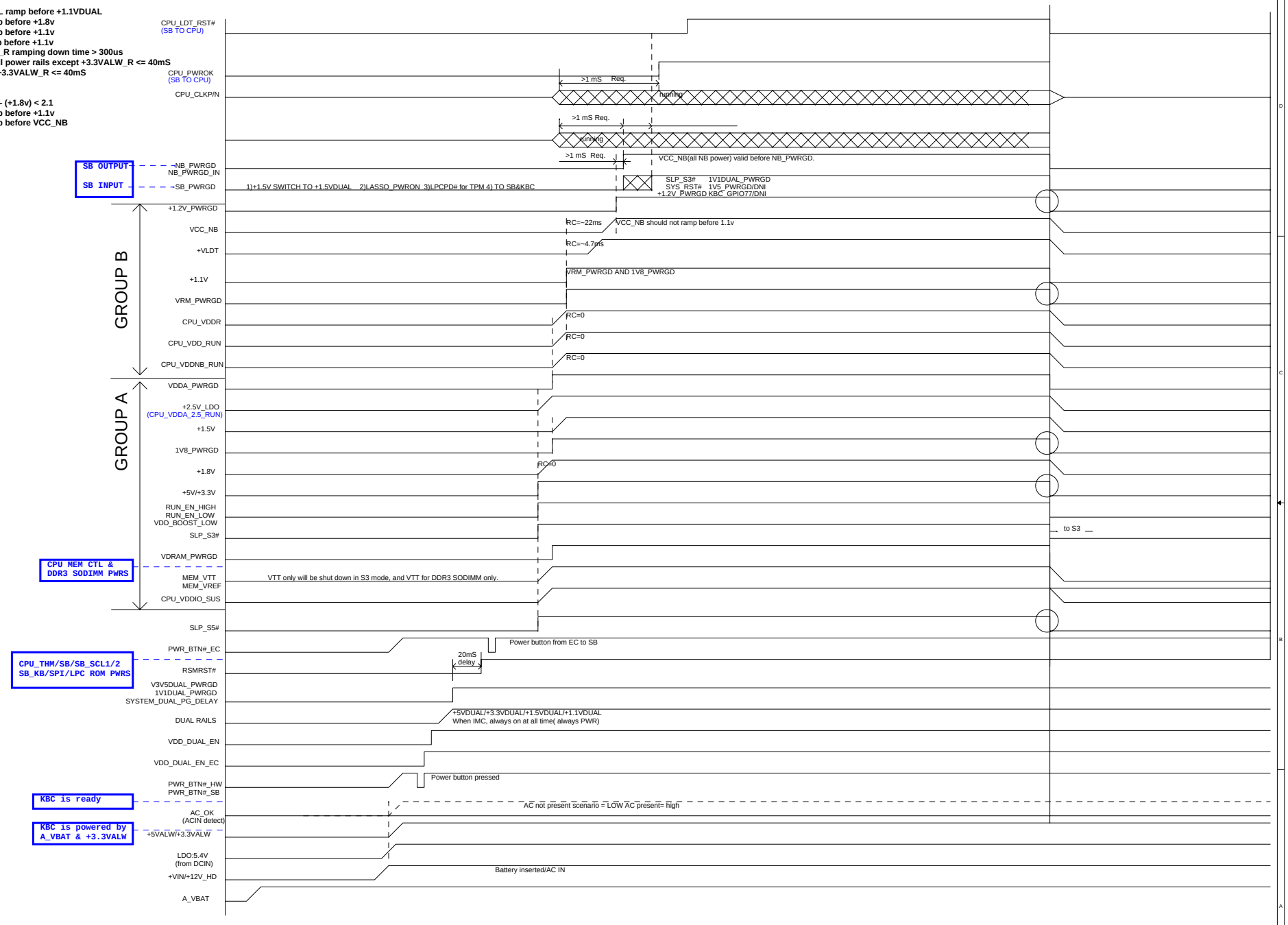
**Power on Sequence required:**

**SB800:**
**1, +3.3VDUAL ramp before +1.1VDUAL**
**2, +3.3V ramp before +1.8v**
**3, +1.8V ramp before +1.1v**
**4, +3.3v ramp before +1.1v**
**5, +3.3VALW_R ramping down time > 300us**
**6, 50uS <= All power rails except +3.3VALW_R <= 40mS**
**7, 100uS <= +3.3VALW_R <= 40mS**

**RS880:**
**1, 0 <(+3.3V) - (+1.8v) < 2.1**
**2, +1.8V ramp before +1.1v**
**3. +1.1V ramp before VCC_NB**

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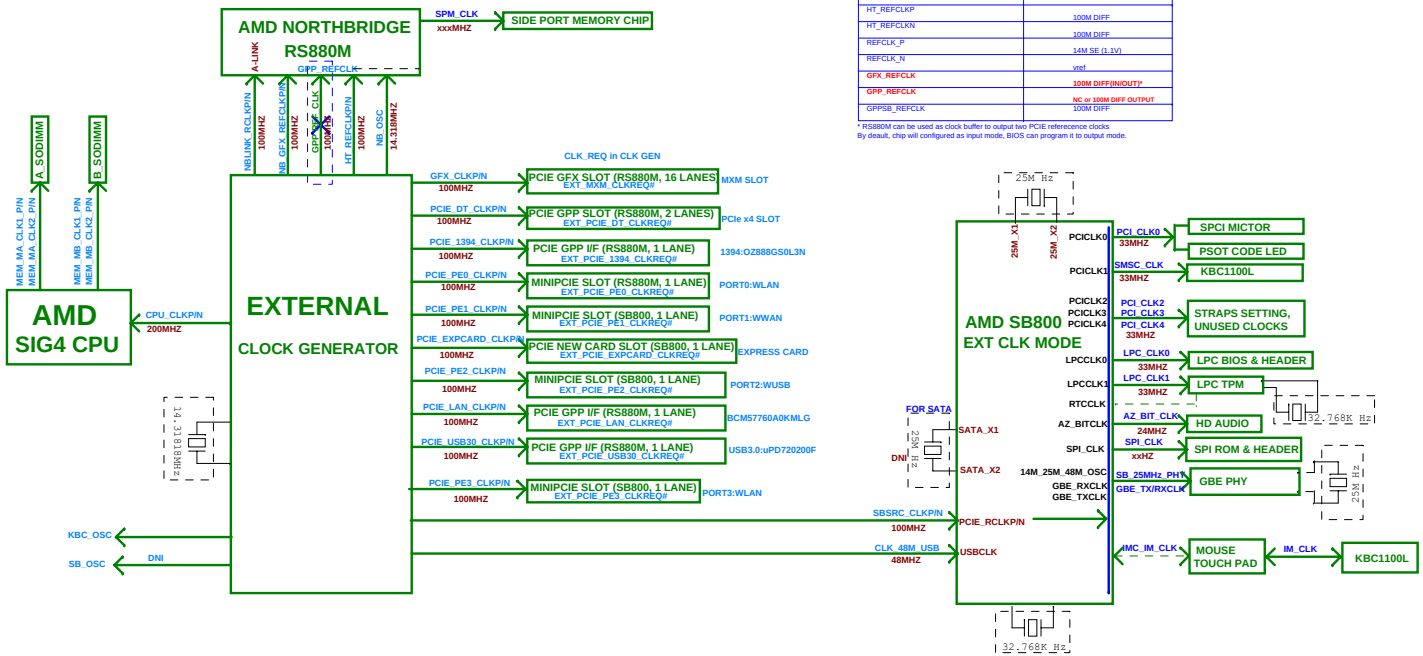
# EXTERNAL CLOCK MODE

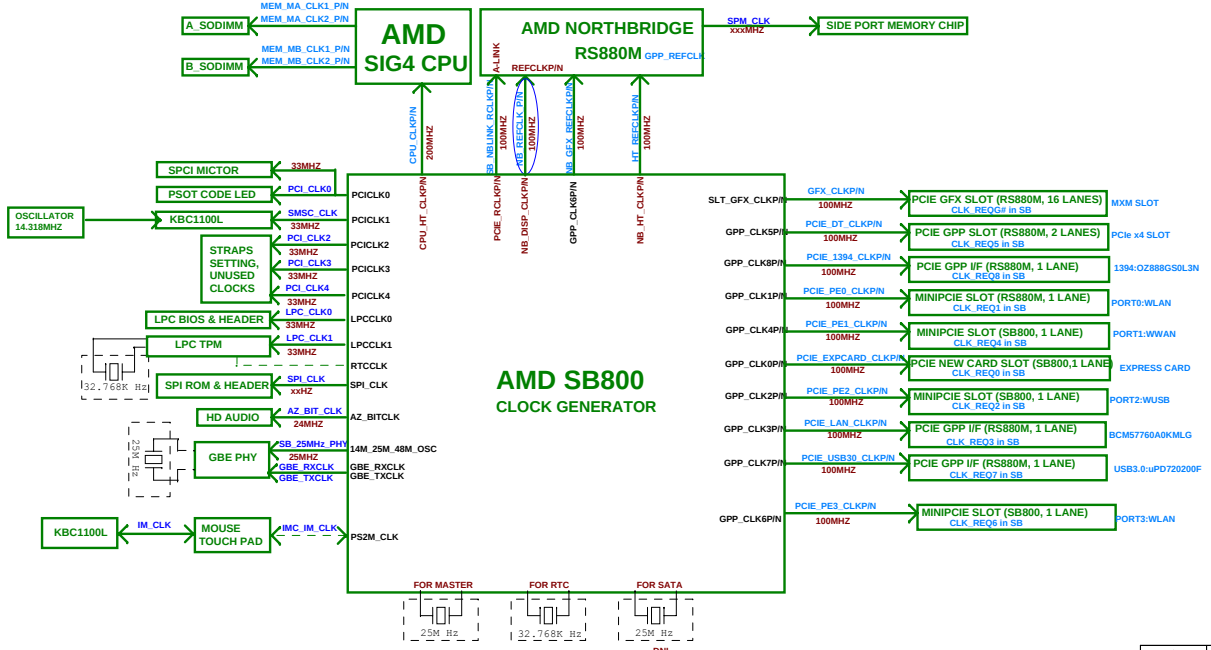



NB CLOCK INPUT TABLE

| NB CLOCKS | RS880M |
|---|---|
| HT_REFCLKP | 100M DIFF |
| HT_REFCLKN | 100M DIFF |
| REFCLK_P | 14M SE (1.1V) |
| REFCLK_N | vref |
| GFX_REFCLK | 100M DIFF(IN/OUT)* |
| GPP_REFCLK | NC or 100M DIFF OUTPUT |
| GPPSB_REFCLK | 100M DIFF |

* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

# INTERNAL CLOCK MODE

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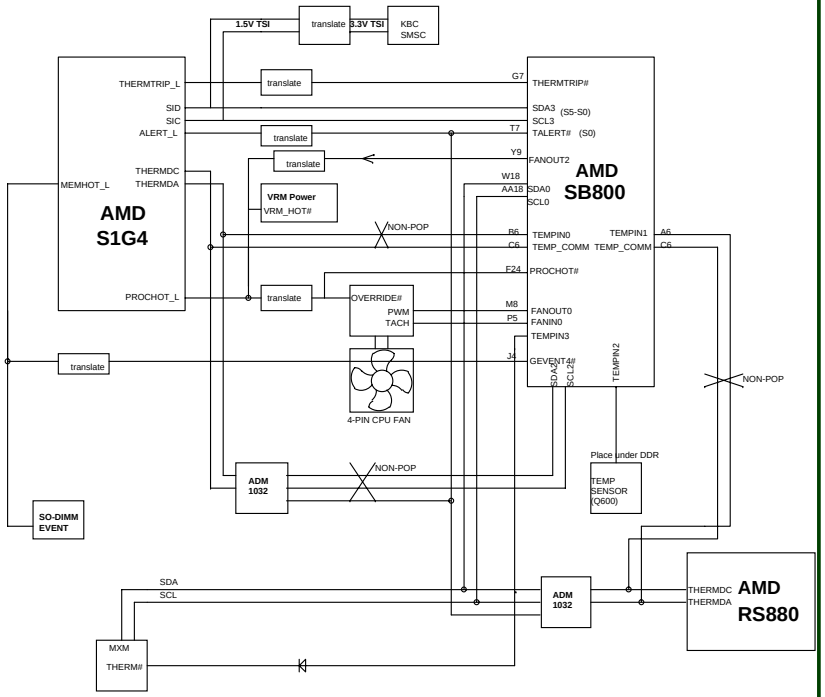
# Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)

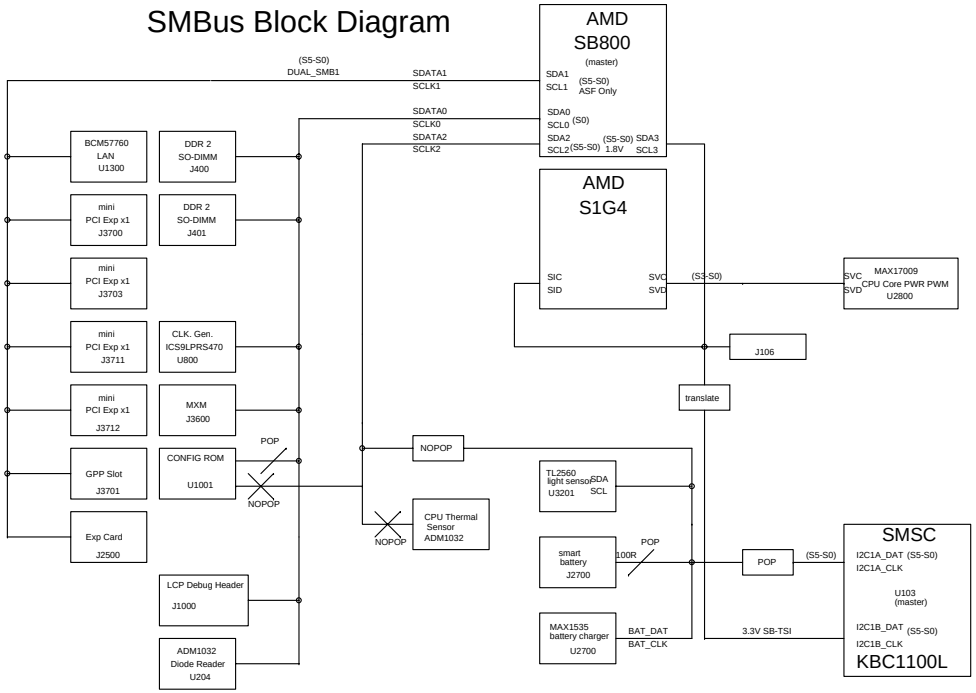



Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

# Power State / Voltage Rail Activity Summary

| Global System State | Sleep State | Processor Power State | Description | | RTC | ALW | DUAL | SUS | RUN |
|---|---|---|---|---|---|---|---|---|---|
| G0 | S0 | C0 | Running | | ON | ON | ON | ON | ON |
| G0 | S0 | C0 | Running | P-state transitions under OS control | ON | ON | ON | ON | ON |
| G0 | S0 | C1 | | Halt | ON | ON | ON | ON | ON |
| G0 | S0 | C2 | | Stop grant, caches snoopable | ON | ON | ON | ON | ON |
| G0 | S0 | C3 | | TBD | ON | ON | ON | ON | ON |
| G0 | S0 | c4 | | TBD | ON | ON | ON | ON | ON |
| G1 | S1 | OFF | Sleeping | Powered on suspend | ON | ON | ON | ON | ON |
| G1 | S3 | OFF | | Suspend to RAM | ON | ON | ON | ON | OFF |
| G2 | S4 | OFF | | Suspend to diskON | ON | ON | ON | OFF | OFF |
| G2 | S5 | OFF | Soft-off | | ON | ON | ON | OFF | OFF |
| G2/G3 | S5 LOW | OFF | Battery IN | | ON | ON | ON | OFF | OFF |
| G3 | | OFF | Mechanical off | | ON | OFF | OFF | OFF | OFF |

# SMBus Block Diagram




## Group Name Description

INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

| | |
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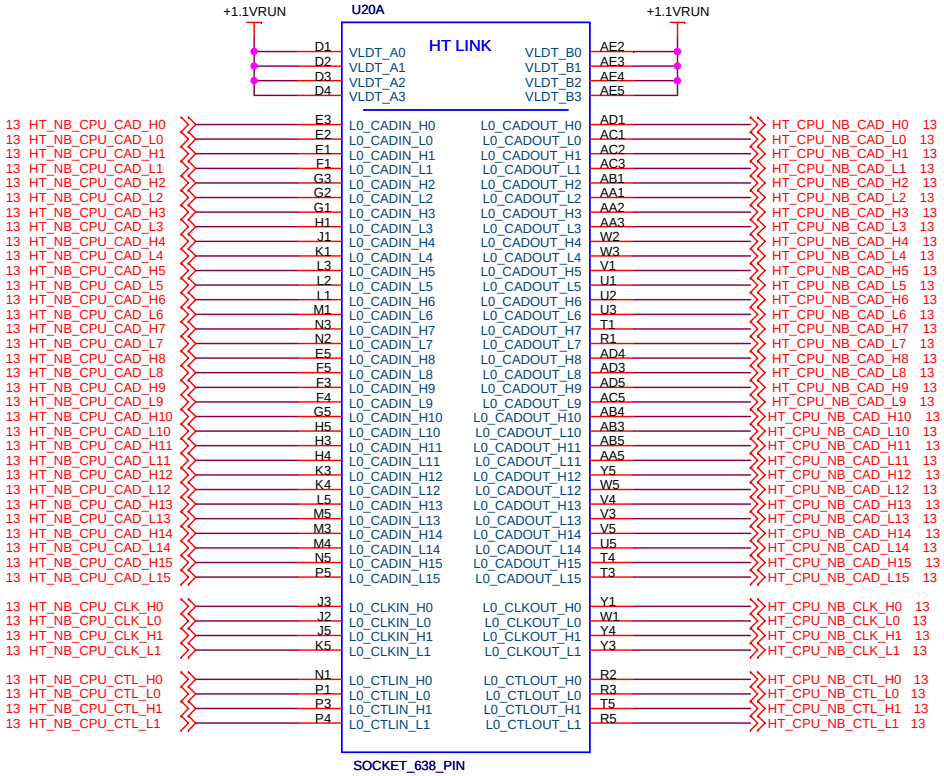
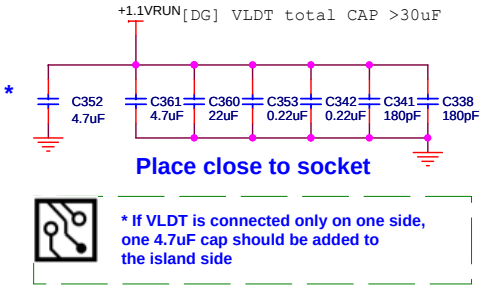
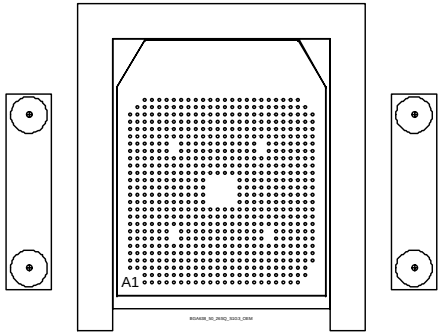



[CheckList] If the I/O device does not support the CTLIN1 pair, pull up 51ohm




[ChckList] Can change 22u*1/4.7u*2 to 10u*3

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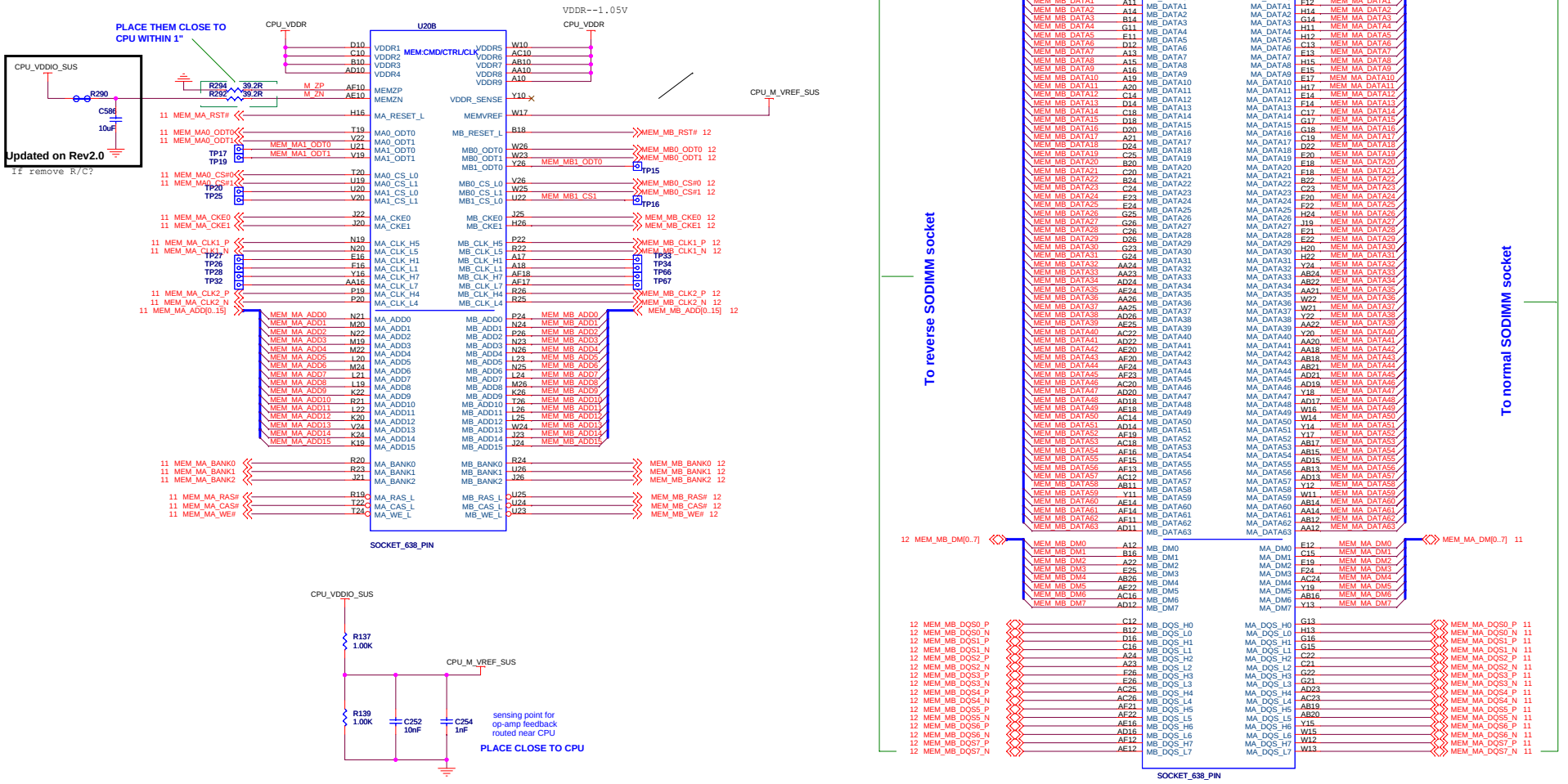
# Processor Memory Interface

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Keep net PWRGD, LDT_STOP#, LDT_RST# no stub

+1.5VRUN
R145 300R
18 CPU_PWRGD — R147 — PWRGD

+1.5VRUN
R138 300R
15,18 CPU_LDT_STOP# — R134 — LDT_STOP#

+1.5VRUN
R141 300R
18 CPU_LDT_RST# — R140 — LDT_RST#
C246 X_180pF

[DG] BEAD: R<40mΩ(about 35), I>500mA
[ChckList] VDDA:100u*1/4.7u*1/0.22u0603*1/3300p0603*1

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

+VDDA
L15 26R_600mA
C282 22uF
C326 4.7UF
C314 220nF
C328 3.3NF
CPU_VDDA_RUN

200MHz
34 CPU_CLKP
34 CPU_CLKN
C596 3.9NF
C597 3.9NF
R296 169R
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
CPU_CLKIN_SC_P
CPU_CLKIN_SC_N

CPU_LDT_REQ# is NOT needed by S1G4
LDT_RST#
PWRGD
LDT_STOP#

19 CPU_SIC
19 CPU_SID
CPU_SIC
CPU_SID
CPU_ALERT
place them to CPU within 1.5"

+1.1VRUN
R174 44.2R
R175 44.2R
CPU_HTREF0
CPU_HTREF1

47 CPU_VDD0_RUN_FB_H
47 CPU_VDD0_RUN_FB_L

[CheckList} VDD1_FB_H/L NC if not use

U20D
VDDA1, VDDA2
CLKIN_H, CLKIN_L
RESET_L, PWROK, LDTSTOP_L, LDTREQ_L
SIC, SID, ALERT_L
HT_REF0, HT_REF1
VDD0_FB_H, VDD0_FB_L
VDD1_FB_H, VDD1_FB_L
DBRDY, TMS, TCK, TRST_L, TDI
TEST23, TEST18, TEST19, TEST25_H, TEST25_L, TEST21, TEST20, TEST24, TEST22, TEST12, TEST27, TEST9, TEST6
RSVD1, RSVD2, RSVD3, RSVD4, RSVD5
VSS, RSVD11
SVC, SVD
THERMTRIP_L, PROCHOT_L, MEMHOT_L
THERMDC, THERMDA
VDDIO_FB_H, VDDIO_FB_L
VDDNB_FB_H, VDDNB_FB_L
DBREQ_L, TDO
TEST28_H, TEST28_L, TEST17, TEST16, TEST15, TEST14, TEST7, TEST10, TEST8, TEST29_H, TEST29_L
RSVD10, RSVD9, RSVD8, RSVD7, RSVD6
SOCKET_638_PIN

CPU_SVC_R
CPU_SVD_R
CPU_THERMTRIP# VDDIO
CPU_VDDIO_SUS
R177 1K
R170 300R
R171 10K Q16
N-MMBT3904_NL_SOT23
R165 X_0R
CPU_THERMTRIP# 19
CPU_PROCHOT# 18
VRD_PROCHOT# 47

S1G4 does not support MEMHOT_L
Thermdc and Thermda should be routed away to VRM, crystal, etc. Customer should follow the MBDG.
However, Guam is using TSI so this does not applies to Guam.

[CheckList] VDDIO_FB_H/L NC if not use
TP40
CPU_VDDNB_RUN_FB_H 47
TP44

CPU_DBRDY
TP41 CPU_TMS
TP68 CPU_TCK
TP69 CPU_TRST#
TP70 CPU_TDI
CPU_DBREQ#
CPU_TDO
TP71

route as differential as short as possible testpoint under package
TP43 CPU_TEST28_H_PLLCHRZ_P
TP42 CPU_TEST28_L_PLLCHRZ_N
TP45 CPU_TEST16_BP2
CPU_TEST15_BP1
CPU_TEST14_BP0
For debug only

CPU_TEST23_TSTUPD
CPU_TEST18_PLLTEST1
CPU_TEST19_PLLTEST0
CPU_TEST25_H_BYPASSCLK_H
CPU_TEST25_L_BYPASSCLK_L
CPU_TEST21_SCANEN
CPU_TEST20_SCANCLK2
CPU_TEST24_SCANCLK1
CPU_TEST22_SCANSHIFTEN
CPU_TEST12_SCANSHIFTENB
CPU_TEST27_SINGLECHAIN
CPU_TEST9_ANALOGIN

R291 510R
R293 510R
R191

TP47 CPU_TEST7_ANALOG_T
CPU_TEST10_ANALOGOUT
TP46 CPU_TEST8_DIG_T

CPU_TEST29_H_FBCLKOUT_P
CPU_TEST29_L_FBCLKOUT_N
R167 80.6R
Route as 80ohm, diff
R184's value is TBD.

TEST23--R358 NC in ref schematic?

CPU_VDDIO_SUS
R198 1K
R199 2.2K
4.7K R190
Q19
CPU_SID
N-MMBT3904_NL_SOT23
SMB_THRMCPU_DATA 30
D13 BAS40WS

R197 1K
R195 2.2K
4.7K R189
Q18
CPU_SIC
N-MMBT3904_NL_SOT23
SMB_THRMCPU_CLK 30
D14 BAS40WS

R180 1K
R184 10K
4.7K R185
Q17
CPU_ALERT
N-MMBT3904_NL_SOT23
SMBALERT# 19,30

THERMDA/THERMDC is not used;
CPU thermal control is based on TSI by default.

RSVD/TEST6/7/8/10/28--NC
TEST14/15/16/17--Test Point
TEST23/25--Test Point
TEST12/18~24--Pull down 1Kohn to VSS
TEST27 pull-up 1Kohm to VDDIO
TEST25_H pull-up 510ohm to VDDIO
TEST25_L pull-down 510ohm to VSS
TEST9 is tied to VSS
There is a (±1%) differential termination between TEST29_L and TEST29_H
CPU_DBRDY not need pull down in checklist

CPU_VDDIO_SUS
CPU_DBREQ# R156 300R
CPU_TEST27_SINGLECHAIN R303 1K
CPU_TEST21_SCANEN R306 1K
CPU_TEST20_SCANCLK2 R307 1K
CPU_TEST24_SCANCLK1 R308 1K
CPU_TEST22_SCANSHIFTEN R304 1K
CPU_TEST12_SCANSHIFTENB R305 1K
CPU_TEST15_BP1 R176 X_300R
CPU_TEST14_BP0 R160 X_300R
CPU_TEST18_PLLTEST1 R159 1K
CPU_TEST19_PLLTEST0 R135 1K
CPU_TEST23_TSTUPD R173 1K
CPU_DBRDY R163 X_300R
CPU_TEST10_ANALOGOUT R161 X_300R +1.1VRUN

R147, R152 is installed ONLY when SCAN is enabled
R215, R185 internal ONLY
R162 is TBD

[DateSheet] Internal Termination:Systems that do not require use of these pins can rely on the internal termination to pull the signals to the proper inactive state. When these pins are used, they must not be driven with open-drain outputs,otherwise additional termination is required

[DateSheet] Internal pull_up 870~1250 ohm:
SSA[2;0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

[DateSheet] Internal pull_down 870~1250 ohm:
TEST12, TEST[20:24]

+1.5VRUN
10K R166
10K R202
2.2K R149
PWRGD pull-up in 2 times (R187 and R163)?

CPU_SVC_R
CPU_SVD_R
PWRGD
R164
R201
R150
CPU_SVC 47
CPU_SVD 47
CPU_PWRGD_SVID_REG 47

Internal pull_up 870~1250 ohm:
SSA[2;0], TCK, TMS, TRST_L, TDI, DBREQ_L, PLATFORM_TYPE, TEST27

| SVC | SVD | BOOT VOLTAGE(VDD) | |
|---|---|---|---|
| | | (CPUVRM_PRO# = VCC/GND) | (CPUVRM_PRO# = OPEN) |
| 0 | 0 | 1.1 | 1.1 |
| 0 | 1 | 1.0 | 1.2 |
| 1 | 0 | 0.9 | 1.0 |
| 1 | 1 | 0.8 | 0.8 |

VID OVERIDE TABLE (VDD)

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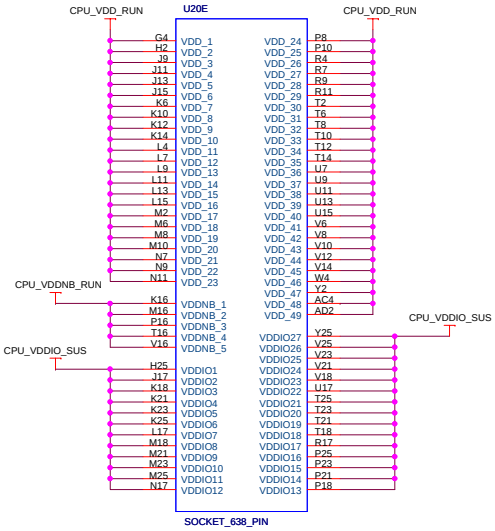
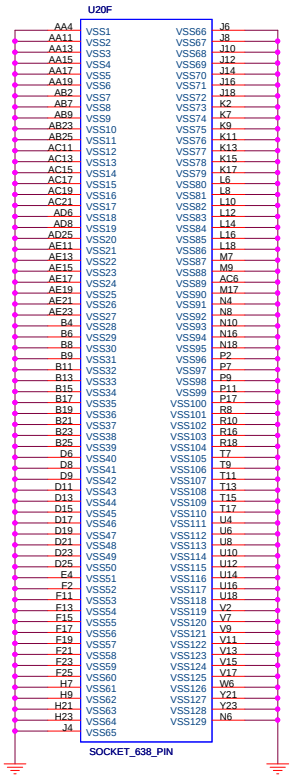
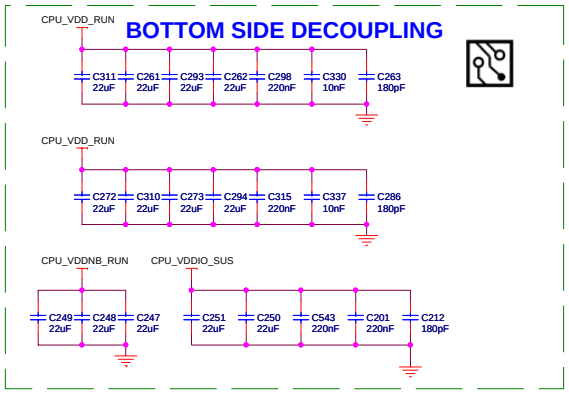
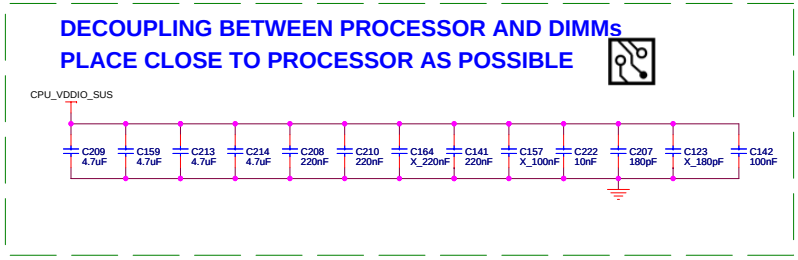


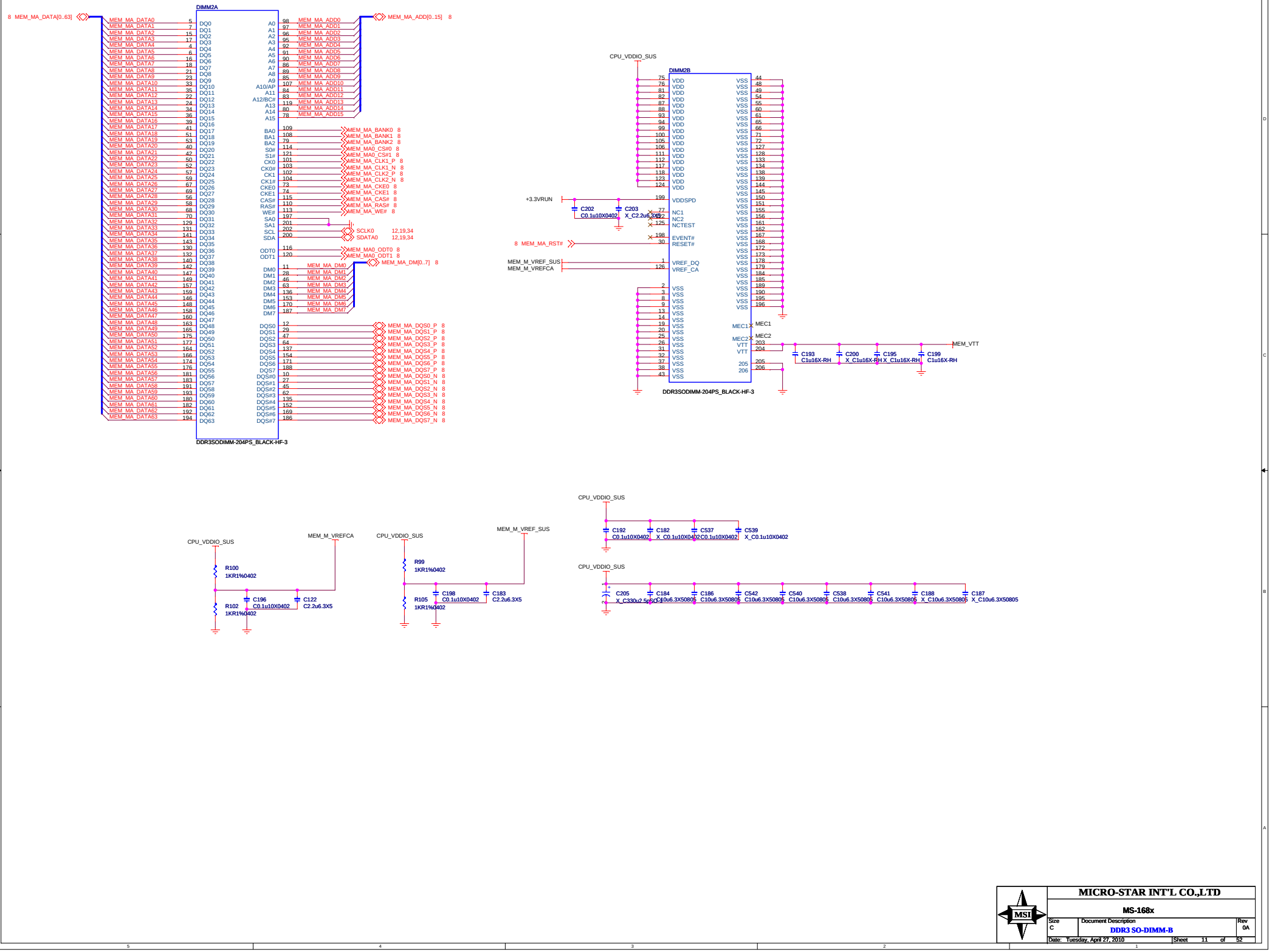

[ChckList] VDD:22u*8/0.22u*2/0.01u0603*2/180p*2
[ChckList] VDDNB:22u*3



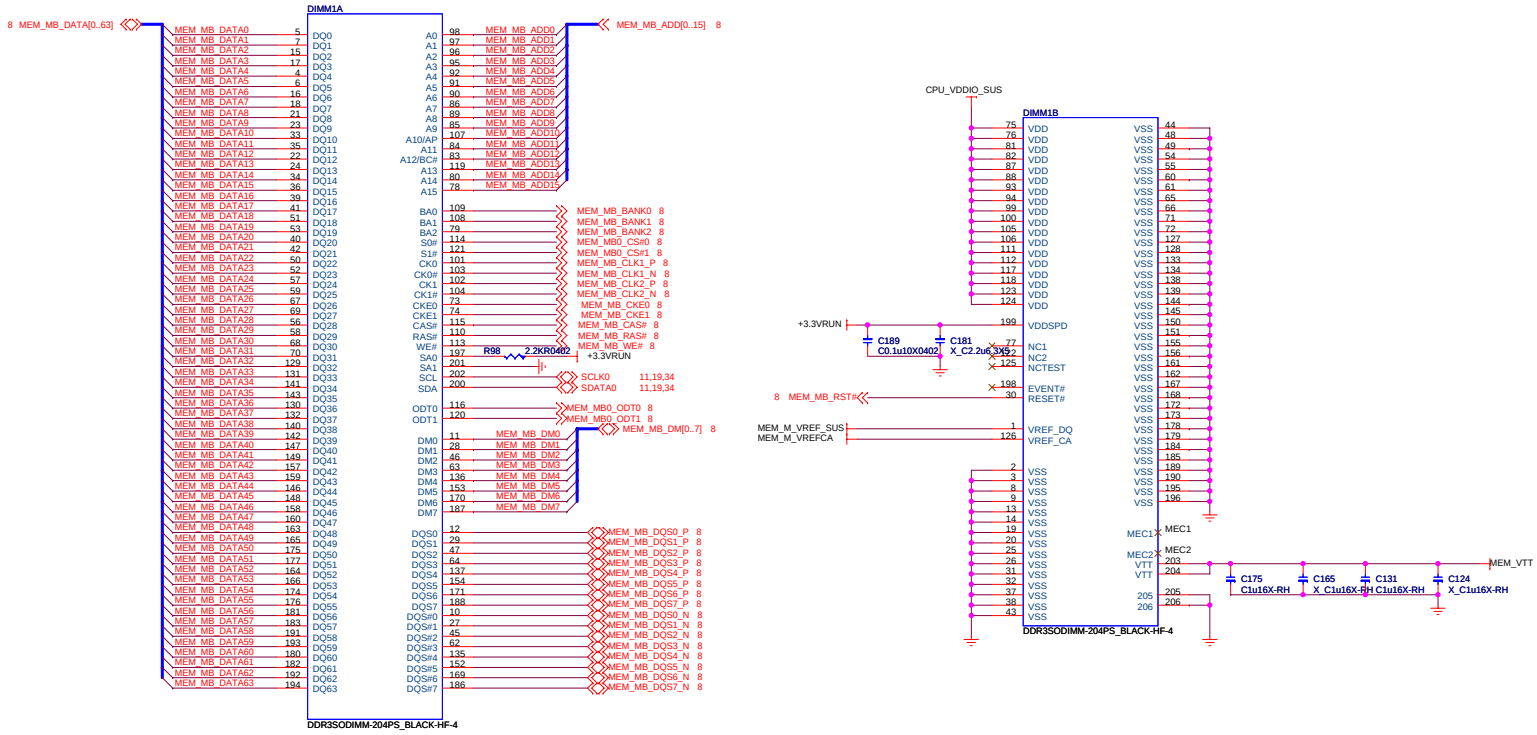

[ChckList] VDDIO:22u*2/0.22u*6/0.1u0603*2/0.01u0603*1/180p*1/4.7u*4

# PROCESSOR POWER AND GROUND

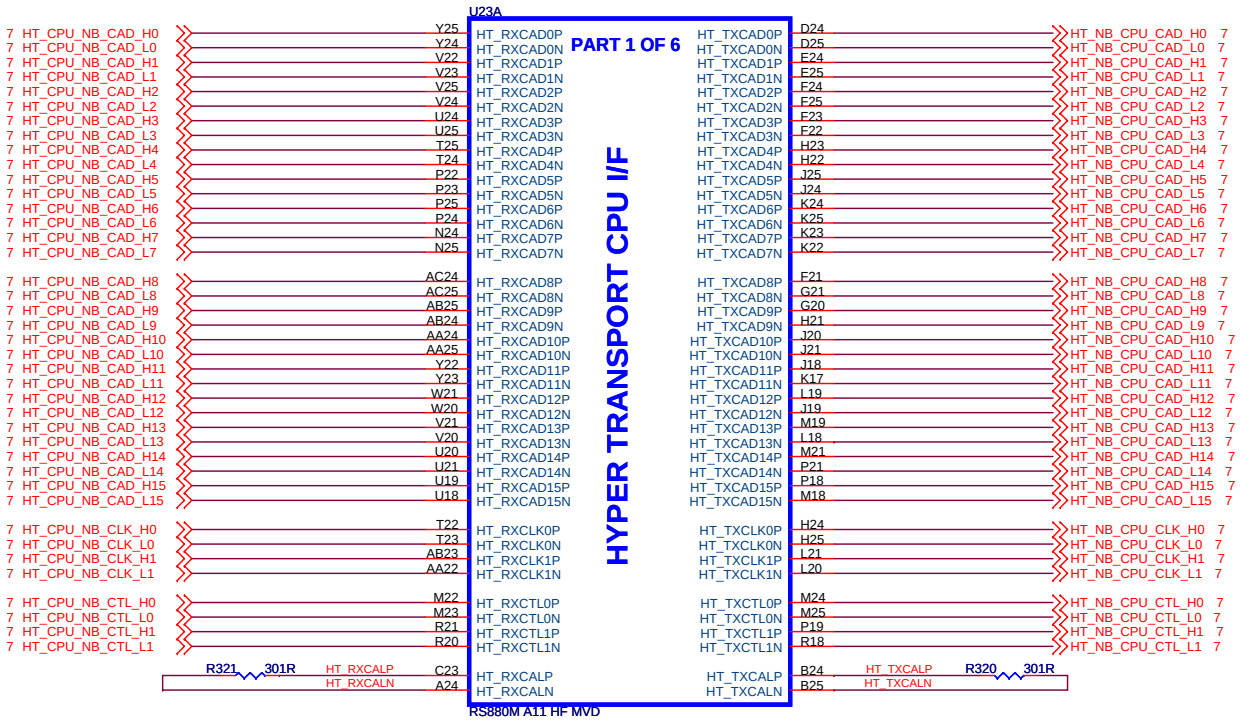
| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: Custom | Document Description: SIG4 POWER and GND | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 10 of 52 | |



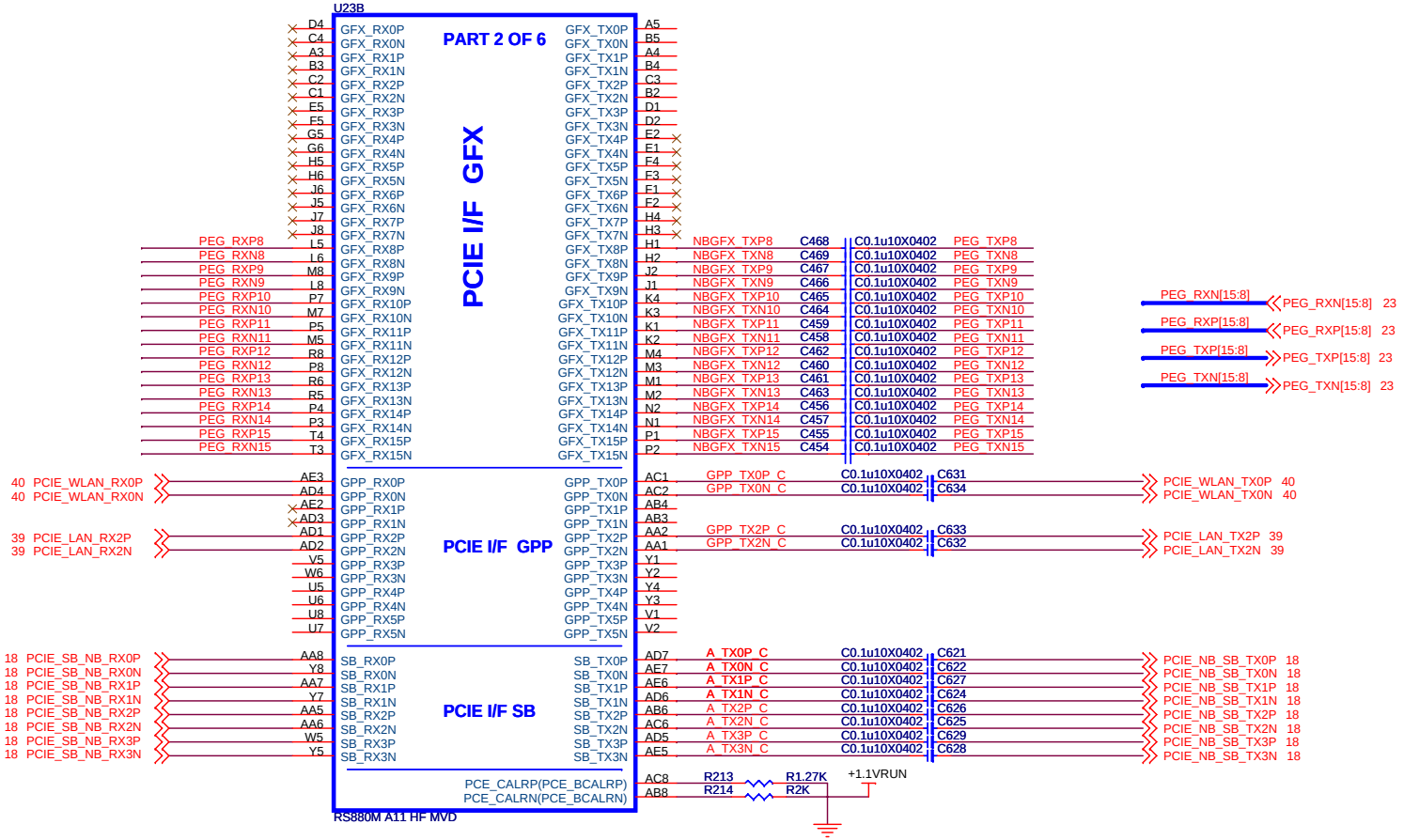

| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: C | Document Description: DDR3 SO-DIMM-B | Rev: 0A |
| Date: Tuesday, April 27, 2010 | Sheet 11 of 52 | |




| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: C | Document Description: DDR3 SO-DIMM-B | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 12 of 52 | |




| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD | |
| MS-168x | |
| Size: B | Document Description: RS880M-HT |
| Rev: 0A | |
| Date: Tuesday, March 30, 2010 | Sheet 13 of 52 |




**RS880M Display Port Support (muxed on GFX)**

| | |
|---|---|
| DP0 | GFX_TX0,TX1,TX2 and TX3<br>AUX0 and HPD0 |
| DP1 | GFX_TX4,TX5,TX6 and TX7<br>AUX1 and HPD1 |

Keep the impendance of PCIE lane to 85ohm +/-15%
Including the A-link

All PCIe lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.

MICRO-STAR INT'L CO.,LTD

MS-168x

| Size | Document Description | Rev |
|---|---|---|
| B | RS880M-PCIE | 0A |

Date: Monday, April 12, 2010 Sheet 14 of 52

DDR3 based CPU and mobile platforms--Level shift to 1.8V

DDR2 based CPU mobile platforms--No need level shift

+1.5VRUN +1.8VRUN R329 1K Q24 R326 2.2K N-MMBT3904_NL_SOT23

9,18 CPU_LDT_STOP# NB_LDT_STOP#

+1.8VRUN R322 1K

18 ALLOW_LDTSTOP ALLOW_LDTSTOP

19,30 NB_PWRGD NB_PWRGD

17,18,30,34 A_RST# R336 X_NC NB_RST#_IN

[CheckList] 200ohm bead?

+1.1VRUN +1.8VRUN L18 220R 3.9R L17 L16 220R L19 220R C397 22uF

65mA 20mA 120mA

C436 2.2uF_4V C425 4.7uF_4V C415 2.2uF_4V C449 2.2uF_4V

Change B204/C262 for black screen issue in AMD 47329 document

+3.3VRUN CP11 X_COPPER 110mA C420 X_2.2uF_4V AVDD

+1.8VRUN CP13 X_COPPER 20mA C428 X_0.1uF AVDDDI

+1.8VRUN CP12 X_COPPER 4mA C424 X_2.2uF_4V AVDDQ

U23C

PART 3 OF 6

F12 AVDD1(NC)
E12 AVDD2(NC)
F14 AVDDDI(NC)
G15 AVSSDI(NC)
H15 AVDDQ(NC)
H14 AVSSQ(NC)

E17 C_Pr(DFT_GPIO5)
F17 Y(DFT_GPIO2)
F15 COMP_Pb(DFT_GPIO4)

G18 RED(DFT_GPIO0)
G17 REDb(NC)
E18 GREEN(DFT_GPIO1)
F18 GREENb(NC)
E19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)

17 HSYNC#1 17 VSYNC#1

A11 DAC_HSYNC(PWM_GPIO4)
B11 DAC_VSYNC(PWM_GPIO6)
F8 DAC_SCL(PCE_RCALRN)
E8 DAC_SDA(PCE_TCALRN)

R200 X_715R1%0402

G14 DAC_RSET(PWM_GPIO1)

CRT/TVOUT

PLLVDD PLLVDD18 VDDA18HTPLL VDDA18PCIEPLL

A12 PLLVDD(NC)
D14 PLLVDD18(NC)
B12 PLLVSS(NC)
H17 VDDA18HTPLL
D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2

PLL PWR

LVTM

NB_RST# IN NB_PWRGD NB_LDT_STOP# ALLOW_LDTSTOP

D8 SYSRESETb
A10 POWERGOOD
C10 LDTSTOPb
C12 ALLOW_LDTSTOP

PM

34 HT_REFCLKP 34 HT_REFCLKN

C25 HT_REFCLKP
C24 HT_REFCLKN

34 NB_OSC NB_REFCLKN

E11 REFCLK_P/OSCIN(OSCIN)
F11 REFCLK_N(PWM_GPIO3)

+1.1VRUN R211 4.7K R210 4.7K

34 GFX_REFCLKP 34 GFX_REFCLKN

T2 GFX_REFCLKP
T1 GFX_REFCLKN

TP74 TP75 GPP_REFCLKP GPP_REFCLKN

U1 GPP_REFCLKP
U2 GPP_REFCLKN

CLOCKs

34 NBLINK_RCLKP 34 NBLINK_RCLKN

V4 GPPSB_REFCLKP(SB_REFCLKP)
V3 GPPSB_REFCLKN(SB_REFCLKN)

R216 X_49.9R A11 R215 X_49.9R A11

I2C_CLK I2C_DATA

B9 I2C_CLK
A9 I2C_DATA
A8 DDC_CLK0/AUX0P(NC)
B8 DDC_DATA0/AUX0N(NC)
B7 DDC_CLK1/AUX1P(NC)
A7 DDC_DATA1/AUX1N(NC)

TP72 TP73

STRP_DATA:
1. Strap function
2. Control NB_CORE power 1-0.95V;0-1.1V

17 STRP_DATA

B10 STRP_DATA

TP49

G11 RSVD

R334 150R RS880_AUX_CAL

C8 AUX_CAL(NC)

MIS.

D9 TMDS_HPD(NC)
D10 HPD(NC)
D12 SUS_STAT#(PWM_GPIO5)
AE8 THERMALDIODE_P
AD8 THERMALDIODE_N
D13 TESTMODE

R209 1.8K

SUS_STAT# 17,19

SUS_STAT#-->Not need connect to SB if Side-Port memory not implemented

RS880M A11 HF MVD

TXOUT_L0P(NC) A22
TXOUT_L0N(NC) B22
TXOUT_L1P(NC) A21
TXOUT_L1N(NC) B21
TXOUT_L2P(NC) B20
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19
TXOUT_L3N(DBG_GPIO2) B19

TXOUT_U0P(NC) B18
TXOUT_U0N(NC) A18
TXOUT_U1P(PCIE_RESET_GPIO3) A17
TXOUT_U1N(PCIE_RESET_GPIO2) B17
TXOUT_U2P(NC) D20
TXOUT_U2N(NC) D21
TXOUT_U3P(PCIE_RESET_GPIO5) D18
TXOUT_U3N(NC) D19

TXCLK_LP(DBG_GPIO1) B16
TXCLK_LN(DBG_GPIO3) A16
TXCLK_UP(PCIE_RESET_GPIO4) D16
TXCLK_UN(PCIE_RESET_GPIO1) D17

LVDS_DIGON(PCE_TCALRP) E9
LVDS_BLON(PCE_RCALRP) F7
LVDS_ENA_BL(PWM_GPIO2) G12

TP48

BIOS control for BLON or PWM function

VDDLTP18(NC) A13
VSSLTP18(NC) B13

15mA

CP25 X_COPPER +1.8VRUN

VDDLT18_1(NC) A15
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14

300mA

CP10 X_COPPER +1.8VRUN

C413 X_0.1uF C411 X_4.7uF C612 X_2.2uF_4V

VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) F20
VSSLT7(VSS) C22

+3.3VRUN R332 4.7K R333 4.7K I2C_CLK I2C_DATA

PLACE R291, R292 CLOSE TO NB(R291, R292 IS FOR A11 SB800 ONLY)

## RS880M DEBUG PIN MAPPING

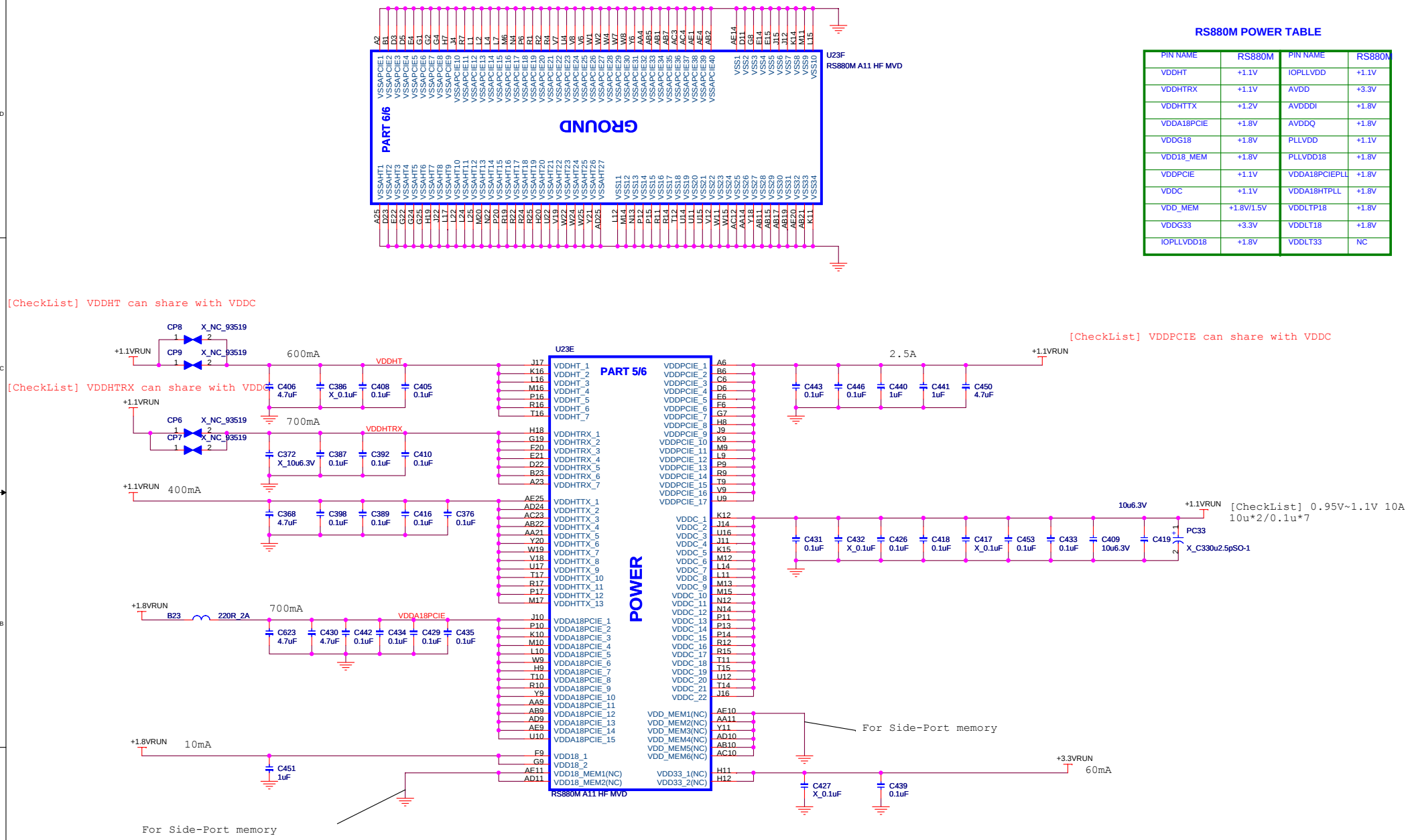
| | |
|---|---|
| DEBUG_OUT0 | LVDS_DIGON |
| DEBUG_OUT1 | LVDS_ENA_BL |
| DEBUG_OUT2 | LVDS_BLON |
| DEBUG_OUT3 | TMDS_HPD |
| DEBUG_OUT4 | AUX1N |
| DEBUG_OUT5 | AUX1P |
| DEBUG_OUT6 | HPD |
| DEBUG_OUT7 | AUX_CAL |

MICRO-STAR INT'L CO.,LTD

MS-168x

Size: Custom | Document Description: RS880M-I/F | Rev: 0A

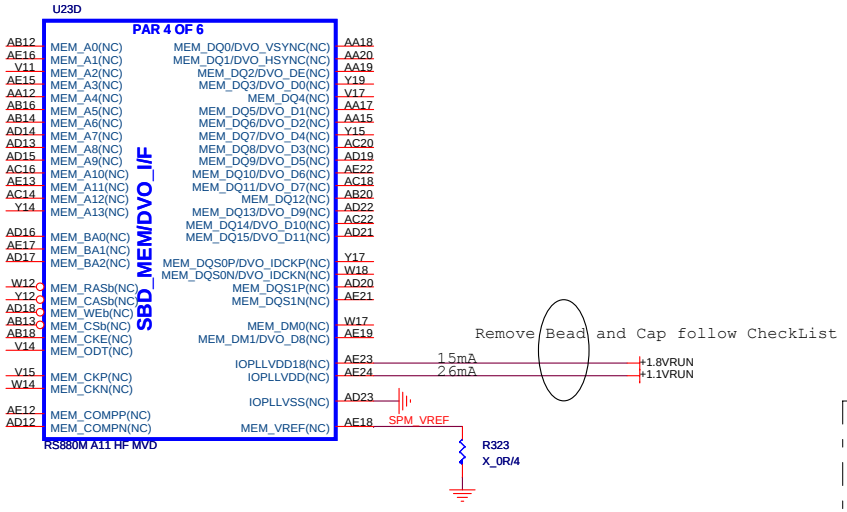
Date: Wednesday, April 21, 2010 | Sheet 15 of 52

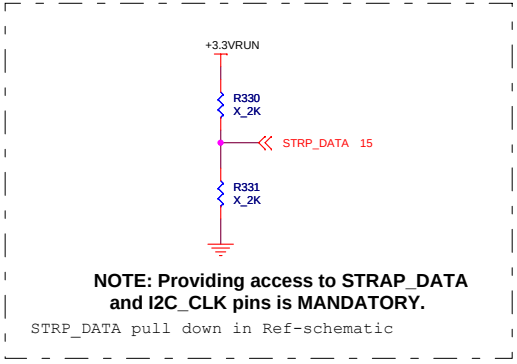


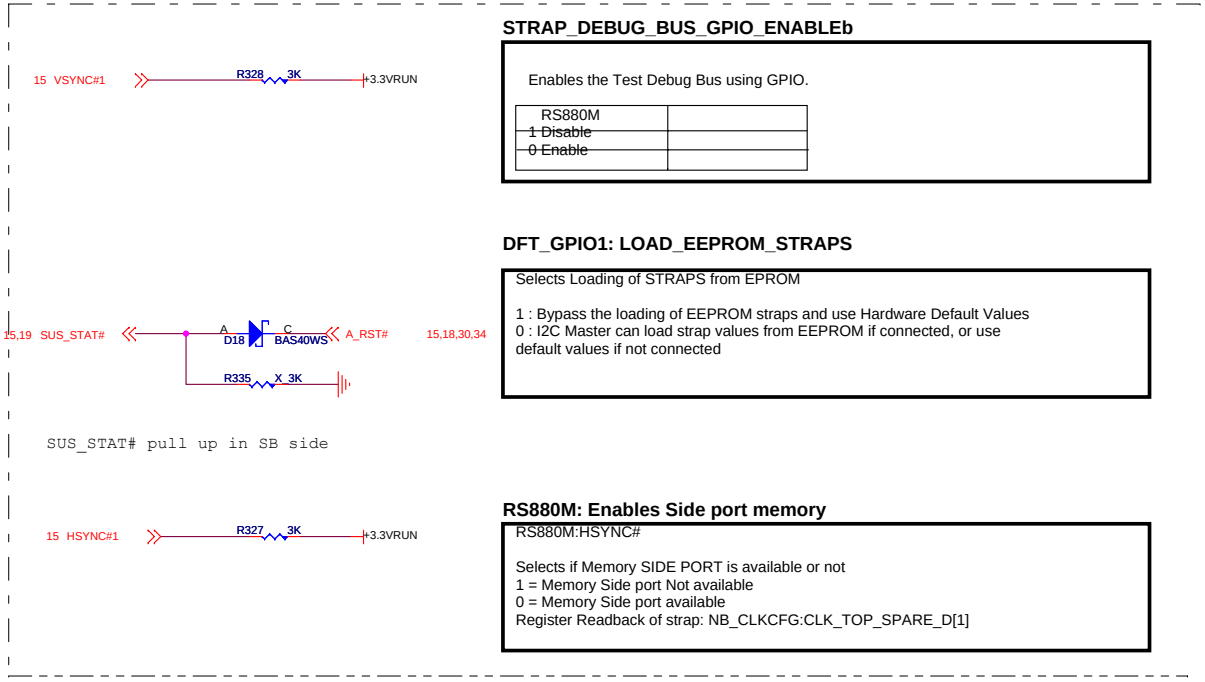

## RS880M POWER TABLE

| PIN NAME | RS880M | PIN NAME | RS880M |
|---|---|---|---|
| VDDHT | +1.1V | IOPLLVDD | +1.1V |
| VDDHTRX | +1.1V | AVDD | +3.3V |
| VDDHTTX | +1.2V | AVDDDI | +1.8V |
| VDDA18PCIE | +1.8V | AVDDQ | +1.8V |
| VDDG18 | +1.8V | PLLVDD | +1.1V |
| VDD18_MEM | +1.8V | PLLVDD18 | +1.8V |
| VDDPCIE | +1.1V | VDDA18PCIEPLL | +1.8V |
| VDDC | +1.1V | VDDA18HTPLL | +1.8V |
| VDD_MEM | +1.8V/1.5V | VDDLTP18 | +1.8V |
| VDDG33 | +3.3V | VDDLT18 | +1.8V |
| IOPLLVDD18 | +1.8V | VDDLT33 | NC |

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD | |
| MS-168x | |
| Size: Custom | Document Description: RS880M-POWER |
| Rev: 0A | |
| Date: Wednesday, April 21, 2010 | Sheet 16 of 52 |




MICRO-STAR INT'L CO.,LTD

MS-168x

| Size | Document Description | Rev |
|---|---|---|
| Custom | RS880M-STRAPS | 0A |

Date: Tuesday, March 30, 2010 Sheet 17 of 52

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

U7A

SB800 Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

PEX_STD_SW#: Low - Standard(desktop) Swing Level Input(3T) - Low Swing Level Mode (Default)

NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED.

NOTE: The 0R serial resistor on SB CLK pair must share Pad with the serial resistor close to U800

PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

| SB_GPP GFX_CLK | DEVICE MXM3.0 | CLKREQ# CLK_REQG# |
|---|---|---|
| 0 | EXPRESS | 0 |
| 1 | PE0 | 1 |
| 2 | PE2 | 2 |
| 3 | LAN | 3 |
| 4 | PE1 | 4 |
| 5 | X4DT | 5 |
| 6 | PE3 | 6 |
| 7 | USB3.0 | 7 |
| 8 | 1394 | 8 |

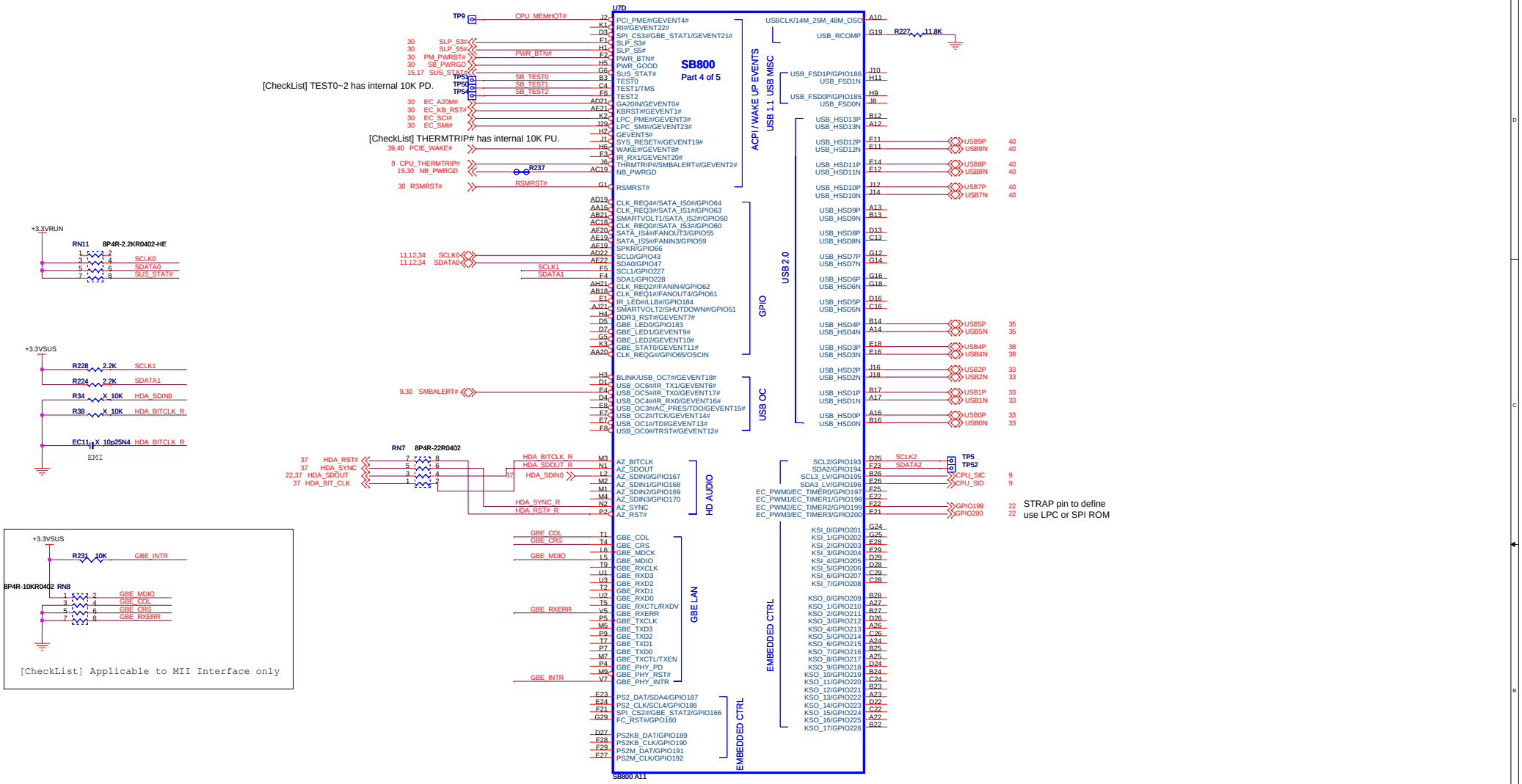
SB800 A11

MICRO-STAR INT'L CO.,LTD

MS-168x

Size: Custom | Document Description: SB820-PCIE/PCI/CPU/LPC/CLK | Rev: 0A

Date: Wednesday, May 05, 2010 | Sheet 18 of 52




MICRO-STAR INT'L CO.,LTD

MS-168x

| Size | Document Description | Rev |
|---|---|---|
| C | SB820-GPIO/USB/AZ | 0A |

Date: Tuesday, April 27, 2010 | Sheet 19 of 52

SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

SATA PORTS DISTRIBUTION:
0, - 2.5 INCH DISK DRIVER
1, SATA ODD
2, - 2.5 INCH DISK DRIVER
3, eSATA
4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

SATA_CALRP:
SB8xx A11: 800-? 1% resistor to GND.
SB8xx A12: 1K-? 1% resistor to GND.

To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts

Connect C7 and D8, then go to GND directly.

U7B

SB800
Part 2 of 5

SB800 A11

| | | | | | |
|---|---|---|---|---|---|
| 36 SATA0TXP | C147 10nF | SATA_TX0+ | AH9 | SATA_TX0P | SERIAL ATA |
| 36 SATA0TXN | C148 10nF | SATA_TX0- | AJ9 | SATA_TX0N | |
| 36 SATA0RXN | C133 10nF | SATA_RX0- | AJ8 | SATA_RX0N | |
| 36 SATA0RXP | C132 10nF | SATA_RX0+ | AH8 | SATA_RX0P | |
| 36 SATA1TXP | C134 10nF | SATA_TX1+ | AH10 | SATA_TX1P | |
| 36 SATA1TXN | C135 10nF | SATA_TX1- | AJ10 | SATA_TX1N | |
| 36 SATA1RXN | C149 10nF | SATA_RX1- | AG10 | SATA_RX1N | |
| 36 SATA1RXP | C150 10nF | SATA_RX1+ | AE10 | SATA_RX1P | |
| | | | AG12 | SATA_TX2P | |
| | | | AF12 | SATA_TX2N | |
| | | | AJ12 | SATA_RX2N | |
| | | | AH12 | SATA_RX2P | |
| | | | AH14 | SATA_TX3P | |
| | | | AJ14 | SATA_TX3N | |
| | | | AG14 | SATA_RX3N | |
| | | | AF14 | SATA_RX3P | |
| | | | AG17 | SATA_TX4P | |
| | | | AF17 | SATA_TX4N | |
| | | | AJ17 | SATA_RX4N | |
| | | | AH17 | SATA_RX4P | |
| | | | AJ18 | SATA_TX5P | |
| | | | AH18 | SATA_TX5N | |
| | | | AH19 | SATA_RX5N | |
| | | | AJ19 | SATA_RX5P | |
| AVDD_SATA | R233 1% 1.0K | SATA_CALP | AB14 | SATA_CALRP | |
| | R234 1% 931R | SATA_CALN | AA14 | SATA_CALRN | |
| 38 SATA_ACTIVE# | | | AD11 | SATA_ACT#/GPIO67 | |
| X_22pF C130 | Y5 X_25.0000_MHz | SATA_X1 | AD16 | SATA_X1 | |
| X_22pF C129 | R79 X_1M | SATA_X2 | AC16 | SATA_X2 | |

| | | | | |
|---|---|---|---|---|
| TP53 | SPI_DATAIN | J5 | SPI_DI/GPIO164 | SPI ROM |
| TP7 | SPI_DATAOUT | E2 | SPI_DO/GPIO163 | |
| TP55 | SPI_CLK | K4 | SPI_CLK/GPIO162 | |
| TP56 | SPI_CS# | K9 | SPI_CS1#/GPIO165 | |
| TP8 | SB700_ROM_RST# | G2 | ROM_RST#/GPIO161 | |

| | | |
|---|---|---|
| FC_CLK | AH28 | FLASH |
| FC_FBCLKOUT | AG28 | |
| FC_FBCLKIN | AE26 | |
| FC_OE#/GPIOD145 | AF28 | |
| FC_AVD#/GPIOD146 | AG29 | |
| FC_WE#/GPIOD148 | AG26 | |
| FC_CE1#/GPIOD149 | AF27 | |
| FC_CE2#/GPIOD150 | AE29 | |
| FC_INT1/GPIOD144 | AF29 | |
| FC_INT2/GPIOD147 | AH27 | |
| FC_ADQ0/GPIOD128 | AJ27 | |
| FC_ADQ1/GPIOD129 | AJ26 | |
| FC_ADQ2/GPIOD130 | AH25 | |
| FC_ADQ3/GPIOD131 | AH24 | |
| FC_ADQ4/GPIOD132 | AG23 | |
| FC_ADQ5/GPIOD133 | AH23 | |
| FC_ADQ6/GPIOD134 | AJ22 | |
| FC_ADQ7/GPIOD135 | AG21 | |
| FC_ADQ8/GPIOD136 | AF21 | |
| FC_ADQ9/GPIOD137 | AH22 | |
| FC_ADQ10/GPIOD138 | AJ23 | |
| FC_ADQ11/GPIOD139 | AF23 | |
| FC_ADQ12/GPIOD140 | AJ24 | |
| FC_ADQ13/GPIOD141 | AJ25 | |
| FC_ADQ14/GPIOD142 | AG25 | |
| FC_ADQ15/GPIOD143 | AH26 | |

| | | |
|---|---|---|
| FANOUT0/GPIO52 | W5 | HW MONITOR |
| FANOUT1/GPIO53 | W6 | |
| FANOUT2/GPIO54 | Y9 | |
| FANIN0/GPIO56 | W7 | |
| FANIN1/GPIO57 | V9 | |
| FANIN2/GPIO58 | W8 | |
| TEMPIN0/GPIO171 | B6 | |
| TEMPIN1/GPIO172 | A6 | |
| TEMPIN2/GPIO173 | A5 | |
| TEMPIN3/TALERT#/GPIO174 | B5 | |
| TEMP_COMM | C7 | |
| VIN0/GPIO175 | A3 | |
| VIN1/GPIO176 | B4 | |
| VIN2/GPIO177 | A4 | |
| VIN3/GPIO178 | C5 | |
| VIN4/GPIO179 | A7 | |
| VIN5/GPIO180 | B7 | |
| VIN6/GBE_STAT3/GPIO181 | B8 | |
| VIN7/GBE_LED3/GPIO182 | A8 | |

RN5 X_8P4R-10KR0402
RN4 X_8P4R-10KR0402
RN6 X_8P4R-10KR0402

NC1 G27
NC2 Y2

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD | |
| MS-168x | |
| Size: Custom | Document Description: SB820-SATA/IDE/SPI/HWM |
| Rev: 0A | |
| Date: Monday, April 12, 2010 | Sheet 20 of 52 |

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

1*22U/3*0.1u

1*10U/2*1U/2*0.1u

SB800 Part 3 of 5

POWER

GROUND

SB800 Part 5 of 5

GPIOD not used-->Tied to GND

No 42ohm bead, Use 30ohm

[CheckList] Bead-- 42 Ω @ 100 MHz/4A/ ≤ 0.01 Ω

GbE Controller Not Enabled: Connected to GND

Updated on Rev2.0

[CheckList] No bead?

USB S3-S5 Wake Implemented: Tied to +3.3V_S5.
USB S3-only Wake Implemented: Tied to +3.3V_S3.
USB S3-S5 Wake Not Implemented: Tied to +3.3V_S3.

USB S3-S5 Wake Implemented: Tied to +1.1V_S5.
USB S3-only Wake Implemented: Tied to +1.1V_S3.
USB S3-S5 Wake Not Implemented: Tied to +1.1V_S3.

Wake on LAN supported: Tied to a +3.3V_S5 rail

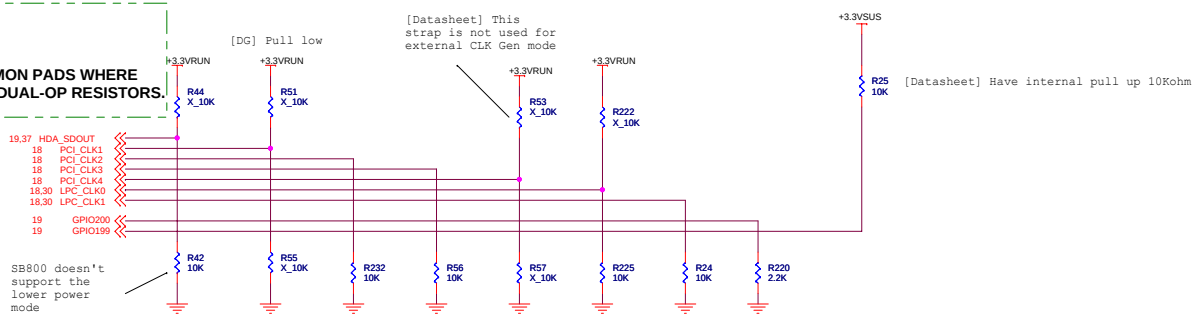
To meet SB800 SCL1.02:
Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

HWM not Implemented and not used as GPIOs: Bead and Decoupling caps not used.

[CheckList] 1.5VSUS or 3.3VSUS

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-168x | | |
| Size: Custom | Document Description: SB820-POWER | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 21 of 52 | |

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.




## REQUIRED STRAPS

| | AZ_SDOUT | PCI_CLK1 | PCI_CLK2 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | GPIO200 GPIO199 |
|---|---|---|---|---|---|---|---|---|
| PULL HIGH | LOW POWER MODE | ALLOW PCIE Gen2 DEFAULT | Watchdog Timer Enabled | USE DEBUG STRAP | non_Fusion CLOCK MODE DEFAULT | EC ENABLED | CLKGEN ENABLED DEFAULT | H,H = Reserved<br>H,L = SPI ROM |
| PULL LOW | PERFORMANCE MODE DEFAULT | FORCE PCIE Gen1 | Watchdog Timer Disabled DEFAULT | IGNORE DEBUG STRAP DEFAULT | FUSION CLOCK MODE | EC DISABLED DEFAULT | CLKGEN DISABLED | L,H = LPC ROM (Default)<br>L,L = FWH ROM |

PCI_CLK1(SMSC_CLK)-->SB820M: Only provision for pull-down is required, not installed by default--checklist

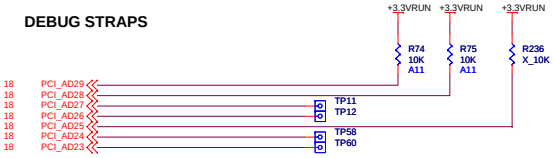
[Fuqun] GPIO199 NC in checklist

[Fuqun] PCI_CLK4 high or low?

## SB PCIE EEPROM STRAPS


SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

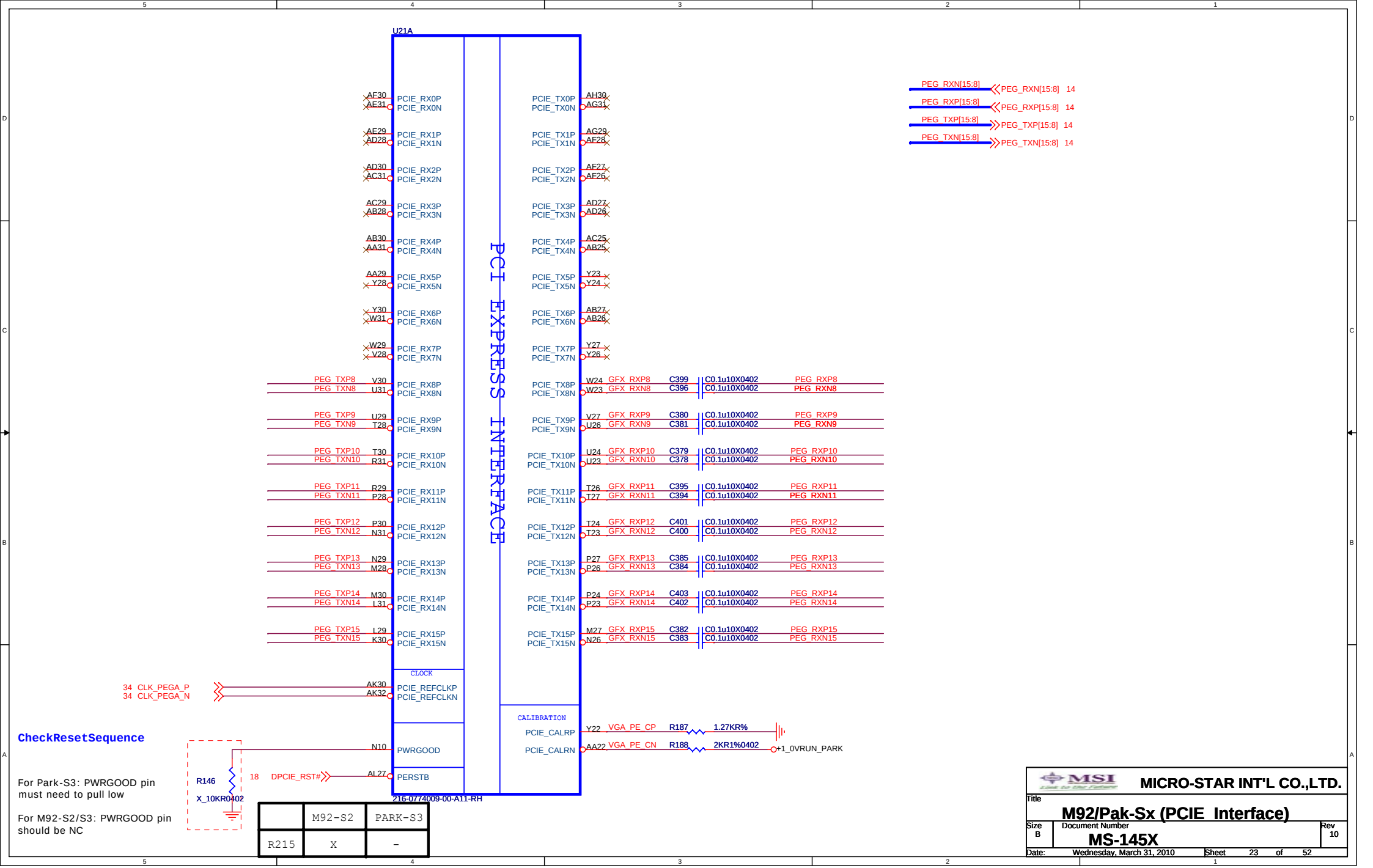
## DEBUG STRAPS




| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

PCI23/24/26/27 have internal pull high 15kohm,But PCI25?
Why PCI28/29 pull high?


MICRO-STAR INT'L CO.,LTD
MS-168x
Size: Custom | Document Description: SB820-STRAPS | Rev: 0A
Date: Wednesday, April 28, 2010 | Sheet 22 of 52




**CheckResetSequence**

For Park-S3: PWRGOOD pin must need to pull low

For M92-S2/S3: PWRGOOD pin should be NC

| | M92-S2 | PARK-S3 |
|---|---|---|
| R215 | X | - |

MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (PCIE Interface)

Size: B | Document Number: MS-145X | Rev: 10

Date: Wednesday, March 31, 2010 | Sheet 23 of 52

| | M92-S2 | PARK-S3 |
|---|---|---|
| R210 | X | - |
| R195 | X | - |
| R208 | X | - |
| C659 | X | - |
| C658 | X | - |
| C512 | X | - |
| C662 | X | - |
| C661 | X | - |
| C660 | X | - |
| R197 | X | - |
| R356 | X | - |
| C665 | X | - |
| C664 | X | - |
| C663 | X | - |
| R406 | X | - |
| R404 | X | - |
| R402 | X | - |

| | M92-S2 | PARK-S3 |
|---|---|---|
| R206 | - | X |
| R300 | X | - |

For PARK-S3: Install All components in this Box INCLUDING Decoupling caps and Bead connecting to DPC_VDD18#

For M92-S2: DO NOT Install any Component in this Box.

ATI suggestion

Sequence

Reserve TEST_EN / JTAG_TMS pull high R for AMD recommend

Reserve JTAG_TRSTB pull low R for AMD recommend

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

AVSSQ have to be away from noisy ground
A2VSSQ have to be away from noisy ground
it is for layout recommendation

OPTIONAL RC NETWORK TO FINE TUNE POWER SEQUENCING

**Note:1**
For M9x-S2/S3 XO_IN and XO_IN2 Pins are NC, can be gronded

For Park-S3: XO_IN and XO_IN2 can be use as 3.3V CLK Input. These poins can be grounded if not in use.

**Check 1.8VRUN and VDDR3 Sequence**
For Park-S3 : Stuff R443
For M92-S2 : Stuff R451

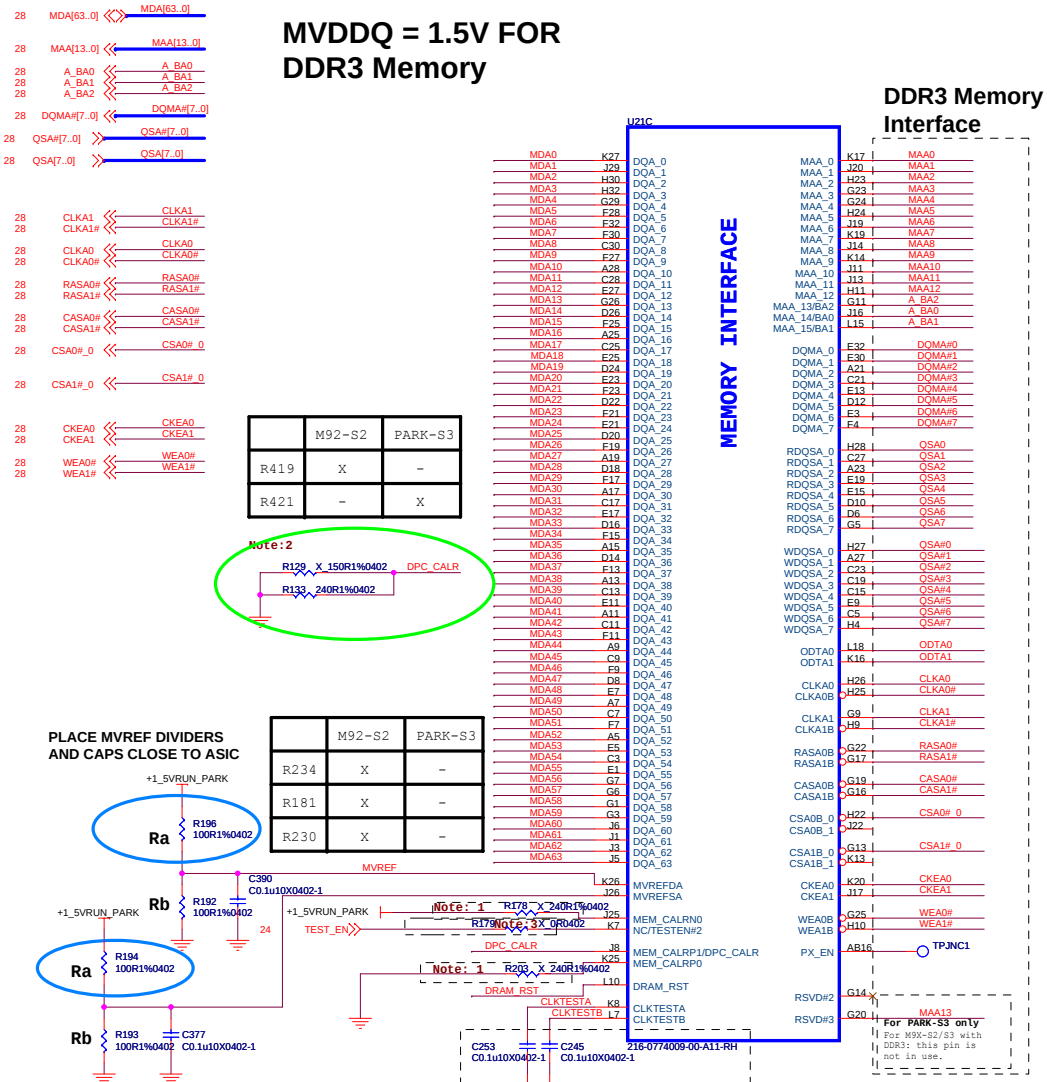
## LVDS Interface

216-0774009-00-A11-RH

| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | M92/Pak-Sx (Main IO) |
| Size: Custom | Document Number: MS-145X |
| Rev | 10 |
| Date: Wednesday, May 12, 2010 | Sheet 24 of 52 |

# MVDDQ = 1.5V FOR DDR3 Memory

## DDR3 Memory Interface




| | M92-S2 | PARK-S3 |
|---|---|---|
| R419 | X | - |
| R421 | - | X |

Note:2



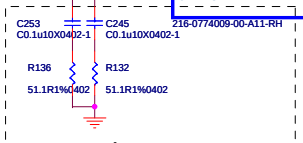

| | M92-S2 | PARK-S3 |
|---|---|---|
| R234 | X | - |
| R181 | X | - |
| R230 | X | - |

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC




| | M92-S2 | PARK-S3 |
|---|---|---|
| R428 | - | X |
| R226 | - | X |

| DIVIDER RESISTORS | DDR3 |
|---|---|
| MVREF TO 1.5V (Ra) | 43R |
| MVREF TO GND (Rb) | 100R |



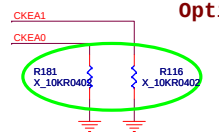

route 50ohms single-ended/100ohms diff and keep short

Use this option ONLY for Park-S3

| | M92-S2 | PARK-S3 |
|---|---|---|
| C568 | R=0ohm | C=0.1U |
| C341 | R=0ohm | C=0.1U |
| R423 | R=4.7k | R=51.1ohm |
| R227 | R=4.7k | R=51.1ohm |

| | M92-S2 | PARK-S3 |
|---|---|---|
| R247 | X | - |
| R246 | X | - |

## Option for DDR3/GDDR3/DDR2 with Park




Do not Install for M9X-S2/S3

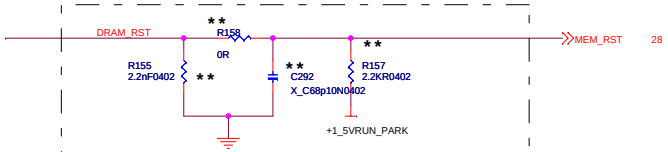
INSTALL for Park-S3 to save power in auto refresh mode

These can be placed close to ASIC side or Memory side.

Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.

Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR

Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24




** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor vvalues are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

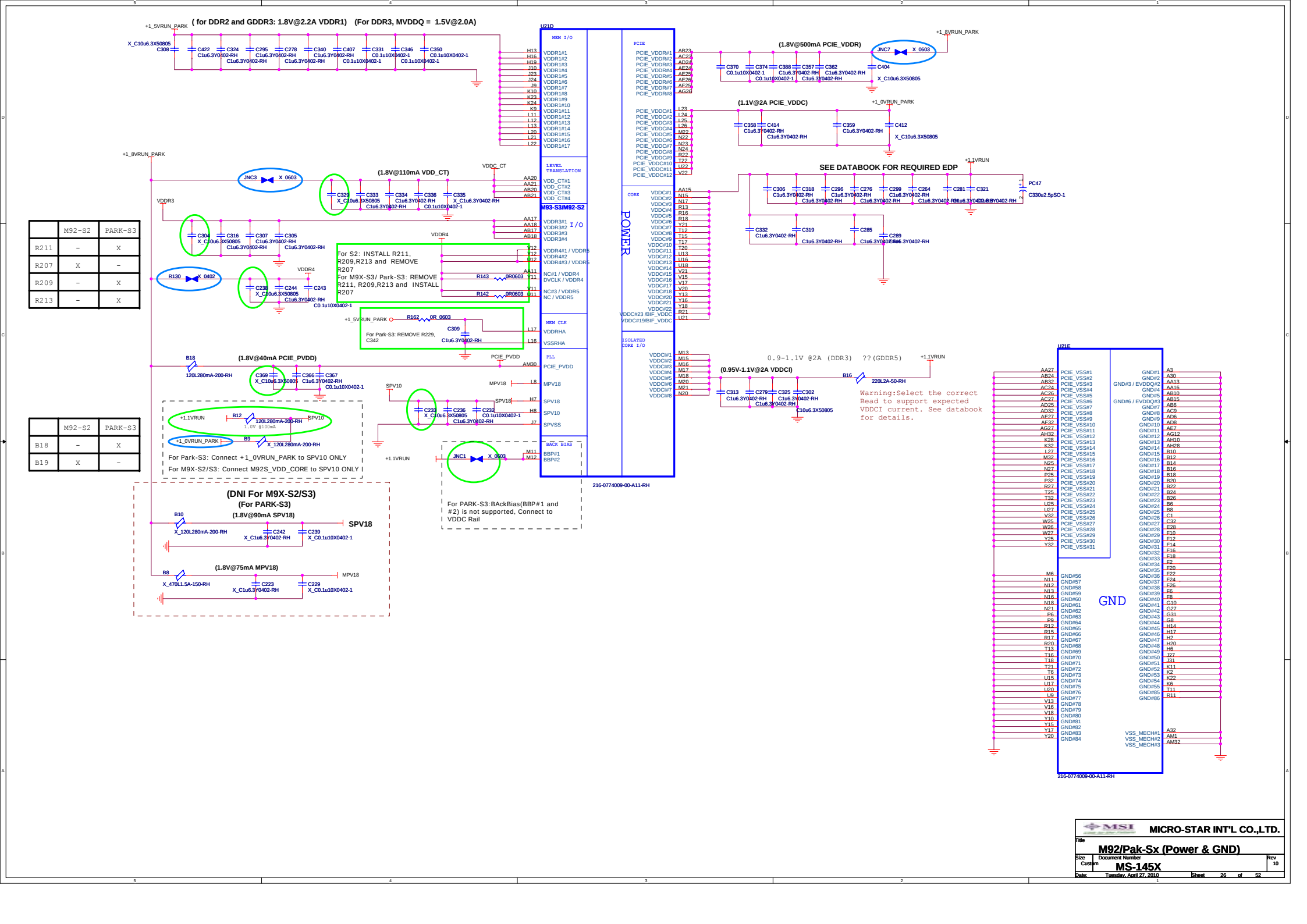
| Designator | For M9X-S2 and M93-S3 | For Park-S3 |
|---|---|---|
| R425 | DNI | 10K |
| R427 | 0R/Short | 680R |
| R430 | 2.2K | DNI |
| C571 | 2.2nF | 68pF |


MICRO-STAR INT'L CO.,LTD.

Title: M92/Pak-Sx (MEM_Interface)

Size: Custom | Document Number: MS-145X | Rev: 10

Date: Tuesday, March 30, 2010 | Sheet 25 of 52

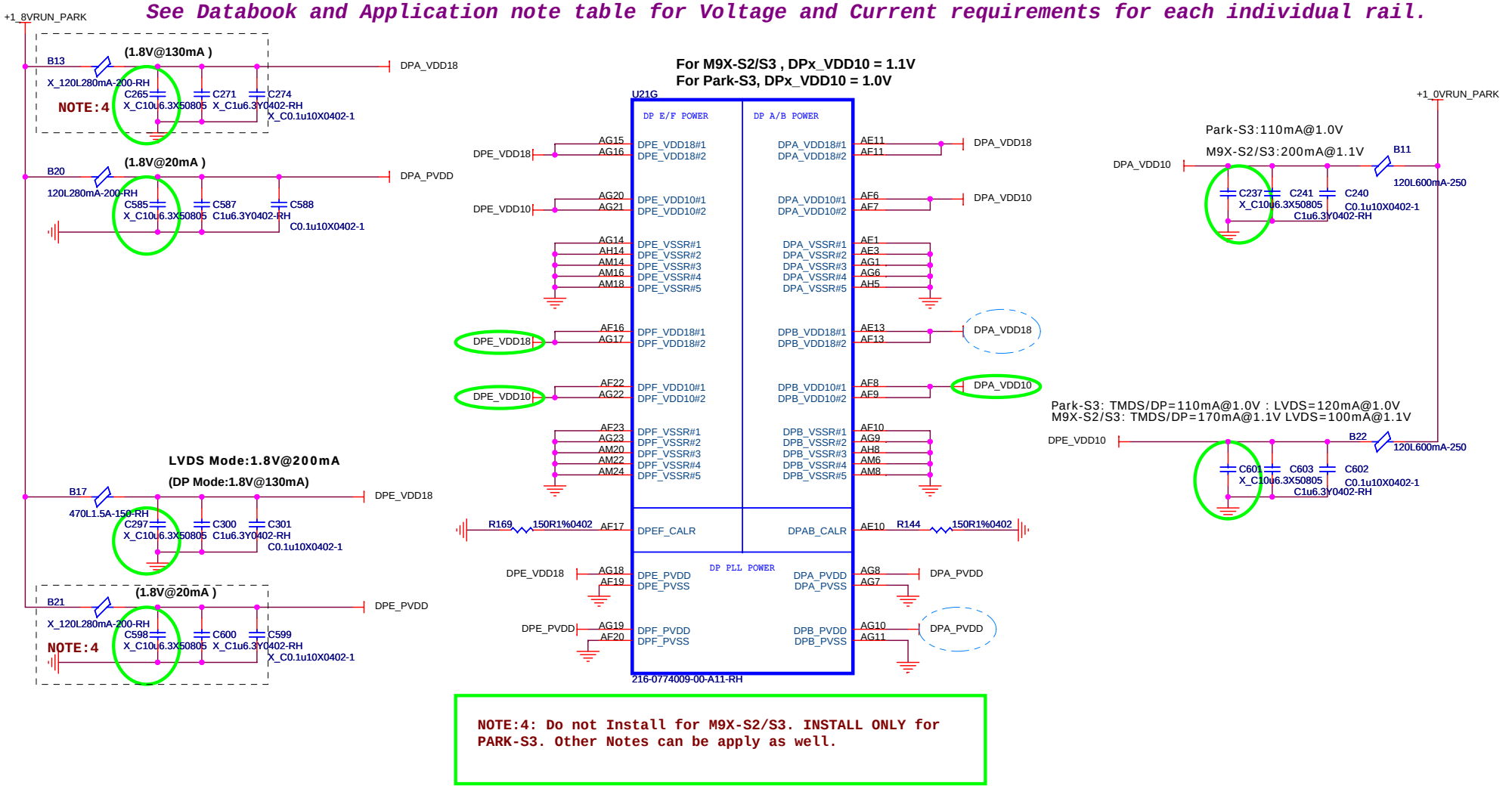



| | M92-S2 | PARK-S3 |
|---|---|---|
| R211 | - | X |
| R207 | X | - |
| R209 | - | X |
| R213 | - | X |

| | M92-S2 | PARK-S3 |
|---|---|---|
| B18 | - | X |
| B19 | X | - |

| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | M92/Pak-Sx (Power & GND) |
| Size: Custom | Document Number: MS-145X |
| Rev | 10 |
| Date: Tuesday, April 27, 2010 | Sheet 26 of 52 |

*See Databook and Application note table for Voltage and Current requirements for each individual rail.*

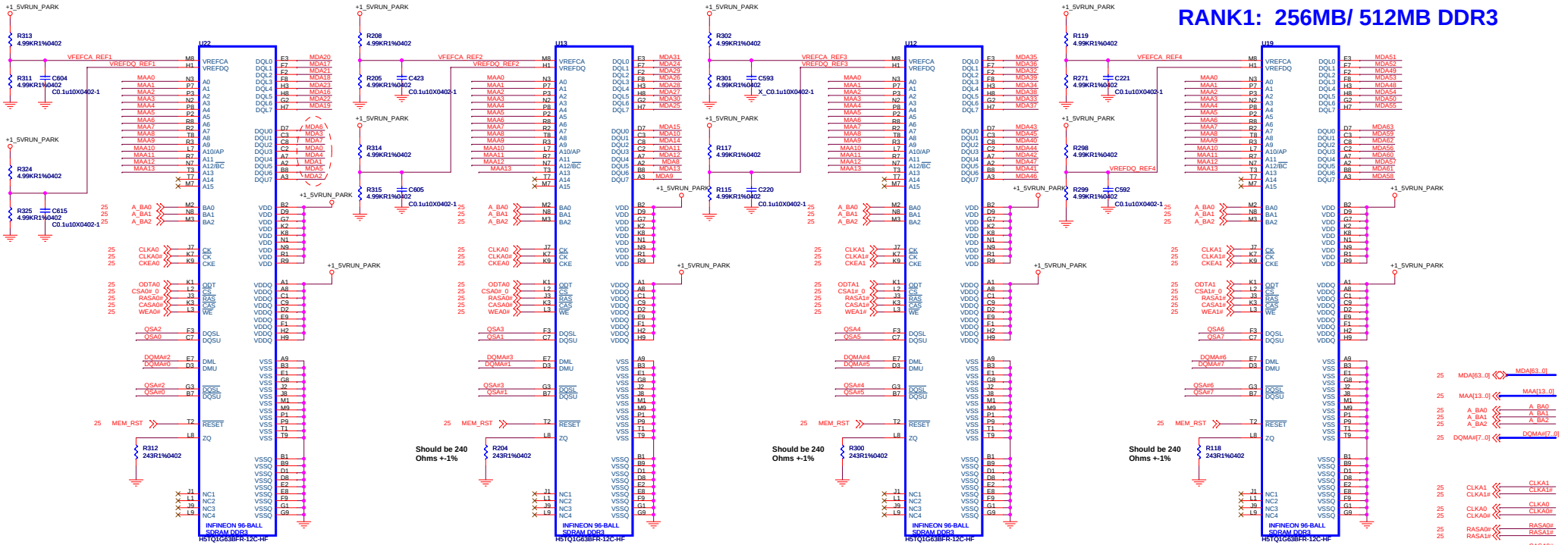


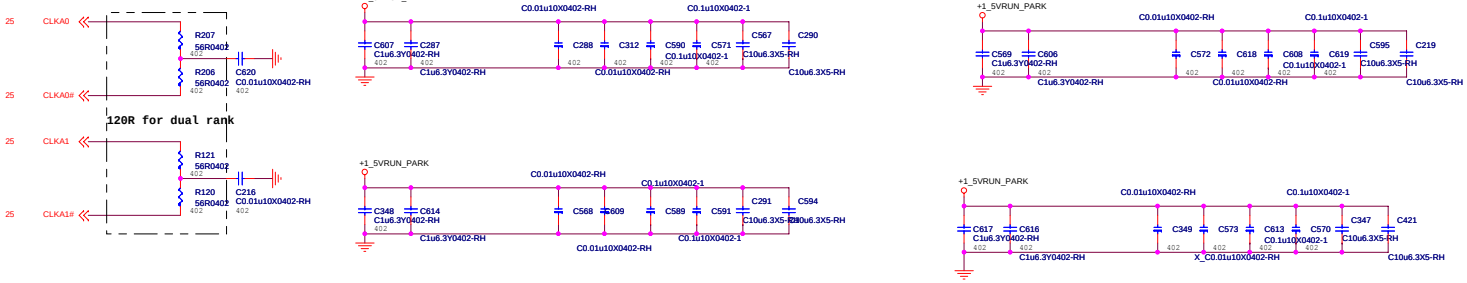

**NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.**

MICRO-STAR INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | M92/Pak-Sx (DP Power) | |
| Size B | Document Number MS-145X | Rev 10 |
| Date: Wednesday, May 05, 2010 | Sheet 27 of 52 | |

# RANK1: 256MB/ 512MB DDR3



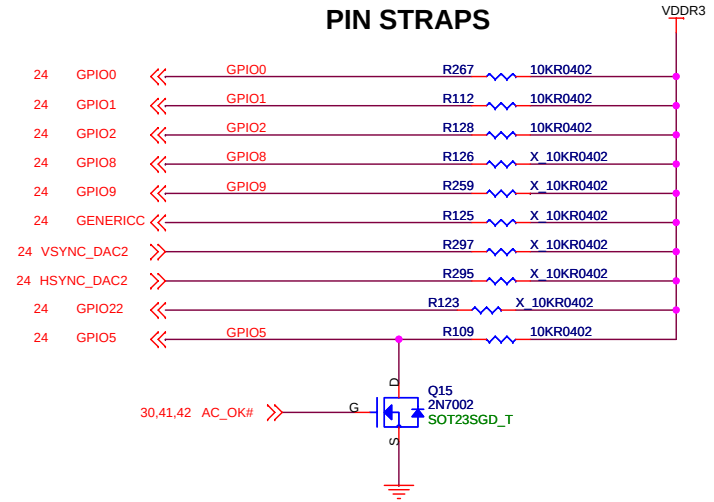

**For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC**

**For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.**

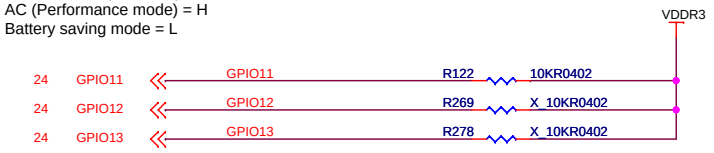
MICRO-STAR INT'L CO.,LTD.

| | | | |
|---|---|---|---|
| Title | DDR2 (64Mx16bit) | | |
| Size | Document Number | | Rev |
| Custom | MS-145X | | 10 |
| Date: | Wednesday, May 05, 2010 | Sheet 28 of 52 | |

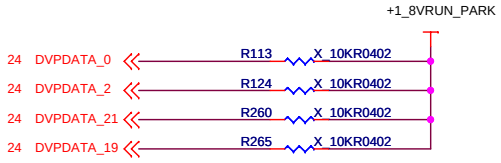
## PIN STRAPS




GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L








## CONFIGURATION STRAPS

| PIN | M92-S2 LP | PARK LP S3 | DESCRIPTION OF DEFAULT SETTINGS |
|---|---|---|---|
| GPIO0 | 1 | | GPIO=0 50% TX output swing<br>GPIO=1 Full TX output swing |
| GPIO1 | 1 | | GPIO=0 TX de-emphasis disabled<br>GPIO=1 TX de-emphasis enabled |
| GPIO2 | 1 | | GPIO=0 Advertises the PCIE device as 2.5 GT/S capable at power -on<br>GPIO=1 Advertises the PCIE device as 5 GT/S capable at power -on |
| GPIO9 | 0 | | GPIO=0 VGA controller capacity enabled.<br>GPIO=1 The device will not be recognized as the system's VGA controler. |
| VSYNC_DAC2 | 0 | | GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset. |
| GPIO22 | 0 | | GPIO=0 not used external BIOS ROM GPIO=1 if used |

| PIN | M92-S2 LP | PARK LP S3 | DESCRIPTION OF DEFAULT SETTINGS |
|---|---|---|---|
| GPIO 13 GPIO 12 GPIO 11 | | | 0 0 0=128 MB |
| | 0 0 1 | | 0 0 1=256 MB |
| | | | 0 1 0=64 MB |

| PIN | M92-S2 LP | PARK LP S3 | DESCRIPTION OF DEFAULT SETTINGS |
|---|---|---|---|
| VGA_HSYNC# VGA_VSYNC# | | | 0 0=No audio function |
| | | | 0 1=Audio for display port only |
| | | | 1 0=Audio for display port and HDMI if dongle is detected |
| | 1 1 | | 1 1=Audio for both displayport and HDMI |

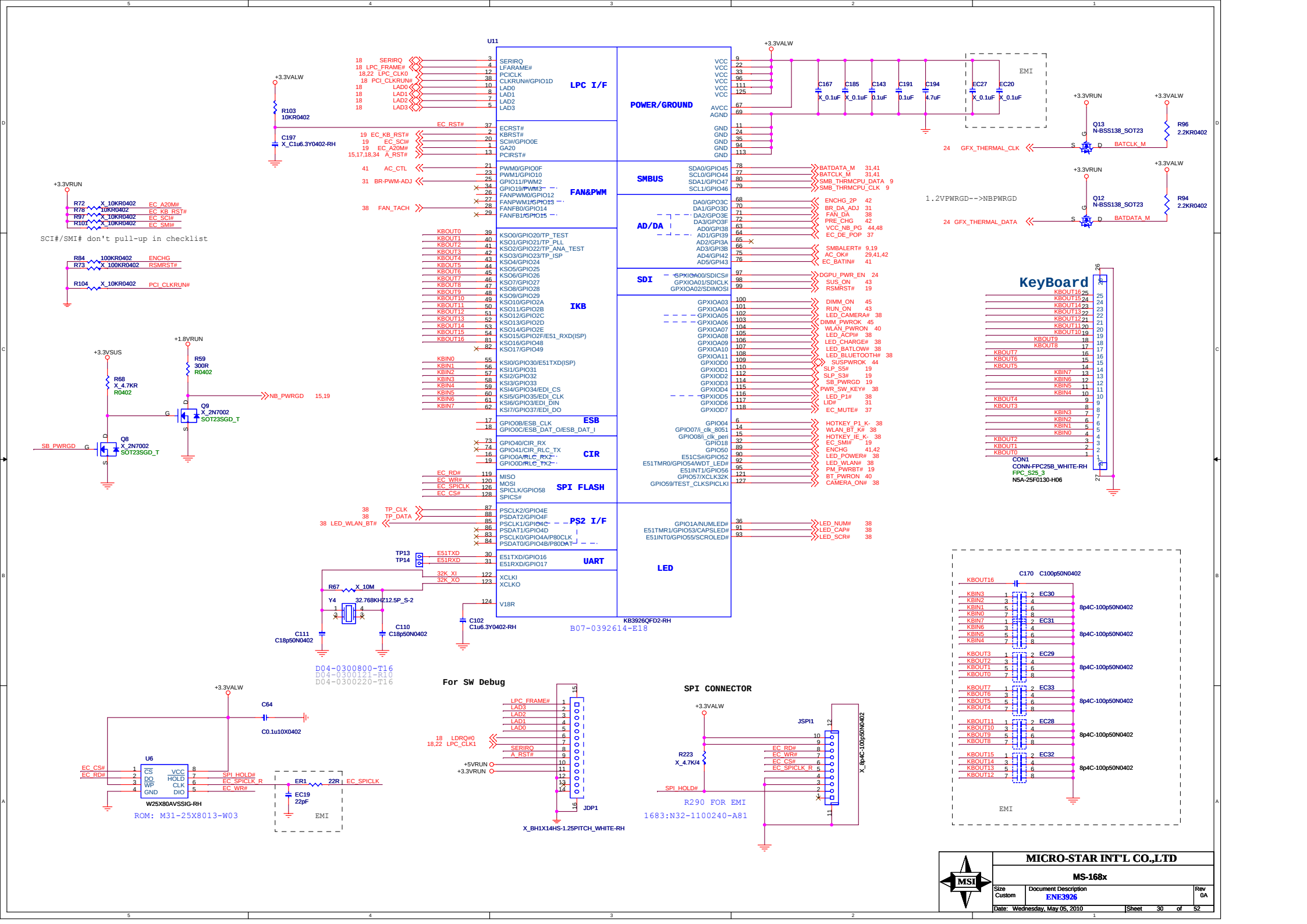
| DVPDATA19 | DVPDATA21 | DVPDATA2 | DVPDATA0 | MEM_TYPE |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23) |
| 0 | 0 | 0 | 1 | Samsung 64Mx16 DDR3 (M12-K4W1G85-S02) |
| 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | |

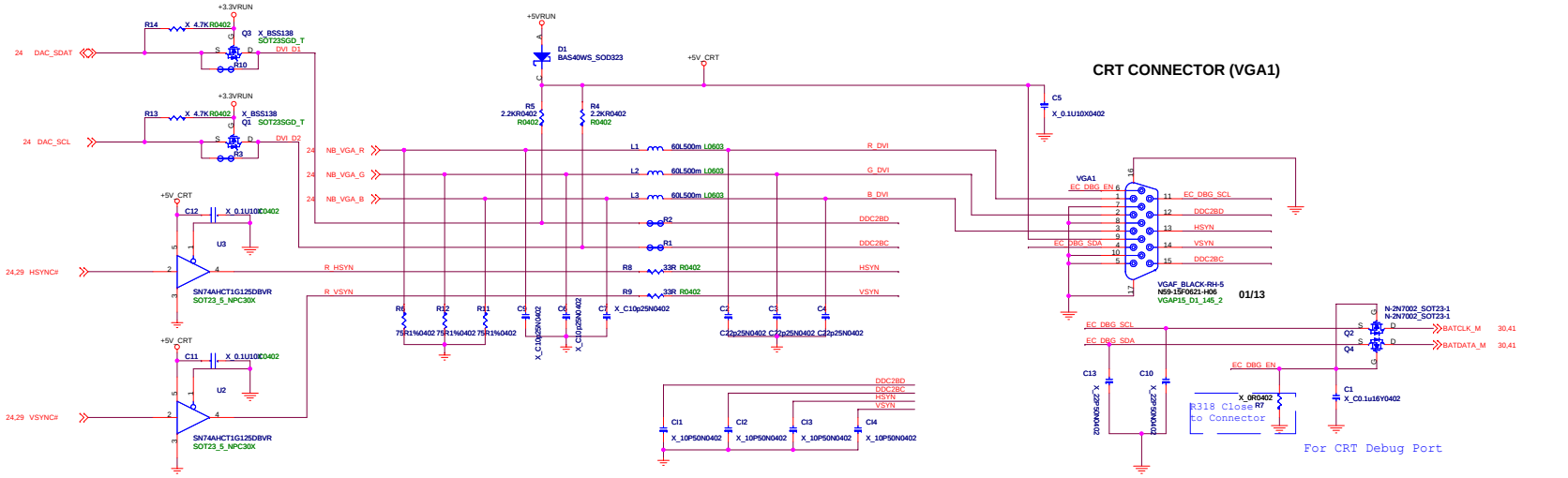
MICRO-STAR INT'L CO.,LTD.

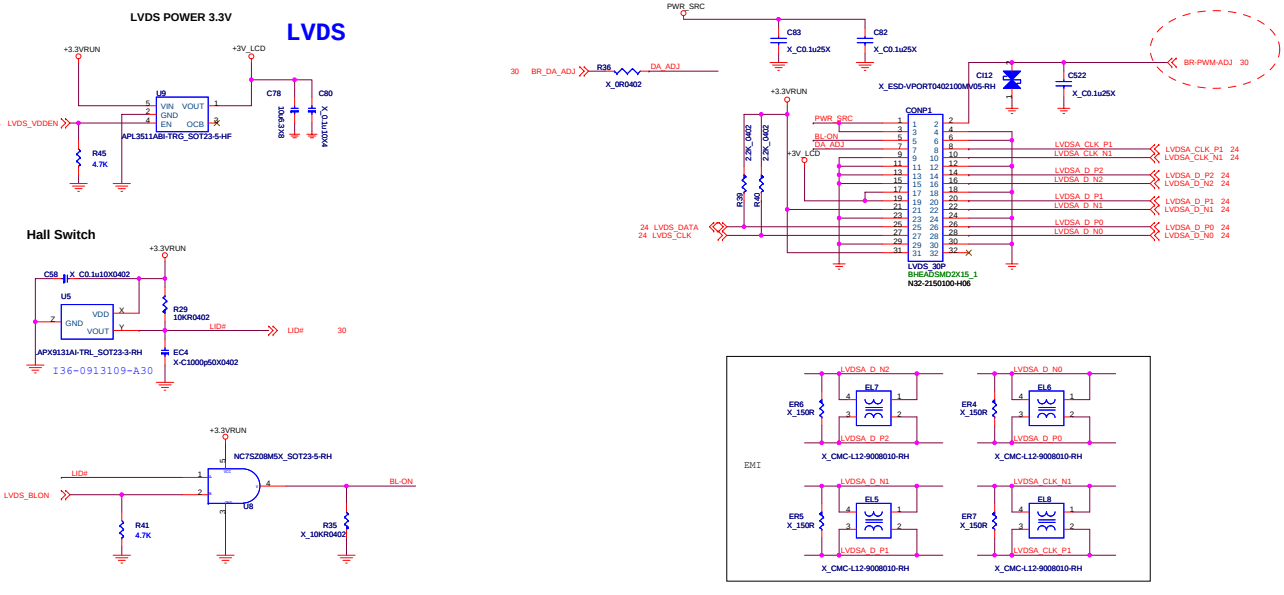
Title: **M92/Pak-Sx (Straps & Thermal)**

Size: B | Document Number: **MS-145X** | Rev: 10

Date: Tuesday, May 04, 2010 | Sheet 29 of 52

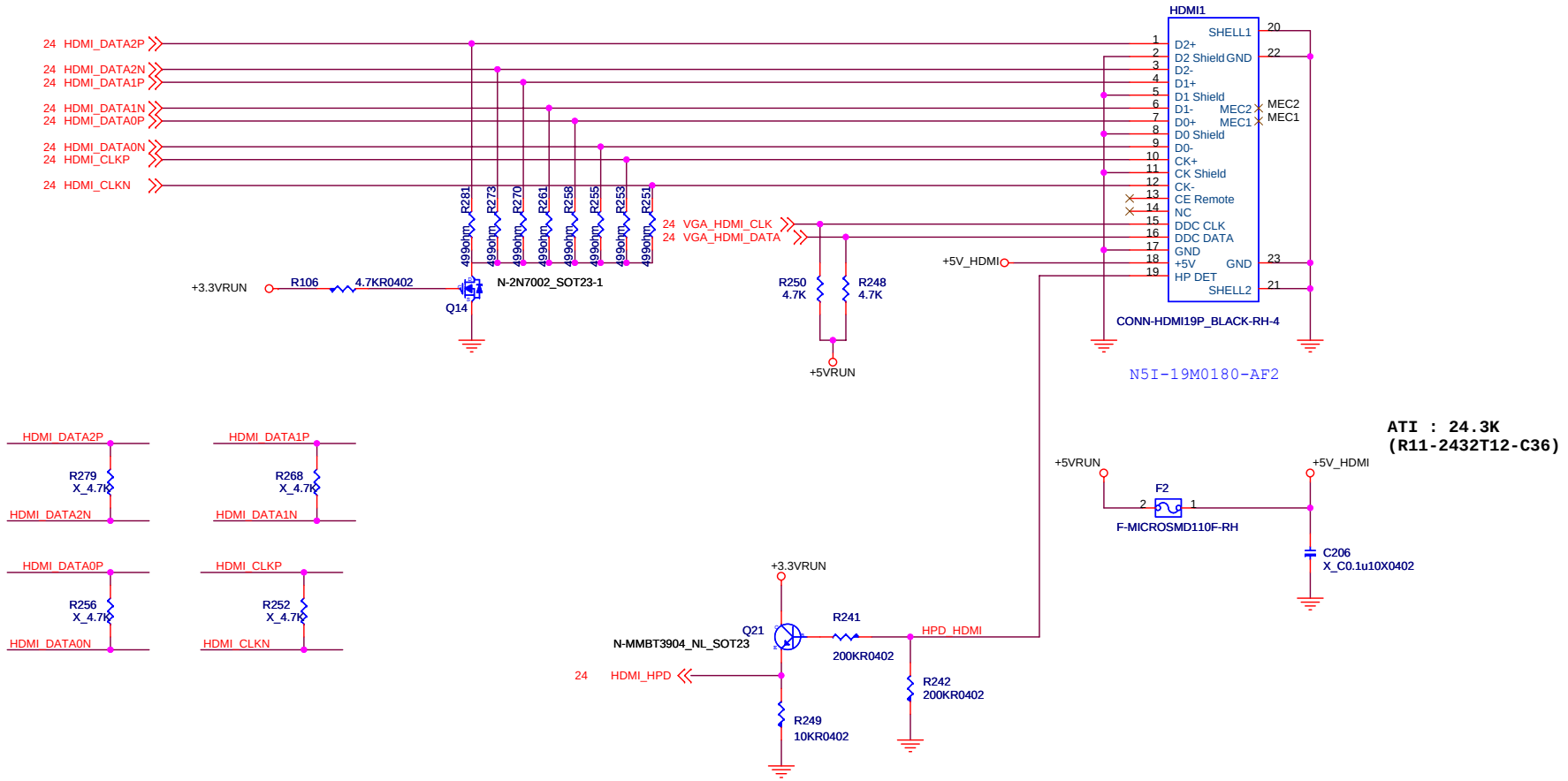

U11
LPC I/F
SERIRQ
LFRAME#
PCICLK
CLKRUN#/GPIO1D
LAD0
LAD1
LAD2
LAD3
ECRST#
KBRST#
SCI#/GPIO0E
GA20
PCIRST#
FAN&PWM
PWM0/GPIO0F
PWM1/GPIO10
GPIO11/PWM2
GPIO19/PWM3
FANPWM0/GPIO12
FANPWM1/GPIO13
FANFB0/GPIO14
FANFB1/GPIO15
IKB
KSO0/GPIO20/TP_TEST
KSO1/GPIO21/TP_PLL
KSO2/GPIO22/TP_ANA_TEST
KSO3/GPIO23/TP_ISP
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F/E51_RXD(ISP)
KSO16/GPIO48
KSO17/GPIO49
KSI0/GPIO30/E51TXD(ISP)
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34/EDI_CS
KSI5/GPIO35/EDI_CLK
KSI6/GPIO3/EDI_DIN
KSI7/GPIO37/EDI_DO
ESB
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT_O/ESB_DAT_I
CIR
GPIO40/CIR_RX
GPIO41/CIR_RLC_TX
GPIO0A/RLC_RX2
GPIO0D/RLC_TX2
SPI FLASH
MISO
MOSI
SPICLK/GPIO58
SPICS#
PS2 I/F
PSCLK2/GPIO4E
PSDAT2/GPIO4F
PSCLK1/GPIO4C
PSDAT1/GPIO4D
PSCLK0/GPIO4A/P80CLK
PSDAT0/GPIO4B/P80DAT
UART
E51TXD/GPIO16
E51RXD/GPIO17
XCLKI
XCLKO
V18R
POWER/GROUND
VCC
AVCC
AGND
GND
SMBUS
SDA0/GPIO45
SCL0/GPIO44
SDA1/GPIO47
SCL1/GPIO46
AD/DA
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
AD4/GPI42
AD5/GPI43
SDI
GPXIOA00/SDICS#
GPXIOA01/SDICLK
GPXIOA02/SDIMOSI
GPXIOA03
GPXIOA04
GPXIOA05
GPXIOA06
GPXIOA07
GPXIOA08
GPXIOA09
GPXIOA10
GPXIOA11
GPXIOD0
GPXIOD1
GPXIOD2
GPXIOD3
GPXIOD4
GPXIOD5
GPXIOD6
GPXIOD7
GPIO04
GPIO07/I_clk_8051
GPIO08/I_clk_peri
GPIO18
GPIO50
E51CS#/GPIO52
E51TMR0/GPIO54/WDT_LED#
E51INT1/GPIO56
GPIO57/XCLK32K
GPIO59/TEST_CLKSPICLKI
LED
GPIO1A/NUMLED#
E51TMR1/GPIO53/CAPSLED#
E51INT0/GPIO55/SCROLED#
KB3926QFD2-RH
B07-0392614-E18
+3.3VALW
+3.3VRUN
+3.3VSUS
+1.8VRUN
EMI
C167 X_0.1uF
C185 X_0.1uF
C143 0.1uF
C191 0.1uF
C194 4.7uF
EC27 X_0.1uF
EC20 X_0.1uF
R103 10KR0402
C197 X_C1u6.3V0402-RH
EC_RST#
R72 X_10KR0402 EC_A20M#
R78 10KR0402 EC_KB_RST#
R97 X_10KR0402 EC_SCI#
R101 X_10KR0402 EC_SMI#
SCI#/SMI# don't pull-up in checklist
R84 100KR0402 ENCHG
R73 X_100KR0402 RSMRST#
R104 X_10KR0402 PCI_CLKRUN#
R68 X_4.7KR R0402
R59 300R R0402
Q9 X_2N7002 SOT23SGD_T
Q8 X_2N7002 SOT23SGD_T
NB_PWRGD 15,19
SB_PWRGD
TP13
TP14
R67 X_10M
Y4 32.768KHZ12.5P_S-2
C111 C18p50N0402
C110 C18p50N0402
C102 C1u6.3V0402-RH
D04-0300800-T16
D04-0300121-R10
D04-0300220-T16
Q13 N-BSS138_SOT23
Q12 N-BSS138_SOT23
R96 2.2KR0402
R94 2.2KR0402
BATCLK_M
BATDATA_M
GFX_THERMAL_CLK
GFX_THERMAL_DATA
1.2VPWRGD-->NBPWRGD
KeyBoard
CON1
CONN-FPC25B_WHITE-RH
FPC_S25_3
N5A-25F0130-H06
C170 C100p50N0402
8p4C-100p50N0402
EC30
EC31
EC29
EC33
EC28
EC32
C64 C0.1u10X0402
U6
W25X80AVSSIG-RH
ROM: M31-25X8013-W03
SPI_HOLD#
EC_SPICLK_R
EC_WR#
ER1 22R
EC19 22pF
For SW Debug
JDP1
X_BH1X14HS-1.25PITCH_WHITE-RH
SPI CONNECTOR
JSPI1
R223 X_4.7K/4
R290 FOR EMI
1683:N32-1100240-A81
MICRO-STAR INT'L CO.,LTD
MS-168x
Size Custom
Document Description ENE3926
Rev 0A
Date: Wednesday, May 05, 2010
Sheet 30 of 52



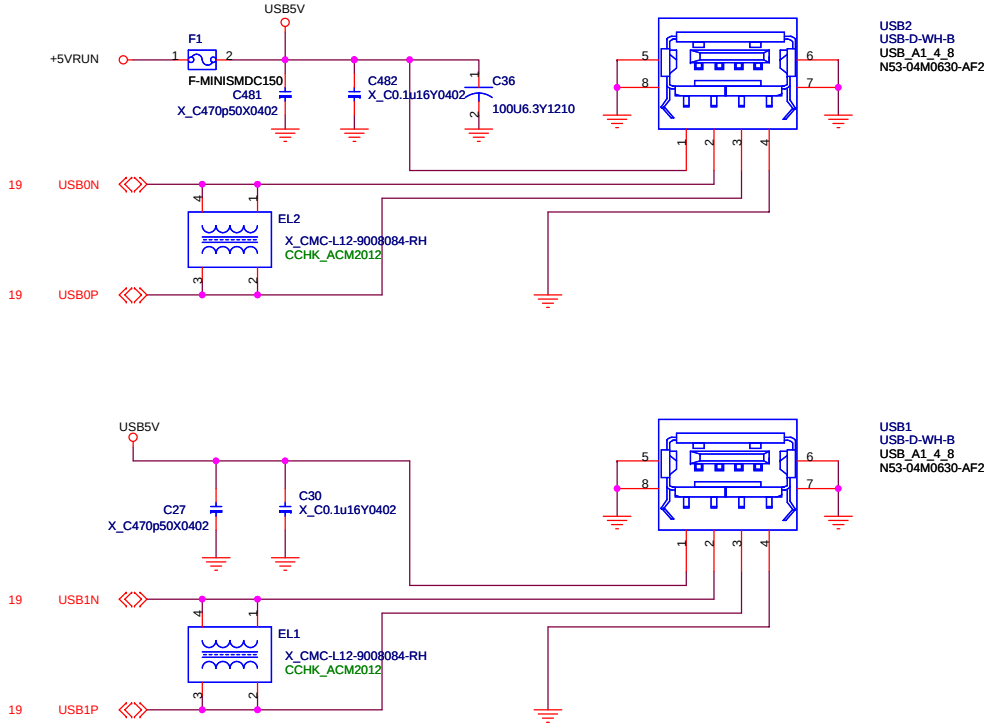



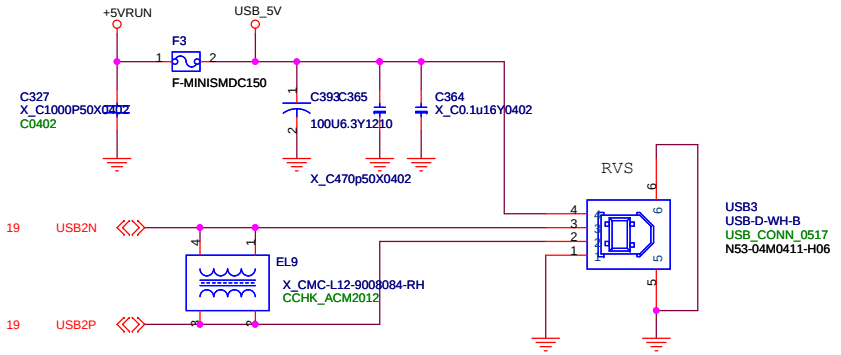

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD | |
| MS-168x | |
| Size: Custom | Document Description: LVDS and CRT |
| Rev: 0A | |
| Date: Wednesday, May 05, 2010 | Sheet 31 of 52 |

# HDMI

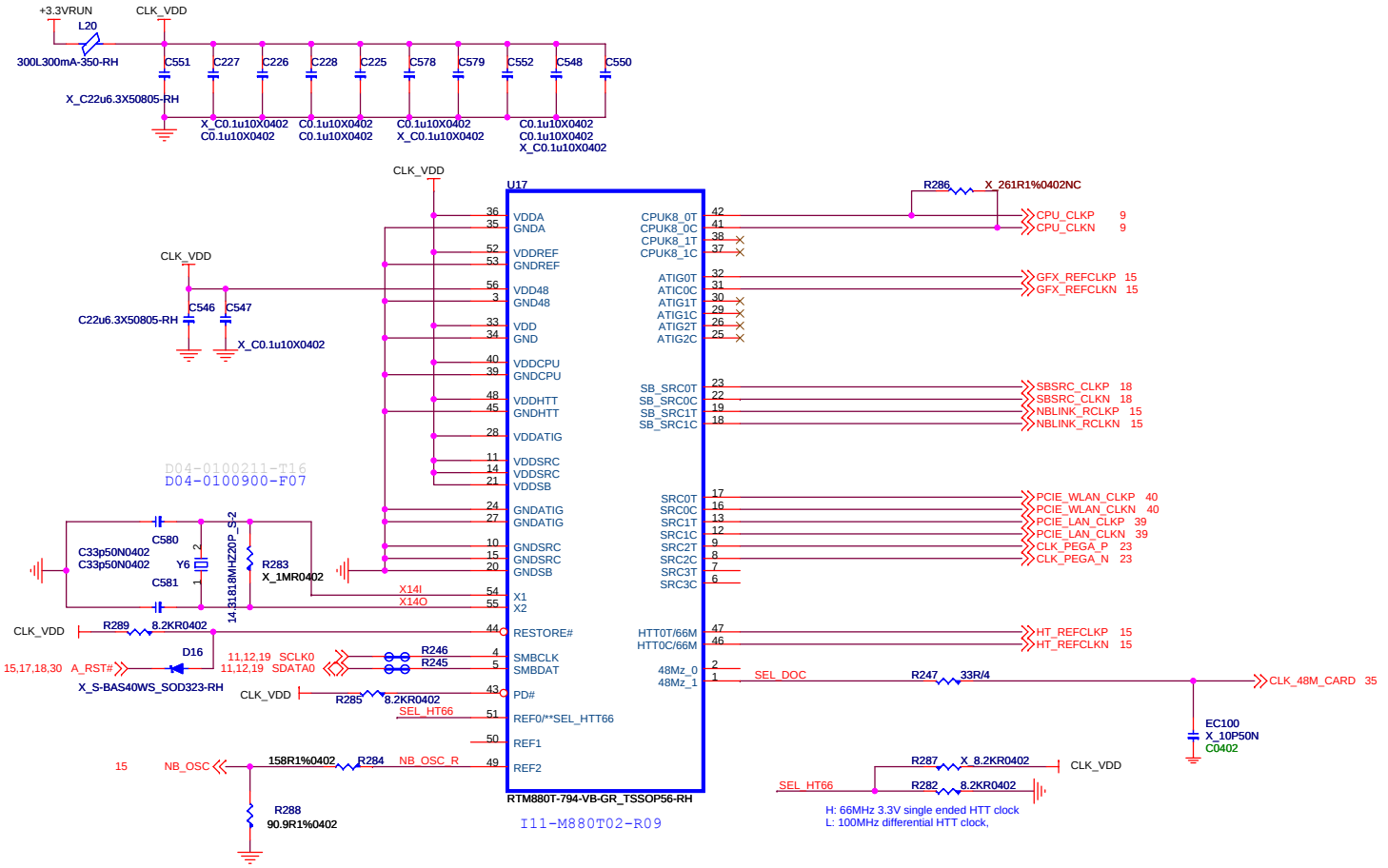



| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-168x | | |
| Size: B | Document Description: HDMI | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 32 of 52 | |



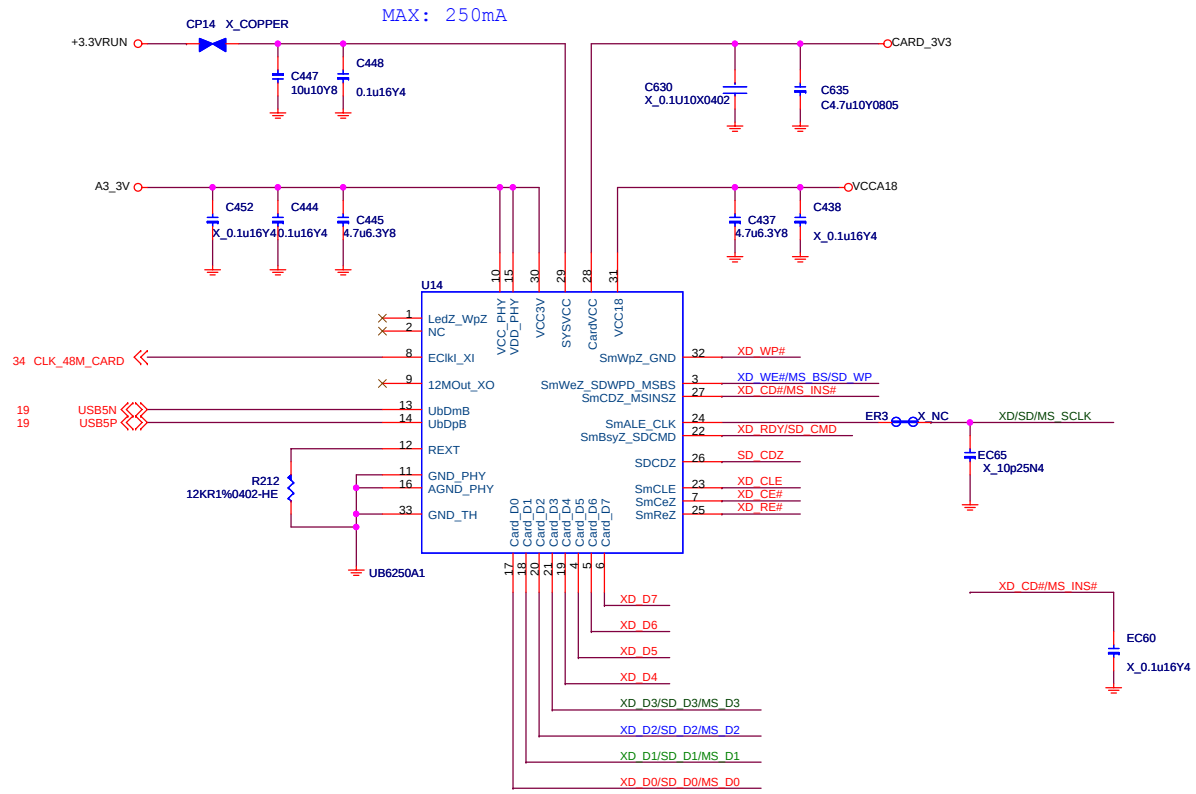




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | | |
| MS-168x | | | |
| Size: Custom | Document Description: USB and ESATA | | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 33 of 52 | | |

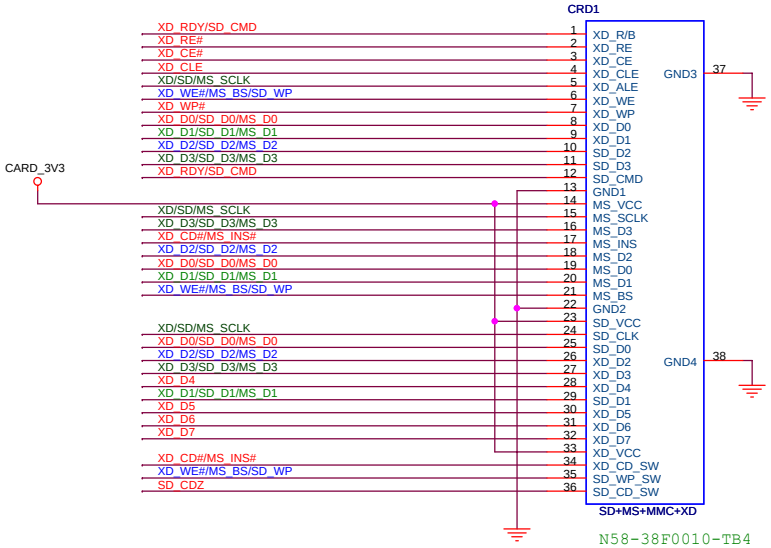



| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: Custom | Document Description: UB6250 | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 34 of 52 | |

# Card Reader controller

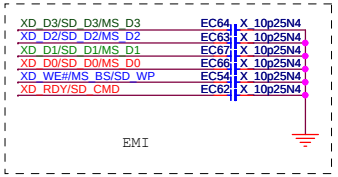



## Flash Card Socket




ENE UB6250 USB20 Flash Card Reader Controller
Pins for SD, MMC, MS, and xD memory cards

| Name | No | I/O | XD | SD | MMC | MS |
|---|---|---|---|---|---|---|
| xDCeZ | 7 | O | xD card EN | | | |
| xDCle | 23 | O | xD CMD latch EN | | | |
| xDAle | 24 | O | xD ADDR latch EN | SD clock | MMC clock | MS serial clock |
| xDBsyZ | 22 | B | xD Ready/busy | SD CMD/response | MMC CMD/response | |
| xDData0 | 17 | B | xD D0 | SD D0 | MMC D0 | MS D0 |
| xDData1 | 18 | B | xD D1 | SD D1 | MMC D1 | MS D1 |
| xDData2 | 20 | B | xD D2 | SD D2 | MMC D2 | MS D2 |
| xDData3 | 21 | B | xD D3 | SD D3 | MMC D3 | MS D3 |
| xDData4 | 19 | B | xD D4 | | MMC D4 | MS D4 |
| xDData5 | 4 | B | xD D5 | | MMC D5 | MS D5 |
| xDData6 | 5 | B | xD D6 | | MMC D6 | MS D6 |
| xDData7 | 6 | B | xD D7 | | MMC D7 | MS D7 |
| xDWeZ | 3 | B | xD W EN | SD WP | | MS Busy |
| xDReZ | 25 | O | xD R EN | | | |
| xDWpZ | 32 | O | xD WP | | | |
| SdCdZ | 26 | I | | SD CD | MMC CD | |
| xDCdZ | 27 | I | xD CD | | | MS CD |



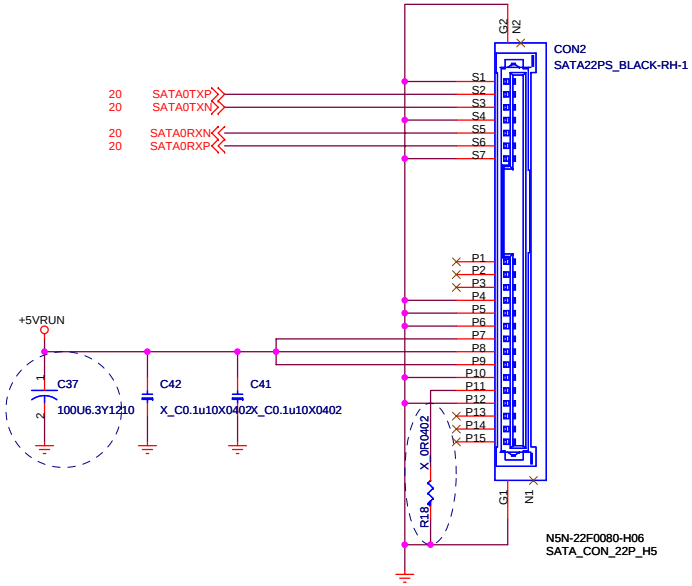

MICRO-STAR INT'L CO.,LTD

MS-168x

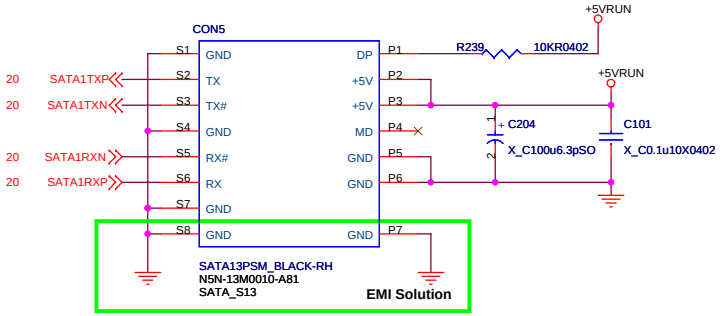
| Size | Document Description | Rev |
|---|---|---|
| Custom | UB6250 | 0A |

Date: Wednesday, May 05, 2010 Sheet 35 of 52

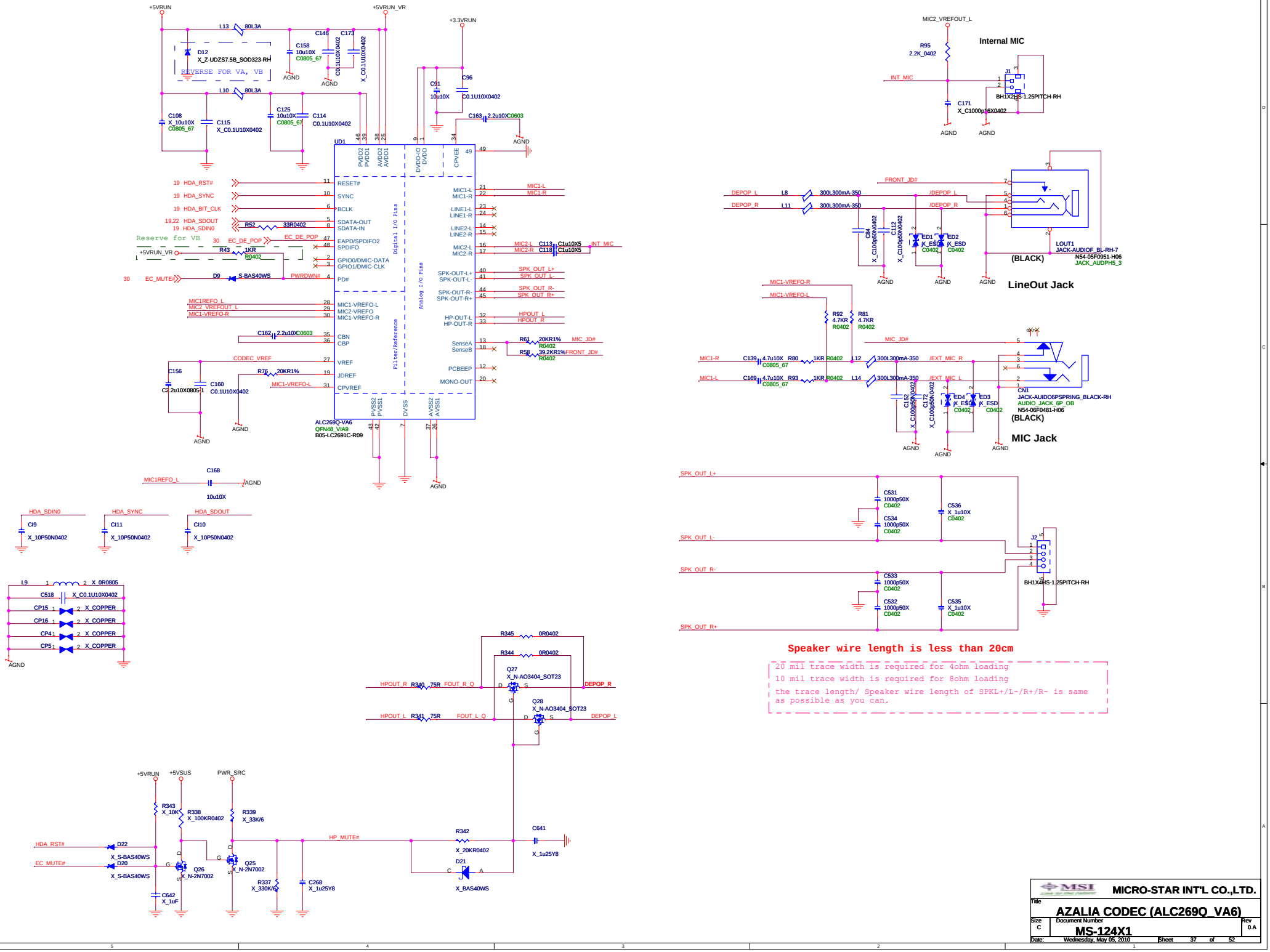
## SATA HDD




## SATA ODD




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-168x | | |
| Size: Custom | Document Description: HDD/ODD/NEW CARD | Rev: 0A |
| Date: Wednesday, April 21, 2010 | Sheet 36 of 52 | |




**Speaker wire length is less than 20cm**

20 mil trace width is required for 4ohm loading
10 mil trace width is required for 8ohm loading
the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same as possible as you can.

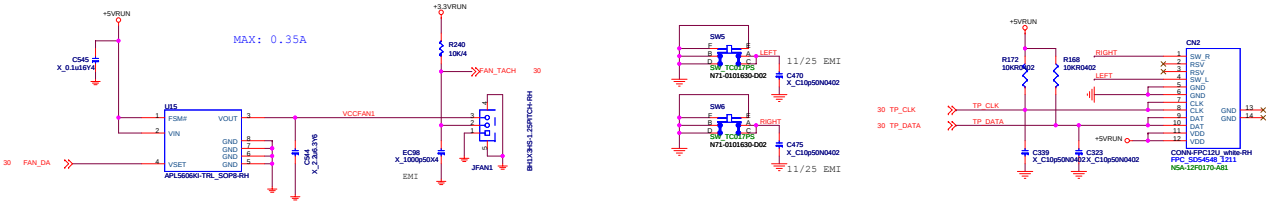
MICRO-STAR INT'L CO.,LTD.

Title: AZALIA CODEC (ALC269Q_VA6)

| Size | Document Number | Rev |
|---|---|---|
| C | MS-124X1 | 0.A |

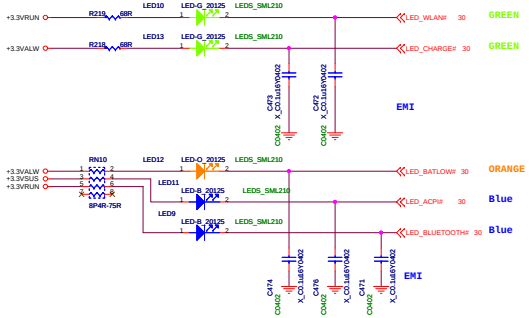
Date: Wednesday, May 05, 2010 Sheet 37 of 52

## FAN

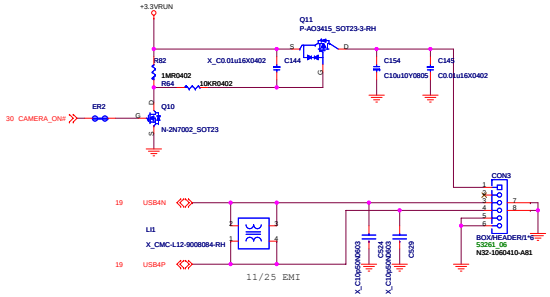



## LED light

del CN8 0716



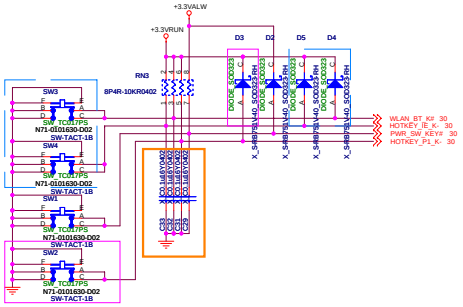

## CAMERA

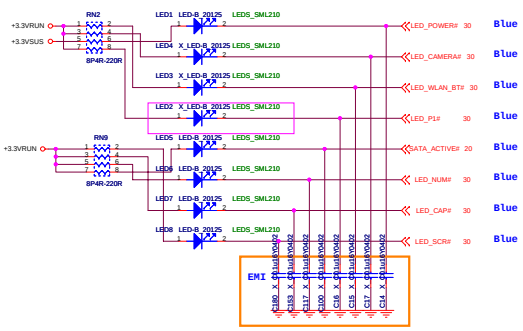



| | LED7 SW7 | LED8 SW8 | LED9 SW9 | LED10 SW10 |
|---|---|---|---|---|
| 1453 | Stuff | Nostuff | Discreate | UMA |
| 1454 | Stuff | Nostuff | P1 | IE |
| OEM | Stuff | P1 | Wireless | Camera |

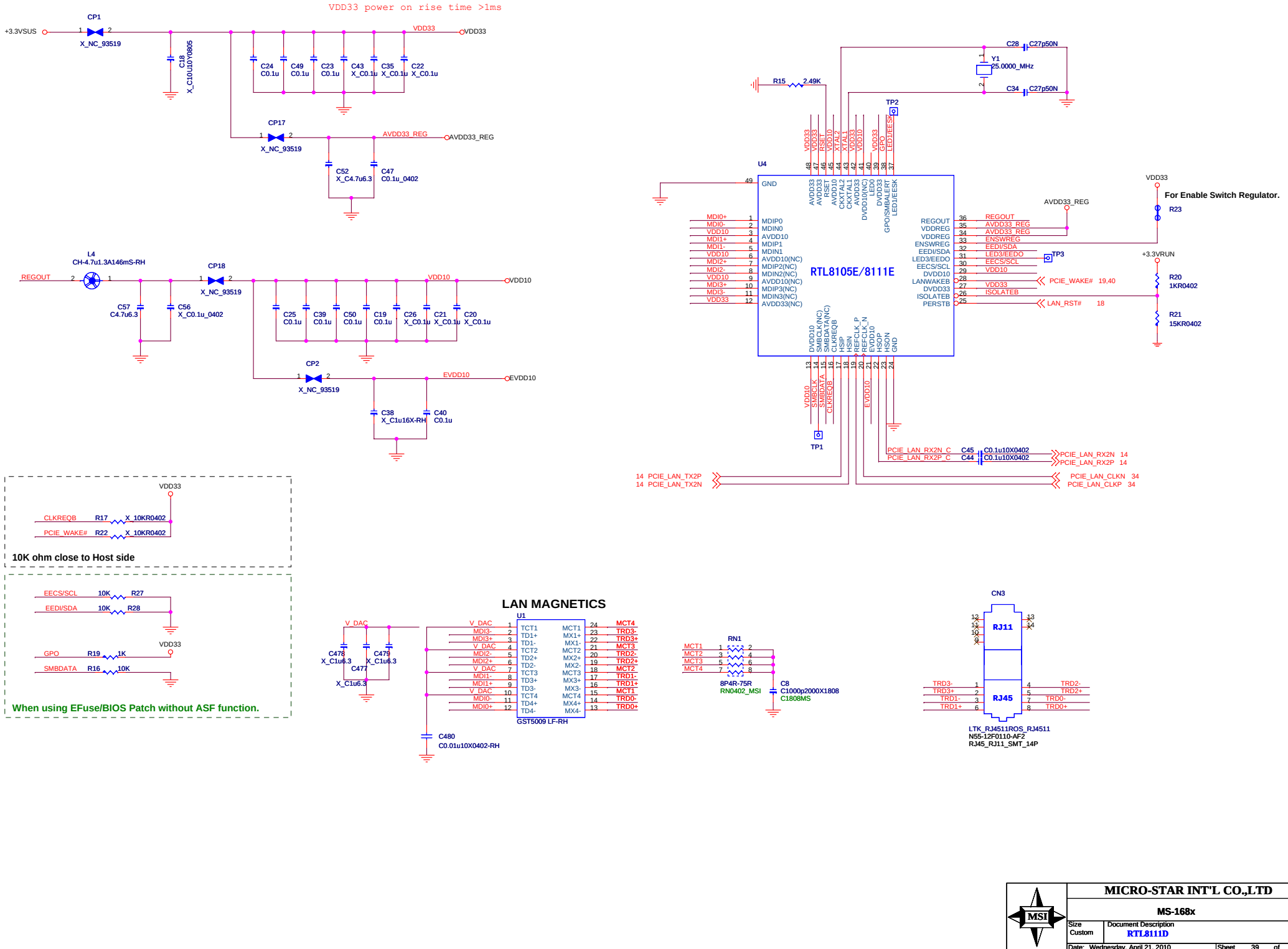
Stuff for CHANNEL

Stuff for OEM



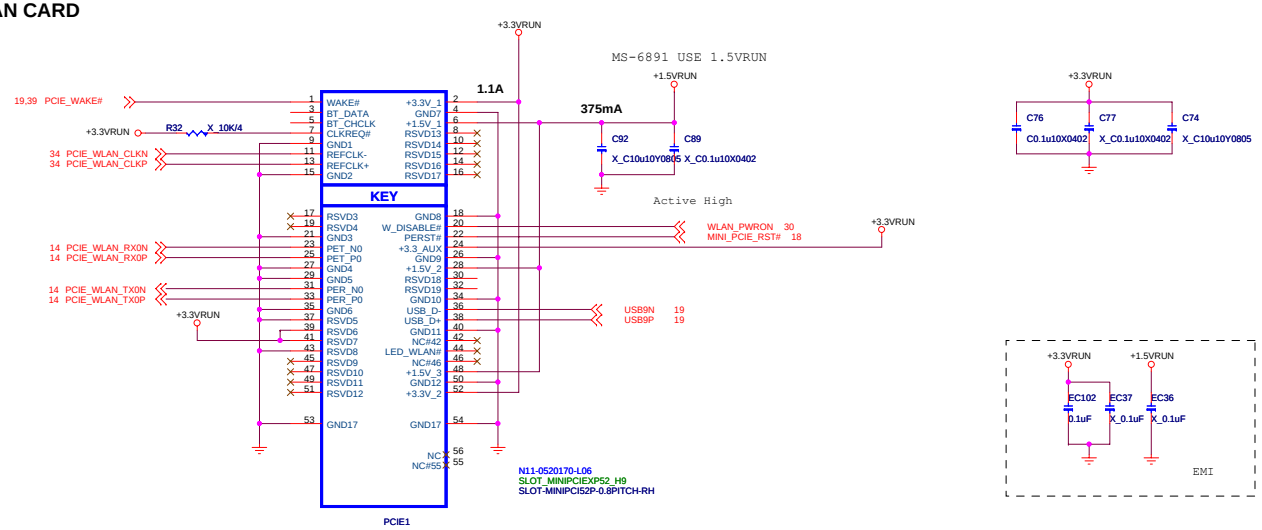




| MICRO-STAR INT'L CO.,LTD | | |
|---|---|---|
| MS-168x | | |
| Size: Custom | Document Description: FAN/LED/TP | Rev: 0A |
| Date: Tuesday, May 04, 2010 | Sheet 38 of 52 | |




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-168x | | |
| Size: Custom | Document Description: RTL8111D | Rev: 0A |
| Date: Wednesday, April 21, 2010 | Sheet 39 of 52 | |

## WLAN CARD

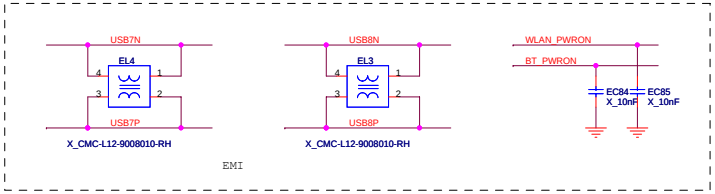


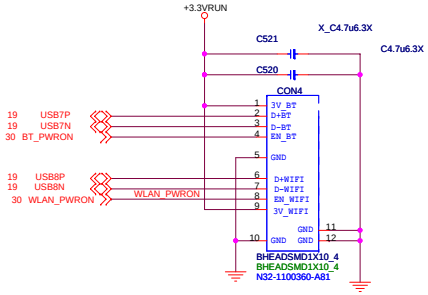






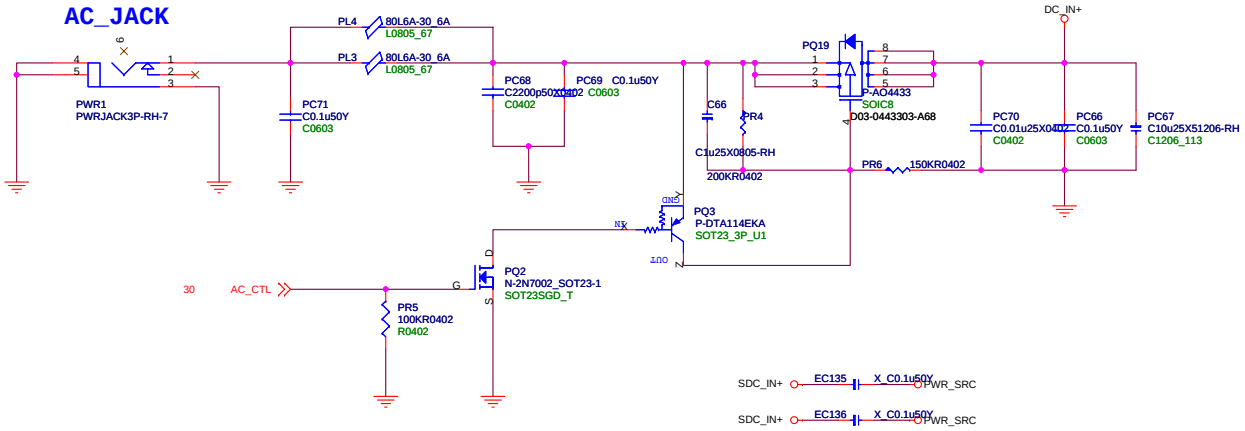

## BLUETOOTH AND WLAN

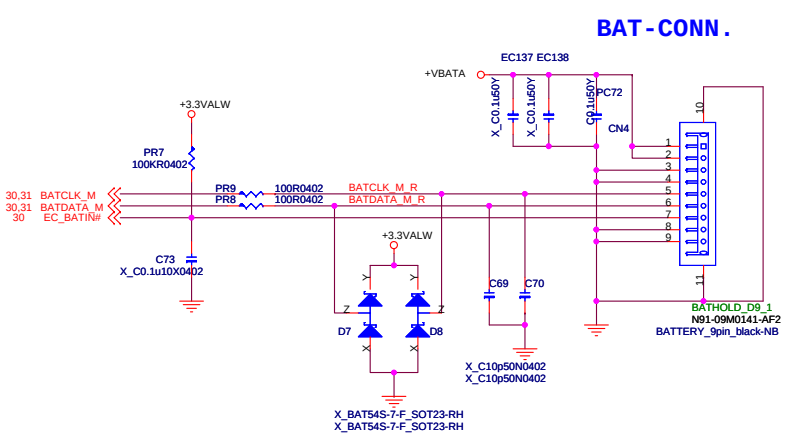


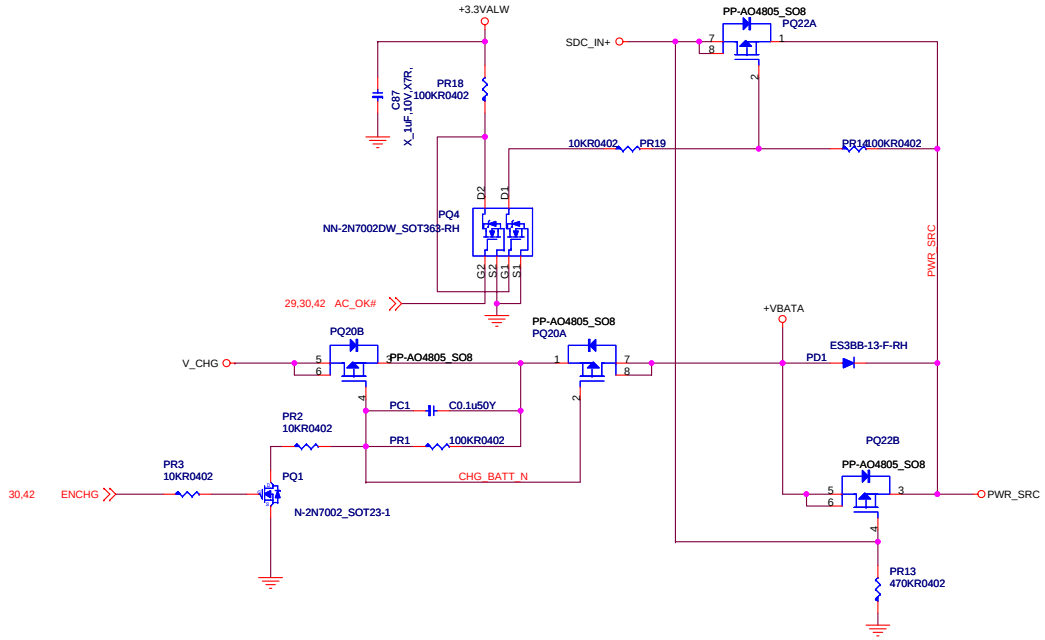




**MS-3870 COLAY MS-3801**

| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: C | Document Description: CAMERA/BT | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 40 of 52 | |

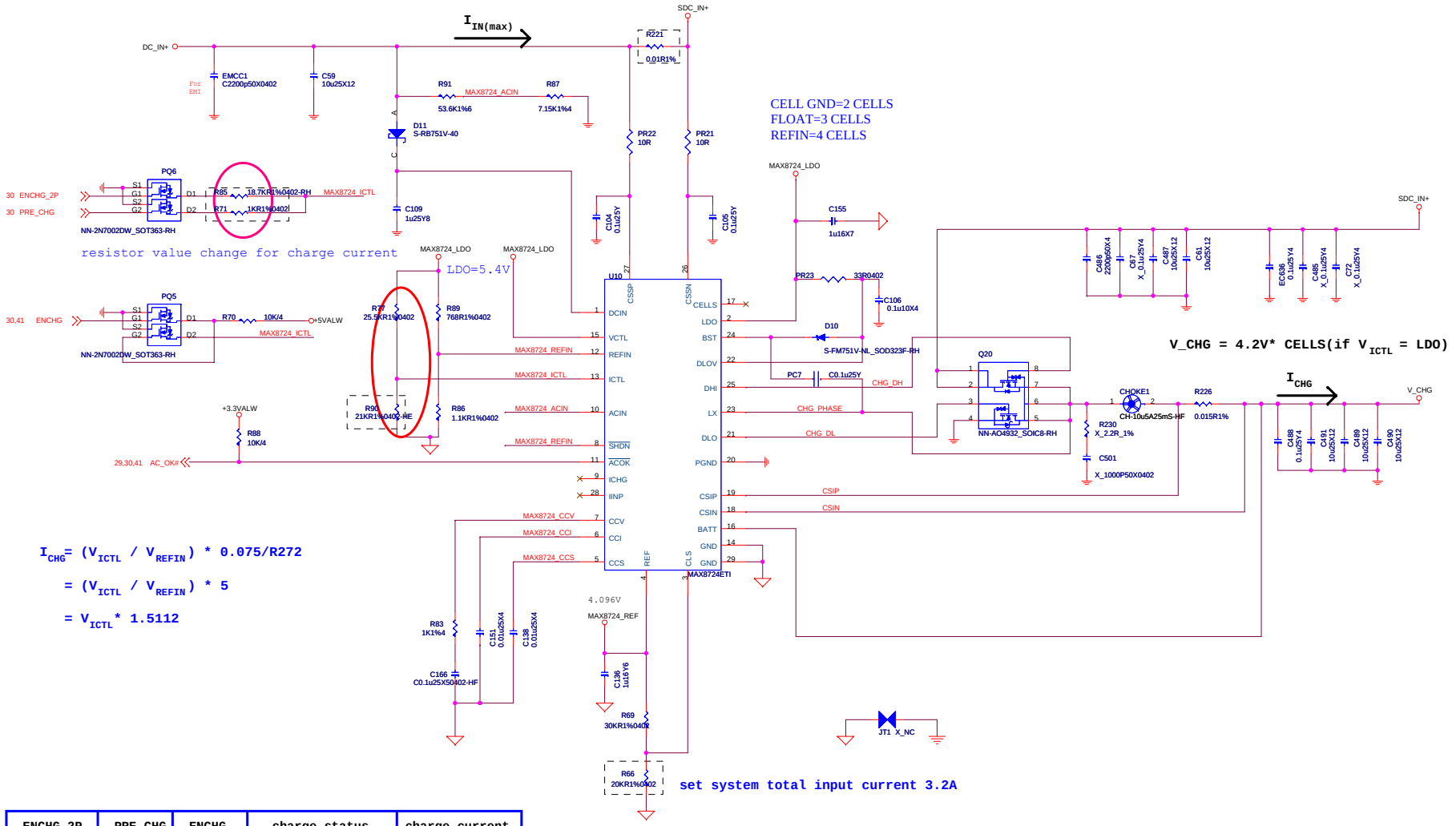



| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-1457 | |
| Size: Custom | Document Description: Battery SELECT | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 41 of 52 | |

**Adapter= 65W**
**Adapter input voltage set 19 Voltage** 3.2 Amps




V_CHG = 4.2V* CELLS(if $V_{ICTL}$ = LDO)

$I_{CHG}$= ($V_{ICTL}$ / $V_{REFIN}$) * 0.075/R272

= ($V_{ICTL}$ / $V_{REFIN}$) * 5

= $V_{ICTL}$* 1.5112

set system total input current 3.2A

| ENCHG-2P | PRE_CHG | ENCHG | charge status | charge current |
|---|---|---|---|---|
| 0 | 1 | 1 | Pre-charge | 220 mA |
| 1 | 0 | 1 | 3S2P-Fast charge | 2.2A |
| 0 | 0 | 1 | 3S3P-Fast charge | 3.5 A |
| X | X | 0 | STOP CHARGE | 0 |

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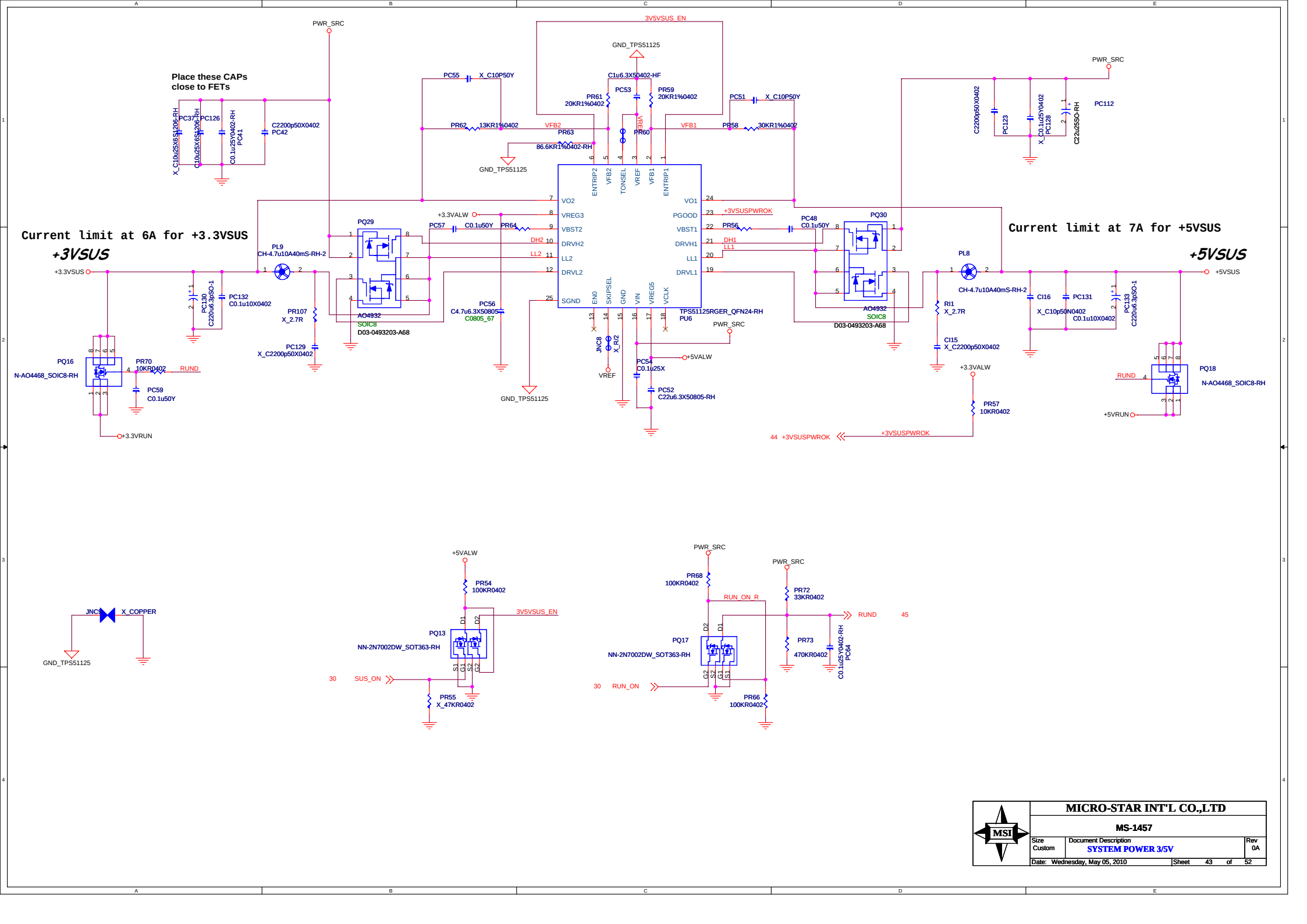
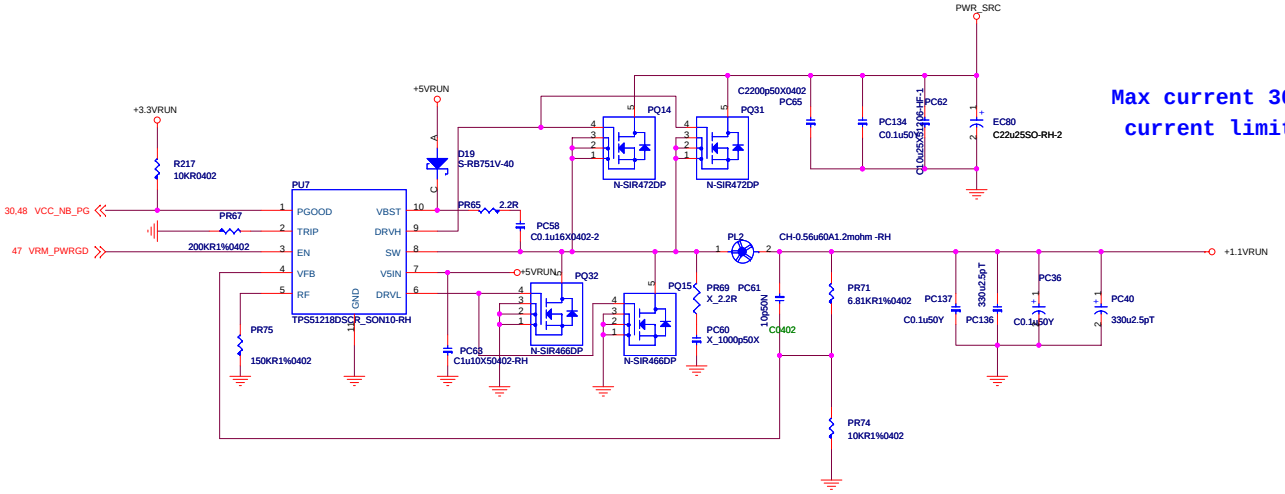
MS-1457

Size C | Document Description CHARGER | Rev 0A

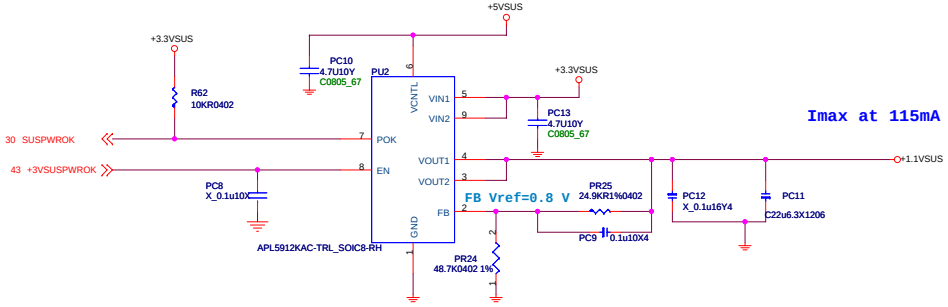
Date: Wednesday, May 05, 2010 | Sheet 42 of 52



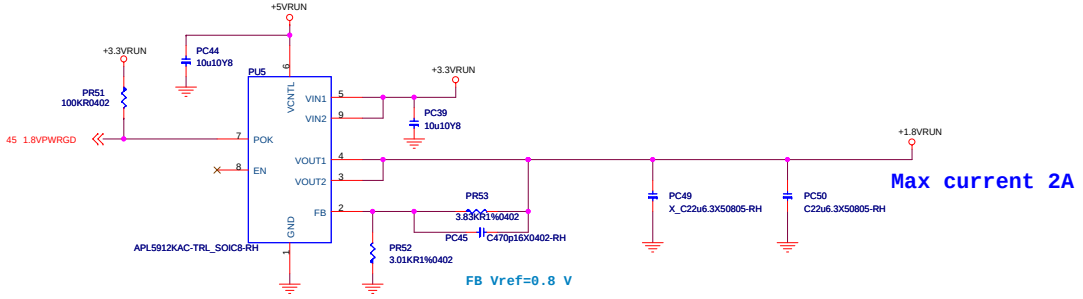

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD | |
| MS-1457 | |
| Size: Custom | Document Description: SYSTEM POWER 3/5V |
| Rev: 0A | |
| Date: Wednesday, May 05, 2010 | Sheet 43 of 52 |




Max current 30A
current limit 35A

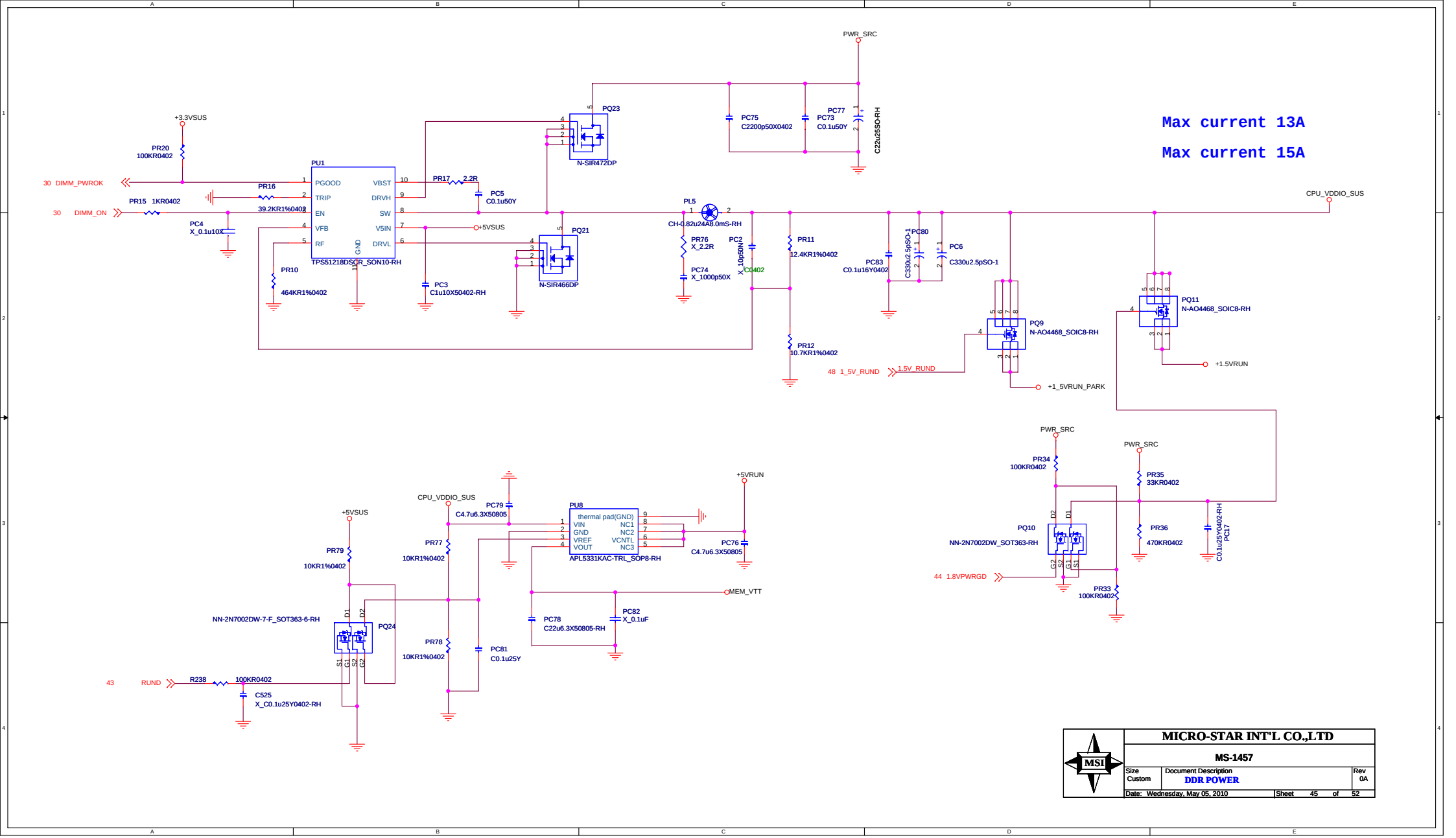



Imax at 115mA

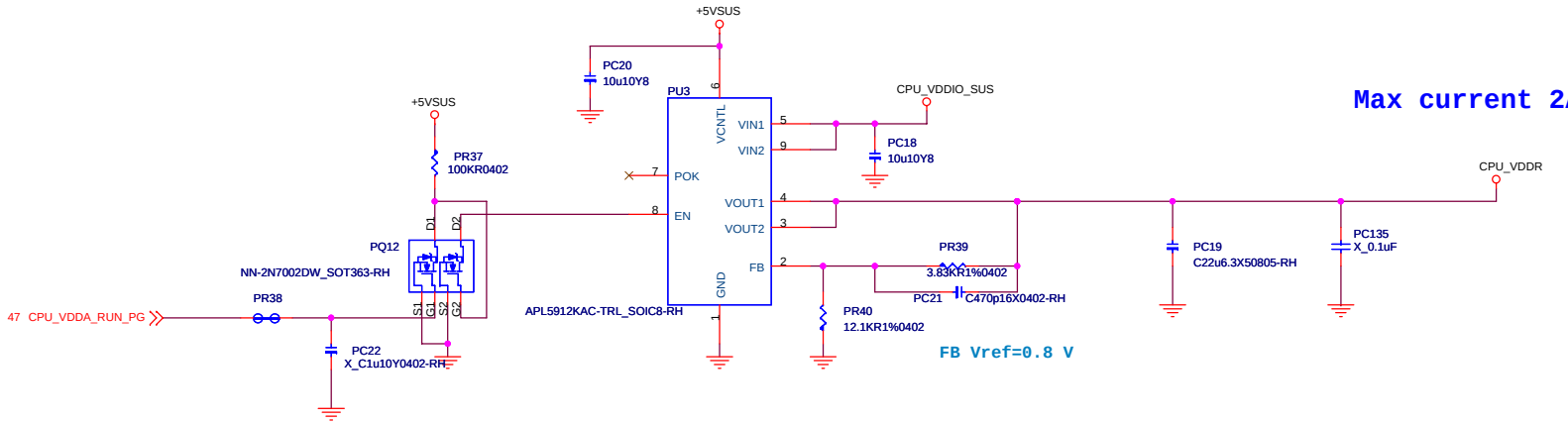


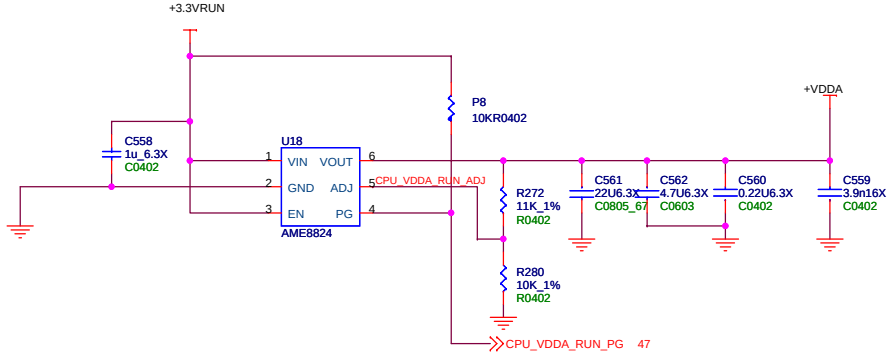

Max current 2A

| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-1457 | |
| Size C | Document Description 1.5V 2.5V VLDT | Rev 0A |
| Date: Wednesday, May 05, 2010 | Sheet 44 of 52 | |

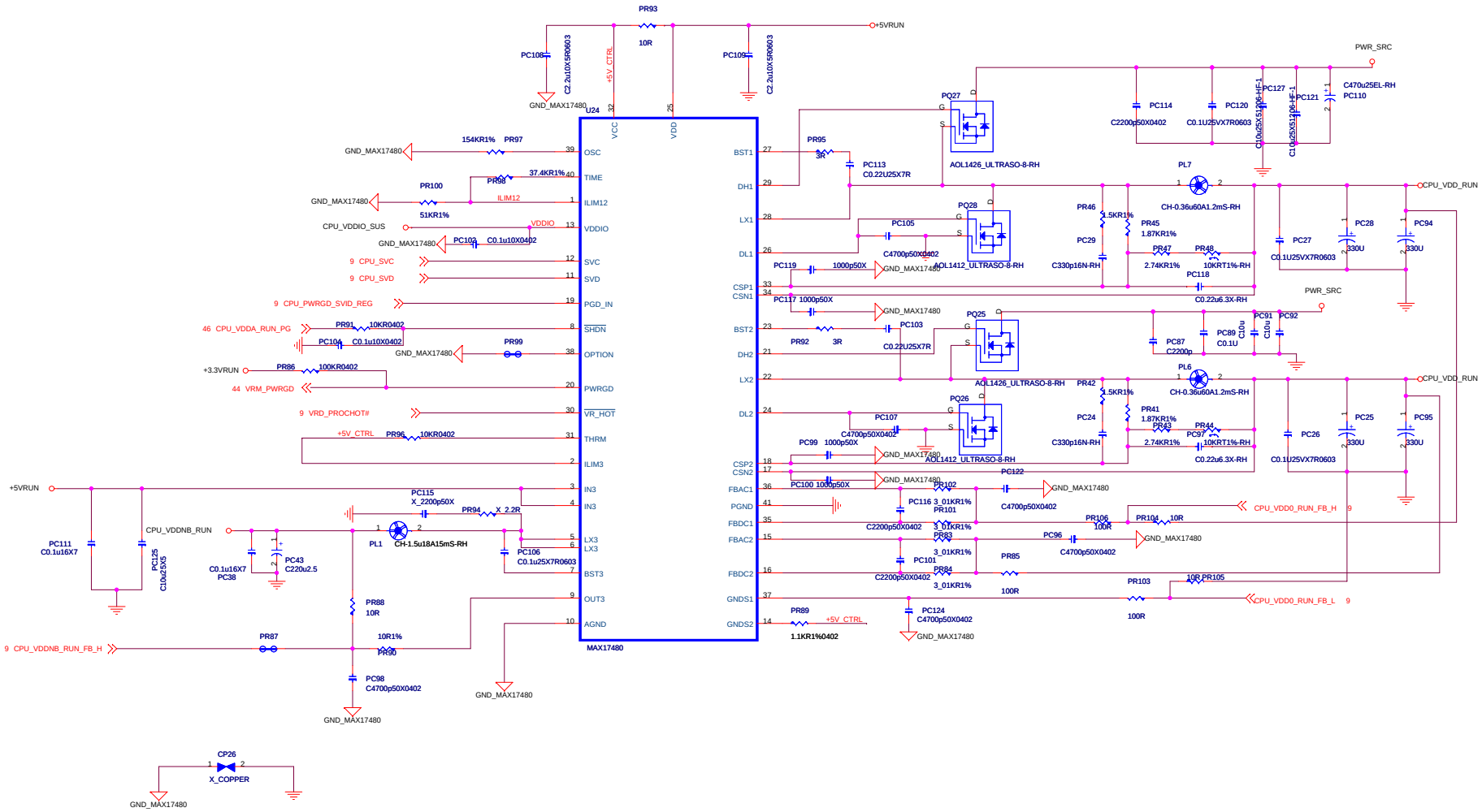



| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-1457 | |
| Size: Custom | Document Description: DDR POWER | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 45 of 52 | |



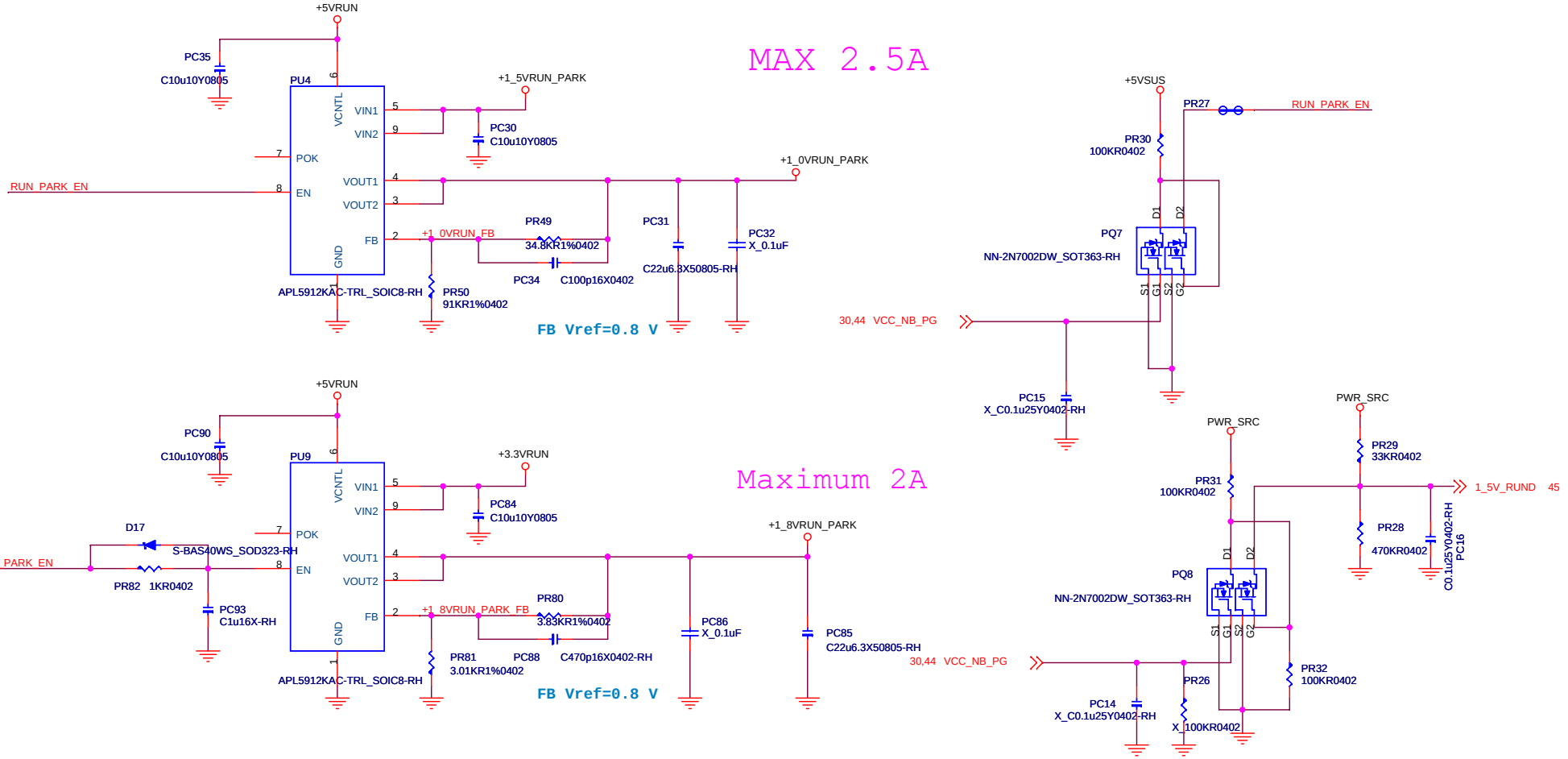




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD | | |
| MS-1457 | | |
| Size: Custom | Document Description: NB SB CORE PWR | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 46 of 52 | |



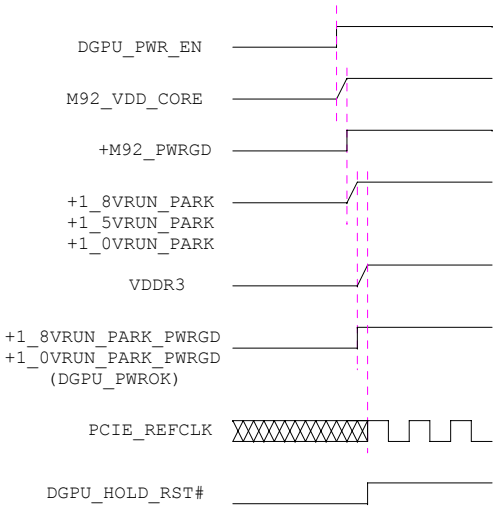

| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: CPU CORE PWR | | | |
| Size: C | Document Number: MS-1457 | | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 47 of 52 | | |

Resistors value is depend on GPU type

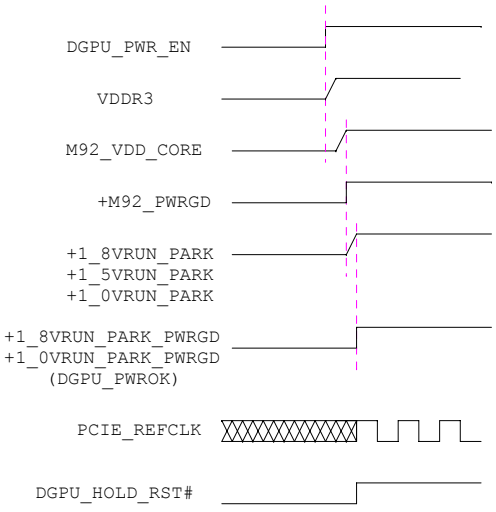



| | | |
|---|---|---|
| MSI CORPORATION | | |
| Title: M92/Pak Power | | |
| Size: B | Document Number: MS-1457 | Rev: A |
| Date: Wednesday, May 05, 2010 | Sheet 48 of 52 | |

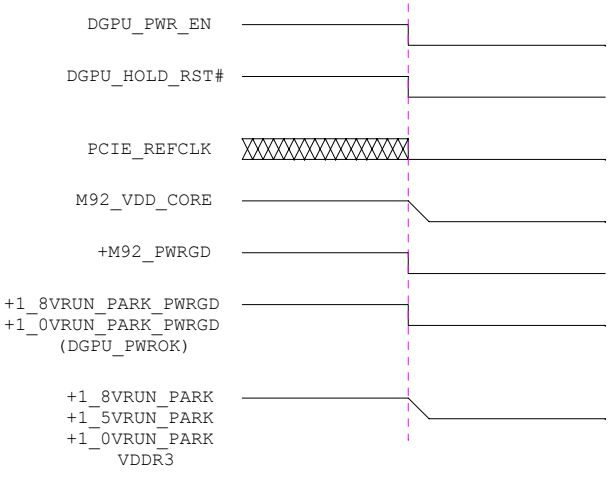
## M92 Power on Sequence



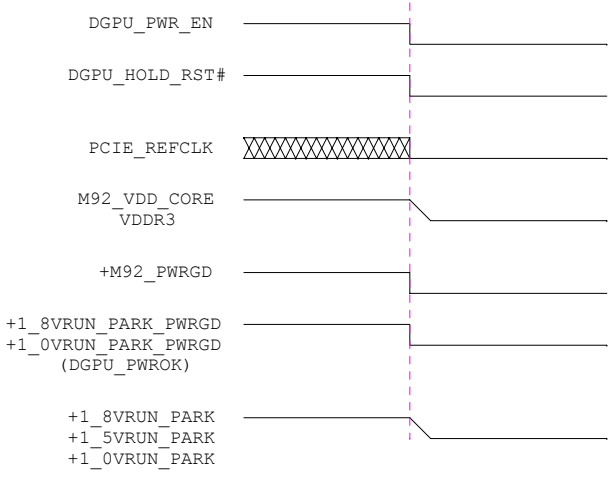

## PARK Power on Sequence




## M92 Power down Sequence




## PARK Power down Sequence

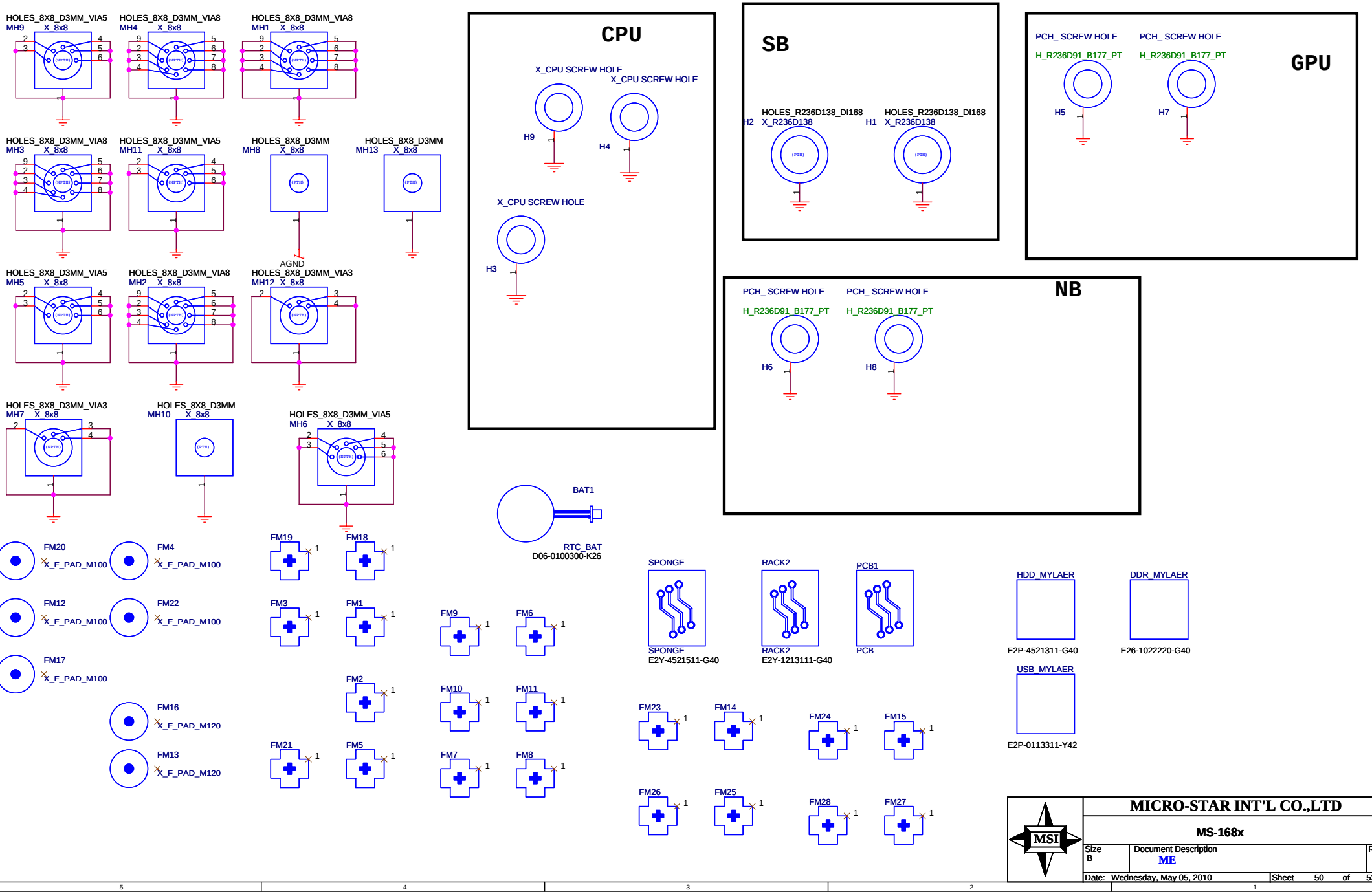



MICRO-STAR INT'L CO.,LTD.

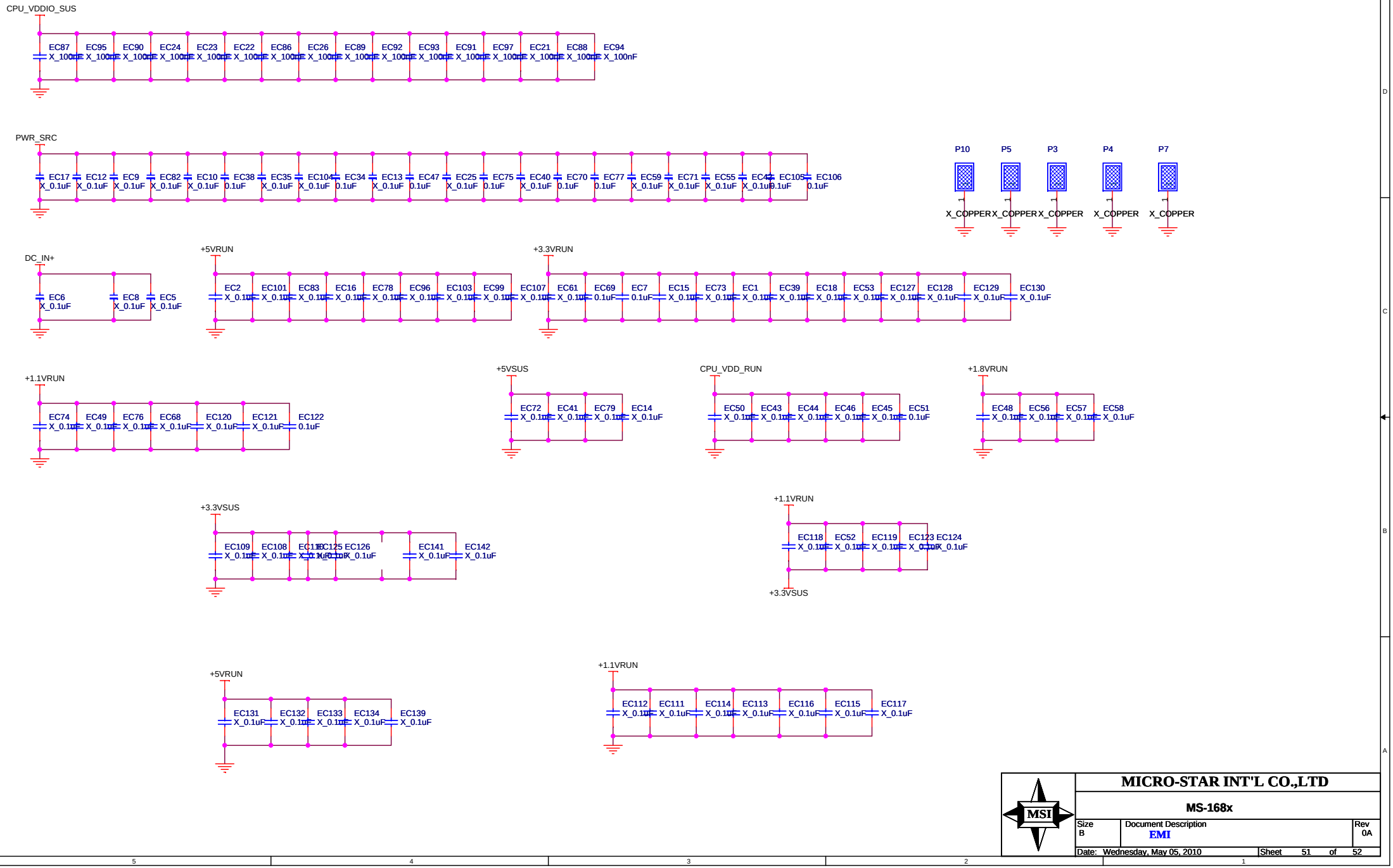
Title: M92/PARK Power down Sequence

| Size | Document Number | Rev |
|---|---|---|
| C | MS-145X | 10 |

Date: Tuesday, March 23, 2010 Sheet 49 of 52




| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size B | Document Description ME | Rev 0A |
| Date: Wednesday, May 05, 2010 | Sheet 50 of 52 | |




| | | |
|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD | |
| | MS-168x | |
| Size: B | Document Description: EMI | Rev: 0A |
| Date: Wednesday, May 05, 2010 | Sheet 51 of 52 | |

## Single ended

SIP5
L6_10mil_40ohm
X_PIN1*2

SIP3
L4_8.5mil_40ohm
X_PIN1*2

SIP14
L6_6mil_45ohm
X_PIN1*2

SIP2
L4_7mil_45ohm
X_PIN1*2

SIP4
L1_10mil_40ohm
X_PIN1*2

SIP11
L3_8.5mil_40ohm
X_PIN1*2

SIP15
L1_6mil_45ohm
X_PIN1*2

SIP33
L3_7mil_45ohm
X_PIN1*2

SIP1
L6_6.5mil_50ohm
X_PIN1*2

SIP13
L4_5.5mil_50ohm
X_PIN1*2

SIP8
L1_6.5mil_50ohm
X_PIN1*2

SIP32
L3_5.5mil_50ohm
X_PIN1*2

SIP6
L6_5mil_55ohm
X_PIN1*2

SIP9
L4_4.5mil_55ohm
X_PIN1*2

SIP10
L1_5mil_55ohm
X_PIN1*2

SIP31
L3_4.5mil_55ohm
X_PIN1*2

SIP12
L6_4mil_60ohm
X_PIN1*2

SIP7
L4_4mil_60ohm
X_PIN1*2

SIP36
L3_4mil_60ohm
X_PIN1*2

SIP17
L1_4mil_60ohm
X_PIN1*2

## Differential signal

SIP28
L1_DIFF_5/4.5/5_85 Ohm-
L1_DIFF_5/4.5/5_85 Ohm+
X_H1X4_black-RH

SIP29
L3_DIFF_4.5/5.5/4.5_85 Ohm-
L3_DIFF_4.5/5.5/4.5_85 Ohm+
X_H1X4_black-RH

SIP27
L6_DIFF_5/4.5/5_85 Ohm-
L6_DIFF_5/4.5/5_85 Ohm+
X_H1X4_black-RH

SIP25
L4_DIFF_4.5/5.5/4.5_85 Ohm-
L4_DIFF_4.5/5.5/4.5_85 Ohm+
X_H1X4_black-RH

SIP26
L1_DIFF_5/5/5_90 Ohm-
L1_DIFF_5/5/5_90 Ohm+
X_H1X4_black-RH

SIP30
L3_DIFF_5/6/5_90 Ohm-
L3_DIFF_5/6/5_90 Ohm+
X_H1X4_black-RH

SIP21
L6_DIFF_5/5/5_90 Ohm-
L6_DIFF_5/5/5_90 Ohm+
X_H1X4_black-RH

SIP22
L4_DIFF_5/6/5_90 Ohm-
L4_DIFF_5/6/5_90 Ohm+
X_H1X4_black-RH

SIP23
L1_DIFF_4.5/5/4.5_93 Ohm-
L1_DIFF_4.5/5/4.5_93 Ohm+
X_H1X4_black-RH

SIP34
L3_DIFF_4.5/7/4.5_93 Ohm-
L3_DIFF_4.5/7/4.5_93 Ohm+
X_H1X4_black-RH

SIP18
L6_DIFF_4.5/5/4.5_93 Ohm-
L6_DIFF_4.5/5/4.5_93 Ohm+
X_H1X4_black-RH

SIP19
L4_DIFF_4.5/7/4.5_93 Ohm-
L4_DIFF_4.5/7/4.5_93 Ohm+
X_H1X4_black-RH

SIP20
L1_DIFF_4/7/4_100 Ohm-
L1_DIFF_4/7/4_100 Ohm+
X_H1X4_black-RH

SIP35
L3_DIFF_4/8/4_100 Ohm-
L3_DIFF_4/8/4_100 Ohm+
X_H1X4_black-RH

SIP24
L6_DIFF_4/7/4_100 Ohm-
L6_DIFF_4/7/4_100 Ohm+
X_H1X4_black-RH

SIP16
L4_DIFF_4/8/4_100 Ohm-
L4_DIFF_4/8/4_100 Ohm+
X_H1X4_black-RH

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MS-168x

| Size | Document Description | Rev |
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