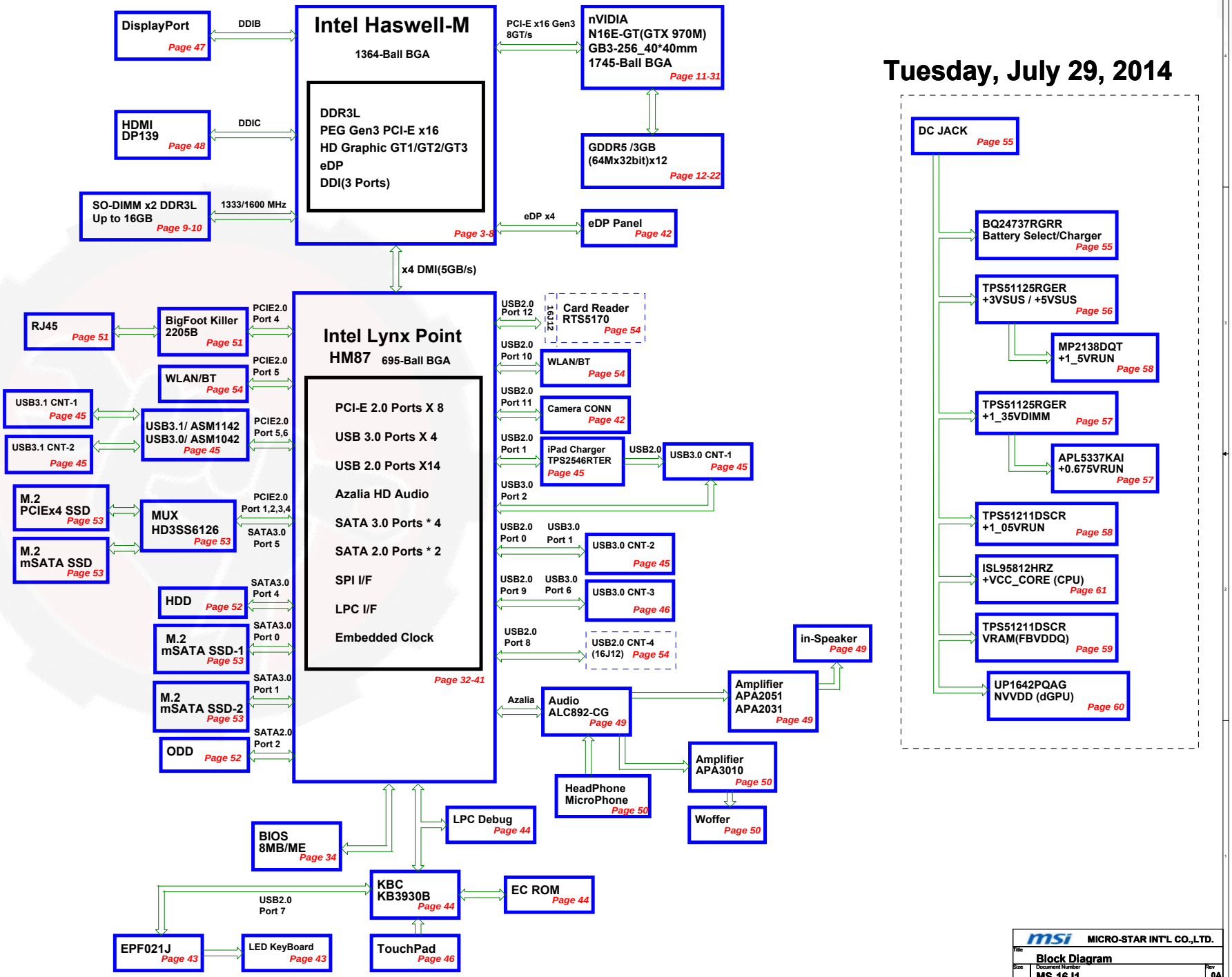
MS-16J1 Ver:0A Shark Bay Mobile



Tuesday, July 29, 2014

msi MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

Size | Document Number: MS-16J1 | Rev: 0A

Date: | Sheet 1 of 70

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	DIMM_ON
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	RUN_ON
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	V Core Voltage for nVIDIA dGPU	NVVDD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVDD_EN

Net Naming Conventions

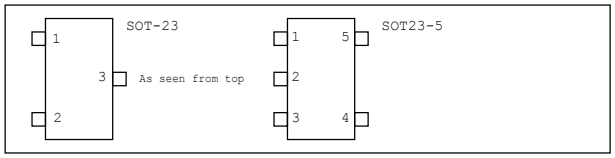
Suffix

```
#  =  Active Low Signal
```

Prefix

```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

MICRO-STAR INT'L CO.,LTD.

Title: Platform

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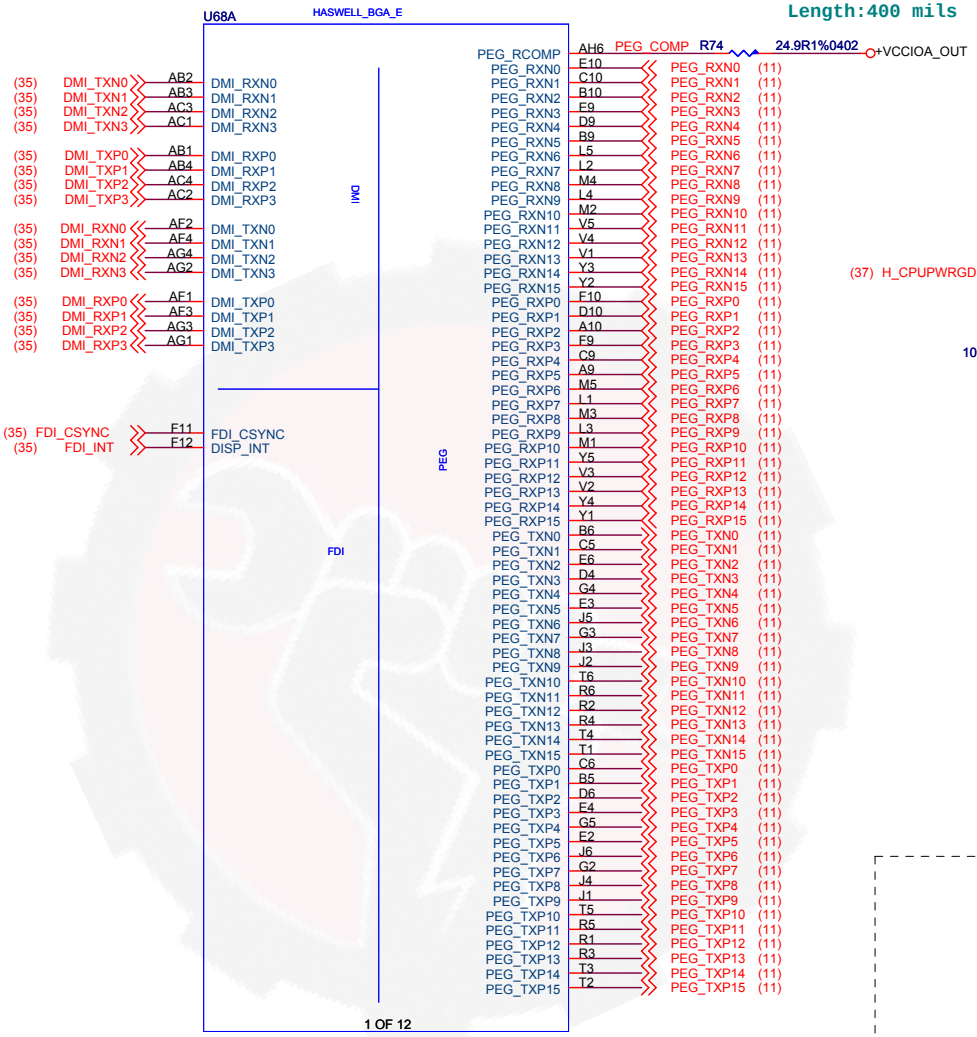
Date: Tuesday, July 29, 2014 | Sheet 2 of 70

Haswell (DMI,PEG,FDI)

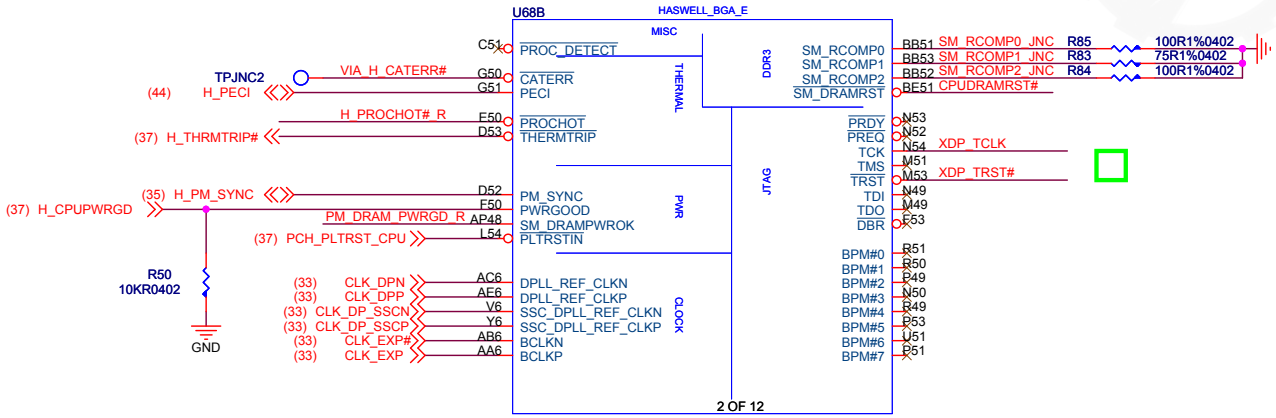
PEG_RCOMP
Width:12 mils
Spacing:15 mils
Length:400 mils

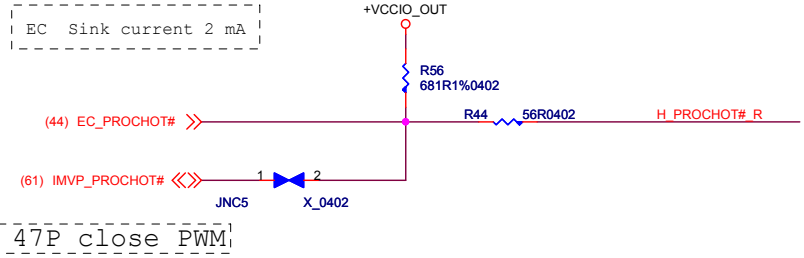


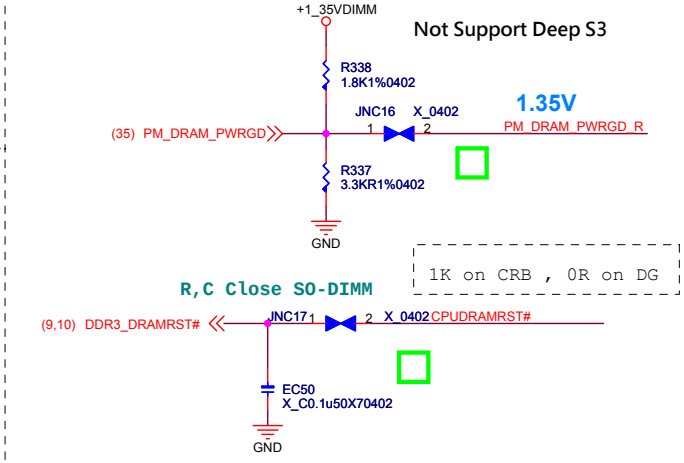
Haswell (CLK,MISC,JTAG)

i7-4710HQ,(SR1PX),2.5GHz

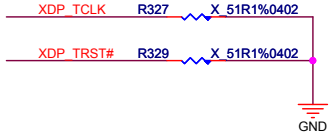
SM_RCOMP_0/1/2 : 15/20/25/15/20/25
SM_RCOMP_0/1/2 Length max: 500mil







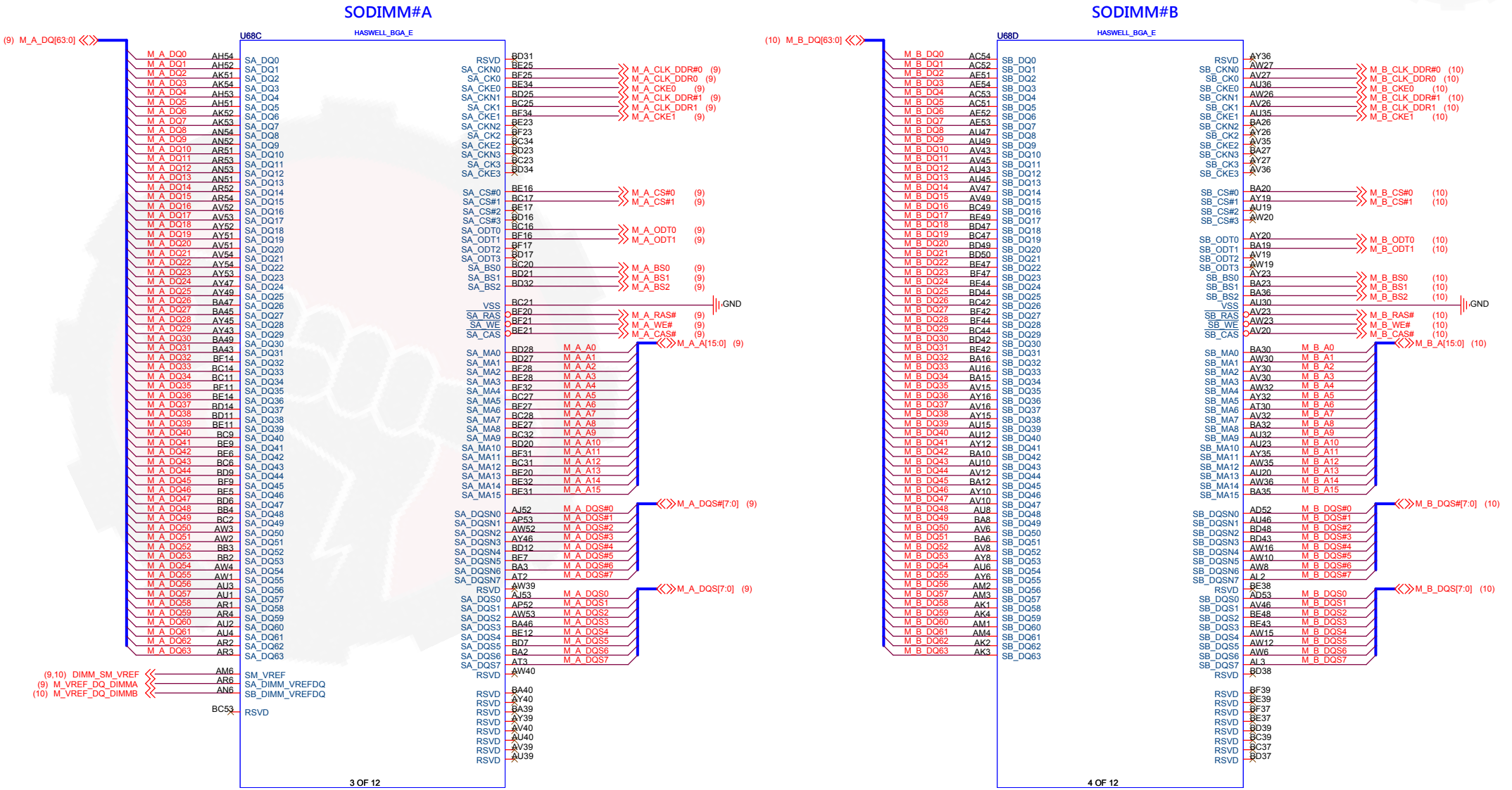
p.11 479493_479493_SharkBay_HSW_ext_rev2.0.pdf
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



MICRO-STAR INT'L CO.,LTD.

Title	CPU-1 (Host Bus)	
Size	Document Number MS-16J1	Rev 0A
Date: Tuesday, July 29, 2014	Sheet 3 of 70	

Haswell (DDR3L)



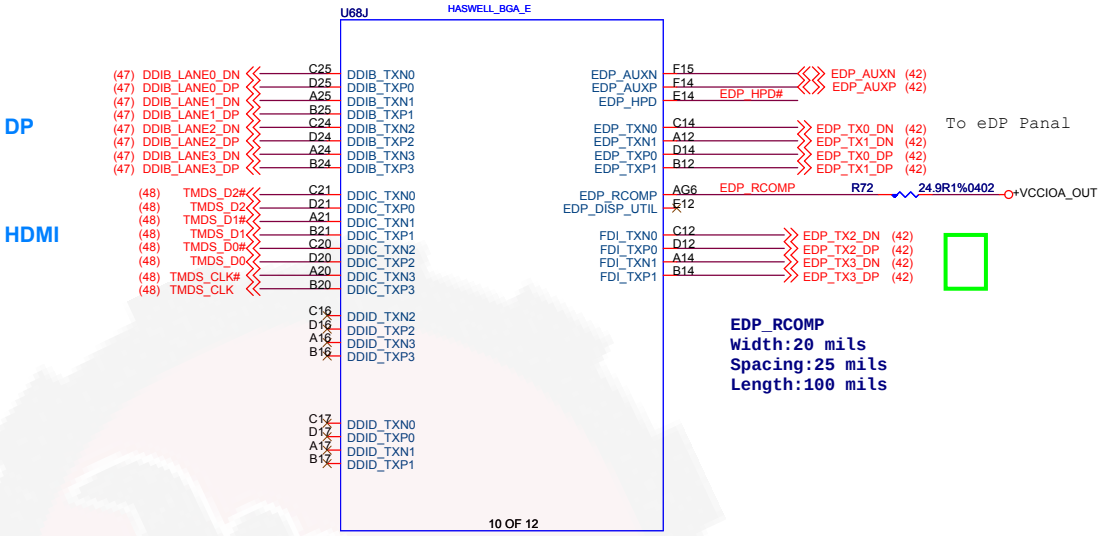
MICRO-STAR INT'L CO.,LTD.

Title: CPU-2 (DDR3L)

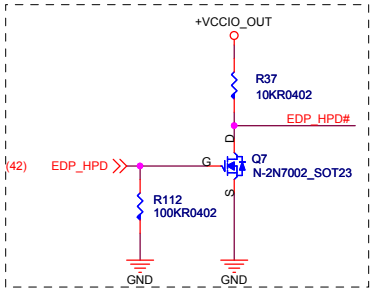
Size | Document Number: MS-16J1 | Rev: 0A

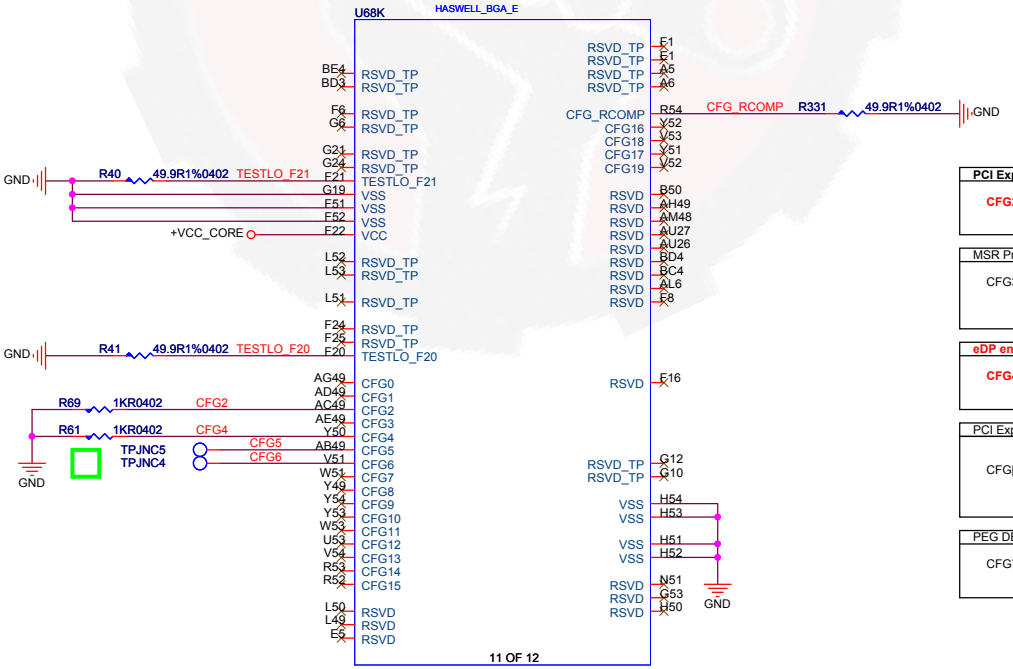
Date: Tuesday, July 29, 2014 | Sheet 4 of 70

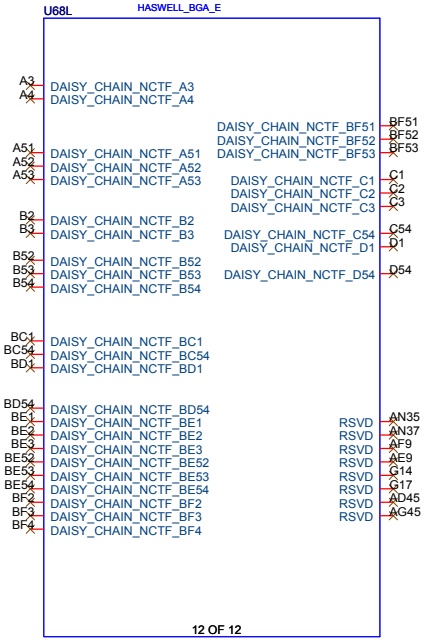
Display/Reserved



EDP_RCOMP
Width:20 mils
Spacing:25 mils
Length:100 mils







PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

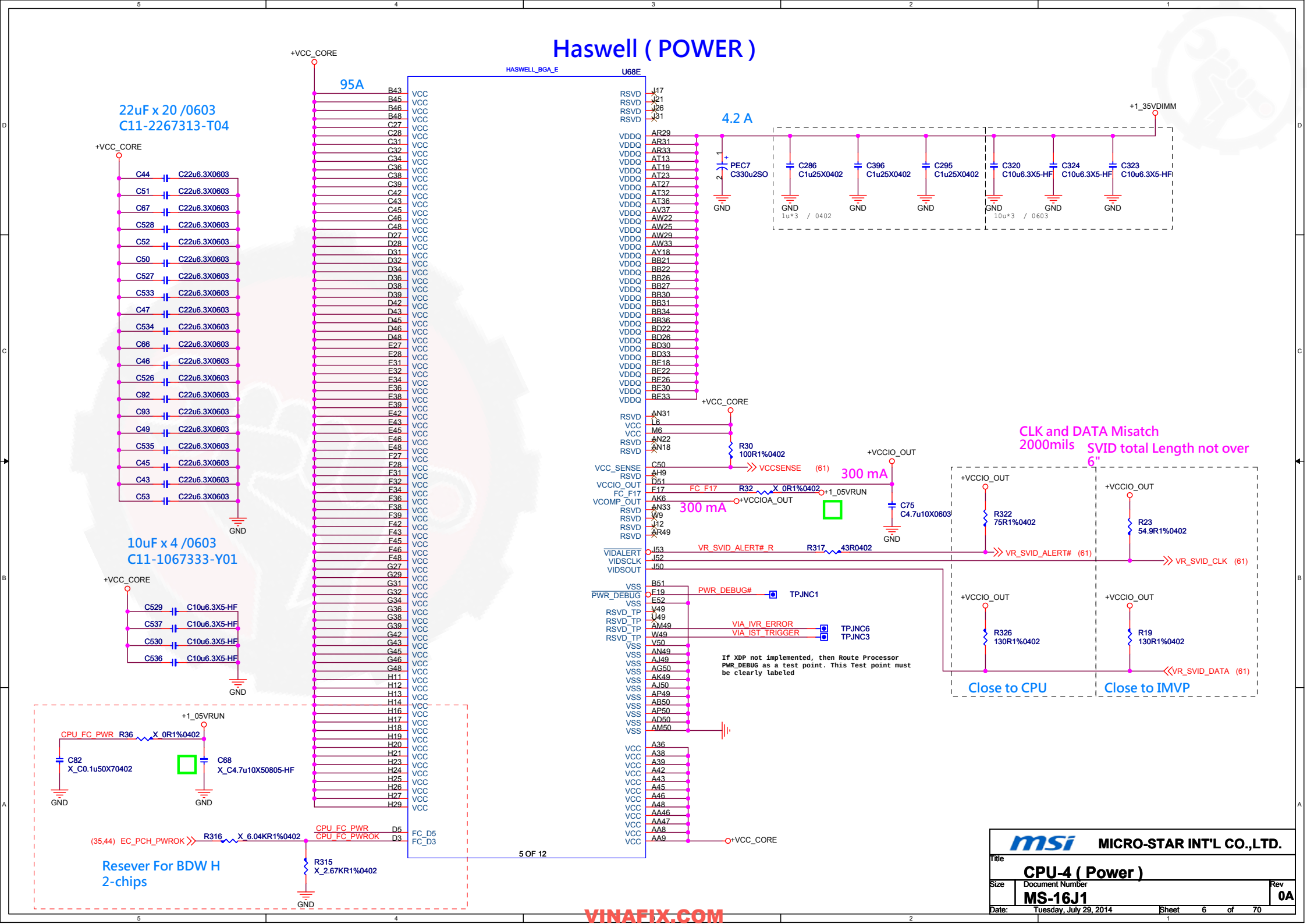
MICRO-STAR INT'L CO.,LTD.

Title: CPU-3 (Display/Reserved)

Size | Document Number: MS-16J1 | Rev: 0A

Date: Tuesday, July 29, 2014 | Sheet 5 of 70

Haswell (POWER)



Title	CPU-4 (Power)
Size	Document Number: MS-16J1
Rev	0A
Date:	Tuesday, July 29, 2014
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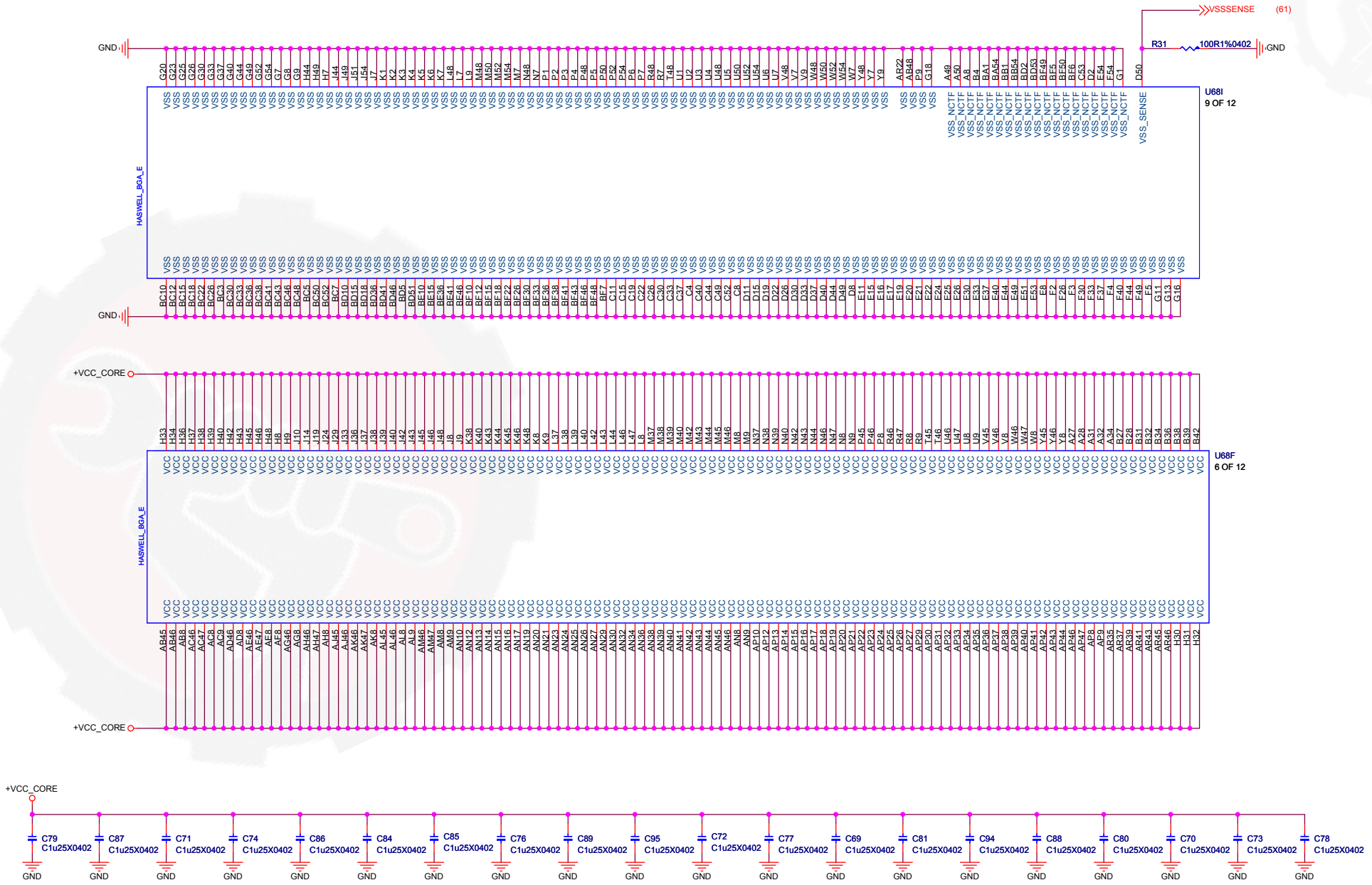
MICRO-STAR INT'L CO.,LTD.

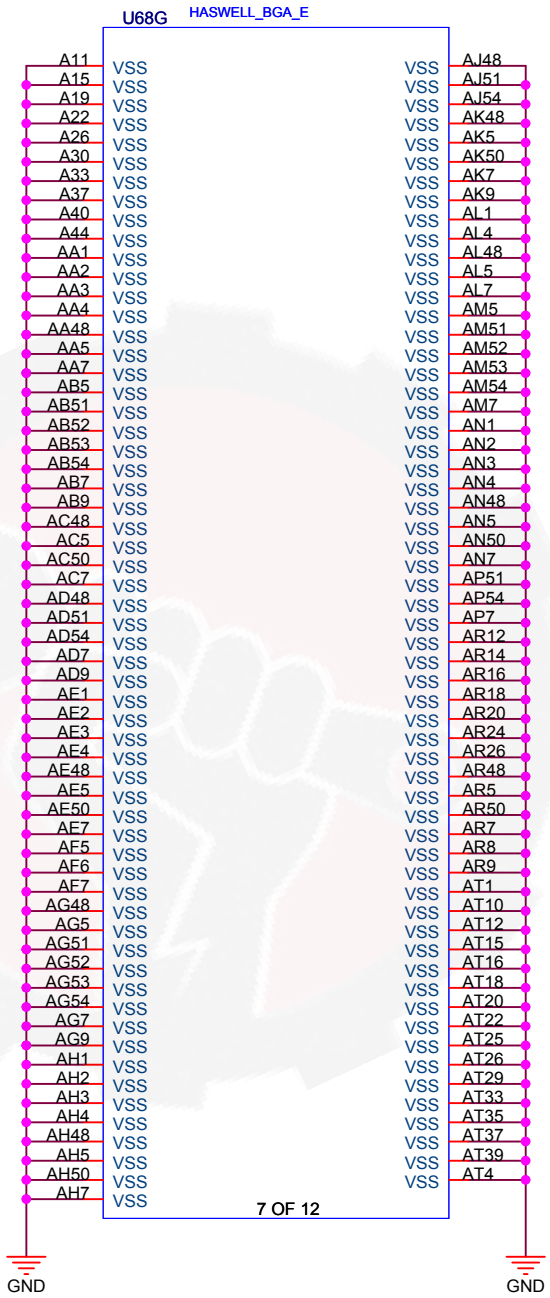
Haswell (Power & GND)

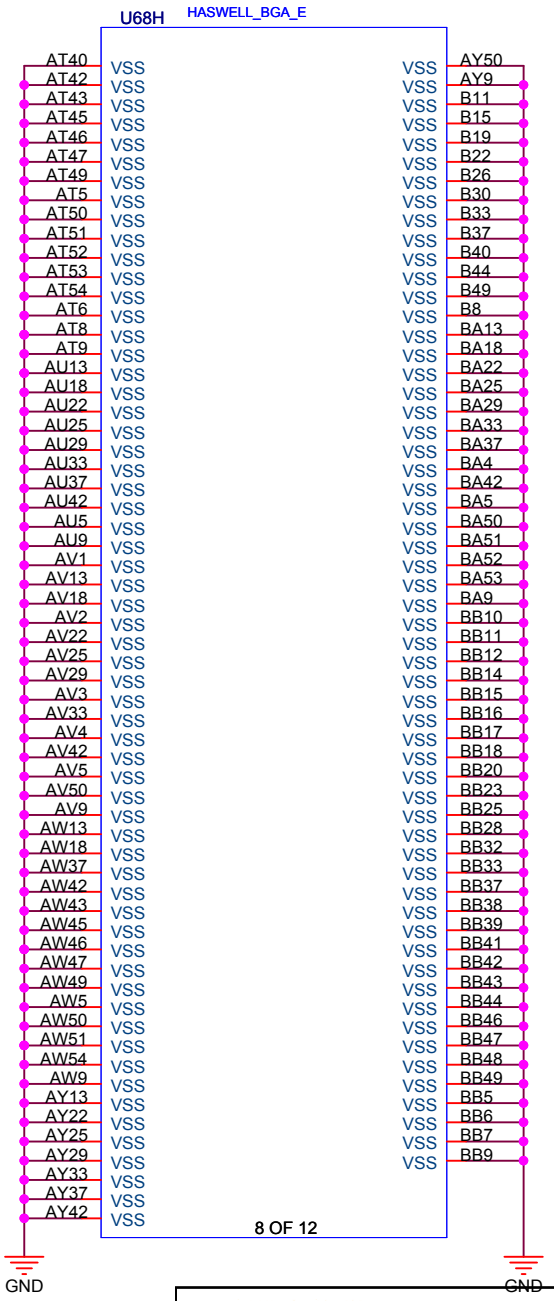


MICRO-STAR INT'L CO.,LTD.

Title	CPU-6 (Power & GND)	
Size	Document Number MS-16J1	Rev 0A
Date: Tuesday, July 29, 2014	Sheet 7 of 70	

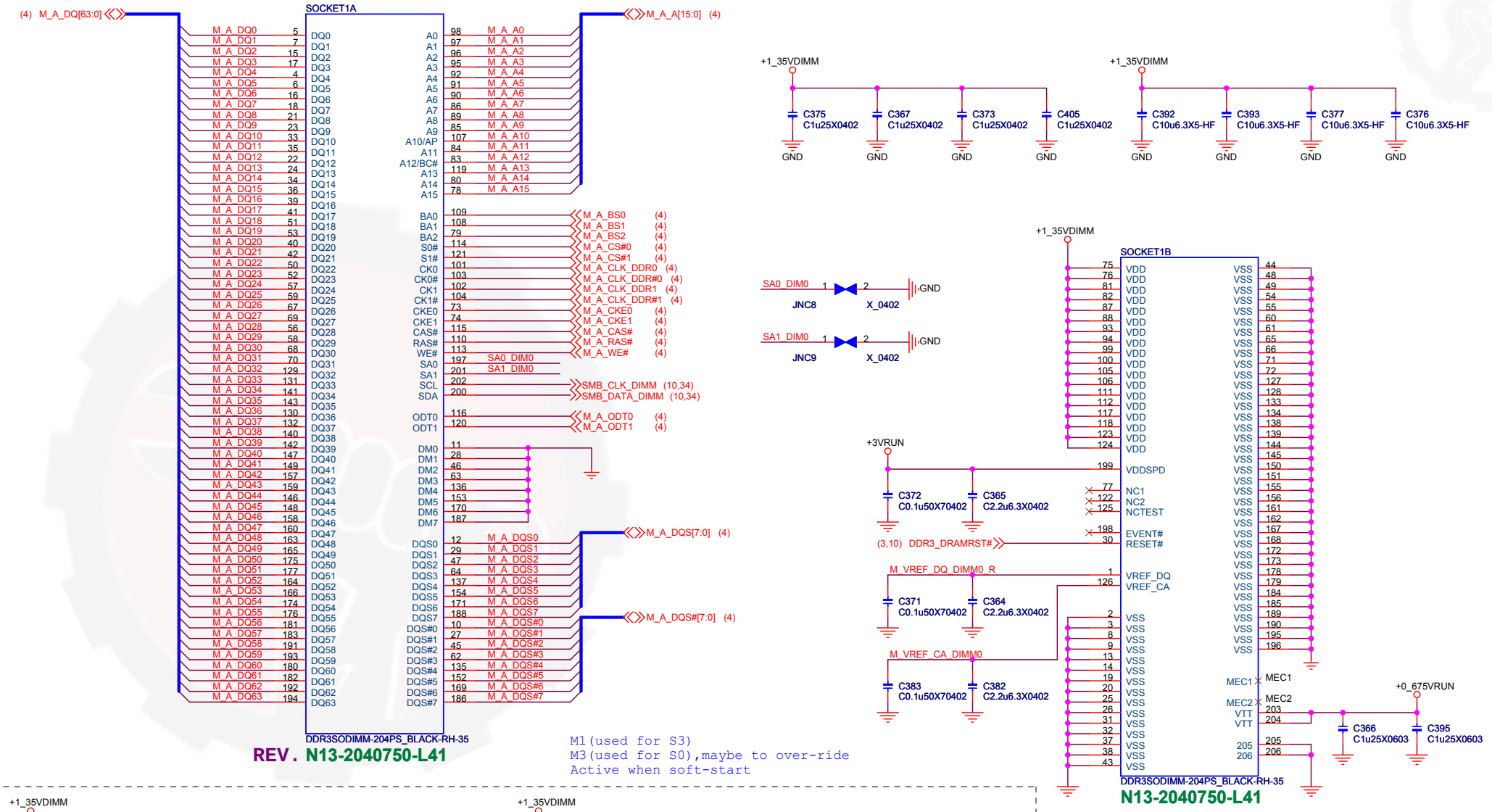
Haswell (GND)

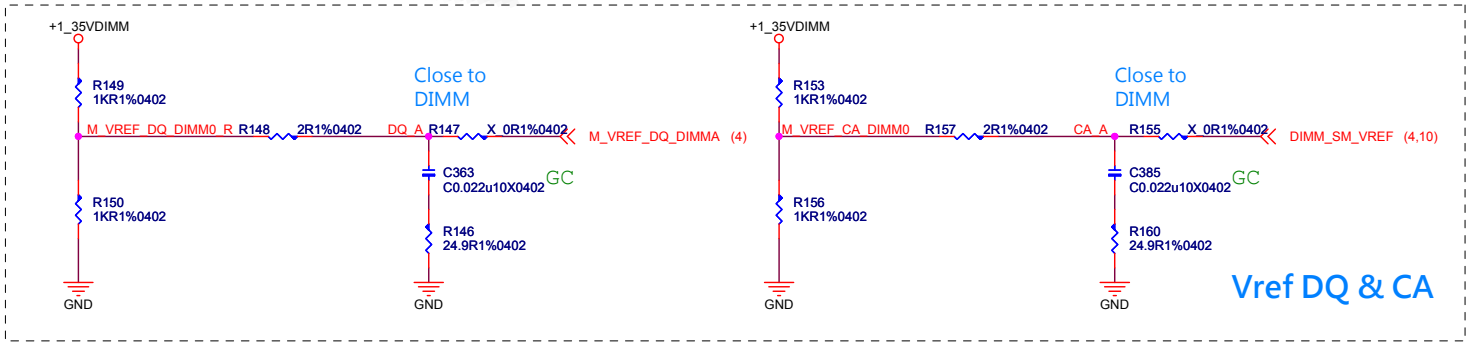




MICRO-STAR INT'L CO.,LTD.		
Title: CPU-5 (GND)		
Size	Document Number: MS-16J1	Rev: 0A
Date: Tuesday, July 29, 2014	Sheet 8 of 70	

SODIMM#A





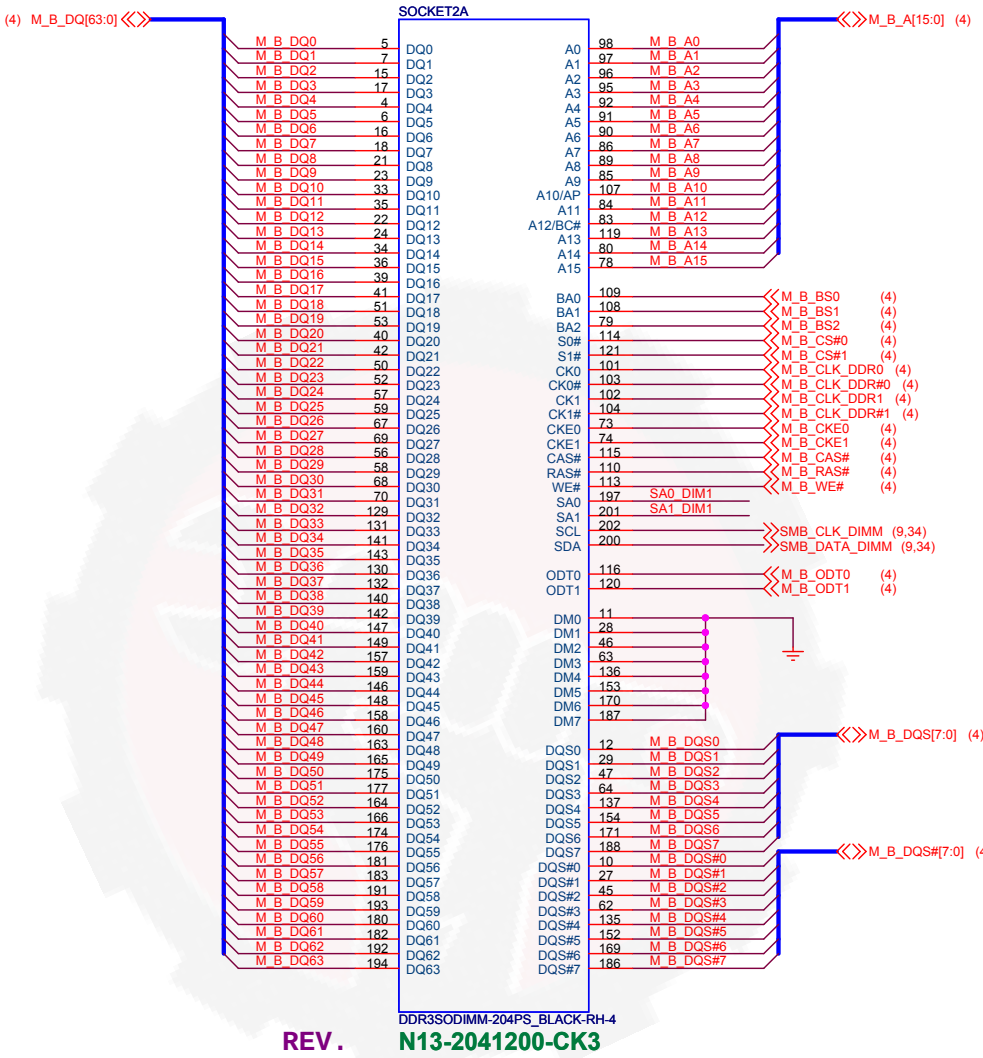
MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 0

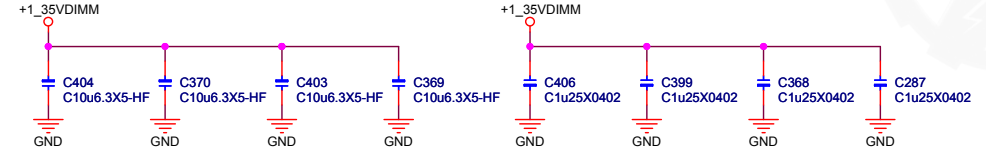
Size | Document Number: MS-16J1 | Rev: 0A

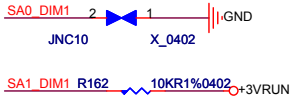
Date: Tuesday, July 29, 2014 | Sheet 9 of 70

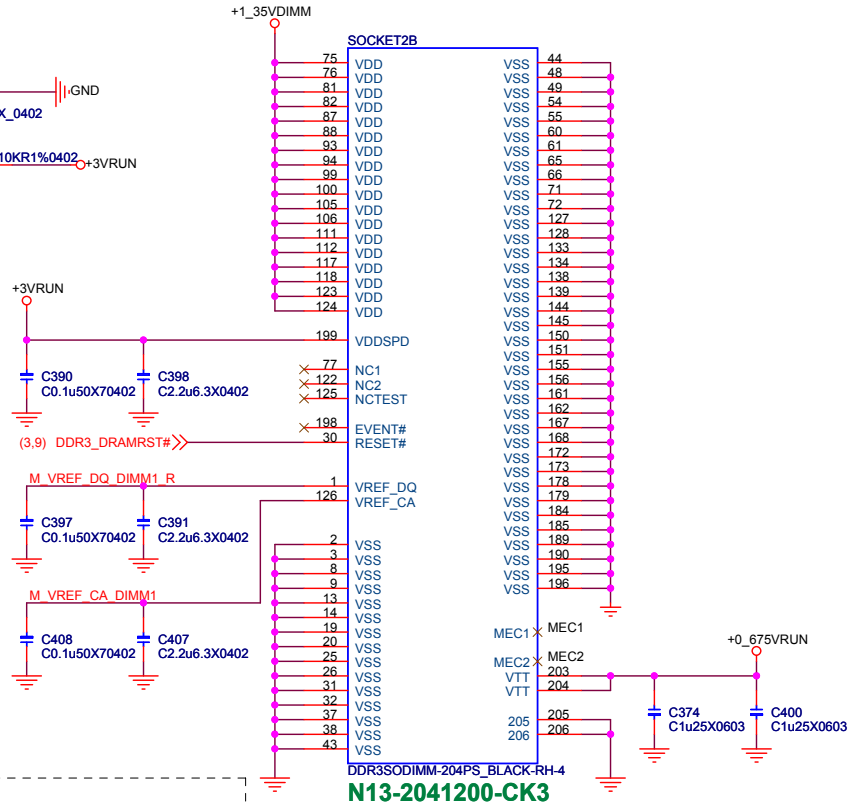
SODIMM#B



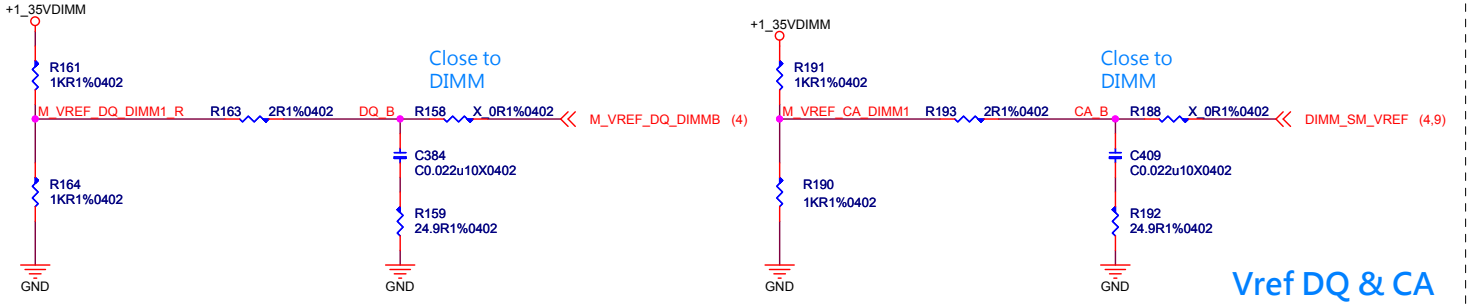
REV. N13-2041200-CK3







N13-2041200-CK3



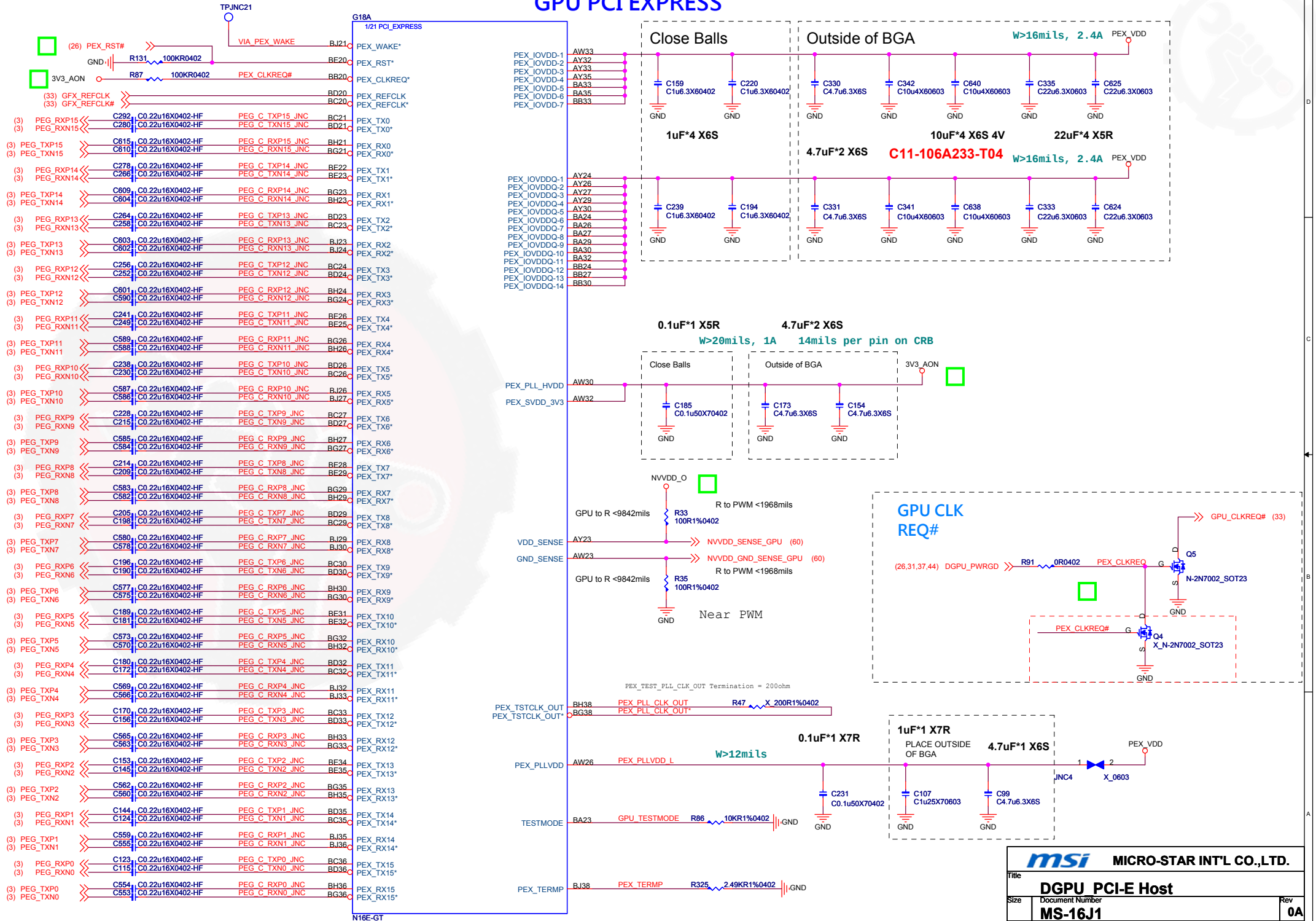
MICRO-STAR INT'L CO.,LTD.

Title: DDR3L SODIMM 1

Size | Document Number: MS-16J1 | Rev: 0A

Date: Tuesday, July 29, 2014 | Sheet 10 of 70

GPU PCI EXPRESS



MSI	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_PCI-E Host
Size	Document Number: MS-16J1
Rev	0A
Date:	Tuesday, July 29, 2014
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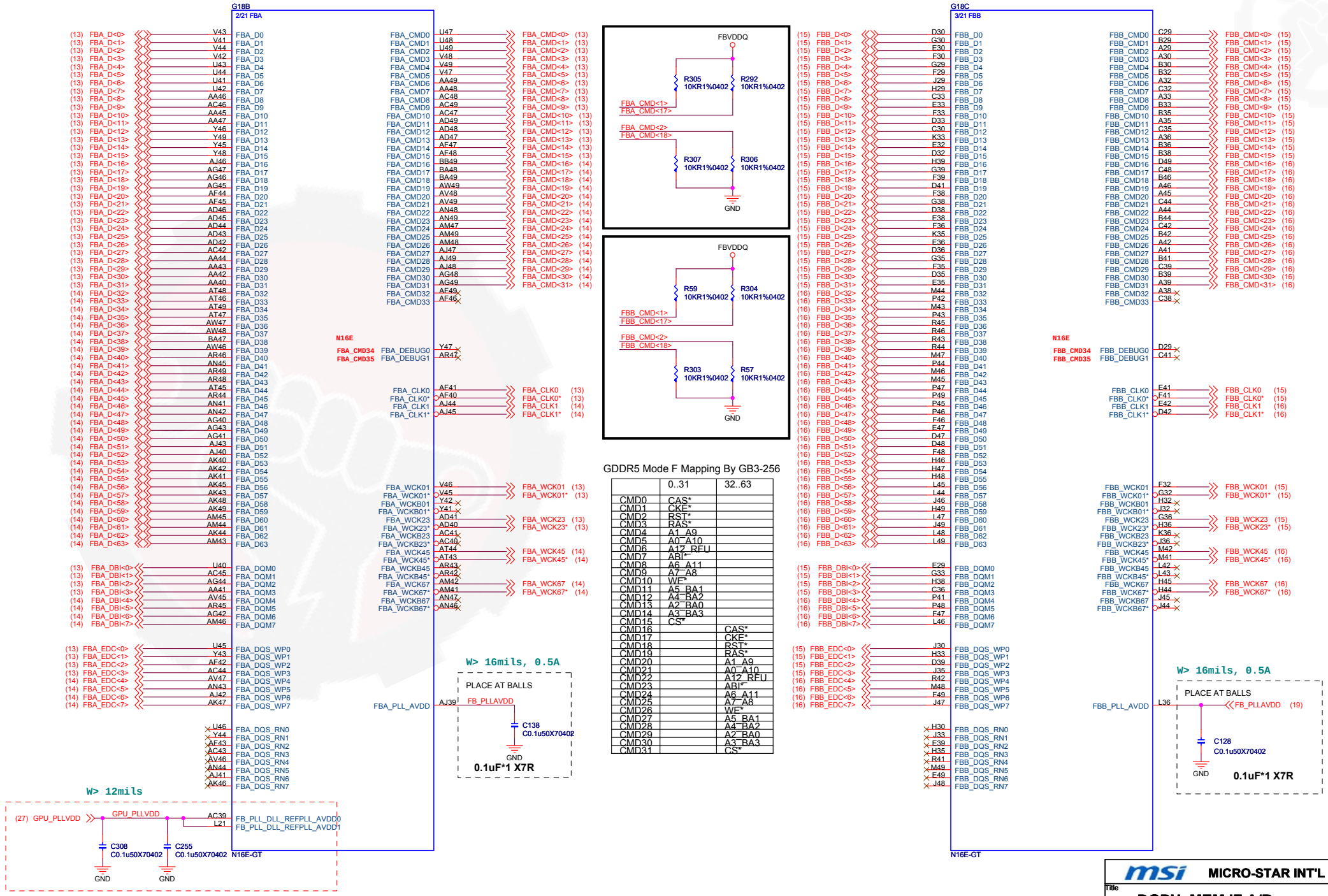
GPU Frame Buffer Partition A/B



GDDR5 Mode F Mapping By GB3-256

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A17_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A17_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

Company	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_MEM IF A/B
Size	
Document Number	MS-16J1
Rev	0A
Date:	Tuesday, July 29, 2014
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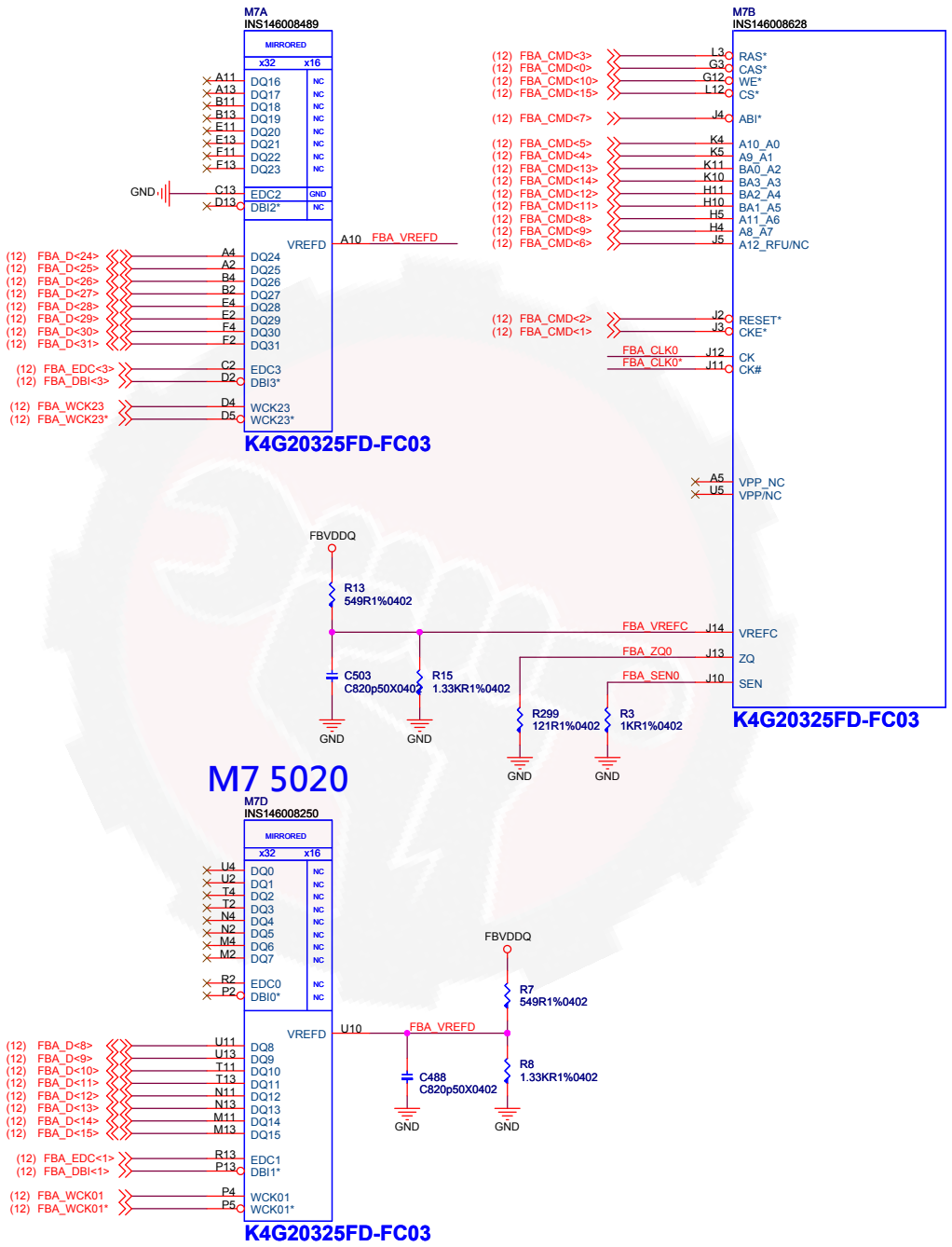
DGPU_GDDR5 FrameBuffer A0

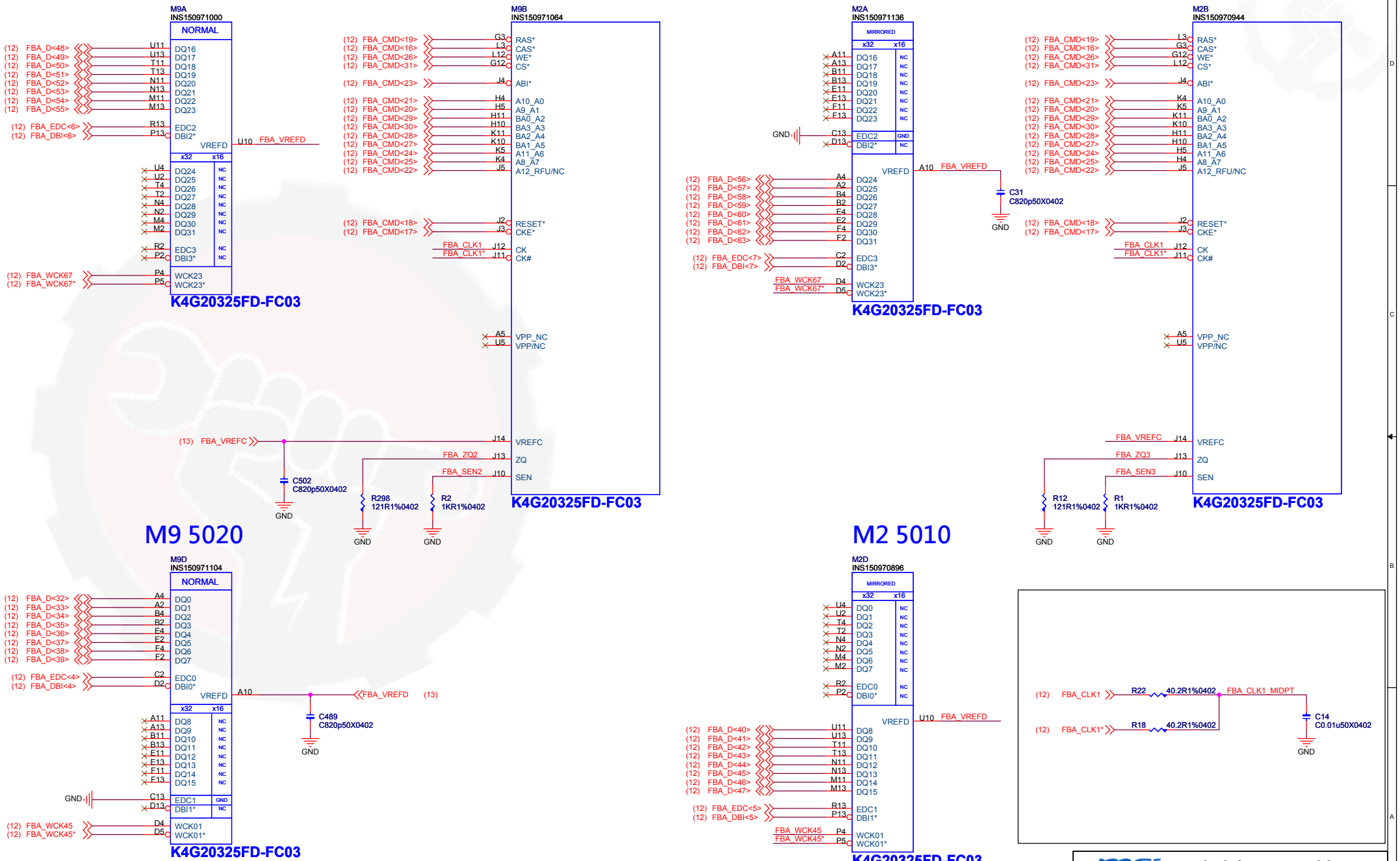


Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

MICRO-STAR INT'L CO.,LTD.

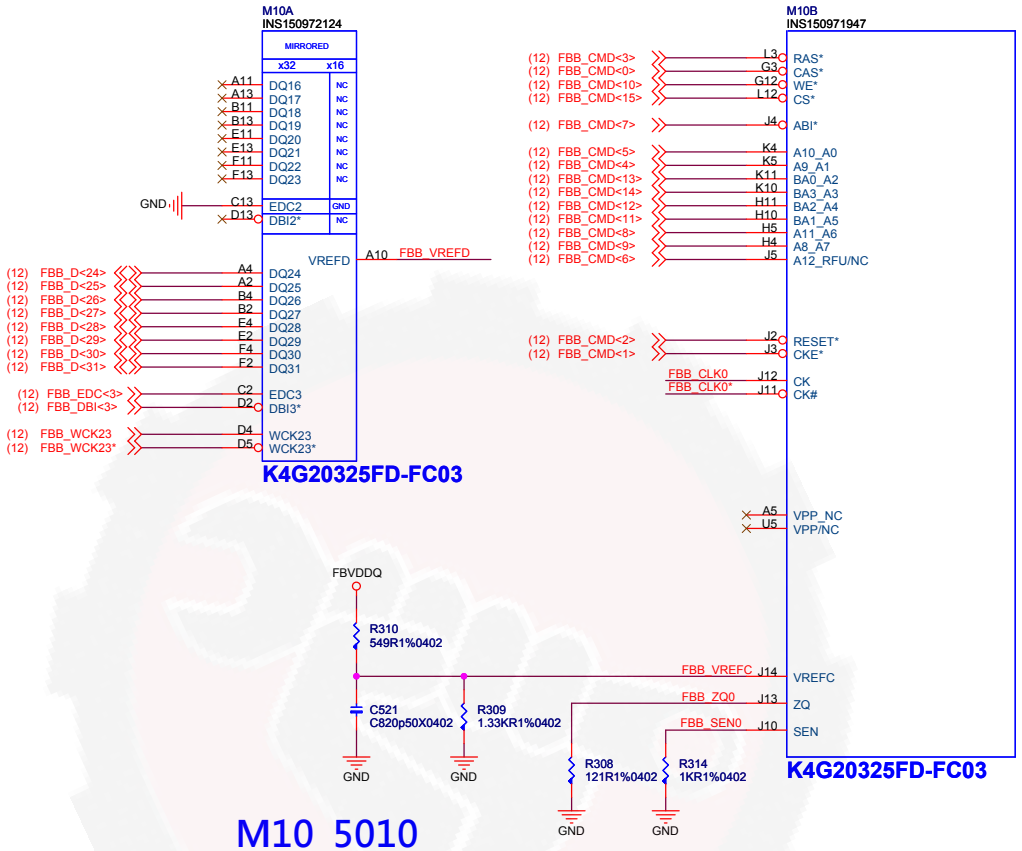
Title	DGPU_GDDR5 FrameBuffer A0	
Size	Document Number MS-16J1	Rev 0A
Date: Tuesday, July 29, 2014	Sheet 13 of 70	

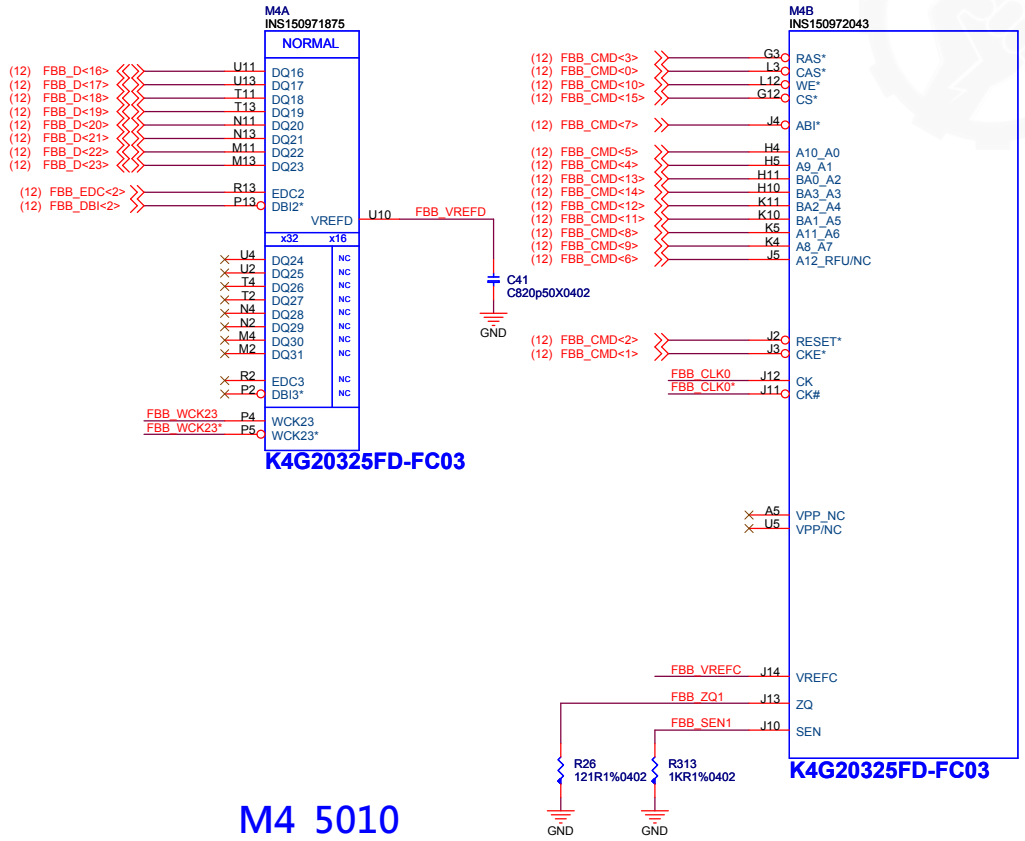
DGPU_GDDR5 FrameBuffer A1



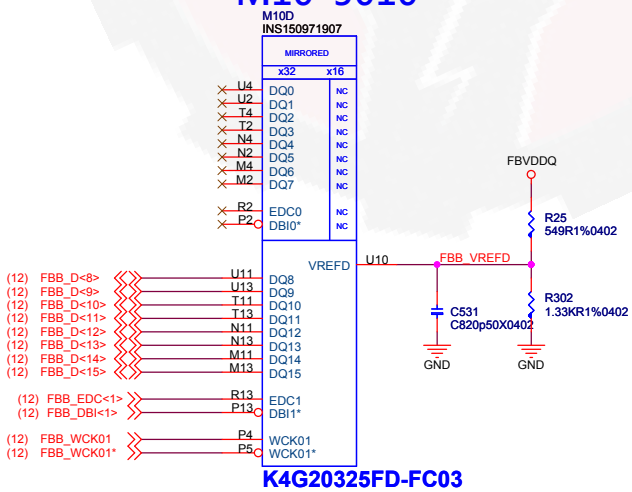
MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer A1			
Size	Document Number: MS-16J1		Rev: 0A
Date: Tuesday, July 29, 2014	Sheet 14 of 70		

DGPU_GDDR5 FrameBuffer B0

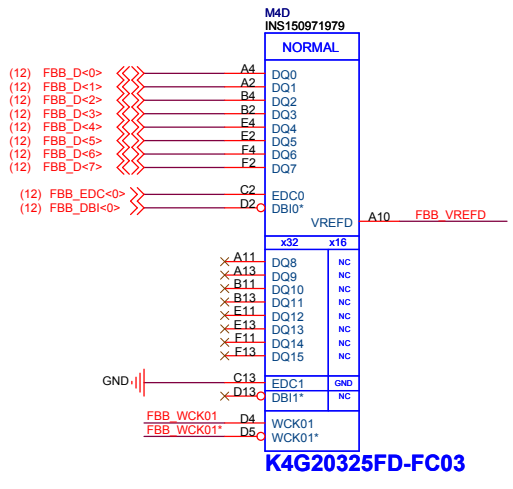


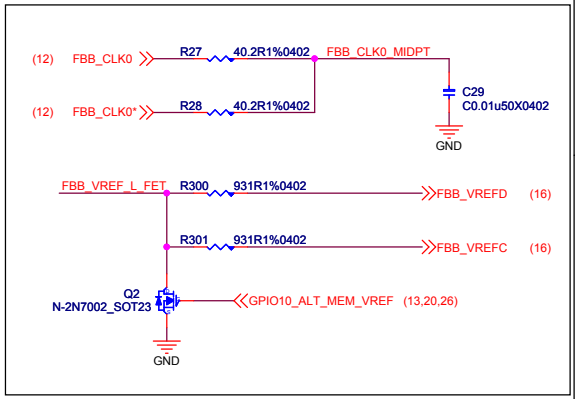


M10 5010



M4 5010





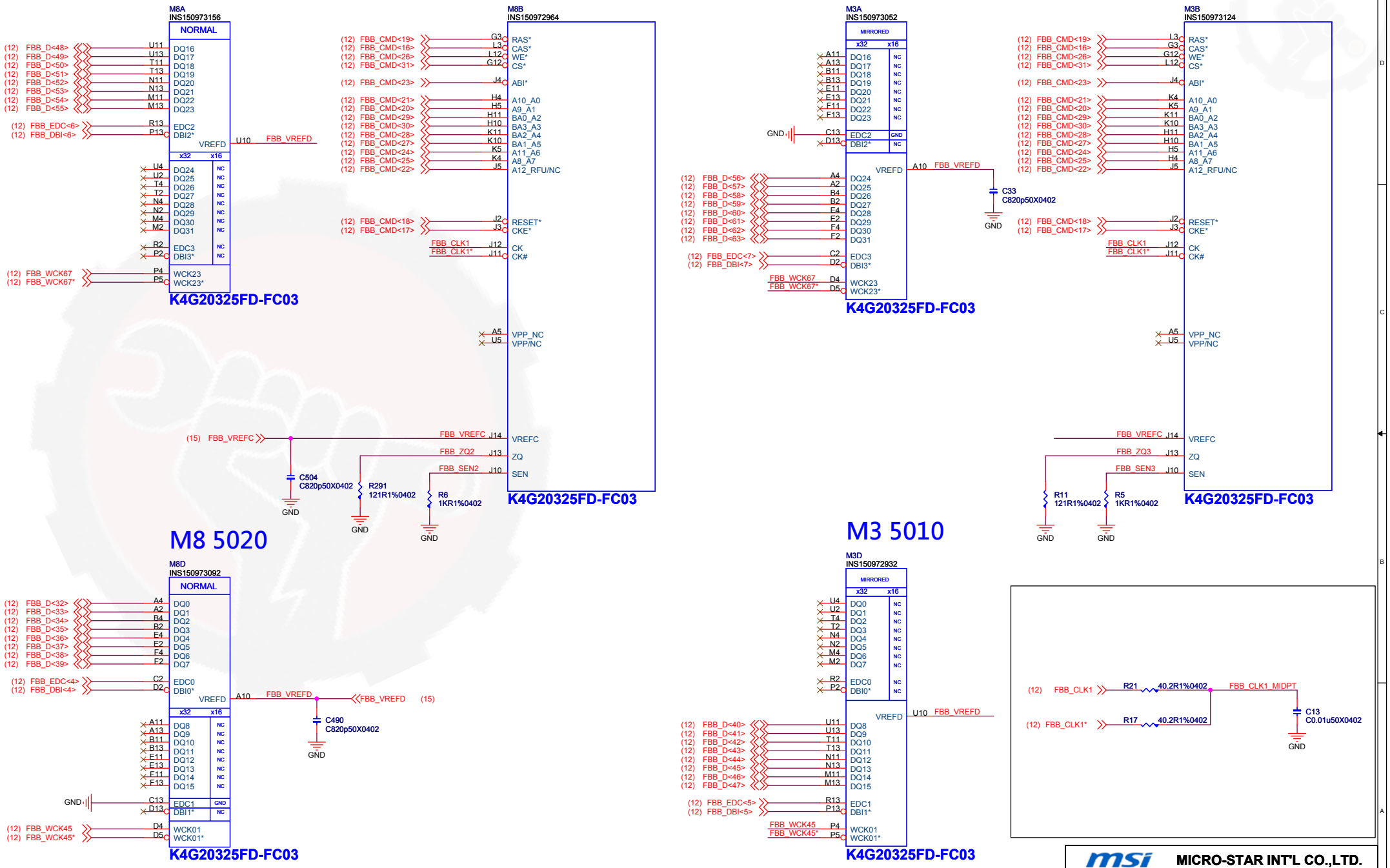
MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer B0

Size | Document Number: MS-16J1 | Rev: 0A

Date: Tuesday, July 29, 2014 | Sheet 15 of 70

DGPU_GDDR5 FrameBuffer B1



Frame Buffer Partition A Decoupling

FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ0-DQ31)

C514 C0.1u50X70402 | C496 C0.1u50X70402 | C498 C0.1u50X70402 | C507 C0.1u50X70402 | C515 C0.1u50X70402 | C17 C0.1u50X70402 | C9 C0.1u50X70402 | C8 C0.1u50X70402 | C23 C0.1u50X70402 | C509 C0.1u50X70402 | C517 C1u6.3X-HF | C494 C1u6.3X-HF | C27 C1u6.3X-HF | C5 C1u6.3X-HF | C491 C10u4X60603 | C1 C10u4X60603

GND

1uF 改0.1uF

4.7uF 改1uF

C11-106A233-T04

FBVDDQ

FBA_MF1 — R20 1KR1%0402 — J1

M1C INS150975090 — Normal — MF add 1k to VSS

FBA_MF0 — R294 1KR1%0402 — J1

M7C INS150975200 — Mirrored — MF add 1k to VDD

FBA_MF2 — R296 1KR1%0402 — J1

M9C INS150974702 — Normal — MF add 1k to VSS

FBA_MF3 — R14 1KR1%0402 — J1

M2C INS150974972 — Mirrored — MF add 1k to VDD

M1C / M9C (Normal)			M7C / M2C (Mirrored)		
B10	VSS	C10	C10	VDD_1	B10
B5	VSS	C5	C5	VDD_2	B5
D10	VSS	D11	D11	VDD_3	D10
G10	VSS	G1	G1	VDD_4	G10
G5	VSS	G11	G11	VDD_5	G5
H1	VSS	G14	G14	VDD_6	H1
H14	VSS	G4	G4	VDD_7	H14
K1	VSS	L1	L1	VDD_8	K1
K14	VSS	L11	L11	VDD_9	K14
L10	VSS	L14	L14	VDD_10	L10
L5	VSS	L4	L4	VDD_11	L5
P10	VSS	P11	P11	VDD_12	P10
T10	VSS	R10	R10	VDD_13	T10
T5	VSS	R5	R5	VDD_14	T5
A1	VSSQ	B1	B1	VDDQ_1	A1
A12	VSSQ	B12	B12	VDDQ_2	A12
A14	VSSQ	B14	B14	VDDQ_3	A14
A3	VSSQ	B3	B3	VDDQ_4	A3
C1	VSSQ	D1	D1	VDDQ_5	C1
C11	VSSQ	D12	D12	VDDQ_6	C11
C12	VSSQ	D14	D14	VDDQ_7	C12
C14	VSSQ	D3	D3	VDDQ_8	C14
C3	VSSQ	E10	E10	VDDQ_9	C3
C4	VSSQ	E5	E5	VDDQ_10	C4
E1	VSSQ	F1	F1	VDDQ_11	E1
E12	VSSQ	F12	F12	VDDQ_12	E12
E14	VSSQ	F14	F14	VDDQ_13	E14
E3	VSSQ	F3	F3	VDDQ_14	E3
F10	VSSQ	G13	G13	VDDQ_15	F10
F5	VSSQ	G2	G2	VDDQ_16	F5
H13	VSSQ	H12	H12	VDDQ_17	H13
H2	VSSQ	H3	H3	VDDQ_18	H2
K13	VSSQ	K12	K12	VDDQ_19	K13
K2	VSSQ	K3	K3	VDDQ_20	K2
M10	VSSQ	L13	L13	VDDQ_21	M10
M5	VSSQ	L2	L2	VDDQ_22	M5
N1	VSSQ	M1	M1	VDDQ_23	N1
N12	VSSQ	M12	M12	VDDQ_24	N12
N14	VSSQ	M14	M14	VDDQ_25	N14
N3	VSSQ	M3	M3	VDDQ_26	N3
R1	VSSQ	N10	N10	VDDQ_27	R1
R11	VSSQ	N5	N5	VDDQ_28	R11
R12	VSSQ	P1	P1	VDDQ_29	R12
R14	VSSQ	P12	P12	VDDQ_30	R14
R3	VSSQ	P14	P14	VDDQ_31	R3
R4	VSSQ	P3	P3	VDDQ_32	R4
U1	VSSQ	T1	T1	VDDQ_33	U1
U12	VSSQ	T12	T12	VDDQ_34	U12
U14	VSSQ	T14	T14	VDDQ_35	U14
U3	VSSQ	T3	T3	VDDQ_36	U3

K4G20325FD-FC03

GND

FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ32-DQ63)

C501 C0.1u50X70402 | C10 C0.1u50X70402 | C22 C0.1u50X70402 | C7 C0.1u50X70402 | C263 C0.1u50X70402 | C511 C0.1u50X70402 | C497 C0.1u50X70402 | C271 C0.1u50X70402 | C12 C0.1u50X70402 | C304 C0.1u50X70402 | C493 C1u6.3X-HF | C334 C1u6.3X-HF | C4 C1u6.3X-HF | C495 C1u6.3X-HF | C492 C10u4X60603 | C2 C10u4X60603

GND

C11-106A233-T04

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-A_DECOUPLING

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Frame Buffer Partition B Decoupling

FBVDDQ

SPARE

DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)

C297 C0.1u50X70402	C18 C0.1u50X70402	C513 C0.1u50X70402	C234 C0.1u50X70402	C620 C0.1u50X70402	C21 C0.1u50X70402	C197 C0.1u50X70402	C619 C0.1u50X70402	C269 C0.1u50X70402	C510 C0.1u50X70402	C518 C1u6.3X-HF	C522 C1u6.3X-HF	C28 C1u6.3X-HF	C36 C1u6.3X-HF	C25 C10u4X60603	C306 C10u4X60603
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

C11-106A233-T04

FBB_MF1

R323 1KR1%0402

M4C INS150977791 — Normal — K4G20325FD-FC03

FBVDDQ

R324 1KR1%0402

FBB_MF0

M10C INS150977435 — Mirrored — K4G20325FD-FC03

FBB_MF2

R295 1KR1%0402

M8C INS150977949 — Normal — K4G20325FD-FC03

FBVDDQ

R16 1KR1%0402

FBB_MF3

M3C INS150977569 — Mirrored — K4G20325FD-FC03

GND

FBVDDQ

SPARE

DECOUPLING AROUND FBB MEMORIES (DQ32-DQ63)

C645 C0.1u50X70402	C3 C0.1u50X70402	C109 C0.1u50X70402	C101 C0.1u50X70402	C19 C0.1u50X70402	C500 C0.1u50X70402	C499 C0.1u50X70402	C11 C0.1u50X70402	C607 C0.1u50X70402	C26 C0.1u50X70402	C519 C1u6.3X-HF	C549 C1u6.3X-HF	C32 C1u6.3X-HF	C547 C1u6.3X-HF	C55 C10u4X60603	C24 C10u4X60603
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

C11-106A233-T04

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-B_DECOUPLING

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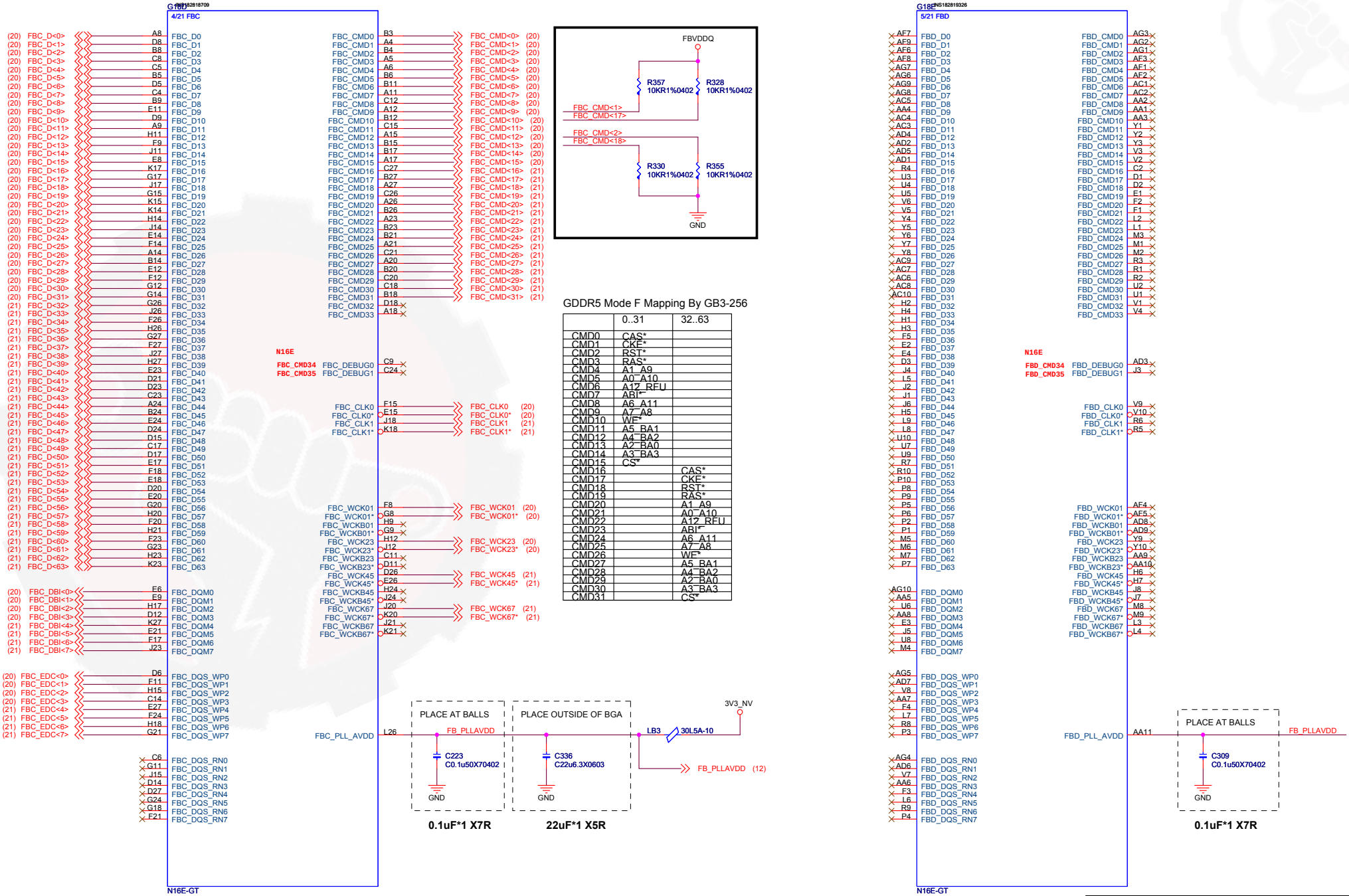
GPU Frame Buffer Partition C/D



Title	MICRO-STAR INT'L CO.,LTD.		
	DGPU_MEM IF C/D		
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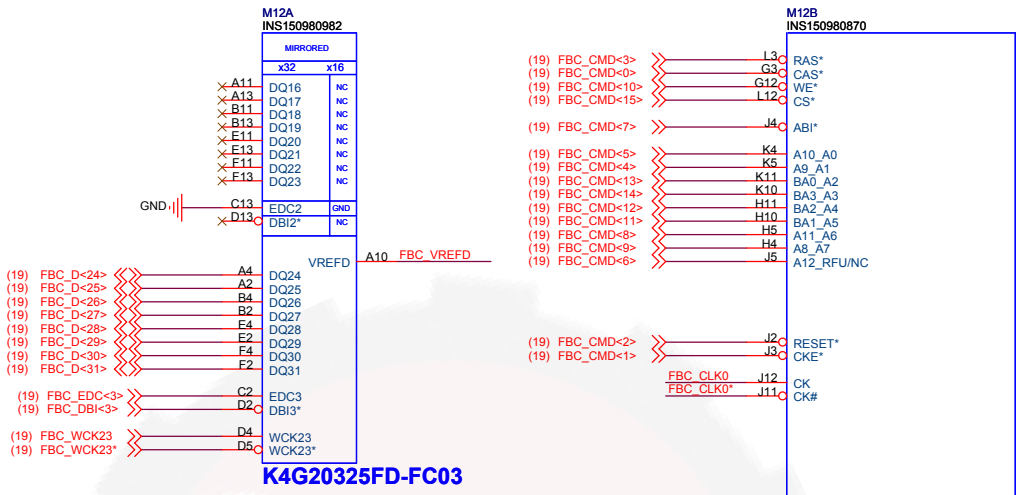
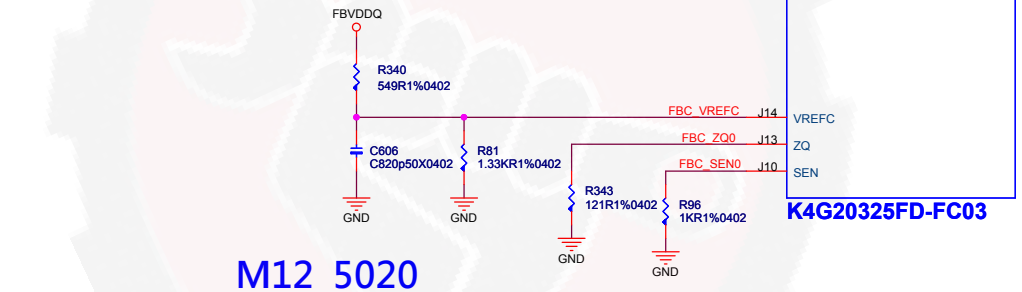
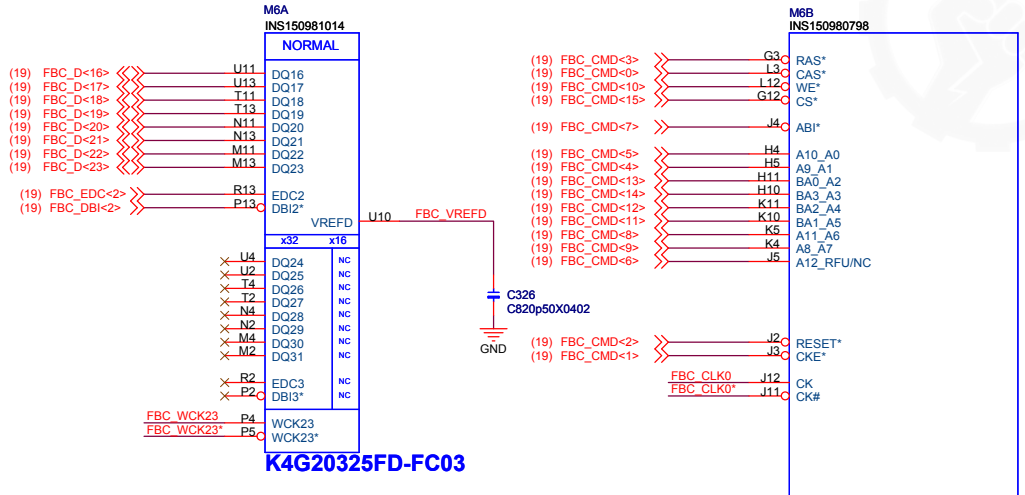
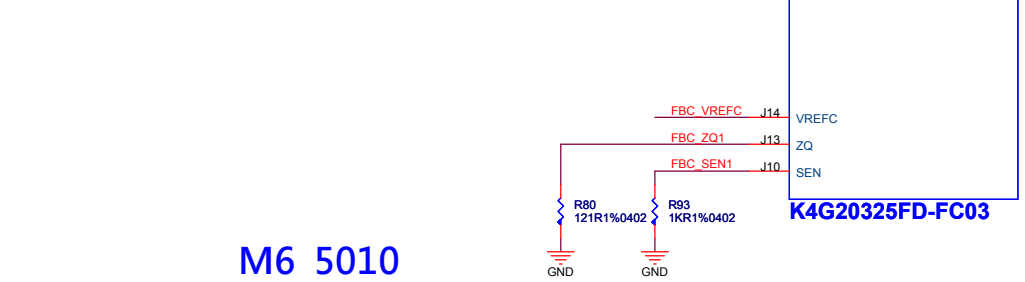
DGPU_GDDR5 FrameBuffer C0

(N16P-GX-B ALL unstuff)

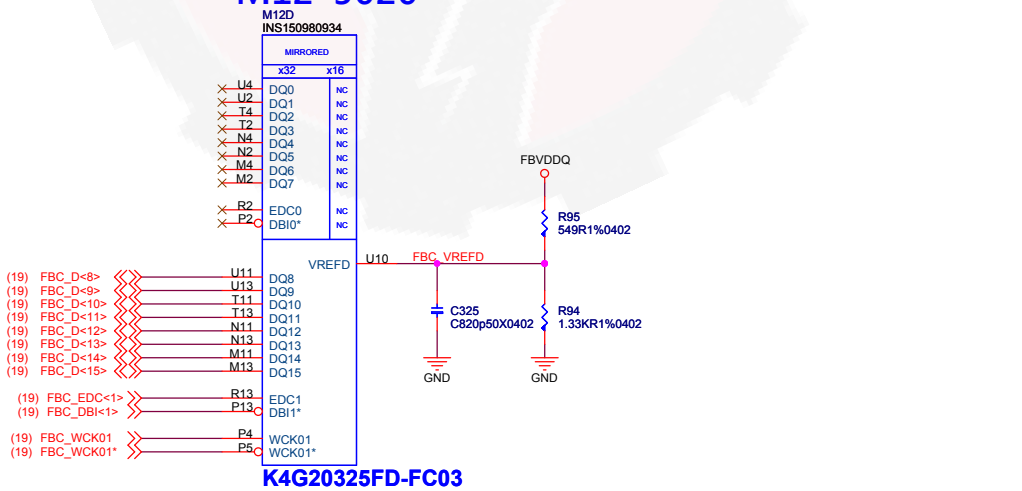




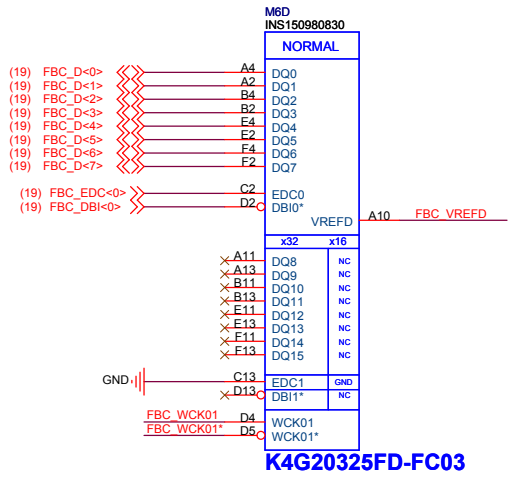


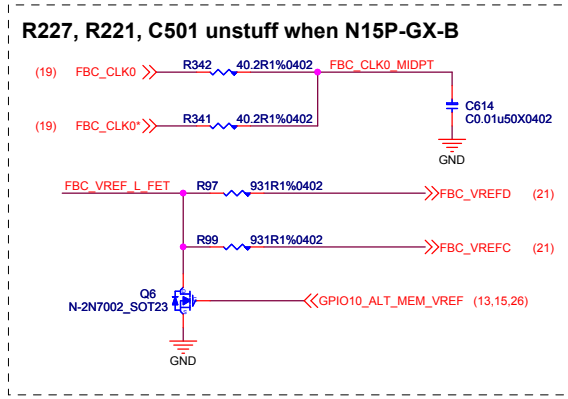


M12 5020



M6 5010





MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer C

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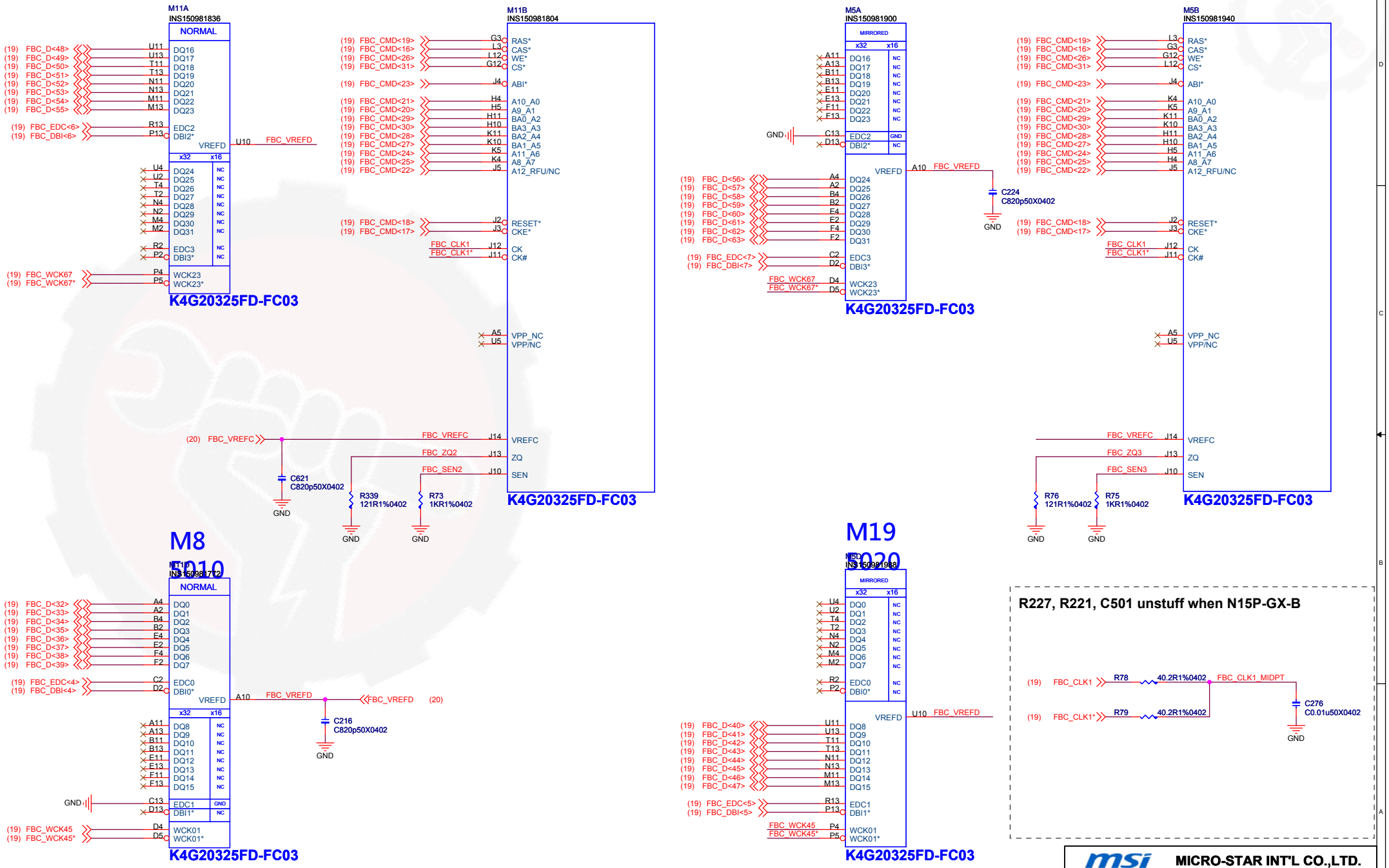
DGPU_GDDR5 FrameBuffer C1

(N16P-GX-B ALL unstuff)



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer C

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Frame Buffer Partition C Decoupling

(N16P-GX-B ALL unstuff)

FBVDDQ

SPARE

DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)

C644 C0.1u50X70402 | C543 C0.1u50X70402 | C102 C0.1u50X70402 | C608 C0.1u50X70402 | C337 C0.1u50X70402 | C550 C0.1u50X70402 | C110 C0.1u50X70402 | C524 C0.1u50X70402 | C339 C0.1u50X70402 | C37 C0.1u50X70402 | C646 C1u6.3X-HF | C546 C1u6.3X-HF | C106 C1u6.3X-HF | C338 C1u6.3X-HF | C548 C10u4X60603 | C105 C10u4X60603

GND

1uF 改0.1uF

4.7uF 改1uF

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FBC_MF1 — R114 1KR1%0402 — J1

M6C INS150983487 — Normal — MF (add 1k to VSS)

FBVDDQ — R370 1KR1%0402 — FBC_MF0 — J1

M12C INS150983985 — Mirrored — MF (add 1k to VDD)

FBC_MF2 — R46 1KR1%0402 — J1

M11C INS150983787 — Normal — MF (add 1k to VSS)

FBVDDQ — R45 1KR1%0402 — FBC_MF3 — J1

M5C INS150983645 — Mirrored — MF (add 1k to VDD)

K4G20325FD-FC03

K4G20325FD-FC03

K4G20325FD-FC03

K4G20325FD-FC03

GND

DECOUPLING AROUND FBC MEMORIES (DQ32-DQ63)

FBVDDQ

SPARE

C38 C0.1u50X70402 | C35 C0.1u50X70402 | C605 C0.1u50X70402 | C296 C0.1u50X70402 | C298 C0.1u50X70402 | C270 C0.1u50X70402 | C542 C0.1u50X70402 | C523 C0.1u50X70402 | C552 C0.1u50X70402 | C520 C0.1u50X70402 | C612 C1u6.3X-HF | C613 C1u6.3X-HF | C284 C1u6.3X-HF | C283 C1u6.3X-HF | C611 C10u4X60603 | C285 C10u4X60603

GND

C11-106A233-T04

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-C_DECOUPLING

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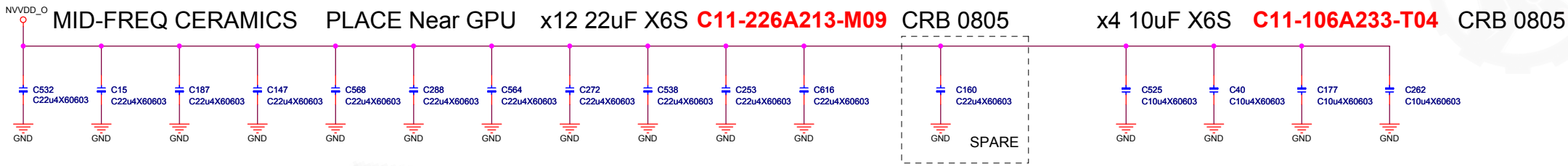
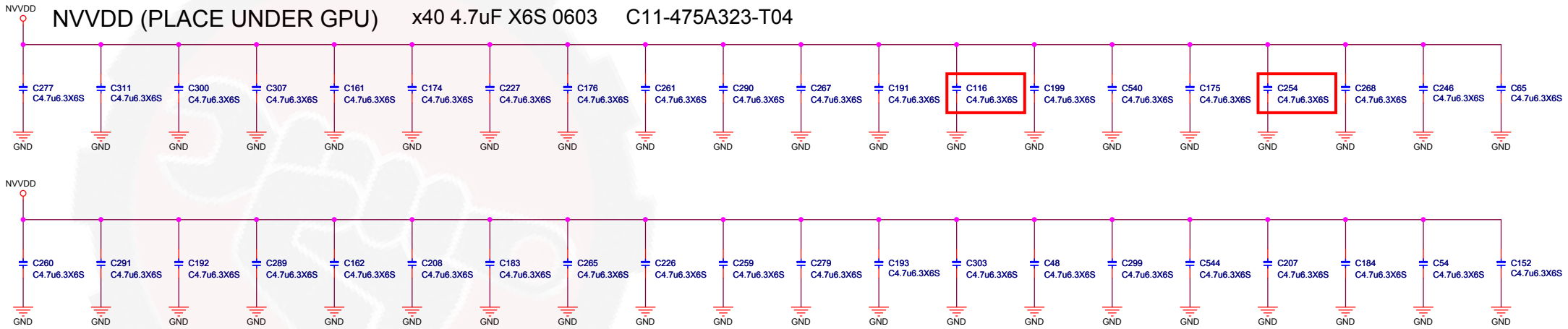
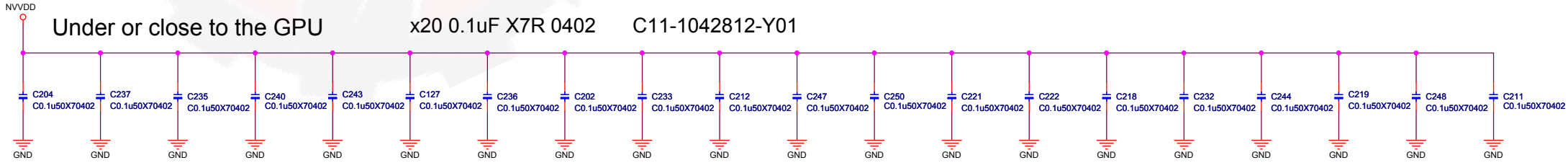
GPU DECOUPLING A







MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_GPU DECOUPLING A		
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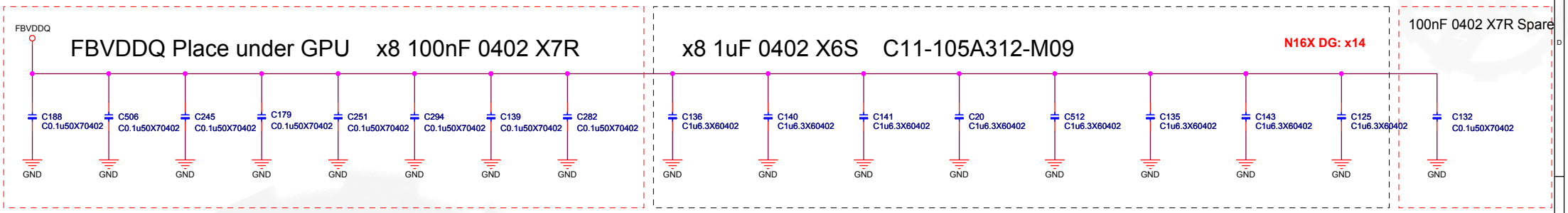
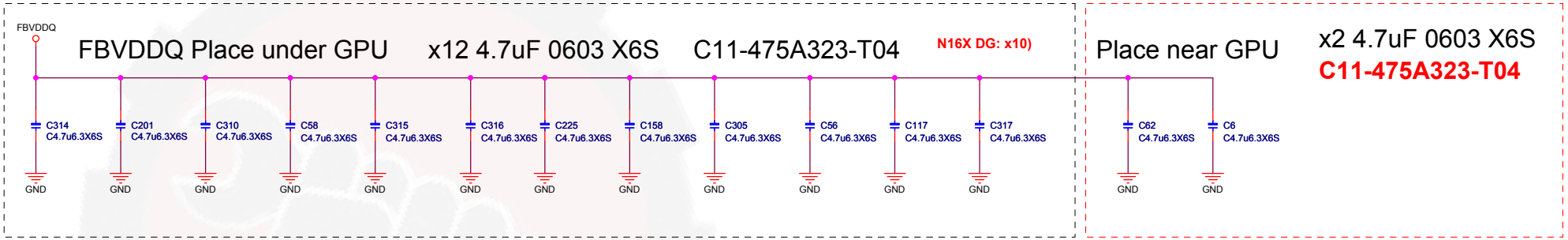
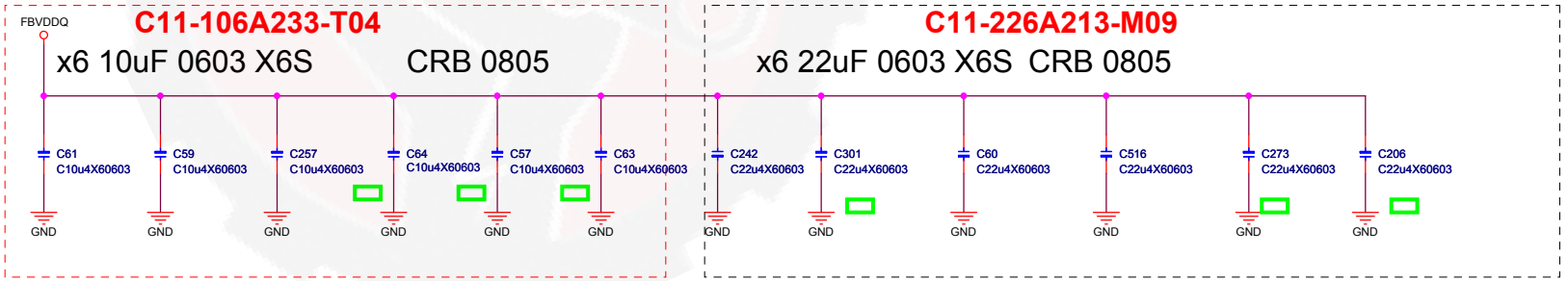
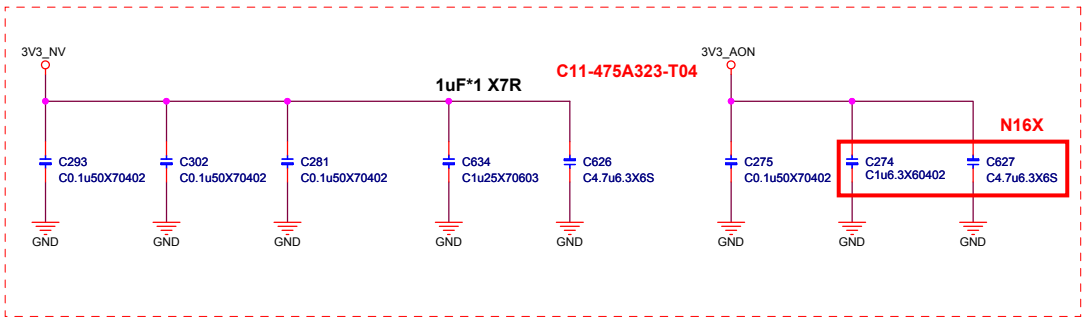
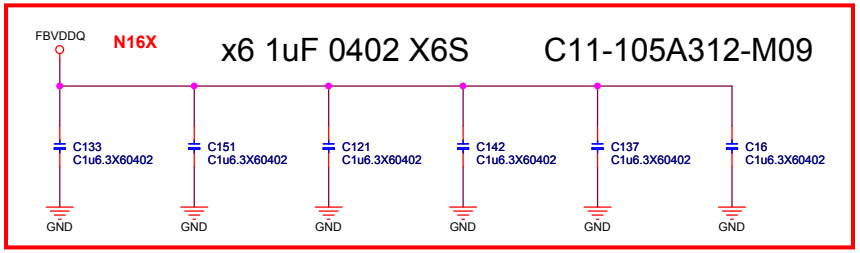
GPU DECOUPLING B











MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GPU DECOUPLING B

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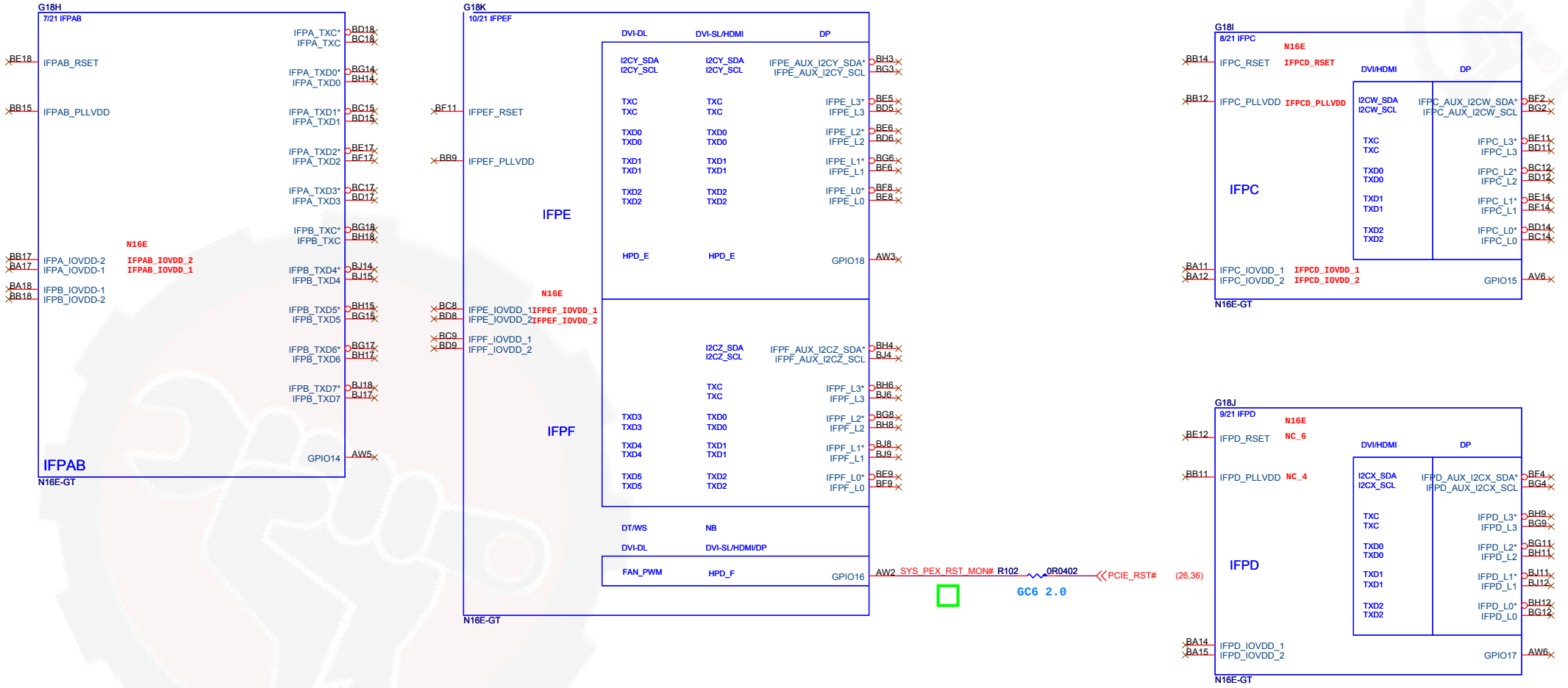
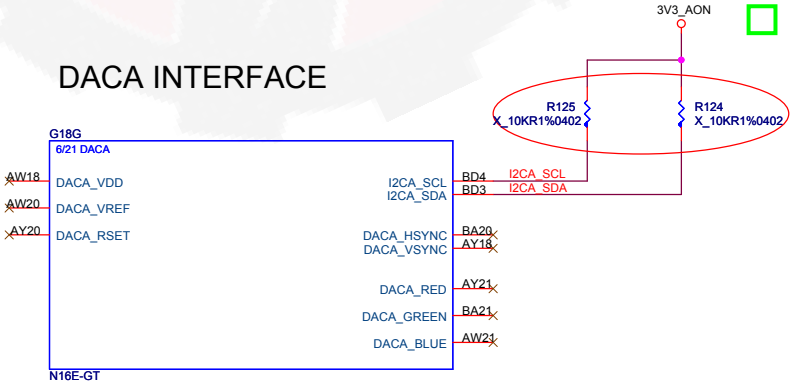
DACA,Display IF



DACA INTERFACE



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Title: DGPU_DACA,Display IF			
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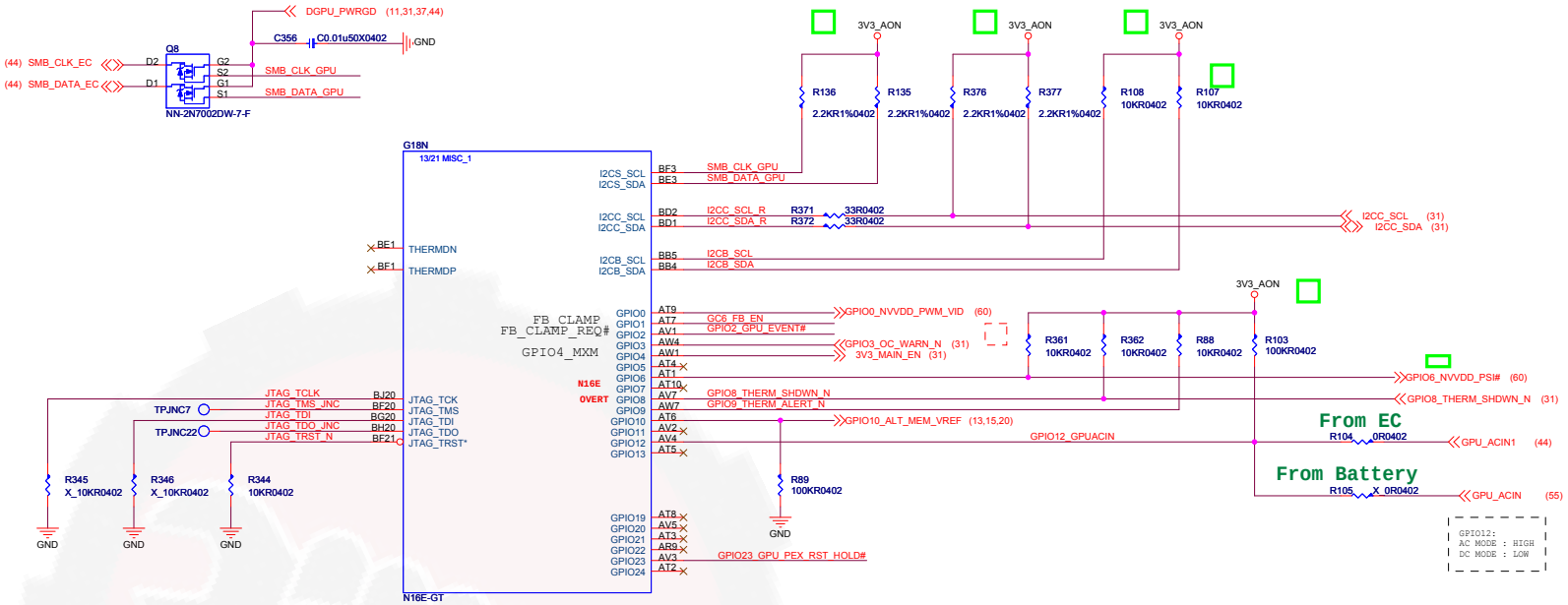
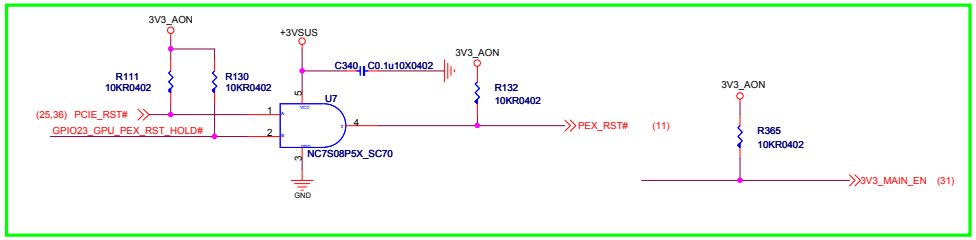
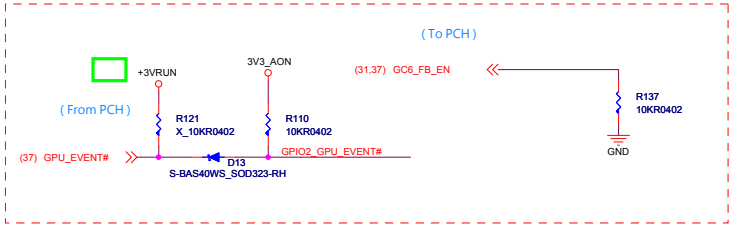
DGPU GPIO, I2C



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3 _AON
GPIO3	OC_WARN	I	Over current throttling	10K pull-up to 3V3 _AON
GPIO4	3V3_MAIN_EN	O	GPU POWER Sequencing for GC6 2.0	10K pull-up to 3V3 _AON
GPIO5	RESERVED			
GPIO6	PSI	O	Phase shedding	
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brighteness Control	100K pull-down
GPIO8	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3 _AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3 _AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPAB	
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	RESERVED			
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3 _AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIE self-reset control	10K pull-up to 3V3 _AON
GPIO24	MEM_VDD_CTL	O	Memory VDD VID	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_B	I	Hot Plug Detect for IFPB	
OVERT	OVERT(OVERT#)	I/O	Catastrophic Over Temperature	100K pull-up to 3V3 _AON





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Title: DGPU_GPIO,I2C

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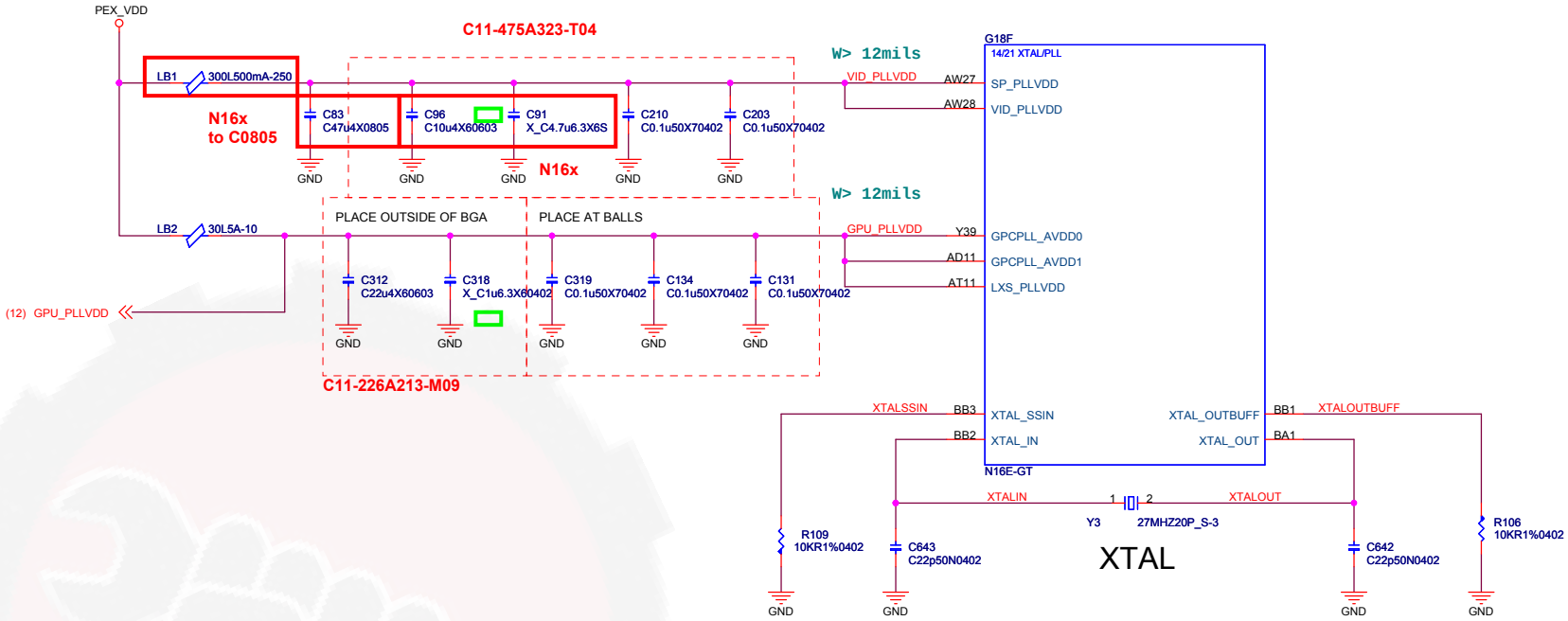
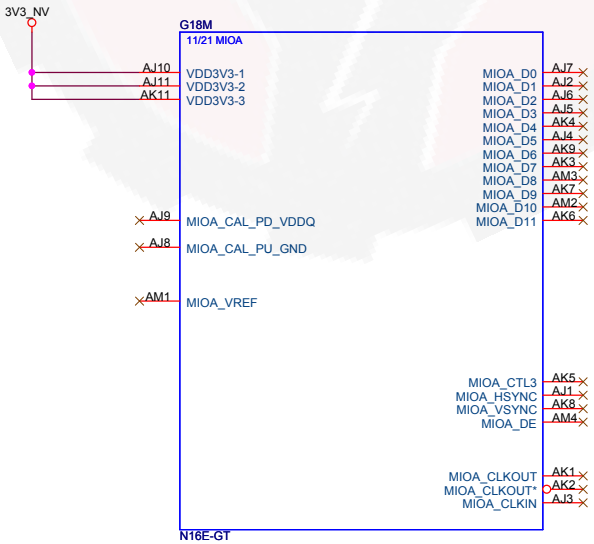
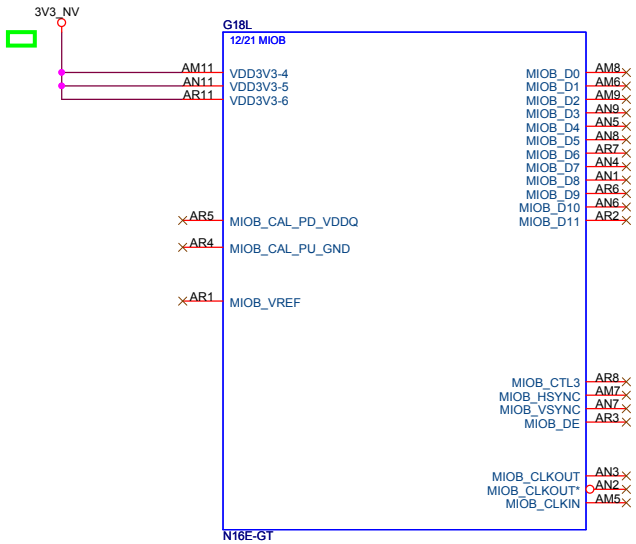
DGPU MIO & XTAL



Multi-use IO(MIO) Interface





MICRO-STAR INT'L CO.,LTD.

Title: DGPU MIO & XTAL

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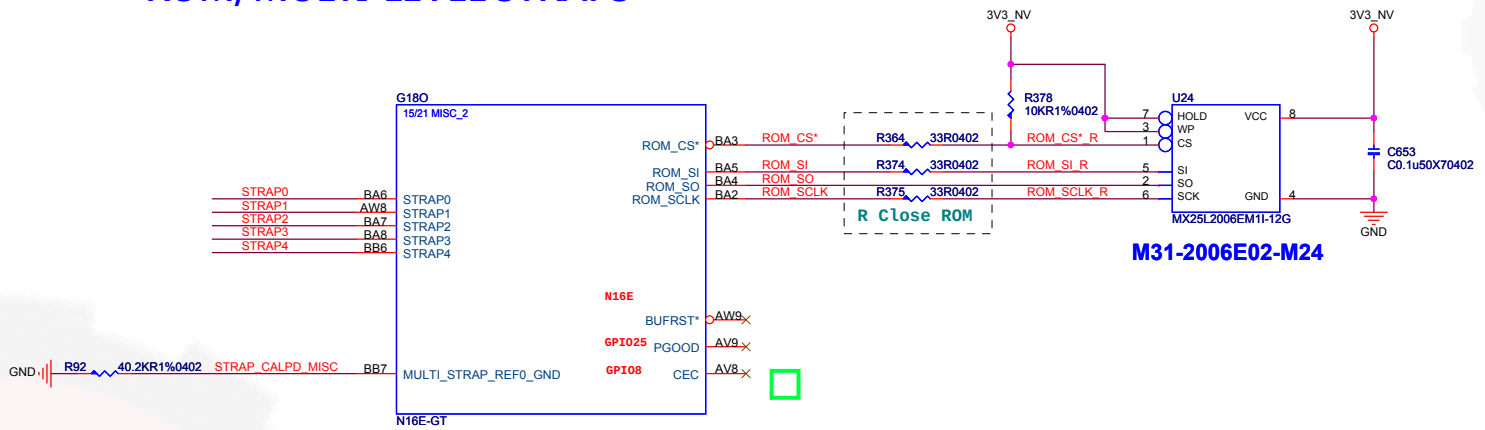
ROM, MULTI-LEVEL STRAPS

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

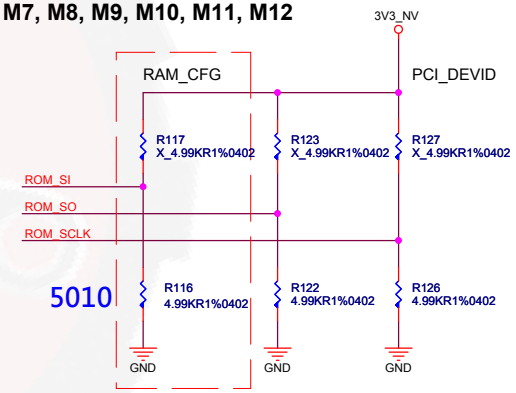


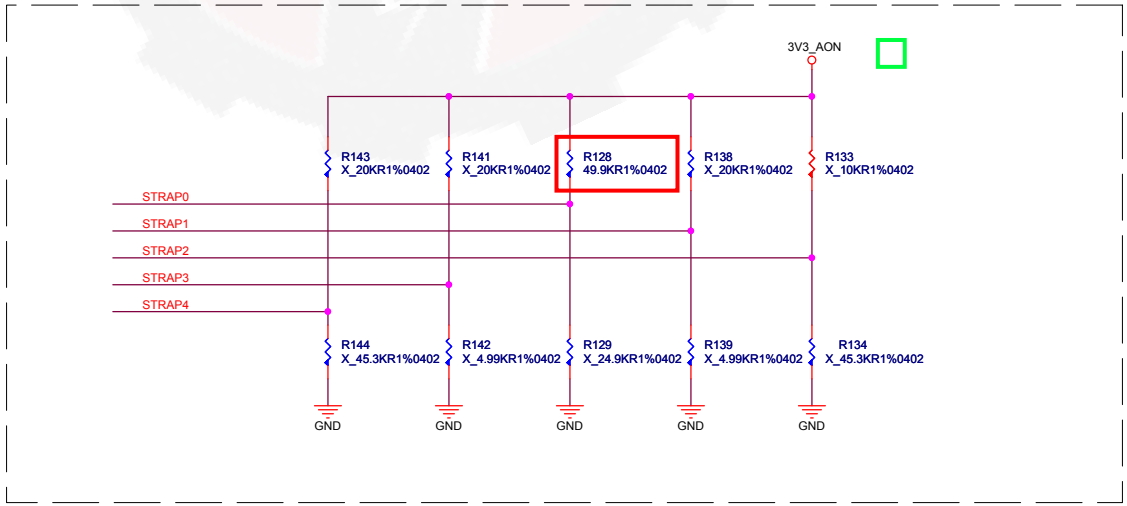
GDDR5 Parts
5010 : M1 , M2 , M3 , M4 , M5 , M6
5020 : M7, M8, M9, M10, M11, M12

ROM_H1 Hynix V_TOP1 V_BOT1
128Mx16bit 5010 5020
R11-0103T12-W08 M12-5GC2H05-H23 M12-5GC2H05-H23
X_10KR1%0402 X_H5GC2H24BFR-T2C X_H5GC2H24BFR-T2C
BOT 記得轉階層

DEFAULT SETTING

ROM_S1 Samsung V_TOP2 V_BOT2
128Mx16bit 5010 5020
R11-4991T12-W08 M12-2032585-S02 M12-2032585-S02
X_4.99KR1%0402 X_K4G20325FD-FC03 X_K4G20325FD-FC03





ROM_SI	RAM_CFG[3:0]	0x1 10K PD 0x0 4.99K PD	Hynix 128x16bit Samsung 128x16bit
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD	
ROM_SCLK	SOR_EXposed[3:0]	5K PD	
STRAP0		50K PU 3V3_AON	
STRAP1		Reserved	
STRAP2		Reserved	
STRAP3		Reserved	
STRAP4		Reserved	

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_ROM,HW Straps

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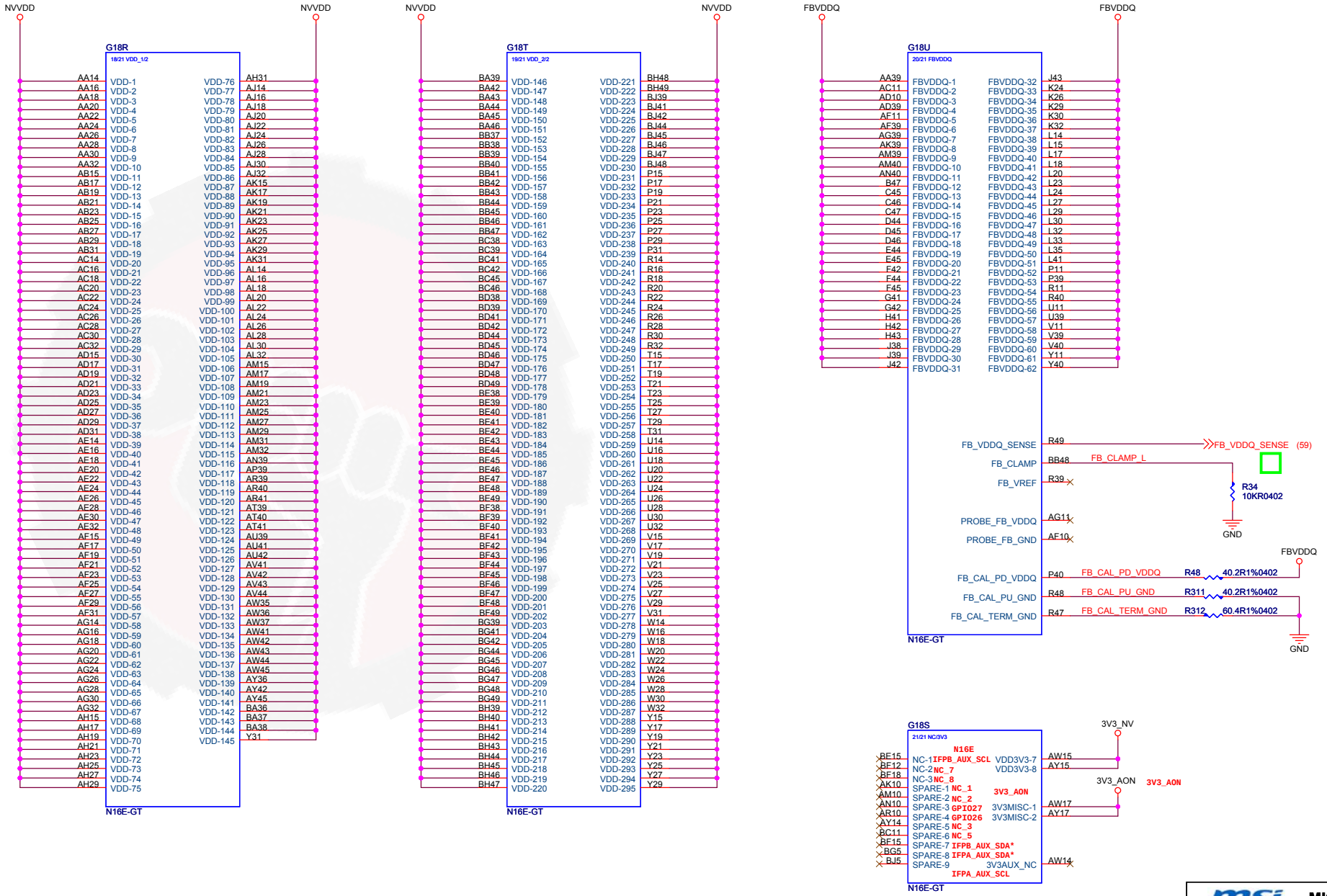
GPU NVVDD, FBVDDQ



Title	DGPU NVVDD, FBVDDQ
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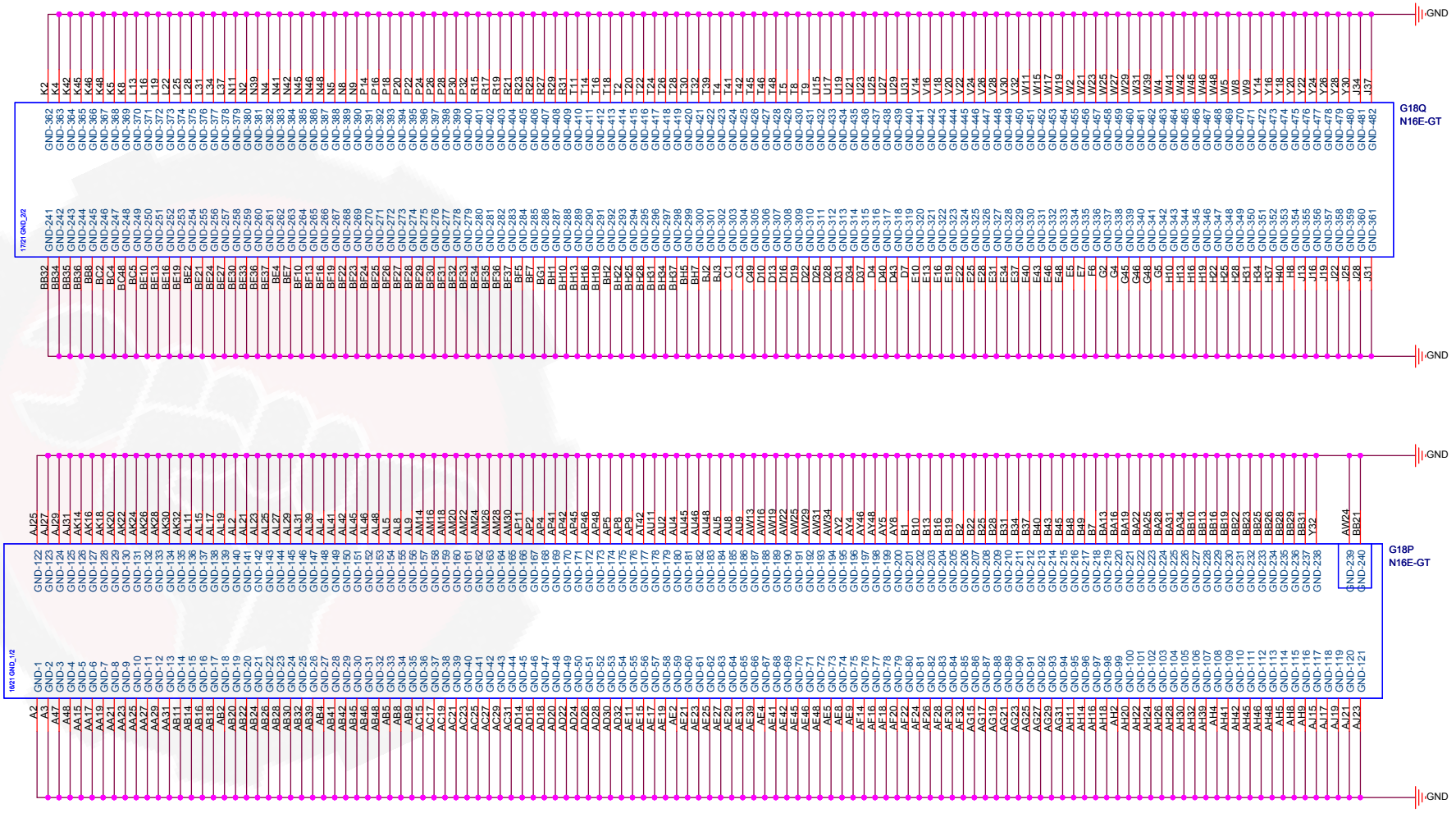
MICRO-STAR INT'L CO.,LTD.

DGPU GND



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Title: DGPU GND			
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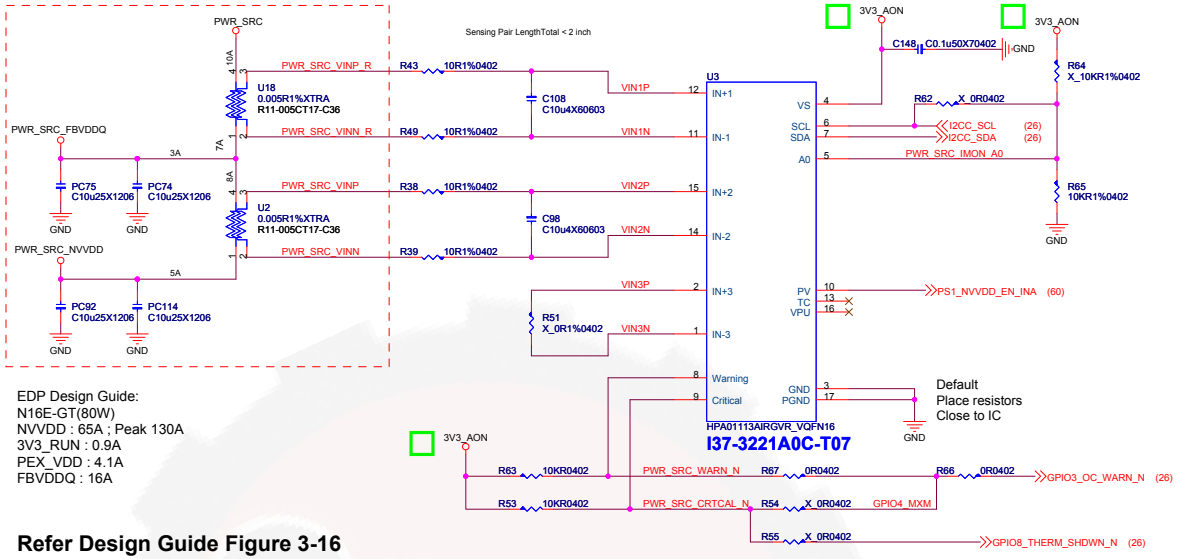
DGPU_Power Control

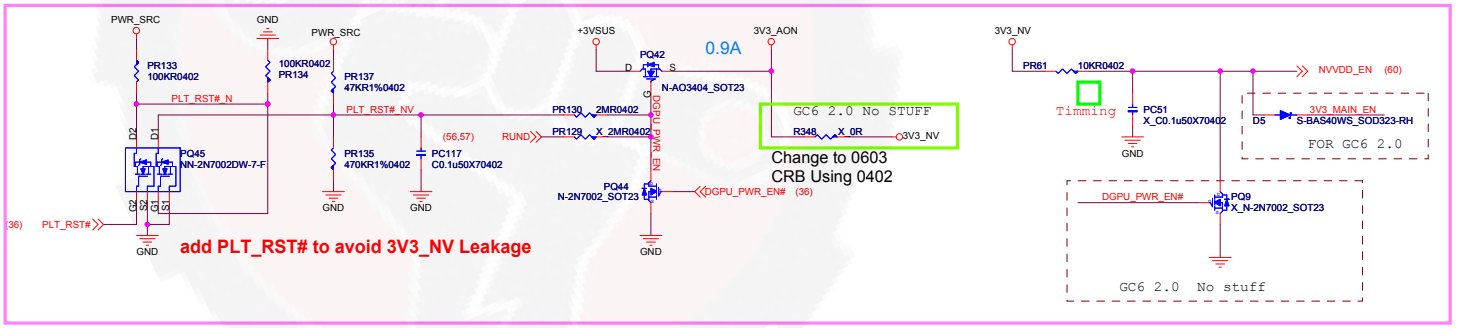


EDP Design Guide:
N16E-GT(80W)
NVVDD : 65A ; Peak 130A
3V3_RUN : 0.9A
PEX_VDD : 4.1A
FBVDDQ : 16A

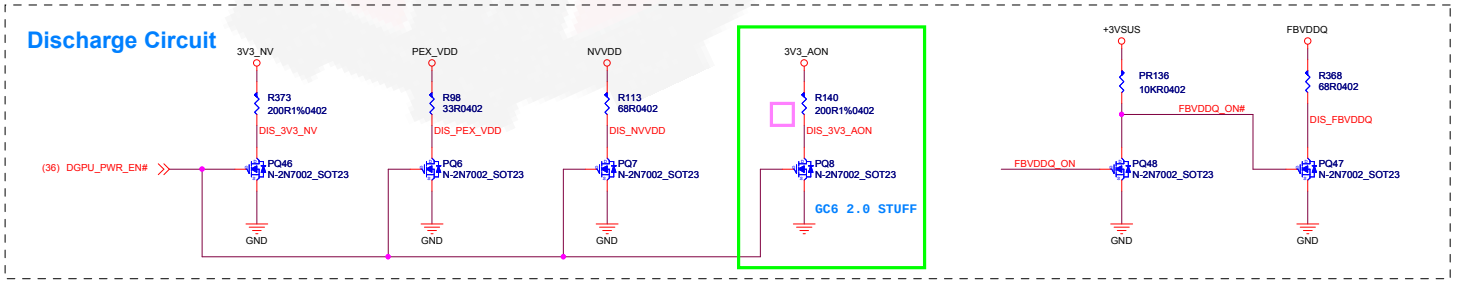
Refer Design Guide Figure 3-16

nVIDIA Power Sequence Control

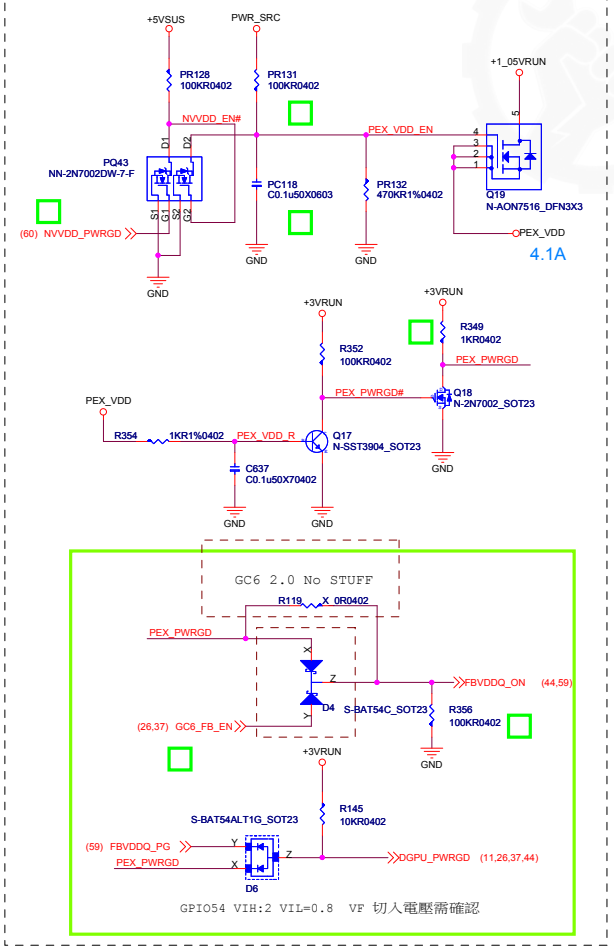
3V3_AON -> 3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD



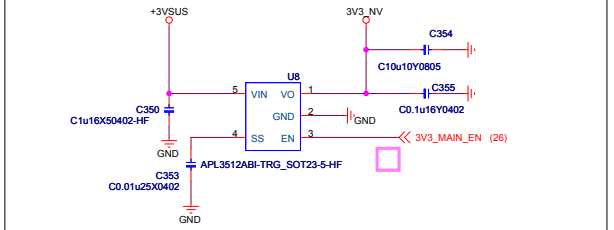
Discharge Circuit



PEX_VDD



GC6 2.0 STUFF



MSI MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_Power Control		
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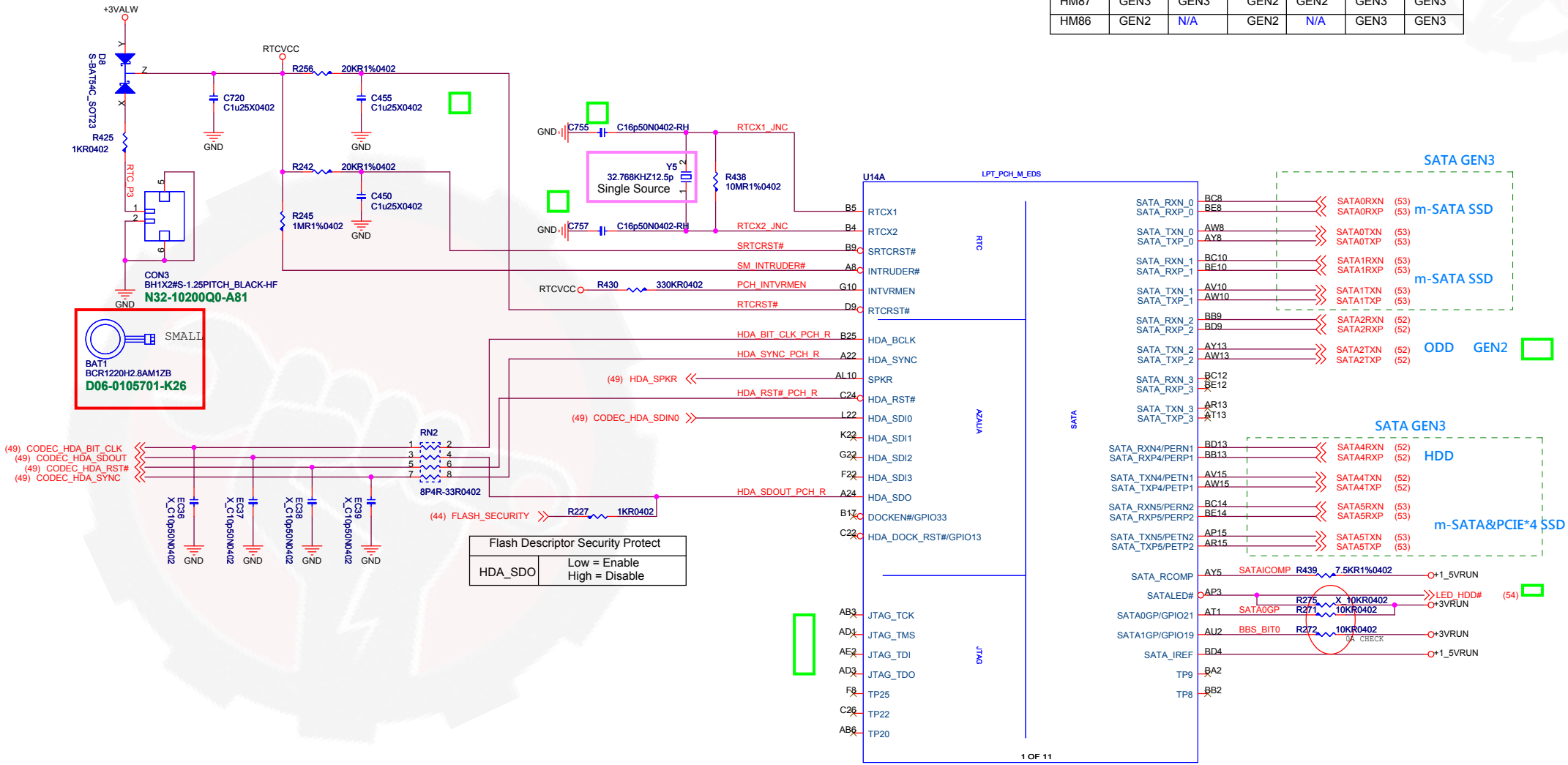
Lynx Point (HDA/JTAG/SATA)

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3



Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)

MICRO-STAR INT'L CO.,LTD.

Title: PCH-1 (HDA/JTAG/SATA)

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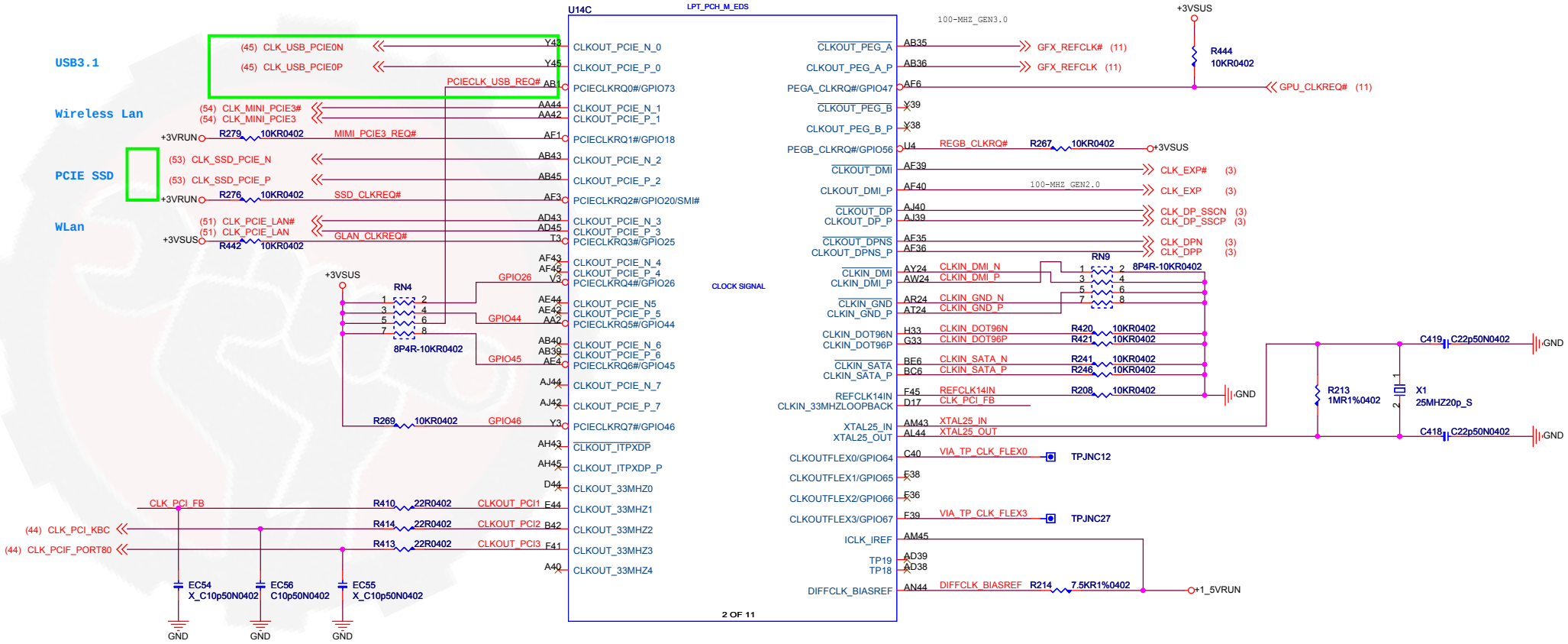
Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH. Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.



The CLKREQ# function can be disabled via intel management engine FW .Please refer to INTEL ME FW Bring up guide for configuring/disabling CLKREQ#

MICRO-STAR INT'L CO.,LTD.		
Title: PCH-2 (CLK)		
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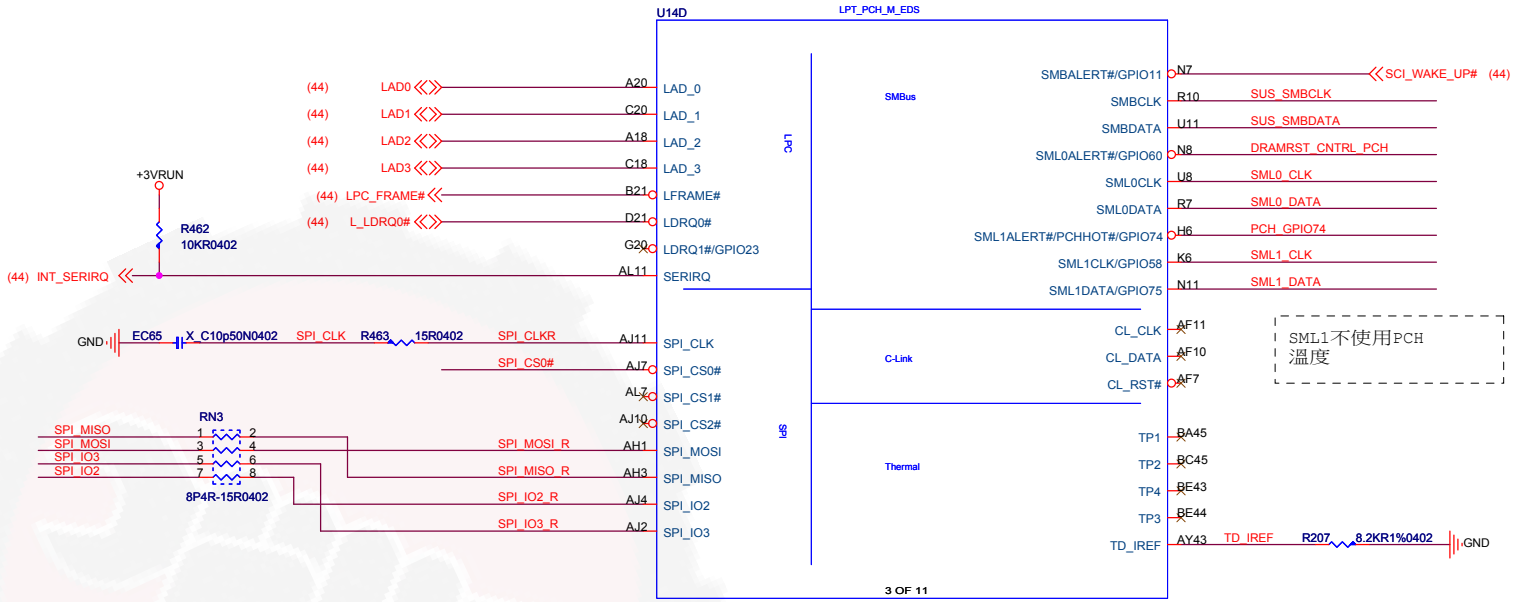
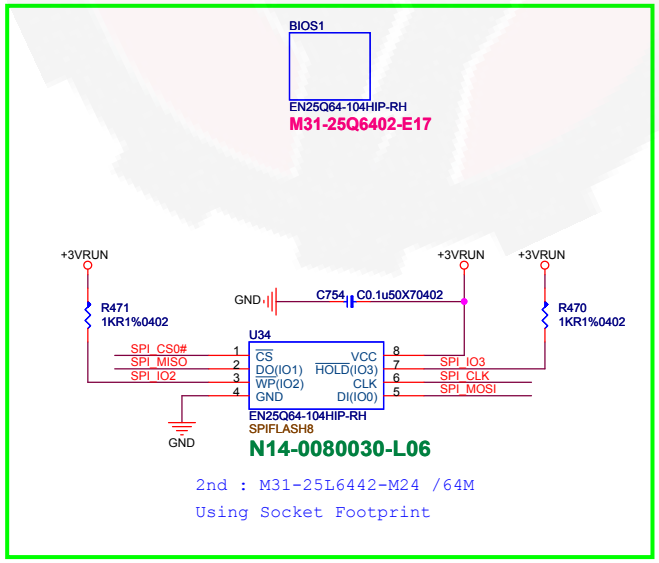
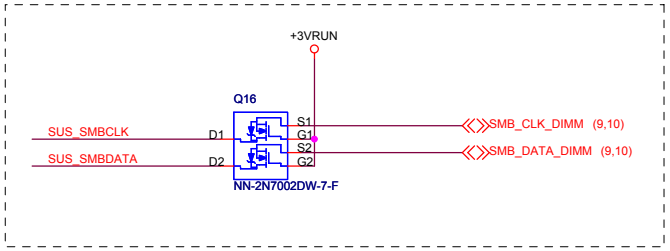
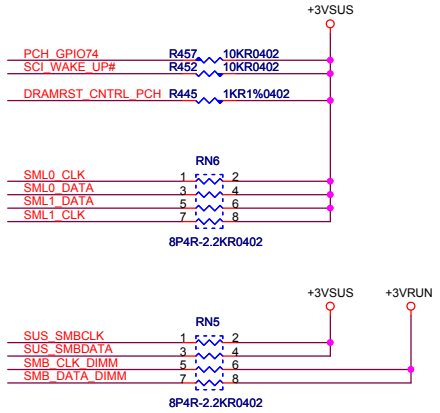
Lynx Point (LPC,SMBUS)









MICRO-STAR INT'L CO.,LTD.

Title: PCH-3 (LPC,SMBUS)

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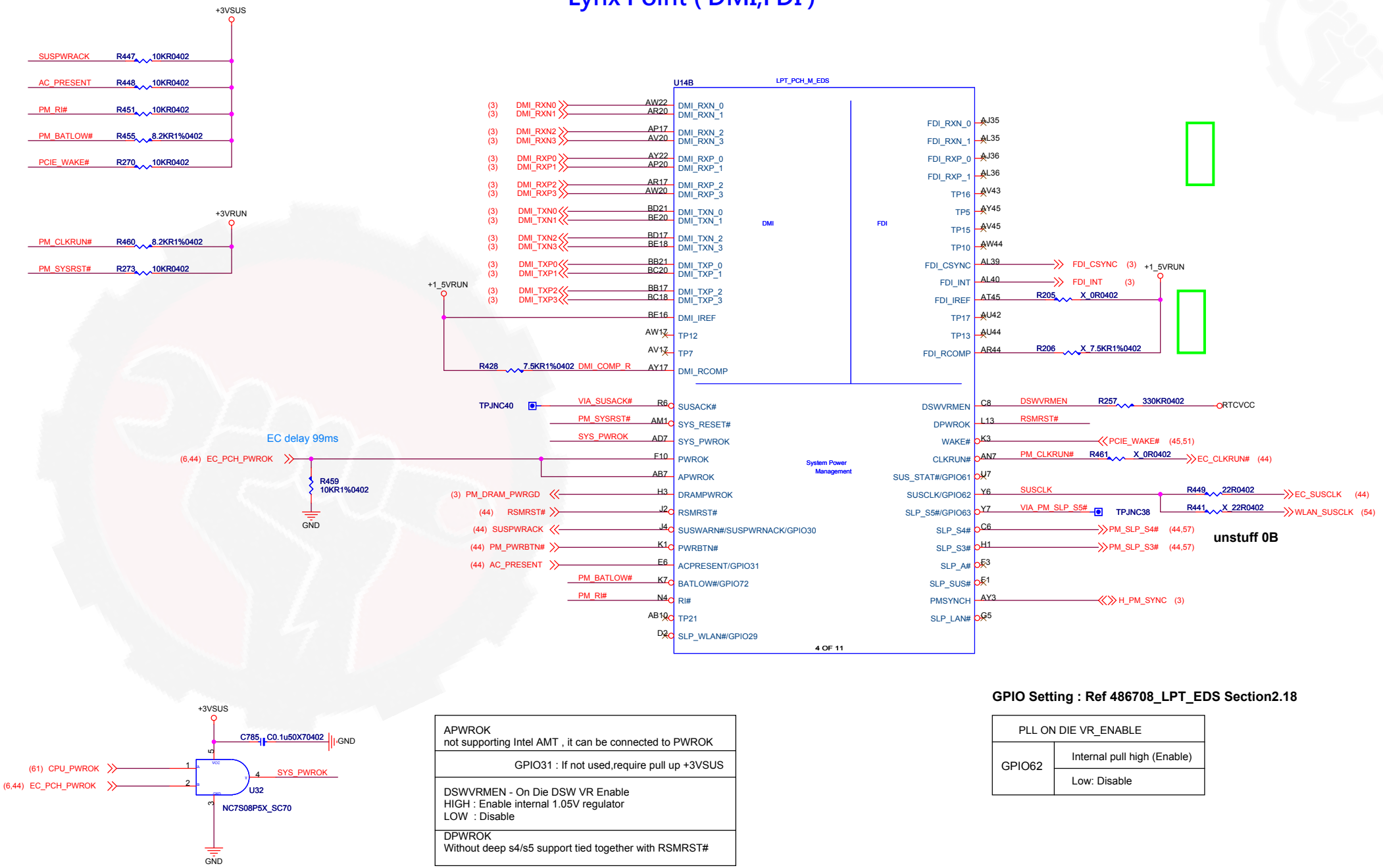
Lynx Point (DMI,FDI)



GPIO Setting : Ref 486708_LPT_EDS Section2.18

PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

APWROK not supporting Intel AMT , it can be connected to PWROK
GPIO31 : If not used,require pull up +3VSUS
DSWVRMEN - On Die DSW VR Enable HIGH : Enable internal 1.05V regulator LOW : Disable
DPWROK Without deep s4/s5 support tied together with RSMRST#

MICRO-STAR INT'L CO.,LTD.

Title: PCH-4 (DMI,FDI)

Size: | Document Number: MS-16J1 | Rev: 0A

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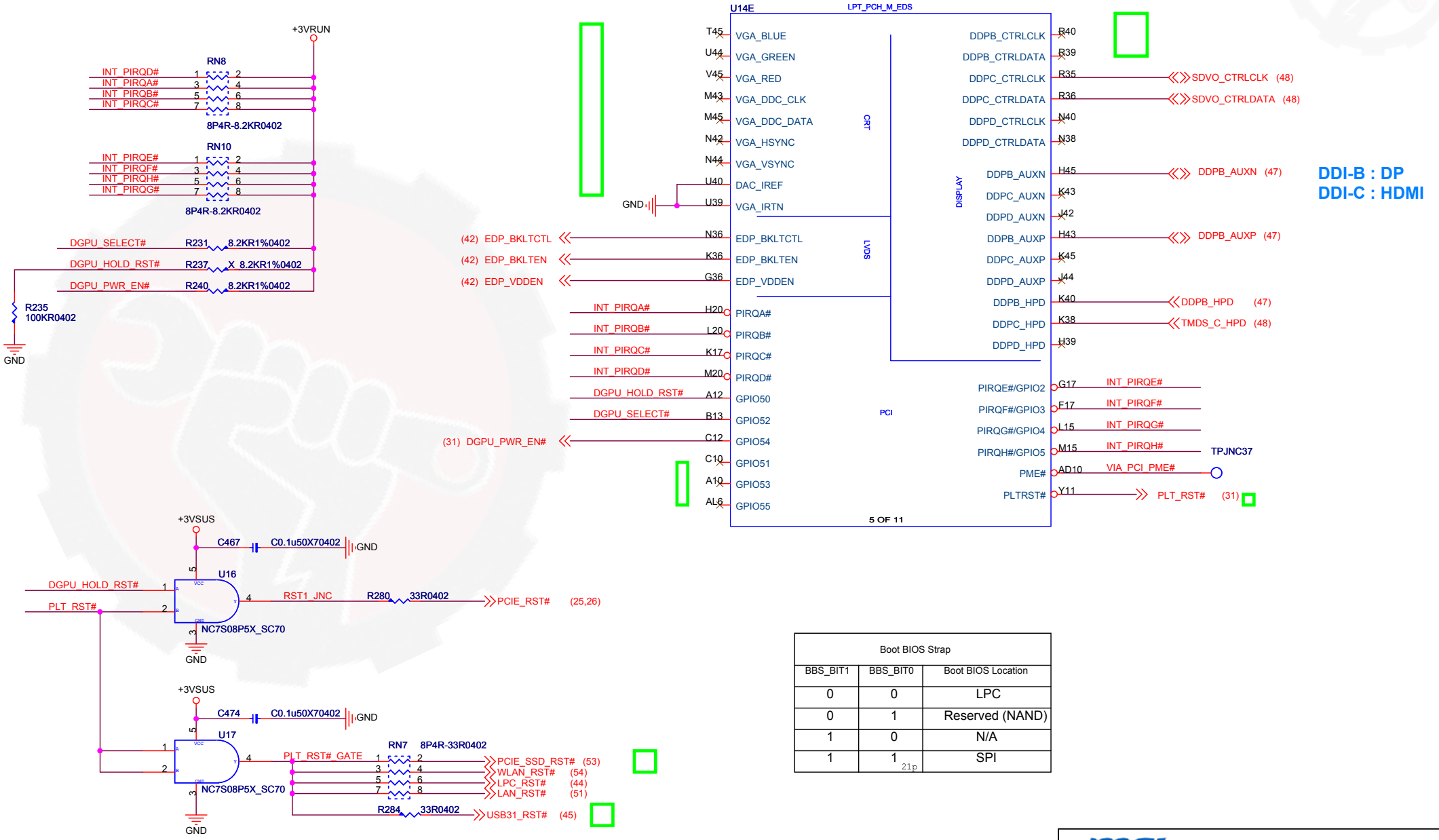
Lynx Point (PCI,DDI)



Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

21p

MICRO-STAR INT'L CO.,LTD.

Title: PCH-5 (PCI,DDI)

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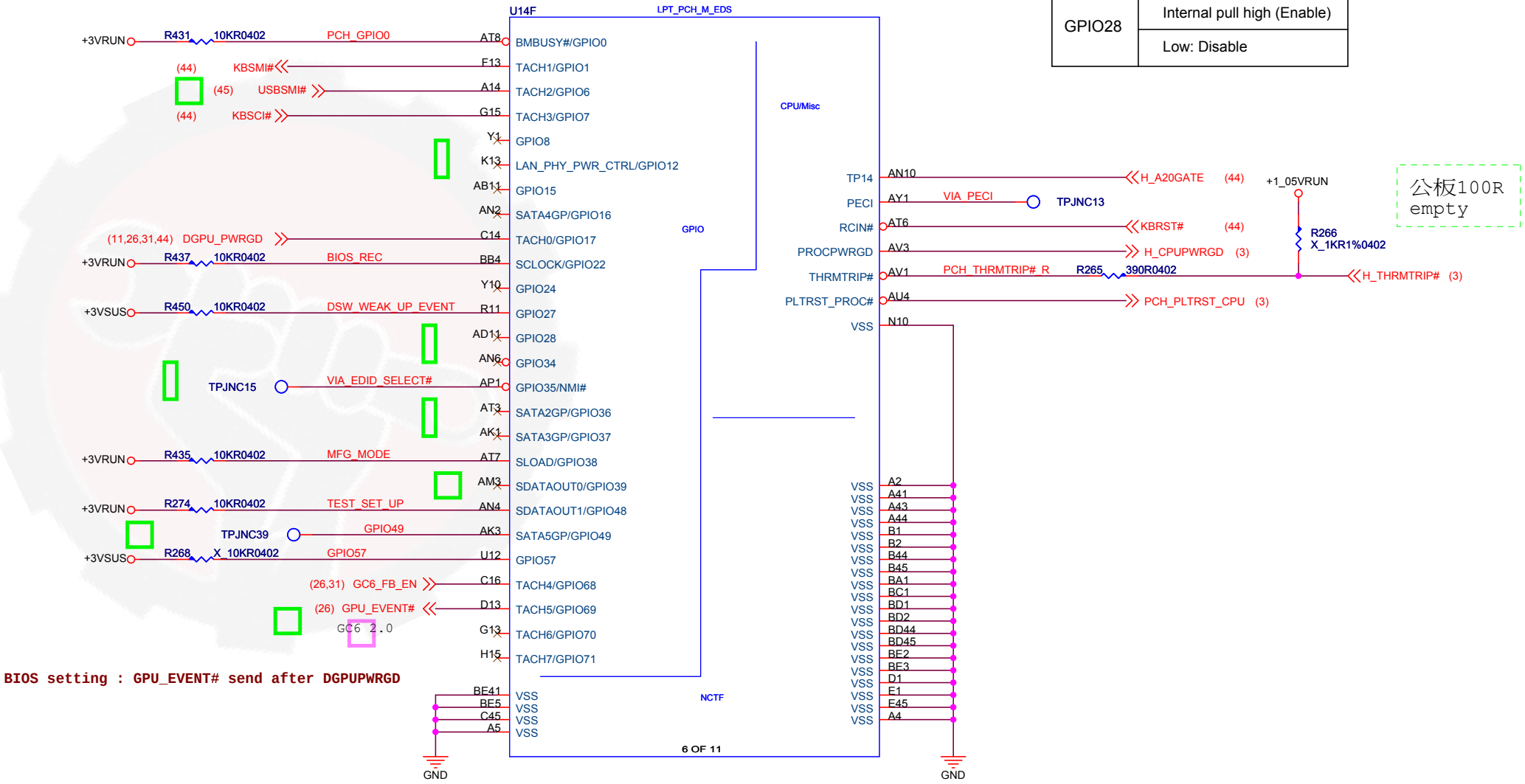
Lynx Point (GPIO,MISC)

GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



BIOS setting : GPU_EVENT# send after DGPUPWRGD

MICRO-STAR INT'L CO.,LTD.			
Title: PCH-6 (GPIO,MISC)			
Size	Document Number: MS-16J1		Rev: 0A
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Lynx Point (PCIE,USB)

Table 5-1. PCI Express* Ports 1 thru 4 - Supported Configurations

Port 1	Port 2	Port 3	Port 4
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

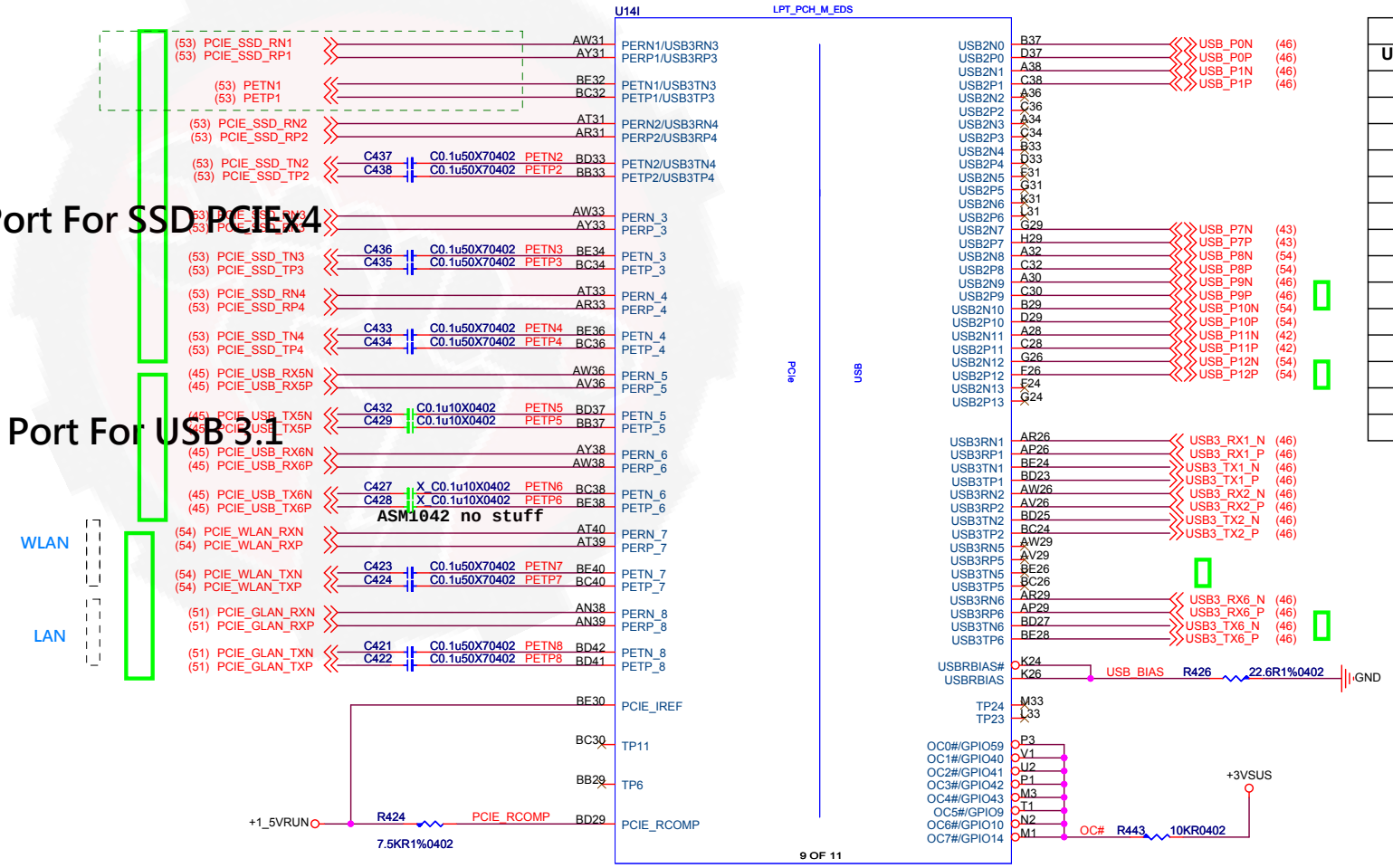
Table 5-2. PCI Express* Ports 5 thru 8 - Supported Configurations

Port 5	Port 6	Port 7	Port 8
x4			
x2		x2	
x2		x1	x1
x1	x1	x1	x1

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9

4 Port For SSD PCIEx4

2 Port For USB 3.1



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16J11
1	2	USB 3.0 Port 2	16J11 DEBUG PORT
2			
3			
4			
5			
6			
7		EPF021	3 色KBC
8		USB 2.0	16J12
9	6	USB 3.0 Port 6	16J11 CHARGER DEBUG PORT
10		WLAN	
11		WebCam	
12		CARDREADER	16J12
13			

HM86 沒USB3.0 PORT 5,6

WLAN

LAN

MICRO-STAR INT'L CO.,LTD.

Title: PCH-7 (PCIE,USB)

Size | Document Number: MS-16J1 | Rev: 0A

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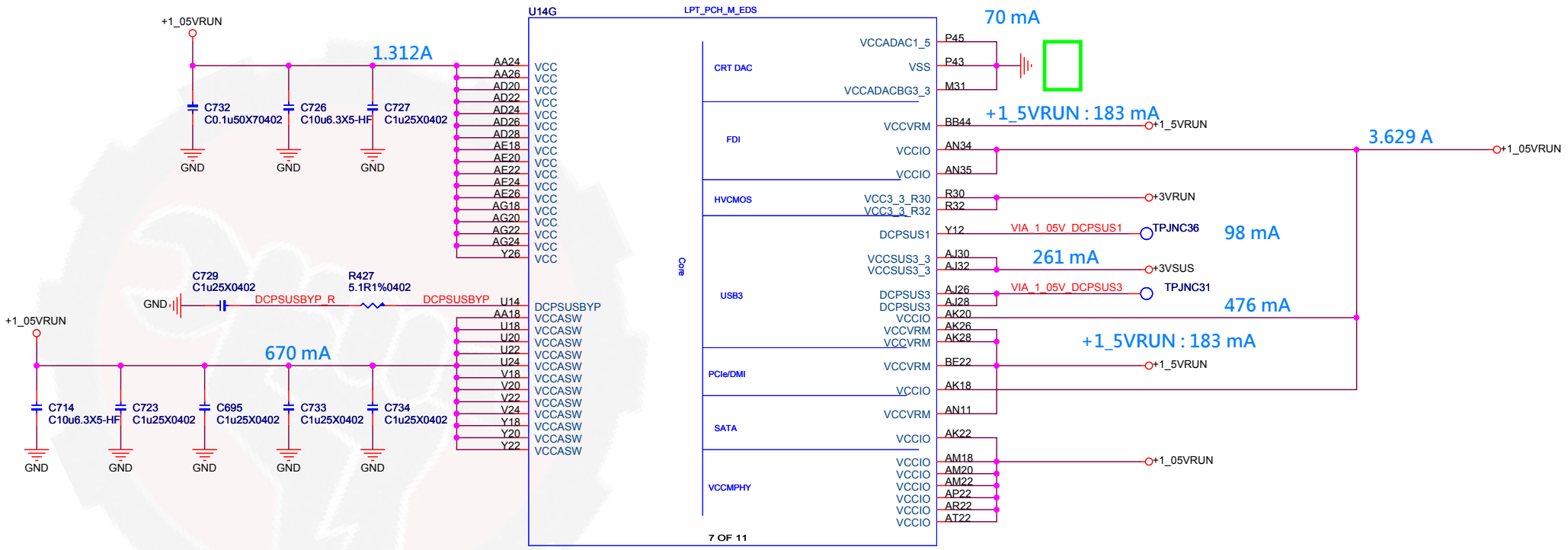
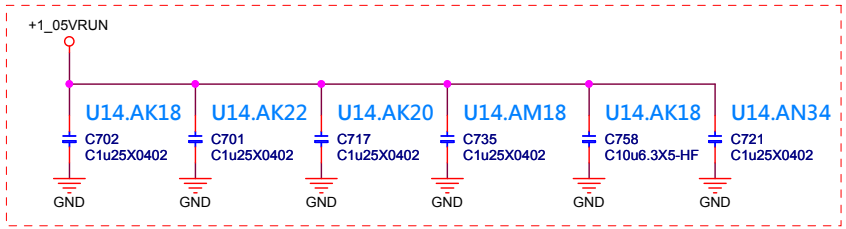
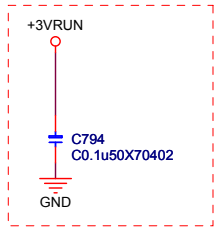
Lynx Point (Power)







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Title: PCH-8 (Power)

Size | Document Number: MS-16J1 | Rev: 0A

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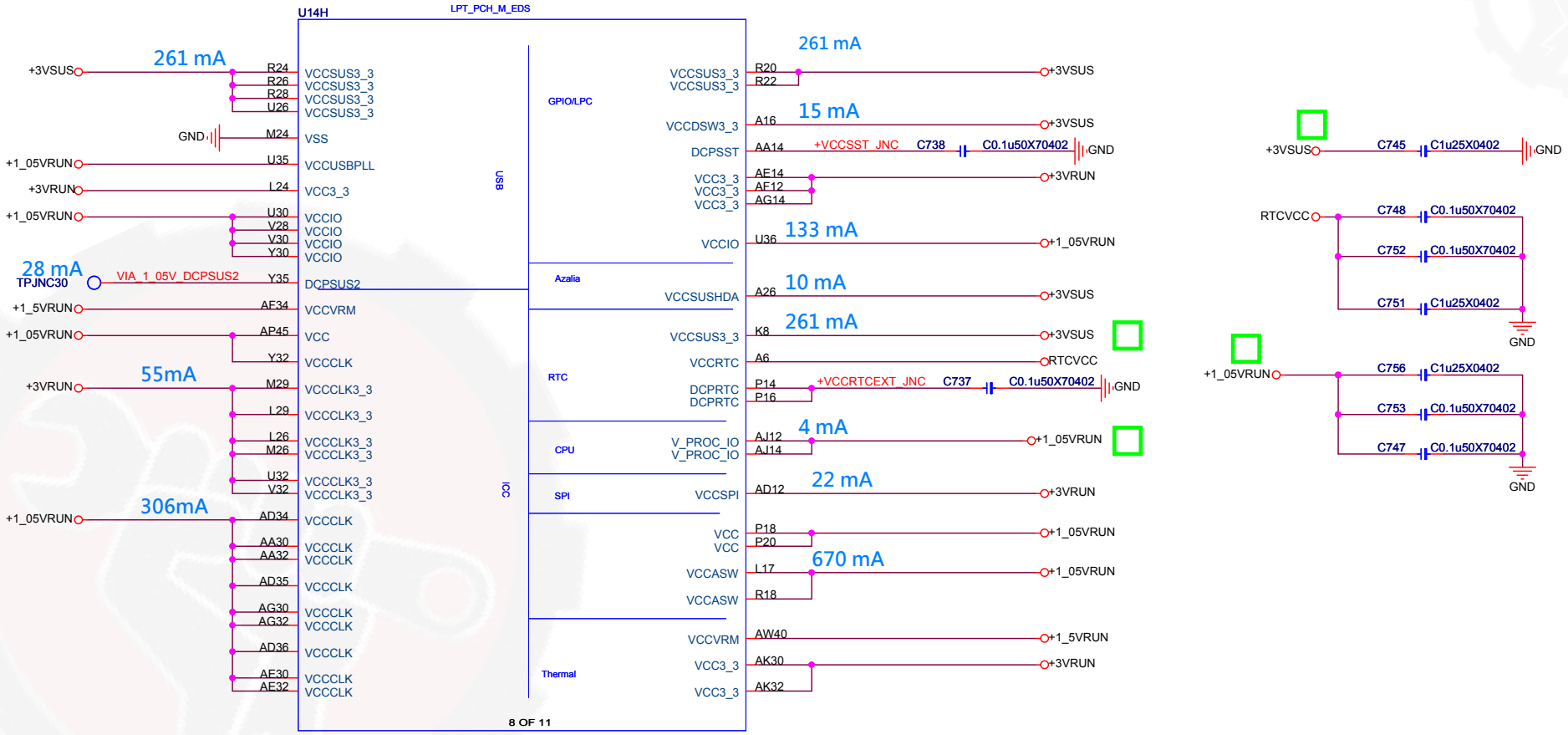
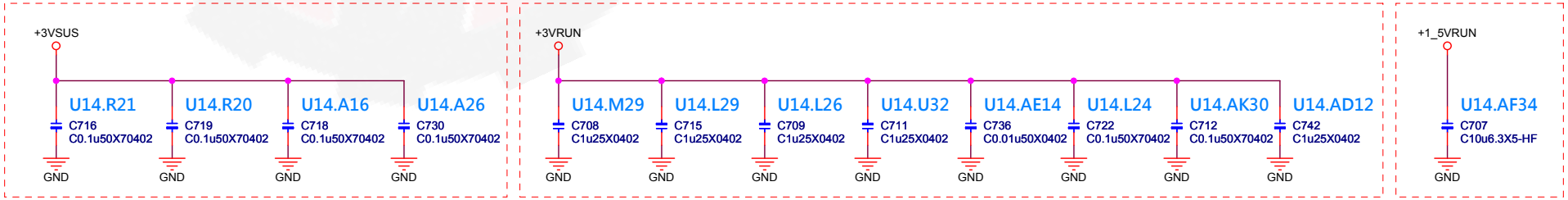
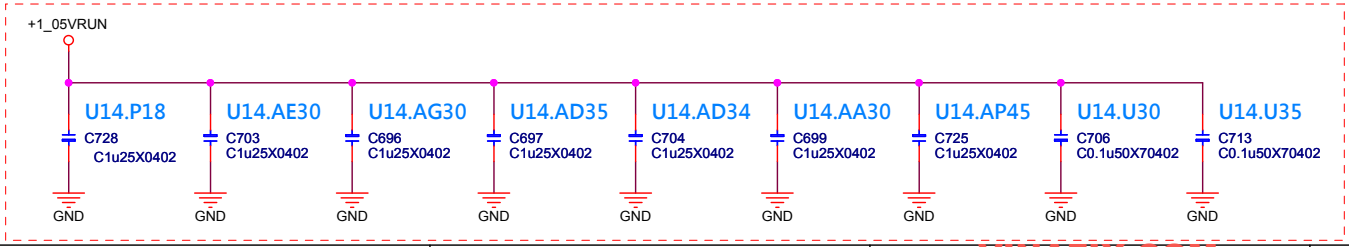
Lynx Point (Power)







MICRO-STAR INT'L CO.,LTD.

Title: PCH-9 (Power)

Size | Document Number: MS-16J1 | Rev: 0A

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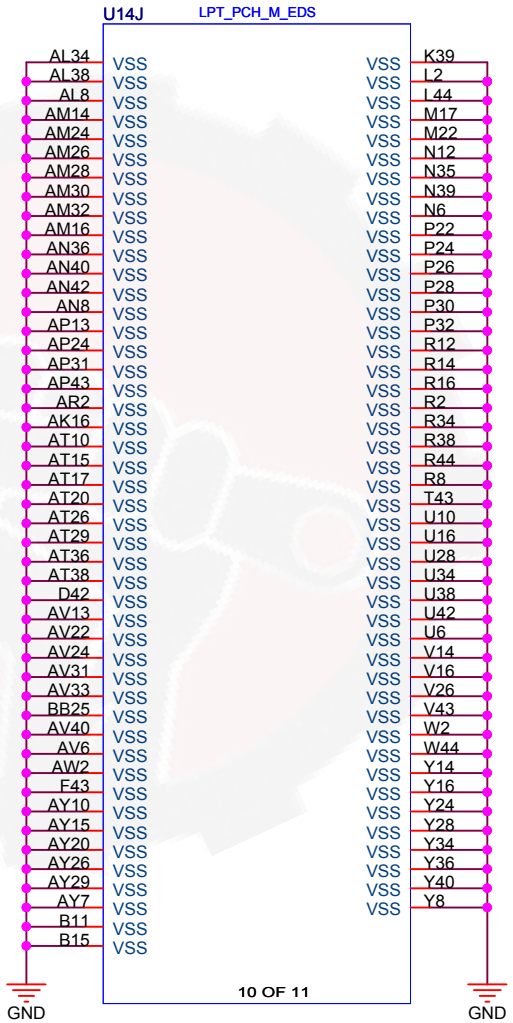
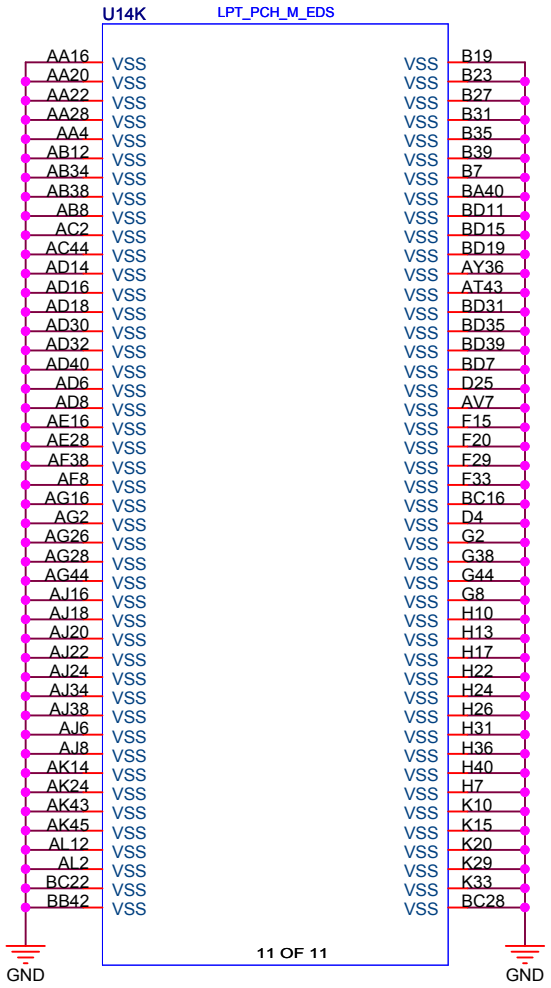
Lynx Point (GND)





MICRO-STAR INT'L CO.,LTD.		
Title: PCH-10 (GND)		
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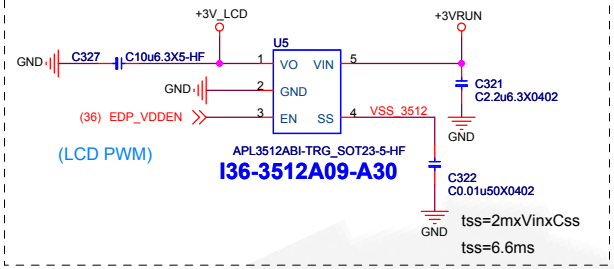
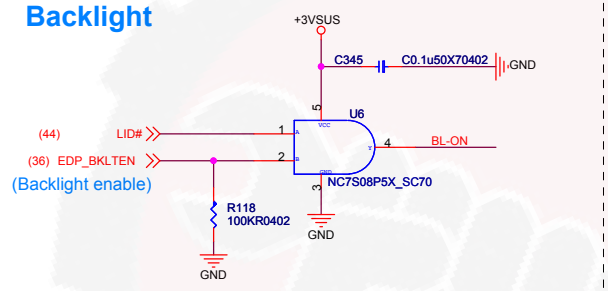
eDP

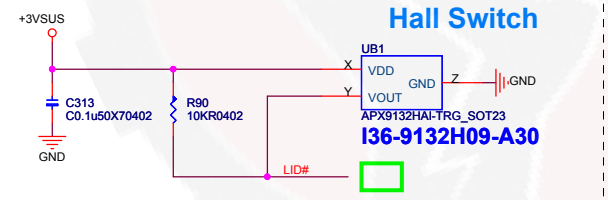
Pannel Device Logic Power



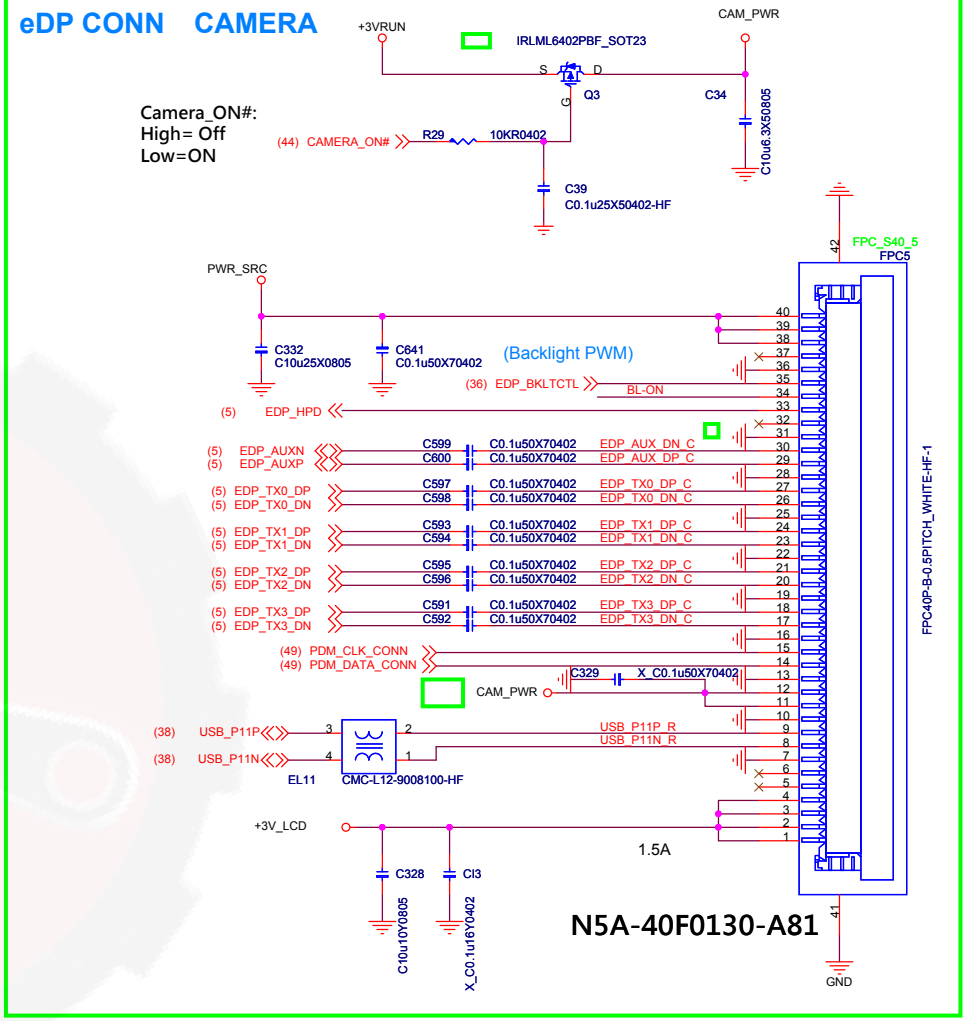
Backlight



Hall Switch

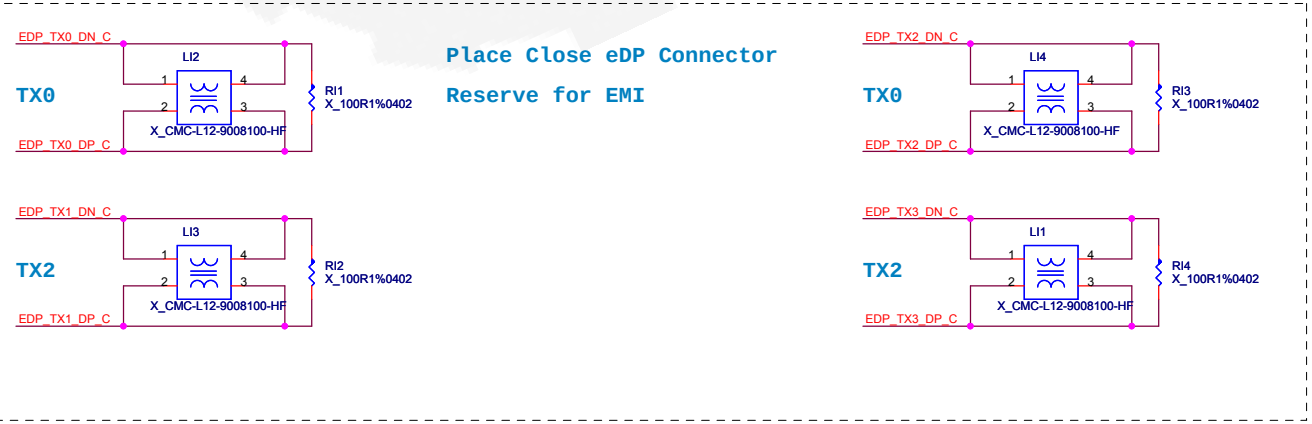


eDP CONN CAMERA



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



MICRO-STAR INT'L CO.,LTD.

Title: eDP /Camera

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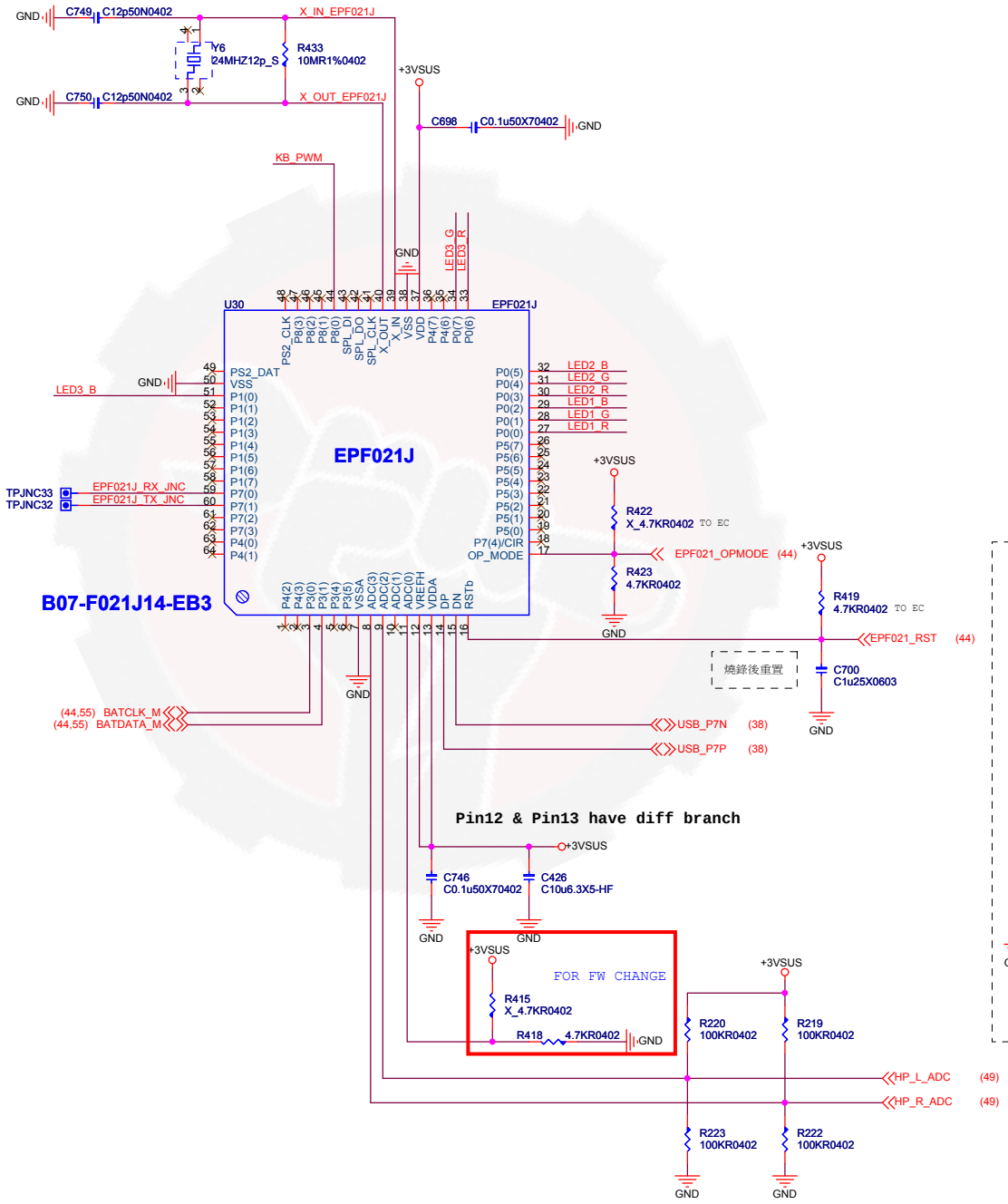
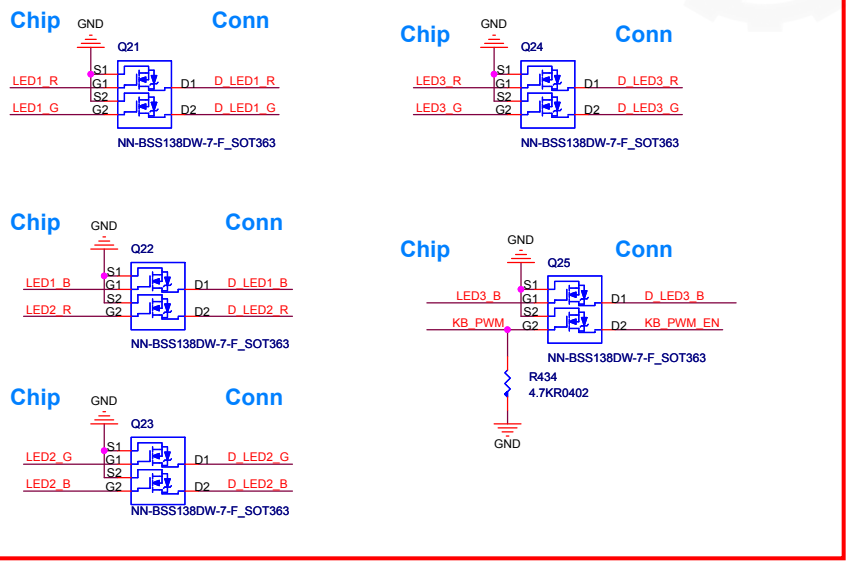
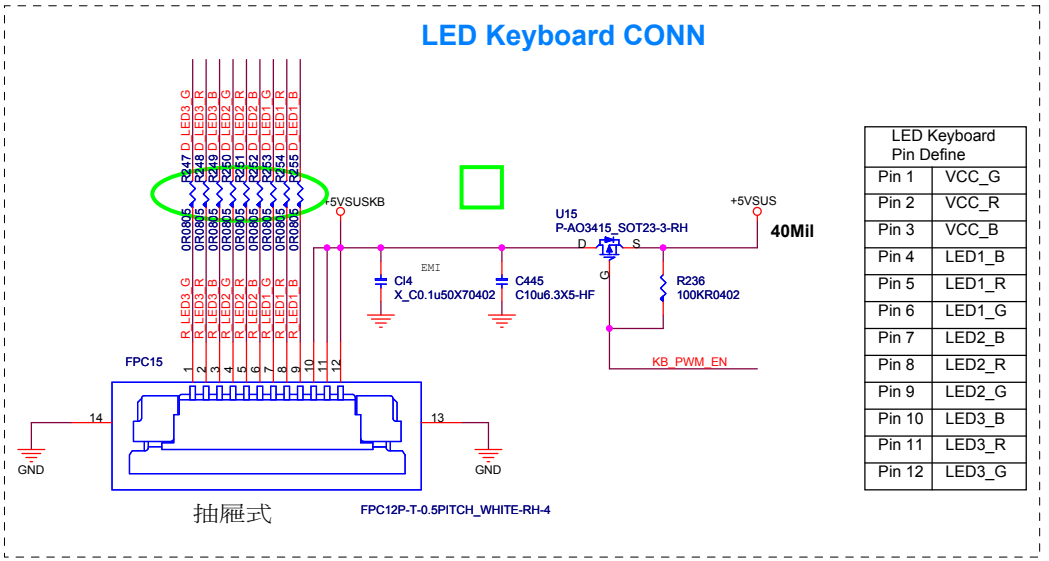
LED 8051 Controller



EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED_8051

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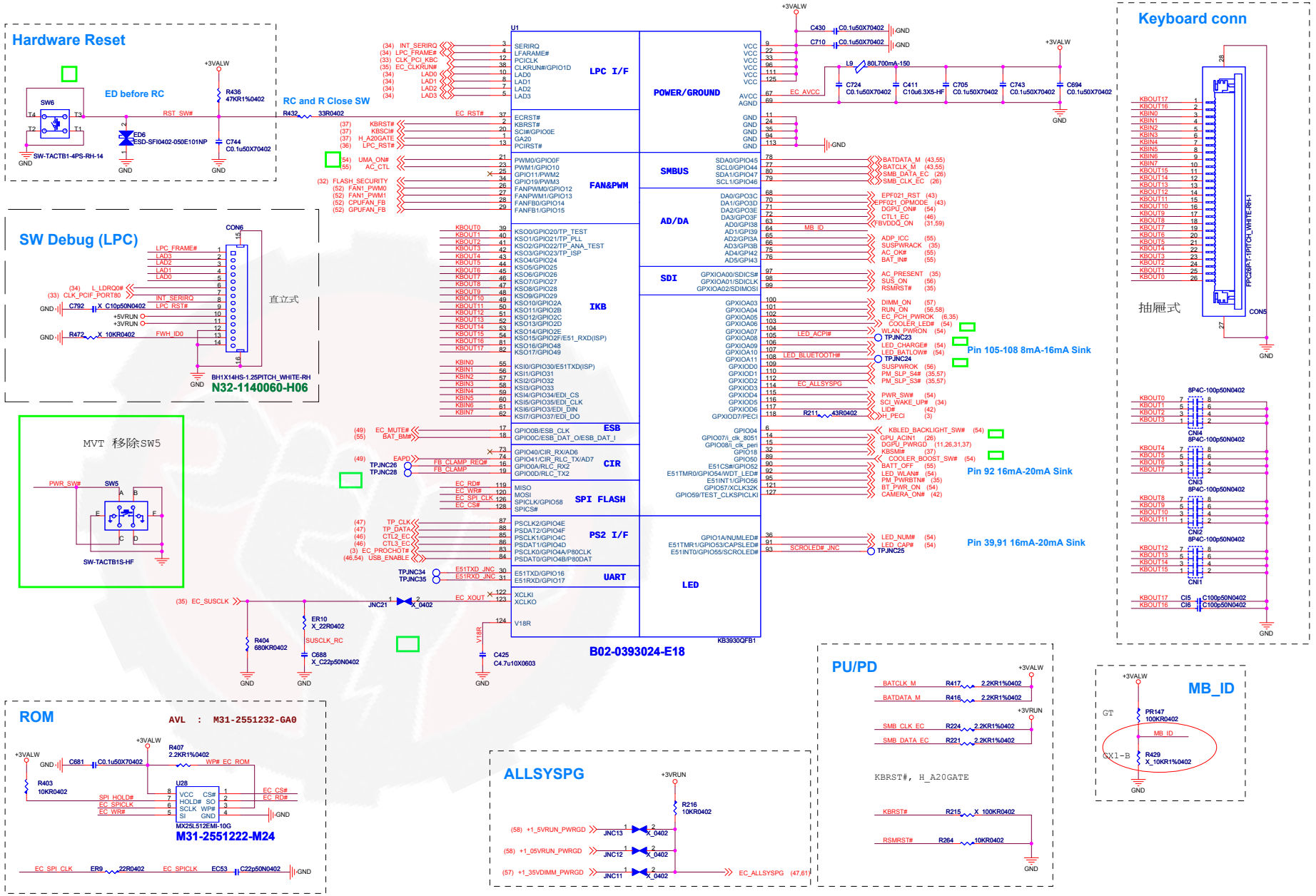
KBC(KB3930QFB1)



msi	MICRO-STAR INT'L CO.,LTD.		
Title	KBC(KB3930QFB1)		
Size	Document Number		Rev
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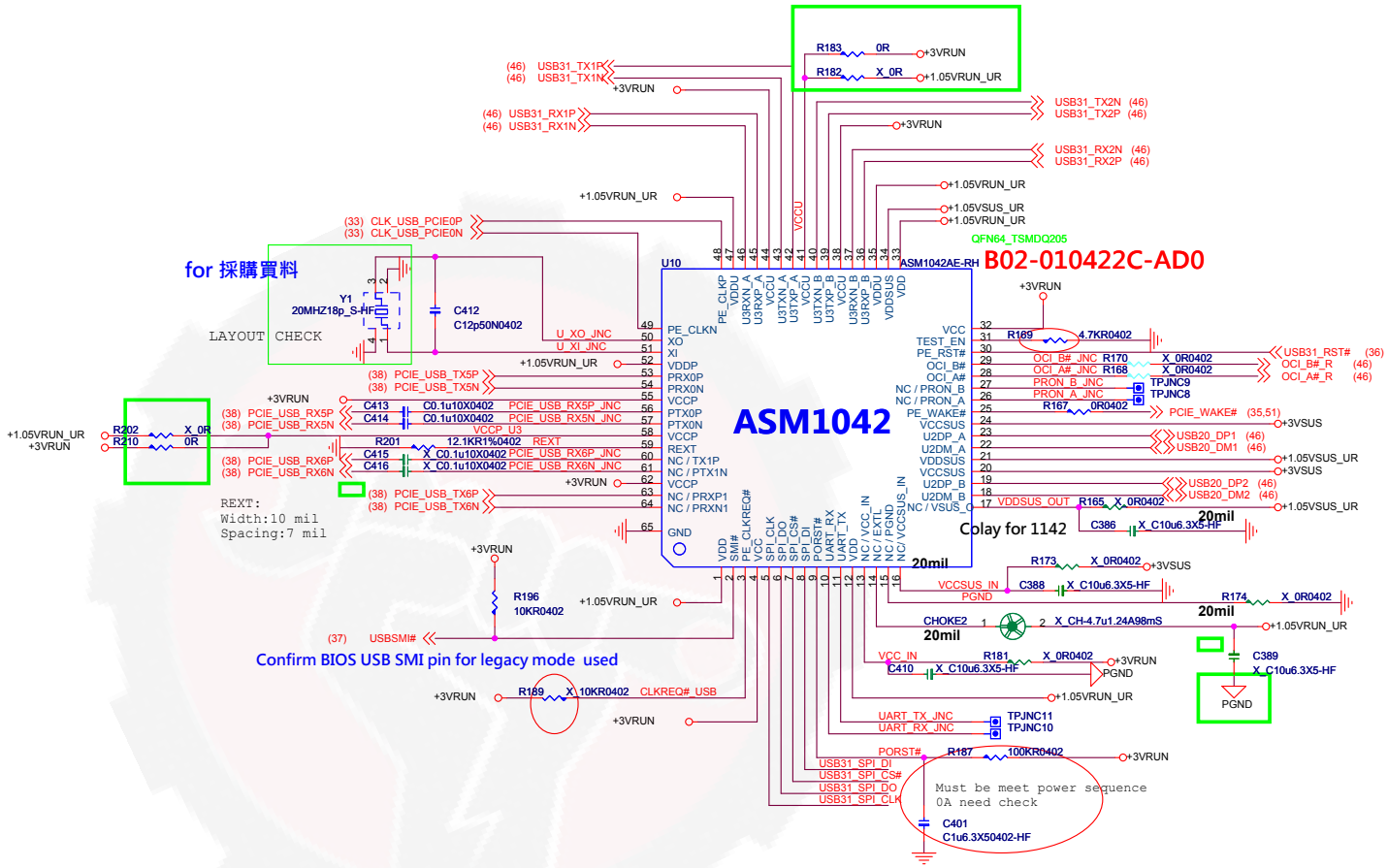
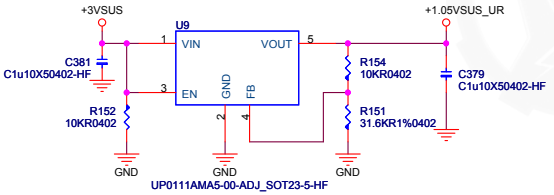
PCIE to USB 3.1

USB 3.0/ USB.3.1

BOM DEFAULT 1042 (USB3.0) CHECK FUNCTION
VDD= 1.05V



ASM1042 stuff



ASM1142 含內轉1.05V時不上件

HW strap

PE_PWRDET fuction

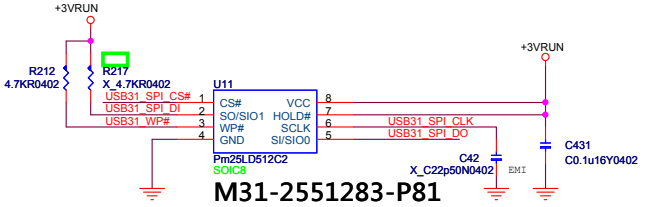
PU for D3cold (detect AUXpower)

Internal PU

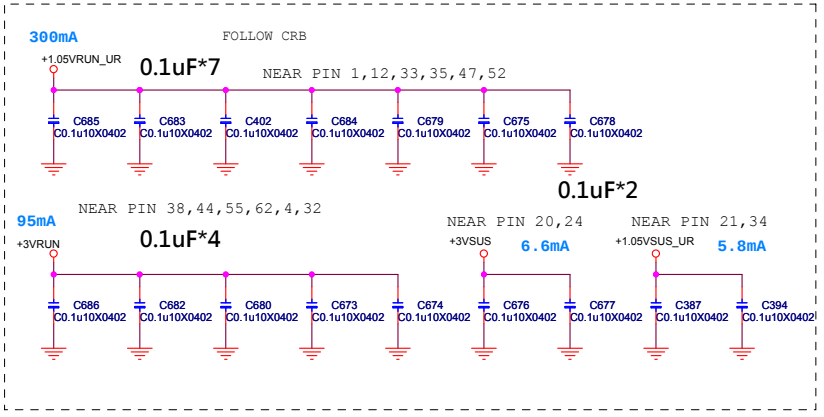
UART_TX_JNC
UART_RX_JNC

CSEL1(RX):CSEL0(TX) Clock select
11:External 20MHz Crystal
01:48MHz Clock Input
X0:Reserve for Test Mode

SPI ROM For FW (stuff first)



需使用與EC ROM不同的料號上件



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Title: USB 3.0 / USB 3.1

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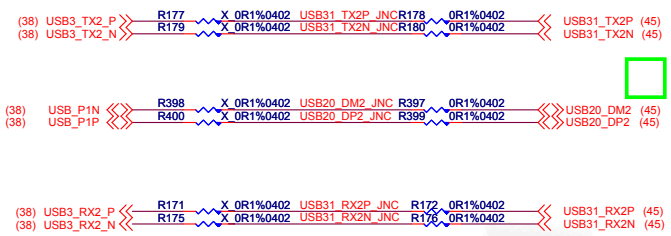
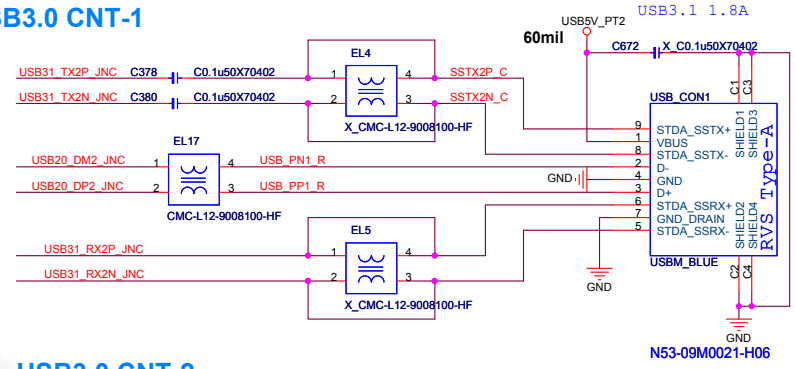
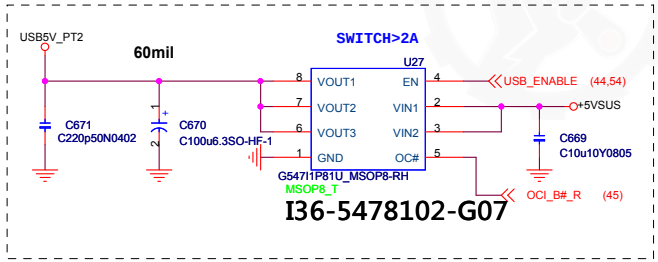
USB 3.1 Port 1

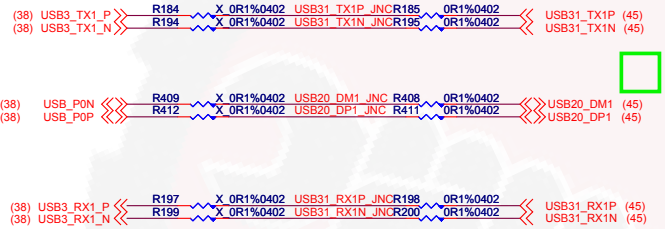


USB3.0 CNT-1

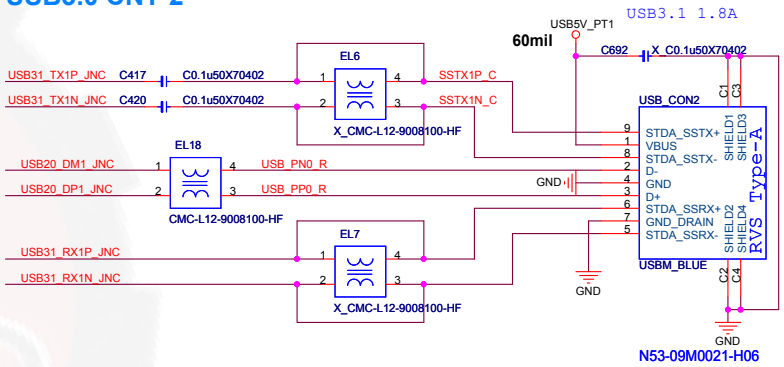


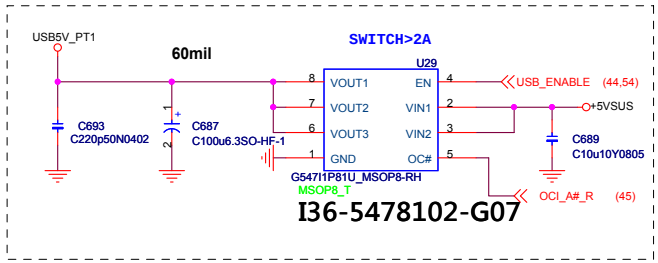


USB 3.1 Port 2

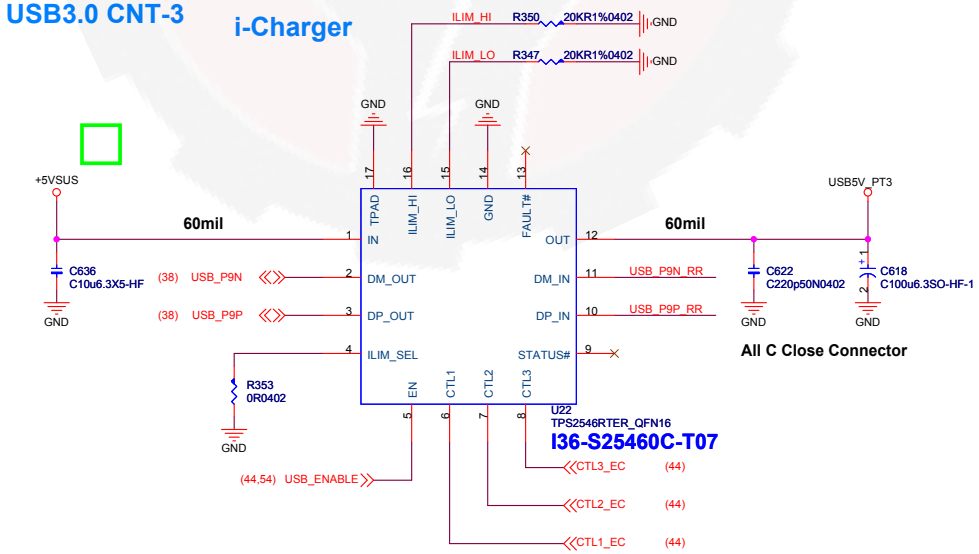


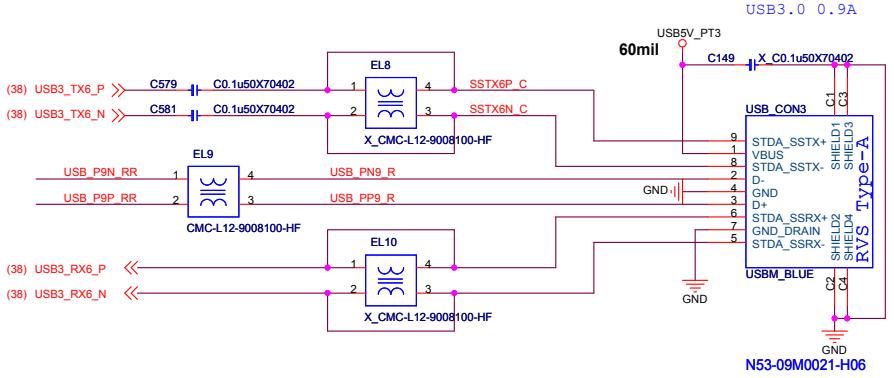
USB3.0 CNT-2





USB3.0 CNT-3





MICRO-STAR INT'L CO.,LTD.

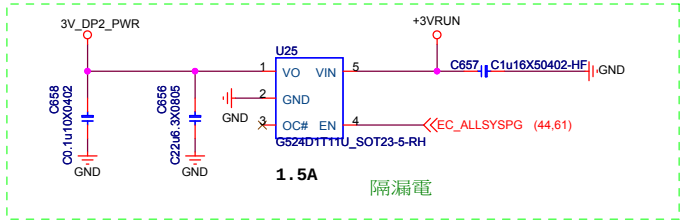
Title: USB 3.0 /iCharger

Size | Document Number: MS-16J1 | Rev: 0A

Date: Tuesday, July 29, 2014 | Sheet 46 of 70

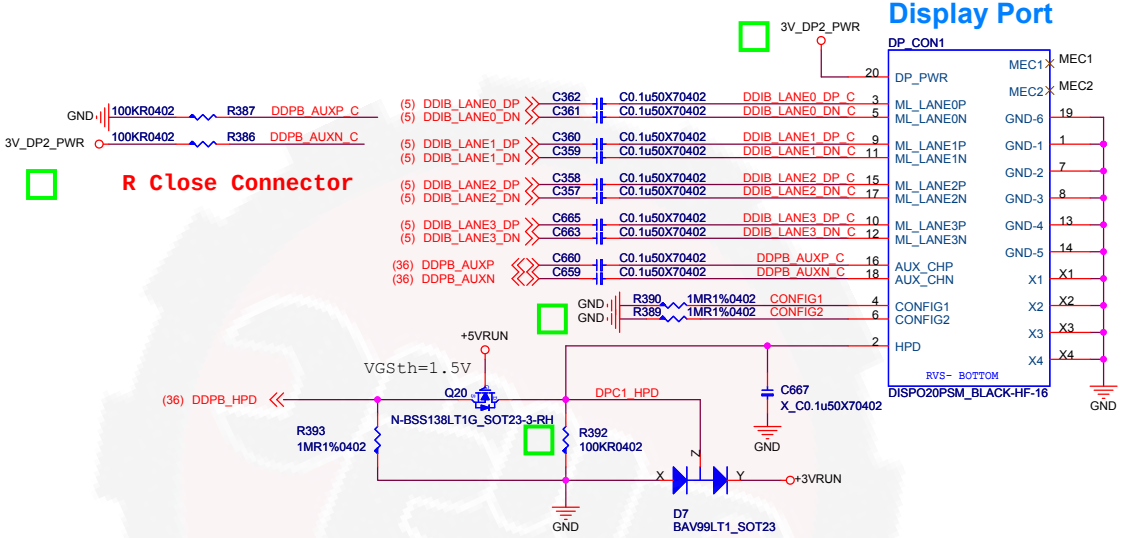
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.

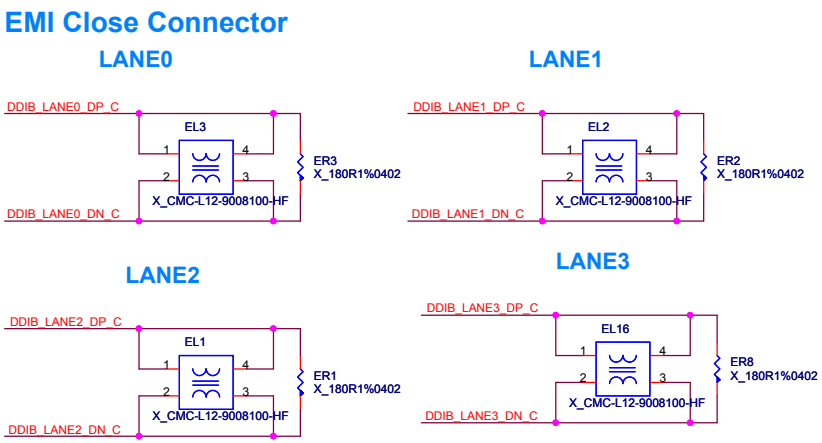


W>20mils

Display Port

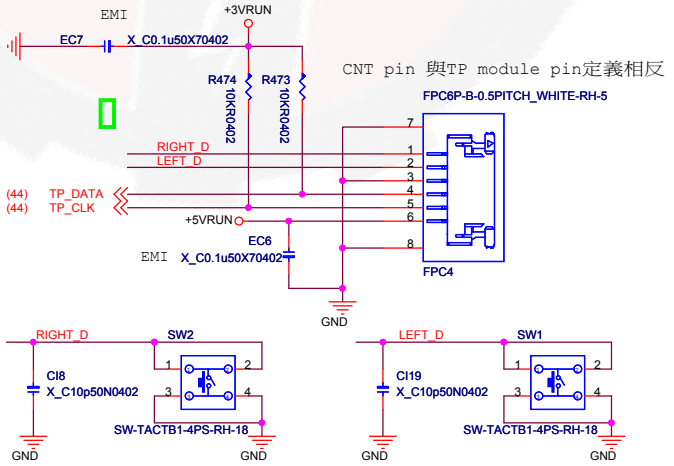


EMI Close Connector

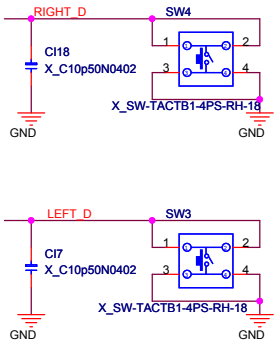


Touch Pad

16J1



1791



MICRO-STAR INT'L CO.,LTD.		
Title: DP / TP		
Size	Document Number: MS-16J1	Rev: 0A
Date: Tuesday, July 29, 2014	Sheet 47 of 70	

HDMI Level Shifter

HP_DET
PLUGGED 5V
UNPLUGGED 0V

HPD_SNK Internal PD 130kohm

V1.0 reserved for AOC TV issue.

R115 2.2KR1%0402

U23 SN75DP139RSBR

C647 C0.1u50X70402 TMDS_B_CLK#
C648 C0.1u50X70402 TMDS_B_CLK
C649 C0.1u50X70402 TMDS_B_D0#
C650 C0.1u50X70402 TMDS_B_D0
C651 C0.1u50X70402 TMDS_B_D1#
C652 C0.1u50X70402 TMDS_B_D1
C654 C0.1u50X70402 TMDS_B_D2#
C655 C0.1u50X70402 TMDS_B_D2

R359 10KR0402
R367 X_0R0402
QB1 N-2N7002_SOT23

X_0402 JNC18
R385 X_100KR0402
R380 4.7KR0402
R381 4.02KR1%0402
R382 2.2KR1%0402
R383 2.2KR1%0402

HDMI Connector

HDMI1 HDMI19PM_BLACK-HF-7

D2 S-BAT54ALT1G_SOT23
R120 2.2KR1%0402
R100 2.2KR1%0402
W>20mils
PF1 F-0805L075WR
R101 X_100KR0402
C639 C0.1u50X70402
D3 BAV99LT1_SOT23

EMI Close Connector

TX0 EL13 ER5 X_180R1%0402 X_CMC-L12-9008100-HF
TX1 EL14 ER6 X_180R1%0402 X_CMC-L12-9008100-HF
TX2 EL15 ER7 X_180R1%0402 X_CMC-L12-9008100-HF
CLK EL12 ER4 X_180R1%0402 X_CMC-L12-9008100-HF

Place Under DUT

C349 C0.1u50X70402
C344 C0.01u50X0402
C351 C1u25X0402
C343 C1u25X0402
C346 C0.1u50X70402
C352 C0.01u50X0402
C348 C1u25X0402
C347 C1u25X0402

OVS R360 X_4.7KR0402 +3VRUN
R369 0R0402 GND

DDC I2C buffer offset select
H:Offset 1
L:Offset 2
Hi-Z:Offset 3

SRC R384 X_4.7KR0402 +3VRUN
R379 X_0R0402 GND

TMDS outputs rise and fall time select
H:Edge Rate:Slowest SRC =High adds ~60ps
L:Edge Rate: Slow SRC =Low adds ~30ps
Hi-Z:Edge Rate VCC/2

HPDINV R366 4.7KR0402 GND
DDC_EN R363 4.7KR0402 +3VRUN

HPD_SOURCE Logic and Level Select
H:HPD Inversion HPD_SOURCE VOH =0.9V
L:HPD non-inversion HPD_SOURCE VOH =3.2V

OE_N

Output Enable and power saving function for High Speed Differential level shifter path.
H: Power Saving OUT_Dx outputs = high impedance
L: Normal Mode OUT_Dx outputs = active

Enables or Disables the DDC I2C buffer
H:DDC Buffer enabled
L:DDC Buffer disabled

MICRO-STAR INT'L CO.,LTD.

Title: HDMI DP139
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Audio CODEC/Audio AMP

0B CHANG FOOTPRINT AND PART REF

EMI(RADIATION SOLUTION)

DVDD

Close Codec

Close Pin25

Close Pin38

AVDD5V

U33

ALC892-CG

B05-LC89214-R09

SPK 2031

SPK 2051

HP

MIC

SUBWOOFER

ALC892 Codec Spec max=1.2Vrms
After SBC the codec output Vpp is 1.38V ,0.488Vrms

U35(APA2051) Pin23: gain set
5.1V*39K/(18K+39K)=3.489V
10dB = 3.48V(R469:18K, R466:39K)
dB=20LOG(Vo/Vi)
喇叭spec = 2W/4Ohm
10dB =20LOG 3.16, Vout = 0.488Vrms *3.16 =1.54Vrms

Po=(1.54*1.54)/4=0.59W

EMI Close Codec

Internal Mic

AMP

10DB/0.59W

U12

APA2051QBI-TRG_TQFN28

I71-020510C-A30

Internal Speaker Conn

APA2031輸出與2051相位相反

	CODEC	喇叭
L	-	-
L	+	+
R	+	+
R	-	-
L2	-	+
L2	+	-
R2	+	-
R2	-	+

WIDTH > 40 mils

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

U13

APA2031RI-TRL_TSSOP20-RH

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

Size: | Document Number: MS-16J1 | Rev: 0A

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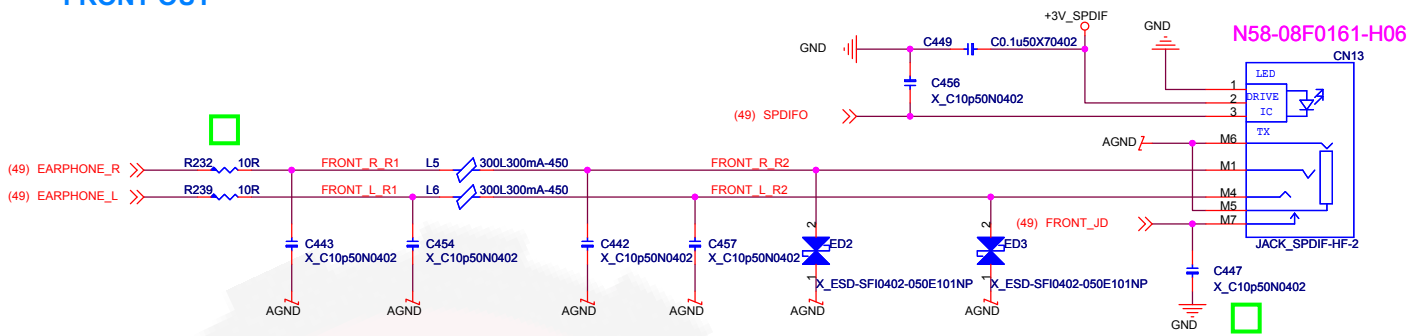
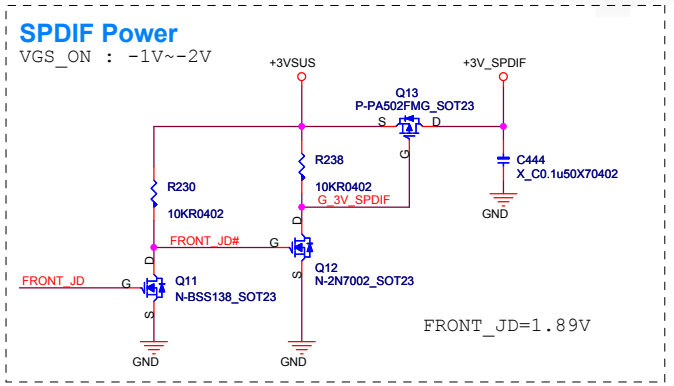
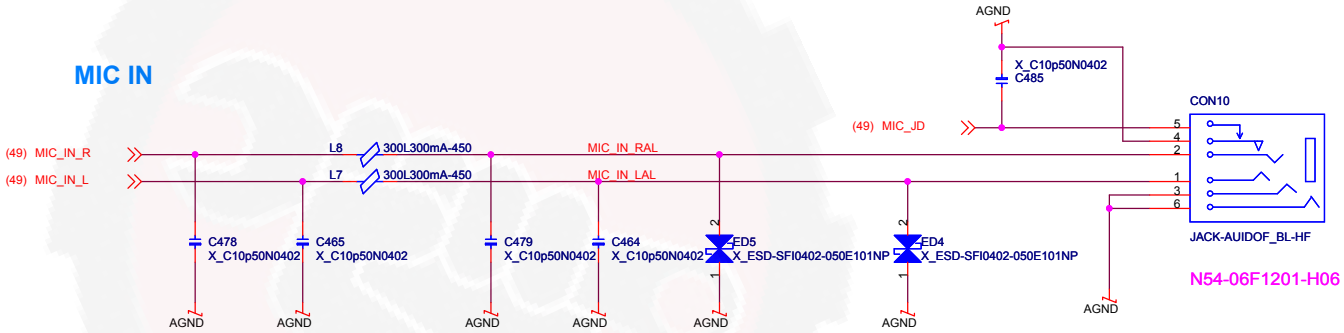
Audio CONN /Woffer

FRONT OUT





MIC IN

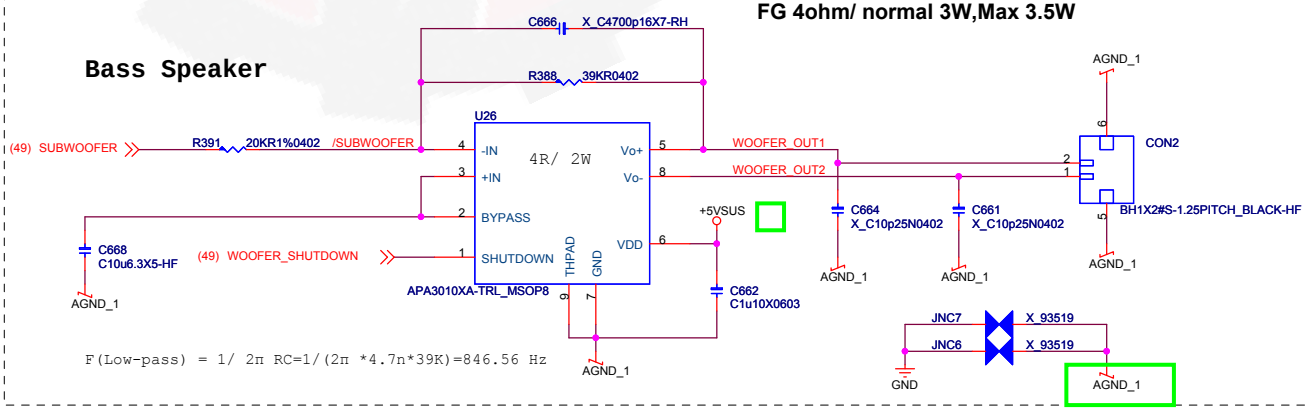


ALC892 SPC MAX 為 1.2Vrms
gain= -2*(R370/R371)= -2*(40K/20K) = -4

Vout= 0.58Vrms *4 = 2.32Vrms , Po=(2.32*2.32)/3.8=1.42W

Woofer SPEC
YG 3.8ohm / normal 3W,Max 3.5W
FG 4ohm/ normal 3W,Max 3.5W

Bass Speaker



msi MICRO-STAR INT'L CO.,LTD.		
Title: Audio / Woffer		
Size	Document Number: MS-16J1	Rev: 0A
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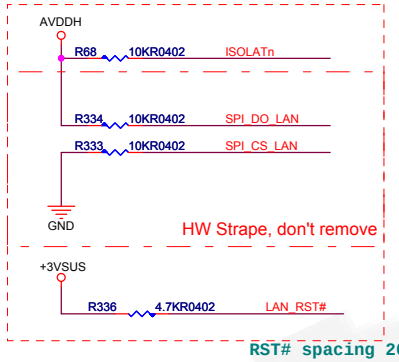
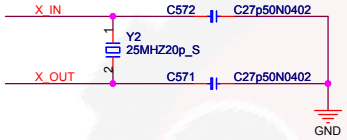
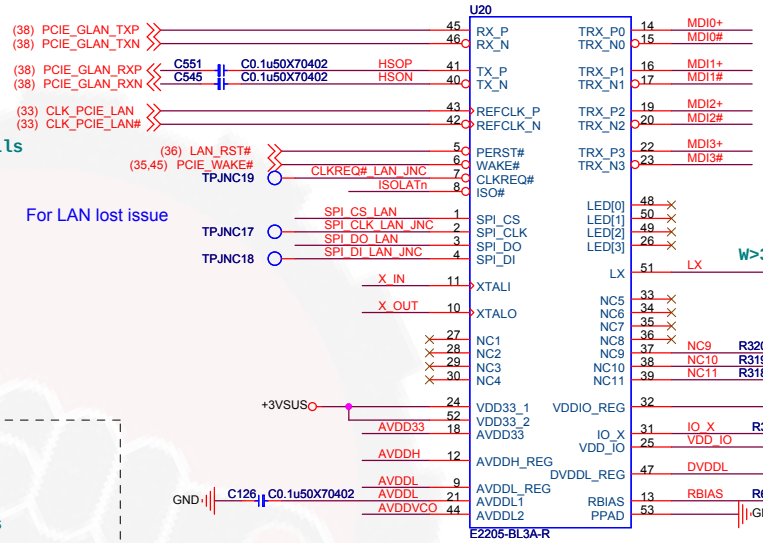
GIGA LAN(BigFoot BFN2205B)



RST# spacing 20mils

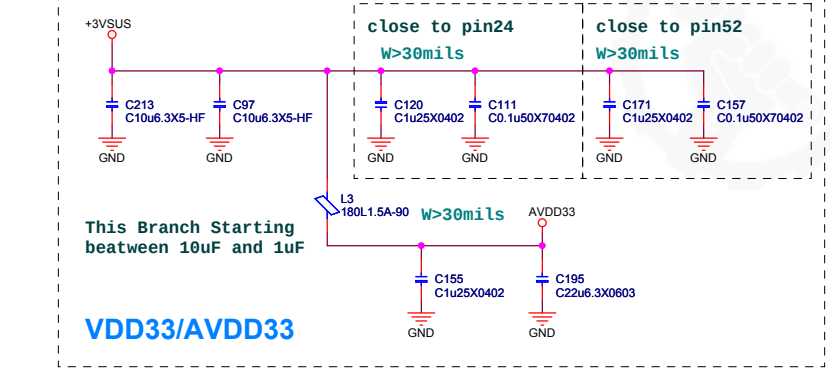


For LAN lost issue

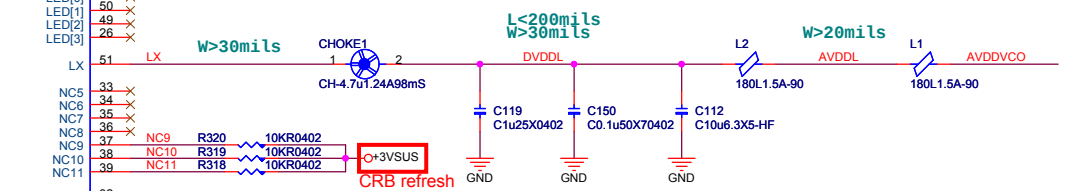


B06-E22050C-Q24

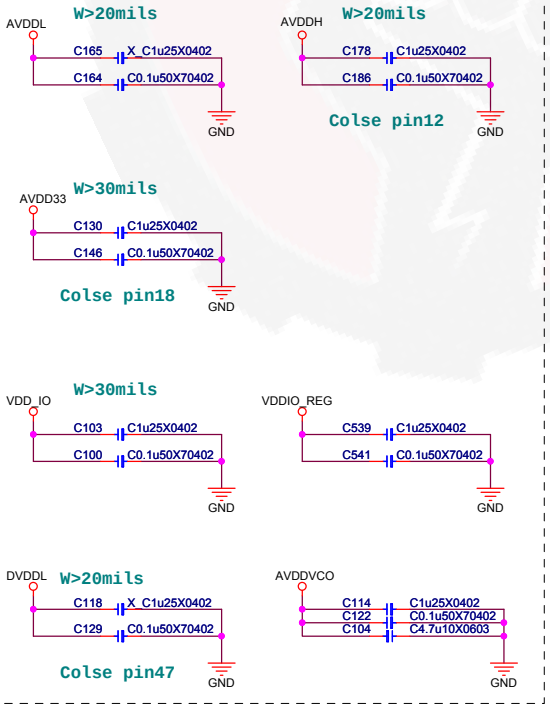
MAC 燒 CHIP 內
,有次數限制

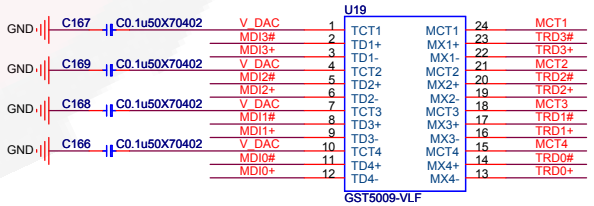


VDD33/AVDD33

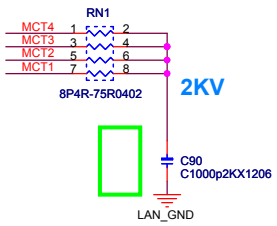


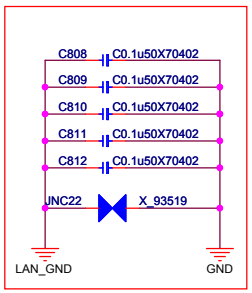
Power CAP

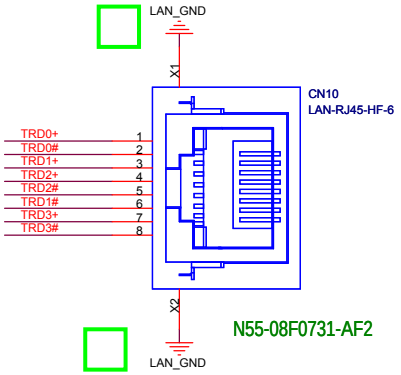




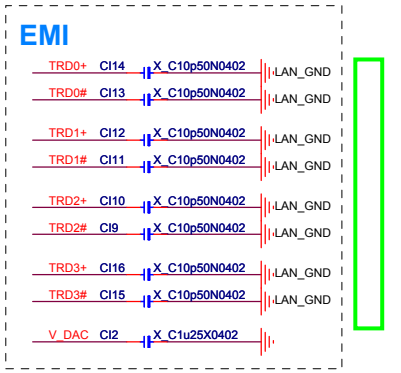
L05-0200150-B09







N55-08F0731-AF2



MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(BigFoot BFN2205B)

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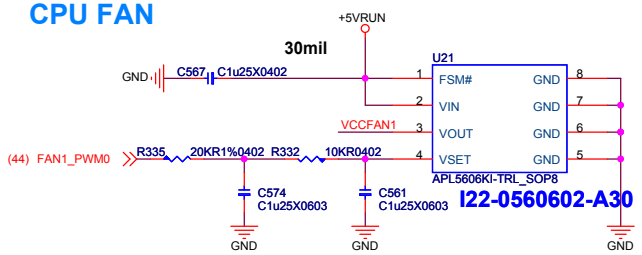
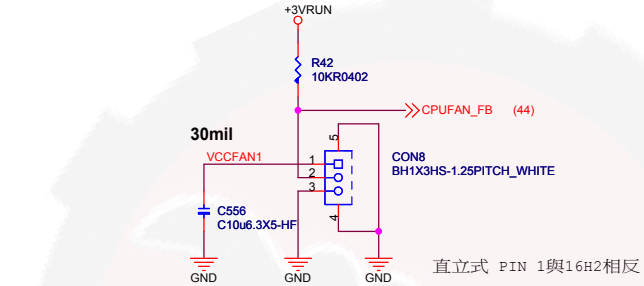
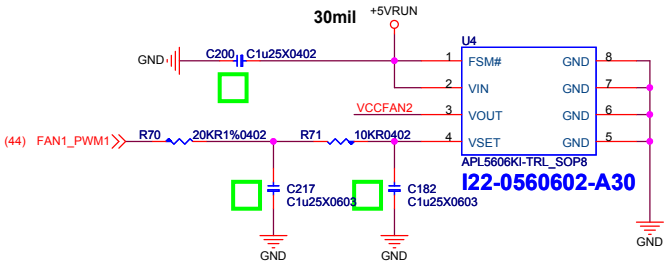
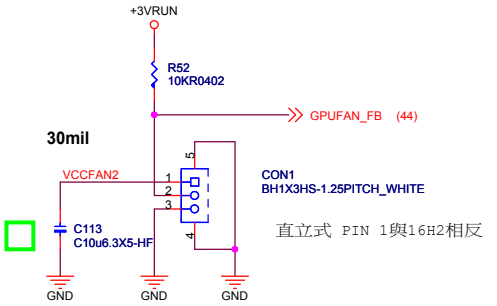
CPU FAN



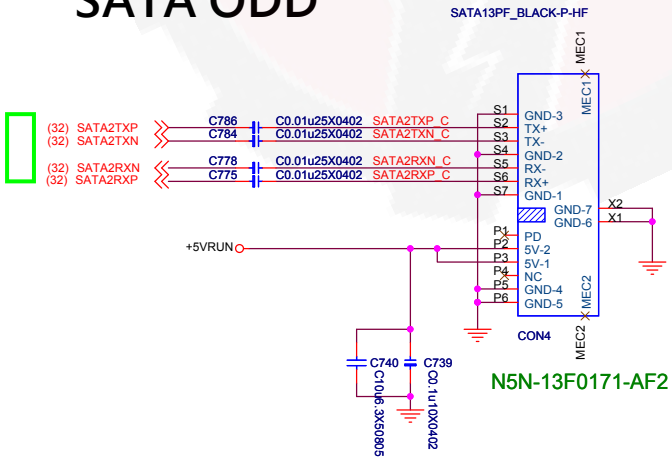


DGPU FAN

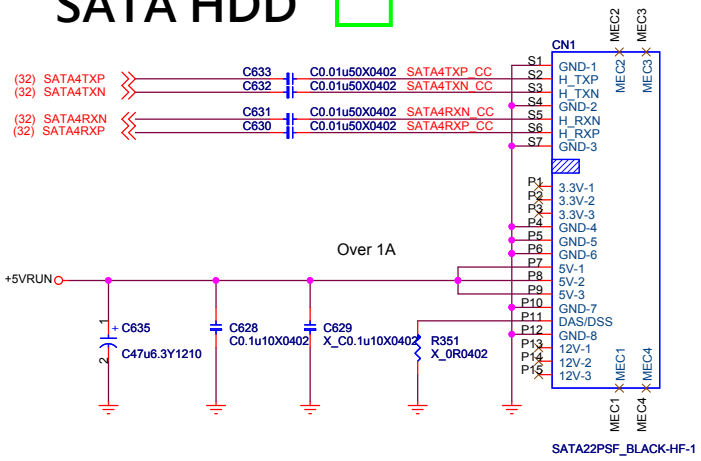




SATA ODD

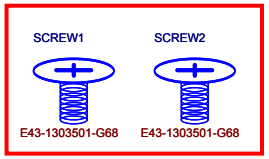


SATA HDD



22.GND
21.TX
20.TX#
19.GND
18.RX#
17.RX
16.GND

15.V33
14.V33
13.V33
12.GND
11.GND
10.GND
9.V5
8.V5
7.V5
6.GND
5.Reserved
4.GND
3.V12
2.V12
1.V12



0B ADD SPONGE CHECK

Title	ODD/HDD/FAN	
Size A3	Document Number MS-16J1	Rev 0A
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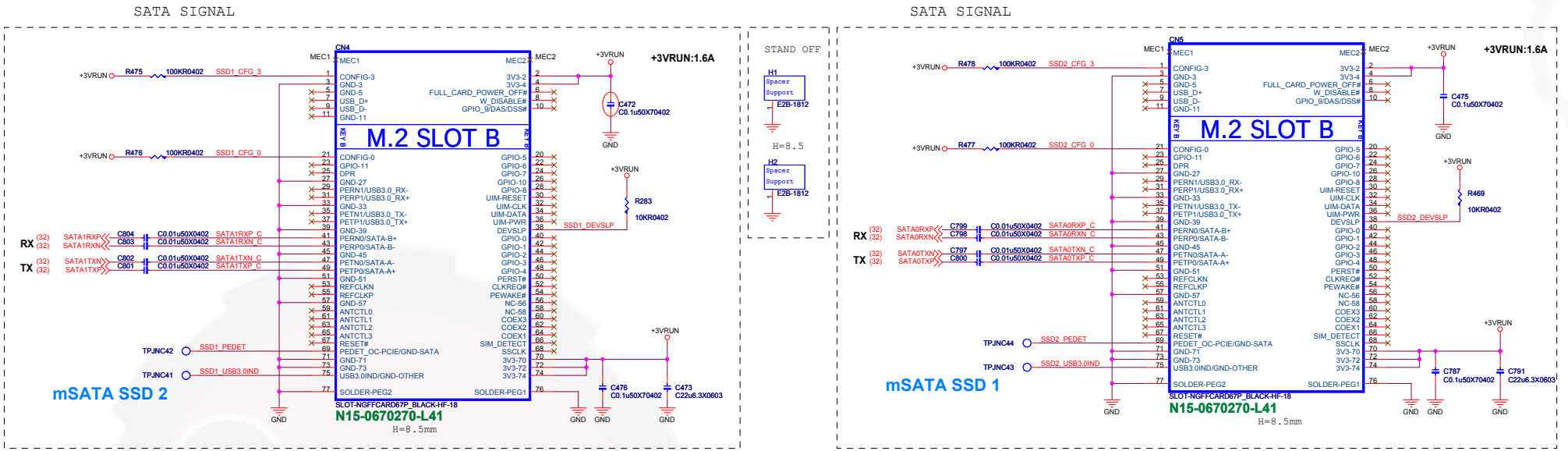
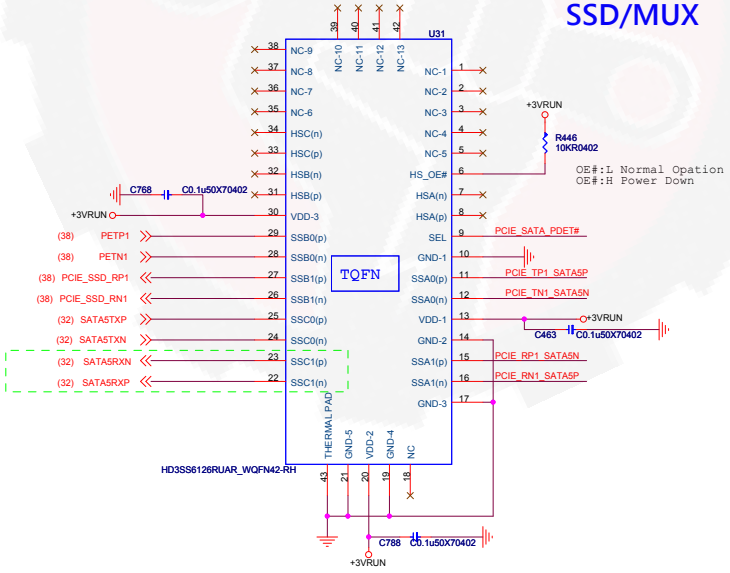
SSD

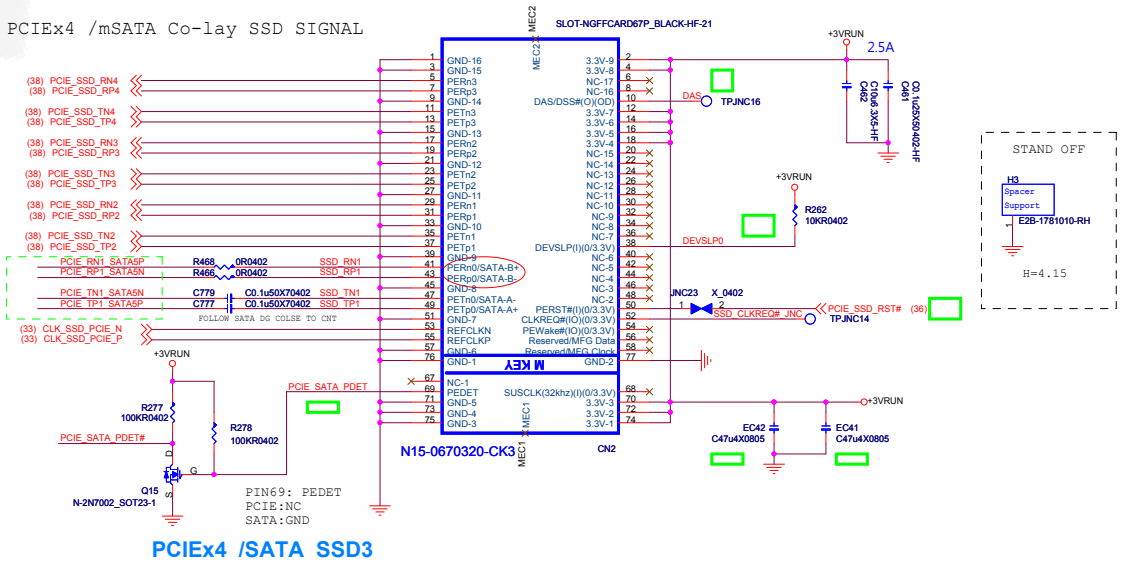


SSD/MUX



TRUTH TABLE USB 3.0 SuperSpeed USB

SEL	USB 3.0 Port Selection		
	SSA0/1	SSB0/1	SSC0/1
0	To/From SSB0/1	To/From SSA0/1	Off
1	To/From SSC0/1	Off	To/From SSA0/1



MSI	MICRO-STAR INT'L CO.,LTD.
Title	SSD/MUX
Size	Document Number: MS-16J1
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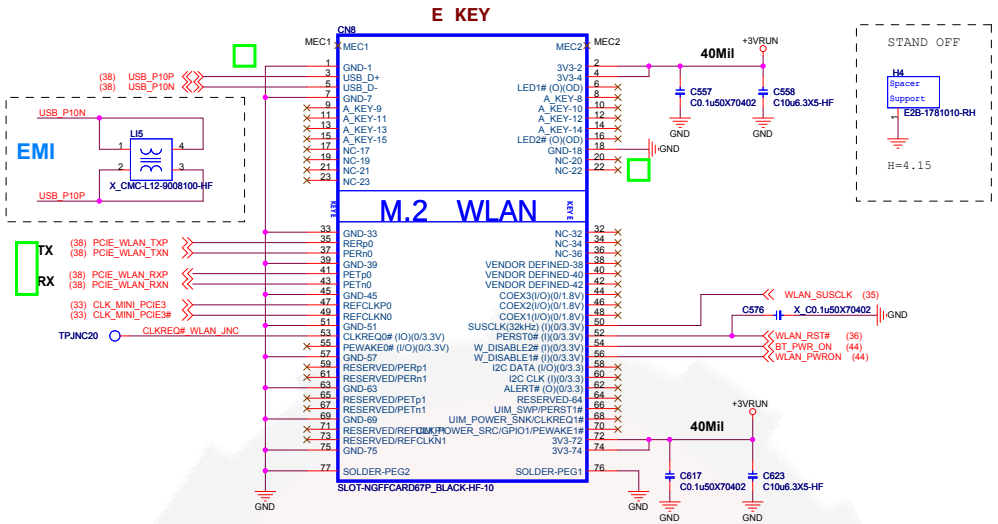
WLAN

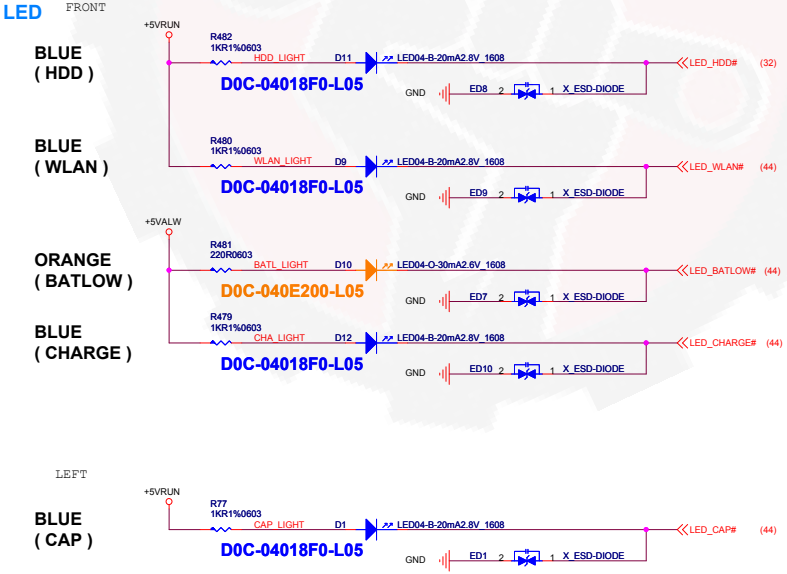
WLAN/LED

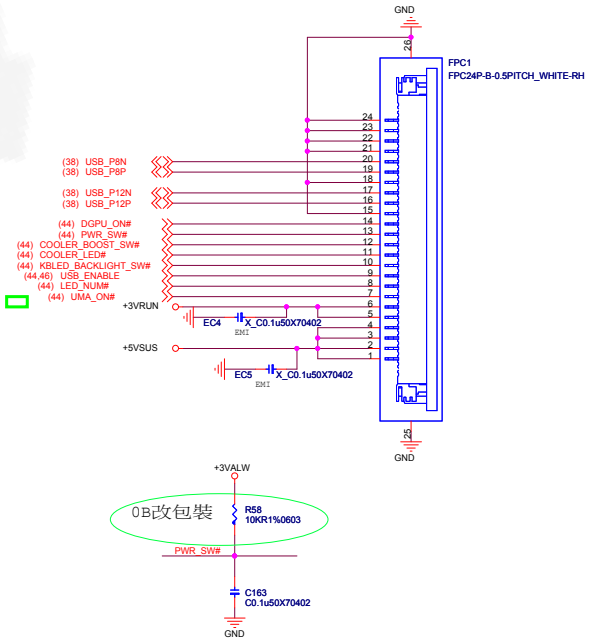


Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN(W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

16J1

LED





Title	WLAN /LED		
Size	Document Number		Rev
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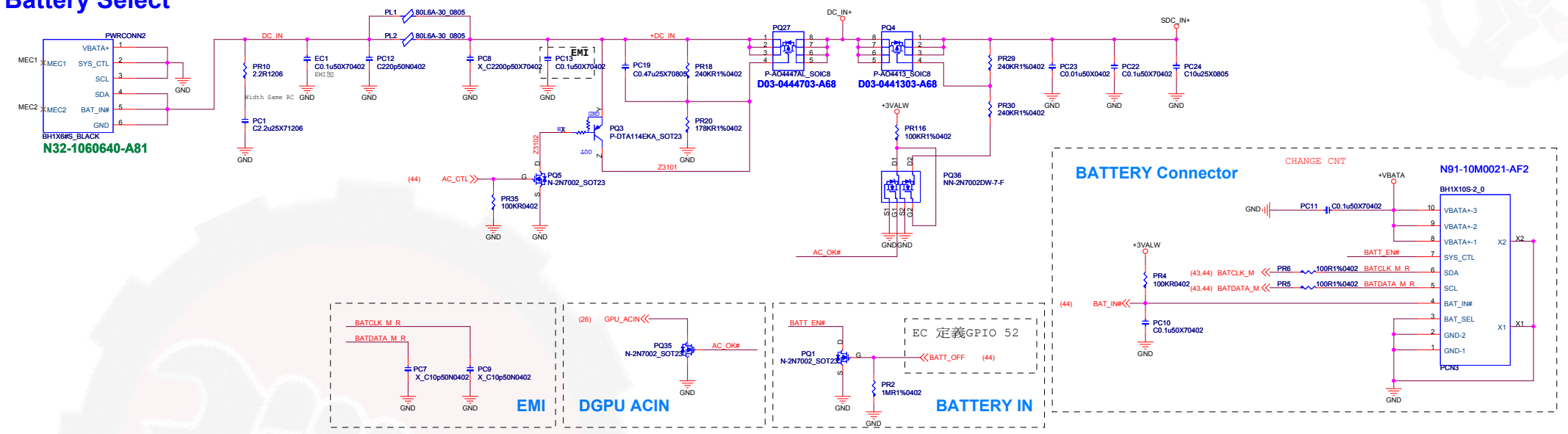
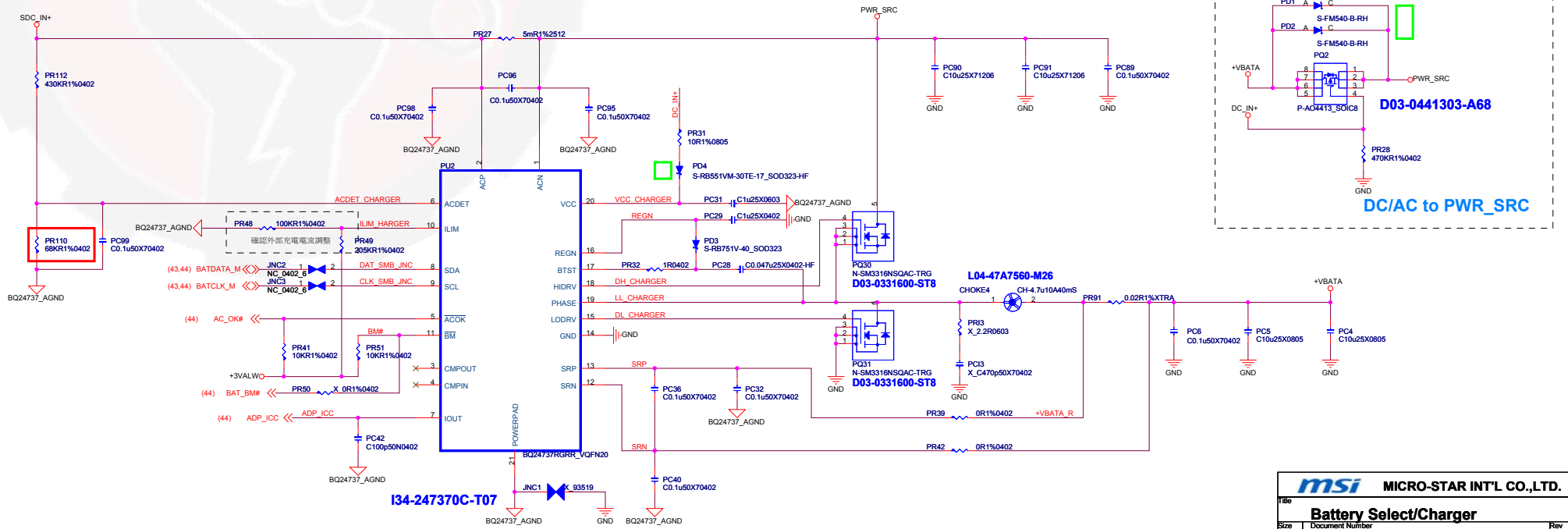
MICRO-STAR INT'L CO.,LTD.

Battery Select/Charger

Battery Select

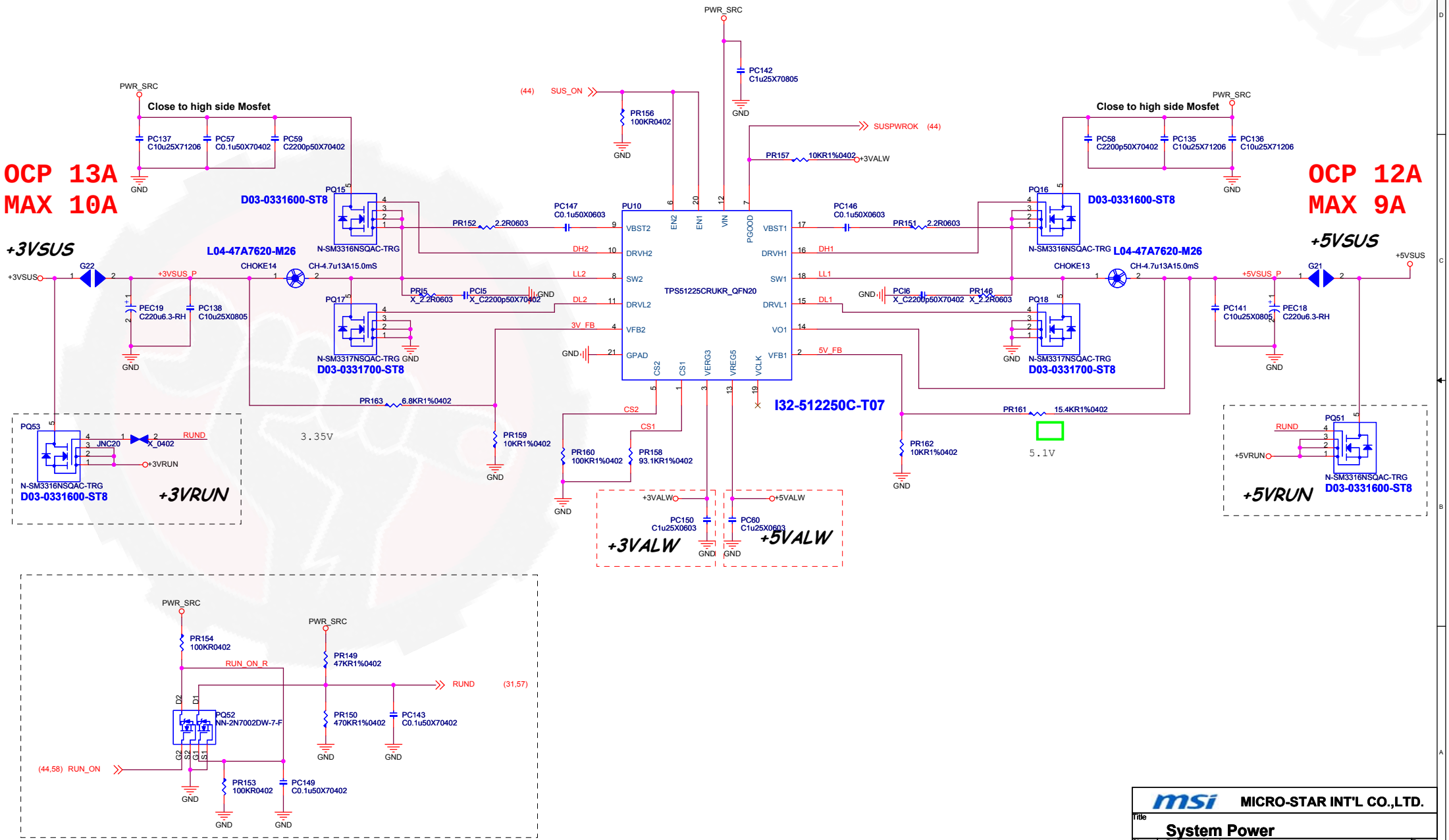


Battery Charger



msi MICRO-STAR INT'L CO.,LTD.			
Title: Battery Select/Charger			
Size	Document Number: MS-16H2		Rev: 0A
Date: Tuesday, July 29, 2014	Sheet 55 of 70		

System Power



MICRO-STAR INT'L CO.,LTD.	
Title	System Power
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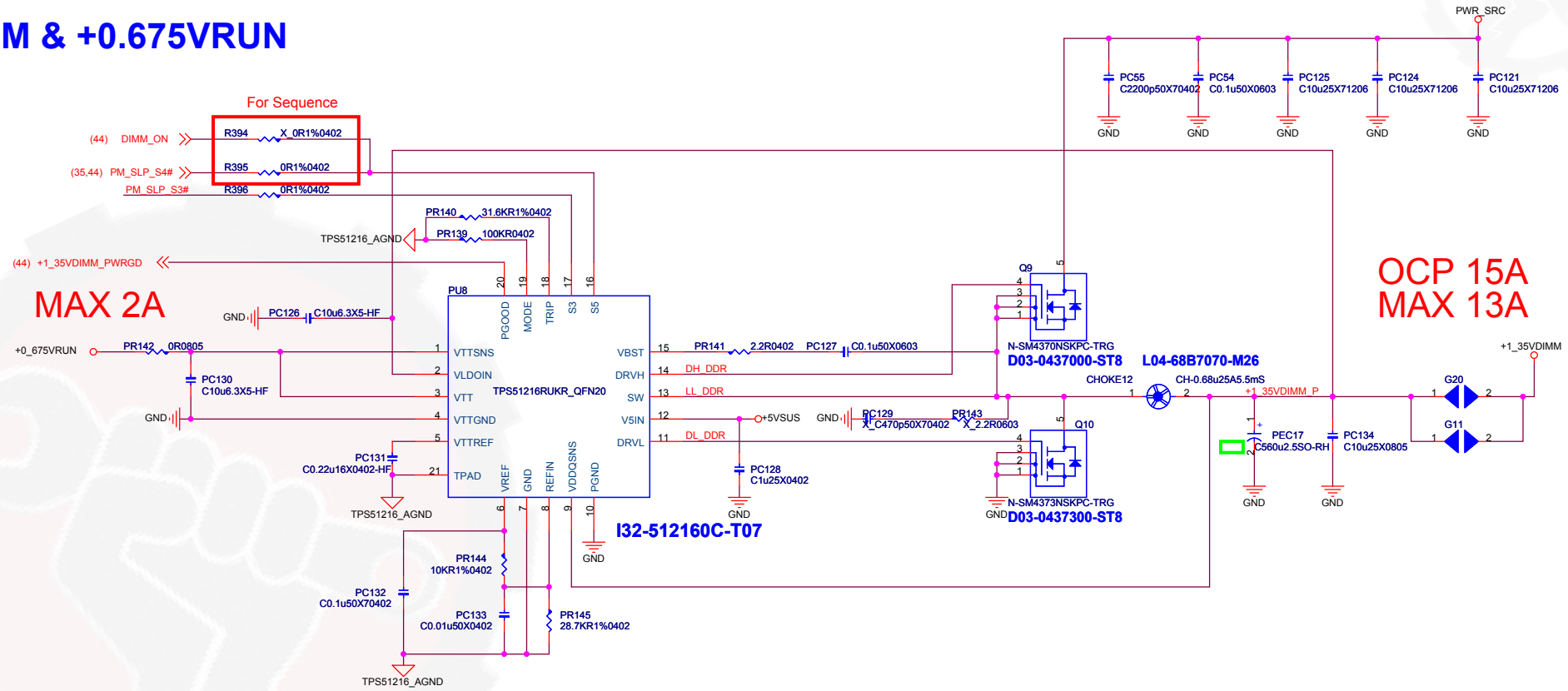
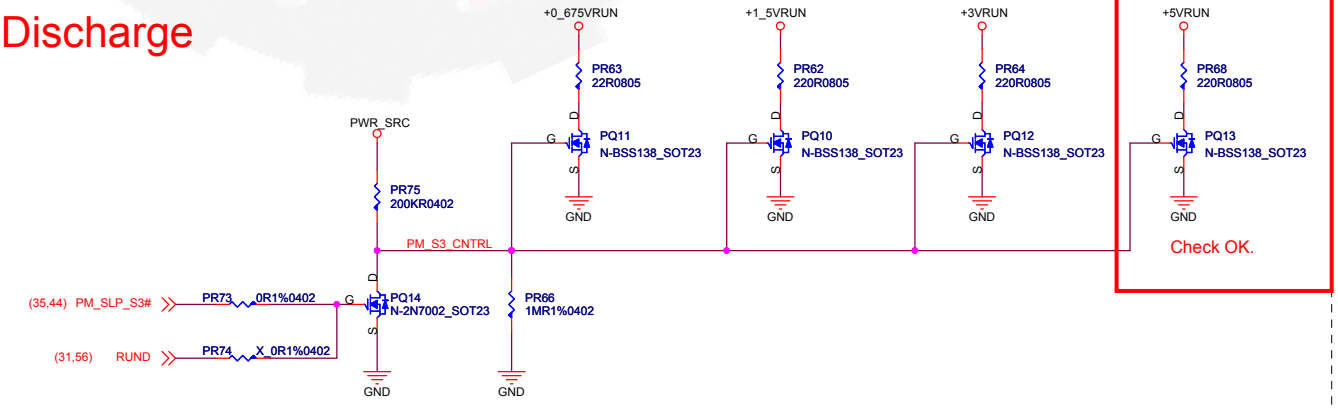
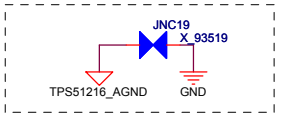
+1.35VDIMM/+0.675VRUN

+1.35VDIMM & +0.675VRUN



Discharge





MICRO-STAR INT'L CO.,LTD.		
Title: +1.35VDIMM/+0.675VRUN		
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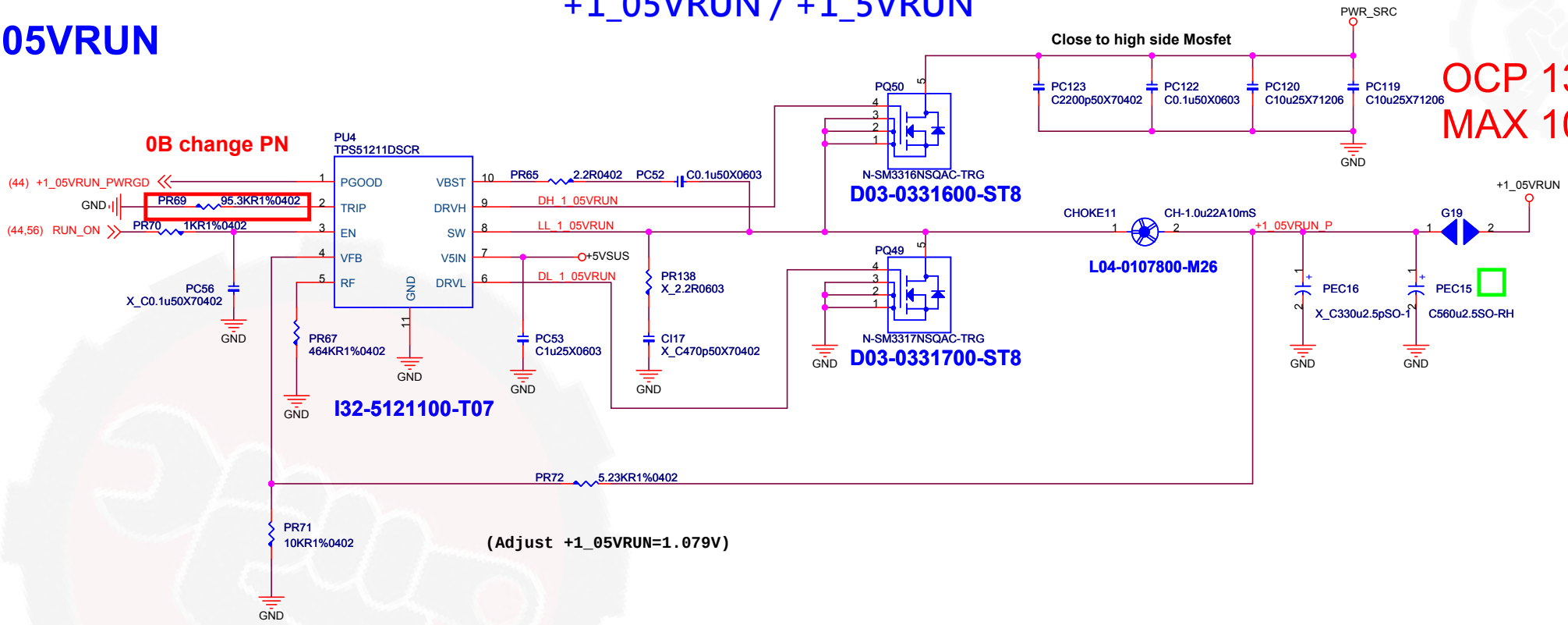
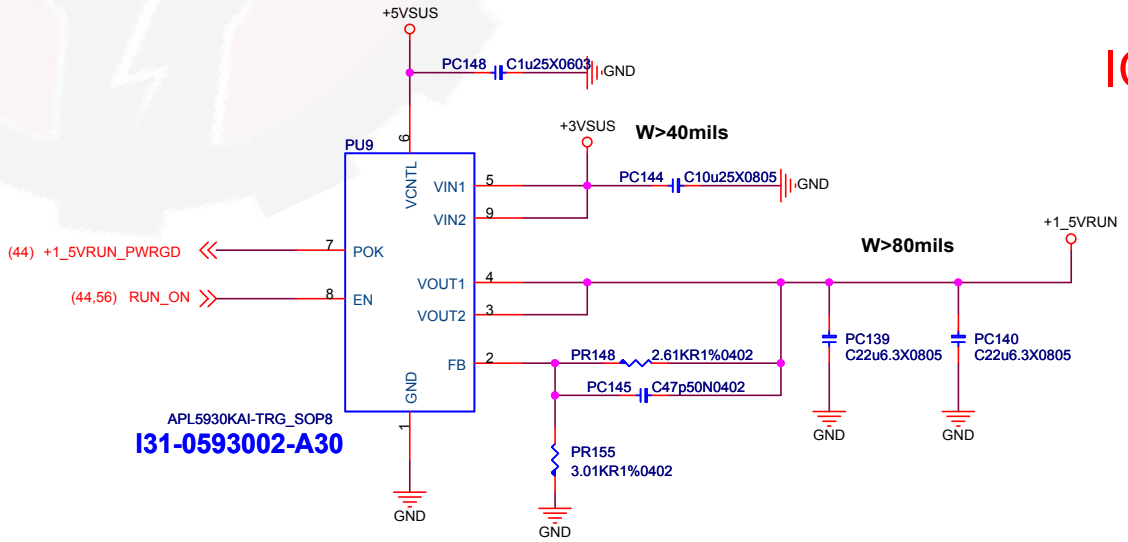
+1_05VRUN / +1_5VRUN

+1.05VRUN



+1.5VRUN



IC MAX 3A
253mA

MICRO-STAR INT'L CO.,LTD.		
Title: +1_05VRUN / +1_5VRUN		
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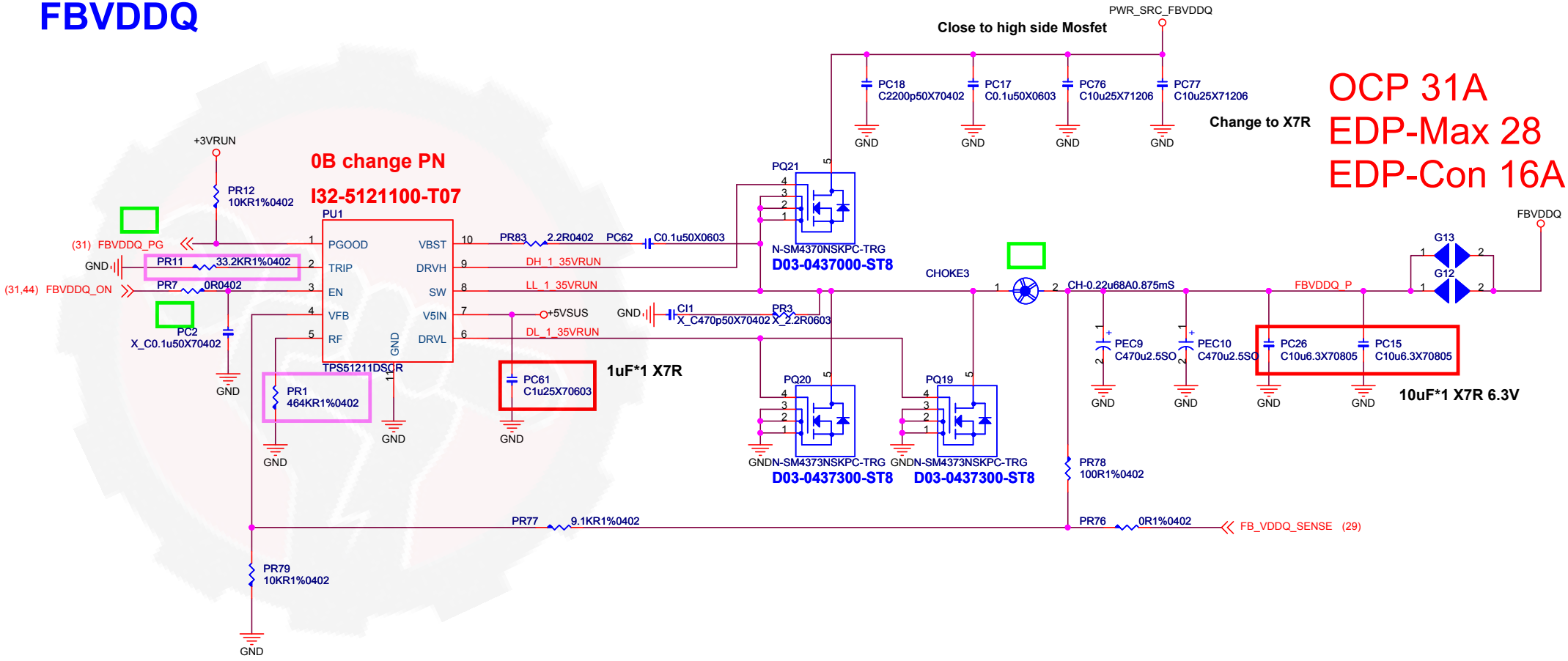
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.		
Title: DGPU POWER FBVDDQ		
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DGPU POWER / UP1642PQAG

EDP-Peak 130A

EDP-MAX 75A

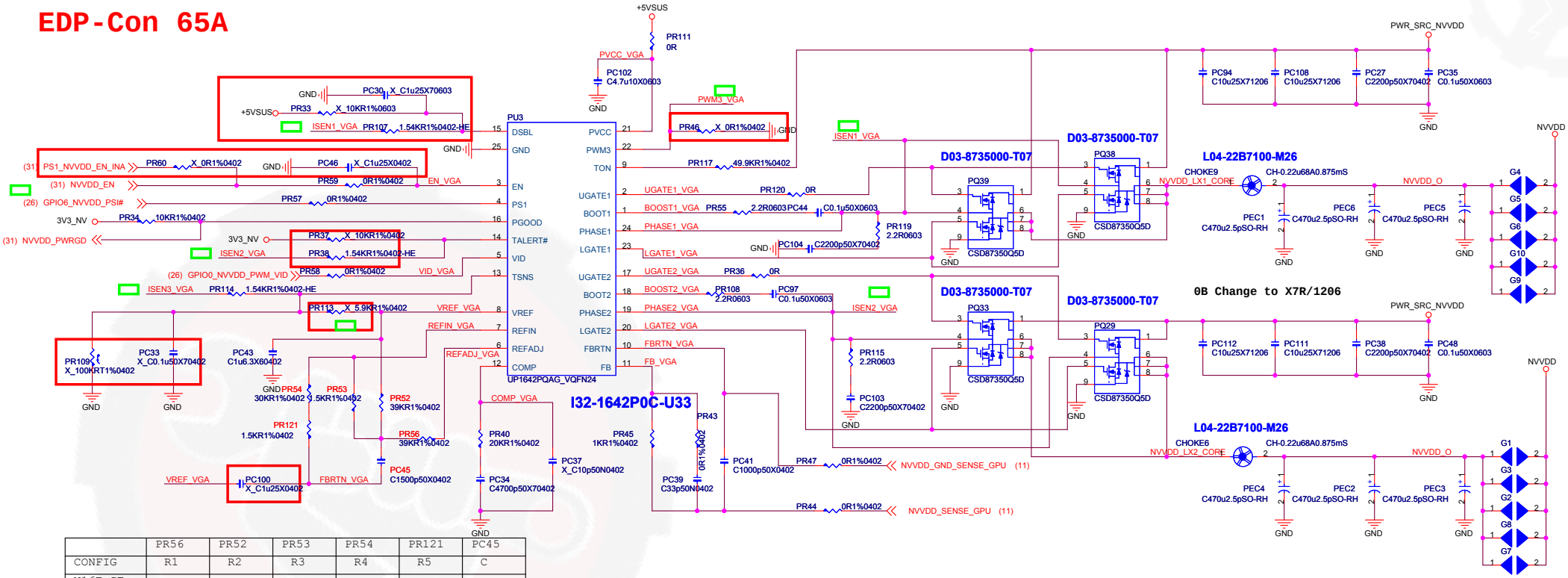
EDP-Con 65A

DGPU POWER NVVDD

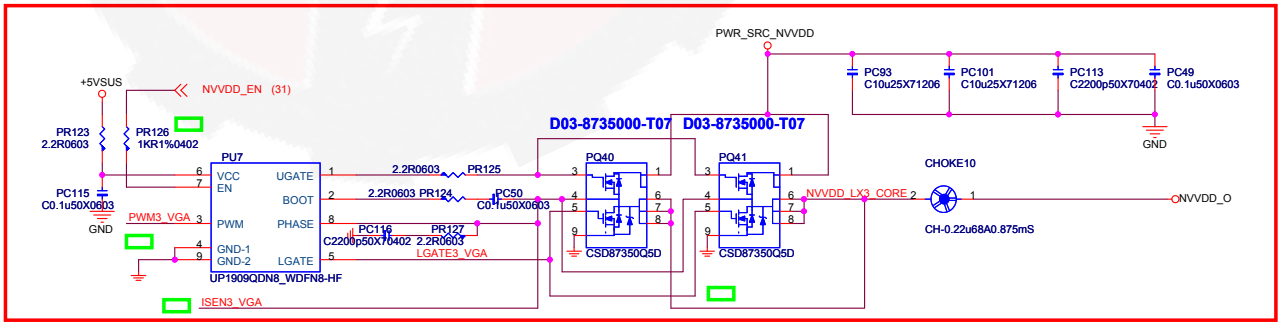
CONFIG A

VBoot:0.875V

Vmin:0.6V / Vmax:1.2V



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT N16P-GX-B	39K	39K	1.5K	30K	1.5K	1.5nF



Title	DGPU POWER NVVDD
Size	
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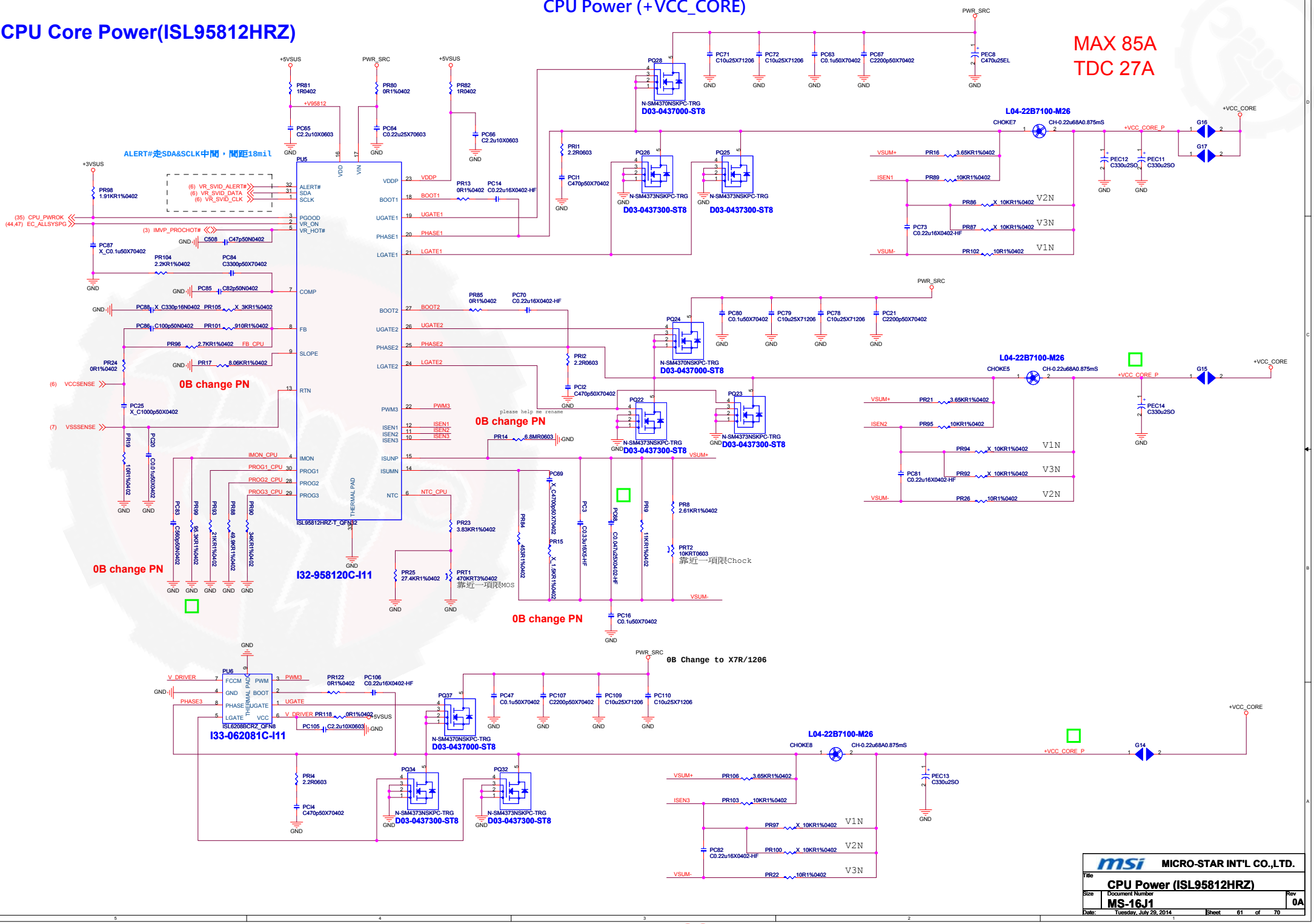
MICRO-STAR INT'L CO.,LTD.

CPU Core Power(ISL95812HRZ)

CPU Power (+VCC_CORE)

MAX 85A
TDC 27A



MSI	MICRO-STAR INT'L CO.,LTD.
Title	CPU Power (ISL95812HRZ)
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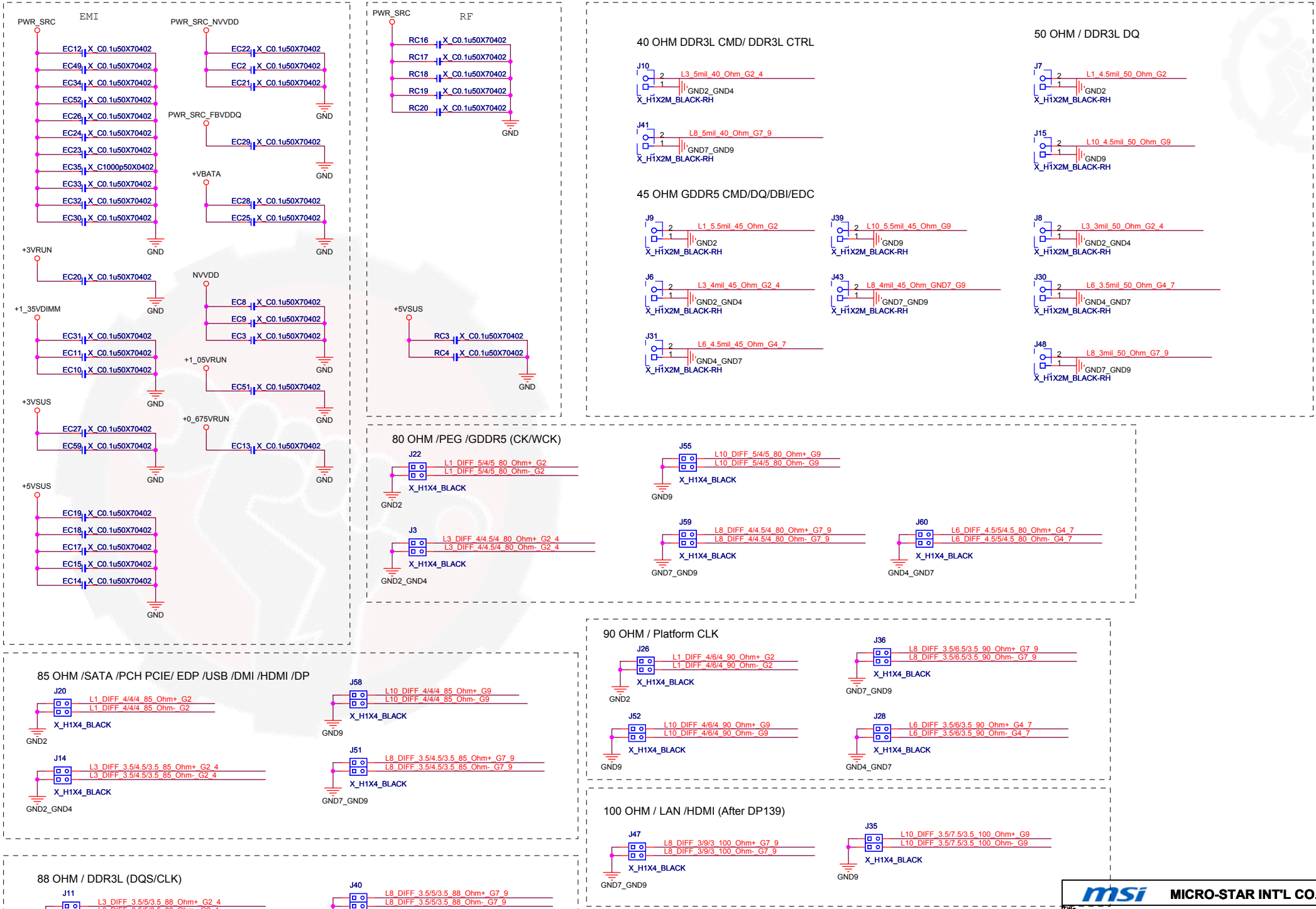

MICRO-STAR INT'L CO.,LTD.

Title: EMI/ Impedence

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CPU/GPU Holes

MCPU4 H_R200D150 — GND X_CPU_HOLE
MCPU2 H_R200D150 — GND X_CPU_HOLE
MCPU3 H_R200D150 — GND X_CPU_HOLE
MCPU1 H_R200D150 — GND X_CPU_HOLE
MGPU2 H_R276D169_PB — GND X_CPU_HOLE
MGPU4 H_R276D169_PB — GND X_CPU_HOLE
MGPU1 H_R276D169_PB — GND X_CPU_HOLE
MGPU3 H_R276D169_PB — GND X_CPU_HOLE

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8 — X_FM
FM9 FM10 FM11 FM12 FM13 FM14 FM15 FM16 — X_FM
FM17 FM18 FM19 FM20 FM21 FM22 FM23 FM24 — X_FM

OD 2.3

MH6 H_R197D91 X_ME_ SCREW HOLE
MH3 H_R197D91 X_ME_ SCREW HOLE
MH7 H_R197D91 X_ME_ SCREW HOLE — AGND
MH5 H_R197D91 X_ME_ SCREW HOLE
MH4 H_R197D91 X_ME_ SCREW HOLE

UME3 CPU BKT — CPU BKT E2M-6H20211-C22
UME4 GPU BKT — GPU BKT E2M-6H20311-C22

UME1 HDMI Lable — HDMI ROYALTY Y01-RHDMI03-000
UME2 BIOS Lable — X_BIOS_LABEL G51-LA01678-A09
For MP

PCB1 P30-16J110A-H73
P30-16J110A-H73
Hannstar: P30-16J110A-H73
TRIPOD: P30-16J110A-T53

版邊 內3 / 外8

MH1 H_R197D118_PT X_ME_ SCREW HOLE

HOLES_8X8_D3MM_VIA8 MH8 X_8x8

HOLE3 NPTH_80 X_NPTH_80
HOLE4 NPTH_80 X_NPTH_80
HOLE2 H_NR118D118_1 X_H_NR118D118_1
HOLE1 H_NR118D118_1 X_H_NR118D118_1
HOLE12 npth_98 X_npth_98
HOLE13 npth_98 X_npth_98
HOLE14 npth_98 X_npth_98
HOLE15 npth_98 X_npth_98

MH9 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — GND
MH2 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — LAN_GND

HOLE5 X_NPTH_80 NPTH_80
HOLE6 X_NPTH_80 NPTH_80
HOLE7 X_NPTH_80 NPTH_80
HOLE8 X_NPTH_80 NPTH_80
HOLE9 X_NPTH_80 NPTH_80
HOLE10 X_NPTH_80 NPTH_80
HOLE11 X_NPTH_80 NPTH_80

MICRO-STAR INT'L CO.,LTD.
Title: Screw/ME
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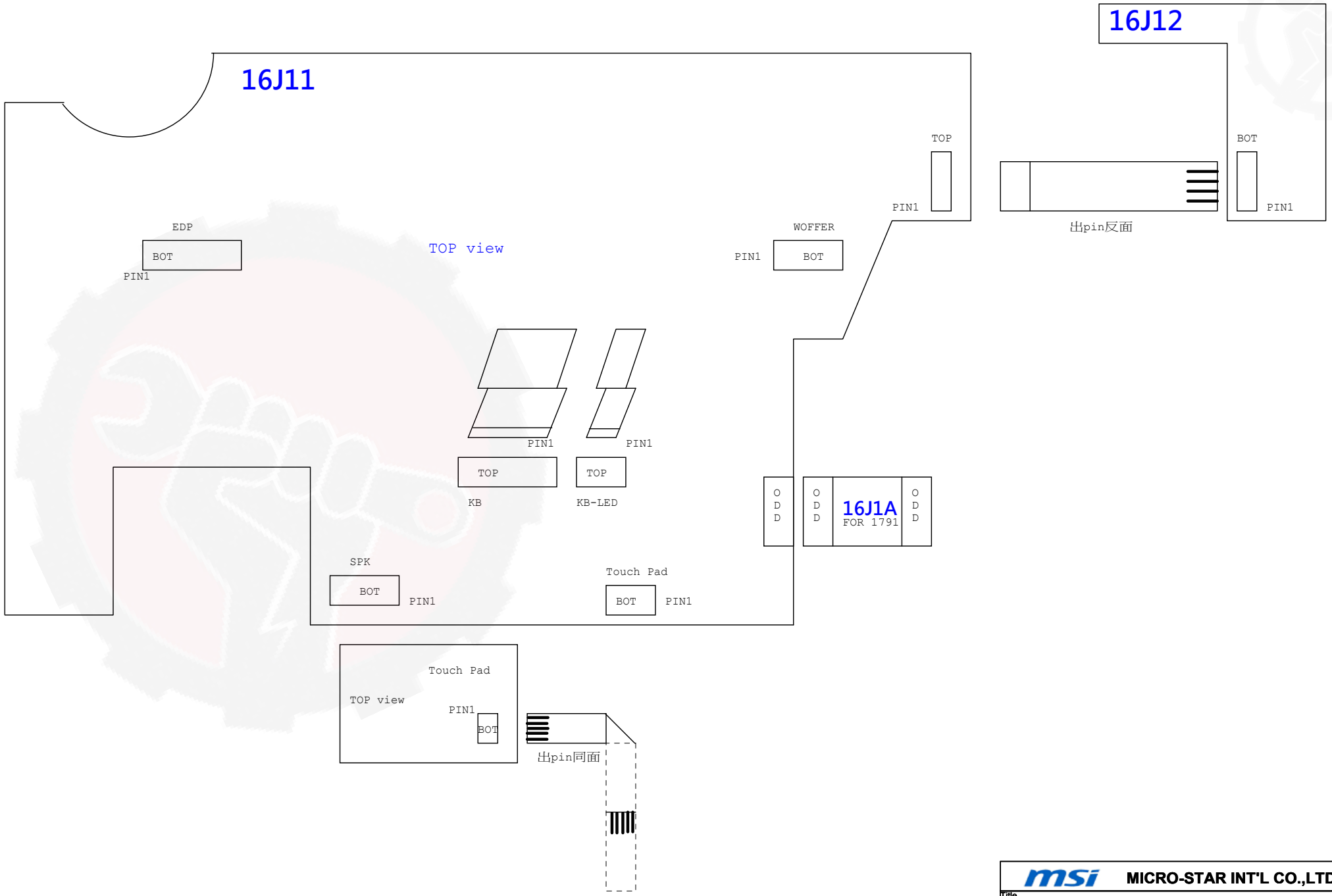

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Title: VIEW		
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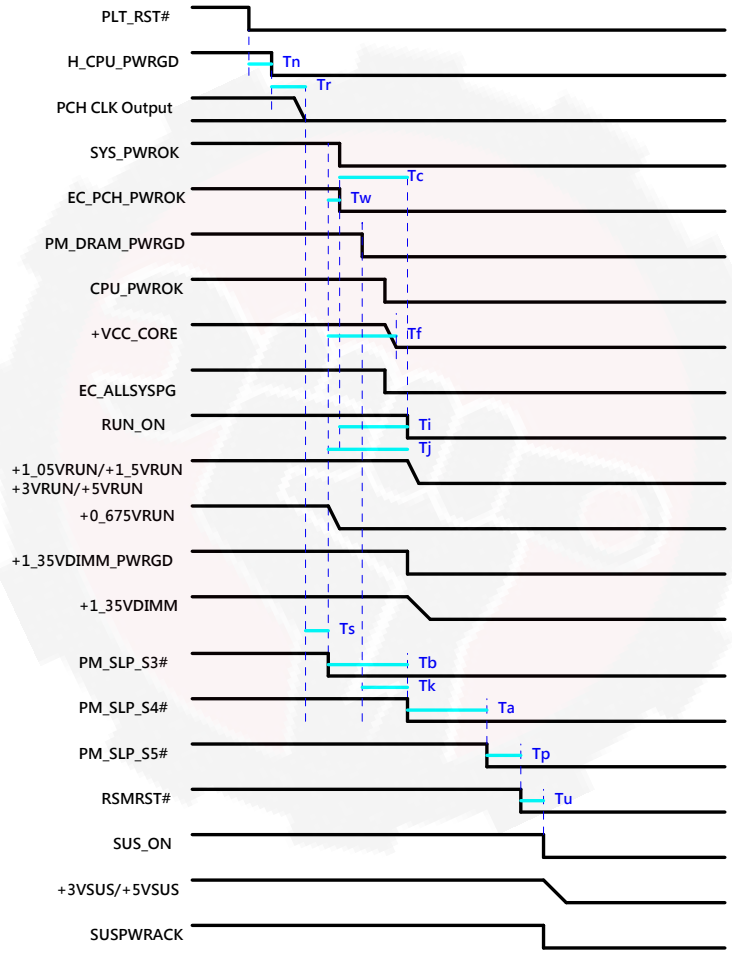
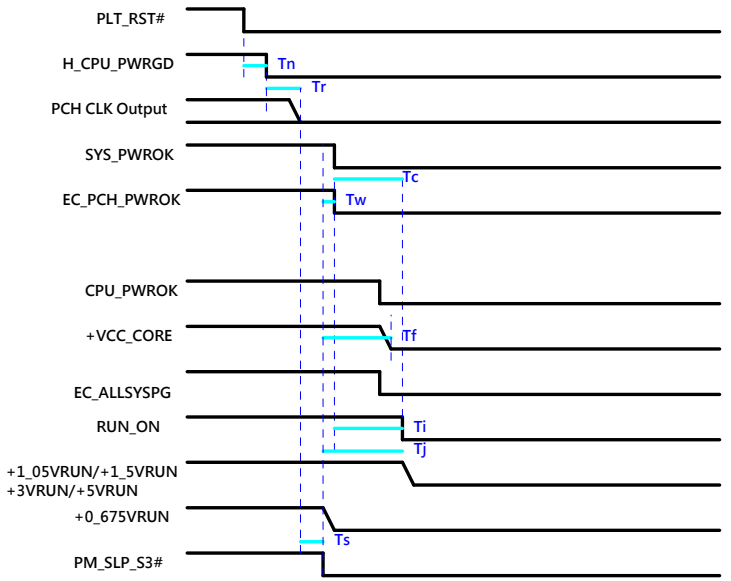
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
Ta	30		us	SLP_S4# assertion to SLP_S5# assertion.
Tb	30		us	SLP_S3# assertion to SLP_S4# assertion.
Tc	40		ns	APWROK de-assertion to VCCASW/VCCSPI rails falling.
Tf		500	ms	SLP_S3# assertion to VCCIN(CPU) rail completely off.
Ti	40		ns	PWROK de-assertion to VCCCore (PCH) rail falling (-5% of nominal value).
Tj	5		us	SLP_S3# assertion to VCCCore (PCH) rails falling (-5% of nominal value).
Tk	-100		ns	DRAMPWROK de-assertion to SLP_S4# assertion
Tn	30		us	PLTRST# assertion to CPUPWRGOOD de-assertion.
Tp	500		us	Last SLP_Sx# or SLP_A# assertion to RSMRST# assertion
Tr	10		us	CPUPWRGOOD de-assertion to PCH clock outputs turning off.
Ts	1		us	PCH Clock outputs turning OFF to SLP_S3# assertion.
Tu	40		ns	RSMRST# assertion to VCCSUS rails falling (-5% of nominal value).
Tw	0		ms	SLP_S3# assertion to PWROK de-assertion.

S0 -> S3



MICRO-STAR INT'L CO.,LTD.

Title: Power down Sequence

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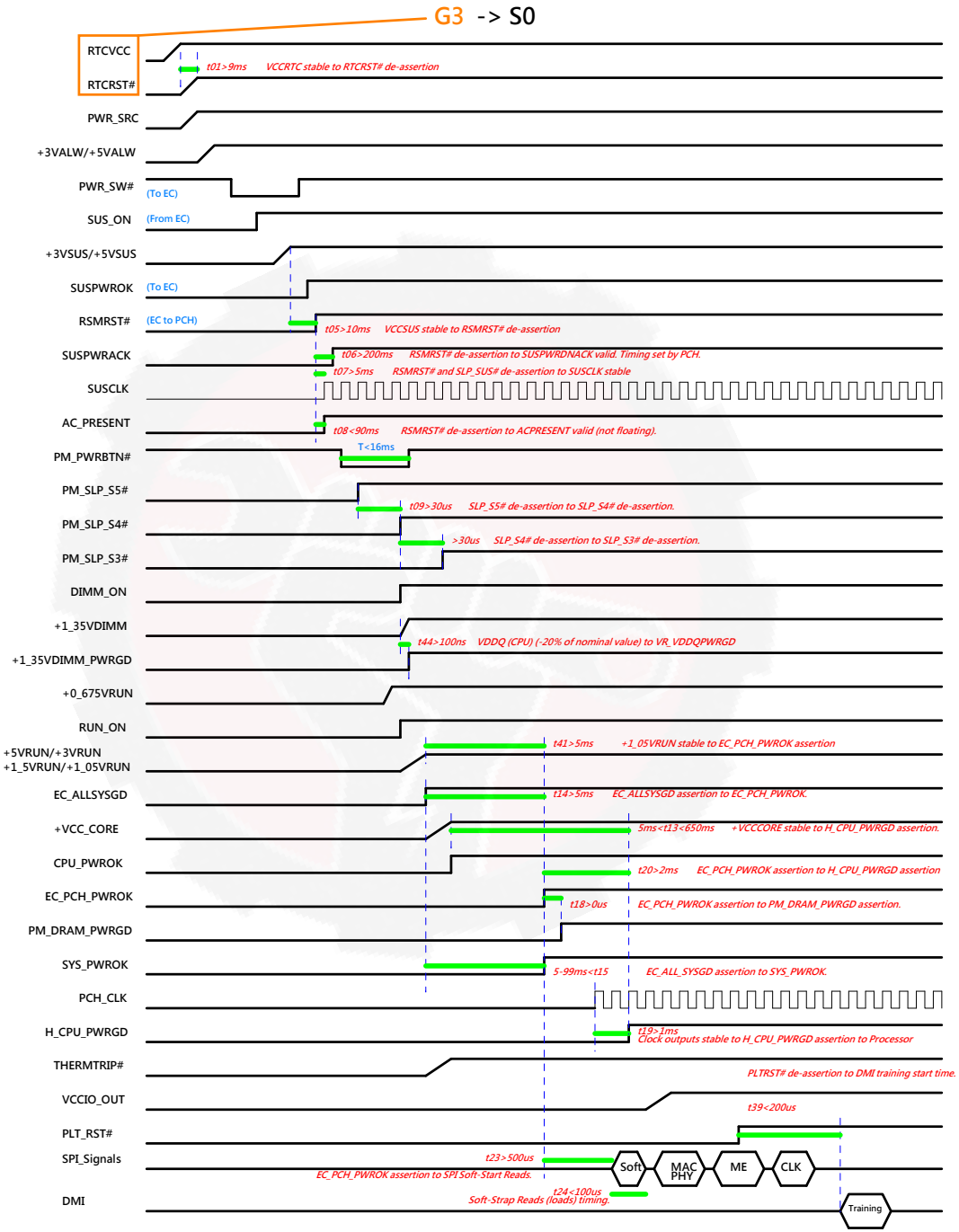
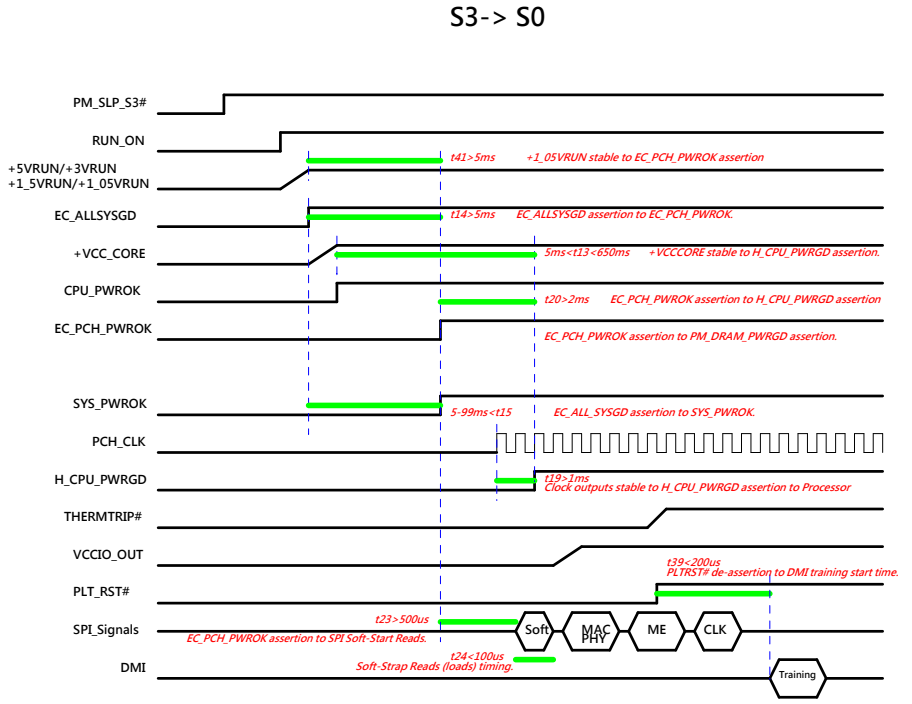
Power on Sequence





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History

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