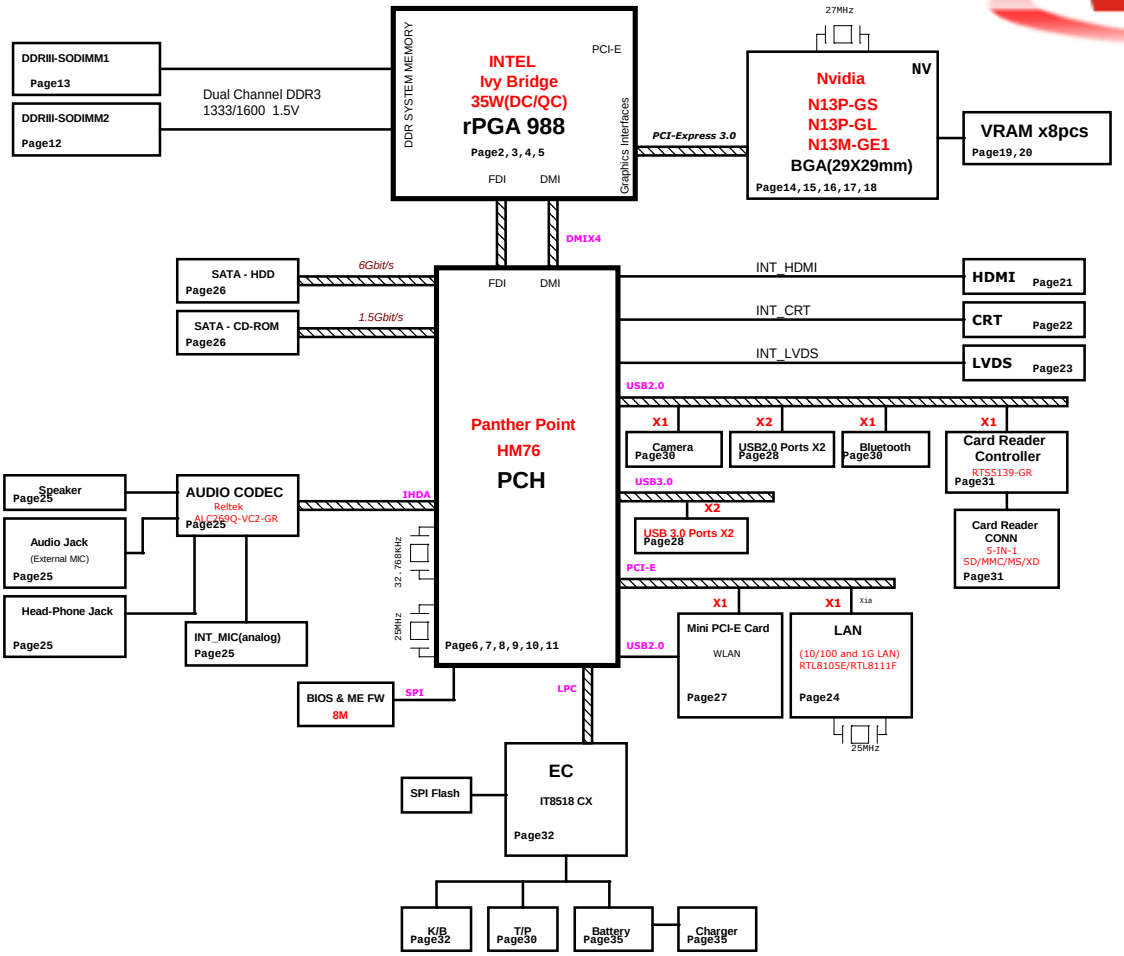
LZ3/LZ3A (Z580) Intel Chief River Platform (Optimus) Block Diagram 0.1



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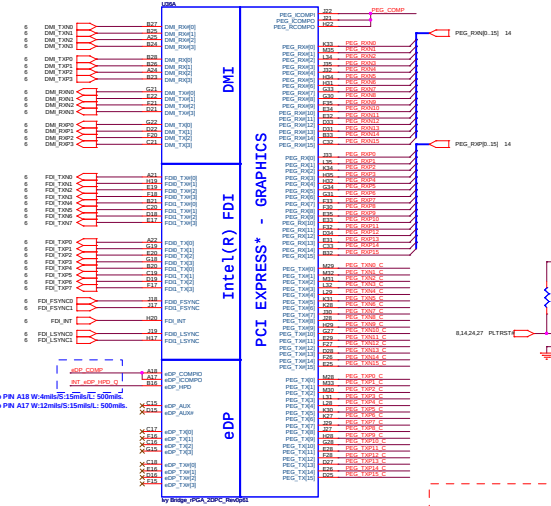
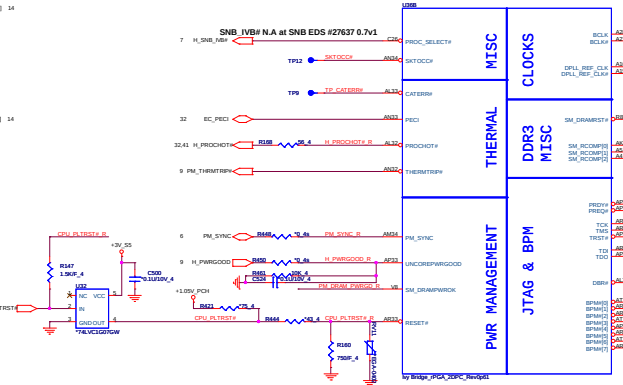
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

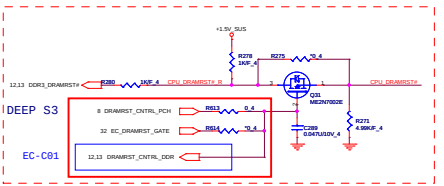
4,6,7,8,10,33,34,38,43 +1.05V_PCH
4,10,12,13,33,34,37,43 +1.5V_SUS
6,7,8,9,10,27,33,34 +3V_S5
4,33 +1.5V_CPU

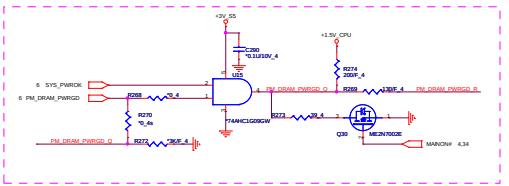
Ivy Bridge Processor (DMI,PEG,FDI)



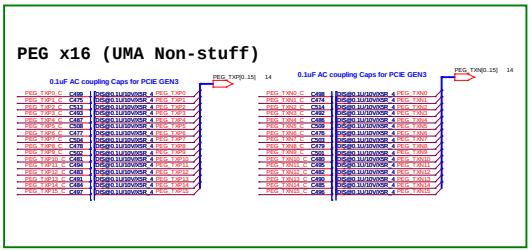
Ivy Bridge Processor (CLK,MISC,JTAG)



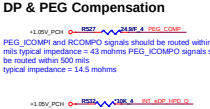




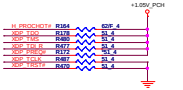
PEG x16 (UMA Non-stuff)



DP & PEG Compensation



Processor pull-up(CPU)



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Quanta Computer Inc.
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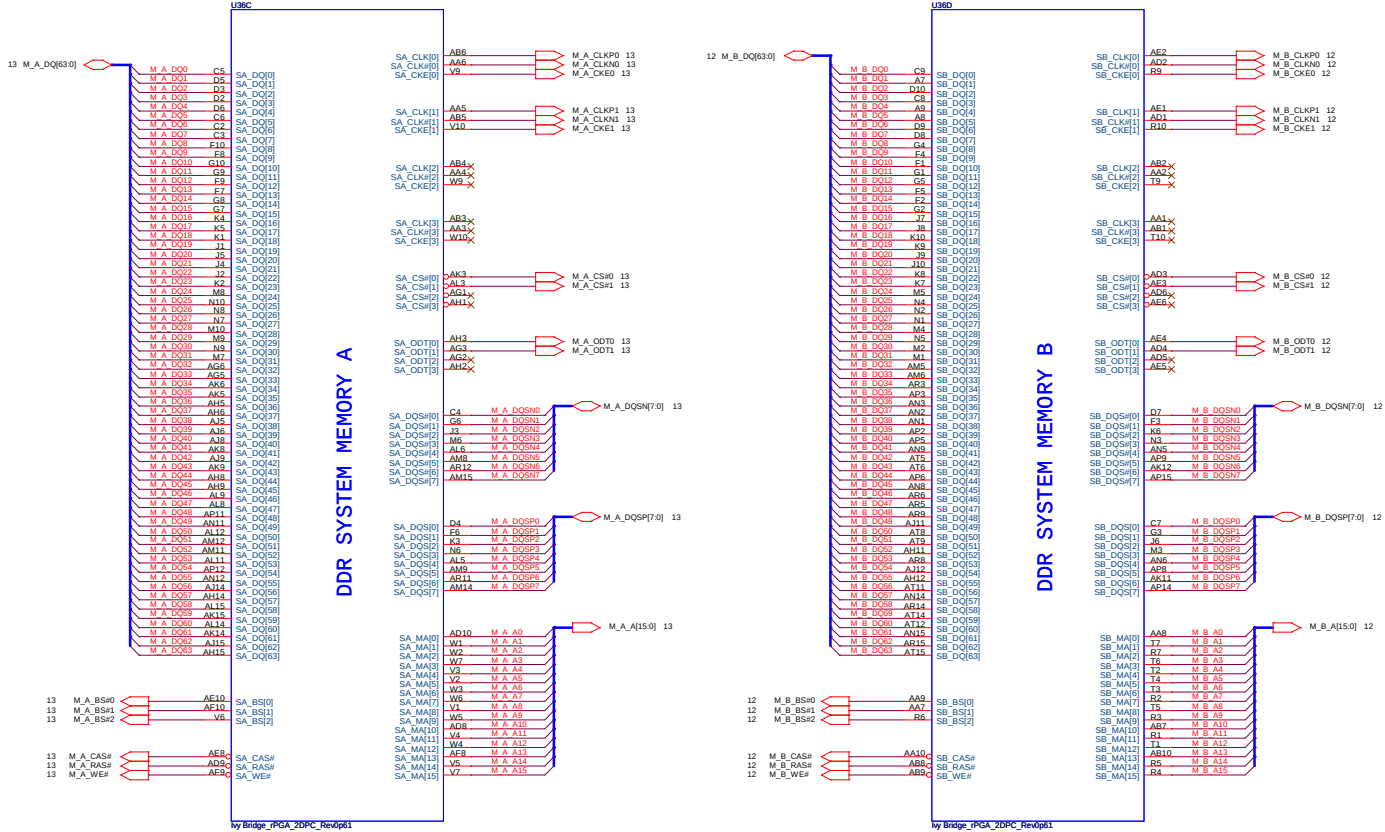
Ivy Bridge Processor (DDR3)



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Quanta Computer Inc.

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CPU Core Power

SNB: 55A
IVY: 55A

SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

22uF_8 x8 Socket TOP cavity

22uF_8 x10 Socket TOP edge

10uF_8 x10 Socket BOT cavity

POWER

CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES

CPU VTT

SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

22uF_8 x7 Socket TOP cavity
22uF_8 xS Socket BOT cavity

22uF (Reserved)

CPU VGT

SNB 45W:33A
22uF x 12
22uF x 4 (Reserved)

POWER

SENSE LINES
VREF
DDR3 -1.5V RAILS
SA RAIL
MISC
1.8V RAIL
GRAPHICS

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

330uF x1, 10uF_8 x6 Socket BOT edge.

22uF (Reserved)

CPU MCH

SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

SNB: 5A
IVY: 5A

SNB: 6A
IVY: 6A

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

CPU SA

SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

CPU VCCPL

SNB 45W:1.5A
330uF/7mohm x 1
10uF x 1
1uF x 2

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR

SVID DATA
Close to VR

Place PU resistor close to CPU

SVID ALERT
Place PU resistor close to CPU

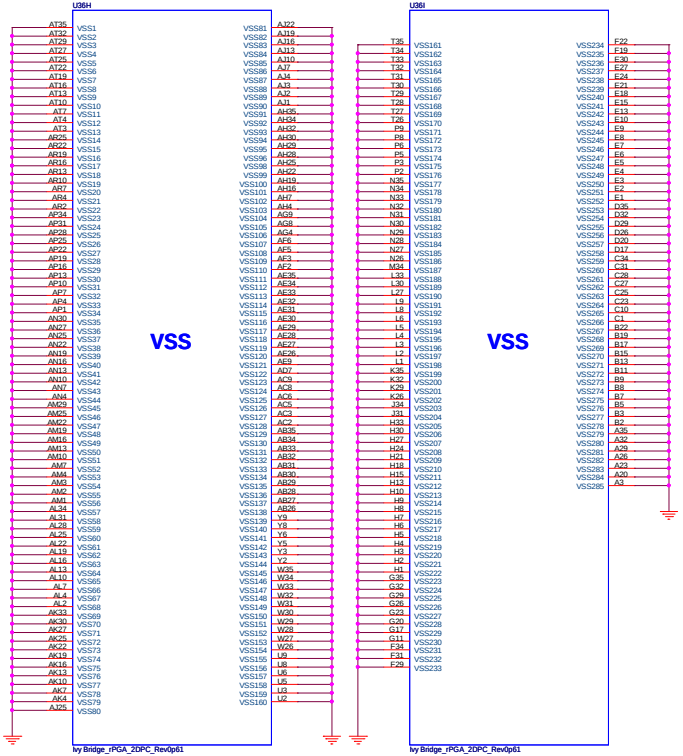
4.5A

Placement close to CPU.

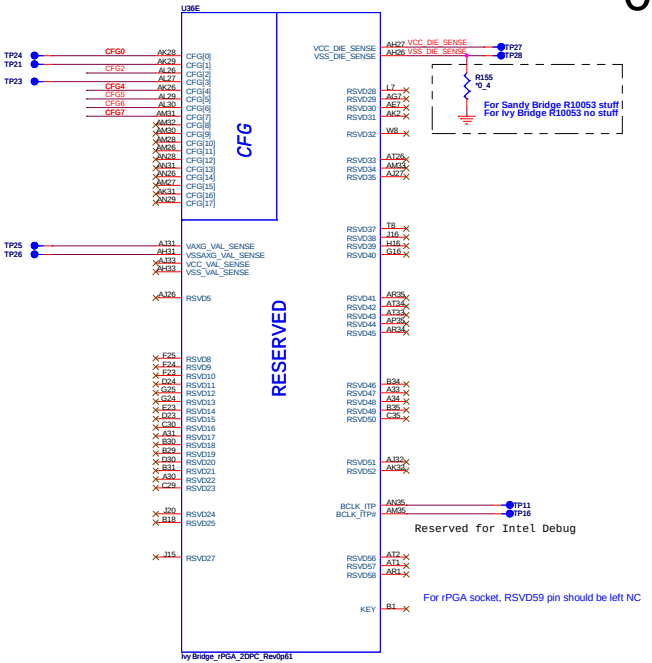
0.5A

PROJECT : LZ2A
Quanta Computer Inc.
IVY Bridge 3/4

Ivy Bridge Processor (GND)



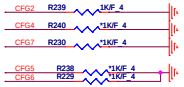
Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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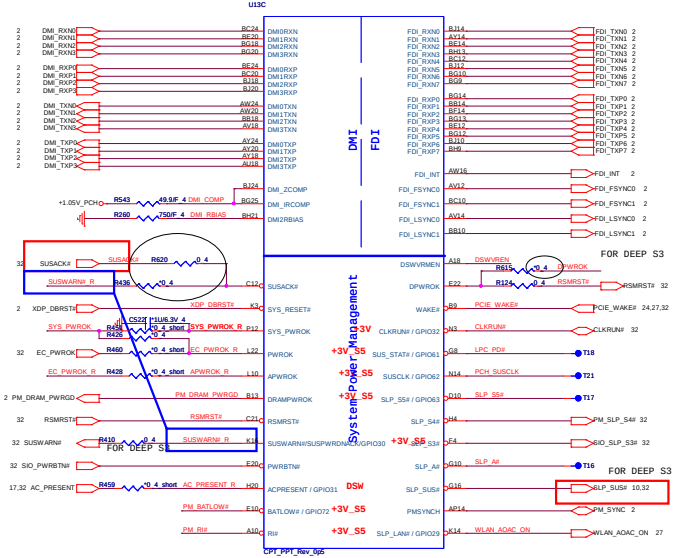
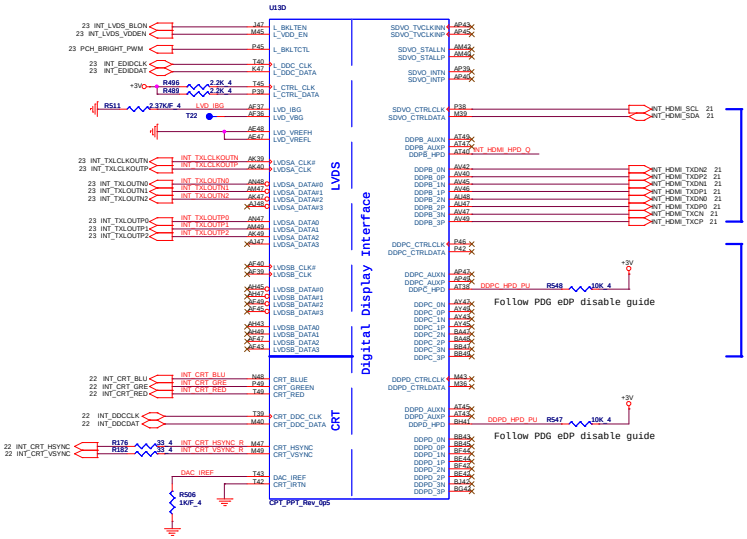
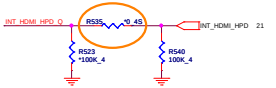
2,4,7,8,10,33,34,38,43 +1.05V_PCH
7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
2,7,8,9,10,27,31,34 +3V_S5
7,10,32 +3V_RTC

Cougar Point/Panther Point (DMI,FDI,PM)

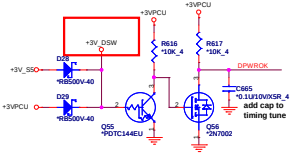


Cougar Point/Panther Point (LVDS,DDI)

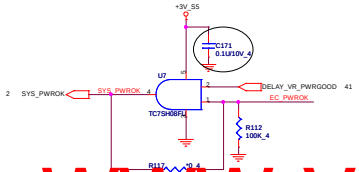


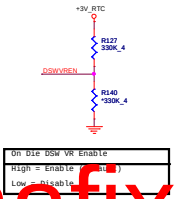


DPWROK FOR DSW (DEEP S3)

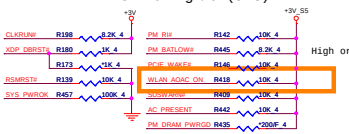


System PWR_OK(CLG)





PCH Pull-high/low(CLG)



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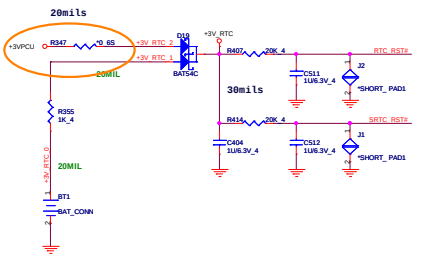
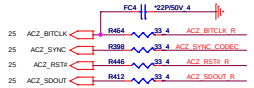
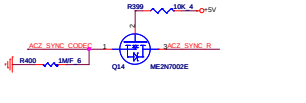
RTC Circuitry(RTC)



HDA Bus(CLG)

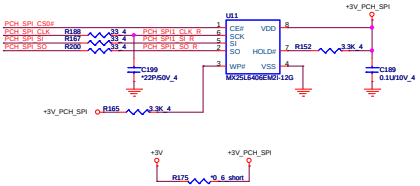




PCH Dual SPI (CLG)

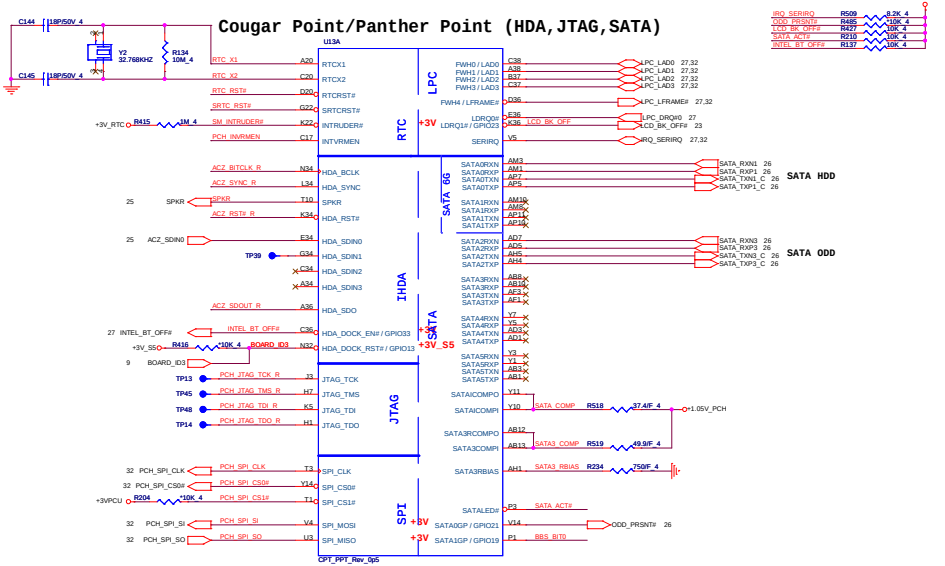
32Mbit (8M Byte), SPI

AKE3EFP0N04: W25Q64CVSSIG
AKE3ENF0Q00: EN25Q64-104HIP
AKE3NFP0Z00: MX25L6406EM2I-12G
Socket: DG0080000031



PCH2(CLG)

Cougar Point/Panther Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NCTF	Level Anti-Fuse HDD protection	PWROK	0 = Disable (weak pull-down 20kohm)

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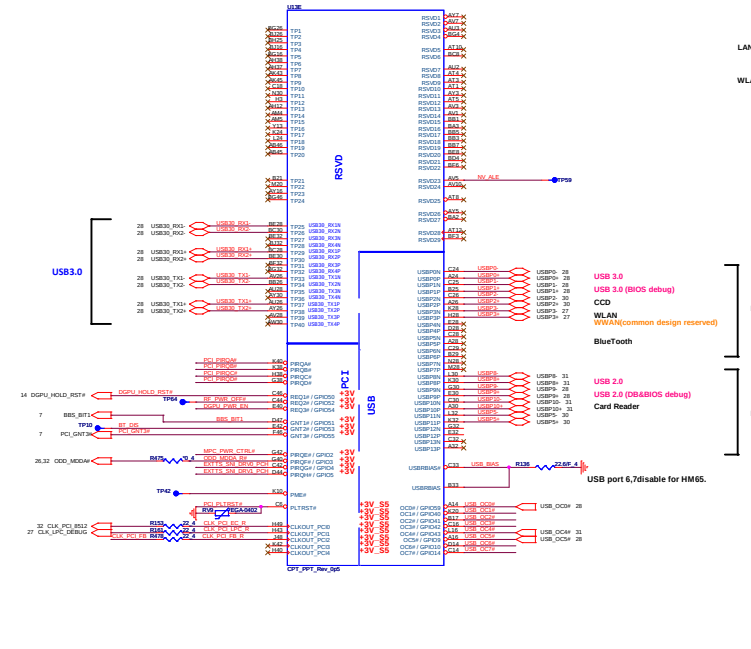
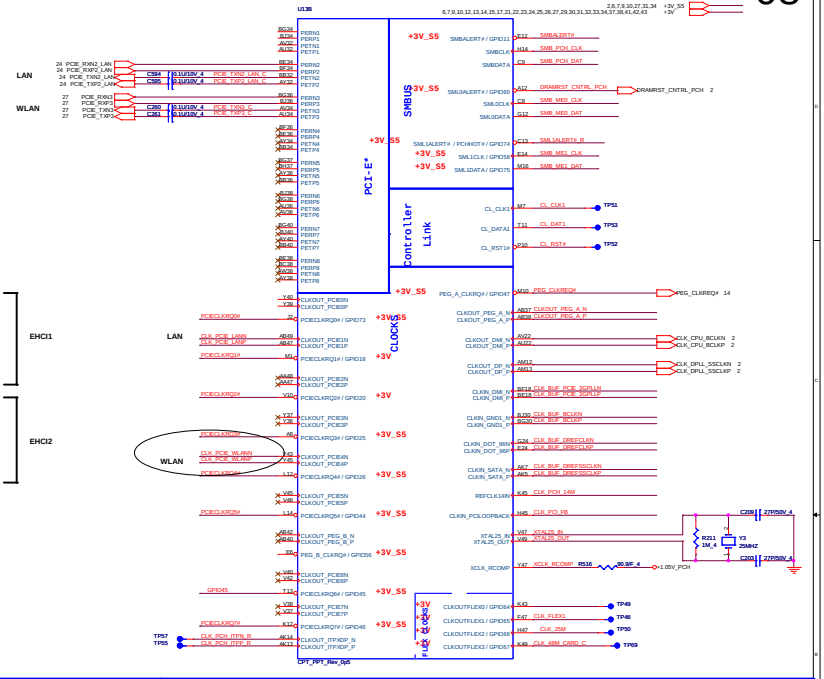
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



USB 3.0

USB 3.0 (BIOS debug)

CCD

WLAN

WWAN(common design reserved)

BlueTooth

EHCI1

USB 2.0

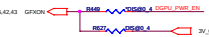
USB 2.0 (DB&BIOS debug)

Card Reader

EHCI2

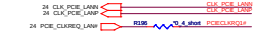
USB port 6,7disable for HM65.

DGPU Power ON

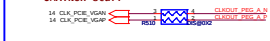


WLAN

LAN



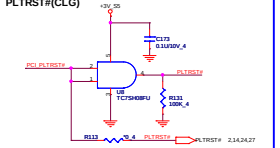
SW:Stuff UMA:Non-stuff



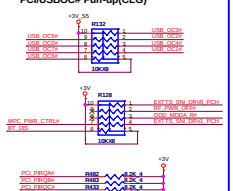
MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

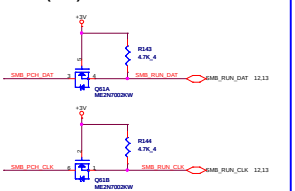
PLTRST#(CLG)



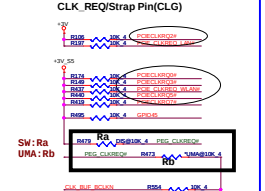
PCI/USBOC# Pull-up(CLG)



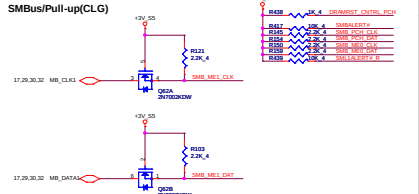
SMBus(CLK)



CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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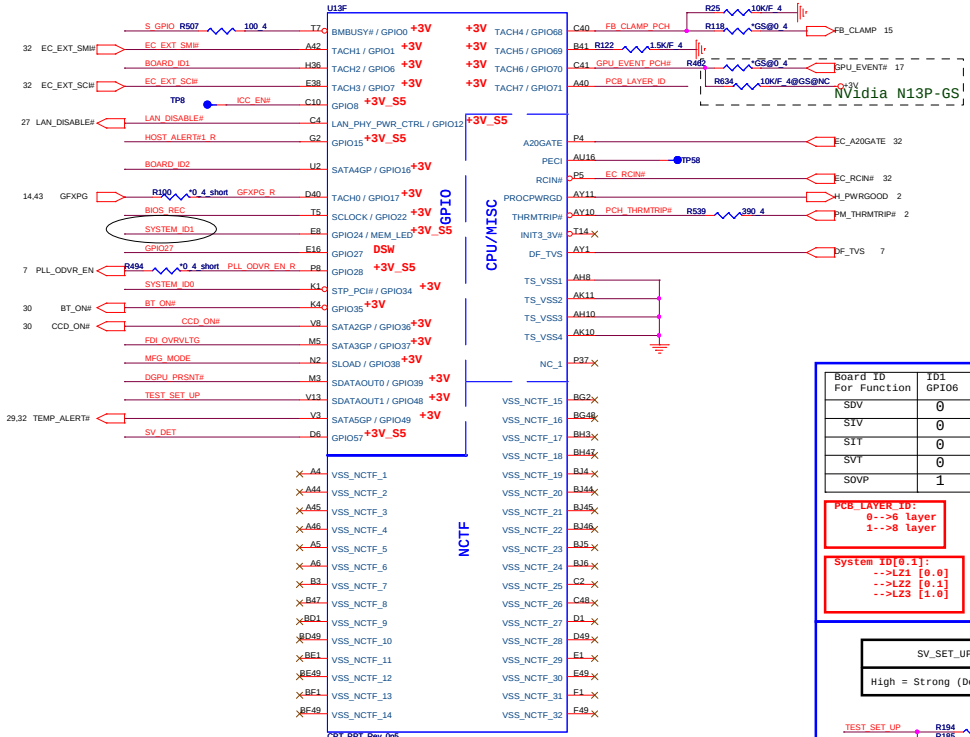
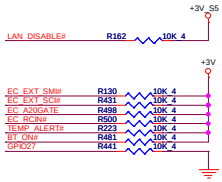
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09



GPIO Pull-up/Pull-down(CLG)



Board ID

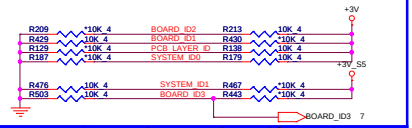
Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT	0	1	1
SOVP	1	0	0

LZ1,LZ2,LZ3

Board ID use below GPIO:
BOARD_ID1
BOARD_ID2
BOARD_ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0.1]:
-->LZ1 [0.0]
-->LZ2 [0.1]
-->LZ3 [1.0]



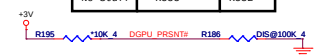
Arvin Wang update table on 9/19 14:12

LZ2	BOARD ID0 GPIO 71	SYSTEM ID0 GPIO 34	SYSTEM ID1 GPIO 24
6 Layer	0	0	1
8 Layer	1	0	1

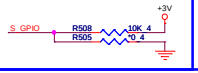
SV_SET_UP
High = Strong (Default)

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

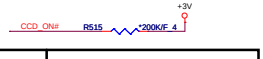
	SWITCHABLE	UMA
Stuff	R532	R533
No Stuff	R533	R532



SGPIO



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

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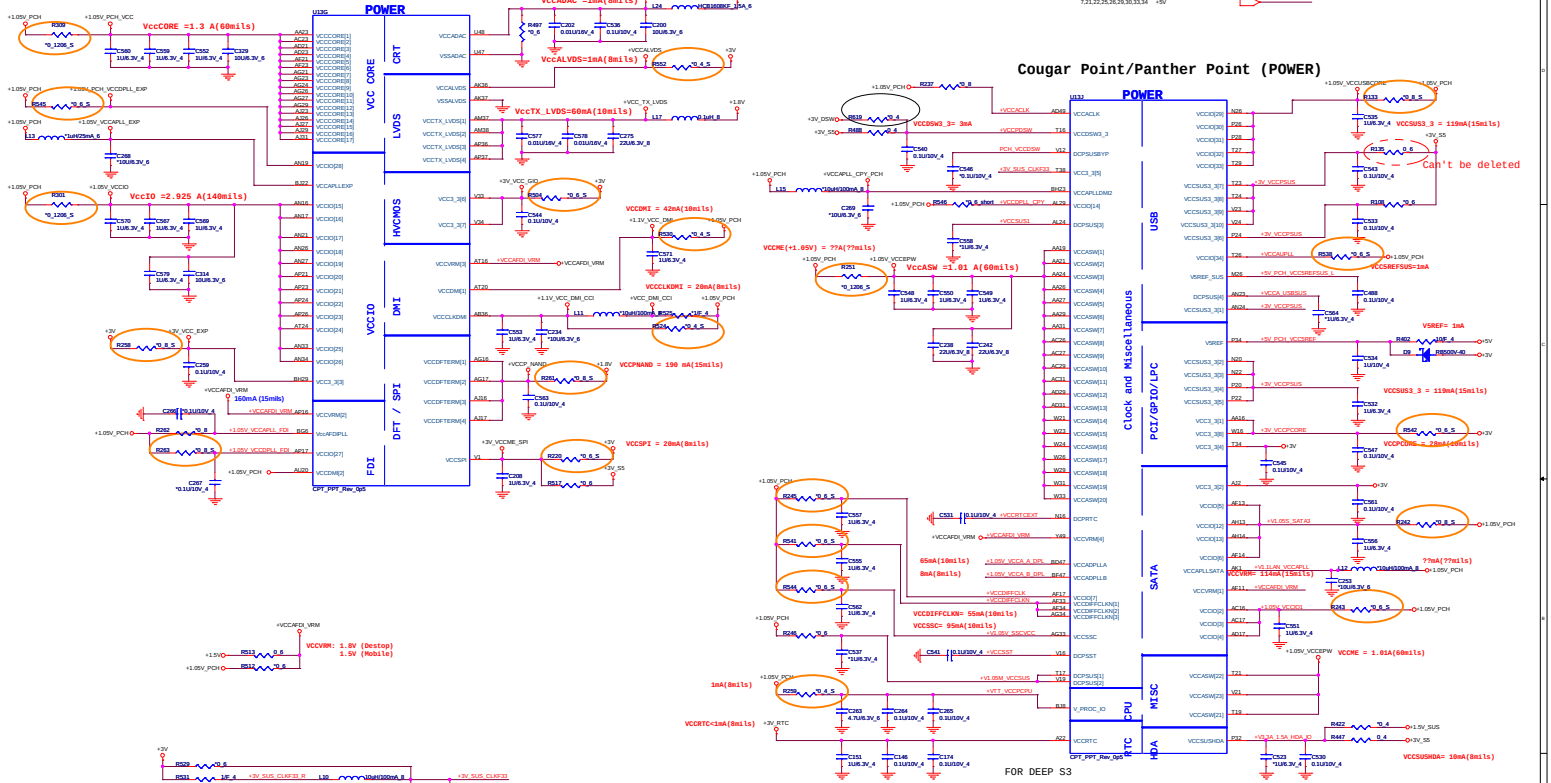
Cougar Point/Panther Point (POWER)



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Quanta Computer Inc.
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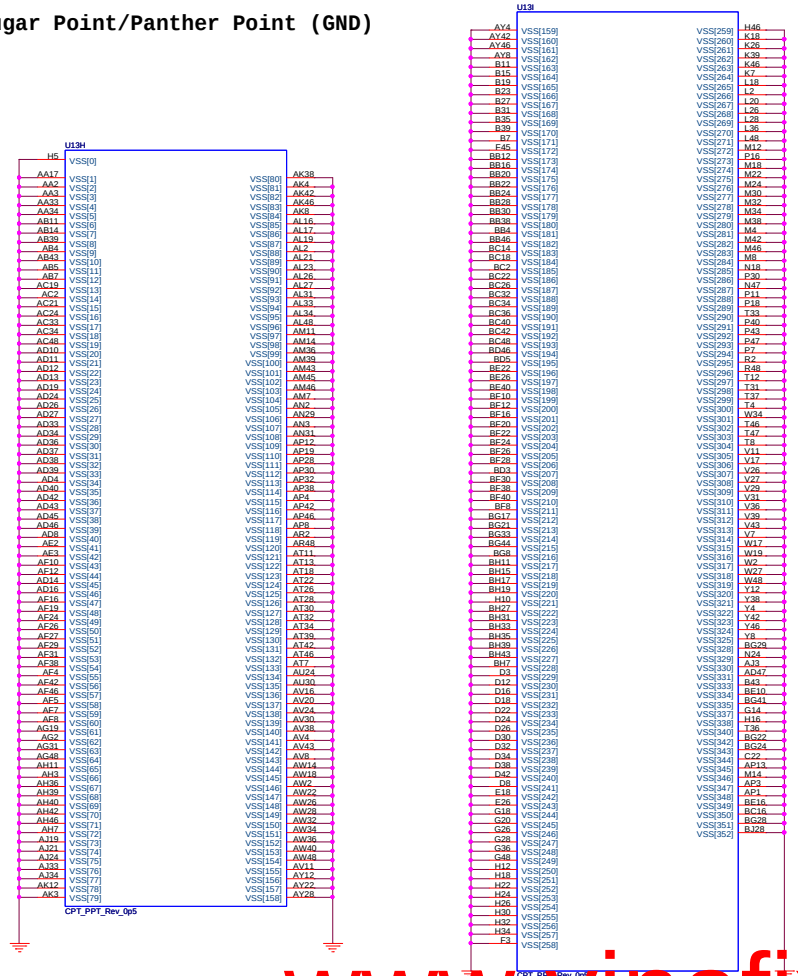
Cougar Point/Panther Point (GND)



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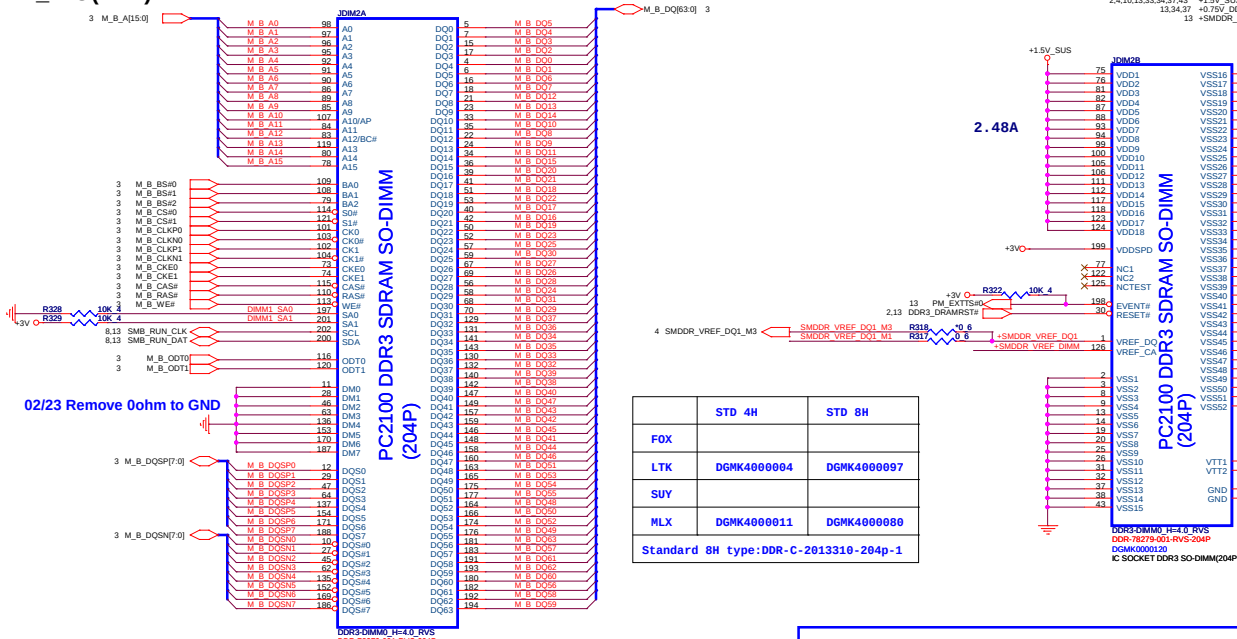
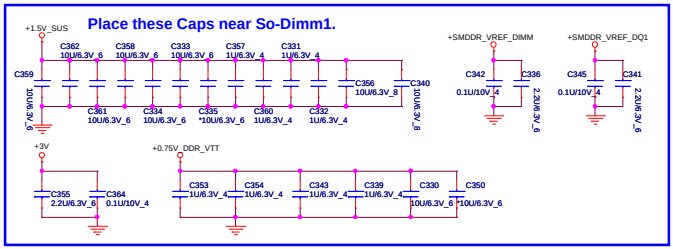
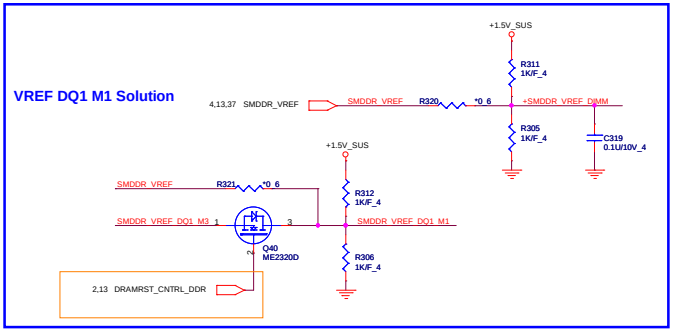
DDR_RVS(DDR)



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1





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Quanta Computer Inc.	
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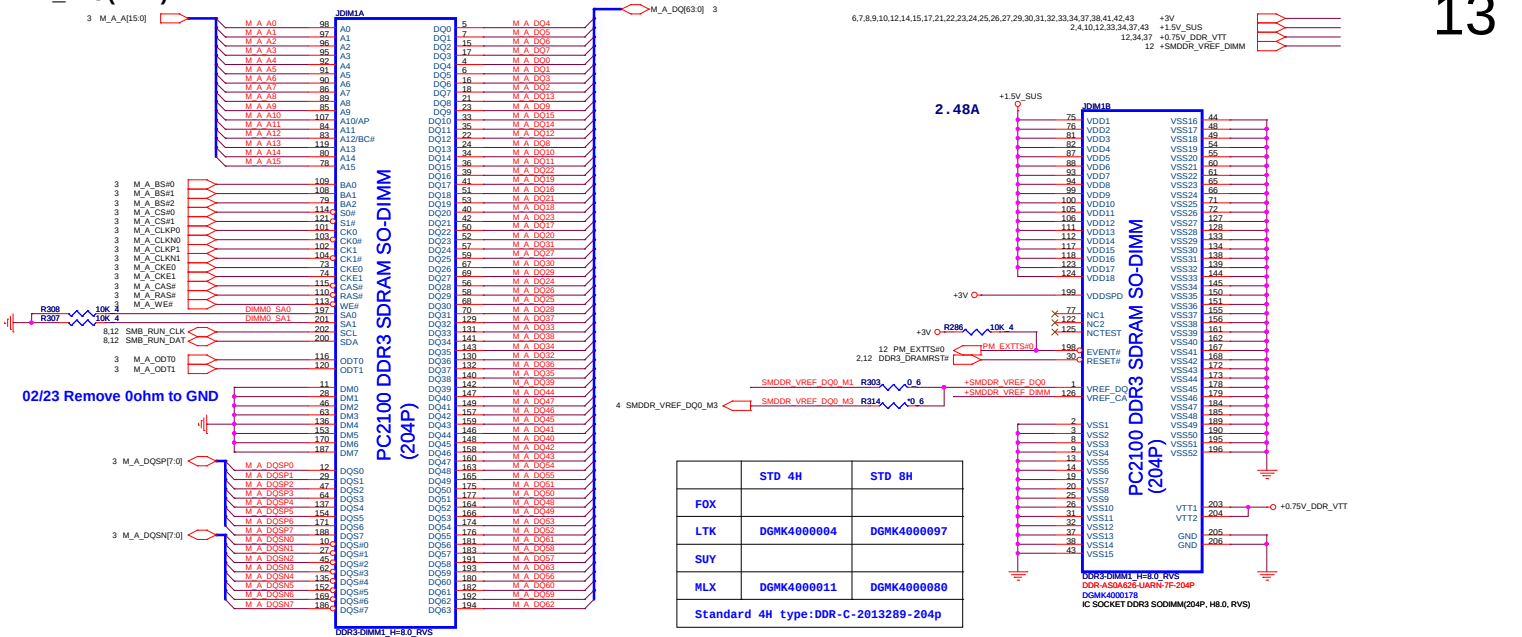
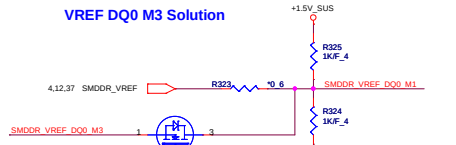
DDR_RVS(DDR)



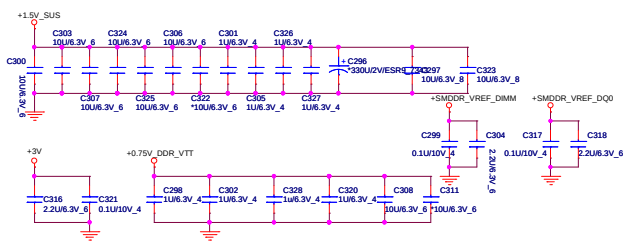
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p

VREF DQ0 M3 Solution



Place these Caps near So-Dimm0.



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PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A

CAP CLOSE TO BGA

12~16 mils width

210mA

0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108) N13M-GE1 (GF119)	unstuff

16 mils width for 110mA

GPU RST#(CLG)

150mA

1/19 PCI_EXPRESS

All GPU power rails must ramp up after VDD33. The following conditions must be met:

- tNVVDD > 0
- tFBVDDQ > 0
- tFPEX_VDD > 0
- tFPx_IOVDD ≥ 0
- tFPy_IOVDD ≥ 0
- The ramp time for any rail must be more than 40 us.

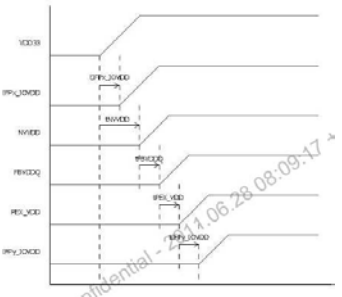


Figure 17. Recommended Power On Sequencing Order

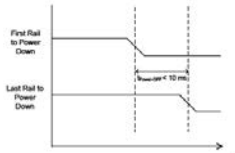
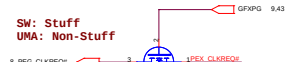


Figure 18. Recommended Power Off Sequencing Order

For power-down sequency

PEG CLK detect

SW: Stuff
UMA: Non-Stuff



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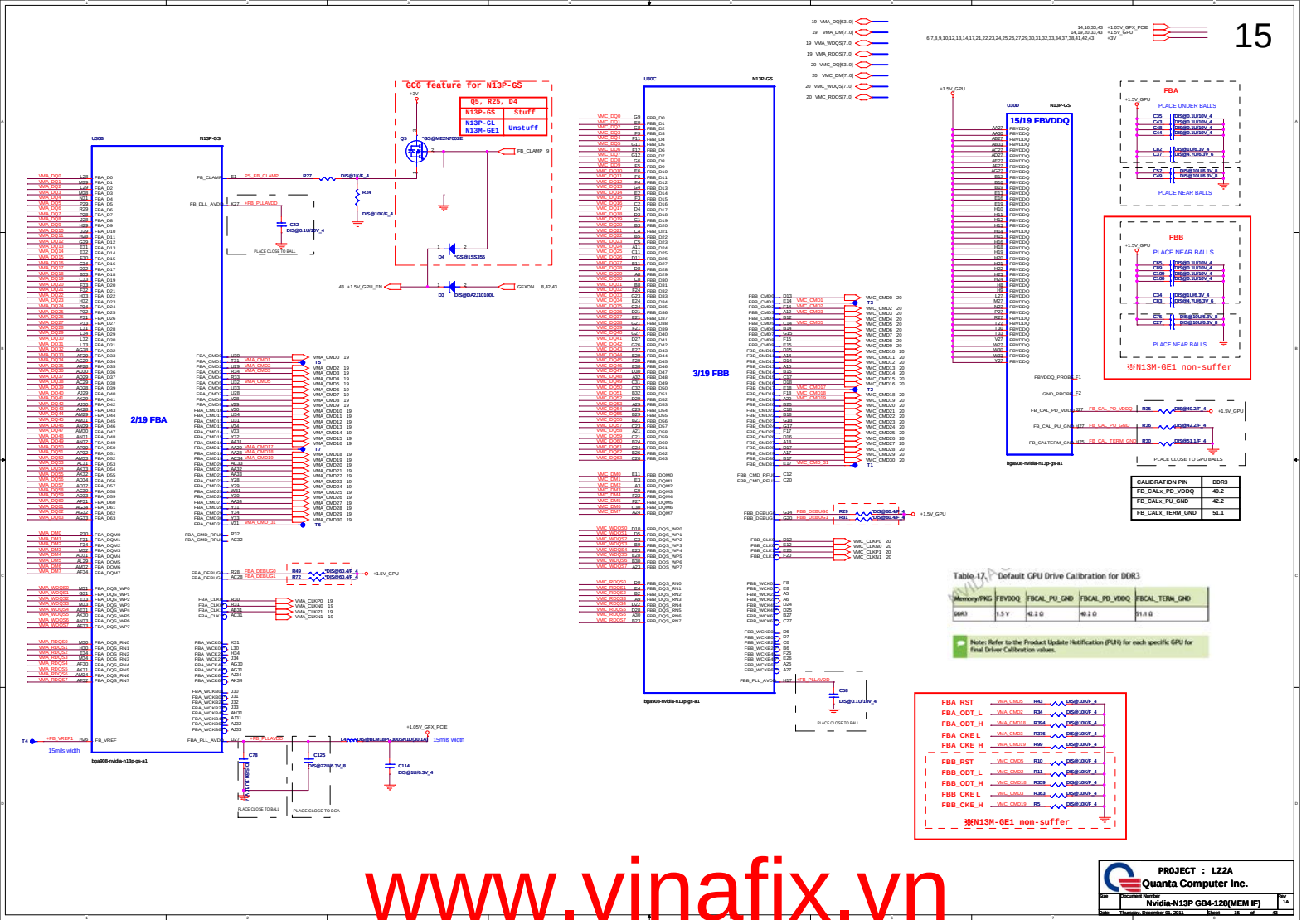

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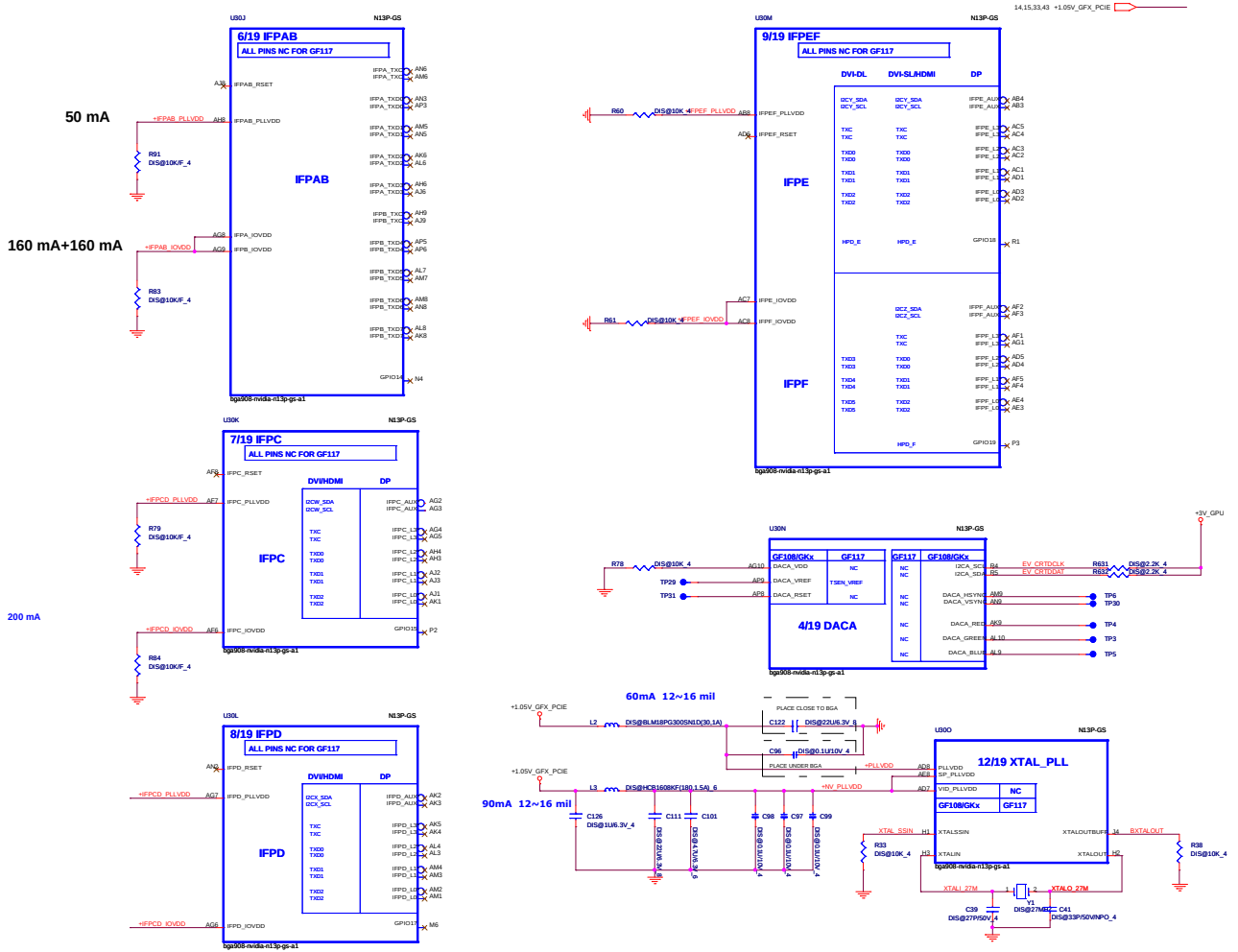

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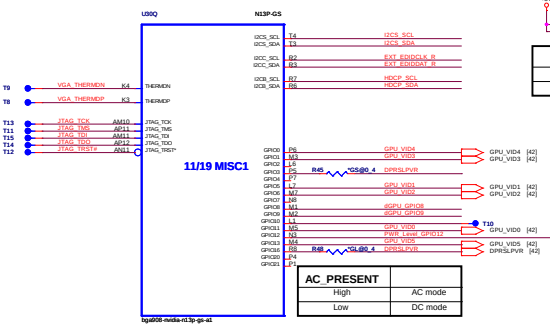
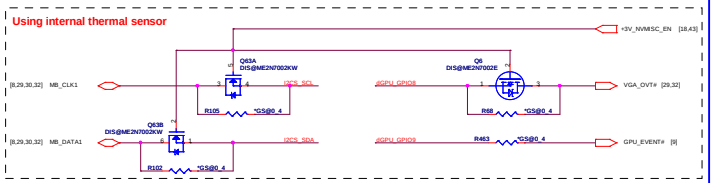


AC_PRESENT	
High	AC mode
Low	DC mode

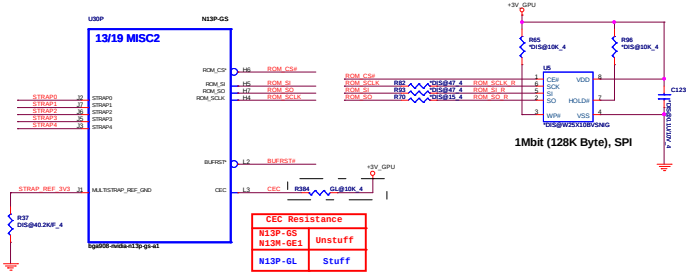
+3.3V_GPU	Output
ON	EXT_HDMI/DP
OFF	INT_HDMI/DP



	Q5,Q63, R81,R104	R88,R102, R105,R463
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor



CEC Resistance	
N13P-GS N13M-GE1	Unstuff
N13P-GL	Stuff

Table 2. GB4-128 Ballout Compatibility

Ball Number	N13P-PES/-GL/-NS1 Signal Names	N13M-GE1 Signal Names	N13P-GV / N13M-GS Signal Names	N13P-GT/-GS/-LP and N14P-Q1/-Q3 Signal Names	Comment
L3	CEC	NC	NC	NC	Place a 10k pull-up to 3V3 on N13P-PES/-GL/-NS1

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_6_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24993FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS21002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS21502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS22002FB29	RES CHIP 20K 1/16W +-1%(0402)
24.9K/F_4	CS22492FB16	RES CHIP 24.9K 1/16W +-1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +-1%(0402))
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +-1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +-1%(0402)

VRAM Configuration Table ※ROM_SI Strap Bit for RAM Mapping

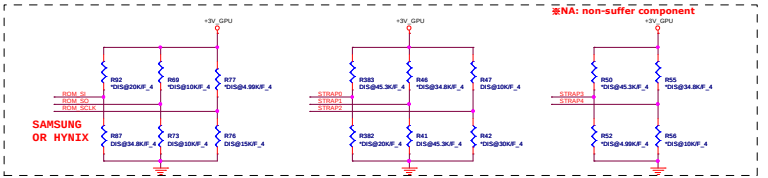
VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKD5EGGT500		K4W1G1646G-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C	0x2(0010)	R87 (15K ohm)

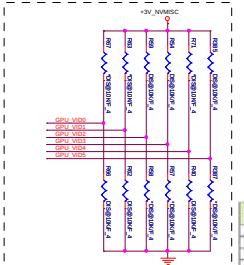
Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

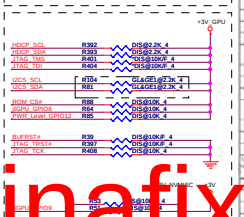
GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

※NA: non-suffer component





NVVDD Table	N13M-GE1-A1 (GF119)	N13P-GL-A1 (GF108)	N13P-GS-A1 (GK107)
	NVVDD (0.9V)	NVVDD (0.95V)	NVVDD (0.9V)
GPU_VID0	0 (R66)	0 (R66)	0 (R66)
GPU_VID1	0 (R62)	0 (R62)	0 (R62)
GPU_VID2	0 (R58)	1 (R59)	0 (R58)
GPU_VID3	0 (R57)	1 (R54)	0 (R57)
GPU_VID4	1 (R71)	0 (R40)	1 (R71)
GPU_VID5	1 (R385)	1 (R385)	1 (R385)



GPIO ASSIGNMENTS

GPIO pin Name	Normal Function	I/O	Functional Description
GPIO00	GPU_VID4	O	GPU Core VDD VID4
GPIO01	GPU_VID3	O	GPU Core VDD VID3
GPIO02	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO03	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding
GPIO04	LCD_BLEN	O	Panel Backlight Enable
GPIO05	GPU_VID1	O	GPU Core VDD VID1
GPIO06	GPU_VID0	O	GPU Core VDD VID0
GPIO07	3D Vision	O	3D Vision Left/Right signal
GPIO08	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO09	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_A0	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		

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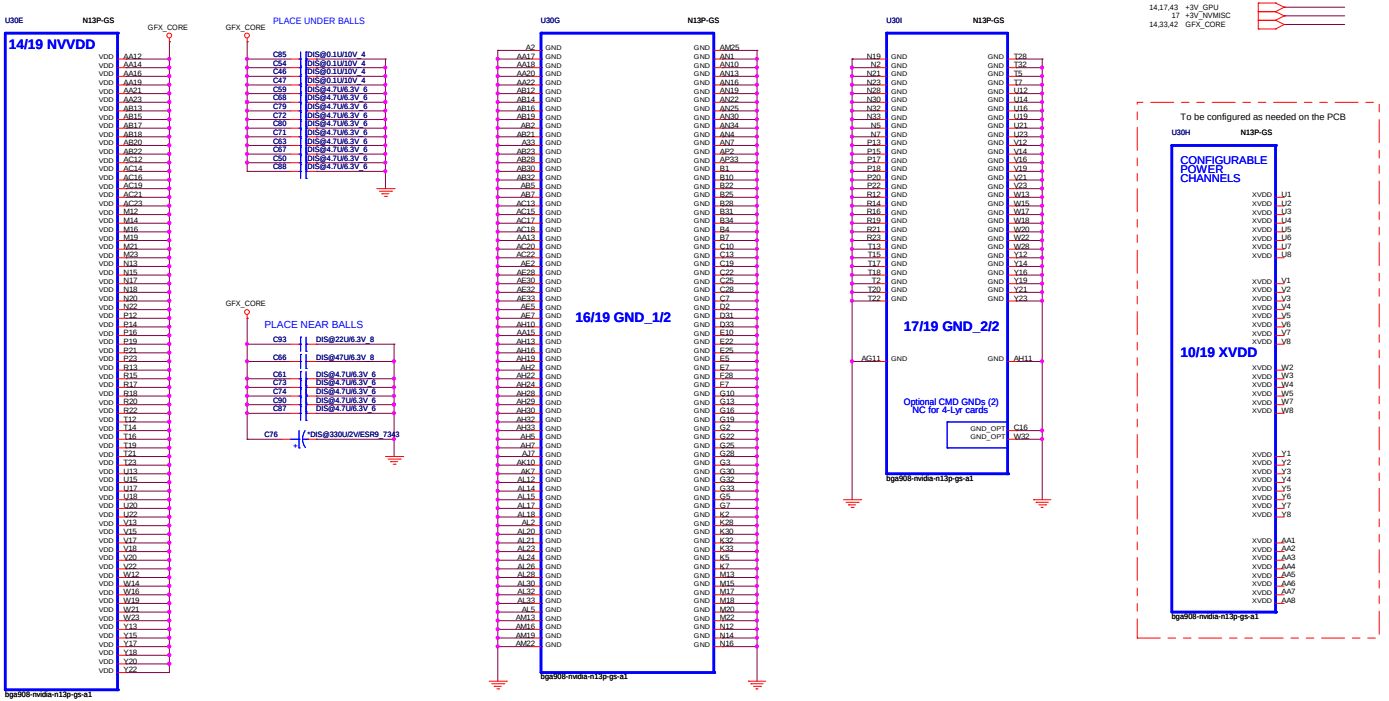

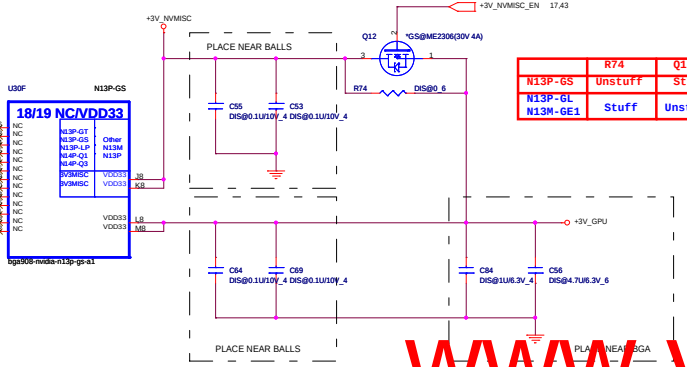

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

Table 5. Stuffing Options

GPU	Signal/Rail	Stuffing Option
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	No stuff FET Stuff 0Ω bypass resistor
	3V3MISC	Stuff FET No stuff 0Ω bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff 0Ω bypass resistor
	3V3MISC	No stuff FET Stuff 0Ω bypass resistor

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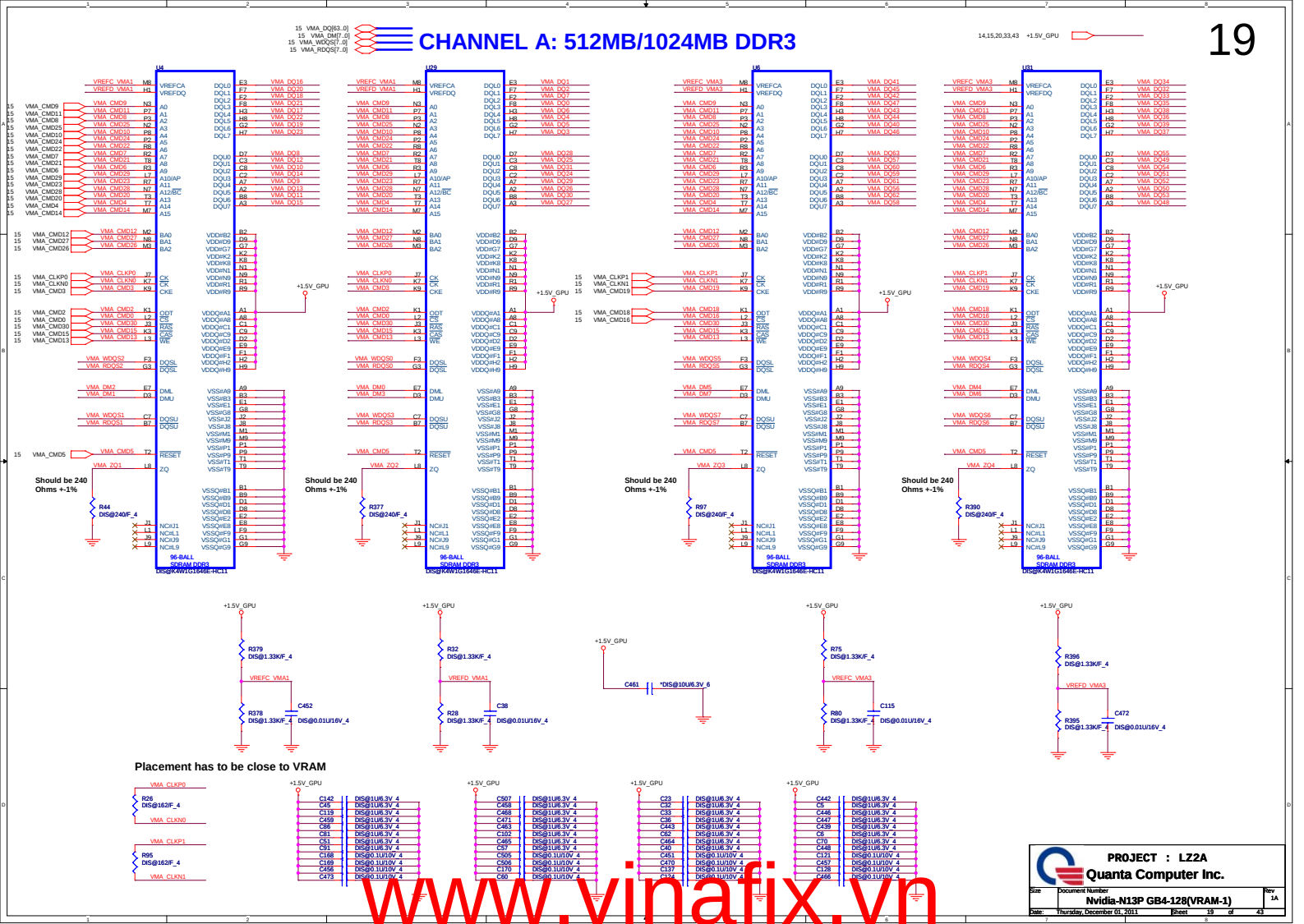
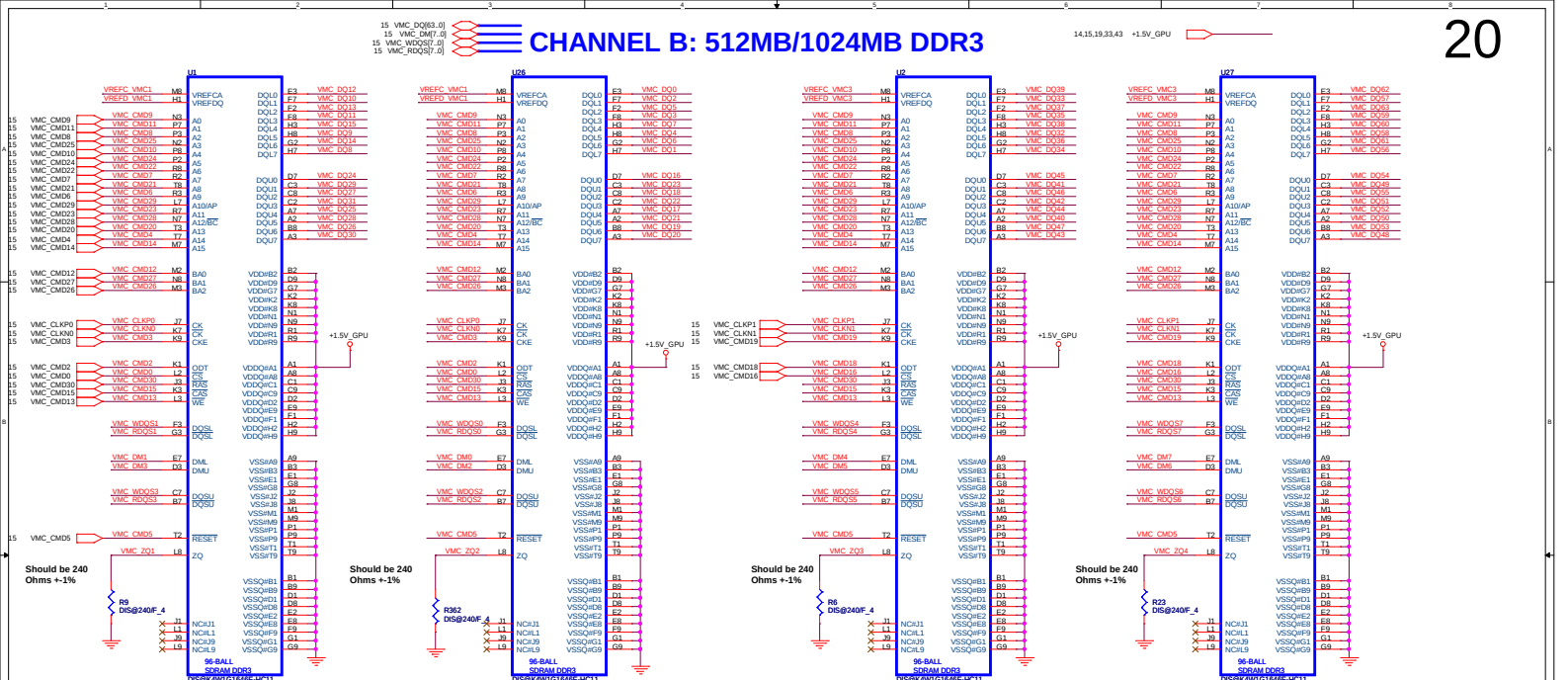
CHANNEL A: 512MB/1024MB DDR3



CHANNEL B: 512MB/1024MB DDR3



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Quanta Computer Inc.			
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6,7,8,9,10,12,13,14,15,17,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43 +3V
7,10,22,25,26,29,30,33,34 +5V

Change to KL6/BC HDMI CONN

6 INT_HDMI_TXDP2 — C620 0.1U/10V_4 — HDMI_TX2+
6 INT_HDMI_TXDN2 — C619 0.1U/10V_4 — HDMI_TX2-
6 INT_HDMI_TXDP1 — C618 0.1U/10V_4 — HDMI_TX1+
6 INT_HDMI_TXDN1 — C617 0.1U/10V_4 — HDMI_TX1-
6 INT_HDMI_TXDP0 — C616 0.1U/10V_4 — HDMI_TX0+
6 INT_HDMI_TXDN0 — C615 0.1U/10V_4 — HDMI_TX0-
6 INT_HDMI_TXCP — C613 0.1U/10V_4 — HDMI_CLK+
6 INT_HDMI_TXCN — C611 0.1U/10V_4 — HDMI_CLK-

6 INT_HDMI_SCL — INT_HDMI_SCL
6 INT_HDMI_SDA — INT_HDMI_SDA
6 INT_HDMI_HPD — INT_HDMI_HPD

+3V — R551 10K_4 — INT_HDMI_HPD — Q69A ME2N7002DKW-G — R553 10K_4 — Q69B ME2N7002DKW-G — HP_DET — R549 20K_4

+3V — R316 2.2K_4 — R297 2.2K_4 — INT_HDMI_SCL — Q43 DMN5L06K-7
+3V — INT_HDMI_SDA — Q39 DMN5L06K-7
+5V — R313 2.2K_4 — R568 2.2K_4
C668 *68p/50V_4 — C669 *68p/50V_4
+5V — FUSE_1.1A_6V_POLY — F2 — HDMIC_5V — HP_DET
C667 0.1U/10V_4

CN16 CONN_HDMI
HDMI_TX2+ — D2+ — SHELL1 SHELL2
HDMI_TX2- — D2 Shield — D2-
HDMI_TX1+ — D1+ — D1 Shield — D1-
HDMI_TX0+ — D0+ — D0 Shield — D0-
HDMI_CLK+ — CK+ — CK Shield — CK-
HDMI_CLK- — CE Remote — NC
HDMI_DDC_CLK — DDC CLK
HDMI_DDC_DAT — DDC DATA
GND — +5V — HDMIC_5V — HP_DET — SHELL3 SHELL4

HDMI Hot-PLUG to EC and GPU

R315 590/F_4 HDMI_TX2+ / R310 590/F_4 HDMI_TX2-
R304 590/F_4 HDMI_TX1+ / R302 590/F_4 HDMI_TX1-
R300 590/F_4 HDMI_TX0+ / R298 590/F_4 HDMI_TX0-
R294 590/F_4 HDMI_CLK+ / R291 590/F_4 HDMI_CLK-
SC51 0.1U/10V_4
3VDMI_F
Q42 2N7002K
+5V — 2 — 1

For ESD

U39 *CM1225: HDMI_TX2+ (6) HDMI_TX2- (7) HDMI_TX1+ (9) HDMI_TX1- (10) — NC CH4 NC CH3 GND GND NC CH2 NC CH1 — (5) HDMI_TX2+ (4) HDMI_TX2- (3) (2) HDMI_TX1+ (1) HDMI_TX1-
U38 *CM1225: HDMI_TX0+ (6) HDMI_TX0- (7) HDMI_CLK+ (9) HDMI_CLK- (10) — (5) HDMI_TX0+ (4) HDMI_TX0- (3) (2) HDMI_CLK+ (1) HDMI_CLK-
U37 *CM1225: HDMI_DDC_DAT (6) HDMI_DDC_CLK (7) HDMIC_5V (9) HP_DET (10) — (5) HDMI_DDC_DAT (4) HDMI_DDC_CLK (3) (2) HDMIC_5V (1) HP_DET

EMI reserve for HDMI

HDMI_TX2+ — R574 140/F_4 — HDMI_TX2-
HDMI_TX1+ — R573 140/F_4 — HDMI_TX1-
HDMI_TX0+ — R572 140/F_4 — HDMI_TX0-
HDMI_CLK+ — R569 140/F_4 — HDMI_CLK-

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Quanta Computer Inc.
Size: Custom | Document Number: Madison_LVDS/HDMI/CRT switchable | Rev: 1A
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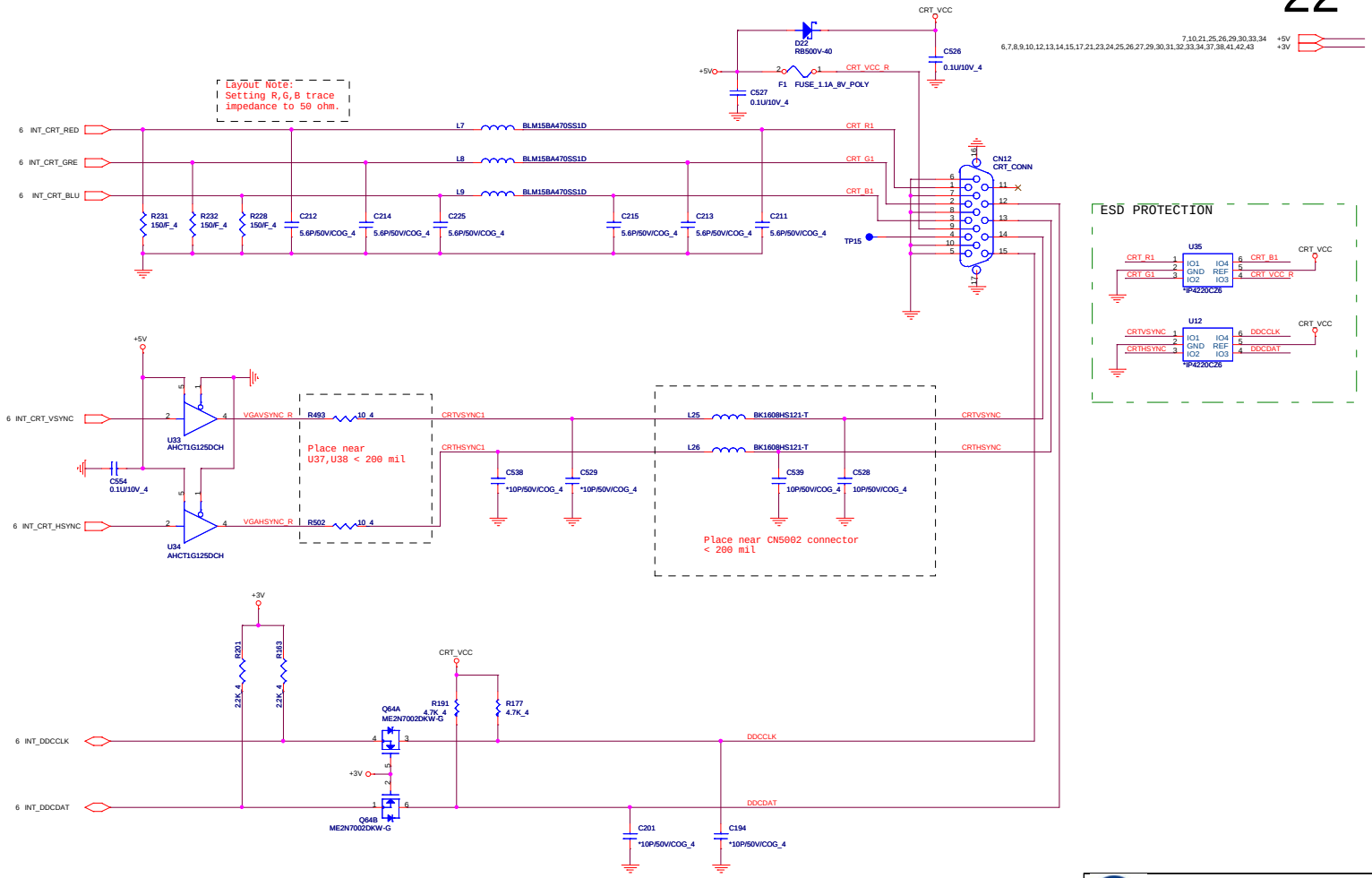

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Custom	CRT CONN	1A

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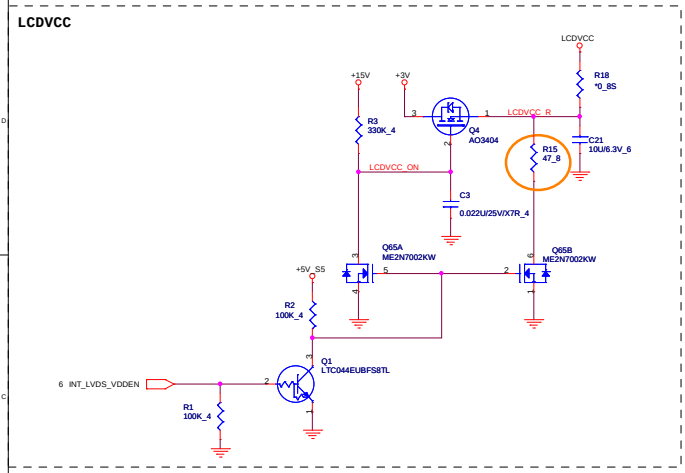
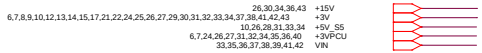
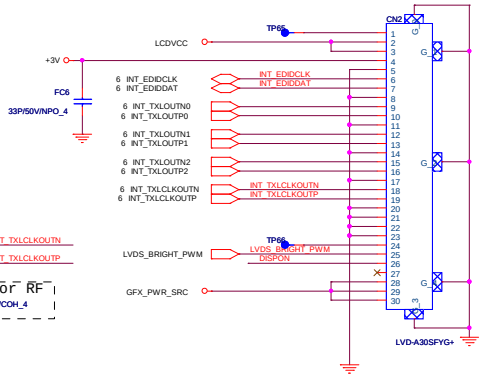
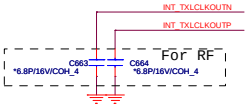
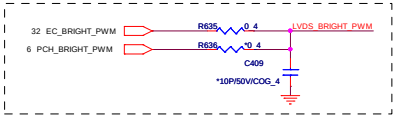
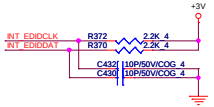




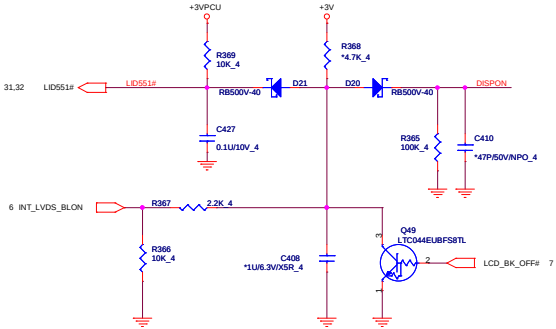


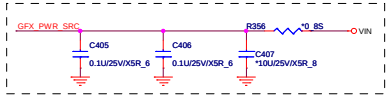






back light





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Quanta Computer Inc.

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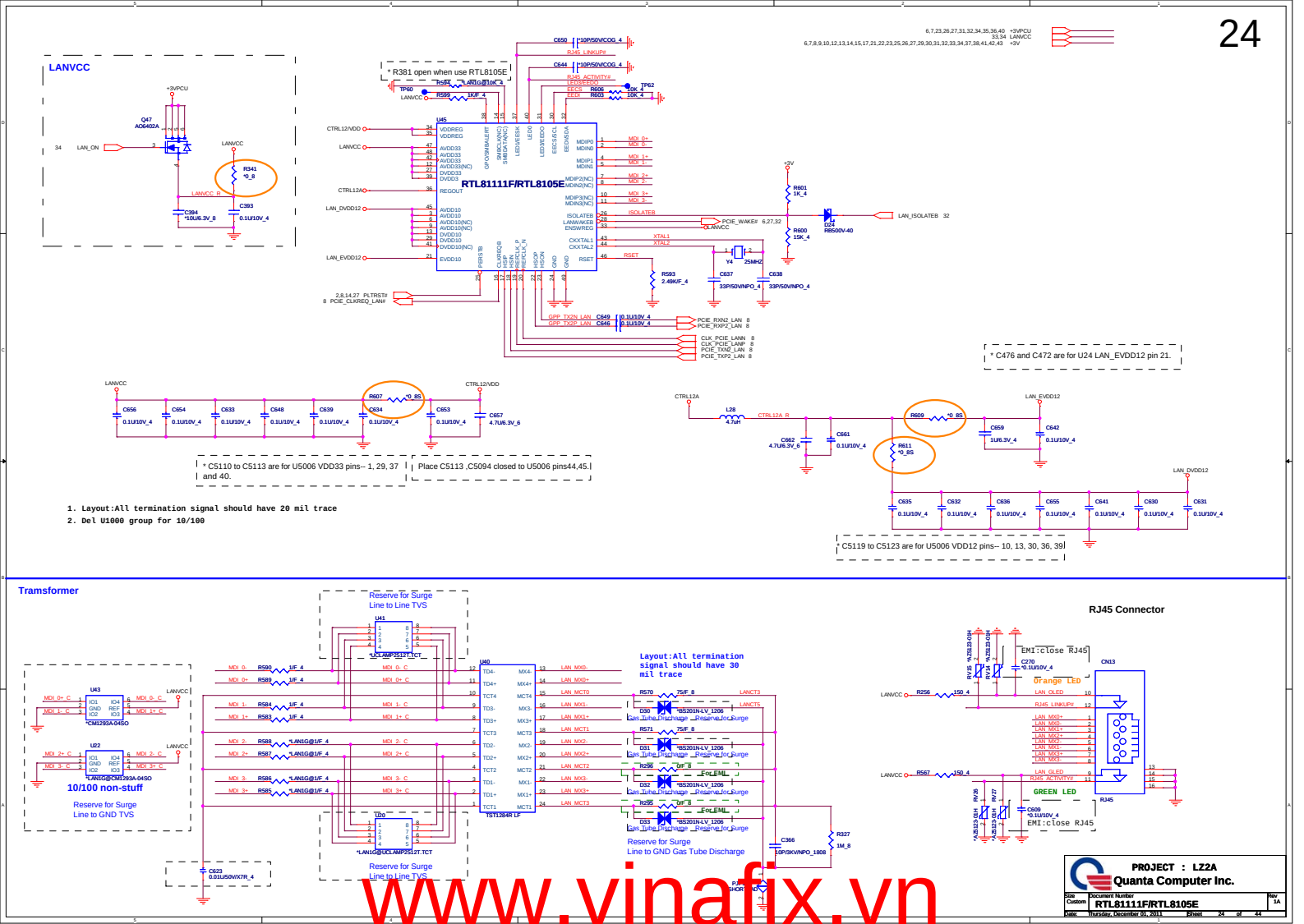
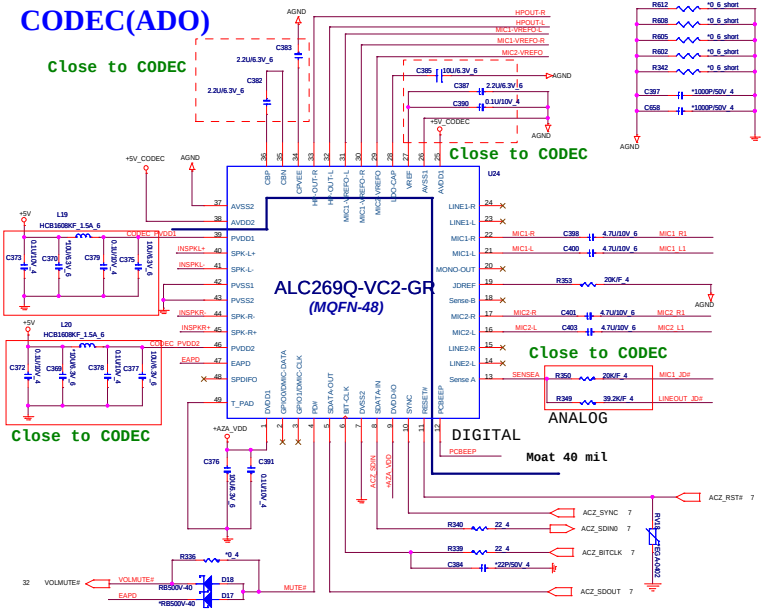
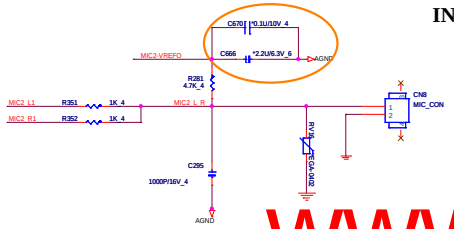


CODEC(ADO)



INTERNAL MIC



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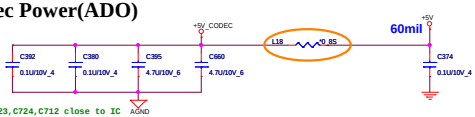
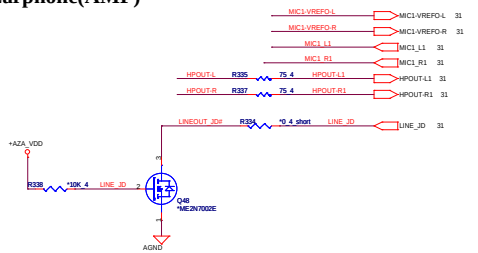
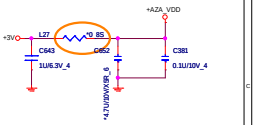


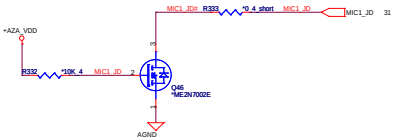
Earphone(AMP)



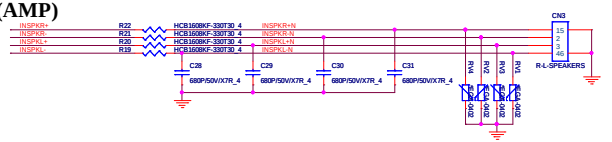
HDA Power(ADO)



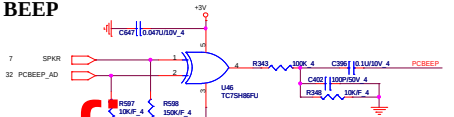
System MIC(AMP)



Speaker(AMP)



PC BEEP



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Quanta Computer Inc.
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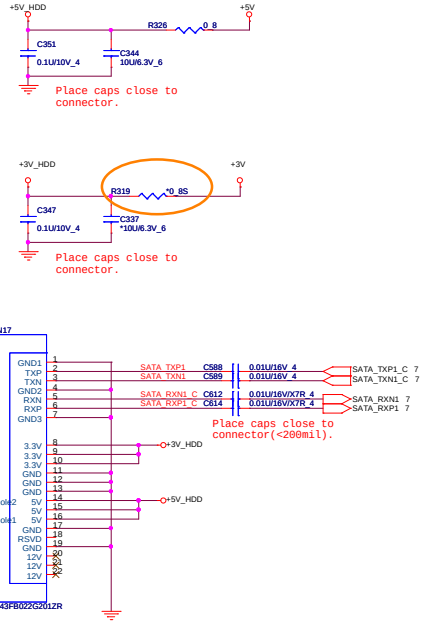
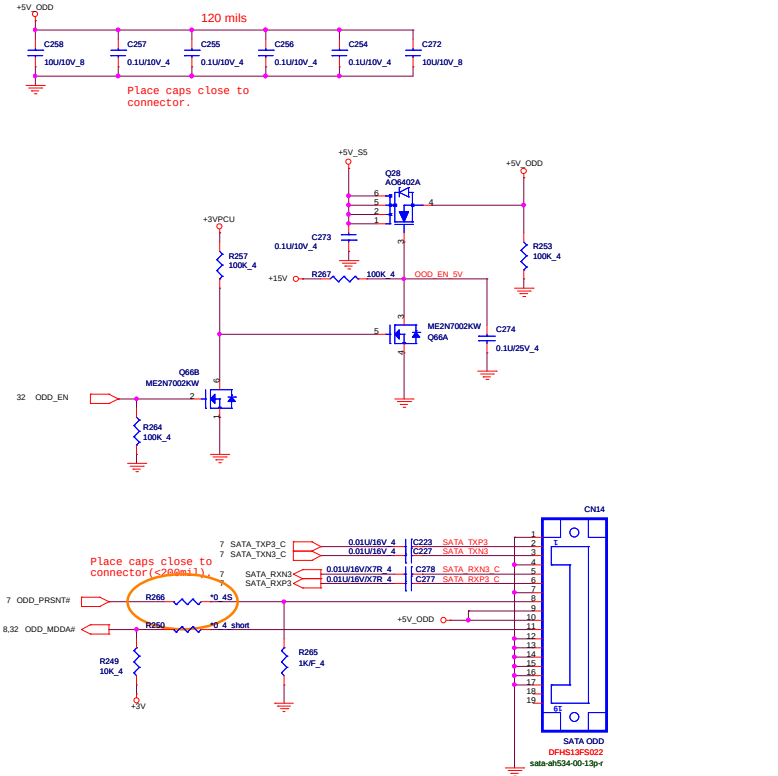
SATA HDD Connector.



SATA ODD Connector.

7,10,21,22,25,29,30,33,34 +5V
6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43 +3V
10,34,35,36,37,38,39,40,41,42,43 +5VPCU
6,7,23,24,27,31,32,34,35,36,40 +3VPCU



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Quanta Computer Inc.		
Size: Custom	Document Number: SATA HDD/CD-ROM	Rev: 1A
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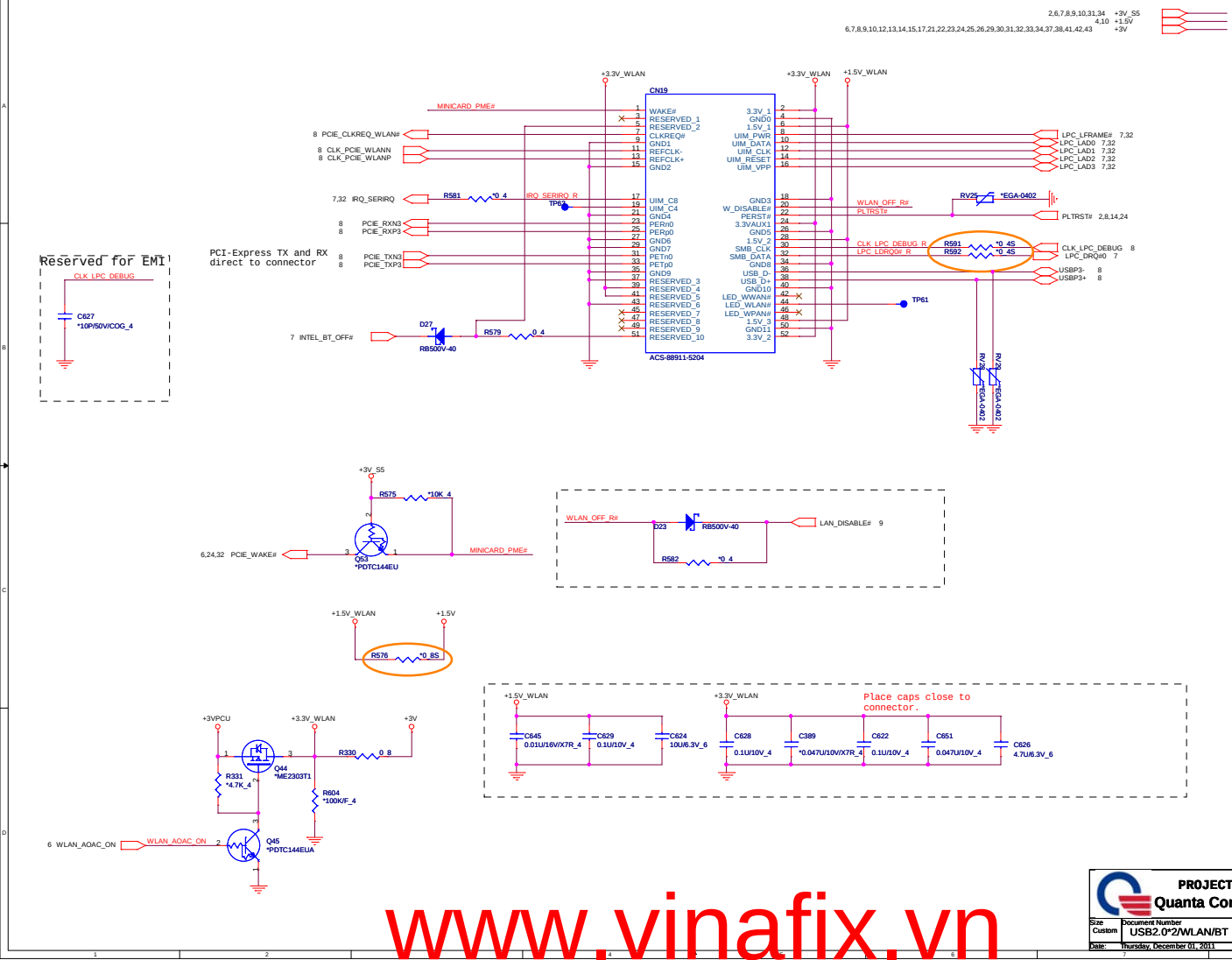

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Quanta Computer Inc.		
Size: Custom	Document Number: USB2.0*2/WLAN/BT	Rev: 1A
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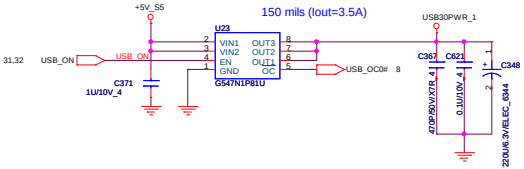
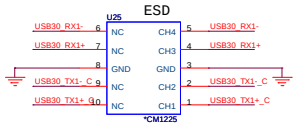
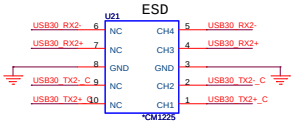
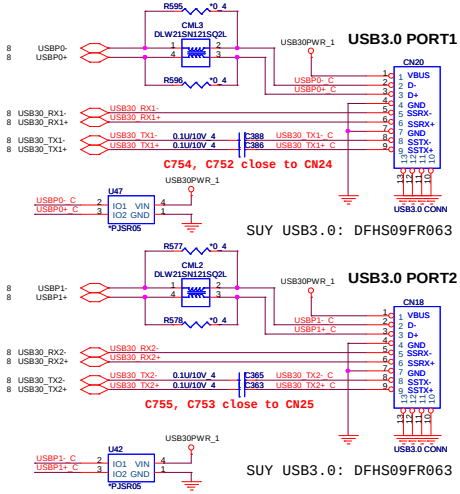
USB3.0*2

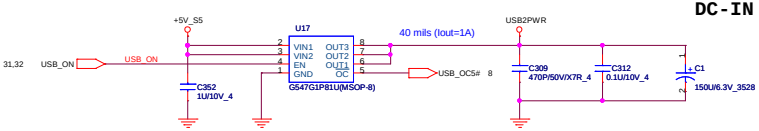


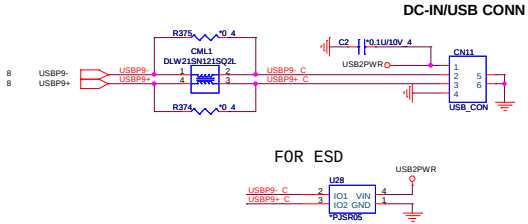






USB2.0*1





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Quanta Computer Inc.			
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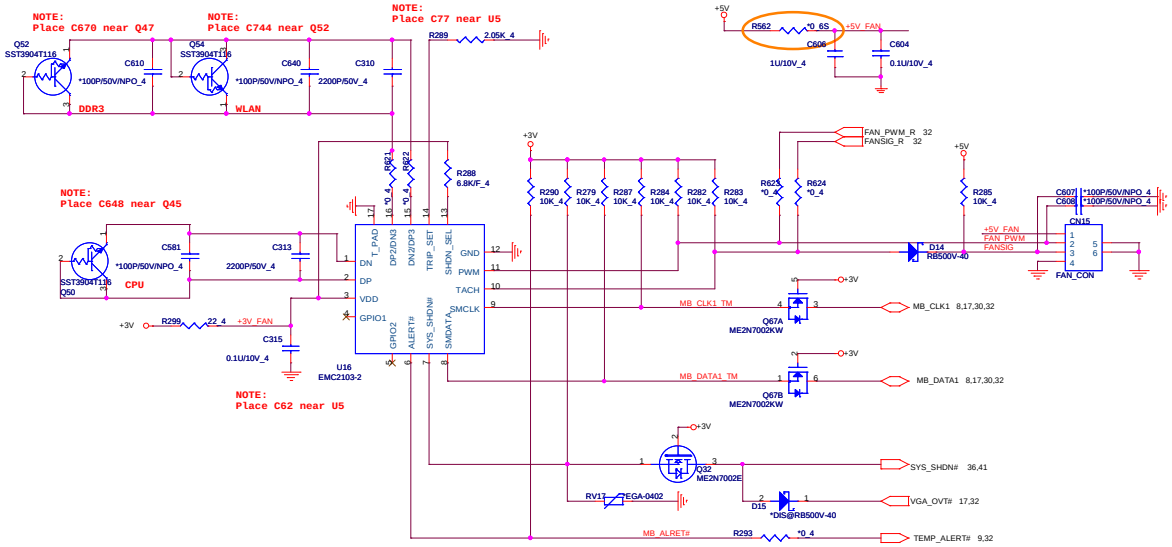
FAN CONTROL



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Quanta Computer Inc.		
Size: Custom	Document Number: FAN /THERMAL	Rev: 1A
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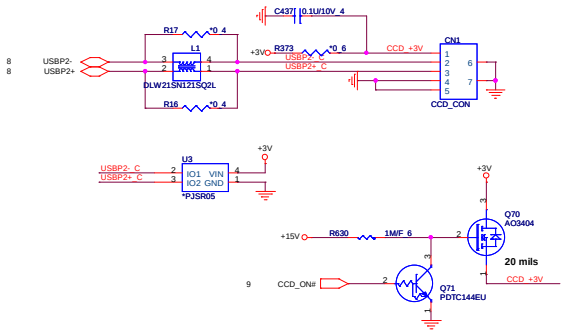
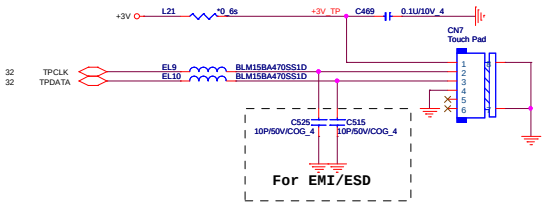
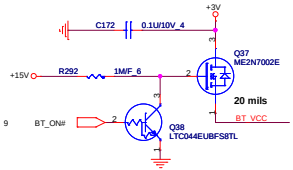
CCD BOARD

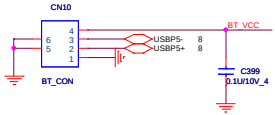


Touch pad

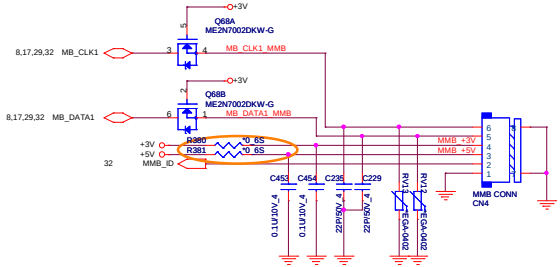


BLUETOOTH





MMB



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Quanta Computer Inc.		
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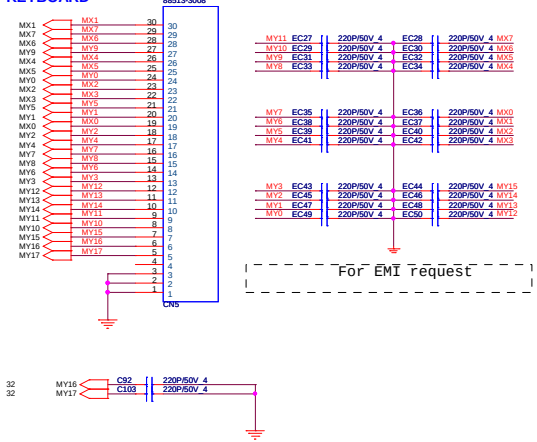
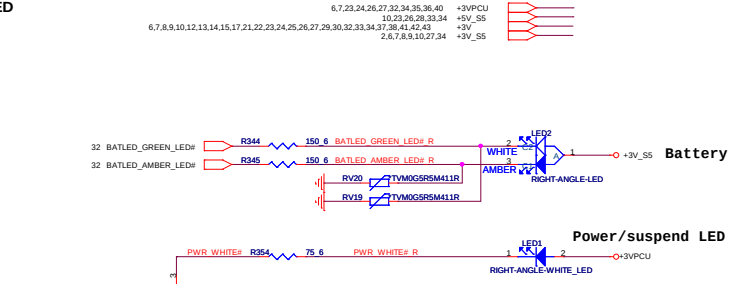
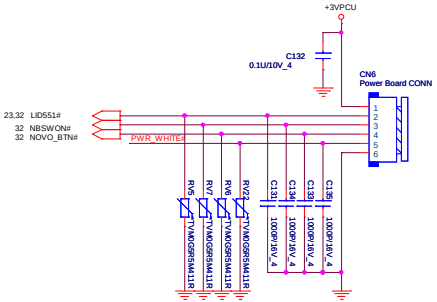
KEYBOARD



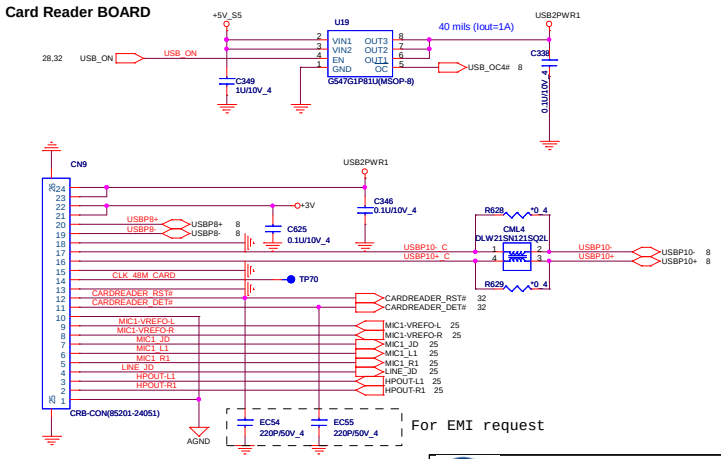
LED



POWER BOARD



Card Reader BOARD



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Quanta Computer Inc.	
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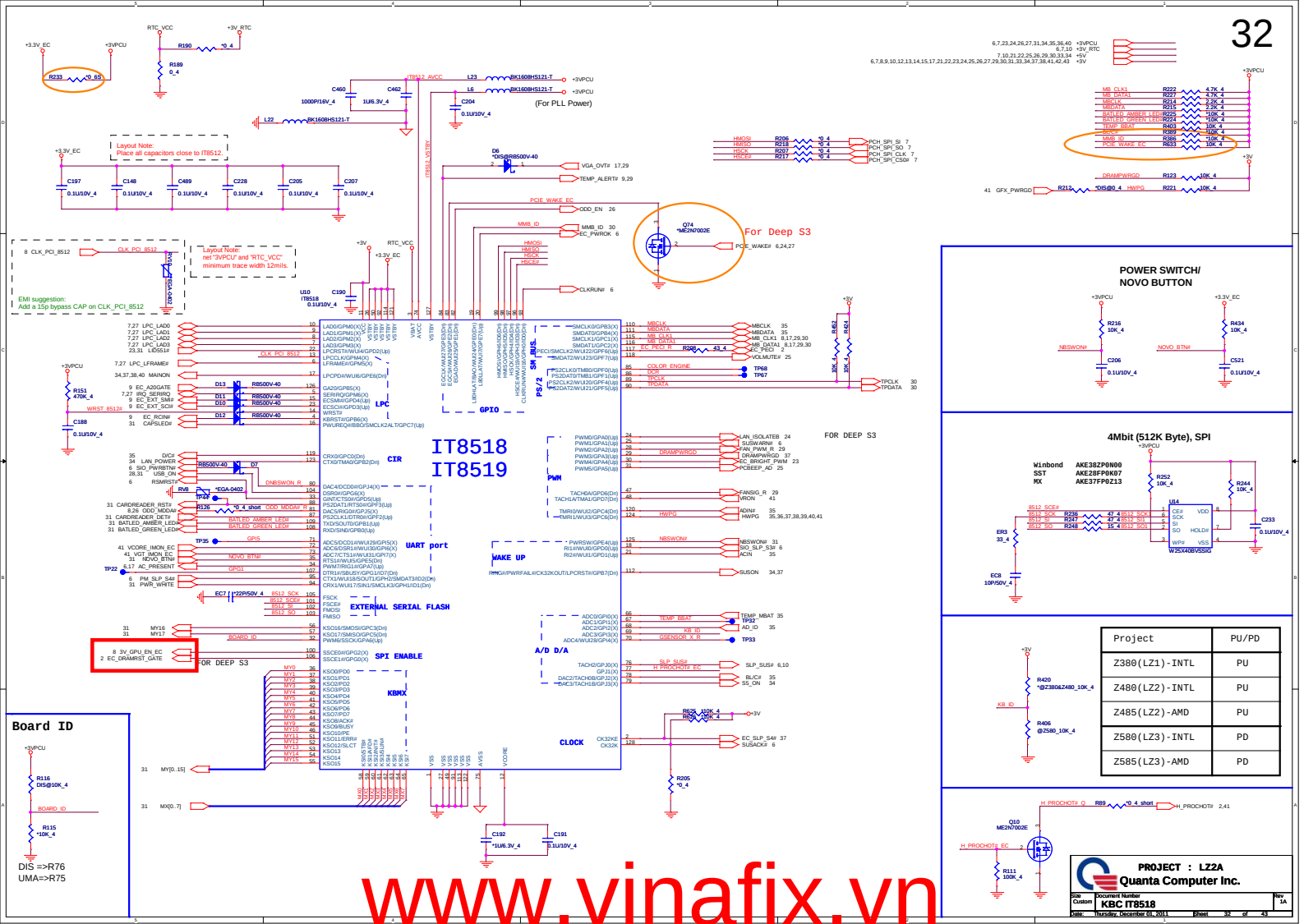
IT8518
IT8519
LPC
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
A/D D/A
CLOCK
KBMX
SPI ENABLE
EXTERNAL SERIAL FLASH
CIR
FOR DEEP S3
For Deep S3
(For PLL Power)
Board ID
DIS =>R76
UMA=>R75
POWER SWITCH/
NOVO BUTTON
4Mbit (512K Byte), SPI
Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13
Project PU/PD
Z380(LZ1)-INTL PU
Z480(LZ2)-INTL PU
Z485(LZ2)-AMD PU
Z580(LZ3)-INTL PD
Z585(LZ3)-AMD PD
PROJECT : LZ2A
Quanta Computer Inc.
KBC IT8518
Thursday, December 01, 2011
www.vinafix.vn

Screw for ME

SPAD1 *SPAD-Z480-1
SPAD3 *SPAD-Z480-1
SPAD4 *SPAD-Z480-2
SPAD2 *SPAD-Z480-2

VGA
HOLE12 DIS@H-TC5_5BC4I3D3P2
HOLE13 H-TC5_5BC4I3D3P2

SMT NUT H=4/7mm

CPU BKT

HOLE8 *HG-TC276BC315D106P2
HOLE10 *HG-TC276BC315D106P2
HOLE15 *HG-TIC248BC256D106P2
HOLE6 *HG-TC256BC315D106P2
HOLE11 *HG-TC276BC315D106P2
HOLE4 *H-C86D86N
HOLE7 *C142D102N
HOLE3 *H-TC217BC256D118P2
HOLE14 *H-TC7IC3_7BC8D2_7P2
HOLE9 *H-C87D87N
HOLE5 *H-O316X276iD91P2
HOLE2 *H-O316X276iD91P2
HOLE1 *H-TC6_3IC3_7BC8D2_7P2

33

For ESD

+0.85V SC23 SC24 *0.1U/10V_4
+1.8V
+1.05V_GFX_PCIE SC31 SC32 *0.1U/10V_4
+1.05V_PCH
+0.85V SC11 SC13 SC12 *0.1U/10V_4
+1.5V_CPU SC27 SC26 *0.1U/10V_4
+5V_S5 SC42 *0.1U/10V_4
+5V_S5 SC41 *0.1U/10V_4
+1.5V_SUS SC29 SC28 *0.1U/10V_4
+1.5V_CPU
+1.5V_SUS SC40 SC39 0.1U/25V_4
VIN
+3V SC33 SC30 0.1U/10V_4
+5V
+VCC_CORE SC9 SC46 0.1U/25V_4
VIN
+VCC_GFX SC15 SC18 *0.1U/10V_4
+5V SC38 SC25 SC37 0.1U/10V_4
+1.05V_GFX_PCIE SC4 *0.1U/10V_4
GFX_CORE
+VCC_GFX SC17 SC16 SC14 *0.1U/10V_4
+1.05V_PCH SC20 SC19 SC21 *0.1U/10V_4
+1.05V_PCH SC49 SC22 SC50 SC47 SC48 *0.1U/10V_4
+1.05V_GFX_PCIE SC6 SC5 *0.1U/10V_4
+VCC_CORE SC8 SC10 *0.1U/10V_4
+1.5V_GPU SC2 SC43 SC3 *0.1U/10V_4
+1.5V_GPU SC7 SC45 *0.1U/10V_4
+1.5V_GPU SC44 SC1 *0.1U/10V_4
+1.5V_SUS SC35 SC34 SC36 *0.1U/10V_4

For EMI

VIN EC6 EC20 EC12 EC25 EC1 EC18 EC2 EC21 EC5 EC3 EC16 0.1U/25V_4
LANVCC EC11 0.1U/10V_4
VBATT EC22 0.1U/25V_4
+1.5V_SUS EC2 3.9p/16V/NPO_4
+1.5V_SUS EC1 3.9p/16V/NPO_4
+1.5V_WLAN EC5 47P/50V/NPO_4
+3.3V_WLAN EC3 47P/50V/NPO_4
+5V EC51 EC52 0.1U/10V_4 *0.1U/10V_4

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Quanta Computer Inc.
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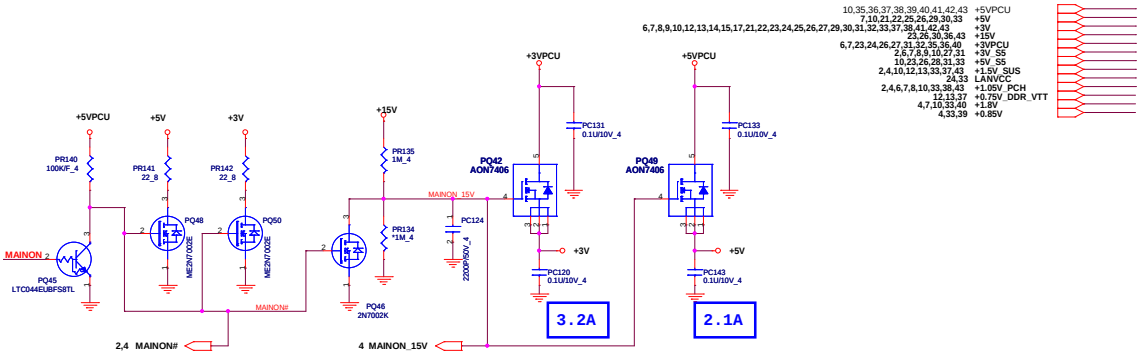
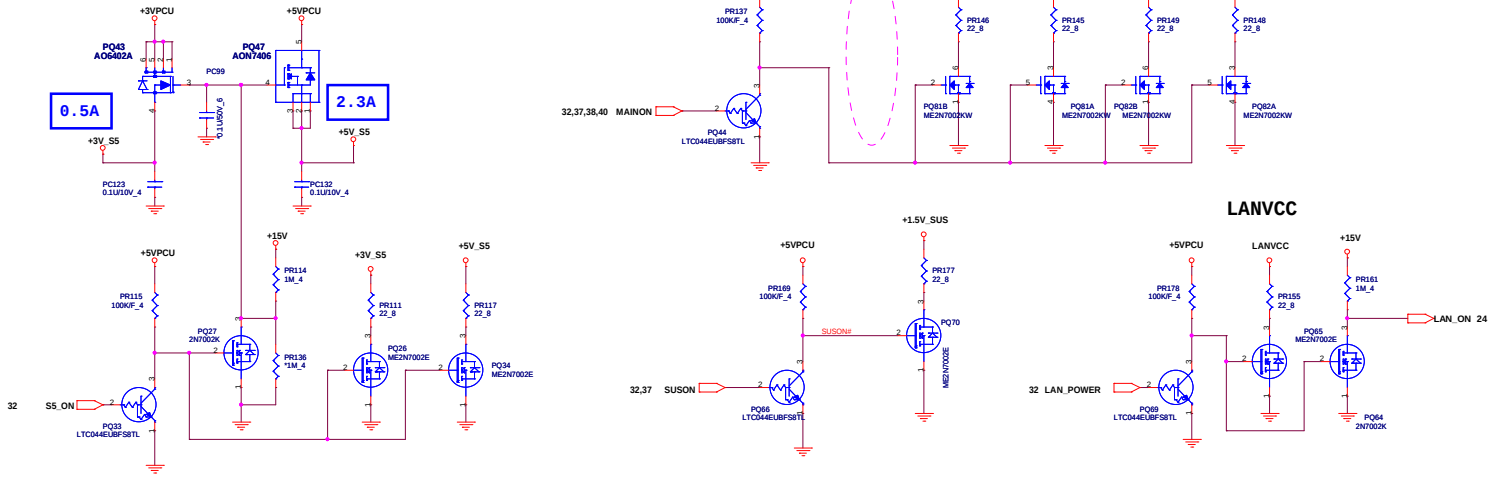
DISCHARGE

+3V, +5V



3V_S5, 5V_S5



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Quanta Computer Inc.
Size | Document Number: Discharge | Rev
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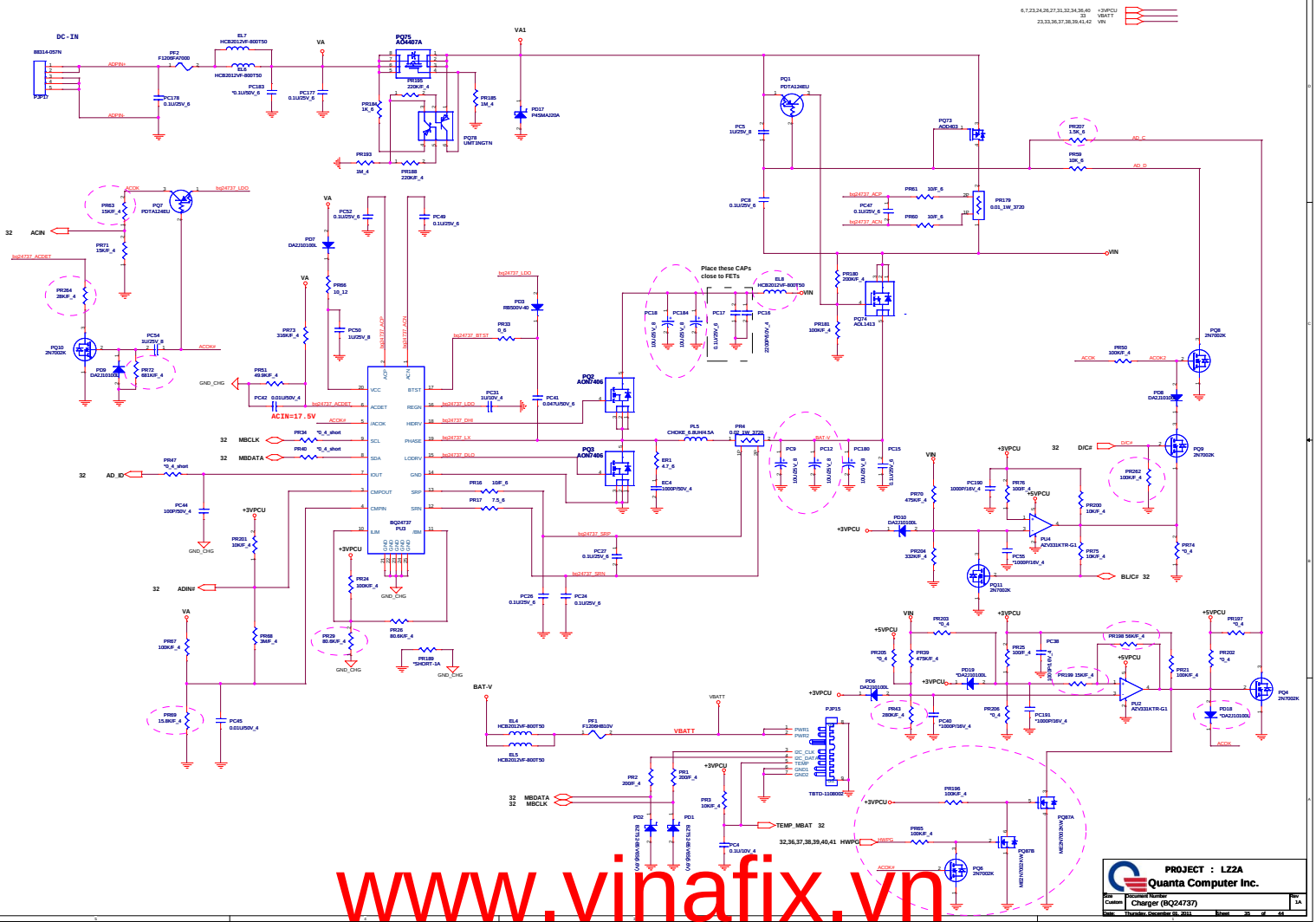

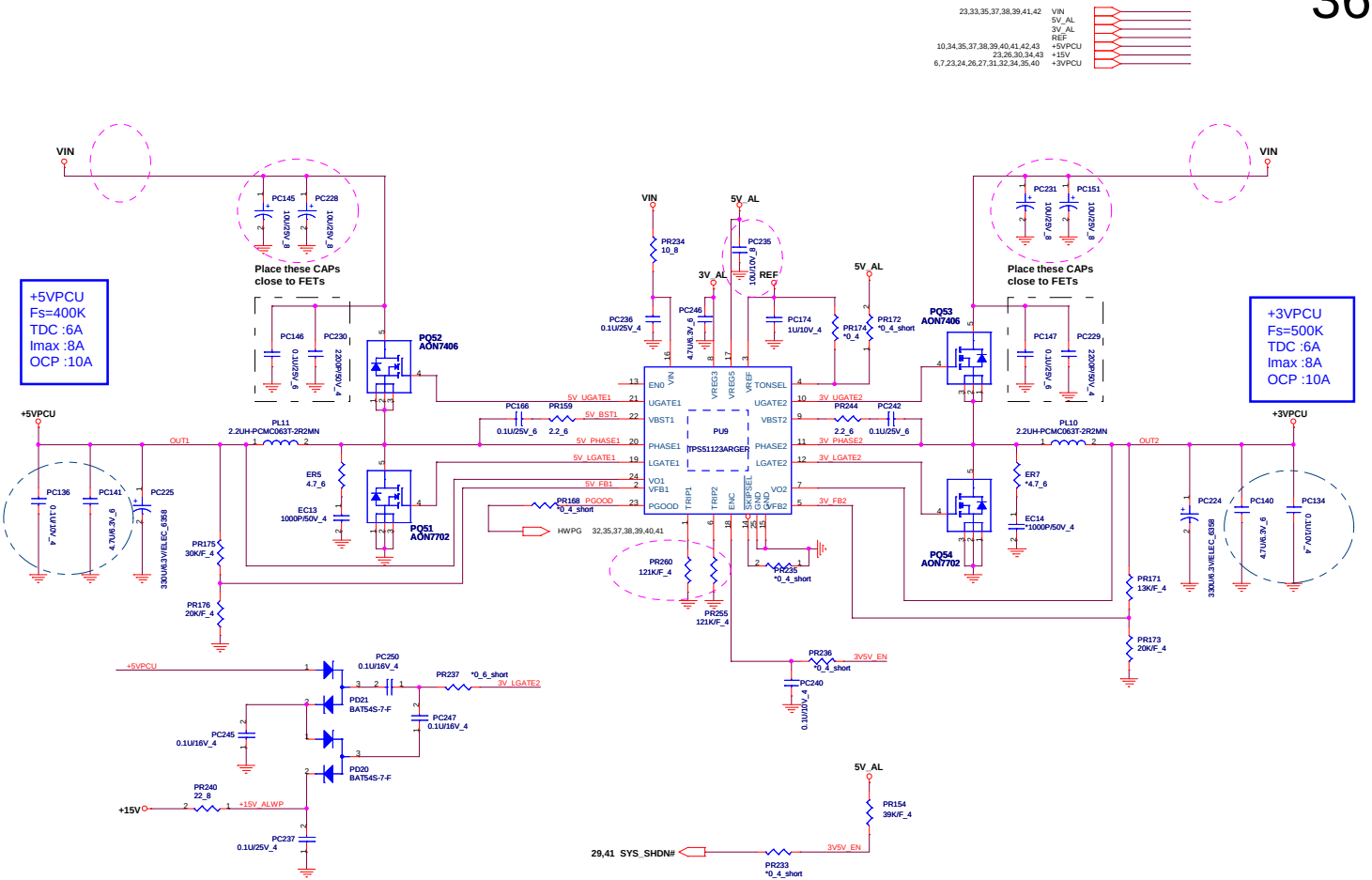

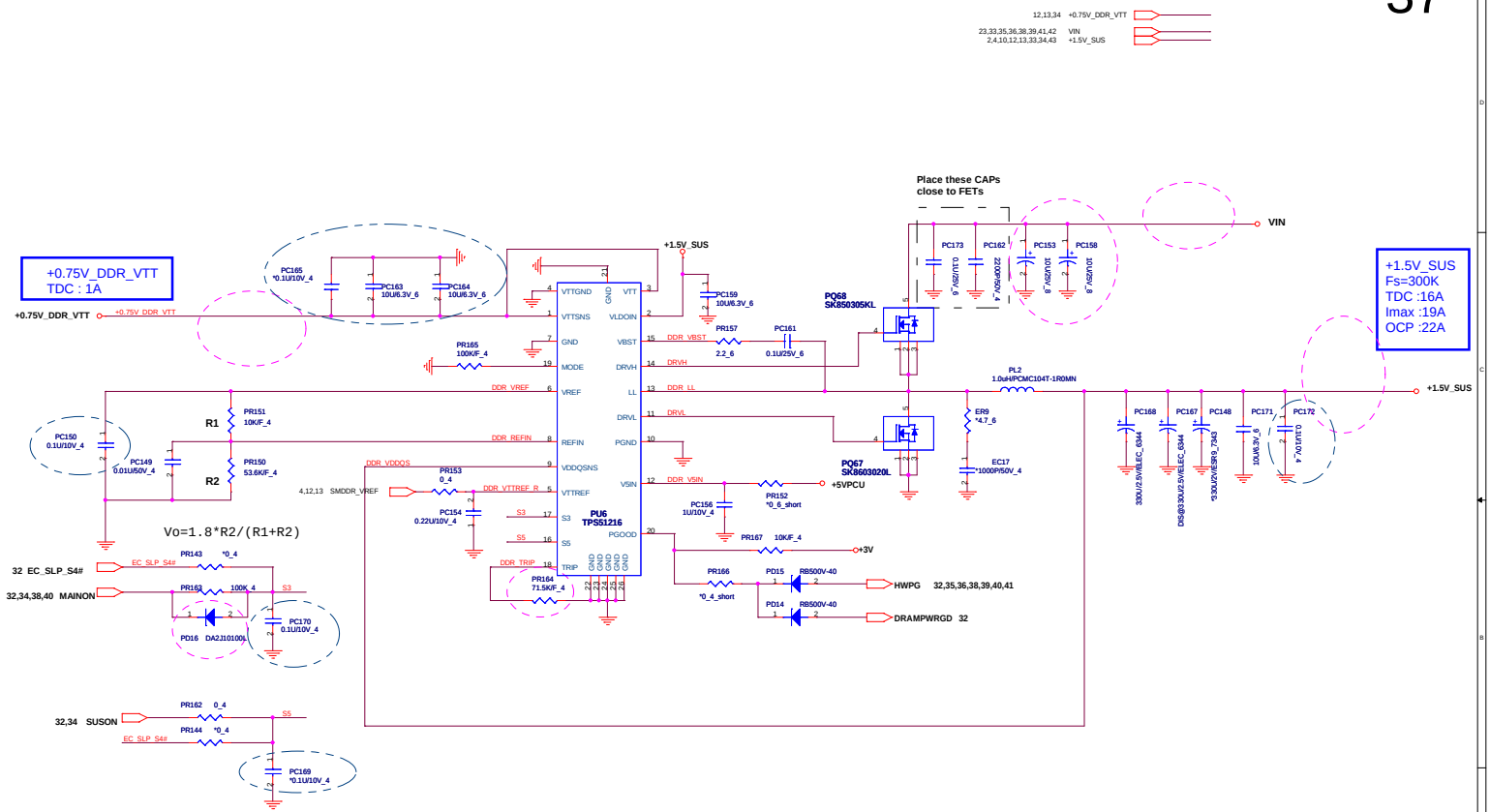

PROJECT : LZ2A
Quanta Computer Inc.
Size | Document Number: DDR3/0.75V (TPS51216) | Rev
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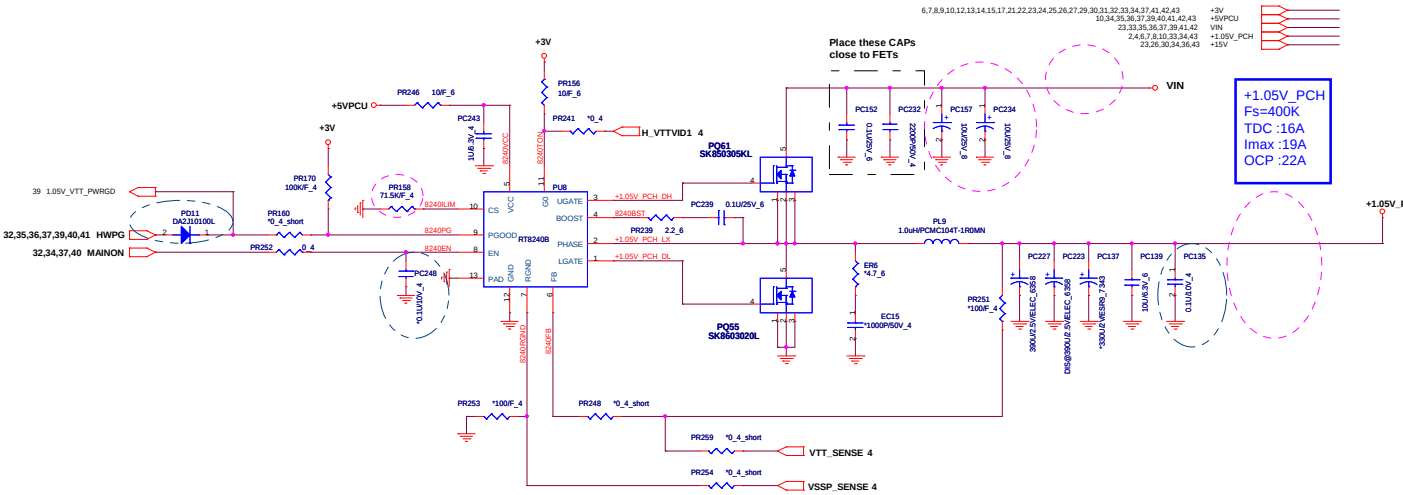

PROJECT : LZ2A
Quanta Computer Inc.

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	+1.05V_PCH	
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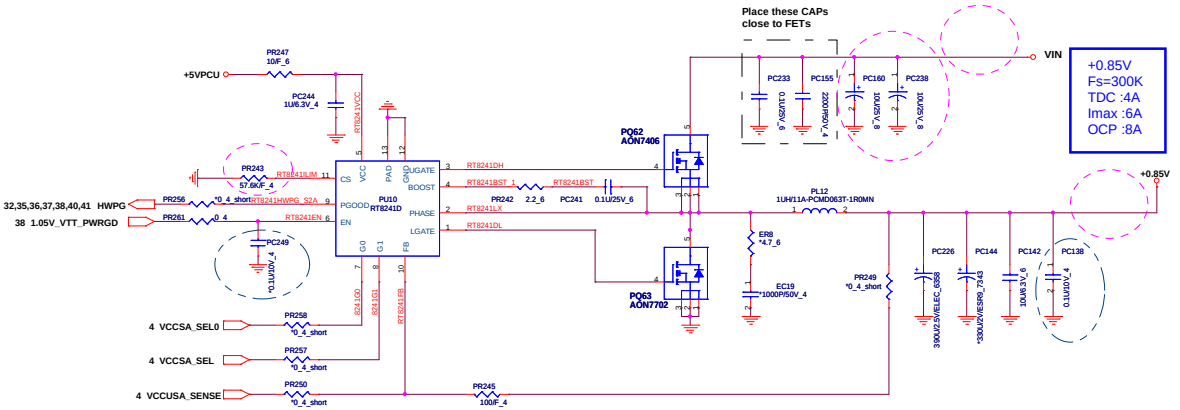
10,34,35,36,37,38,40,41,42,43 +5VPCU
23,33,35,36,37,38,41,42 VIN
4,33,34 +0.85V



G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

PROJECT : LZ2A
Quanta Computer Inc.
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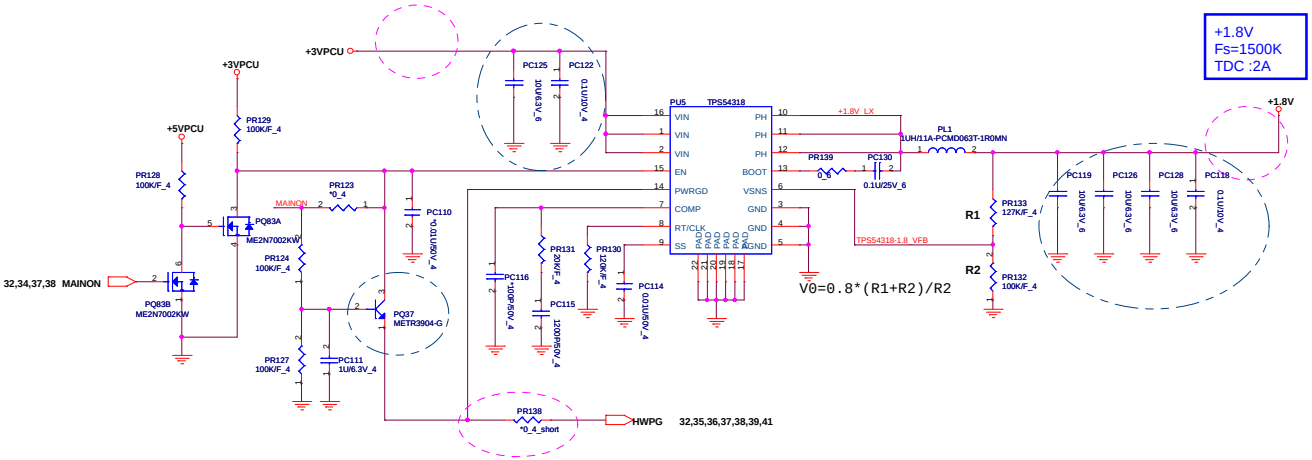
10,34,35,36,37,38,39,41,42,43 +5VPCU
6,7,23,24,26,27,31,32,34,35,36 +3VPCU
4,7,10,33,34 +1.8V



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	1.8V (TPS54318)	
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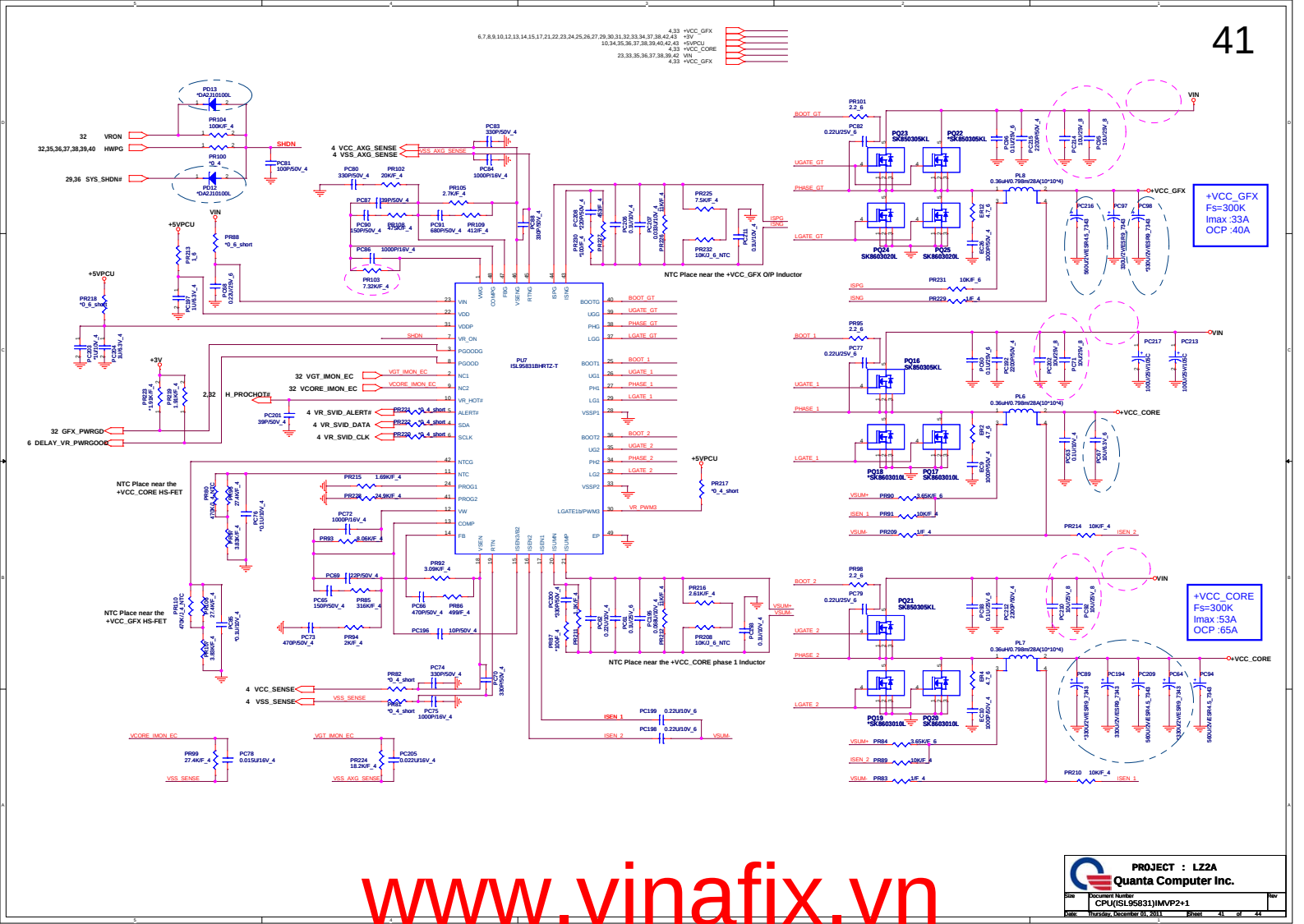

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CPU(ISL95831)IMVP2+1
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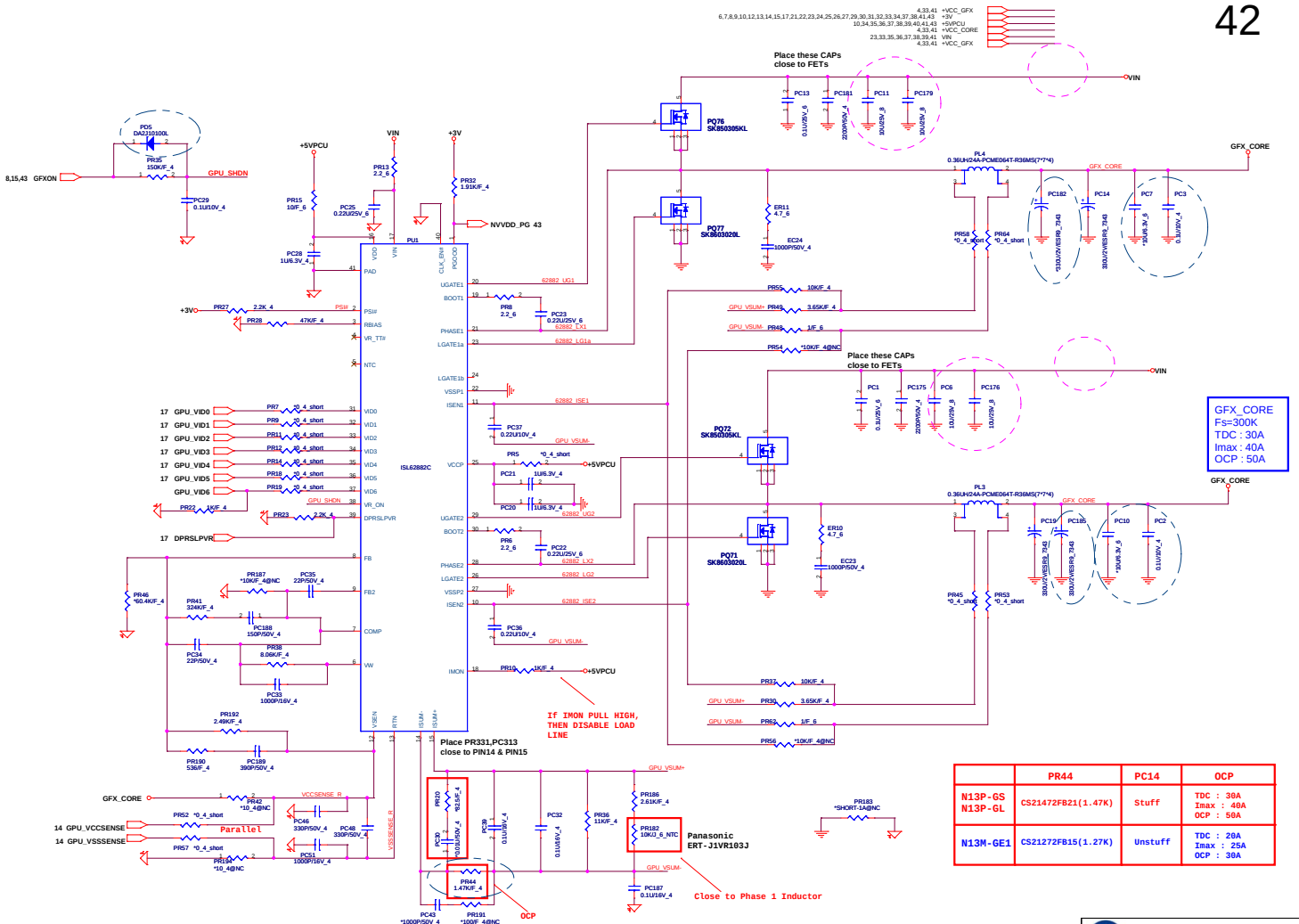

	PR44	PC14	OCP
N13P-GS N13P-GL	CS21472FB21(1.47K)	Stuff	TDC : 30A Imax : 40A OCP : 50A
N13M-GE1	CS21272FB15(1.27K)	Unstuff	TDC : 20A Imax : 25A OCP : 30A

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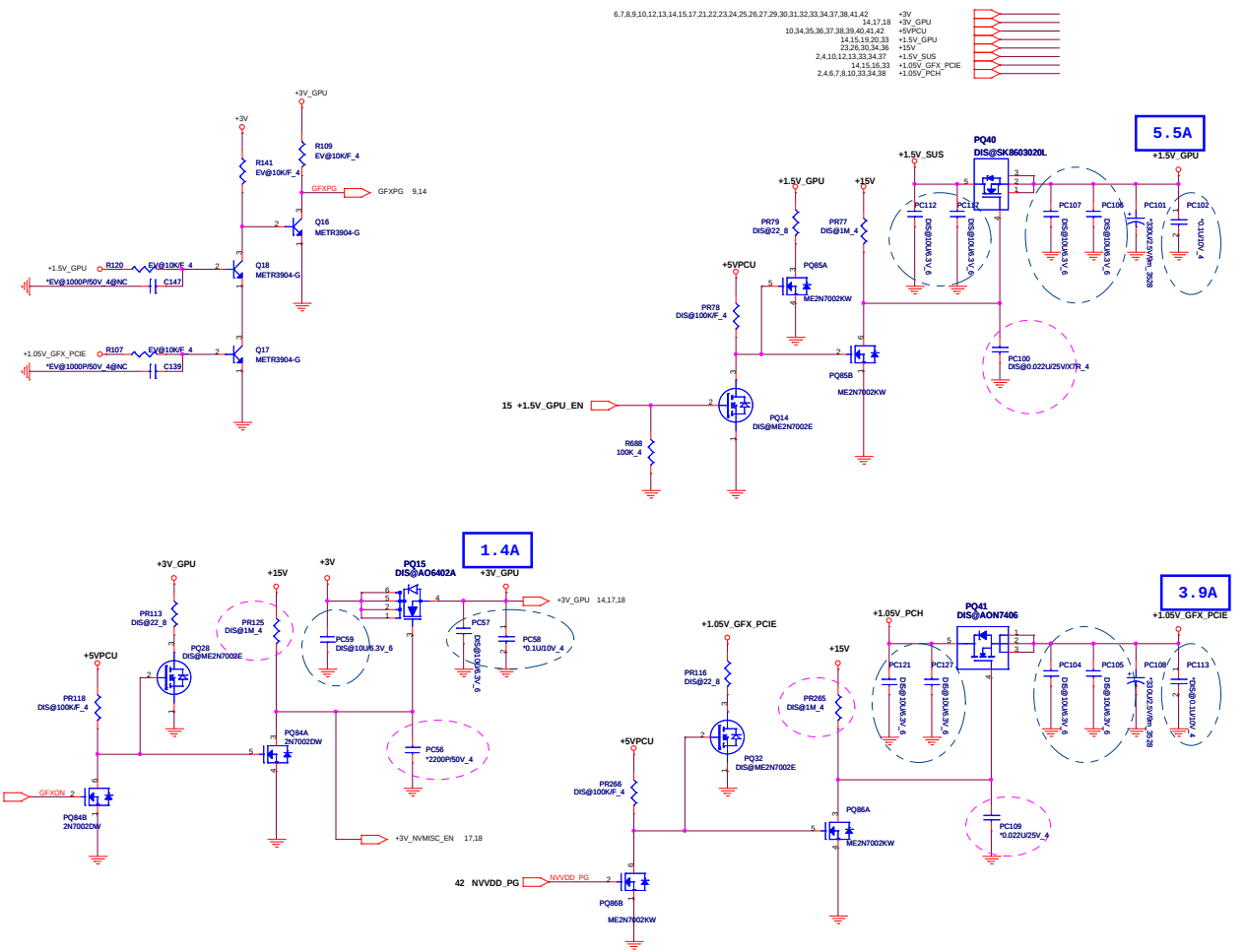

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	GPU	
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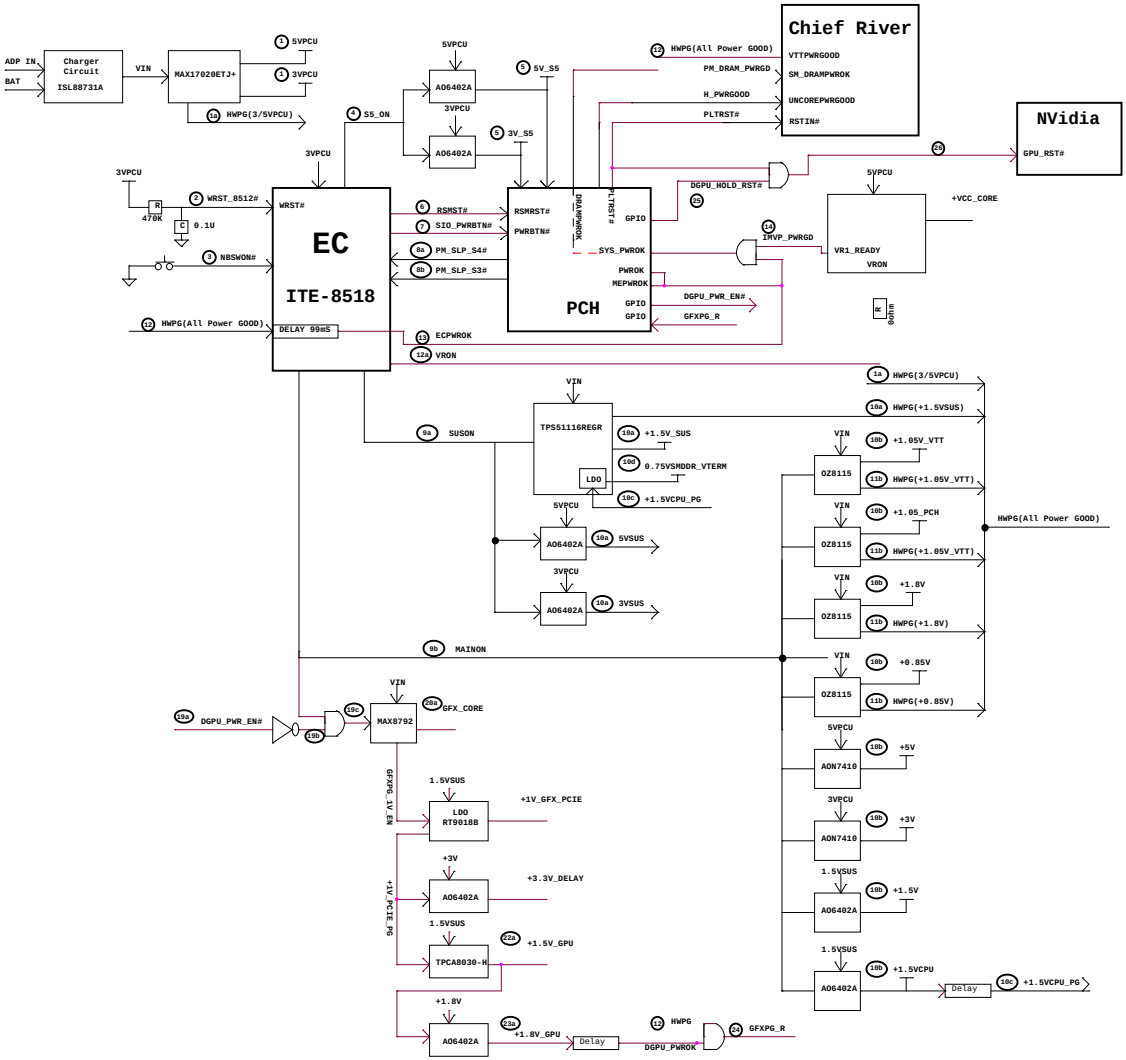

PROJECT LZ1
Quanta Computer Inc.
Power Sequence Diagram