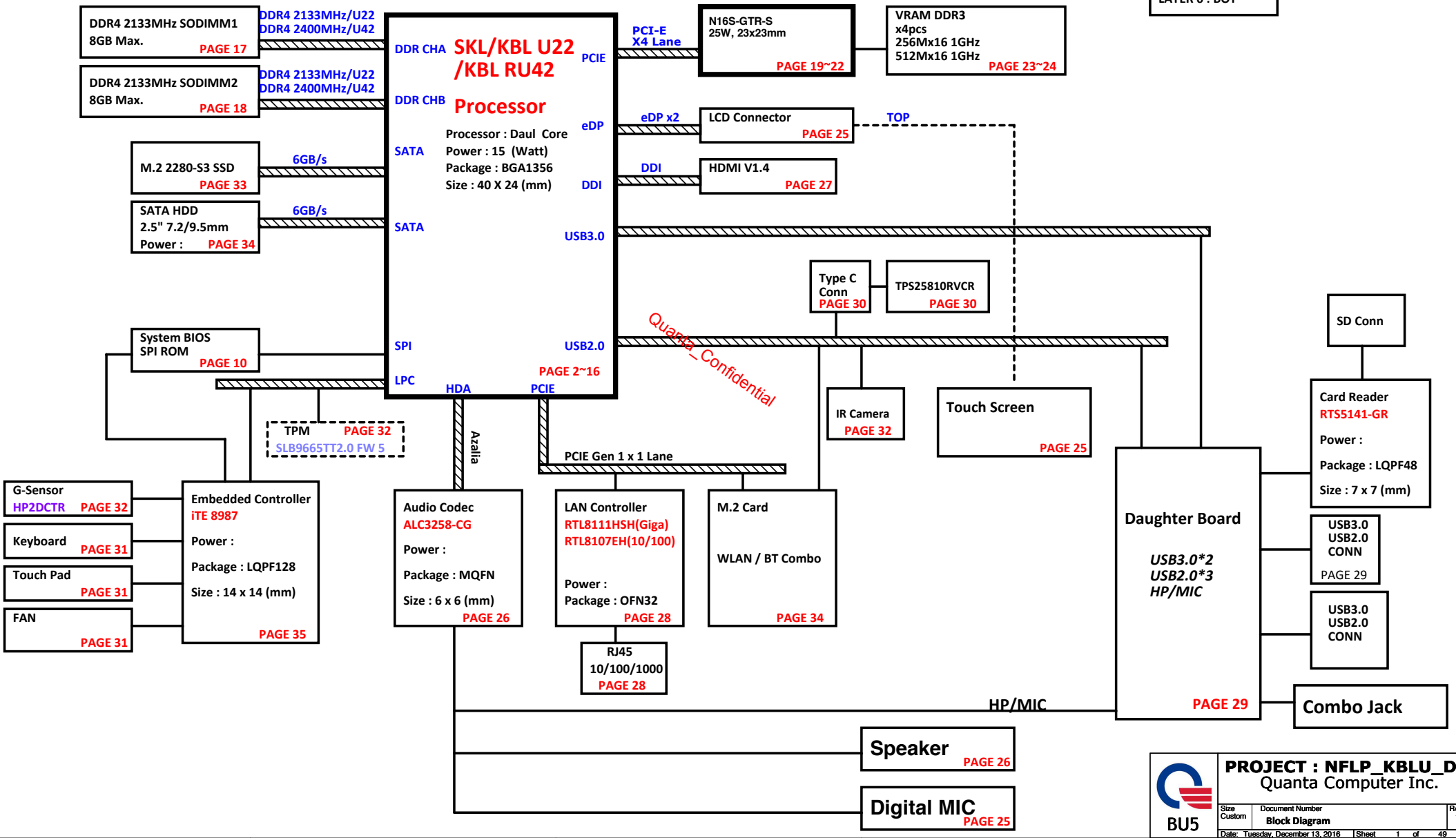
NFL_1SPD DIS (14/15")
Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT



PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

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Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, December 13, 2016 Sheet 1 of 49

+3V 4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49
+1.0V 4,6,35,40
+VCCSTPLL 4,5,6,9,40,41

HDMI

Need apply PN

Justsurport FHD 1920x1080

U1A — SKL_ULT ?

27 IN_D2# → IN_D2# → E55 DDI1_TXN[0]
27 IN_D2 → IN_D2 → F55 DDI1_TXP[0]
27 IN_D1# → IN_D1# → E58 DDI1_TXN[1]
27 IN_D1 → IN_D1 → F58 DDI1_TXP[1]
27 IN_D0# → IN_D0# → F53 DDI1_TXN[2]
27 IN_D0 → IN_D0 → G53 DDI1_TXP[2]
27 IN_CLK# → IN_CLK# → F56 DDI1_TXN[3]
27 IN_CLK → IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 25
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 25
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 25
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 25
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN 25
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP 25
EDP_DISP_UTIL B52 → EDP_DISP_UTIL → TP1

DISPLAY SIDEBANDS

DDI1_AUXN G50
DDI1_AUXP C50
DDI2_AUXN F48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E18/DDPB_CTRLCLK L13 ← 27 SDVO_CLK
GPP_E19/DDPB_CTRLDATA L12 ← 27 SDVO_DATA

GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N8
TP2 1 DDPC_CTRLDATA

GPP_E22/DDPD_CTRLCLK N11
GPP_E23/DDPD_CTRLDATA N12
TP3 1 DDPD_CTRLDATA

+VCCIO — R3 24.9_1%_4 — EDP_RCOMP E52 — EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 → HDMI_HPD_CON → HDMI_HPD_CON 27
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L5
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → ULT_EDP_HPD → ULT_EDP_HPD 25

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_LVDS_BLON 25
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM 25
EDP_VDDEN U13 → PCH_DISP_ON → PCH_DISP_ON 25

*SKL_ULT
REV = 1
1 OF 20 ?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R1 *10K/F_4
ULT_EDP_HPD
R2 100K_4

35,41 H_PROCHOT# → R4 499/F_4 → 35 EC_PECI / 35 PM_THRMTRIP#

U1D — SKL_ULT ? — Need apply PN

CATERR# D63 ← EC_PECI A54 ← PROCHOT# C63 ← PM_THRMTRIP# A63
SKTOCC# A65

CPU MISC

TP127 1 XDP_BPM0 C55
TP128 1 XDP_BPM1 D55
BPM#[0] BPM#[1] BPM#[2] BPM#[3] B54 C56

TP5 1 CPU_GP2 BA5
TP6 1 CPU_GP3 AY5
A6 A7
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP AT16
R11 49.9/F_4 PCH_OPI_RCOMP AU16
R12 49.9/F_4 EDRAM_OPIO_RCOMP H66
R14 49.9/F_4 EOPIO_RCOMP H65
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0
PROC_TDI D60 XDP_TDI_CPU 1 → TP999
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU 1 → TP998
PROC_TRST# B59 PROC_TRST#

PCH_JTAG_TCK B56 JTAG_TCK_PCH
PCH_JTAG_TDI D59 JTAG_TDI_PCH
PCH_JTAG_TDO A56 JTAG_TDO_PCH
PCH_JTAG_TMS C59 JTAG_TMS_PCH
PCH_TRST# C61 XDP_TRST#_CPU
JTAGX A59 JTAGX_PCH

XDP_TRST#_CPU R863 0_4 PROC_TRST#

*SKL_ULT
REV = 1
4 OF 20 ?

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+VCCSTPLL
R6 *49.9/F_4 CATERR#

+1.0V
R9 *0_4/S
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

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PROJECT : NFLP_KBLU_DR
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Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A
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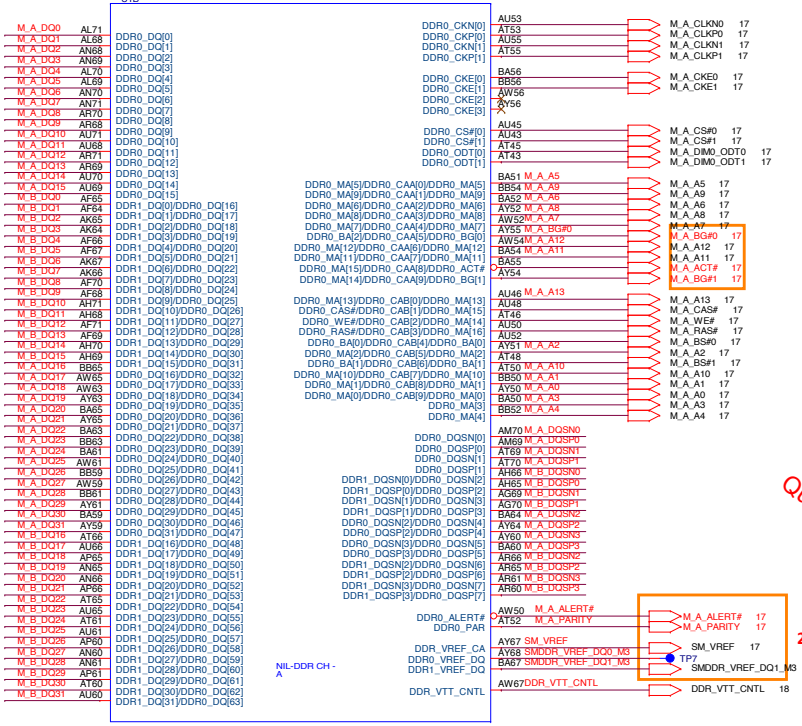
SkyLake ULT Processor (DDR4)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

+1.2VSUS 6,17,18,38,40,46

Need apply PN

U1B SKL_ULT



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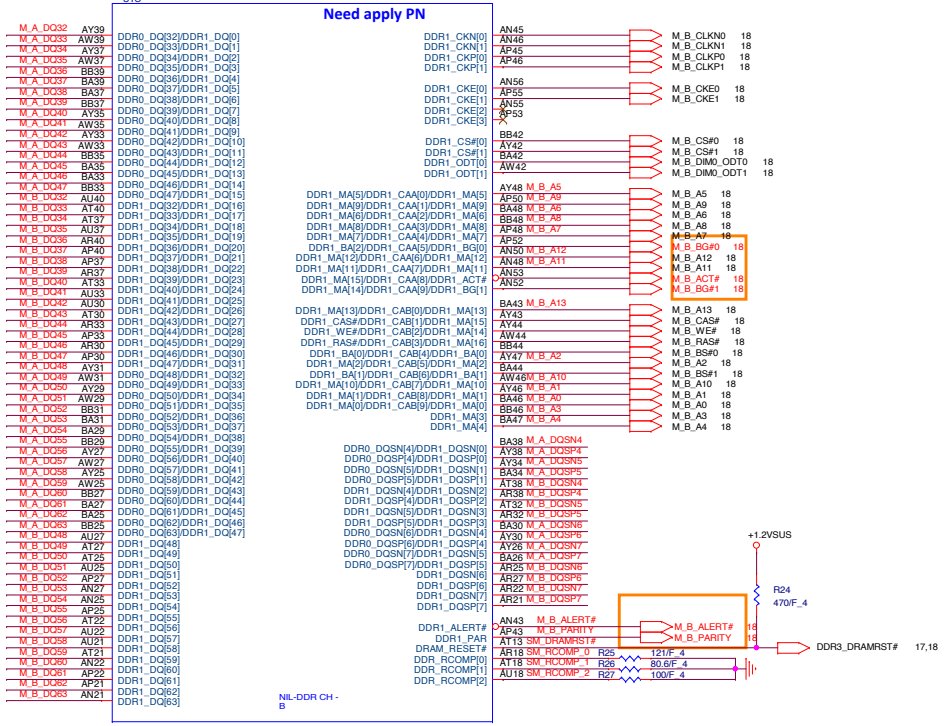
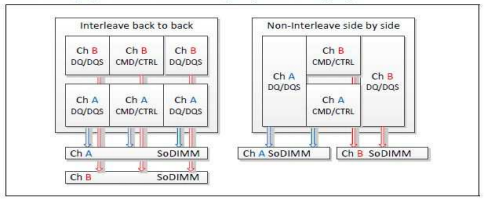
20mils width

U1C SKL_ULT

Need apply PN



Interleave (IL) and Non-Interleave (NIL) Modes Mapping



BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 -- SKYLAKE 2/15(DDR4 I/F)	1A

Date: Tuesday, December 13, 2016 Sheet 3 of 49

10,11,12,14,15,18 +3V_DEEP_SUS
2,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49 +3V
10,15,34,35,37,38,39,40,46,49 +3VS5
2,5,6,9,40,41 +VCCSTPLL
2,6,35,40 +1.0V
13,15,29,36,47 +BAT_RTC
13,15 +3V_RTC_2

U1K SKL_ULT ?

SYSTEM POWER MANAGEMENT

Need apply PN

35 RSMRST#
EC1 *220p/50V_4
R29 *10K_4 PROCPWRGD
C1 *0.1u/16V_4
35 EC_PWROK
SUSWARN# 0_4 R32
TP9020 1 *0_4 R34
TP411 1 *0_4 R33
28,34 PCIE_WAKE#
TP789 1 GPD7

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
H_VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DSWROK_EC_R BB20
SUSWARN# AR13
SUSACK# AP11
PCIE_WAKE# BB15
LAN_WAKE# AM15
AW17
GPD7 AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

*SKL_ULT
REV = 1
11 OF 20
?

GPP_B12/SLP_S0# AT11 PCH_SLP_S0_N 1 TP942 SUSB# 35
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16 1 TP941 SUSC# 35
SLP_SUS# AN15 SLP_SUS#_EC SLP_SUS#_EC 35
SLP_LAN# AW15
GPD9/SLP_WLAN# BB17 GPD9 1 TP8
GPD6/SLP_A# AN16 SLP_A# 1 TP940
GPD3/PWRBTN# BA15 DNBSWON# DNBSWON# 35
GPD1/ACPRESENT AY15 AC_PRESENT_EC AC_PRESENT_EC 35
GPD0/BATLOW# AU13 RF_OFF_PCH RF_OFF_PCH 34
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER# R
GPP_B11/EXT_PWR_GATE# AM10
GPP_B2/VRALERT# AM11 GPP_B2 1 TP9

Ra R36 1M_4 +BAT_RTC
R305 *1M_4 +3V_RTC_2
Rb

Modify 0922
Main BAT -->Ra
Coin BAT -->Rb (default)
1005 Change +3V_RTC to +BAT_RTC

PCH Pull-high/low(CLG)

+3V_DEEP_SUS
SUSWARN# R28 *10K_4
SUSACK# R30 *10K_4
RF_OFF_PCH R31 10K_4
+3VS5
PCIE_WAKE# R35 1K_4
AC_PRESENT_EC R37 *10K_4
LAN_WAKE# R38 *10K_4
+3V
SYS_RESET# R39 10K_4
RSMRST# R40 10K_4
DSWROK_EC R41 100K/F_4

For DS3 Sequence

For DS3 -->Ra
Non-DS3 -->Rb
RSMRST# R42 Rb *0_4
35 DSWROK_EC R46 0_4 DSWROK_EC_R
Ra

PLTRST#(CLG)

Check Rise/Fall time less than 100ns

PLTRST# 19,28,32,33,34,35
R52 100K/F_4

System PWR_OK(CLG)

SYS_PWROK R53 *0_4/S EC_PWROK
R54 10K/F_4

+1.0V +VCCSTPLL
R47 *1K_4
R48 *1K_4
Ra
35,37,38,39 HWPG D1 1 2 MEK500V-40 H_VCCST_PWRGD R50 60.4/F_4 H_VCCST_PWRGD
C3 *10P/50V_4

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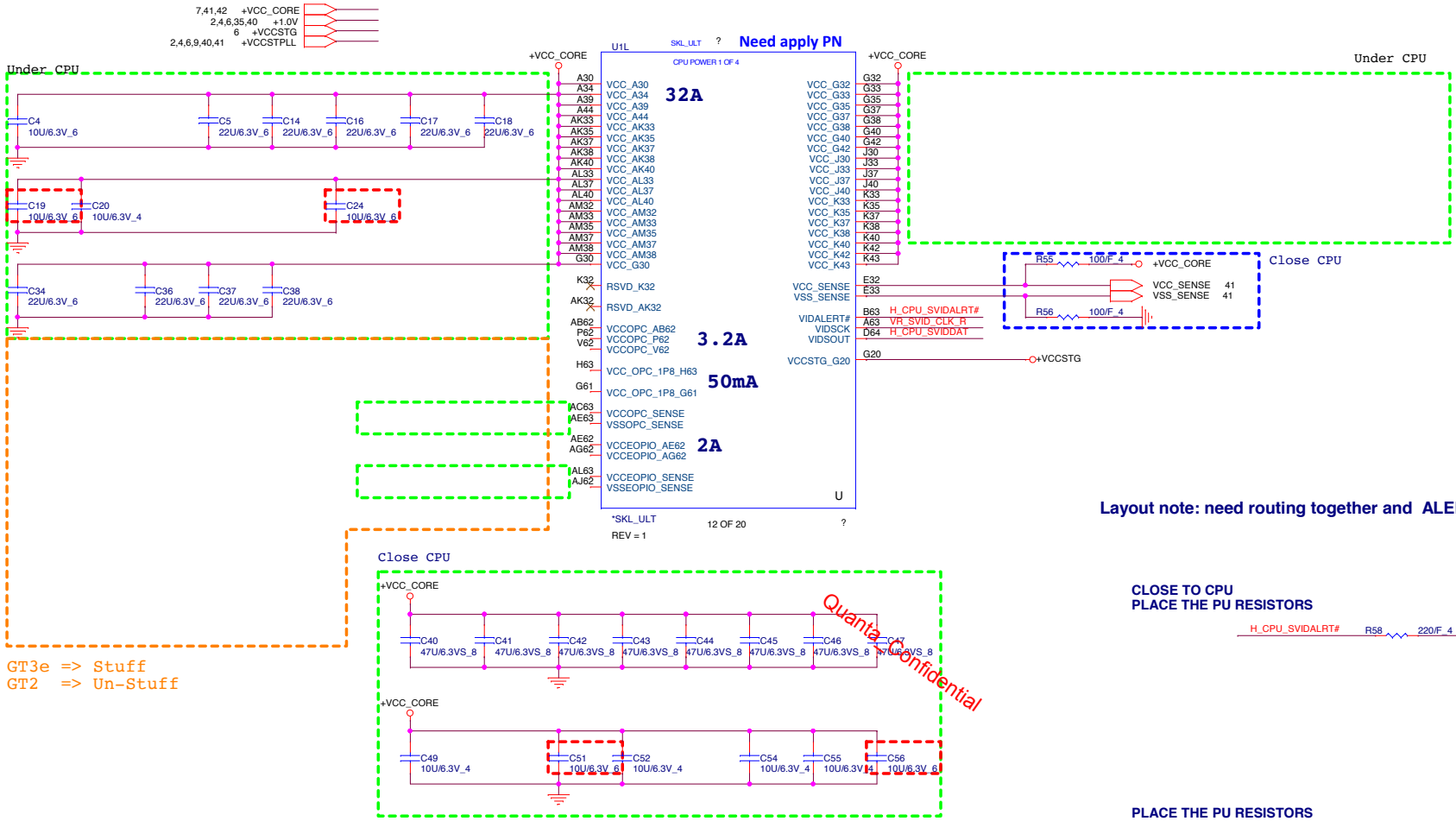
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+1.0V +5VS5 +3VS5
R43 15K/F_4
R44 100K_4
R45 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q1 2N7002K
R49 100K_4
+1.0V_PWRGD_G1 2 Q2 METR3904-G
C2 0.1U/16V_4
R51 100K_4

BU5

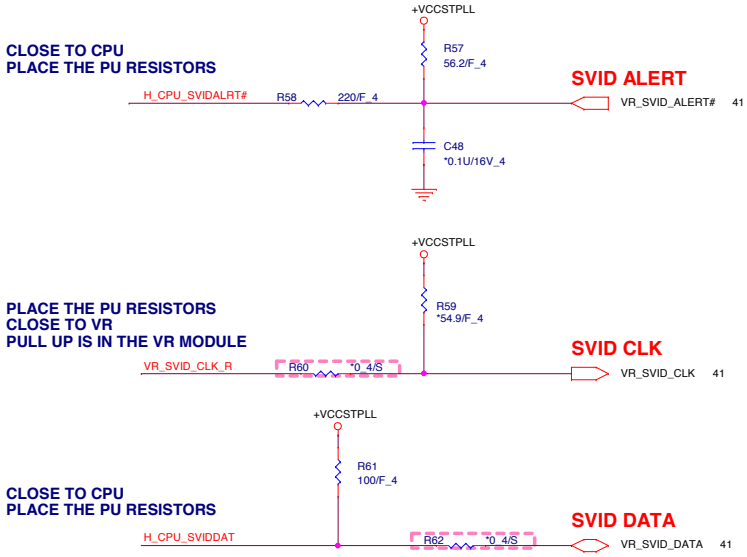
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYLAKE 3/15(PowerManger)	1A
Date: Tuesday, December 13, 2016	Sheet 4 of 49	



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Layout note: need routing together and ALERT need between CLK and DATA.



PROJECT :	NFLP_KBLU_DR
Quanta Computer Inc.	
Size: Custom	Document Number: 05 -- SKYLAKE 4/15 (POWER-1)
Rev: 1A	
Date: Tuesday, December 13, 2016	Sheet 5 of 49

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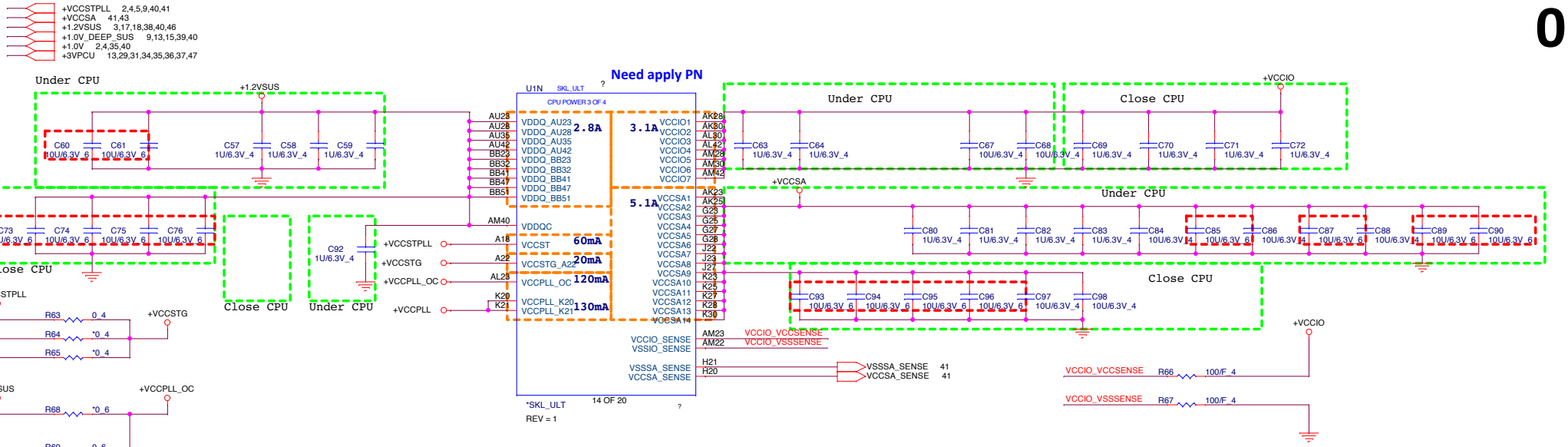
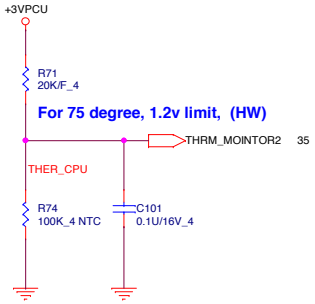
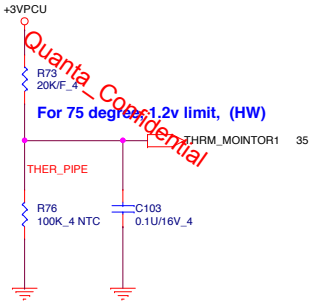


IO Thrm Protect

For CPU USE



For PIPE USE



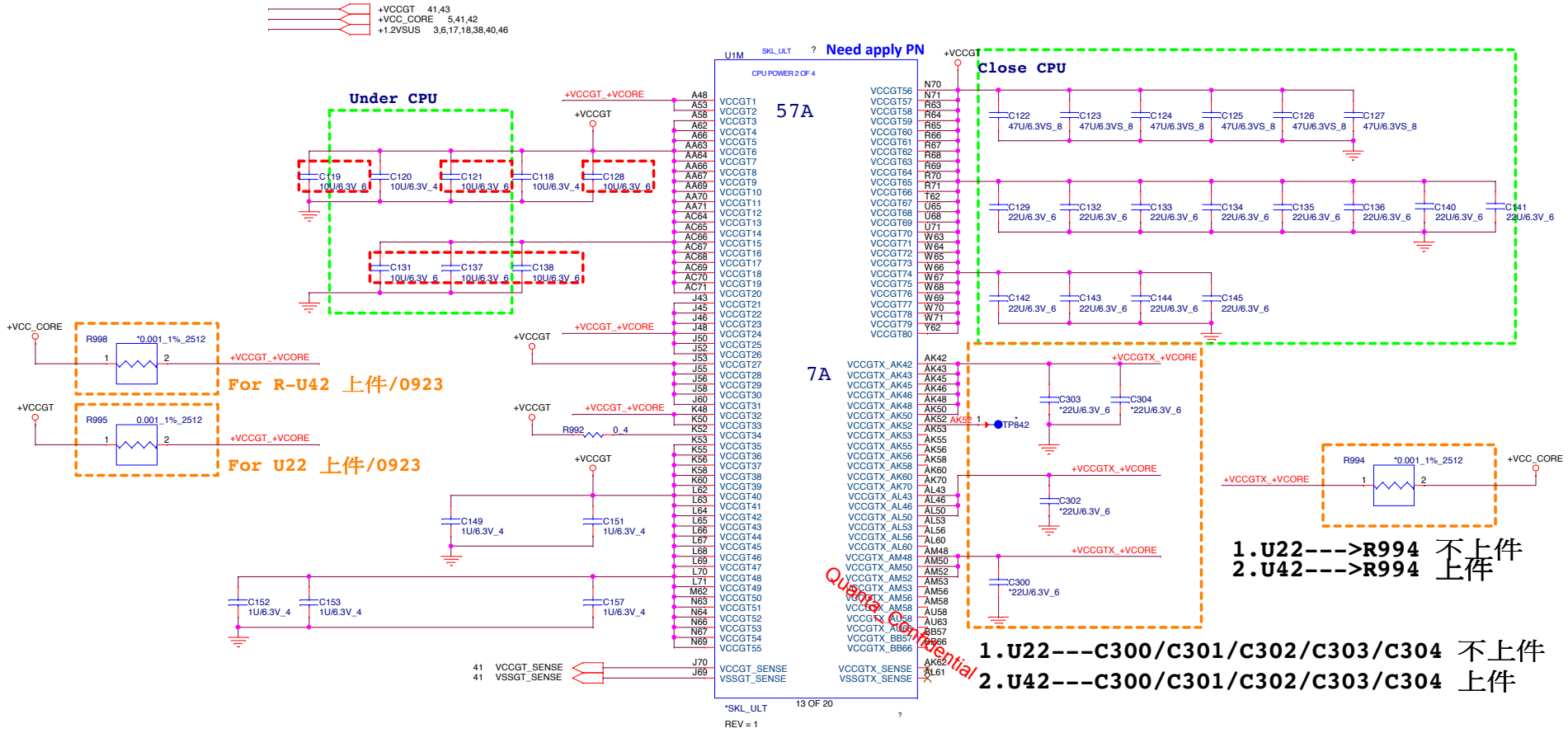
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYLAKE 5/15 (POWER-2)	1A

Date: Wednesday, December 21, 2016 | Sheet 6 of 49



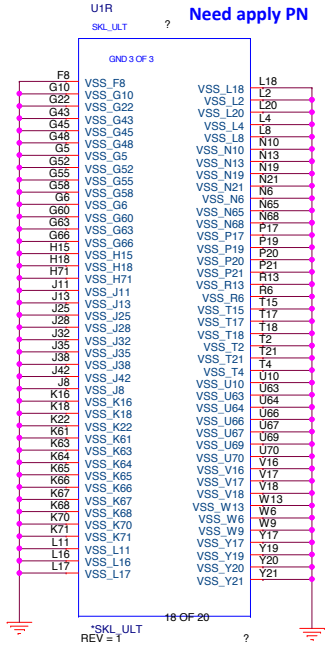
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

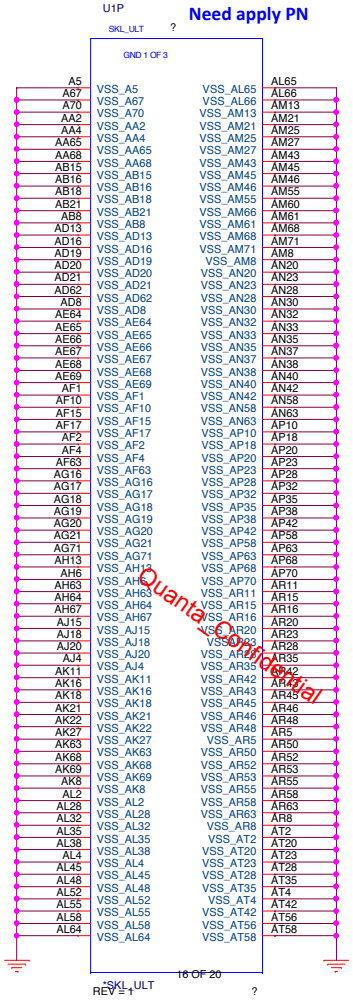
BU5

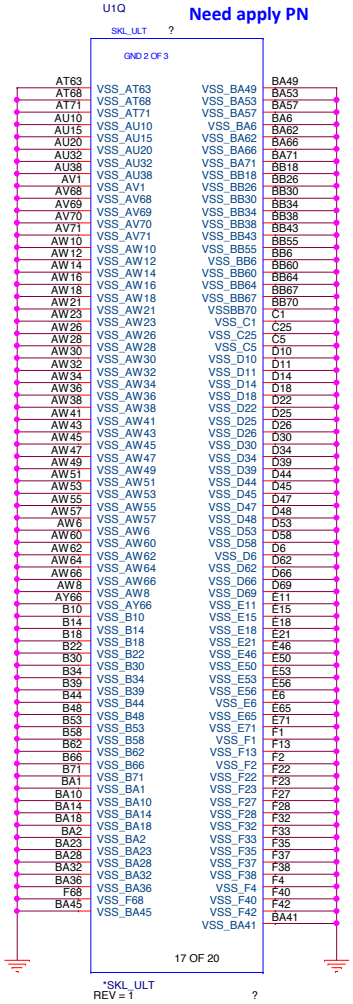
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYLAKE 6/15 (POWER-3)	1A

Date: Tuesday, December 13, 2016 Sheet 7 of 49







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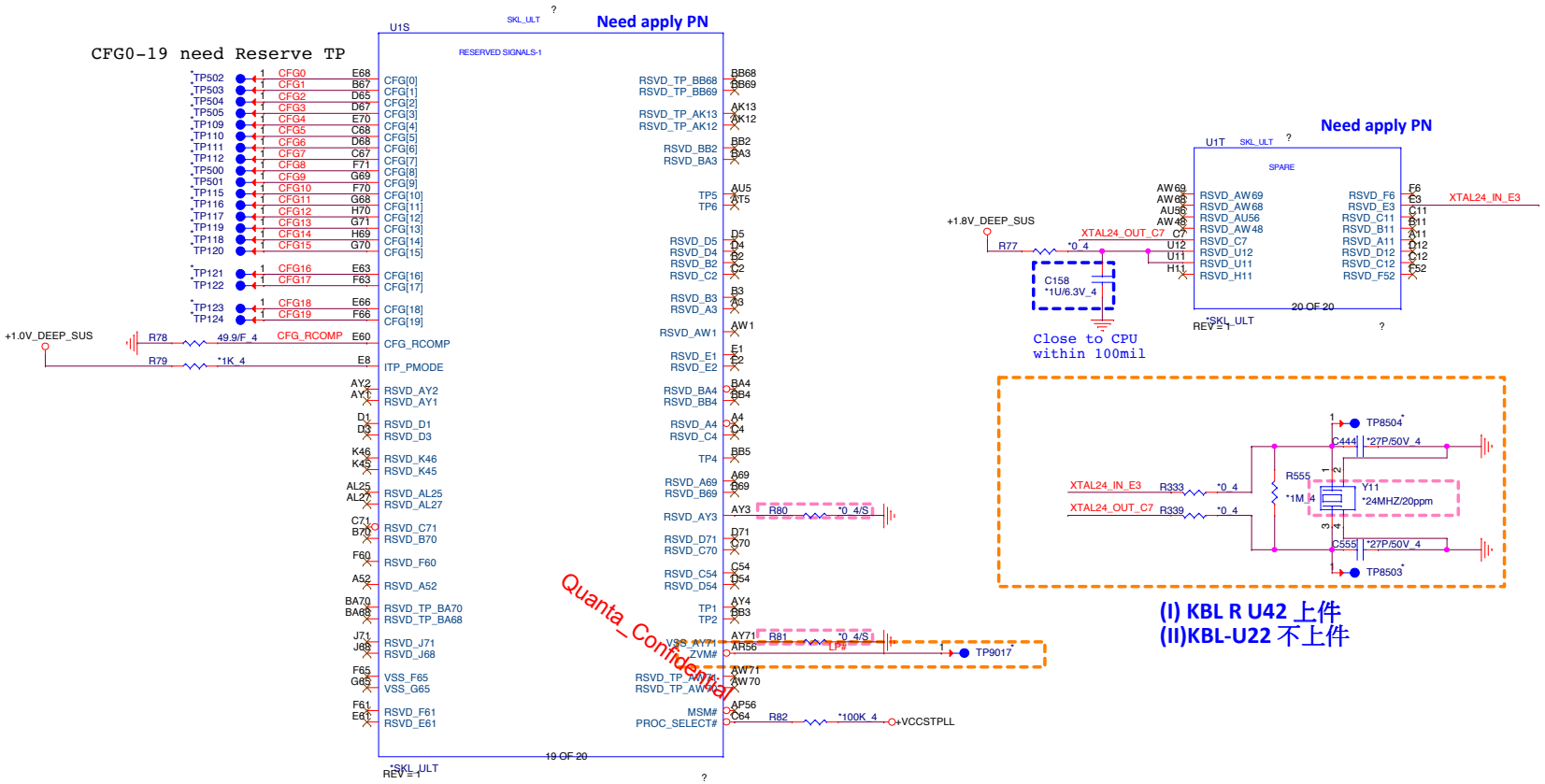
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A
Date: Tuesday, December 13, 2016	Sheet 8 of 49	



Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

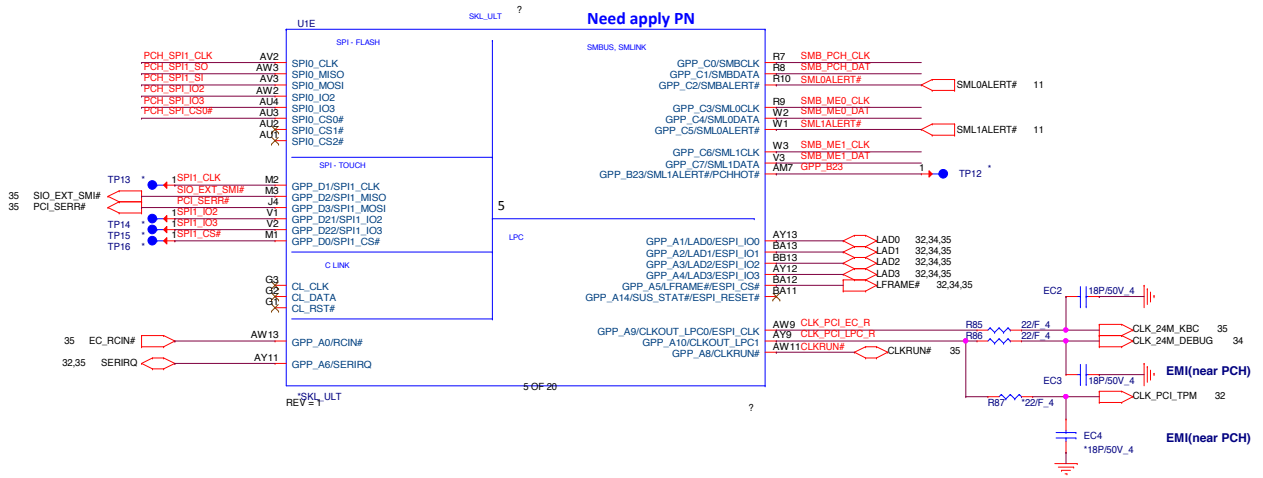
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

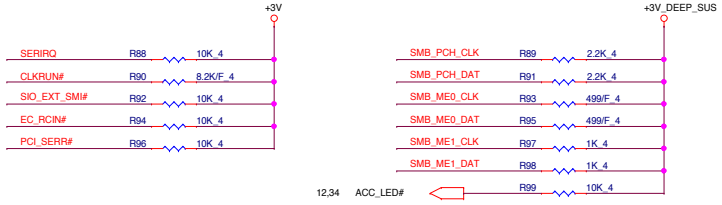
Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

Date: Tuesday, December 13, 2016 Sheet 9 of 49

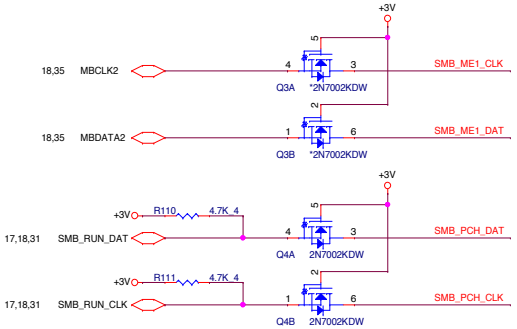
+3V_DEEP_SUS 4,11,12,14,15,18
+3V 2,4,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49
+5V 25,26,27,31,32,34,49
+1.0V 2,4,6,35,40
+3VS5 4,15,34,35,37,38,39,40,46,49



GPIO Pull UP



SMBus/Pull-up(CLG)



CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

PCH SPI ROM(CLG)

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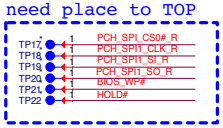
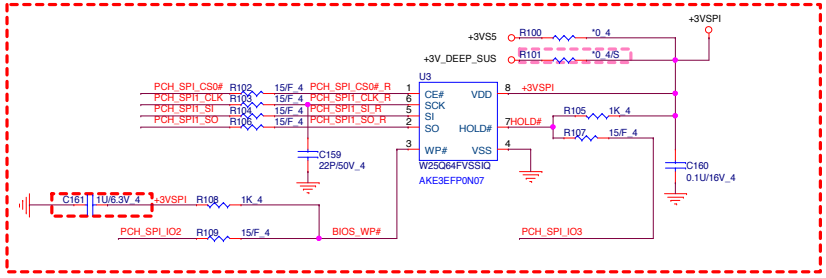
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



PCH SPI ROM(CLG)

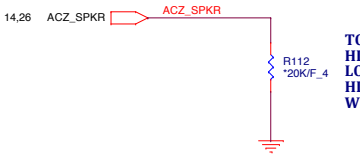


1005 Change P/N to DFHS08FS023(Socket)

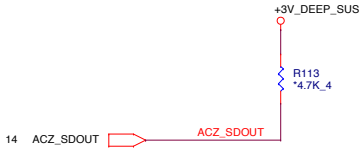
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.		
Size: Custom	Document Number: 10 -- SKYLAKE 09/15(SPI/LPC/SM)	Rev: 1A	
Date: Wednesday, December 21, 2016	Sheet 10 of 49		

Functional Strap Definitions

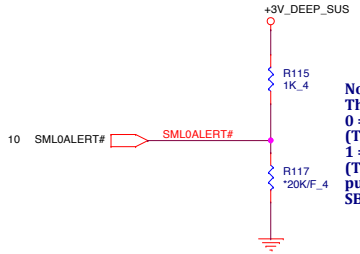
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



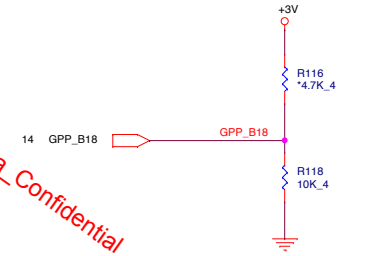
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



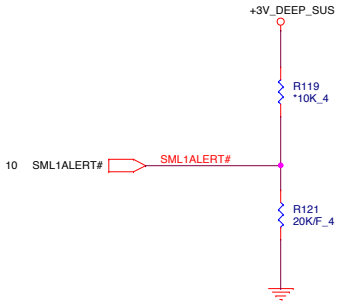
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

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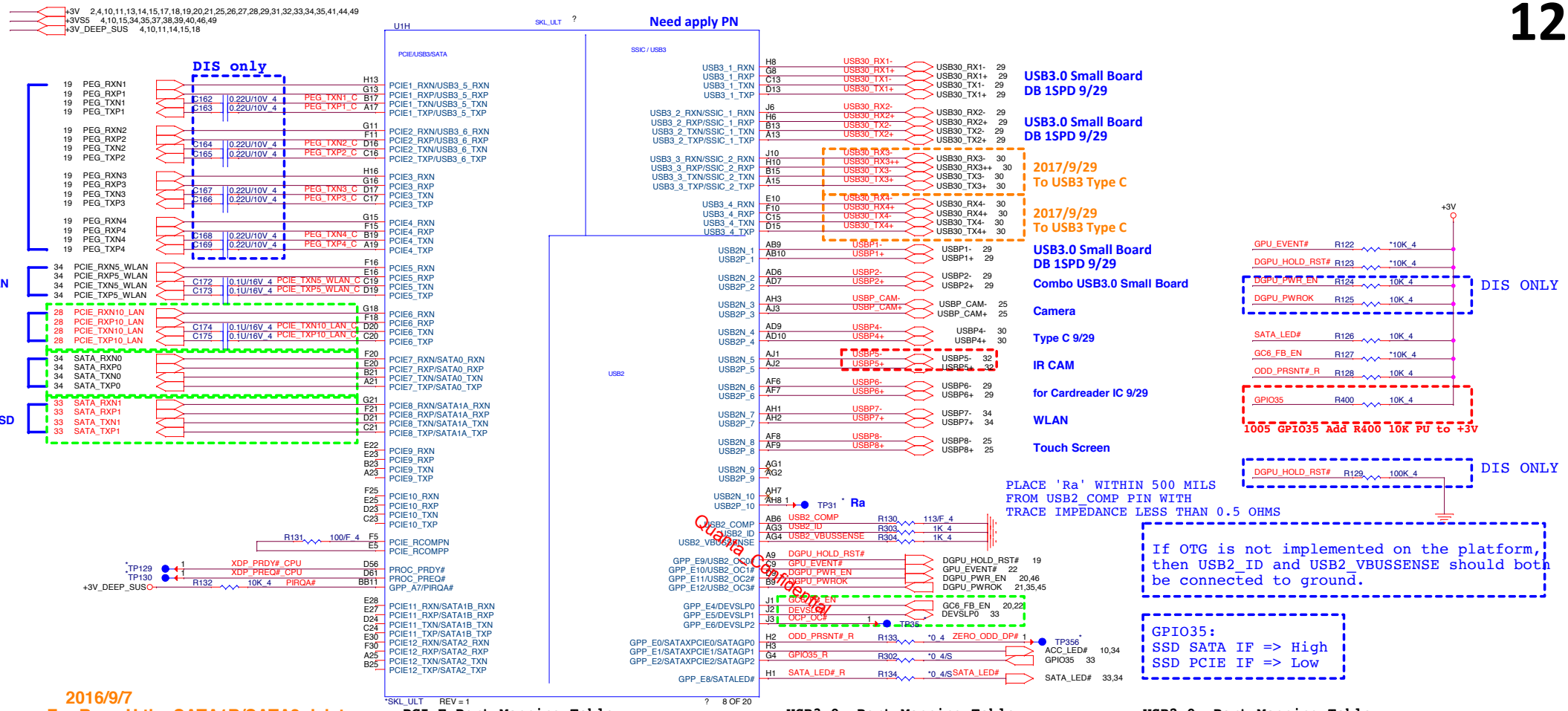

2016/9/7
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	Un-used
Port3	dGPU	Port2	Un-used
Port4	dGPU	Port3	WLAN
Port5	WLAN	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SATA SSD		
Port9	Un-used		
Port10	Un-used		
Port11	Un-used		
Port12	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Cardreader IC
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

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+3V_RTC_2 4,15
+BAT_RTC 4,15,29,36,47
+1.8V_DEEP_SUS 9,15,39
+3V 2,4,10,11,12,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49

VGA
Cardreader
SSD
WLAN
LAN

19 CLK_VGA_N → CLK_VGA_N
19 CLK_VGA_P → CLK_VGA_P
19 PCIE_CLKREQ_VGA# → PCIE_CLKREQ_VGA#
PCIE_CLKREQ_CR#
PCIE_CLKREQ_SSD#
34 CLK_PCIE_WLANN → CLK_PCIE_WLANN
34 CLK_PCIE_WLANP → CLK_PCIE_WLANP
34 PCIE_CLKREQ_WLAN# → PCIE_CLKREQ_WLAN#
28 CLK_PCIE_LANN → CLK_PCIE_LANN
28 CLK_PCIE_LANP → CLK_PCIE_LANP
28 PCIE_CLKREQ_LAN# → PCIE_CLKREQ_LAN#
PCIE_CLKREQ5#

U1J SKL_ULT ? Need apply PN
CLOCK SIGNALS

D42 CLKOUT_PCIE_N0
C42 CLKOUT_PCIE_P0
AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
A17 GPP_B6/SRCCLKREQ1#
D41 CLKOUT_PCIE_N2
C41 CLKOUT_PCIE_P2
A18 GPP_B7/SRCCLKREQ2#
D40 CLKOUT_PCIE_N3
C40 CLKOUT_PCIE_P3
AT10 GPP_B8/SRCCLKREQ3#
B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
AU8 GPP_B9/SRCCLKREQ4#
E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
AU7 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43 CK_XDP_N_R 1 TP125
CLKOUT_ITPXDP_P E43 CK_XDP_P_R 1 TP126
GPD8/SUSCLK BA17
XTAL24_IN E37 XTAL24_IN
XTAL24_OUT E35 XTAL24_OUT
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 RTC_X1
RTCX2 AM20 RTC_X2 TP38
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#

TBT
10 OF 20
*SKL_ULT REV = 1

+1.0V_DEEP_SUS
R135 2.7K/F_4
XCLK_BIASREF
R137 *60.4/F_4

CLK_REQ/Strap Pin(CLG)
+3V
PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN
CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3
C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A33 CSI2_DN6
B33 CSI2_DP6
A31 CSI2_DN7
B31 CSI2_DP7
A29 CSI2_DN8
B29 CSI2_DP8
C29 CSI2_DN9
D29 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

C37 CSI2_CLKN0
C37 CSI2_CLKP0
C32 CSI2_CLKN1
C32 CSI2_CLKP1
C29 CSI2_CLKN2
C29 CSI2_CLKP2
C26 CSI2_CLKN3
C26 CSI2_CLKP3
E13 CSI2_COMP
B7 GPP_D4/FLASHTRIG

EMMC
AP2 GPP_F13/EMMC_DATA0
AP1 GPP_F14/EMMC_DATA1
AN2 GPP_F15/EMMC_DATA2
AN1 GPP_F16/EMMC_DATA3
AM4 GPP_F17/EMMC_DATA4
AM2 GPP_F18/EMMC_DATA5
AM1 GPP_F19/EMMC_DATA6
AM3 GPP_F20/EMMC_DATA7
AM2 GPP_F21/EMMC_RCLK
AP4 GPP_F22/EMMC_CLK
GPP_F12/EMMC_CMD
AT1 EMMC_RCOMP

R143 100/F_4
1005 Delete TP
Quanta_Confidential
EMMC_RCOMP R144 200/F_4

9 OF 20
*SKL_ULT REV = 1

RTC Clock 32.768KHz

C177 15P/50V_4 — Y1 32.768KHZ/20ppm — C179 15P/50V_4
RTC_X1 — R147 10M_4 — RTC_X2

RTC Circuitry(RTC)

+3V_RTC_2 +BAT_RTC 30mils
Main BAT -->Ra
Coin BAT -->Rb (default)
Rb R306 *0_4
Ra R307 0_4
R145 *0_6 RTC_RST#
R146 20K/F_4
C178 1U/6.3V_4
RTC Power trace width 20mils.
+3V_RTC_0
+3VPCU R150 1K_4 +3V_RTC_1 D2 BAT54CW-7-F C181 1U/6.3V_4
R149 20K/F_4 SRTC_RST#
C182 1U/6.3V_4
R9042 *0_6
R9041 0_6
RTC_RST# R152 *0_6 SRTC_RST#
CN101 *BAT_CONN DFHS02FS027 BAT-23_2-4_2
CN11 88266-020L

R151 10K_4
EC_RTC_RST 35
RTC_RST#
Q5A 2N7002KDW
R942 *0_4
EC_SRTC_RST 35
SRTC_RST#
Q5B 2N7002KDW
R153 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

TPS1 C176 27P/50V_4
XTAL24_IN R666 0_4
XTAL24_OUT R667 0_4
R148 1M_4 Y2 24MHZ/20ppm
C180 27P/50V_4 TPS2

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE 12/15 (CLK/EMMC)	1A

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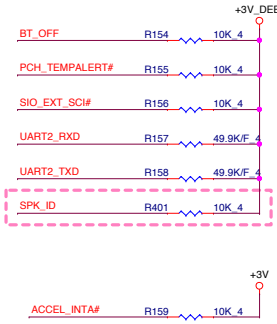
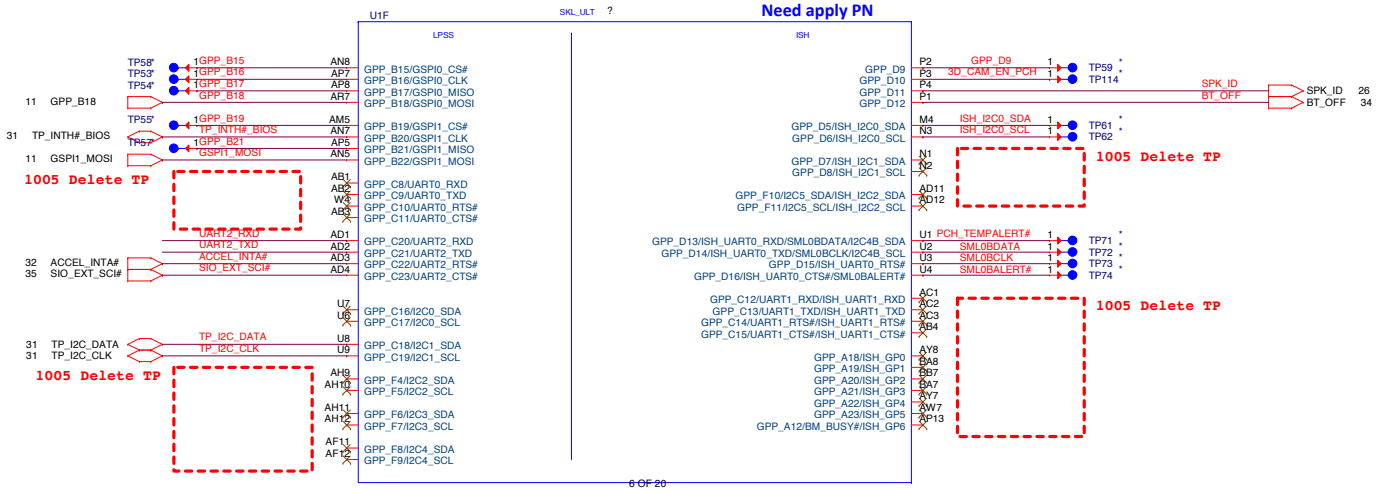
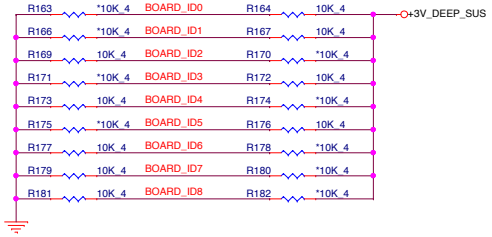
Skylake (GPIO)

+3V 2,4,10,11,12,13,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44,49
+3V_DEEP_SUS 4,10,11,12,15,18



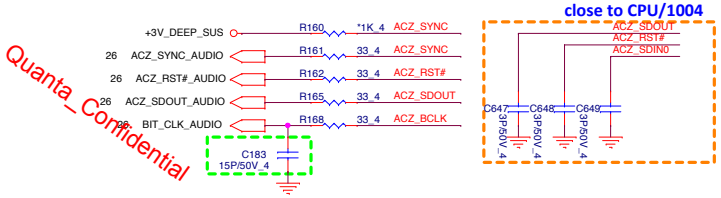


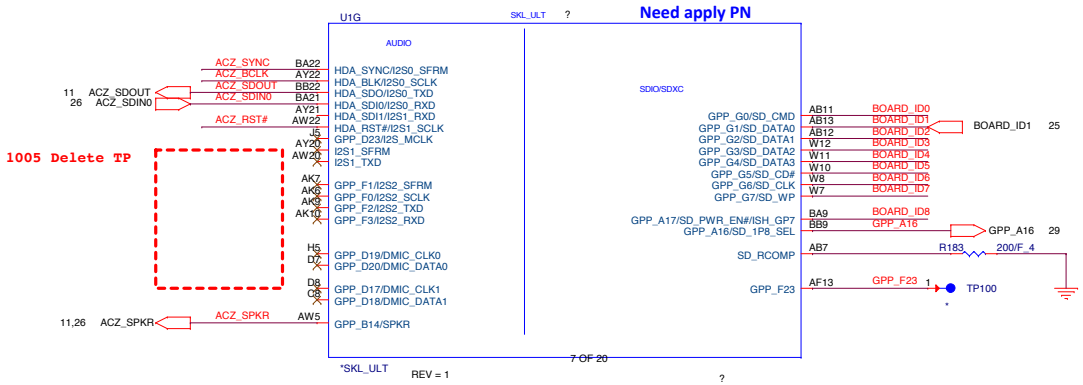
HDA Bus(CLG)

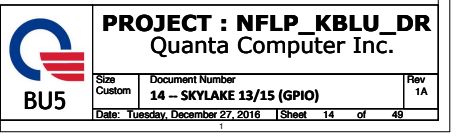


Skylake U	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 0)	0:AMD 1:NV GPU type	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	01 14" 01 15" 1SPD (by cable ---->00) 10 17" 11 2SPD	0 : UMA 1 : DIS

ID1(R167)always 上件







4,10,11,12,14,18 +3V_DEEP_SUS
9,13,39,40 +1.0V_DEEP_SUS
9,39 +1.8V_DEEP_SUS
4,13,29,36,47 +BAT_RTC
4,10,34,35,37,38,39,40,46,49 +3VSS

U1O SKL_ULT
CPU POWER 4 OF 4
*SKL_ULT
REV = 1
15 OF 20

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

Ca

Cb

2.899A
2.57A
1.714A
0.03A
0.09A

close to CPU/1004

L668 120/300MA
C654 3P/50V_4
C653 3P/50V_4

close to CPU/1004

L666 120/300MA
C651 3P/50V_4
C650 3P/50V_4

Main BAT -->Ra
Coin BAT -->Rb (default)

20mils

1005 Change +3V_RTC to +BAT_RTC

for DS3

U4 AP2821KTR-G1

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BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- SKYLAKE 15/15 XDP&APS *	1A
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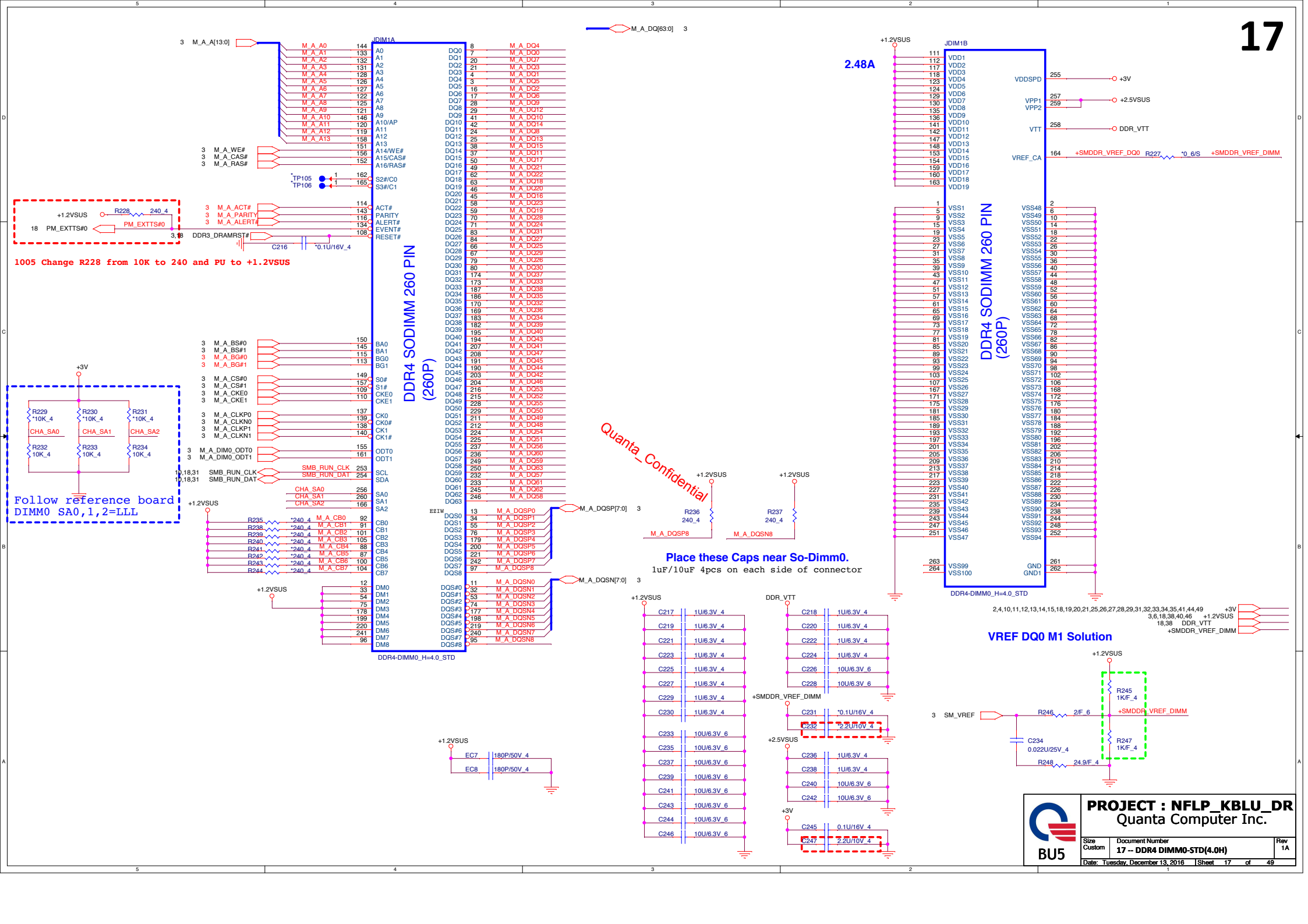
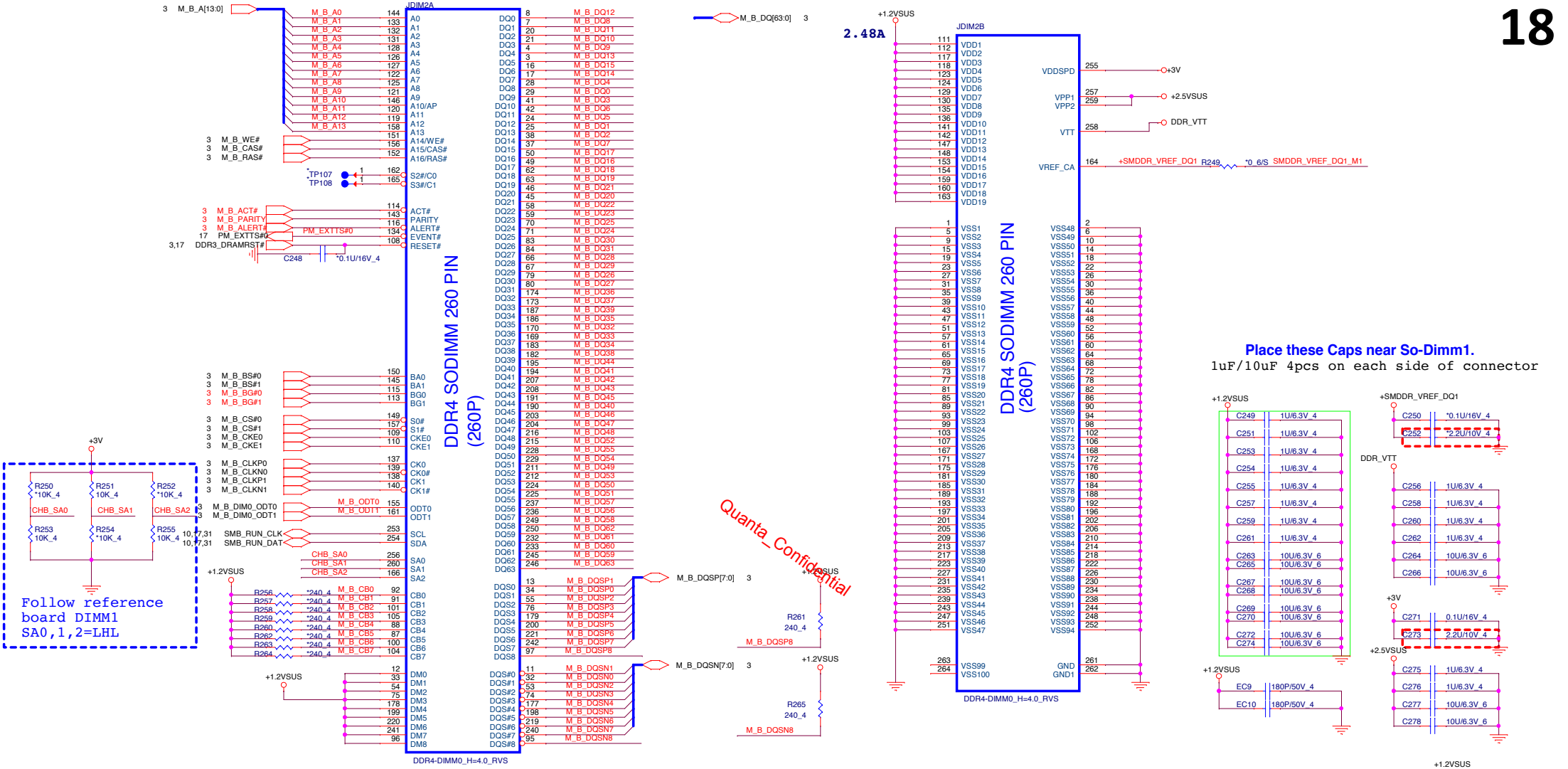

JDIM1A
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
DDR4-DIMM0_H=4.0_STD
M_A_DQ[63:0]
M_A_A[13:0]
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_ACT#
M_A_PARITY
M_A_ALERT#
DDR3_DRAMRST#
M_A_BS#0
M_A_BS#1
M_A_BG#0
M_A_BG#1
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_CLKP0
M_A_CLKN0
M_A_CLKP1
M_A_CLKN1
M_A_DIM0_ODT0
M_A_DIM0_ODT1
SMB_RUN_CLK
SMB_RUN_DAT
M_A_DQSP[7:0]
M_A_DQSN[7:0]
+1.2VSUS
+3V
+2.5VSUS
DDR_VTT
+SMDDR_VREF_DIMM
PM_EXTTS#0
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
2.48A
Quanta_Confidential
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, December 13, 2016
Sheet 17 of 49



Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	18 -- DDR4 DIMM1-RVS(4.0H)	1A

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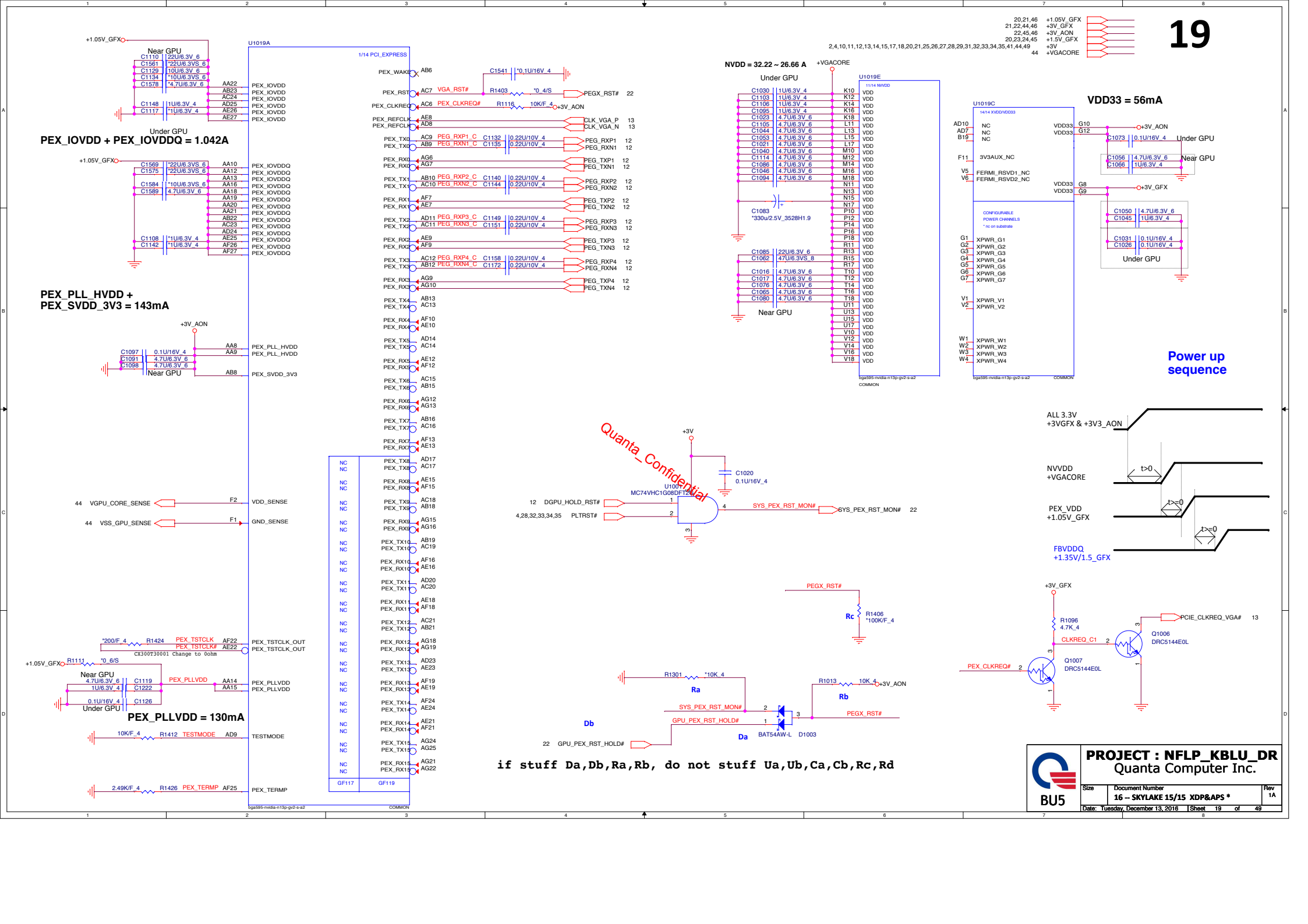
19
PEX_IOVDD + PEX_IOVDDQ = 1.042A
PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA
PEX_PLLVDD = 130mA
NVDD = 32.22 ~ 26.66 A
VDD33 = 56mA
Power up
sequence
ALL 3.3V
+3VGFX & +3V3_AON
NVVDD
+VGACORE
PEX_VDD
+1.05V_GFX
FBVDDQ
+1.35V/1.5_GFX
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if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Document Number
16 – SKYLAKE 15/15 XDP&APS *
Rev
1A
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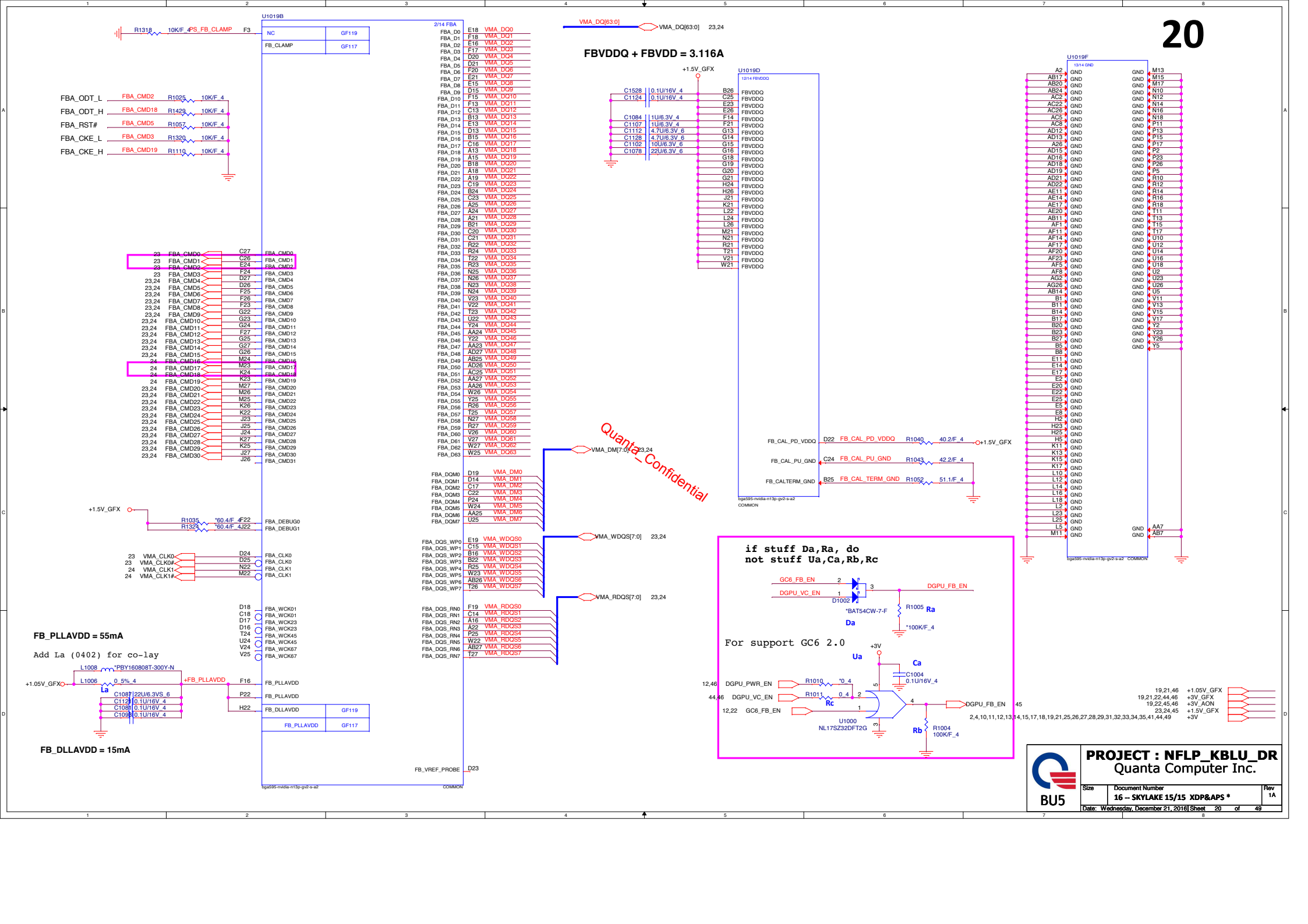
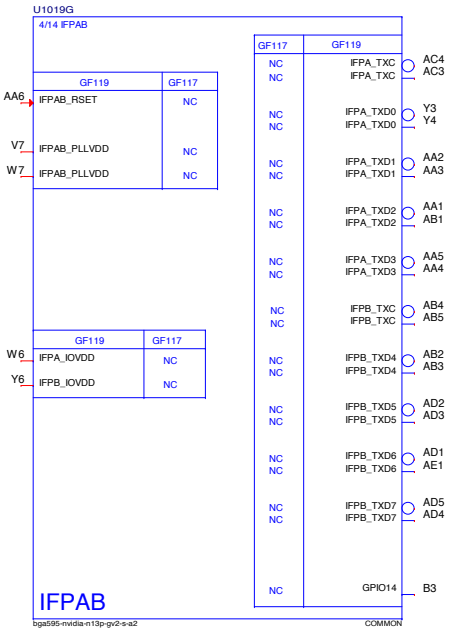
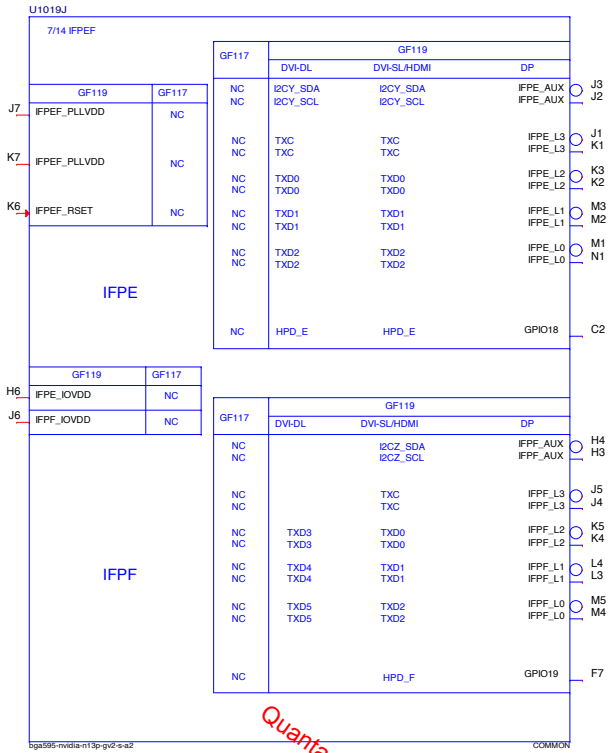
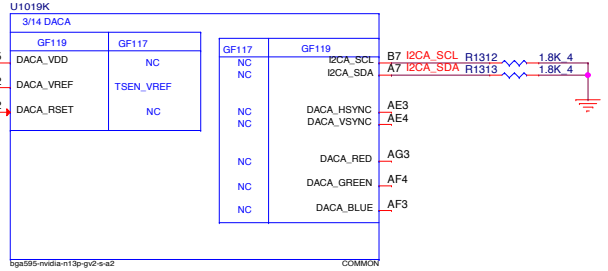
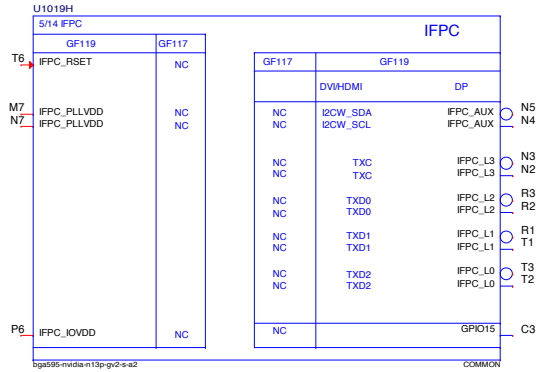


PROJECT :	NFLP_KBLU_DR
	Quanta Computer Inc.
Size	BU5
Document Number	16 – SKYLAKE 15/15 XDP&APS *
Rev	1A
Date: Wednesday, December 21, 2016	Sheet 20 of 49

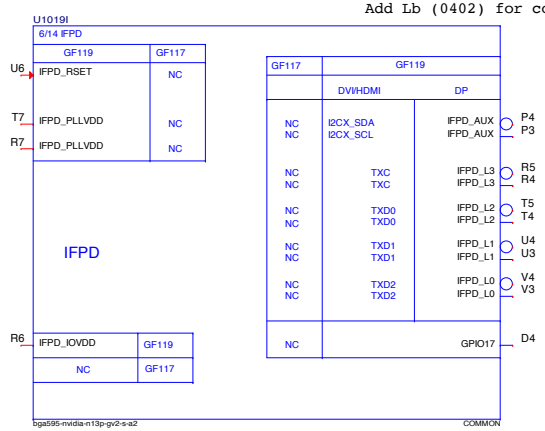








Add Lb (0402) for co-lay



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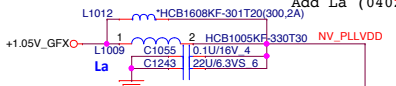
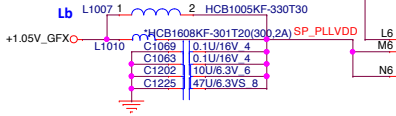
PLLVDD = 38mA

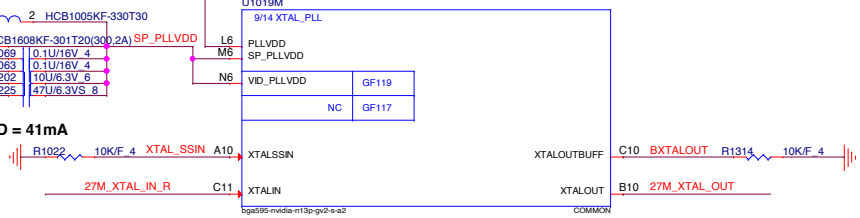
Add La (0402) for co-lay

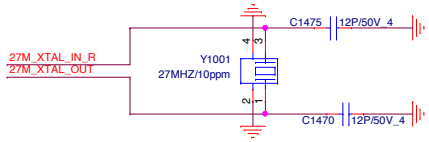


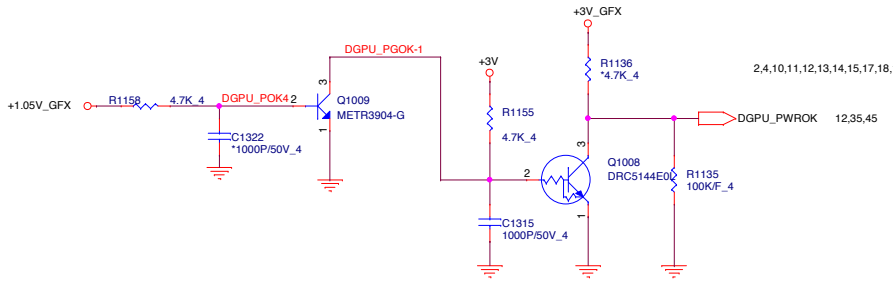
SP_PLLVDD = 17mA

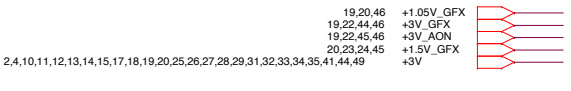


VID_PLLVDD = 41mA









BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

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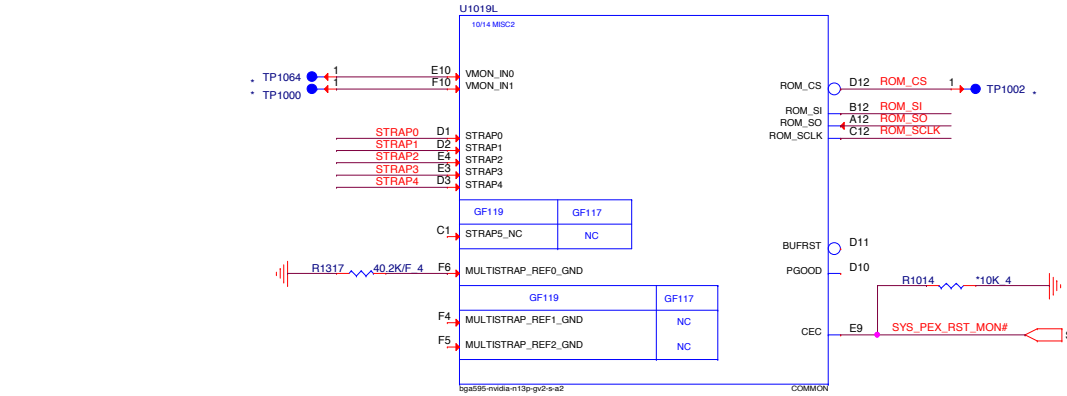

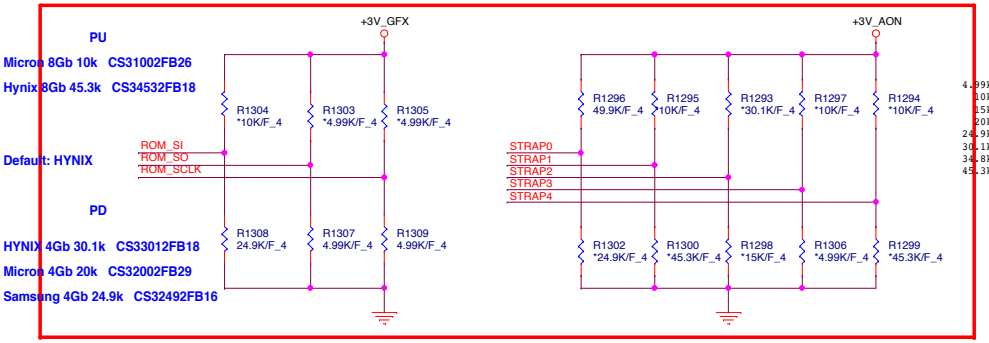

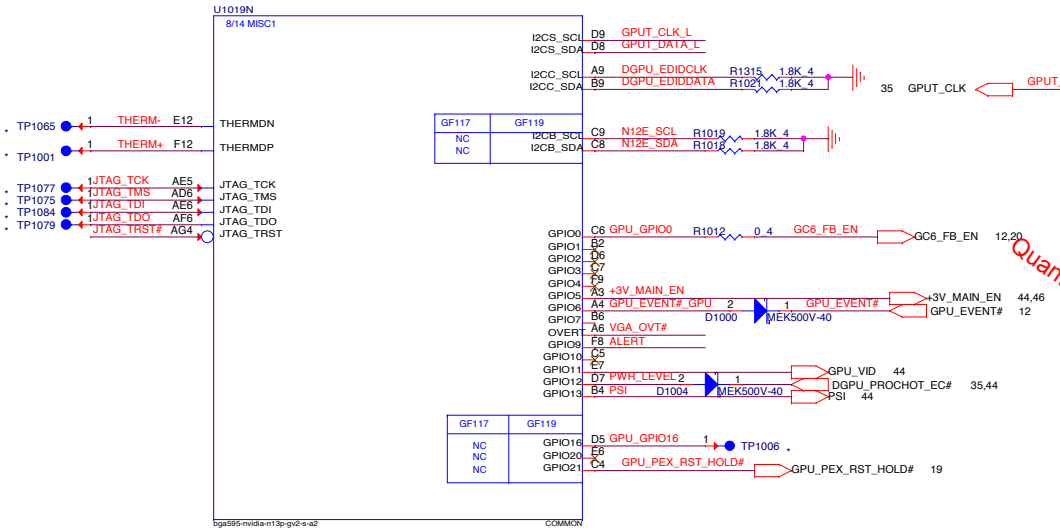

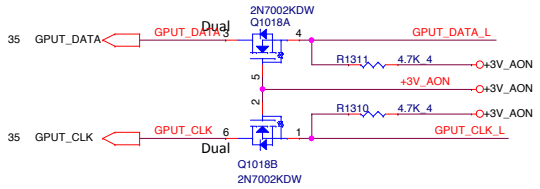

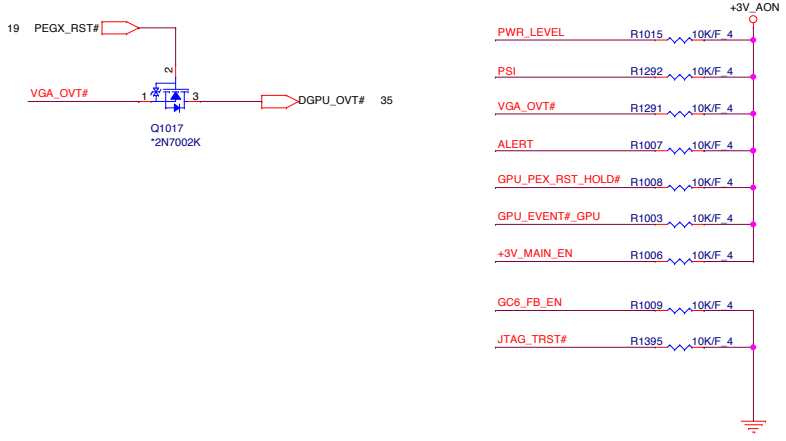

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table ROM_SI S F

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000						
0101	DDR3 256Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC4G63CFR-NOC	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 256Mx16, 64bit, 4Gb,900MHz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 4Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16RA-107G:A	0x9	AKD5QGSTL05	AKD5QGSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0xF	AKD5QFDTW00	AKD5QFDTW01

19,21,44,46 +3V_GFX
19,45,46 +3V_AON
20,23,24,45 +1.5V_GFX

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

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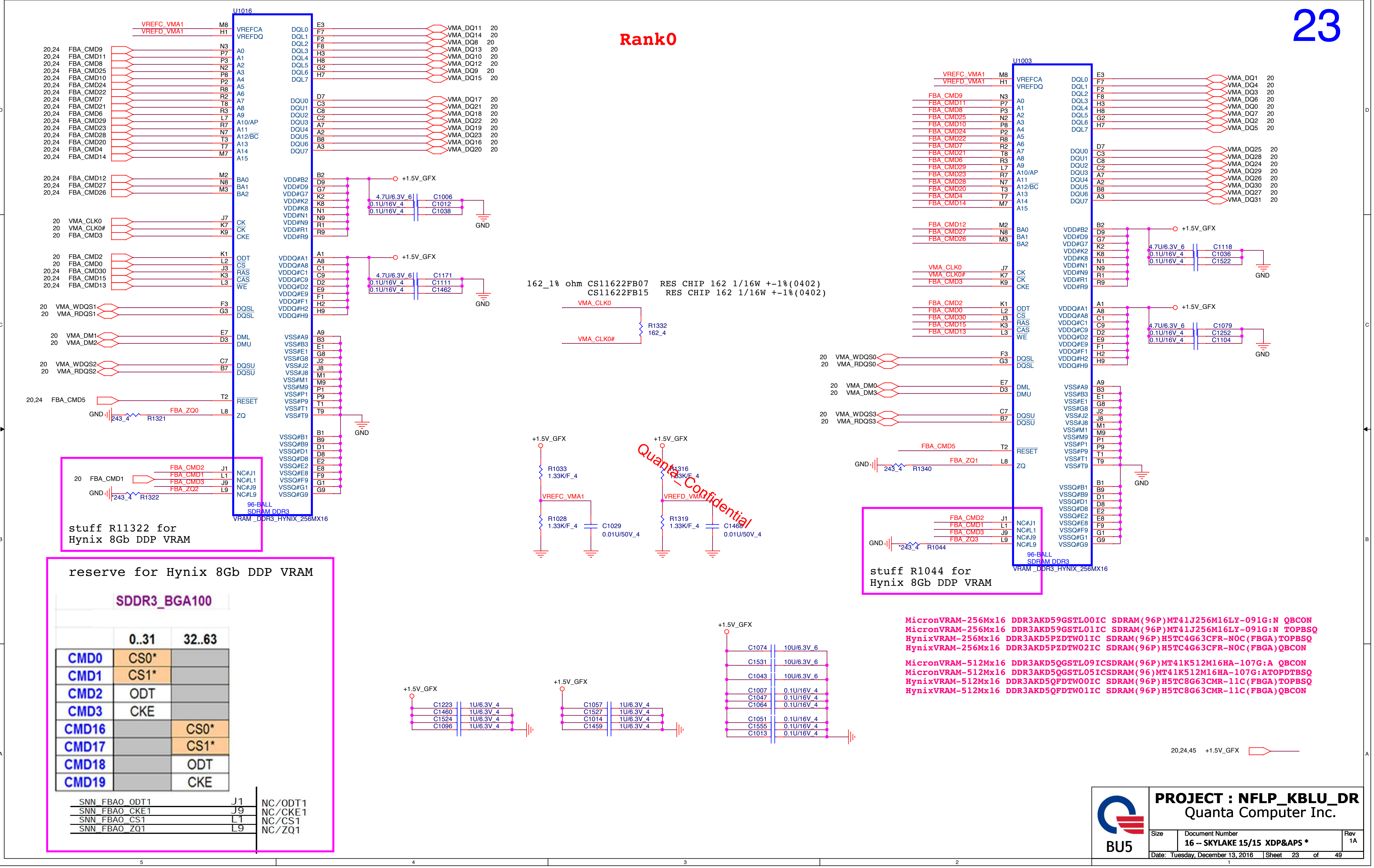

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

stuff R11322 for Hynix 8Gb DDP VRAM

stuff R1044 for Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBA0_ODT1 J1 NC/ODT1
SNN_FBA0_CKE1 J9 NC/CKE1
SNN_FBA0_CS1 L1 NC/CS1
SNN_FBA0_ZQ1 L9 NC/ZQ1

MicronVRAM-256Mx16 DDR3AKD59GSTL00IC SDRAM(96P)MT41J256M16LY-091G:N QBCON
MicronVRAM-256Mx16 DDR3AKD59GSTL01IC SDRAM(96P)MT41J256M16LY-091G:N TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW01IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW02IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)QBCON

MicronVRAM-512Mx16 DDR3AKD5QGSTL09ICSDRAM(96P)MT41K512M16HA-107G:A QBCON
MicronVRAM-512Mx16 DDR3AKD5QGSTL05ICSDRAM(96)MT41K512M16HA-107G:ATOPDTBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW00IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)TOPBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW01IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)QBCON

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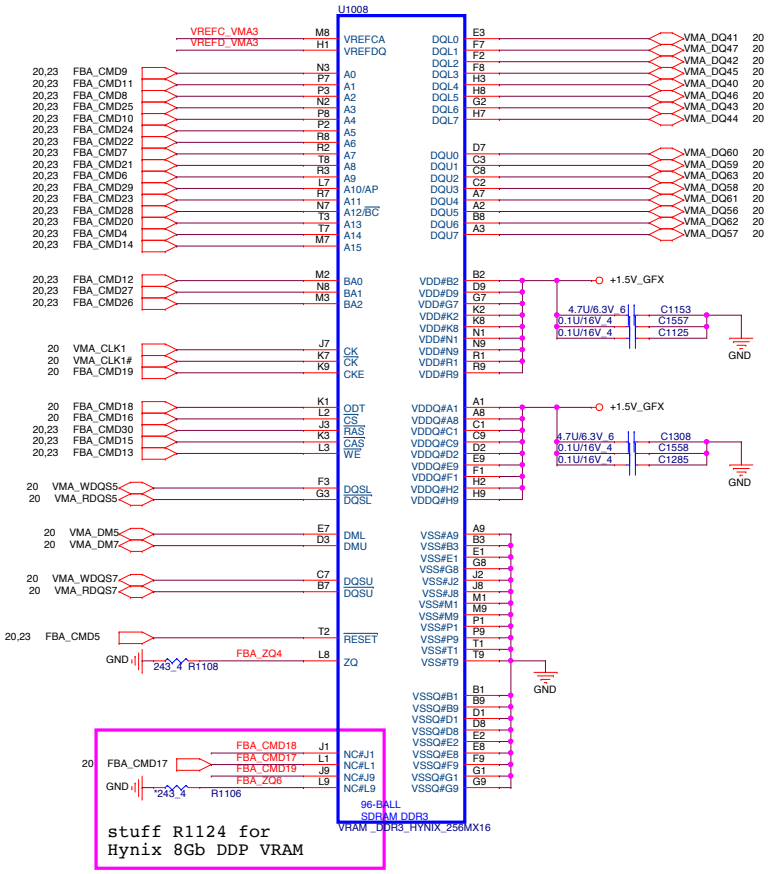
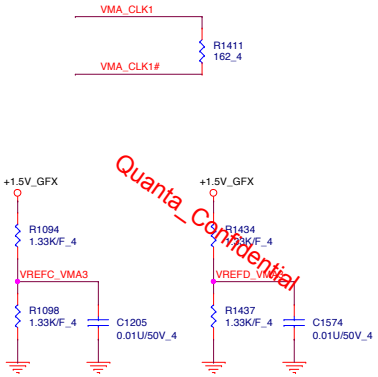
Rank0

1114SWAP

1114SWAP



162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)



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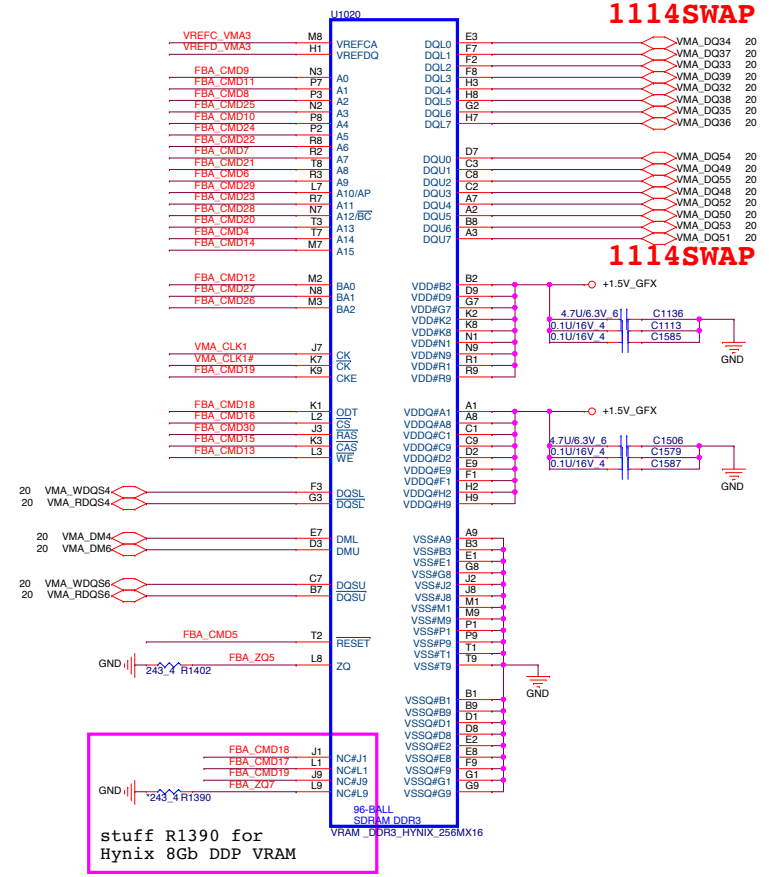
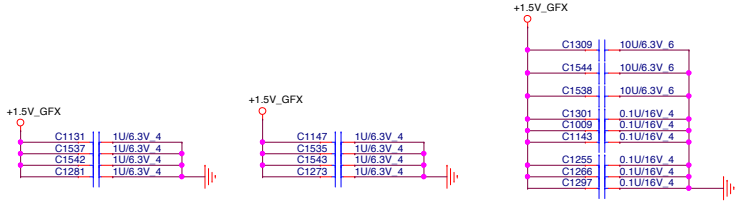
1114SWAP





20,23,45 +1.5V_GFX

MicronVRAM-256Mx16 DDR3AKD59GSTL00IC SDRAM(96P)MT41J256M16LY-091G:N QBCON
MicronVRAM-256Mx16 DDR3AKD59GSTL01IC SDRAM(96P)MT41J256M16LY-091G:N TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW01IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)TOPBSQ
HynixVRAM-256Mx16 DDR3AKD5PZDTW02IC SDRAM(96P)H5TC4G63CFR-N0C(FBGA)QBCON

MicronVRAM-512Mx16 DDR3AKD5QGSTL09ICSDRAM(96P)MT41K512M16HA-107G:A QBCON
MicronVRAM-512Mx16 DDR3AKD5QGSTL05ICSDRAM(96)MT41K512M16HA-107G:ATOPDTBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW00IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)TOPBSQ
HynixVRAM-512Mx16 DDR3AKD5QFDTW01IC SDRAM(96P)H5TC8G63CMR-11C(FBGA)QBCON

BU5

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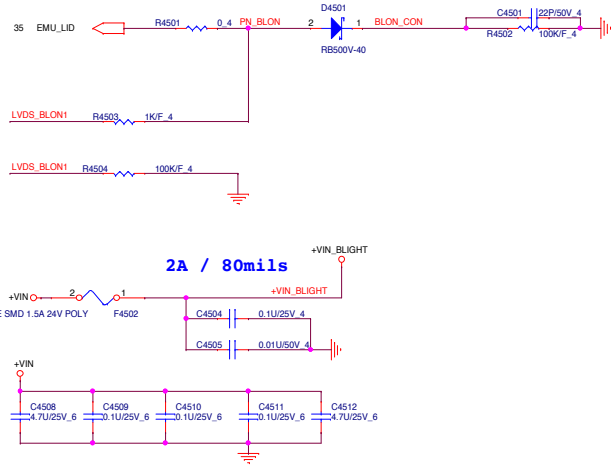
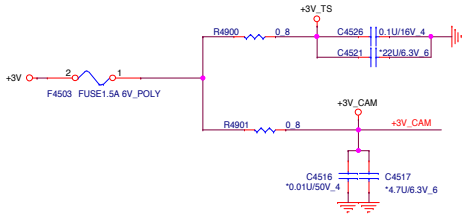
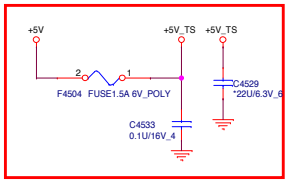
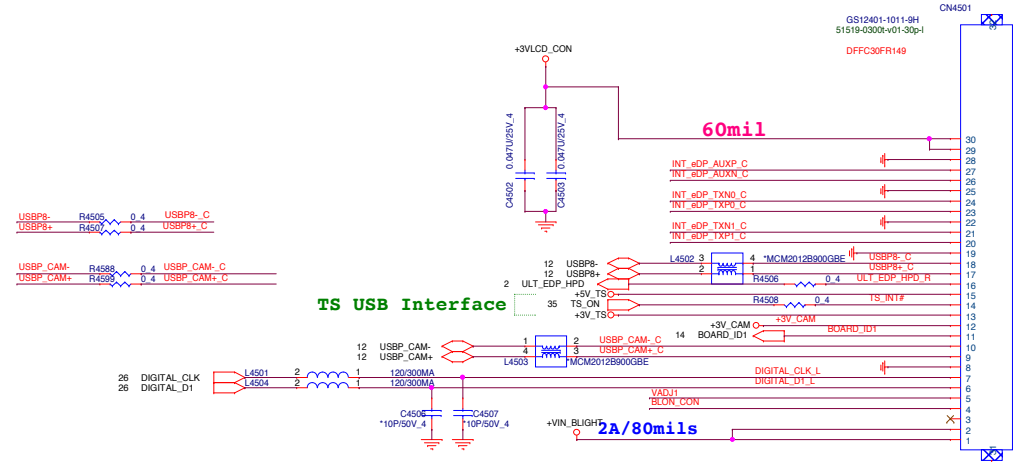
LID Switch

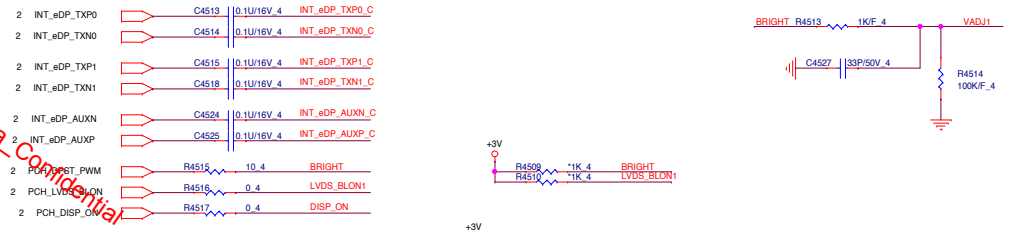


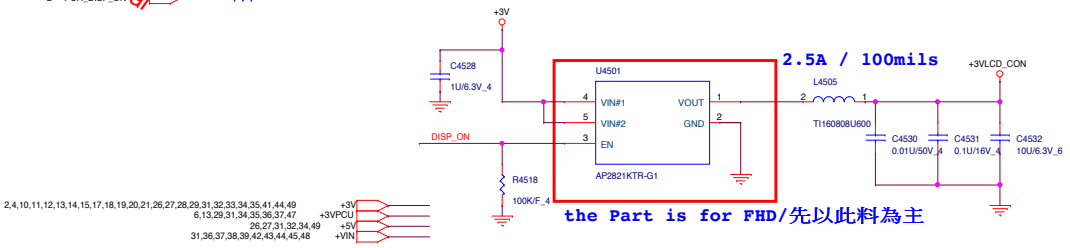




eDP Conn.







BU5

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Quanta Computer Inc.

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Custom	27 -- eDP CONN/LID/CAM/D-MIC/TS	1A

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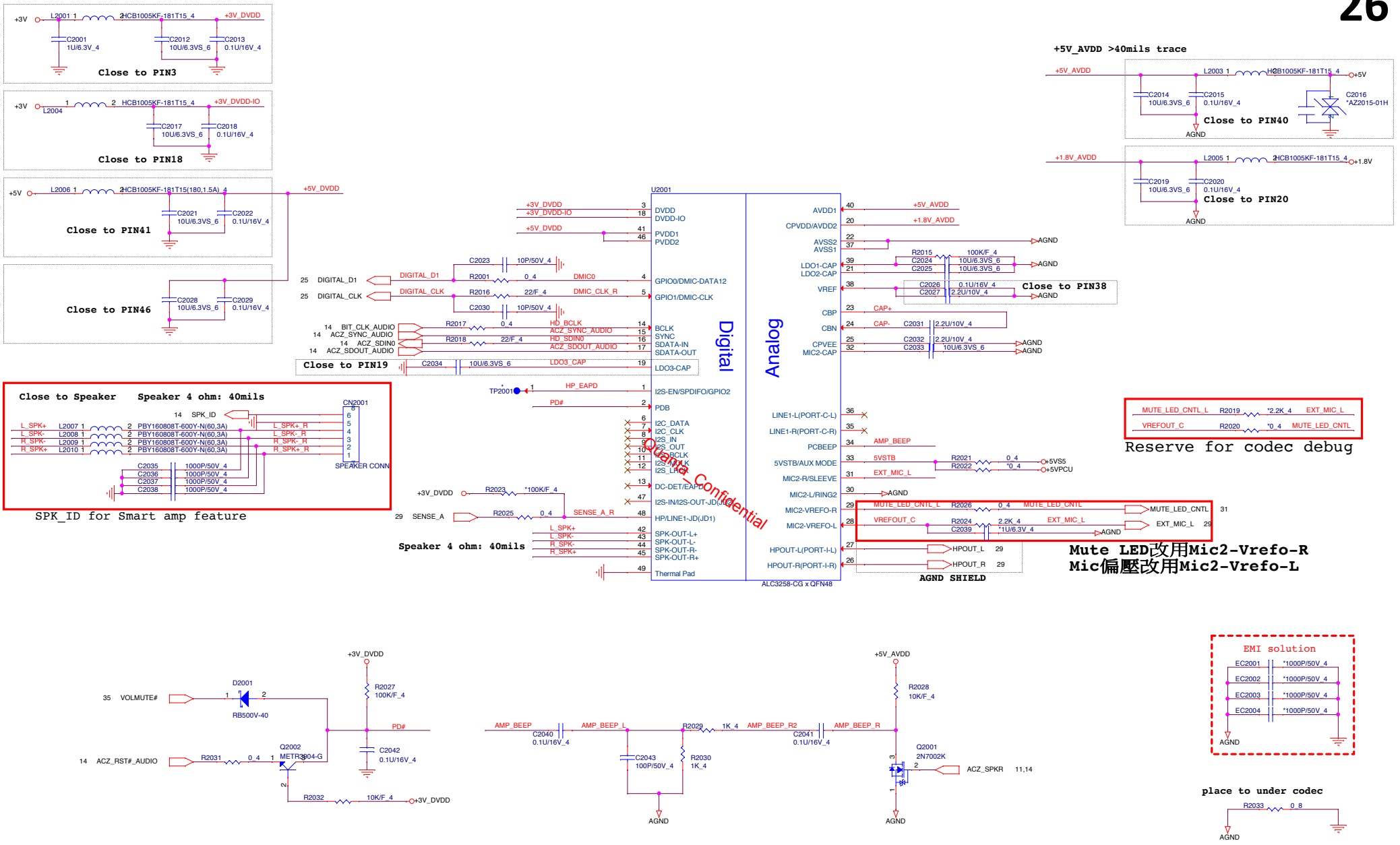

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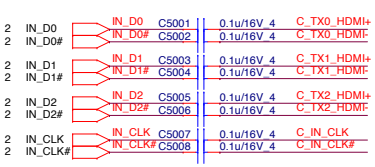
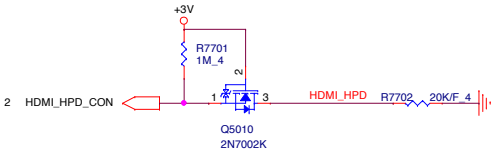
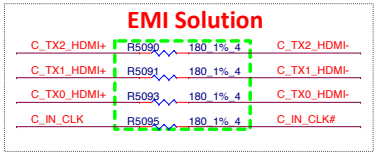
HDMI CONN

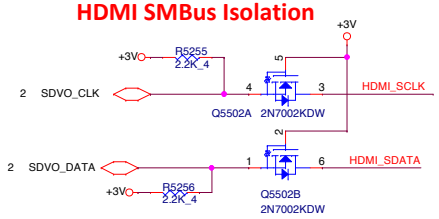




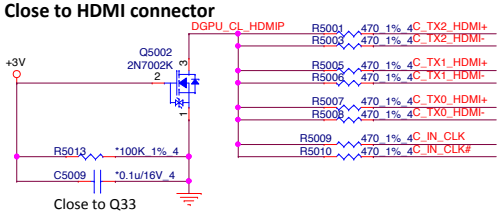
EMI Solution

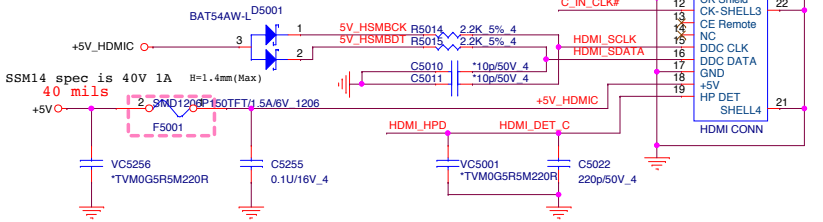


HDMI SMBus Isolation



Close to HDMI connector





Head Phone out

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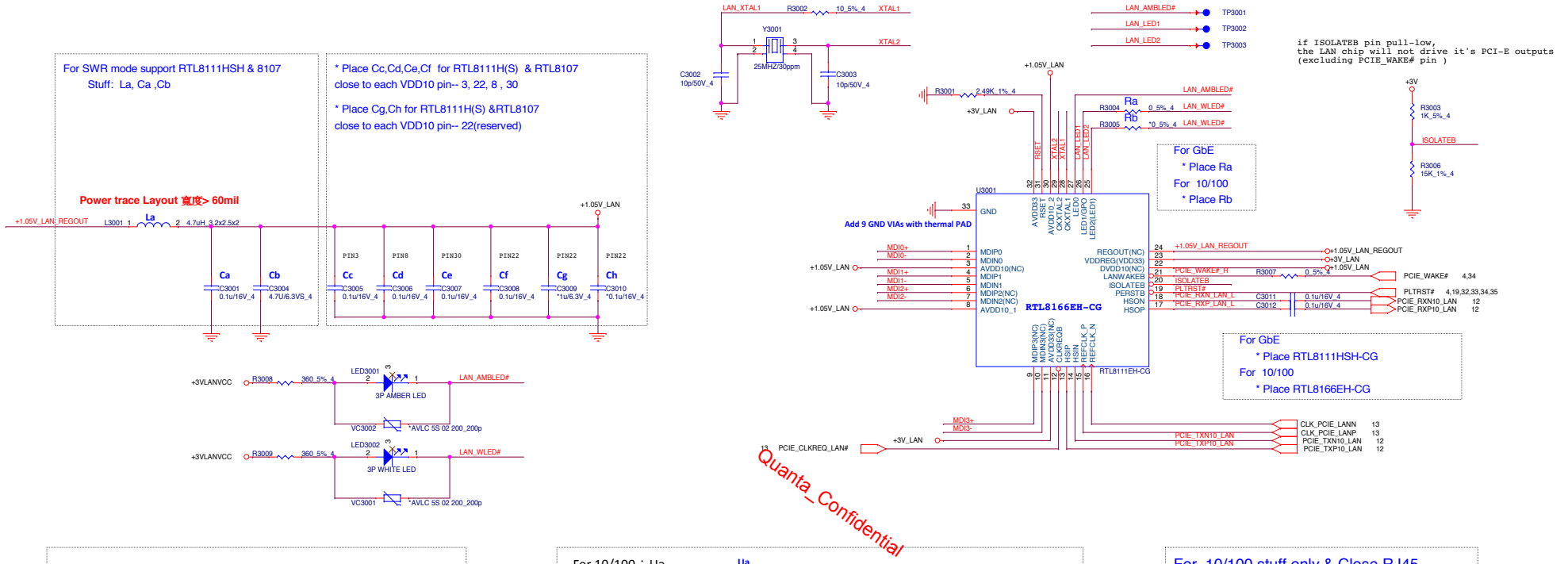
LAN RTL8107EH/RTL8111HSH



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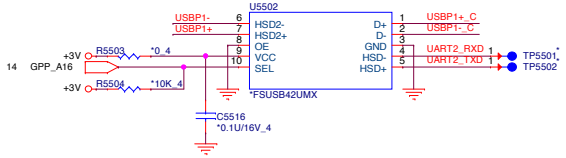
12,29 USBP1-
12,29 USBP1+
USBP1- R5502 0_4 USBP1-_C
USBP1+ R5501 0_4 USBP1+_C

+3VPCU R9045 360_5%_4 LED7011 3P WHITE LED DEEP_PWRLED#
VC9002 *AVLC 5S 02 200_200p

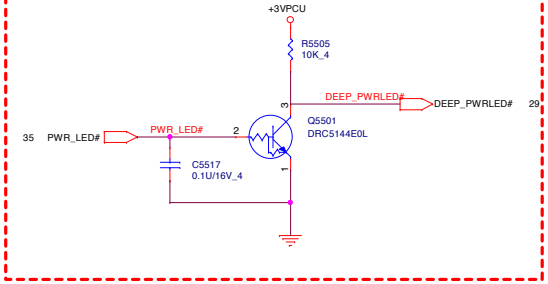
UART for Win7 WHQL DEBUG



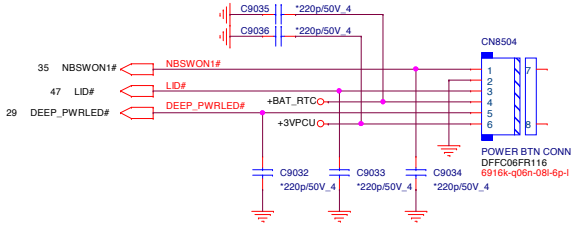
Place Back to Back La

Daughter Board

1123 Add PWR LED MOS Circuit



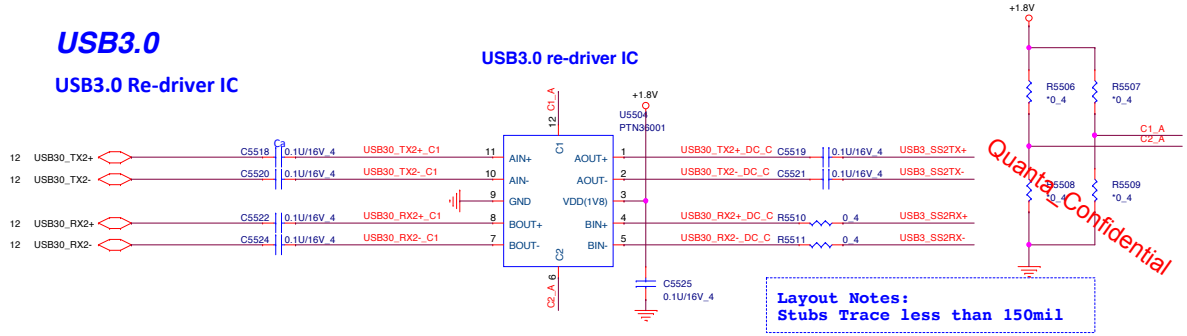
Power Board



USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC



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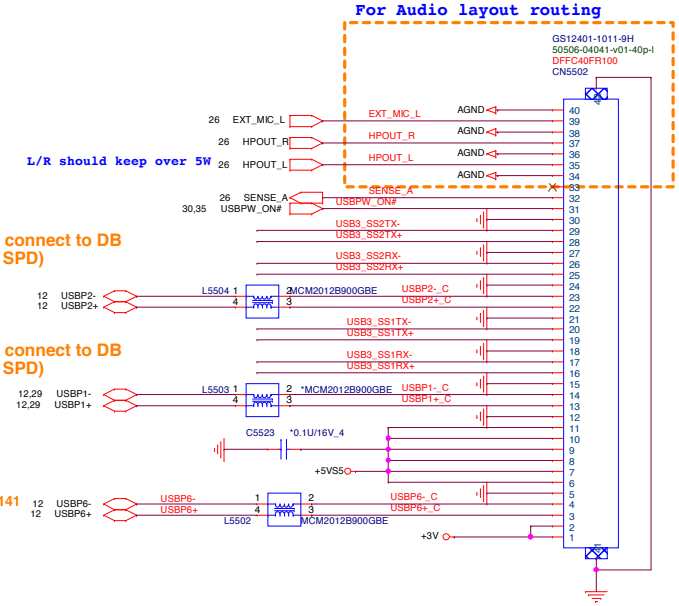
Layout Notes:
Stubs Trace less than 150mil

Daughter Board

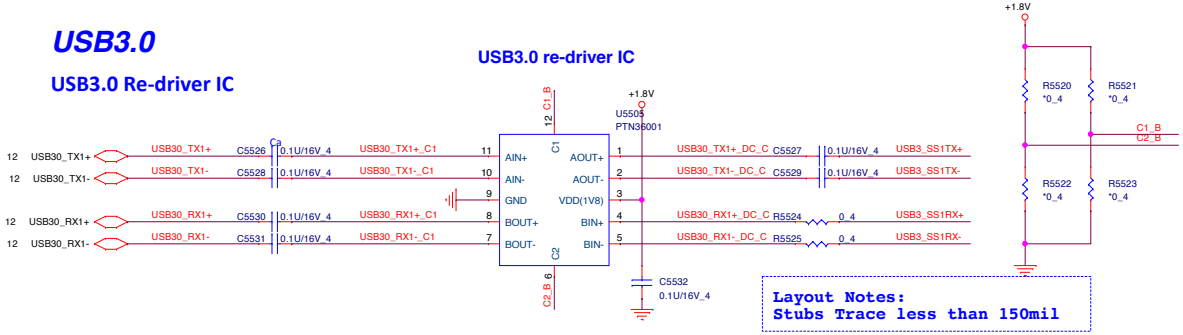
For Audio layout routing



USB3.0

USB3.0 Re-driver IC

USB3.0 re-driver IC



Layout Notes:
Stubs Trace less than 150mil

BU5

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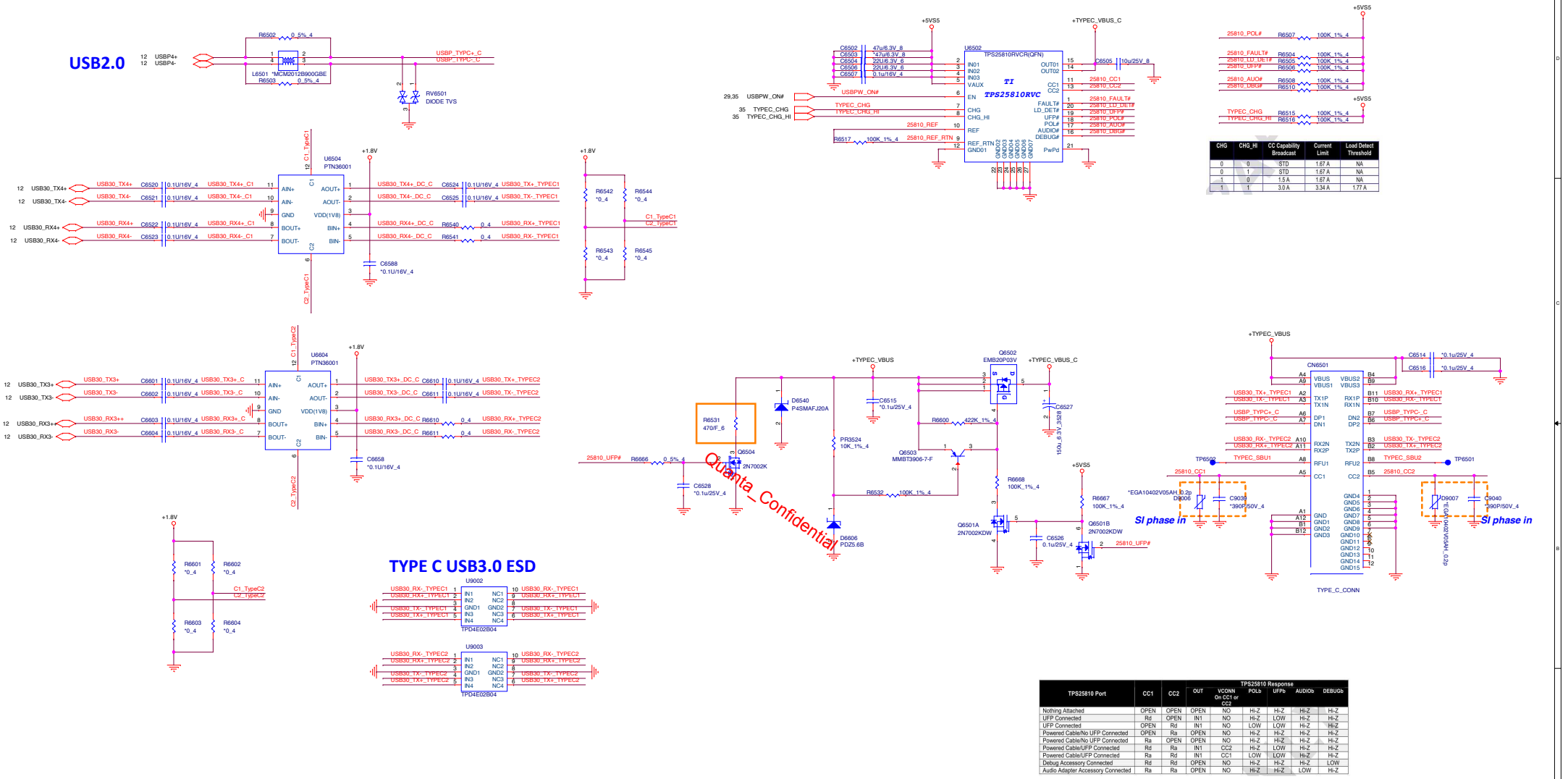
USB TYPE-C - TPS25810



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	CC1	CC2	TPS25810 Response OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

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Size	Document Number	Rev
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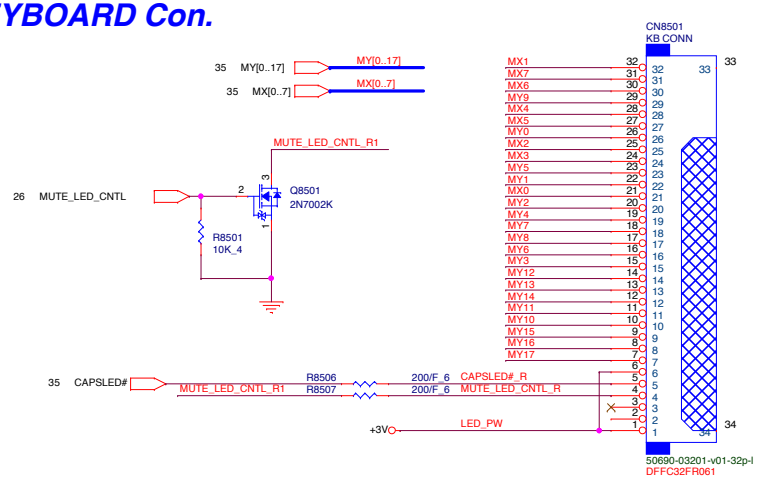
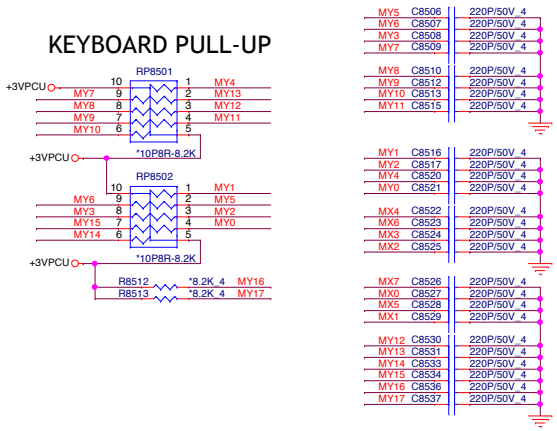
KEYBOARD Con.



KEYBOARD PULL-UP



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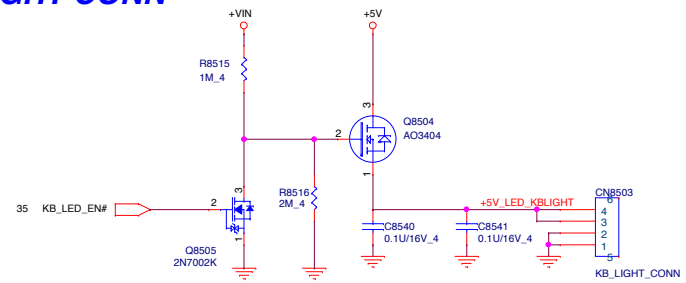
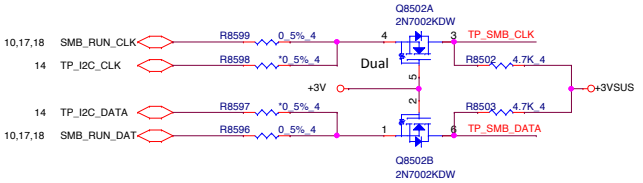
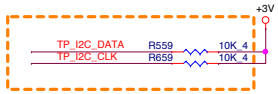
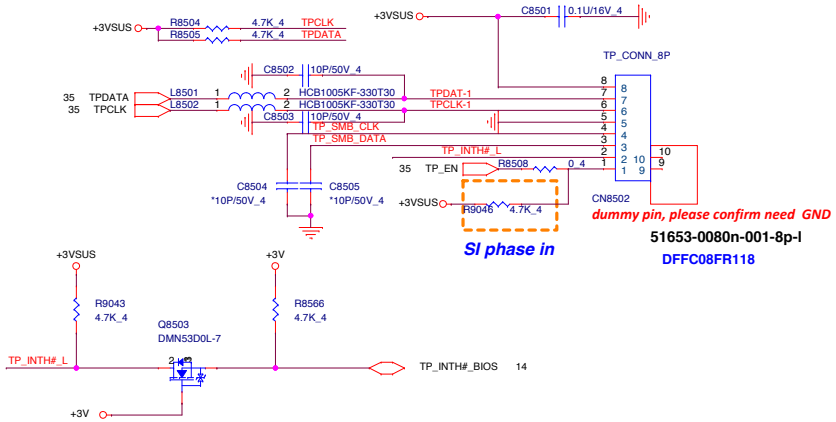
KB LIGHT CONN



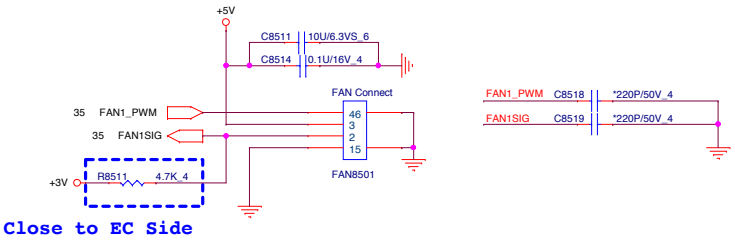
Touch Pad Connector







FAN



BU5

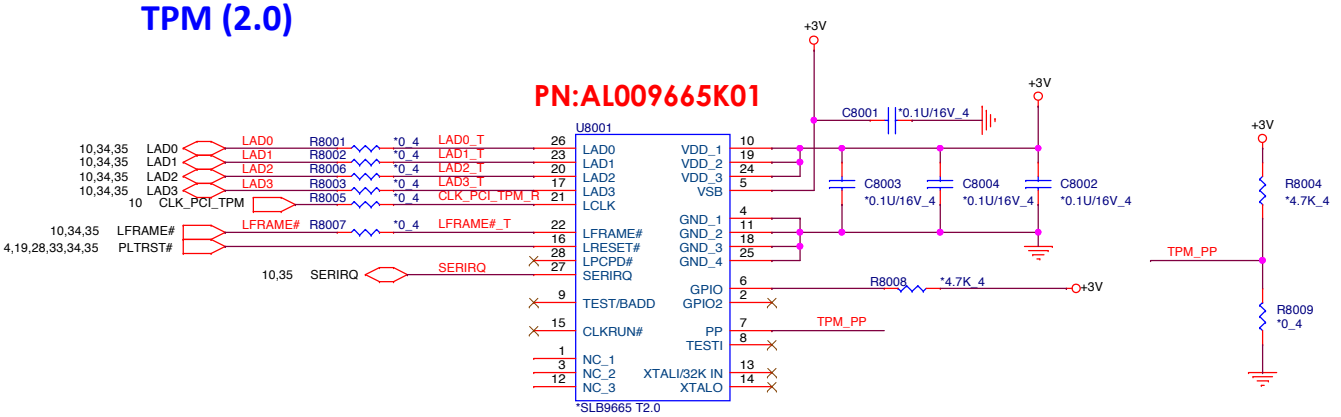
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- KB/TP/FAN	1A

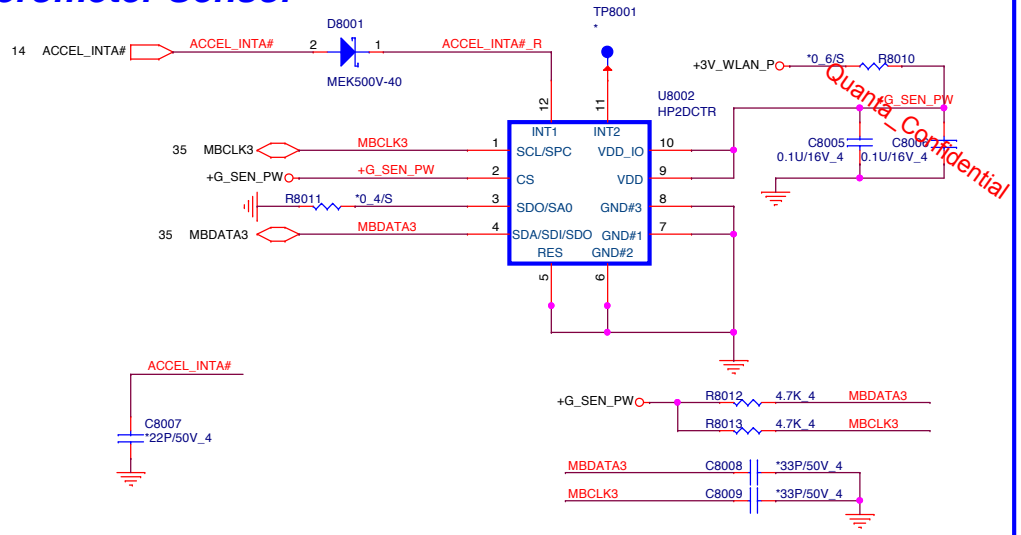
Date: Tuesday, December 13, 2016 | Sheet 31 of 49

TPM (2.0)

PN:AL009665K01

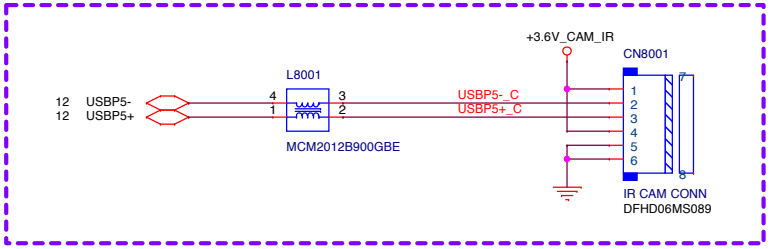


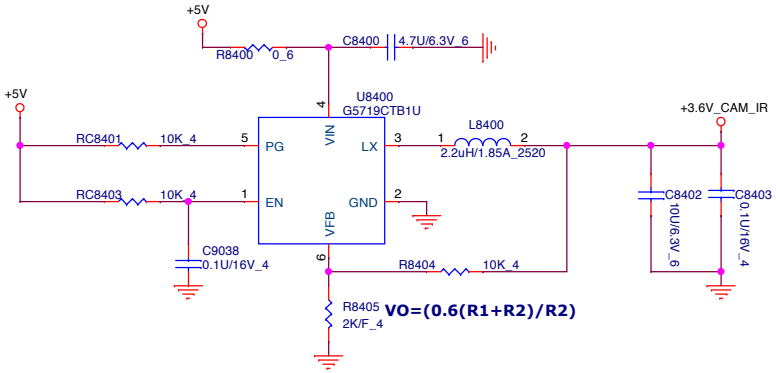
Accelerometer Sensor



IR CAM

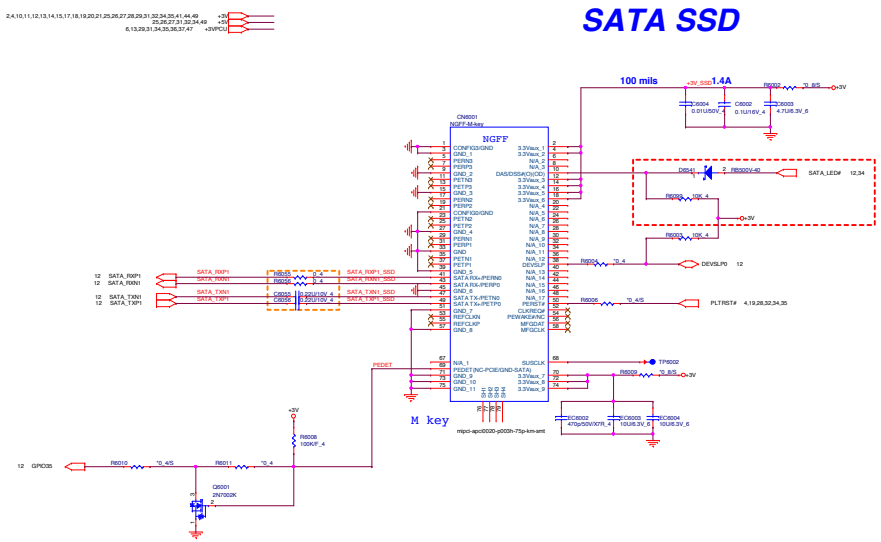
current:4A





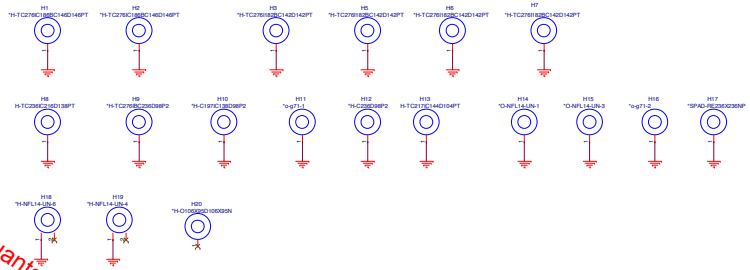
BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: 34 -- TPM/G-Sensor/IR CAM	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 32 of 49	

SATA SSD



SATA ODD

Screw Hole

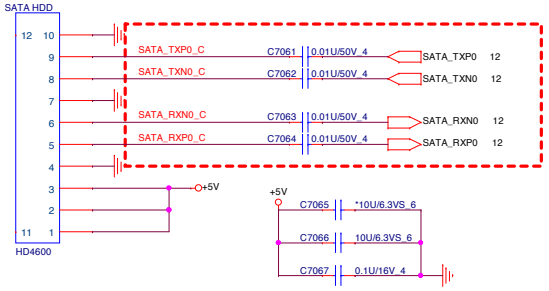


eMMC

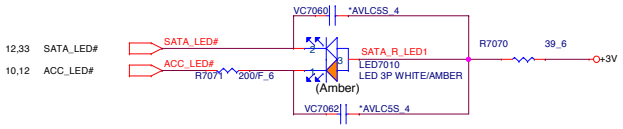
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
Size: Custom | Document Number: 35 – SSD_ODD_EMMC_ASM1154 | Rev: 1A
Date: Tuesday, December 18, 2018 | Sheet 33 of 49

HDD

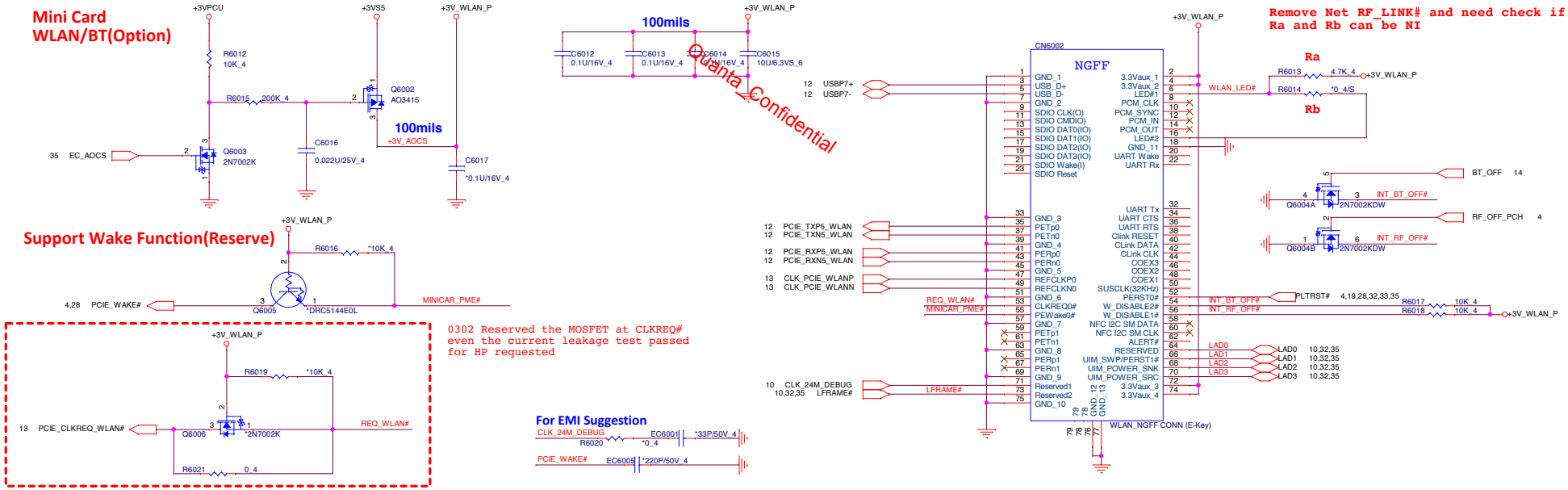
SATA HDD

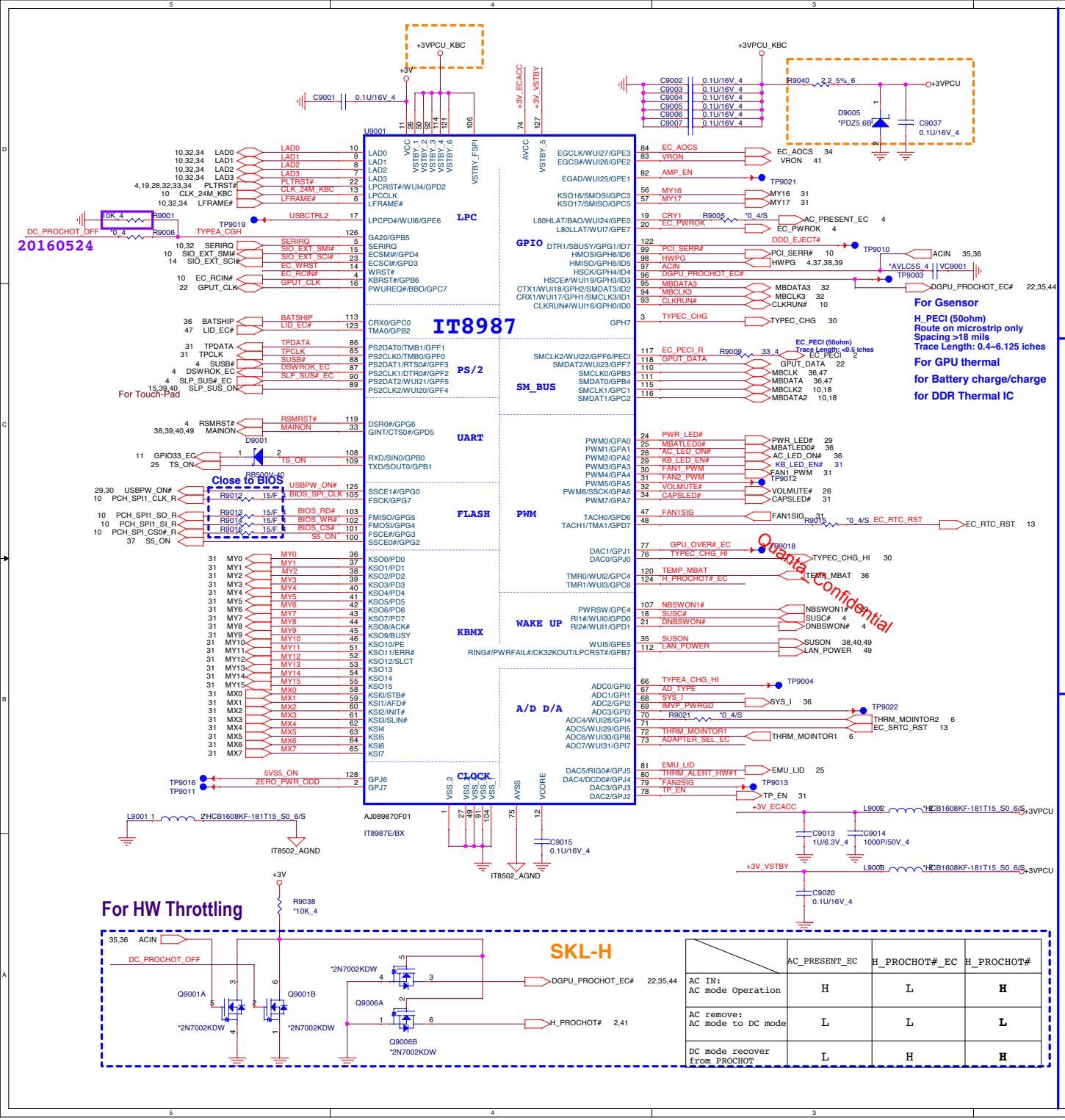


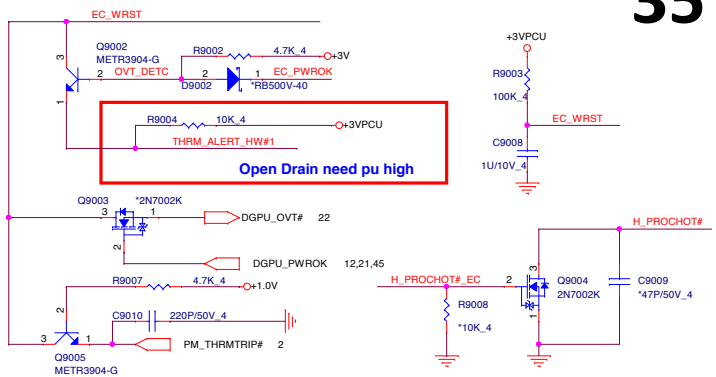
SATA LED



WLAN



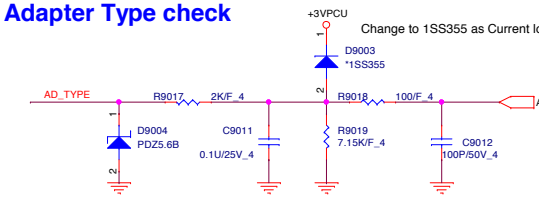


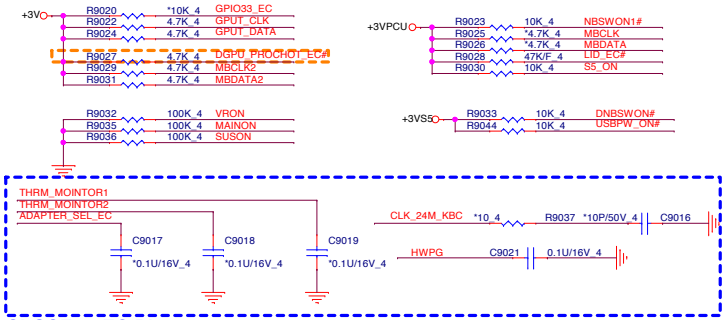


Adapter select for EC

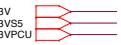
	Ra	Rb	ADAPTER_SEL_EC	BOM
200W				
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	3V	
120W	10K(CS31002FB26)		2.25V	
90W	10K(CS31002FB26)		1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB0)	0.75V	DIS
45W	NC	10K(CS31002FB26)	0V	UMA

Adapter Type check





CLOSE to EC Pin



	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

+3VPCU 6,13,29,31,34,35,36,37,47
+5VPCU 26,37,46,49
+BAT_RTC 4,13,15,29,47
+VIN 25,31,37,38,39,42,43,44,45,48
+3VPCU 6,13,29,31,34,35,36,37,47

ADP=65W

3S1P 41Whr

CN1 51483-00801-V01_Header

N-channel MOS

PQ1 AP0203GMT-HF

PQ2 AON7408

PQ3 AON6414AL

PD1 P4SMAFJ20A

PD2 *P4SMAFJ20A

Place this ZVS close to DC_IN conn

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

PU9 BQ24738HRGRR

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ACDET

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Vacdet=2.4V

Ra

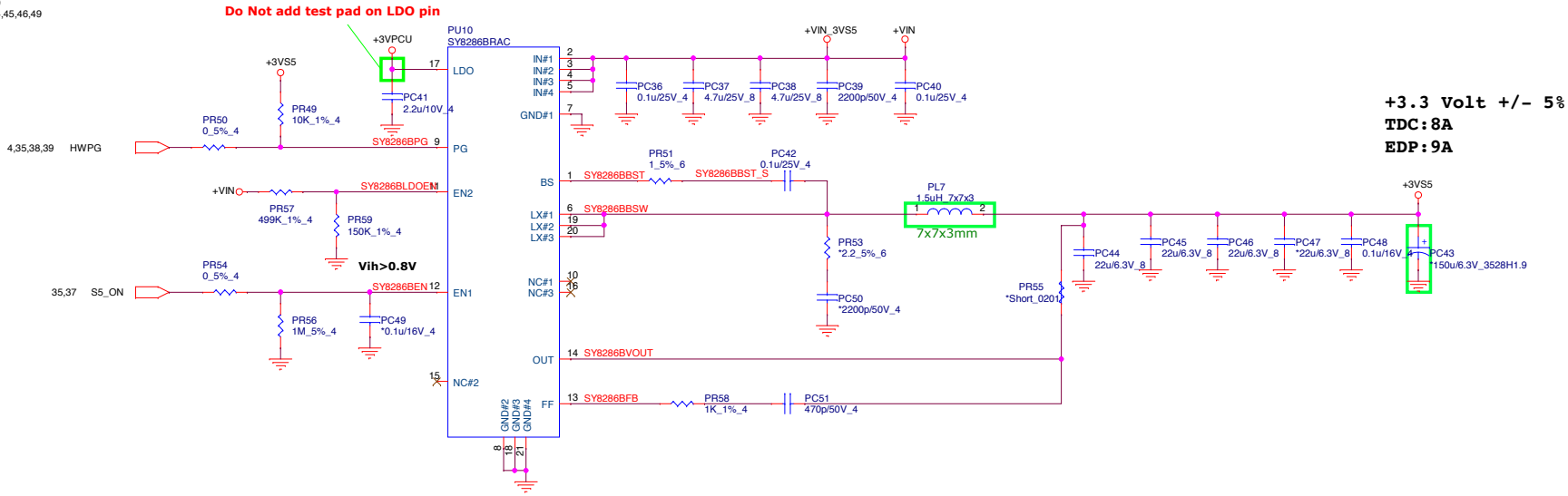
MIN. BATV=7.2V

+BAT_RTC SET
BAT= 1S---10-ohm
BAT >2S---100ohm

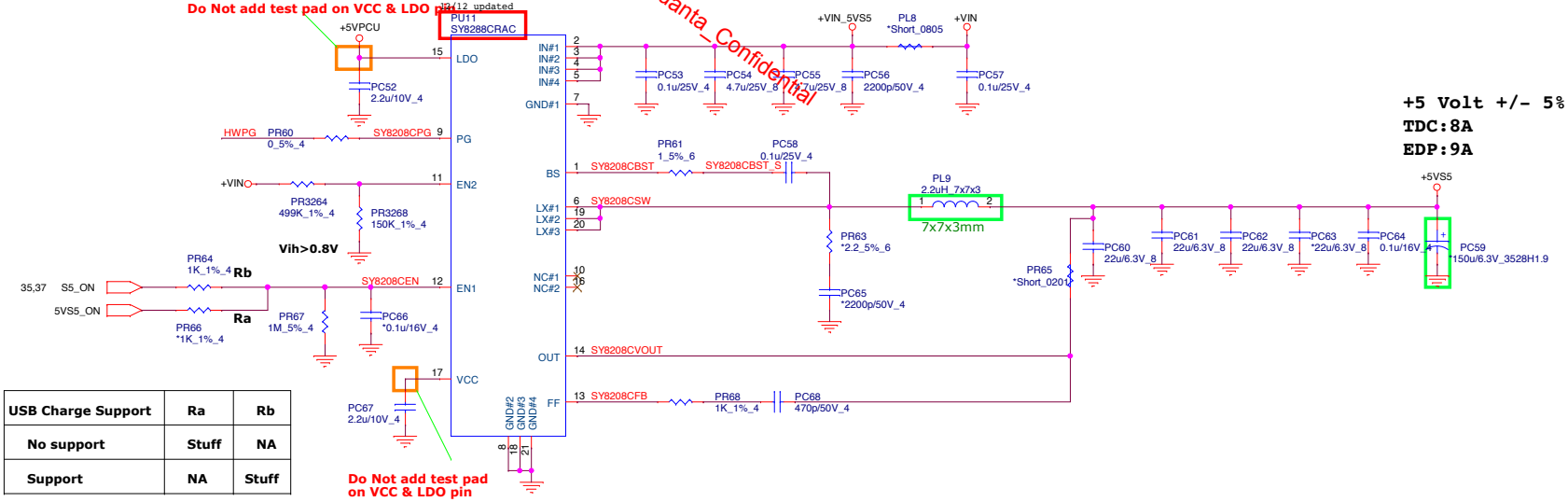
PROJECT : NFLP_KBLU_DR		
Quanta Computer Inc.		
BU5	Size: Custom	Document Number: Charger (BQ24738H) Rev: 1A
	Date: Tuesday, December 13, 2016	Sheet 36 of 49

DC/DC +3VS5/+5VS5

+VIN 25,31,36,38,39,42,43,44,45,48
+3VS5 4,10,15,34,35,38,39,40,46,49
+5VS5 4,26,29,30,38,39,40,41,42,44,45,46,49
+3VPCU 6,13,29,31,34,35,36,47
+5VPCU 26,36,46,49



+3.3 Volt +/- 5%
TDC:8A
EDP:9A



+5 Volt +/- 5%
TDC:8A
EDP:9A

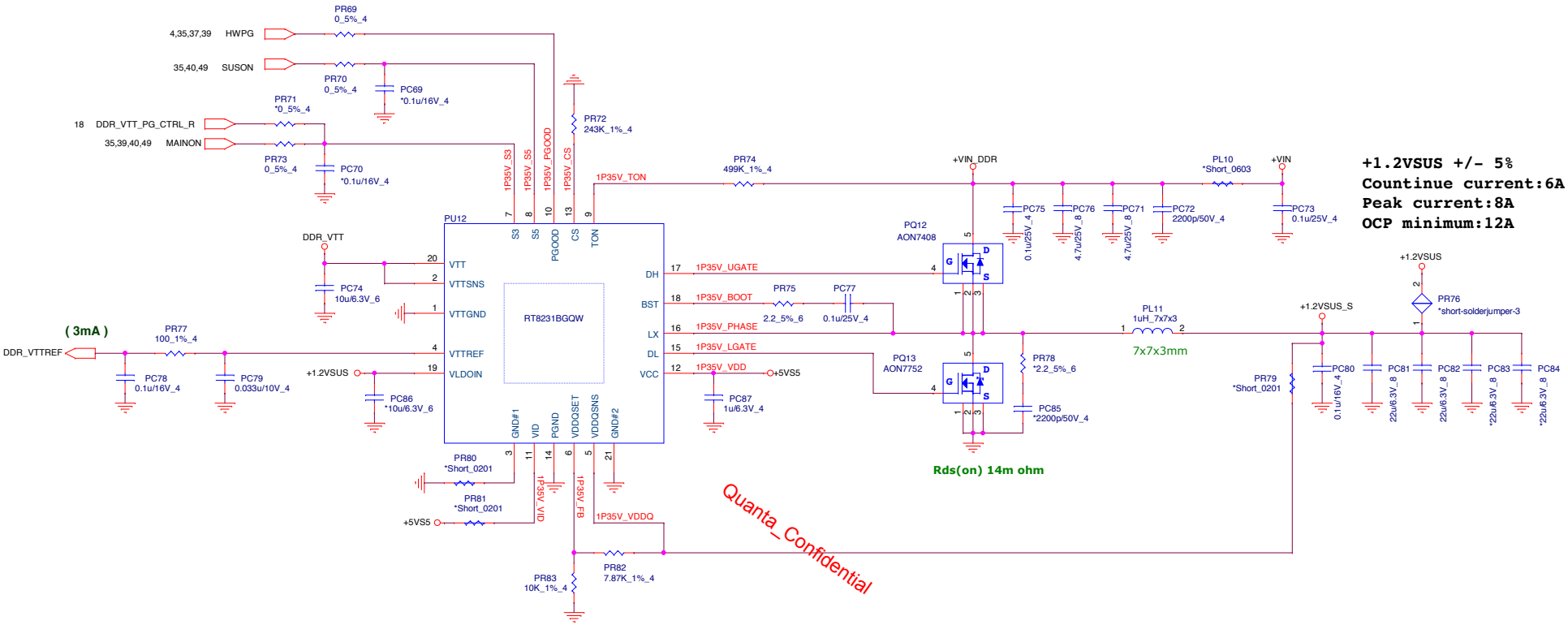
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

BU5

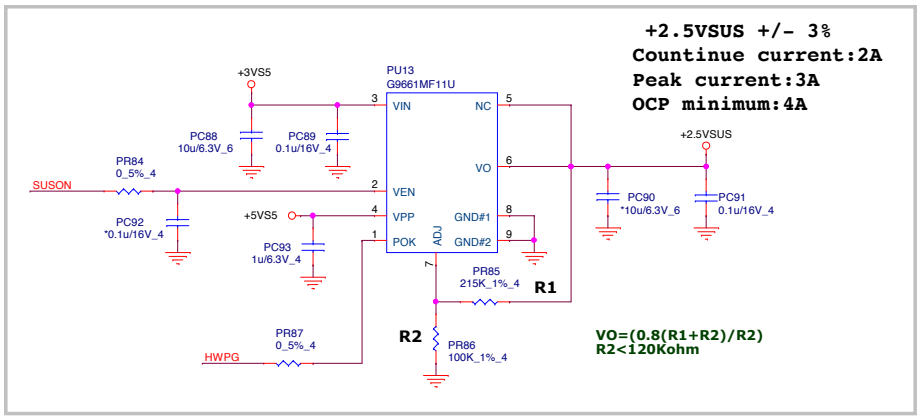
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Tuesday, December 13, 2016	Sheet 37 of 49	

+VIN 25,31,36,37,39,42,43,44,45,48
+5VS5 4,26,29,30,37,39,40,41,42,44,45,46,49
+1.2VSUS 3,6,17,18,40,46
DDR_VTT 17,18



20151015 updated

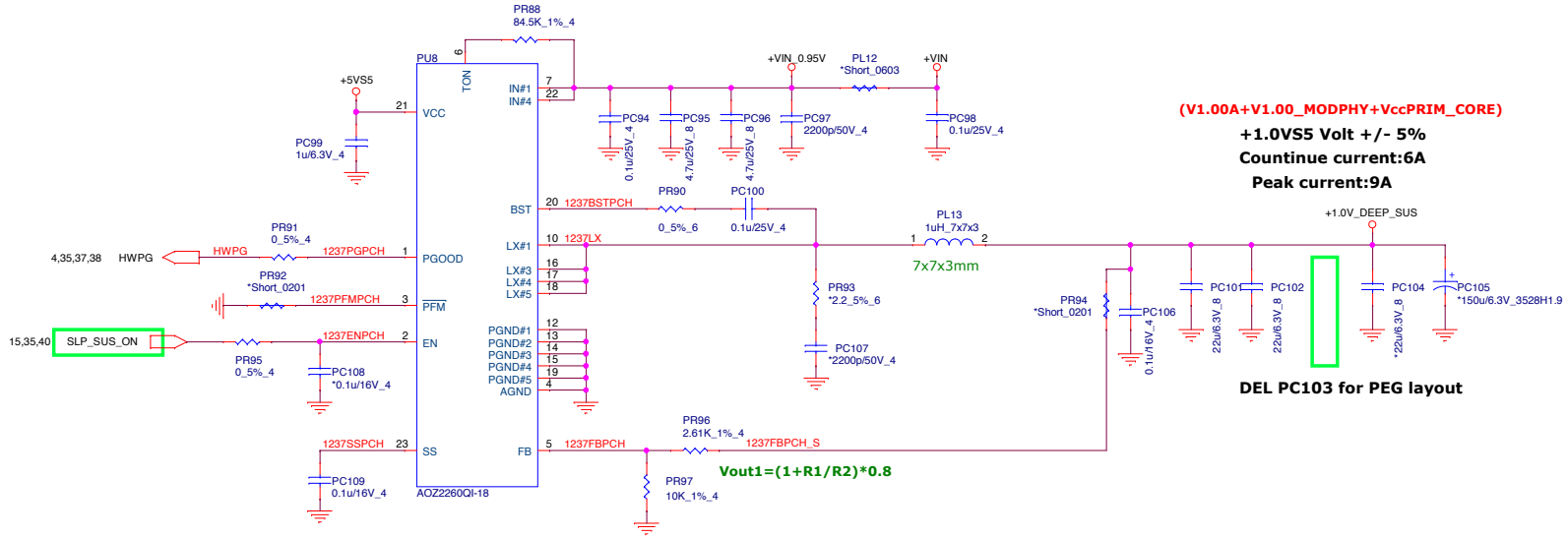


PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
	DDR4 (G5619RZ1U)	1A
Date: Tuesday, December 13, 2016	Sheet 38 of 49	

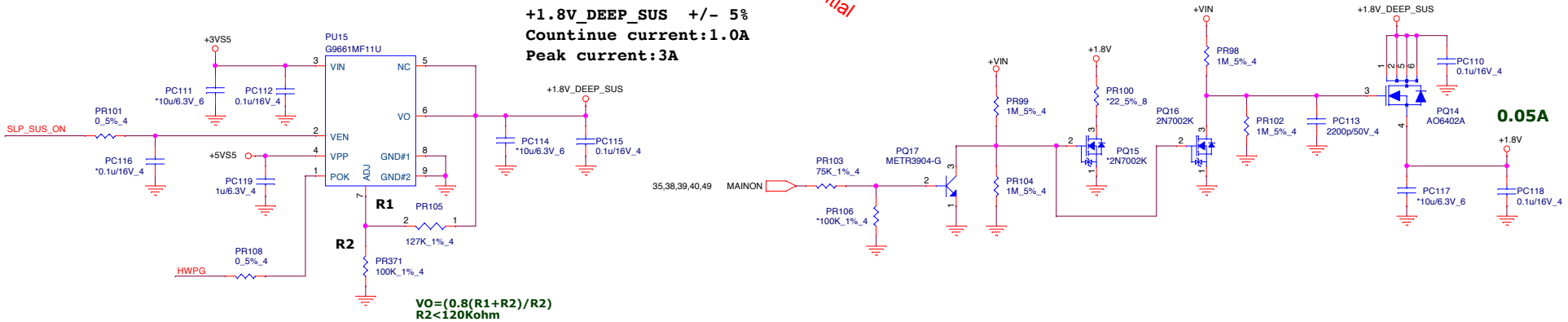
BU5

+VIN 25,31,36,37,38,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,40,46,49
+5VS5 4,26,29,30,37,38,40,41,42,44,45,46,49
+1.0V_DEEP_SUS 9,13,15,40
+1.8V_DEEP_SUS 9,15
MAINON 35,38,39,40,49
+1.5V



Quanta_Confidential

+1.8V_DEEP_SUS +/- 5%
Countinue current:1.0A
Peak current:3A

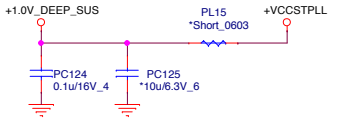


+1.0V 2,4,6,35
+3VS5 4,10,15,34,35,37,38,39,46,49
+5VS5 4,26,29,30,37,38,39,41,42,44,45,46,49
+VCCIO 2,6
+1.2VSUS 3,6,17,18,38,46
+VCCSTPLL 2,4,5,6,9,41
+1.0V_DEEP_SUS 9,13,15,39
+1.2V_VCCPLL_OC 6
MAINON 35,38,39,49

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

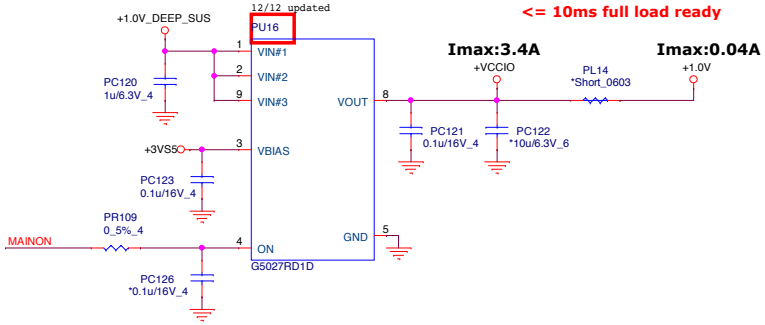
Imax:0.24A

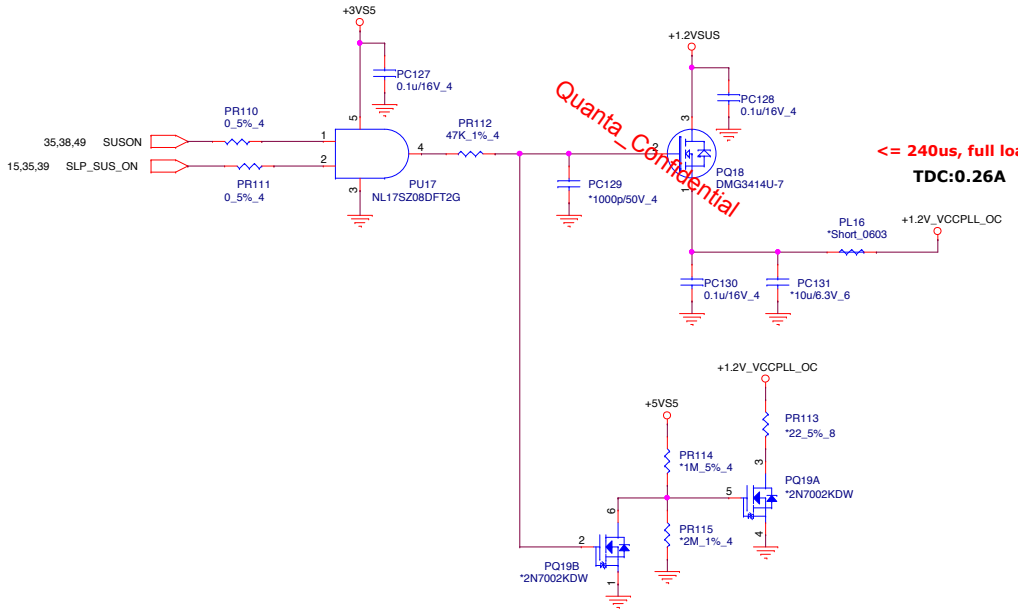


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**





<= 240us, full load ready
TDC:0.26A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
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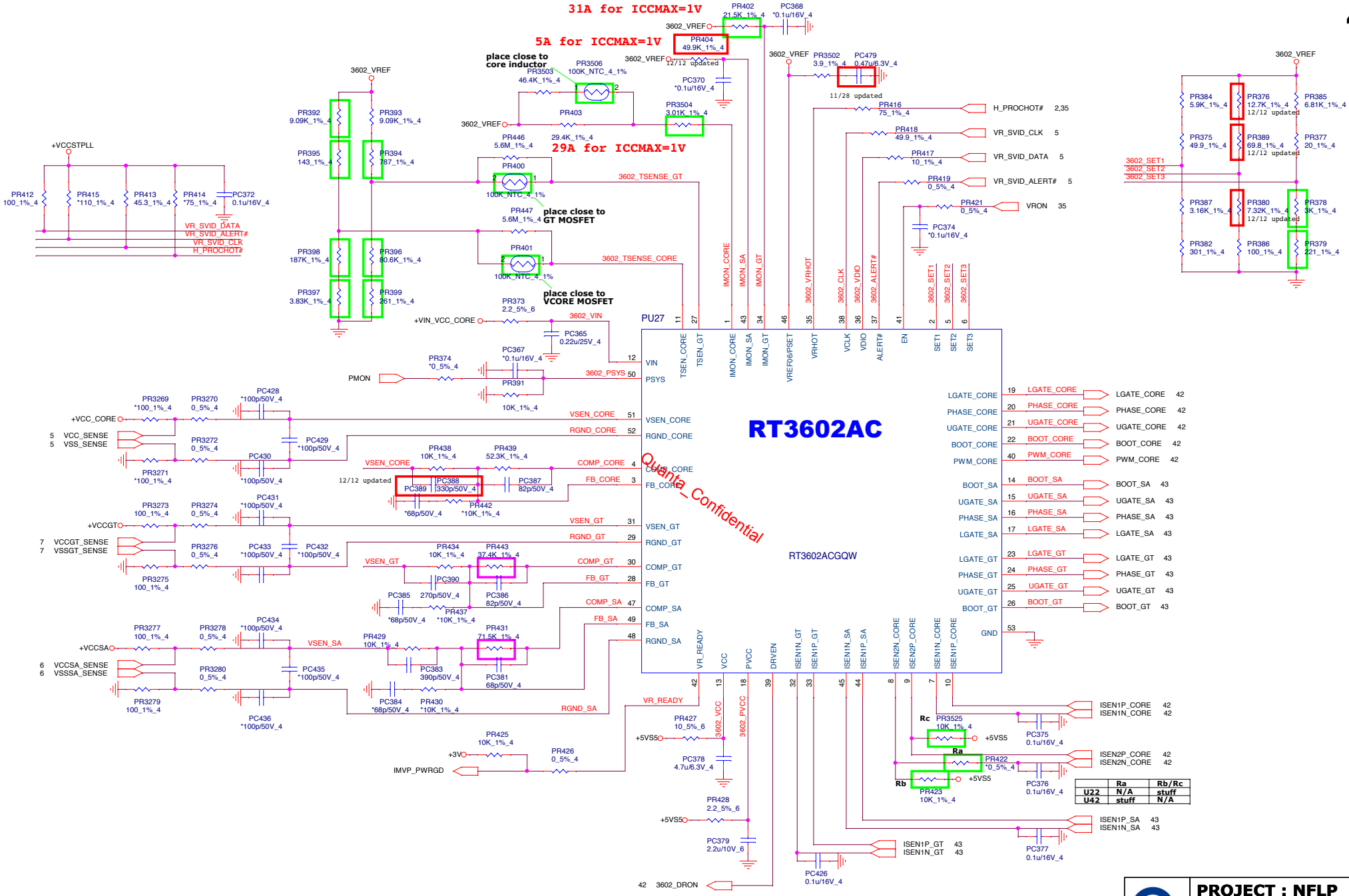

PROJECT	NFLP_KBLU_DR
	Quanta Computer Inc.
Size	Custom
Document Number	CPU VR IC (RT3602AC)
Rev	2A
Date:	Tuesday, December 13, 2016
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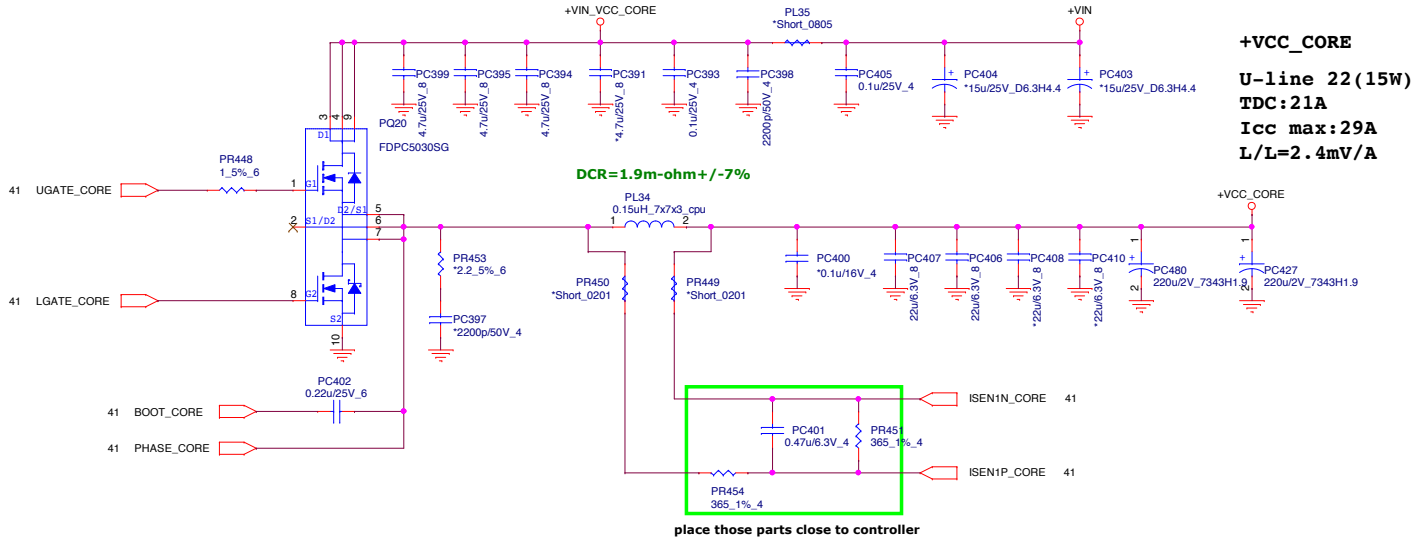
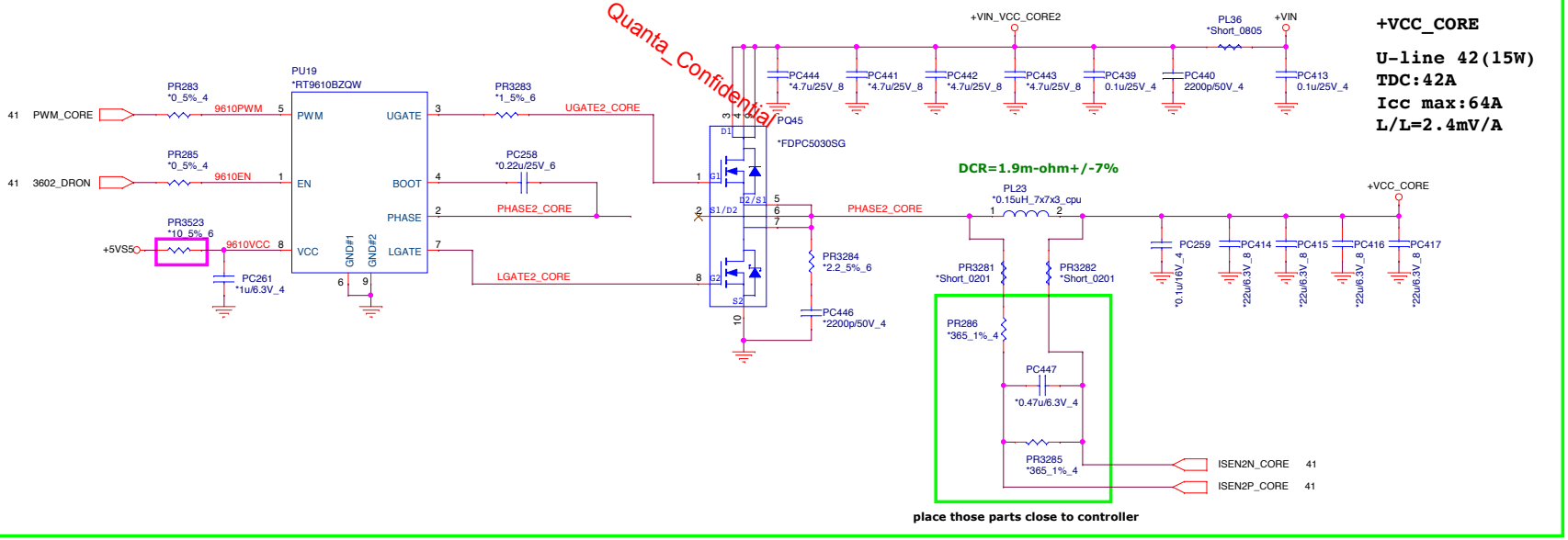
BU5

+VIN 25,31,36,37,38,39,43,44,45,48
+5VS5 4,26,29,30,37,38,39,40,41,44,45,46,49

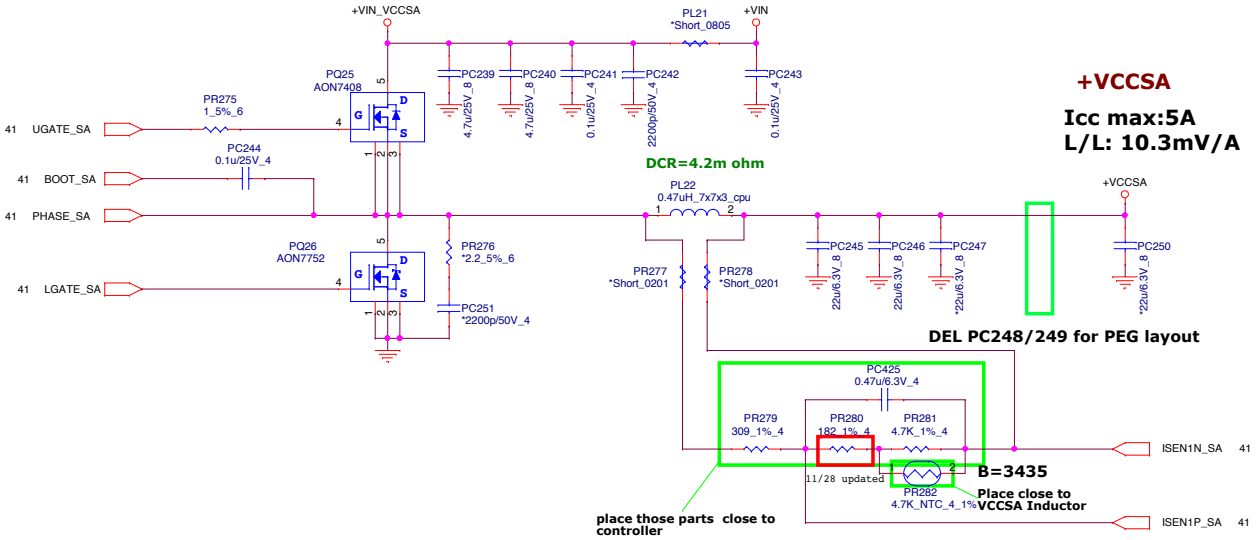


For U42 --> Add These Components

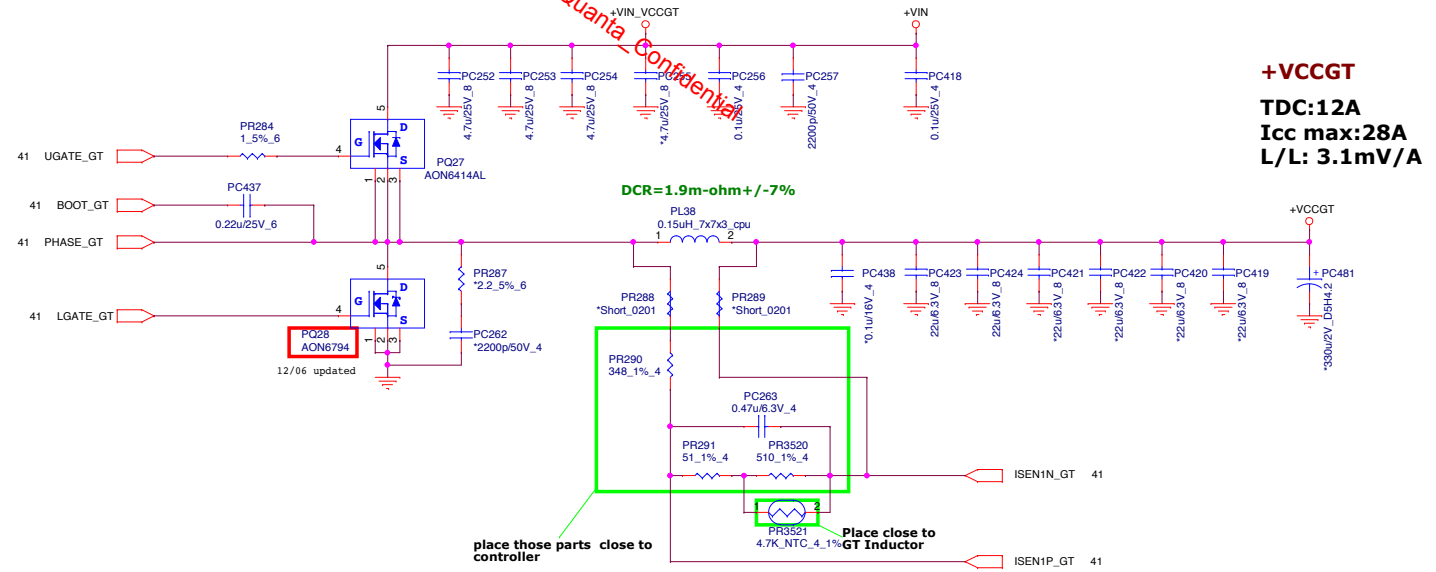


BU5	PROJECT : NFLP_KBLU_DR Quanta Computer Inc.	
Size: Custom	Document Number: +VCCSA (NCP81253)	Rev: 2A
Date: Tuesday, December 13, 2016	Sheet 42 of 49	

+VIN 25,31,36,37,38,39,42,44,45,48
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,46,49
+VCCSA 6,41
+VCCGT 7,41



+VCCSA
Icc max:5A
L/L: 10.3mV/A



+VCCGT
TDC:12A
Icc max:28A
L/L: 3.1mV/A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A

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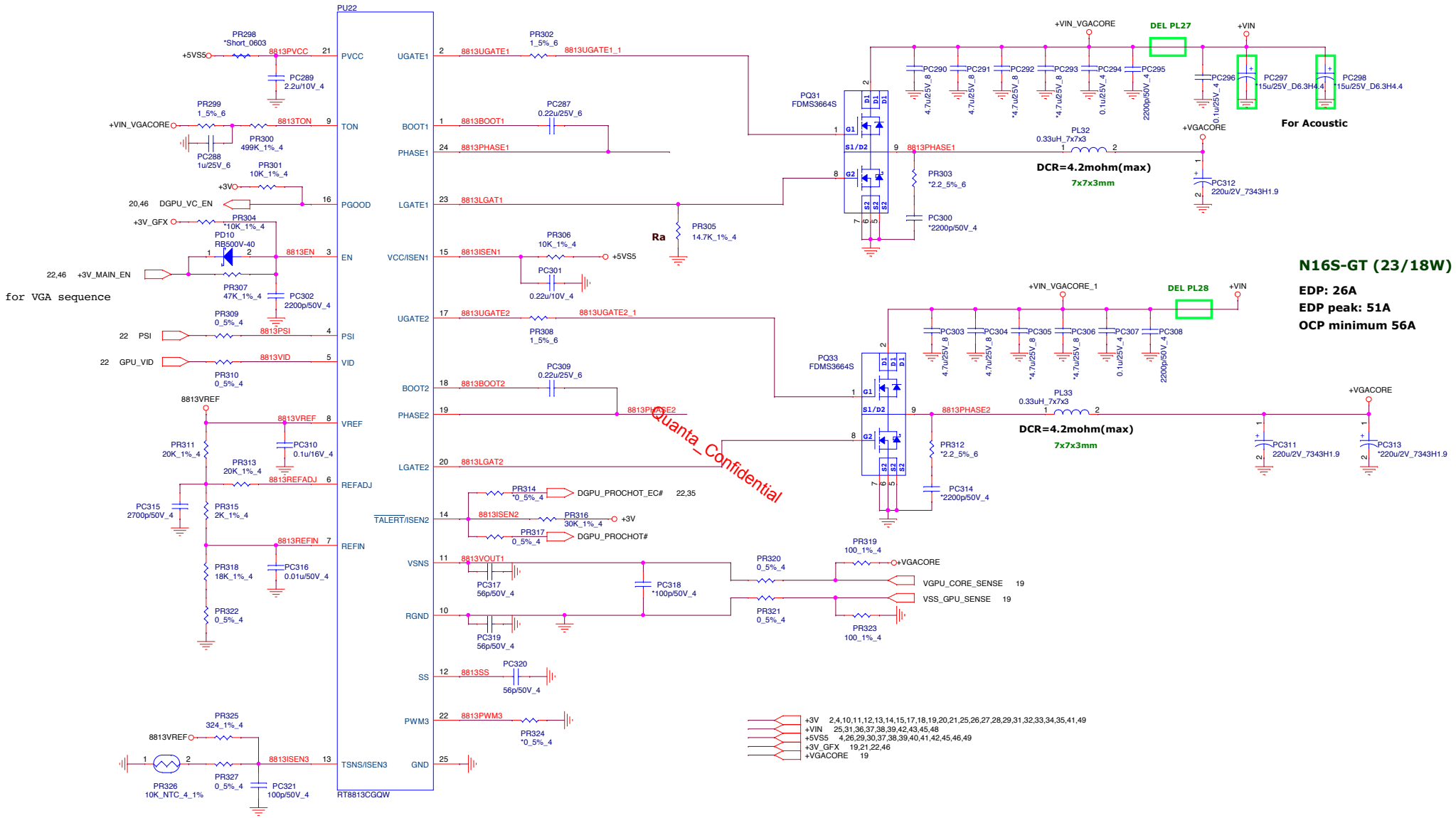
VGA Core



N16S-GT (23/18W)

EDP: 26A

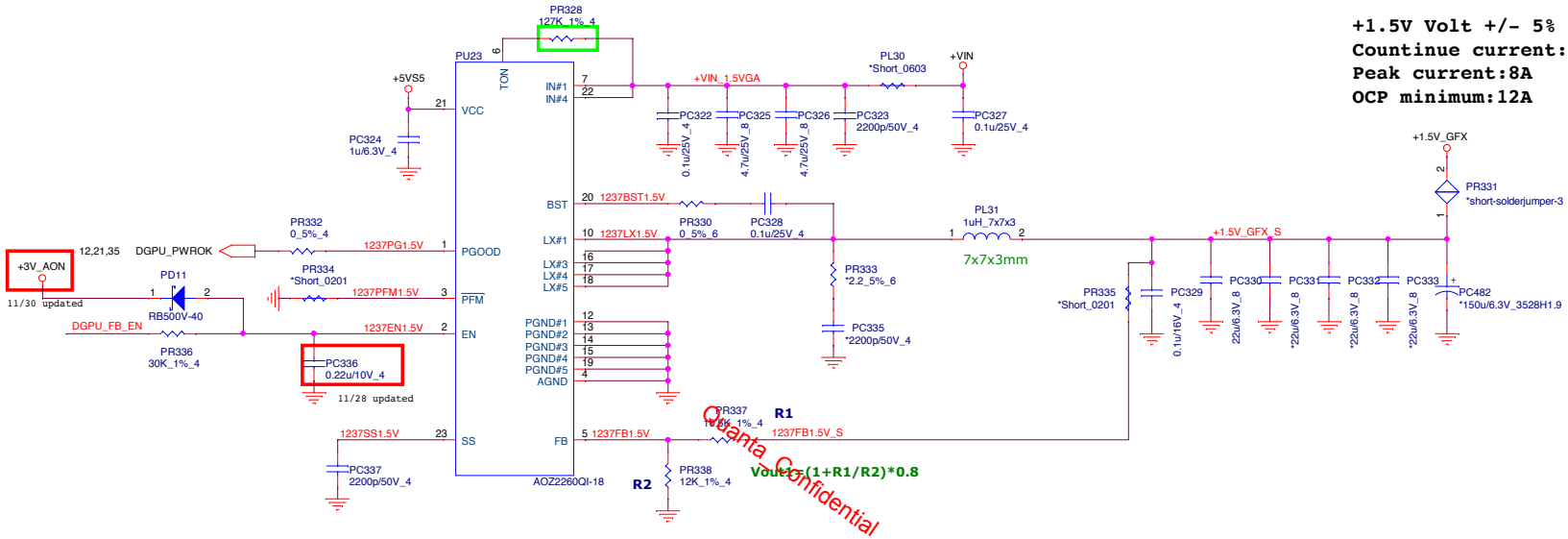
EDP peak: 51A

OCP minimum 56A

BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size Custom	Document Number **+VGACORE (RT8813C)**	Rev 2A
Date: Tuesday, December 13, 2016	Sheet 44 of 49	

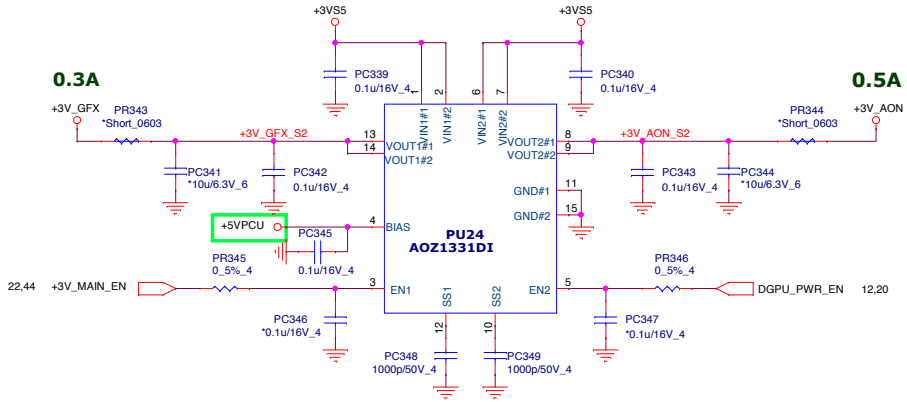
+VIN 25,31,36,37,38,39,42,43,44,48
+5VS5 4,26,29,30,37,38,39,40,41,42,44,46,49
+1.5V_GFX 20,23,24

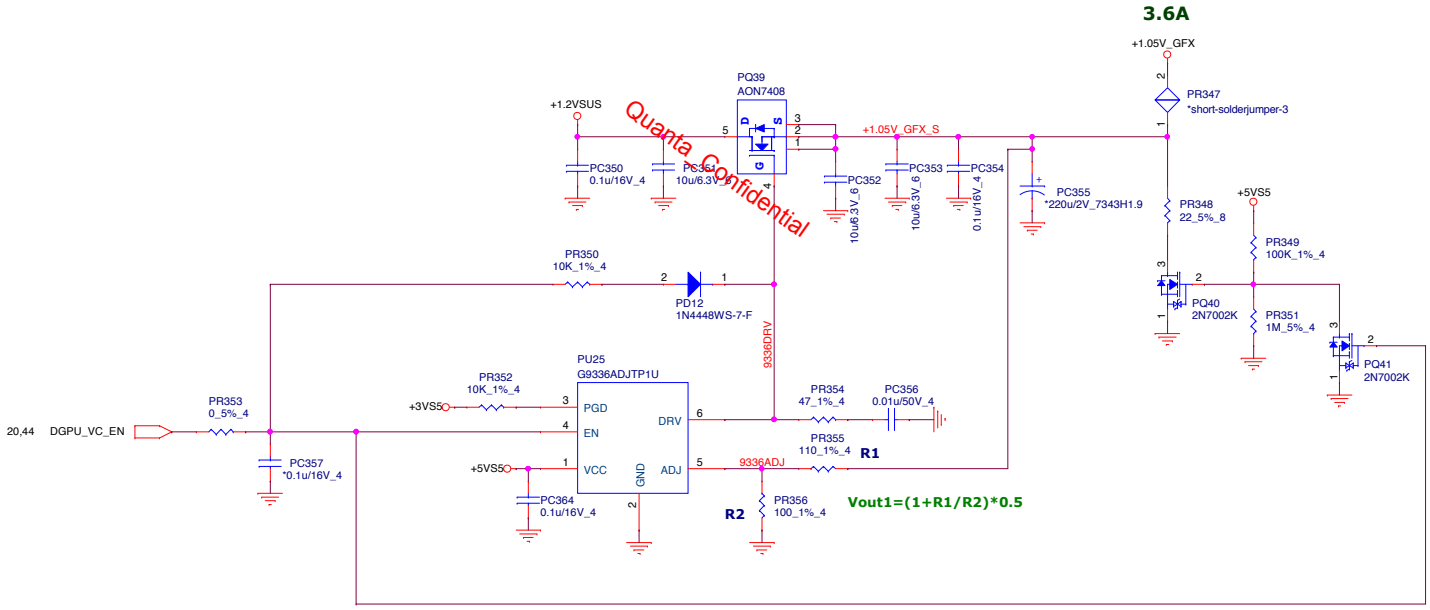
+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size: Custom	Document Number: +1.5V_GFX (AOZ2260QI-18)	Rev: 1A
Date: Tuesday, December 13, 2016	Sheet 45 of 49	

+VIN 25,31,36,37,38,39,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,39,40,49
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,49
+3V_GFX 19,21,22,44
+3V_AON 19,22,45
+1.2VSUS 3,6,17,18,38,40
+1.05V_GFX 19,20,21



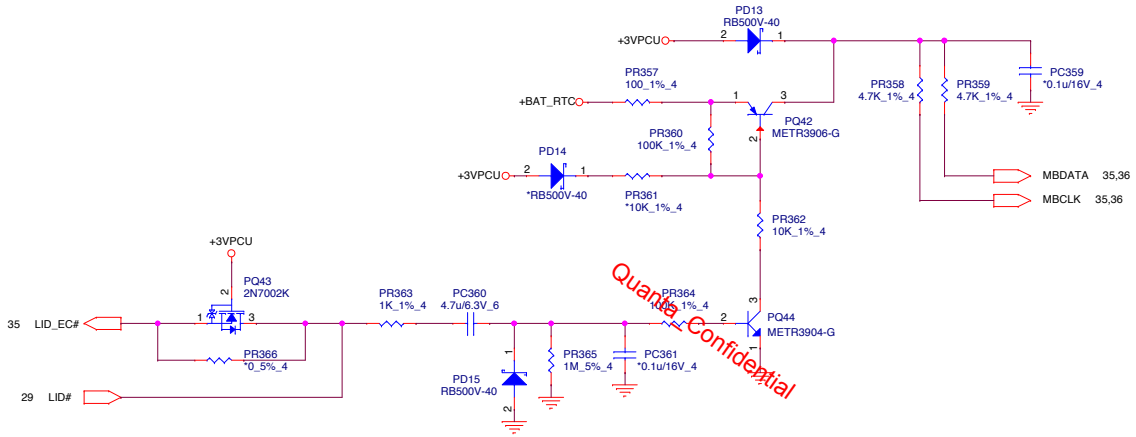


BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(APL3523A)	1A
Date: Tuesday, December 27, 2016	Sheet 46 of 49	

+3VPCU 6,13,29,31,34,35,36,37
+BAT_RTC 4,13,15,29,36

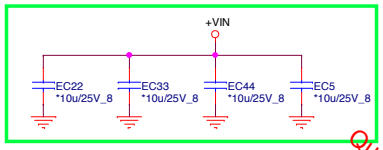


BU5

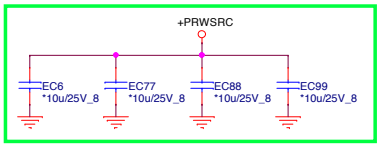
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LID SW for storage mode	1A
Date: Tuesday, December 13, 2016	Sheet 47 of 49	

EMI request for ISN



EMI request for ISN

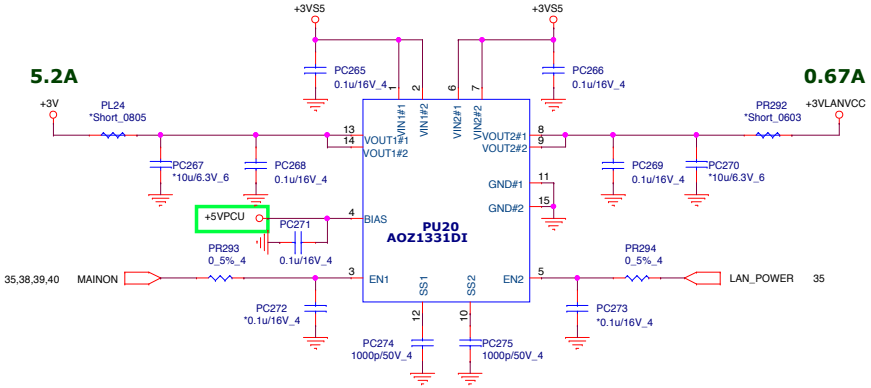


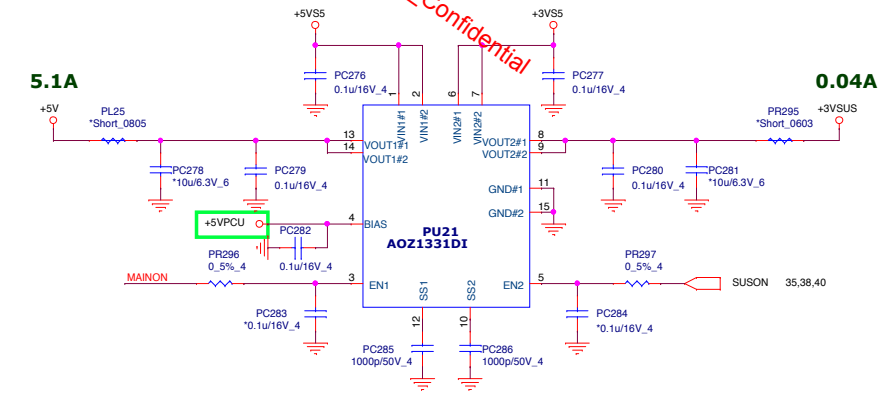
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI solution	1A
Date: Tuesday, December 13, 2016	Sheet 48 of 49	

+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,25,26,27,28,29,31,32,33,34,35,41,44
+5V 25,26,27,31,32,34
+VIN 25,31,36,37,38,39,42,43,44,45,48
+3VS5 4,10,15,34,35,37,38,39,40,46
+5VS5 4,26,29,30,37,38,39,40,41,42,44,45,46
+3VSUS 31
+5VPCU 26,36,37,46
+3VLANVCC 28





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
Date: Tuesday, December 13, 2016	Sheet 49 of 49	