COMPAL CONFIDENTIAL

MODEL NAME : ADM80

PCB NO : DAA000AD000

BOM P/N : 4319XY31L01/L02

Park City 12" UMA

Skylake U

2015-09-25

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

X76@ : SATA REDRIVER OPTION

MB.PCB

Part Number	Description
DAA000AD000	PCB 1DK LA-C642P REV0 MB

Layout Dell logo

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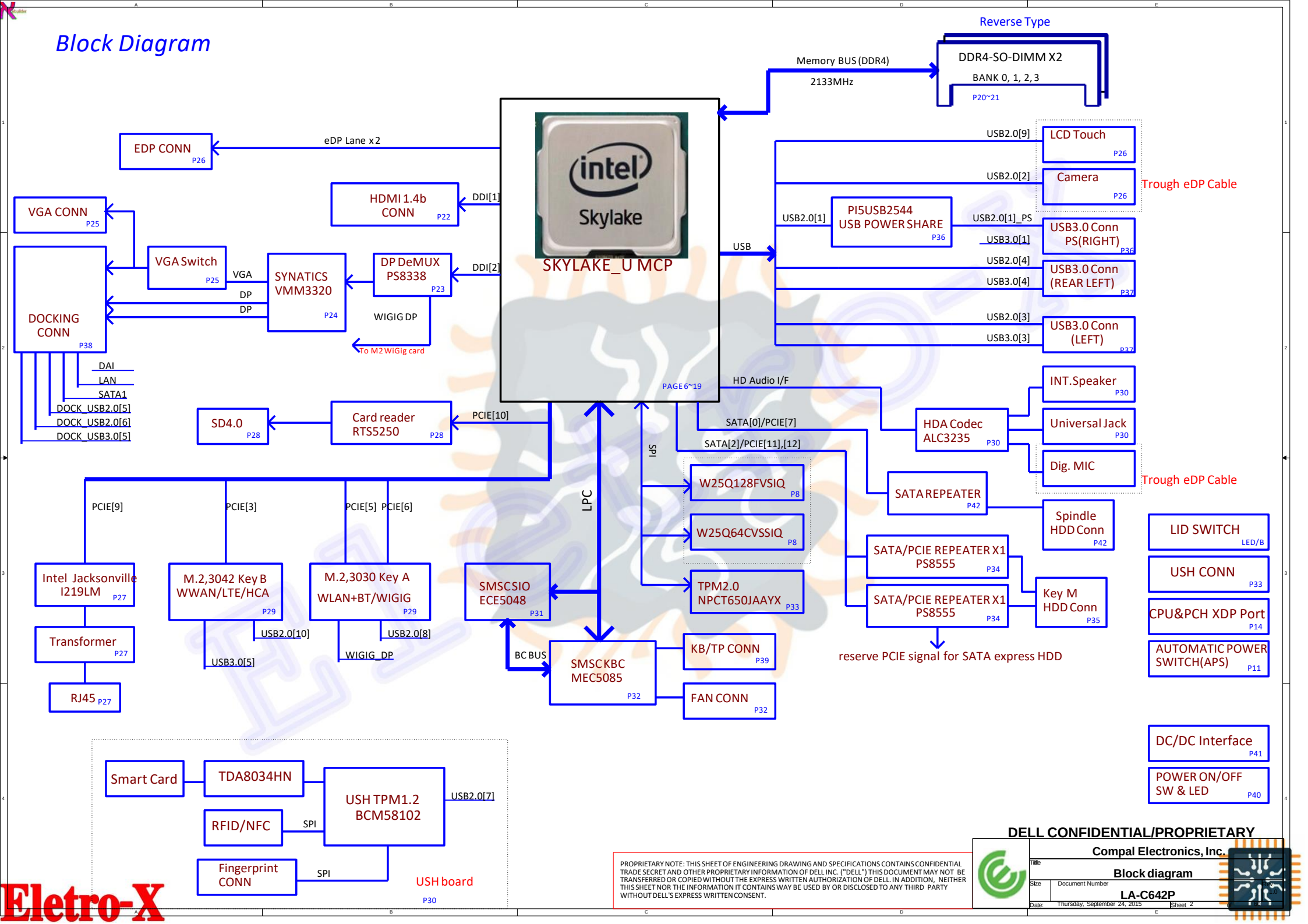
Compal Electronics, Inc.

Title: Cover Sheet

Size: Document Number: LA-C642P Rev: 1.0

Date: Thursday, September 24, 2015 Sheet 1 of

Block Diagram

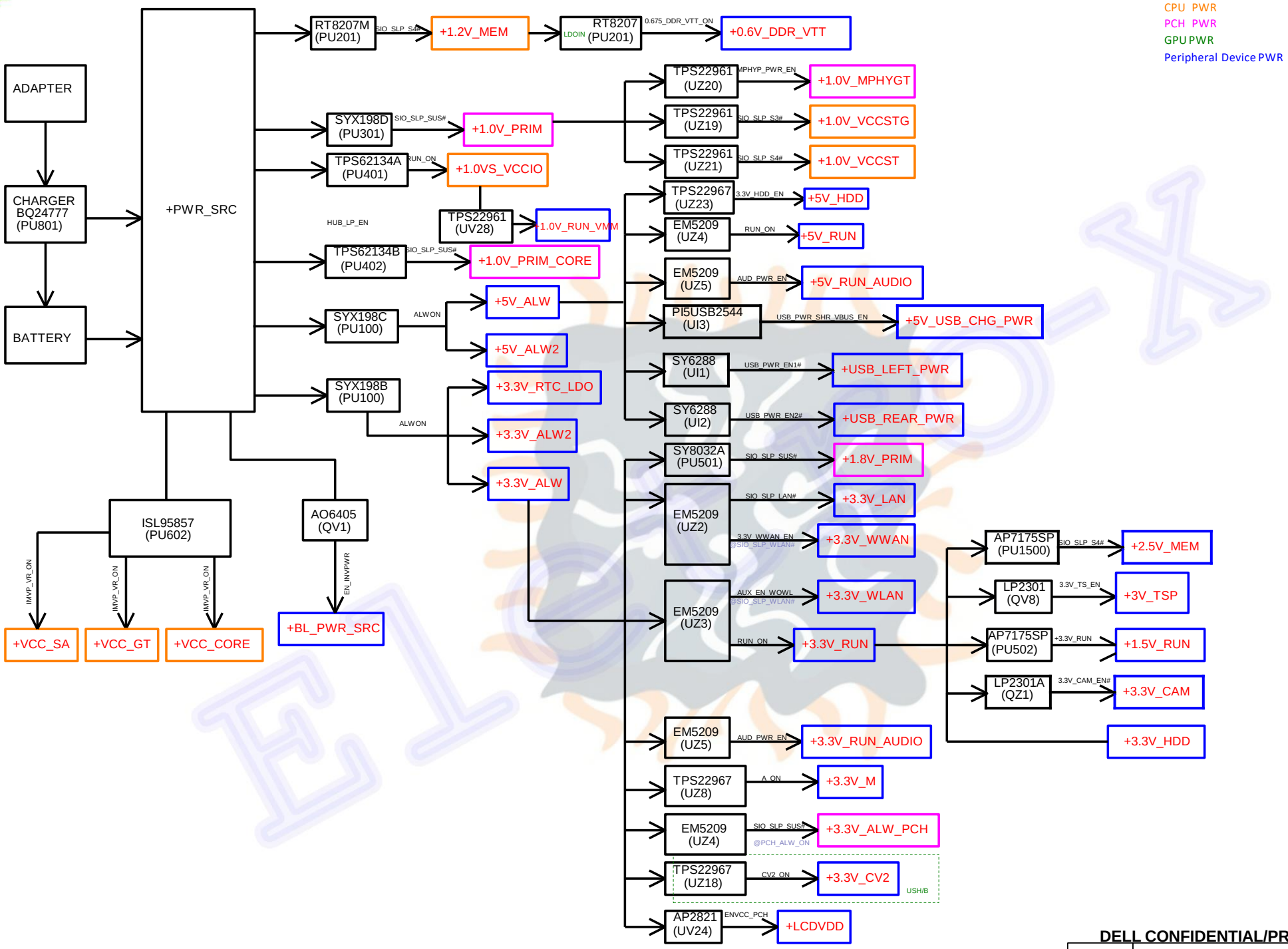


Compal Electronics, Inc.

Title: Block diagram

Size: | Document Number: LA-C642P | Rev: 1.0

Date: Thursday, September 24, 2015 | Sheet 2



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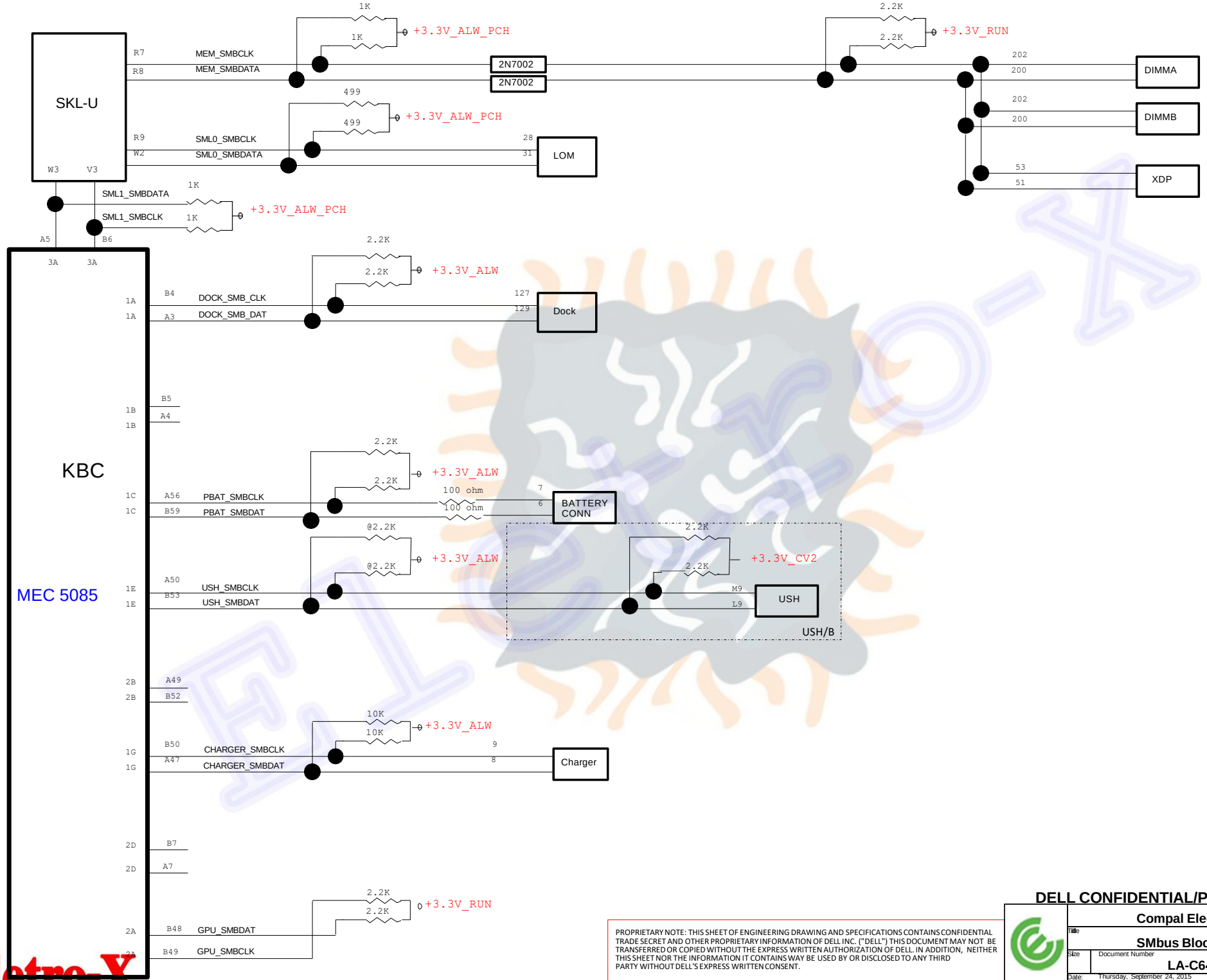
Compal Electronics, Inc.

Title	Power rails	
Size	Document Number	LA-C642P
Date: Thursday, September 24, 2015	Sheet 4	of



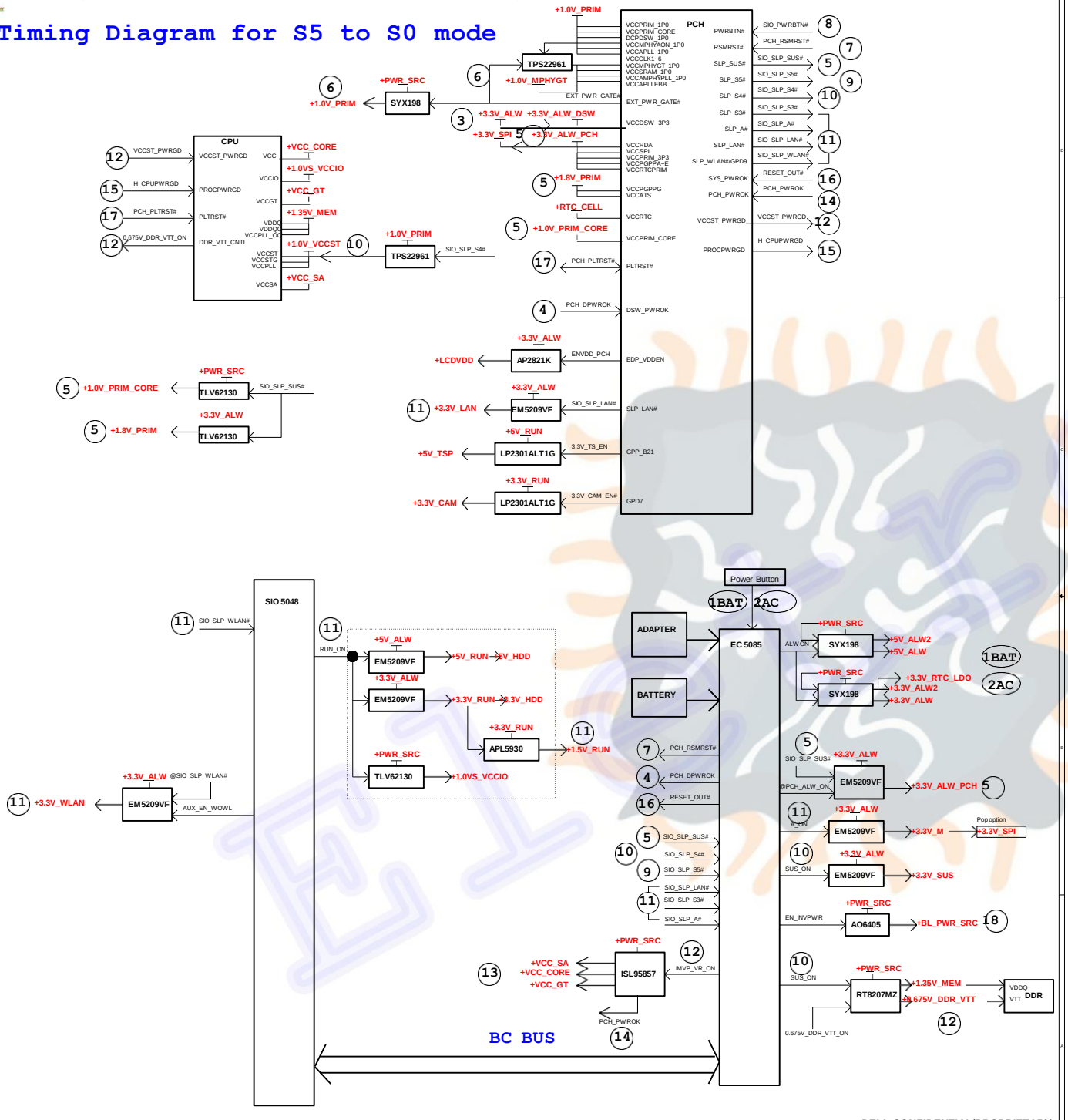
Compal Electronics, Inc.

Title: SMbus Block diagram

Size: | Document Number: LA-C642P

Date: Thursday, September 24, 2015 | Sheet 5 of

Timing Diagram for S5 to S0 mode



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Compal Electronics, Inc.

Power Sequence

LA-C631P,C641P

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN	+3.3V_M	(M-OFF) +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	TU662	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.8
		3.7	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.67
3	IN 1		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.67
5	IN 2		Copper foil	1oz	1.25
		3.8	Prepreg	1080H x2	4.4
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.67
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.67
9	GND		Copper foil	1oz	1.25
		3.7	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.8
			Add Plating		
			SolderMask	TU662	0.5
Overall Thickness (1.2mm ± 10%)					48.28000 1.226312

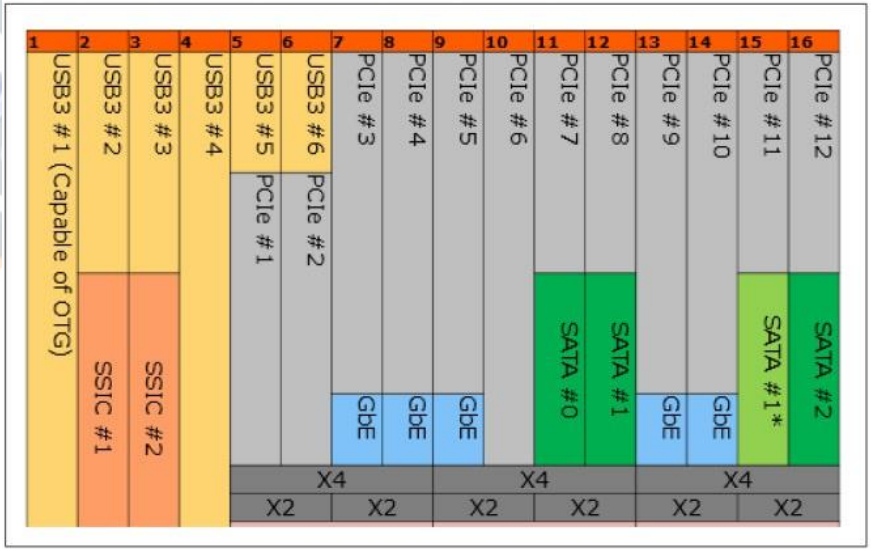
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right
USB3.0-2	SSIC-1			EDOCK PORT1
USB3.0-3	SSIC-2			JUSB1-->LEFT
USB3.0-4				JUSB2-->Rear LEFT
USB3.0-5		PCIE-1		M2 3042(WWAN)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3042(HCA or QCA LTE)
		PCIE-4		NA
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	HDD SATA
		PCIE-8	SATA-1	EDOCK E-SATA
		PCIE-9		LOM
		PCIE-10		Card Reader
		PCIE-11	SATA-1*	M.2 Socket 3 (Key M) (PCIex2 or SATA)
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	Camera
3	JUSB2-->LEFT
4	JUSB3-->Rear LEFT
5	EDOCK PORT1
6	EDOCK PORT2
7	USH
8	M.2 304230(BT)
9	Touch Screen
10	M2 3042(WWAN)

USH	0	BIO
	1	NA

Check

High Speed I/O (HSIO) Lane Multiplexing in SKL U



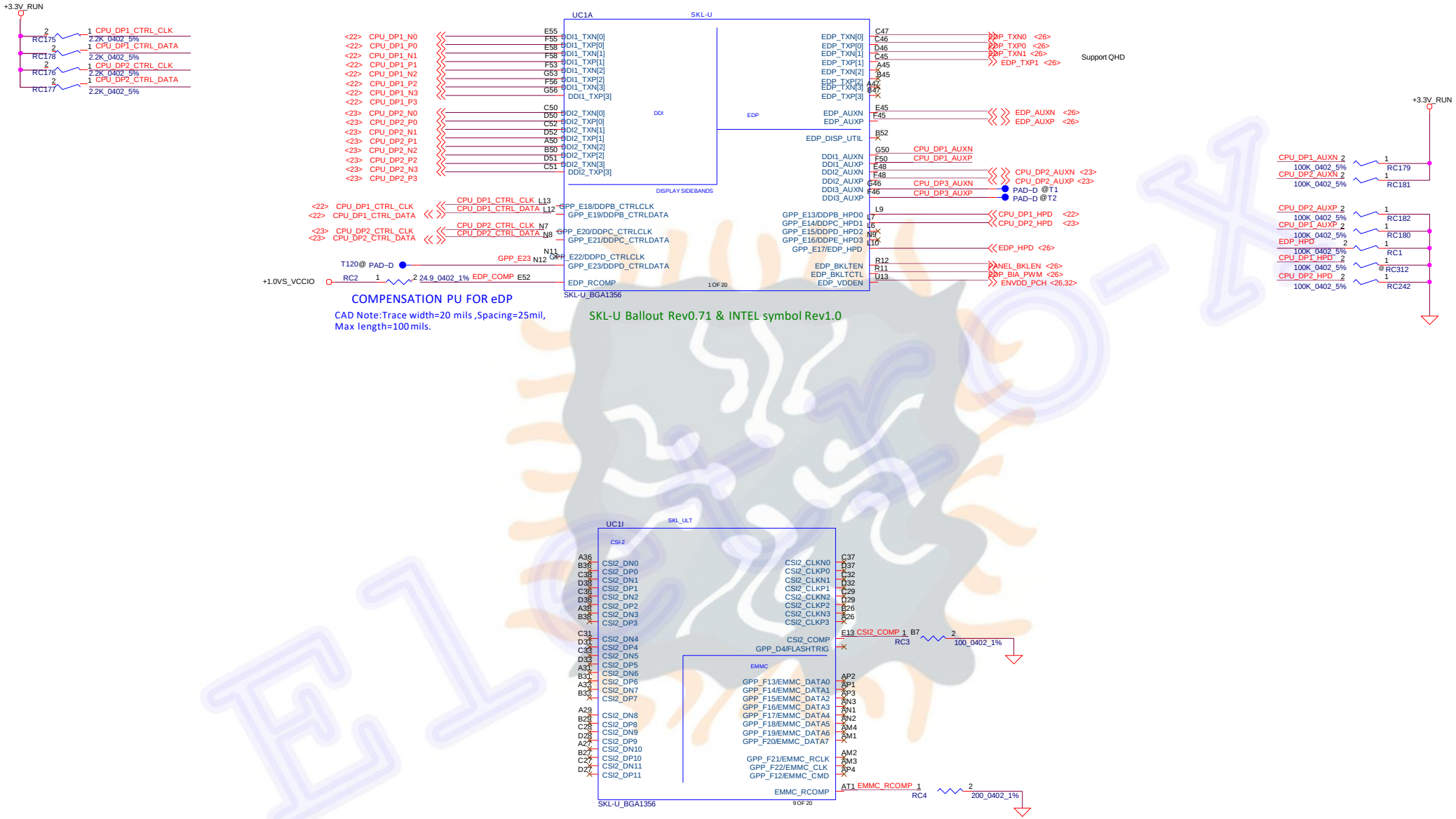
Compal Electronics, Inc.

Title: Port assignment

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 3

Eletro-X



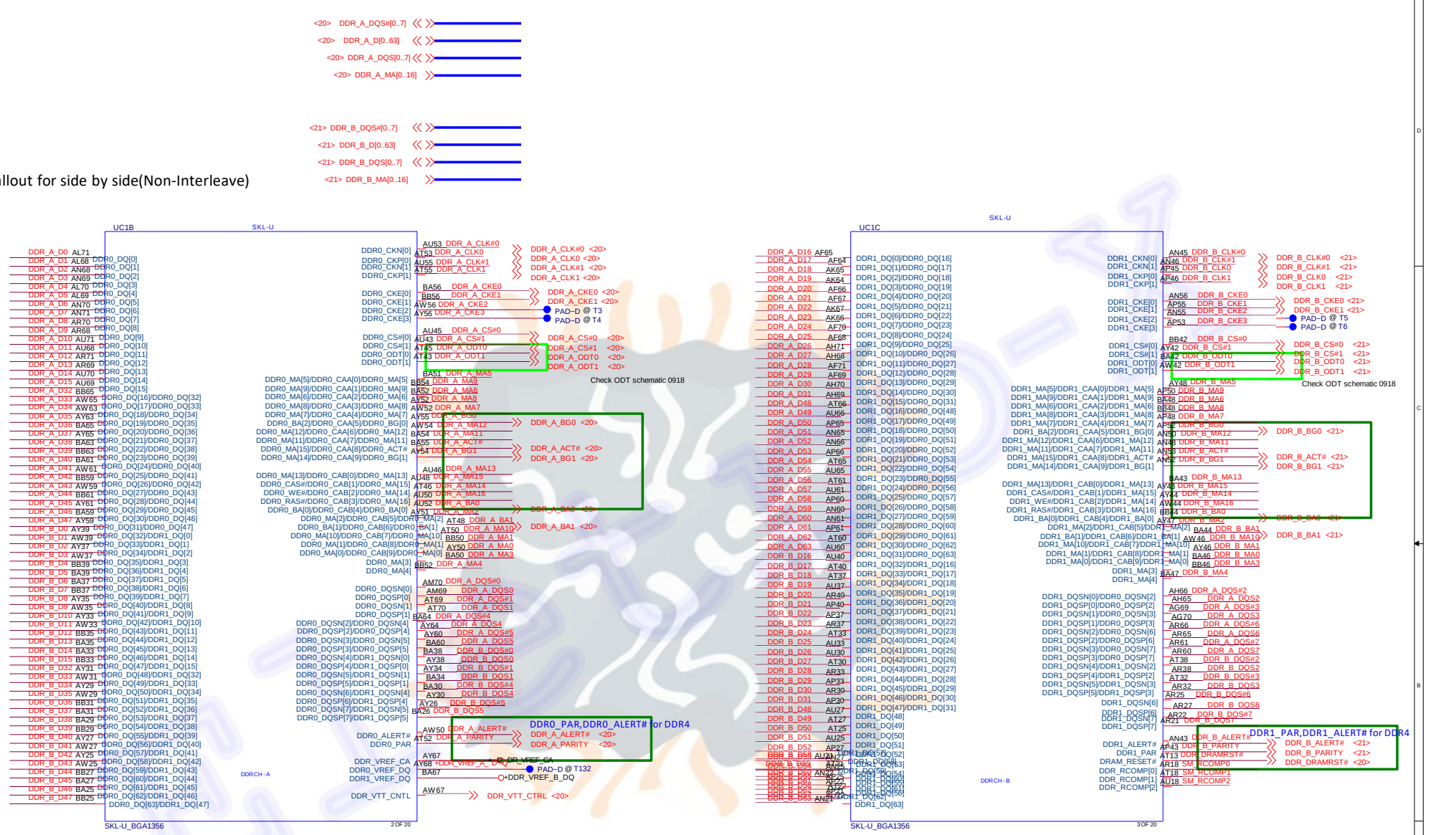
Compal Electronics, Inc.

Title: CPU (1/14)

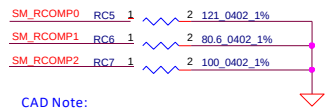
Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 6 of

DDR4, Ballot for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Compal Electronics, Inc.

Title	CPU (2/14)
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 7 of 60

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E SKL-U

SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C LINK
CL_CLK
CL_DATA
CL_RST#

GPP_A0/RCIN#
GPP_A6/SERIRQ

SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#

GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

SKL-U_BGA1356
5 OF 20

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

SOFTWARE TAA

9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

128Mb Flash ROM
UC5
W25Q128FVSIQ_SO8

64Mb Flash ROM
UC6 @
W25Q64FVSSIQ_SO8

Reserve for RF

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

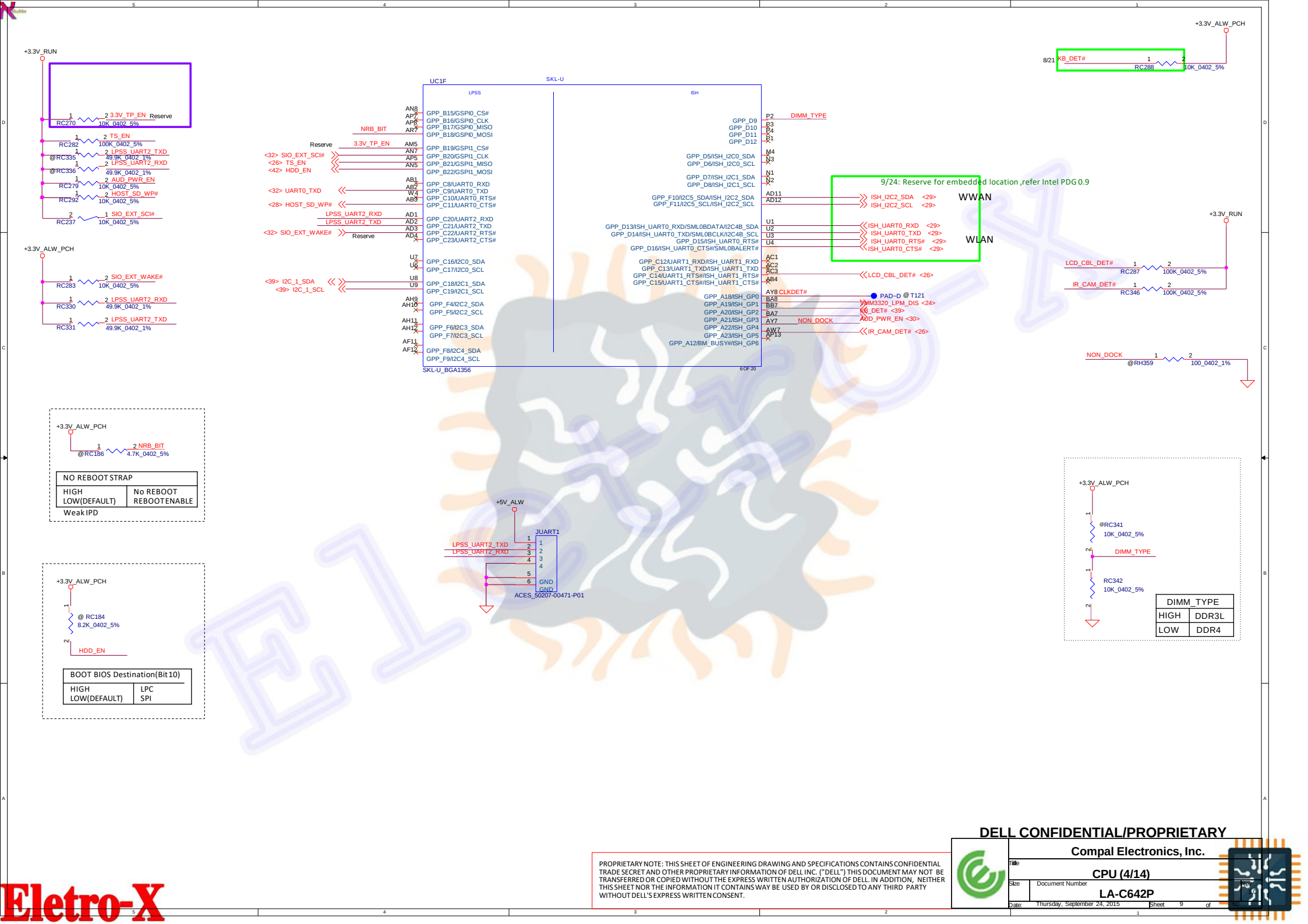
EXI BOOT STALL BYPASS	
HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

Compal Electronics, Inc.

Title: CPU (3/14)
Size: Document Number: LA-C642P
Date: Thursday, September 24, 2015 Sheet 8 of

Eletro-X

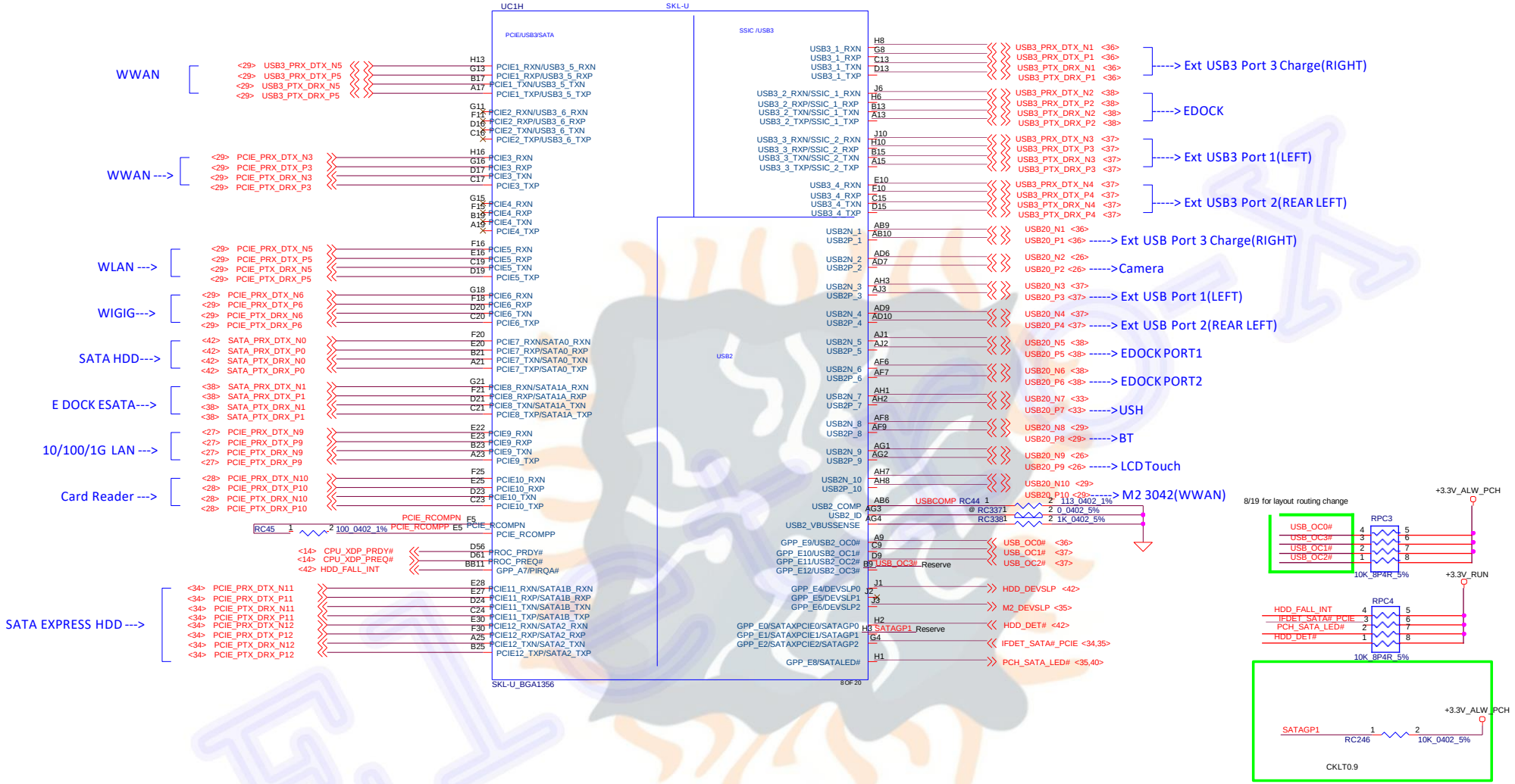


Compal Electronics, Inc.

Title: CPU (4/14)

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 9 of



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Compal Electronics, Inc.	
Title	CPU (5/14)
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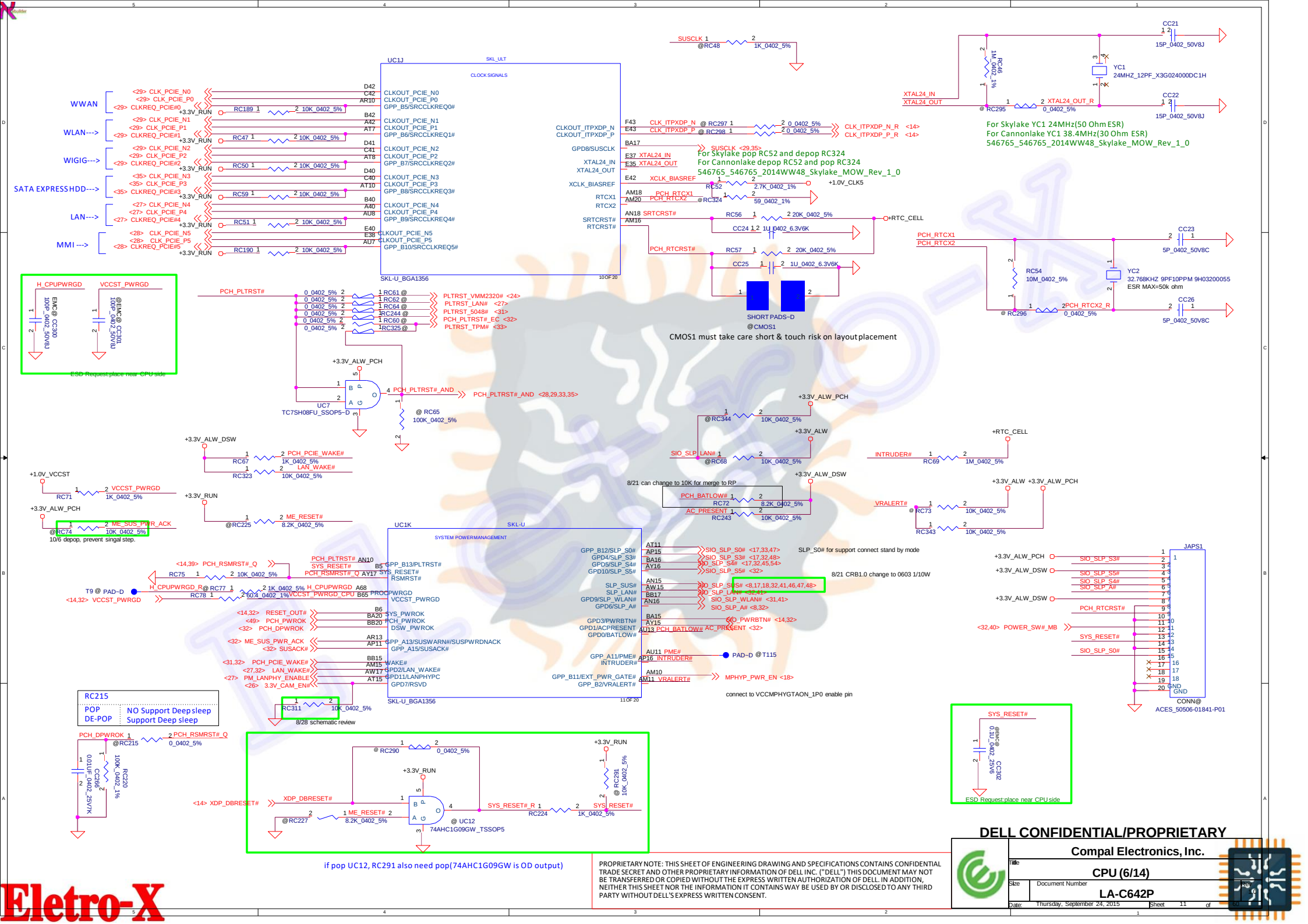
WWAN
WLAN--->
WIGIG--->
SATA EXPRESS HDD--->
LAN--->
MMI --->
UC1J
SKL_ULT
CLOCK SIGNALS
SKL-U_BGA1356
10 OF 20
For Skylake YC1 24MHz(50 Ohm ESR)
For Cannonlake YC1 38.4MHz(30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0
For Skylake pop RC52 and depop RC324
For Cannonlake depop RC52 and pop RC324
546765_546765_2014WW48_Skylake_MOW_Rev_1_0
CMOS1 must take care short & touch risk on layout placement
ESD Request:place near CPU side
UC7
TC7SH08FU_SSOP5-D
UC1K
SKL-U
SYSTEM POWERMANAGEMENT
SKL-U_BGA1356
11 OF 20
8/21 can change to 10K for merge to RP
SLP_S0# for support connect stand by mode
8/21 CRB1.0 change to 0603 1/10W
connect to VCCMPHYGTAON_1P0 enable pin
8/28 schematic review
RC215
POP
DE-POP
NO Support Deep sleep
Support Deep sleep
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)
UC12
74AHC1G09GW_TSSOP5
JAPS1
CONN@
ACES_50506-01841-P01
ESD Request:place near CPU side
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
CPU (6/14)
LA-C642P
Thursday, September 24, 2015
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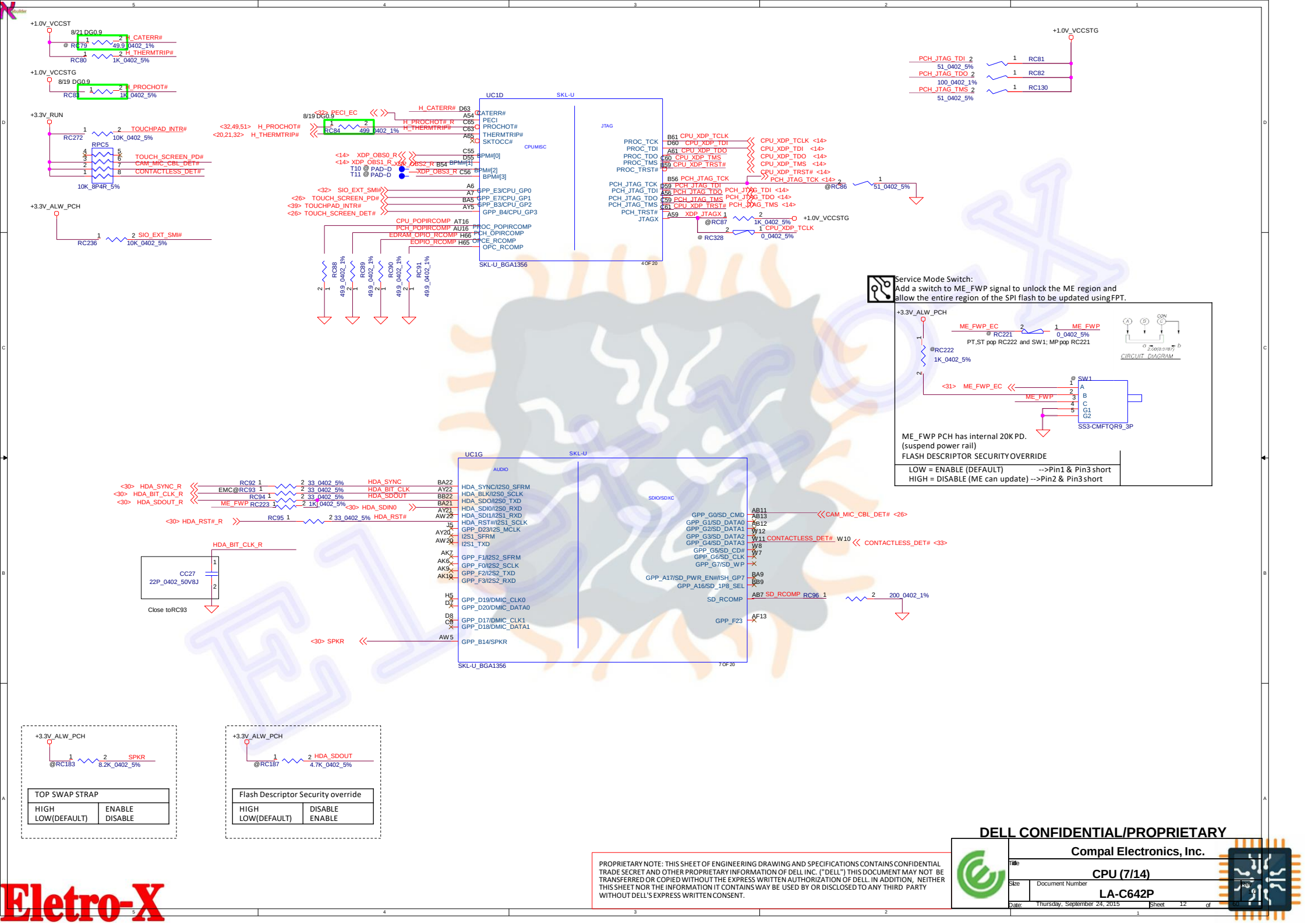

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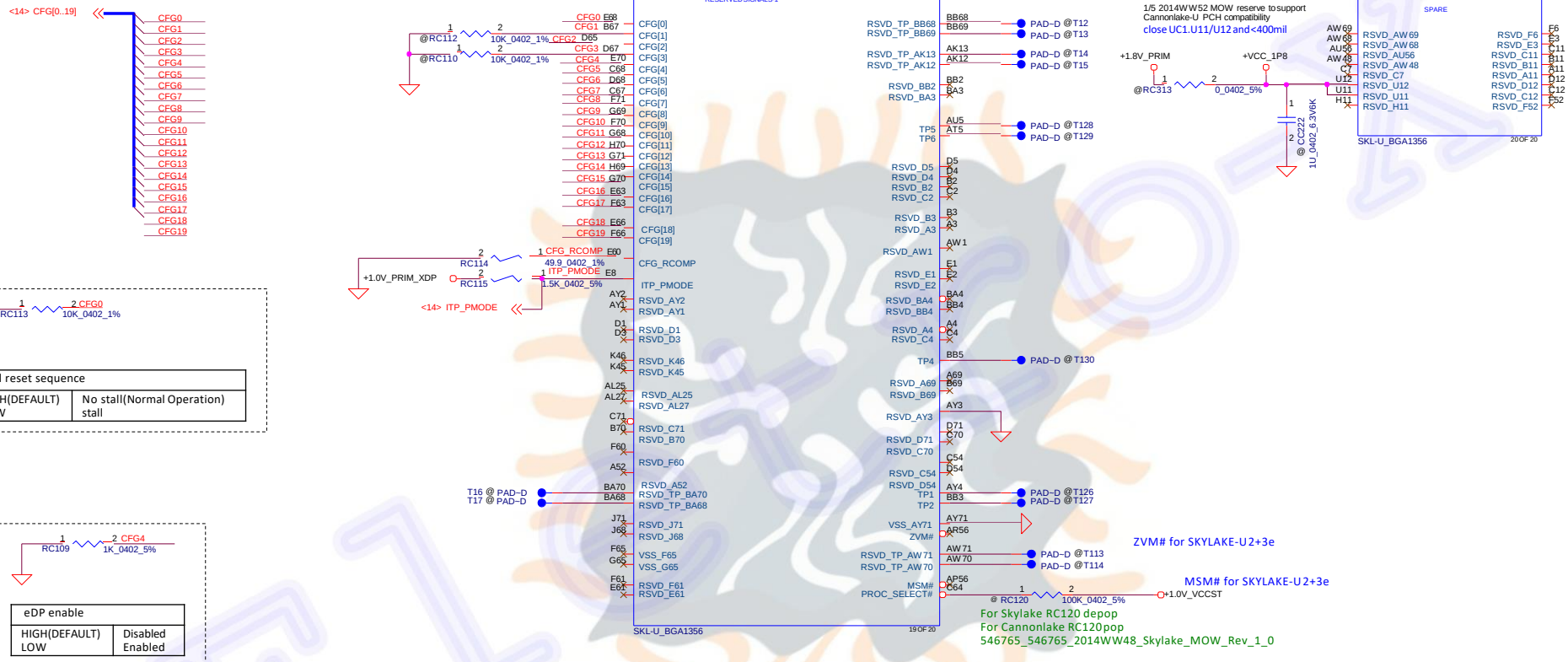
Title: CPU (7/14)

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 12 of

CFG[2][5][6][7] for SKYLAKE-H CPU CFG strappin



@RC113 10K_0402_1%

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

RC109 1K_0402_5%

eDP enable	
HIGH(DEFAULT)	Disabled
LOW	Enabled

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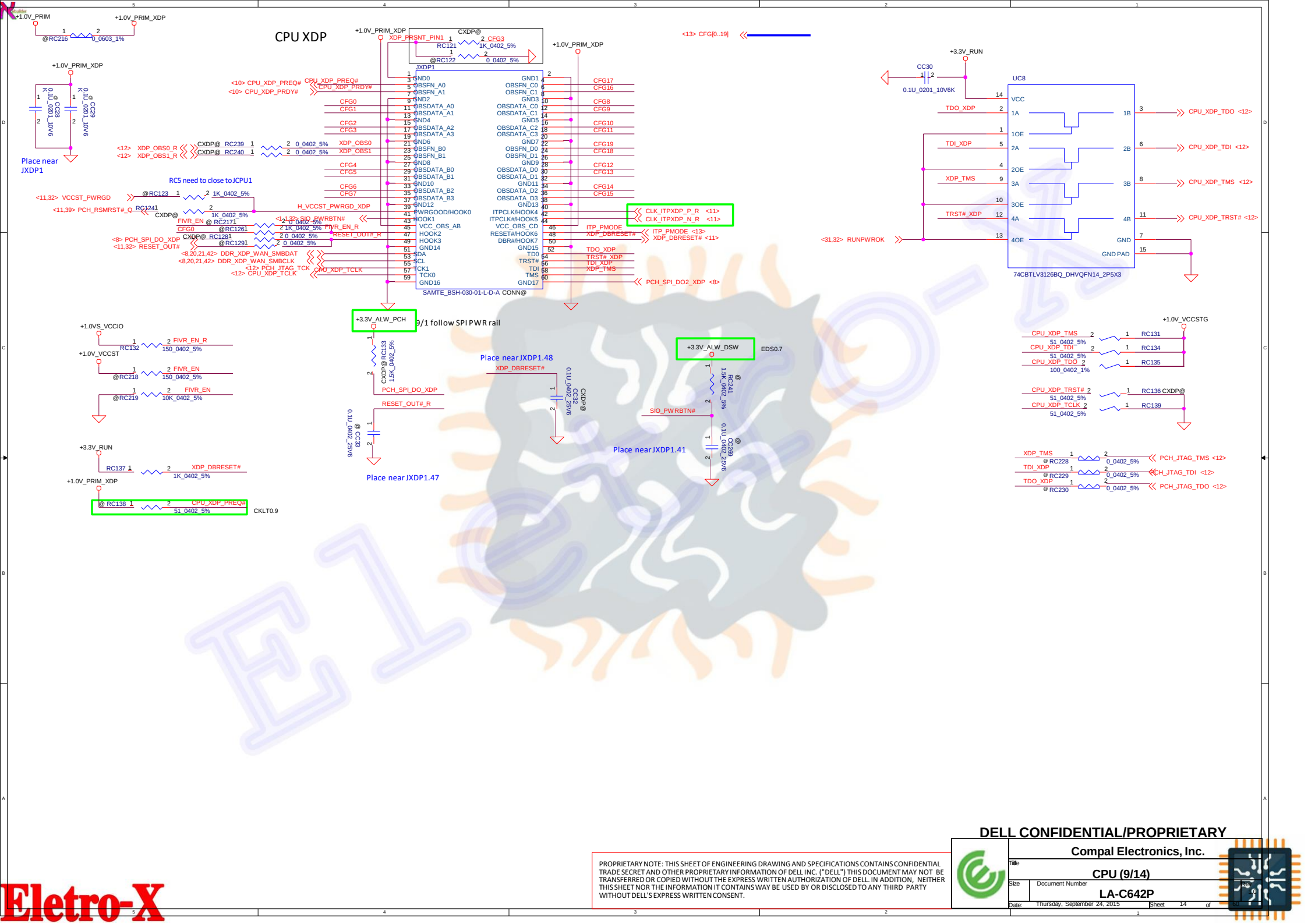
Title: CPU (8/14)

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 13 of

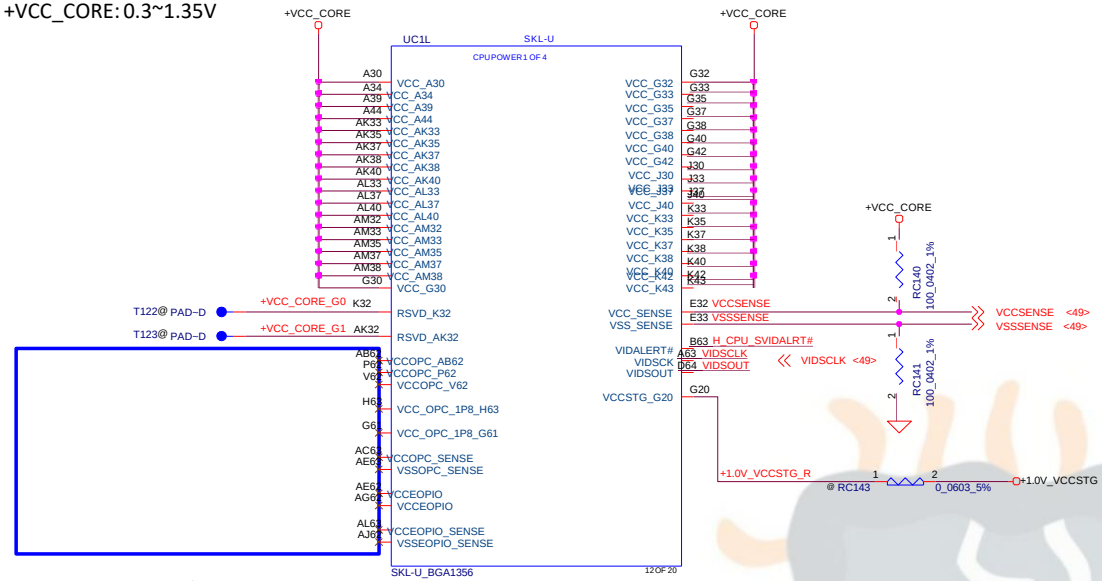
CPU XDP



Compal Electronics, Inc.

Title	CPU (9/14)
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 14 of

+VCC_CORE: 0.3~1.35V

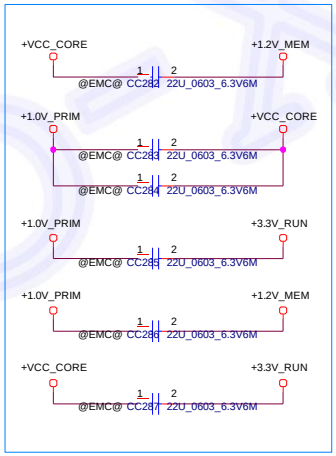


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

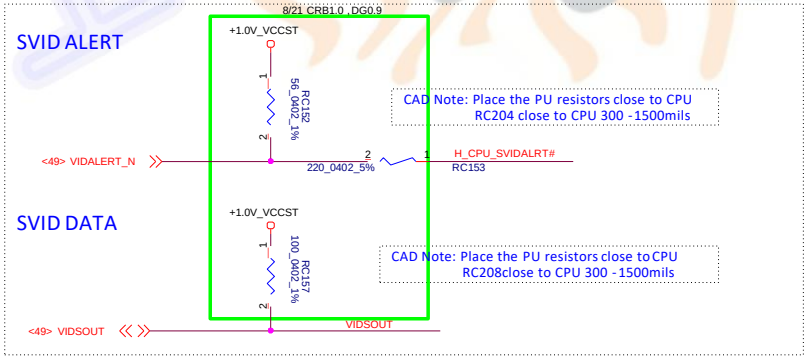
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

ESD Request



8/21 CRB1.0 , DG0.9

SVID ALERT



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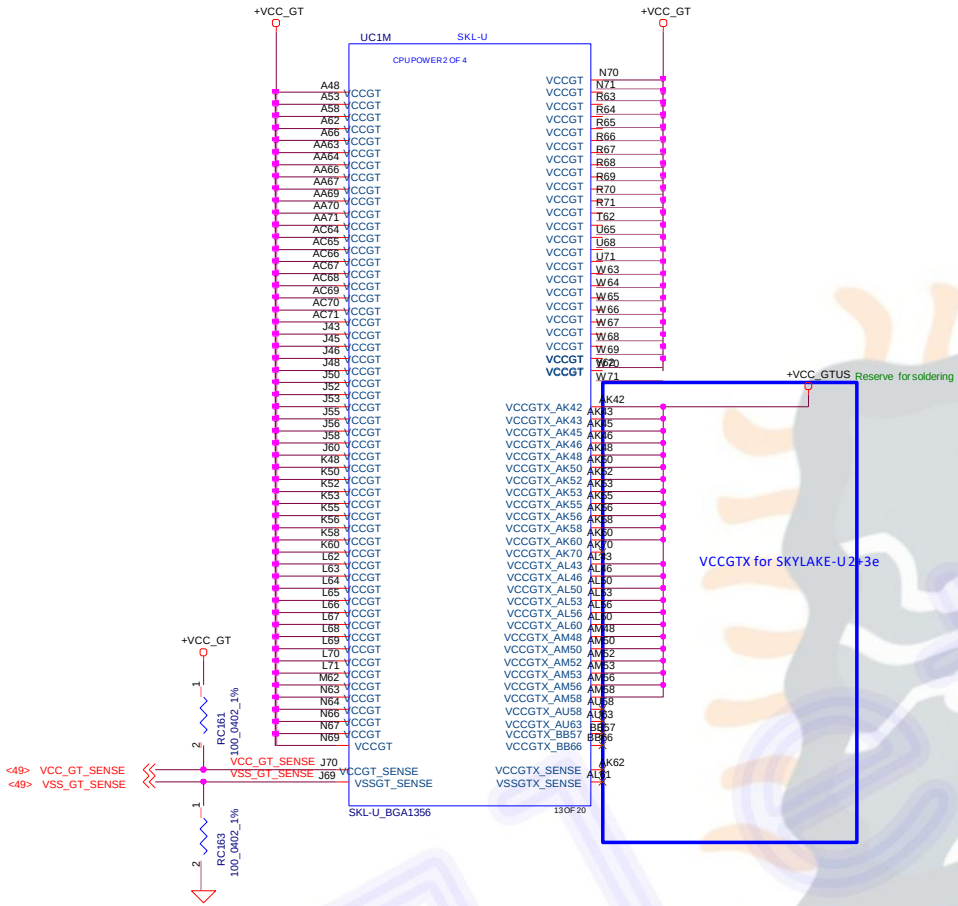
Compal Electronics, Inc.

Title: CPU (10/14)

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 15 of

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

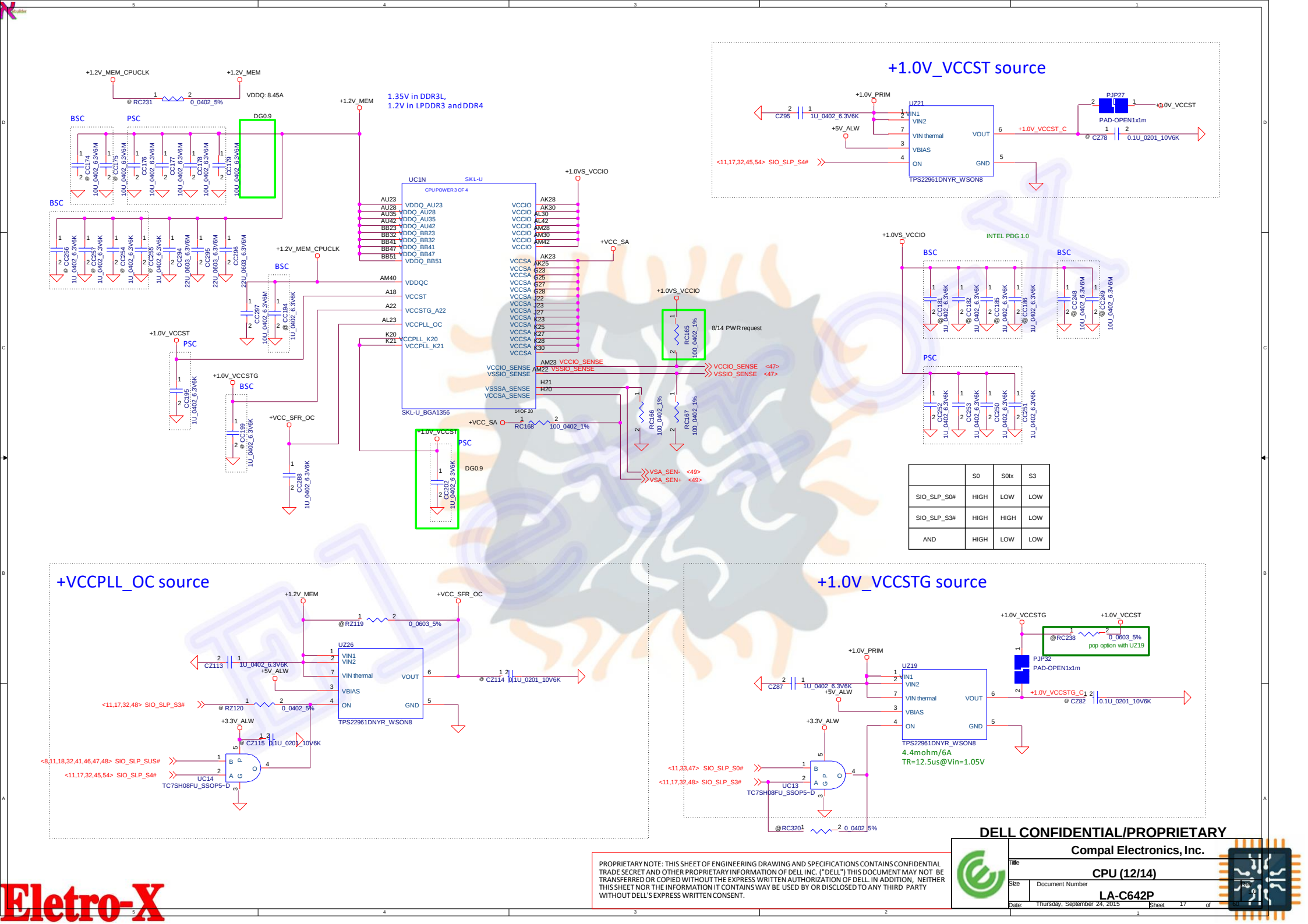


Compal Electronics, Inc.

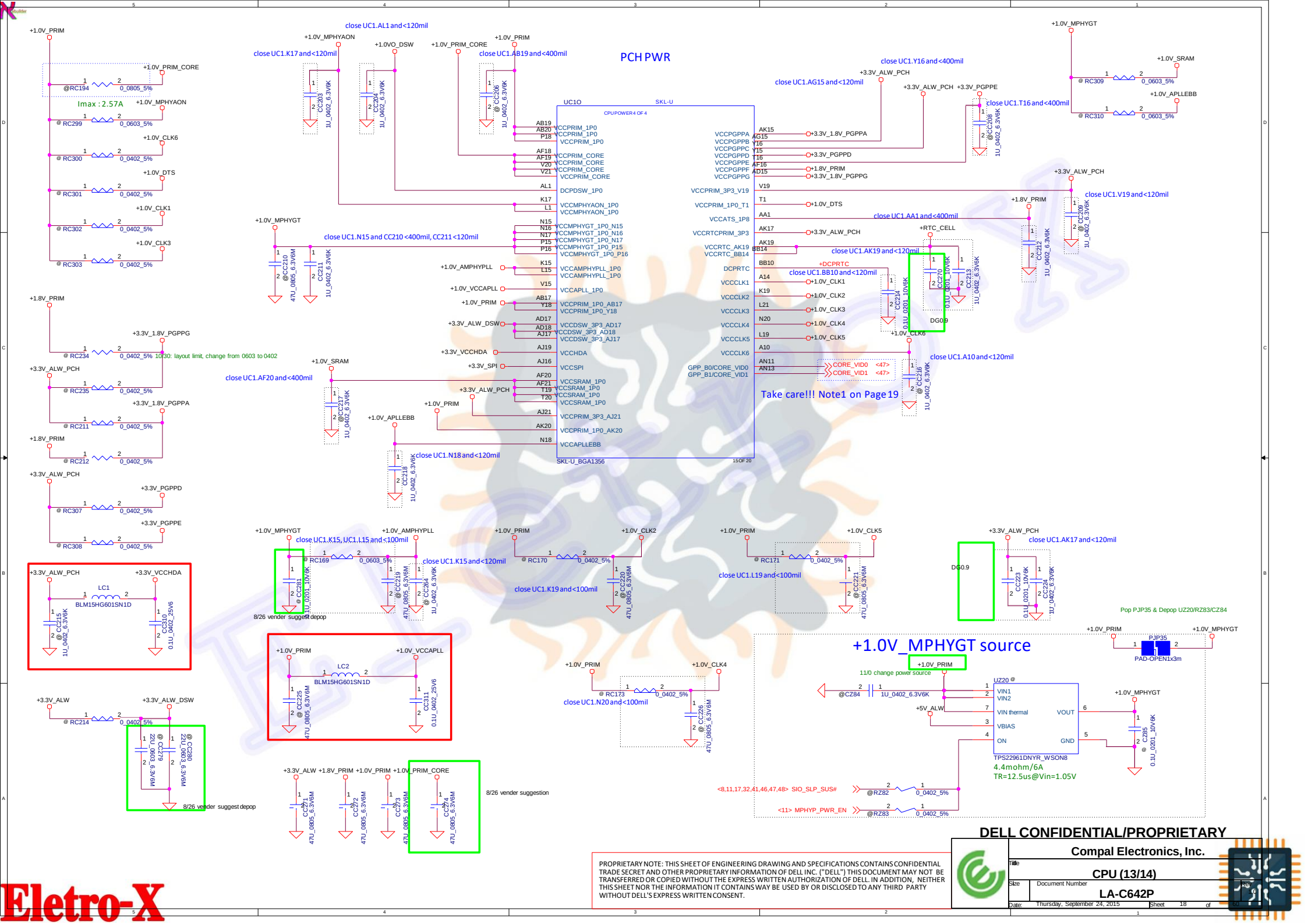
Title: CPU (11/14)

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 16 of



	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW


PCH PWR
UC1O
SKL-U
CPUPOWER4 OF 4
SKL-U_BGA1356
15OF 20
close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.V19 and <120mil
close UC1.AA1 and <400mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.N15 and CC210 <400mil, CC211 <120mil
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
Take care!!! Note1 on Page 19
Imax : 2.57A
10/30: layout limit, change from 0603 to 0402
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.K19 and <100mil
close UC1.L19 and <100mil
close UC1.N20 and <100mil
close UC1.AK17 and <120mil
8/26 vender suggest depop
8/26 vender suggestion
Pop PJP35 & Depop UZ20/RZ83/CZ84
+1.0V_MPHYGT source
11/0 change power source
TPS22961DNYR_WSON8
4.4mohm/6A
TR=12.5us@Vin=1.05V
DG0.9
PAD-OPEN1x3m
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Compal Electronics, Inc.
CPU (13/14)
LA-C642P
Thursday, September 24, 2015
Sheet 18 of 60
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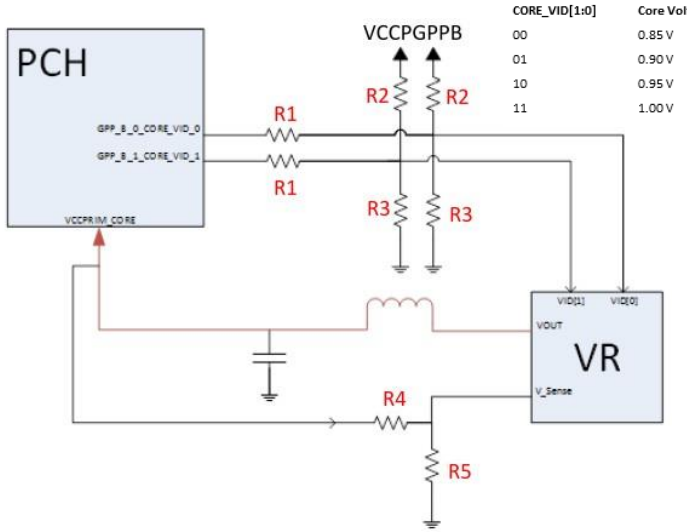
Eletro-X

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

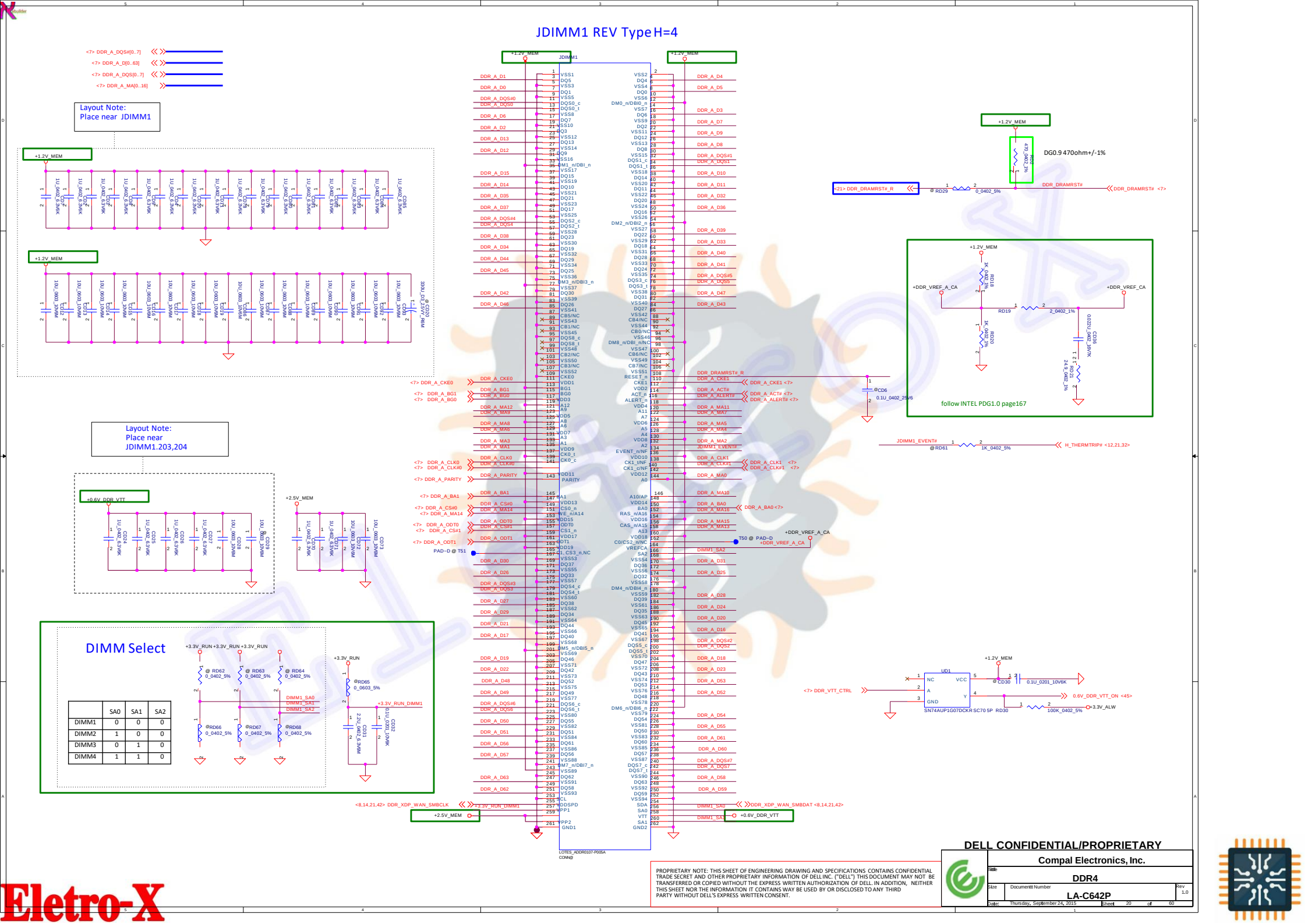
Compal Electronics, Inc.

Title: CPU (14/14)

Size: | Document Number: LA-C642P

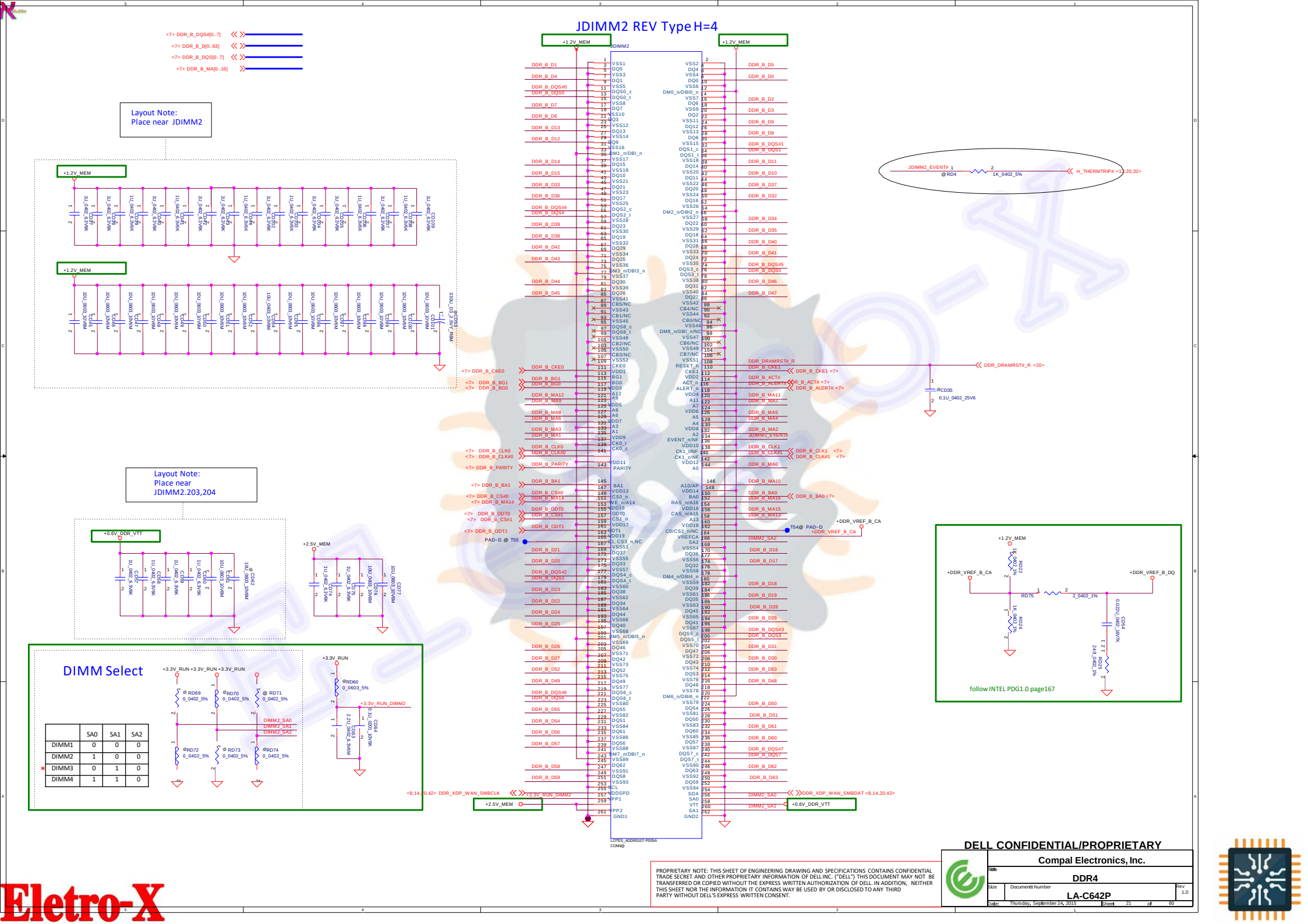
Date: Thursday, September 24, 2015 | Sheet 19 of

JDIMM1 REV Type H=4



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

JDIMM2 REV Type H=4



	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

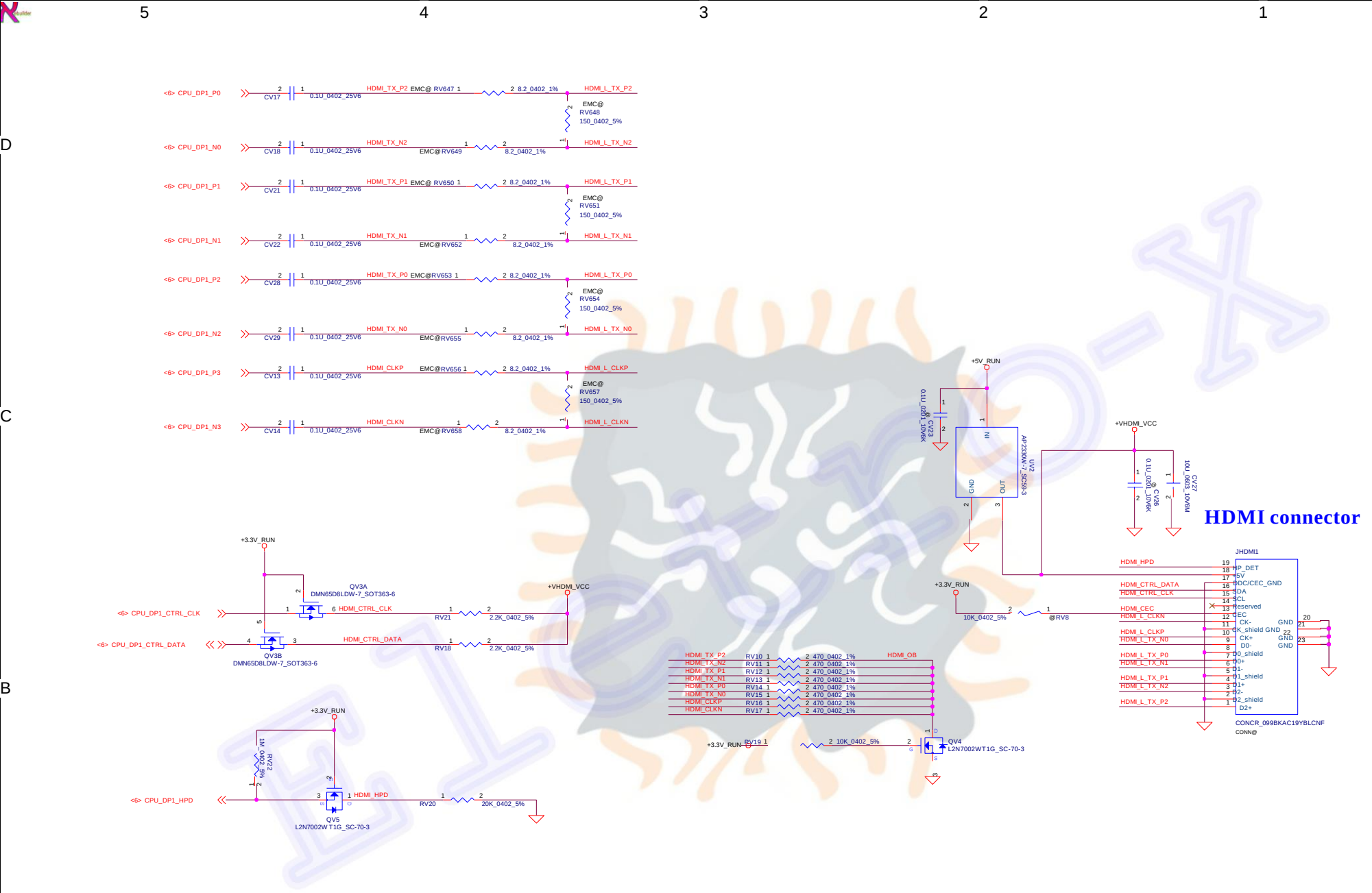
Compal Electronics, Inc.

DDR4

LA-C642P

Rev 1.0

Date: Thursday, September 24, 2015 Sheet 21 of 60

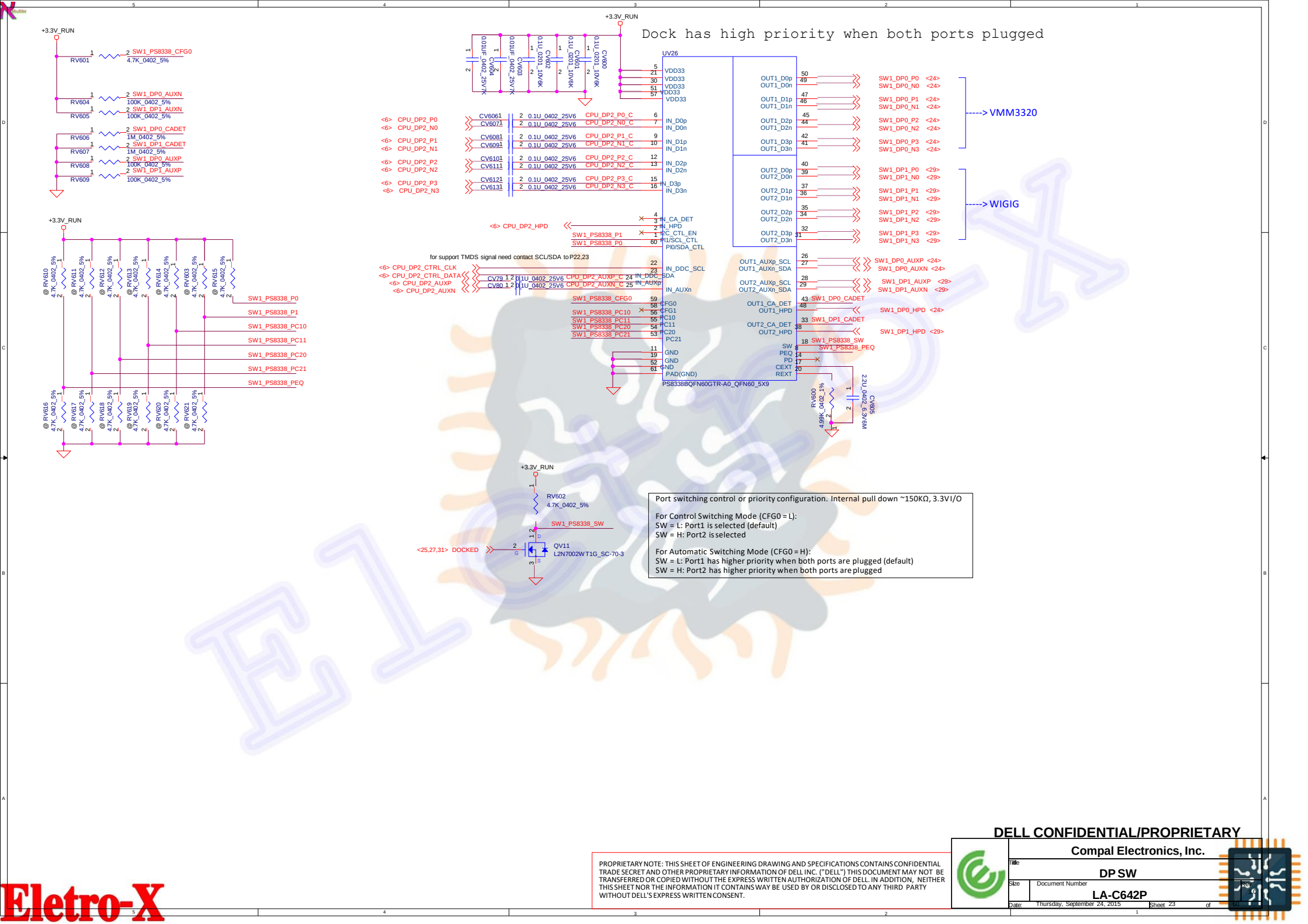


Compal Electronics, Inc.

Title: HDMI CONN

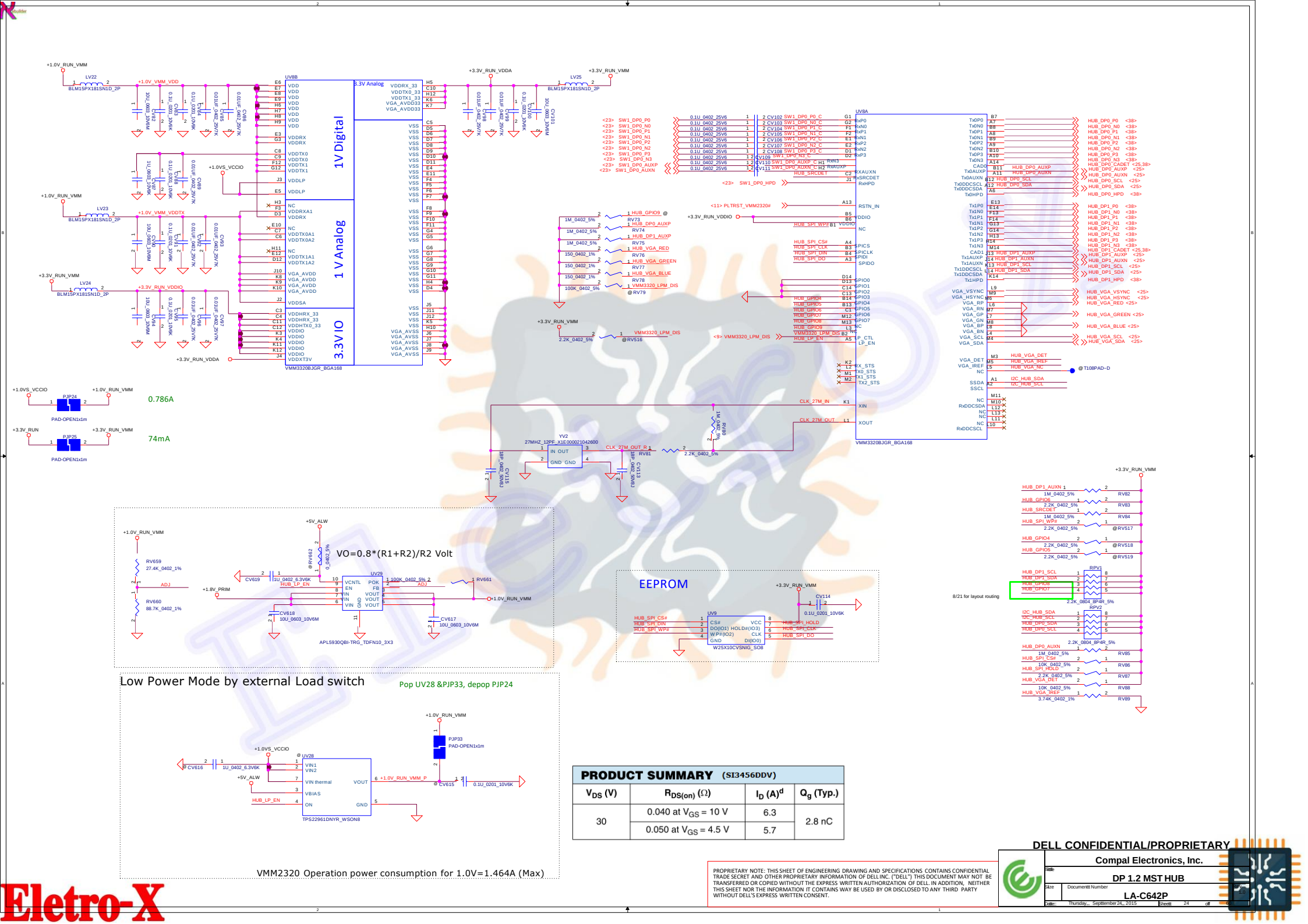
Size: | Document Number: LA-C642P | Rev: 1.0

Date: Thursday, September 24, 2015 | Sheet 22 of 60



Compal Electronics, Inc.

Title	DP SW
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 23 of 50



PRODUCT SUMMARY (SI3456DDV)			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[d]	Q_g (Typ.)
30	0.040 at V_{GS} = 10 V	6.3	2.8 nC
	0.050 at V_{GS} = 4.5 V	5.7	

Compal Electronics, Inc.

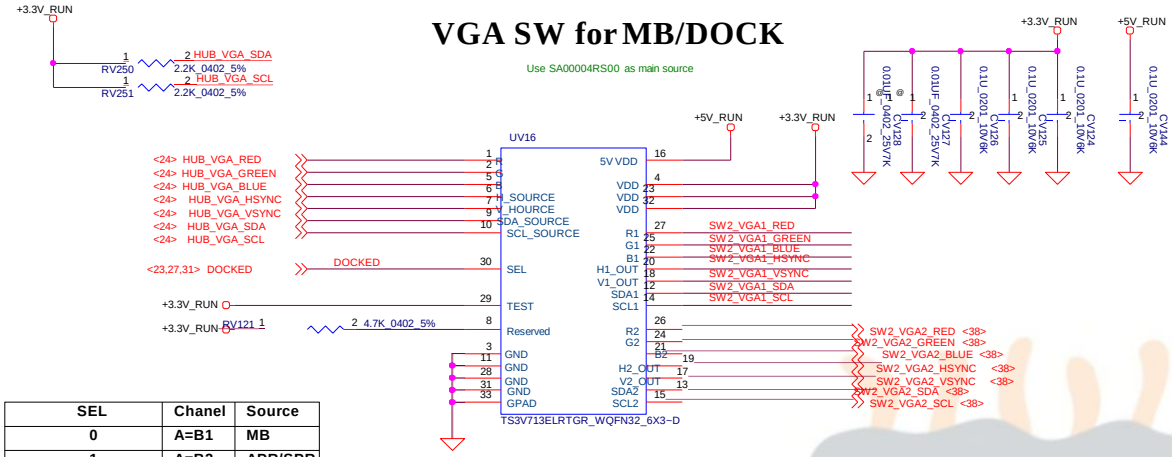
DP 1.2 MST HUB

LA-C642P

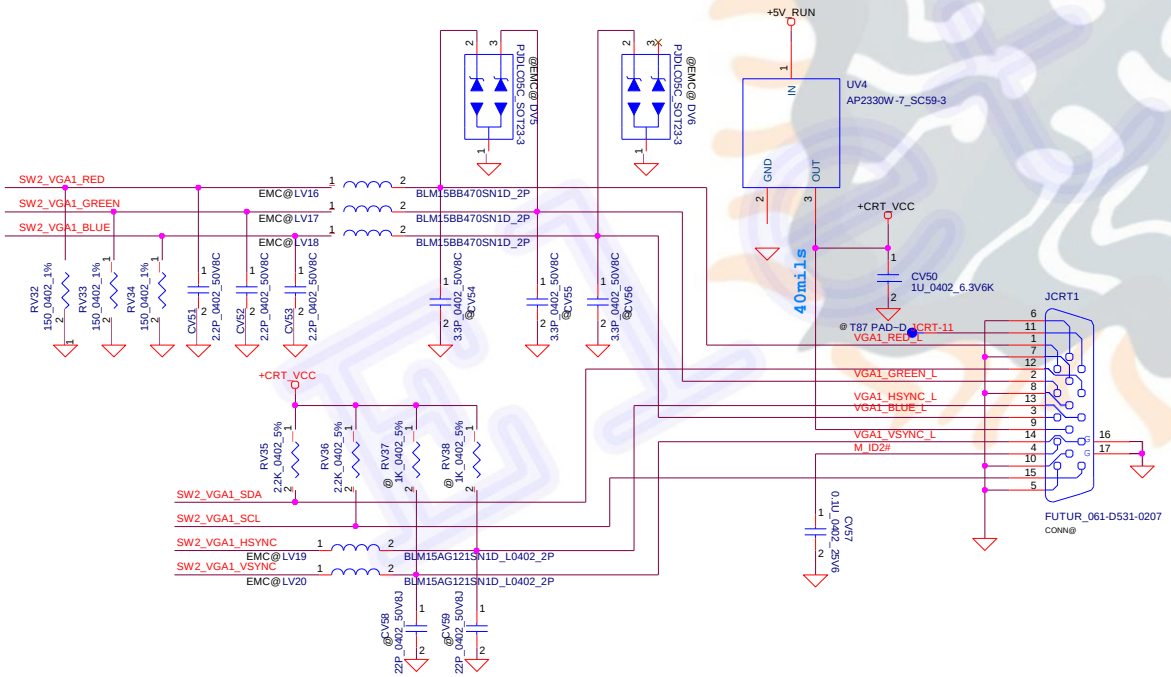
Thursday, September 24, 2015

VGA SW for MB/DOCK

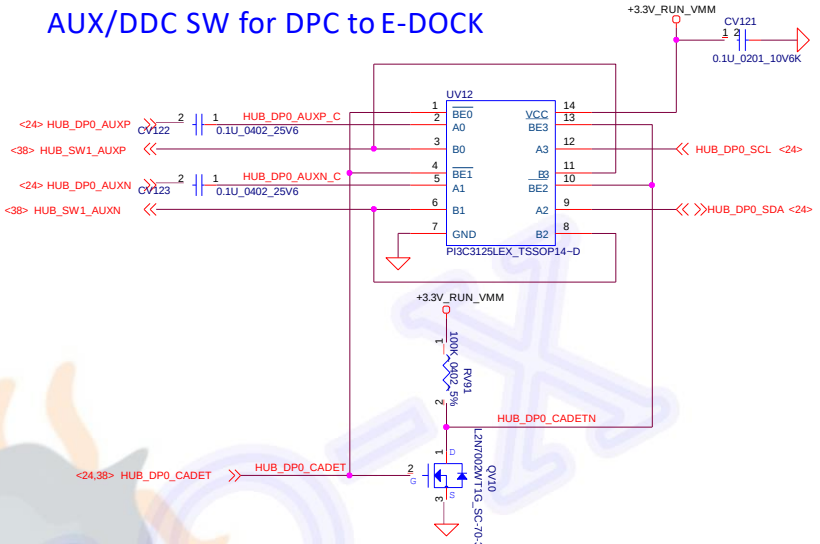
Use SA00004RS00 as main source



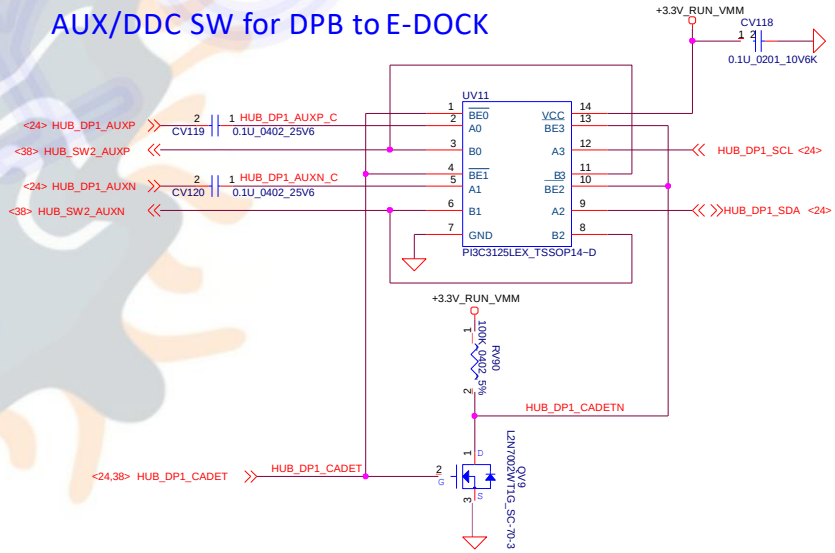
SEL	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

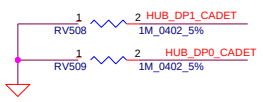


AUX/DDC SW for DPC to E-DOCK



AUX/DDC SW for DPB to E-DOCK





	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

Compal Electronics, Inc.

Title: DP SW

Size | Document Number: LA-C642P

Date: Thursday, September 24, 2015 | Sheet 25 of

LINK 50398-04041-001 DONE

JEDP1

+3.3V_TSP

TOUCH_SCREEN_PD# <12>

DMIC0 <30>

DMIC_CLK0 <30>

+3.3V_RUN

+3.3V_CAM

USB20_N2_R

USB20_P2_R

CAM_MIC_CBL_DET# <12>

Pin15: LOOP_BACK

+BL_PWR_SRC

EMC@LV1

BIA_PWM

BLM15BB221SN1D_2P

DISP_ON

EDP_HPD <6>

LCD_TST <31>

+LCDVDD

TOUCH_SCREEN_DET#

TOUCH_SCREEN_DET# <12>

EDP_AUXN_C

EDP_AUXP_C

EDP_TXP0_C

EDP_TXN0_C

EDP_TXP1_C

EDP_TXN1_C

CV1 0.1U_0402_25V6

CV2 0.1U_0402_25V6

CV3 0.1U_0402_25V6

CV4 0.1U_0402_25V6

CV5 0.1U_0402_25V6

CV6 0.1U_0402_25V6

EDP_AUXN <6>

EDP_AUXP <6>

EDP_TXP0 <6>

EDP_TXN0 <6>

EDP_TXP1 <6>

EDP_TXN1 <6>

LCD_CBL_DET# <9>

ACES_50398-04041-001

CONN@

@EMC@ CA5 100P_0402_50V8J

@EMC@ CA6 100P_0402_50V8J

TOUCH_PANEL_INTR#;

Close lid >> TP_EN = 0 >> Disable touch events

Open lid >> TP_EN = 1 >> Enable touch events

USB20_N9_R

USB20_P9_R

EMC@ LV27

USB20_N9 <10>

USB20_P9 <10>

MCM1012B900F06BP_4P

@EMC@ DV4 PESD5V0U2BT_SOT23-3

ESD depoplocation

+3.3V_RUN

RV623 10K_0402_5%

TOUCH_SCREEN_DET#

IR CAM Conn

+PWR_SRC

JIR1

<9> IR_CAM_DET#

GND

GND

ACES_50450-0067N-P01

CONN@

+BL_PWR_SRC

0.1U_0603_50V7K @ CV7

Close to JEDP1.17~19

+LCDVDD

0.1U_0201_10V6K CV8

Close to JEDP1.30~31

+3.3V_CAM

0.1U_0201_10V6K @ CZ1

Close to JEDP1.11

+3.3V_TSP

0.1U_0201_10V6K @ CZ2

Close to JEDP1.1

+3.3V_RUN

0.1U_0201_10V6K @ CA7

Close to JEDP1.10

For Touchscreen

+3.3V_RUN

10K_0402_5% RV6

+3.3V_TSP

QV8 LP2301ALT1G_SOT23-3

+3.3V_RUN

<9> TS_EN

QV7 L2N7002WT1G_SC-70-3

DV1

BIA_PWM

BAT54CW_SOT323-3

EDP_BIA_PWM <6>

BIA_PWM_EC <32>

4.7K_0402_5% RV1

DV2

DISP_ON

BAT54CW_SOT323-3

PANEL_BKLEN <6>

PANEL_BKEN_EC <31>

4.7K_0402_5% RV2

WebCAM

+3.3V_CAM

+3.3V_RUN

QZ1 LP2301ALT1G_SOT23-3

<11> 3.3V_CAM_EN#

MCM1012B900F06BP_4P

<10> USB20_P2

USB20_P2_R

<10> USB20_N2

USB20_N2_R

LZ1 EMC@

Backlight POWER

+PWR_SRC

+BL_PWR_SRC

QV1 AO6405_TSOP6

1000P_0402_50V7K CV11

270K_0402_5% RV4

0.1U_0603_50V7K CV12

BL_PWR_SRC_ON

QV2 L2N7002WT1G_SC-70-3

RV5 47K_0402_5%

0.01U_0402_50V7K CV374

<32> EN_INVPWR

LCDVDD POWER

+LCDVDD

@ CV9

10U_0603_10V6M

+EDP_VDD

PJP29

PAD-OPEN1x1m

UV24 G524B1T11U_SOT23-5

VOUT

GND

/OC

VIN

EN

+3.3V_ALW

@ CV10 0.01UF_0402_25V7K

<31> LCD_VCC_TEST_EN

<6,32> ENVDD_PCH

DV3 BAT54CW_SOT323-3

EN_LCDPWR

100K_0402_5% RV3

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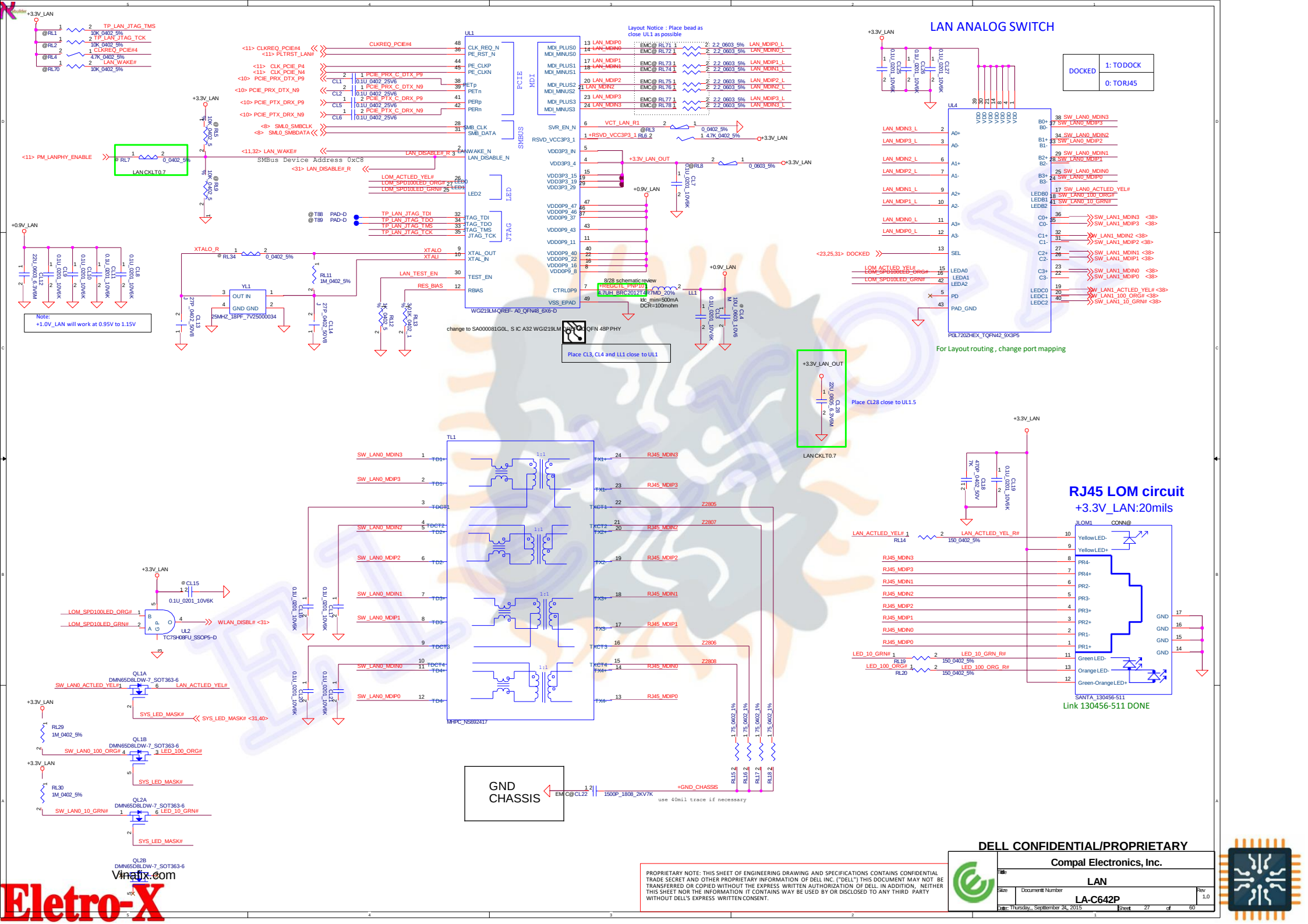
Compal Electronics, Inc.

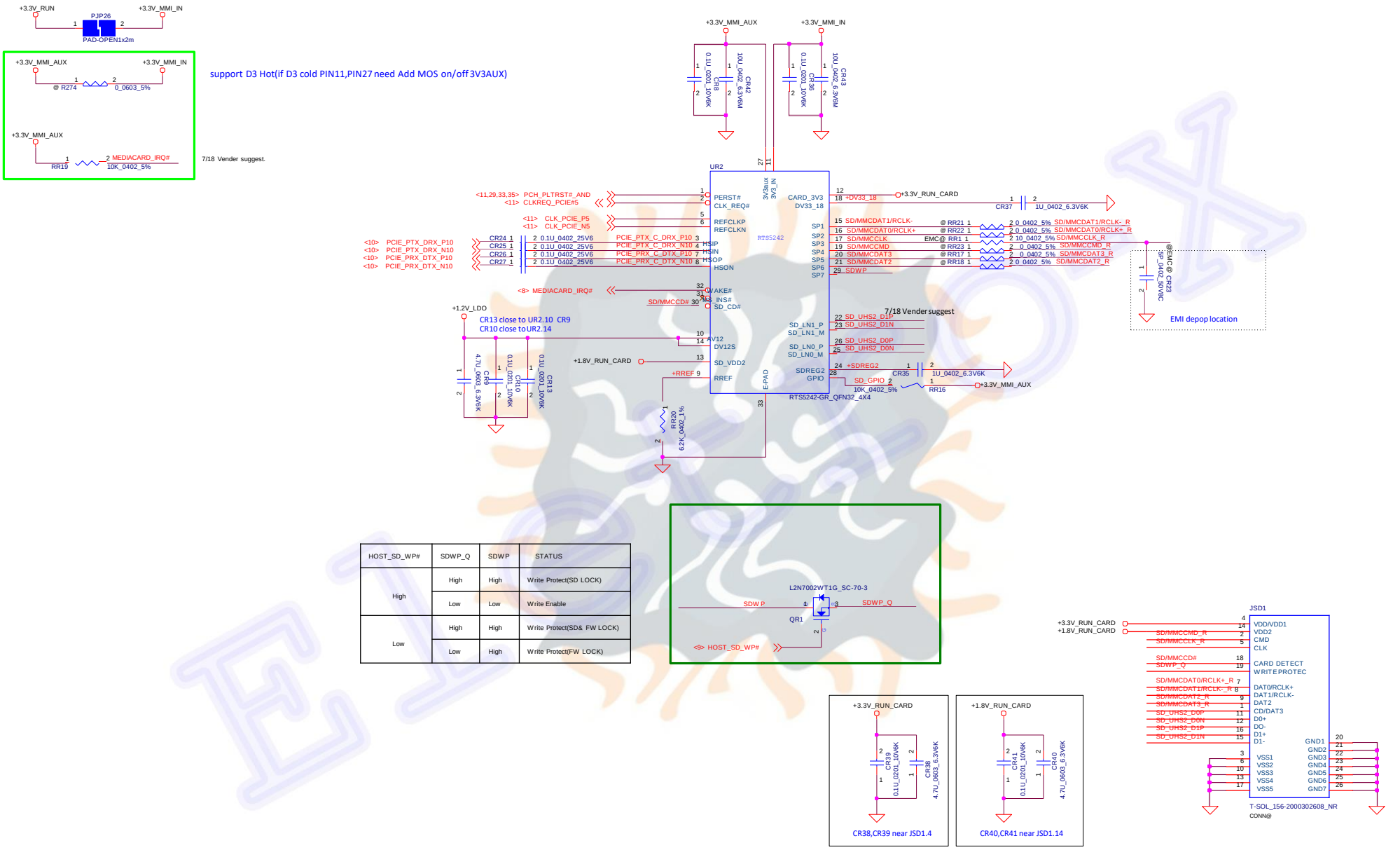
Title: eDP CONN & Touch screen

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 26 of

Eletro-X


LAN ANALOG SWITCH
RJ45 LOM circuit
+3.3V_LAN:20mils
DOCKED
1: TODOCK
0: TORJ45
Layout Notice : Place bead as close UL1 as possible
For Layout routing , change port mapping
Place CL3, CL4 and LL1 close to UL1
Place CL28 close to UL1.5
Link 130456-511 DONE
Note: +1.0V_LAN will work at 0.95V to 1.15V
change to SA000081G0L, S IC A32 WG1219LM QFN 48P PHY
SMBus Device Address 0xC8
GND CHASSIS
use 40mil trace if necessary
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
LAN
LA-C642P
Vinafix.com
Eletro-X



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)

Compal Electronics, Inc.

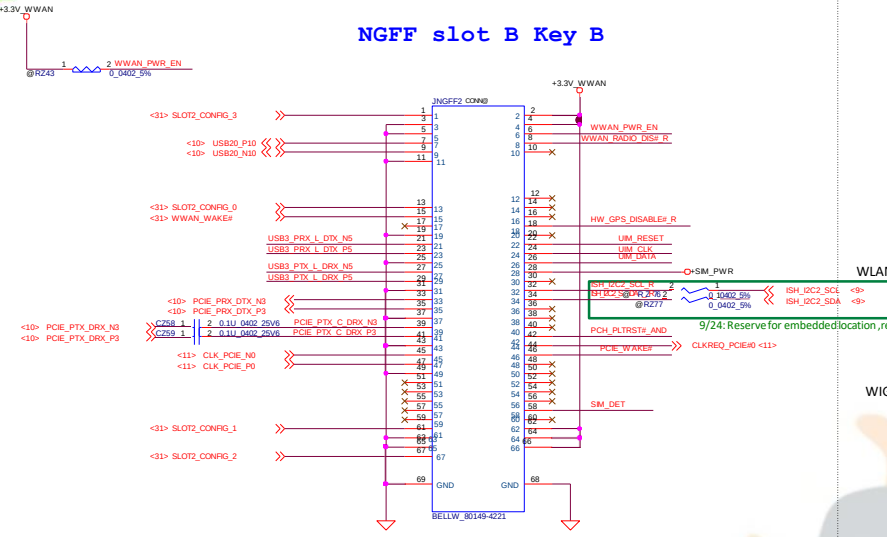
Title: Card Reader

Size: Document Number: LA-C642P

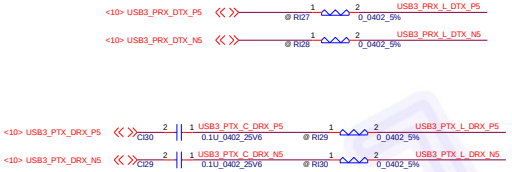
Rev: 1.0

Date: Thursday, September 24, 2015 Sheet 28 of 60

NGFF slot B Key B

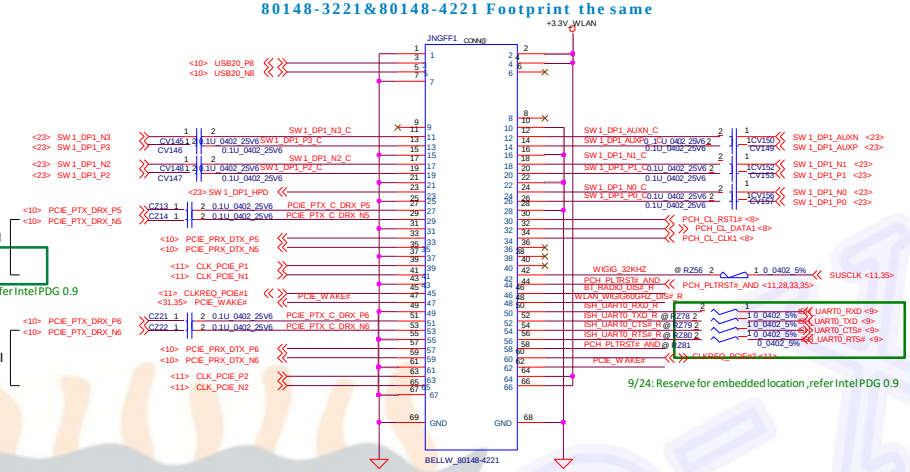


80149-4221 LINK DONE

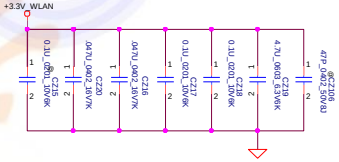


NGFF slot A Key A

80148-3221&80148-4221 Footprint the same



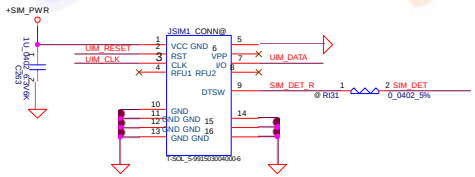
BELLW_80148-4221 LINK DONE



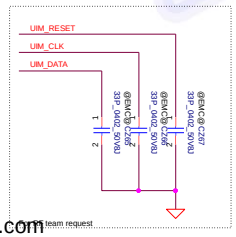
Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

SIM Card Push-Push



T-SOL_5-991503004000-6 LINK DONE



Compal Electronics, Inc.

NGFF Card

LA-C642P

Rev 1.0

Date: Thursday, September 24, 2015 Sheet 29 of 60

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

INT_SPK_L+
INT_SPK_L-
INT_SPK_R+
INT_SPK_R-

EMC@ LA6 1 2 BLM15PX330SN1D_2P
EMC@ LA7 1 2 BLM15PX330SN1D_2P
EMC@ LA8 1 2 BLM15PX330SN1D_2P
EMC@ LA9 1 2 BLM15PX330SN1D_2P

INT_SPKR_L+
INT_SPKR_L-
INT_SPKR_R+
INT_SPKR_R-

JSPK1
GND1
GND2
ACES_50271-0040N-001
CONN@

Close to UA1

Close to UA1 pin6

HDA_BIT_CLK_R

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

AUD_SENSE_A

AUD_HP_NB_SENSE <31>

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

AUD_SENSE_B

<31> DOCK_HP_DET

DOCK_MIC_DET <31>

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

+5V_RUN_AUDIO 2.5A

+3.3V_RUN_AUDIO 0.5A

<9> AUD_PWR_EN

Vinafix.com

Eletro-X

+3.3V_RUN_AUDIO

CA11 close to pin9
CA10 close to pin3

<31> EN_I2S_NB_CODEC#

UA1
I2S I/F Float
DVDD_IO
DVDD
BCLK
SDATA-OUT
SYNC
SDATA-IN
RESET#
I2S_MCLK
I2S_SCLK
I2S_DOUT
I2S_LRCK
I2S_DIN
MIC1-L(PORT-B-L)
MIC1-R(PORT-B-R)
EAPD+PD
LDO1-CAP
LDO2-CAP
LDO3-CAP
GND
ALC3235-CG_MQFN48_6X6

<12> HDA_BIT_CLK_R
<12> HDA_SDOUT_R
<12> HDA_SYNC_R
<12> HDA_SDIN0
<12> HDA_RST#_R

Place RA9 close to codec

<38> DAI_12MHZ#
<38> DAI_BCLK#
<38> DAI_DO#
<38> DAI_LRCK#
<38> DAI_DI

Place RA32 close to codec

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

<31> AUD_NB_MUTE#

Place CA29 close to Codec

+VDDA_AVDD1
+VDDA_PVDD
+5V_RUN_PVDD
+1.5V_RUN_AUDIO
+5V_RUN_AUDIO
+3.3V_RUN_AUDIO
+1.5V_RUN

place close to pin27
place close to pin40
place close to pin38
place close to pin41
place close to pin46

AUD_SENSE_A
AUD_SENSE_B
SLEEVE/RING2 please keep 40 mils trace width
AUD_HP_OUT_L
AUD_HP_OUT_R
AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

+VREFOUT

SPKR <12>
BEEP <32>
DMIC_CLK0 <26>
DMIC0 <26>

place close to UA1 pin2

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC
Global Headset
Universal Jack

JHP1
SINGA_2SJ3095-022111F
CONN@

Normal
Open

AUD_HP_NB_SENSE

SLEEVE
+RTC_CELL

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

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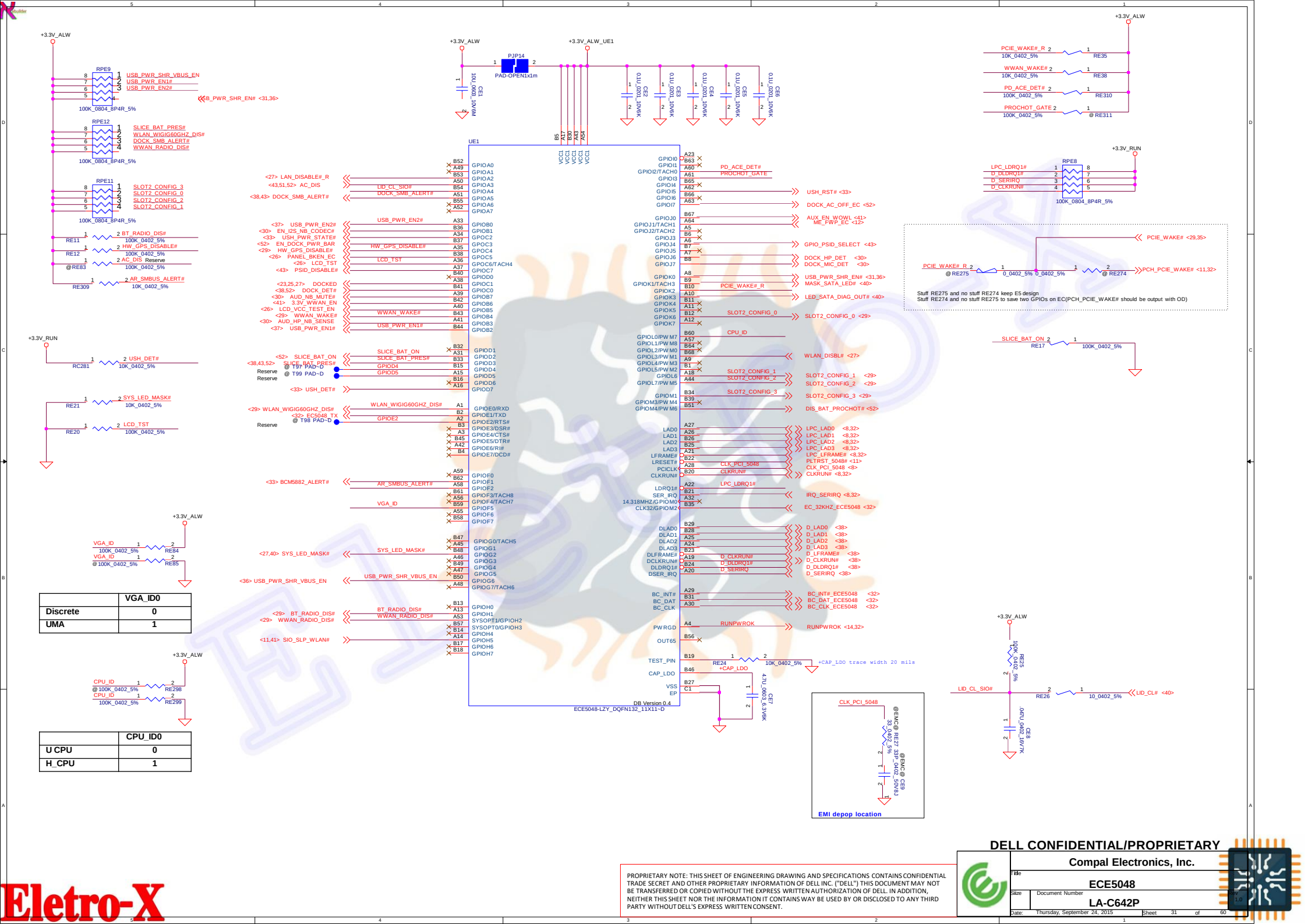
Compal Electronics, Inc.	
Title:	Codec ALC3235
Size	Document Number: LA-C642P
Rev	1.0
Date:	Thursday, September 24, 2015
Sheet	30 of 60



	VGA_ID0
Discrete	0
UMA	1

	CPU_ID0
U CPU	0
H_CPU	1

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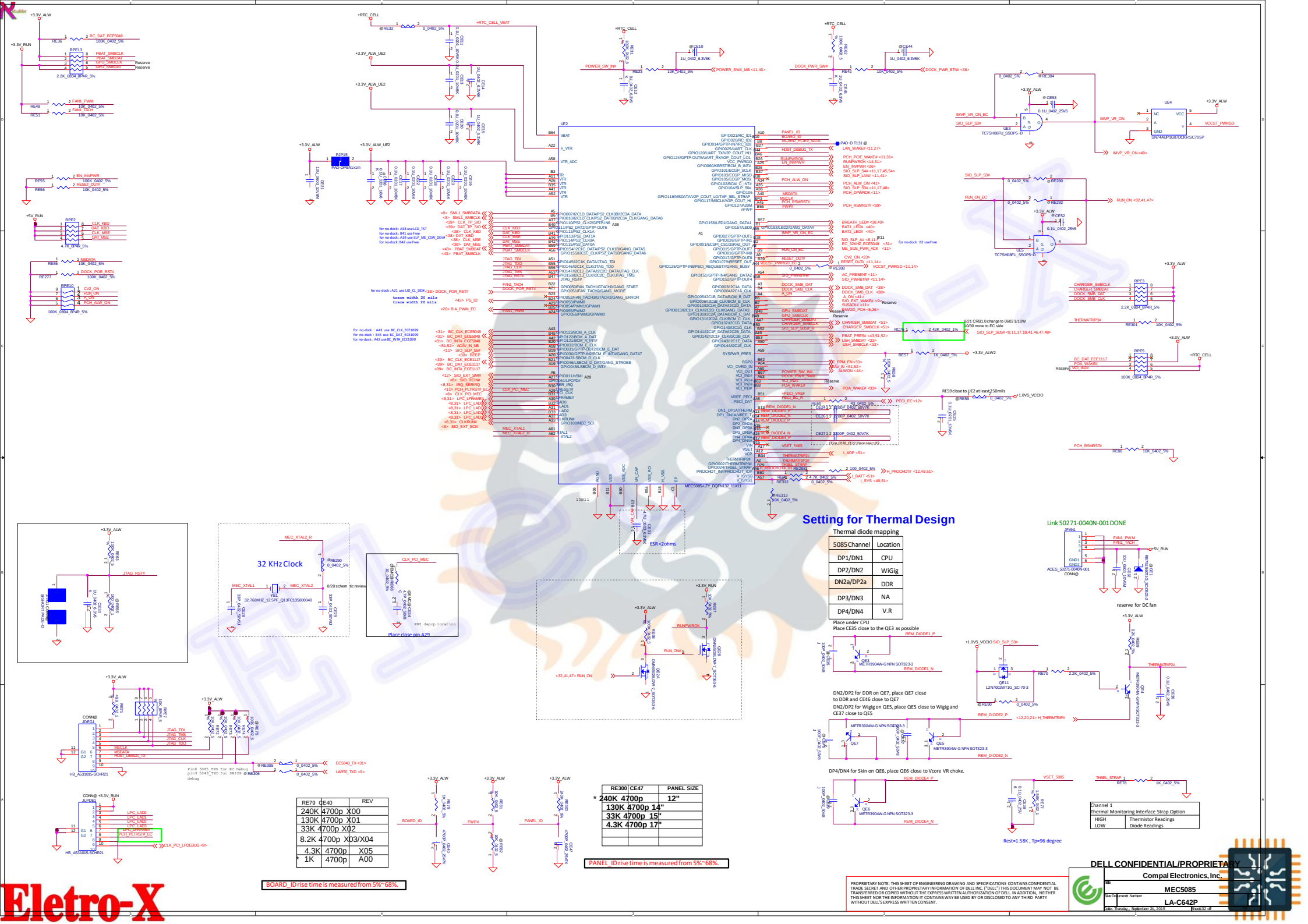
Compal Electronics, Inc.

Title: ECE5048

Size: | Document Number: LA-C642P | Rev: 1.0

Date: Thursday, September 24, 2015 | Sheet 31 of 60


Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | WiGig
DN2a/DP2a | DDR
DP3/DN3 | NA
DP4/DN4 | V.R
Place under CPU
Place CE35 close to the QE3 as possible
DN2/DP2 for DDR on QE7, place QE7 close to DDR and CE46 close to QE7
DN2/DP2 for Wigig on QE5, place QE5 close to Wigig and CE37 close to QE5
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
Rest=1.58K , Tp=96 degree
Link 50271-0040N-001 DONE
reserve for DC fan
32 KHz Clock
ESR<2ohms
Place close pin A29
RE79 | CE40 | REV
240K 4700p X00
130K 4700p X01
33K 4700p X02
8.2K 4700p X03/X04
4.3K 4700p X05
* 1K 4700p A00
RE300 | CE47 | PANEL SIZE
* 240K 4700p 12"
130K 4700p 14"
33K 4700p 15"
4.3K 4700p 17"
BOARD_ID rise time is measured from 5%~68%.
PANEL_ID rise time is measured from 5%~68%.
Channel 1
Thermal Monitoring Interface Strap Option
HIGH | Thermistor Readings
LOW | Diode Readings
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Compal Electronics, Inc.
MEC5085
LA-C642P
Eletro-X

power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)

+3.3V_M — @ RZ72 — 0_0603_5%

+3.3V_ALW_PCH — PJP11 — PAD-OPEN1x1m — +3.3V_M_TPM

+3.3V_M_TPM — RZ69 — TPM_PIRQ# — 10K_0402_5%

7/18 vender suggest.

+3.3V_M_TPM — @ RZ88 — 0_0402_5% — +UZ12_TPM

+3.3V_RUN — @ RZ89 — 0_0402_5% — +UZ12_TPM

+3.3V_ALW — @RZ8 — USH_SMBCLK — 2.2K_0402_5%

@RZ9 — USH_SMBDAT — 2.2K_0402_5%

RZ10 — USH_PWR_STATE# — 1M_0402_5%

+3.3V_RUN — @ RZ90 — 10K_0402_5%

<11,17,47> SIO_SLP_S0# — @ RZ112 — 0_0402_5% — TPM_LPM#

UZ12

GPIO0/SDA/XOR_OUT
GPIO1/SCL
GPIO2/GPX
GPIO3/BADD

<8> PCH_SPI_D1_R1 — RZ58 — 33_0402_5% — PCH_SPI_D1_2_R — LAD0/MISO
<8> PCH_SPI_D0_R1 — RZ59 — 33_0402_5% — PCH_SPI_D0_2_R — LAD1/MOSI
<8> TPM_PIRQ# — LAD2/SPI_IRQ#
LAD3

<8> PCH_SPI_CLK_R1 — RZ60 — 33_0402_5% — PCH_SPI_CLK_2_R — LCKL/SCLK
<8> PCH_SPI_CS#2 — @ RZ61 — 0_0402_5% — PCH_SPI_CS#2_R — LFRAME#/SCS#

<11> PLTRST_TPM# — LRESET#/SPI_RST#/SRESET#
SERIRQ
@RZ110 — 0_0402_5% — TPM_GPIO4 — CLKRUN#/GPIO4/SINT#
LPCPD#
RP
TEST

RZ62 10K_0402_5%

NPCT650JAAYX_QFN32_5X5

VSB
VDD
VDD
VDD
NC
GND
PGND
Reserved

+3.3V_M_TPM — +3.3V_ALW

+UZ12_TPM

0.1U_0201_10V6K — CZ274
0.1U_0201_10V6K — CZ275
10U_0603_10V6M — CZ276
0.1U_0201_10V6K — CZ273
0.1U_0201_10V6K — CZ271
10U_0603_10V6M — CZ272

place CZ73 as close as UZ12.8
CZ74,CZ76 as close as UZ12.14
CZ75 as close as UZ12.22

place CZ71,CZ72 as close as UZ12.1

USH CONN

+PWR_SRC — @ RZ85 — 0_0402_5% — +PWR_SRC_R
+3.3V_ALW2 — @ RZ84 — 0_0402_5% — +3.3V_ALW2_R

<32> CV2_ON
<32> POA_WAKE#
<32> EC_FPM_EN

<10> USB20_N7
<10> USB20_P7

<32> USH_SMBCLK
<32> USH_SMBDAT
<31> BCM5882_ALERT#

+3.3V_ALW

+5V_ALW2 — @ RZ86 — 0_0402_5% — +5V_ALW2_R

+5V_ALW
+3.3V_RUN
+5V_RUN — PCH_PLTRST#_AND_R

<31> USH_PWR_STATE#
<12> CONTACTLESS_DET#

<31> USH_DET# — @RZ87 — 0_0402_5% — USH_DET#_R1 — DZ7 — RB751S40T1G_SOD523-2

JUSH1 CONN@
GND
GND
E-T_6705K-Y26N-00L

<11,28,29,35> PCH_PLTRST#_AND — @RZ114 — 0_0402_5% — @RZ115 — 0_0402_5% — <31> USH_RST#

PCH_SPI_CLK_2_R — RZ63 33_0402_5% — @EMC@ — 0.1U_0402_25V6 — CZ77 — @EMC@

+3.3V_M_TPM

PCH_SPI_CS#2_R — RZ113 — 100_0402_5% — LP2301ALT1G_SOT23-3 — QZ9

TPM_LPM# — RZ111 — 10K_0402_5%

RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A

PCH_PLTRST#_AND — .047U_0402_16V7K — EMC@ — CZ68

For ESD solution

+5V_ALW2 — 0.1U_0201_10V6K — CZ294
+3.3V_ALW2 — 0.1U_0201_10V6K — CZ224
+5V_RUN — 0.1U_0201_10V6K — CZ210
+3.3V_RUN — 0.1U_0201_10V6K — CZ211
+3.3V_ALW — 0.1U_0201_10V6K — CZ212

Close to JUSH1

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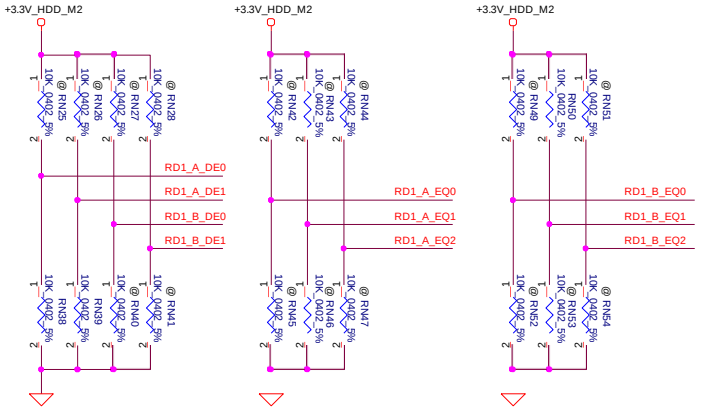
Compal Electronics, Inc.

Title: USH & TPM

Size: — Document Number: LA-C642P

Date: Thursday, September 24, 2015 — Sheet 33 of 50



Programmable output de-emphasis level setting for channel A .
A_DE0: internally pulled up at ~150K;
A_DE1 internally pulled down at ~150K

[A_DE1,A_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

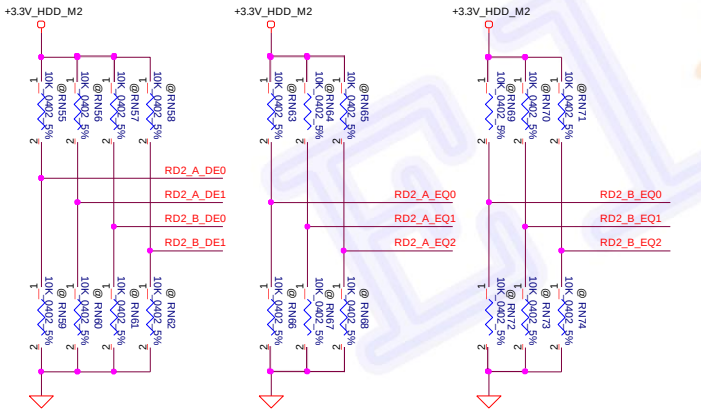
[A_EQ2,A_EQ1,A_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HHL: EQ Level4
LLH: EQ Level5
LHH: EQ Level6
HLH: EQ Level7
HHH: EQ Level8

Programmable output de-emphasis level setting for channel B.
B_DE0: internally pulled up at ~150K;
B_DE1 internally pulled down at ~150K

[B_DE1,B_DE0] ==
LL: -7.5dB
HL: -2dB
LH: -3.5dB (default)
HH: -6dB

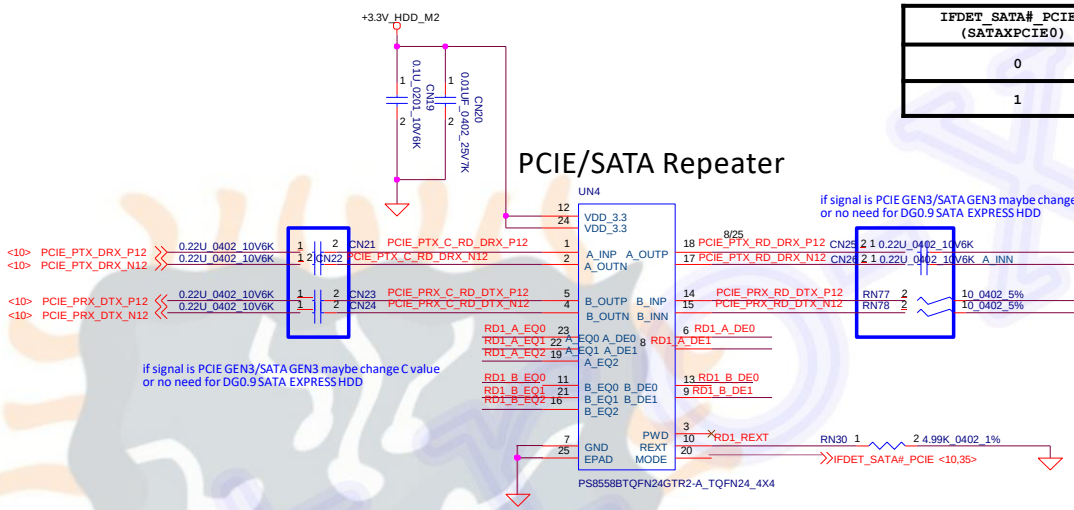
Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

[B_EQ2,B_EQ1,B_EQ0] ==
LLL: EQ Level1(default)
LHL: EQ Level2
HLL: EQ Level3
HHL: EQ Level4
LLH: EQ Level5
LHH: EQ Level6
HLH: EQ Level7
HHH: EQ Level8



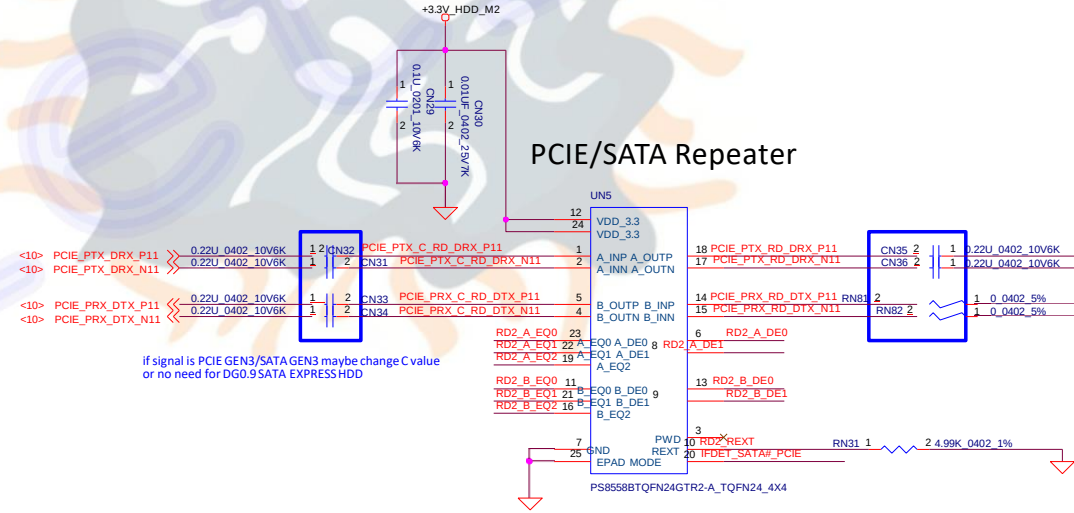
IFDET_SATA#_PCIE (SATAXPCIE0)	FLEX IO 11
0	PCIE
1	SATA

PCIE/SATA Repeater



PWD	Funtion
0	Normal mode(default)
1	power down mode

PCIE/SATA Repeater



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

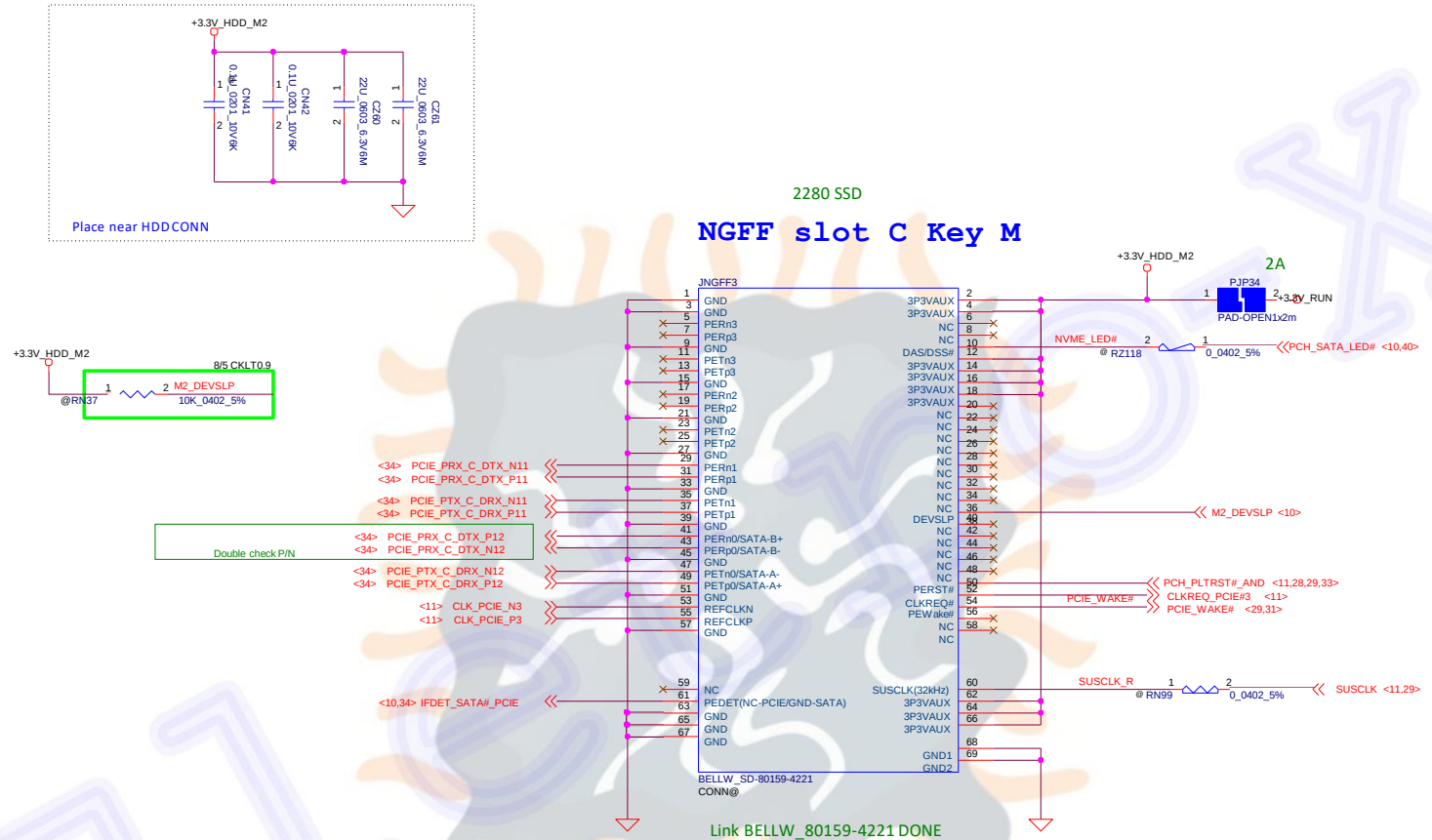
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Mini Card-2/2

Size: Document Number: LA-C642P Rev:

Date: Thursday, September 24, 2015 Sheet 34 of 60



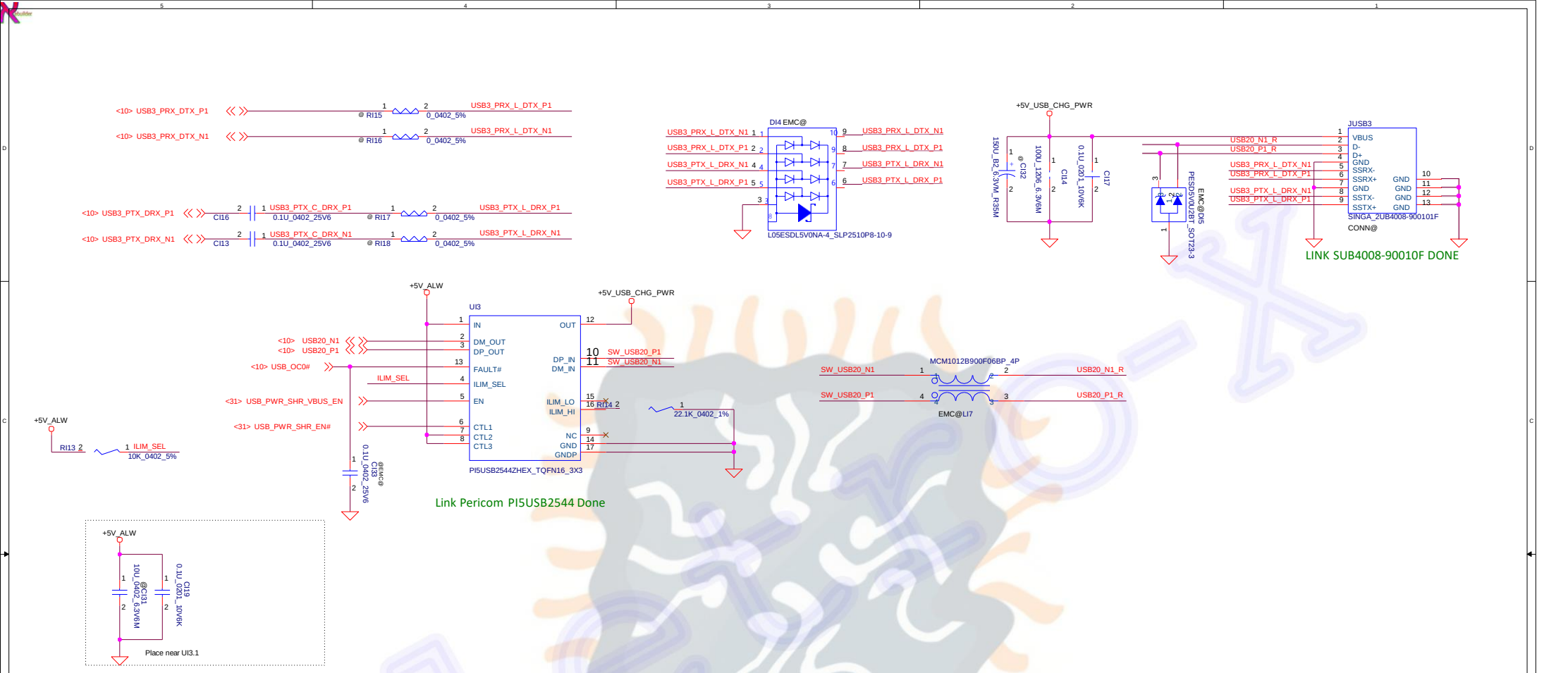
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: HDD CONN

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 35 of

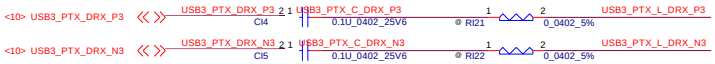


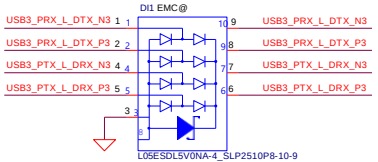
Compal Electronics, Inc.

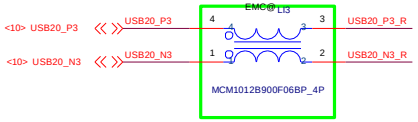
Title: USB SW

Size: | Document Number: LA-C642P

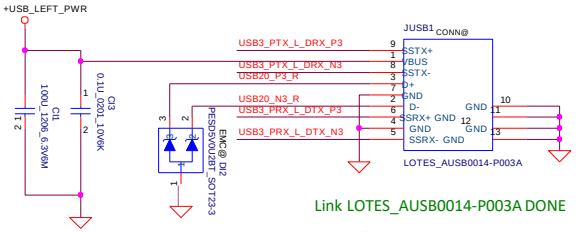
Date: Thursday, September 24, 2015 | Sheet 38 of



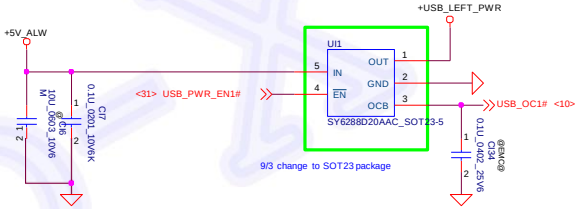




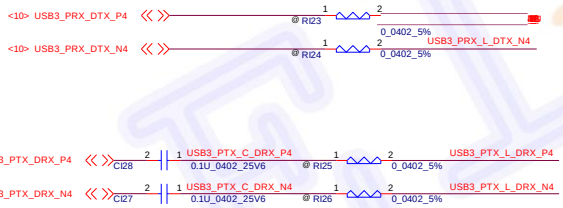
8/19 for layout routing change

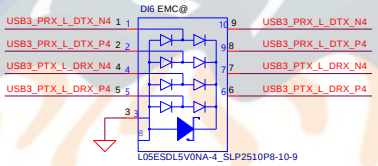


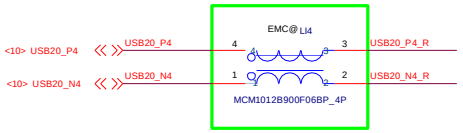
Link LOTES_AUSB0014-P003A DONE



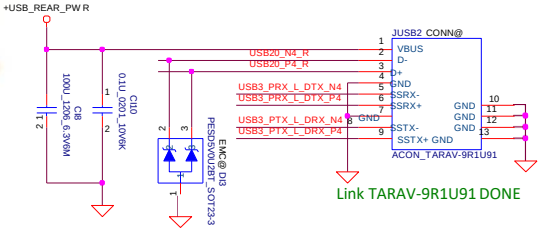
9/3 change to SOT23 package



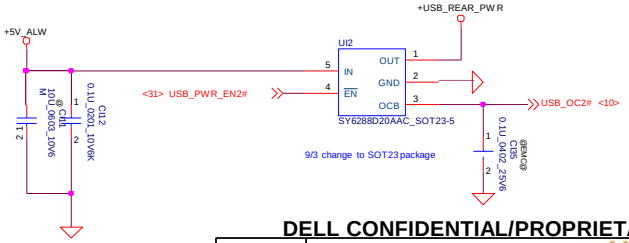




8/19 for layout routing change



Link TARAV-9R1U91 DONE



9/3 change to SOT23 package

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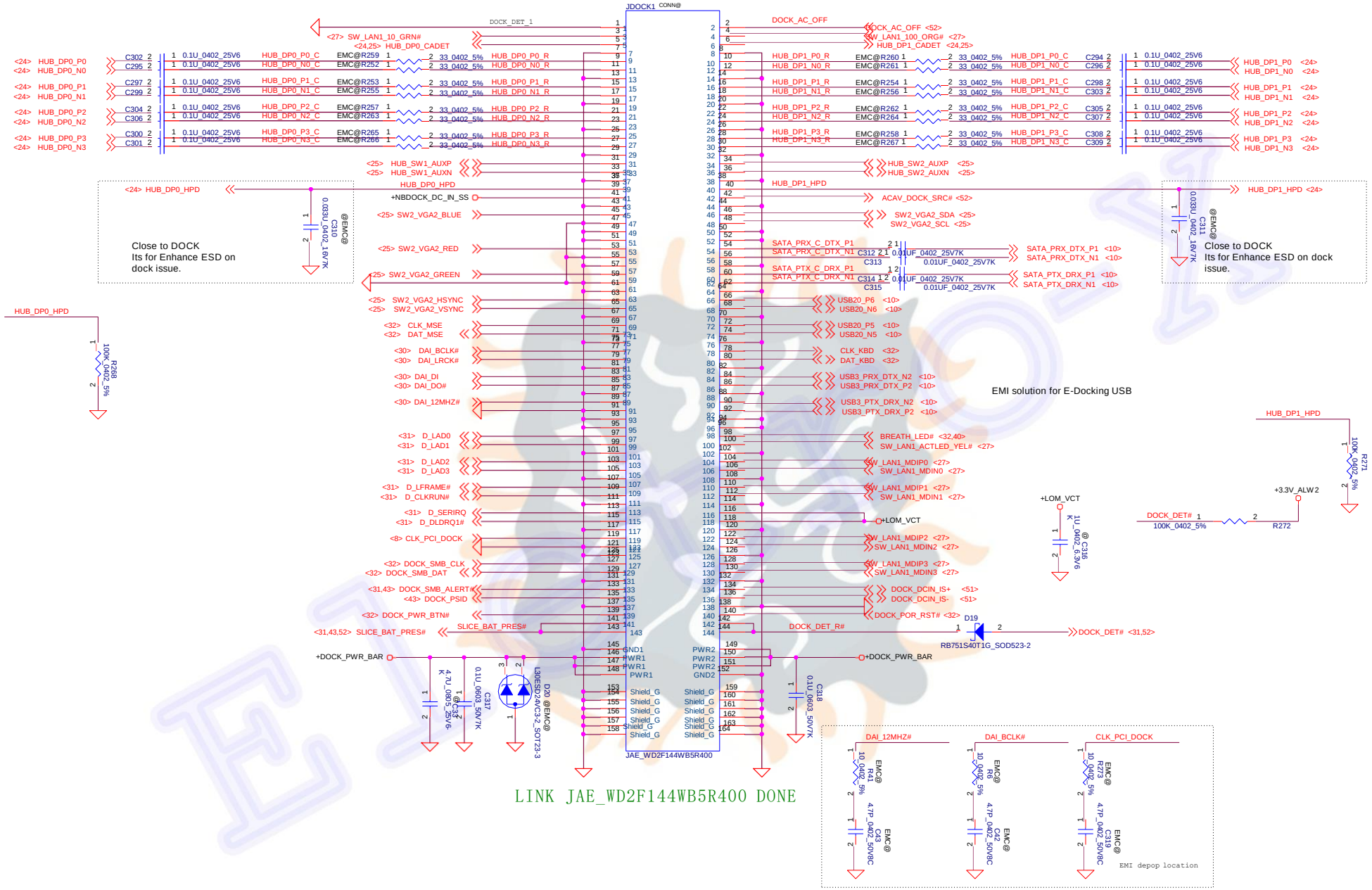
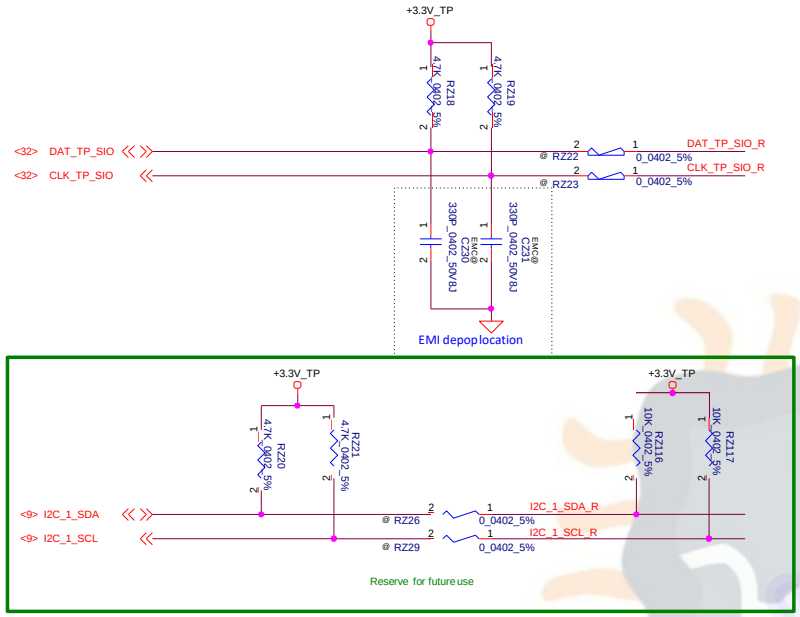
Compal Electronics, Inc.	
Title	USB3.0
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 37 of 56



Compal Electronics, Inc.

Title	E-Dock
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 38 of 60

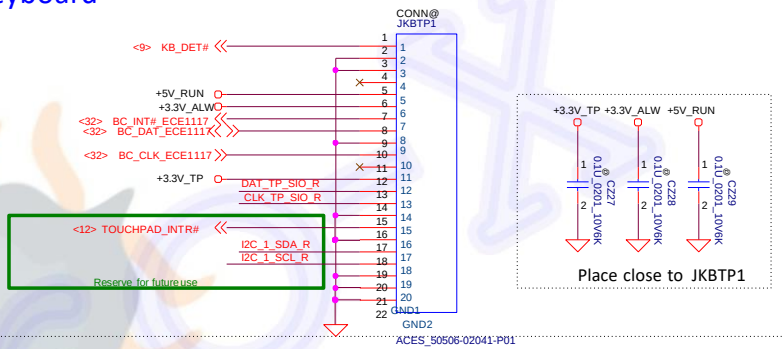
Touch Pad



+3.3V_RUN — PJP16 — +3.3V_TP

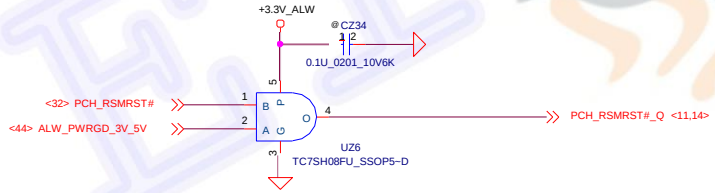
PAD-OPEN1x1m

Keyboard



Link 50506-02041-P0 DONE

RSMRST circuit



@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@ LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@ TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

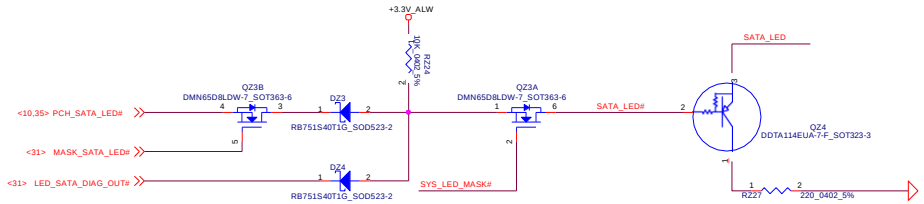
Compal Electronics, Inc.

Title: Keyboard

Size: | Document Number: LA-C642P

Date: Thursday, September 24, 2015 | Sheet 39 of

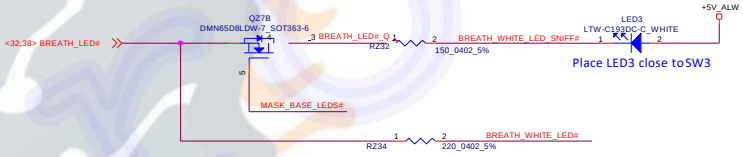
HDD LED solution for White LED

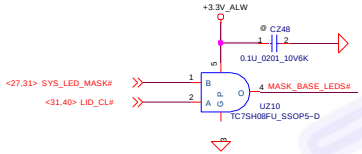


Battery LED

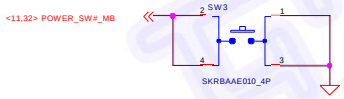
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

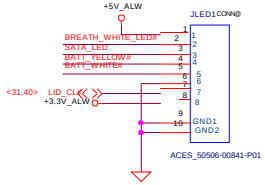




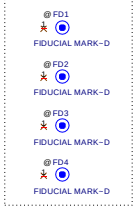
POWER & INSTANT ON SWITCH



LED board CONN

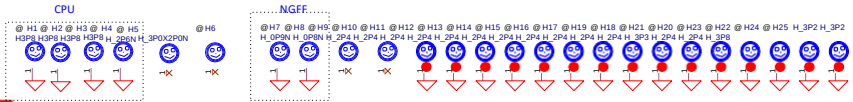


Fiducial Mark



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

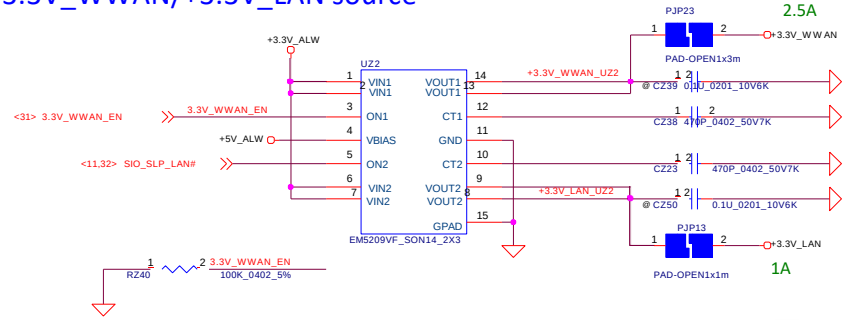
Title: PAD, LED

Size: Document Number: LA-C642P

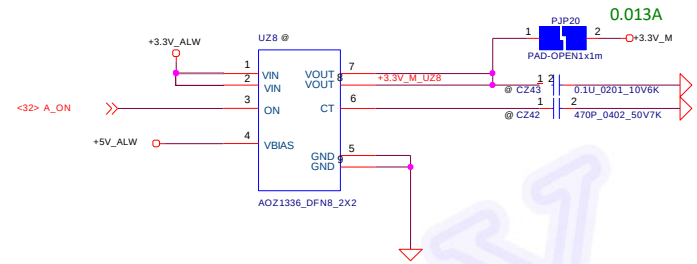
Rev: 1.0

Date: Thursday, September 24, 2015 Sheet 40 of 40

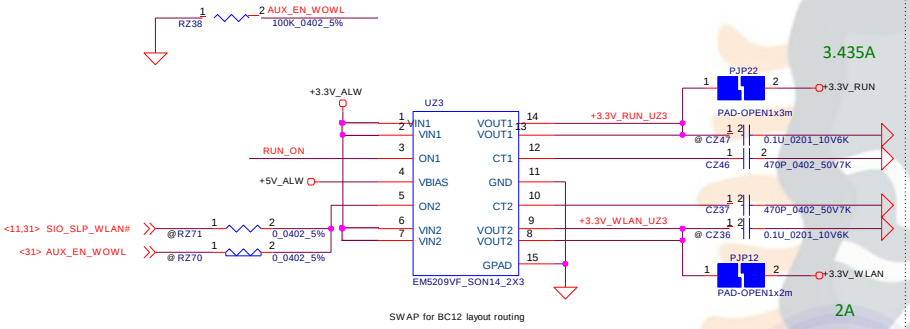
+3.3V_WWAN/+3.3V_LAN source



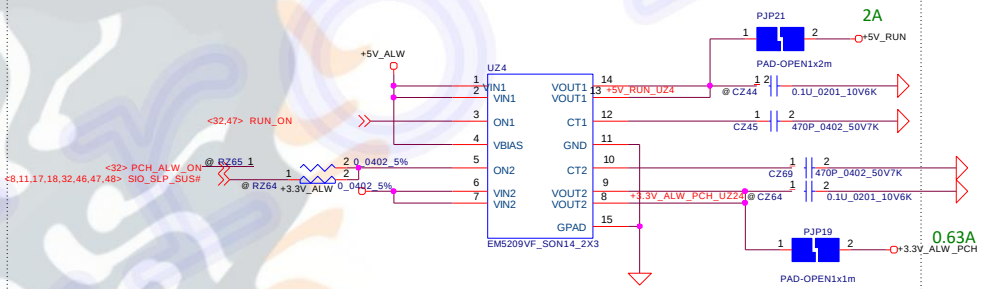
+3.3V_M source



+3.3V_WLAN/+3.3V_RUN source



+5V_RUN/+3.3V_ALW_PCH source

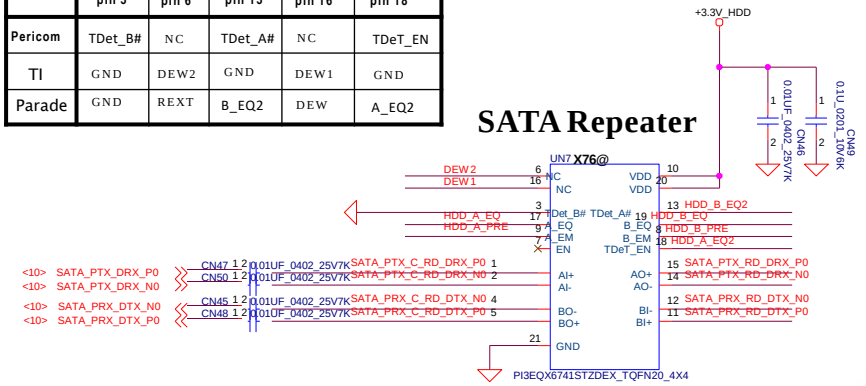


DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Power control
Size	Document Number: LA-C642P
Date: Thursday, September 24, 2015	Sheet 41

	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

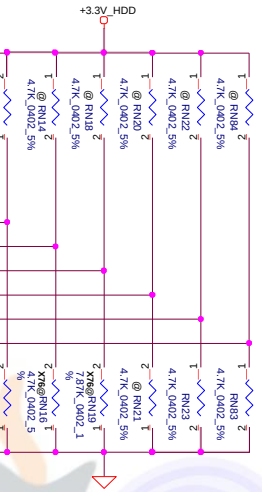
SATA Repeater

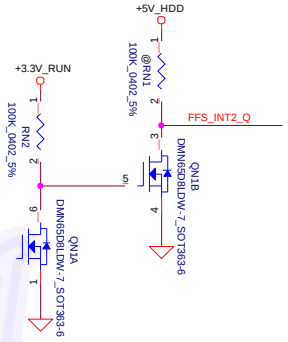


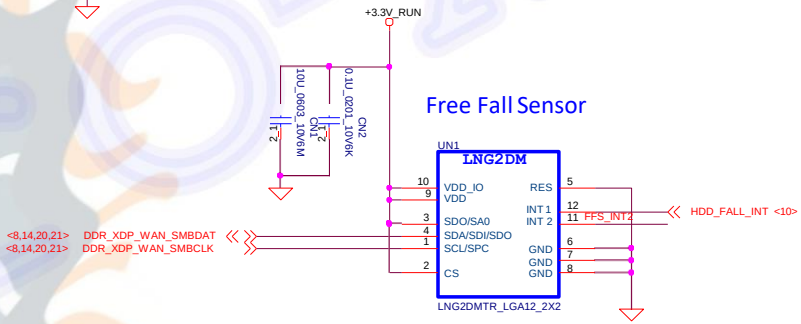
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	NC	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

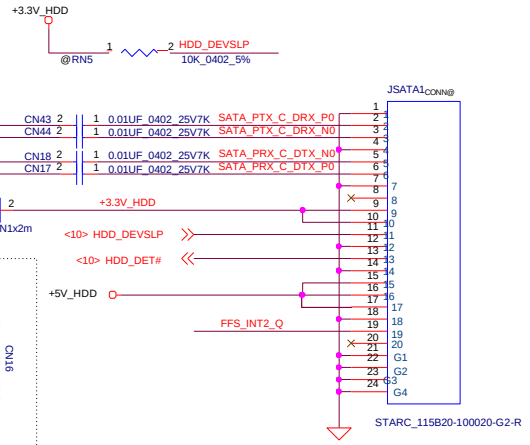
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-4dB	-4dB
		1	14dB	14dB	1	-2dB	-2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2)	A_EQ	B_EQ		A_EM	B_EM
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

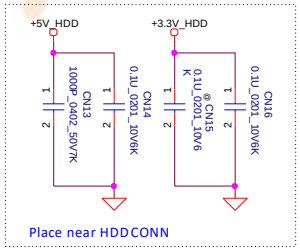
* red color is current setting

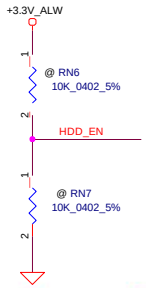


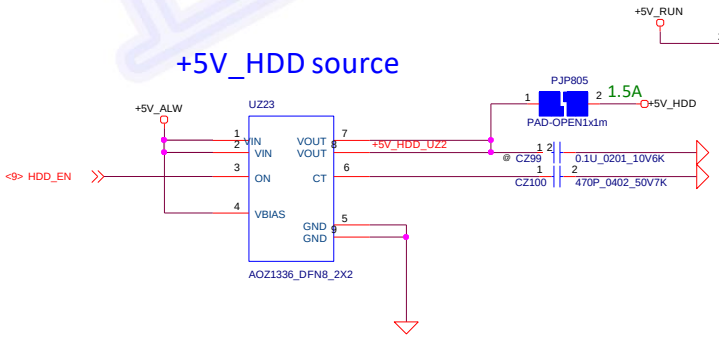










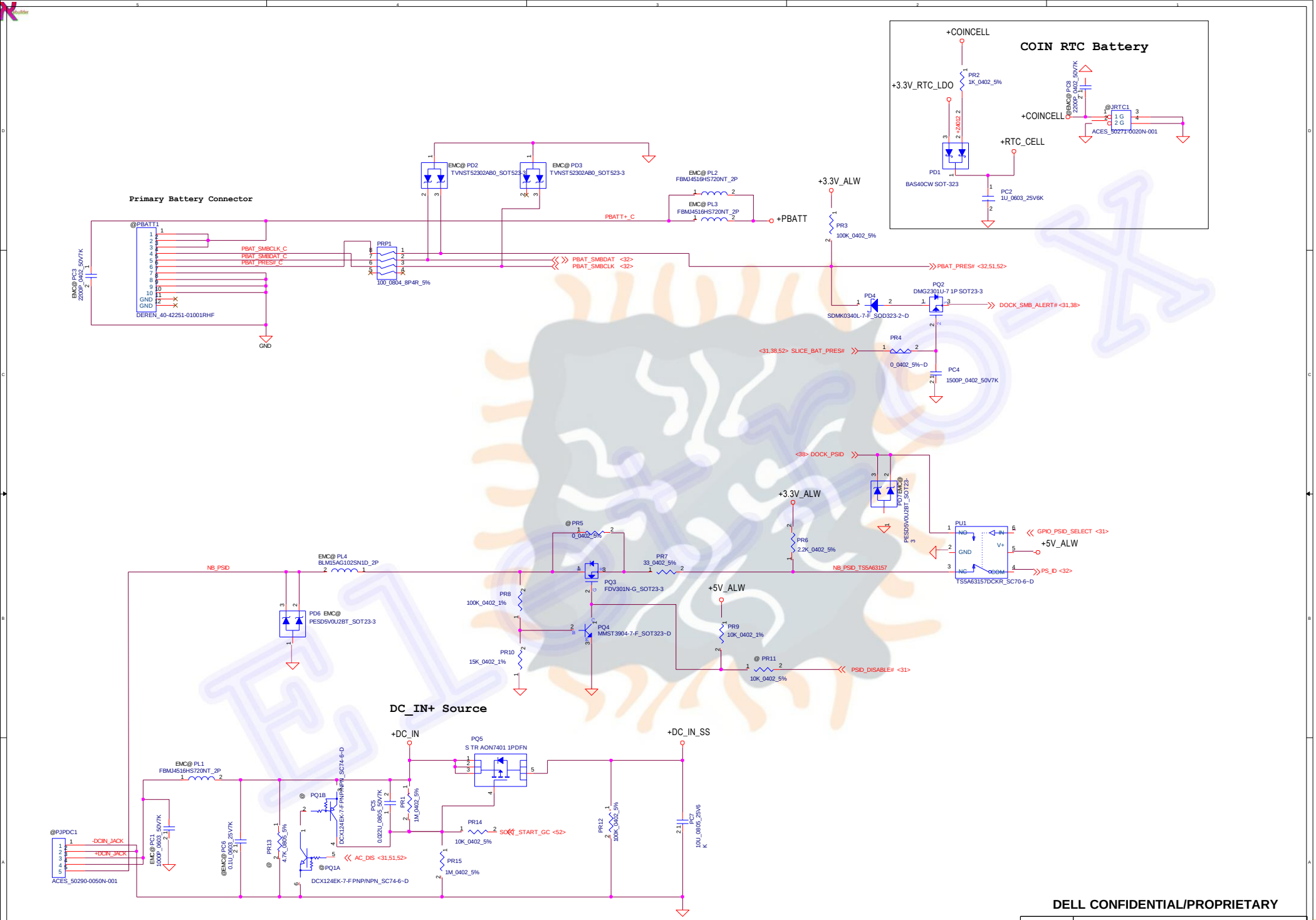


Compal Electronics, Inc.

Title: HDD CONN

Size: Document Number: LA-C642P

Date: Thursday, September 24, 2015 Sheet 42 of 50



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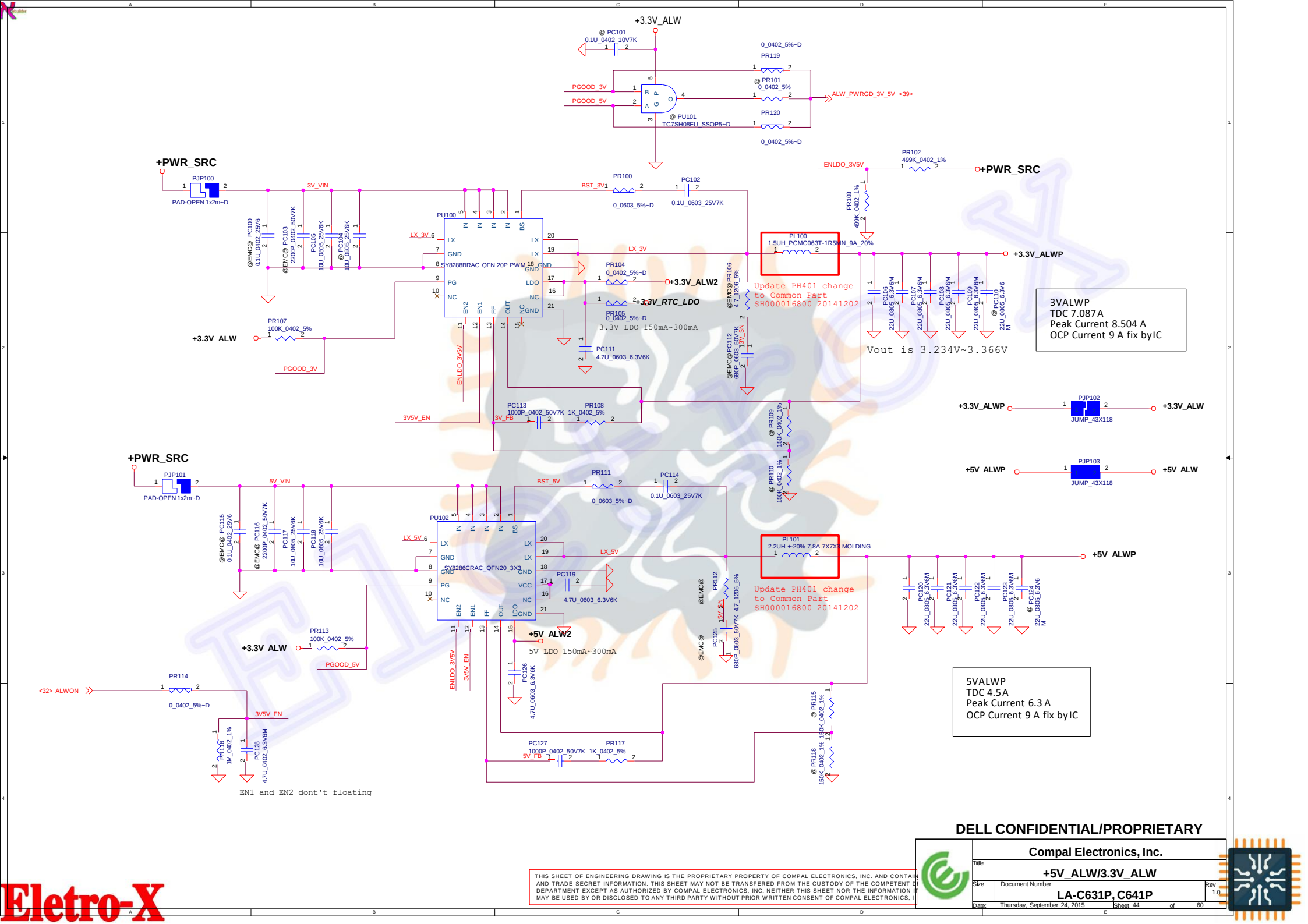
Compal Electronics, Inc.

Title: +DCIN

Size: | Document Number: LA-C631P, C641P | Rev: 1.0

Date: Thursday, , September 24, 2015 | Sheet 43 of 60



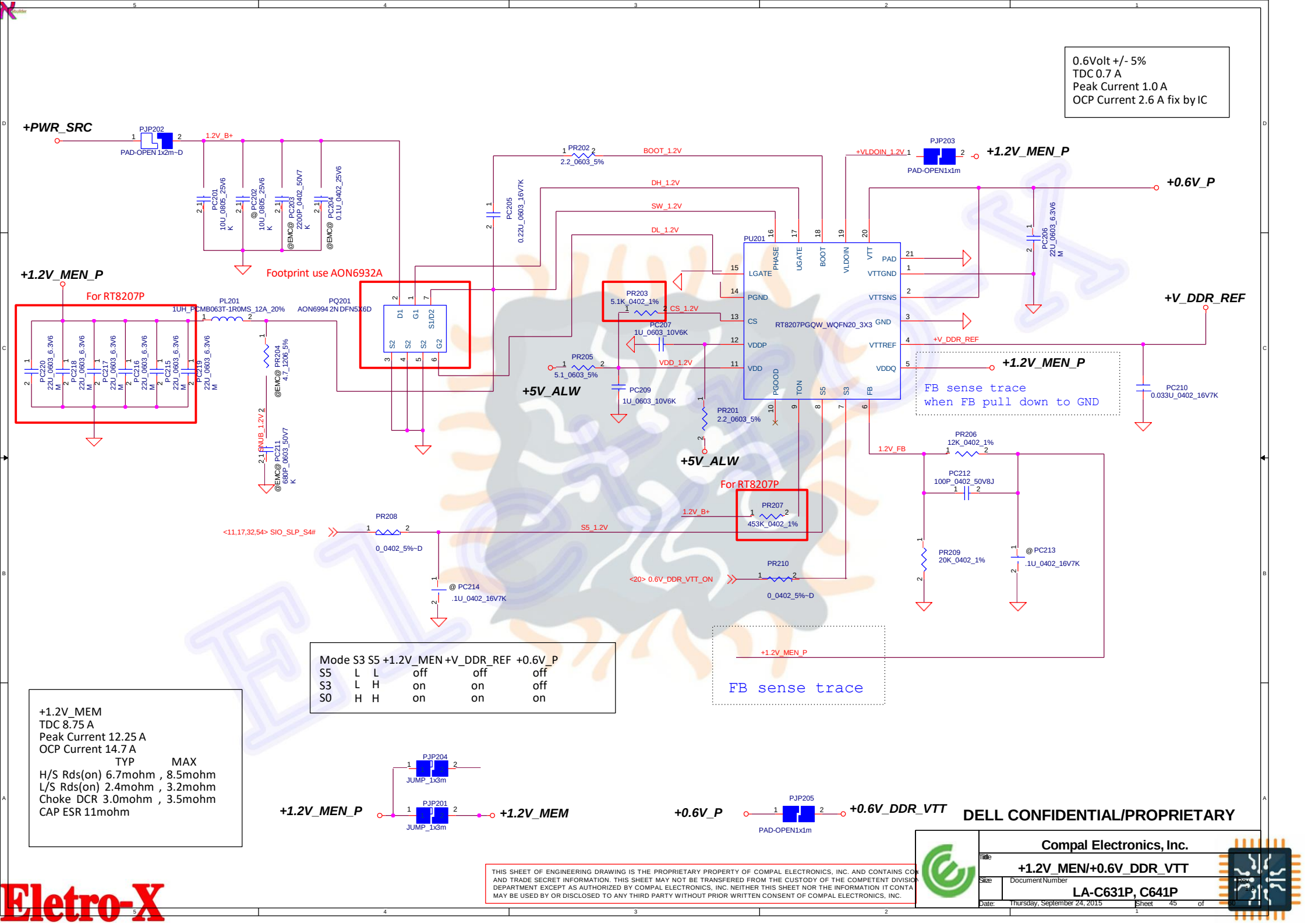
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size: | Document Number: LA-C631P, C641P | Rev: 1.0

Date: Thursday, September 24, 2015 | Sheet 44 of 60


0.6Volt +/- 5%
TDC 0.7 A
Peak Current 1.0 A
OCP Current 2.6 A fix by IC
+PWR_SRC
PJP202
PAD-OPEN 1x2m~D
1.2V_B+
PC201 10U_0805_25V6 K
@ PC202 10U_0805_25V6 K
@EMC@ PC203 2200P_0402_50V7 K
@EMC@ PC204 0.1U_0402_25V6
PR202 2.2_0603_5%
BOOT_1.2V
PC205 0.22U_0603_16V7K
DH_1.2V
SW_1.2V
DL_1.2V
PJP203
PAD-OPEN1x1m
+1.2V_MEN_P
+0.6V_P
PC206 22U_0603_6.3V6 M
+V_DDR_REF
+1.2V_MEN_P
For RT8207P
Footprint use AON6932A
PL201 1UH_PCMB063T-1R0MS_12A_20%
PQ201 AON6994 2N DFN5X6D
PC220 22U_0603_6.3V6 M
PC218 22U_0603_6.3V6 M
PC217 22U_0603_6.3V6 M
PC216 22U_0603_6.3V6 M
PC215 22U_0603_6.3V6 M
PC219 22U_0603_6.3V6 M
@EMC@ PR204 4.7_1206_5%
@EMC@ PC211 680P_0603_50V7 K
PR203 5.1K_0402_1%
CS_1.2V
PC207 1U_0603_10V6K
PR205 5.1_0603_5%
VDD_1.2V
PC209 1U_0603_10V6K
PR201 2.2_0603_5%
+5V_ALW
PU201
RT8207PGQW_WQFN20_3X3
LGATE
PHASE
UGATE
BOOT
VLDOIN
VTT
PAD
VTTGND
VTTSNS
GND
VTTREF
VDDQ
PGND
CS
VDDP
VDD
PGOOD
TON
S5
S3
FB
FB sense trace
when FB pull down to GND
PC210 0.033U_0402_16V7K
PR206 12K_0402_1%
1.2V_FB
PC212 100P_0402_50V8J
PR209 20K_0402_1%
@ PC213 .1U_0402_16V7K
For RT8207P
PR207 453K_0402_1%
PR208 0_0402_5%~D
<11,17,32,54> SIO_SLP_S4#
S5_1.2V
@ PC214 .1U_0402_16V7K
PR210 0_0402_5%~D
<20> 0.6V_DDR_VTT_ON
FB sense trace
Mode S3 S5 +1.2V_MEN +V_DDR_REF +0.6V_P
S5 L L off off off
S3 L H on on off
S0 H H on on on
+1.2V_MEM
TDC 8.75 A
Peak Current 12.25 A
OCP Current 14.7 A
TYP MAX
H/S Rds(on) 6.7mohm , 8.5mohm
L/S Rds(on) 2.4mohm , 3.2mohm
Choke DCR 3.0mohm , 3.5mohm
CAP ESR 11mohm
PJP204
JUMP_1x3m
PJP201
JUMP_1x3m
+1.2V_MEN_P
+1.2V_MEM
+0.6V_P
PJP205
PAD-OPEN1x1m
+0.6V_DDR_VTT
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Compal Electronics, Inc.
Title
+1.2V_MEN/+0.6V_DDR_VTT
Size
Document Number
LA-C631P, C641P
Rev
1.0
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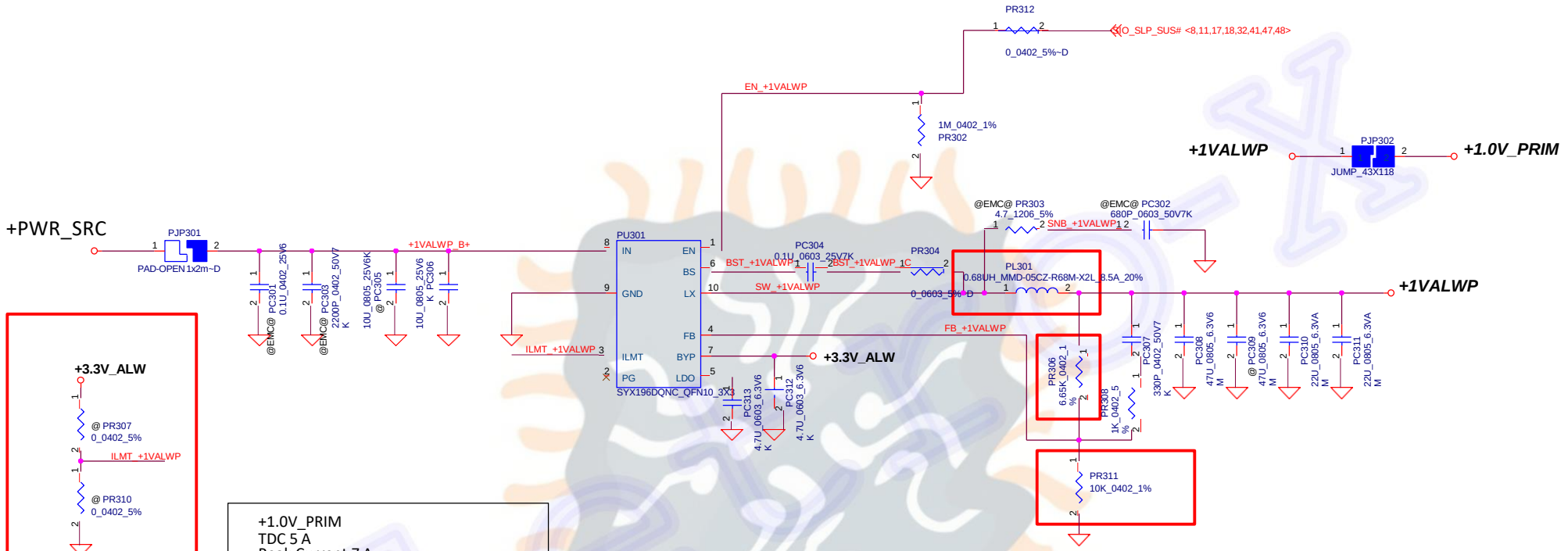
Eletro-X



+1.0V_PRIM
TDC 5 A
Peak Current 7 A
OCP Current 9 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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Compal Electronics, Inc.

Title	+1VALWP	
Size	Document Number	Rev
	LA-C631P, C641P	1.0
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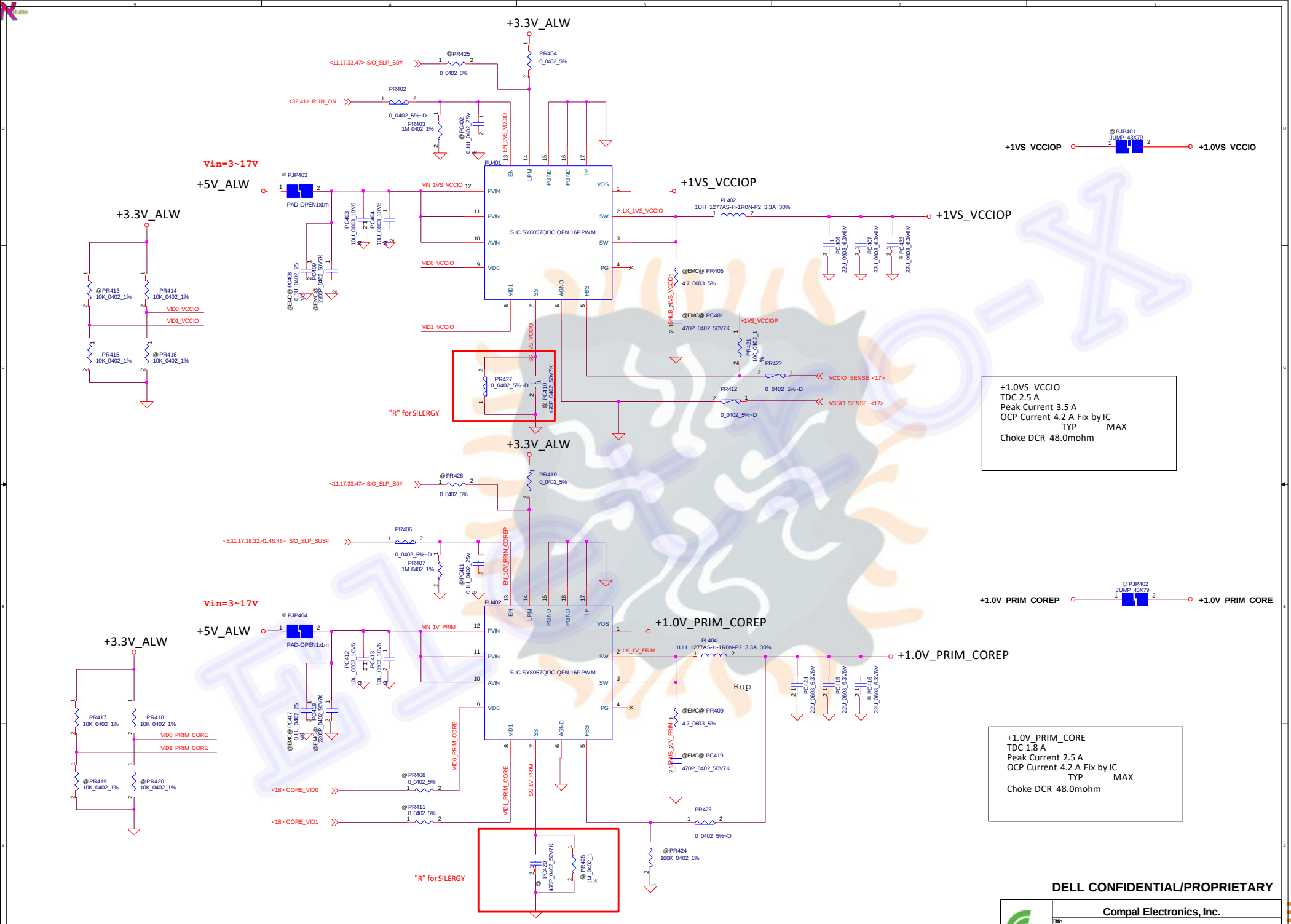
+3.3V_ALW
<11,17,33,47> SIO_SLP_S0#
@PR425
0_0402_5%
PR404
0_0402_5%
PR402
<32,41> RUN_ON
0_0402_5%~D
PR403
1M_0402_1%
@PC402
0.1U_0402_25V
EN_1VS_VCCIO
Vin=3~17V
+5V_ALW
@ PJP403
PAD-OPEN1x1m
PU401
S IC SY8057QDC QFN 16PPWM
EN
LPM
PGND
PGND
TP
VOS
PVIN
PVIN
AVIN
VID0
VID1
SS
AGND
FBS
SW
SW
PG
VIN_1VS_VCCIO
VID0_VCCIO
VID1_VCCIO
LX_1VS_VCCIO
SS_1VS_VCCIO
+1VS_VCCIOP
PL402
1UH_1277AS-H-1R0N-P2_3.3A_30%
PC403
10U_0603_10V6
PC404
10U_0603_10V6
@EMC@ PC408
0.1U_0402_25
PC409
2200P_0402_50V7K
@EMC@ PR405
4.7_0603_5%
@EMC@ PC401
470P_0402_50V7K
PR421
100_0402_1%
PR422
PR427
0_0402_5%~D
@ PC410
470P_0402_50V7K
"R" for SILERGY
PR412
0_0402_5%~D
VCCIO_SENSE <17>
VSSIO_SENSE <17>
PC406
22U_0603_6.3V6M
PC407
22U_0603_6.3V6M
@ PC422
22U_0603_6.3V6M
PR413
10K_0402_1%
PR414
10K_0402_1%
PR415
10K_0402_1%
@PR416
10K_0402_1%
@PJP401
JUMP_43X79
+1VS_VCCIOP
+1.0VS_VCCIO
+1.0VS_VCCIO
TDC 2.5 A
Peak Current 3.5 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm
+3.3V_ALW
<11,17,33,47> SIO_SLP_S0#
@PR426
0_0402_5%
PR410
0_0402_5%
PR406
<8,11,17,18,32,41,46,48> SIO_SLP_SUS#
0_0402_5%~D
PR407
1M_0402_1%
@PC411
0.1U_0402_25V
EN_1.0V_PRIM_COREP
Vin=3~17V
+5V_ALW
@ PJP404
PAD-OPEN1x1m
PU402
S IC SY8057QDC QFN 16PPWM
EN
LPM
PGND
PGND
TP
VOS
PVIN
PVIN
AVIN
VID0
VID1
SS
AGND
FBS
SW
SW
PG
VIN_1V_PRIM
LX_1V_PRIM
+1.0V_PRIM_COREP
PL404
1UH_1277AS-H-1R0N-P2_3.3A_30%
PC412
10U_0603_10V6
PC413
10U_0603_10V6
@EMC@ PC417
0.1U_0402_25
PC418
2200P_0402_50V7K
@EMC@ PR409
4.7_0603_5%
@EMC@ PC419
470P_0402_50V7K
VID0_PRIM_CORE
VID1_PRIM_CORE
SS_1V_PRIM
<18> CORE_VID0
<18> CORE_VID1
@PR408
0_0402_5%
@PR411
0_0402_5%
PR423
0_0402_5%~D
@PR424
100K_0402_1%
PC420
470P_0402_50V7K
@ PR428
1M_0402_1%
"R" for SILERGY
PC424
22U_0603_6.3V6M
PC415
22U_0603_6.3V6M
@ PC416
22U_0603_6.3V6M
PR417
10K_0402_1%
PR418
10K_0402_1%
@PR419
10K_0402_1%
@PR420
10K_0402_1%
@PJP402
JUMP_43X79
+1.0V_PRIM_COREP
+1.0V_PRIM_CORE
+1.0V_PRIM_COREP
TDC 1.8 A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm
Rup
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
+1VS_VCCIOP/+1.0V_PRIM_COREP
LA-C631P, C641P
1.0
Thursday, September 24, 2015
47
60
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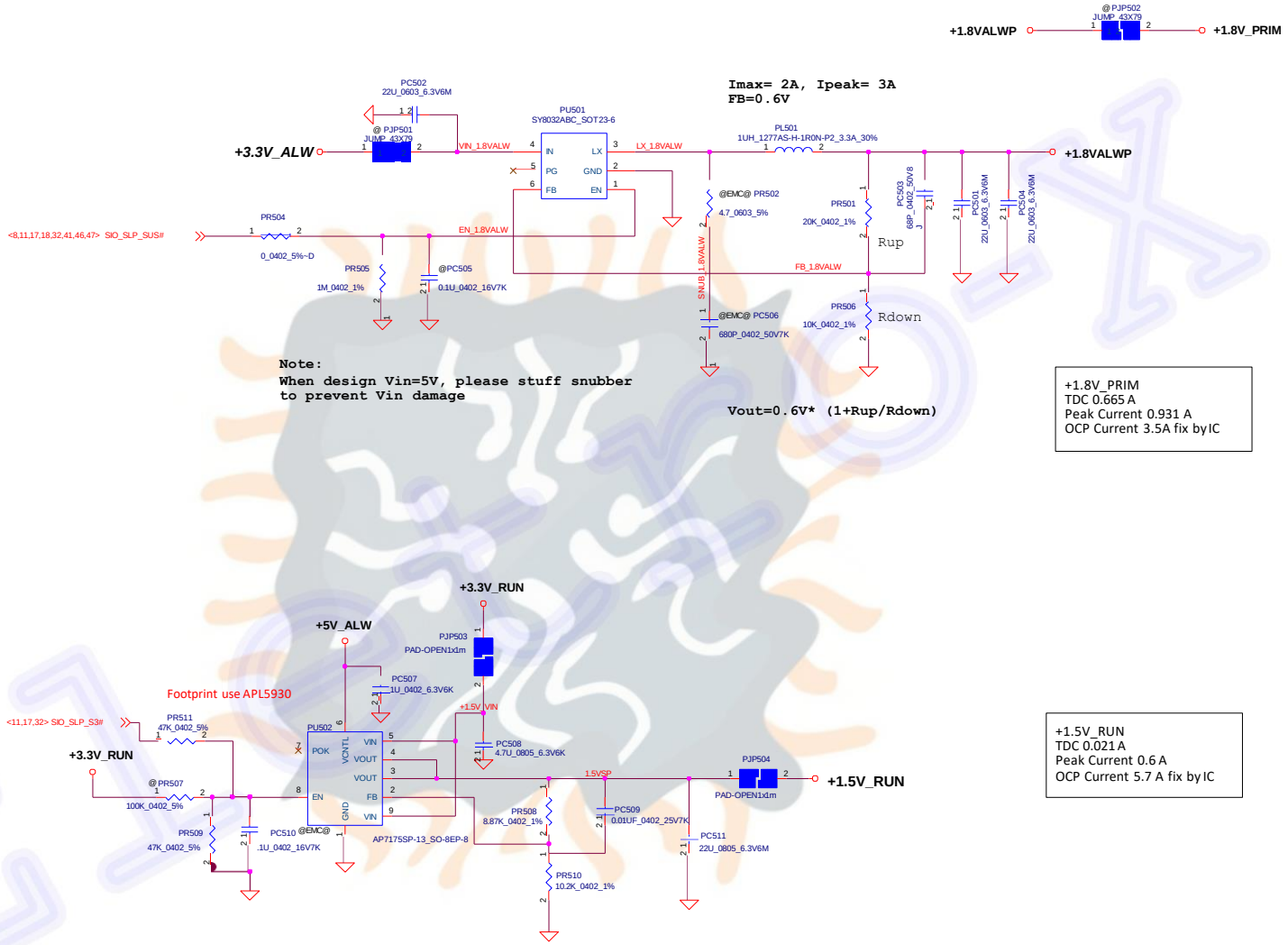

Compal Electronics, Inc.		
Title: +1.8VALWP/+1.5VSP		
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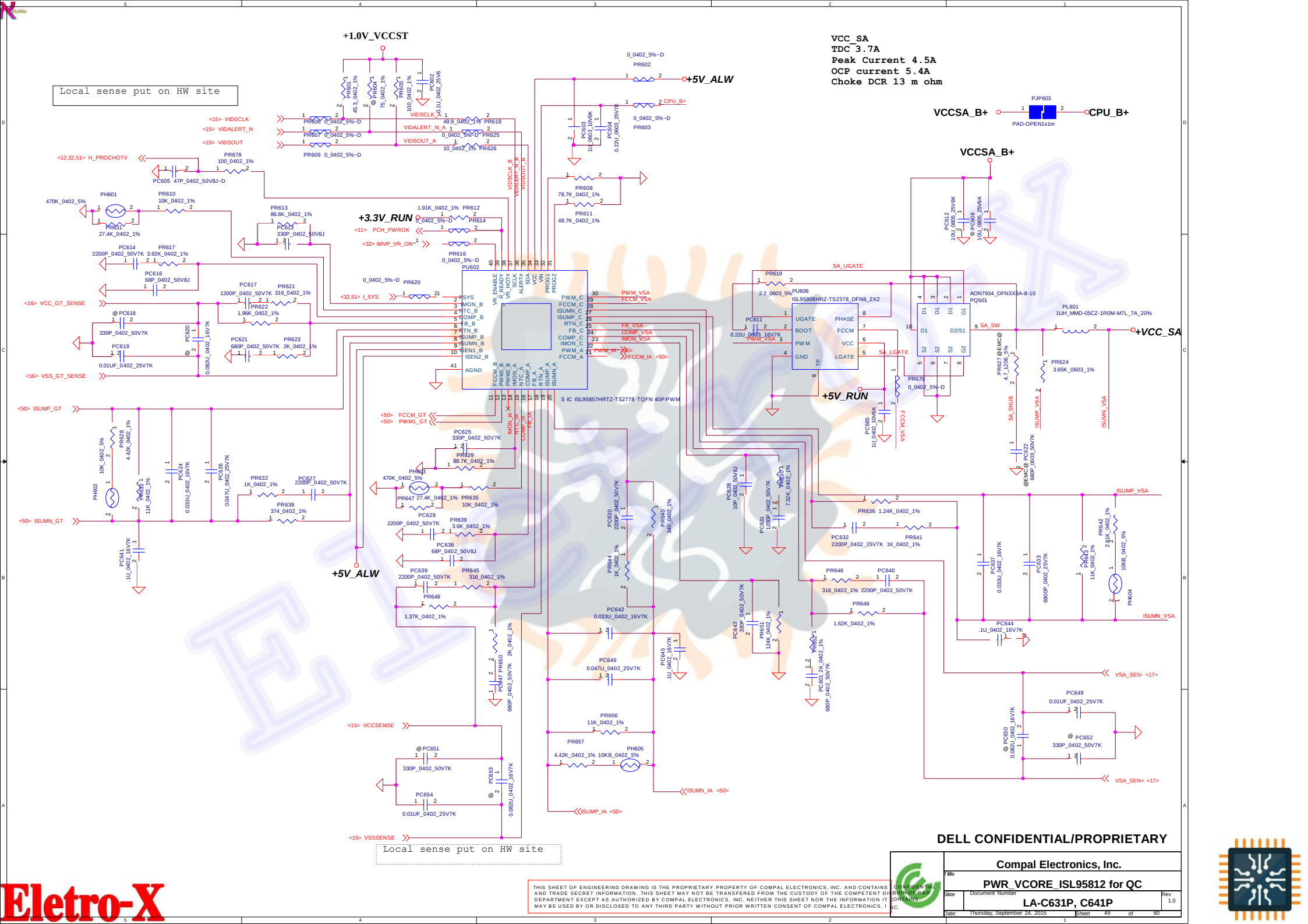

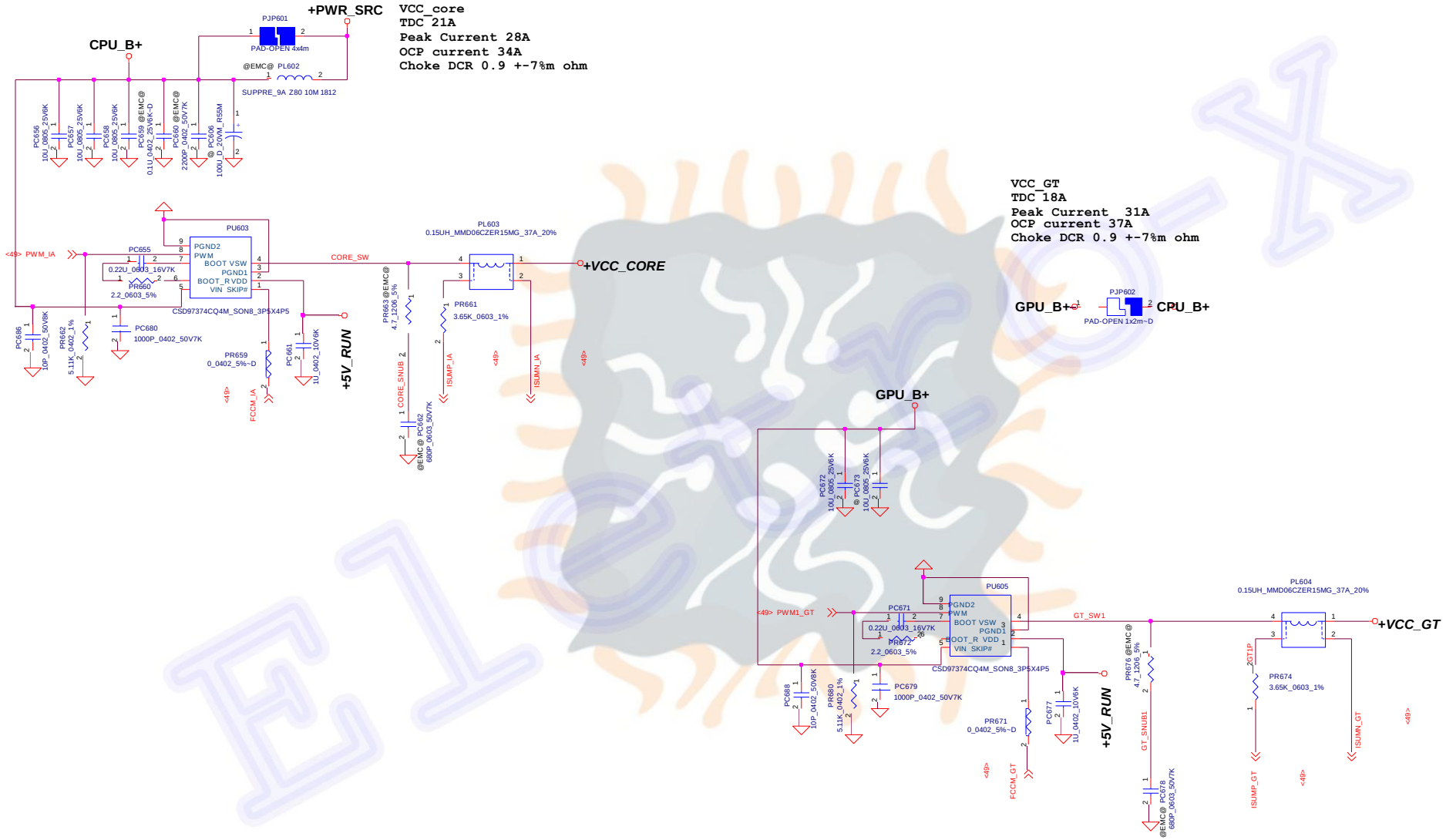

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Compal Electronics, Inc.	
Title	PWR_VCORE_ISL95812 for QC
Size	Document Number: LA-C631P, C641P
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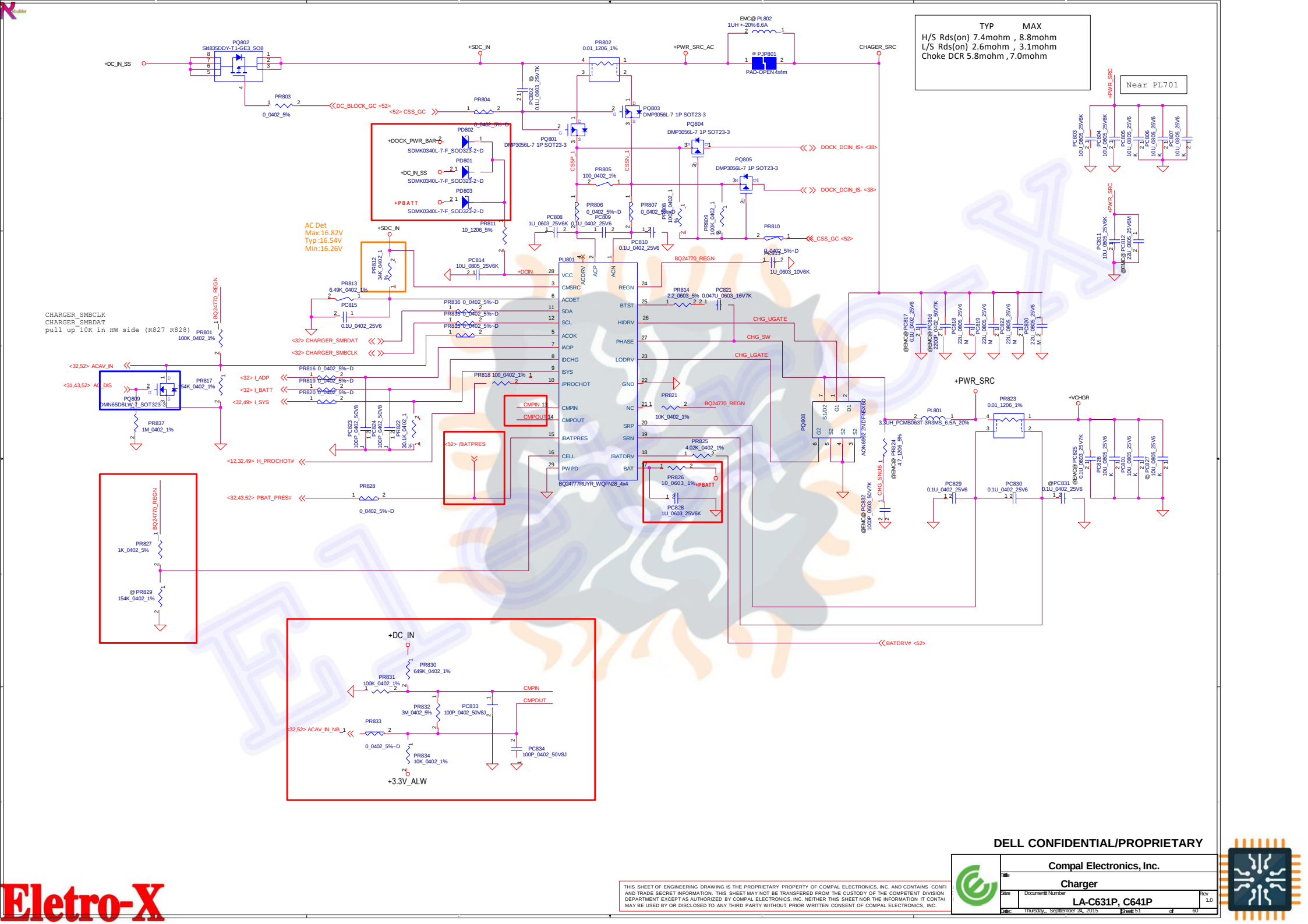
TYP MAX
H/S Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm
Near PL701
AC Det
Max:16.82V
Typ :16.54V
Min:16.26V
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)
+DC_IN_SS
+SDC_IN
+PWR_SRC_AC
CHAGER_SRC
+PWR_SRC
+VCHGR
+DCIN
+PBATT
+3.3V_ALW
BQ24770_REGN
BQ24777RUYR_WQFN28_4x4
CHG_UGATE
CHG_SW
CHG_LGATE
CMPIN
CMPOUT
/BATPRES
H_PROCHOT#
PBAT_PRES#
BATDRV# <52>
DOCK_DCIN_IS+ <38>
DOCK_DCIN_IS- <38>
CSS_GC <52>
DC_BLOCK_GC <52>
CSS_GC <52>
ACAV_IN
AC_DIS
I_ADP
I_BATT
I_SYS
ACAV_IN_NB
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Charger
LA-C631P, C641P
Rev 1.0
Thursday, September 24, 2015
Sheet 51 of 60
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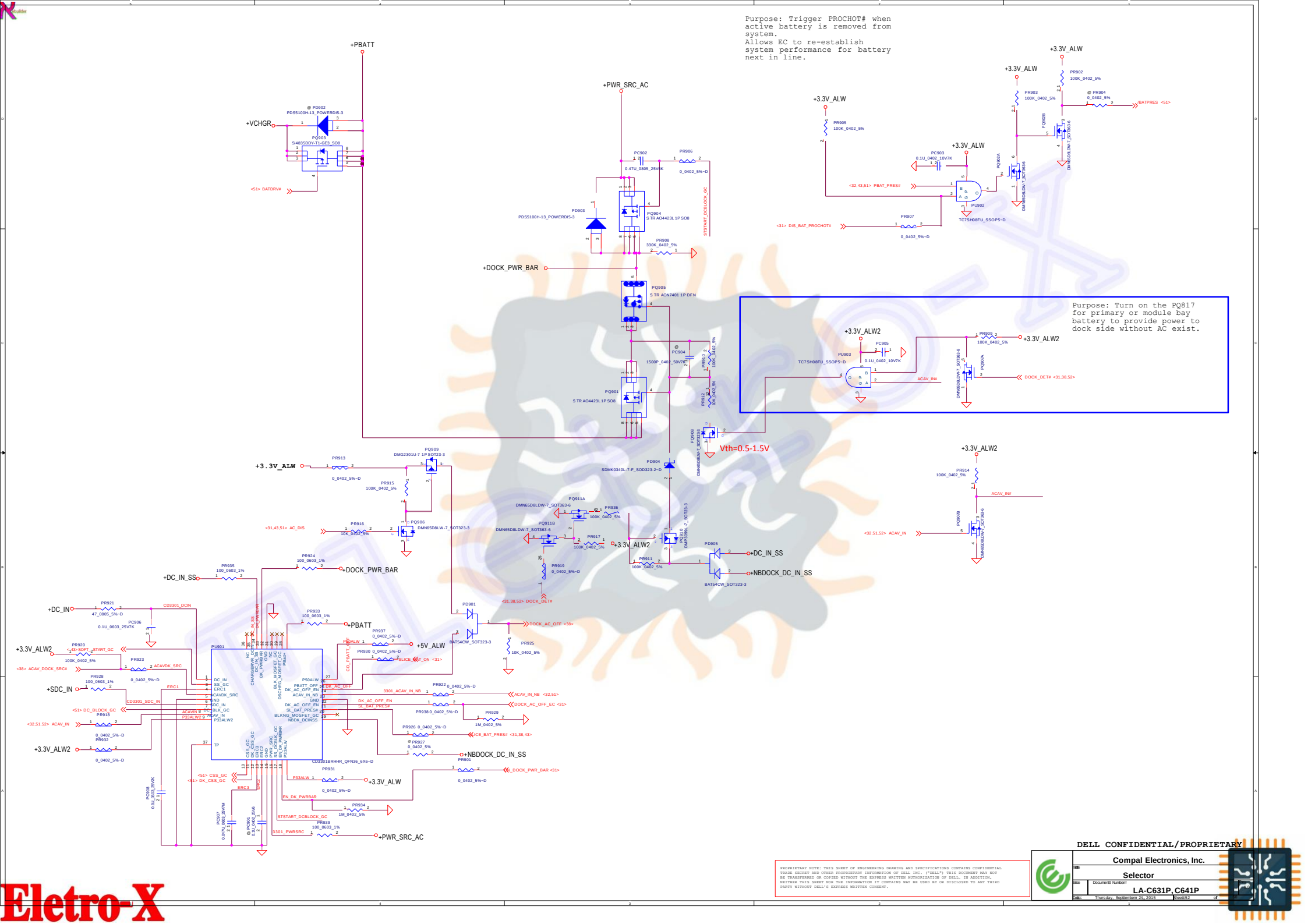
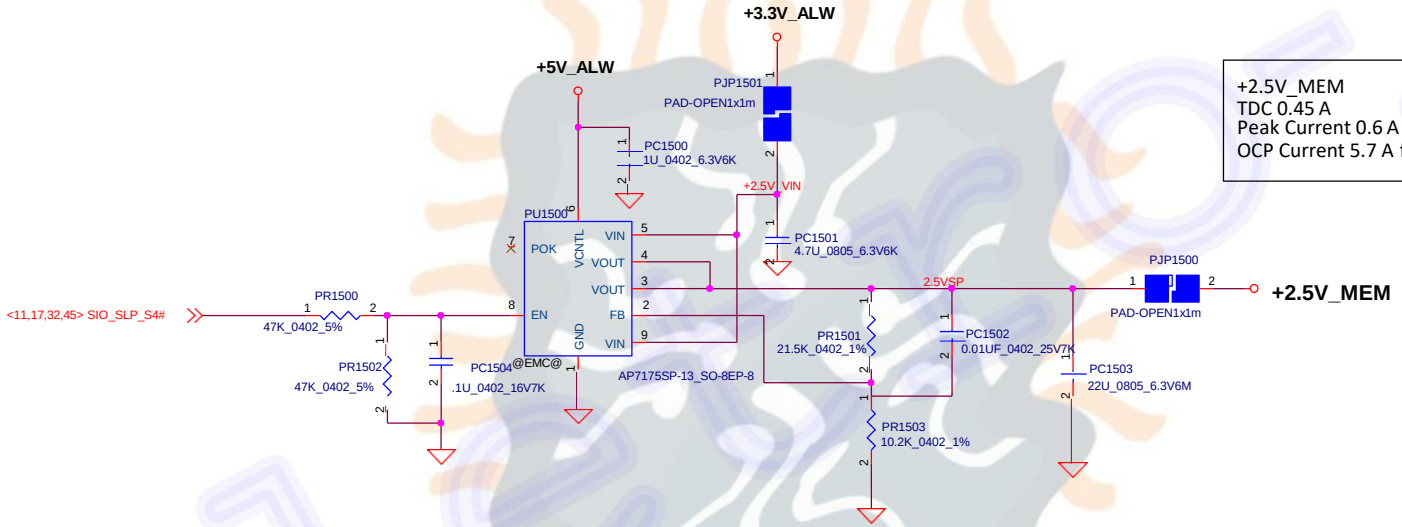
Eletro-X


Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.
Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.
Vth=0.5-1.5V
+PBATT
+VCHGR
+PWR_SRC_AC
+DOCK_PWR_BAR
+3.3V_ALW
+3.3V_ALW2
+5V_ALW
+DC_IN
+DC_IN_SS
+SDC_IN
+NBDOCK_DC_IN_SS
+PWR_SRC_AC
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
Selector
LA-C631P, C641P
Thursday, September 24, 2015
Eletro-X



+2.5V_MEM
TDC 0.45 A
Peak Current 0.6 A
OCP Current 5.7 A fix by IC

Compal Electronics, Inc.

Title: +2.5V_MEM

Size: | Document Number: LA-C451P | Rev:

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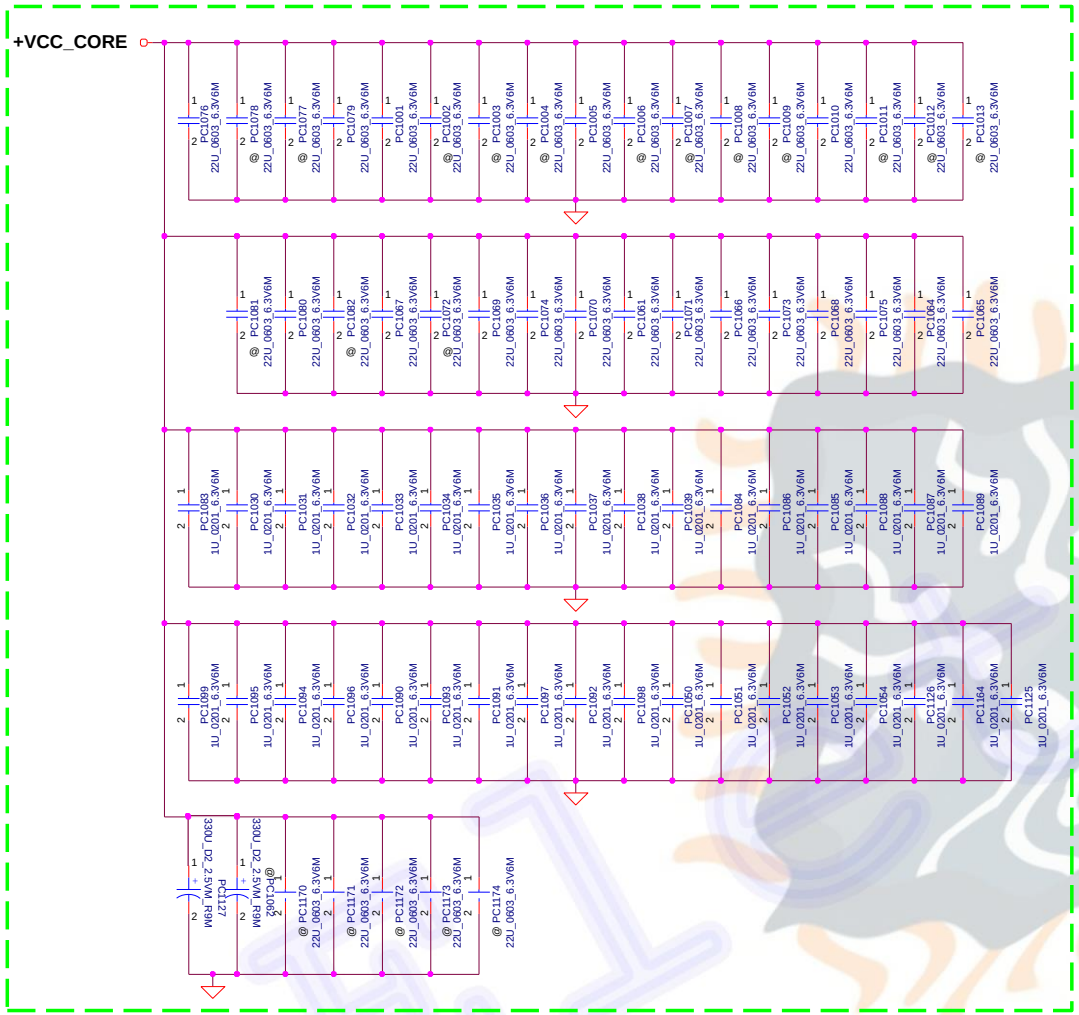
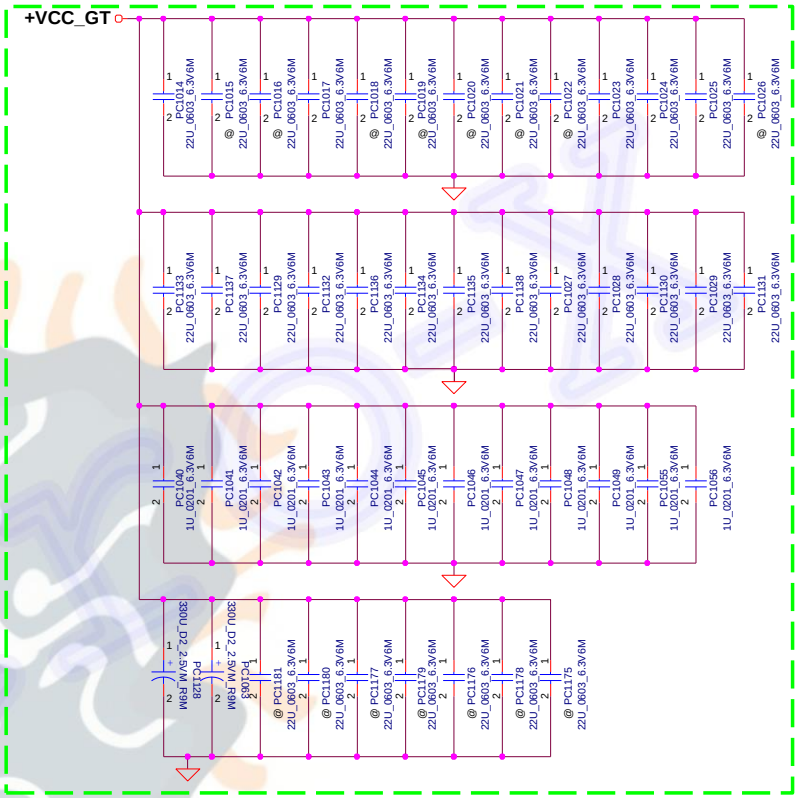
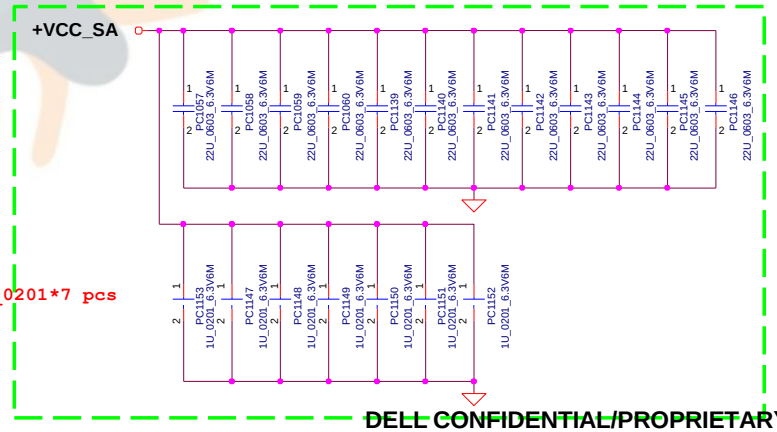
VCC_CORE Place on CPU
Back Side.
22U_0603 * 7 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 13 pcs+330u_D2*1 pcs

VCC_GT Place on CPU
Back Side.
22U_0603 * 11 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 7 pcs +330u_D2*2 pcs







VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size | Document Number: LA-C631P, C641P | Rev: 1.0

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tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCCIOP PRIM_COREP	1/27	Compal	For +1.0VS_VCCIO, +1.0V_PRIM_CORE IC 2nd source	Add PR403, PR406, PR427, PR428	
2	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune IMON	change PR613 to 86.6k change PR651 to 124k change PR629 to 88.7k	
3	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune VR current loop	change PR638 to 374 change PC624 to 0.033uF change PC642 to 0.1uF depop PC646	
4	44	+5V_ALW +3.3V_ALW	1/27	Compal	For 3V5V Pgood	Remove PU101, PR101, PC101 Add PR119, PR120	
5	45	+1.35V_MEN +2.5V_MEM GPU_VRAM	3/3	Compal	For DDR change to DDR3L	Remove +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.2 to +1.35	
6	49	+VCC_CORE +VCC_SA +VCC_GT	3/27	Compal	Fine tune VR control loop	change PR640 to 340 change PC642 to 0.033uF change PC646 to 0.047uF change PR657 to 4.42k change PR628 to 4.42k	
7	45	+1.2V_MEN +2.5V_MEM GPU_VRAM	4/10	Compal	For DDR change to DDR4	Add +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.35 to +1.2	
8	54	+2.5V_MEM +1.8VALWP +1.5VSP	4/20	Compal	Disable LDO pull up when floating enable pin	change PR1500, PR1502, PR509, PR511 to 47k	
9	51	Charger	4/20	Compal	fine tune monitor Psys	change PR822 to 40.2k	
10		+1VS_VCCIOP +1.0V_PRIM_COREP				change to SY80657	
11		CPU MLCC cap cost down			CPU MLCC cap cost down	depop +VCC_CORE, 22U*15,330U*1 +VCC_GT, 22U*8	

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Compal Electronics, Inc.

Title: PWR P.I.R(1/1)

Size | Document Number: LA-C631P, C641P

Date: Thursday, September 24, 2015 | Sheet 56 of 60

tfersion Change List (P. I. R. List)

Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
1	8/22/27/ 30/40/42	Material	2015/01/05	COMPAL	Material EOL	QA2, QA3, QC2, QE2, QL1, QL2, QN1, QV3, QZ3 and QZ7 from SB00000DH00 change to SB00000ZU00	0.2(X01)
2	32	MEC5085	2015/01/05	DELL	For Next Gen EC debug	Add Re305 and RE306 reserve UART0_TXD path	0.2(X01)
3	33	USH & TPM	2015/01/12	COMPAL	system will shut down when insert FP.	change USH conn pin define, and add RZ85, RZ86, DZ7, reserve RZ84, RZ87	0.2(X01)
4	32	MEC5085	2015/01/12	COMPAL	change BID to X01.	change RE79 to 130K ohm.	0.2(X01)
5	9	CPU (4/14)	2015/01/12	COMPAL	add UART port 2 for USB debug.	add net name "LPSS_UART2_TXD", "LPSS_UART2_RXD", and add RC330, RC331 and JUART1 CON	0.2(X01)
6	13	CPU (8/14)	2015/01/12	INTEL	Follow 546765_546765_2014WW52_Skylake_ MOW_Rev_1_0	reserve CC222 and RC313.	0.2(X01)
7	8	CPU (3/14)	2015/01/12	INTEL	support DCI.	add RC327 and reserve RC326, QC3	0.2(X01)
8	32	MEC5085	2015/01/12	COMPAL	For Power down sequence.	add UE3, UE4, RE304,RE308.	0.2(X01)
9	11	CPU (6/14)	2015/01/12	COMPAL	For PLTRST glitch issue.	1.UC7.5 change from +3.3V_RUN to +3.3V_ALW_PCH 2.Pop RC325,depop RC60.	0.2(X01)
10	21	DDR4	2015/01/12	COMPAL	DIMM select error cause can't recognize DIMM2.	Stuff RD70, RD72 and no stuff RD69, RD73.	0.2(X01)
11	27	Transformer	2015/01/12	COMPAL	ME height limit	TL1 changed from SP050006F00 to SP050006Y00	0.2(X01)
12	11	Crystal	2015/01/12	TXC	Material EOS	YC2 changed from SJ10000LD00 to SJ10000LV00	0.2(X01)
13	22	HDMI CONN	2015/01/20	COMPAL	For HDMI EMI solution.	add RV647 ~ RV658 path and depop commom-chock	0.2(X01)
14	26	LCD	2015/01/20	COMPAL	BOM changed	UV24 from SA00006EE00 to SA00006Y800	0.2(X01)
15	32	EC	2015/01/20	COMPAL	BOM changed	QE3/QE4/QE5/QE6/QE7 from SB000008P00 to SB000013V00	0.2(X01)
16	32	EC	2015/01/20	COMPAL	BOM changed	UD1 and UE4 from SA00005U600 to SA00007UR00	0.2(X01)
17	33	TPM	2015/01/20	COMPAL	TPM issue	1. Reserve10K ohm (RZ90) and Pull-up to +3.3V_RUN on UZ12 pin 29. 2. change VSB power (UZ12.1) to +3.3V_ALW_PCH. 3. added QZ8 and RZ109 between pin3/pin20 to control LPM 4. reserve RZ110 and de-pop. 5. Reserve +3.3V_RUN on UZ12 pin 8 (add RZ88, RZ89) 6. change RZ109 pin 1to +3.3V_M_TPM add QZ9, RZ111	0.2(X01)
18	9	CPU (4/14)	2015/01/20	COMPAL	Non-Dock config	Reserve RH359 pull-down for non-dock config	0.2(X01)
19	32	EC	2015/01/20	COMPAL	Power sequence fail	Depop RE280 and RE304 then pop RE292 and UE3	0.2(X01)
20	18	CPU (13/14)	2015/02/04	COMPAL	KB boss and stand off interferen ce	Removed RC304/RC305/RC306/CC205/CC207/CC265	0.3(X02)
21	10	CPU (5/14)	2015/02/04	INTEL	MOW update	Add RC337 connect to GND and RC338 1K pull down	0.3(X02)
22	12	CPU (7/14)	2015/02/04	INTEL	MOW update	Add RC328 XDP_JTAGX need connect to CPU_XDP_TCLK for DCI Changed	0.3(X02)
23	8	CPU (3/14)	2015/02/04	INTEL	MOW update	RC317 from 4.7k to 150k and reserved SIO_SLP_SUS# on RC34 0	0.3(X02)
24	20,21	DDR4	2015/02/04	INTEL	Follow 546765_546765_2015WW02_Sk ylake _MOW_Rev_1_0	No stuff CD6, CD35.	0.3(X02)

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25	33	USH & TPM	2015/03/02	Nuvoton	1. for allow further reducing power in TPM 2.0 F/W,when system is in S3/4/5 and main power is off. 2. for support modern standby.	1.reserve RZ90 2.reserve RZ112. 3.Depop RZ88 and pop RZ89, pop RZ112	0.3(X02)
26	11,27	CPU (6/14)	2015/03/02	COMPAL	Solve auto power on issue.	De-pop RL70 and pop RC323.	0.3(X02)
27	32	MEC5085	2015/03/02	COMPAL	Solve power down sequence fail.	De-pop RE308.	0.3(X02)
28	32	MEC5085	2015/03/02	COMPAL	change BID to X02.	change RE79 to 33K ohm.	0.3(X02)
29	26	eDP CONN & TS	2015/03/02	DELL	Customer request.	add 6 pin IR Conn.	0.3(X02)
30	40	PAD, LED	2015/03/02	COMPAL	ME design change.	change H6 from 4mm to 3mm.	0.3(X02)
31	11/32	Crystal	2015/03/02	COMPAL	X'tal EA measurement.	change CC23 and CC26 from 18pf to 12pf	0.3(X02)
32	8	CPU (3/14)	2015/03/02	Intel	Intel MOW_2015WW06:Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update	de-pop RC30, RC316	0.3(X02)
33	8	CPU (3/14)	2015/03/02	COMPAL	Follow CRB setting	RC23 changed from 8.2K to 2.2K	0.3(X02)
34	33	TPM	2015/03/02	COMPAL	support modern standby	Add RZ112 connect to SIO_SLP_S0# with TPM	0.3(X02)
35	32	EC	2015/03/02	COMPAL	Option DDR3L and DDR4	Add GPP_D9(DIMM_TYPE), RC342 and RC341 that selected DDR3L and DDR4.	0.3(X02)
36	32	EC	2015/03/02	COMPAL	Follow Intel power sequence	Pop RE292 and depop RE280	0.3(X02)
37	8	CPU (3/14)	2015/03/02	COMPAL	RF request	Pop CC3/CC4/CC5/CC6 from 22p to 27p	0.3(X02)
38	33	TPM	2015/03/02	Nunoton	TPM detected sequence	Add RZ113 100 ohm	0.3(X02)
39	11	CPU (6/14)	2015/03/02	COMPAL	Deep S3 leakage	VRALERT# changed power rail from +3.3V_ALW to +3.3V_ALW_PCH	0.3(X02)
40	27	LAN	2015/03/02	COMPAL	IEEE EA measurement.	change LL2 ~ LL9 to 2.2 ohm Res (RL71~RL78).	0.3(X02)
41	9	CPU (4/14)	2015/04/02	COMPAL	IR Function	1. add IR_CAM_DET# on JIR1 pin 1. 2. add IR_CAM_DET# on UC1.AW7, and PU 100K(RC346) to +3.3V_RUN	0.4(X03)
42	31/33	EC/USH	2015/04/02	Broadcom	Vender recommend	1.Reserve RZ114/RZ115 on JUSH1 pin 21 2.add USH_RST# on UE1.A62	0.4(X03)
43	12	CPU (7/14)	2015/04/02	COMPAL	SIO_EXT_SMI# to wake up system when non-deep S3	Add RC236 SIO_EXT_SMI# change power to +3.3V_ALWS_PCH	0.4(X03)
44	29	NGFF Card	2015/04/02	COMPAL	ME request	Change JSIM1 conn to T-SOL_5-991503004000-6	0.4(X03)
45	32	MEC5085	2015/04/02	COMPAL	change BID to X03	change RE79 to 1K ohm.	0.4(X03)
46	9	CPU (4/14)	2015/04/02	COMPAL	for DIMM type option	Pop RC342 and de-pop RC341	0.4(X03)
47	40	PAD, LED	2015/04/02	COMPAL	ME request	Add H9 and H10 for different SIM CON	0.4(X03)
48	29	NGFF	2015/04/02	COMPAL	SIM detect	Add RI31 connecting with JSIM1.9 and NGFF2.58	0.4(X03)

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49	39	KB	2015/04/20	ALPS	For new U1 TP module	Add RZ116 and RZ117 PU on I2C._1_SDA_R/I2C_1_SCL_R	0.4(X03)
50	31	5048	2015/04/20	COMPAL	PC common EC code issue need reserved PU	Add AR_SMBUS_ALERT# 10K(RE309) PU on ECE5048 pin58 GPIOF2	0.4(X03)
51	31	All	2015/04/20	COMPAL	Changed 0 ohm short-pad	R274,RA35,RA36,RA37,RC143,RC169,RC170,RC171,RC172,RC173,RC211,RC214, RC228,RC229,RC230,RC231,RC235,RC290,RC295,RC296,RC299,RC300,RC301,RC302, RC303,RC307,RC308,RC309,RC310,RC325,RC327,RC328,RC337,RC37,RD29,RD60, RD65,RD66,RD67,RD68,RD70,RD72,RD74,RE290,RE305,RI15,RI16,RI17 RI18,RI19,RI20,RI21,RI22,RI23,RI24,RI25,RI26,RI27,RI28,RI29,RI30,RI31 RL34,RL7,RN99,RR17,RR18,RR21,RR22,RR23,RZ22,RZ23,RZ56,RZ70,RZ85, RZ86	0.4(X03)
	52	8	CPU(3/14)	2015/04/20	COMPAL	SMBUS LAN backdrive	Add RC347 and RC348 PU to +3.3V_ALW_PCH
	53	11	CPU(6/14)	2015/05/20	COMPAL	Crystal EA -R issue	Changed YC2-CL 9pf from 12pf and cc23/cc26 changed
57	31	5048	2015/05/20	COMPAL	For Type-C function	1. Add 5048 GPIO(PROCHOT_GATE) and reserve RE311 pull high 2. Add 5048(PD_ACE_DET#) for AR config and pull high on RE310	0.5(X04)
58	32	MEC5085	2015/05/20	COMPAL	change BID to X04	change RE79 to 8.2K ohm.	0.5(X04)
59	54	CPU(13/14)	2015/05/27	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	1.Add RC349 and CC303 on VCCHDA 2.Add RC350 and CC304 on VCCAPLL_1P0	0.5(X04)
60	36/37	USB3.0	2015/05/27	COMPAL	ESD request	1.Add CI33 0.1U cap to GND on USB_OC0# 2.Add CI34 0.1U cap to GND on USB_OC1# 3.Add CI35 0.1U cap to GND on USB_OC2#	0.5(X04)
61	26	eDP	2015/06/27	COMPAL	Material shortage	Changed DV1, DV2 and DV3 from SCS00003800 to SCS00006400	0.6(X05)
62	33	TPM	2015/06/27	COMPAL	Change TPM FW to 1.2 version	Changed UZ12 from SA000082D00 to SA00008EL20	0.6(X05)
63	32	KBC	2015/06/27	COMPAL	WinPE Global reset shutdown issue	Add QE11 prevent +1.0V_VCCST timing down before +1.0V_VCCIO	0.6(X05)
64	32	KBC	2015/06/27	COMPAL	Follow intel power sequence	Add UE5 AND Gate control Run_on timing and depop RE292	0.6(X05)
65	11	CPU(6/14)	2015/06/27	COMPAL	Crystal EA	Changed CC21 and CC22 from 22p to 15p	0.6(X05)
66	33	USH	2015/06/27	COMPAL	TPM1.2 deep S3 resume issue	UZ12.1 changed power rail from +3.3V_ALW_PCH to +3.3V_ALW	0.6(X05)
67	24	DP HUB	2015/07/20	COMPAL	For DP hub display flicker issue	1.Add UV29,CV617,CV618,CV619,RV659,RV650,RV661 2.Depop UV28,PJP33,CV615,CV616	0.6(X05)
68	36	HW	2015/07/20	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	0.6(X05)
69	32	MEC5085	2015/07/20	COMPAL	change BID to X05	change RE79 to 4.3K ohm.	0.6(X05)

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Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
70	41	CPU(12/14)	2015/07/31	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control to +VCCPLL_OC power rail	0.6(X05)
71	18	CPU(13/14)	2015/07/31	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	Change RC349 and RC350 to LC1 and LC2	0.6(X05)
72	36	USB	2015/08/12	COMPAL	Low battery shut down issue	Depop CI32 and then pop CI14	0.6(X05)
73	32	5085	2015/08/12	COMPAL	DC mode CPU trubo issue	Reserved RE313 pull down path on I_SYS	0.6(X05)
7434	PCIE	2015/08/12	COMPAL	M.2 SATA iEMT 75		Pop RN50 change to level2	0.6(X05)
	11	CPU(6/14)	2015/08/12	COMPAL	RTC delay	YC2 changed to 10ppm(SJ10000Q800) and CC23/CC26 changed to 5pf	0.6(X05)
76	24	HUB	2015/09/12	COMPAL	Display no function	RV662 chnanged to 0 ohm from 1 ohm.	1.0(A00)
77	ALL	All	2015/09/12	COMPAL	Changed 0 ohm short-pad	RC41,RC289,RZ89,RZ112,RZ64,RC221,RZ118,RV662	1.0(A00)
78	12	CPU(7/14)	2015/09/12	COMPAL	Service mode switch	Depop RC222 and SW1 and then short RC221	1.0(A00)
79	32	5085	2015/09/12	COMPAL	syn-up with power material issue	1.Change SC600001600 to SCA00000T00(DI2,DI3,DI5,DV4) 2.Change SB000013V00 to SB00000Z500(QE3,QE4,QE5,QE6,QE7)	1.0(A00)
80	32	MEC5085	2015/09/12	COMPAL	change BID to A00	change RE79 to 1K ohm.	1.0(A00)
81	22	HDMI	2015/09/18	COMPAL	DFX request	Delete LV3/LV6/LV9/LV12 co-lay footprint	1.0(A00)
82	12/14	XDP	2015/09/20	COMPAL	Follow PDG2.0	Changed RC82 and RC135 to 100 from 51.	1.0(A00)

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