X407UBR SCHEMATIC

Revision 1.0

NON CONNECTED STANDBY

（UAR：UMA）(45W) (Power BOM)
（UBR：DGPU = Nvidia N16V-GMR1, MX110）(65W) (Power BOM)
（UER：DGPU = Nvidia N16S-GTR, MX130）(65W) (Power BOM)

Project Name	X407UA/UV
Title :	LVDS CONNECTOR
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet 47 of 102

SYSTEM PAGE REF.

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	021_CPU_PCH_CGPIO, LPIO, MISC
	022_CPU_PCH_AUDIO,SDIO,SDXC
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	024_CPU_PCH_CLOCK SIGNALS,RTC
	025_CPU_PCH_SYS_POWER
	026_CPU_PCH_POEWR,GND
	027_CPU_PCH_POEWR,GND
	028_PCH-SPI ROM,OTH /DEBUG PORT
	029_Silego_Green_CLK_Gen
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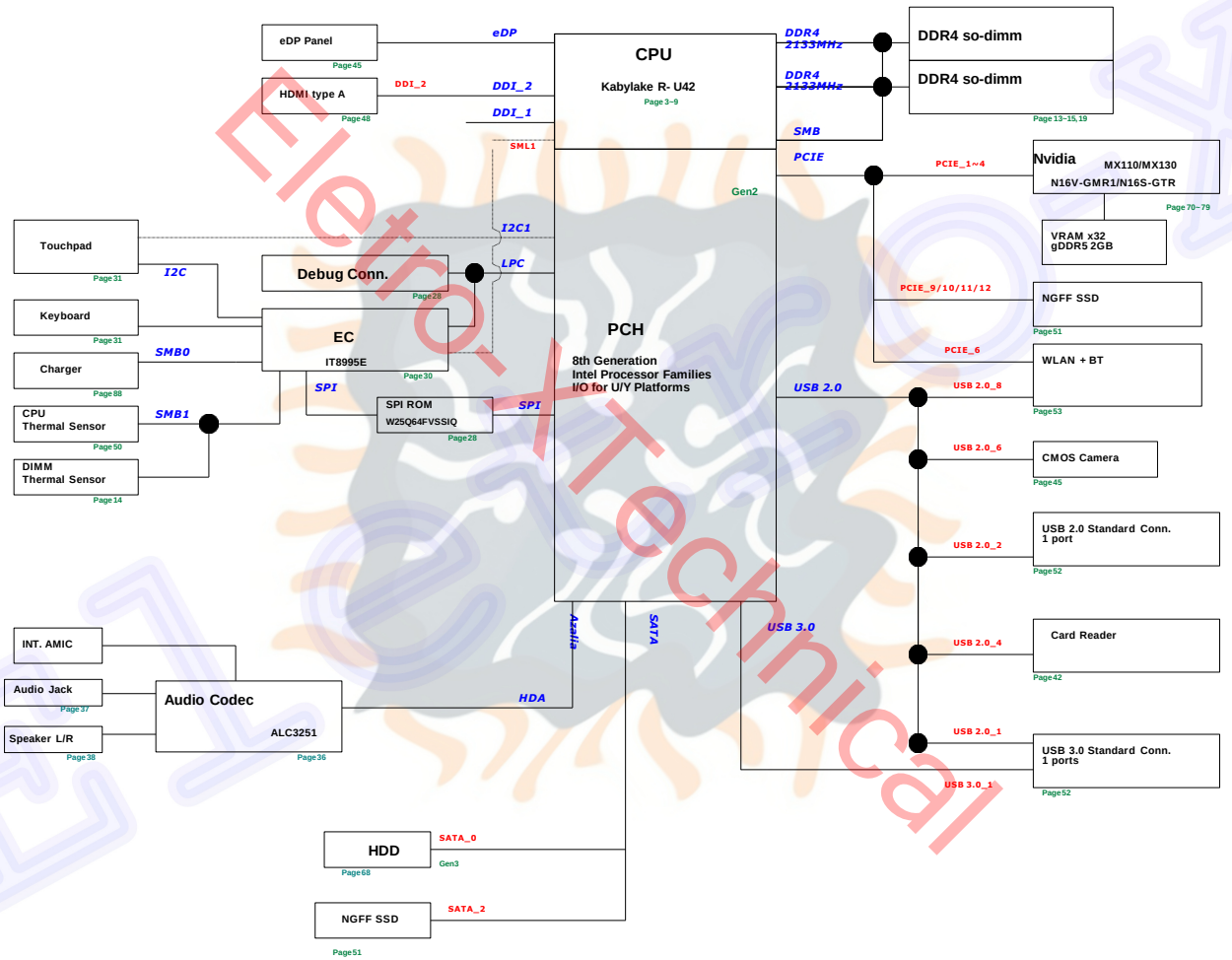
	031_KBC_KB,TP
	032_RST_Reset Circuit
	036_AUD-ALC3251
	037_AUD-HEADPHONE JACK
	038_AUD_SPEAKER
	042_CardReader Connector
	045_eDP Connector
	048_HDMI-type D
	050_FAN & SENSOR
	051_NGFF(KEY-M)_SSD
	052_USB 3.0 + 2.0 CONN
	053_NGFF(KEY-E)_WLAN
	057_DSG_Discharge
	058_PRO_Protect
	059_Power & WIFI & CAP LED&LID
	060_DC_DC & BAT IN
	064_
	065_ME_Conn & Skew Hole
	066_
	067_
	068_HDD COnnector
	069_EMI
	070_VGA_nVIDIA_N16V/S_PCIE
	071_VGA_nVIDIA_N16V/S_FB-IF
	072_VGA_nVIDIA_N16V/S_FB-DDR3
	073_VGA_nVIDIA_N16V/S_VDD
	074_VGA_nVIDIA_N16V/S_DISPLAY
	075_VGA_nVIDIA_N16V/S_ROM,XTAL
	076_VGA_nVIDIA_N16V/S_GPIO
	077_VGA_nVIDIA_N16V/S_POWER

080_PW_IMVP8 (1) (RT3601BCGQW)
081_PW_IMVP8 (2) (RT3601BCGQW)
083_PW_+1.0VSUS / +1.8VSUS
084_PW_+1.2VS
086_PW_1.35V/+0.675VS (UP9011Q)
087_PW_+3VADSW/+5VSUS (RT8249C)
088_PW_LOAD SWITCH
089.PW_CHARGER(BQ24780)
090_PW_PROTECTION
091_PW_DGPU_2PHASE(RT8815A)

BLOCK DIAGRAM



Power

+VCCGT
+VCCCORE
+VCCST
+VCCSA
Page 80 &81

+1.0VSUS / +1.8VSUS
Page 83

+0.95VSG
+VCCPRIM_CORE
Page 84

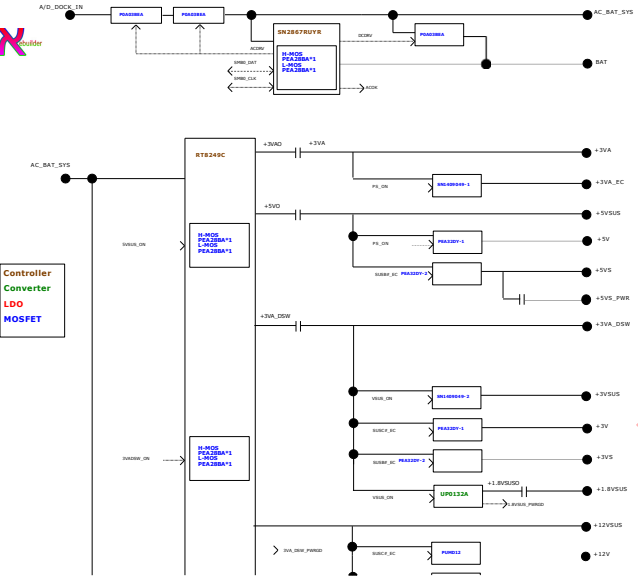
+1.2V / +VTT / +2.5V
Page 86

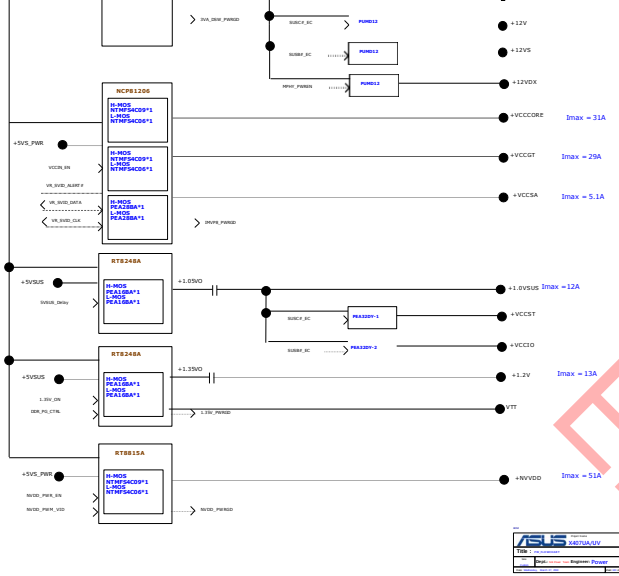
+3VADSW/+5VSUS
Page 87

Load Switch
Page 88

Charger
Page 89

+VDDC
Page 91





X541UV/UA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode

1 +3VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 5VSUS_ON 3VA_DSW_ON

+3VA_DSW/+5VSUS/+12VSUS

(PCH to EC) 4 ME_SusPwrDnAck_R

(power to EC) 5 3VSUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

(EC to power) ME_SLP_M_EC#

(EC to power) 13 SUSC_EC#

+1.2V/+2.5V/+3V/+12V/+VCCST

(EC to power) 14 SUSB_EC#

+1.8VS/+3VS/+5VS/+12VS
+VCCIO/+VccSTG

VccST/VccPLL

+VCCSA

(power to EC) 15 IMVP8_PWRGD

16 ALL_SYSTEM_PWRGD

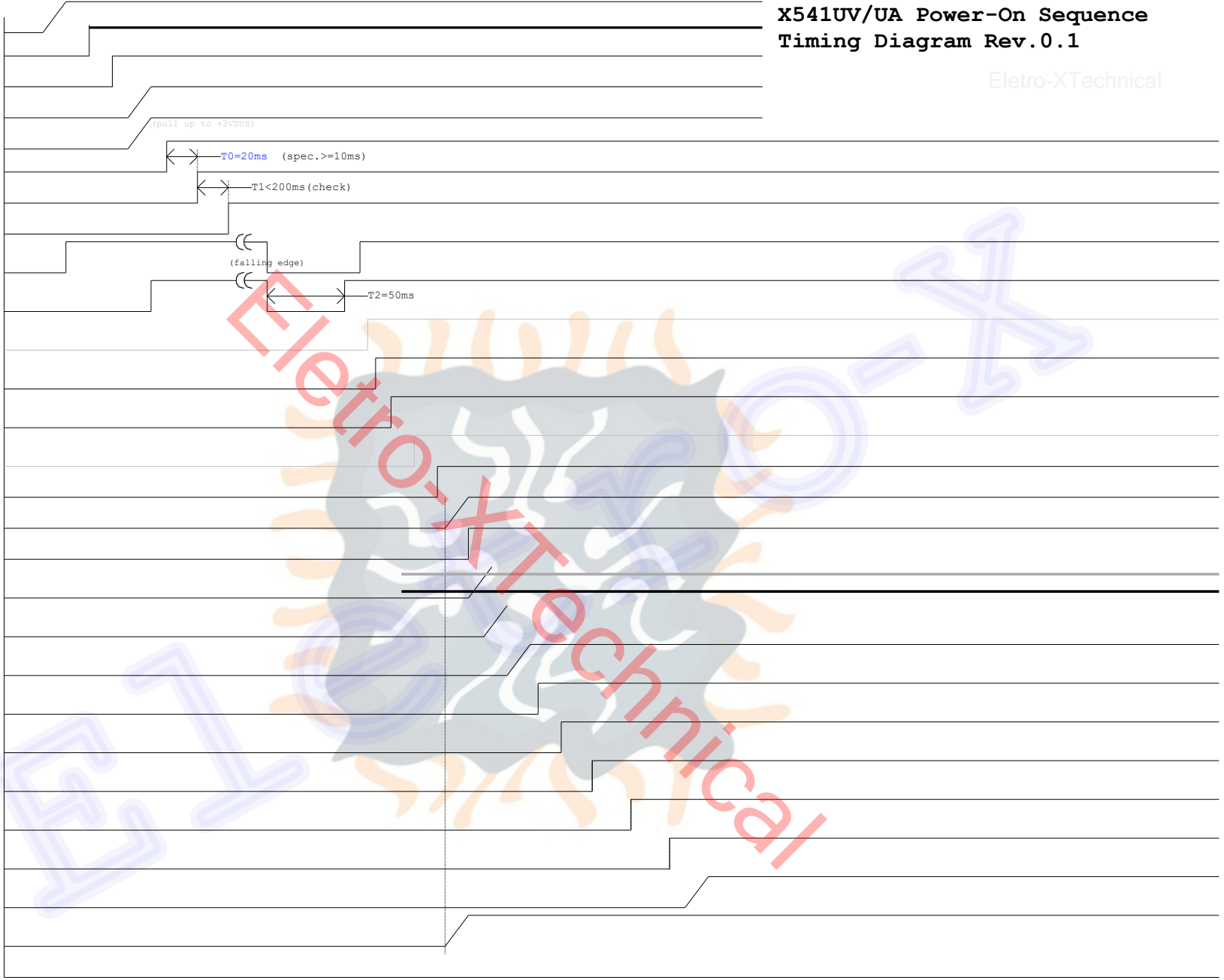
(EC to PCH) 17 PM_PWROK_PCH

(PCH to EC) PCH_SUS_STAT#

(PCH to EC) 18 PLT_RST#

+VCCGT

THERMTRIP#



Eletro-X

BOM

ASUS Project Name X407UA/UV

Title : Power On Timing

Size C | Dept.: ASUSTeK COMPUTER INC. | Engineer: Brian Chen

X541UV/UA Power-On Sequence Timing Diagram Rev.0.1

DC-IN Mode

1 +3VA/+3VA_EC

(to EC) 2 EC_RST#

(EC to power) 3 5VSUS_ON 3VA_DSW_ON

+3VA_DSW/+5VSUS/+12VSUS

(PCH to EC) 4 ME_SusPwrDnAck_R

(power to EC) 5 3VSUS_PWRGD

(EC to PCH) 6 PM_RSMRST#

(EC to PCH) 7 AC_PRESENT

(to EC) 8 PWR_SW#

(EC to PCH) 9 PM_PWRBTN#

(PCH to EC) 10 PM_SLP_A#

(PCH to EC) 11 PM_SUSC#

12 PM_SUSB#/SLP_LAN#

(PCH to EC) (PCH to power)

(EC to power) ME_SLP_M_EC#

(EC to power) 13 SUSC_EC#

+1.2V/+2.5V/+3V/+12V/+VCCST

(EC to power) 14 SUSB_EC#

+1.8VS/+3VS/+5VS/+12VS
+VCCIO/+VccSTG

VccST/VccPLL

+VCCSA

(power to EC) 15 IMVP8_PWRGD

16 ALL_SYSTEM_PWRGD

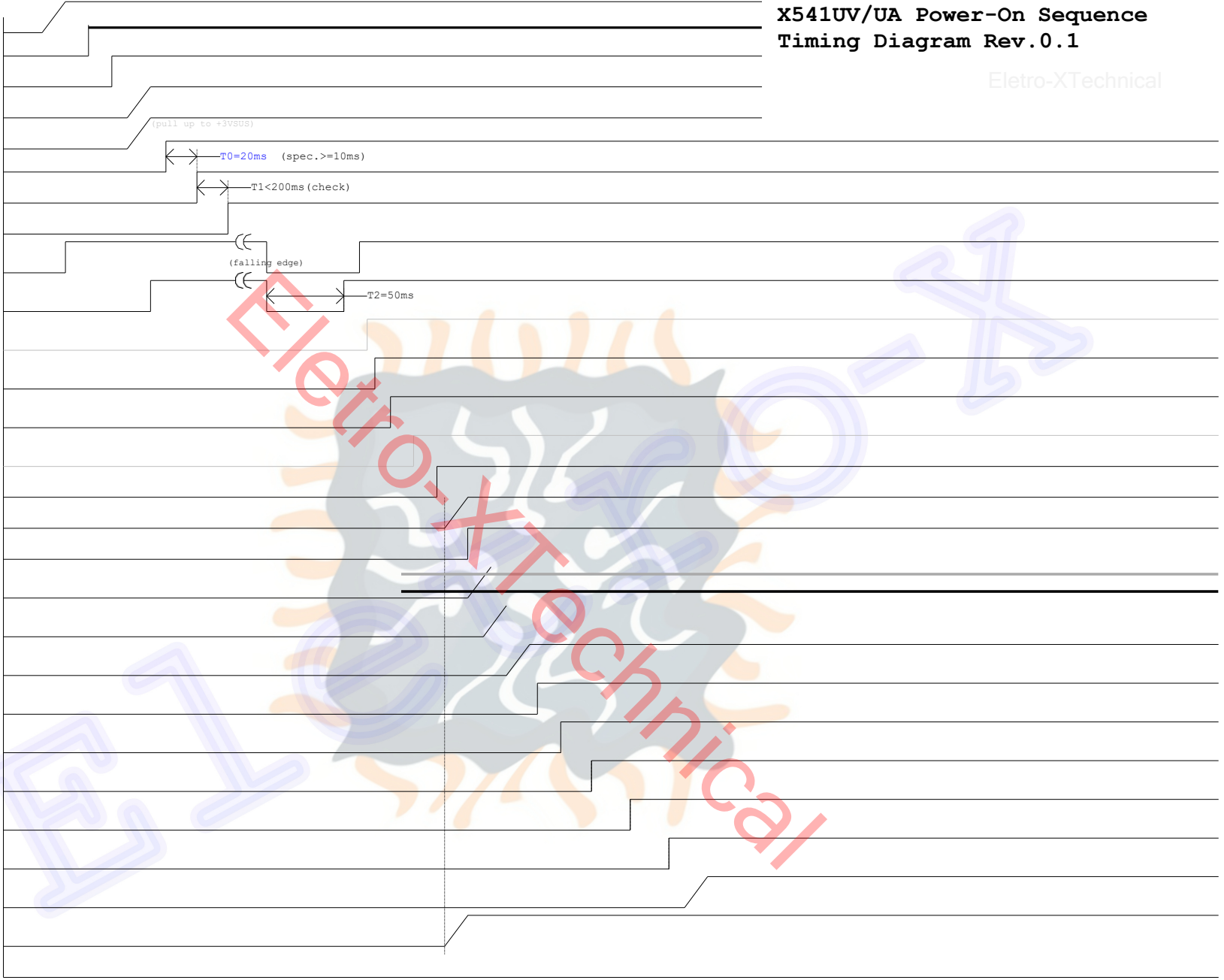
(EC to PCH) 17 PM_PWROK_PCH

(PCH to EC) PCH_SUS_STAT#

(PCH to EC) 18 PLT_RST#

+VCCGT

THERMTRIP#



Eletro-X

BOM

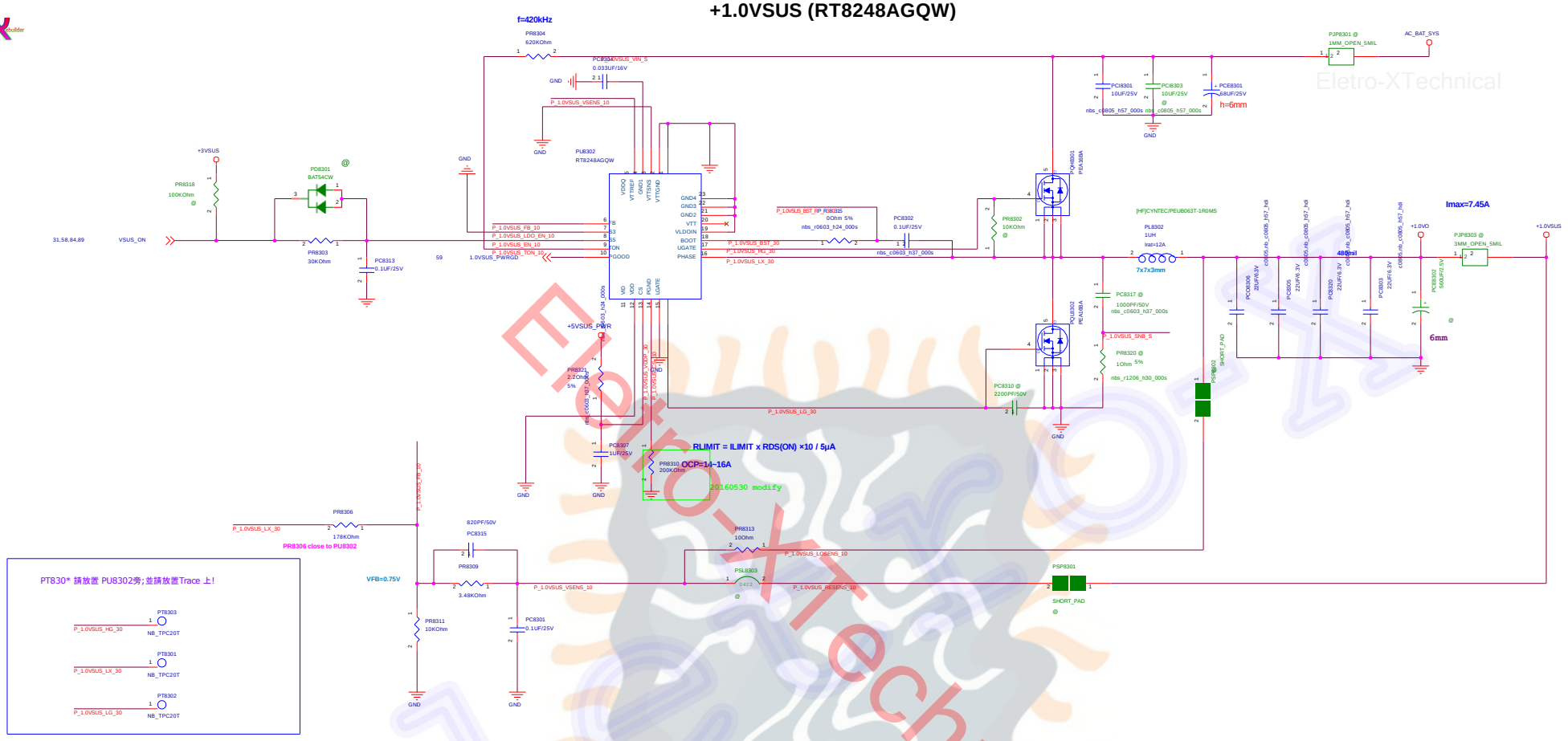
ASUS Project Name X407UA/UV

Title : Power On Timing

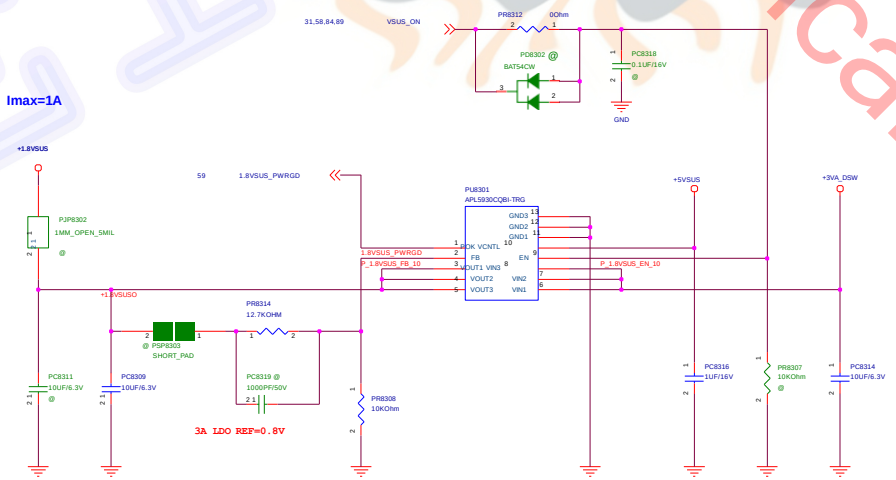
Size C

Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen

+1.0VSUS (RT8248AGQW)

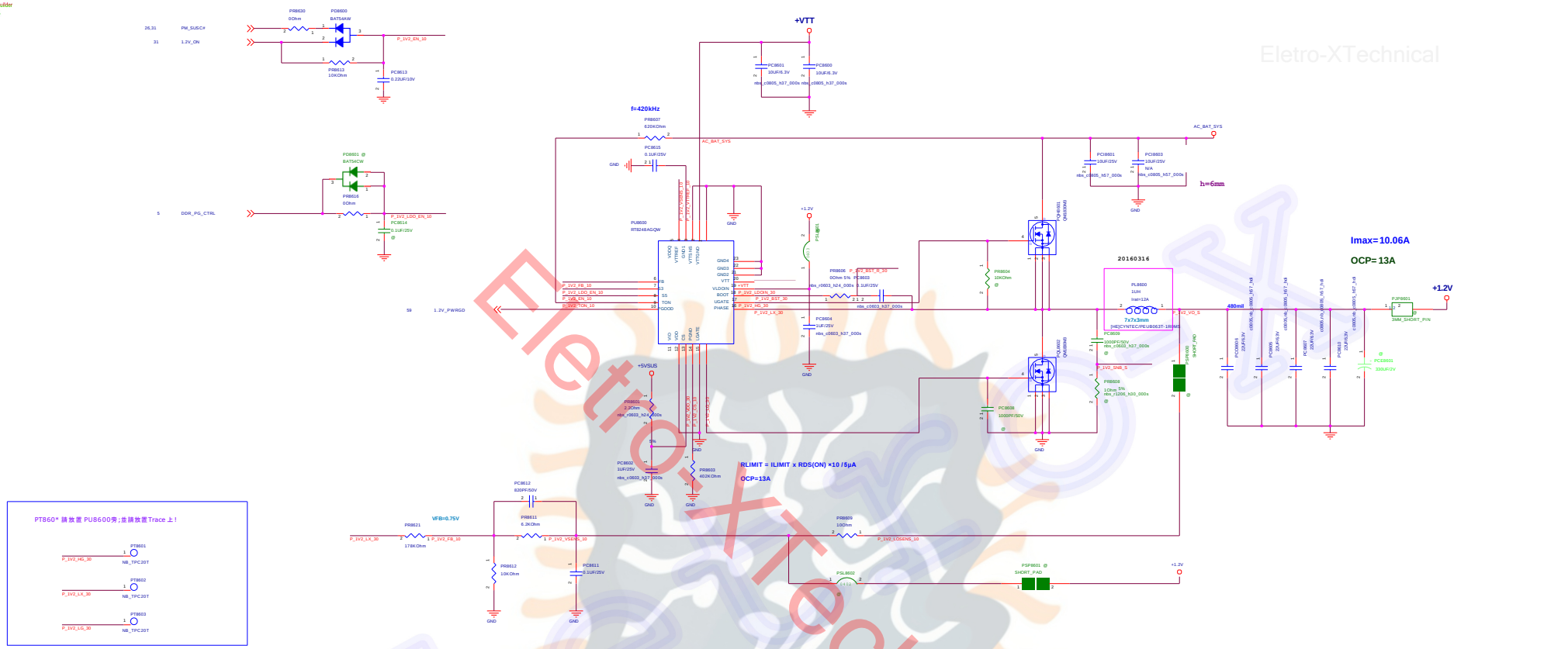


+1.8VSUS [For PCH]

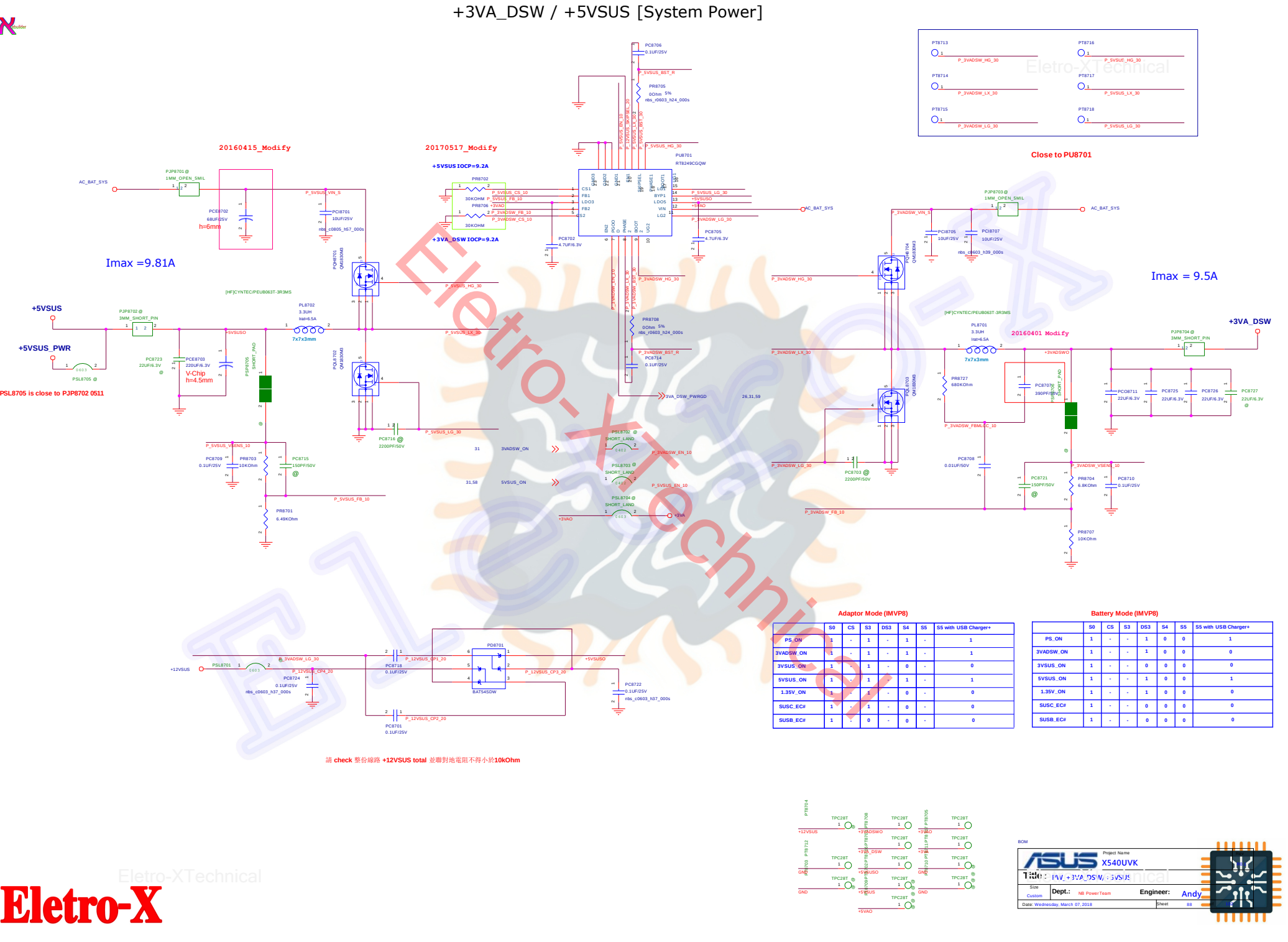


Project Name	X540UVK		Rev.
Title :	PW_+1.0VSUS / +1.8VSUS		
Size C	Dept.: NB Power Team	Engineer: Andy	

+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]



Adaptor Mode (IMVP8)

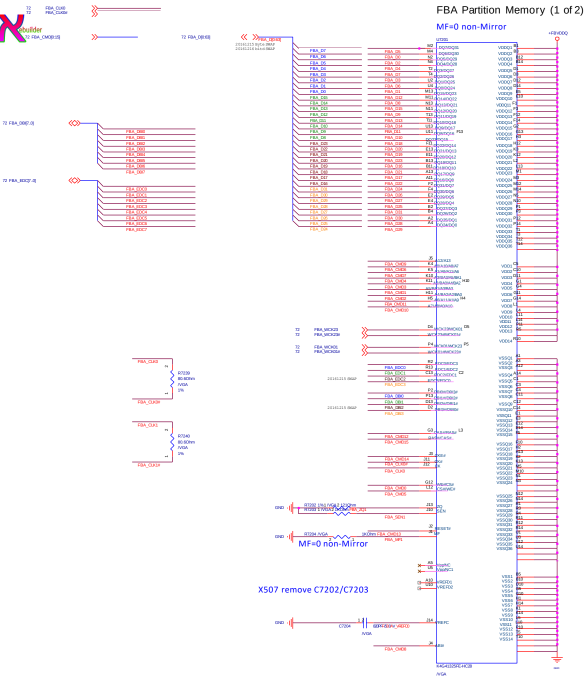
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

BOM

Project Name	X540UVK
Title	+3VA_DSW / +5VSUS
Size	Custom
Dept.	NB Power Team
Engineer	Andy
Date	Wednesday, March 07, 2018
Sheet	88



GDDR5 X32

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	**Channel 0 & 1**		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

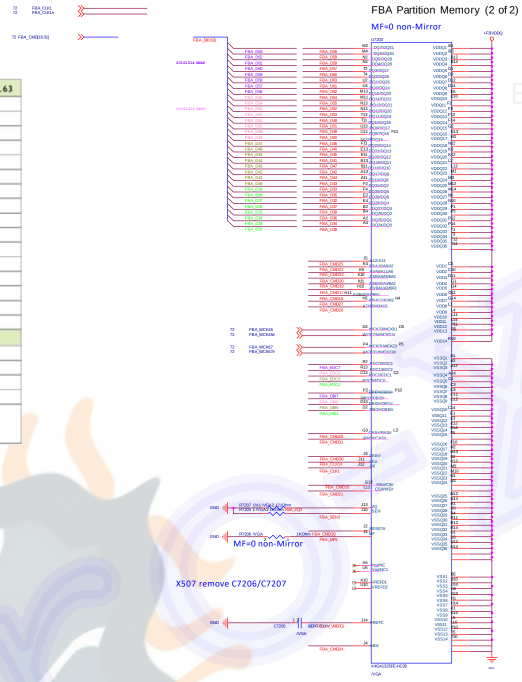


Table 7-14. VREF Configuration

Configuration	Requirement	Notes
×32	Share one Vref-C circuit for two memory parts.	GDDR5 DRAMs have internal VREF for DQ, DBI, EDC (VREF-D). Command, Address VREF (VREF-C) needs to be externally supplied since DRAMs do NOT internally generate VREF for these signals.
×16	Share one VREF-C circuit for four memory parts.	

7.1.12.1 VREF-D

VREF-D pins can be left floating.

7.1.12.2 VREF-C

VREF-C connections for the ×16 mode are shown in Figure 7-8.

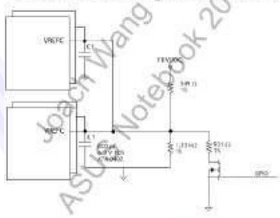
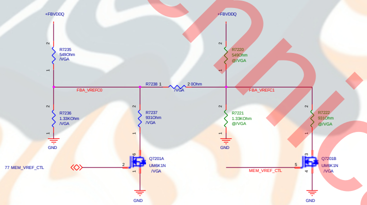
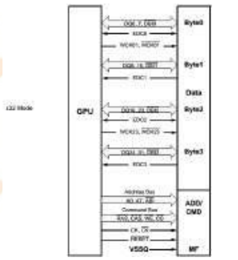
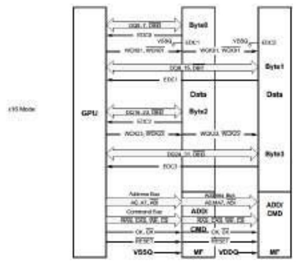


Figure 7-8. VREF-C Connections for ×16 Mode







5.1 GDDR5 SGRAM 170ball BGA Ball-out MF=0

	1	2	3	4	5	10	11	12	13	14
			Byte0					Byte1		
A	VSSQ	DQ1	VSSQ	DQ0	NC	VREFD	DQ8	VSSQ	DQ9	VSSQ
B	VDDQ	DQ3	VDDQ	DQ2	VSS	VSS	DQ10	VDDQ	DQ11	VDDQ
C	VSSQ	EDC0	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	EDC1	VSSQ
D	VDDQ	DBI0	VDDQ	WCK01	WCK01	VSS	VDD	VDDQ	DBI1	VDDQ
E	VSSQ	DQ5	VSSQ	DQ4	VDDQ	VDDQ	DQ12	VSSQ	DQ13	VSSQ
F	VDDQ	DQ7	VDDQ	DQ6	VSSQ	VSSQ	DQ14	VDDQ	DQ15	VDDQ
G	VDD	VDDQ	RAS	VDD	VSS	VSS	VDD	CS	VDDQ	VDD
H	VSS	VSSQ	VDDQ	A10/A0	A9/A1	BA3/A3	BA0/A2	VDDQ	VSSQ	VSS
J	MF	RESET	CKE	ABI	A12/A13	SEN	CK	CK	ZQ	VREFC
K	VSS	VSSQ	VDDQ	A8/A7	A11/A6	BA1/A5	BA2/A4	VDDQ	VSSQ	VSS
L	VDD	VDDQ	CAS	VDD	VSS	VSS	VDD	WE	VDDQ	VDD
M	VDDQ	DQ31	VDDQ	DQ30	VSSQ	VSSQ	DQ22	VDDQ	DQ23	VDDQ
N	VSSQ	DQ29	VSSQ	DQ28	VDDQ	VDDQ	DQ20	VSSQ	DQ21	VSSQ
P	VDDQ	DBI3	VDDQ	WCK23	WCK23	VSS	VDD	VDDQ	DBI2	VDDQ
R	VSSQ	EDC3	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	EDC2	VSSQ
T	VDDQ	DQ27	VDDQ	DQ26	VSS	VSS	DQ18	VDDQ	DQ19	VDDQ
U	VSSQ	DQ25	VSSQ	DQ24	NC	VREFD	DQ16	VSSQ	DQ17	VSSQ

5.2 GDDR5 SGRAM 170ball BGA Ball-out MF=1

	1	2	3	4	5	10	11	12	13	14
			Byte3					Byte2		
A	VSSQ	DQ25	VSSQ	DQ24	NC	VREFD	DQ16	VSSQ	DQ17	VSSQ
B	VDDQ	DQ27	VDDQ	DQ26	VSS	VSS	DQ18	VDDQ	DQ19	VDDQ
C	VSSQ	EDC3	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	EDC2	VSSQ
D	VDDQ	DBI3	VDDQ	WCK23	WCK23	VSS	VDD	VDDQ	DBI2	VDDQ
E	VSSQ	DQ29	VSSQ	DQ28	VDDQ	VDDQ	DQ20	VSSQ	DQ21	VSSQ
F	VDDQ	DQ31	VDDQ	DQ30	VSSQ	VSSQ	DQ22	VDDQ	DQ23	VDDQ
G	VDD	VDDQ	CAS	VDD	VSS	VSS	VDD	WE	VDDQ	VDD
H	VSS	VSSQ	VDDQ	A8/A7	A11/A6	BA1/A5	BA2/A4	VDDQ	VSSQ	VSS
J	MF	RESET	CKE	ABI	A12/A13	SEN	CK	CK	ZQ	VREFC
K	VSS	VSSQ	VDDQ	A10/A0	A9/A1	BA3/A3	BA0/A2	VDDQ	VSSQ	VSS
L	VDD	VDDQ	RAS	VDD	VSS	VSS	VDD	CS	VDDQ	VDD
M	VDDQ	DQ7	VDDQ	DQ6	VSSQ	VSSQ	DQ14	VDDQ	DQ15	VDDQ
N	VSSQ	DQ5	VSSQ	DQ4	VDDQ	VDDQ	DQ12	VSSQ	DQ13	VSSQ
P	VDDQ	DBI0	VDDQ	WCK01	WCK01	VSS	VDD	VDDQ	DBI1	VDDQ
R	VSSQ	EDC0	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	EDC1	VSSQ
T	VDDQ	DQ3	VDDQ	DQ2	VSS	VSS	DQ10	VDDQ	DQ11	VDDQ
U	VSSQ	DQ1	VSSQ	DQ0	NC	VREFD	DQ8	VSSQ	DQ9	VSSQ

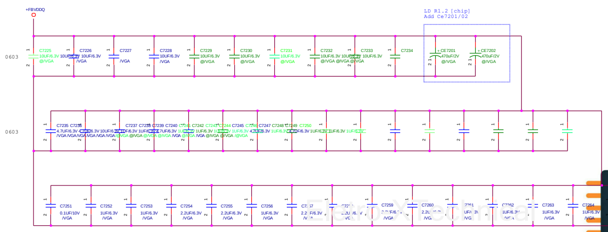
Signal Assignment in MF=0 and MF=1

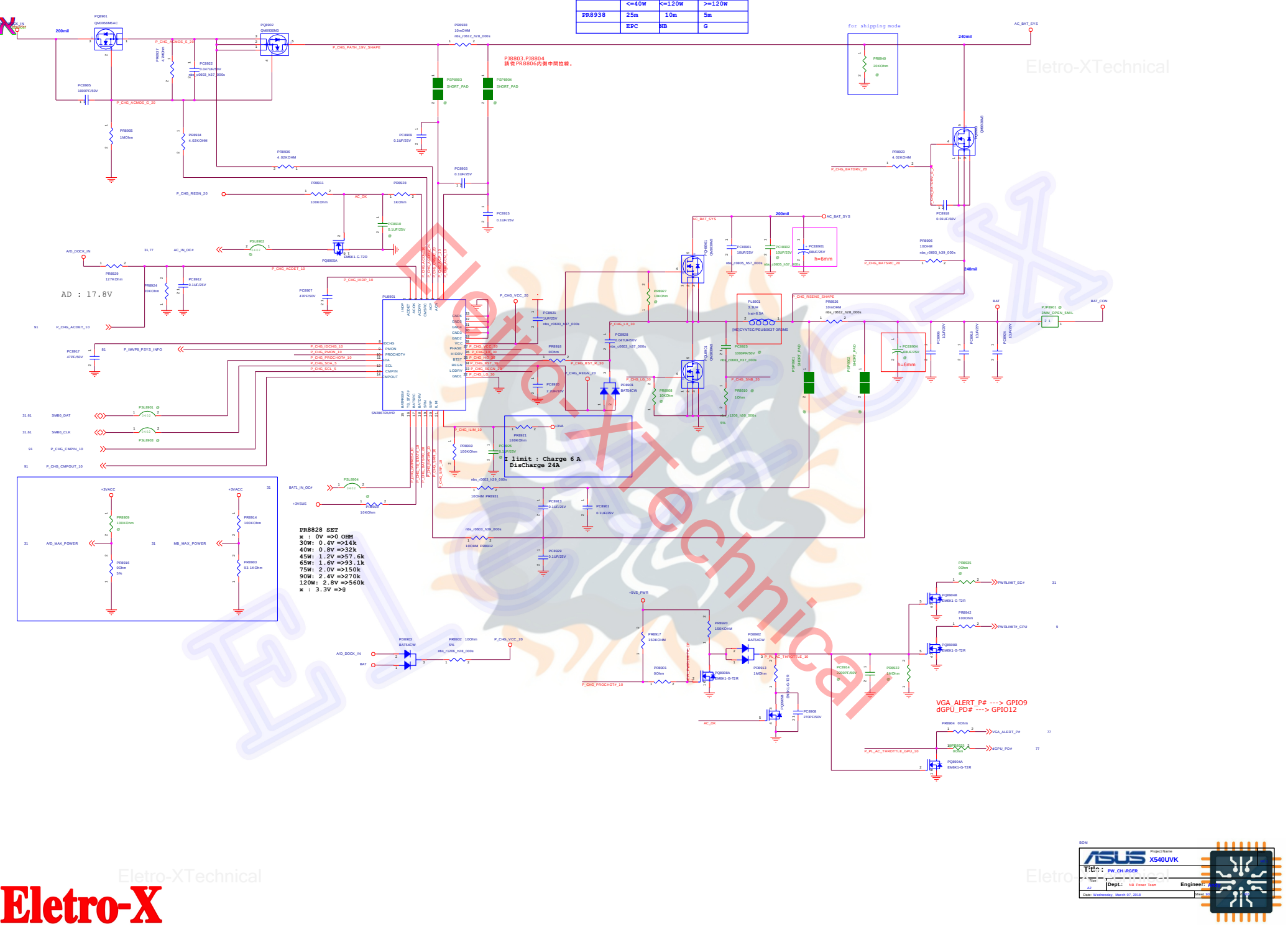
Mirror Function Signal Mapping Columns 1 to 5

PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A1	VSSQ		A2	DQ1	DQ25	A3	VSSQ		A4	DQ0	DQ24	A5	NC	
B1	VDDQ		B2	DQ3	DQ27	B3	VDDQ		B4	DQ2	DQ26	B5	VSS	
C1	VSSQ		C2	EDC0	EDC3	C3	VSSQ		C4	VSSQ		C5	VDD	
D1	VDDQ		D2	DBI0	DBI3	D3	VDDQ		D4	WCK01	WCK23	D5	WCK01	WCK23
E1	VSSQ		E2	DQ5	DQ29	E3	VSSQ		E4	DQ4	DQ28	E5	VDDQ	
F1	VDDQ		F2	DQ7	DQ31	F3	VDDQ		F4	DQ6	DQ30	F5	VSSQ	
G1	VDD		G2	VDDQ		G3	RAS	CAS	G4	VDD		G5	VSS	
H1	VSS		H2	VSSQ		H3	VDDQ		H4	A10/A0	A8/A7	H5	A9/A1	A11/A6
J1	MF		J2	RESET		J3	CKE		J4	ABI		J5	A12/A13	
K1	VSS		K2	VSSQ		K3	VDDQ		K4	A8/A7	A10/A0	K5	A11/A6	A9/A1
L1	VDD		L2	VDDQ		L3	CAS	RAS	L4	VDD		L5	VSS	
M1	VDDQ		M2	DQ31	DQ7	M3	VDDQ		M4	DQ30	DQ6	M5	VSSQ	
N1	VSSQ		N2	DQ29	DQ5	N3	VSSQ		N4	DQ28	DQ4	N5	VDDQ	
P1	VDDQ		P2	DBI3	DBI0	P3	VDDQ		P4	WCK23	WCK01	P5	WCK23	WCK01
R1	VSSQ		R2	EDC3	EDC0	R3	VSSQ		R4	VSSQ		R5	VDD	
T1	VDDQ		T2	DQ27	DQ3	T3	VDDQ		T4	DQ26	DQ2	T5	VSS	
U1	VSSQ		U2	DQ25	DQ1	U3	VSSQ		U4	DQ24	DQ0	U5	NC	

Mirror Function Signal Mapping Columns 10 to 14

PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1	PIN	MF=0	MF=1
A10	VREFD		A11	DQ8	DQ16	A12	VSSQ		A13	DQ9	DQ17	A14	VSSQ	
B10	VSS		B11	DQ10	DQ18	B12	VDDQ		B13	DQ11	DQ19	B14	VDDQ	
C10	VDD		C11	VSSQ		C12	VSSQ		C13	EDC1	EDC2	C14	VSSQ	
D10	VSS		D11	VDD		D12	VDDQ		D13	DBI1	DBI2	D14	VDDQ	
E10	VDDQ		E11	DQ12	DQ20	E12	VSSQ		E13	DQ13	DQ21	E14	VSSQ	
F10	VSSQ		F11	DQ14	DQ22	F12	VDDQ		F13	DQ15	DQ23	F14	VDDQ	
G10	VSS		G11	VDD		G12	CS	WE	G13	VDDQ		G14	VDD	
H10	BA3/A3	BA1/A5	H11	BA0/A2	BA2/A4	H12	VDDQ		H13	VSSQ		H14	VSS	
J10	SEN		J11	CK		J12	CK		J13	ZQ		J14	VREFC	
K10	BA1/A5	BA3/A3	K11	BA2/A4	BA0/A2	K12	VDDQ		K13	VSSQ		K14	VSS	
L10	VSS		L11	VDD		L12	WE	CS	L13	VDDQ		L14	VDD	




PR8938
<=40W
<=120W
>=120W
PR8938
25m
10m
5m
EPC
NB
G
PJ8803,PJ8804
請從PR8806內側中間拉線。
for shipping mode
AD : 17.8V
I limit : Charge 6 A
DisCharge 24A
PR8828 SET
x : 0V =>0 OHM
30W: 0.4V =>14k
40W: 0.8V =>32k
45W: 1.2V =>57.6k
65W: 1.6V =>93.1k
75W: 2.0V =>150k
90W: 2.4V =>270k
120W: 2.8V =>560k
x : 3.3V =>@
VGA_ALERT_P# ---> GPIO9
dGPU_PD# ---> GPIO12
Eletro-X
Eletro-XTechnical
X540UVK
PW_CH_RGER
NB Power Team

Address Selection Table

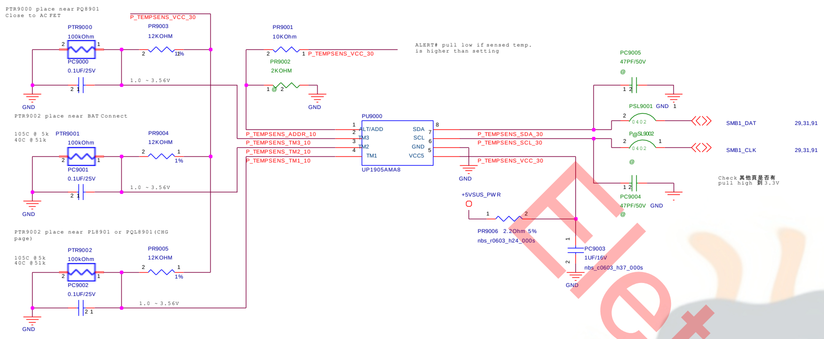
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

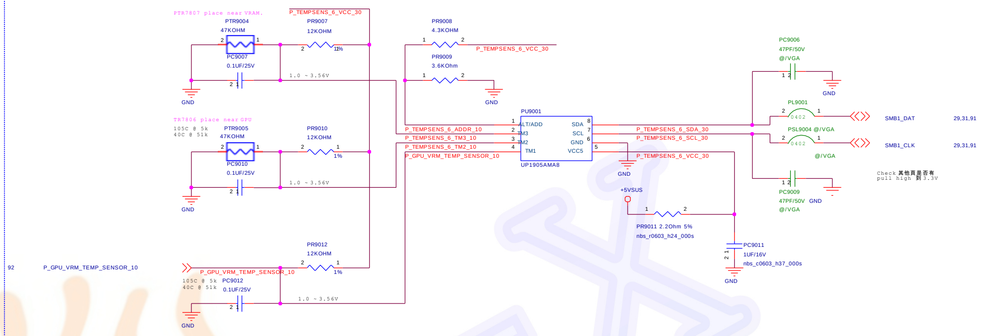
Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 =0 bit 5 =0 bit 6 =0 When ALERT# assert

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9008	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9009	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

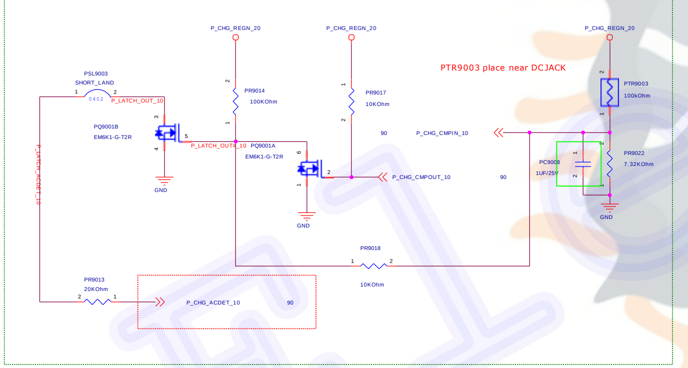


PTR9000 place near PQ8901
Close to AC FET
PTR9000
100kOhm
PR9003
12KOHM
PC9000
0.1UF/25V
PR9001
10KOhm
PR9002
2KOHM
ALERT# pull low if sensed temp. is higher than setting
PTR9002 place near BAT Connect
PTR9001
PR9004
PC9001
PTR9002 place near PL8901 or PQL8901(CHG page)
PTR9002
PR9005
PC9002
PU9000
UP1905AMA8
P_TEMPSENS_ADDR_10
P_TEMPSENS_TM3_10
P_TEMPSENS_TM2_10
P_TEMPSENS_TM1_10
P_TEMPSENS_SDA_30
P_TEMPSENS_SCL_30
P_TEMPSENS_VCC_30
PC9005
47PF/50V
PSL9001
SMB1_DAT
SMB1_CLK
29,31,91
PC9004
47PF/50V
+5VSUS_PWR
PR9006 2.2Ohm_5%
PC9003
1UF/16V
GND



PTR7807 place near VRAM.
P_TEMPSENS_6_VCC_30
PTR9004
47KOHM
PR9007
12KOHM
PR9008
4.3KOHM
PR9009
3.6KOHM
PC9007
0.1UF/25V
TR7805 place near GPU
PTR9005
47KOHM
PR9010
12KOHM
PC9010
0.1UF/25V
PU9001
UP1905AMA8
P_TEMPSENS_6_ADDR_10
P_TEMPSENS_6_TM3_10
P_TEMPSENS_6_TM2_10
P_GPU_VRM_TEMP_SENSOR_10
P_TEMPSENS_6_SDA_30
P_TEMPSENS_6_SCL_30
P_TEMPSENS_6_VCC_30
PC9006
47PF/50V
@/VGA
PL9001
PSL9004 @/VGA
SMB1_DAT
SMB1_CLK
29,31,91
PC9009
47PF/50V
+5VSUS
PR9011 2.2Ohm 5%
PC9011
1UF/16V
PR9012
12KOHM
PC9012
0.1UF/25V
P_GPU_VRM_TEMP_SENSOR_10
GND

DC Jack Thermal Latch



P_CHG_REGN_20
PTR9003 place near DCJACK
PSL9003
SHORT_LAND
P_LATCH_OUT_10
PQ9001B
EM6K1-G-T2R
PR9014
100KOhm
PR9017
10KOhm
PQ9001A
EM6K1-G-T2R
P_CHG_CMPIN_10
P_CHG_CMPOUT_10
PTR9003
100kOhm
PC9008
1UF/25V
PR9022
7.32KOhm
PR9018
10KOhm
PR9013
20KOhm
P_CHG_ACDET_10
GND

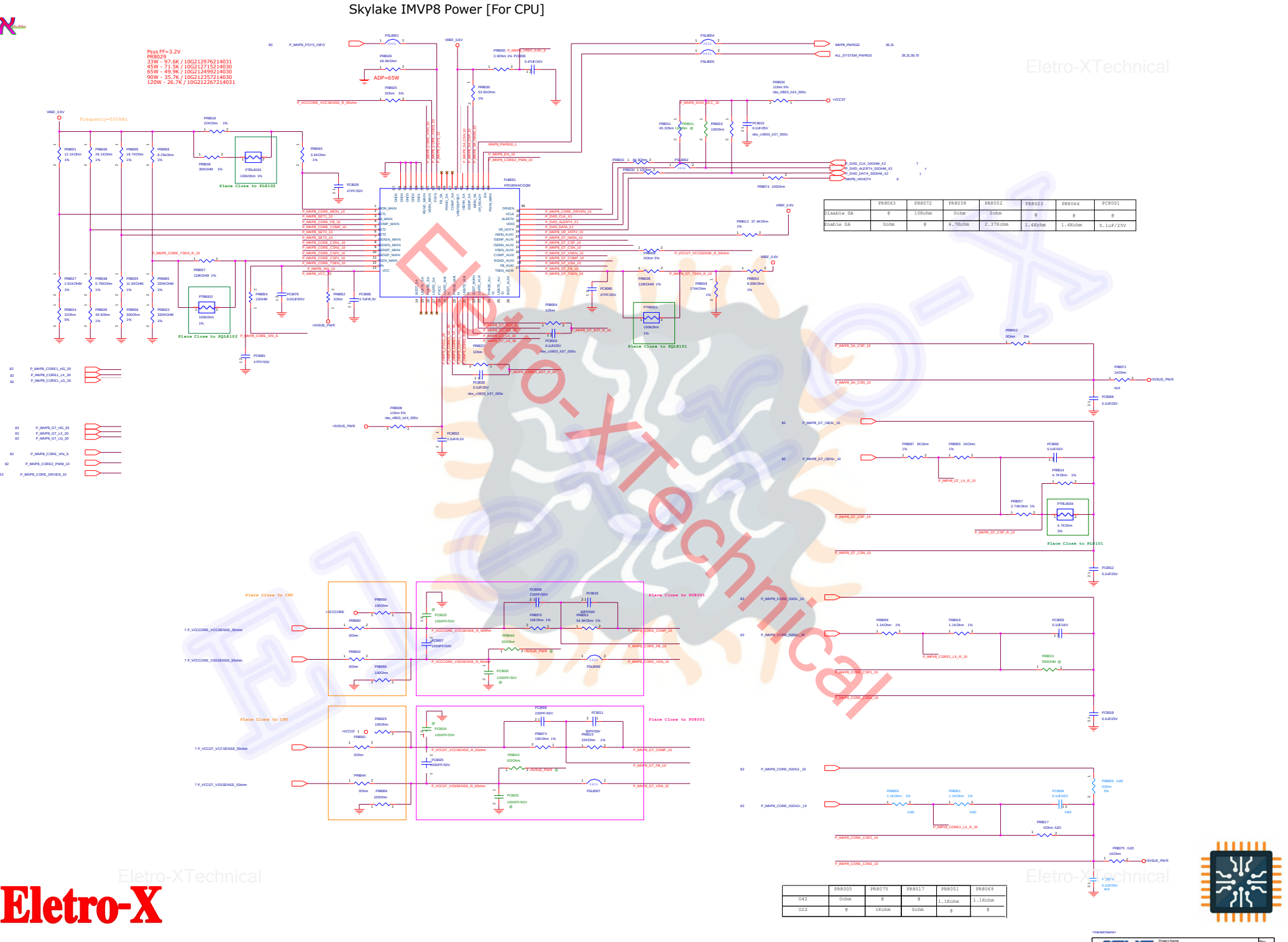
Project Name: X540UVK

Title : PW_PROTECTION

Engineer:

Date: Wednesday, March 07, 2018

Skylake IMVP8 Power [For CPU]



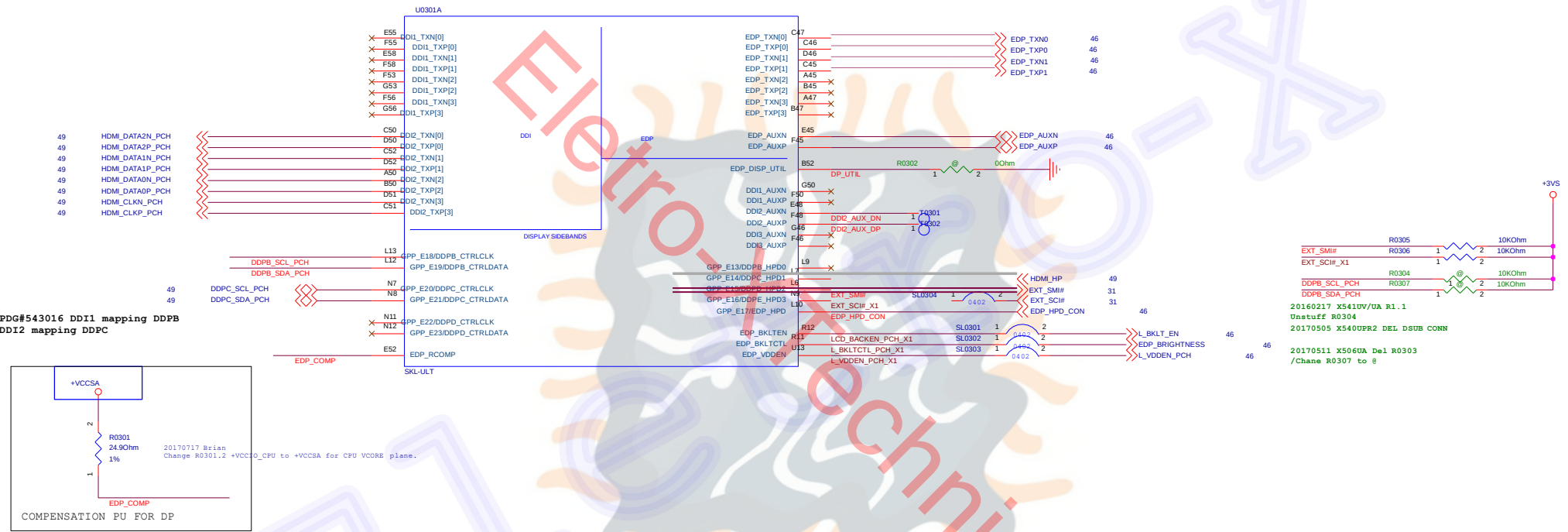
	PR8063	PR8072	PR8038	PR8052	PR8003	PR8066	PC8001
Disable SA	0	10Kohm	0ohm	0ohm	0	0	0
Enable SA	0ohm	0	4.7Kohm	2.37Kohm	1.4Kohm	1.4Kohm	0.1uF/25V

	PR8005	PR8075	PR8017	PR8051	PR8069
U42	0ohm	0	0	1.1Kohm	1.1Kohm
U22	0	1Kohm	0ohm	0	0

Display Port

A	EDP
B	
C	HDMI

Intel Version	ASUS P/N



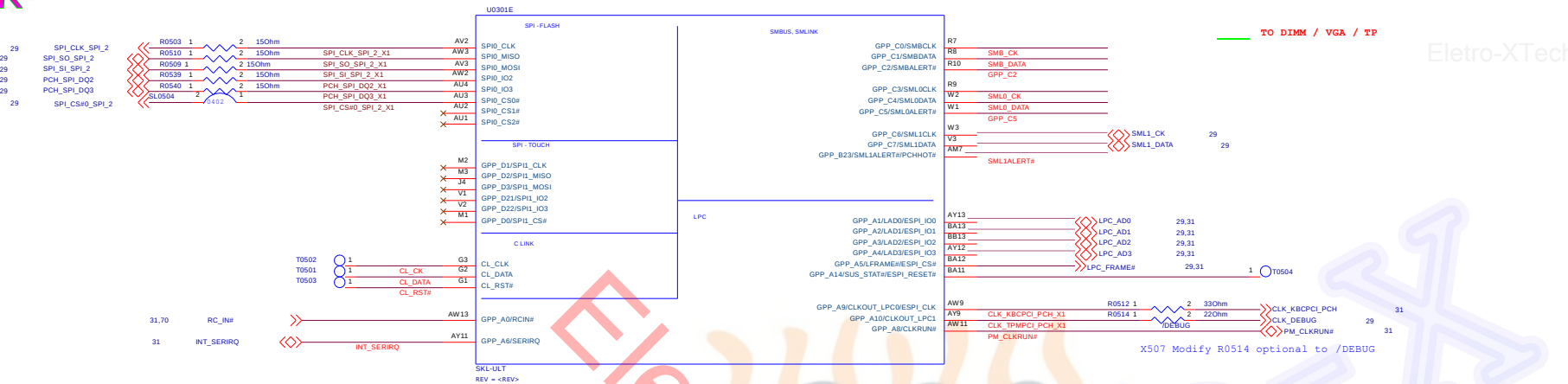
PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC

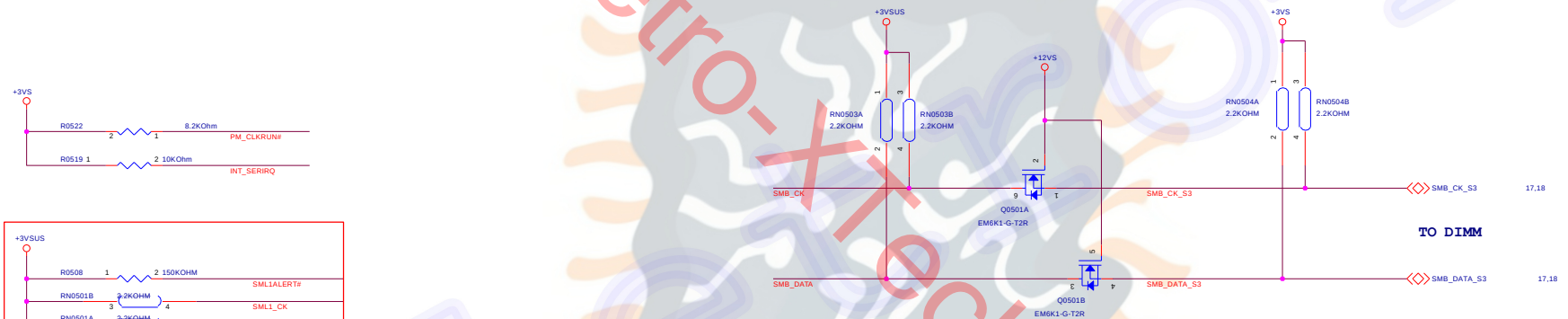
20160217 X541UV/UA R1.1
Unstuff R0304
20170505 X540UPR2 DEL DSUB CONN

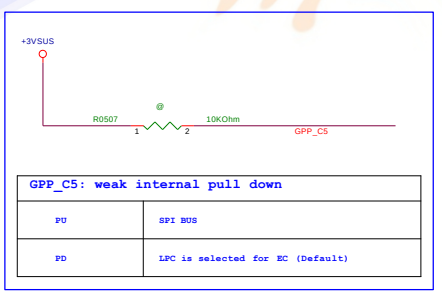
20170511 X506UA Del R0303
/Chane R0307 to @

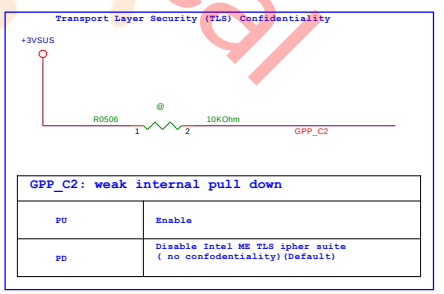
BOM

ASUS	Project Name: X407UA/UV	Rev: R1.0
Title : CPU_DISPLAY		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 4 of 102	



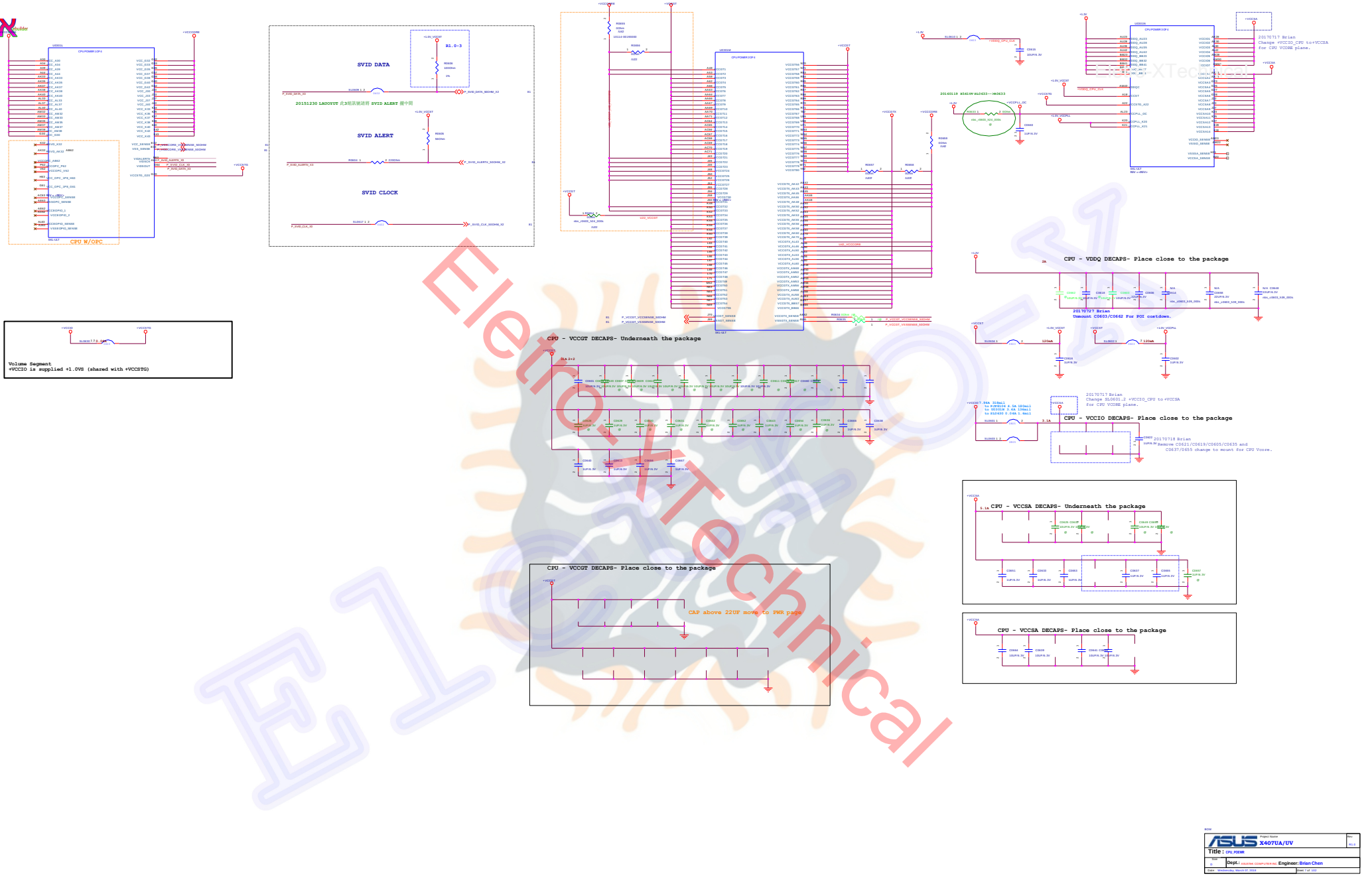


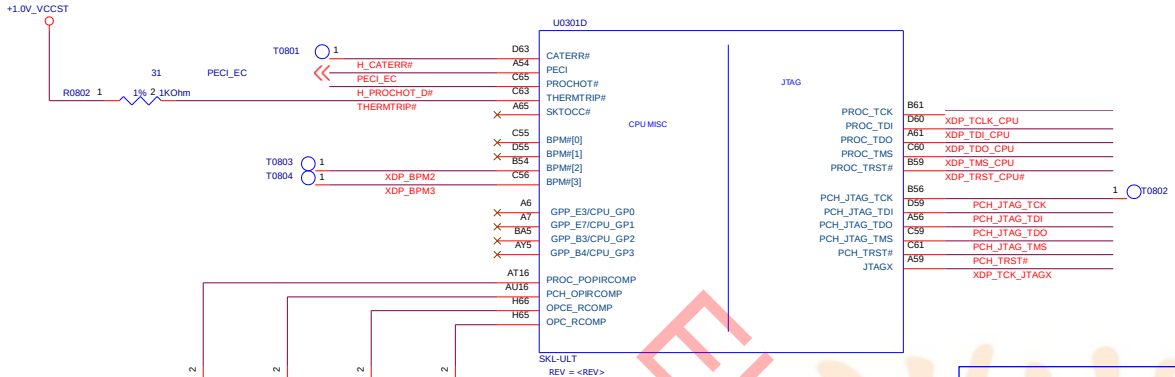




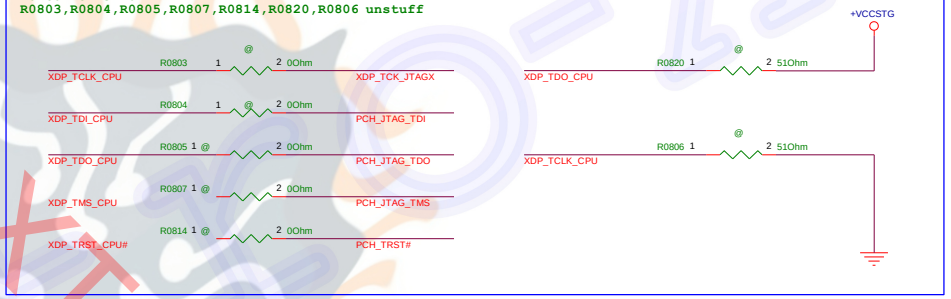
BOM

ASUS	Project Name: X407UA/UV	ev: R1.0
Title : CPU_LPC,SPI,SMB,CLINK		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet 6	



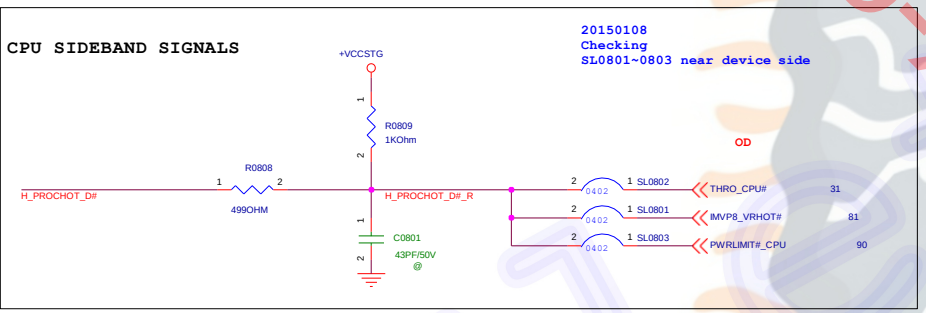


20160218 X541UV
R0803,R0804,R0805,R0807,R0814,R0820,R0806 unstuff



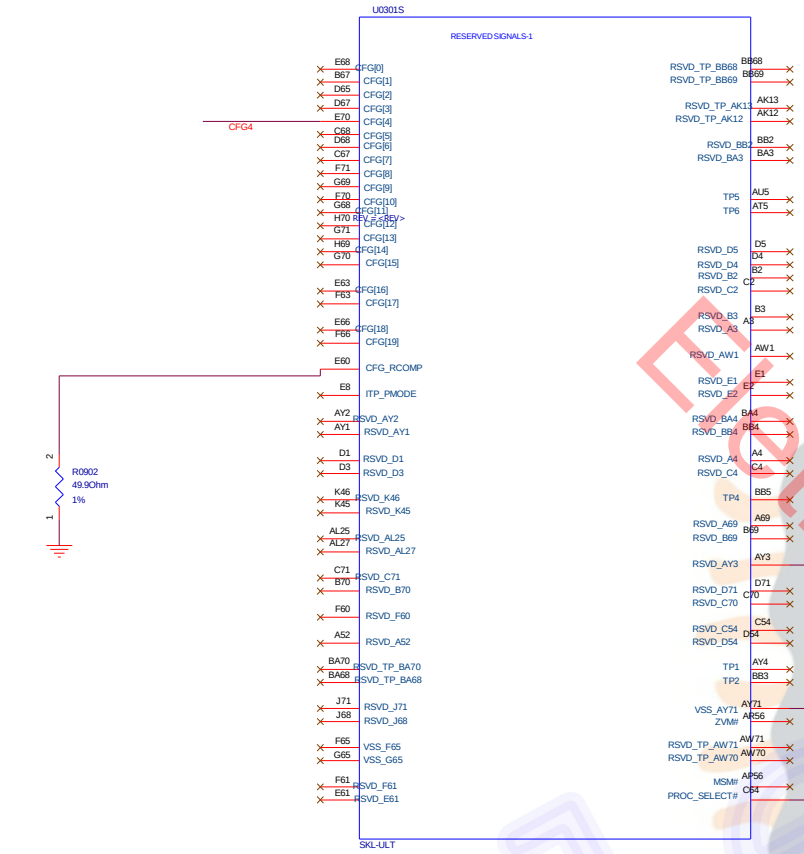
CPU SIDEBAND SIGNALS

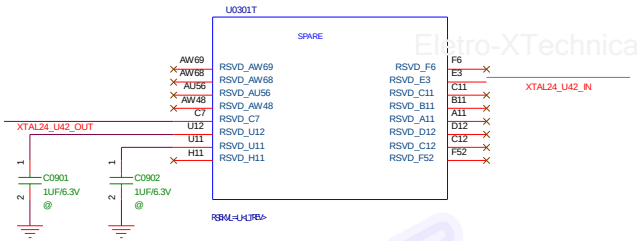
20150108
Checking
SL0801~0803 near device side



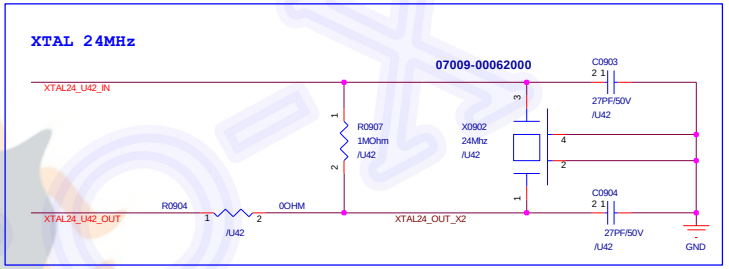
BOM

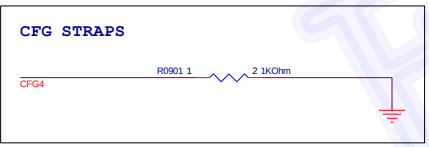
ASUS	Project Name: X407UA/UV	ev: R1.0
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet 9 of 102	





20171023 Jack Add XTAL 24M for KBL-R.





	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

BOM

ASUS	Project Name: X407UA/UV	ev: R1.0
Title : CPU_CFG,RSVD		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet 10 of 102	

2016/12/05 X542UA_R1.0 #98, DDR SWAP
2016/12/07 X542UA_R1.0 #A3, DDR SWAP

SWAP

J1601A

M_A_DQ[63:0] 5

M_A_CLK_DDR0
M_A_CLK_DDR#0
M_A_CLK_DDR1
M_A_CLK_DDR#1
M_A_CKE0
M_A_CKE1
M_A_CS#0
M_A_CS#1
M_A_ODT0
M_A_ODT1
M_A_BG0
M_A_BG1
M_A_BA0
M_A_BA1
M_A_A[13:0]
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_ACT#
M_A_PAR
M_A_ALERT#
M_A_DIMM0_EVENT#
M_A_VREFCA
SMB_DATA_S3
SMB_CK_S3
M_A_DIMM0_SA2
M_A_DIMM0_SA1
M_A_DIMM0_SA0

D0 2017/0606 X507 SWAP
D1 2017/0606 X507 SWAP
D2 2017/0606 X507 SWAP
D3 2017/0606 X507 SWAP
D4 2017/0606 X507 SWAP
D5 2017/0606 X507 SWAP
D6 2017/0606 X507 SWAP
D7 2017/0606 X507 SWAP

M_A_DQS[7:0] 5
X507/2017/06/06 SWAP

M_A_DQS#[7:0] 5
X507/2017/06/06 SWAP

Place close to SO-DIMM

For ECC
T1601
T1602

DDR4_DIMM_260P
12002-00082100

20170707 Brian
Change J1601 12002-00080100 to 12002-00082100(5.2H).

'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

J1601B
DDR4_DIMM_260P

2017/02/02 X542UA_R1.1 #24, 0ohm modify to SL

2017/02/02 X542UA_R1.1 #24, 0ohm modify to SL
2017/03/16 X542UA_R2.0 #03, Modify SA0 to pull down

Place close to SO-DIMM

WRITE ADDRESS: 0X

Place close to SO-DIMM Socket (+VTT Pin)

Place close to SO-DIMM Socket (+VPP Pin)

2017/02/06 X542UA_R1.1 #26, EMI solution

Place close to SO-DIMM Socket (VDD Pin)

20170719 Brian
Remove C1601 and add C1629/C1630/C1631.

20170727 Brian
Add C1605/C1621/C1624 For POI cost down.

BOM

Project Name X507UA/UV

Title : DDR3_ON-BOARD_B_L32

Size C

Dept.: NB2_RD1_EE1

Engineer: Bull Tsai

2016/11/16 X542UA_#78, Remove R1709

2016/12/05 X542UA_R1.0 #99, DDR SWAP

SWAP

M_B_DQ[63:0] 5

J1701A

M_B_CLK_DDR0	137	CK0_T	DQ0	8	M_B_DQ8
M_B_CLK_DDR#0	139	CK0_C	DQ1	7	M_B_DQ12
M_B_CLK_DDR1	138	CK1_T	DQ2	20	M_B_DQ15
M_B_CLK_DDR#1	140	CK1_C	DQ3	21	M_B_DQ11
			DQ4	4	M_B_DQ13
M_B_CKE0	109	CKE0	DQ5	3	M_B_DQ9
M_B_CKE1	110	CKE1	DQ6	16	M_B_DQ10
			DQ7	17	M_B_DQ14
M_B_CS#0	149	S0*	DQ8	28	M_B_DQ4
M_B_CS#1	157	S1*	DQ9	29	M_B_DQ5
			DQ10	41	M_B_DQ7
M_B_ODT0	155	ODT0	DQ11	42	M_B_DQ6
M_B_ODT1	161	ODT1	DQ12	24	M_B_DQ1
			DQ13	25	M_B_DQ0
M_B_BG0	115	BG0	DQ14	38	M_B_DQ3
M_B_BG1	113	BG1	DQ15	37	M_B_DQ2
M_B_BA0	150	BA0	DQ16	50	M_B_DQ20
M_B_BA1	145	BA1	DQ17	49	M_B_DQ17
M_B_A[13:0]			DQ18	62	M_B_DQ21
	144	A0	DQ19	63	M_B_DQ22
M_B_A0	133	A1	DQ20	46	M_B_DQ19
M_B_A1	132	A2	DQ21	45	M_B_DQ18
M_B_A2	131	A3	DQ22	58	M_B_DQ23
M_B_A3	128	A4	DQ23	59	M_B_DQ18
M_B_A4	126	A5	DQ24	70	M_B_DQ28
M_B_A5	127	A6	DQ25	71	M_B_DQ24
M_B_A6	122	A7	DQ26	83	M_B_DQ26
M_B_A7	125	A8	DQ27	84	M_B_DQ27
M_B_A8	121	A9	DQ28	66	M_B_DQ27
M_B_A9	148	A10_AP	DQ29	67	M_B_DQ29
M_B_A10	120	A11 A12	DQ30	79	M_B_DQ25
M_B_A11	119	A13	DQ31	80	M_B_DQ31
M_B_A12	158	A14 WE*	DQ32	174	M_B_DQ30
M_B_A13	151	A15_CAS*	DQ33	173	M_B_DQ36
	156	A16_RAS*	DQ34	187	M_B_DQ32
	152		DQ35	186	M_B_DQ39
		ACT*	DQ36	170	M_B_DQ34
M_B_ACT#	114		DQ37	169	M_B_DQ33
		PARITY	DQ38	183	M_B_DQ37
M_B_PAR	143	ALERT*	DQ39	182	M_B_DQ38
M_B_ALERT#	134	EVENT*	DQ40	195	M_B_DQ35
		RESET*	DQ41	194	M_B_DQ41
M_B_DIMM0_EVENT#	108		DQ42	207	M_B_DQ40
		VREFCA	DQ43	208	M_B_DQ42
	164		DQ44	191	M_B_DQ47
		SDA	DQ45	190	M_B_DQ46
SMB_DATA_S3	254	SCL	DQ46	203	M_B_DQ44
SMB_CK_S3	253		DQ47	204	M_B_DQ43
		SA2	DQ48	216	M_B_DQ49
	166	SA1	DQ49	215	M_B_DQ55
M_B_DIMM0_SA2	260	SA0	DQ50	228	M_B_DQ53
M_B_DIMM0_SA1	256		DQ51	229	M_B_DQ54
M_B_DIMM0_SA0			DQ52	211	M_B_DQ48
			DQ53	212	M_B_DQ52
			DQ54	224	M_B_DQ49
		CB0_NC	DQ55	225	M_B_DQ51
	92	CB1_NC	DQ56	237	M_B_DQ50
	91	CB2_NC	DQ57	236	M_B_DQ57
	101	CB3_NC	DQ58	249	M_B_DQ59
	105	CB4_NC	DQ59	250	M_B_DQ62
	88	CB5_NC	DQ60	232	M_B_DQ61
	87	CB6_NC	DQ61	233	M_B_DQ58
	100	CB7_NC	DQ62	245	M_B_DQ56
	104		DQ63	246	M_B_DQ60
					M_B_DQ63

M_B_DQS[7:0] 5

20161205 swap

	12	DM0*/DBI0*	DQS0_T	13	M_B_DQS1
	33	DM1*/DBI1*	DQS1_T	34	M_B_DQS0
	54	DM2*/DBI2*	DQS2_T	55	M_B_DQS2
	75	DM3*/DBI3*	DQS3_T	76	M_B_DQS3
	178	DM4*/DBI4*	DQS4_T	179	M_B_DQS4
	199	DM5*/DBI5*	DQS5_T	200	M_B_DQS5
	220	DM6*/DBI6*	DQS6_T	221	M_B_DQS6
	241	DM7*/DBI7*	DQS7_T	242	M_B_DQS7
	96	DM8*/DBI8*	DQS8_T	97	M_B_DQS7

M_B_DQS#[7:0] 5

20161205 swap

			DQS0_C	11	M_B_DQS#1
			DQS1_C	32	M_B_DQS#0
			DQS2_C	53	M_B_DQS#2
			DQS3_C	74	M_B_DQS#3
			DQS4_C	177	M_B_DQS#4
			DQS5_C	198	M_B_DQS#5
			DQS6_C	219	M_B_DQS#6
			DQS7_C	240	M_B_DQS#7
			DQS8_C	95	M_B_DQS#7

For ECC

T1702 1 — 1 M_B_DIMM0_S2 — 162

T1701 1 — 1 M_B_DIMM0_S3 — 165

S2*/C0 162

S3*/C1 165

DDR4_DIMM_260P

12002-00080300

'EVENT_N': INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

20170707 Brian
Change J1701 12002-00082500 to 12002-00080300(4H).

+1.2V — R1707 240Ohm — M_B_VREFCA

C1704 0.1UF/10V — C1701 2.2UF/10V — 6,17 — 6,17 — GND GND

Place close to SO-DIMM

5,17,70 DDR4_DRAMRST#

+1.2V — C1711 10UF/6.3V — C1726 10UF/6.3V — C1717 0.1UF/16V @/EMI — GND GND GND

nbs_c0603_h37_000s

Place close to SO-DIMM Socket (+VTT Pin)

+2.5V — C1725 10UF/6.3V — C1710 10UF/6.3V — C1727 1UF/6.3V — C1721 1UF/6.3V

Place close to SO-DIMM Socket (+VPP Pin)

2017/02/06 X542UA_R1.1 #26, EMI solution

+1.2V

20170707 Brian
Remove CE1701 for no-location.

Place close to SO-DIMM Socket (VDD Pin)

C1712 10UF/6.3V @/EMI — C1715 10UF/6.3V @ — C1707 10UF/6.3V — C1722 10UF/6.3V @/EMI — C1719 10UF/6.3V @ — C1703 10UF/6.3V — C1716 10UF/6.3V — C1706 10UF/6.3V

C1708 1UF/6.3V @ — C1718 0.1UF/16V @/EMI — C1702 1UF/6.3V — C1714 1UF/6.3V — C1723 0.1UF/16V @/EMI — C1724 1UF/6.3V @ — C1720 1UF/6.3V — C1713 1UF/6.3V

20170727 Brian
Add C1703/C1716 and unmount C1715/C1719 For POI cost down.

2017/02/06 X542UA_R1.1 #26, EMI solution

+1.2V — J1701B — +VTT — +2.5V — +3VS

VDD19 VDD18 VDD17 VDD16 VDD15 VDD14 VDD13 VDD12 VDD11 VDD10 VDD9 VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1

VTT 258 — VPP2 259 — VPP1 257

VDDSPD 255 — SL1704 Q402 — C1705 0.1UF/10V — C1709 2.2UF/10V — GND GND

2017/02/02 X542UA_R1.1 #24, Ohm modify to SL

NP_NC1 263 — NP_NC2 264

MT1 261 — MT2 262

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47

VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94

DDR4_DIMM_260P

2017/02/02 X542UA_R1.1 #24, Ohm modify to SL

+3VS — R1703 0Ohm — SL1702 — R1704 0Ohm

SL1703 — R1701 0Ohm — SL1701

M_B_DIMM0_SA2 M_B_DIMM0_SA1 M_B_DIMM0_SA0

Place close to SO-DIMM

WRITE ADDRESS: 0XA4

<Variant Name>

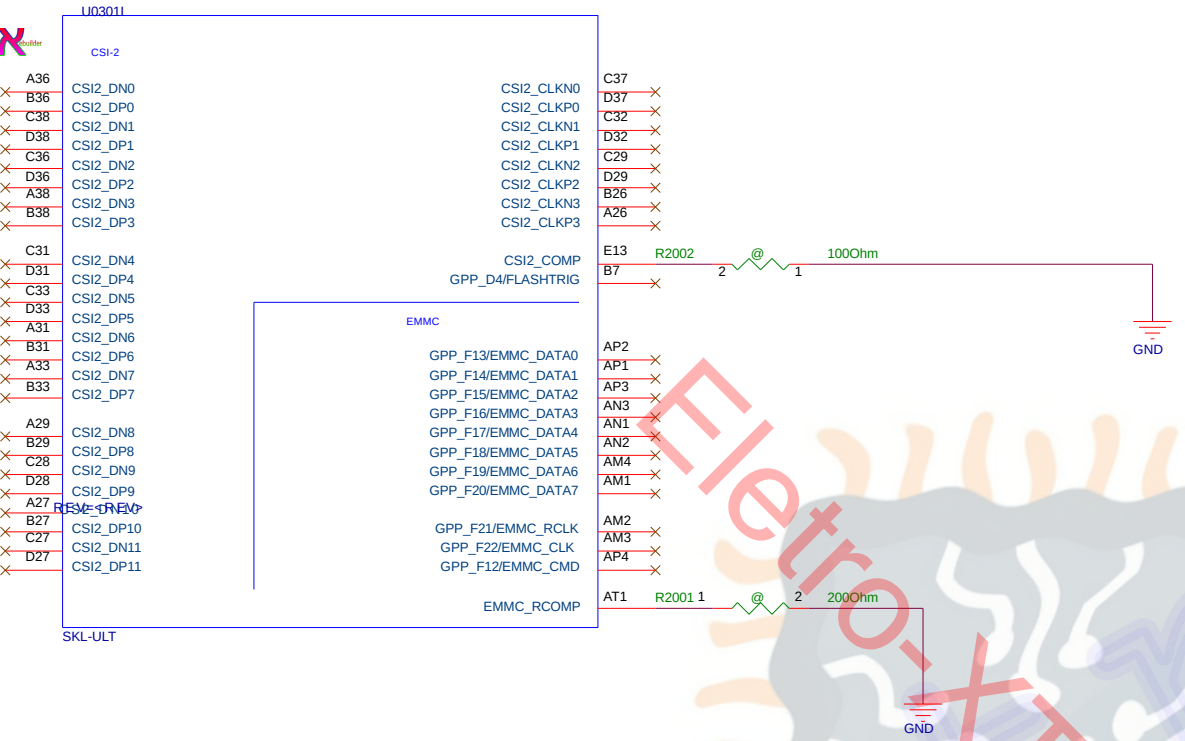
ASUS X507UA/UV

Title : DDR4_SO-DIMM_1

Size C — Dept.: — Engineer: Bull Tsai

Date: Wednesday, March 07, 2018 — Sheet 18 of 102

Eletro-X



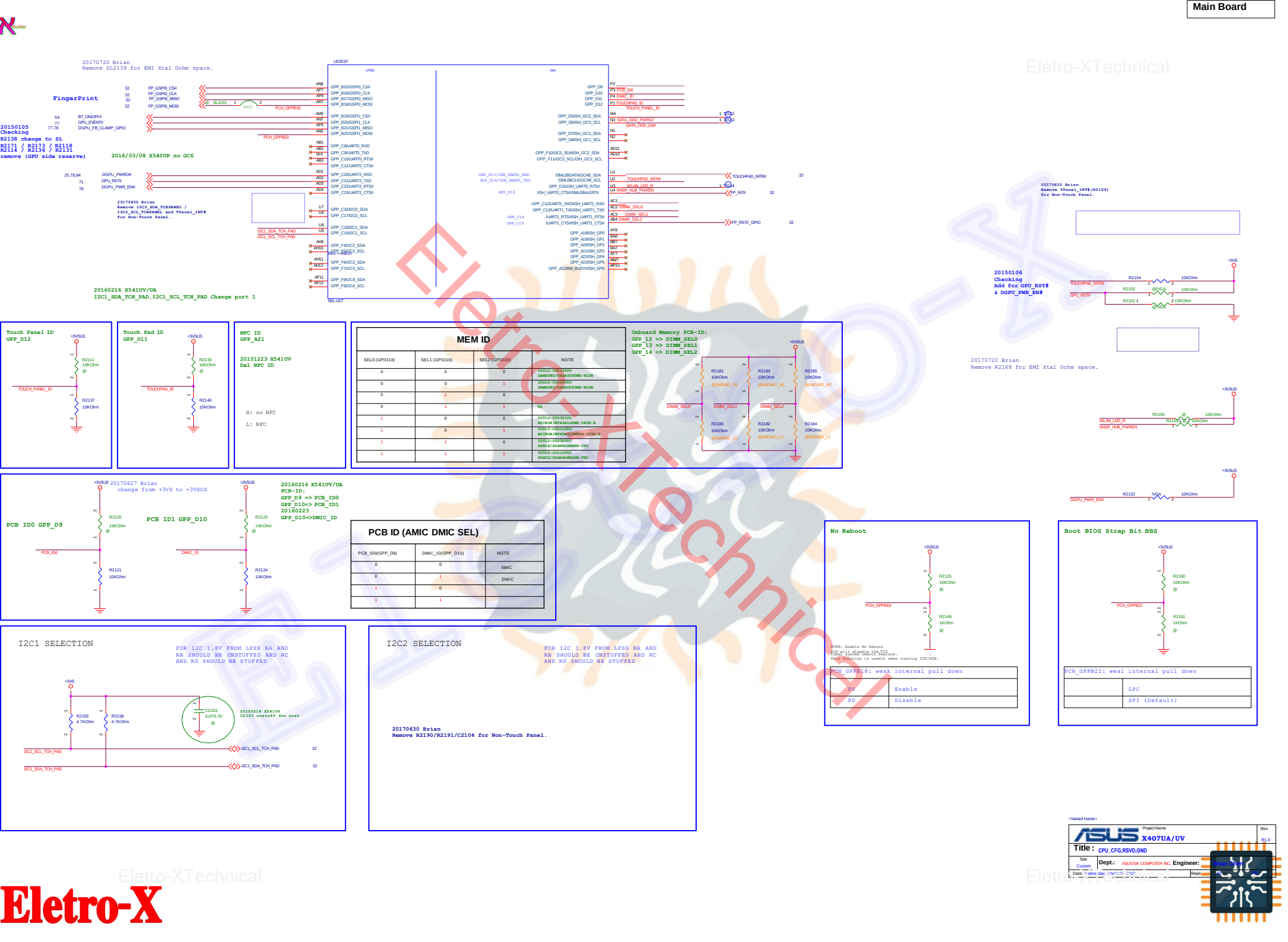
BOM

Project Name: X407UA/UV

Title : CPU_PCH_CSI2,EMMC

Size

Dept : Engineer :

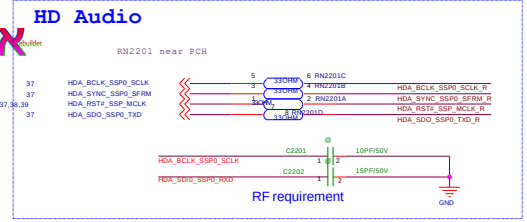


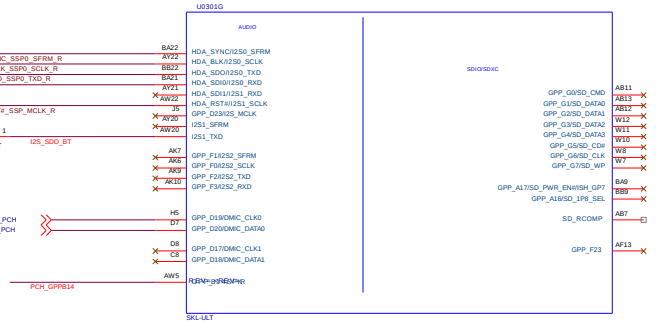
SEL0 (GPIO18)	SEL1 (GPIO19)	SEL2 (GPIO20)	NOTE
0	0	0	03012-00010200 SAMSUNG/K4A8G085WE-BCPB
0	0	1	03012-00030000 SAMSUNG/K4A8G085WB-BCPB
0	1	0	
0	1	1	0G
1	0	0	03012-00030100 MICRON/MT40A1G8WE-083E:B
1	0	1	03012-00010300 MICRON/MT40A512M8RH-083E:B
1	1	0	03012-00030300 HYNIX/H5AN8G8NMFR-TFC
1	1	1	03012-00010000 HYNIX/H5AN4G8NAFR-TFC

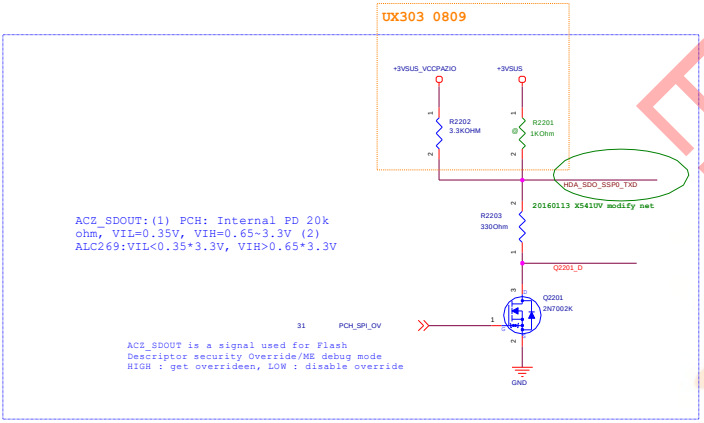
PCB_ID0(GPP_D9)	DMIC_ID(GPP_D10)	NOTE
0	0	AMIC
0	1	DMIC
1	0	
1	1	

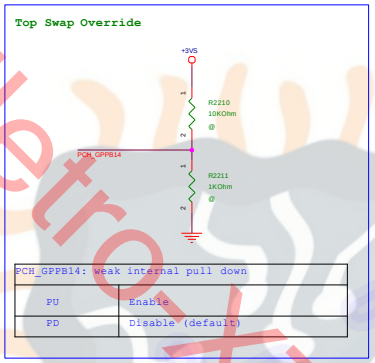
PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable

PCH_GPPB22: weal internal pull down	
	LPC
	SPI (Default)









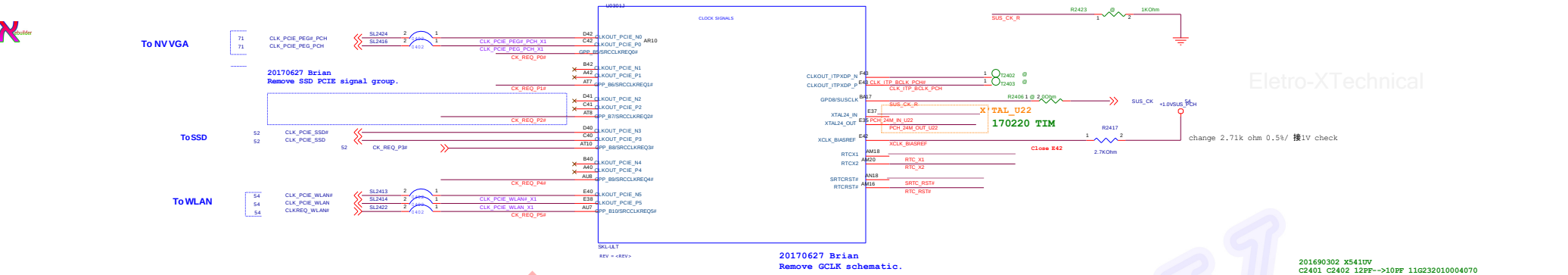
Eletro-X

ASUS X407UA/UV

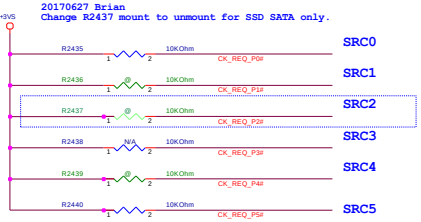
Title : CPU_PCH_AUDIO,SDIO,SDXC

Size: C | Dept.: ASUSTeK COMPUTER INC. | Engineer: Brian Chen

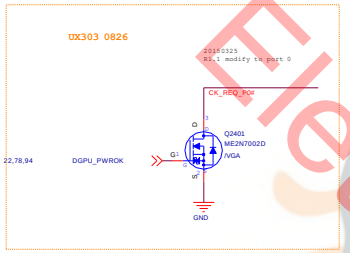
Date: Wednesday, March 07, 2018 | Sheet 23 of 102



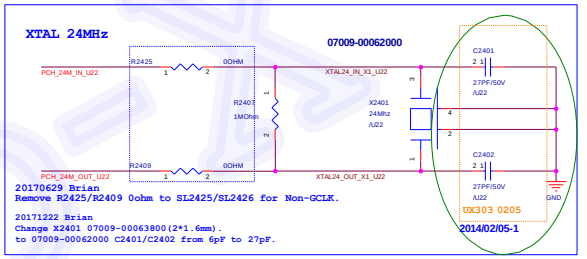
20170627 Brian
Change R2437 mount to unmount for SSD SATA only.



X506UA for No Use can be NC



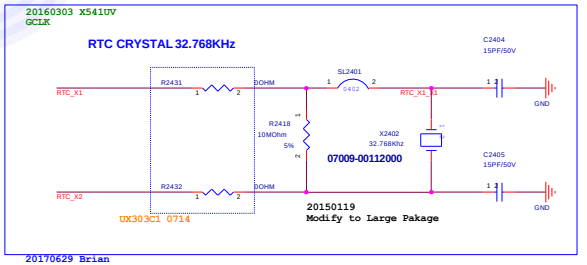
201690302 X541UV
C2401 C2402 12PF-->10PF 11G232010004070



20170629 Brian
Remove R2425/R2409 0ohm to SL2425/SL2426 for Non-GCLK.

20171222 Brian
Change X2401 07009-00063800(2*1.6mm).
to 07009-00062000 C2401/C2402 from 6pF to 27pF.

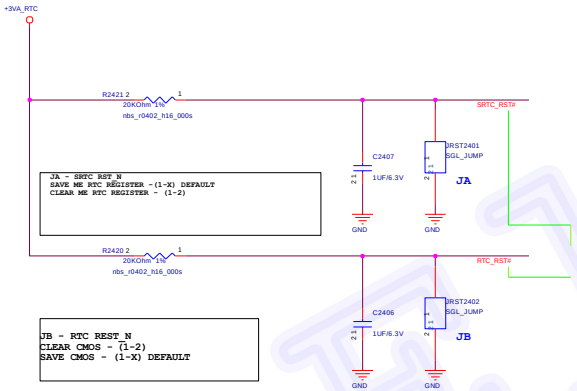
20160303 X541UV
GCLK

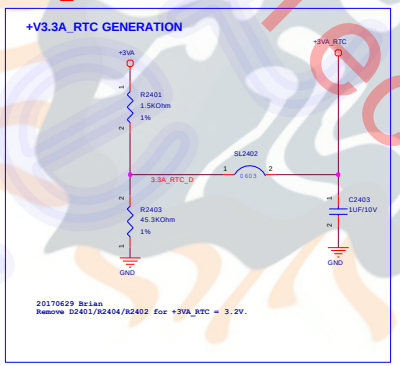


20170629 Brian
Remove R2431/R2432 0ohm to short for Non-GCLK.

20170720 Brian
Add R2431/R2432/R2409/R2425 for EMI 黑屏issue.

Kabylake +3VA_RTC MAX:3.2V min:3.0V





Eletro-X

BOM

ASUS Project Name X407UA/UV

Title : CPU_PCH_CLOCK SIGNALS,RTC

Size C | Dept.: ASUSTeK COMPUTER INC. | Engineer: Brian Chen

20150108
Checking
Add R2507

U0301K
SYSTEM POWER MANAGEMENT
SKL-ULT
REV = <REV>

20160219 X5410V R1.1
U2502 unstuff,r2518 stuff for cost

Checking
待SR 回來驗，是否拿掉U2502

U2502
74LVC1G08GW

UX303CN 0311

09'MoW04:
Optional if ME FW is Ignition FW

UX303C1 0620

2014/04/09-1

Power failure solution (S0-->G3,S5-->G3):

D2207: Prevent EC drive high, SUS_PWRGD sink low in S5-->G3.

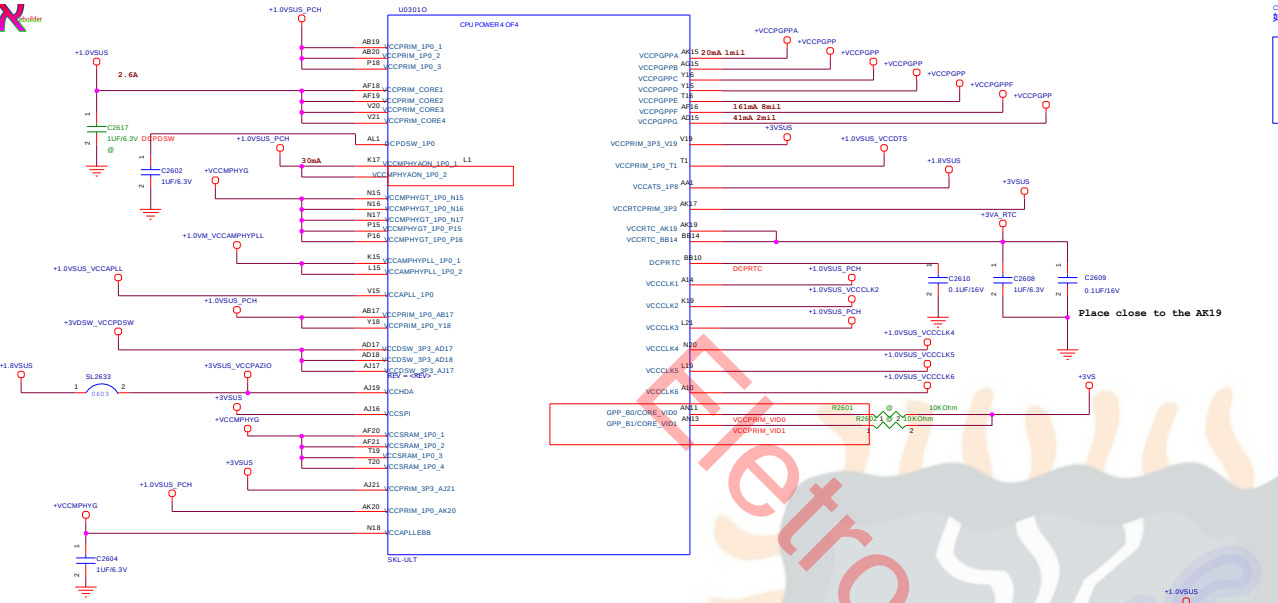
EMI solution

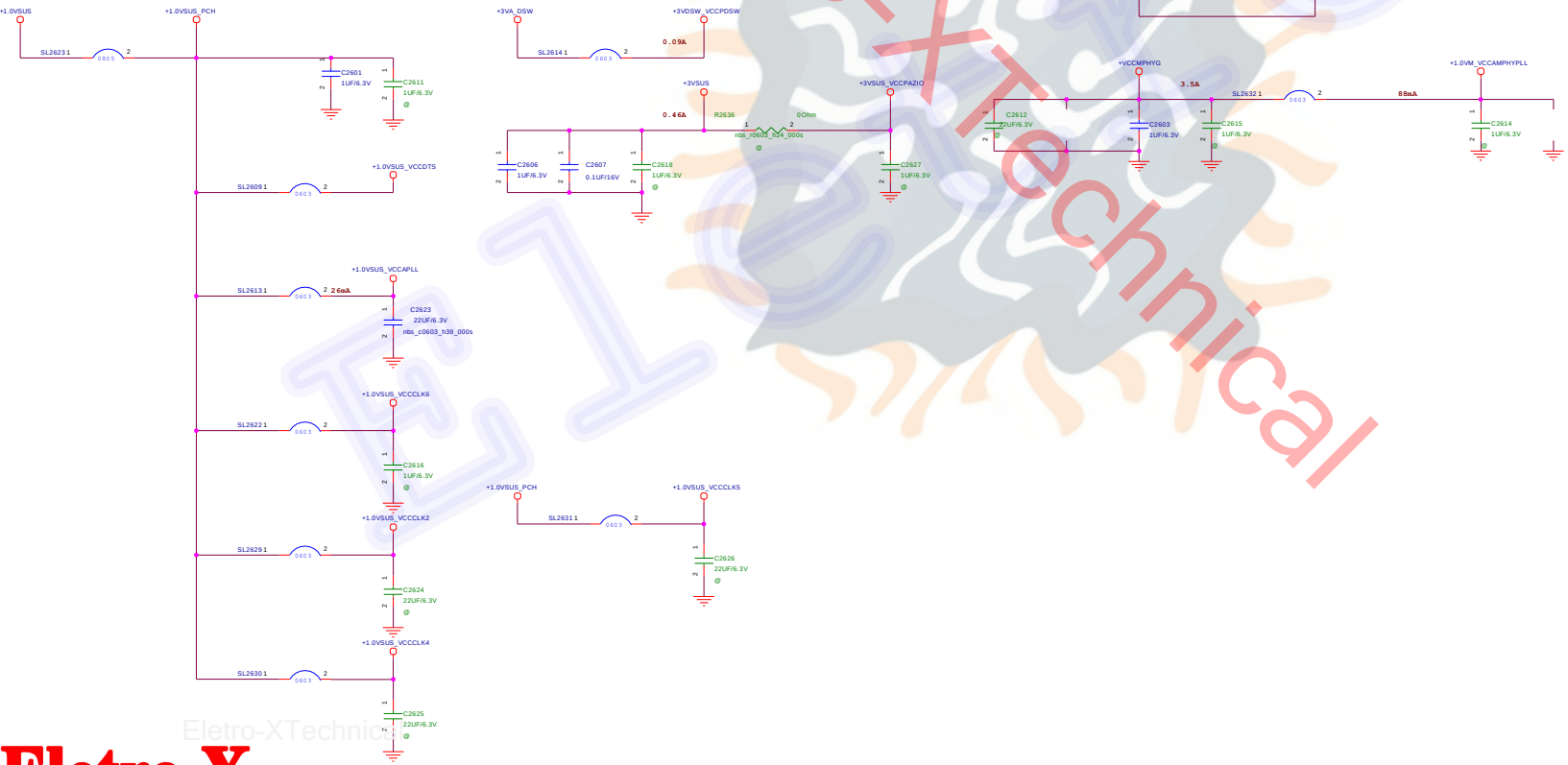
Close D2501

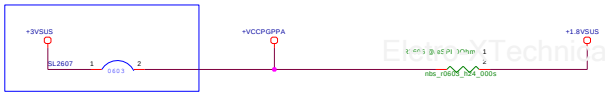
2017/05/12 remove R2505 ,power sequence will be check

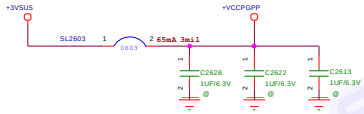
Project Name	X407UA/UV		
Title :	CPU_PCH_SYS_POWER		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 26 of 102		

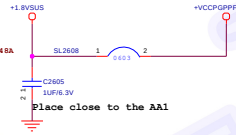
Checking
20150318
cost 考量被改SI
如果用eSPI 要移除

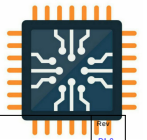






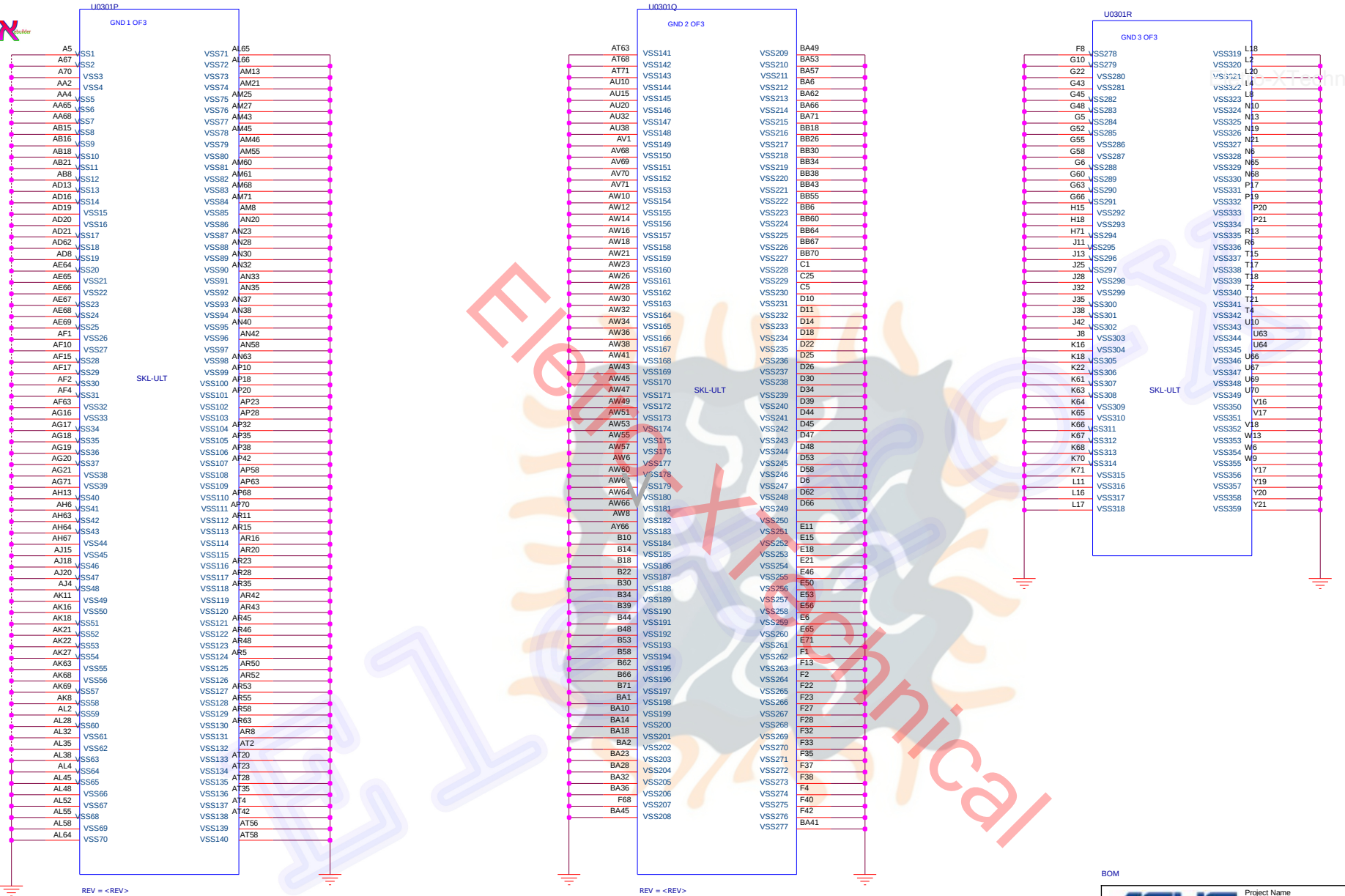






BOM

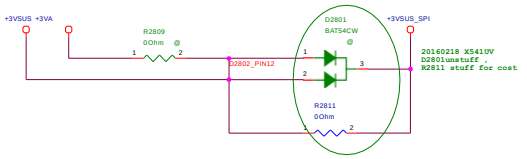
Project Name	X407UA/UV
Rev	R1.0
Title :	CPU_PCH_POEWR,GND



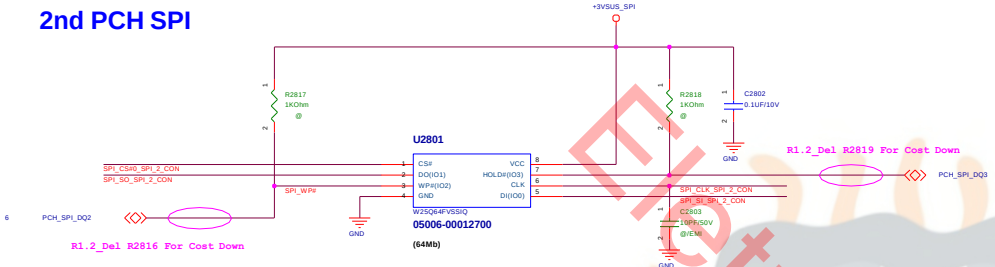
BOM

R V	Project Name: X407UA/UV	ev: R1.0
	Title : CPU_PCH_POEWR,GND	
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen
Date: Wednesday, March 07, 2018	Sheet 28 of 102	

SPI PCH Power

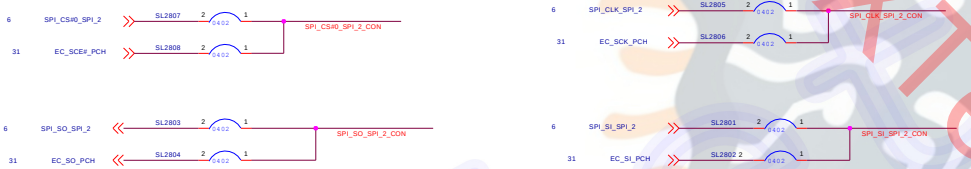


2nd PCH SPI

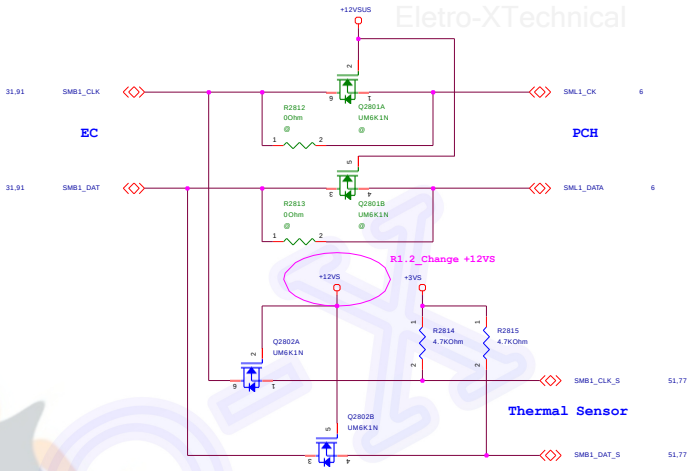


2nd : 05006-00012700 GIGADEVICE
X540LJ/LA add
X541UV/UA add 20160223
X540UPR BOM change_20170419
M: 05006-00013600
05006-00013400
05006-00012700

20170505 X540UPR2 BOM
M: 05006-00012700
05006-00013700
05006-00013600

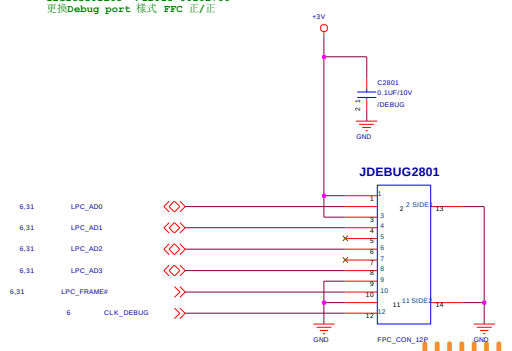


System Management Interface

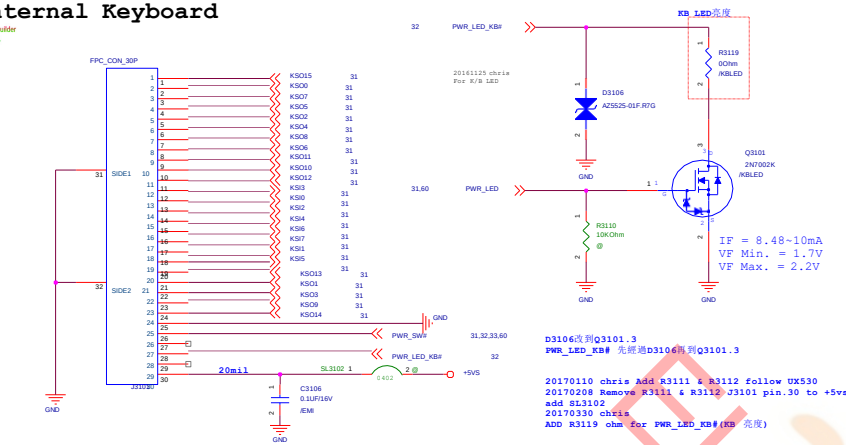


LPC Debug Port

20151225
12G183301208-->12018-00102700
更換Debug port 樣式 FFC 正/正

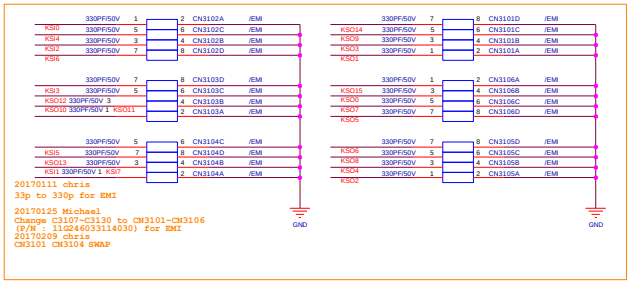


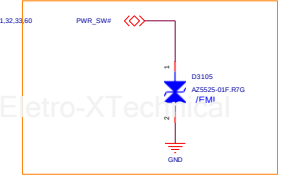
Internal Keyboard



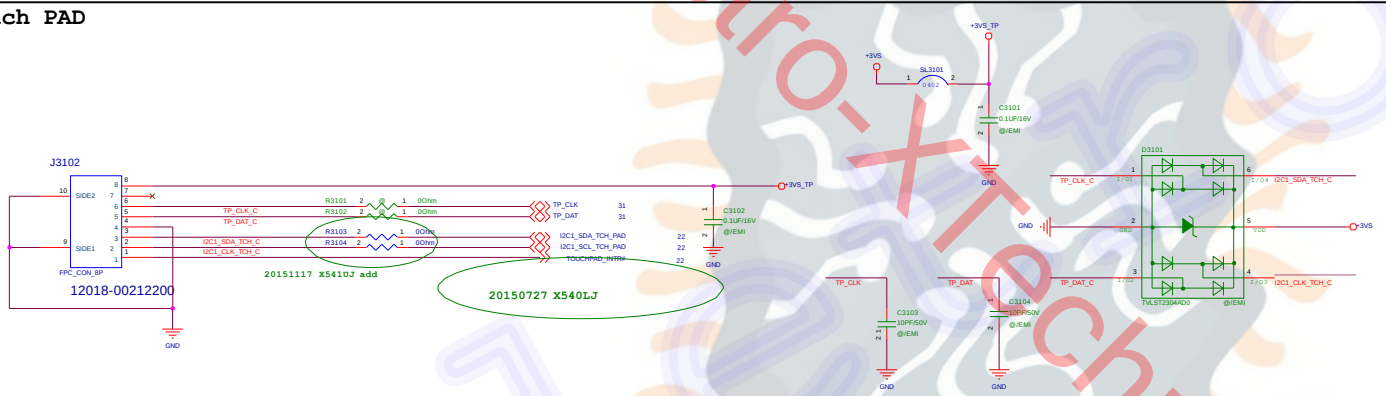
20170629 Brian
Change J3101 from 12018-00200900 to
12018-00380700 (X405).

EMI



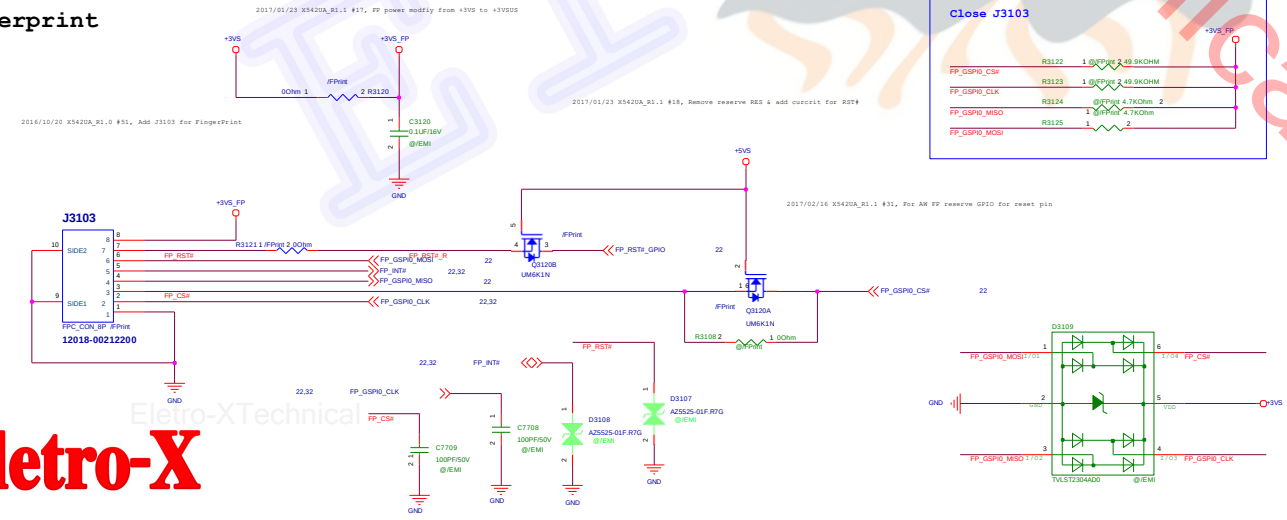


Touch PAD



PIN NO.	PIN DEFINE
1	VDD_3.3V
2	NC
3	D-
4	D+
5	GND
6	I2C_DATA
7	I2C_CLK
8	TOUCH -INT

Fingerprint

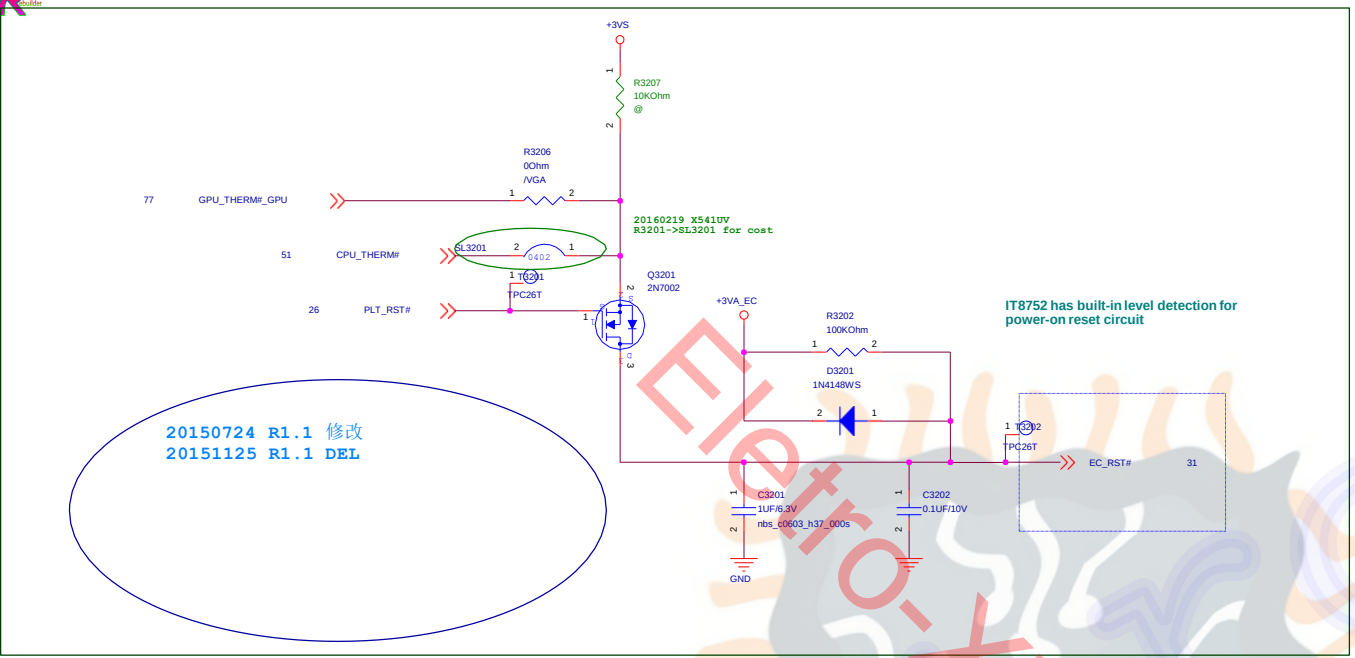


CN1 PIN NO.	CN1 PIN DEFINE	CN2 PIN NO.	CN2 PIN DEFINE
1	VDD_3.3V_TP	1	VDD_3.3V_FP
2	GND	2	FP_RSTN
3	PS2_CLK	3	FP_MOSI
4	PS2_DATA	4	FP_INTN
5	GND	5	FP_MISO
6	SDA	6	FP_CSN
7	SCL	7	FP_SCK
8	INT	8	GND

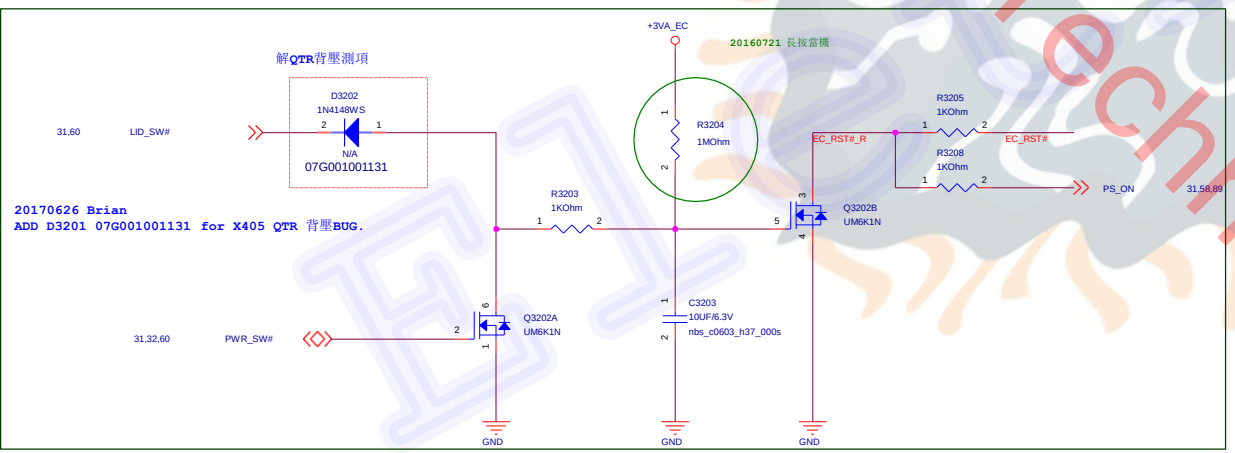
Eletro-X

Project Name	X407UA/UV	
Title :	EC-IT8995_KB,TP	
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen

Thermal Policy



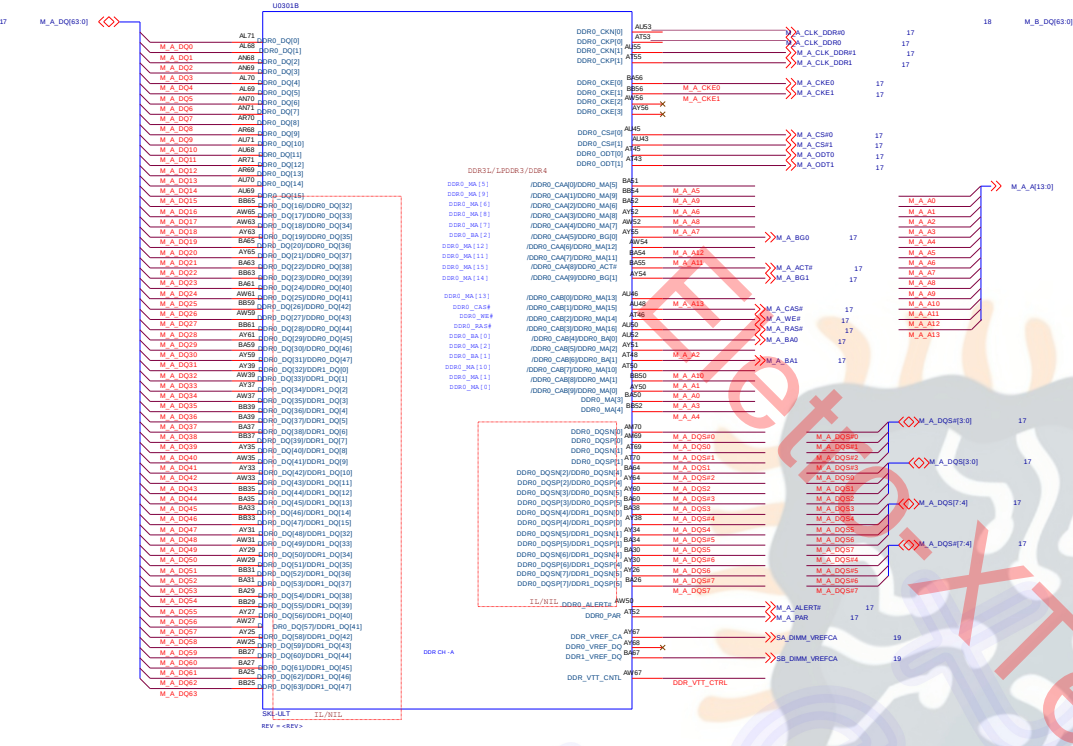
battery embedded (press pwr_sw 10sec, then reset ec)



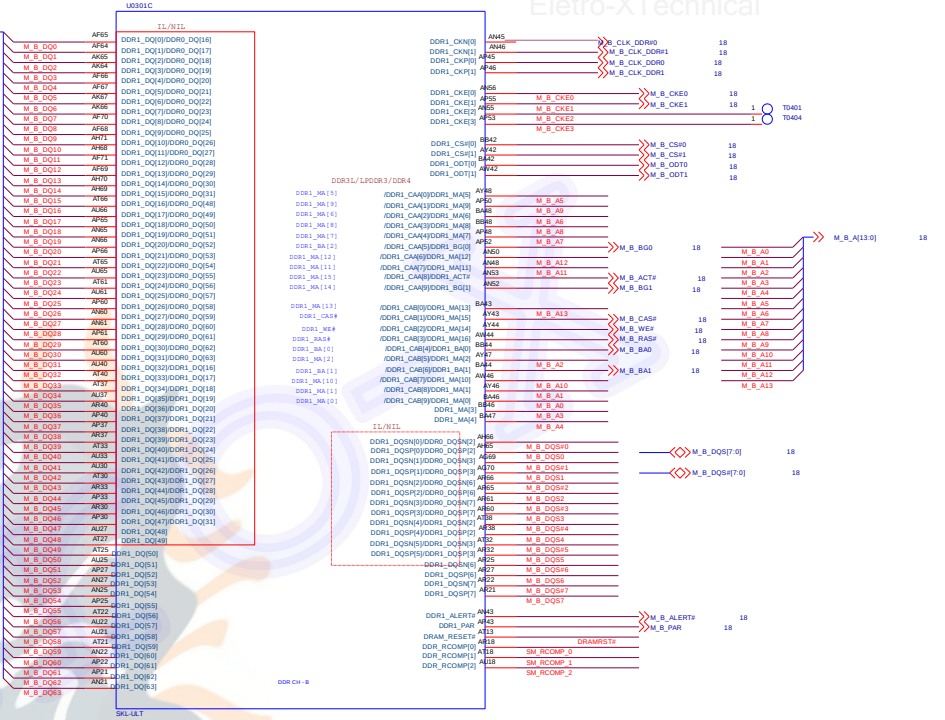
<variant_name>

ASUSTeK COMPUTER INC. NB4	Title : 32_RST_Reset Circuit	
	Engineer: Brian Chen	
Size: B	Project Name: X407UA/UV	Rev: R1.0
Date: Wednesday, March 07, 2018	Sheet 33 of 102	

For SO-DIMM (A)

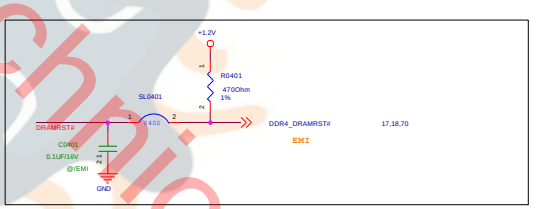


For SO-DIMM (B)



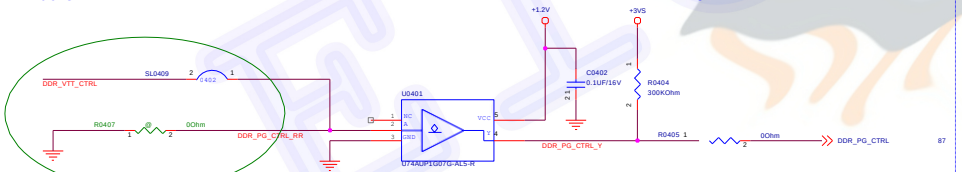
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

DDR_Vref_DQ = Not in use in DDR4,
DDR1_Vref_DQ = DDR4_CA_ch1,
DDR_Vref_CA = DDR4_CA_ch0



DDR4 COMPENSATION SIGNALS

VTT Enable



20160216 X541UV R1.1
R0407->R7739,R0408->R7740,R0409->R7741 20160218 X541UV R1.1
R0409->SL0409 for cost

20171204 Brian
Change U0401 from 06G004259030 to 06004-00620000.

Table 4-44. SKL U DDR4/-RS x8 Memory Down Routing Guideline (Sheet 3 of 3)

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω) DIff	Target Impedance (Ω) Single Ended	Target Impedance (Ω) Tolerance (%)	Min Trace Spacing (mils) DIff	Min Trace Spacing (mils) Group	Min Trace Spacing (mils) Group to Group(2W)	Min Trace Spacing (mils) Byte (3W)	Max (mils) Length Region	Max (mils) Length Breakout	Max (mils) Length Total	R (1±1%) (1/4")	Notes
RCOMP[0]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	121	
RCOMP[1]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	80.6	
RCOMP[2]	M	MS/SL/DSL	VSS	4	12-15					13	13		500		500	100	

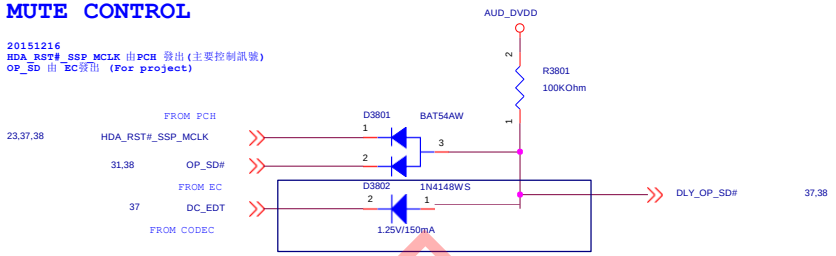
BOM

Project Name	X507UA/UV
Title :	CPU_DDR3
Size	
Dept.:	Engineer:

20160530
1. Del R3833 & Add D3801
2. AUD_DVDD_IO--->AUD_DVDD

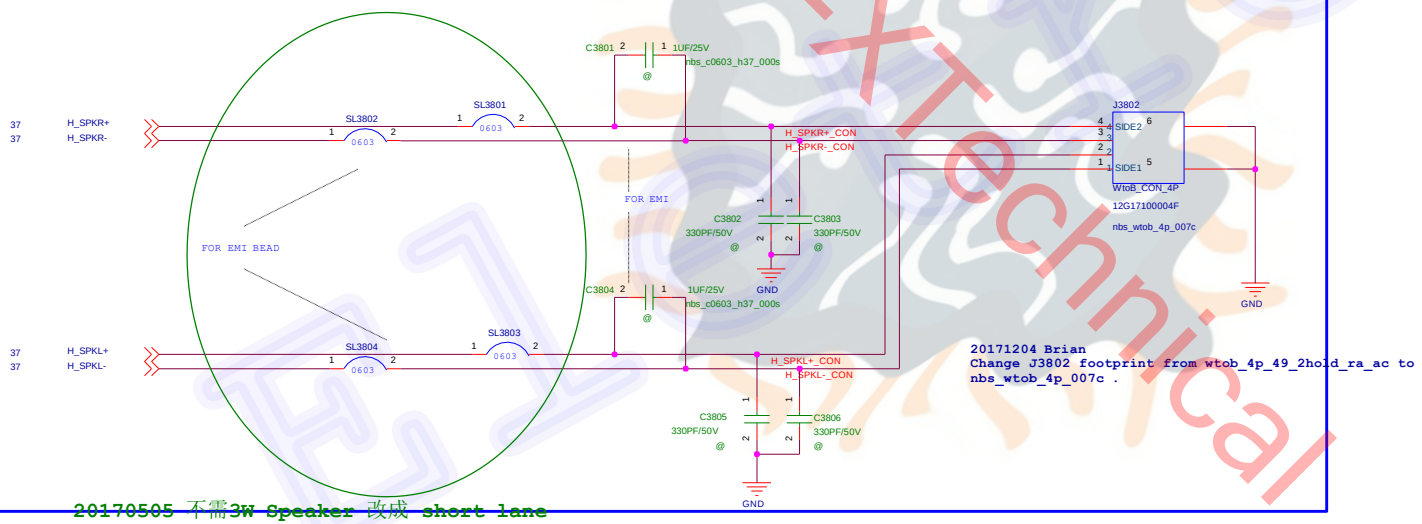
MUTE CONTROL

20151216
HDA_RST#_SSP_MCLK 由PCH 發出(主要控制訊號)
OP_SD 由 EC發出 (For project)



20171020 Brian
Change R3833 to D3802 for De-pop.

Trace width for
H_SPKL+_O/H_SPKL-_O/H_SPKR+_O/H_SPKR-_OSpeaker
Speaker :4 ohm : 40mil ;8 ohm : 20mil



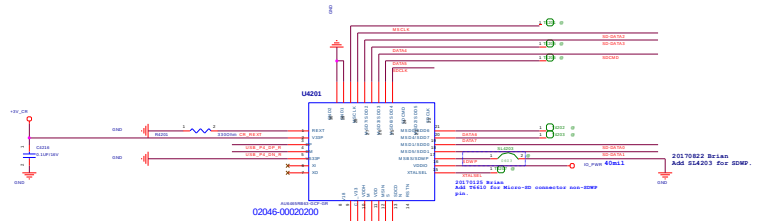
20171204 Brian
Change J3802 footprint from wtob_4p_49_2hold_ra_ac to nbs_wtob_4p_007c .

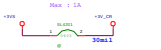
~~20170505 不需3W Speaker 改成 short lane~~

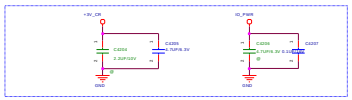
SD Card Reader

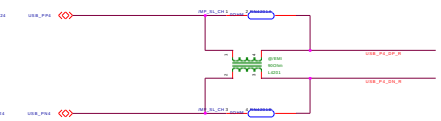
AU6465

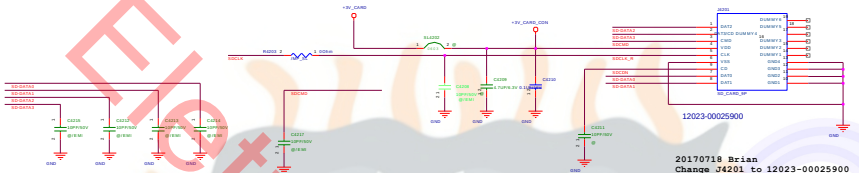
	mode	Vin(V)	Iin (mA)	mW
AU6465 (Enable Power saving mode)	Suspend with card	3.3V	0.33	1.1
	Suspend without card	3.3V	0.14	0.46
	Idle with card	3.3V	32.8	108.24
	Idle without card	3.3V	0.14	0.46
	operating	3.3V	119	392.7
Use SanDisk SDHC 8G card (Extreme Pro)				





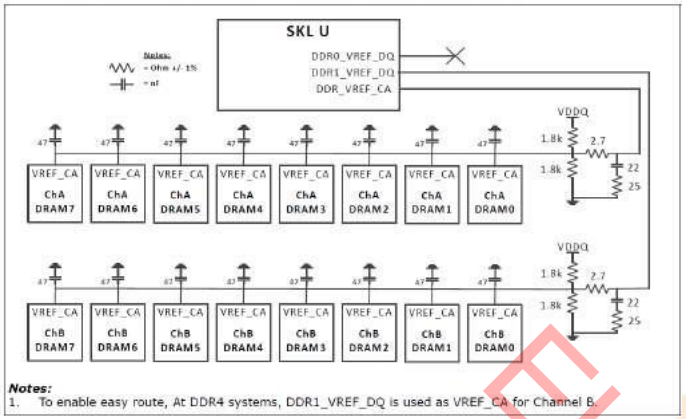






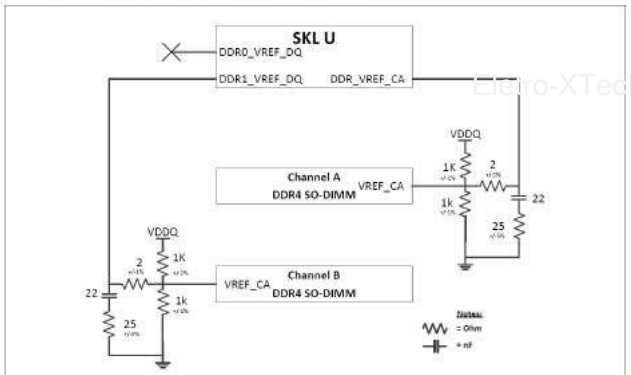
ASUS	Project Name: X407UA/UV		Rev: R1.0
Title : CARD READER CONNECTOR			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet: 22 of 103		

Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview



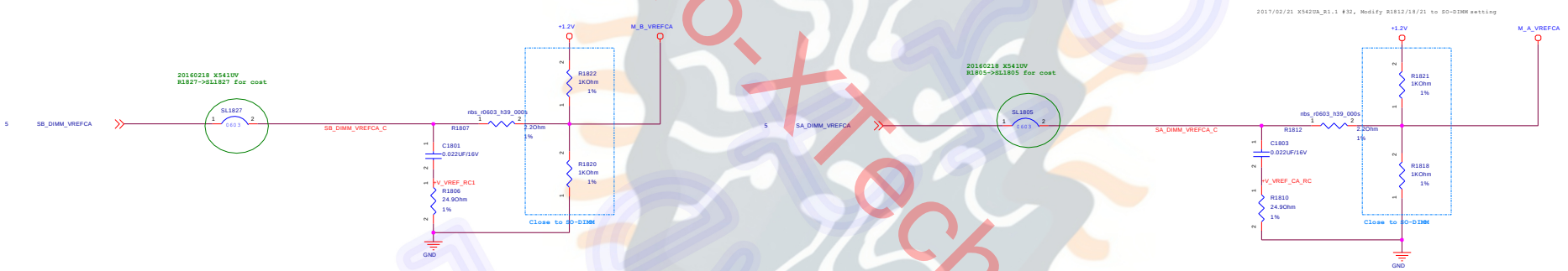
Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

All Vref trace must be 20 mils width



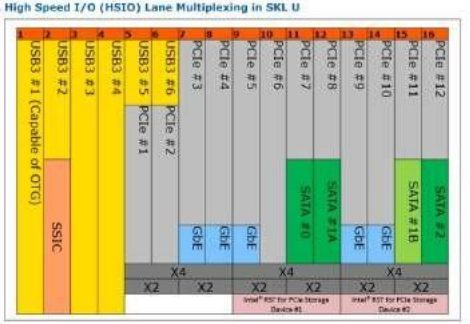
USB 2.0		Mapping	USB 3.0	
1	USB 2.0 Port		1	USB 3.0 Port0
2	USB 2.0 Port		2	
3			3	
4	Cardreader		4	
5				
6	CAMERA			
7				
8	WLAN / BT combo			

	USB2.0	USB3.0	OC	LOCATION	POWER
X540UJ X541UV	1	1	0	USB3	+5V_USB_CON1
	2	2	1	USB3.1 TYPE-C	+USB_C_VBUS
		3	1	USB3.1 TYPE-C	+USB_C_VBUS
	3			USB2.0	+5V_USB_CON1
	4				
	5				
	6			CAMERA	+3V_CAM
	7			TOUCH PENAL	+5VSUS
	8			WLAN / BT combo	+3VS_WLAN
	9				
	10				

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	DGPU		Port0
PCIE 2	DGPU		
PCIE 3	DGPU		
PCIE 4	DGPU		
PCIE 5	N/A		
PCIE 6	WLAN		Port5
PCIE 7/SATA 0	HDD		
PCIE 8/SATA 1A			
PCIE 9	SSD_PCIE3		
PCIE 10	SSD_PCIE2		
PCIE 11/SATA 1B	SSD_PCIE1		
PCIE 12/SATA 2	SSD_PCIE0	SSD_SATA	

SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A OPTION PCIE
PORT 3	SSD OPTION PCIE

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U



20170505 X540UPR2 DEL Type C

20160218 X541UV R2321 unstuff for cost

USB2_ID R2321 PD 1K: OTG PD 0ohm: non OTG

20170720 Brian Remove SL2321 for EMI Xtal 0ohm space.

20160218 X541UV R2301 unstuff for cost R2302 unstuff for cost R2303 unstuff for cost 20160603 X540UP R2301 R2302 R2303 1ff

UX303C1 0520

20171221 Brian Change SATA2_DEVSLP from port1 to port2.

20170720 Brian Change R2312 to unmount.

1007-9 Dean

Eletro-X

BOM

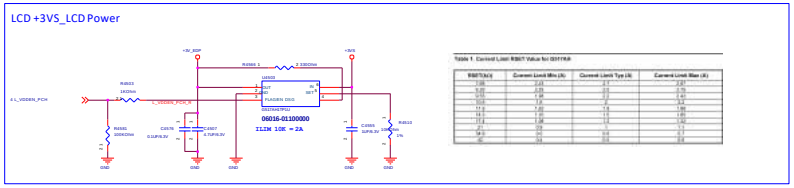
ASUS X407UA/UV

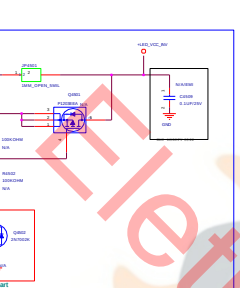
Title : CPU_PCH_PCIE,USB,SATA

Size C | Dept.: ASUSTeK COMPUTER INC. | Engineer: Brian Chen

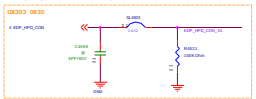
Date: Wednesday, March 07, 2018 | Sheet 24 of 102

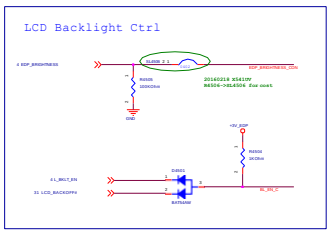
eDP (LVDS) Panel

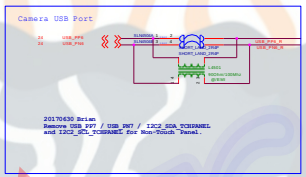


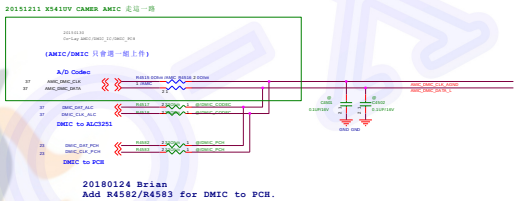


CHECK HPD WITH P20

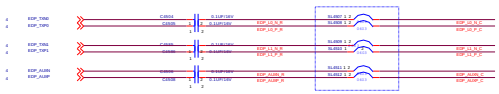








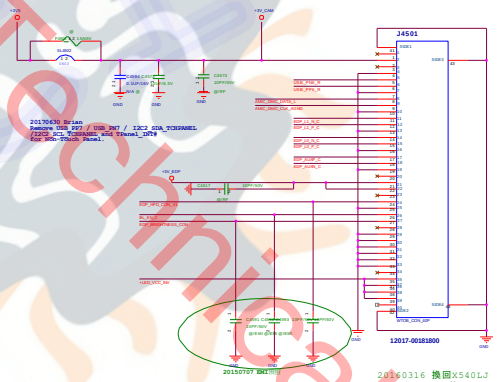
eDP Panel differential signals

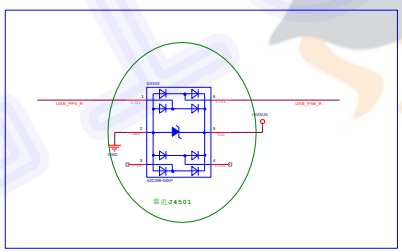


20170705 Brian
Change RM4501/RM4502/RM4503 footprint to
temp_T_001805 for relay ECMF.

20170707 Brian
Change RM4501/RM4502/RM4503 footprint to
1005Z0200306020 for relay ECMF.

20170714 Brian
Remove
RM4501/RM4502/RM4503/L4504/L4509/L4510
for Non-CMF relay





EC 8585

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

Power

20160104 X541UV del +1.8VS

20160218 X541UV
R3025->8L3025 for cost

2013/03/15 Paul :For EMI reserved

ITE Version	ASUS P/N
IT8995E/AX	06037-00050400
IT8995E-128/CX	06037-00050500

06037-00050700

2014/02/06-3

X541UA MODIFY

R1.0-6

R1.2-8

for X455
internal battery always PD

EMI solution

UX303 1002

UX303 0826

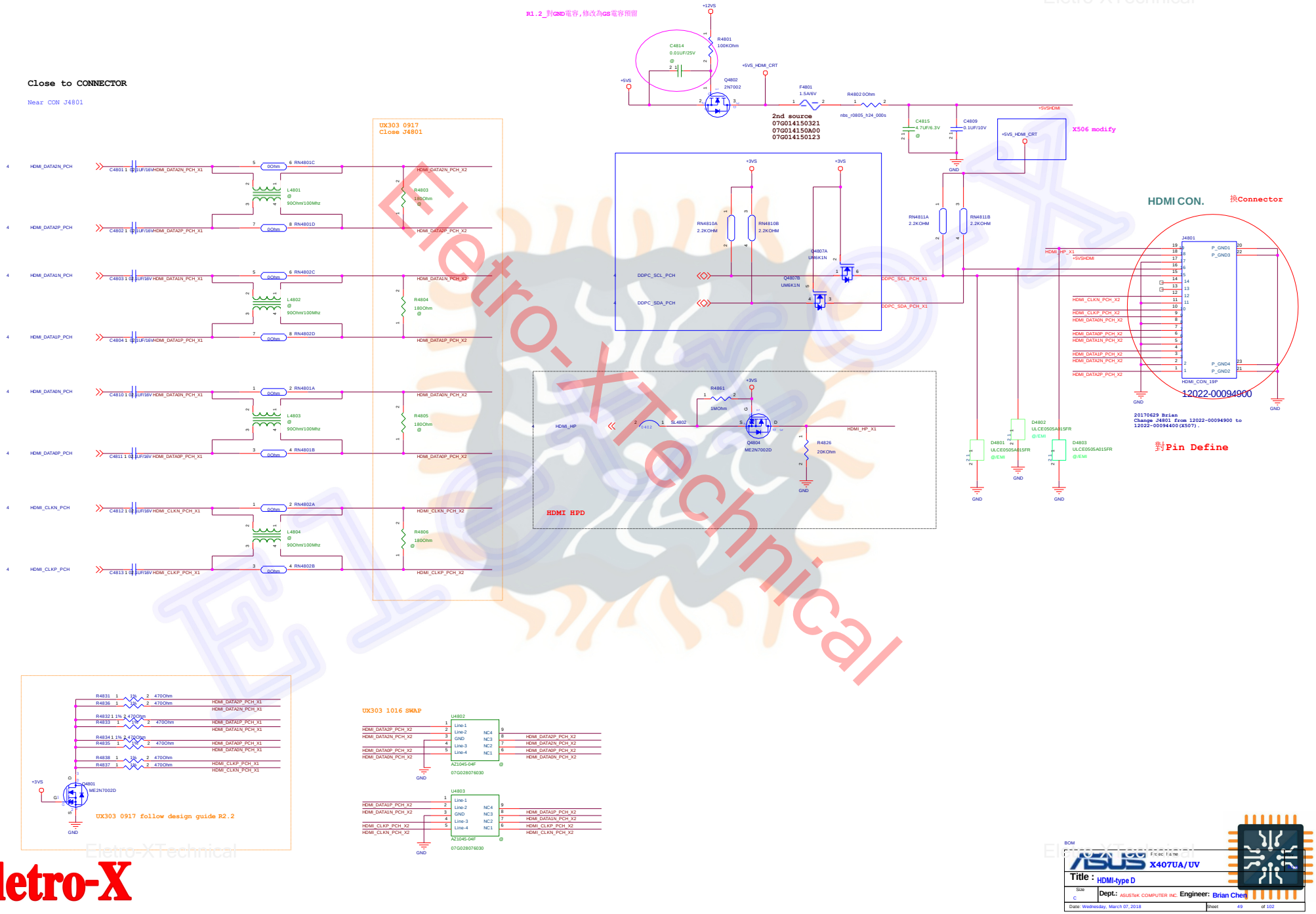
UX303 1202 EMI

Project Name X407UA/UV

Title : IT8995E-128/CX

Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen

HDMI type-A

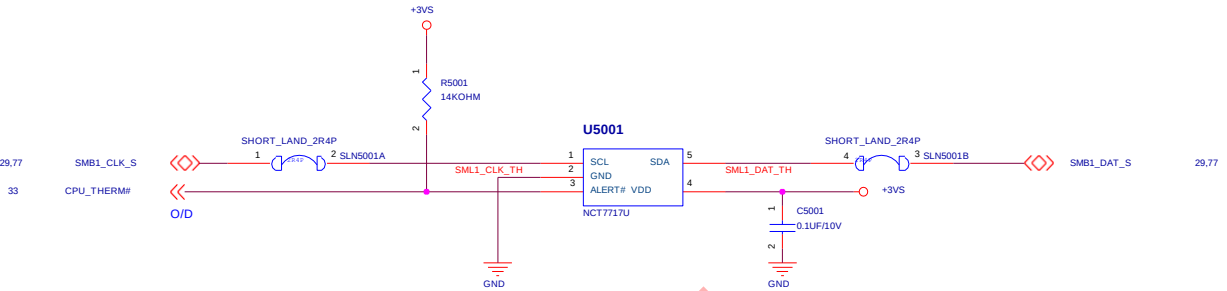


Eletro-X

Title : HDMI-type D			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 49 of 102		

ASUS X407UA/UV

CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

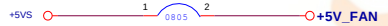
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

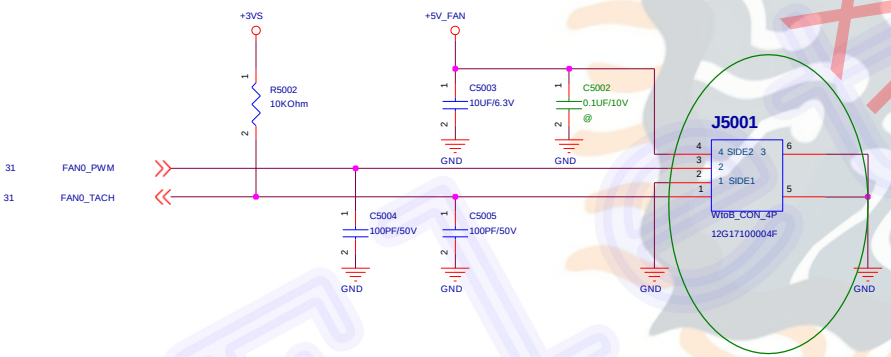
PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

DC FAN Control





20160316 換回X540LJ

<Variant Name>

ASUSTeK COMPUTER INC. NB3

Title : 50_FAN_Thermal Sensor

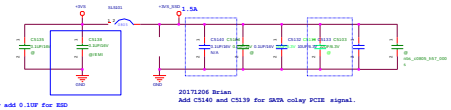
Engineer: Brian Chen

Size	Project Name	Rev
B	X407UA/UV	R1.0

Date: Wednesday, March 07, 2018 Sheet 51 of 102

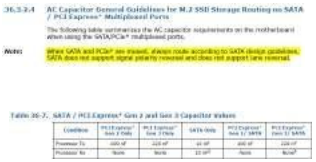
SSD CONN.
PCIE colay SATA signals

0310-1 Dean
0314-2 Dean

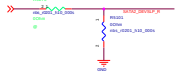


6/8 Jacky add 0.1UF for ESD

20171206 Brian
Add CS140 and CS139 for SATA colay PCIE signal.



SATA DEVSLP.



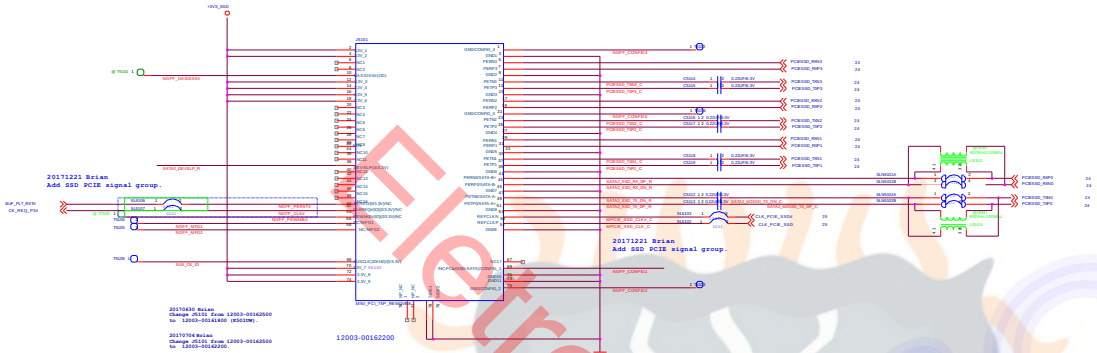
1007-11 Dean

PCIE Wake-up.

20170628 Brian
Remove PCIE Wake-up schematic select for SSD SATA only.

For PCIE/SATA select.

20171206 Brian
Add PCIE/SATA schematic select for SSD SATA colay PCIE.



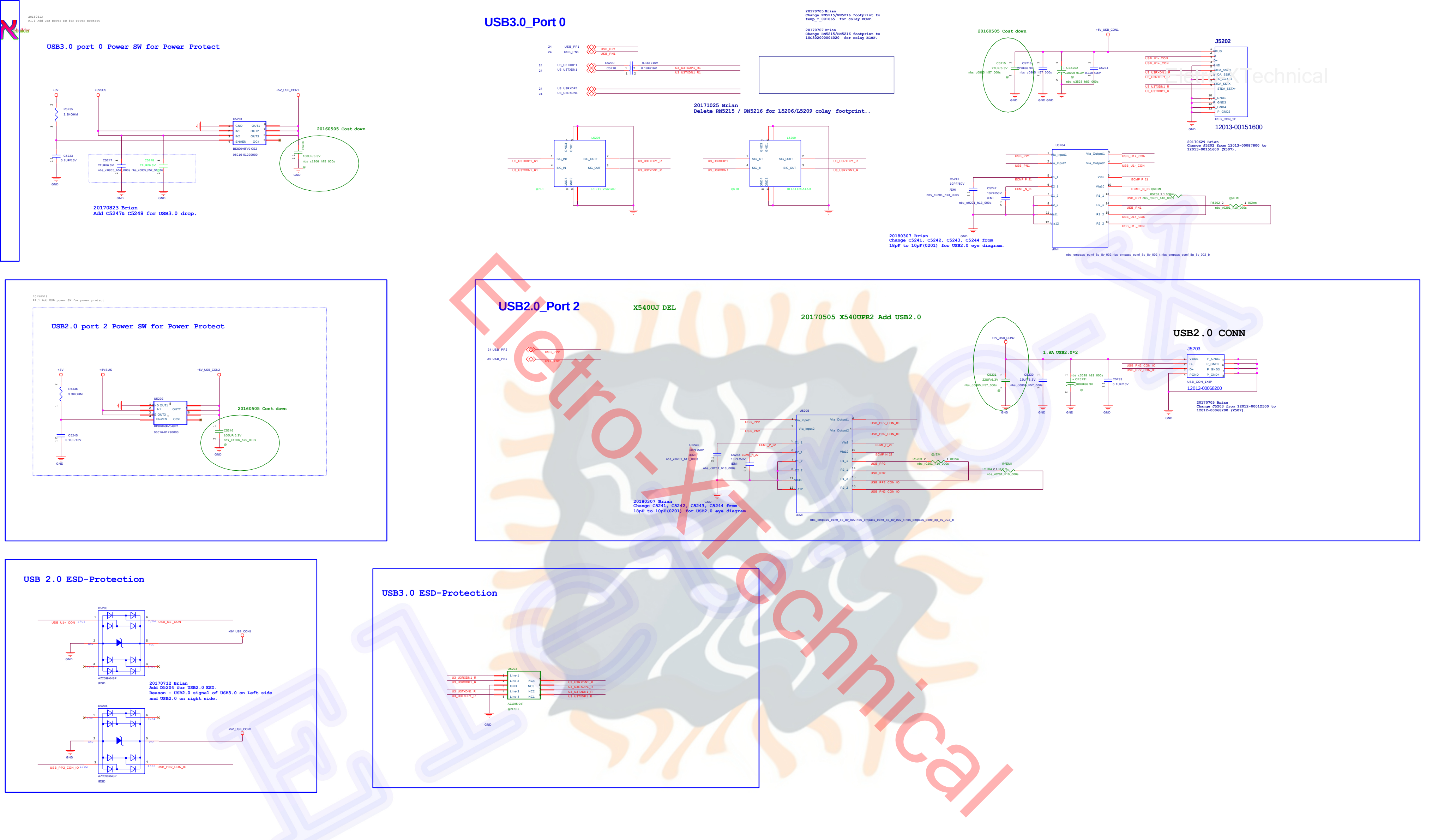
20171221 Brian
Add SSD PCIE signal group.

20170630 Brian
Change JS101 from 12003-00162500
to 12003-00161400 (6531HW).

20170704 Brian
Change JS101 from 12003-00161400
to 12003-00162200.

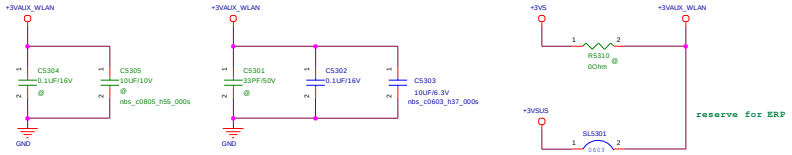
12003-00162200

20171221 Brian
Add SSD PCIE signal group.

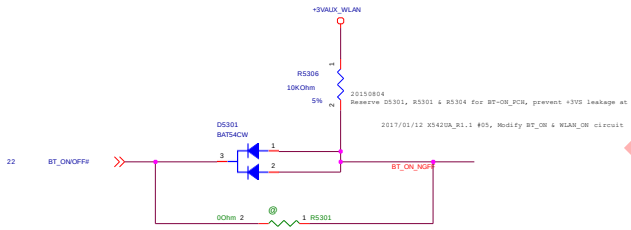

USB3.0_Port 0
USB3.0 port 0 Power SW for Power Protect
20160505 Cost down
20170823 Brian
Add C5247& C5248 for USB3.0 drop.
20170705 Brian
Change RN5215/RN5216 footprint to temp_T_001865 for colay EC9F.
20171025 Brian
Delete RN5215 / RN5216 for L5206/L5209 colay footprint..
J5202
12013-00151600
20170629 Brian
Change J5202 from 12013-00087800 to 12013-00151600 (X507).
20180307 Brian
Change C5241, C5242, C5243, C5244 from 18pF to 10pF(0201) for USB2.0 eye diagram.
USB2.0 port 2 Power SW for Power Protect
20160505 Cost down
USB2.0_Port 2
X540UJ DEL
20170505 X540UPR2 Add USB2.0
USB2.0 CONN
J5203
12012-00068200
20170705 Brian
Change J5203 from 12012-00012500 to 12012-00068200 (X507).
20180307 Brian
Change C5241, C5242, C5243, C5244 from 18pF to 10pF(0201) for USB2.0 eye diagram.
USB 2.0 ESD-Protection
20170712 Brian
Add D5204 for USB2.0 ESD.
Reason : USB2.0 signal of USB3.0 on Left side and USB2.0 on right side.
USB3.0 ESD-Protection

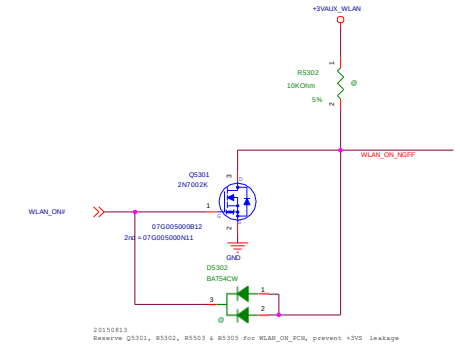
Project Name	X407UA/UV	Rev R1.0
Title : USB3.0 + 2.0 CONN.		
Dept.: ASUSTeK COMPUTER INC	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 53 of 102	

0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707
=> 120OHM/2A 09G013120802



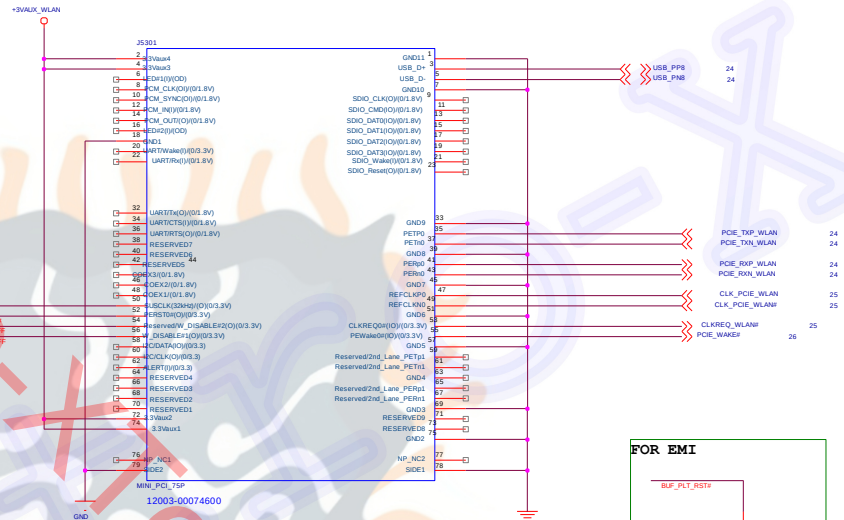
0309-11 Dean_cost check keypart list上的WLAN均無+1.5V的需求
=> unstuff C5304, C5305



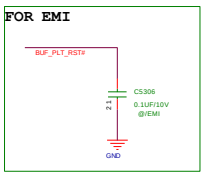


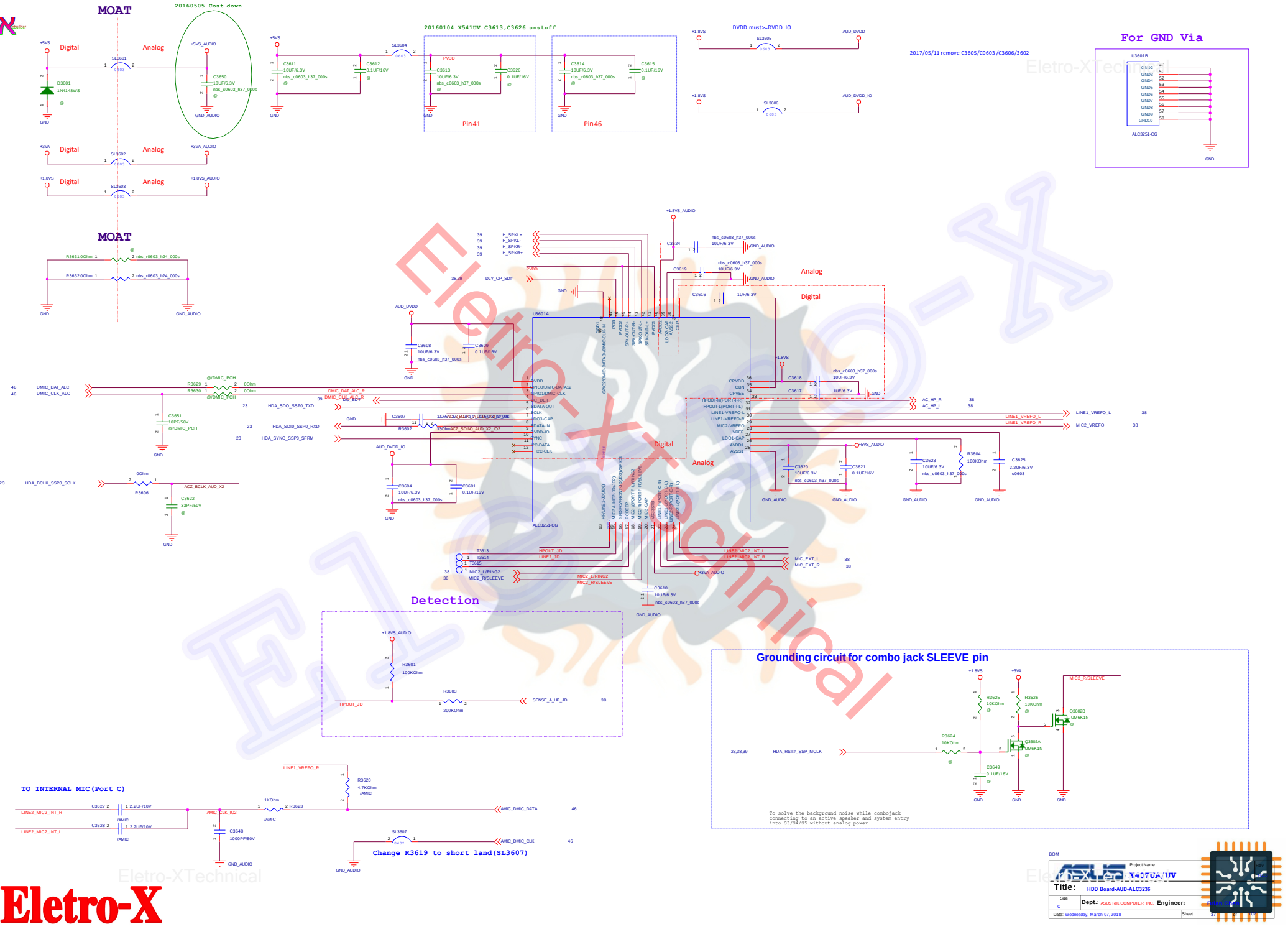
2017/05/11 BT/WLAN ON OFF Follow X452UQ PR

2017/05/11 Modify R5309 to Shortland SL5309



20170704 Brian
Change J5301 from 12003-00076900 to 12003-00074600.

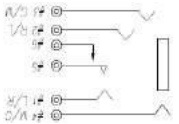


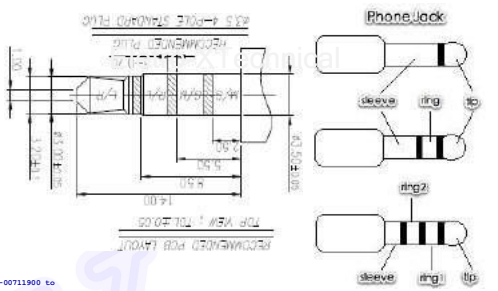

MOAT
20160505 Cost down
Digital
Analog
20160104 X541UV C3613,C3626 unstuff
Pin41
Pin46
DVDD must>=DVDD_IO
2017/05/11 remove C3605/C0603 /C3606/3602
For GND Via
ALC3251-CG
Detection
Grounding circuit for combo jack SLEEVE pin
To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power
TO INTERNAL MIC(Port C)
Change R3619 to short land(SL3607)
Eletro-X
Eletro-XTechnical
Title: HDD Board-AUD-ALC3236
Project Name X407UA/UV
Dept.: ASUSTeK COMPUTER INC.
Engineer:
Date: Wednesday, March 07,2018

Universal Jack (Normal open type)

R1.4. Item 12.
Add 4 pole headset jack normal open type for project demand.

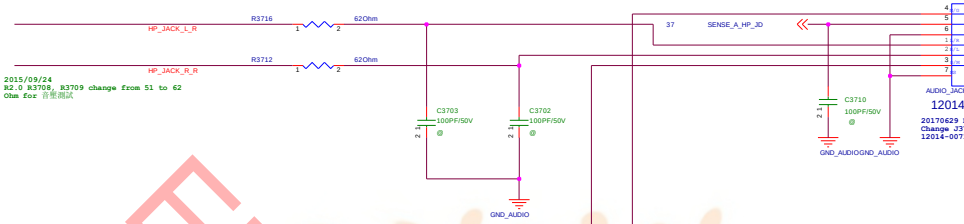
- 尺寸：一般分三種規格，2.5mm、3.5mm、6.35mm。
- 種類：一般分也三種規格，TS 端子 (Mono)、TRS 端子 (Stereo)、TRRS 端子 (Stereo + Mic/Video)。





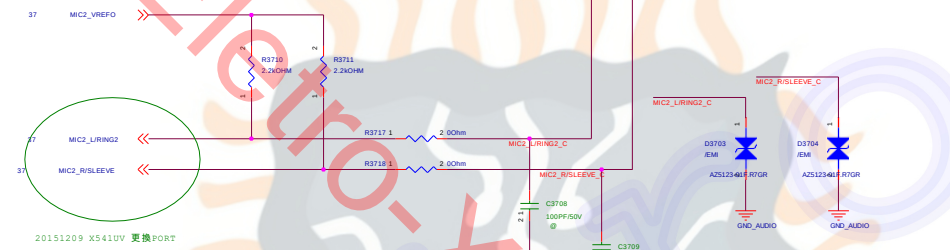
R1.4. Item 13.
Recommand the HP damping resistance 56 ohm for CB certification.
Depend on your project, you can change the resistance value to meet CB certification (under 150mV), best chioce is between 140mV~150mV section.

Global Headset
Normal Open
Supported iPhone/Nokia headset, headphone



2015/09/24
R2.0 R3708, R3709 change from 51 to 62 Ohm for 音重測試

20170629 Brian
Change J3701 from 12014-00711900 to 12014-00716600 (X507).



20151209 X541UV 更換PORT

20180307 Brian
Add D3703/D3704 for EMI MIC burn issue.

R0.93. Item 3.
Realtek suggest PCB trace width of RING2 & SLEEVE at least 40 mils.

CITA:國際標準

Apple iPhone/HTC/小米 的 Phone Jack 定義：

Apple	iPad (Stereo)	iPod (Stereo)	iPhone (Mic)	iPod (AV)
1. Tip	Left channel	Leftchannel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mic	Video

OMTP:國家標準

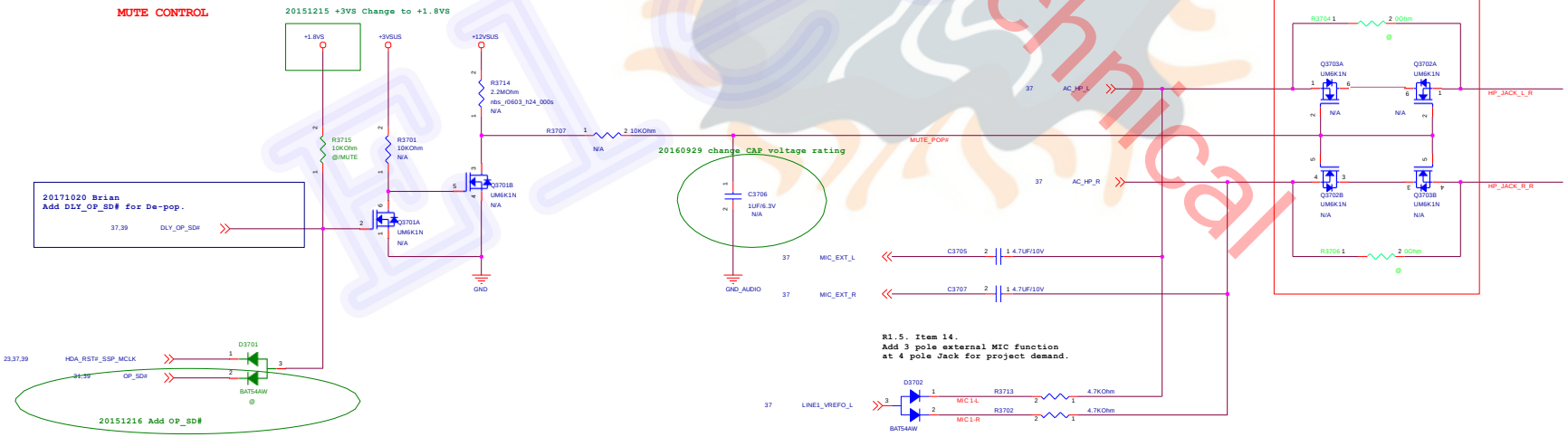
Nokie Type 的 Phone Jack 定義：

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel

耳機pop noise mute線路

MUTE CONTROL

20151215 +3VS Change to +1.8VS



Eletro-X

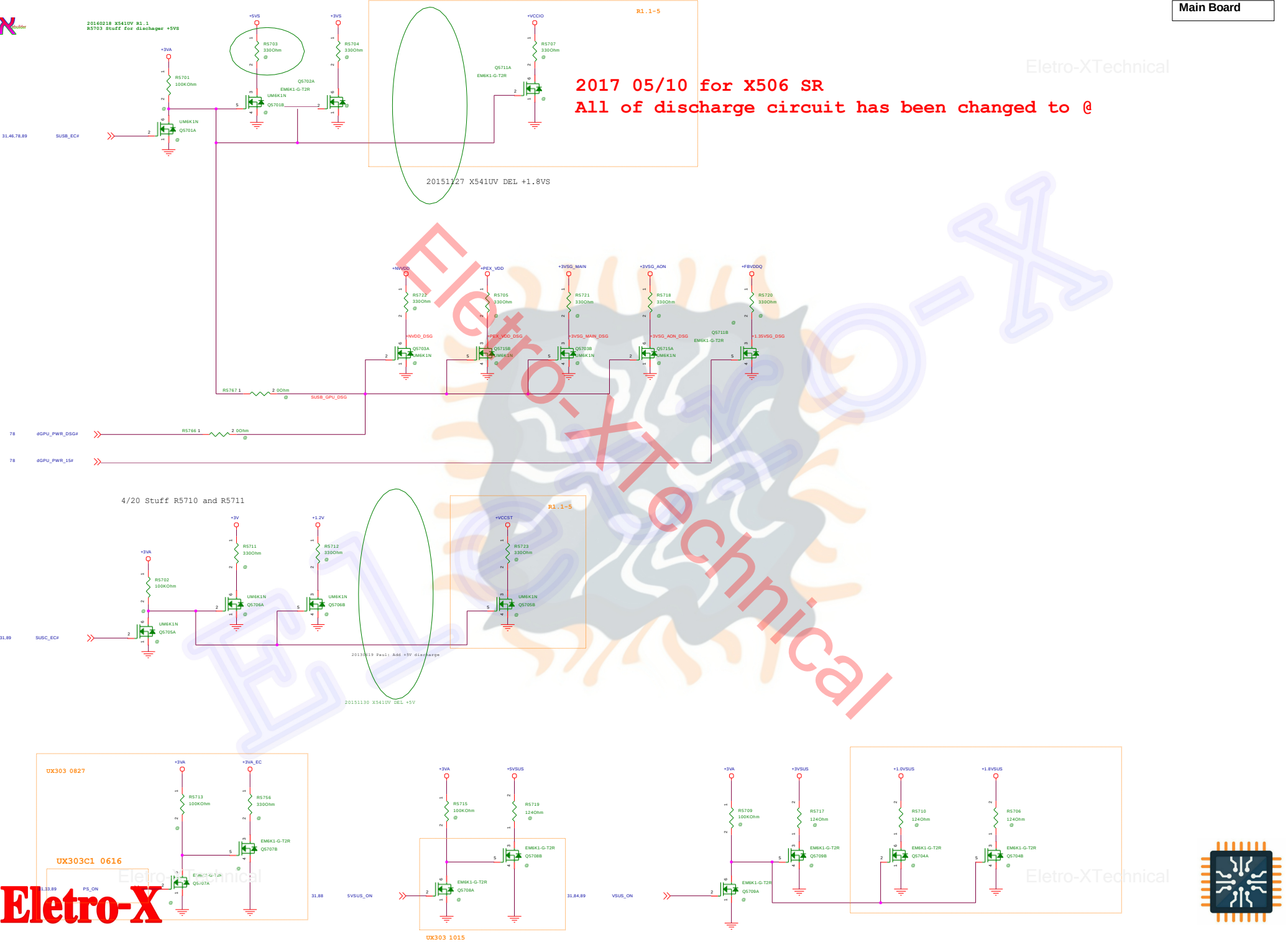
BOM

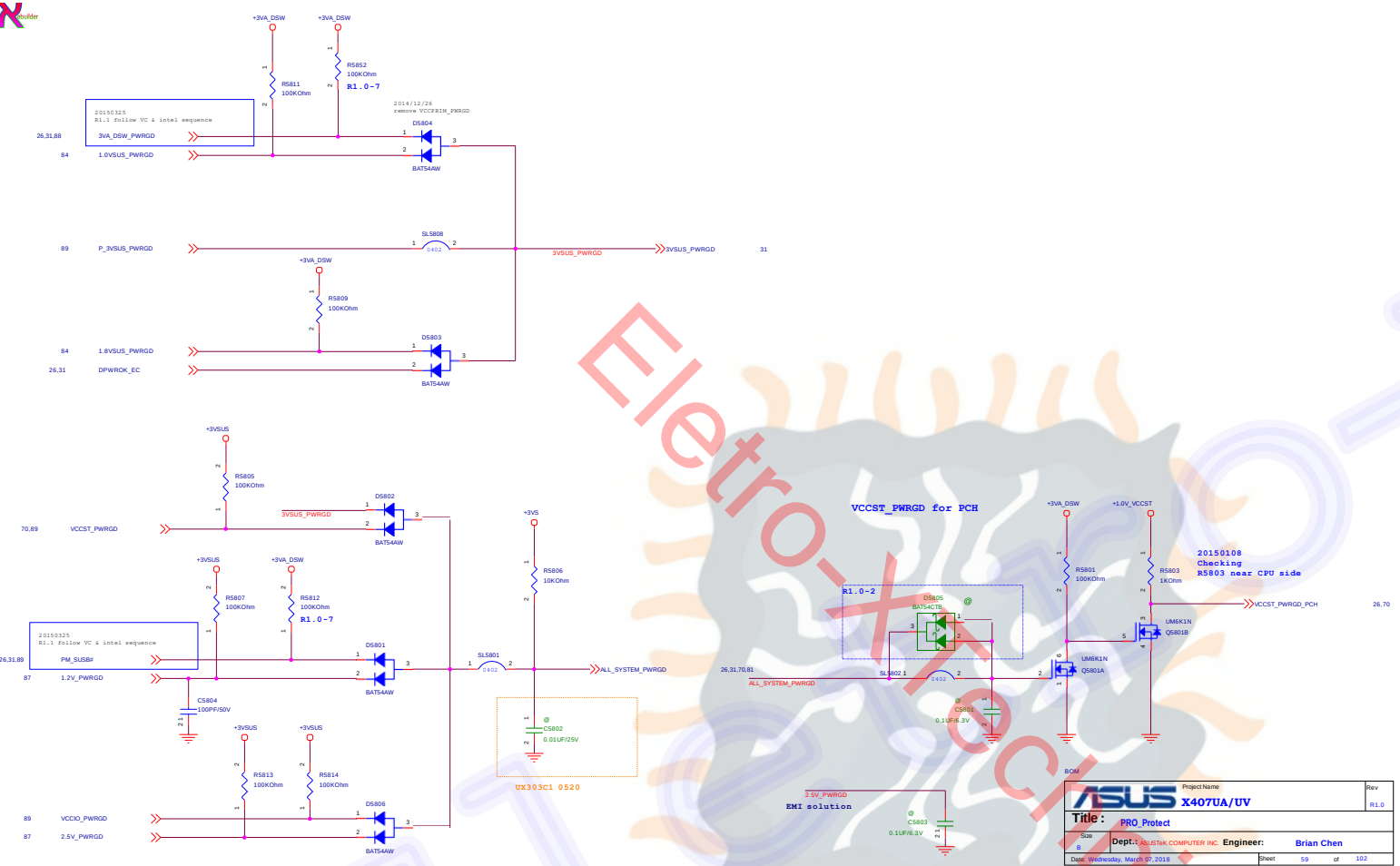
Project Name: X407UA/UV

Title : IO Board-Audio Jack

Size: C

Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen

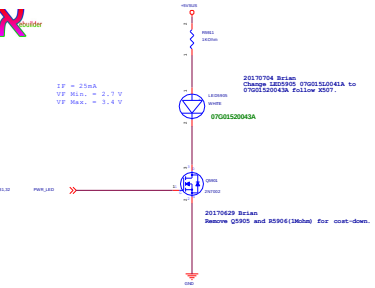


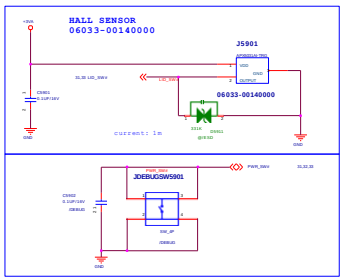


POWER LED

WIRELESS/ BT LED

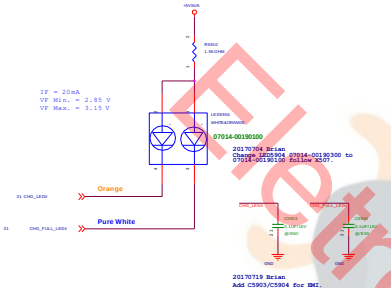
CAP Lock LED





LED indicator

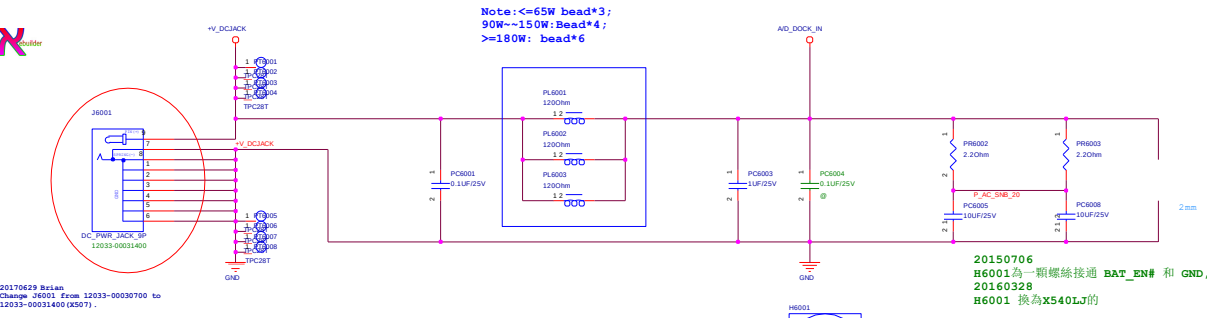
Charger LED



Title : 5E Power & WiFi & CAP LED

Engineer: Brian Chen

X407UA/UV



20170629 Brian
Change J6001 from 12033-00030700 to 12033-00031400(X507).

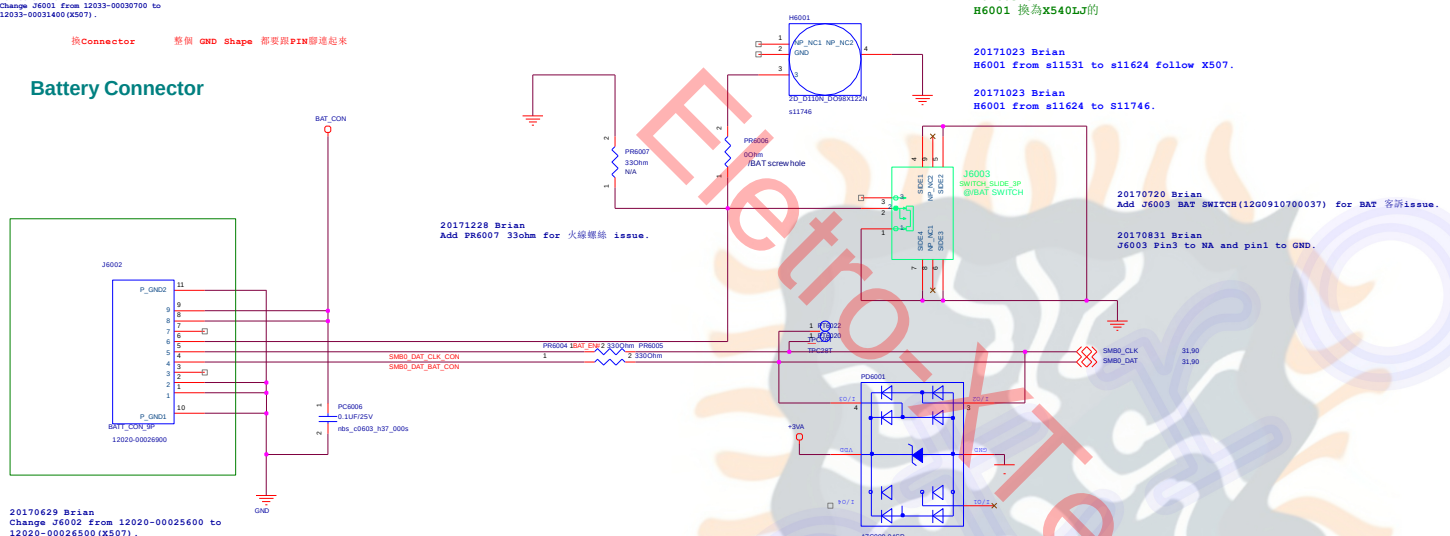
20150706
H6001為一顆螺絲接通 BAT_EN# 和 GND,電池才開始送電
20160328
H6001 換為X540LJ的

換Connector 整個 GND Shape 都要跟PIN腳連起來

20171023 Brian
H6001 from s11531 to s11624 follow X507.

20171023 Brian
H6001 from s11624 to S11746.

Battery Connector



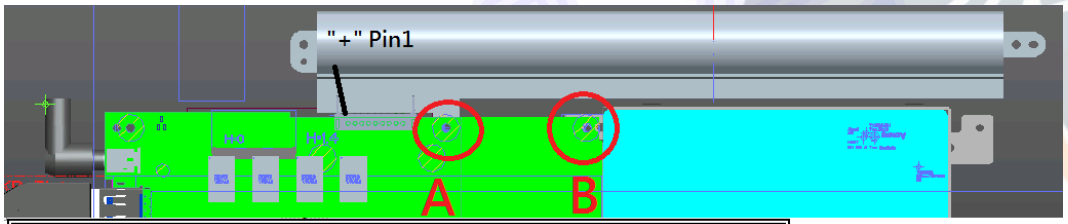
20171228 Brian
Add PR6007 33ohm for 火線螺絲 issue.

20170720 Brian
Add J6003 BAT SWITCH(12G0910700037) for BAT 客訴issue.

20170831 Brian
J6003 Pin3 to NA and pin1 to GND.

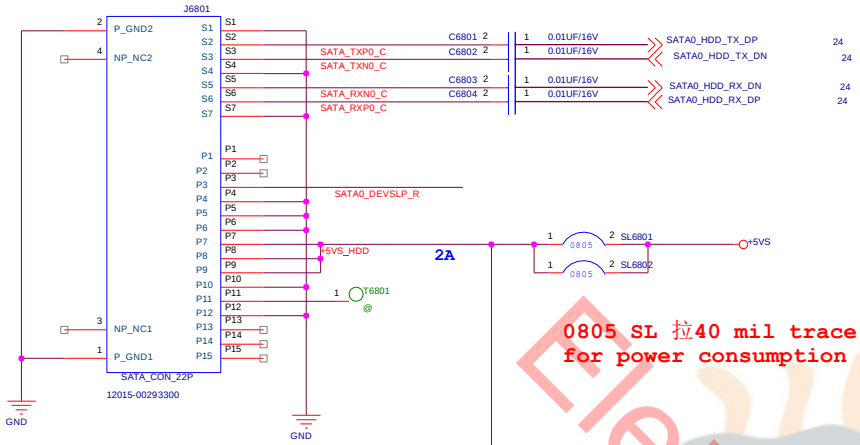
20170629 Brian
Change J6002 from 12020-00025600 to 12020-00026500(X507).

20170718 Brian
Change J6002 from 12020-00025600 to 12020-00026700.

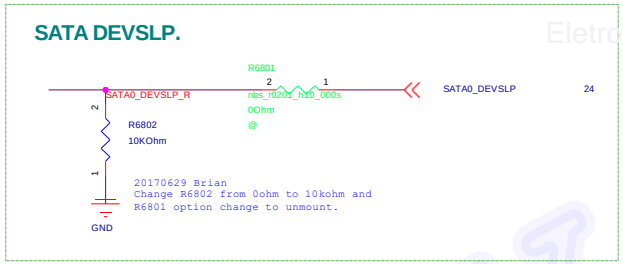


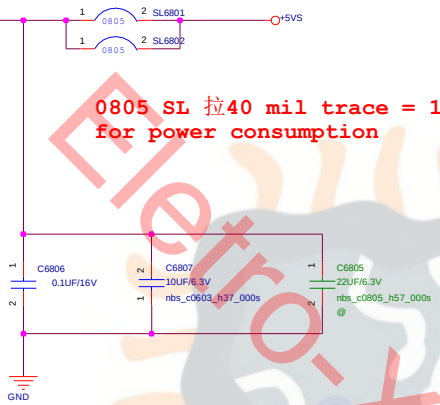
Pin Seq.	Name	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	NC		
4	EN#	External charge & discharge Mosfet control pin.	SYSTEM Connection to GND for charge & discharge (Enable Function)
5	SMBC	Serial clock input	SMBC
6	SMBD	Serial data input	SMBD
7	NC		
8	P-	Battery pack negative terminal.	GND
9	P-	Battery pack negative terminal.	GND

SATA HDD

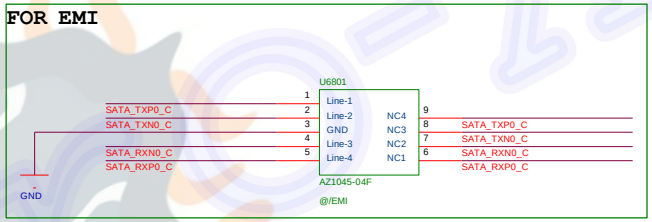


2nd source: 12015-00012300



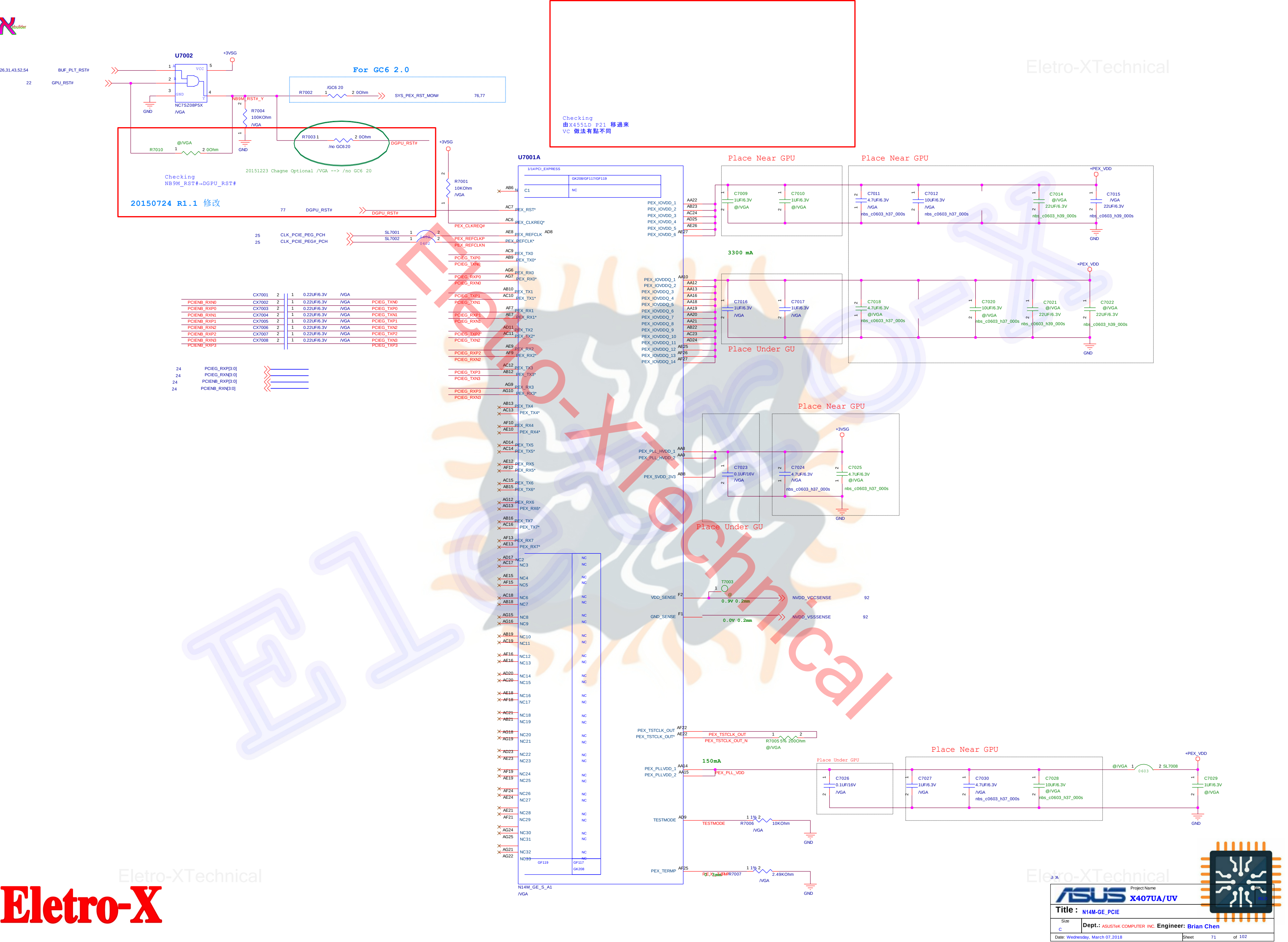


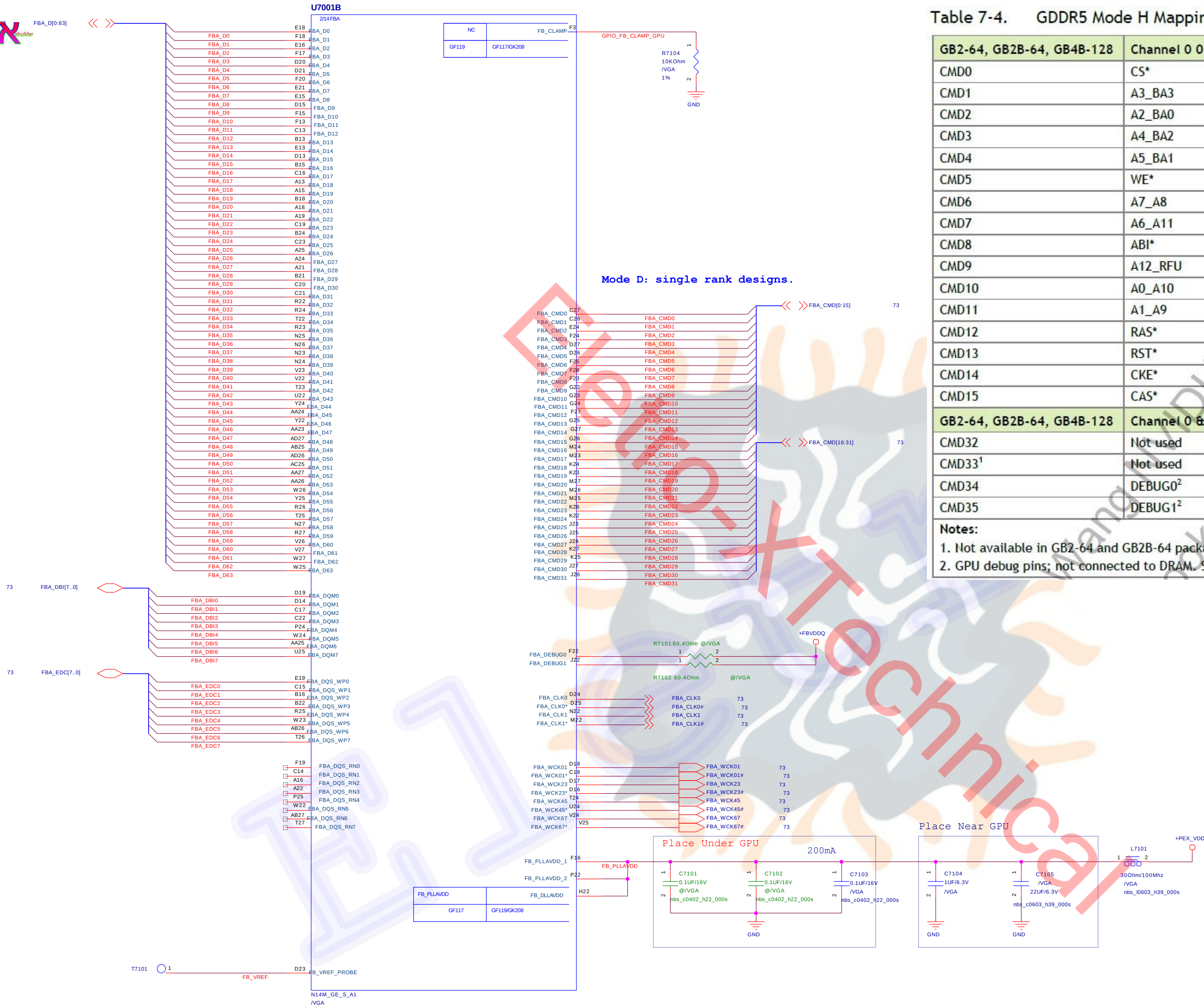
0805 SL 拉40 mil trace = 1A
for power consumption



BOM

ASUS	Project Name: X407UA/UV	Rev: R1.0
Title : B TO B CONNECTOR		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 69 of 102	


U7002
NC7SZ08P5X
/VGA
BUF_PLT_RST#
GPU_RST#
+3VSG
GND
For GC6 2.0
R7002
/GC6 20
0Ohm
SYS_PEX_RST_MON#
76,77
NB9M_RST#_Y
R7004
100KOhm
/VGA
R7003
/no GC620
DGPU_RST#
R7010
@/VGA
0Ohm
Checking
NB9M_RST#→DGPU_RST#
20150724 R1.1 修改
20151223 Chagne Optional /VGA --> /no GC6 20
R7001
10KOhm
/VGA
U7001A
1/14 PCI_EXPRESS
GK208/GF117/GF119
DGPU_RST#
PEX_RST*
PEX_CLKREQ*
PEX_REFCLK
PEX_REFCLK*
CLK_PCIE_PEG_PCH
CLK_PCIE_PEG#_PCH
SL7001
SL7002
PCIEG_RXP[3:0]
PCIEG_RXN[3:0]
PCIENB_RXP[3:0]
PCIENB_RXN[3:0]
Checking
由X455LD P21 移過來
VC 做法有點不同
Place Near GPU
C7009 1UF/6.3V @/VGA
C7010 1UF/6.3V @/VGA
C7011 4.7UF/6.3V /VGA
C7012 10UF/6.3V /VGA
C7014 @/VGA 22UF/6.3V
C7015 /VGA 22UF/6.3V
+PEX_VDD
3300 mA
Place Under GU
C7016 1UF/6.3V /VGA
C7017 1UF/6.3V /VGA
C7018 4.7UF/6.3V @/VGA
C7020 10UF/6.3V @/VGA
C7021 @/VGA 22UF/6.3V
C7022 @/VGA 22UF/6.3V
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
C7023 0.1UF/16V /VGA
C7024 4.7UF/6.3V /VGA
C7025 4.7UF/6.3V @/VGA
VDD_SENSE
GND_SENSE
T7003
0.9V 0.2mm
0.0V 0.2mm
NVDD_VCCSENSE 92
NVDD_VSSSENSE 92
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*
R7005 5% 200Ohm @/VGA
150mA
PEX_PLLVDD_1
PEX_PLLVDD_2
PEX_PLL_VDD
Place Under GPU
C7026 0.1UF/16V /VGA
C7027 1UF/6.3V /VGA
C7030 4.7UF/6.3V /VGA
C7028 10UF/6.3V @/VGA
SL7008
C7029 1UF/6.3V @/VGA
TESTMODE
R7006 10KOhm /VGA
PEX_TERMP
R7007 2.49KOhm /VGA
N14M_GE_S_A1
/VGA
Project Name
X407UA/UV
Title : N14M-GE_PCIE
Dept.: ASUSTeK COMPUTER INC.
Engineer: Brian Chen
Size C
Date: Wednesday, March 07,2018
Sheet 71 of 102
Eletro-X
Eletro-XTechnical


U7001B
2/14FBA
FBA_D[0:63]
GPIO_FB_CLAMP_GPU
R7104
10KOhm
/VGA
1%
GND
Mode D: single rank designs.
FBA_CMD[0:15]
FBA_CMD[16:31]
FBA_DBI[7..0]
FBA_EDC[7..0]
+FBVDDQ
R7101 60.4Ohm @/VGA
R7102 60.4Ohm @/VGA
Place Under GPU
200mA
Place Near GPU
C7101 0.1UF/16V @/VGA
C7102 0.1UF/16V @/VGA
C7103 0.1UF/16V /VGA
C7104 1UF/6.3V /VGA
C7105 22UF/6.3V /VGA
L7101 30Ohm/100Mhz /VGA
+PEX_VDD
T7101
FB_VREF
N14M_GE_S_A1
/VGA

BOM Mount: 02004-00300400

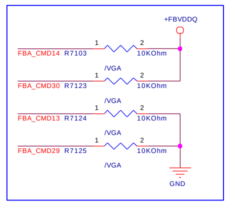
Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	**Channel 0 & 1**		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:

1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

Add for FDDR5

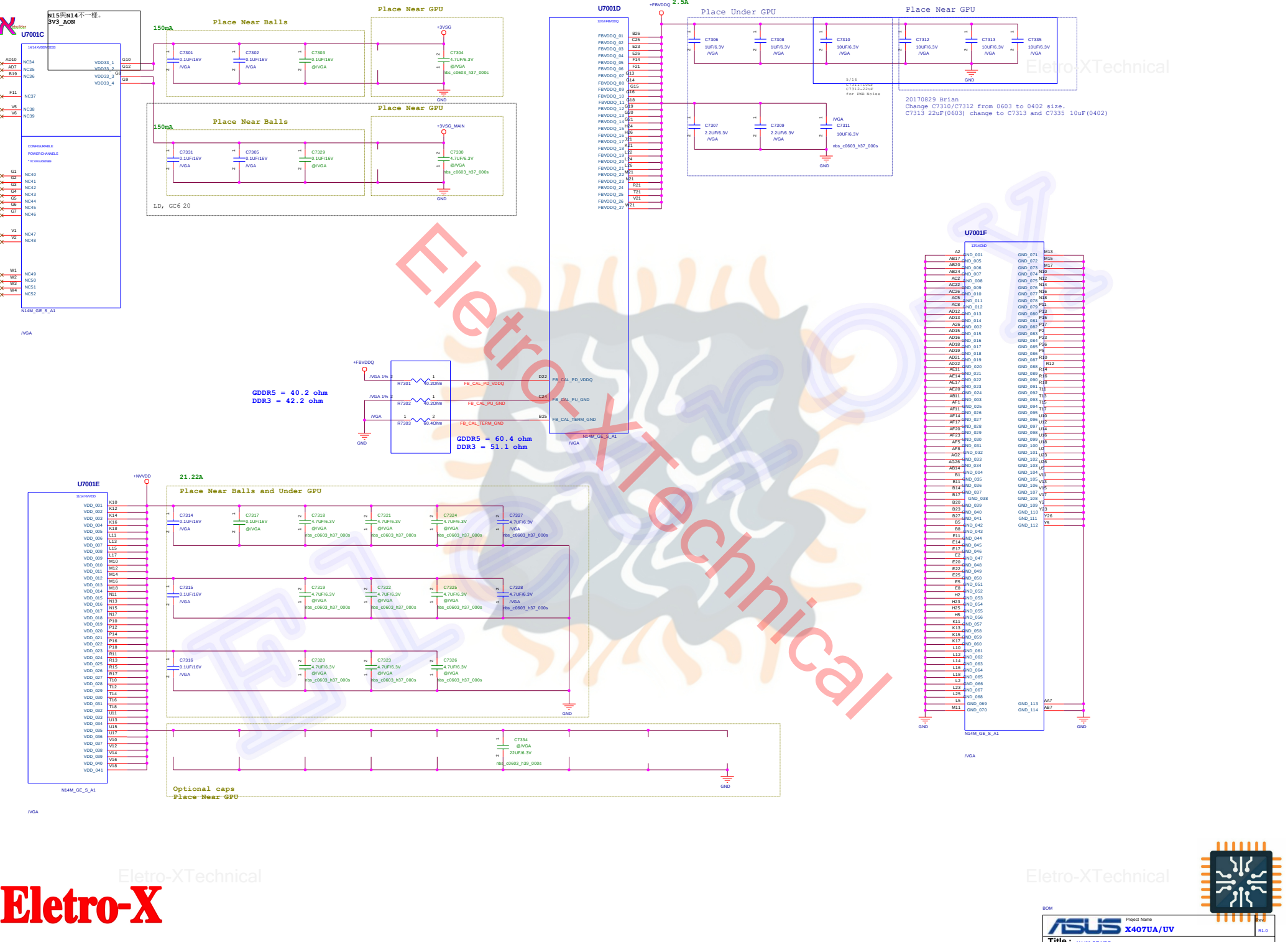


<Variant Name>

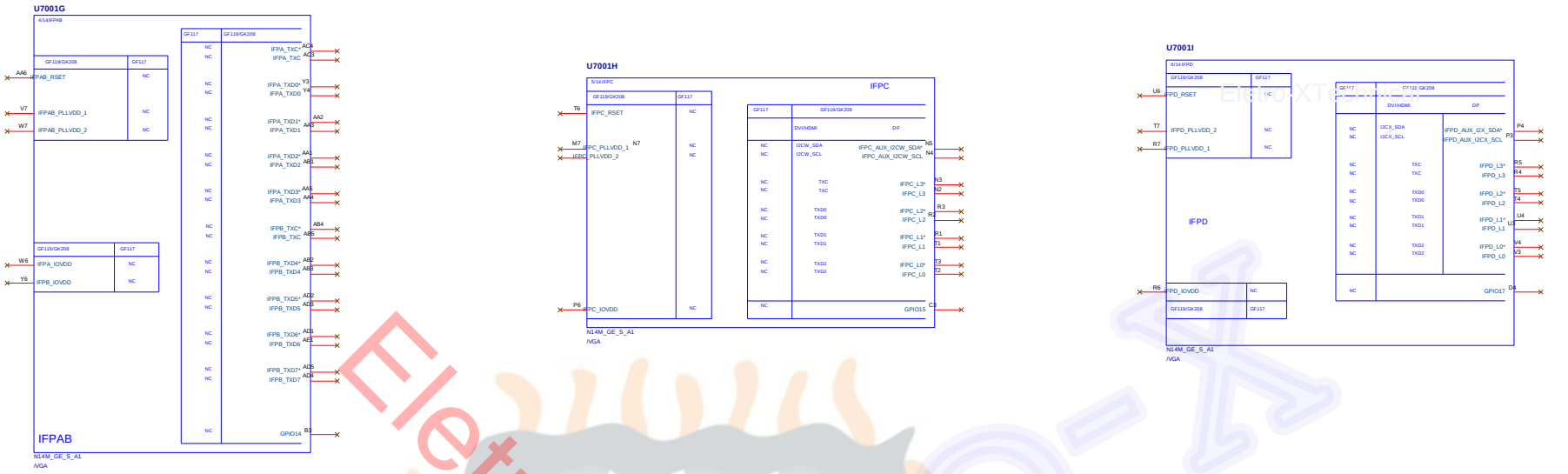
Project Name: X407UA/UV

Title : N14M-GE_FB-IF

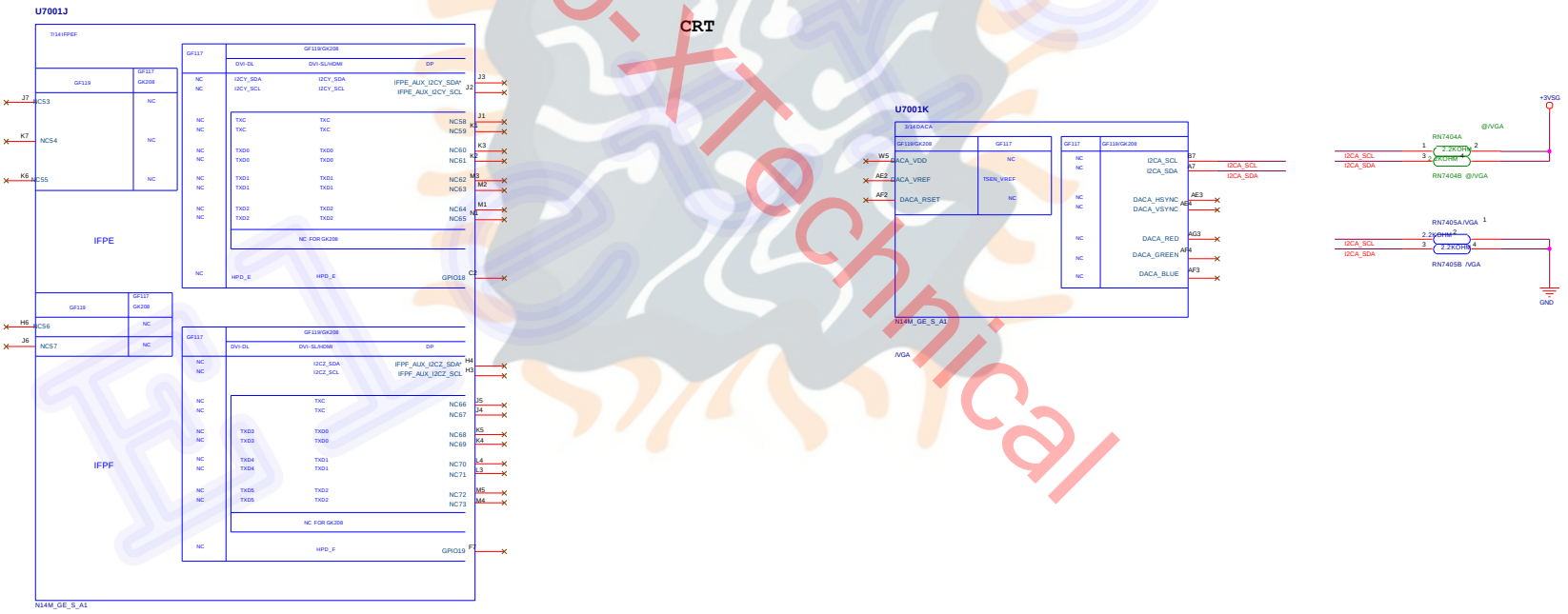
Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen


N15與N14不一樣。
3V3_AON
U7001C
150mA
Place Near Balls
Place Near GPU
+3VSG
C7301 0.1UF/16V /VGA
C7302 0.1UF/16V /VGA
C7303 0.1UF/16V @/VGA
C7304 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND
150mA
Place Near Balls
Place Near GPU
+3VSG_MAIN
C7331 0.1UF/16V /VGA
C7305 0.1UF/16V /VGA
C7329 0.1UF/16V @/VGA
C7330 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND
LD, GC6 20
CONFIGURABLE POWER CHANNELS
* nc consultrate
N14M_GE_S_A1
/VGA
U7001D
+FBVDDQ
2.5A
Place Under GPU
Place Near GPU
C7306 1UF/6.3V /VGA
C7308 1UF/6.3V /VGA
C7310 10UF/6.3V /VGA
C7312 10UF/6.3V /VGA
C7313 10UF/6.3V /VGA
C7335 10UF/6.3V /VGA
GND
C7307 2.2UF/6.3V /VGA
C7309 2.2UF/6.3V /VGA
C7311 10UF/6.3V nbs_c0603_h37_000s
GND
20170829 Brian
Change C7310/C7312 from 0603 to 0402 size.
C7313 22uF(0603) change to C7313 and C7335 10uF(0402)
+FBVDDQ
/VGA 1%
R7301 40.2ohm
R7302 40.2ohm
R7303 60.4ohm
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
GDDR5 = 40.2 ohm
DDR3 = 42.2 ohm
GDDR5 = 60.4 ohm
DDR3 = 51.1 ohm
U7001F
U7001E
+NVVDD
21.22A
Place Near Balls and Under GPU
C7314 0.1UF/16V /VGA
C7317 0.1UF/16V @/VGA
C7318 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7321 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7324 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7327 4.7UF/6.3V /VGA nbs_c0603_h37_000s
C7315 0.1UF/16V /VGA
C7319 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7322 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7325 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7328 4.7UF/6.3V /VGA nbs_c0603_h37_000s
C7316 0.1UF/16V /VGA
C7320 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7323 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
C7326 4.7UF/6.3V @/VGA nbs_c0603_h37_000s
GND
C7334 @/VGA 22UF/6.3V nbs_c0603_h39_000s
Optional caps
Place Near GPU
Eletro-X
Project Name
X407UA/UV
BOM
Rev
R1.0
Title

LVDS



CRT



Project Name	X407UA/UV
Title :	N14M-GE_DISPLAY
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Brian Chen
Date:	Wednesday, March 07, 2018
Sheet	75 of 102

Table 15-3. GB2B-64, GB4B-128 and GB1B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_ADN and pull-down to GND. Stuff 49.9 kΩ pull up.			
STRAP1	Keep foot print for pull-up to 3V3_ADN and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

	Size	Part Number			Strap		ROM_SI
VRAM	128x16b (2Gb)	03007-00030400	gDDR3 128M*16 1.35V FBGA-96	MICRON/MT41J128M16JT-093G:K	0xA	1010	PU 15K Ohm
	256x16b (4Gb)	03007-00021100	GDDR3 256M*16-1.35V FBGA96	[illegible]	0x2	0010	PD 15K Ohm
		03007-00021300	GDDR3 256M*16 1.35V FBGA96	MICRON/MT41J256M16LY-091G:N	0x6	0110	PD 34K Ohm

15.5.13 SORx_EXPOSED Straps

SORx_EXPOSED is used to define audio capability on each digital display link.

Display links with audio capability should have the corresponding SORx_EXPOSED bit set to one. These include links used for HDMI, DisplayPort, and DFP1 ports that can be used with a DVI-to-HDMI dongle or routed to the HDMI of DisplayPort connector on a docking station.

Display links with no audio capability should have the corresponding SORx_EXPOSED bit set to 0. These include LVDS, eDP, or unused links.

Table 15-13 shows the correlation between display configurations and the SORx_EXPOSED strap settings.

Table 15-13. SORx_EXPOSED - Display Link to Strap Bit Mapping

15.5.14 DEVID_SEL Strap

This strap selects the pre-programmed Device IDs inside the NVIDIA GPU, replacing the PCI_DEVID straps. This strap only exists in the GB2B-64, GB4B-128, and GB1B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification document for the latest configuration.

15.5.15 PCIE_CFG Strap

This strap selects the pre-programmed PCIe settings inside the NVIDIA GPU, replacing XCFG PACKING. This strap only exists in the GB2B-64, GB4B-128, and GB1B-256 package GPUs. Set this strap to 0 by default. Please refer to the latest GPU specific Platform Update Notification document for the latest configuration.

15.5.6 SMB_ALT_ADDR Strap

This strap is used to configure the address of the I2C slave device on the GPU's PCI interface.

Table 15-6. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x90 (Default)
1	0x92 (Multi-GPU usage)

15.5.5 VGA_DEVICE Strap

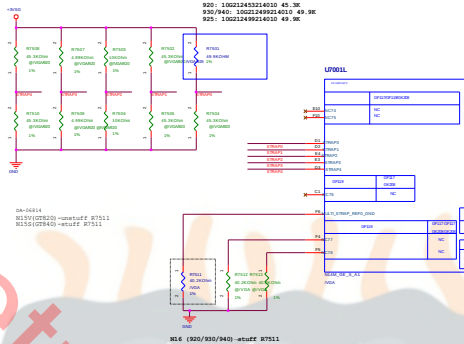
The VGA_DEVICE strap is used to identify the device type (or class code) of the GPU within the PCI configuration space. Set ID Access this as Device for GPU in Optimus configuration or secondary GPU in SLI configuration.

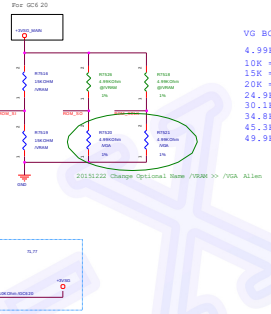
Table 15-7. VGA_DEVICE Settings

VGA_DEVICE	Description
0	Non-Primary 3D Accelerated Device (Class Code 0302)
1	Primary Display or VGA Device (Class Code 0300)

Table 15-1. Device Specific Strap Mode Selection

	eDP/Int GPUs
Multi_Strap_Auto_ONB	Keep foot print for pull-up to 3V3_ADN and pull-down to GND. Stuff 49.9K in to ONE



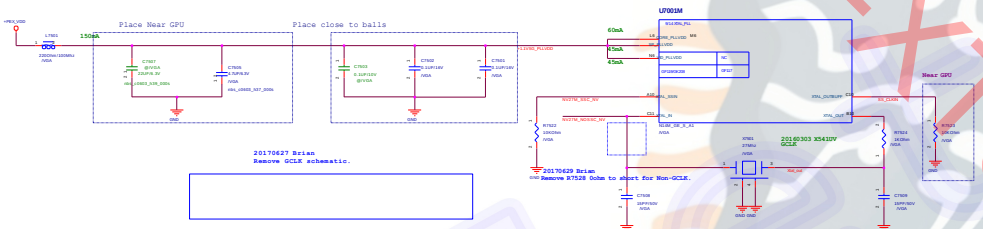


VG BOM 帶入主料時記得要加2nd Source

4.99K = 10G2124991140l0
10K = 10G2121002140l0
15K = 10G2121502140l0
20K = 10G2122002140l0
24.9K = 10G2122492140l0
30.1K = 10G2123012140l0
34.8K = 10G2123482140l0
45.3K = 10G2124532140l0
49.9K = 10G2124992140l0

LD_for GC6 20

Xtal

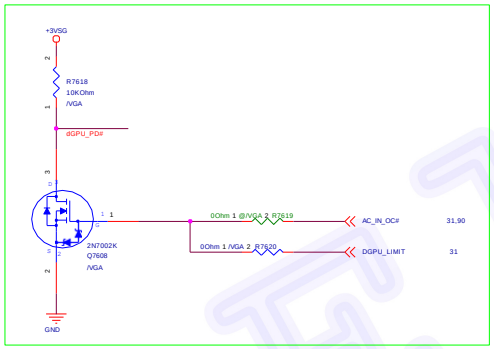


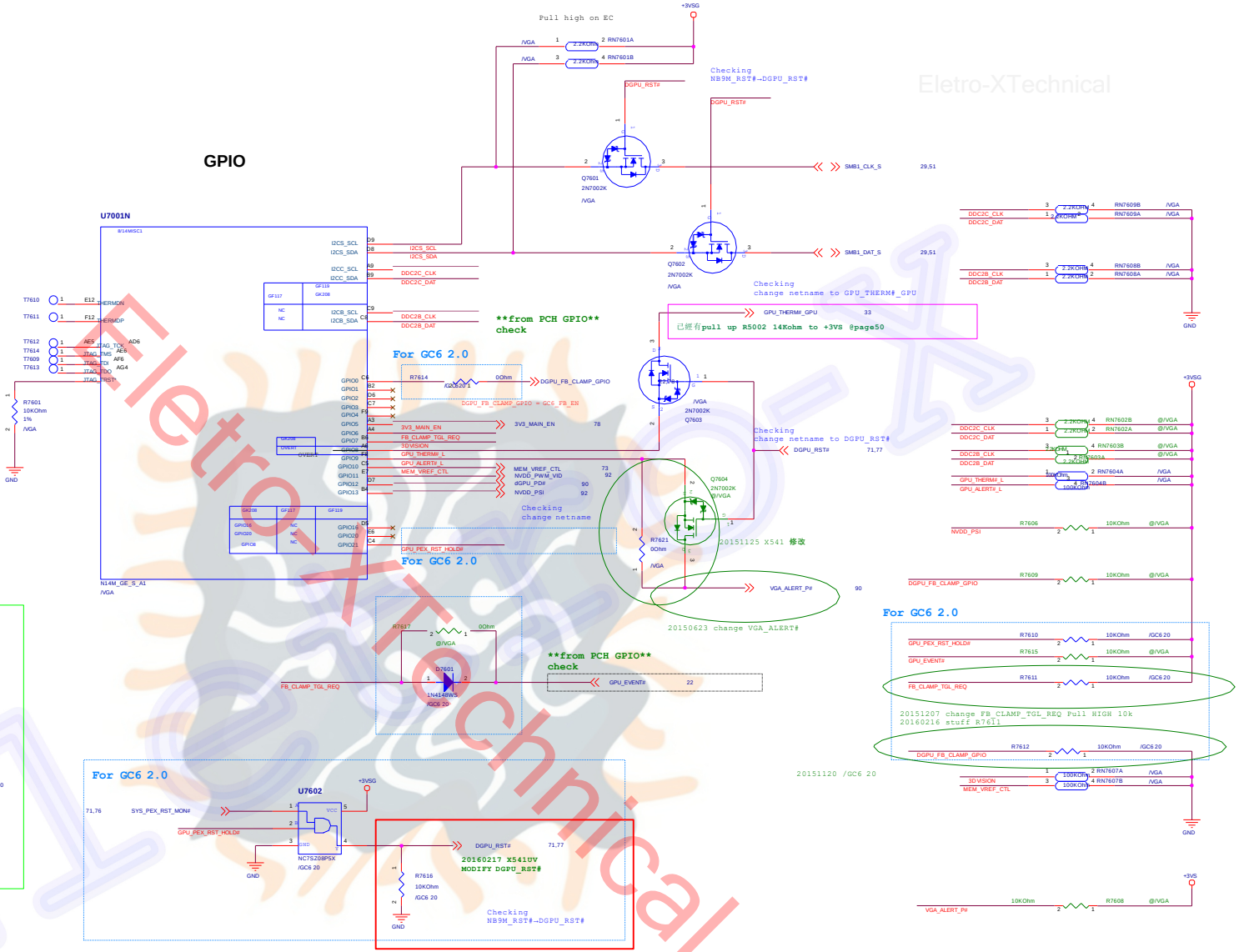
ASUS	Project Name: X407UA/UV		Rev: 0.1
Title : N4M-GE_ROM,XTAL			
Size: D	Dept.: ASUSTeK COMPUTER INC	Engineer: Brian Chen	
Date: Wednesday, March 07, 2018		Sheet: 76 of 102	

Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM_VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe soft-reset control	10K pull-up to 3V3_AON
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

GPIO





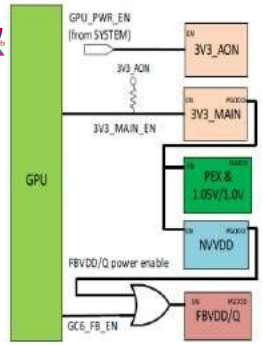
Eletro-X

BOM

ASUS Project Name X407UA/UV

Title : N14M-GE_GPIO

Size | Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen



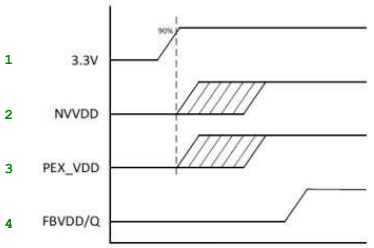
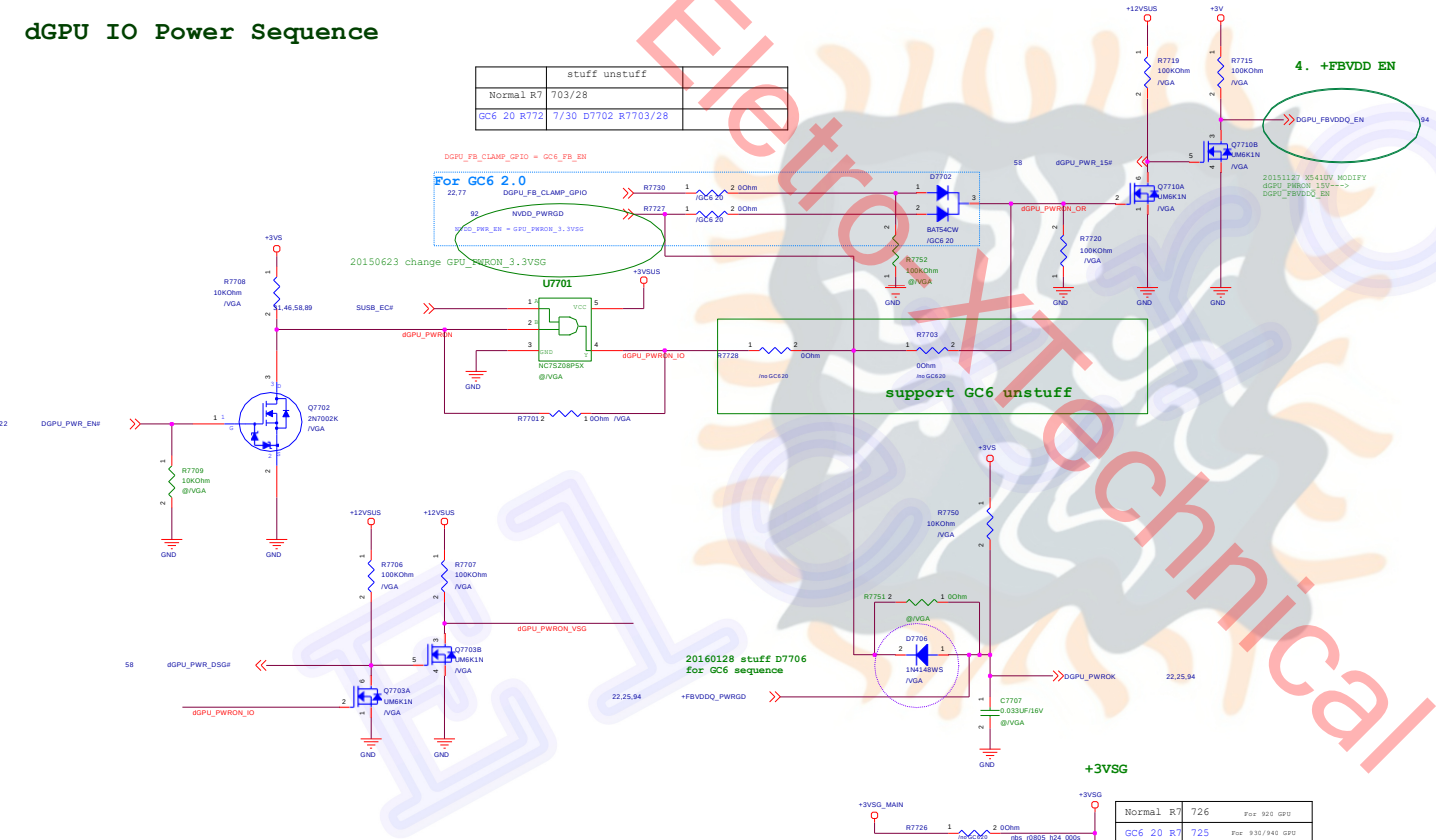
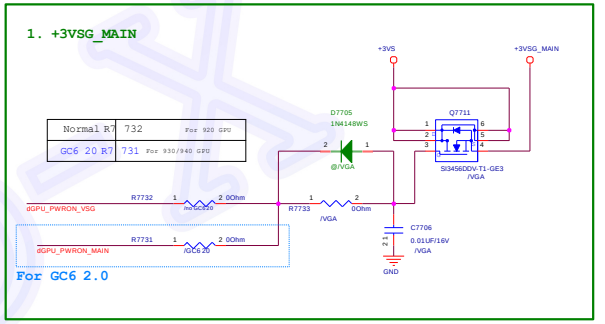


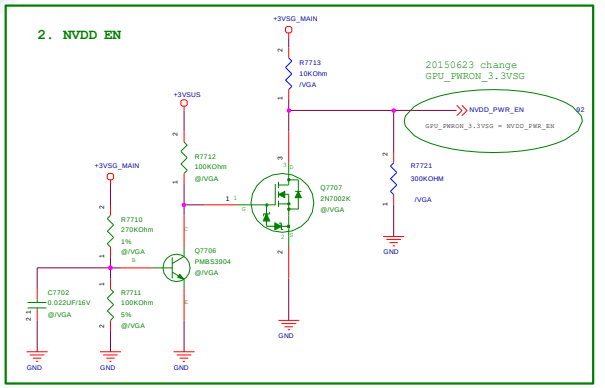
Figure 3-7. Example of Power-Up Sequencing Order

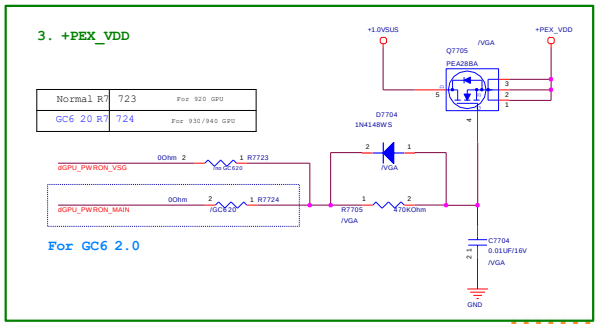
dGPU IO Power Sequence

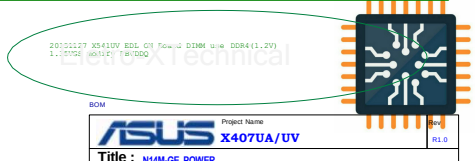


dGPU Core Power Sequence





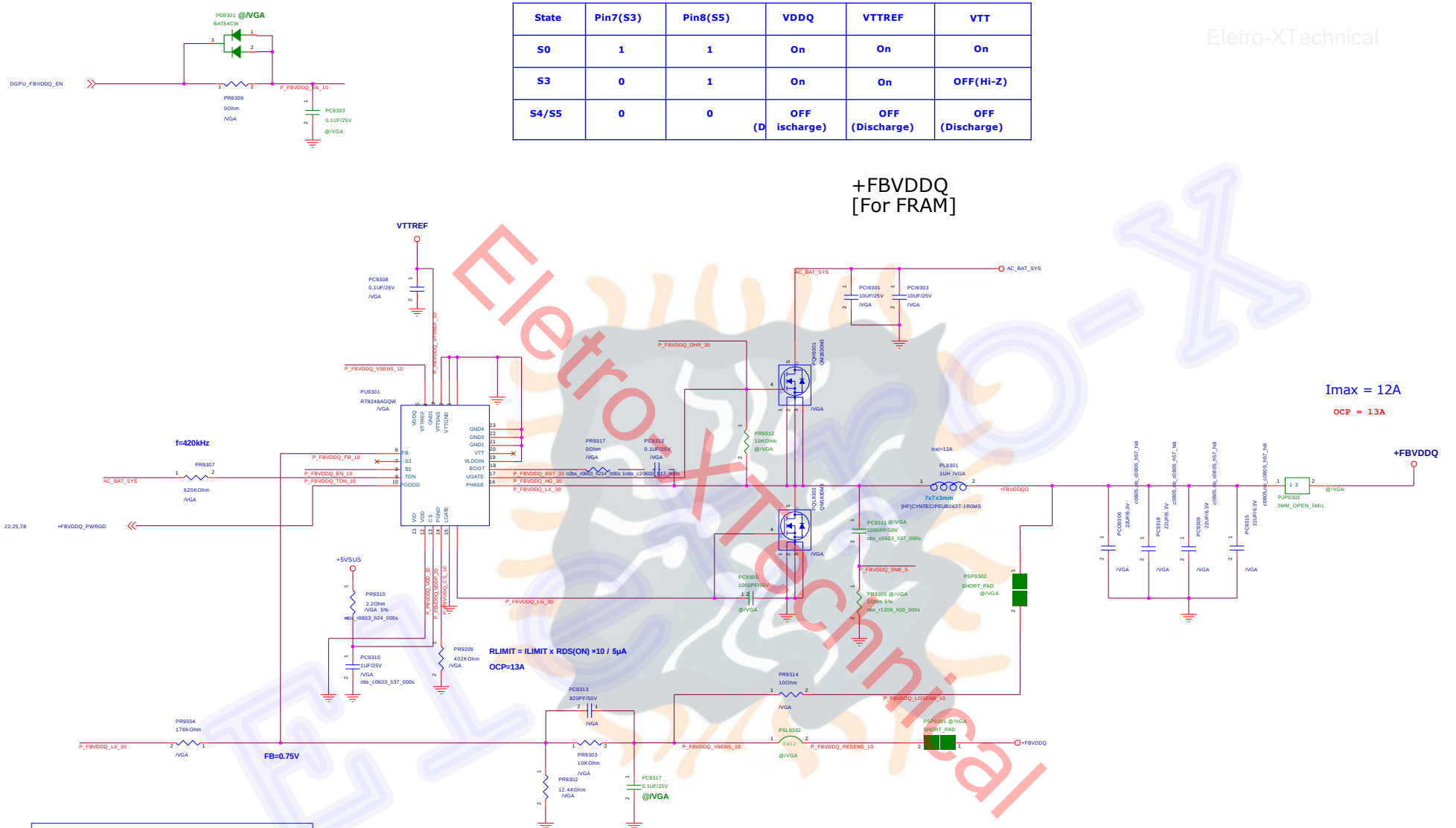




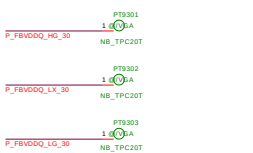
S3 And S5 Truth Table

State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

+FBVDDQ
[For FRAM]



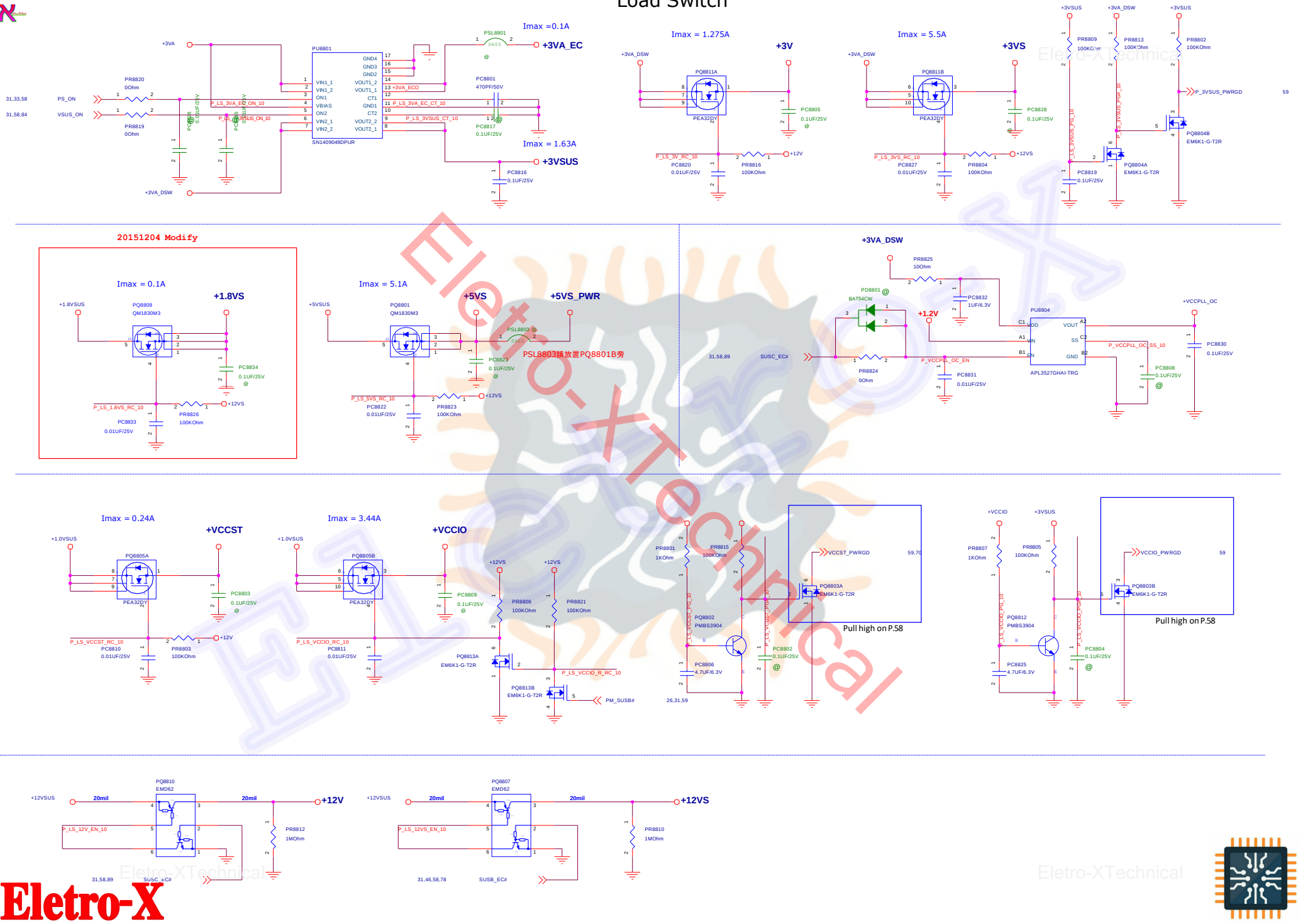
PT930* 請放置 PU9301旁;並請放置Trace 上!



<Variant Name>

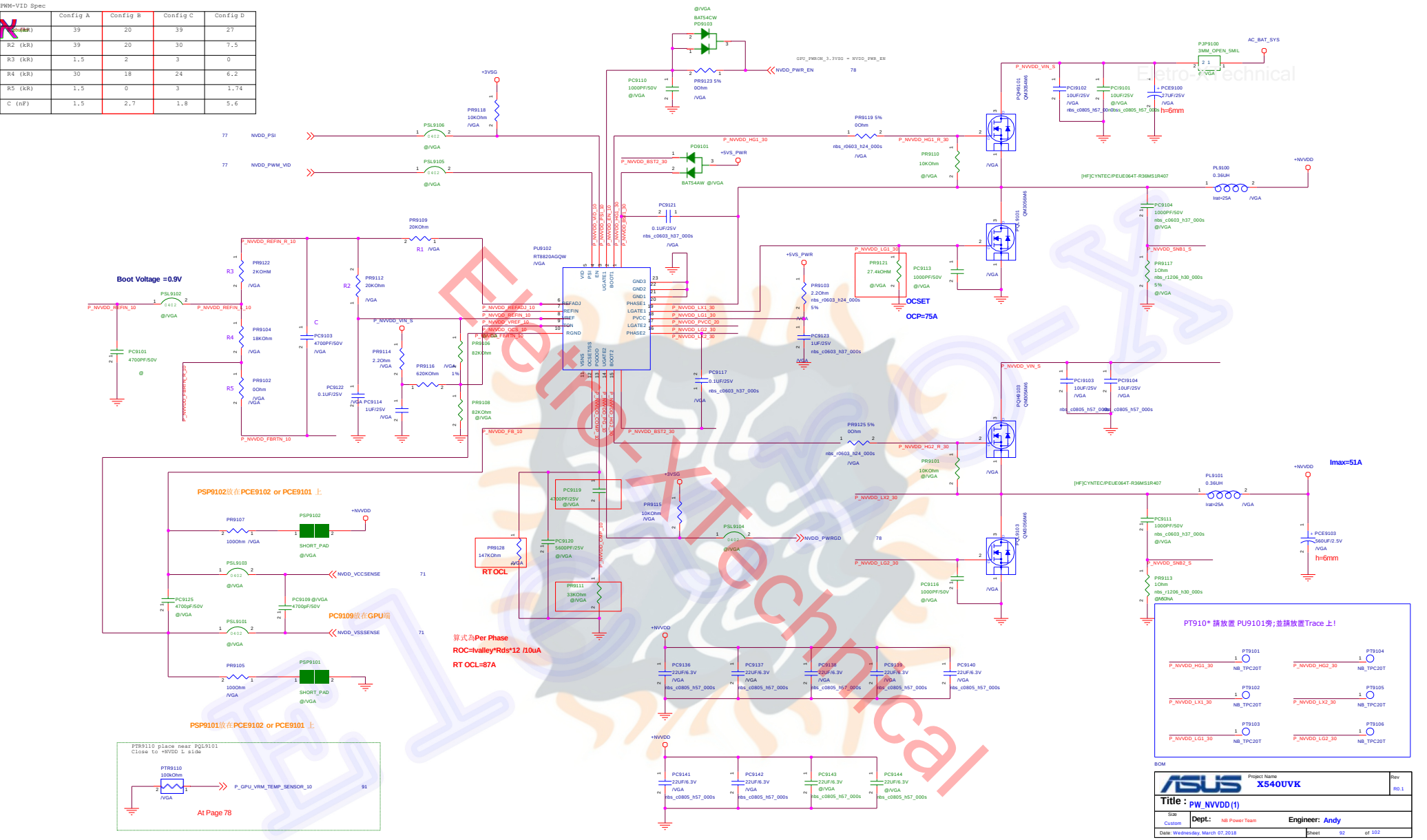
ASUS	Project Name: X540UVK	Rev: R0.1
Title : PW_+FBVDDQ		
Size: Custom	Dept.: NB Power Team	Engineer:
Date: Wednesday, March 07, 2018	Sheet	

Load Switch

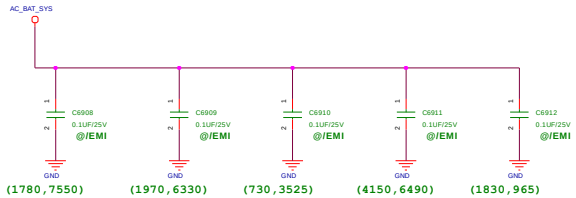

Imax =0.1A
+3VA_EC
Imax = 1.63A
+3VSUS
Imax = 1.275A
+3V
Imax = 5.5A
+3VS
20151204 Modify
Imax = 0.1A
+1.8VS
Imax = 5.1A
+5VS
+5VS_PWR
PSL8803錯放置PQ8801B旁
+3VA_DSW
+1.2V
Imax = 0.24A
+VCCST
Imax = 3.44A
+VCCIO
Pull high on P.58
Pull high on P.58
+12V
+12VS
Eletro-XTechnical

PWM-VID Spec

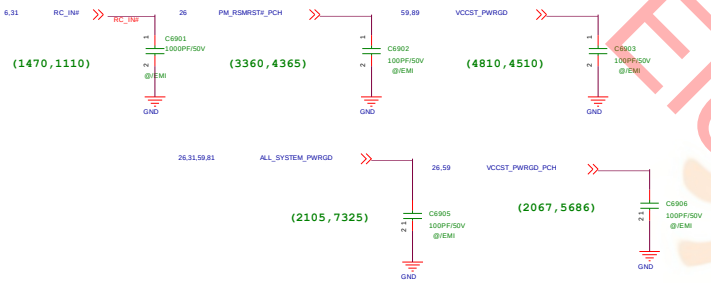
	Config A	Config B	Config C	Config D
R1 (kR)	39	20	39	27
R2 (kR)	39	20	30	7.5
R3 (kR)	1.5	2	3	0
R4 (kR)	30	18	24	6.2
R5 (kR)	1.5	0	3	1.74
C (nF)	1.5	2.7	1.8	5.6



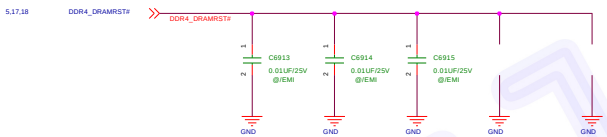
EMI AC_BAT_SYS CAP



EMI CAP



DDR4 CAPs



Gasket

BOM

Project Name: X407UA/JV

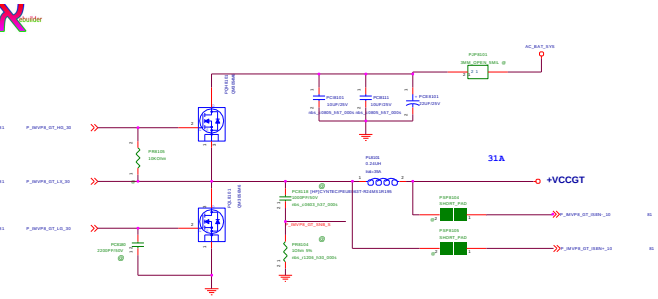
Title : EMI

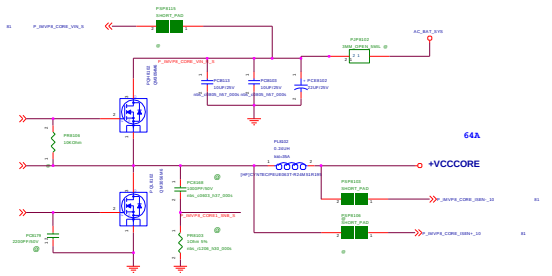
Size: C

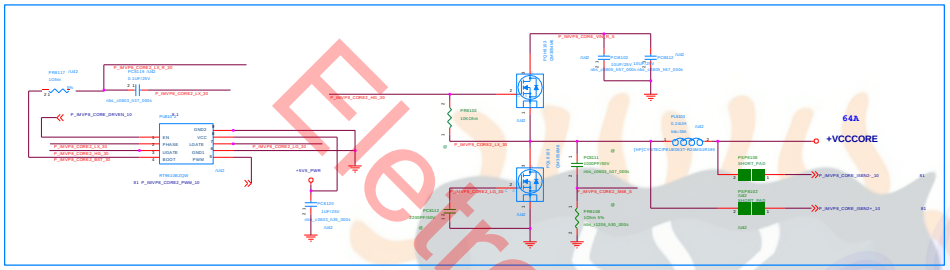
Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen

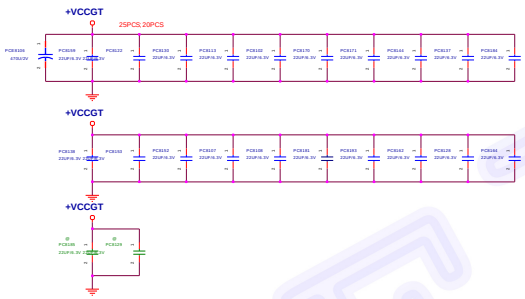
Date: Wednesday, March 07, 2018 Sheet 70 of 80

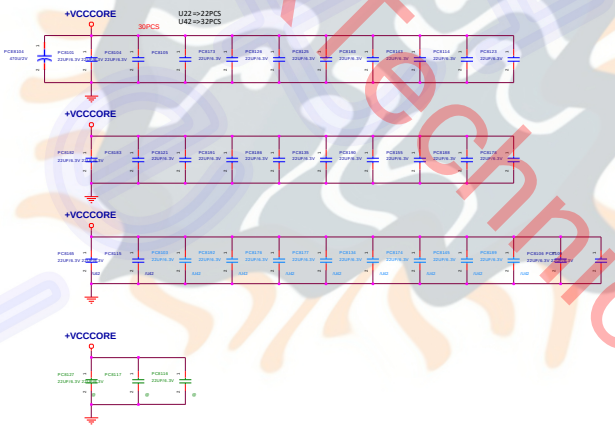
Kaby Lake-U IMVP8 Power (2) [For CPU]

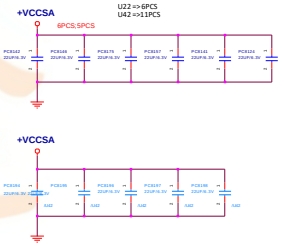


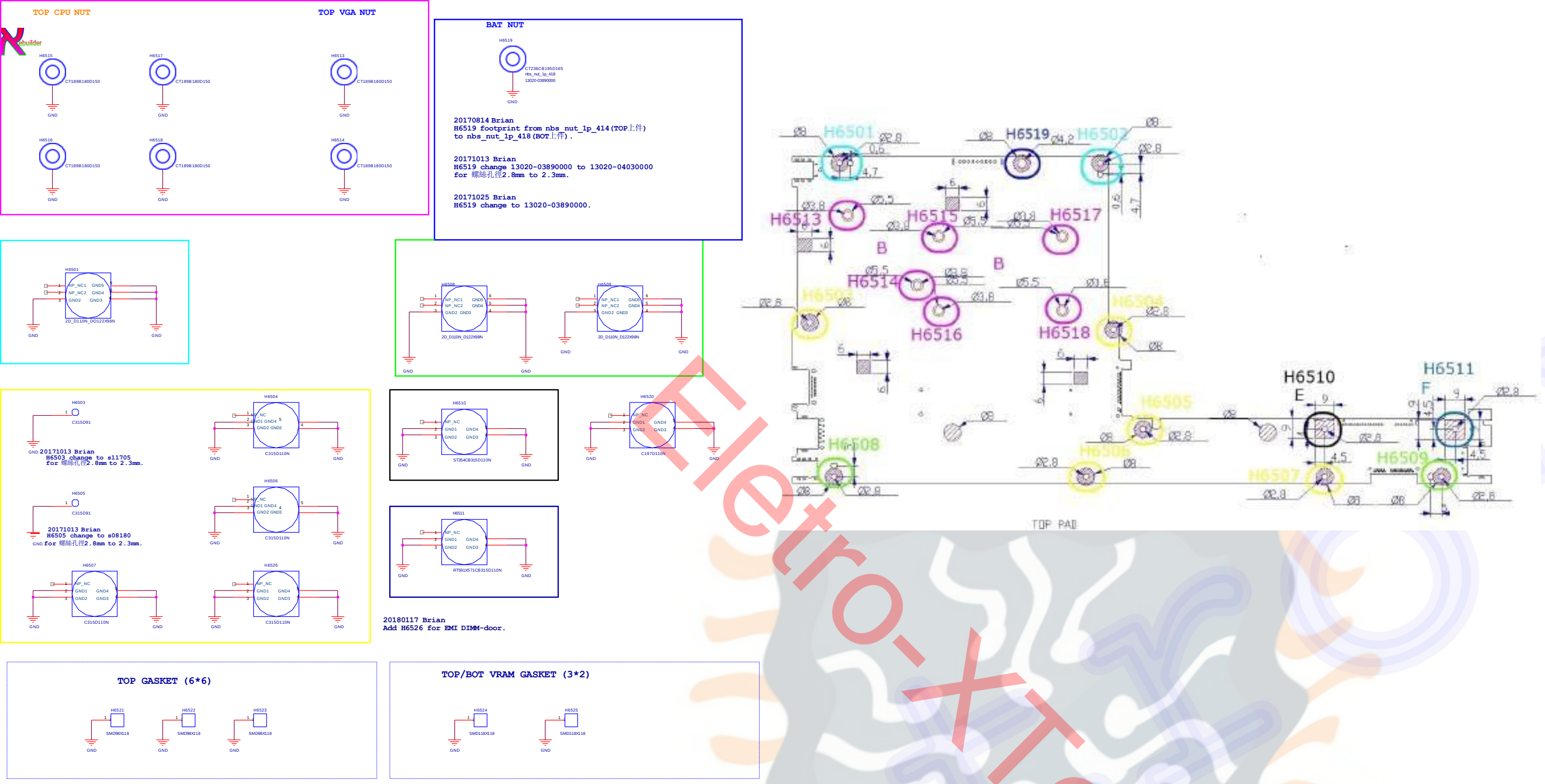








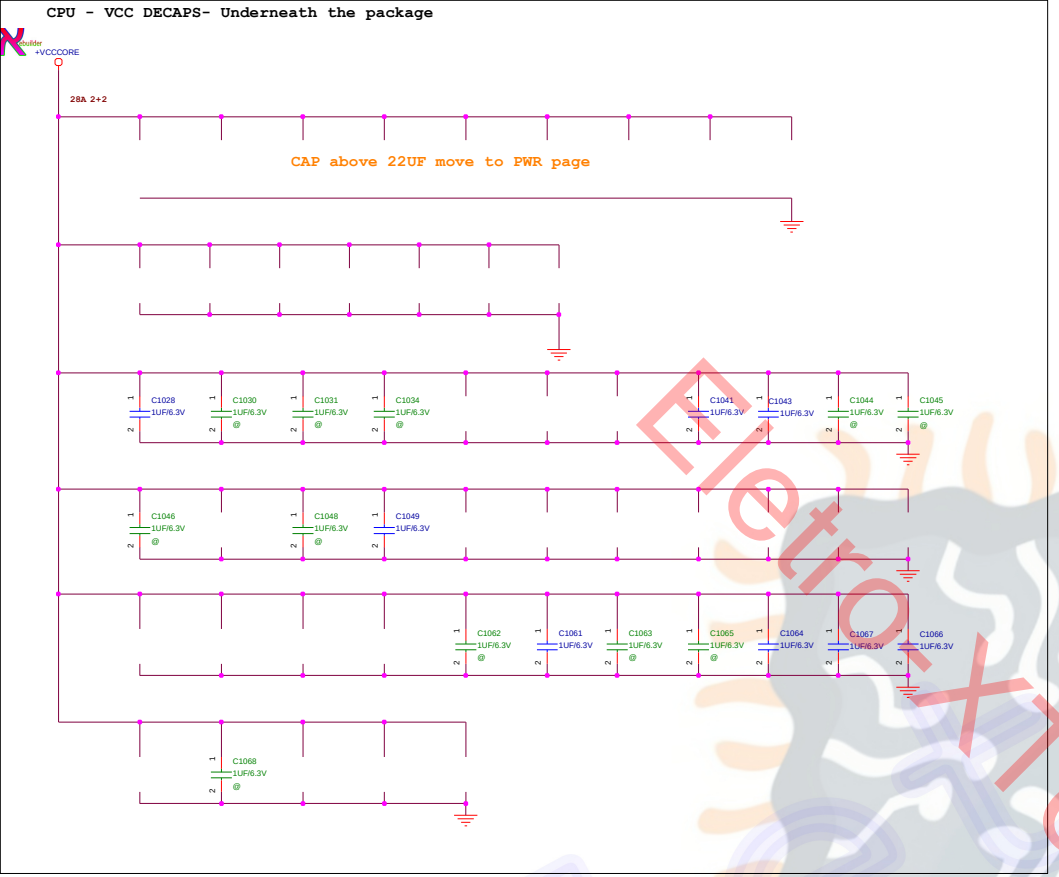



TOP CPU NUT
TOP VGA NUT
BAT NUT
H6515
H6517
H6513
H6516
H6518
H6514
H6519
CT236CB195D165
nbs_nut_1p_418
13020-03890000
20170814 Brian
H6519 footprint from nbs_nut_1p_414(TOP上件)
to nbs_nut_1p_418(BOT上件).
20171013 Brian
H6519 change 13020-03890000 to 13020-04030000
for 螺絲孔徑2.8mm to 2.3mm.
20171025 Brian
H6519 change to 13020-03890000.
H6501
H6508
H6509
H6502
2D_D110N_DO122X98N
H6503
C315D91
20171013 Brian
H6503 change to s11705
for 螺絲孔徑2.8mm to 2.3mm.
H6505
20171013 Brian
H6505 change to s08180
for 螺絲孔徑2.8mm to 2.3mm.
H6504
H6506
H6507
H6526
C315D110N
H6510
H6520
H6511
20180117 Brian
Add H6526 for EMI DIMM-door.
TOP GASKET (6*6)
H6521
H6522
H6523
TOP/BOT VRAM GASKET (3*2)
H6524
H6525
GND
TOP PAD
H6510
H6511
E
F

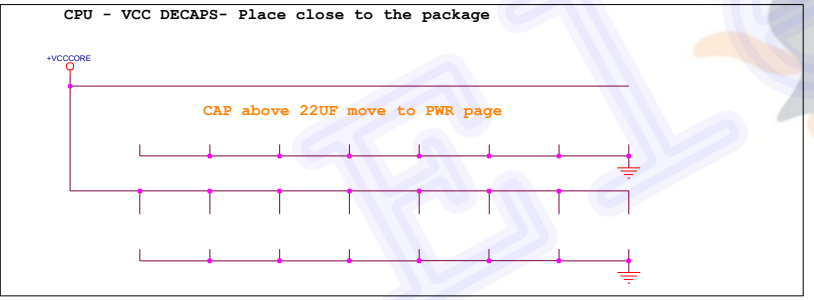
<Variant Name>

ASUS	Title : 65_ME_Conn & Skew Hole
ASUSTeK COMPUTER INC. NB4	Engineer: Bull Tsai
Size: D	Project Name: X507UA/UV	Rev: R1.0
Date: Wednesday, March 07, 2018	Sheet 66 of 102

CPU - VCC DECAPS- Underneath the package



CPU - VCC DECAPS- Place close to the package



BOM

Project Name
X407UA/UV

Title :

Rev
R1.0

Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0],ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

<Variant Name>

Title : DDR4_TERMINATION_A

Engineer: Brian Chen

Size	Project Name	Rev
C	X407UA/UV	R1.0

Date: Wednesday, March 07, 2018 Sheet 14 of 102

PCH_CPT GPIO

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	Note
	GPP_A0	Native1	RC_IN#		EXT PU 10K	+3VS	PU EC
	GPP_A1	Native1	LPC_AD0				
	GPP_A2	Native1	LPC_AD1				
	GPP_A3	Native1	LPC_AD2				
	GPP_A4	Native1	LPC_AD3				
	GPP_A5	Native1	LPC_FRAME#				
	GPP_A6	Native1	INT_SERIRQ		EXT PU 10K	+3VS	
	GPP_A7	GPO	N/A				
	GPP_A8	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS	
	GPP_A9	Native1	CLK_KBCPCI_PCH				
	GPP_A10	Native	CLK_DEBUG				
For 555 N/A	GPP_A11	GPO	N/A	需確認是否具wake 功能			
	GPP_A12	GPO	N/A				
	GPP_A13	Native1	SUSWARN#		EXT PU 10K	+3VSUS	
	GPP_A14	Native1	PCH_SUS_STAT#				
Need Add EC	GPP_A15	Native1	PCH_SUSACK#				
For 555 N/A	GPP_A16	GPO	N/A (SD_1P8_SEL)				
For 555 N/A	GPP_A17	GPO	N/A (SD_PWR_EN#)				
	GPP_A18	GPO	N/A				
	GPP_A19	GPO	N/A				
	GPP_A20	GPO	N/A				
	GPP_A21	GPO	N/A				
	GPP_A22	GPO	N/A				
	GPP_A23	GPO	N/A				
For 555 N/A	GPP_B0	Native	N/A (VCCPRIM_VID0)		EXT PU 10K	+3VS	
For 555 N/A	GPP_B1	Native	N/A (VCCPRIM_VID1)		EXT PU 10K	+3VS	
	GPP_B2	GPO	N/A				
	GPP_B3	GPO	N/A				
	GPP_B4	GPO	N/A				
	GPP_B5	Native	CK_REQ_P0# DGPU		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B6	Native	CK_REQ_P1#		EXT PU 10K	+3VS	For X541UV ADD
	GPP_B7	Native	CK_REQ_P2#		EXT PU 10K	+3VS	
	GPP_B8	Native	CK_REQ_P3#		EXT PU 10K	+3VS	
	GPP_B9	Native	CK_REQ_P4# GLAN		EXT PU 10K	+3VS	
	GPP_B10	Native	CK_REQ_P5# WLAN		EXT PU 10K	+3VS	
	GPP_B11	Native	MPHY_PWREN (N/A)		EXT PU 20K	+3VSUS	
	GPP_B12	Native	PCH_SLP_S0#				
	GPP_B13	Native	PLT_RST#				
	GPP_B14	GPO	PCH_GPPB14				
For 555 N/A	GPP_B15	GPO	N/A (GSPI0_CS_R#)				
For 555 N/A	GPP_B16	GPO	N/A (GSPI0_CLK_R)				
For 555 N/A	GPP_B17	GPO	N/A (GSPI0_MISO_R)				
	GPP_B18	GPO	N/A (PCH_GPPB18)				
	GPP_B19	GPO	BT_ON/OFF#				
	GPP_B20	GPO	GPU_EVENT#		EXT PU 10K	+3VSG	
	GPP_B21	GPI	DGPU_FB_CLAMP_GPIO		EXT PD 10K	PU at DGPU	
	GPP_B22	GPO	PCH_GPPB22				
	GPP_B23	Native	SML1ALERT#		EXT PU 150K	+3VSUS	
	GPP_C0	Native	SMB_CK		EXT PU 2.2K	+3VSUS	
	GPP_C1	Native	SMB_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C2	GPO	GPP_C2				
For 555 N/A	GPP_C3	GPO	SML0_CK		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C4	GPO	SML0_DATA		EXT PU 2.2K	+3VSUS	
	GPP_C5	GPO	GPP_C5				
	GPP_C6	GPO	SML1_CK		EXT PU 2.2K	+3VSUS	
	GPP_C7	GPO	SML1_DATA		EXT PU 2.2K	+3VSUS	
For 555 N/A	GPP_C8	GPO	N/A (PCH_GPPC8)				
For 555 N/A	GPP_C9	GPO	N/A (PCH_GPPC9)				
For 555 N/A	GPP_C10	GPO	N/A (PCH_GPPC10)				
For 555 N/A	GPP_C11	GPO	N/A (PCH_GPPC11)				
	GPP_C12	GPO	DIMM_SEL0		EXT PU 10K	+3VSUS	
	GPP_C13	GPO	DIMM_SEL1		EXT PU 10K	+3VSUS	
	GPP_C14	GPO	DIMM_SEL2	UART1_RTS#	EXT PU 10K	+3VSUS	
	GPP_C15	GPO	FP_RST#_GPIO	UART1_CTS#			
	GPP_C16	GPO	AOAC_WLANLED (N/A)				
For 555 N/A	GPP_C17	GPO	N/A (ALS_INT#)				
For X541UV N/A	GPP_C18	Native	I2C1_SDA_TCH_PAD		PU 4.7K	+3VSUS	
For X541UV N/A	GPP_C19	Native	I2C1_SCL_TCH_PAD		PU 4.7K	+3VSUS	
	GPP_C20	GPI	DGPU_PWROK		EXT PU 10K	+3VSG PU at DGPU	
	GPP_C21	GPO	GPU_RST#		EXT PU 10K	+3VS	
	GPP_C22	GPO	DGPU_PWR_EN#		EXT PU 10K	+3VSUS	
	GPP_C23	GPO	TPanel_INT#		EXT PU 10K	+3VS	
	GPP_D0	GPO	N/A				
	GPP_D1	GPO	N/A				
	GPP_D2	GPO	N/A				
	GPP_D3	GPO	N/A				
For 555 N/A	GPP_D4	GPI	GPIO_SMI_ASM1142 (N/A)				
	GPP_D5	GPO	SATA_ODD_PWRGT		EXT PU 10K	+3VS	
	GPP_D6	GPI	SATA_ODD_DA#		EXT PU 10K	+3VS	
	GPP_D7	GPO	N/A				
	GPP_D8	GPO	N/A				
	GPP_D9	GPI	PCB_ID0		EXT PD 10K		
For X541UV N/A	GPP_D10	GPI	DMIC_ID		EXT PD 10K		
	GPP_D11	GPI	TOUCHPAD_ID		EXT PD 10K		
	GPP_D12	GPI	TOUCH_PANEL_ID		EXT PD 10K		
	GPP_D13	GPI	TOUCHPAD_INTR#		EXT PU 10K	+3VS	
	GPP_D14	GPO	WLAN_LED_R				
X541UV Change	GPP_D15	GPO	SNSR_HUB_PWREN				
	GPP_D16	GPI	FP_INT#	UART0_CTS#			
	GPP_D17	GPO	N/A				
	GPP_D18	GPO	N/A				
For 555 N/A	GPP_D19	GPO	(N/A) DMIC_CLK_PCH				
For 555 N/A	GPP_D20	GPO	(N/A) DMIC_DATA_PCH				
	GPP_D21	GPO	N/A				
	GPP_D22	GPO	N/A				

Note	PCH_IBEX GPIO	Use As	Signal Name	Power on Default States	Int.& Ext Pull up / down	Power	Note
	GPP_D23	GPO	N/A				
	GPP_E0	GPO	DIRECT_ESATA_DETECT_R#		EXT PU 10K	+3VS	
	GPP_E1	GPO	SATA_ODD_PRSNT_R#		EXT PU 10K	+3VS	
	GPP_E2	GPO	MSATA_MPCIE_DET#		EXT PU 10K	+3VS	
	GPP_E3	GPO	N/A				
	GPP_E4	GPO	SATA0_DEVSLP				
	GPP_E5	GPO	SATA1_PHYSLP_DIRECT				
	GPP_E6	GPO	SATA2_DEVSLP				
	GPP_E7	GPO	N/A				
	GPP_E8	NATIVE	PCH_SATA_LED#		EXT PU 10K	+3VS	
	GPP_E9	NATIVE	USB_OC_1_2#_R		EXT PU 10K	+3VSUS	
	GPP_E10	GPI	USB_OC_3_4#		EXT PU 10K	+3VSUS	
	GPP_E11	GPI	USB_OC_5_6#		EXT PU 10K	+3VSUS	
	GPP_E12	GPI	USB_OC_7_8#		EXT PU 10K	+3VSUS	
	GPP_E13	GPO	N/A		EXT PD 100K	PD at IC of eDP	to VGA
	GPP_E14	NATIVE	HDMI_HP		EXT PU 1M	+3VS PD at HDMI	conn
	GPP_E15	GPO	EXT_SMI#		EXT PU 10K	+3VS	
	GPP_E16	GPI	EXT_SCI#		EXT PU 10K	+3VS	
	GPP_E17	NATIVE	EDP_HPD_CON			PD at LVDS conn	
	GPP_E18	GPO	DDPB_SCL_PCH				
	GPP_E19	GPO	DDPB_SDA_PCH		EXT PU 10K	+3VS	
	GPP_E20	NATIVE	DDPC_SCL_PCH		EXT PU 2.2K	+3VS PU at	HDMI conn
	GPP_E21	NATIVE	DDPC_SDA_PCH		EXT PU 2.2K	+3VS PU at	HDMI conn
	GPP_E22	GPO	N/A				
	GPP_E23	GPO	N/A				
	GPP_F0	GPO	N/A				
	GPP_F1	GPO	N/A				
	GPP_F2	GPO	N/A				
	GPP_F3	GPO	N/A				
	GPP_F4	GPO	N/A				
	GPP_F5	GPO	N/A				
	GPP_F6	GPO	N/A				
	GPP_F7	GPO	N/A				
	GPP_F8	GPO	N/A				
	GPP_F9	GPO	N/A				
	GPP_F10	GPO	N/A				
	GPP_F11	GPO	N/A				
	GPP_F12	GPO	N/A				
	GPP_F13	GPO	N/A				
	GPP_F14	GPO	N/A				
	GPP_F15	GPO	N/A				
	GPP_F16	GPO	N/A				
	GPP_F17	GPO	N/A				
	GPP_F18	GPO	N/A				
	GPP_F19	GPO	N/A				
	GPP_F20	GPO	N/A				
	GPP_F21	GPO	N/A				
	GPP_F22	GPO	N/A				
	GPP_F23	GPO	N/A				
For 555 N/A	GPP_G0	GPO	N/A (SDIO_CMD)				
For 555 N/A	GPP_G1	GPO	N/A (SDIO_D0)				
For 555 N/A	GPP_G2	GPO	N/A (SDIO_D1)				
For 555 N/A	GPP_G3	GPO	N/A (SDIO_D2)				
For 555 N/A	GPP_G4	GPO	N/A (SDIO_D3)				
For 555 N/A	GPP_G5	GPO	N/A (SDIO_CD#)				
For 555 N/A	GPP_G6	GPO	N/A (SDIO_CLK)				
For 555 N/A	GPP_G7	GPO	N/A (SDIO_WP)				
For 555 ADD	GPD0	Native	PM_BATLOW_R#		EXT PU 8.2K	+3VA_DSW	
	GPD1	Native	ME_AC_PRESENT_PCH		EXT PU 100K	+3VA_DSW	
	GPD2	GPO	PCH_GPD2#		EXT PU 10K	+3VA_DSW	
	GPD3	Native	PM_PWRBTN#				
	GPD4	Native	PM_SUSB#		EXT PD 100K	PD at EC	
	GPD5	Native	PM_SUSC#		EXT PD 100K	PD at EC	
For 555 ADD	GPD6	Native	PM_SLP_A_R#				
	GPD7	GPO	WLAN_ON#				
For 555 N/A	GPD8	GPO	NA (SUS_CK)		EXT PD 1K		
	GPD9	GPO	PCH_SLP_WLAN# (N/A)				
	GPD10	GPO	SLP_S5# (N/A)				
	GPD11	GPO	LAN_PWREN (N/A)				

EC IT8995 GPIO

Note	Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
	GPA0	O	PWR_LED	LOW		
	GPA1	OD	CHG_LED#	HIGH	EXT 10K PU	+3VA_EC
	GPA2	OD	CHG_FULL_LED#	HIGH	EXT 10K PU	+3VA_EC
For 555 N/A	GPA3	Alt	EC_GPA3	LOW		
For 555 N/A	GPA4	O	EC_GPA4	LOW	EXT 10K PU	+3VA_EC
	GPA5	Alt	FAN0_PWM	LOW		
	GPA6	Alt	KB_LED_PWM	LOW		
For 555 N/A	GPA7	O	EC_GPA7 (N/A)	HIGH		
	GPB0	Alt	AC_IN_OC#	HIGH	EXT 10K PU	+3VA
	GPB1	I	LID_SW#	HIGH	EXT 10K PU	+3VA
For 555 N/A	GPB2	OD	(N/A)	LOW	EXT 10K PU	+3VA_EC
	GPB3	I	PWR_SW#	HIGH	EXT 10K PU	+3VA
	GPB4	O	PS_ON	HIGH		
For 555 N/A	GPB5	O	A20GATE (N/A)	LOW	EXT 10K PU	+3VS
	GPB6	OD	RC_IN#	HIGH	EXT 10K PU	+3VS
For 555 N/A	GPC0	O	(N/A)	LOW		
	GPC1	Alt	SMB1_CLK	LOW	EXT 4.7K PU	+3VA_EC
	GPC2	Alt	SMB1_DAT	LOW	EXT 4.7K PU	+3VA_EC
	GPC3	O	PM_PWRBTN#	HIGH		
For 555 N/A	GPC4	I	EC_GPC4 (N/A)	LOW	EXT 10K PU	+3VS
	GPC5	I	PM_SUSC#	HIGH	EXT 100K PD	
	GPC6	Alt	BAT1_IN_OC#	HIGH	EXT 10K PD	
For555 N/A	GPC7	I	(N/A)	LOW		
	GPD0	I	PCH_SLP_S0#	HIGH		
	GPD1	O	ME_AC_PRESENT	LOW	EXT 100K PU	+3VA_DSW
	GPD2	Alt	BUF_PLT_RST#	HIGH	EXT 100K PD	
	GPD3	OD	EXT_SCI#	HIGH	EXT 10K PU	+3VS
	GPD4	OD	EXT_SMI#	HIGH	EXT 10K PU	+3VS
	GPD5	O	OP_SD#	HIGH		
	GPD6	Alt	FAN0_TACH	LOW	EXT 10K PU	+3VS
For 555 N/A	GPD7	Alt	(N/A)	LOW	EXT 10K PU	+3VS
	GPE0	O	SUSB_EC#	HIGH	EXT 10K PD	
	GPE1	O	SUSC_EC#	HIGH	EXT 10K PD	
	GPE2	O	1.2V_ON	LOW		
	GPE3	O	N/A	HIGH		
For 555 N/A	GPE4	O	(N/A)	HIGH		
	GPE5	I	PM_SUSB#	LOW	EXT 100K PD	
For 555 N/A	GPE6	OD	CAP_LED#	HIGH		
	GPE7	OD	THRO_CPU#	HIGH	EXT 1K PU	+VCCSTG
	GPF0	O	5VSUS_ON	LOW	EXT 10K PU/ 1M PD	+3VA_EC
	GPF1	O	VSUS_ON	LOW	EXT 100K PU	+3VA_EC
	GPF2	Alt	SMB0_CLK	HIGH	EXT 4.7K PU	+3VA_EC
	GPF3	Alt	SMB0_DATA	HIGH	EXT 4.7K PU	+3VA_EC
	GPF4	Alt	TP_CLK	HIGH	EXT 4.7K PU	+3VS
	GPF5	Alt	TP_DAT	HIGH	EXT 4.7K PU	+3VS
	GPF6	Alt	PECI_EC	LOW		
	GPF7	O	PCH_SPI_OV	LOW		
	GPG0	O	DGPU_LIMIT	LOW		
	GPG1	O	PCH_SUSACK#	HIGH		
	GPG2	I	PWRLIMIT_EC#	HIGH	EXT 100K PU	+3VA_EC
For 555 N/A	GPG6	O	(N/A)	LOW		
	GPH0	Alt	PM_CLKRUN#	HIGH	EXT 8.2K PU	+3VS
For 555 N/A	GPH1	Alt	SMB3_CLK N/A	HIGH		
For 555 N/A	GPH2	Alt	SMB3_DAT N/A	HIGH		
	GPH3	O	PM_RSMRST#	HIGH	EXT 10K PD	
	GPH4	O	DPWROK_EC	LOW	EXT 10K PD	
	GPH5	O	PM_PWROK	LOW	EXT 100K PD	
	GPH6	O	PM_SYSPWROK	LOW	EXT 10K PD	
	GPH7	O	LCD_BACKOFF#	HIGH		
	GPI0	I	PM_SLP_SUS#	HIGH	EXT 10K PU/ 100K PD	+3VA_EC
	GPI1	I	3VSUS_PWRGD	LOW		
	GPI2	I	ALL_SYSTEM_PWRGD	LOW	EXT 10K PU	+3VS
	GPI3	I	IMVP8_PWRGD	LOW	EXT 10K PU	+3VS
	GPI4	I	3VA_DSW_PWRGD	LOW	EXT 100K PU	+3VA_DSW
	GPI5	I	ME_SusPwrDnAck_EC	LOW		
	GPI6	Alt	A/D_MAX_POWER	LOW	EXT 0 PD	
	GPI7	Alt	MB_MAX_POWER	LOW	EXT 100K PU/93.1K PD	+3VACC
	GPJ0	I	EC_WAKE_SCI	LOW		
VC lose	GPJ1	O	3VADSW_ON	LOW	EXT 100K PU	+3VA_EC
For 555 N/A	GPJ2	Alt	PL_REF_EC N/A	LOW		
	GPJ3	O	WLAN_PWR_EN	LOW		
For 555 N/A	GPJ4	Alt	IBAT_REF_EC N/A	LOW		
For 555 N/A	GPJ5	I	EC_GPJ5	LOW		
For 555 N/A	GPJ6	I	N/A	LOW		+3VS
For 555 N/A	GPJ7	O	N/A	HIGH		

*1: EC config GPI; Function output

Design IP Source:

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

USB3 Port

USB3_1	USB 3.0 Port 0
USB3_2	
USB3_3	
USB3_4	

PCI Express

PCIE 1 PCIE 2 PCIE 3 PCIE 4	DGPU
PCIE 5	
PCIE 6	WLAN
PCIE 9	
PCIE 10	
PCIE 11	
PCIE 12	

SATA Port

SATA 0	HDD
SATA 1A	SSD

PCI CLK

CLK0	DGPUx4
CLK1	
CLK2	
CLK3	
CLK4	
CLK5	WLAN

USB Port

USB 1	USB 2.0 Port
USB 2	USB 2.0 Port
USB 3	
USB 4	Cardreader
USB 5	
USB 6	CAMERA
USB 7	
USB 8	WLAN/BT
USB 9	
USB 10	

USB 3.0 Port 0

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

For X540UPR ADD

BOM

ASUS Project Name: X407UA/UV		Rev R1.0
Title : System Setting		
Size D	Dept.: ASUSTeK COMPUTER INC. Engineer: Brian Chen	
Date: Wednesday, March 07, 2018	Sheet 3 of 102	

Rev	Date	Description
R1.0	2016/05/26	1. Remove Q5706 2.改J3101 K/B CONN footprint 3. R7505由100k改為10k 4. Remove R7121, R7122改為4.7k
	2016/05/30	1. updated power 線路 2. Del R3833 & Add D3801 3. P.38 AUD_DVDD_IO--->AUD_DVDD 4. 更換P.55 Type-C Short Pin
	2016/06/03	1. updated power 線 路 (p.88) 2.R7505 改回100k (for +1.8vsg power up smooth) 3. R2301 R2302 R2303 上件
	2016/06/08	1. updated power 線 路 (p.87) 2. updated power 線路 (p.80) - change option
R2.0	2016/07/01	1. J4501 LBS換footprint 2. C2901 換 12 pF 3. C2505 for power sequence 4. Updated page 68, page 24 remove net
	2016/07/12	1. Change page 68 pin defined
	2016/07/13	1. Change 7/12 EMI 更動
	2016/07/21	1. updated power 線路 (p.84, p.88) 2. GPU PCIE change for Gen 2 3.Remove R7114 , R7505 change 10k 4. R3204 換1M, R3205上件
	2016/09/29	1. change CAP voltage rating (p.37)
X540UPR R1.0	2017/03/28	• 更新Block Diagram (page 1) • 新增U42 / U22 colay power plane(+VCCCORE/+VCCGT)切換線路 (page 6) • 新增 24M XTAL 預留線路 for U42 (page 9) • GCLK generator換料 (page 29) • PCH 24M clock 改由 GCLK輸入 (page 9, 29) • power更新線路for U42 (page 78, 80, 81, 91) • ESD pool建議用料更換 (page 55)
	2017/03/29	• 更新SVID / VCCCORE / VCCGT / VCCSA sense pin name (page6)
	2017/03/30	• power移除+VCCSA線路, 原+VCCSA 改為 +VCCIO_CPU (page 6, 80, 81)
	2017/03/31	• merge 2 USB port to 1ESD component (page 52)
	2017/04/05	• 新增wake on WAN預留線路 (page 30, 53)
	2017/04/07	• P_SVID_DATA_X2(Page 6) 改為P_SVID_DATA_50OHM_X2
	2017/04/11	• C1067 改為上件 C1065 改為不上件 (Page 10)
X506NA X506UA R1.0	2017/05/08	• Remove ODD (moidify IO) (Page 68) • Remove Carder Reader /direct connect from PCH (Page 42) • ADD M.2 SSD Schematic refer UX310UV (Page 51) • Modify Wlan connector / Schematic refer UX310UV (Page 53)
	2017/05/09	• Modify R2430,R3079,R2635,R2810 from 0 Ohm to Shortland for cost • Reduce Wake on WLAN Solution (Page 53) • Modify DDR to 2SO DIMM refer X542UQ_PR_0327
	2017/05/10	• Follow X542UA_R1.0 #79, Remove PM_EXTTS#0 & R3091 (page 30) • Remove D3602 (Page 36) • All Discharge BOM to @ (Page 57) • Audio A/D GND left one 0 ohm at SR (Page 36)
	2017/05/11	• remove C3605/C0603/C3606/3602 these cap already had near Pin side (Page 36)
	2017/05/12	• Change R4515/R4516 to shortland(SL4507/SL4508) (Pahe45) • Change R3619 to short land SL3607 (Page 36) • Modify R5309 to Shortland SL5309 (Page 53) • BT/WLAN ON OFF Follow X452UQ PR (Pae 53) • For SDCX; SD_RCOMP need PD 200Ohm(Page22) • ADD Cardreader power solution, and PU/PD resistor move to PCH side • Del R0303 for better placement /Change R0307 to @ for No Port B at X506UA •DDR_PG_CTRL PU change to +3VS /Del R0408 refer UX310 X452UQ (Page 4) •Modify R4803/R4804/R4805/R4806 to @ RN4801/RN4802 to 0ohm (Page 48) • Change RN2401/RN2402 to R2435~R2440 No use CLK REQ be @ (Page 24) • Change RN2502 to R2560/R2561(Page 25) for Cost • remove R2505 ,power sequence will be check in X506 SR (page 25) • ADD FingerPrint Function • Remove RN2104 /RN2103 refer UX310/X542UQ/Z450. • Remove R2196 for X506 No oDD
	2017/05/15	• Remove R2135 refer X542UQ • Remove R2161/R2161 • Remove C6920 & NET:SATA0_DEVSLP (Page23/69) • Remove R2310/R2308 • Change R2301 to SL2321 , • Add F4502 reserve (Page 45) • Add USB EMCF (Page 52) • Remove C6920 for X506UA/UV no ODD • Remove EDP TX2/TX3 (Page 45) • Add Touch panel I2C • Change J4201 PN to 12023-00015200 /add R4203 (page 42) • UPADTE Poewer SCH (BAY MAX_20170515)
	2017/05/16	•modify J3101 PN to 12018-00200500 J3102 to 12018-00211200 J3701 to 12014-00711900 J6001 to 12033-00030700 J6002 to 12020-00025600 J6002 to 12003-00072200
	2017/05/17	• modify U4503/U4201 to 06016-01100000 • Add TPanel_INT# inJ4501.33 • Add R4505 for SD_PWR_EN_# • Modify R0607/R0608 to JP0607/JP0608
	2017/05/18	• Update power SCH (X540UVK_MB_20170517_U22) • Modify Q4807 to 07G005107010 (N-MOSFET EM6K1GT2R EMT6)
	2017/05/19	• Rmove L5233 /L5204 /L5210 /SLN5213 /RN5203 /RN5201 for EMCF had reserve
	2017/05/24	• Modify Edp trace shortland location • Modify RN4811 PU to +5VS_HDMI_CRT
	2017/05/25	• Update Power SCH (X540UVK_MB_20170525_1350_U22)
	2017/05/26	• Remove R0602/R0603 JP0607/JP0608 / modify VCCSA power net
	2017/05/31	• Update Power SCH (X507_MB_20170531_1350_U22)
	2017/06/01	• Modify D6901 to D4502 • ADD SATA0 DEVSLP function • remove U42 XTAL@ page 9
	2017/06/05	• remove Q4501 /R4511/R4501/C4503
	2017/06/06	• DDR SWAP follow Layout : ddr_swap_1404 • ADD J6802/C6809/C6810 for USB IO Board
	2017/06/07	• Update X507_MB_20170607_1050_U22 • Modify GPU Power CAP • Modify L4504/4509/4510 L5206/L5209 to temp_T_001687 • Modify C2623 : 22UF from 11G235222625390 to 11G233222625320
	2017/06/08	• ADD USB IO Board Page.66
	2017/06/09	• X507_MB_20170609_1426_U22
	2017/06/12	• Change VRAM to GDDR5 256M X32 refer X542UQ • X507_MB_20170612_1856_U22
	2017/06/13	• X507_MB_201706131014_U22 • Change connector follow connector list
	2017/06/14	• Modify TPanel_INT# to J4501 pin28
	2017/06/15	• MOVE I2C2_SDA_TCHPANEL/I2C2_SCL_TCHPANEL from GPP_F4/5 to GPP_C16/17 • Remove R2142 • Remove C1730
	2017/06/16	• Update J4201 to 12023-00025900
	2017/06/20	• Remove USB2.0 port 3

BOM

ASUS Project Name: X407UA/UV	Rev
Title : System History	
Size: D — Dept.: ASUSTeK COMPUTER INC. Engineer:	
Date: Wednesday, March 07, 2018	Sheet 103 of 102