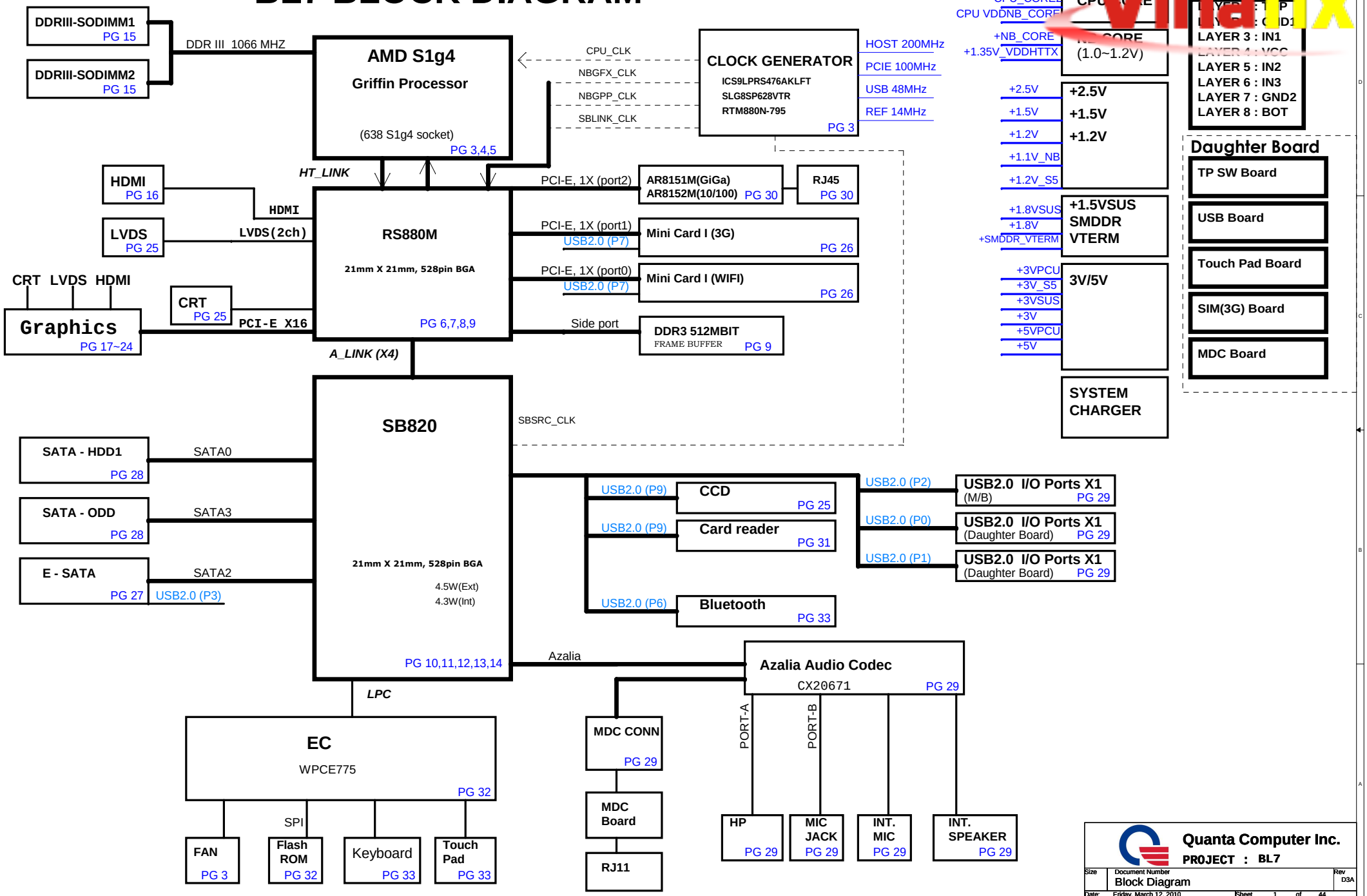
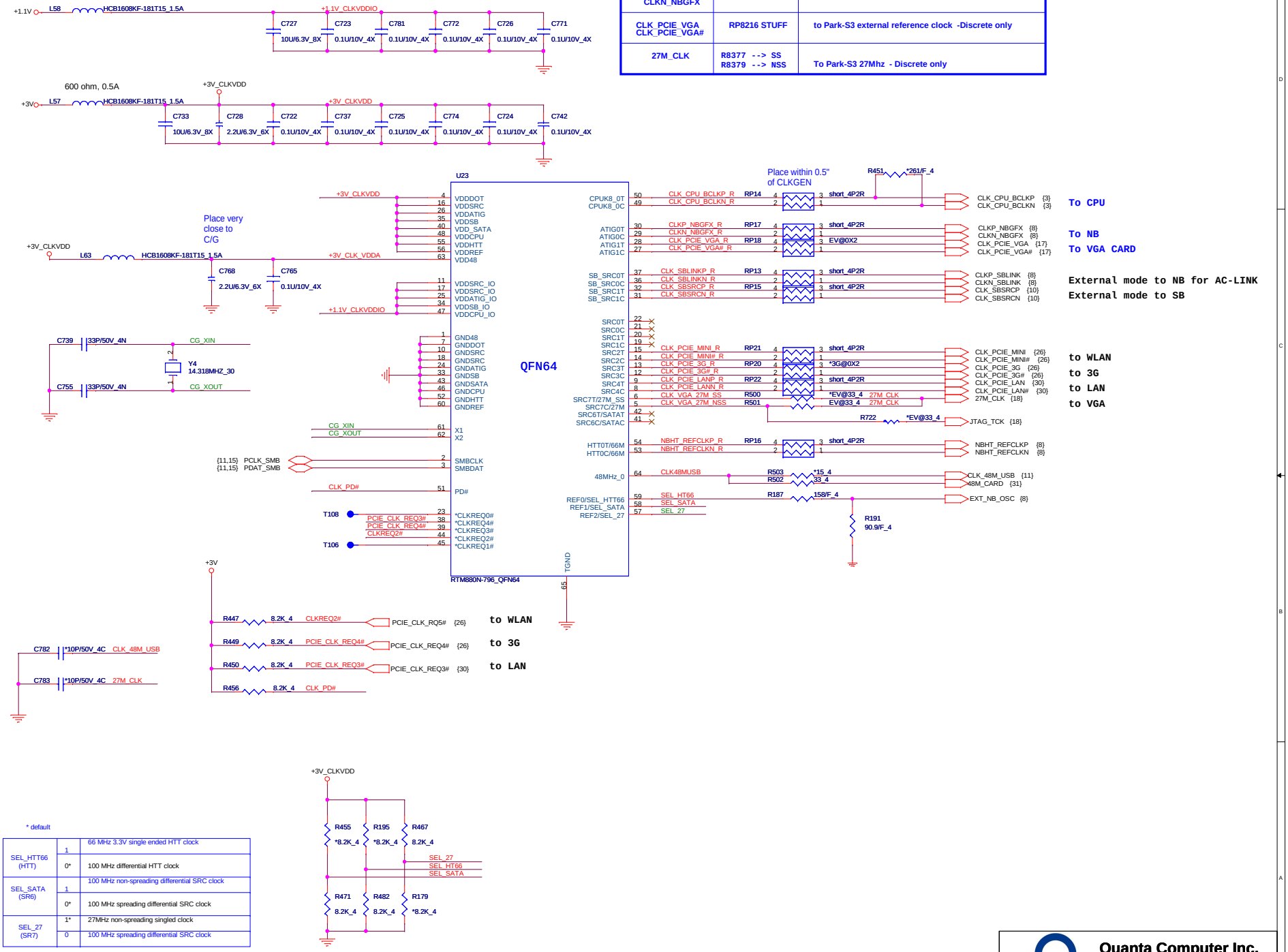
BL7 BLOCK DIAGRAM



CLOCK GENERATOR

02

CLOCKS name	Discrete	Clock pin function
CLKP_NBGFX CLKN_NBGFX	RP8217 STUFF	to NB for VGA reference clock
CLK_PCIE_VGA CLK_PCIE_VGA#	RP8216 STUFF	to Park-S3 external reference clock -Discrete only
27M_CLK	R8377 --> SS R8379 --> NSS	To Park-S3 27Mhz - Discrete only



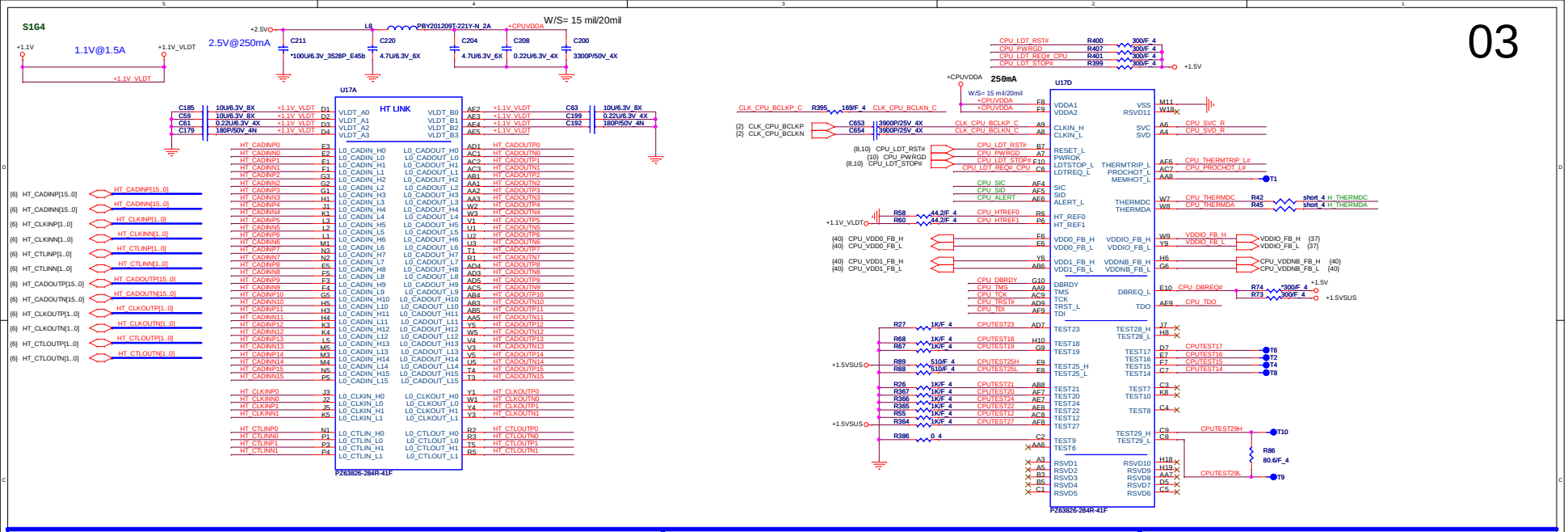
* default

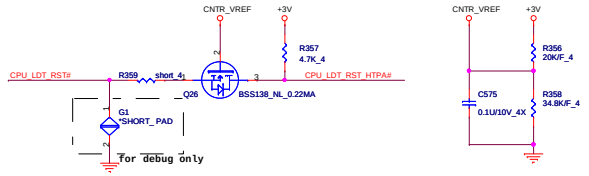
SEL_HTT66 (HTT)	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA (SR6)	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27 (SR7)	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

Quanta Computer Inc.

PROJECT : BL7

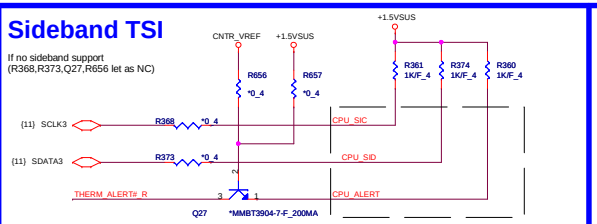
Size	Document Number	Rev
	Clock Gen	D3A
Date: Friday, March 12, 2010	Sheet 2 of 44	



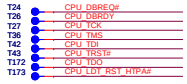


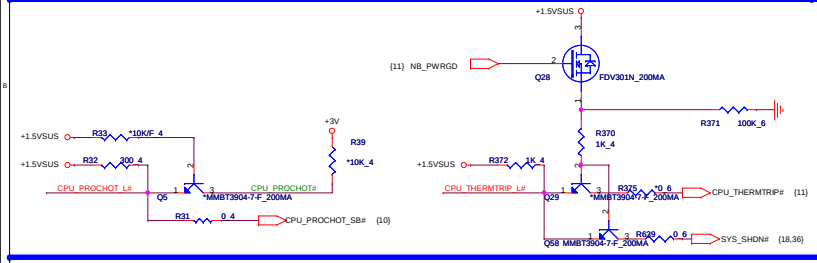
Sideband TSI

If no sideband support
(R368,R373,Q27,R656 let as NC)

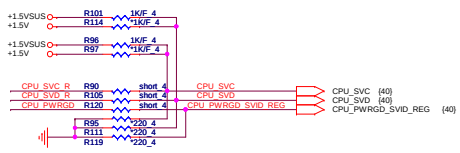


HDT(Hardware Debug Tool) Connector





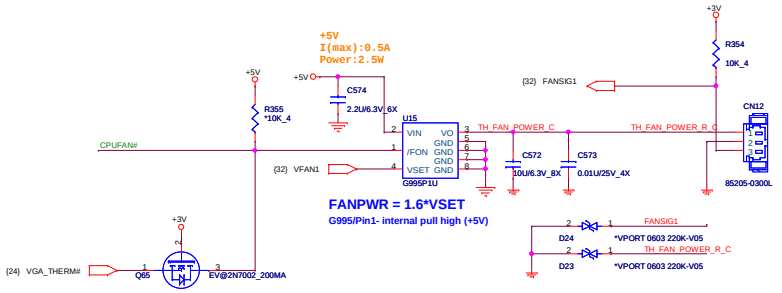
Serial VID



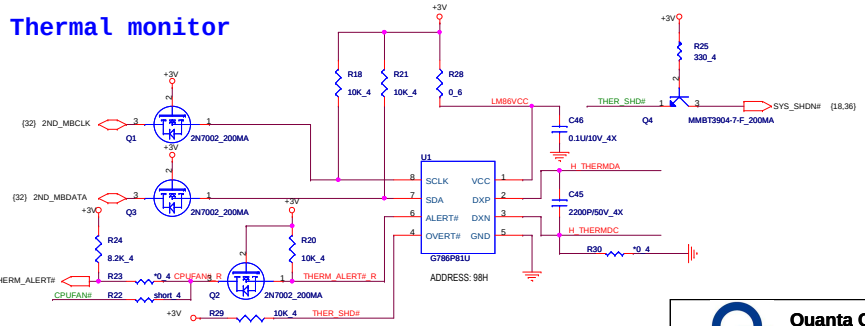
VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPU FAN



CPU Thermal monitor



Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	S1G2 HT,CTL I/F 1/3	D3A
Date: Friday, March 12, 2010	Sheet 3 of 44	

Processor Memory Interface

04

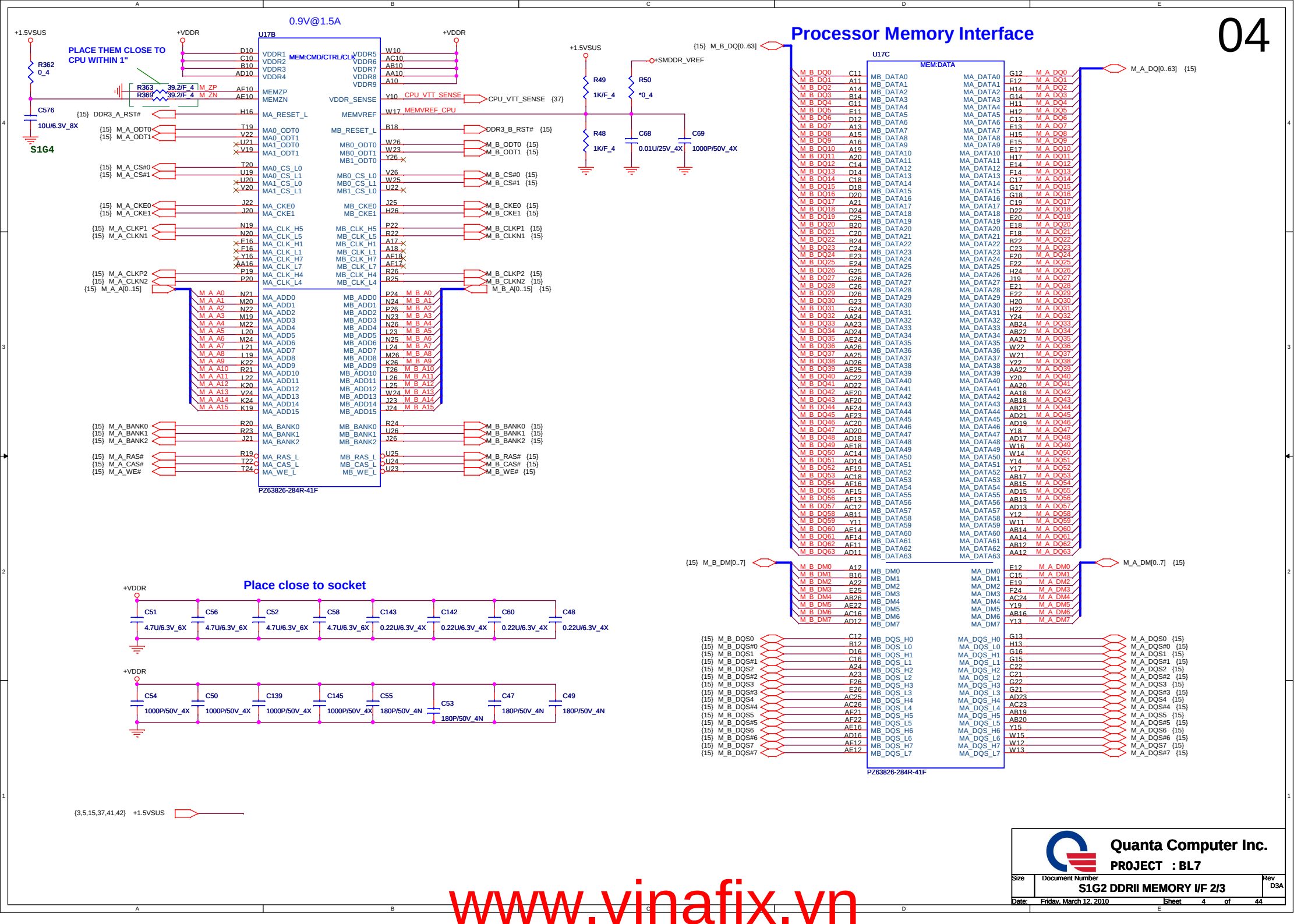
0.9V@1.5A

PLACE THEM CLOSE TO CPU WITHIN 1"

U17B — MEM:CMD/CTRL/CLK — PZ63826-284R-41F

U17C — MEM:DATA — PZ63826-284R-41F

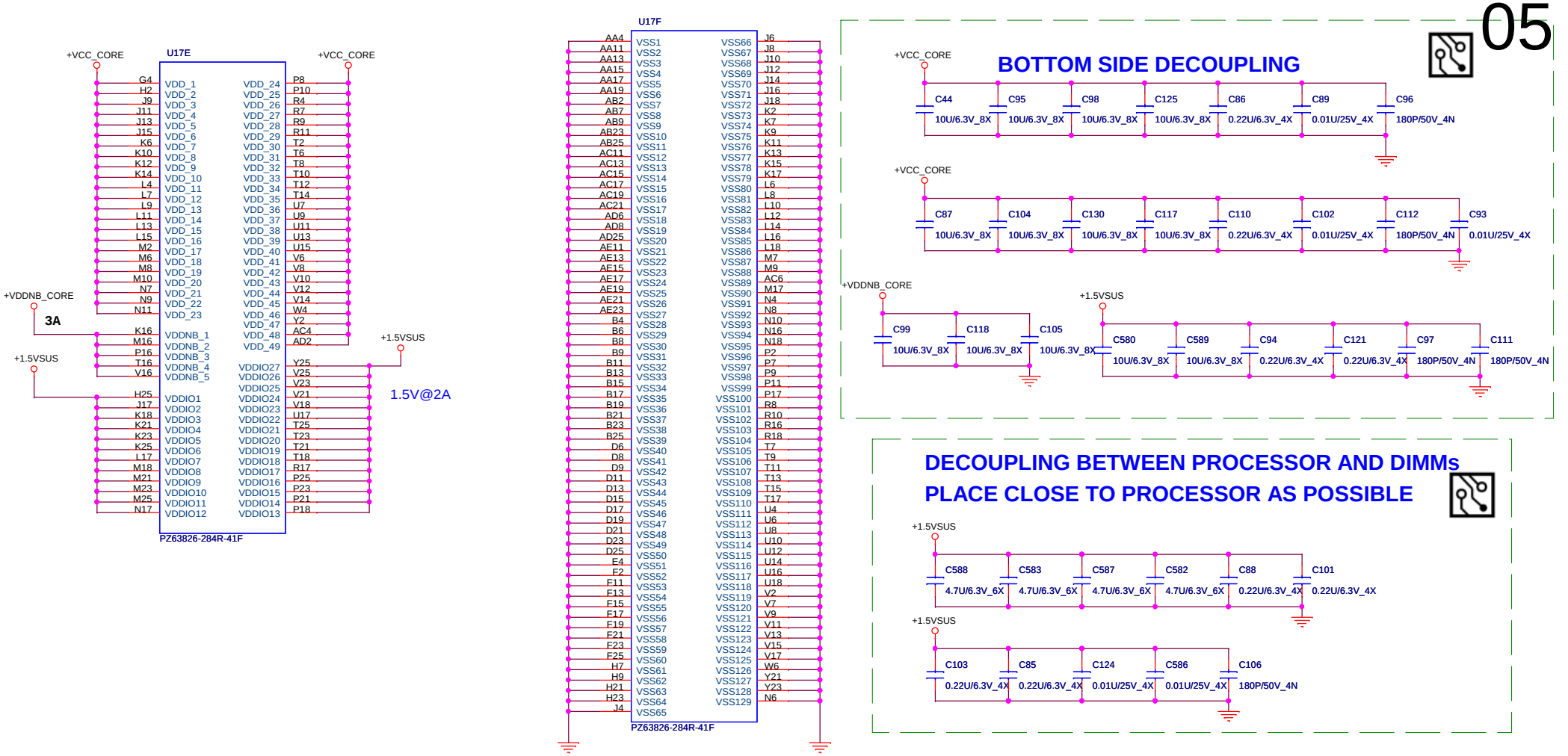
Place close to socket

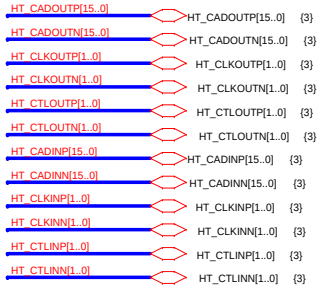


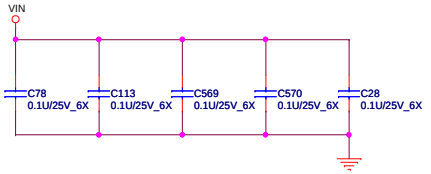
Quanta Computer Inc.

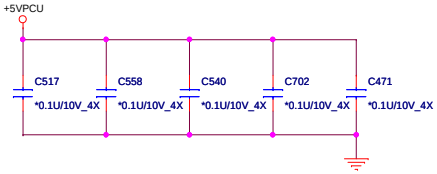
PROJECT : BL7

Size	Document Number	Rev
	S1G2 DDRII MEMORY I/F 2/3	D3A
Date: Friday, March 12, 2010	Sheet 4 of 44	



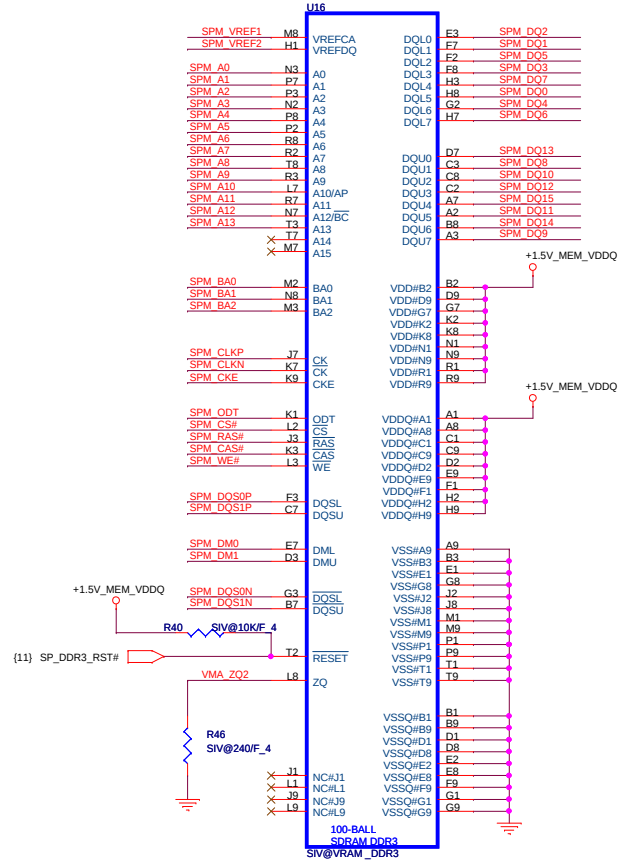


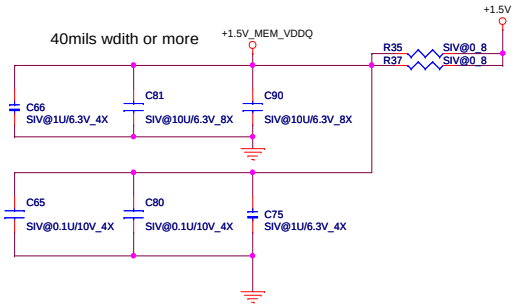


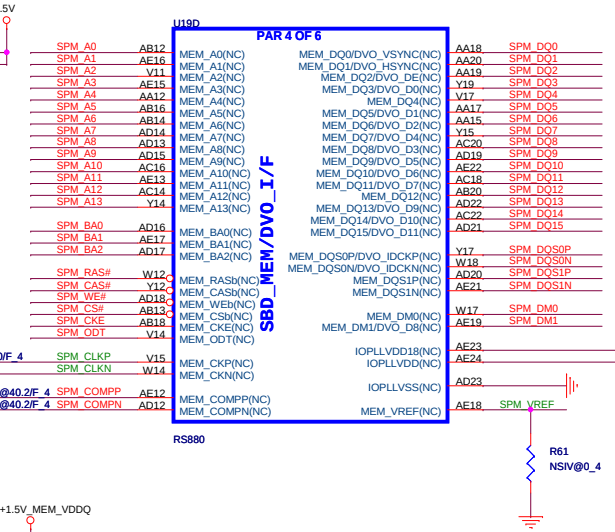


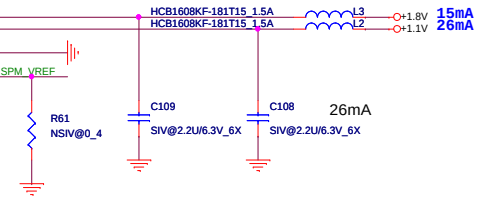
Memory Side Port

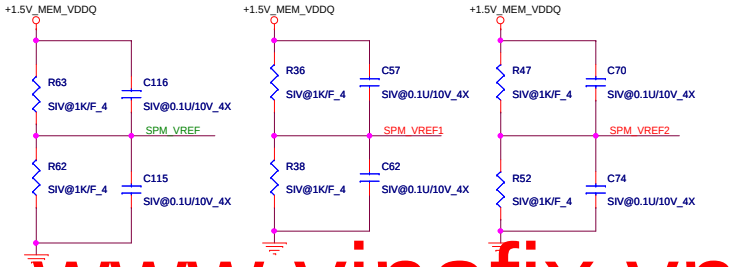
This block is for UMA only . Discrete can remove all component



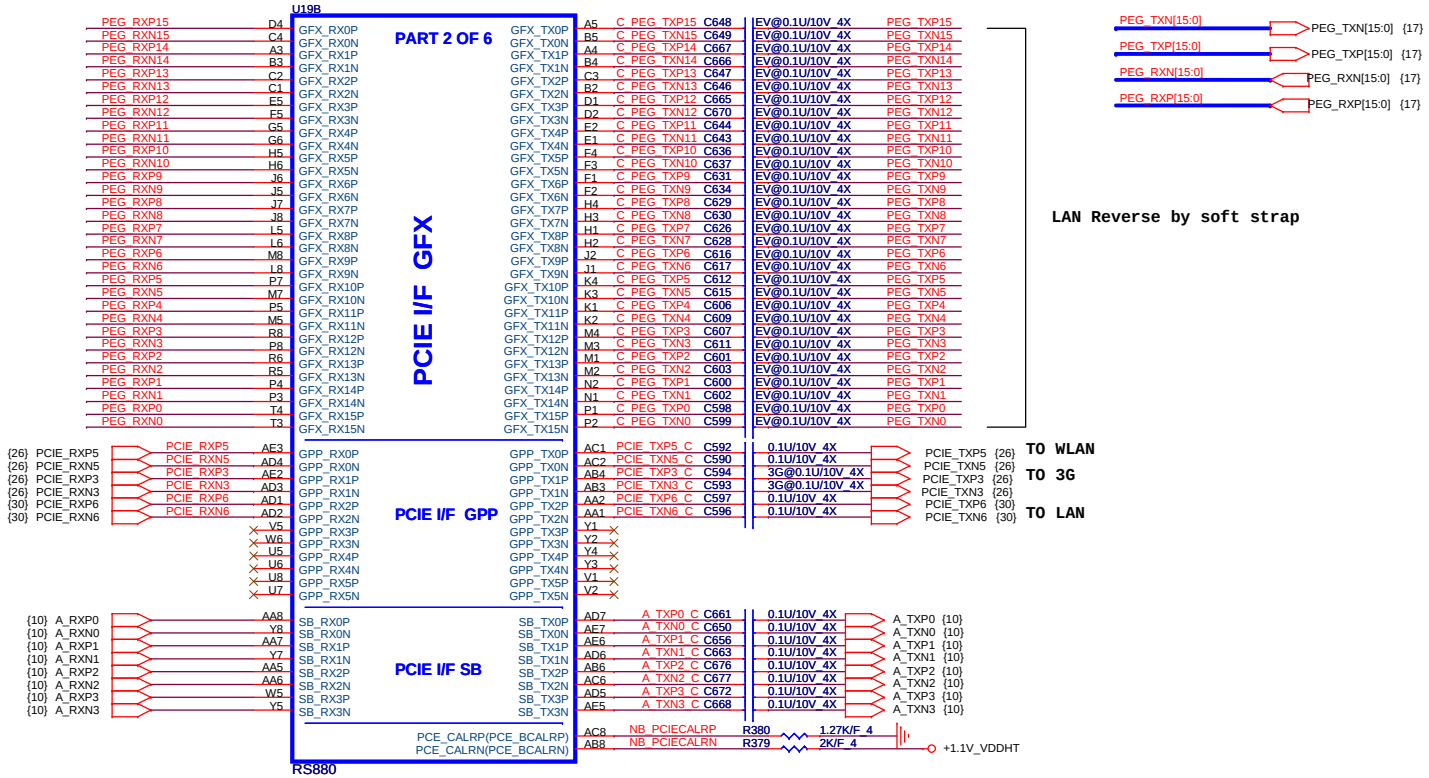


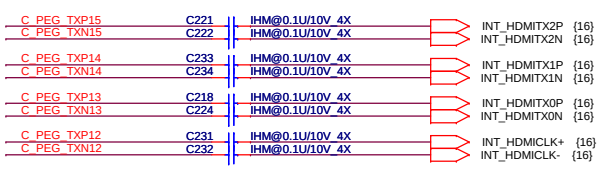




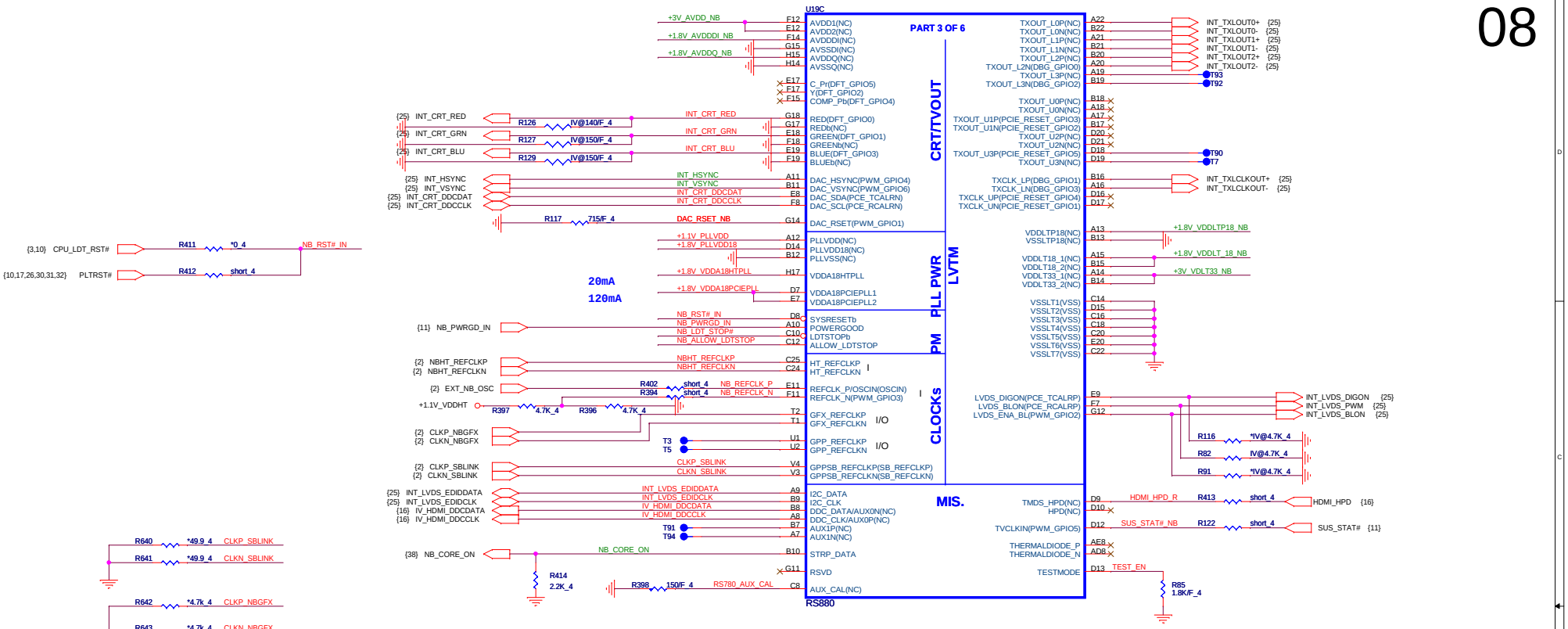


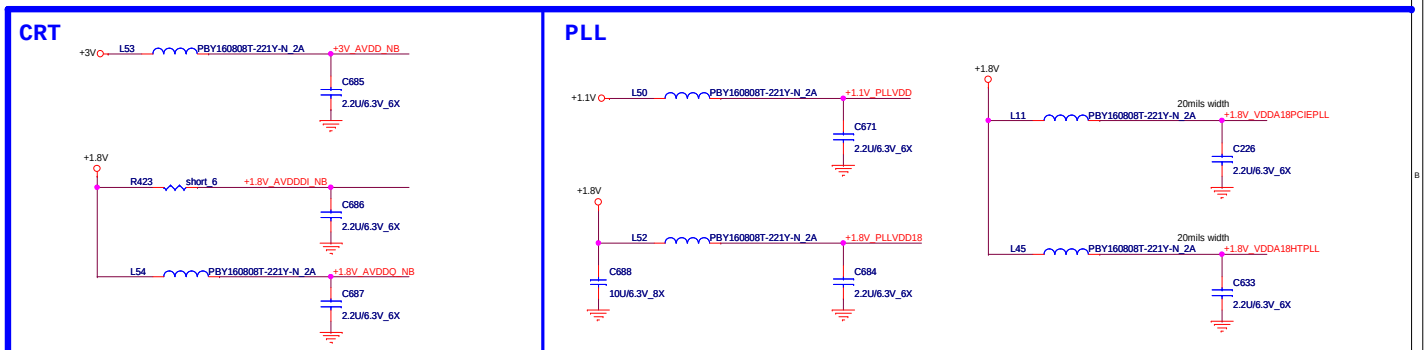
Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: RX881-HT LINK I/F 1/4	Rev: D3A
Date: Friday, March 12, 2010	Sheet 6 of 44	

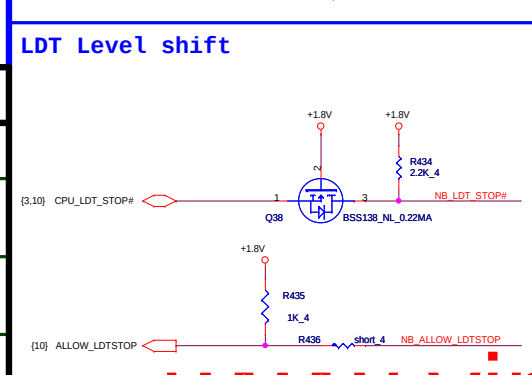


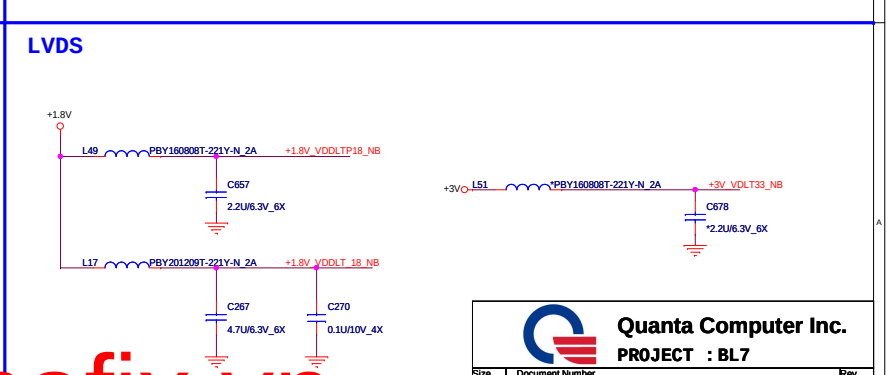


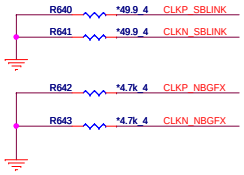
Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: RX881-PCIE I/F 2/4	Rev: D3A
Date: Friday, March 12, 2010	Sheet 7 of 44	











RS880M Strapping

Function	Setting
EEPROM Strap 0-->Enable 1-->Disable	R121 *3K/F_4 — R123 3K/F_4 — SUS_STAT#_NB — +3V
Debug Bus 0-->Enable 1-->Disable	R403 *3K/F_4 — R404 3K/F_4 — INT_VSYNC — +3V
Sideport Enable 0-->Enable 1-->Disable	R406 SIV@3K/F_4 — R405 NSIV@4.7K/F_4 — INT_HSYNC — +3V

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	RX881-SYSTEM I/F 3/4	D3A

Date: Friday, March 12, 2010 Sheet 8 of 44

U19F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RS880 POWER DIFFERENCE TABLE

PIN NAME	RS880	PIN NAME	RS880
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

U19E

PART 5/6

POWER

RS880

+1.1V

0.6A L1 short_8 +1.1V_VDDHT

C119 4.7U/6.3V_6X C176 0.1U/10V_4X C120 0.1U/10V_4X C166 0.1U/10V_4X

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7

0.7A L7 short_8 +1.1V_VDDHTRX

C203 4.7U/6.3V_6X C206 0.1U/10V_4X C189 0.1U/10V_4X C193 0.1U/10V_4X

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7

+1.1V L5 short_4 0.4A +1.1V_VDDHTTX

C131 4.7U/6.3V_6X C158 0.1U/10V_4X C136 0.1U/10V_4X C148 0.1U/10V_4X C141 0.1U/10V_4X

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13

+1.8V L4 PBY201209T-221Y-N_2A 1.8V@0.7A +1.8V_VDDA18PCIE

C138 4.7U/6.3V_6X C134 4.7U/6.3V_6X C173 0.1U/10V_4X C151 0.1U/10V_4X C137 0.1U/10V_4X C133 0.1U/10V_4X

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15

+1.8V R87 short_6 +1.8V_VDDG18_NB 25mA

C205 1U/6.3V_4X

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2)

+1.8V R71 SIV@0_6 +1.8V_VDD18_MEM 25mA

R70 NSIV@0_4 C132 SIV@1U/6.3V_4X

VDD18_MEM1(NC) VDD18_MEM2(NC)

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC)

VDDG33_1(NC) VDDG33_2(NC)

+1.1V +1.1V_VDD_PCIE 1.1V@2.5A

C114 0.1U/10V_4X C155 0.1U/10V_4X C165 1U/6.3V_4X C160 1U/6.3V_4X C147 4.7U/6.3V_6X

R64 short_8 +1.1V_VDDHT

0.95~1.1V@10A +NB_CORE

C149 0.1U/10V_4X C153 0.1U/10V_4X C144 0.1U/10V_4X C181 0.1U/10V_4X C202 10U/6.3V_8X

C163 0.1U/10V_4X C161 0.1U/10V_4X C172 0.1U/10V_4X C212 10U/6.3V_8X

+1.5V_VDD_MEM

C135 SIV@0.1U/10V_4X C577 SIV@0.1U/10V_4X C122 SIV@1U/6.3V_4X C578 SIV@1U/6.3V_4X C581 SIV@4.7U/6.3V_6X

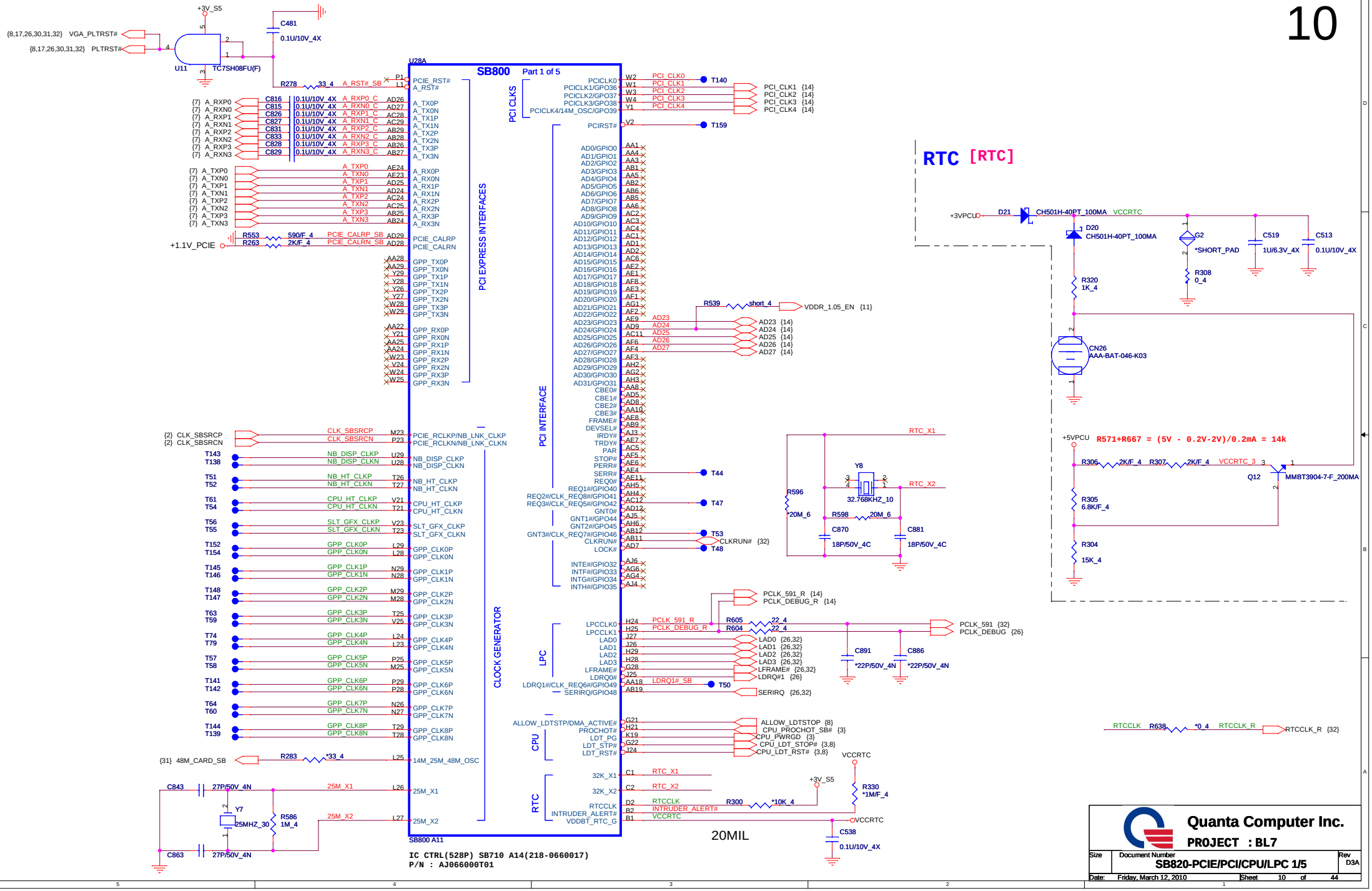
R376 SIV@0_8 +1.5V R377 NSIV@0_4

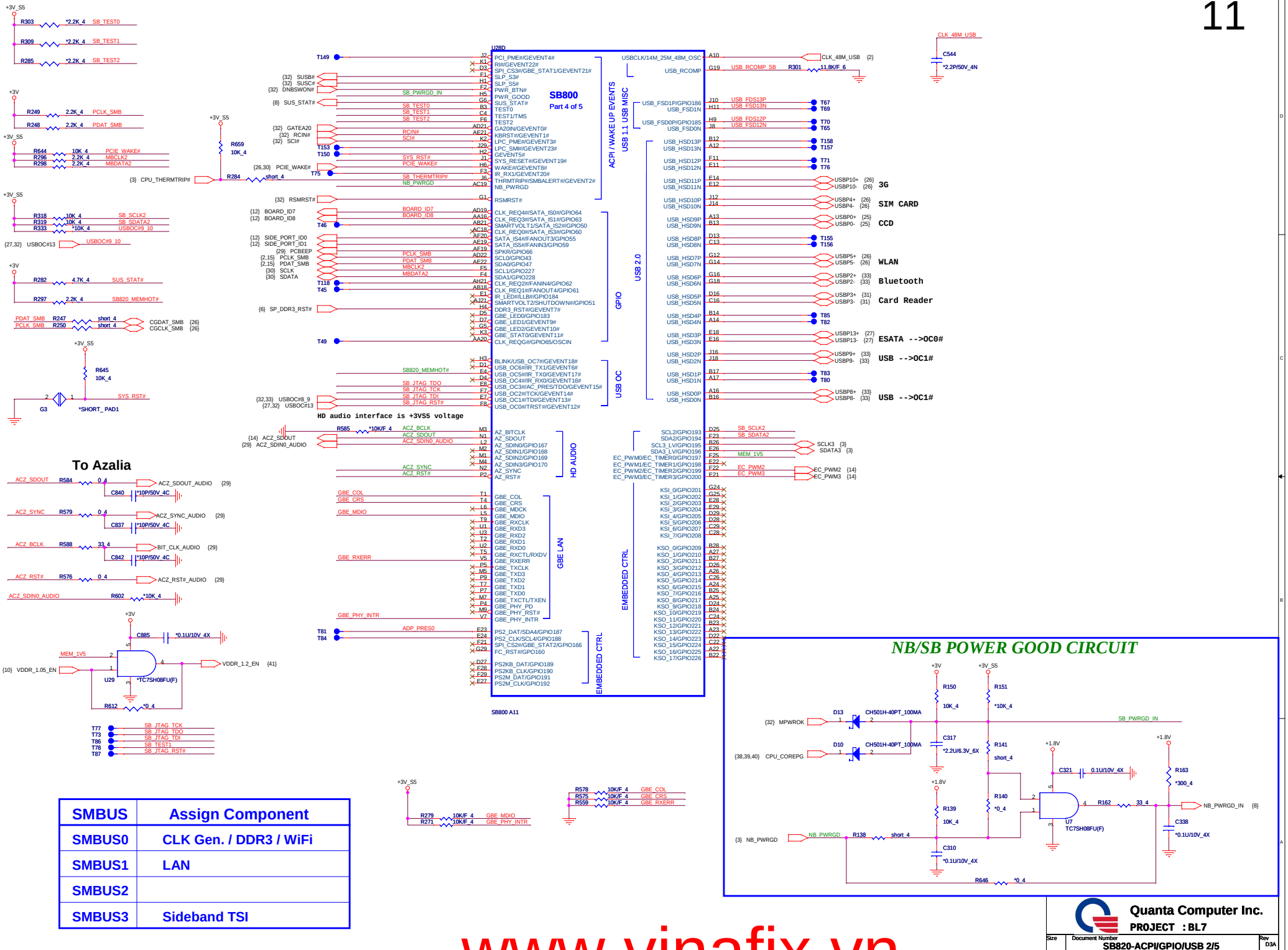
+3V_VDDG33 C146 0.1U/10V_4X C140 0.1U/10V_4X

R75 short_4 60mA +3V

VDD33 - 3.3V I/O
Not applicable to RX780

Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: RX881-POWER5 4/4	Rev: D3A
Date: Friday, March 12, 2010	Sheet 9 of 44	



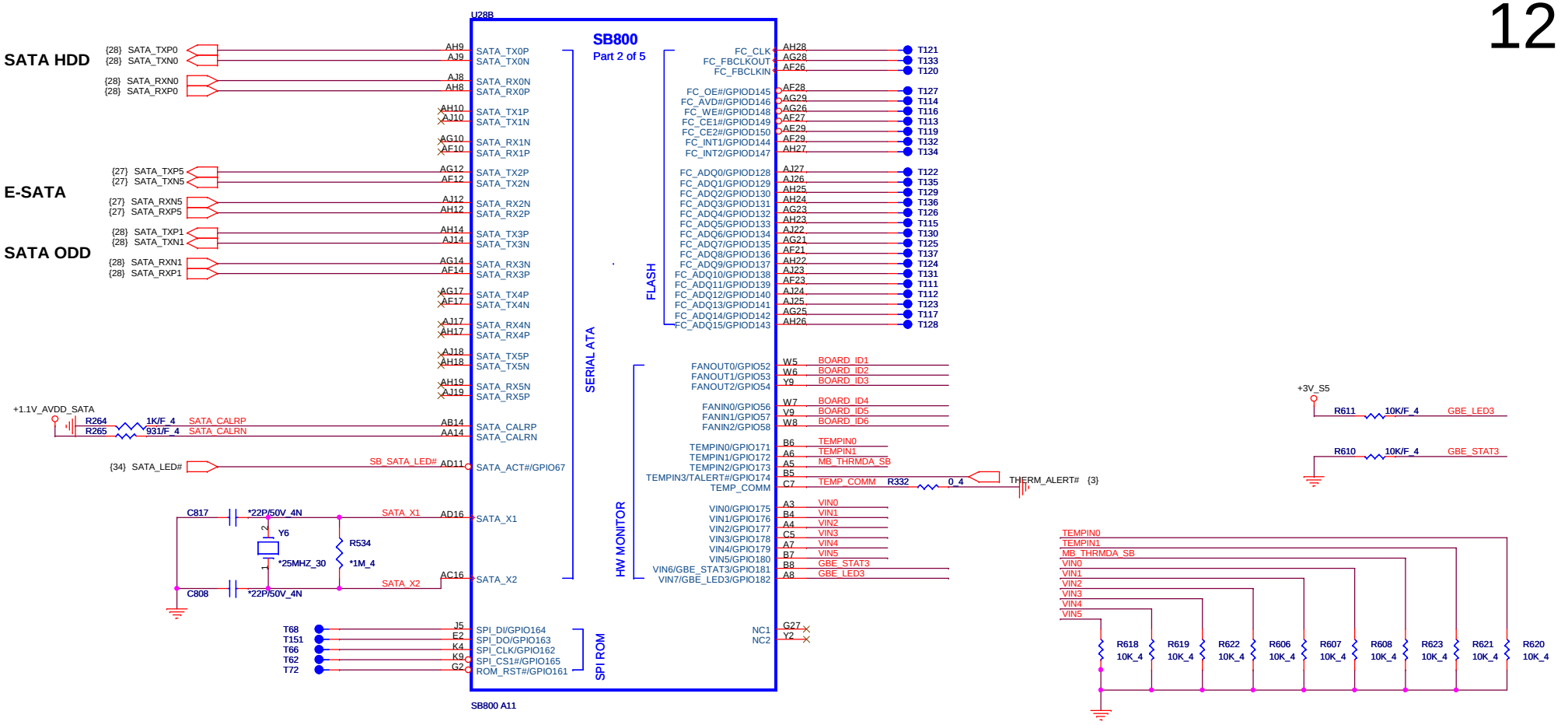


SMBUS	Assign Component
SMBUS0	CLK Gen. / DDR3 / WiFi
SMBUS1	LAN
SMBUS2	
SMBUS3	Sideband TSI

Quanta Computer Inc.
PROJECT : BL7

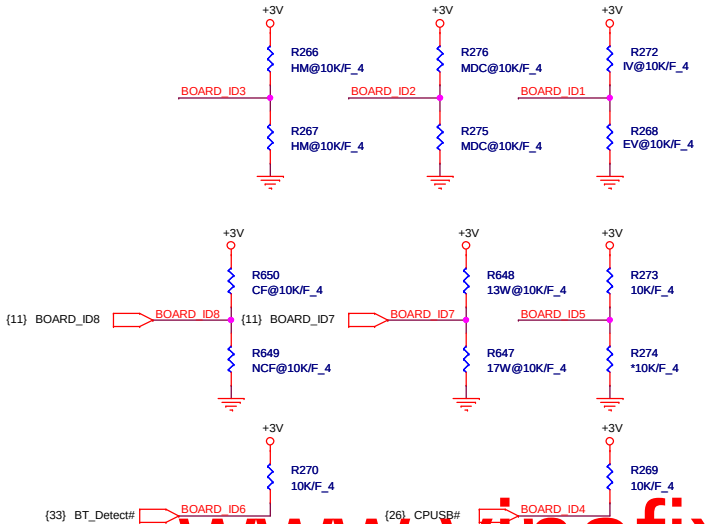
Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/5	D3A

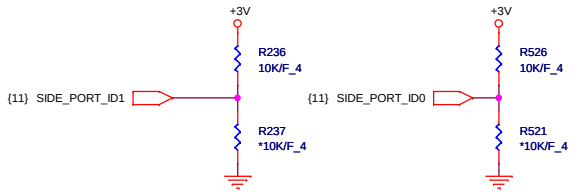
Date: Friday, March 12, 2010 Sheet 11 of 44



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8
UMA SKU VGA SKU	H L							
W/ MDC W/O MDC		H L						
W/ HDMI W/O HDMI			H L					
W/O 3G W/ 3G				H L				
15" 14"					H L			
W/O BT W/ BT						H L		
13W 17W							H L	
W/ CF W/O CF								H L



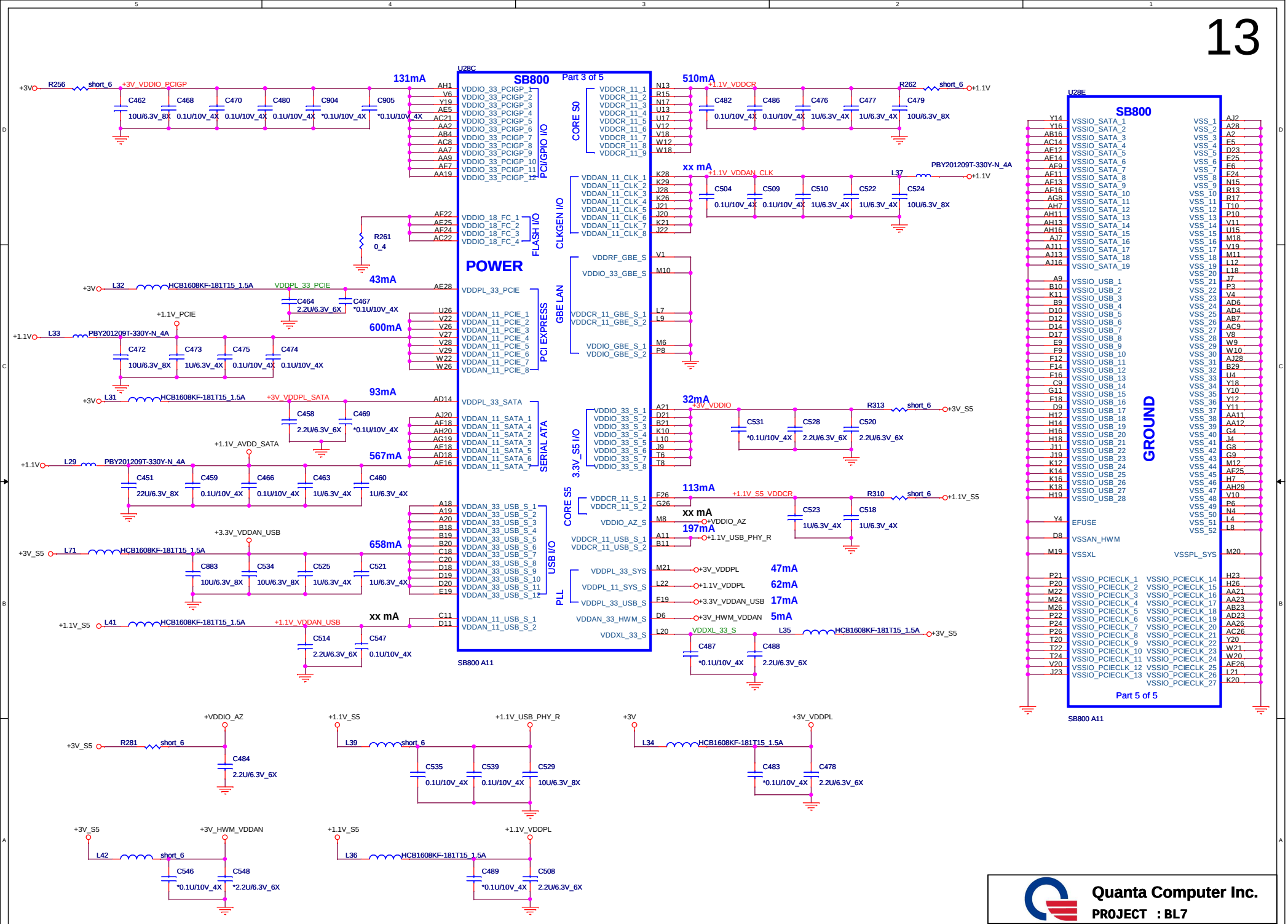


ID1	ID0	Function
0	0	Samsung
0	1	Hynix
1	0	Reserve
1	1	No sideport support

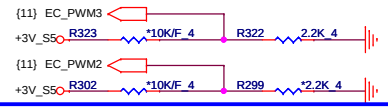
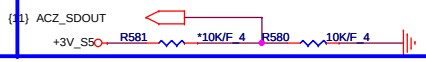
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/5	D3A

Date: Friday, March 12, 2010 Sheet 12 of 44

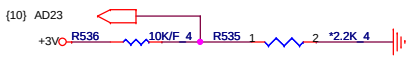


REQUIRED STRAPS

Ball Name	Strap Name	Default	Description	Setting
LPCCLK0	ECEnableStrap	0	0 -- Disable 1 -- Enable Enable to support enhanced hardware monitor feature	
EC_PWM3 EC_PWM2	ROMTYPE_1 ROMTYPE_0	(0,1)	(0,0) = Firmware Hub (0,1) = LPC (1,0) = SPI (1,1) = Reserved	
LPCCLK1	CLKGEN	0	0 -- External clock 1 -- Integrate clock	
PCICLK1	BIF_GEN2_COMPLIANCE_Strap	1	0 -- PCIE at Gen I mode 1 -- PCIE at Gen II mode	
PCICLK2	BootFailTmeEn	0	0 -- Disable watchdog function 1 -- Enable watchdog function	
PCICLK3	DefaultStrapMode	0	0 -- Disable debug Straps 1 -- Select ext. Debug Straps	
PCICLK4	CPUClksel	1	0 -- Reserved 1 -- Integrated clock mode	
AZ_SDOUT	CoreSpeedMode	0	0 -- Performance mode 1 -- Low Power mode	

DEBUG STRAPS

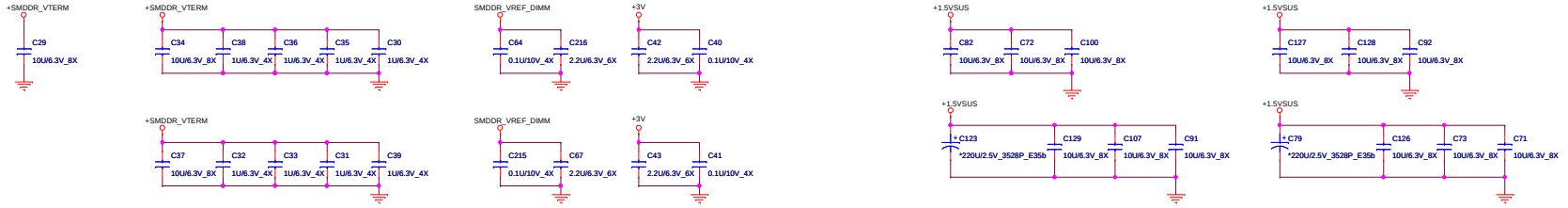
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

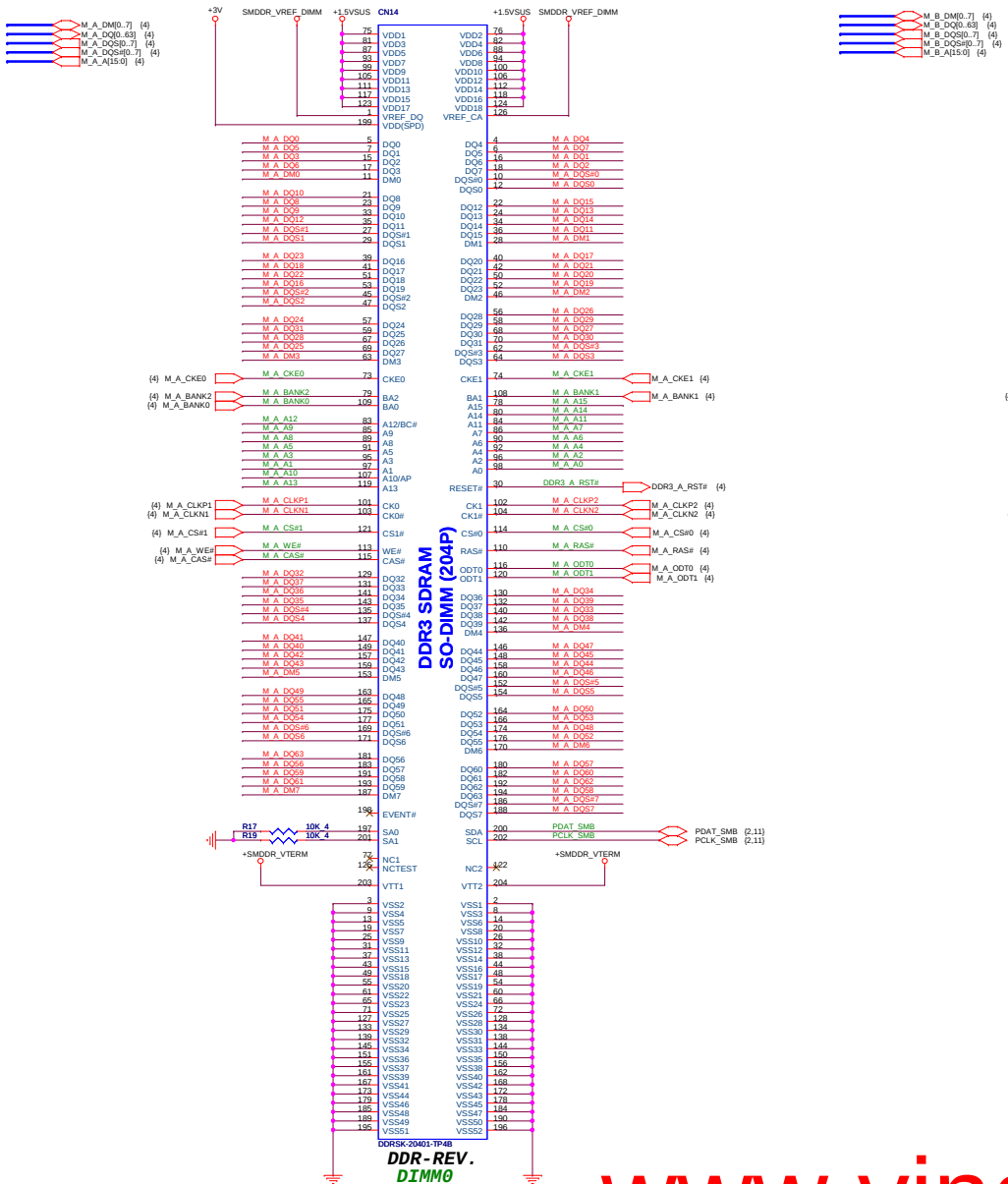
Ball Name	Strap Name	Default	Description	Setting
AD27	PciPllByp	1	0 -- ByPass Int PLL 1 -- Int. PLL	
AD26	ILAAutronEnB	1	0 - IAL auto run enable 1 -- IAL auto run disable	
AD25	FCClkByP	1	0 -- Bypass FC Clk 1 -- Int. FC Clk	
AD24	I2CRomEn	1	0 -- Enable EEPROM 1 -- Disable EEPROM	
AD23	PCI_ROM_BOOT	1	0 -- Disable PCI MEM Boot 1 -- Enable PCI MEM Boot	

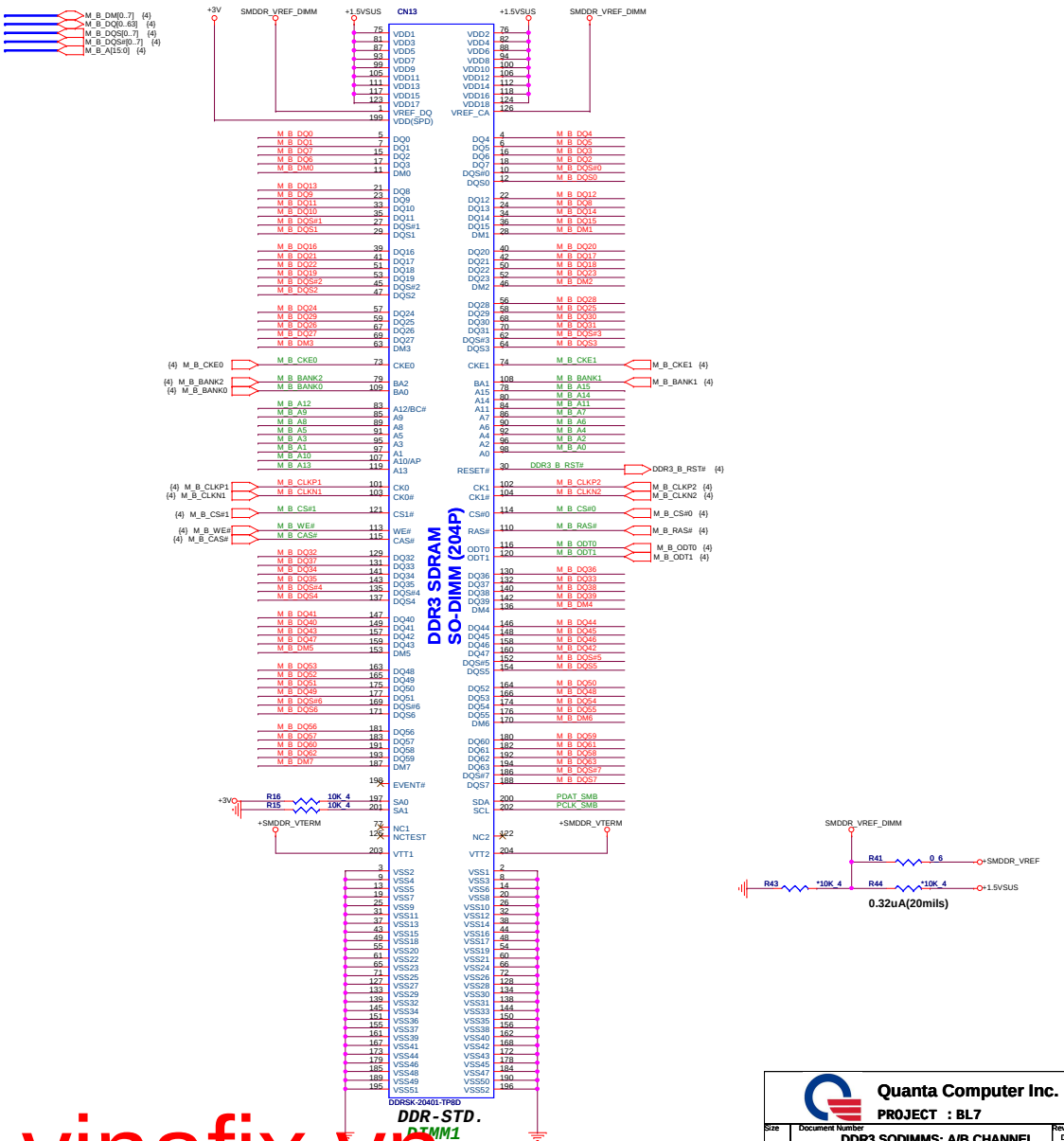
All signals ihas nternal PU

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: SB820-STRAPS 5/5 | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 14 of 44

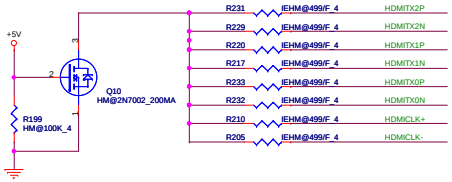
TERMINATOR DECOUPLING CAPACITOR

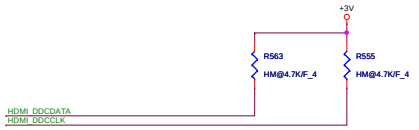


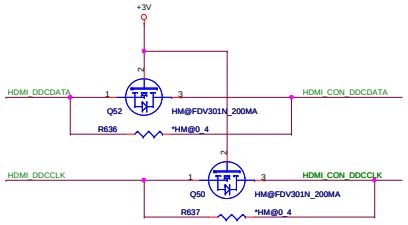




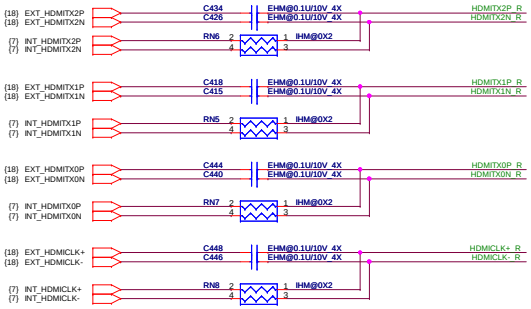
Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: DDR3 SODIMMS: A/B CHANNEL | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 15 of 44



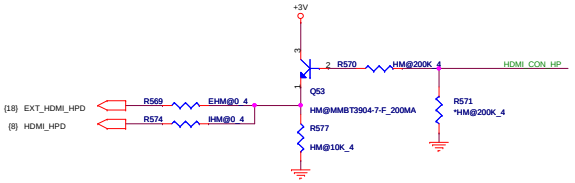


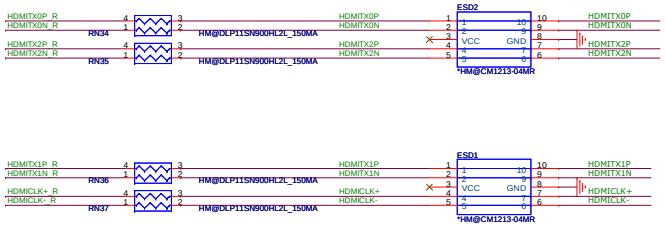


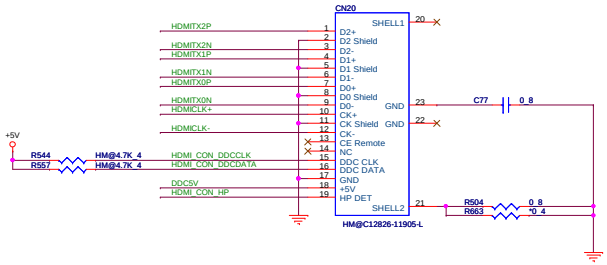
Discrete HDMI

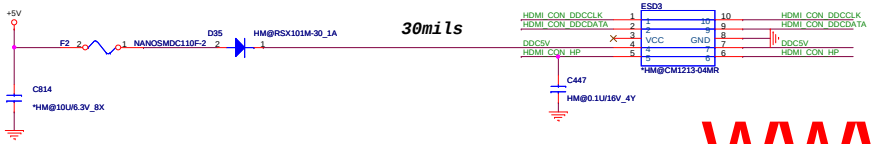


HDMI HPD





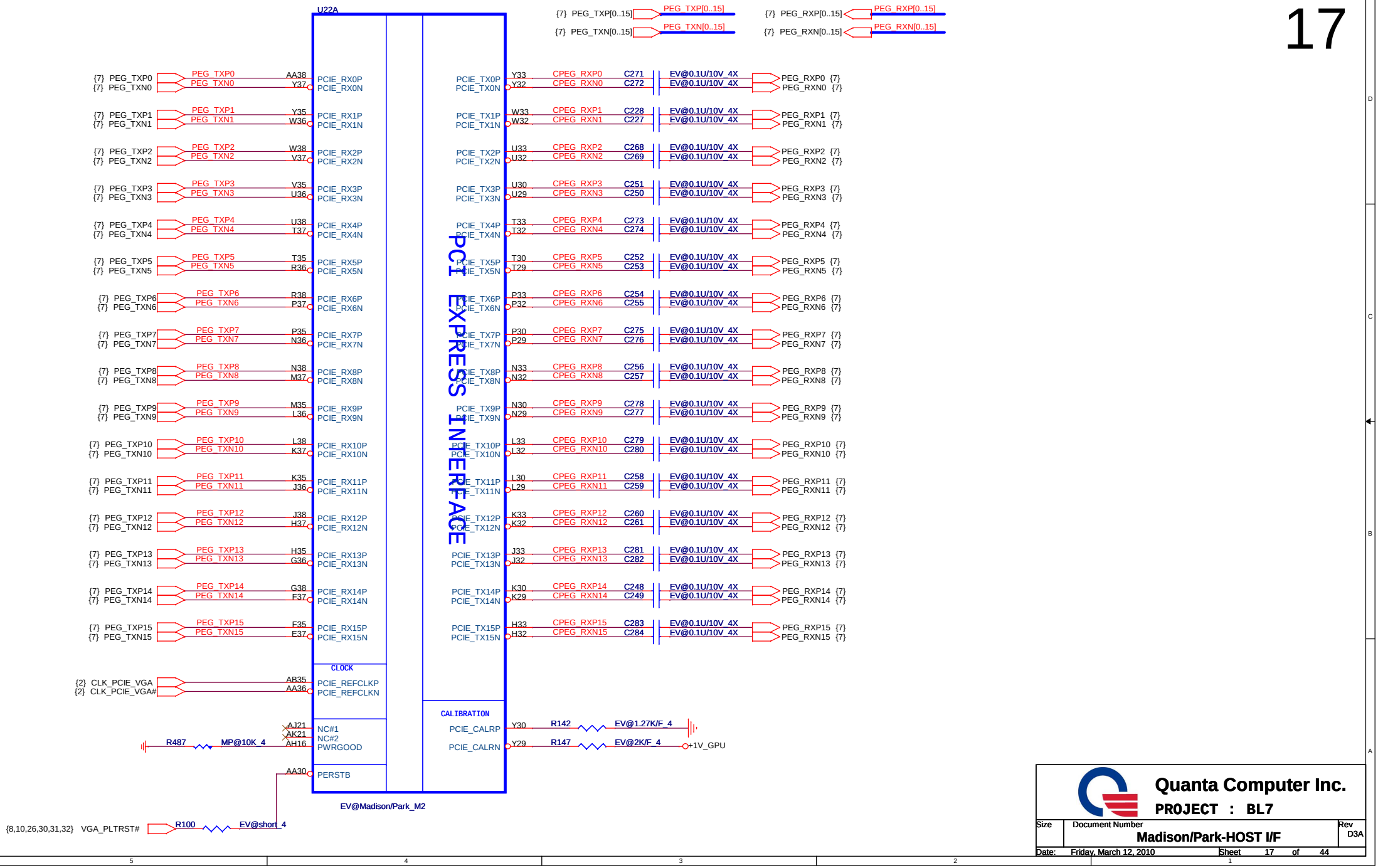




Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	HDMI CONN	D3A

Date: Friday, March 12, 2010 Sheet 16 of 44



17

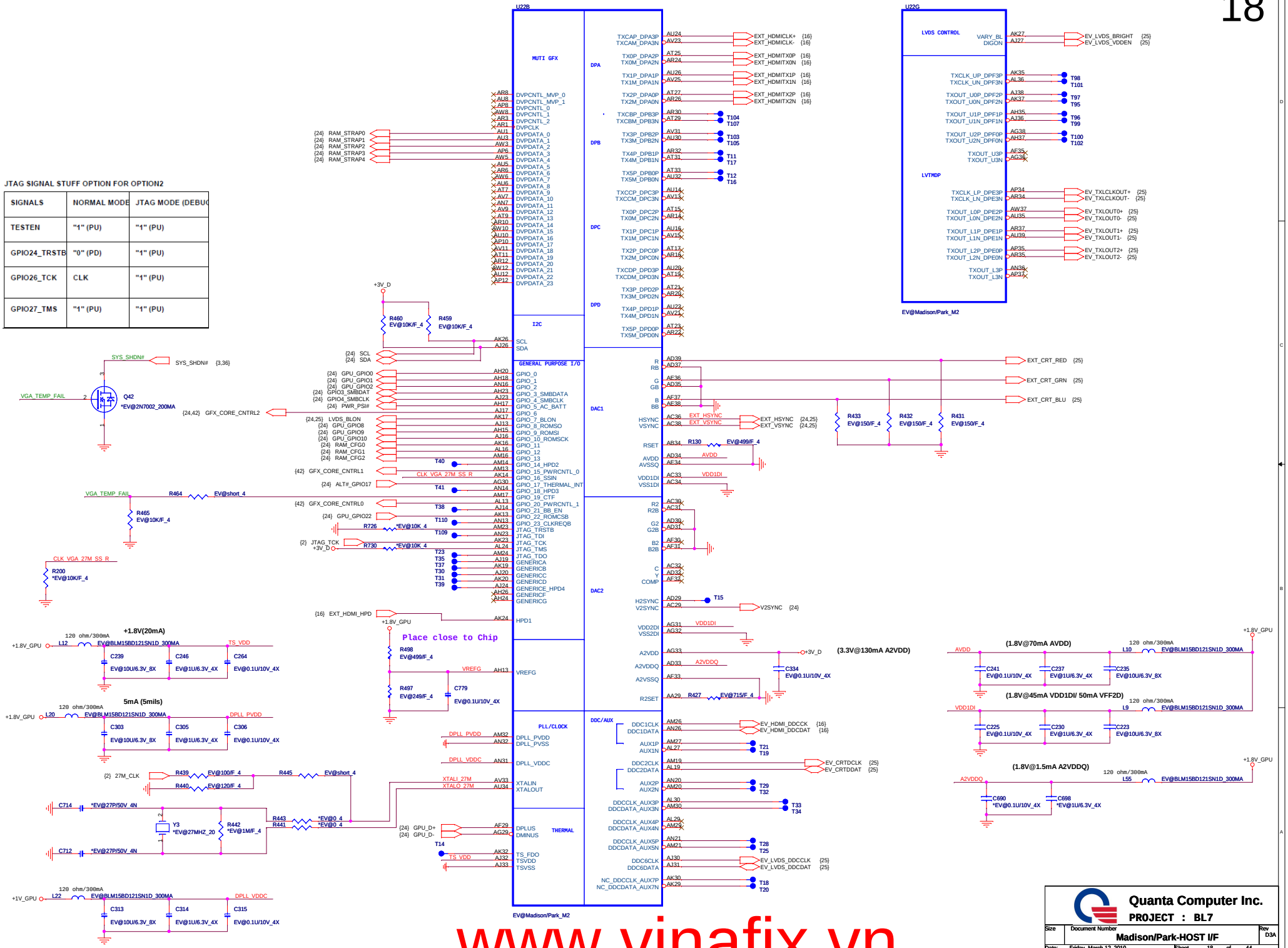
Quanta Computer Inc.

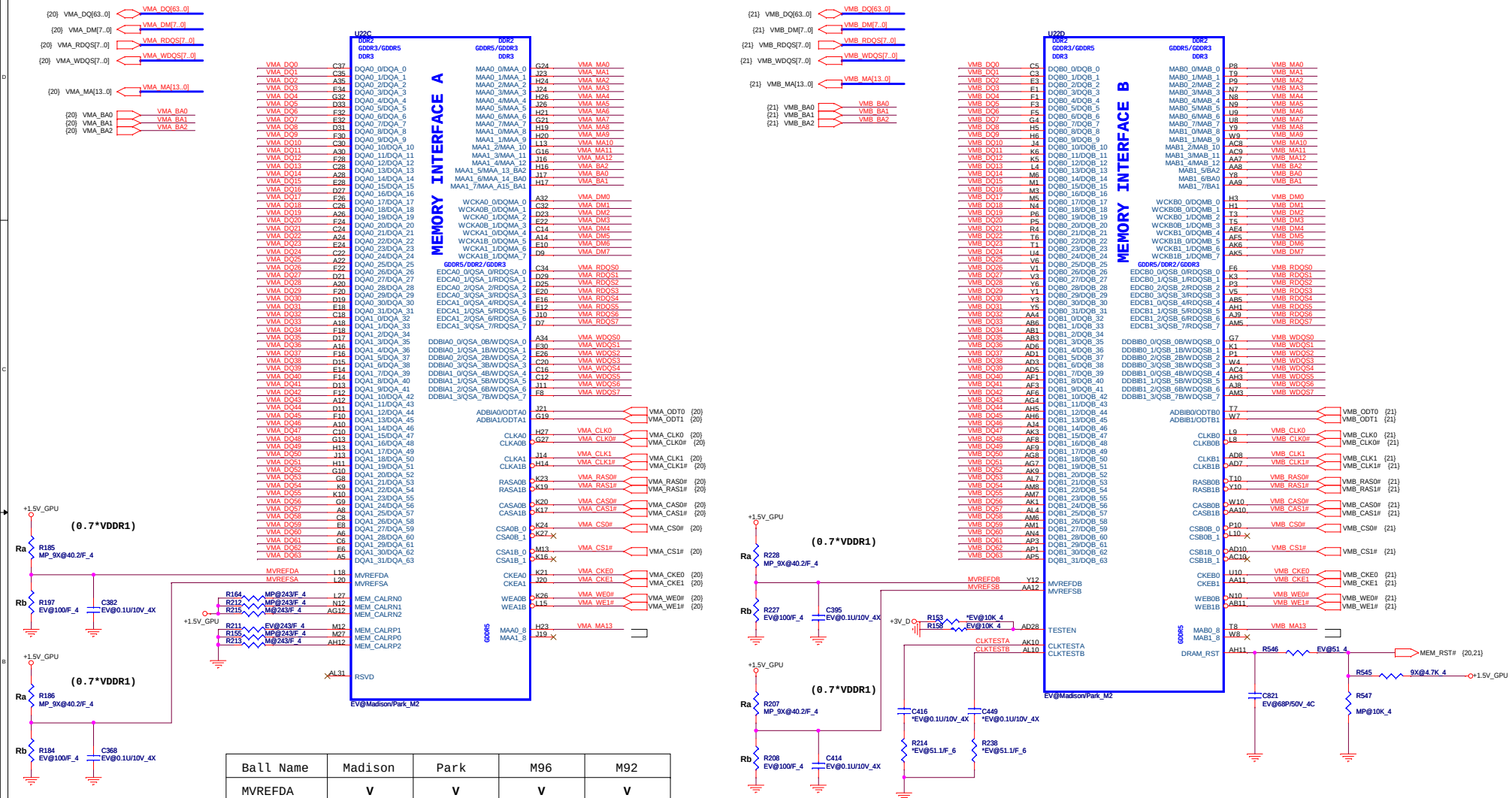
PROJECT : BL7

Size	Document Number	Rev
	Madison/Park-HOST I/F	D3A
Date: Friday, March 12, 2010	Sheet 17 of 44	

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)





DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

	Value	
	MP@	9X@
R185	40.2/F_4	100/F_4
R186	40.2/F_4	100/F_4
R207	40.2/F_4	100/F_4
R228	40.2/F_4	100/F_4

Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: Madison/Park-MEM I/F | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 19 of 44

CHANNEL A: 512MB DDR3 (64M*16*4pcs)

{19} VMA_DQ[63..0] — VMA_DQ[63..0]
{19} VMA_DM[7..0] — VMA_DM[7..0]
{19} VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
{19} VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]
{19} VMA_MA[13..0] — VMA_MA[13..0]

TOP Left | BOT Left | BOT Right | TOP Right

Group-A0 VREF

Group-A1 VREF

MEM_A0 CLK

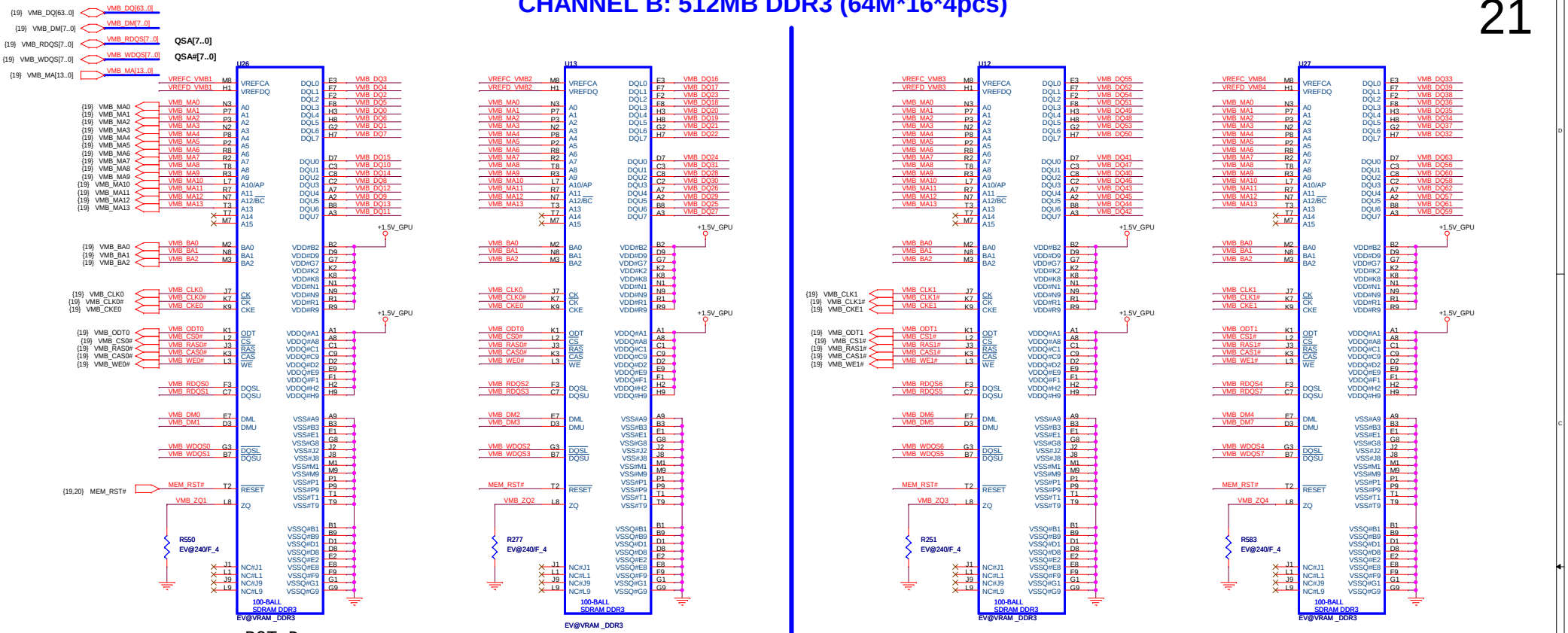
Group-A0 decoupling CAP

Group-A1 decoupling CAP

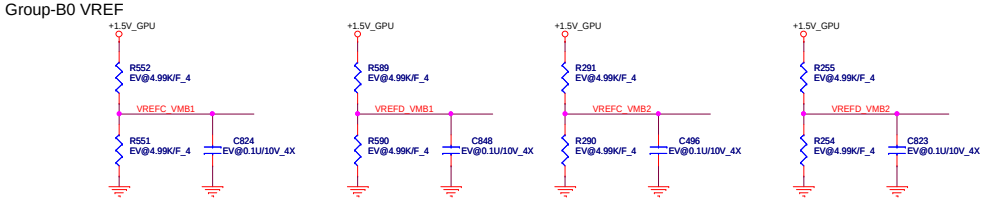
MEM_A1 CLK

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: VRAM_A: DDR3-64M*16*4PCS | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 20 of 44

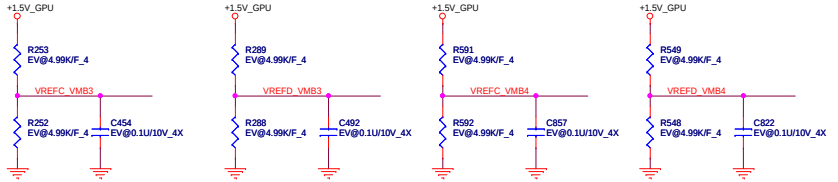
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



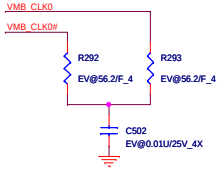
Group-B0 VREF



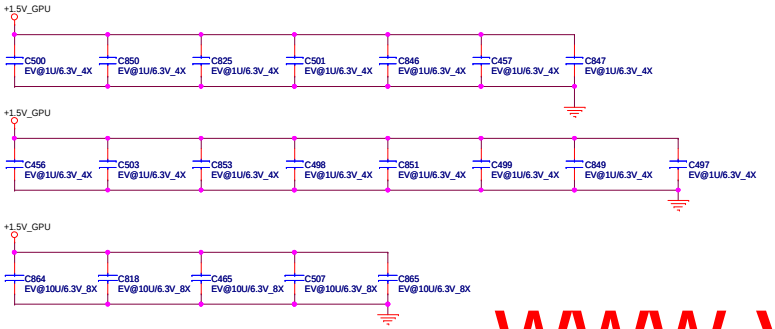
Group-B1 VREF



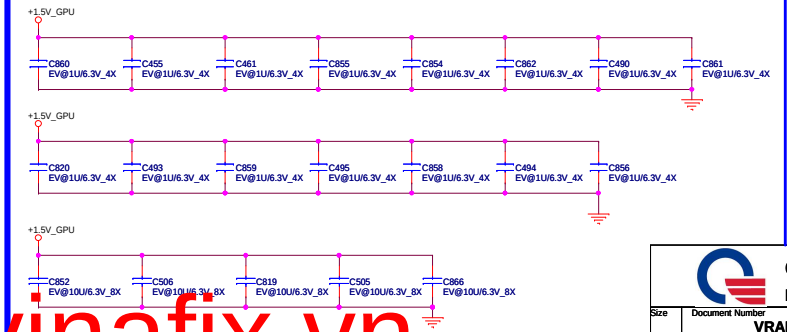
MEM_B0 CLK



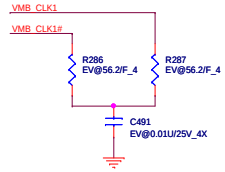
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK

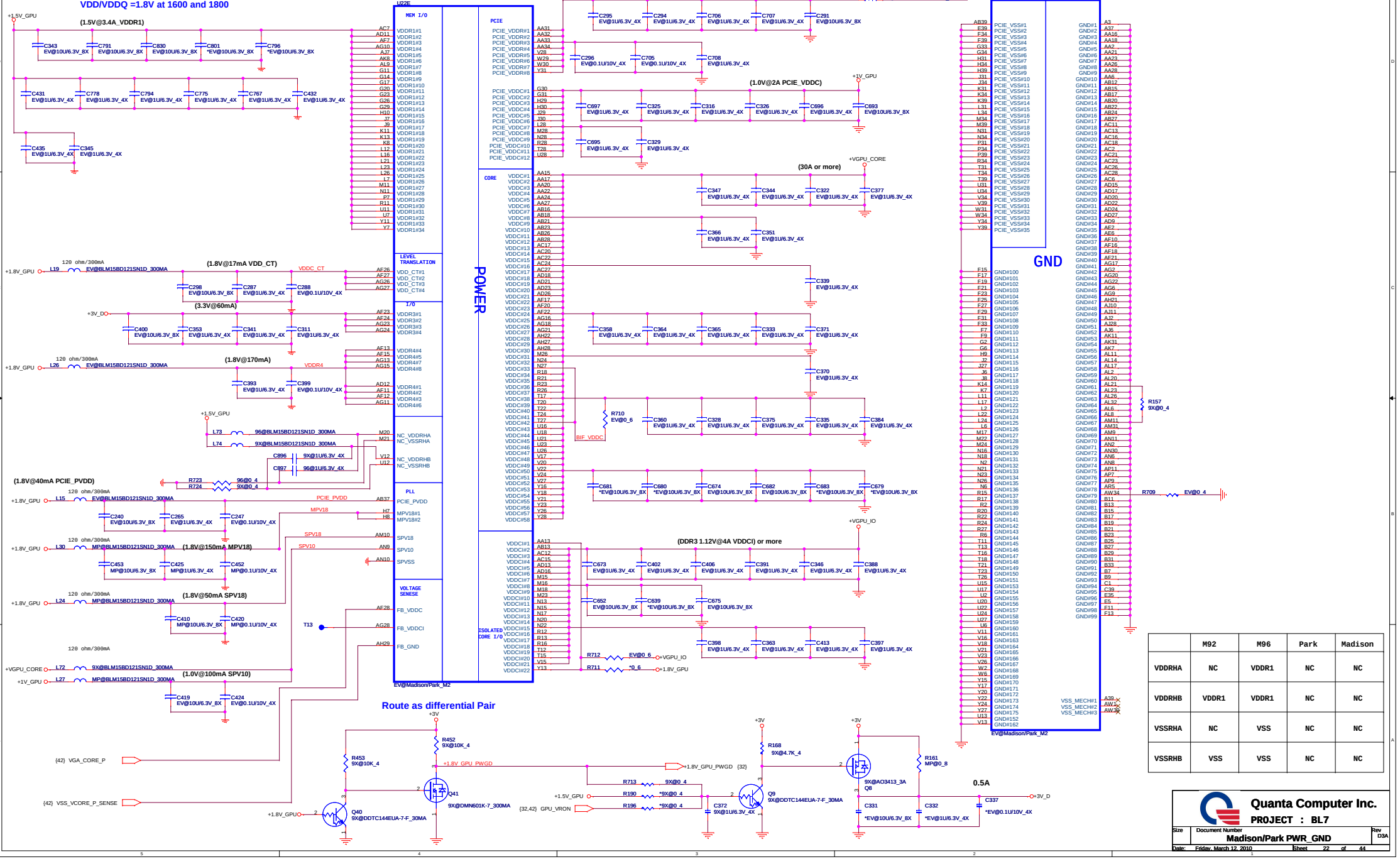


Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	D3A
Date: Friday, March 12, 2010	Sheet 21 of 44	

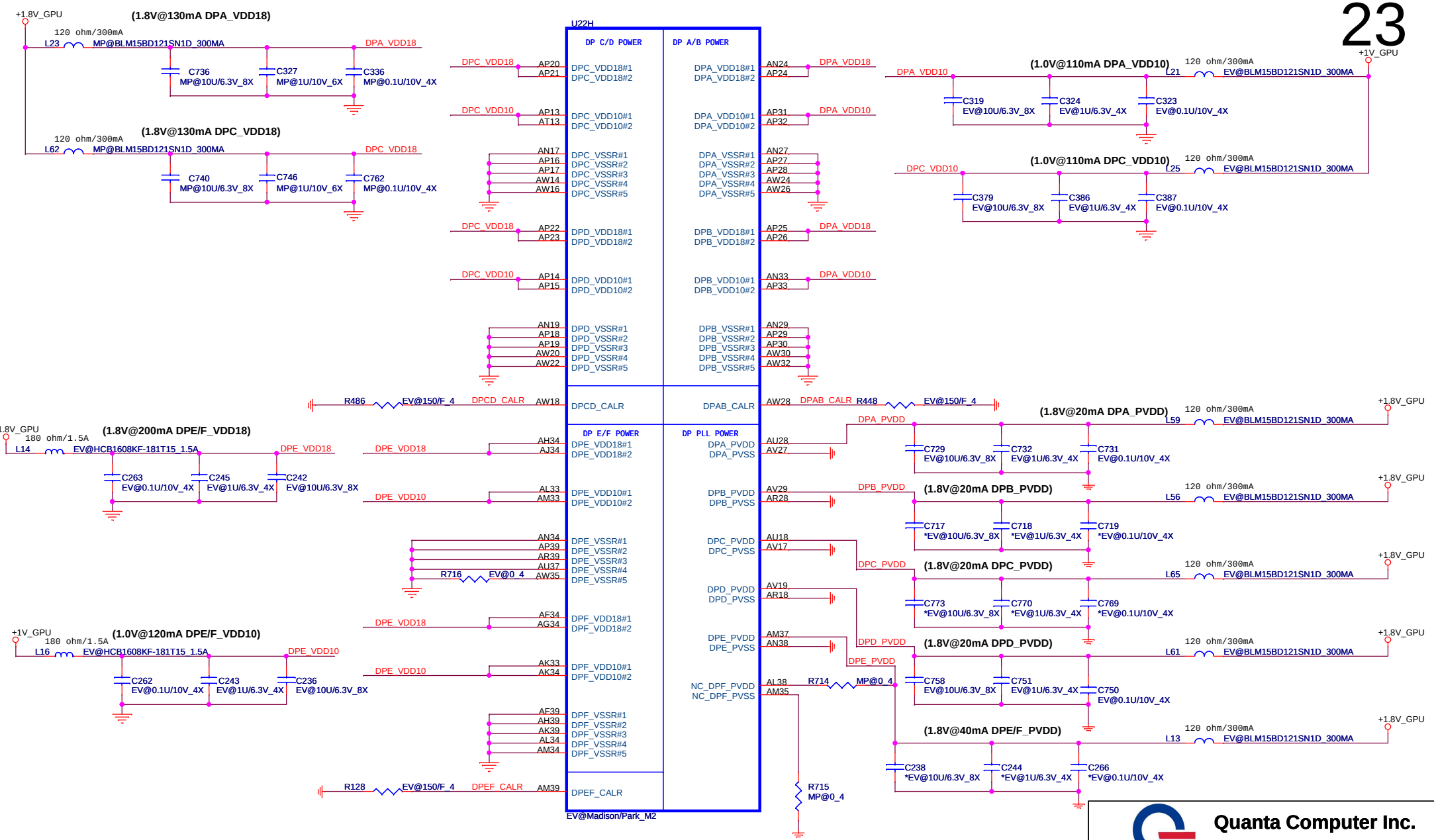
For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800



	M92	M96	Park	Madison
VDDRHA	NC	VDDR1	NC	NC
VDDRHB	VDDR1	VDDR1	NC	NC
VSSRHA	NC	VSS	NC	NC
VSSRHB	VSS	VSS	NC	NC

Quanta Computer Inc.
PROJECT : BL7
Size: Document Number: Madison/Park PWR_GND Rev: D3A
Date: Friday, March 12, 2010 Sheet 22 of 44

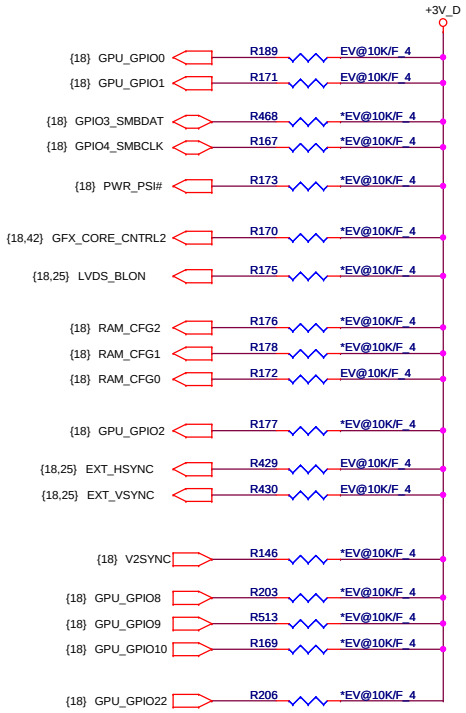


Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	Madison/Park DPPW_GND	D3A

Date: Friday, March 12, 2010 Sheet 23 of 44

PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

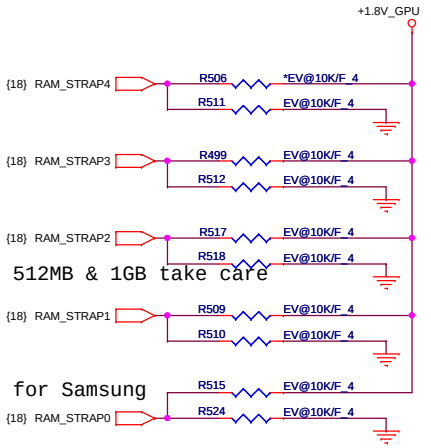
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

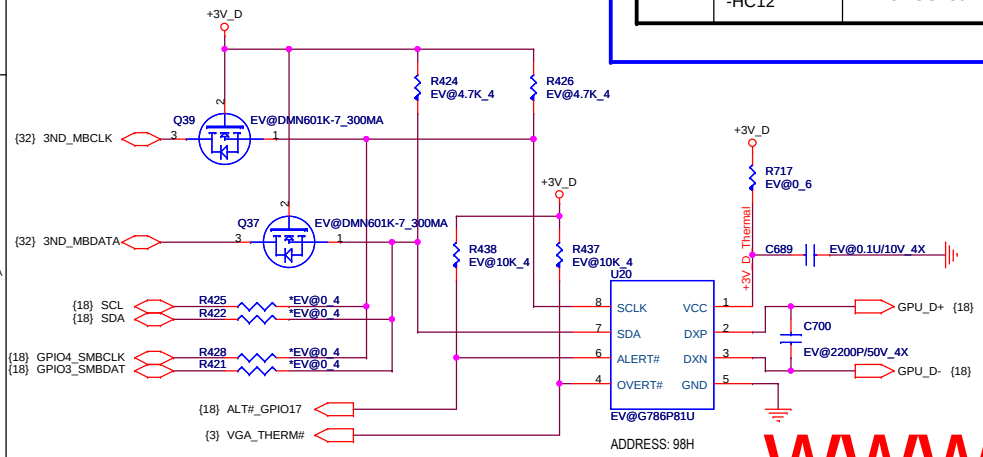
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

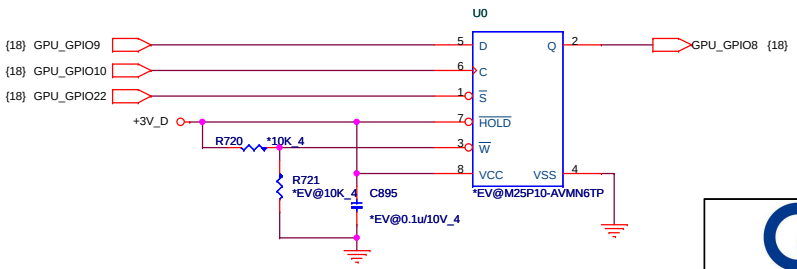
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



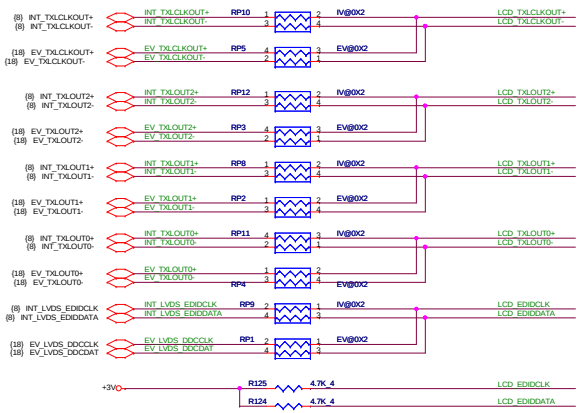
EEPROM



Quanta Computer Inc.
PROJECT : BL7

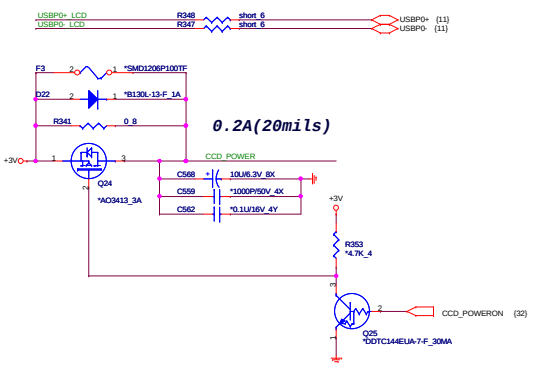
Size	Document Number	Rev
	Memory strip/Thermal/HDCP	D3A
Date: Friday, March 12, 2010	Sheet 24 of 44	

LVDS Signals

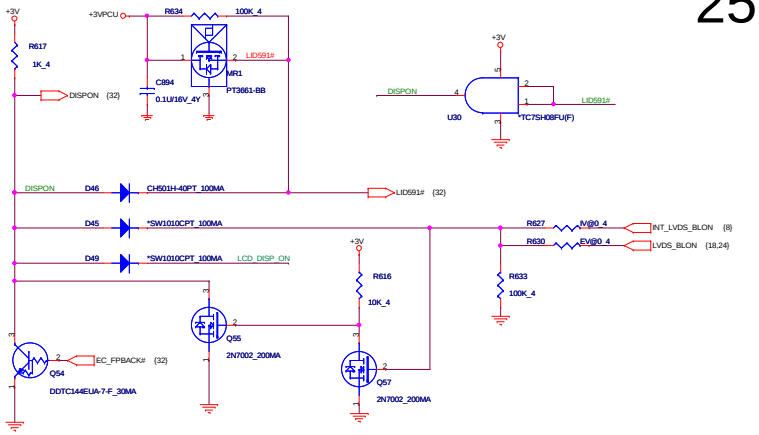


LVDS Enable

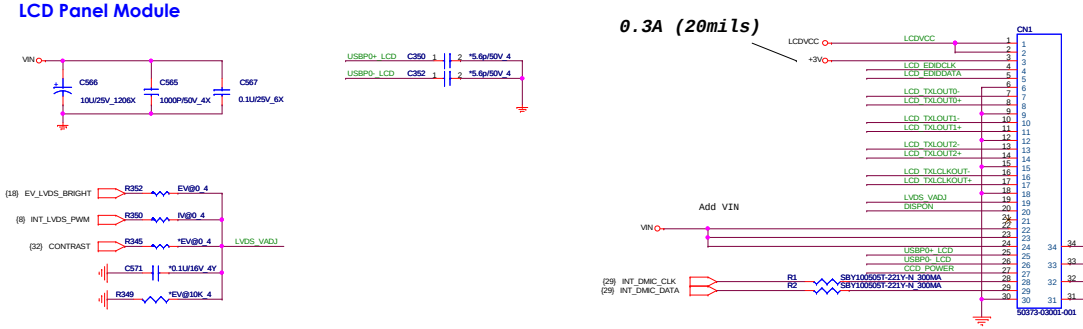
CCD



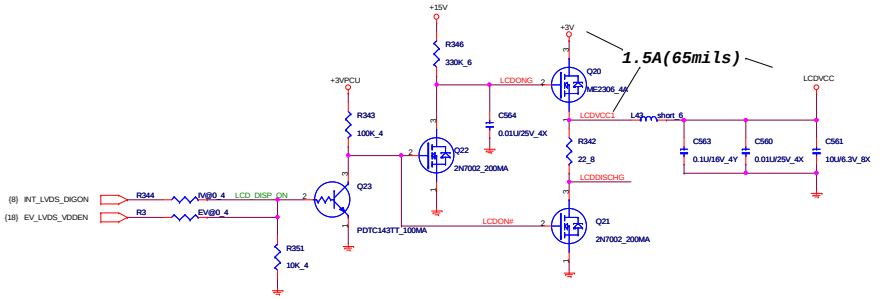
HALL SENSOR&BACK LIGHT SWITCH



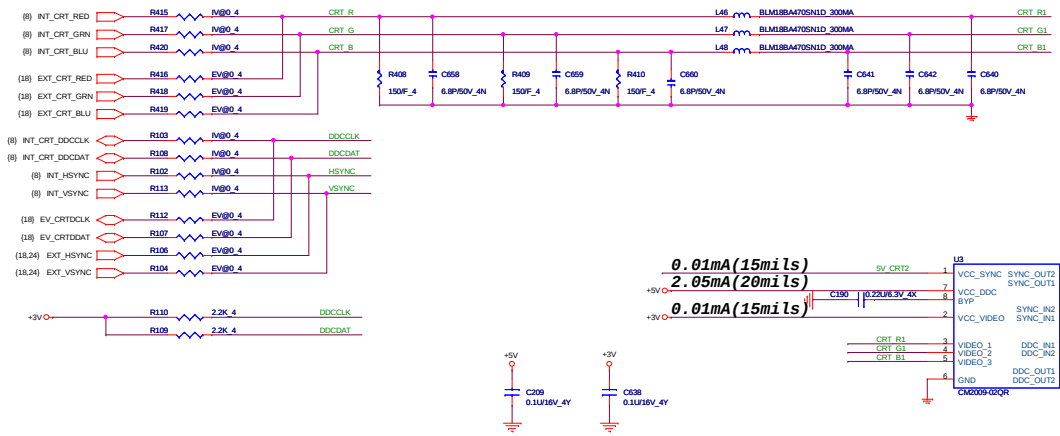
LCD Panel Module

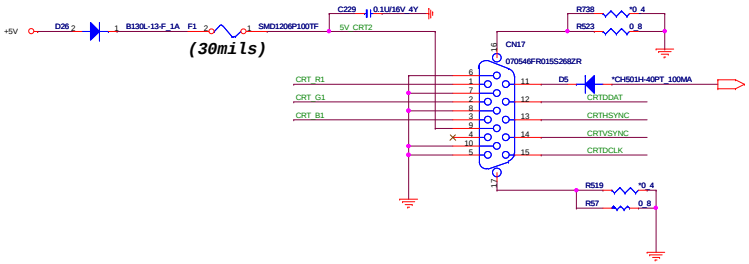


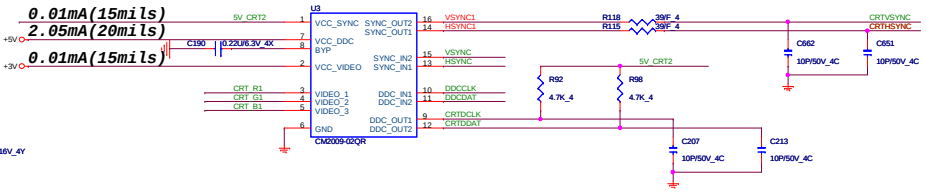
LCD POWER SWITCH



CRT

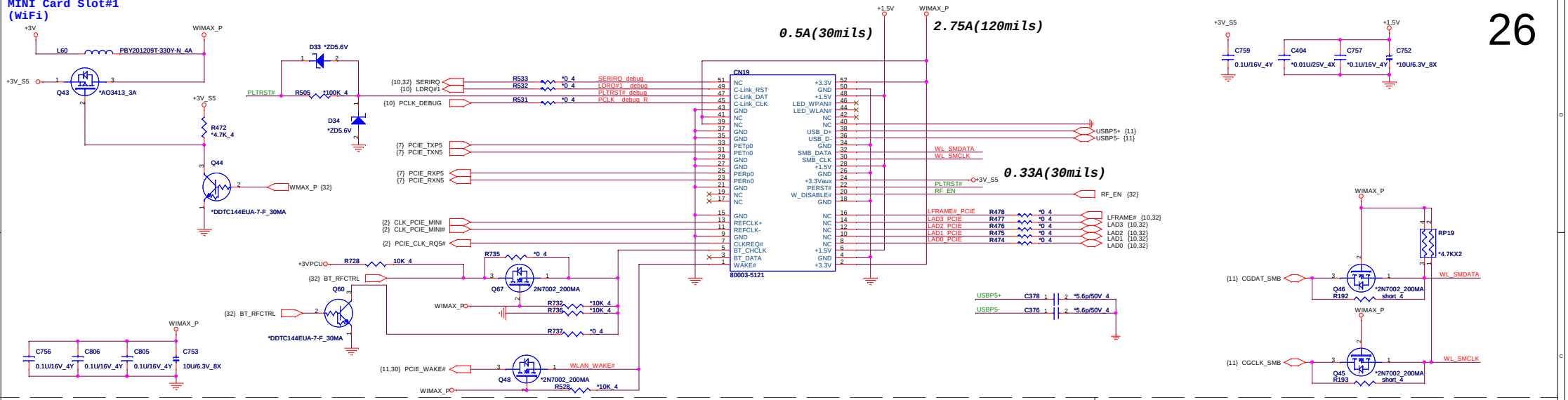




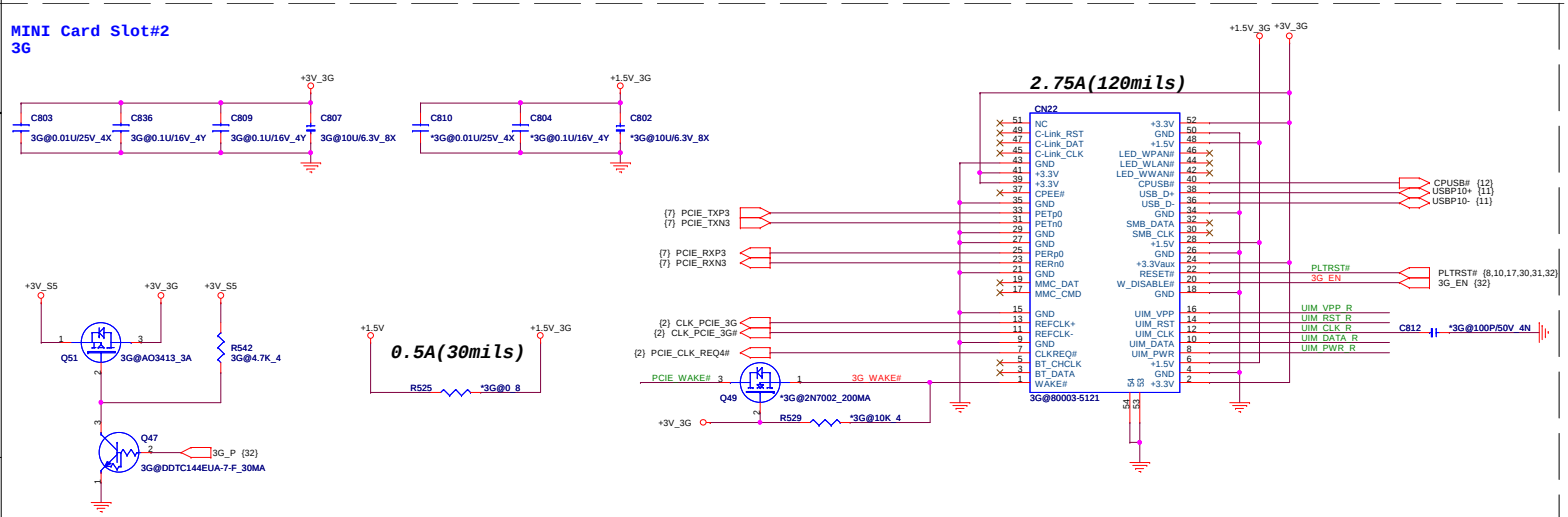


Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: LCD/LED Panel/CCD | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 25 of 44

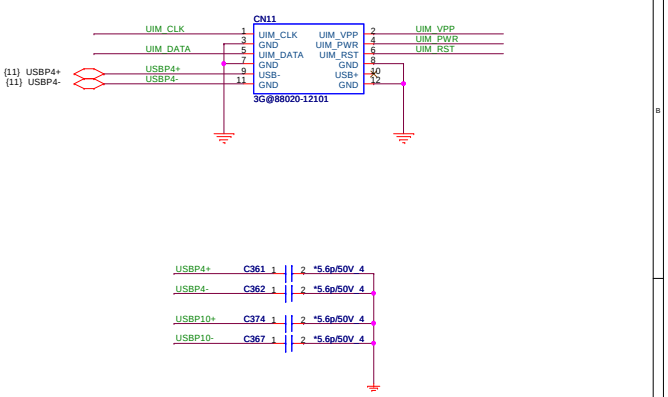
MINI Card Slot#1 (WiFi)



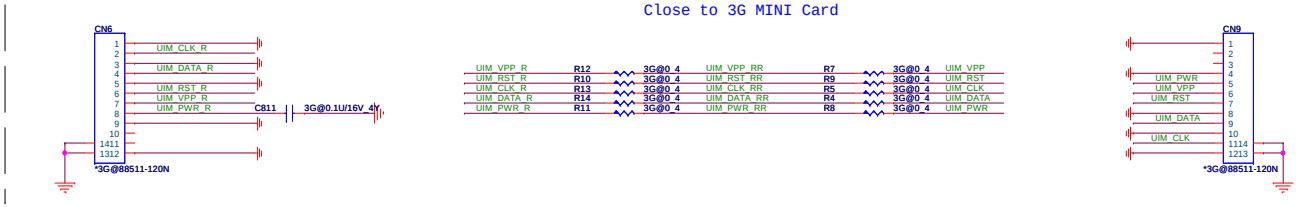
MINI Card Slot#2 3G



SIM CARD board to board

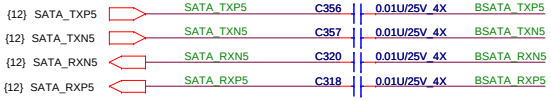


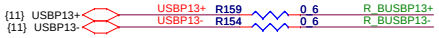
3G CONN

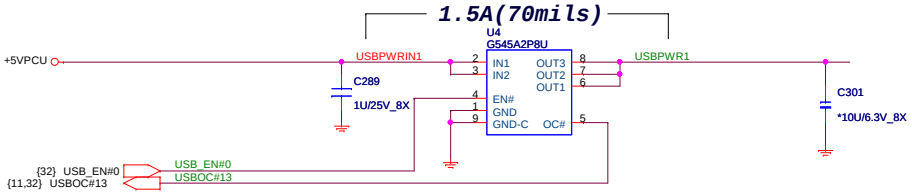


Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: MINI CARD(WLAN/3G/SIM Card) | Rev D3A
Date: Friday, March 12, 2010 | Sheet 26 of 44

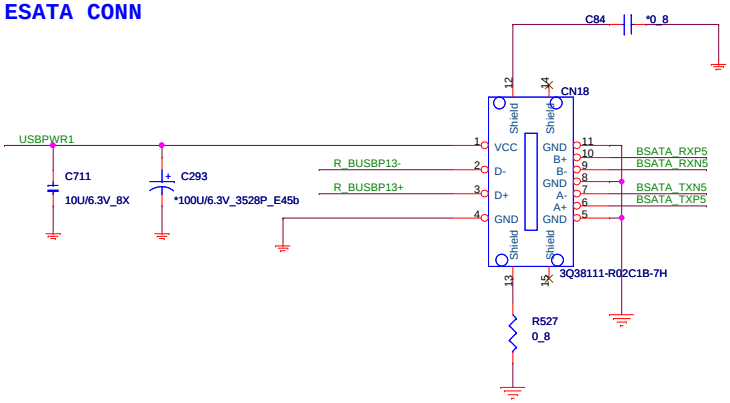
ESATA Re-driver IC

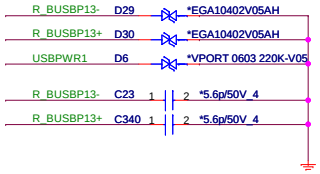


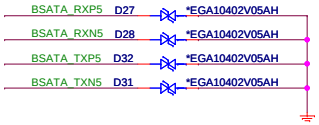




ESATA CONN





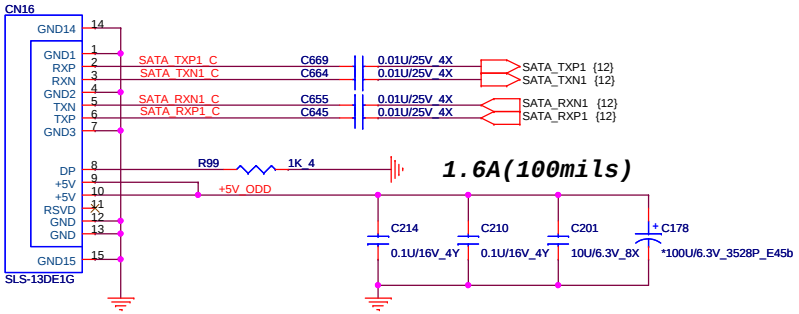


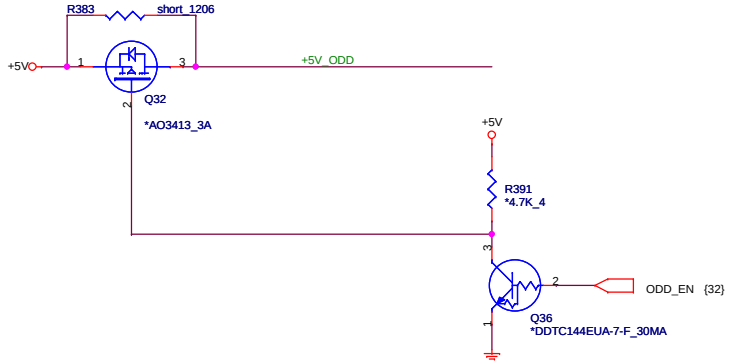
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	ESATA	D3A
Date:	Friday, March 12, 2010	Sheet 27 of 44

SATA ODD

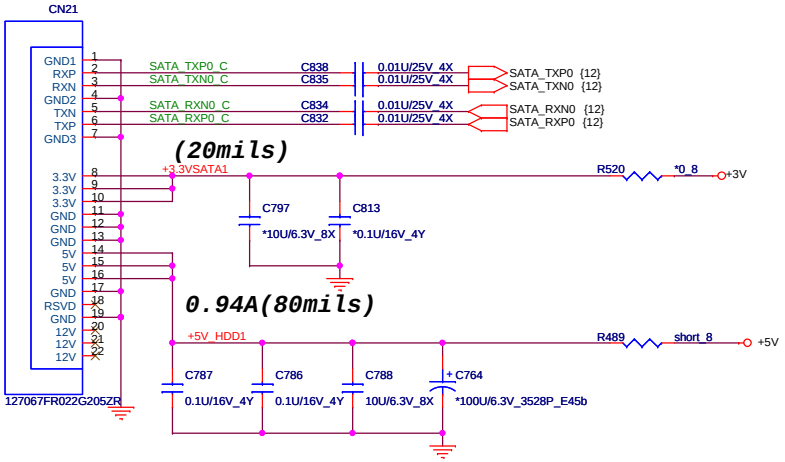
[ODD]





SATA HDD

[HDD]



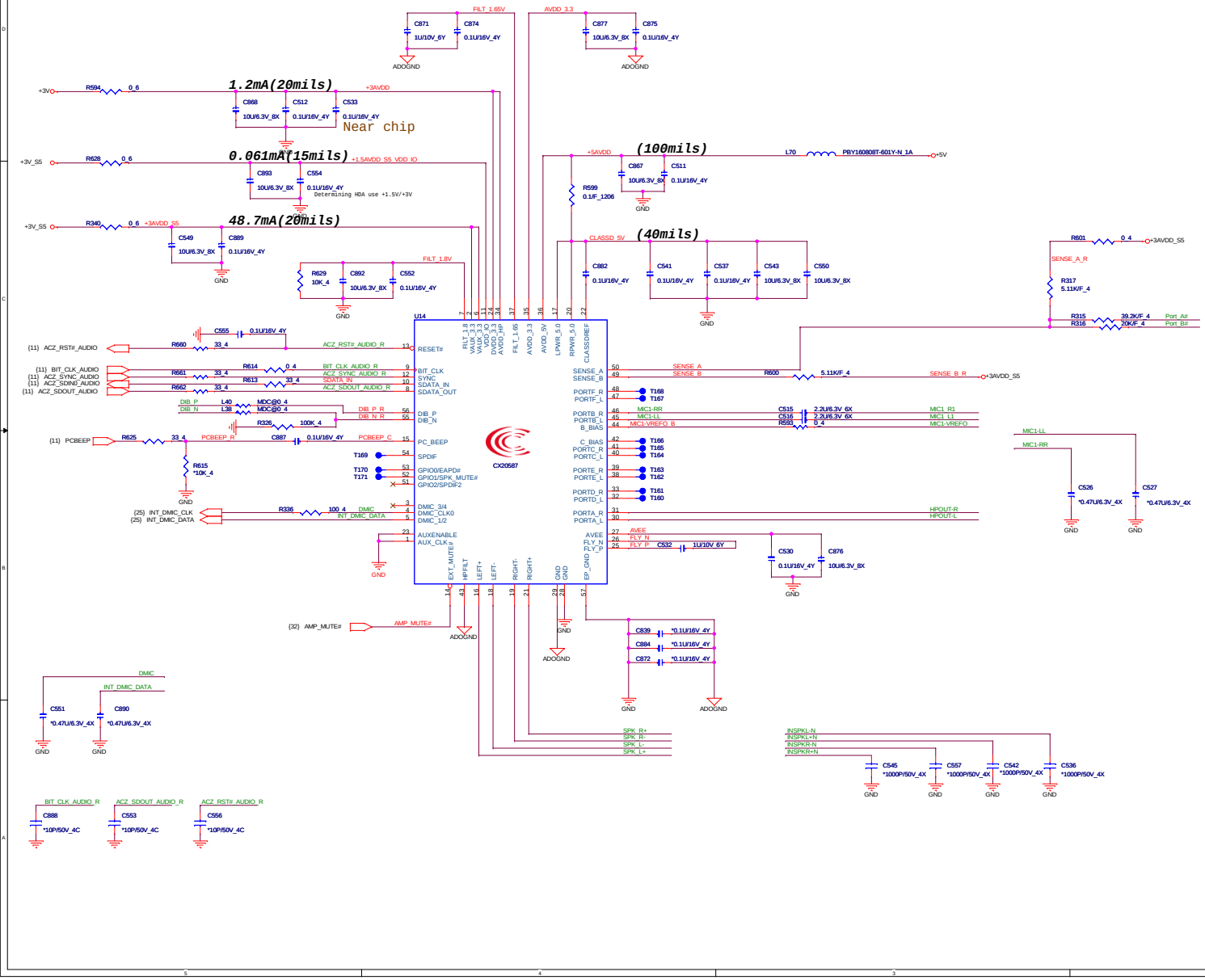
Quanta Computer Inc.

PROJECT : BL7

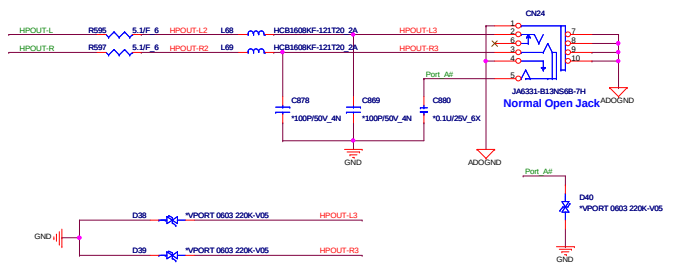
Size	Document Number	Rev
	HDD/ODD	D3A

Date: Friday, March 12, 2010 Sheet 28 of 44

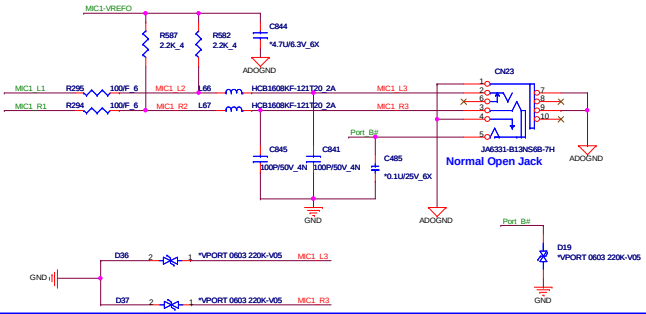
Codec (CX20587)



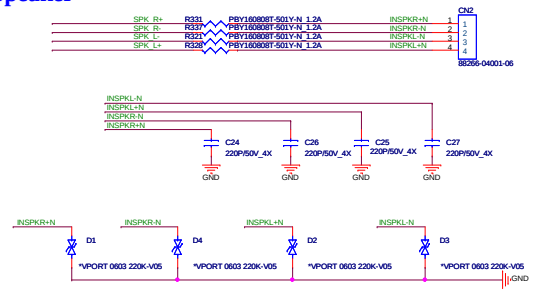
Earphone



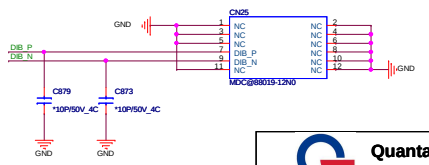
External MIC



Internal Speaker

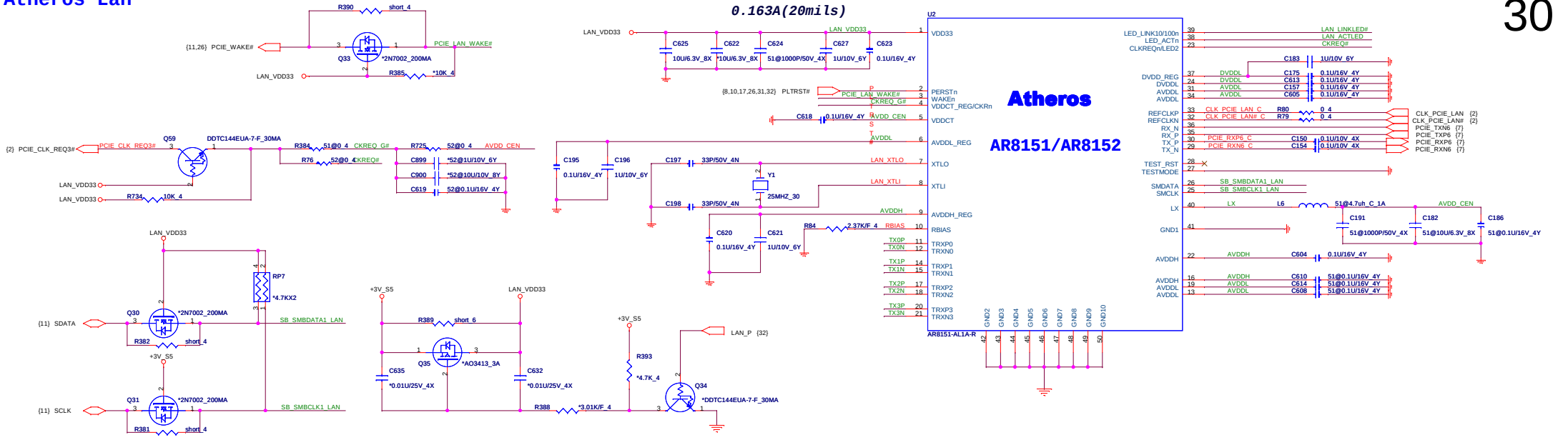


MDC

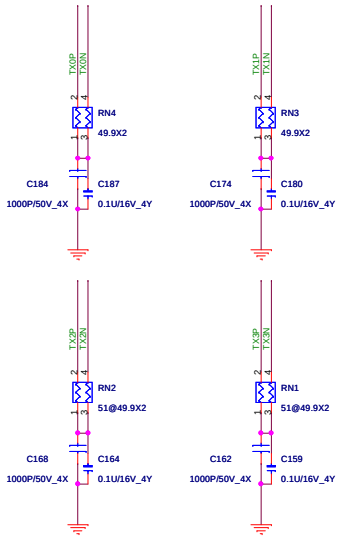


Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number	Rev
	Audio Codec (CX20583)	03A
Date: Friday, March 12, 2010	Sheet 29 of 44	

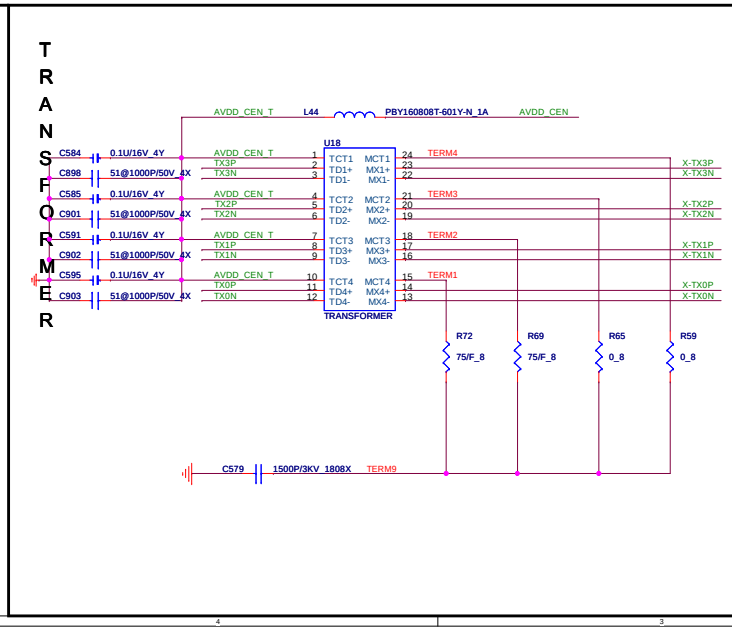
Atheros Lan



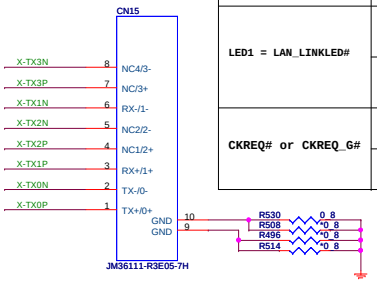
PLACE NEAR LAN IC SIDE



TRANSFORMER



RJ45



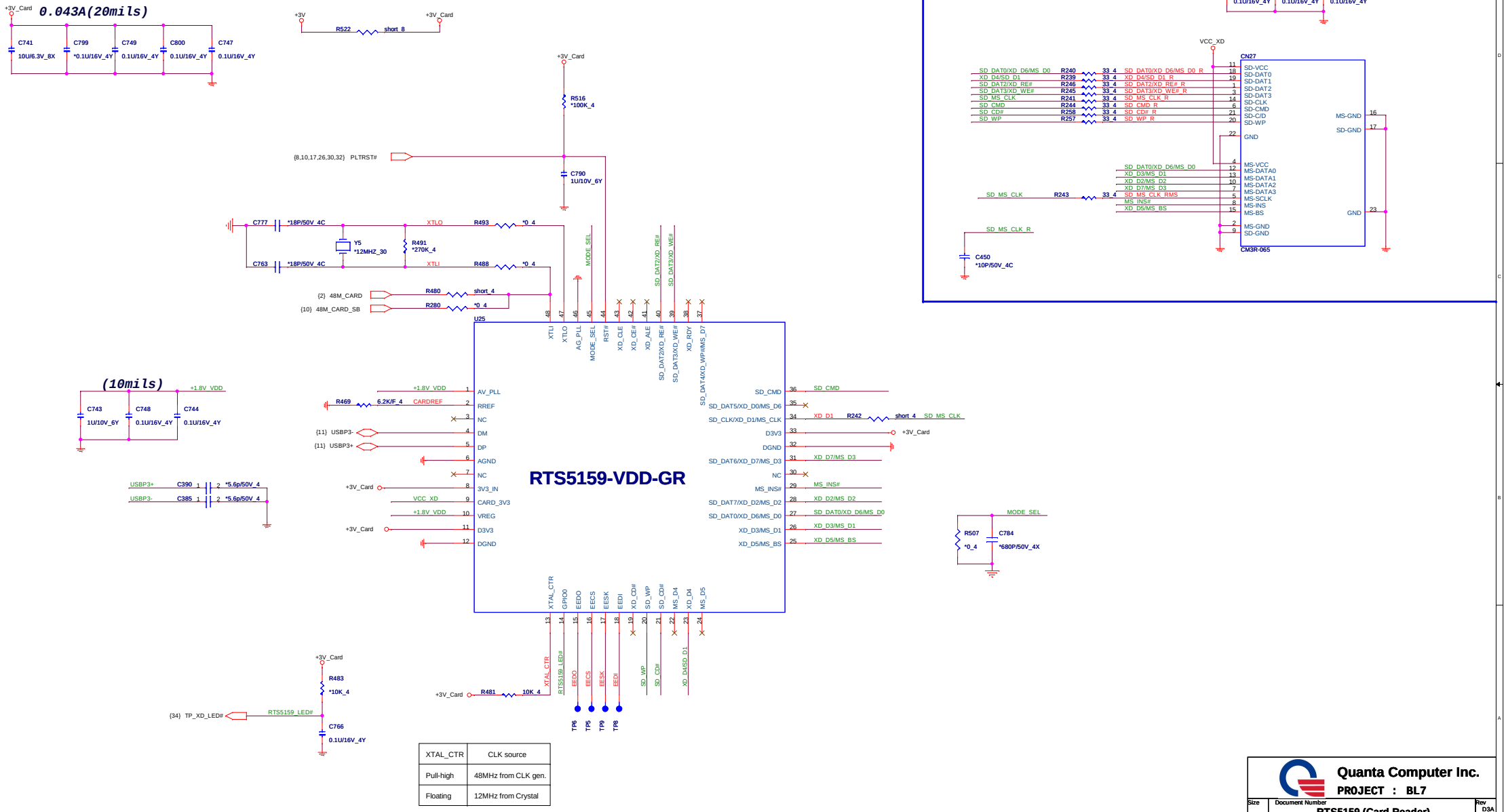
LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	Atheros Lan	D3A

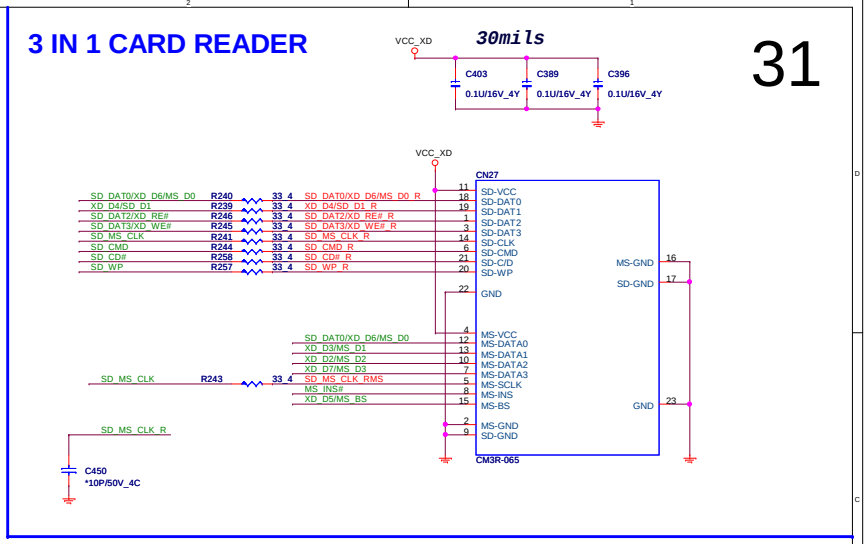
Date: Friday, March 12, 2010 Sheet 30 of 44

5 IN 1 CARD READER



XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER

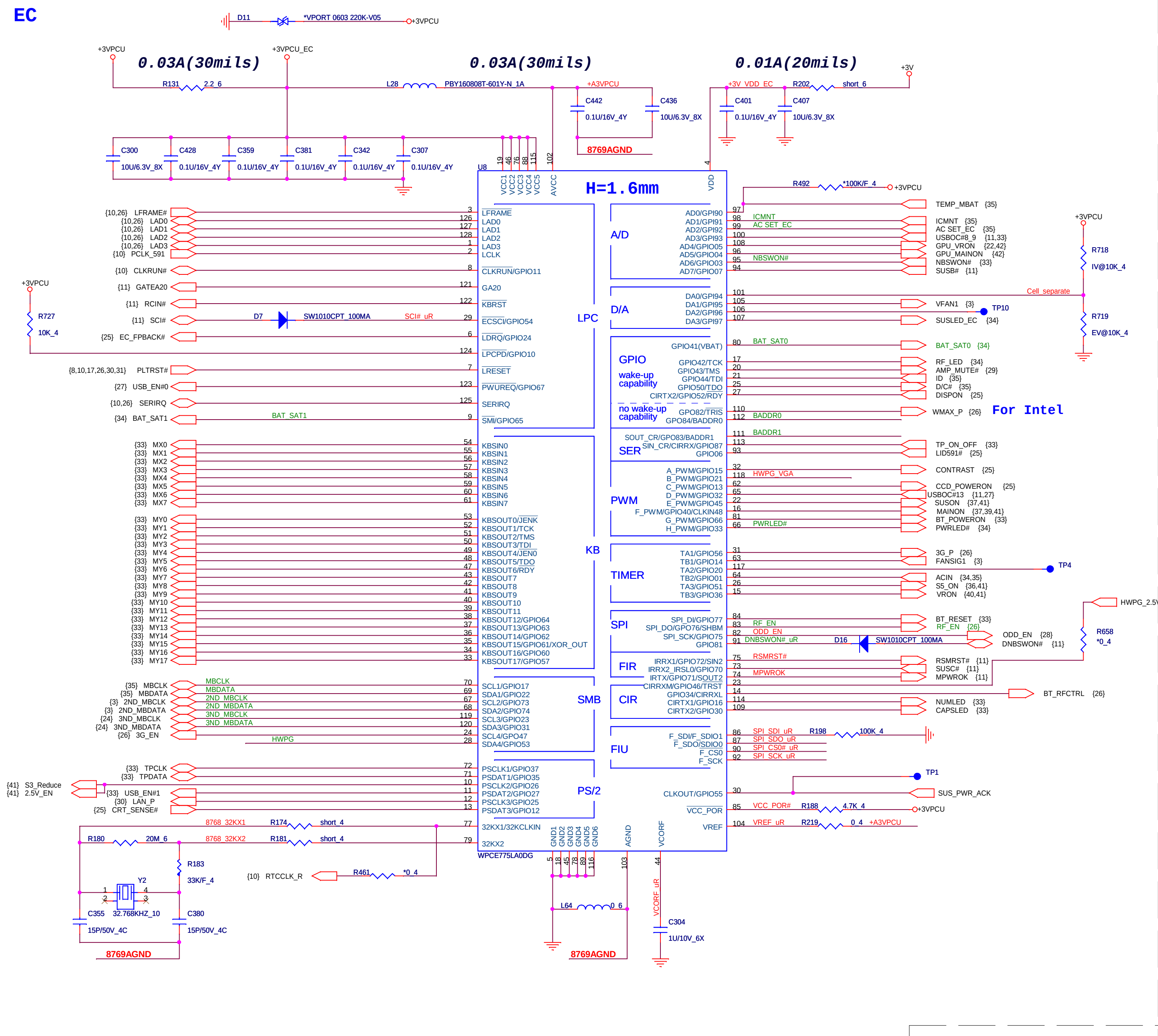


Quanta Computer Inc.
PROJECT : BL7

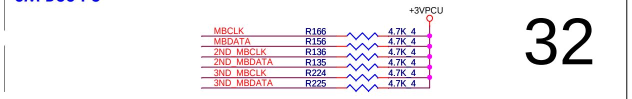
Size	Document Number	Rev
	RTS5159 (Card Reader)	D3A

Date: Friday, March 12, 2010 Sheet 31 of 44

EC



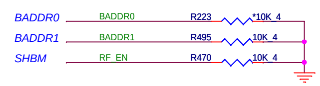
SM BUS PU



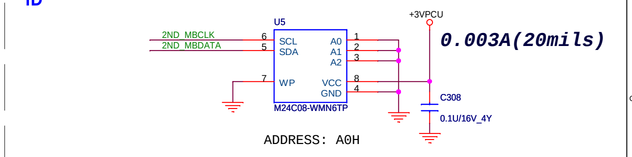
I/O Base Address

I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

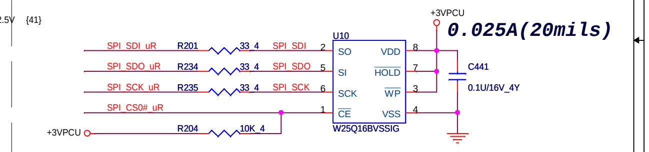
SHBM=0: Enable shared memory with host BIOS



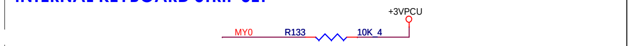
ID



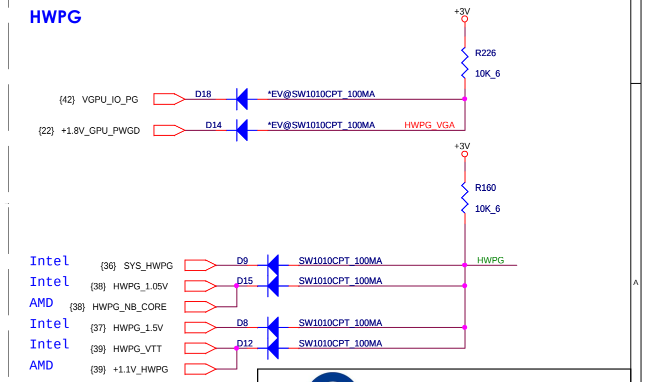
SPI FLASH



INTERNAL KEYBOARD STRIP SET

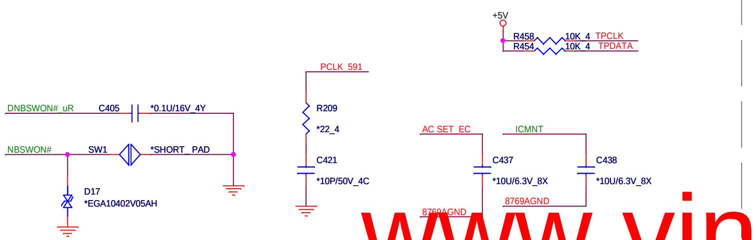


HWPG

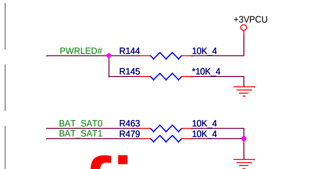


SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H



LED PU/PD



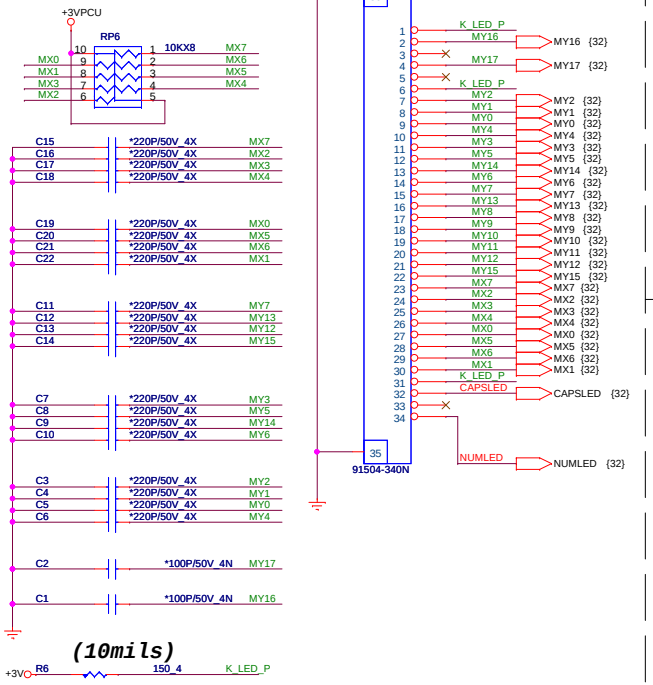
Quanta Computer Inc.

PROJECT : BL7

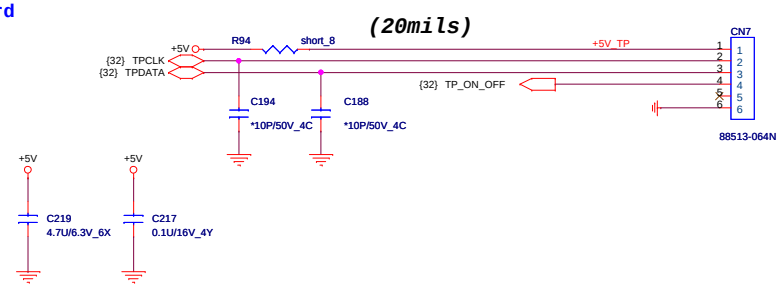
Size | Document Number: EC-WPC8763LDG/WPC8769L(O) | Rev D3A

Date: Friday, March 12, 2010 | Sheet 32 of 44

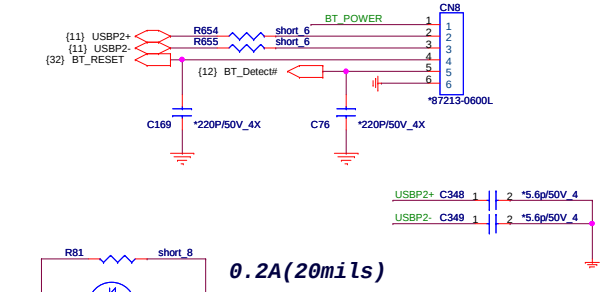
INT KeyBoard



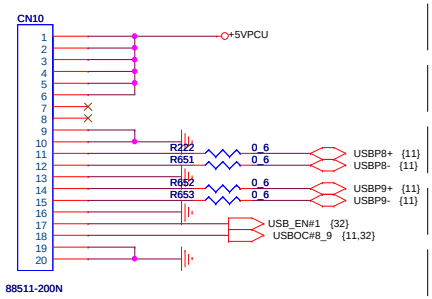
TP board



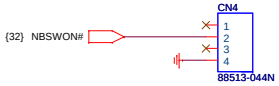
Bluetooth

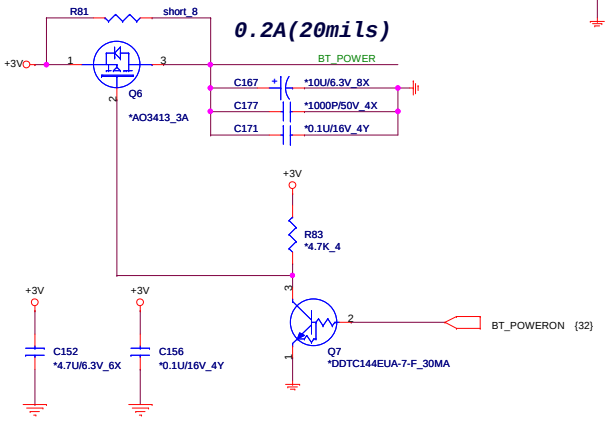


USB board

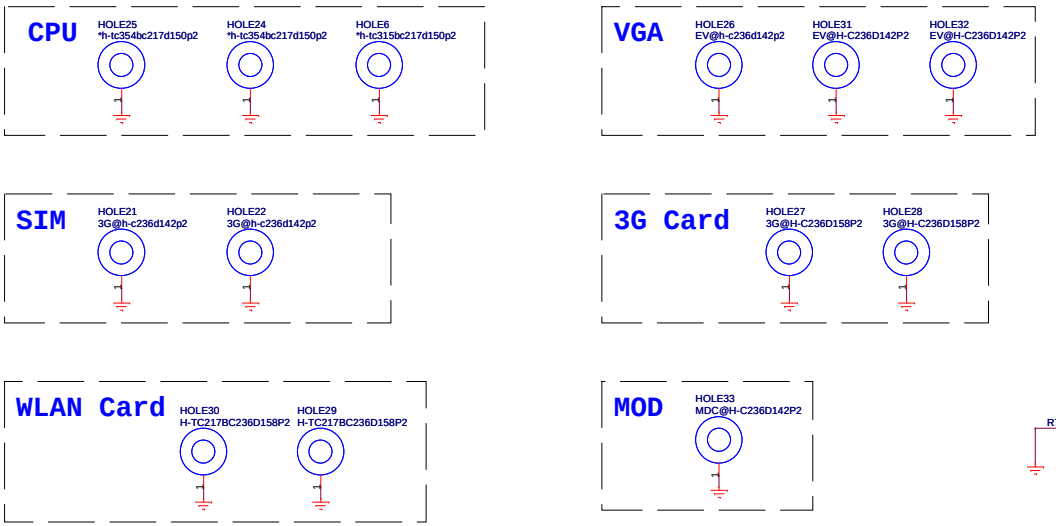


Power board

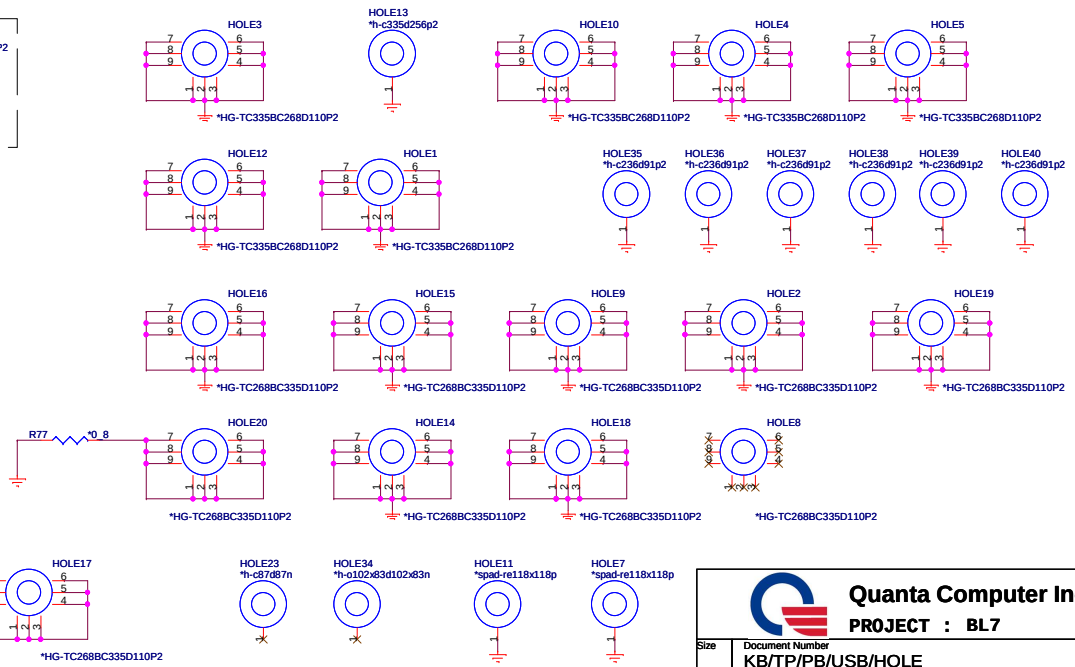




NUT



HOLE

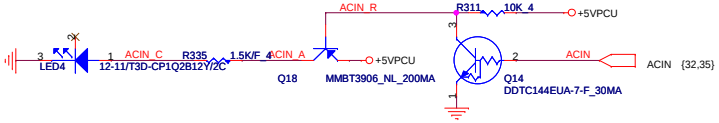


Quanta Computer Inc.
PROJECT : BL7

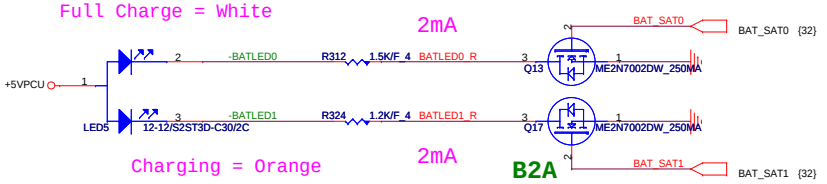
Size	Document Number	Rev
	KB/TP/PB/USB/HOLE	D3A
Date: Friday, March 12, 2010	Sheet 33 of 44	

LED

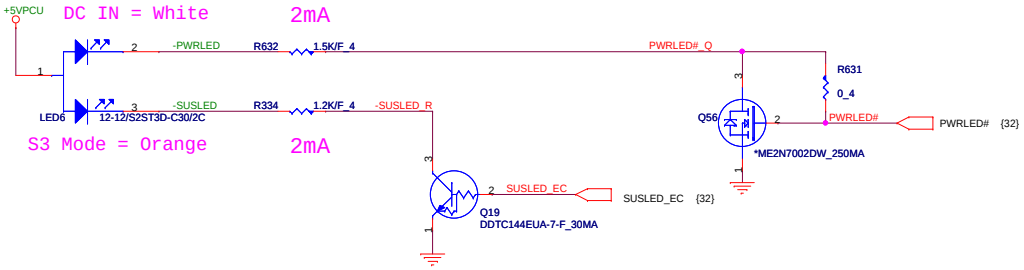
AC-IN



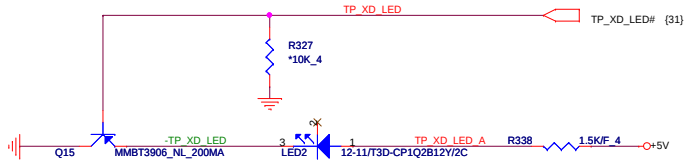
BATERRY



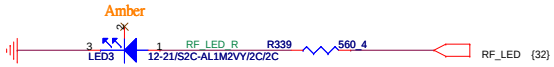
POWER



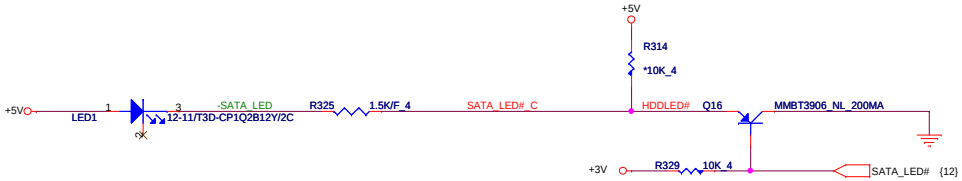
CARDREADER



RF LED



HDD/ODD

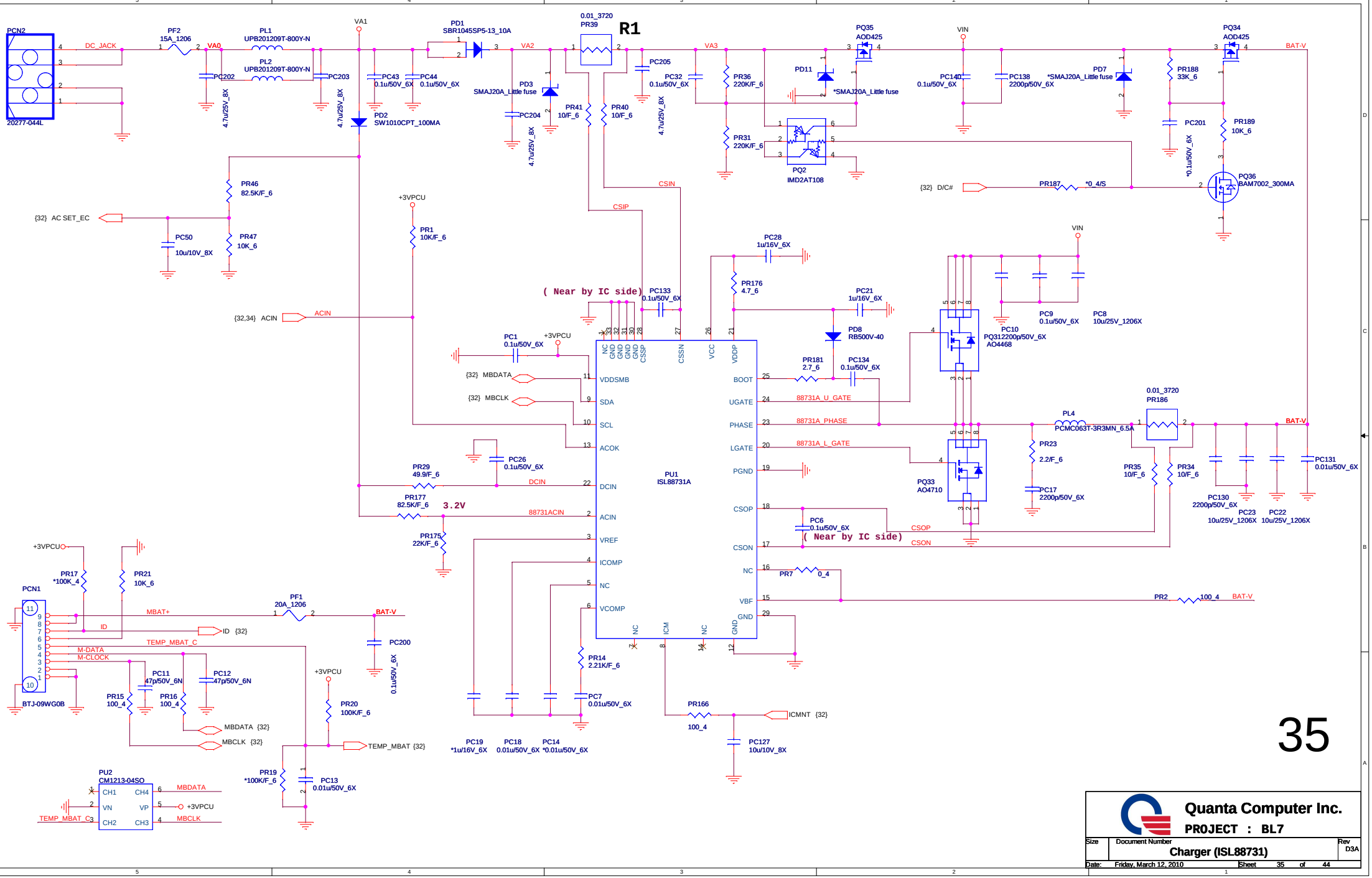


ESD Protect

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	LED	D3A

Date: Friday, March 12, 2010 Sheet 34 of 44

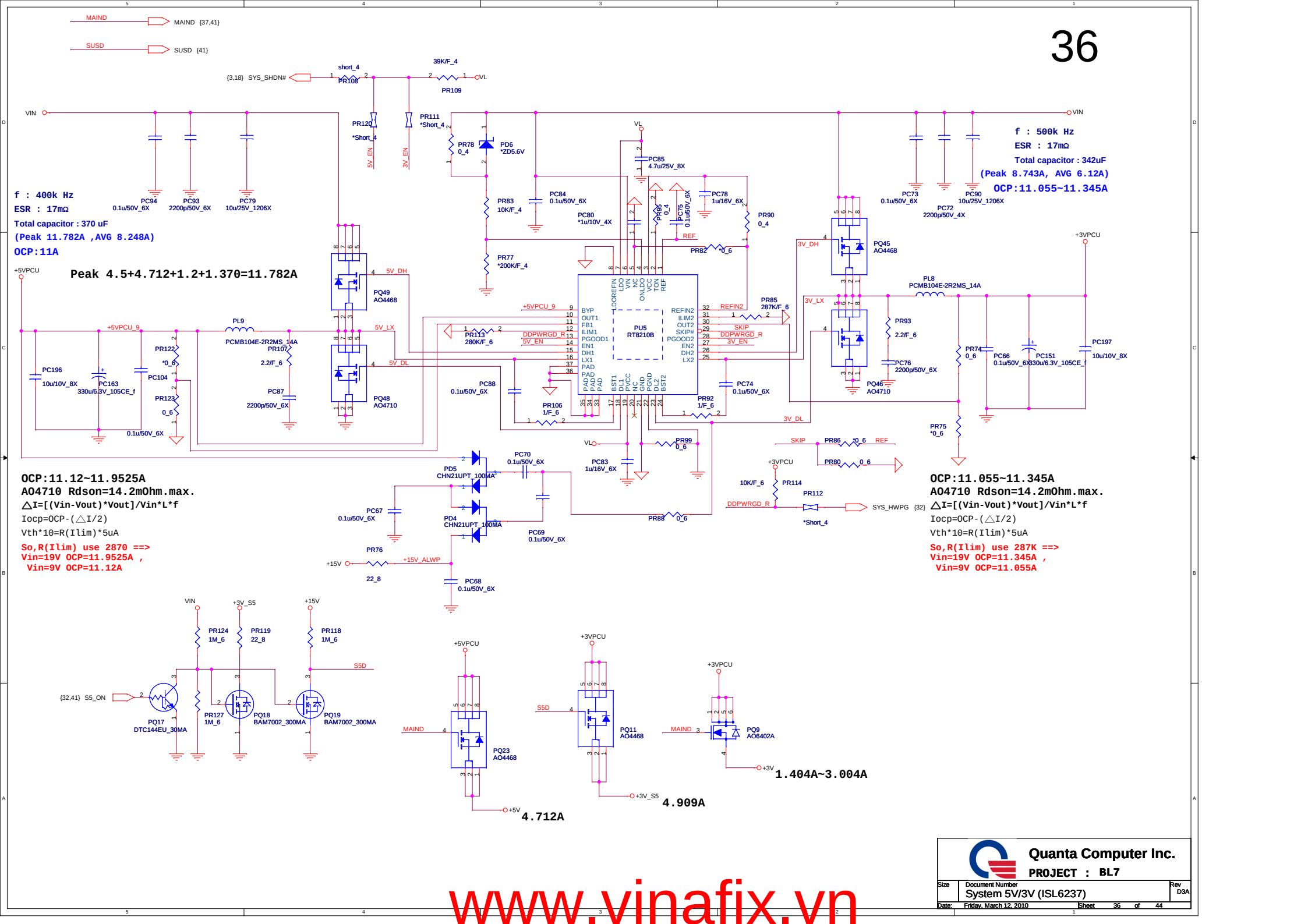


35

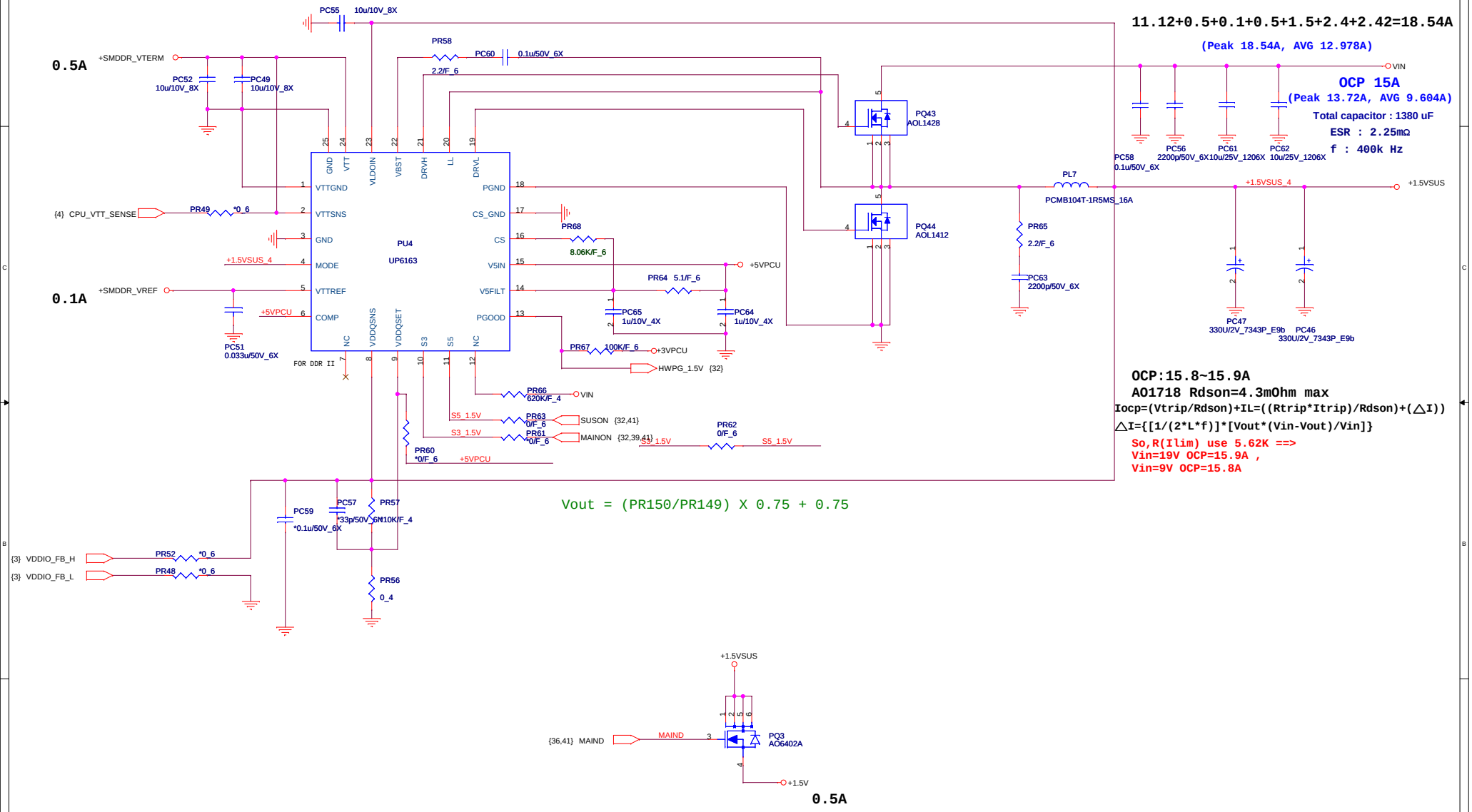
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	Charger (ISL88731)	D3A

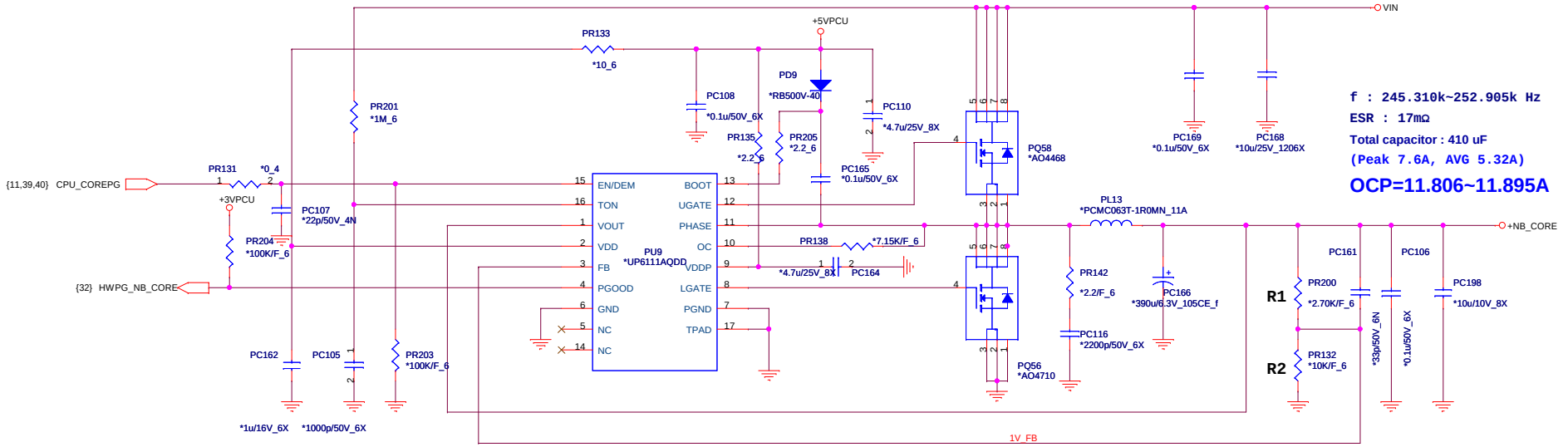
Date: Friday, March 12, 2010 Sheet 35 of 44



Quanta Computer Inc.	PROJECT : BL7	
Size	Document Number: System 5V/3V (ISL6237)	Rev: D3A
Date: Friday, March 12, 2010	Sheet 36 of 44	



Quanta Computer Inc.			
PROJECT : BL7			
Size	Document Number: DDR 1.5V (UP6163)		Rev: D3A
Date: Friday, March 12, 2010		Sheet 37 of 44	



Vout=0.75*[1+(R1+R2)]

Ton=3.85p*Rton*Vout/(Vin-0.5) F=Vout/(Vin*Ton)

AO4710 Rdson=14.2mOhm.max.

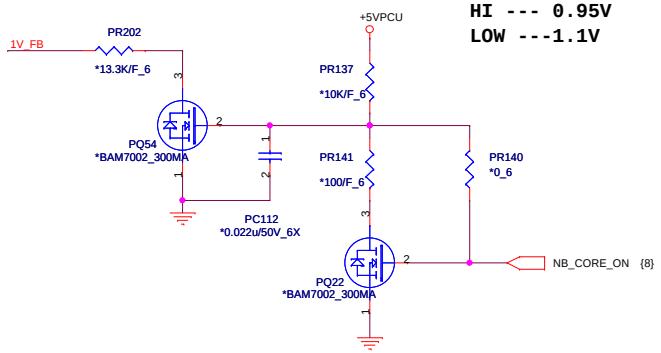
Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)

OCP =(Rimax*20uA/LRdson)+(Ripple/2)

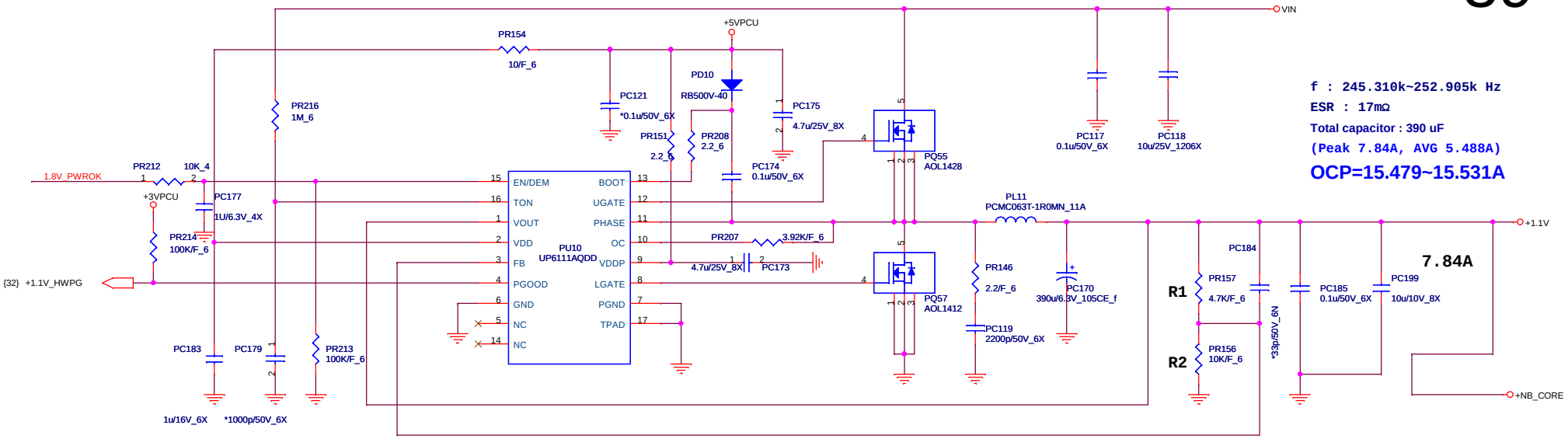
Vout=0.75*[1+(R1+R2)]

R2=10KΩ,R1=2.7KΩ

So,Vin=19V==>
OCP=11.895A;
Vin=9V==>
OCP=11.806A



Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: NB_CORE (UPI6111)	Rev: D3A
Date: Friday, March 12, 2010	Sheet 38 of 44	



Vout=0.75*[1+(R1+R2)]

Ton=3.85p*Rton*Vout/(Vin-0.5) F=Vout/(Vin*Ton)

AO4710 Rdson=14.2mOhm.max.

Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)

OCP =(Rimax*20uA/LRdson)+(Ripple/2)

Vout=0.75*[1+(R1+R2)]

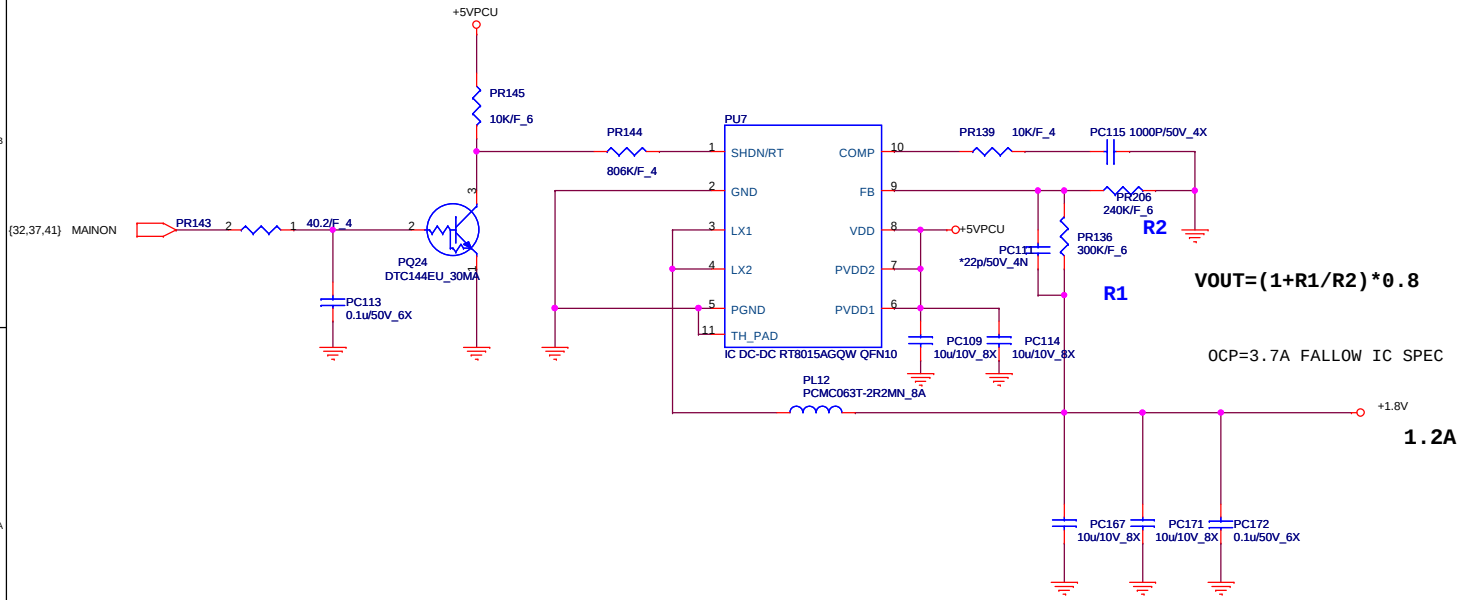
R2=10KΩ,R1=4.7KΩ

So,Vin=19V==>

OCP=15.531A;

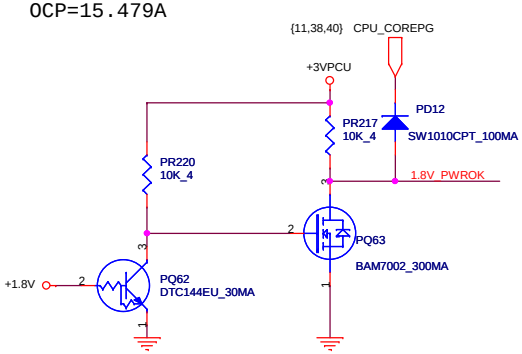
Vin=9V==>

OCP=15.479A



VOUT=(1+R1/R2)*0.8

OCP=3.7A FALLOW IC SPEC



Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: +1.1V/+1.8V (UP6111)	Rev: D3A
Date: Friday, March 12, 2010	Sheet 39 of 44	

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

VDDNB Core(Peak 4A,AVG 2.8A) OCP 4.5A

OCP_NB=ROCSET*10uA/Rdson

ROCSET=PR34

OCP_NB=11.3k*10uA/23m=4.91A

Total capacitor : 370 uF

ESR : 9mΩ

f : 300k Hz

4A

+VDDNB_CORE

PL3 PCMC063T-1R0MN_11A

{3} CPU_VDDNB_FB_H

{3} CPU_VDDNB_FB_L

PR26 10/F_6

PR27 10/F_6

PC29 10u/25V_1206X

PC135 330U/2V_7343P_E9b

LGATE_NB

UGATE_NB

PQ1 AO4932

PC142 0.1u/50V_6X

PR28 2.2/F_4

PC24 2200p/50V_4X

PC141 PC36 PC139 PC34 4.7u/25V_8X

PC206 100u/25V_105CE_f

VIN

PR24 10/F_6

+5VPCU

PC15 1u/25V_8X

PR163 0_8

PR25 22.1K/F_4

PC20 1000p/50V_4X

PC129 33p/50V_4N

PC128 1200p/50V_4X

PR171 44.2K/F_4

PR9 10/F_6

PC5 0.1u/50V_6X

PR30 11.3K/F_4

PHASE_NB

UGATE_NB

PC31 0.1u/50V_6X

PR33 1/F_6

PC37 0.1u/50V_6X

PQ41 AOL1428

PC40 PC143 PC144 PC45 4.7u/25V_8X

PC148 *100u/25V_105CE_f

Total capacitor : 1404.4 uF

ESR : 2.25mΩ

f : 300k Hz

Core (Peak 20A,AVG 16A)

OCP 28A

PL5 PCMB104T-R36MT_30A

+VCC_CORE

PR37 2.2/F_4

PC38 2200p/50V_4X

PR42 0_6

PR44 0_6

PC53 330U/2V_7343P_E9b

PC149 330U/2V_7343P_E9b

PQ39 AOL1412

PQ40 AOL1412

ISP_0

ISN_0

+3VPCU

PR12 0_4

PR165 *0_4

PR168 *10K/F_4

PR3 10K/F_6

PR6

{11,38,39} CPU_COREPG

+1.8V

+3V

*Short_4

PQ32 *DTC144EU_SOT

PR161 *10K/F_6

PR160 0_4

{3} CPU_PWRGD_SVID_REG

{3} CPU_SVD

{3} CPU_SVC

{32,41} VRON

PR11 0_4

PR4 10K/F_4

PR8 107K/F_4

PR13 10K/F_4

Pin 49 is GND Pin

PU3 ISL6265A

GND VIN VCC FB_NB COMP_NB FSET_NB VSEN_NB RTN_NB OCSET_NB PGND_NB LGATE_NB PHASE_NB UGATE_NB

1 OFS/VFIXEN

2 PGOOD

3 PWROK

4 SVD

5 SVC

6 ENABLE

7 RBIAS

8 OCSET

9 VDIFF_0

10 FB_0

11 COMP_0

12 VW_0

36 BOOT_NB

35 BOOT_0

34 UGATE_0

33 PHASE_0

32 PGND_0

31 LGATE_0

30 PVCC

29 LGATE_1

28 PGND_1

27 PHASE_1

26 UGATE_1

25 BOOT_1

PR185 1/F_6

PC35 0.1u/50V_6X

PC137 2.2u/10V_8X

PR184 1/F_6

PC33 0.1u/50V_6X

PR162 255/F_4

PC126 4700p/25V_4X

PR164 1K/F_4

PR5 54.9K/F_4

PC3 1200p/50V_4X

PC4 180p/50V_4X

PR10 6.81K/F_4

PC2 1000p/50V_4X

PR18 18.2K/F_4

PR22 3.92K/F_4

PC16 0.1u/50V_6X

ISP_0 ISN_0 VSEN_0 RTN_0 RTN_1 VSEN_1 VDIFF_1 FB_1 COMP_1 VW_1 ISP_1 ISN_1

13 14 15 16 17 18 19 20 21 22 23 24

VIN 46A

B TEST DEL JP 13

PC146 PC145 PC41 PC42 4.7u/25V_8X

PC207 *100u/25V_105CE_f

PC147 0.1u/50V_6X

PQ42 AOL1428

Total capacitor : 1404.4 uF

ESR : 2.25mΩ

f : 300k Hz

Core (Peak 20A,AVG 16A)

OCP 28A

PL6 PCMB104T-R36MT_30A

+VCC_CORE

PR38 2.2/F_4

PC39 2200p/50V_4X

PR43 0_6

PR45 0_6

PC150 330U/2V_7343P_E9b

PC48 330U/2V_7343P_E9b

PQ37 AOL1412

PQ38 AOL1412

PC136 0.1u/50V_6X

PR182 3.92K/F_4

PR183 18.2K/F_4

PR32 *6.81K/F_4

PC30 *1000p/50V_4X

ISP_1

ISN_1

+VCC_CORE

PR169 10/F_6

{3} CPU_VDD0_FB_H

{3} CPU_VDD0_FB_L

PR170 10/F_6

R2

PR172 1K/F_4

+1.8V

R1

PR167 *10K/F_6

R3

PR173 *0_4

{3} CPU_VDD1_FB_L

{3} CPU_VDD1_FB_H

+VCC_CORE

PR174 10/F_6

PC132 *4700p/25V_4X

PR178 *1K/F_4

PC27 *1200p/50V_4X

PC25 *180p/50V_4X

PR179 *255/F_4

PR180 *54.9K/F_4

OCP 28A

VOSET=1.17V*Rocset/(Rbias+Rocset)

Ioc=VOCSET/30/(K*DCR*1.4)

K=PR33/(PR33+PR32)

VOSET=1.17V*107/(107+10)=1.07V, K=18.2/(18.2+3.92)=0.822

Ioc=1.07V/30/(0.822*1.1m*1.4)=28.175A.

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PROJECT : BL7

Size | Document Number: AMD CPU Core (ISL6265A) | Rev: D3A

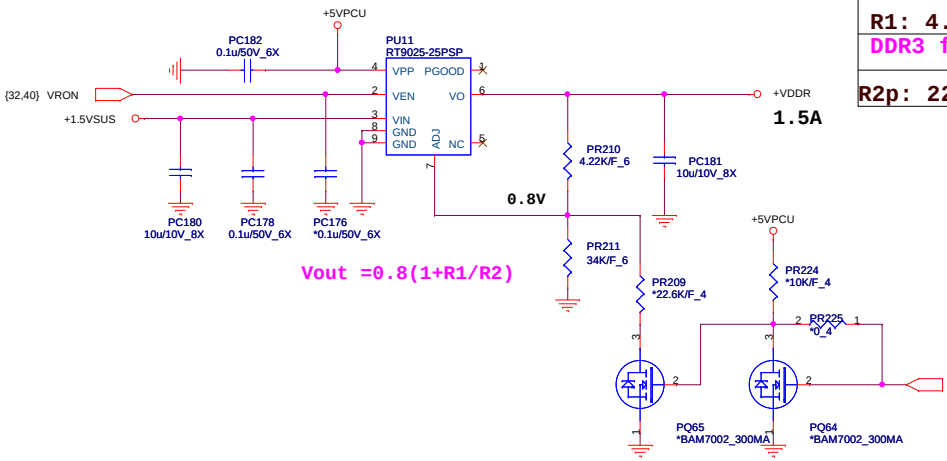
Date: Friday, March 12, 2010 | Sheet 40 of 44

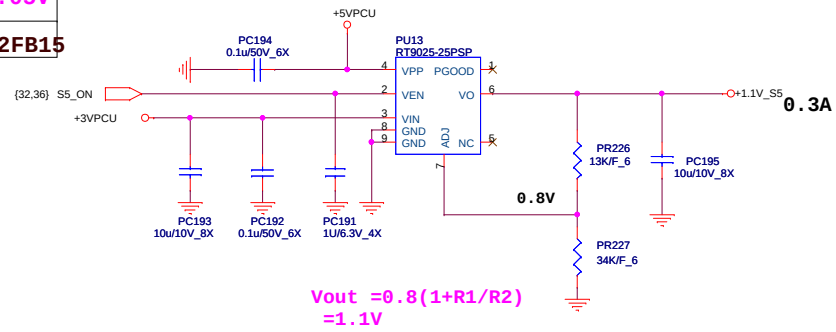
DDR3 for 1066MHZ----0.9V

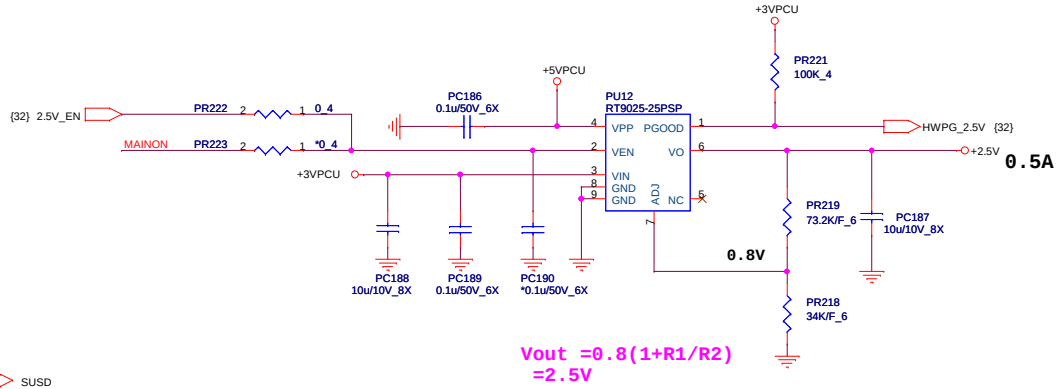
R1: 4.22K/F_6: CS24223F917

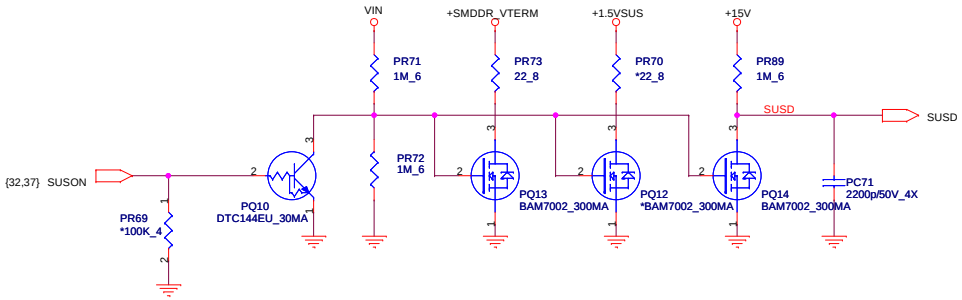
DDR3 for 1333MHZ----1.05V

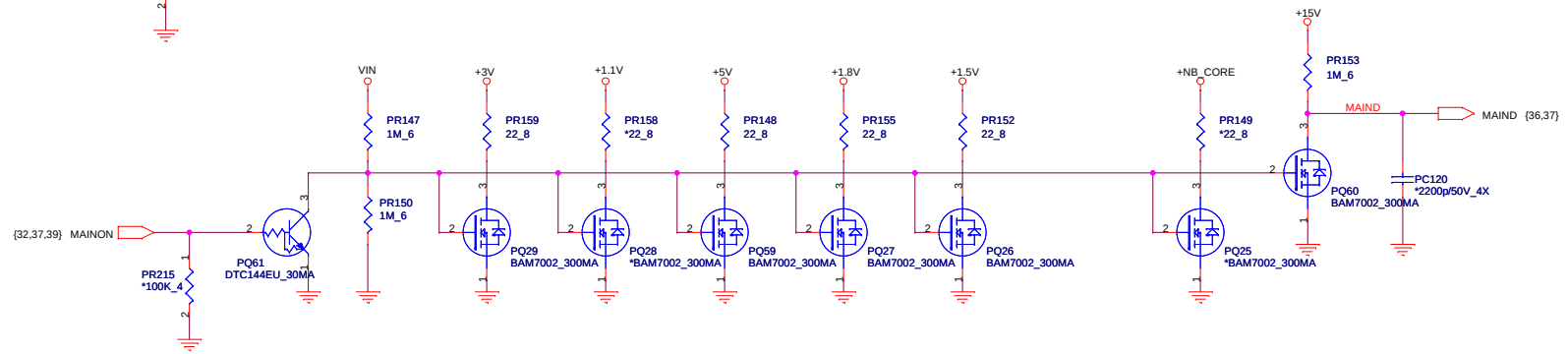
R2p: 22.6K/F_4: CS32262FB15











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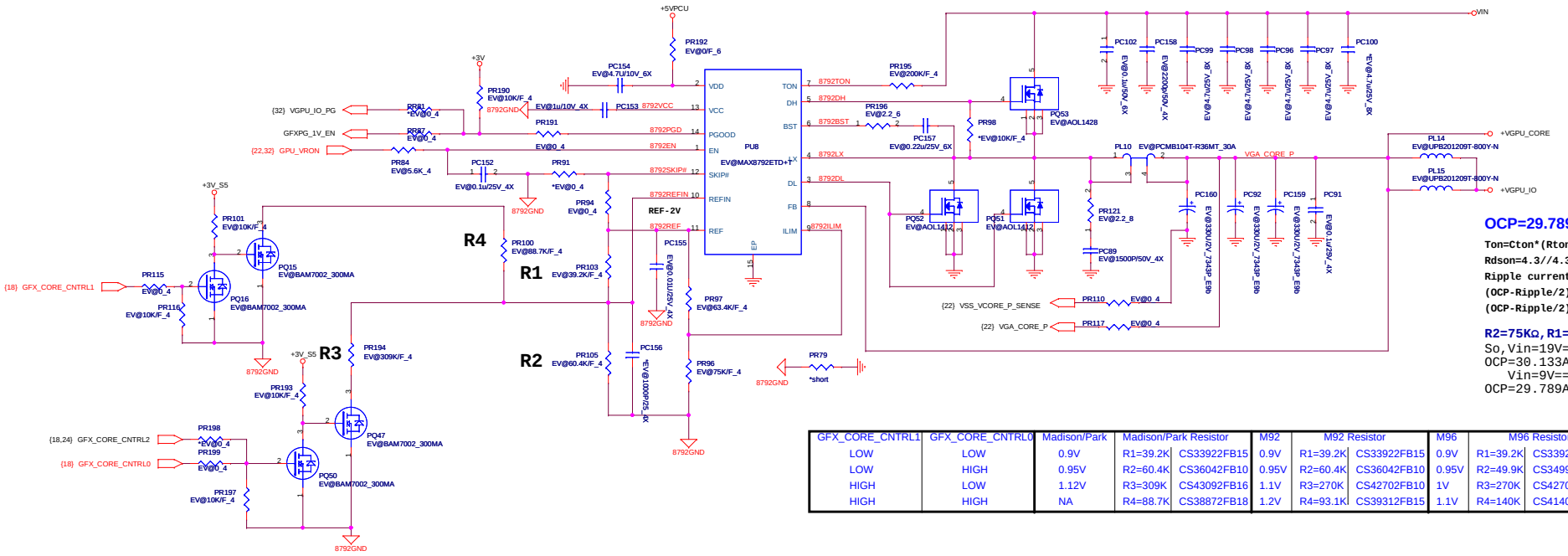
PROJECT : BL7

Size	Document Number	Rev
	Discharge/2.5/1.1/VDDR	D3A

Date: Friday, March 12, 2010 Sheet 41 of 44



OCP=29.789~30.133A

(Peak 28A, AVG 23.1A)

Total capacitor : 1400 uF

ESR : 2.25mΩ

F: 297k Hz

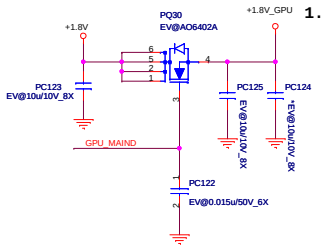
OCP=29.789~30.133A

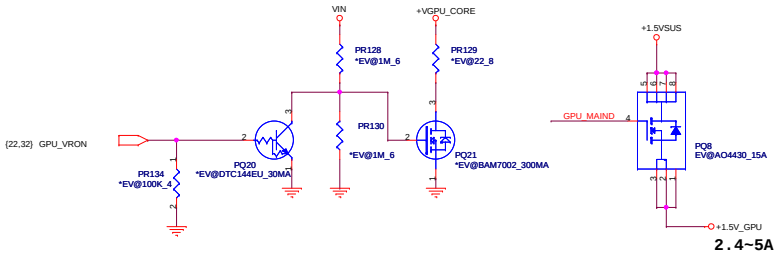
Ton=Cton*(Rton+6.5k)*(Vfb/Vout),F=297kHz
Rdson=4.3//4.3=2.15mΩ
Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)
(OCP-Ripple/2)=25.57
(OCP-Ripple/2)*Rds=Vref*((R2/(R1+R2))/20)

R2=75KΩ,R1=63.4KΩ

So,Vin=19V==>
OCP=30.133A;
Vin=9V==>
OCP=29.789A

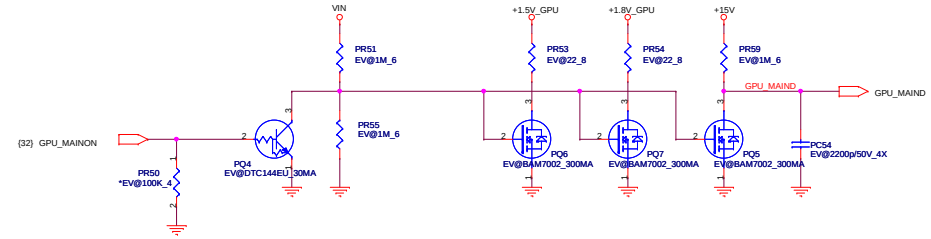
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor		M92	M92 Resistor		M96	M96 Resistor	
LOW	LOW	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15
LOW	HIGH	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=49.9K	CS34992FB10
HIGH	LOW	1.12V	R3=309K	CS43092FB16	1.1V	R3=270K	CS42702FB10	1V	R3=270K	CS42702FB10
HIGH	HIGH	NA	R4=88.7K	CS38872FB18	1.2V	R4=93.1K	CS39312FB15	1.1V	R4=140K	CS41402FB14

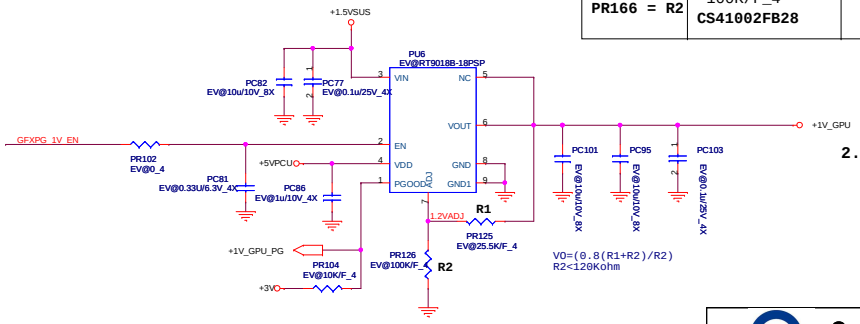




PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28



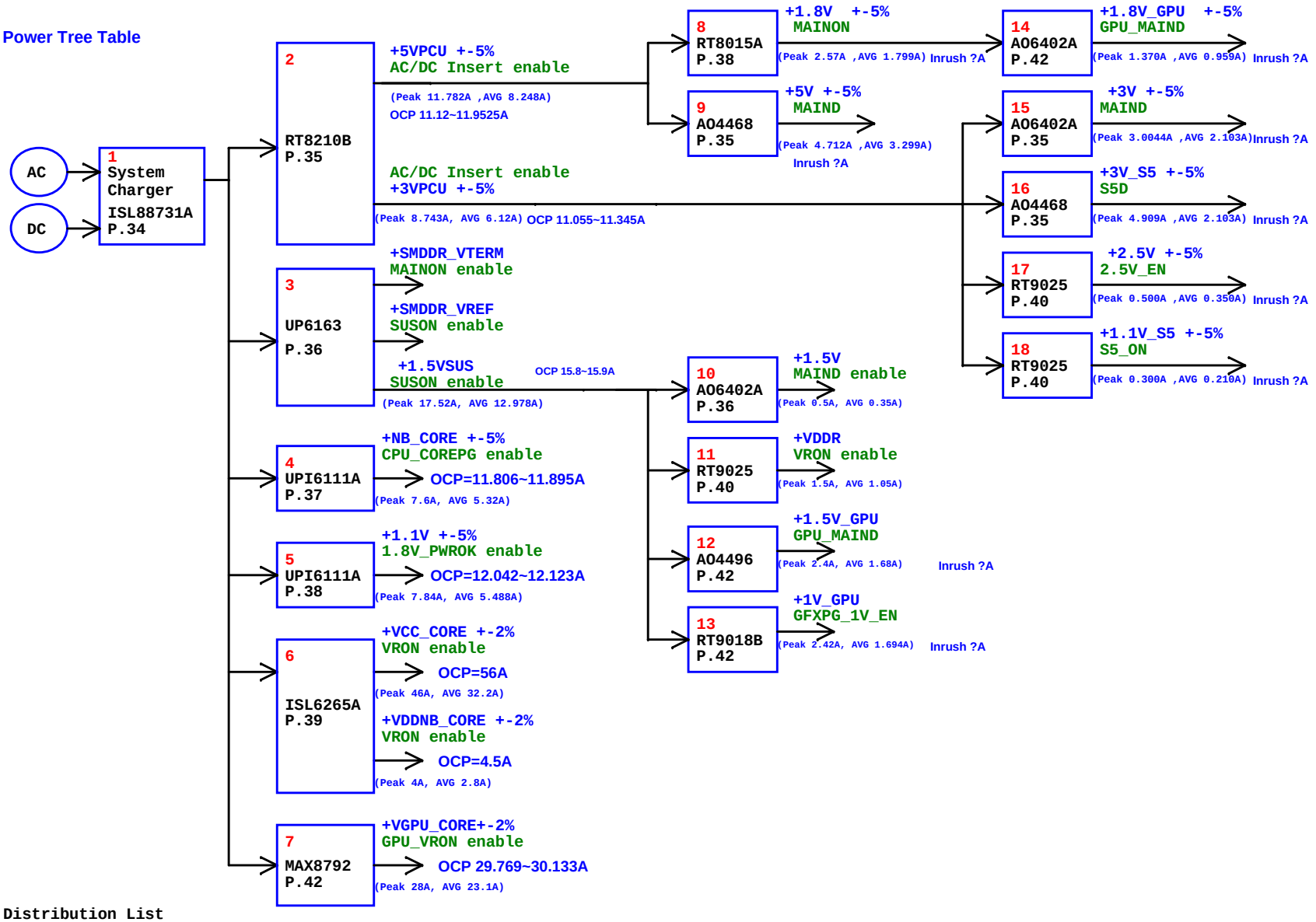


VO=(0.8(R1+R2)/R2)
R2<120Kohm

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	+VGPU_CORE (MAX8792)	D3A
Date: Friday, March 12, 2010	Sheet 42 of 44	

Power Tree Table



Power Distribution List

Power	Distribution

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: Power Tree Table | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 43 of 44

Model	REV	CHANGE LIST
BL7 MB	B1B	PAGE 2 : Change RP18 Value and Add R722 for VGA SKU,Change RP20 Value for 3G,and change R187 to SEL_HT66
		PAGE 3 : Mount R24,and Add Q58,R639,D47 and del R372,R33,Q5 for VGA Therm Detec
		PAGE 6 : Mount C78,C113,C569,C570,C28 for EMI request
		PAGE 11 : Add Board ID7 and Board ID8 and R644,R645,R646, and del R136 and change R578,R575,R559 for AMD suggestion
		PAGE 14 : Mount R573 and Del R572 for Gen I mode
		PAGE 18 : Change CTR port for Madison,Park,M92,M96 co-lay
		PAGE 19 : Change R546 value to 51 ohm port for Madison,Park,M92,M96 co-lay
		PAGE 22 : Delete reserve C423,C429,C427,C417,C430,C433,C422,C390,C409,C361,C376,C362,C378,C348,C349,C385,C374,C340,C352,C367,C350 for layout placement
		PAGE 22 : Add L73,L74,C896,C897,R723,R724,L72,R713,R711,R712R709 for Madison,Park,M92,M96 co-lay
		PAGE 23 : Add R714,R715,R716 for Madison,Park,M92,M96 co-lay
		PAGE 24 : Add U0,R720,R721,C895,R717 for Madison,Park,M92,M96 co-lay
		PAGE 25 : Change R1&R2 to bead for EMI request
		PAGE 26 : Add Q67,R735,R732,R736 for WLAN & BT Combo Module
		PAGE 27 : Del F2
		PAGE 30 : Add R636,R637,R635,R729,Q59,R734,R725,C899,C900,C619 for non over clocking
		PAGE 32 : Add R718,R719 for 3 cell Battery protect
		PAGE 33 : Add R222,R651,R652,R653 for EMI request
		PAGE 39 : Change PR207 to 3.92Kohm for OCP setting
		PAGE 39 : change PQ55,PQ57 footprint for higher current requirement
		PAGE 39 : Add PC199 for EMI
	C3A	PAGE 2 : Change RP13,RP14,RP15,RP16,RP17,RP21 to shortpad,RP22,And Change CLKREQ3#/CLKREQ4# netname to PCIE_CLK_REQ4#/PCIE_CLK_REQ3#
		PAGE 3 : Change R22,R90,R105,R120,R359,R34,R93,R42,R45 to shortpad,And Change T9,T10 Footprint and change R28 value,and mount R372,Q58,And del D25,D47,R368,R373,Q27,CN5,and Add Q65
		PAGE 7 : Change C594,C593 value
		PAGE 8 : Change R412,R402,R394,R423,R436,R413,R122 to shortpad
		PAGE 9 : Change R64,R75,L1,L5,L7,R87 to shortpad
		PAGE 10 : Change C843,C863,C870,C881 Value,and change R539 to shortpad
		PAGE 11 : Add R659 and change R247,R250,R141,R138 to shortpad,and mount R139,and del C885,U29
		PAGE 13 : Change R256,R262,R313,R310,R281,L42,L39 to shortpad
		PAGE 16 : Del R523,R519,R514,R508,R504,R496,R530,R527,R259,R260, and Add RN34,RN35,RN36,RN37,R496,R504,R508,R514 for EMI
		PAGE 17 : Change R100 to shortpad
		PAGE 18 : Change R464,R445 to shortpad
		PAGE 24 : Change R717 to 0 ohm
		PAGE 25 : Change R347,R348,L43 to shortpad ,and mount Q55,Q57,and change R633 value and add D46 and del D45
		PAGE 26 : Change R192,R193 to shortpad
		PAGE 27 : Del C301
		PAGE 28 : Change R383 and R489 to shortpad
		PAGE 30 : Change R390,R382,R389,R381,and change C197,C198,R65,R59 Value
		PAGE 31 : Change R480,R522,R242 to shortpad
		PAGE 32 : Add R727,and change R174,R181,R202 to shortpad,and change C355,C380 value,and reverse R658
		PAGE 33 : Change R94,R81,R654,R655 to shortpad
		PAGE 35 : Add PC202,PC203,PC204,PC205,PC201 for EMI
		PAGE 36: CHange PR108 footprint to shortpad
		PAGE 37: Change PQ43,PQ44 Value
		PAGE 39: Change PQ55,PQ57,PR144,PL12,PR139 Value
		PAGE 40: Change PL3,PQ41,PQ39,PQ40,PQ37,PQ38 Value,and Add PC206
		PAGE 41: Reverse PR70,PQ12,PQ158,PQ28,PR149,PQ25
	D3A	PAGE 11 : Reverse R163 and change R584,R579,R576 Value to 0_4
		PAGE 12 : Reverse R534,Y6,C817,C808
		PAGE 13 : Reverse C904,C905
		PAGE 16 : Add F2 for HDMI Safety issue
		PAGE 27 : Reverse C23 and C340
		PAGE 29 : Add R660,R661,R662
		PAGE 34 : Change R335,R312,R338,R632,R325 value to 1.5K_4 for LED lightness issue

MODEL BL7

PAGE	FROM	To
1	1A	1B
2	1A	1B
3	1A	1B
4	1A	1B
5	1A	1B
6	1A	1B
7	1A	1B
8	1A	1B
9	1A	1B
10	1A	1B
11	1A	1B
12	1A	1B
13	1A	1B
14	1A	1B
15	1A	1B
16	1A	1B
17	1A	1B
18	1A	1B
19	1A	1B
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22	1A	1B
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27	1A	1B
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36	1A	1B
37	1A	1B
38	1A	1B
39	1A	1B
40	1A	1B
41	1A	1B
42	1A	1B
43	1A	1B
44	1A	1B
45	1A	1B

DOC NO. 204					
PROJECT MODEL :	BL7	APPROVED BY:	Eric Lai	DATE:	2010/03/11
PART NUMBER:	31BL7MB0010	DRAWING BY:	Eric Lai	REVISON:	D3A

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: EE change list | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 44 of 44