Redwood BSW 11.6" Schematic Document

Braswell

2015-03-27
REV : A00

DY : None Installed
XDP: For CPU XDP Debug Port installed
APS: For Intel Auto Power Switch Debug Port
Share/nonS: Share ROM or Non Share ROM

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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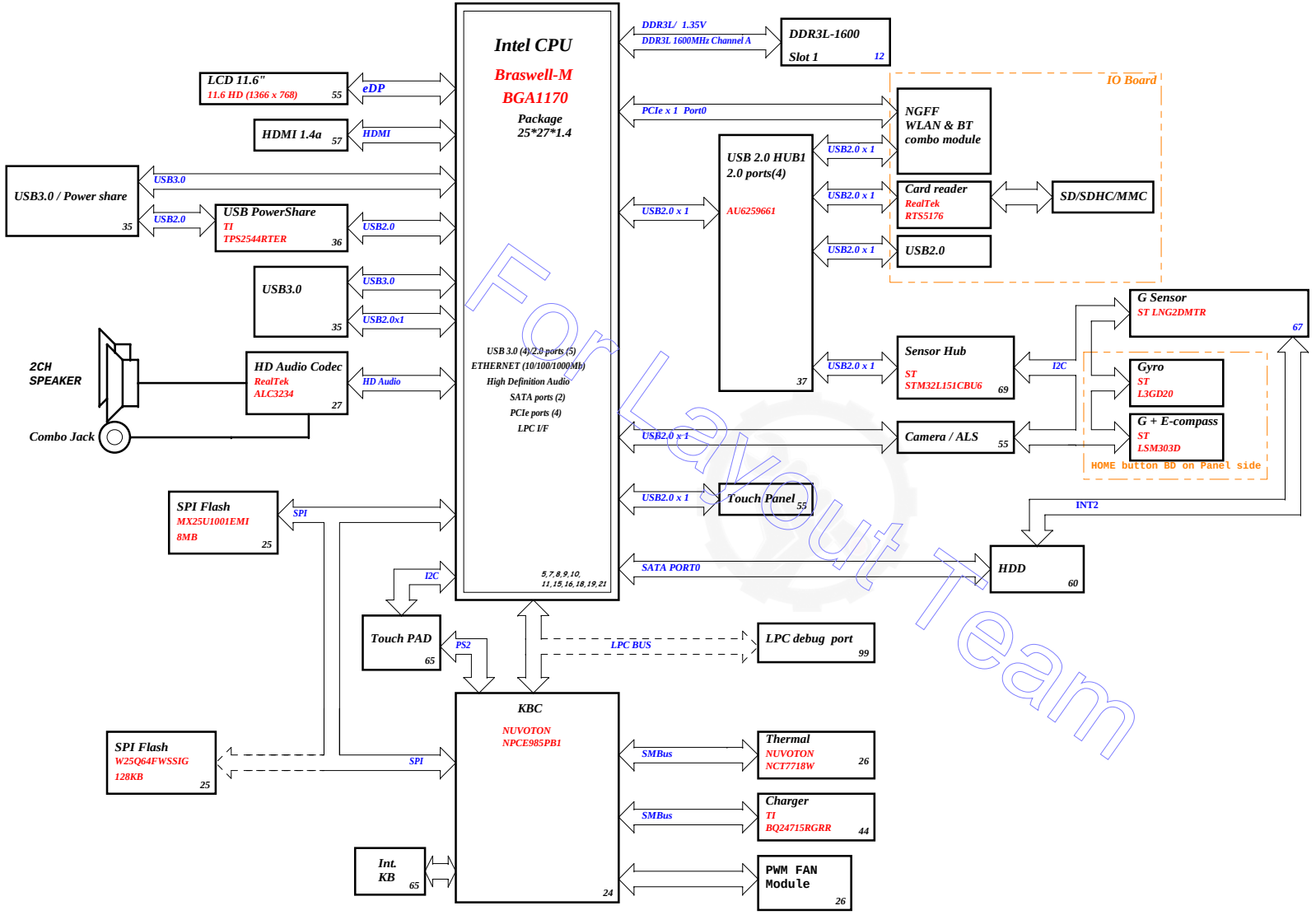
Project code : 4PD04K010001
PCB P/N : 14274
Revision : -1

Redwood BSW 11.6" Board Block Diagram



CHARGER BQ24715RGRR	44
INPUTS	OUTPUTS
19V_AD+	12V_BT+

SYSTEM DC/DC TPS51225	45
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5

CPU DC/DC NCP81201MNTXG	46-47
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC NCP81201MNTXG	48
INPUTS	OUTPUTS
19V_DCBATOUT	GFX_CORE

SYSTEM DC/DC SY8208DQNC	50
INPUTS	OUTPUTS
19V_DCBATOUT	1D05V_S5

Step Down Regulator TLV70218	50
INPUTS	OUTPUTS
3D3V_S5	1D15V_S5

SYSTEM DC/DC SY8206DQNC	51
INPUTS	OUTPUTS
19V_DCBATOUT	1D35V_CPU_VDDQ_S3

SYSTEM DC/DC APL5338XAI	51
INPUTS	OUTPUTS
1D35V_CPU_VDDQ_S3	0D675V_VREF_S0

Step Down Regulator SYW232DFC	52
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM LDO S-1339D15-M5001	53
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

SYSTEM LDO APL5930KAI	54
INPUTS	OUTPUTS
3D3V_S5	1D24V_S5

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Title: Block Diagram

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A2	Redwood BSW 11.6"	A00

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SSID = CPU

Blanking

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Title

(Reserved)

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A4	*Redwood BSW 11.6"*	*A00*

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SSID = CPU

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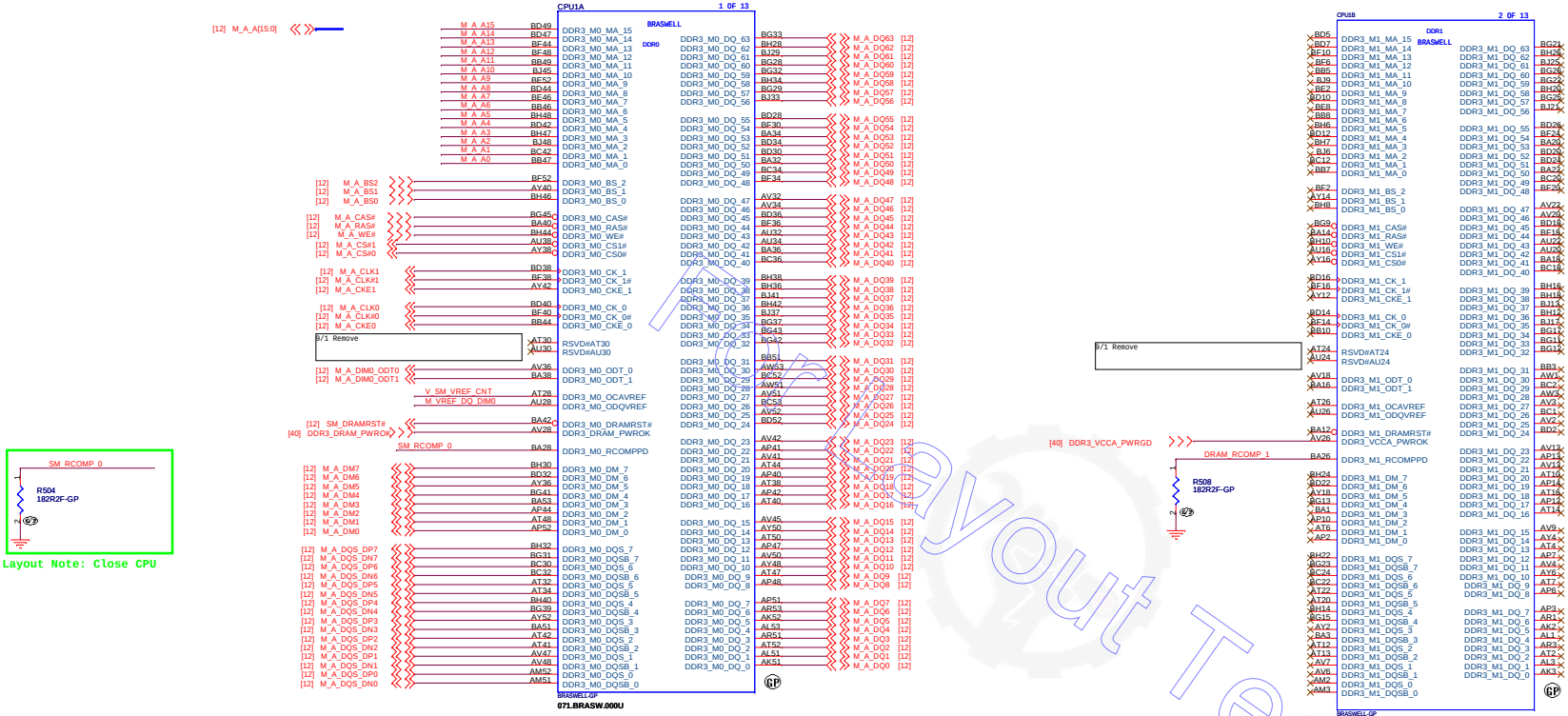
Title

(Reserved)

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

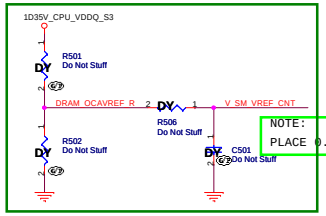
Date: Thursday, March 19, 2015 Sheet 4 of 109

SSID = CPU



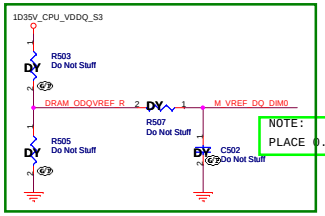
Layout Note: Close CPU

X01



NOTE:
PLACE 0.1U CAP CLOSE TO CPU

X01

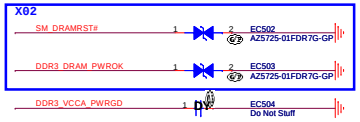


NOTE:
PLACE 0.1U CAP CLOSE TO CPU

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU TO CPU PINS ON M_VREF ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

X02



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Title: CPU (DDR)

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A2	Redwood BSW 11.6"	A00

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SSID = CPU

Blanking

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Title	CPU (CFG)	
Size: A4	Document Number: Redwood BSW 11.6"	Rev: A00
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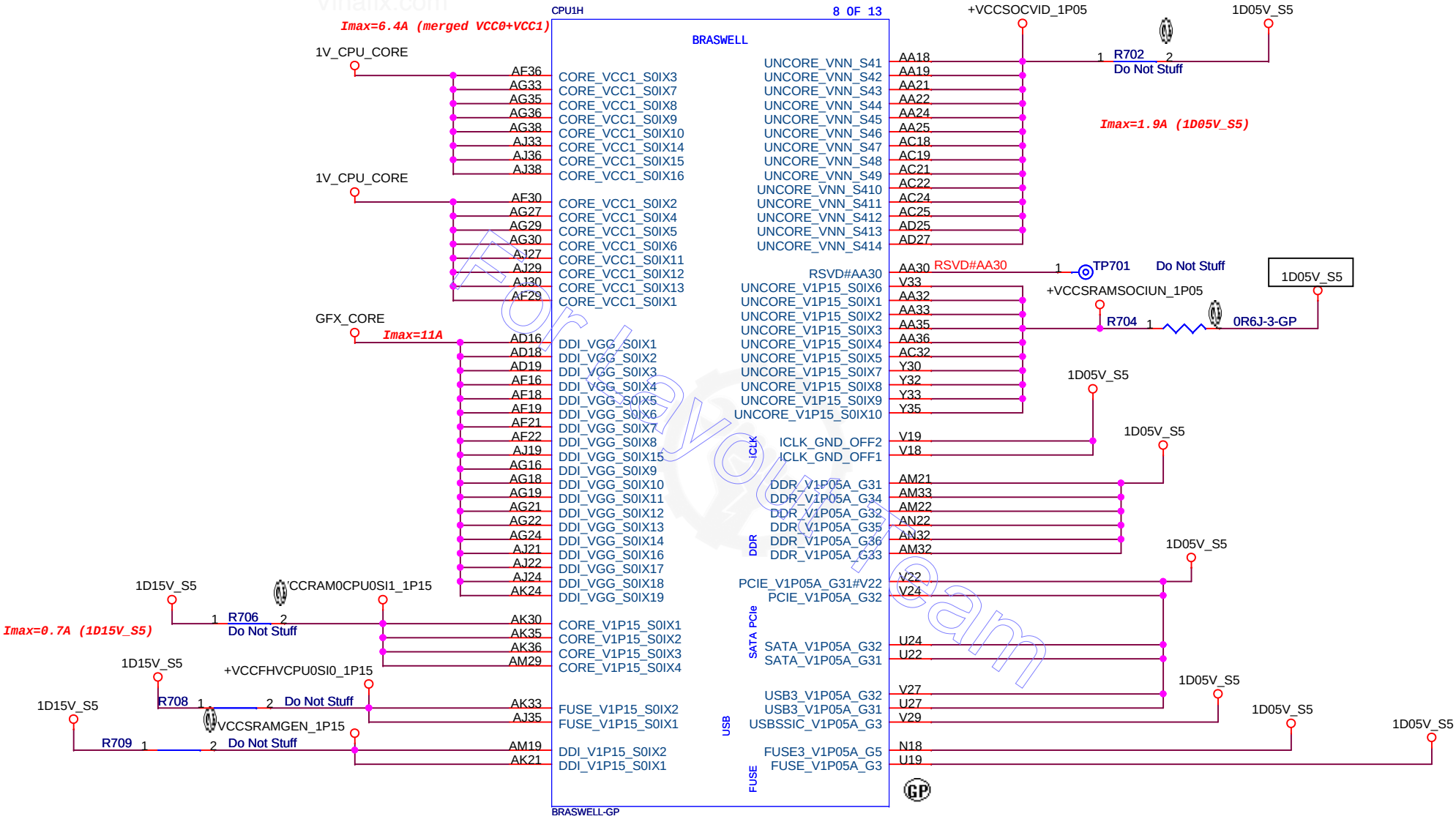
SSID = CPU



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Title: *CPU (VCC_CORE)*

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

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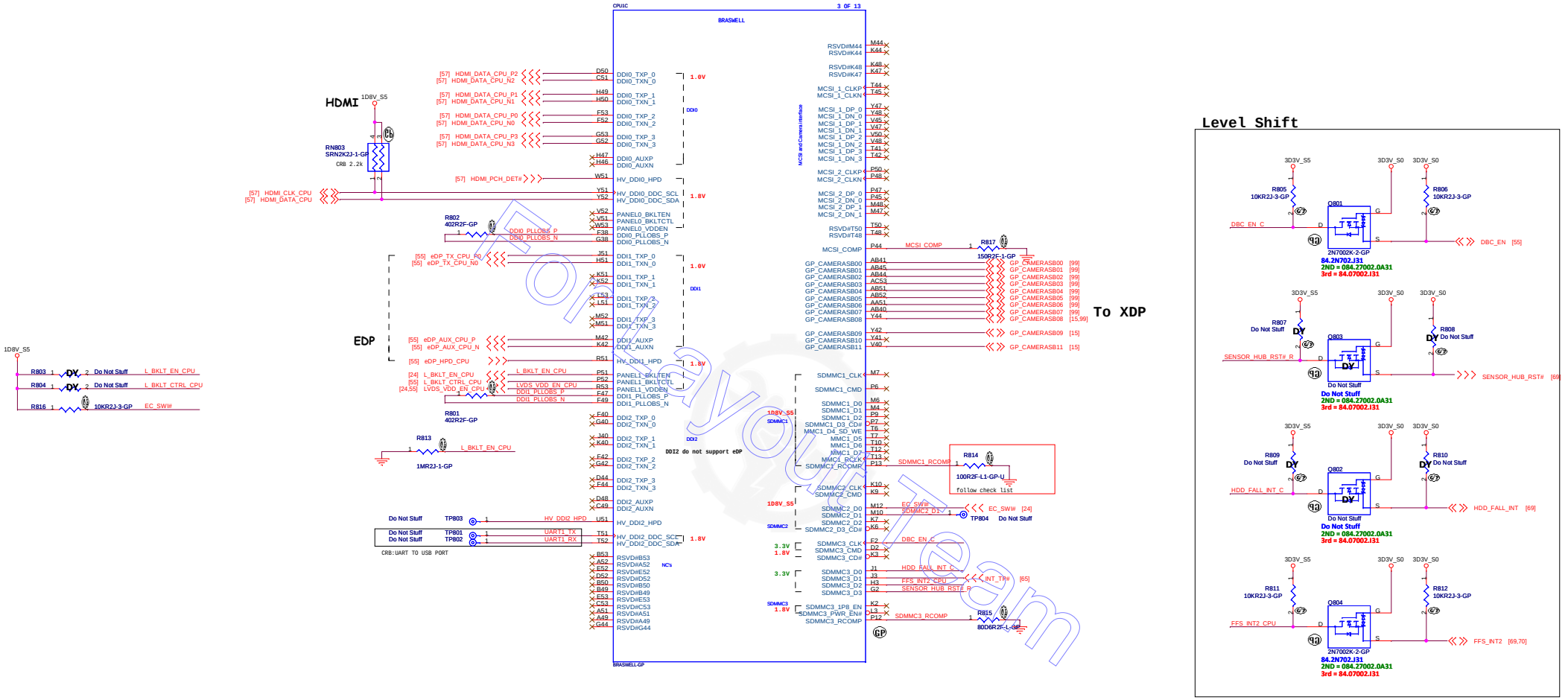
SSID = CPU



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Title: CPU (DDI/EDP/GPIO)

Size	Document Number	Rev
A2	Redwood BSW 11.6"	A00

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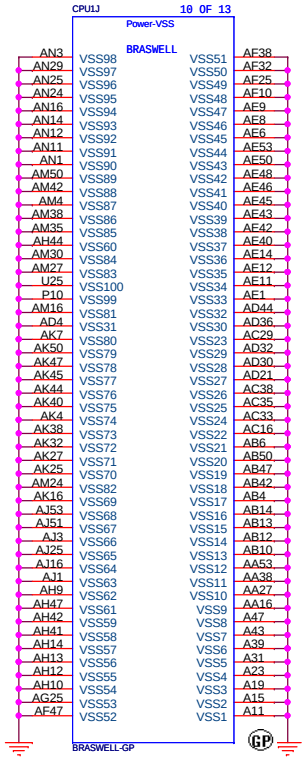
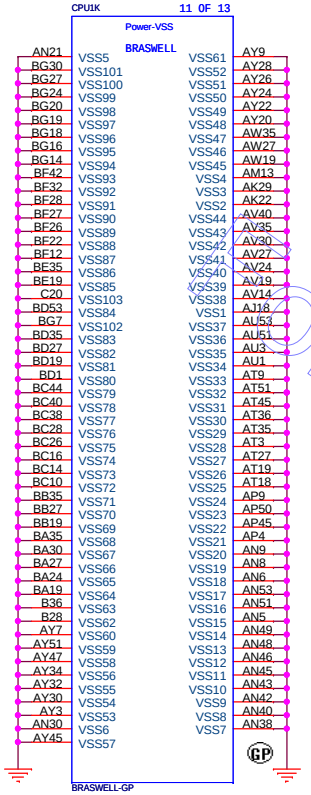
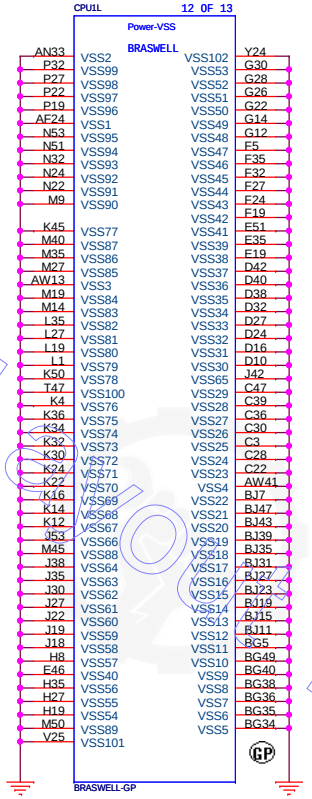
SSID = CPU







2014/04/25
Intel suggest

TP901 1
Do Not Stuff

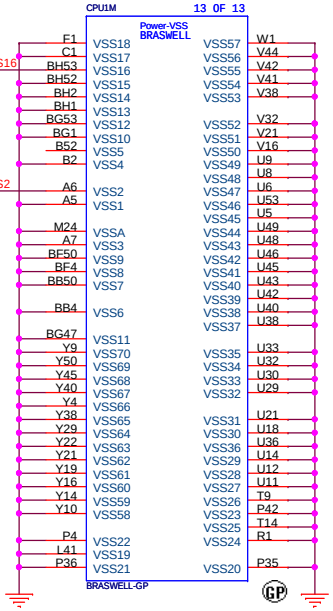
CPU_VSS16

B52 MAY NOT BE ABLE TO BREAK OUT IN ROUTING

TP902 1
Do Not Stuff

CPU_VSS2

2014/04/25
Intel suggest



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Title: CPU (VSS)

Size	Document Number	Rev
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SSID = CPU

PLACE ALL THE CAPS UNDER THE PKG SHADOW

1V_CPU_CORE

AF36, AG33, AG35, AG36, AG38, AJ33, AJ36, AJ38

PC1042 SC22U6D3V3MX-1-GP DY
PC1048 Do Not Stuff
C1027 SC4D7U6D3V2MX-GP-U
C1030 SC4D7U6D3V2MX-GP-U
C1029 SC4D7U6D3V2MX-GP-U
PC1058 SC22U6D3V3MX-1-GP
PC1059 Do Not Stuff

X02

PLACE ALL THE CAPS UNDER THE PKG SHADOW

1V_CPU_CORE

AF30, AG27, AG29, AG30, AJ27, AJ29, AJ30, AF29

PC1040 SC22U6D3V3MX-1-GP
PC1041 SC22U6D3V3MX-1-GP
C1033 SC4D7U6D3V2MX-GP-U
C1032 SC4D7U6D3V2MX-GP-U
C1036 SC4D7U6D3V2MX-GP-U
PC1060 Do Not Stuff DY
PC1061 Do Not Stuff DY

X02

+VCCSOCVID_1P05

AA18, AA19, AA21, AA22, AA24, AA25, AC18, AC19, AC21, AC22, AC24, AC25, AD25, AD27

C1024 SC1U10V2KX-1GP
C1025 SC1U10V2KX-1GP
C1001 SC1U10V2KX-1GP
C1002 SC1U10V2KX-1GP
C1008 SC1U10V2KX-1GP
PC1009 SC22U6D3V3MX-1-GP
PC1010 SC22U6D3V3MX-1-GP
PC1011 SC22U6D3V3MX-1-GP

1V_CPU_CORE

Near CPU Power 1V_CPU_CORE

PC1066 SC22U6D3V3MX-1-GP
PC1067 SC22U6D3V3MX-1-GP
PC1068 Do Not Stuff DY
PC1069 SC22U6D3V3MX-1-GP

+VCCSRAMSOCIUN_1P05

V33, AA32, AA33, AA35, AA36, AC32, Y30, Y32, Y33, Y35

C1006 SC1U10V2KX-1GP
C1007 SC1U10V2KX-1GP
C1003 SC1U10V2KX-1GP
C1004 SC1U10V2KX-1GP
C1005 SC1U10V2KX-1GP

+VCCSRAMSOCIUN_1P05

C1057 SC1U10V2KX-1GP
C1056 SC1U10V2KX-1GP

GFX_CORE

Near CPU Power GFX_CORE

PC1070 SC22U6D3V3MX-1-GP
PC1071 SC22U6D3V3MX-1-GP
PC1072 SC22U6D3V3MX-1-GP
PC1073 SC22U6D3V3MX-1-GP
PC1074 Do Not Stuff DY
PC1075 Do Not Stuff DY
PC1076 Do Not Stuff DY
PC1077 Do Not Stuff DY
PC1078 SC22U6D3V3MX-1-GP
PC1079 SC22U6D3V3MX-1-GP
PC1080 SC22U6D3V3MX-1-GP

GFX_CORE

PC1031 SC10U6D3V2MX-GP-U
PC1043 SC10U6D3V2MX-GP-U
PC1044 SC10U6D3V2MX-GP-U
PC1046 SC10U6D3V2MX-GP-U
PC1045 SC10U6D3V2MX-GP-U
PC1062 SC22U6D3V3MX-1-GP
PC1063 Do Not Stuff DY
PC1064 Do Not Stuff DY
PC1065 Do Not Stuff DY

1D05V_S5

AM21, AM33, AM22, AN22, AN32, AM32

C1013 SC1U10V2KX-1GP
PC1012 SC22U6D3V3MX-1-GP
PC1014 SC22U6D3V3MX-1-GP

1D05V_S5

V18, V19

C1018 SC1U10V2KX-1GP
C1050 Do Not Stuff DY

1D05V_S5

N18

C1015 SC1U10V2KX-1GP

+VCCRAM0CPU0SI1_1P15

C1034 SC1U10V2KX-1GP
C1035 SC1U10V2KX-1GP
C1037 SC1U10V2KX-1GP
C1038 SC1U10V2KX-1GP
C1039 SC1U10V2KX-1GP
C1049 SC1U10V2KX-1GP

1D05V_S5

V29

C1017 SC1U10V2KX-1GP
C1016 SC1U10V2KX-1GP

1D05V_S5

U19

C1022 SC1U10V2KX-1GP
C1023 SC1U10V2KX-1GP

1D05V_S5

V22, V24, U24, U22, V27, U27

C1020 SC1U10V2KX-1GP
C1021 SC1U10V2KX-1GP
C1019 SC1U10V2KX-1GP

+VCCSRAMGEN_1P15

C1047 SC1U10V2KX-1GP
C1026 SC1U10V2KX-1GP
C1028 SC1U10V2KX-1GP

1D05V_S5

PC1051 SC22U6D3V3MX-1-GP
PC1052 SC22U6D3V3MX-1-GP

PLACE CLOSE TO PIN 1 OF RA

1D05V_S5

PC1053 SC22U6D3V3MX-1-GP
PC1054 SC22U6D3V3MX-1-GP
PC1055 SC22U6D3V3MX-1-GP

PLACE CLOSE TO PIN 1 OF RB

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Title: CPU (Power CAP1)

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SSID = CPU

+VCCSFRPLLDDR_1P24_1P35

Close to CPU — SC1U10V2KX-1GP C1101; SC22U6D3V3MX-1-GP PC1118; DY Do Not Stuff C1143 — Close to DDR

+VCCCLKDDR_1P24_1P35

Close to CPU — SC1U10V2KX-1GP C1112; SC22U6D3V3MX-1-GP PC1119; DY Do Not Stuff C1144 — Close to DDR

1D05V_S5 — H10, G10 — SC1U10V2KX-1GP C1125

RTC_AUX_S5 — C5, B6 — SC1U10V2KX-1GP C1132 — 9/22 removed

3D3V_S5_PRIME — D4, E3 — SC1U10V2KX-1GP C1103 — 9/22 removed

1D35V_CPU_VDDQ_S3 — Place close to CPU — SC22U6D3V3MX-1-GP PC1120; SC22U6D3V3MX-1-GP PC1122; SC22U6D3V3MX-1-GP PC1123; SC22U6D3V3MX-1-GP PC1124

1D24V_S5 — V36, Y36 — SC1U10V2KX-1GP C1131

1D24V_S5 — T40, P40 — SC1U10V2KX-1GP C1106; SC1U10V2KX-1GP C1107

+V1P8_FUSE — SC1U10V2KX-1GP C1114

1D24V_S5 — M41 — SC1U10V2KX-1GP C1128

1D24V_S5 — U35, V35 — SC1U10V2KX-1GP C1138; SC1U10V2KX-1GP C1137

1D24V_S5 — Y27, Y25 — SC1U10V2KX-1GP C1134; DY Do Not Stuff C1147

1D24V_S5 — P38, V30, AC30 — SC1U10V2KX-1GP C1116; SC1U10V2KX-1GP C1117; DY Do Not Stuff C1148

+VCCUSB2_1P8 — SC1U10V2KX-1GP C1104; SC1U10V2KX-1GP C1105

+VCCUSB2_3P3 — SC1U10V2KX-1GP C1115

1D24V_S5 — AF35, AD35, AD38, AC36 — SC1U10V2KX-1GP C1109; DY Do Not Stuff C1149

1D24V_S5 — H44 — SC1U10V2KX-1GP C1108; DY Do Not Stuff C1150

1D24V_S5 — P41 — SC1U10V2KX-1GP C1129

+VCCPADCF2SI0_E_1P80 — SC1U10V2KX-1GP C1113; SC1U10V2KX-1GP C1121; SC1U10V2KX-1GP C1130

+VCCPADCF1SI0_1P80 — SC1U10V2KX-1GP C1110; SC1U10V2KX-1GP C1111

+VCCCFIOAZA_1P80 — SC1U10V2KX-1GP C1102

+VCCPADCF1SI0_1P8_3P3 — SC1U10V2KX-1GP C1133

+VCCPADCF3SI0_1P8_3P3 — SC1U10V2KX-1GP C1126; SC1U10V2KX-1GP C1127

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Title: CPU (Power CAP2)

Size: A3 | Document Number: Redwood BSW 11.6" | Rev: A00

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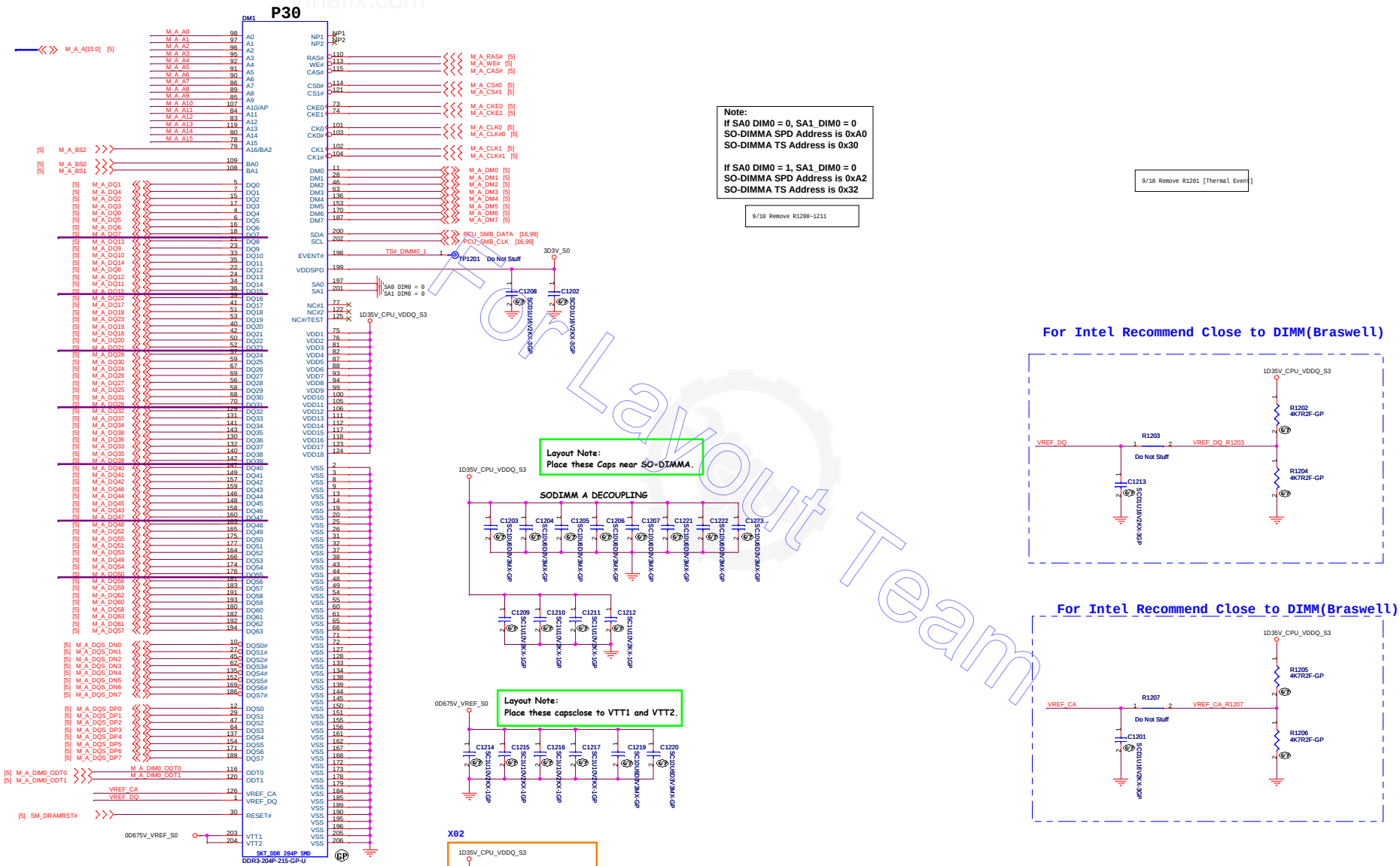
SSID = MEMORY



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Title: DDR3-SODIMM1

Size: A2 | Document Number: Redwood BSW 11.6" | Rev: A00

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SSID = MEMORY

Blanking

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Title: *(Reserved)*

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SSID = CPU

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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the PMC_RSMRST_N signal (check list)

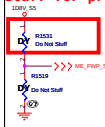
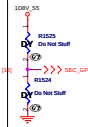
Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERASB08	GP_CAMERASB09	GP_CAMERASB11
Schematic						Stuff for production 								
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal Operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable Weak internal pull-down	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller Weak internal pull-down	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Week)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1 - DDI0 Detect, 0 - Disable	High
DDI1 Detected	GPIO_SUS1	PD	1 - DDI1 Detect, 0 - Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1 - Boot from SPI, 0 - Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0 - Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select-	SEC_GPIO_SUS8	PU	1 - 1.35V, 0 - 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1 - Bypass with 1.05V, 0 - No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1 - PMC, 0 - Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	PD	1 - Bypass, 0 - No bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	PD	1 - Bypass, 0 - No bypass	Low
RTC OSC Bypass	GP_CAMERASB11	PD	1 - Bypass, 0 - No bypass	Low

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

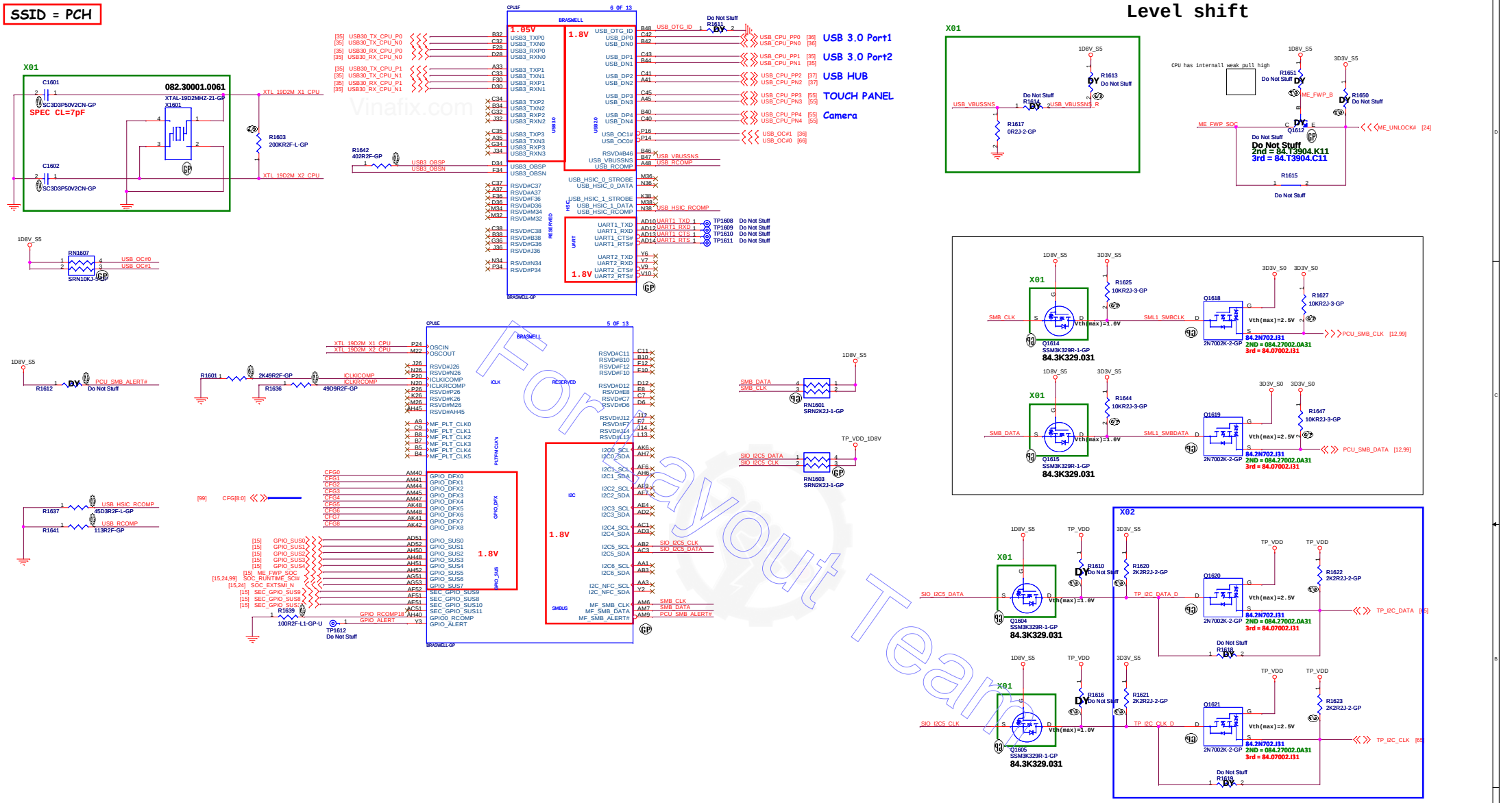
File: CPU(STRAP)

Size: A1 | Document Number: Redwood BSW 11.6" | Rev: A00

Date: Wednesday, March 26, 2014 | Sheet 15 of 39

SSID = PCH

Level shift



Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (USB/LPC/GPIO)

Size	Document Number	Rev
A2	Redwood BSW 11.6"	A00

Date: Wednesday, March 25, 2015 Sheet 16 of 109

SSID = CPU

Blanking

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

Date: Thursday, March 19, 2015 Sheet 17 of 109

SSID = PCH

Layout Note:
place on bottom side

APS debug port

reserve the 0402 0.1u caps on reset for EMI.

reserve the 0402 0.1u caps on reset for EMI

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CLK/SPI/SIDEBAND/JTAG)

Size: A2 | Document Number: Redwood BSW 11.6" | Rev: A00

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SSID = PCH

CPU1D 4 OF 13 BRASWELL

WLAN [66] PCIE_TX_CON_P0 [66] PCIE_TX_CON_N0 [66] PCIE_RX_CPU_P0 [66] PCIE_RX_CPU_N0

C1915 C1916 SCD1U16V2KX-3GP PCIE_TX_CPU_P0 PCIE_TX_CPU_N0

PCIE_TXP0 PCIE_TXN0 PCIE_RXP0 PCIE_RXN0 PCIE_TXP1 PCIE_TXN1 PCIE_RXP1 PCIE_RXN1 PCIE_TXP2 PCIE_TXN2 PCIE_RXP2 PCIE_RXN2 PCIE_TXP3 PCIE_TXN3 PCIE_RXP3 PCIE_RXN3 — 1.0V, PCIe

PEG_CLKREQ0_CPU# PEG_CLKREQ1_CPU# PEG_CLKREQ2_CPU# PEG_CLKREQ3_CPU# — PCIE_CLKREQ0# PCIE_CLKREQ1# PCIE_CLKREQ2# PCIE_CLKREQ3# — 1.8V

[66] PEG_CLK0_CPU [66] PEG_CLK0_CPU# — CLK_DIFF_P_0 CLK_DIFF_N_0 CLK_DIFF_P_1 CLK_DIFF_N_1 CLK_DIFF_P_2 CLK_DIFF_N_2 CLK_DIFF_P_3 CLK_DIFF_N_3 CLK_DIFF_P_4 CLK_DIFF_N_4

R1930 402R2F-GP PCIE_OBSP_CPU PCIE_OBSN_CPU — PCIE_OBSP PCIE_OBSN

SPI1_CLK SPI1_CS0# SPI1_CS1# SPI1_MISO SPI1_MOSI — 1.8V, SPI

SATA_TXP0 SATA_TXN0 SATA_RXP0 SATA_RXN0 SATA_TXP1 SATA_TXN1 SATA_RXP1 SATA_RXN1 — 1.8V, SATA

SATA_LED# SATA_GP0 SATA_GP1 SATA_GP2 SATA_GP3 — SATA_DEVSLP_SOC, SATA_GP3, TP1901 Do Not Stuff

SATA_OBSP SATA_OBSN — R1931 402R2F-GP

FST_SPI_CLK FST_SPI_CS0# FST_SPI_CS1# FST_SPI_CS2# FST_SPI_D0 FST_SPI_D1 FST_SPI_D2 FST_SPI_D3 — 1.8V, FAST SPI

SPI_CLK_CPU R1911 10R2J-2-GP SPI_CLK_ROM [25]

SPI_CS_CPU_N0 R1909 33R2J-2-GP SPI_CS_ROM_N0 [25]

SPI_SI_CPU R1910 10R2J-2-GP SPI_SI_ROM [25] SPI_SO_CPU [25]

SPI_WP_CPU [25] SPI_HOLD_CPU [25]

MF_HDA_RST# MF_HDA_SDI1 MF_HDA_CLK MF_HDA_SDI0 MF_HDA_SYNC MF_HDA_SDO MF_HDA_DOCKEN# MF_HDA_DOCKRST# — 1.5V

HDA_RST# CPU HDA_BITCLK_CPU HDA_SDIN0_CPU HDA_SYNC_CPU HDA_SDOUT_CPU — HDA_SDIN0_CPU [27]

SPKR — HDA_SPKR [27] — AUDIO

GP_SSP_2_CLK GP_SSP_2_FS GP_SSP_2_TXD GP_SSP_2_RXD — 1.8V

HDD

SATA_TXP0 SATA_TXN0 SATA_RXP0 SATA_RXN0 — SATA_TX_CPU_P0 [60] SATA_TX_CPU_N0 [60] SATA_RX_CPU_P0 [60] SATA_RX_CPU_N0 [60]

1D8V_S5

RN1901 SRN10K1-5-GP — PEG_CLKREQ1_CPU# PEG_CLKREQ2_CPU#

R1901 10KR2J-3-GP PEG_CLKREQ0_CPU#

R1903 10KR2J-3-GP PEG_CLKREQ3_CPU#

HDA_RST# CPU — C1910 DY Do Not Stuff

X01

HDA_RST# CPU — R1928 75R2F-GP — HDA_RST#_CODEC [27,29]

HDA_BITCLK_CPU — R1927 75R2F-GP — HDA_BITCLK_CODEC [27]

HDA_SYNC_CPU — R1926 75R2F-GP — HDA_SYNC_CODEC [27]

HDA_SDOUT_CPU — R1929 75R2F-GP — HDA_SDOUT_CODEC [27]

X02

1D8V_S0 1D8V_S0 3D3V_S0

R1906 100KR2J-1-GP R1907 10KR2J-3-GP

SATA_DEVSLP_SOC — Q1902 DMN5L06K-7-GP — SATA_DEVSLP [60]

84.05067.031

VIL=0.35*1.8=0.63 V

3D3V_S5 R1902 DY Do Not Stuff

PEG_CLKREQ0_CPU# D1901 DY Do Not Stuff

PEG_CLKREQ0_D

3D3V_S0 Q1901 DY Do Not Stuff

3D3V_S0 R1904 DY Do Not Stuff — PEG_CLKREQ0_WLAN# [66]

Do Not Stuff
2ND = 084.27002.0A31
3rd = 84.07002.I31

PEG_CLKREQ0_CPU# R1905 DY Do Not Stuff

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SATA/PCIE/IHDA)

Size: A3 | Document Number: Redwood BSW 11.6" | Rev: A00

Date: Wednesday, March 25, 2015 | Sheet 19 of 109

SSID = PCH

Blanking

Redwood MLK list

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
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SSID = CPU

1D35V_CPU_VDDQ_S3 — +VCCSFRPLLDDR_1P24_1P35
R2111 Do Not Stuff

1D35V_CPU_VDDQ_S3 — +VCCCLKDDR_1P24_1P35
R2112 Do Not Stuff

3D3V_S5_PRIME — +VCCPADCF3SI0_1P8_3P3
R2113 Do Not Stuff
Imax=141mA (VSDIO 3.3V)
3D3V_S0
R2114 DY Do Not Stuff
SD IO SUPPLY

3D3V_S5_PRIME — +VCCPADCF1SI0_1P8_3P3
R2115 Do Not Stuff
Imax=147.59mA
LPC IO SUPPLY

1D5V_S0 — +VCCCFIOAZA_1P80
R2105 Do Not Stuff
Imax=16.53mA
1D8V_S5
R2106 DY Do Not Stuff
AUDIO IO SUPPLY

1D8V_S5 Imax=550mA
R2107 +VCCPADCF1SI0_1P80 Do Not Stuff
R2108 +VCCPADCF2SI0_E_1P80 Do Not Stuff
R2109 +VCCUSB2_1P8 Do Not Stuff
R2110 +V1P8_FUSE Do Not Stuff

Imax=200mA (3.3V_PRIME)
3D3V_S5_PRIME — +VCCUSB2_3P3
R2118 Do Not Stuff

P21

CPU1I 9 OF 13 BRASWELL-GP

+VCCCLKDDR_1P24_1P35 — +VCCSFRPLLDDR_1P24_1P35
1D35V_CPU_VDDQ_S3 Imax=1.9A (VDDQ)

DDR:
AN27 DDRSFR_VDDQ_G_S4
AM25 DDR_VDDQ_G_S42
BE1 DDR_VDDQ_G_S416
BE53 DDR_VDDQ_G_S419
BJ2 DDR_VDDQ_G_S426
BJ3 DDR_VDDQ_G_S427
BJ49 DDR_VDDQ_G_S428
BJ5 DDR_VDDQ_G_S429
BH50 DDR_VDDQ_G_S425
BH5 DDR_VDDQ_G_S424
BH49 DDR_VDDQ_G_S423
BH4 DDR_VDDQ_G_S422
BE3 DDR_VDDQ_G_S417
BG51 DDR_VDDQ_G_S421
BG3 DDR_VDDQ_G_S420
BJ51 DDR_VDDQ_G_S430
BJ52 DDR_VDDQ_G_S431
AY10 DDR_VDDQ_G_S414
AY44 DDR_VDDQ_G_S415
AV44 DDR_VDDQ_G_S413
AV10 DDR_VDDQ_G_S410
BE51 DDR_VDDQ_G_S418
AV38 DDR_VDDQ_G_S412
AV16 DDR_VDDQ_G_S411
AU36 DDR_VDDQ_G_S49
AU18 DDR_VDDQ_G_S48
AN36 DDR_VDDQ_G_S47
AN35 DDR_VDDQ_G_S46
AN19 DDR_VDDQ_G_S45
AN18 DDR_VDDQ_G_S44
AM36 DDR_VDDQ_G_S43
AM18 DDR_VDDQ_G_S41

+VCCPADCF1SI0_1P8_3P3 — +VCCPADCF3SI0_1P8_3P3
+VCCCFIOAZA_1P80
+VCCPADCF2SI0_E_1P80
E1 SDIO_V3P3A_V1P8A_G31
E2 SDIO_V3P3A_V1P8A_G32
G1 SDIO_V3P3A_V1P8A_G33
AH4 UNCORE_V1P8A_G32
AF4 UNCORE_V1P8A_G31
Y18 GPIO_V1P8A_G35
AD33 GPIO_V1P8A_G31
AK18 GPIO_V1P8A_G33
AF33 GPIO_V1P8A_G32
AK19 GPIO_V1P8A_G34
+VCCPADCF1SI0_1P80

BRASWELL Removal of 1.24V VR
Imax=0.55A (1.24V)

DDR:
V36 DDI_VDDQ_G31
Y36 DDI_VDDQ_G32
T40 MIPI_V1P2A_G32
P40 MIPI_V1P2A_G31
Y27 ICLK_VSFR_G32
Y25 ICLK_VSFR_G31
P38 CORE_VSFR_G35
V30 CORE_VSFR_G36
AC30 CORE_VSFR_G3
AF35 CORE_VSFR_G34
AD35 CORE_VSFR_G32
AD38 CORE_VSFR_G33
AC36 CORE_VSFR_G31

USB:
M41 USBHSIC_V1P2A_G3
U35 USB_VDDQ_G32
V35 USB_VDDQ_G33
H44 USB_VDDQ_G31
P41 USBSSIC_V1P2A_G3
AA29 USB_V1P8A_G3
C23 USB_V3P3A_G32
B22 USB_V3P3A_G31

RTC:
C5 RTC_V3P3RTC_G52
B6 RTC_V3P3RTC_G51
D4 RTC_V3P3A_G51
E3 RTC_V3P3A_G52

FUSE:
U16 FUSE_V1P8A_G3
H10 FUSE1_V1P05A_G4
G10 FUSE0_V1P05A_G3
A3 RSVD_VSS#A3
K20 RSVD#K20
M20 RSVD#M20

1D24V_S5 — R2104 MIPI_V1P2A Do Not Stuff
1D24V_S5 — R2116 USBHSIC_V1P2A Do Not Stuff
1D24V_S5 — R2117 USBSSIC_V1P2A Do Not Stuff
+VCCUSB2_1P8
+VCCUSB2_3P3
RTC_AUX_S5 — 3D3V_S5_PRIME
+V1P8_FUSE
1D05V_S5
RSVD_VSS#A3 — TP2101 Do Not Stuff

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)
Size: A3 | Document Number: Redwood BSW 11.6" | Rev: A00
Date: Wednesday, March 25, 2015 | Sheet 21 of 109

Blanking

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
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Redwood MLK 1st

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Taipei Hsien 221, Taiwan, R.O.C.

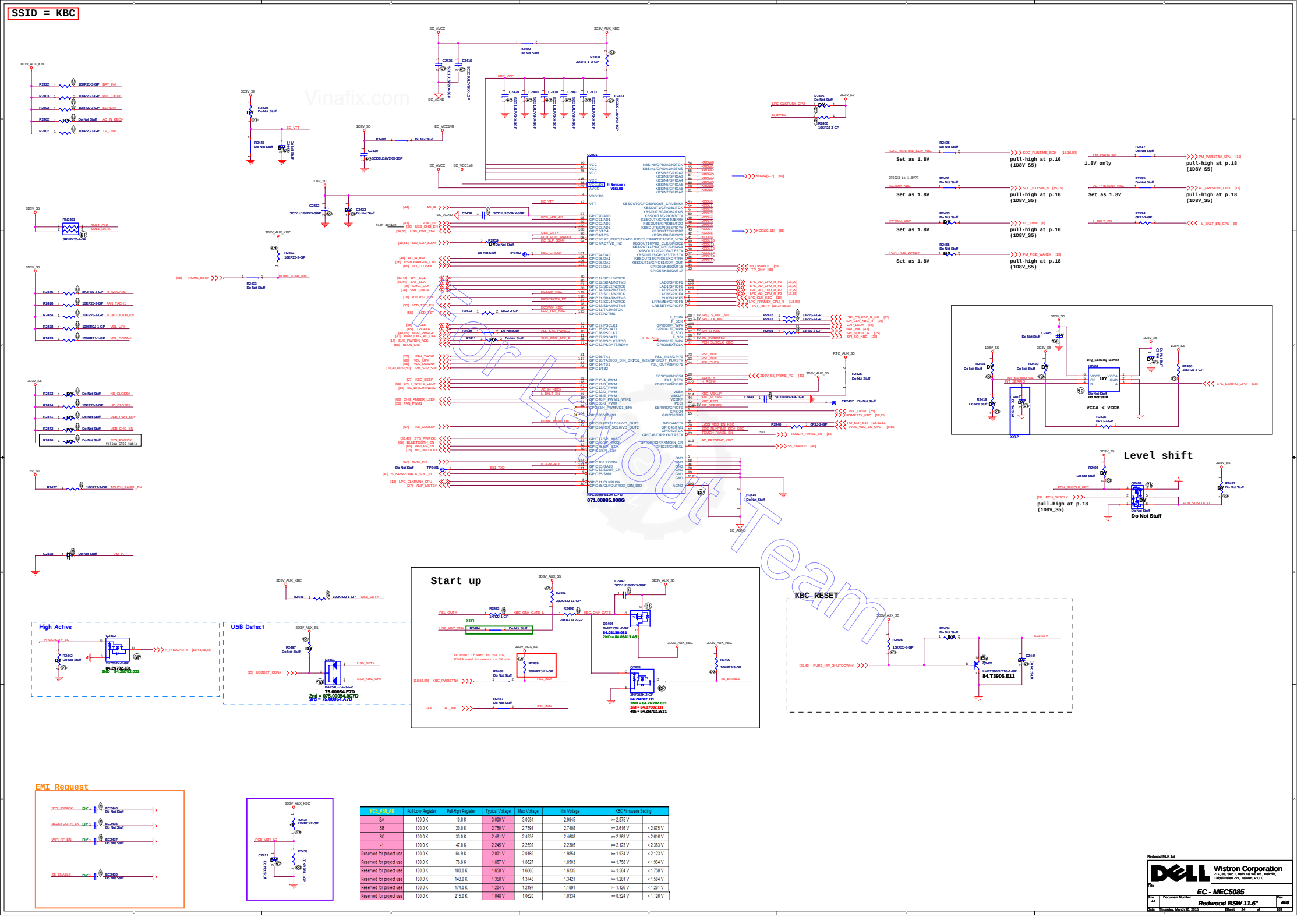
Title

(Reserved)

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

Date: Thursday, March 19, 2015 Sheet 23 of 109

SSID = KBC



PCB_VER_A0	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	>= 2.123 V	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0629	1.0334	>= 0.524 V	< 1.126 V

Redwood MLK 1st

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Taipei Hsien 221, Taiwan, R.O.C.

Title: EC - MEC5085

Size: A1 | Document Number | Rev: A00

Redwood BSW 11.6"

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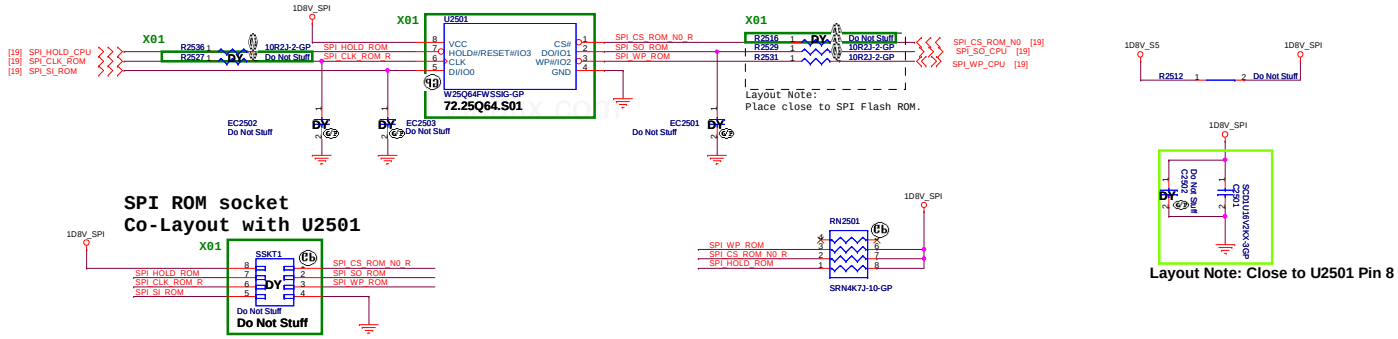
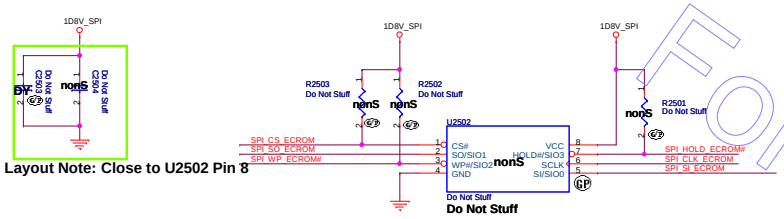
SSID = Flash.ROM

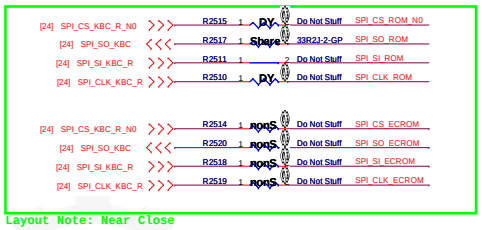
SPI FLASH ROM (8M byte) for CPU



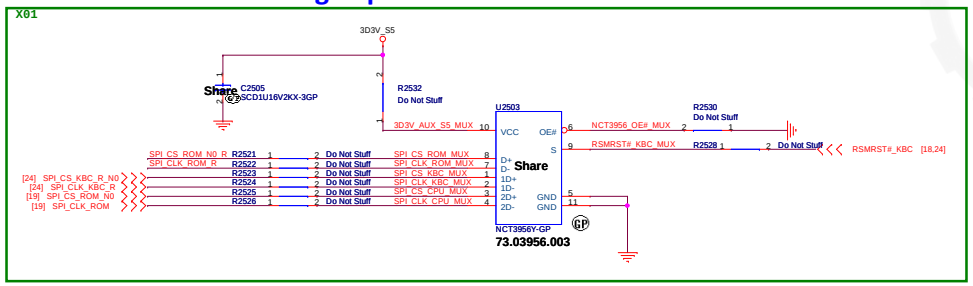
SPI FLASH ROM (128k byte) for KBC



SPI ROM link to KBC



High Speed Switch for Share ROM

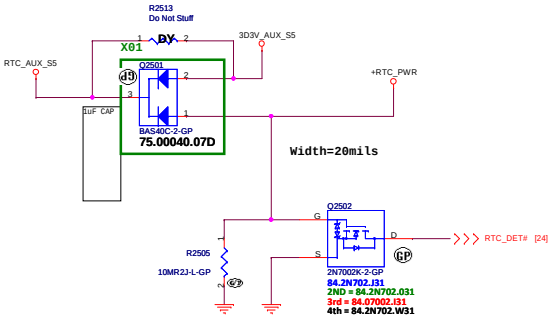


5240626:SPI Signals do not get tri-stated / MUX Sol.

Truth Table

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

SSID = RTC



Redwood MLK 1st

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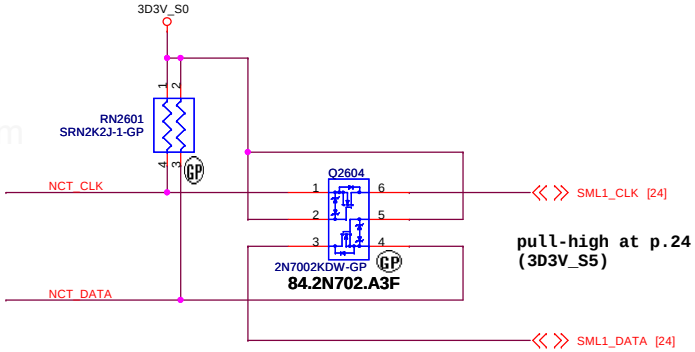
Title: Flash/RTC

Size: A2 | Document Number: Redwood BSW 11.6" | Rev: A00

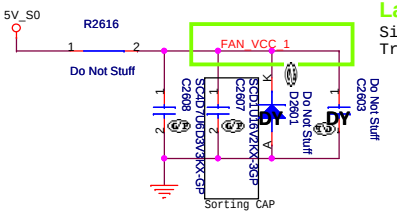
Date: Wednesday, March 25, 2015 | Sheet 25 of 109

SSID = Thermal

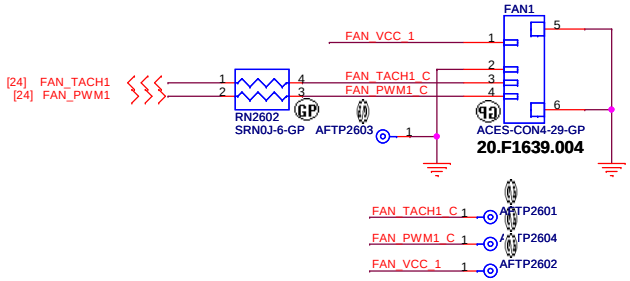
EE Note:
1. T8: PURE_HW_SHUTDOWN# through Q2603.
2. THM_SENSOR: Thermal sensor NCT7718W solution.



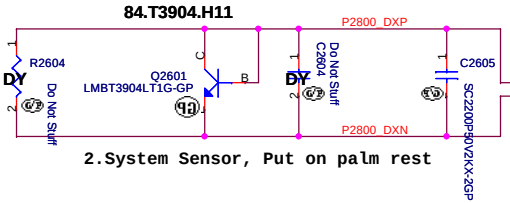
PWM FAN1

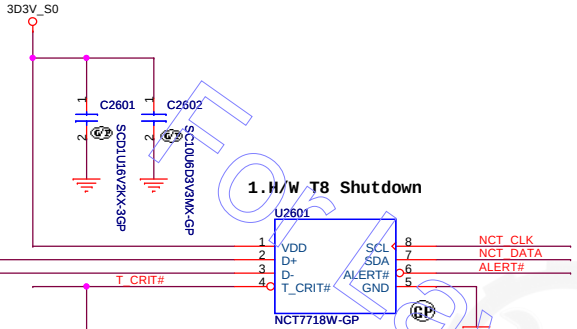


Layout Note:
Signal Routing Guideline:
Trace width = 15mil

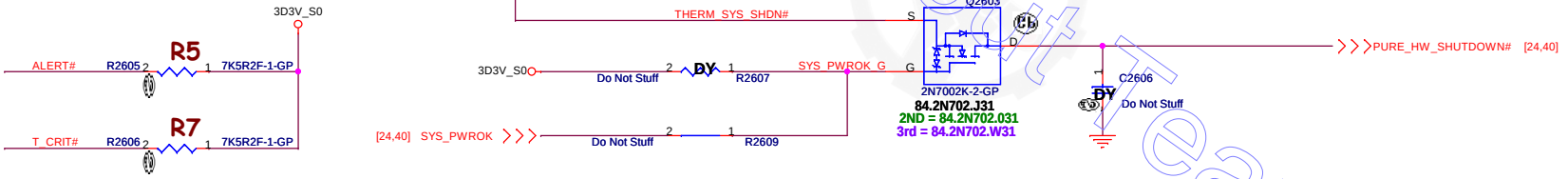


Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.





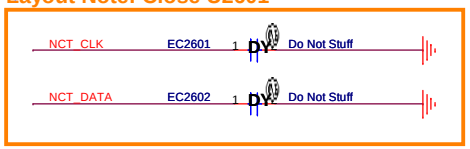
Thermal sensor NCT 7718W



The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Layout Note: Close U2601



Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal
Size: A3
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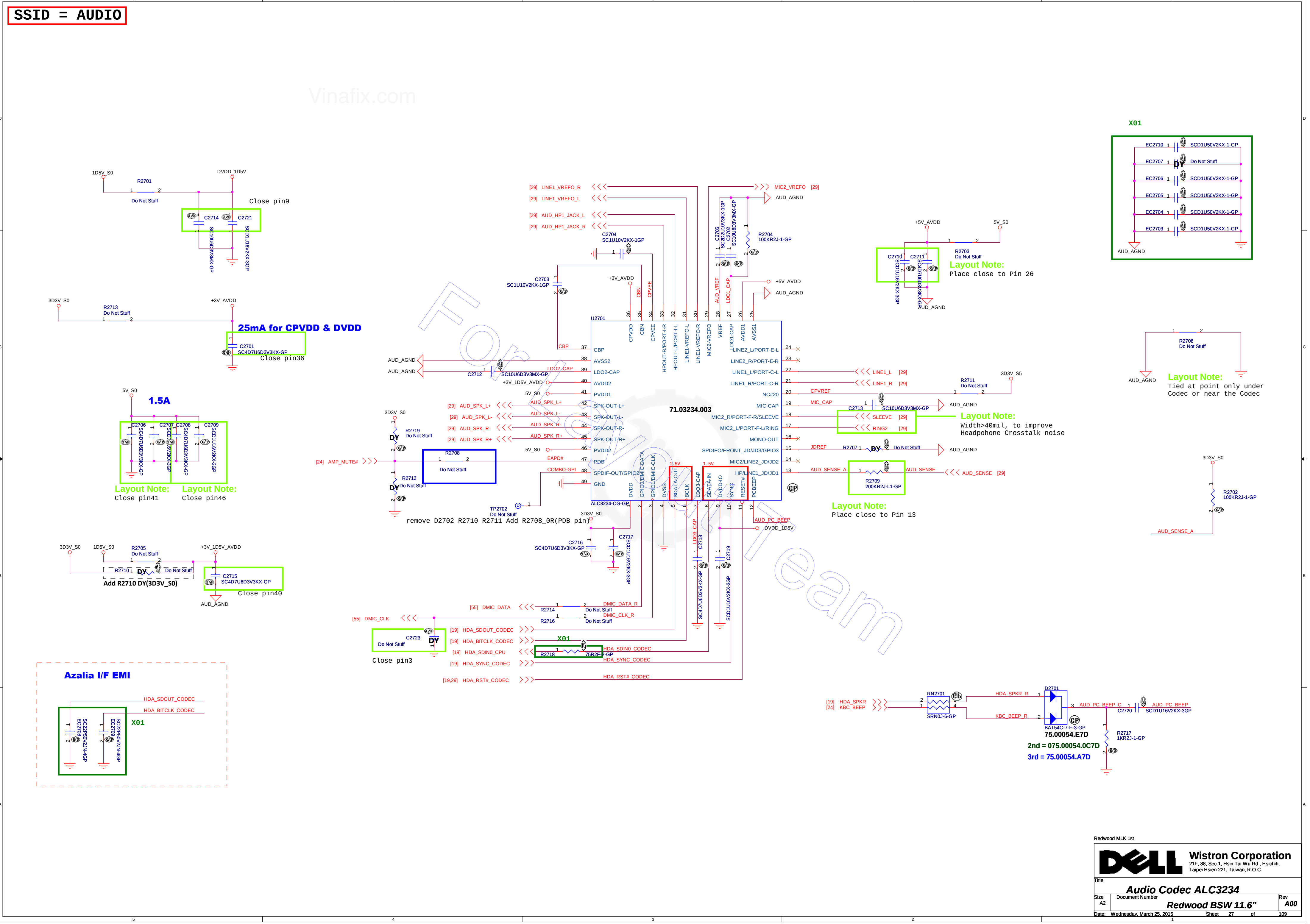

SSID = AUDIO
X01
EC2710 SCD1U50V2KX-1-GP
EC2707 DY Do Not Stuff
EC2706 SCD1U50V2KX-1-GP
EC2705 SCD1U50V2KX-1-GP
EC2704 SCD1U50V2KX-1-GP
EC2703 SCD1U50V2KX-1-GP
AUD_AGND
1D5V_S0
R2701
Do Not Stuff
DVDD_1D5V
Close pin9
C2714 SC10U6D3V3MX-GP
C2721 SCD1U16V2KX-3GP
3D3V_S0
R2713 Do Not Stuff
+3V_AVDD
25mA for CPVDD & DVDD
C2701 SC4D7U6D3V3KX-GP
Close pin36
5V_S0
1.5A
C2706 SC4D7U6D3V3KX-GP
C2707 SCD1U16V2KX-3GP
C2708 SC4D7U6D3V3KX-GP
C2709 SCD1U16V2KX-3GP
Layout Note: Close pin41
Layout Note: Close pin46
R2705 Do Not Stuff
+3V_1D5V_AVDD
R2710 DY Do Not Stuff
Add R2710 DY(3D3V_S0)
C2715 SC4D7U6D3V3KX-GP
Close pin40
Azalia I/F EMI
HDA_SDOUT_CODEC
HDA_BITCLK_CODEC
EC2708 SC22P50V2JN-4GP
EC2709 SC22P50V2JN-4GP
X01
[29] LINE1_VREFO_R
[29] LINE1_VREFO_L
[29] AUD_HP1_JACK_L
[29] AUD_HP1_JACK_R
MIC2_VREFO [29]
AUD_AGND
C2704 SC1U10V2KX-1GP
C2703 SC1U10V2KX-1GP
C2705 SC2D2U10V3KX-1GP
C2702 SC10U6D3V3MX-GP
R2704 100KR2J-1-GP
+5V_AVDD
AUD_VREF
LDO1_CAP
U2701
CPVDD CBN CPVEE HPOUT-R/PORT-I-R HPOUT-L/PORT-I-L LINE1-VREFO-L LINE1-VREFO-R MIC2-VREFO VREF LDO1-CAP AVDD1 AVSS1
CBP AVSS2 LDO2-CAP AVDD2 PVDD1 SPK-OUT-L+ SPK-OUT-L- SPK-OUT-R- SPK-OUT-R+ PVDD2 PDB SPDIF-OUT/GPIO2 GND
LINE2_L/PORT-E-L LINE2_R/PORT-E-R LINE1_L/PORT-C-L LINE1_R/PORT-C-R NC#20 MIC-CAP MIC2_R/PORT-F-R/SLEEVE MIC2_L/PORT-F-L/RING MONO-OUT SPDIFO/FRONT_JD/JD3/GPIO3 MIC2/LINE2_JD/JD2 HP/LINE1_JD/JD1
DVDD GPIO0/DMIC-DATA GPIO1/DMIC-CLK DVSS SDATA-OUT BCLK LDO3-CAP SDATA-IN DVDD-IO SYNC RESET# PCBEEP
ALC3234-CG-GP
71.03234.003
AUD_AGND
C2712 SC10U6D3V3MX-GP
LDO2_CAP
+3V_1D5V_AVDD
[29] AUD_SPK_L+
[29] AUD_SPK_L-
[29] AUD_SPK_R-
[29] AUD_SPK_R+
3D3V_S0
R2719 Do Not Stuff
DY
[24] AMP_MUTE#
R2708 Do Not Stuff
EAPD#
COMBO-GPI
R2712 Do Not Stuff
TP2702 Do Not Stuff
remove D2702 R2710 R2711 Add R2708_0R(PDB pin)
LINE1_L [29]
LINE1_R [29]
CPVREF
MIC_CAP
C2713 SC10U6D3V3MX-GP
SLEEVE [29]
RING2 [29]
Layout Note: Width>40mil, to improve Headphone Crosstalk noise
JDREF
R2707 DY Do Not Stuff
AUD_SENSE_A
R2709 200KR2J-L1-GP
AUD_SENSE [29]
Layout Note: Place close to Pin 13
+5V_AVDD
5V_S0
R2703 Do Not Stuff
C2710 SCD1U16V2KX-3GP
C2711 SC4D7U6D3V3KX-GP
Layout Note: Place close to Pin 26
R2706 Do Not Stuff
Layout Note: Tied at point only under Codec or near the Codec
R2711 Do Not Stuff
3D3V_S5
R2702 100KR2J-1-GP
AUD_SENSE_A
AUD_PC_BEEP
DVDD_1D5V
C2716 SC4D7U6D3V3KX-GP
C2717 SCD1U16V2KX-3GP
C2718 SC4D7U6D3V3KX-GP
C2719 SCD1U16V2KX-3GP
[55] DMIC_DATA
R2714 Do Not Stuff
DMIC_DATA_R
[55] DMIC_CLK
R2716 Do Not Stuff
DMIC_CLK_R
C2723 DY Do Not Stuff
Close pin3
[19] HDA_SDOUT_CODEC
[19] HDA_BITCLK_CODEC
[19] HDA_SDIN0_CPU
[19] HDA_SYNC_CODEC
[19,29] HDA_RST#_CODEC
X01
R2718 75R2F-2-GP
HDA_SDIN0_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
[19] HDA_SPKR
[24] KBC_BEEP
RN2701 SRN0J-6-GP
HDA_SPKR_R
KBC_BEEP_R
D2701 BAT54C-7-F-3-GP
75.00054.E7D
2nd = 075.00054.0C7D
3rd = 75.00054.A7D
AUD_PC_BEEP_C
C2720 SCD1U16V2KX-3GP
AUD_PC_BEEP
R2717 1KR2J-1-GP
Redwood MLK 1st
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec ALC3234
Size A2
Document Number
Redwood BSW 11.6"
Rev A00
Date: Wednesday, March 25, 2015
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Blanking

Redwood MLK 1st

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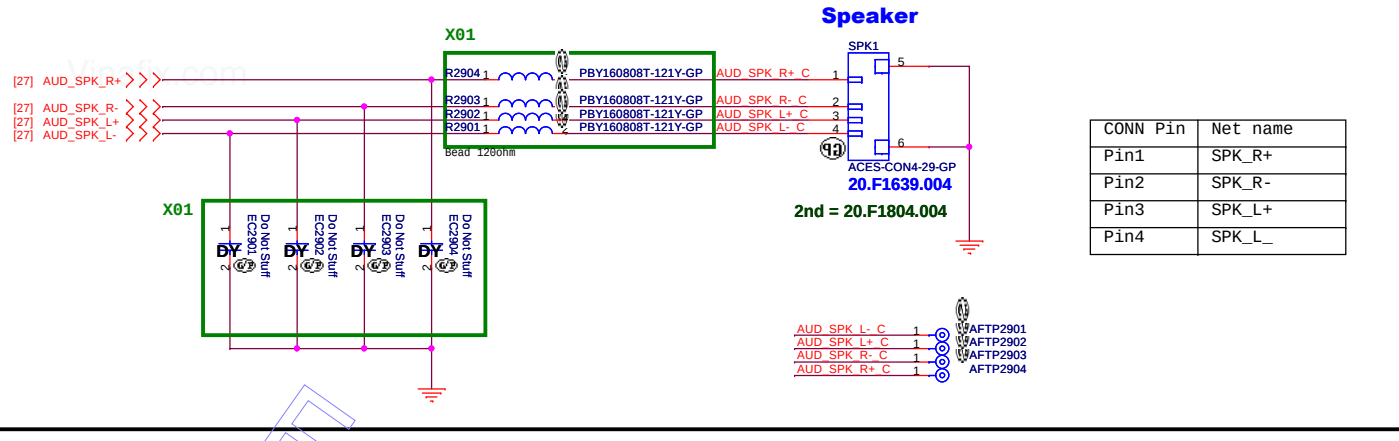
Title

(Reserved)

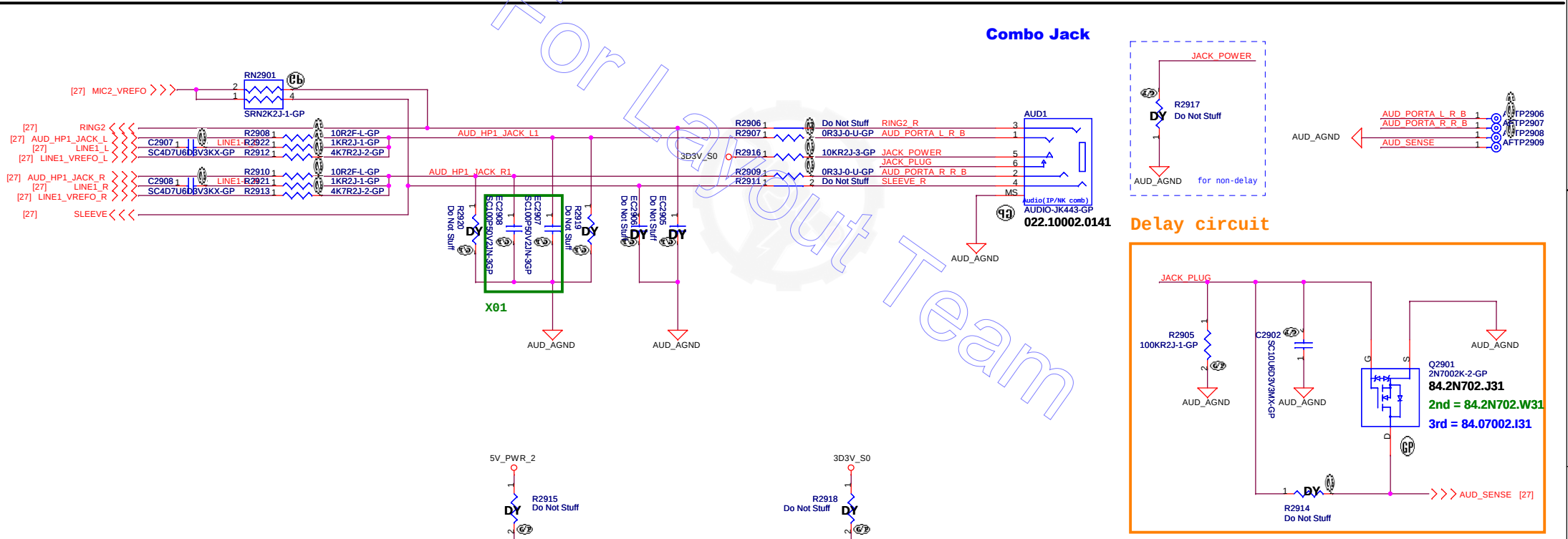
Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

Date: Thursday, March 19, 2015 Sheet 28 of 109

SSID = AUDIO



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_



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Title: Speaker/HPMIC CONN

Size	Document Number	Rev
A3	Redwood BSW 11.6"	A00

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SSID = LOM

Blanking

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Title: *(Reserved)LOM*		
Size: A4	Document Number: *Redwood BSW 11.6"*	Rev: *A00*
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SSID = LAN

Blanking

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Title	*(Reserved)LAN*	
Size: A4	Document Number: Redwood BSW 11.6"	Rev: A00
Date: Thursday, March 19, 2015	Sheet 31 of 109	

SSID = LAN CONN

Blanking

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Title: *(Reserved)RJ45+Transformer*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

Date: Thursday, March 19, 2015 Sheet 32 of 109

SSID = Card Reader

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Title: (Reserved)Card Reader + CONN

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

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SSID = USB

Blanking

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Title: *(Reserved)USB 2.0 Port*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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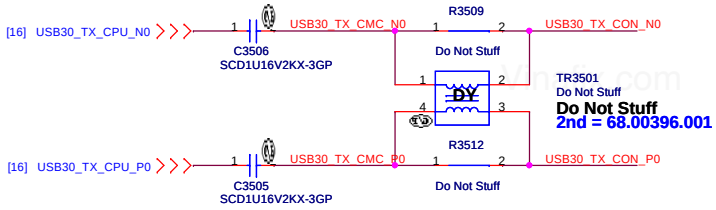
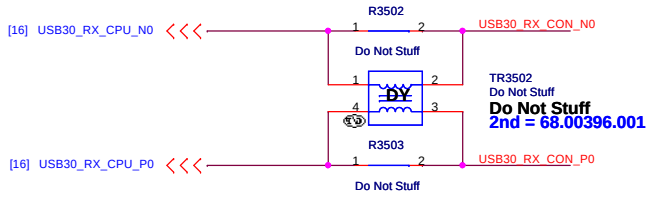
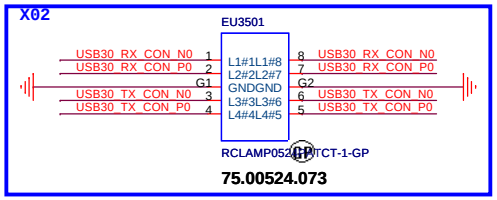
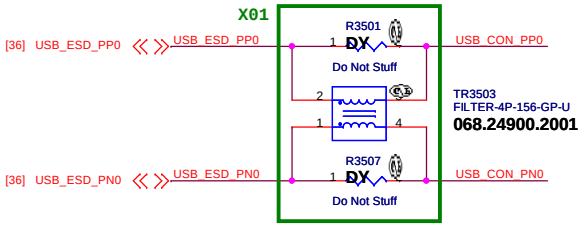
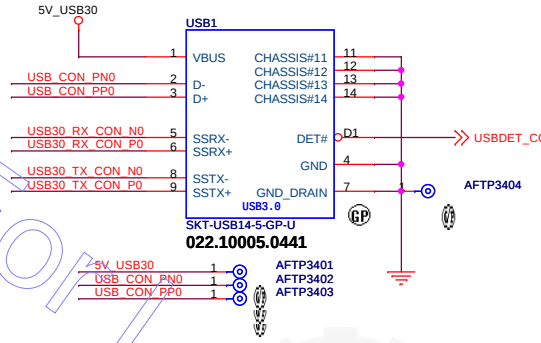
SSID = USB

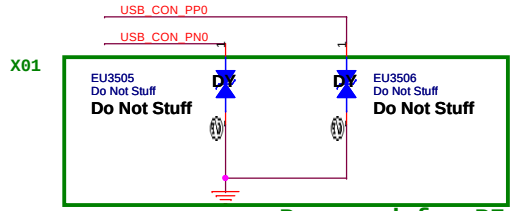




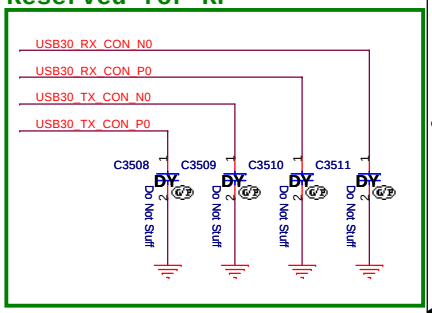




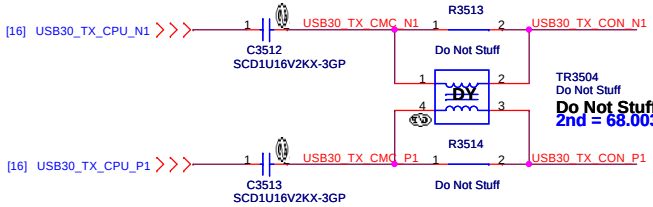


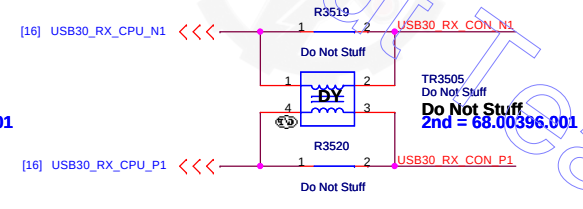


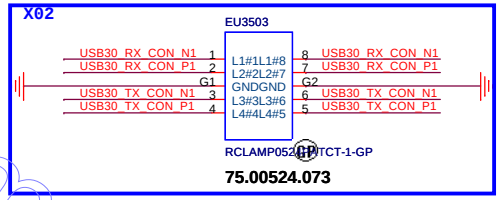
USB 3.0 Connector Pin definition		
1	*POWER*	
2	*USB 2.0 D-*	
3	*USB 2.0 D+*	
4	*GND*	
5	*StdA_SSRX-*	*SuperSpeed RX*
6	*StdA_SSRX+*	
7	*GND*	
8	*StdA_SSTX-*	*SuperSpeed TX*
9	*StdA_SSTX+*	

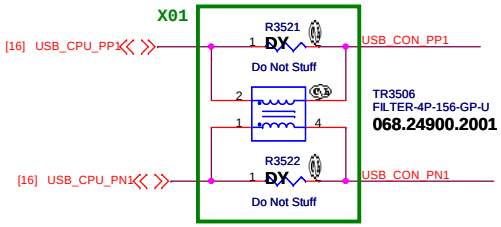


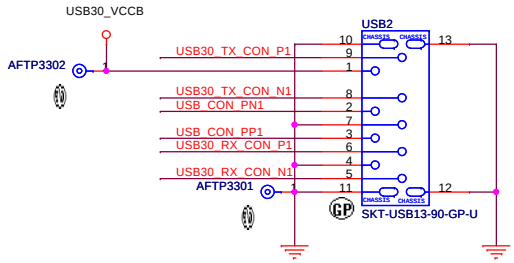
USB3.0 Port2

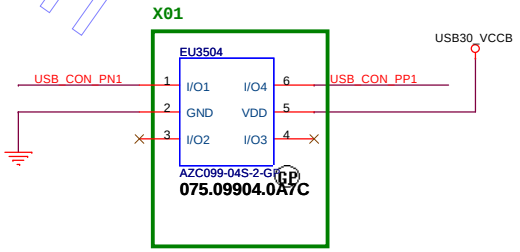


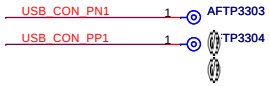












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Title: *USB3.0 CONN*

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	Redwood BSW 11.6"	*A00*

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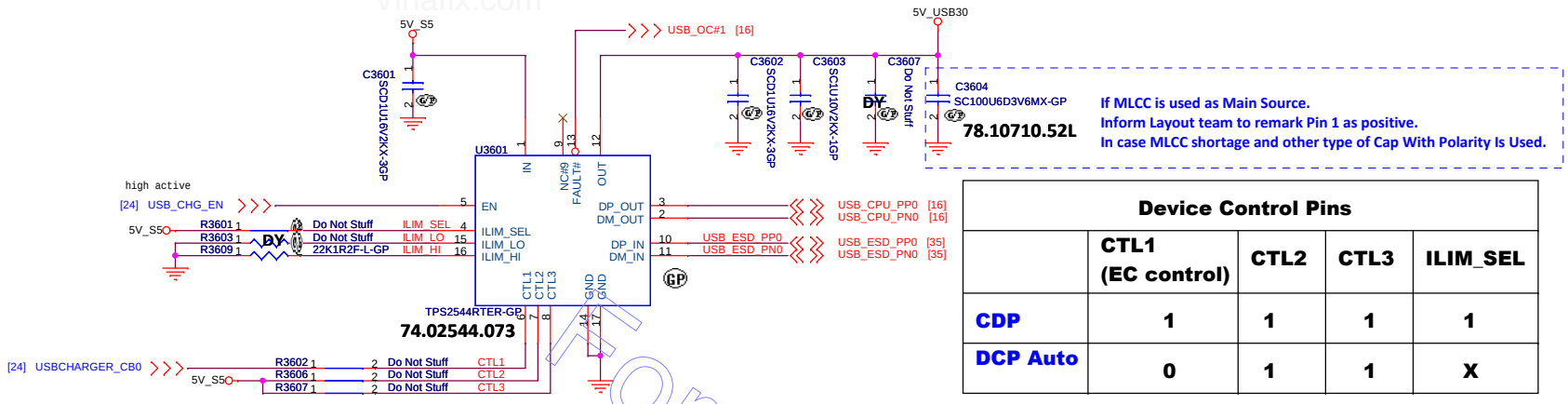
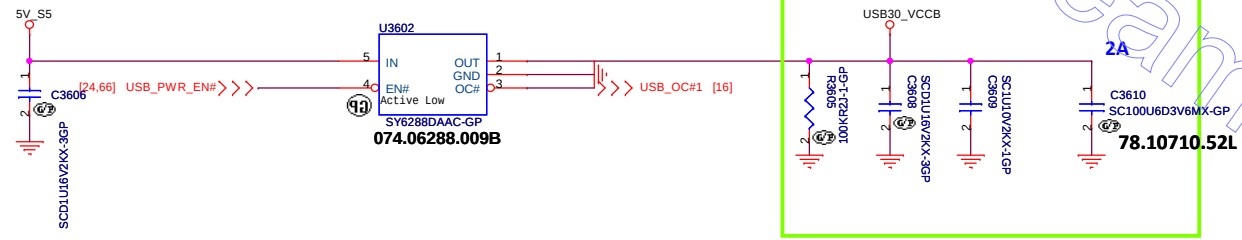
USB Charger Port1



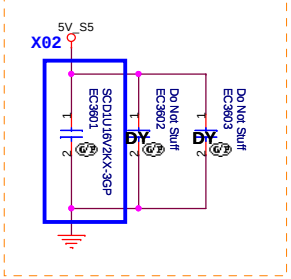
Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

USB3.0 Port2

Layout Note: Close CON1



Reserved For Antenna



Redwood MLK 1st

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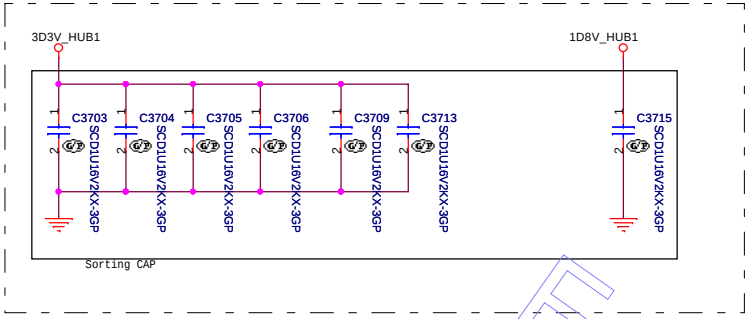
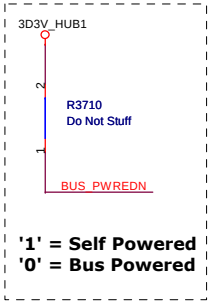
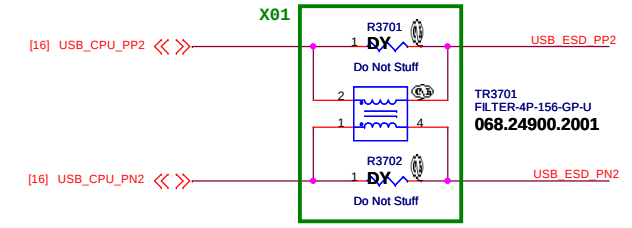
Title	USB Power SW	
Size A3	Document Number: Redwood BSW 11.6"	Rev A00
Date: Wednesday, March 25, 2015	Sheet 36 of 109	

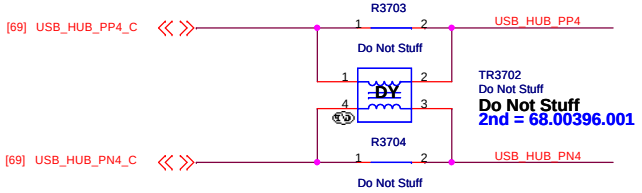
SSID = USB



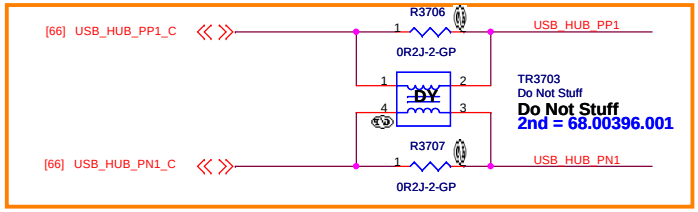
Near the chip side.

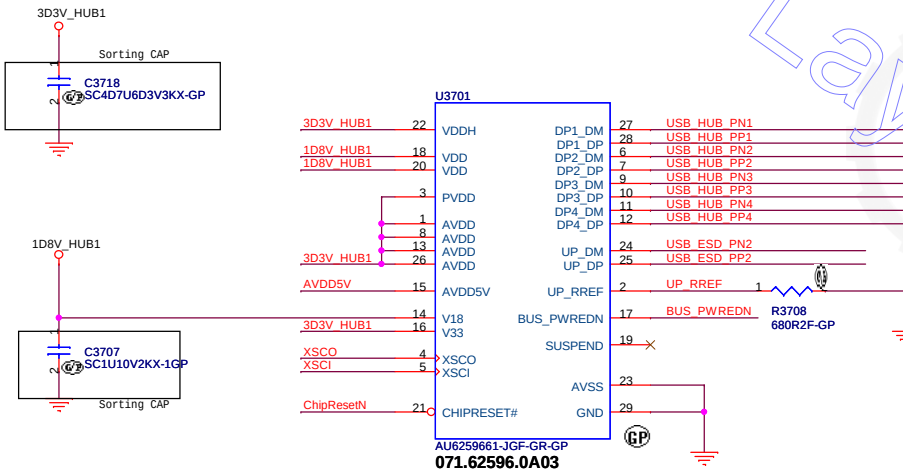






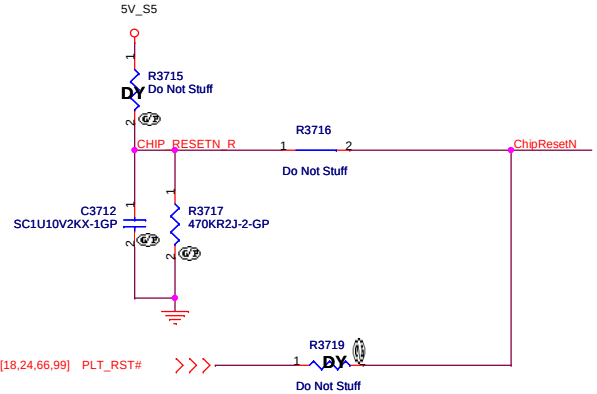
A00 Layout Note: Need Close CONN IOBD1

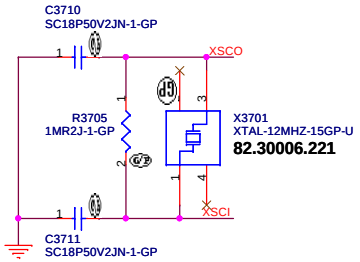


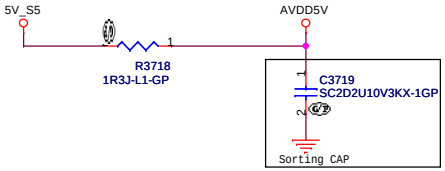


From CPU

USB2.0 Port3
Card Reader
Bluetooth
Sensor Hub







USB Table

Pair	Device
1	USB2.0 Port3
2	Card Reader
3	Bluetooth
4	Sensor Hub

Redwood MLK 1st

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Title: USB2.0 HUB

Size: A3 | Document Number: Redwood BSW 11.6" | Rev: A00

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Blanking

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Title

(Reserved)

Size	Document Number	Rev
A4	**Redwood BSW 11.6"**	A00

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Redwood MLK 1st

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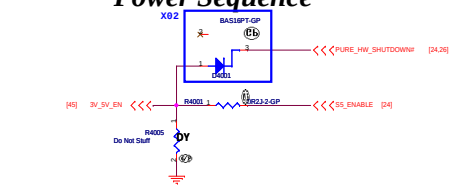
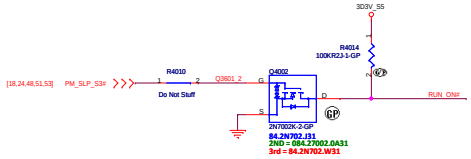
Title: *(Reserved)*		
Size: A4	Document Number: *Redwood BSW 11.6"*	Rev: *A00*
Date: Thursday, March 19, 2015	Sheet 39 of 109	

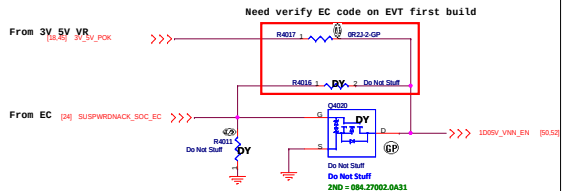
SSID = Reset.Suspend

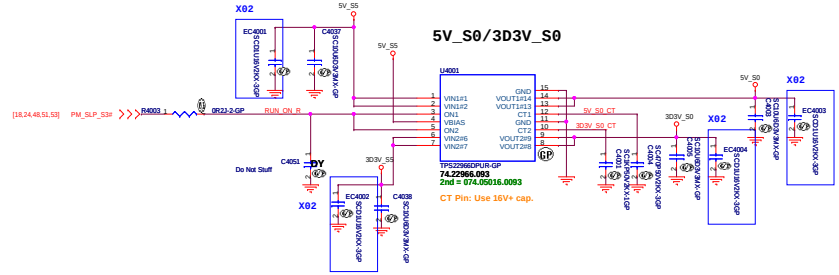
Power Sequence

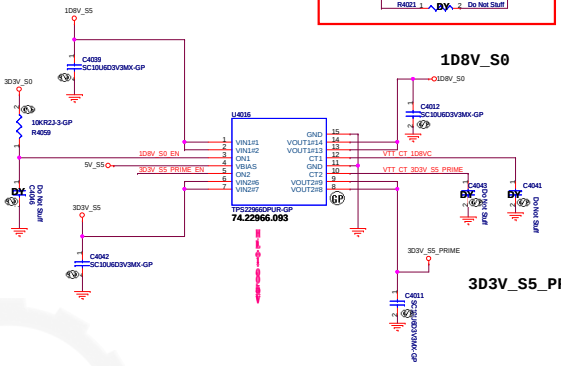


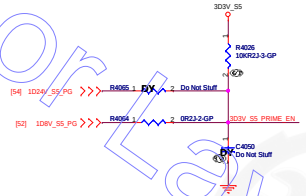


Need verify EC code on EVT first build

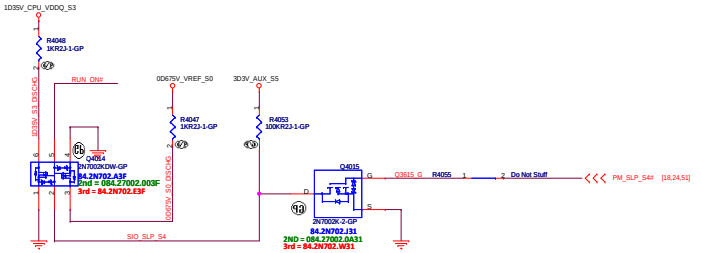


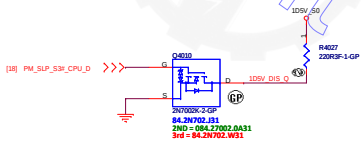


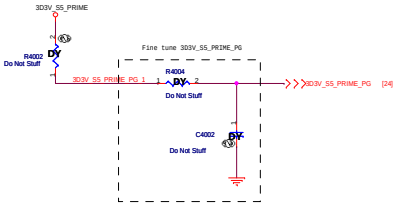




Discharge circuit

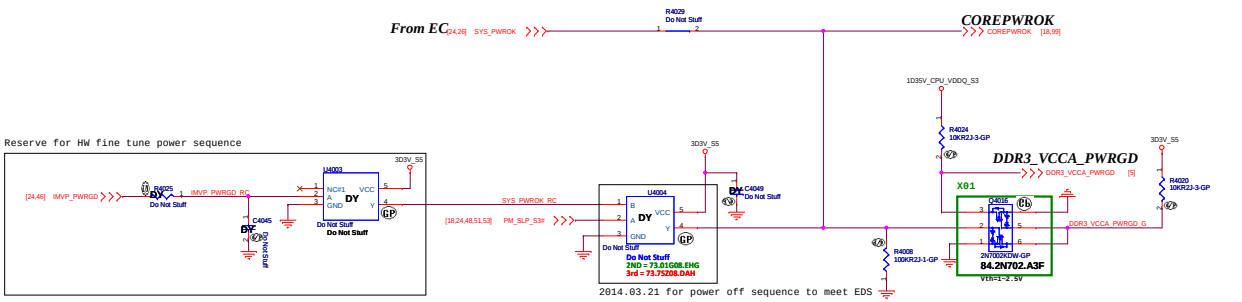




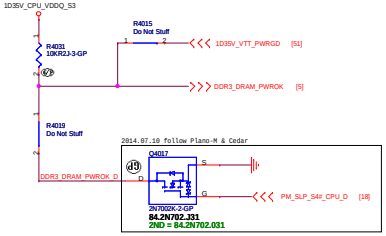


Power Sequence

DDR3_VCCA_PWRGD



DDR3_DRAM_PWROK



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Title: Power Plane Enable

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Custom	Redwood BSW 11.6"	A00

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SSID = PWR.Support

X02

EC4303
SCD1U25V2KX-GP

PD4302
Do Not Stuff

Batt Connecter

X01

BATT1

DEREN-CON8-GP
20.82003.008

AFTP4305

RN4301

SRN100J-4-GP

[24,44] BAT_SCL
[24,44] BAT_SDA
[24] BAT_IN#

PBAT_SMBCLK1
PBAT_SMBDAT1
PBAT_PRES1#
SYS_PRES1#

EC4301 Do Not Stuff
EC4302 Do Not Stuff
EC4305 Do Not Stuff

PBAT_PRES1#
PBAT_SMBDAT1
PBAT_SMBCLK1
12V_BT+

AFTP4301
AFTP4302
AFTP4303
AFTP4304

R4301
Do Not Stuff

SYS_PRES1#

Placement: Close to Batt Connector

D4302 Do Not Stuff
D4303 Do Not Stuff
D4301 Do Not Stuff

3D3V_AUX_KBC

Do Not Stuff	Do Not Stuff	Do Not Stuff
2nd = 83.00099.K11	2nd = 83.00099.K11	2nd = 83.00099.K11
3rd = 83.00099.M11	3rd = 83.00099.M11	3rd = 83.00099.M11

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil

5V_S5

84.T3904.H11

PR4302 15KR2F-GP
PQ4302 LMBT3904LT1G-GP
PR4303 10KR2J-3-GP
PR4311 100KR2J-1-GP
PQ4301 FDV301N-NL-GP
84.00301.A31
2nd = 84.3K329.031
3rd = 84.27002.131

PS_ID_R
PS_ID
PR4307 33R2J-2-GP

3D3V_S5
PD4303 DA3X101F0L-1-GP
PR4306 2K2R2J-2-GP
PSID_EC [24]

DCIN1
ACES-CON6-20-GP-U
20.F1639.006
2nd = 20.F1804.006

AFTP4203

+DC_IN_C
EC4304 Do Not Stuff
10/13 EMC add

EMI reqiurement

EL4301 Do Not Stuff
EL4303 Do Not Stuff

PR4316 3K3R6J-GP
PQ4209_D
PQ4309 2N7002K-2-GP
3rd = 84.07002.I31
2nd = 84.2N702.W31
84.2N702.J31

PR4312 1KR2J-1-GP
[24] PWR_CHG_AD_OFF
PWR_CHG_AD_OFF_R

PD4301 1SMB22AT3G-GP-U1
83.22R03.03G
2nd = 83.P6SBM.DAG

PQ4304 PDTC124EU-GP
84.00124.H1K
2nd = 84.05124.011

AD_OFF_L
AD_OFF_R

PQ4305 PDTA124EU-1-GP
84.00124.K1K
2nd = 84.05124.A11

+DC_IN

PR4309 47KR3J-GP
PR4310 47KR3J-L-GP

BJ4301 SI7121DN-T1-GP

19V_AD+

EMI reqiurement

AFTP4201
AFTP4202

+DC_IN
PS_ID_R

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Title: BATTERY CONN

Size: A2
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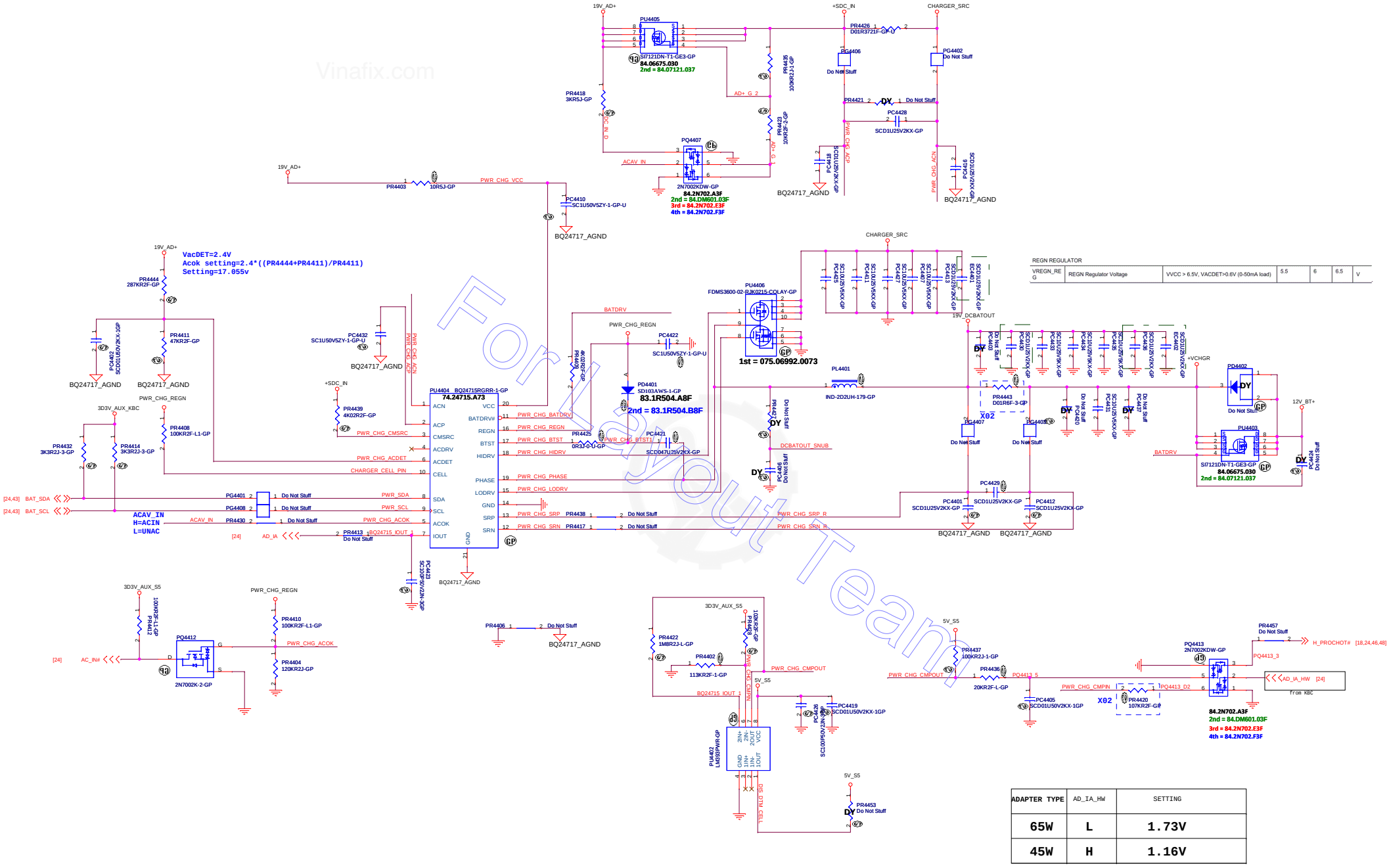
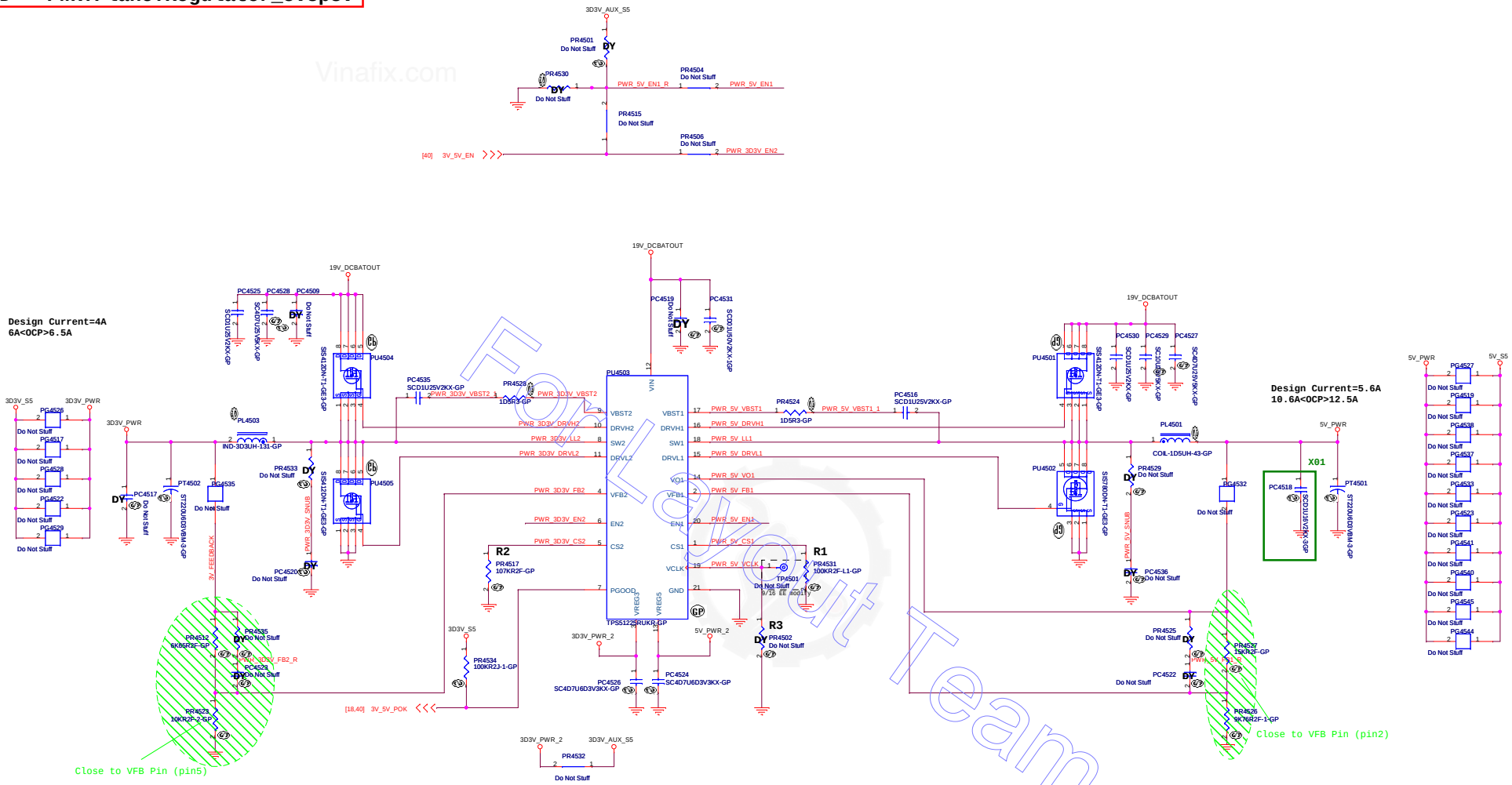
SSID = Charger



SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 4.7UH PCMB063T-4R7MS Cyntec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	107K	21.5K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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Title: *TPS51225 5V/3D3V*

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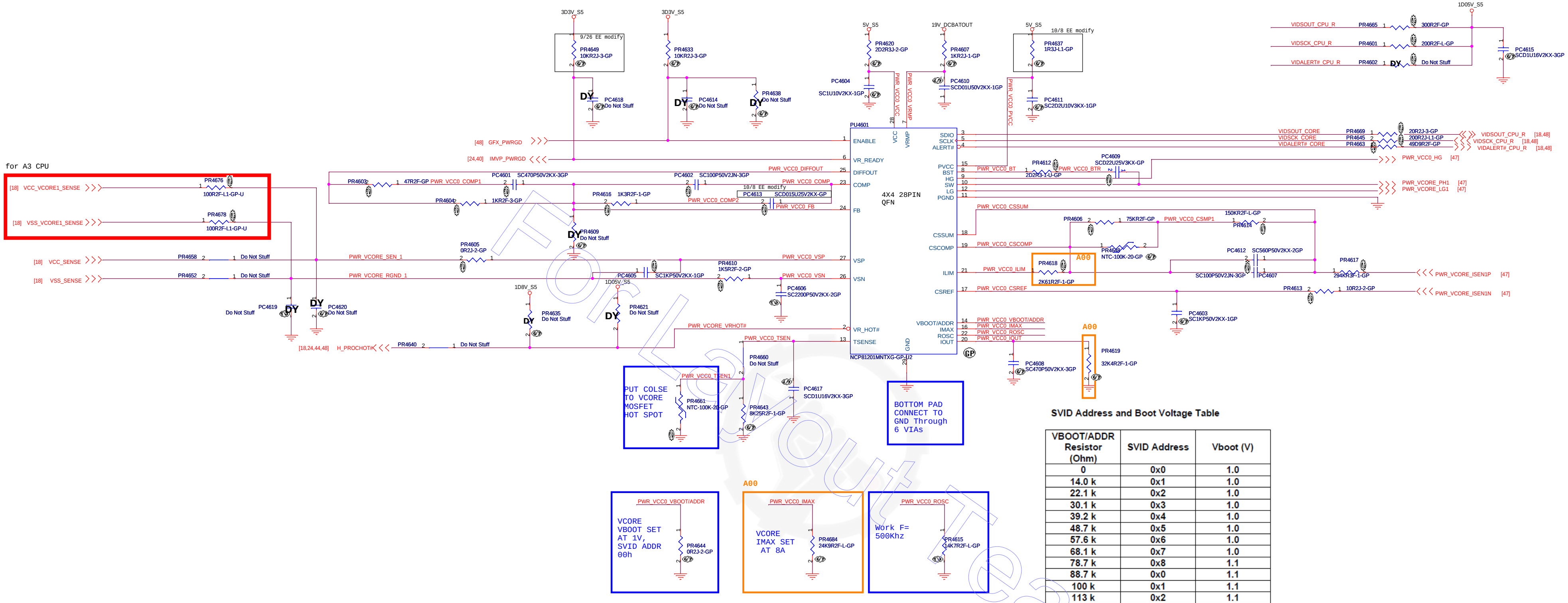
SSID = CPU Regulator



SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	SVID Address	Vboot (V)
0	0x0	1.0
14.0 k	0x1	1.0
22.1 k	0x2	1.0
30.1 k	0x3	1.0
39.2 k	0x4	1.0
48.7 k	0x5	1.0
57.6 k	0x6	1.0
68.1 k	0x7	1.0
78.7 k	0x8	1.1
88.7 k	0x0	1.1
100 k	0x1	1.1
113 k	0x2	1.1
124 k	0x3	1.1
137 k	0x4	1.1
150 k	0x5	1.1
165 k	0x6	1.1
178 k	0x7	1.1
196 k	0x8	1.1

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Title: NCP81201MNTXG_CPUCORE(1/3)
Size: Custom | Document Number: Redwood BSW 11.6" | Rev: A00
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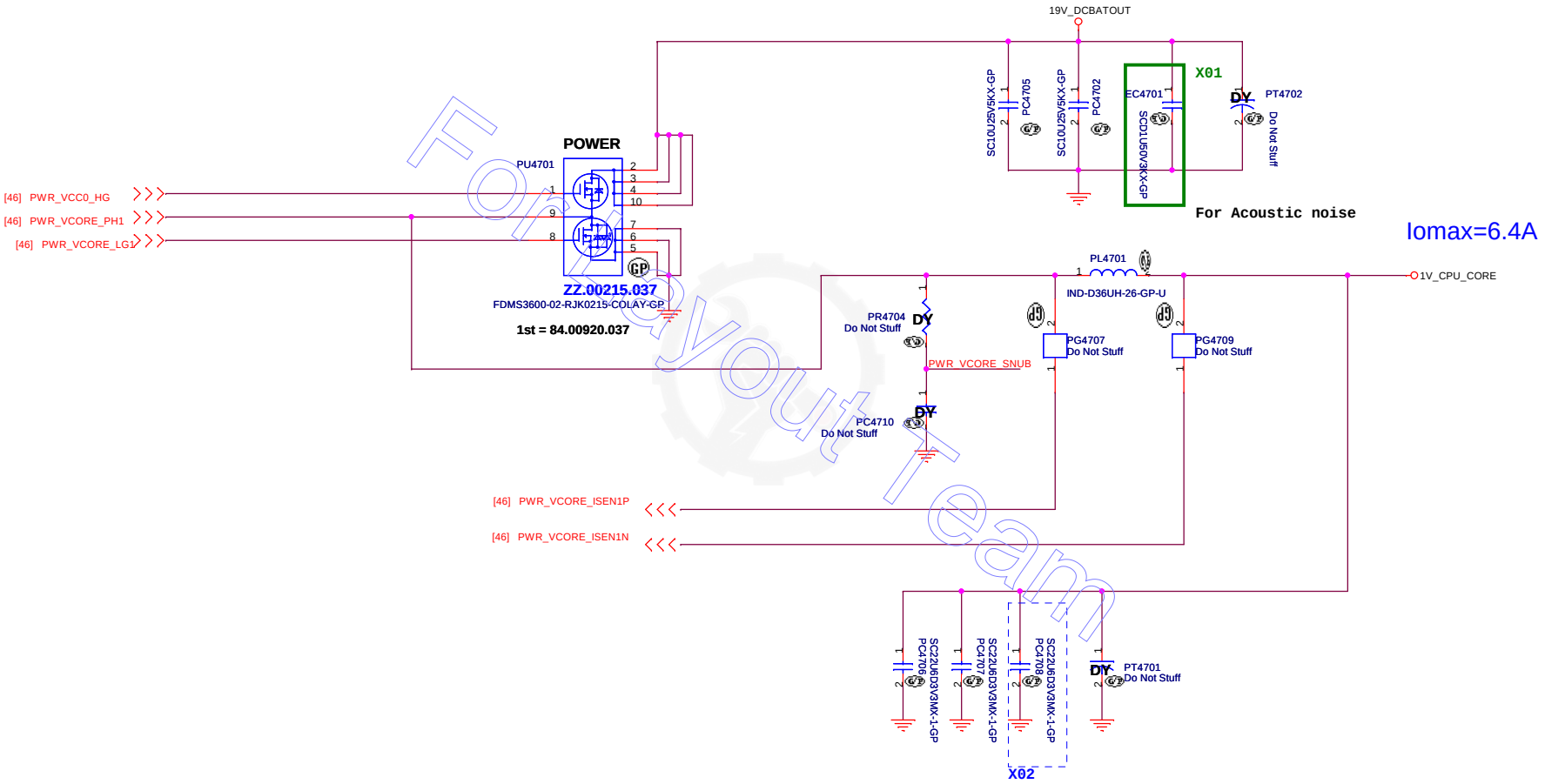
SSID = CPU Regulator



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Title: NCP81201MNTXG CPUCORE(2/3)

Size	Document Number	Rev
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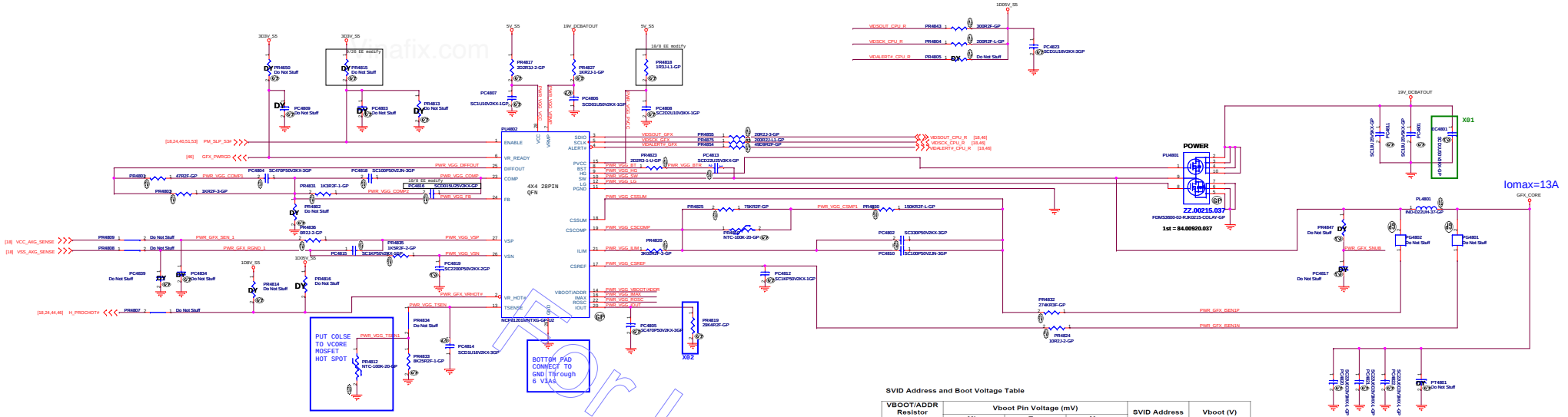
SSID = GFX Regulator



SVID Address and Boot Voltage Table

VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

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File: NCP81201MNTXG_GFXCORE(3/3)

Size: A3 | Document Number: Redwood BSW 11.6" | Rev: A00

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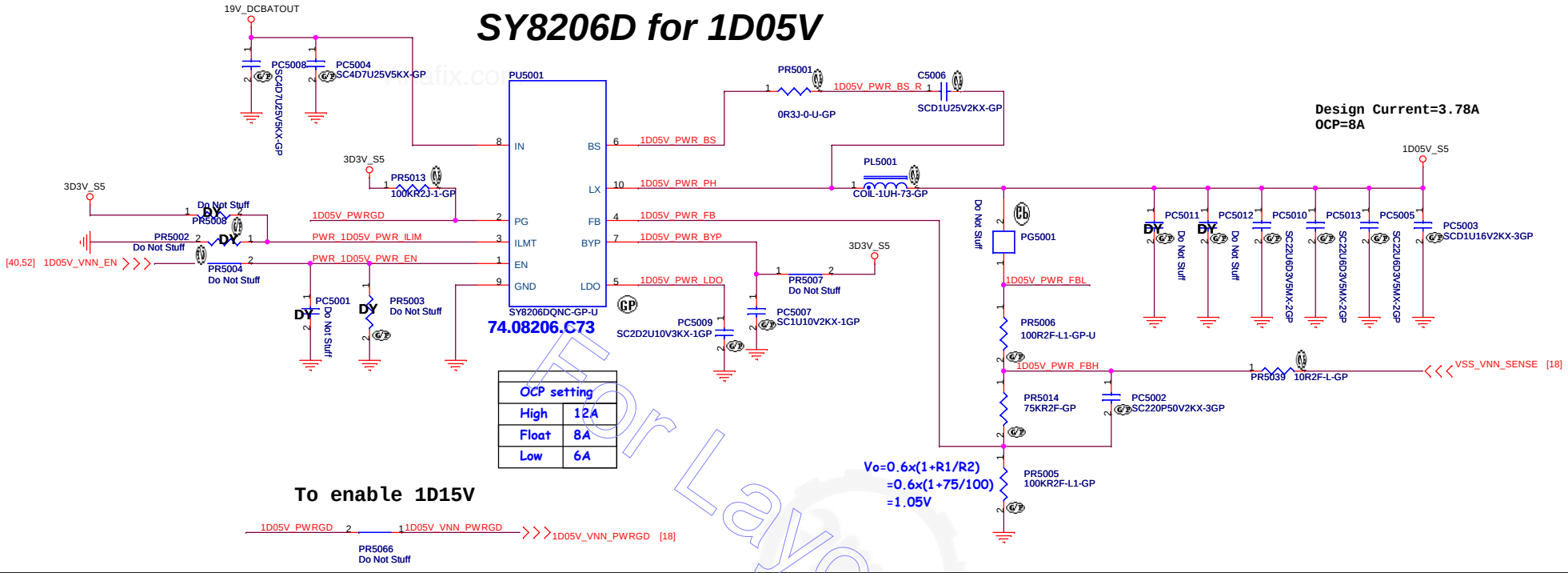
SSID = PWR.Plane.Regulator_1p05v

SY8206D for 1D05V

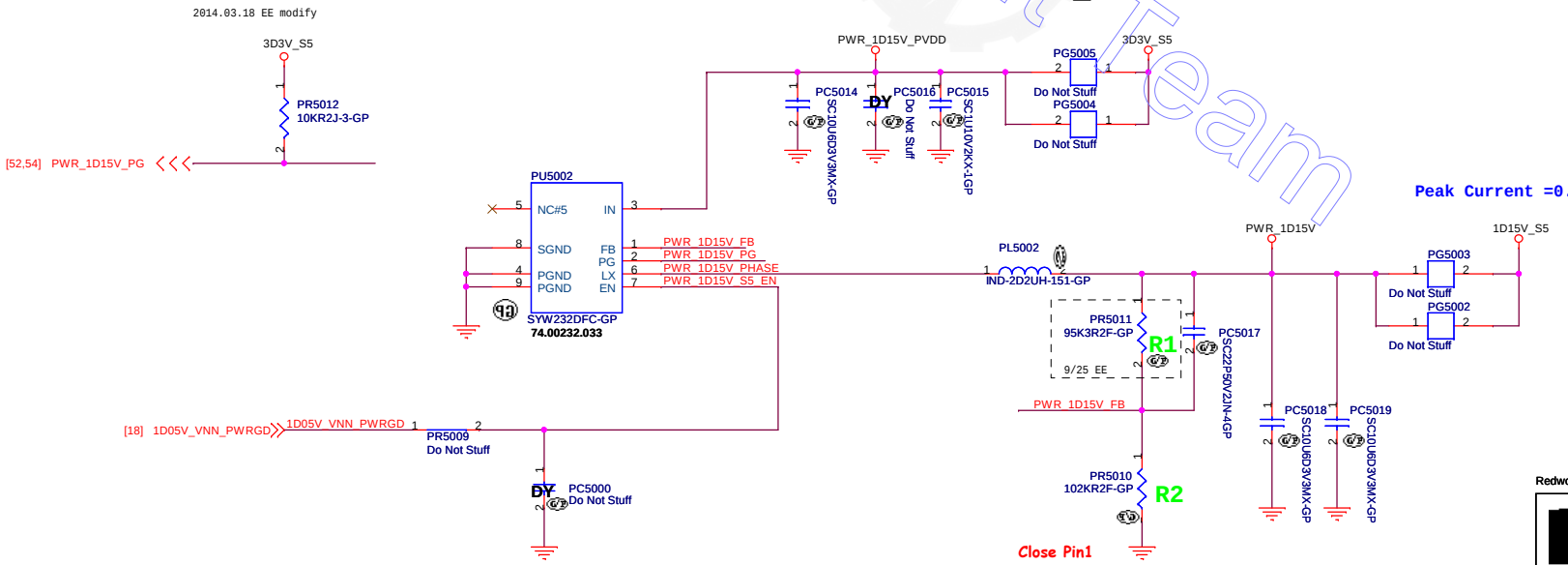


OCP setting	
High	12A
Float	8A
Low	6A

To enable 1D15V

SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D15V_S5



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Title: DCDC_VNN_1D05V_1D15V

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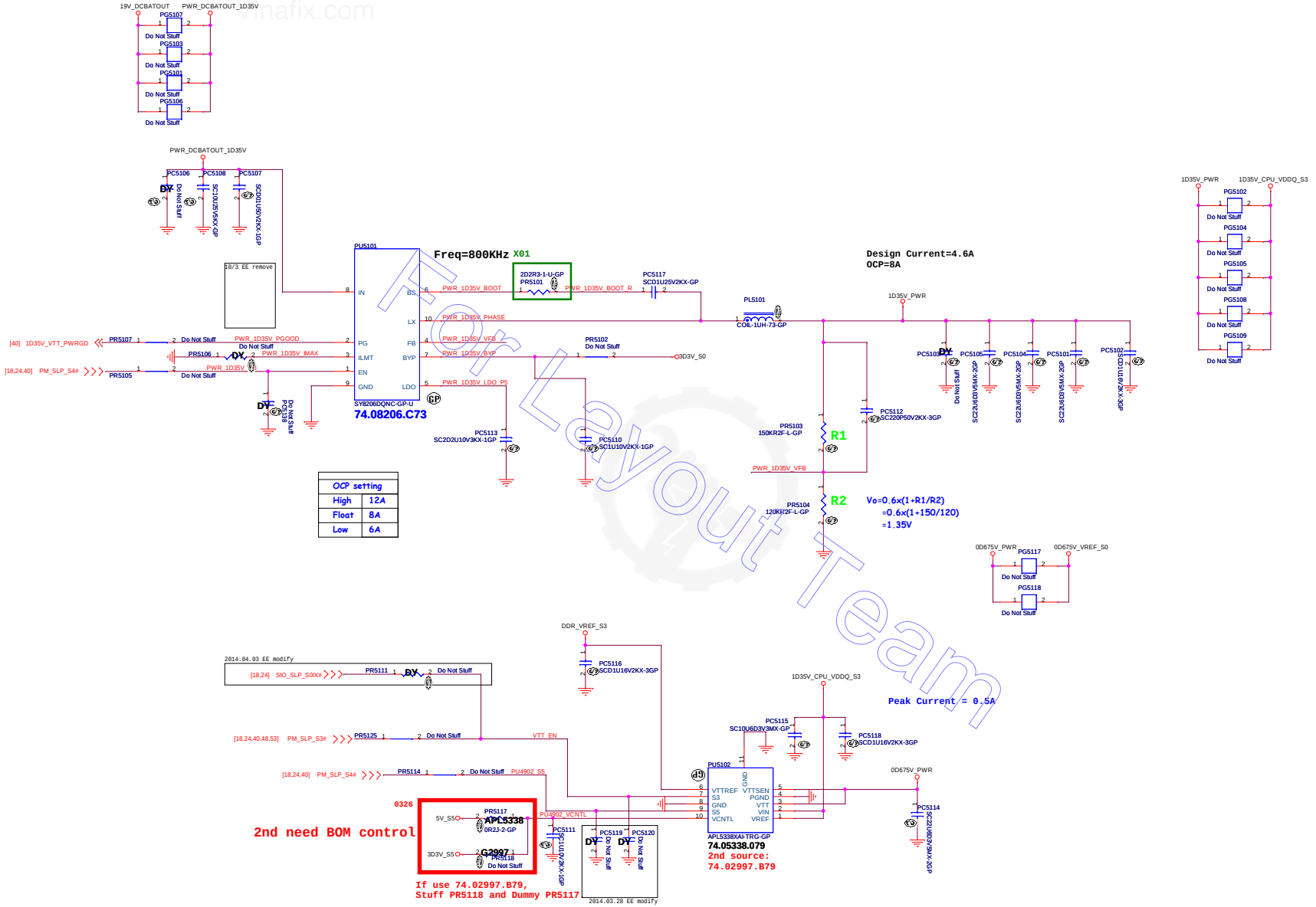
SY8206D for 1D35V



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Title: DC to DC 1D35V(SY8206DQNC)

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A2	Redwood BSW 11.6"	A00

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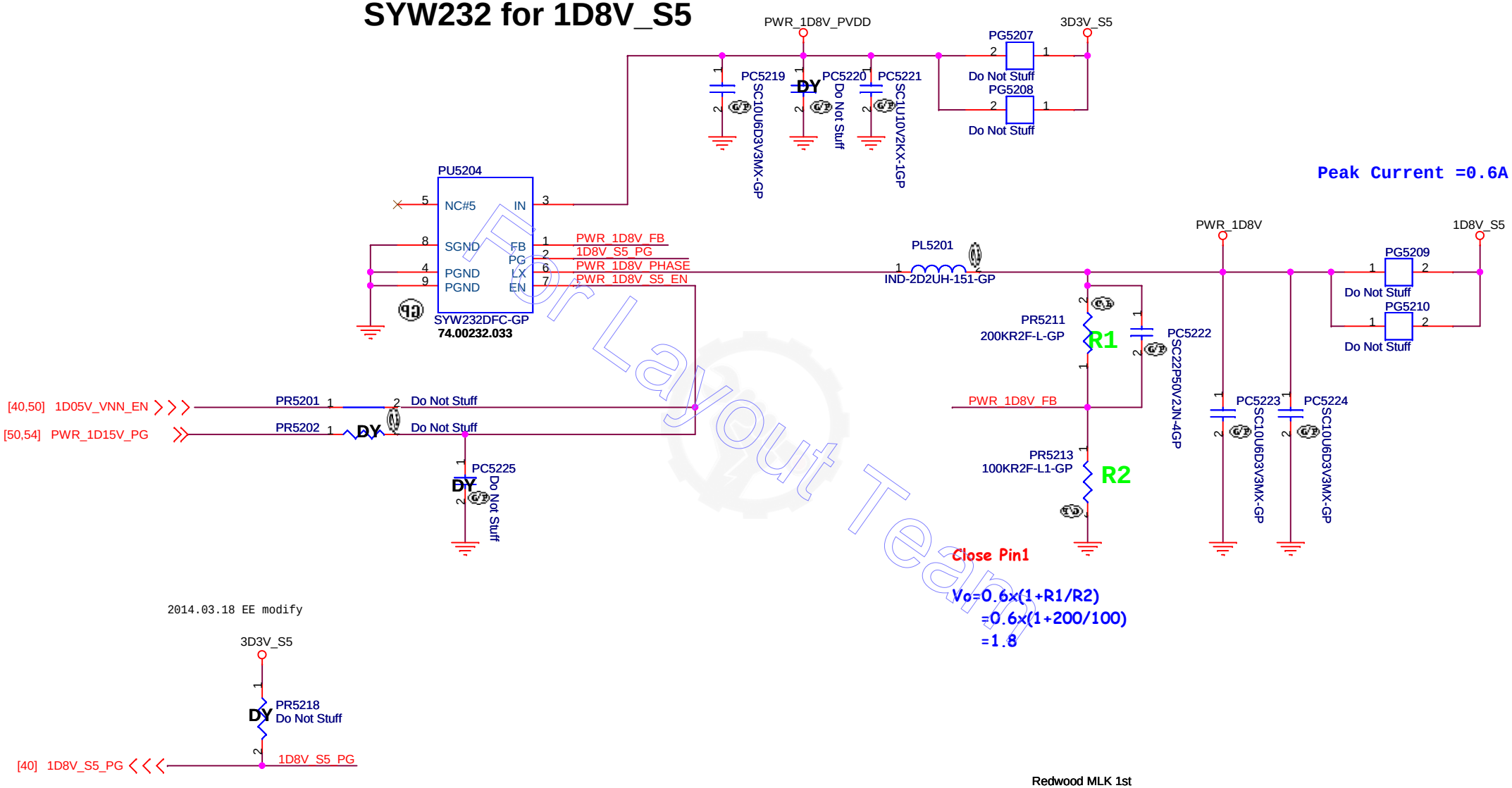
SSID = PWR.Plane.Regulator_1p8v

SYW232 for 1D8V_S5



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Title	SYW232DFC_1D8V	
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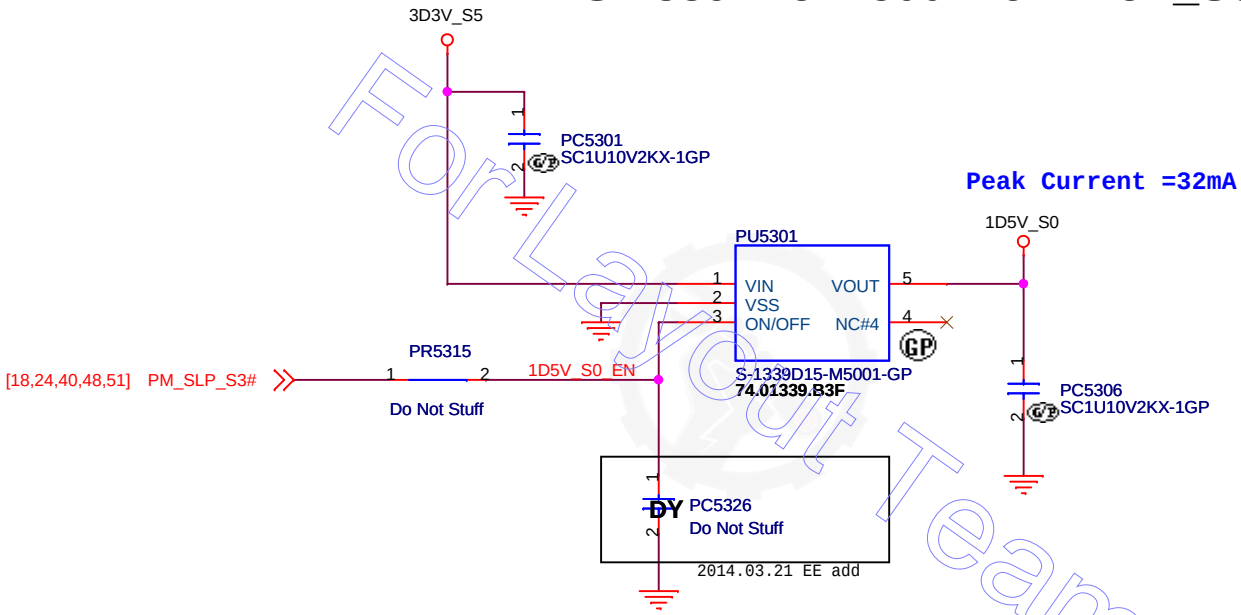
S-1339D15-M5001 for 1D5V_S0



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Title: ***S1339D15_1D5V***

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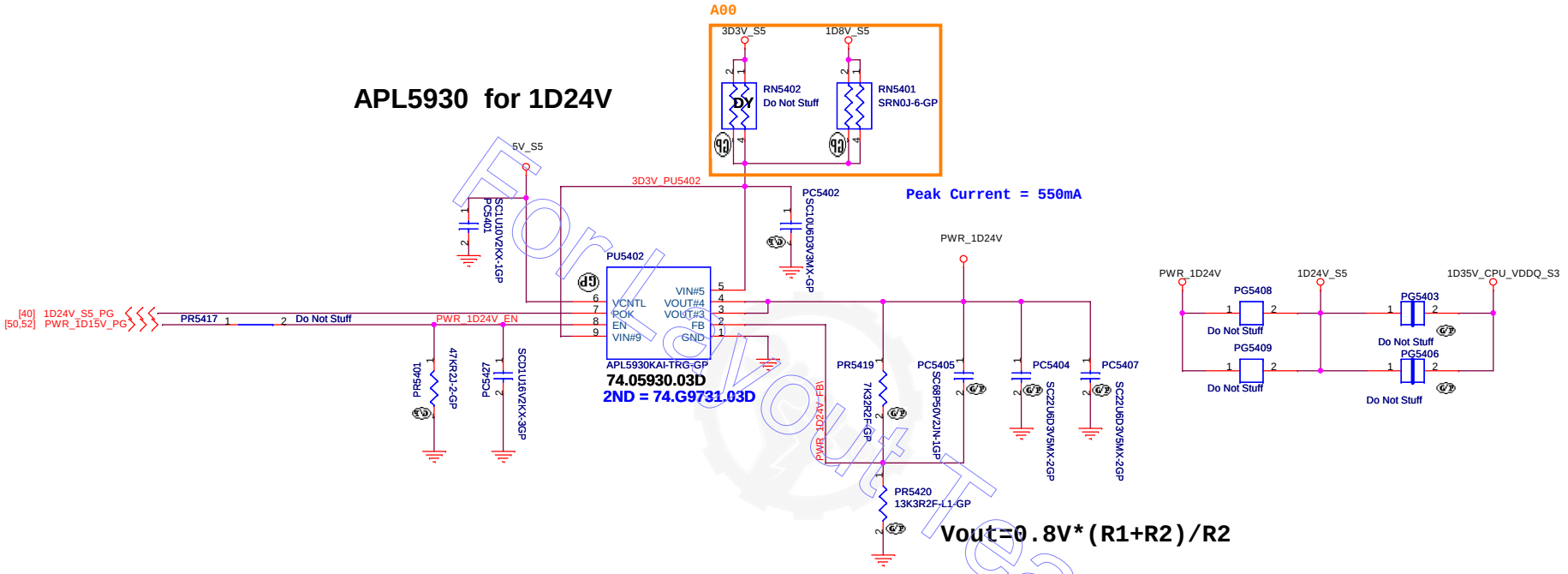
APL5930 for 1D24V



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Title	APL5930_1D24V	
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SSID = VIDEO

Panel Conn.

LCD1 — STAR-CON40-GP — 20.F2248.040

Power Pin Count : 7
GND Pin Count : 9

CAMERA POWER

INVERTER POWER

Level shift

TOUCH PANEL POWER

To Home board

HOMBD1 — PSC-CON16-GP — 020.K0028.0016

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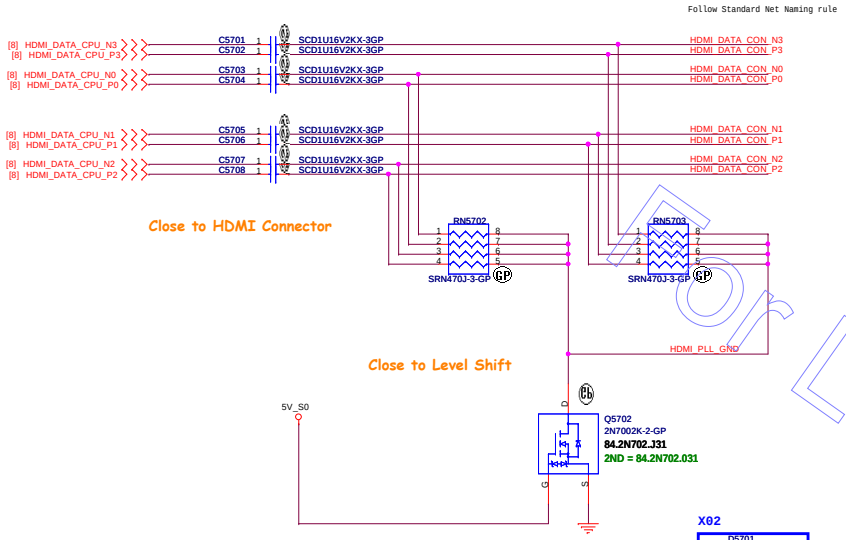
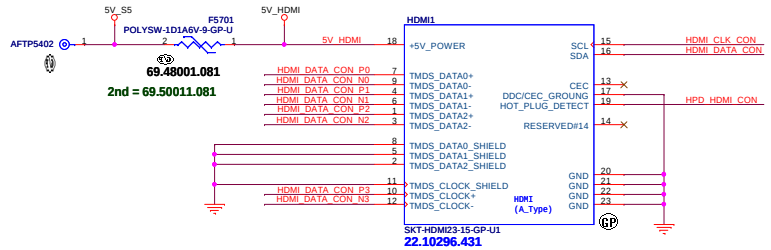
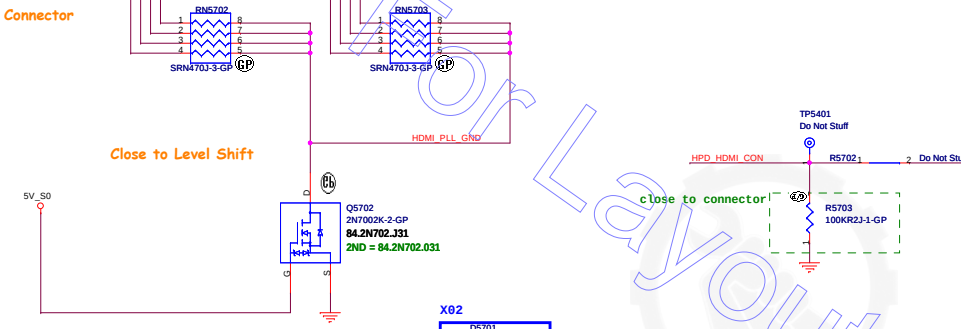
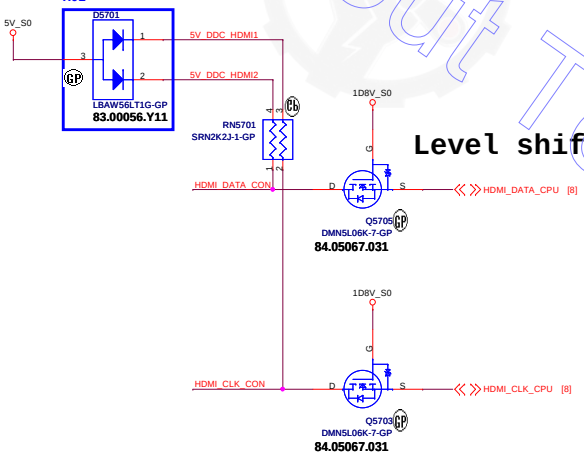
SSID = VIDEO

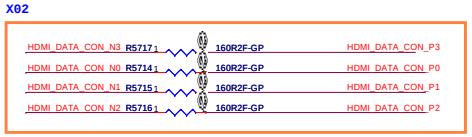
HDMI Level Shifter & CONNECTOR





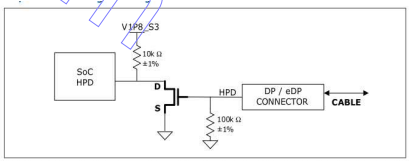






Reseve 150 ohm bridge resistance
on the HDMI trace as circle for EMI

Reseve 0.1uF for ESD



NOTE: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage <=1.5V.
NOTE: The HPD PU resistor tolerance can be relaxed to 5%.

4.2.9 Hot Plug Detect Signal (HPD)

The ground reference for the Hot Plug Detect signal is the DDC/CEC Ground pin.

Table 4-38 Required Output Characteristics of Hot Plug Detect Signal

Item	Value
High voltage level (Sink)	Minimum 2.4 Volts, Maximum 5.3 Volts
Low voltage level (Sink)	Minimum 0 Volts, Maximum 0.4 Volts
Output resistance	1000 ohms ±20%

Table 4-39 Required Detection Levels for Hot Plug Detect Signal

Item	Value
High voltage level (Source)	Minimum 2.0 Volts, Maximum 5.3 Volts
Low voltage level (Source)	Minimum 0 Volts, Maximum 0.8 Volts

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Title: HDMI Level Shifter/Connector

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SSID = Display Port

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Title: *(Reserved) Display Port*

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SSID = DVI

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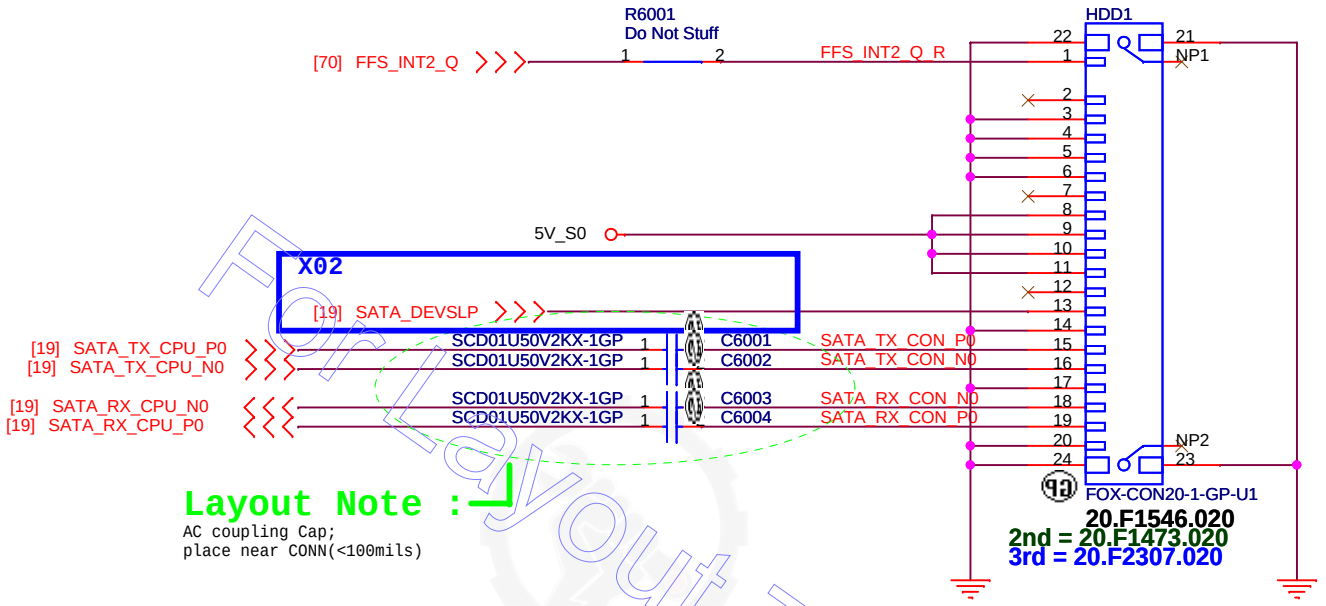
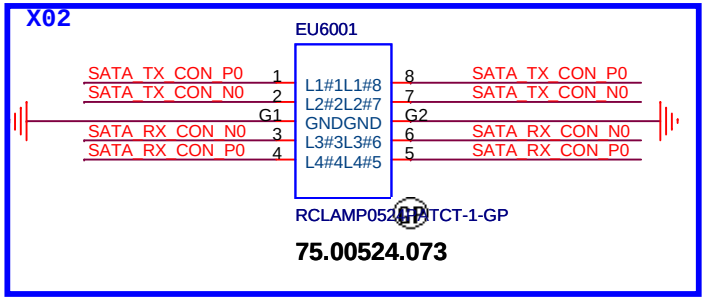
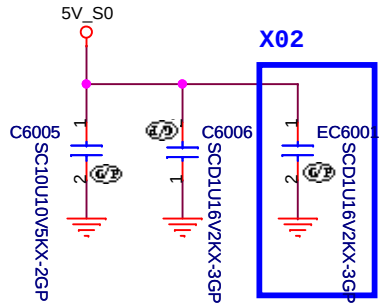
SSID = SATA

SATA HDD Connector







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Title		
HDD		
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SSID = WLAN

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SSID = WWAN

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Title

(Reserved) WWAN

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SSID = SSD-NGFF

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Title: *(Reserved) SSD-NGFF*

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SSID = LED / PWRBTN

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Title	(Reserved) LED / PWRBTN	
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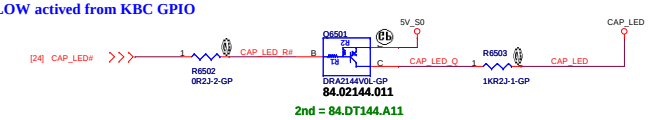
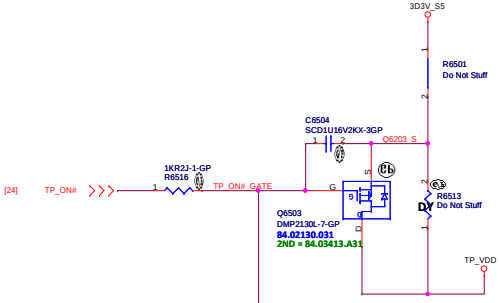
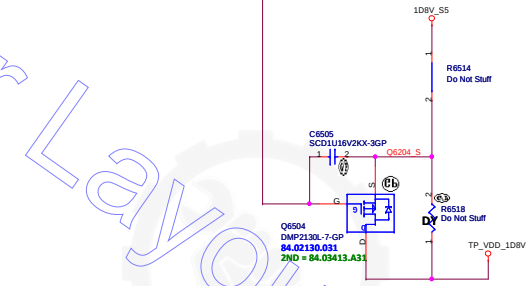
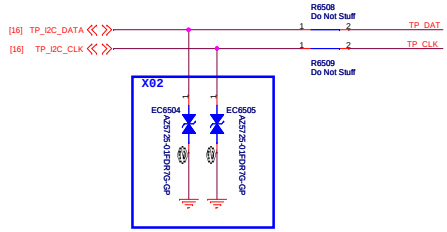
SSID = KB / TOUCH PAD

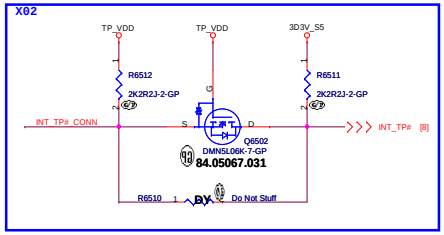
CAP LED Control
LOW actived from KBC GPIO

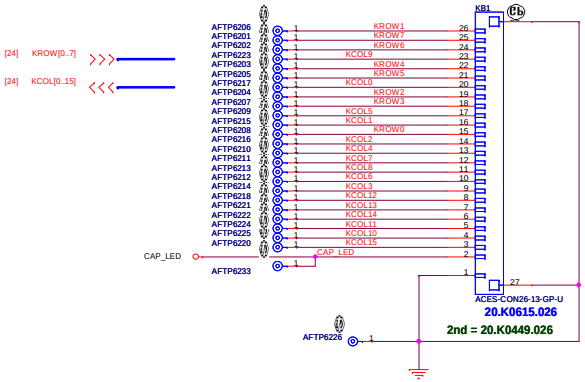




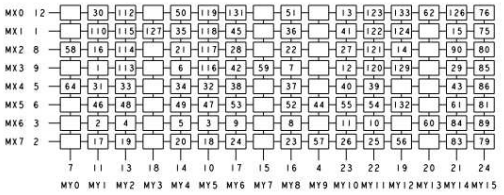


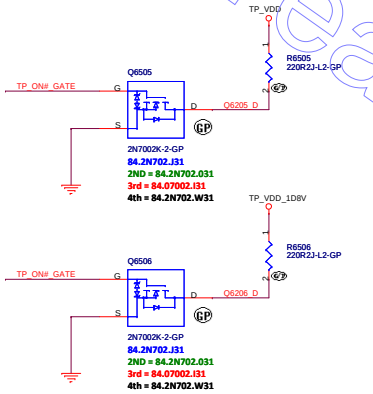


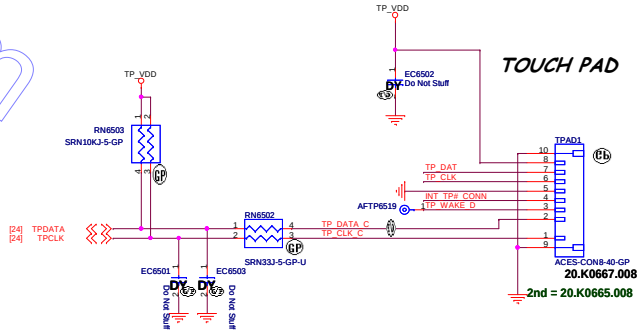


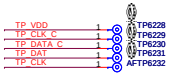


Pin	Signal
1	KSI1
2	KSI7
3	KSI6
4	KSO9
5	KSI4
6	KSI5
7	KSO0
8	KSI2
9	KSI3
10	KSO5
11	KSO1
12	KSI0
13	KSO2
14	KSO4
15	KSO7
16	KSO8
17	KSO6
18	KSO3
19	KSO12
20	KSO13
21	KSO14
22	KSO11
23	KSO10
24	KSO15
25	LED+
26	LED-









Redwood MLK 1st

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug connector

Size	Document Number	Rev
	Redwood BSW 11.6"	A00

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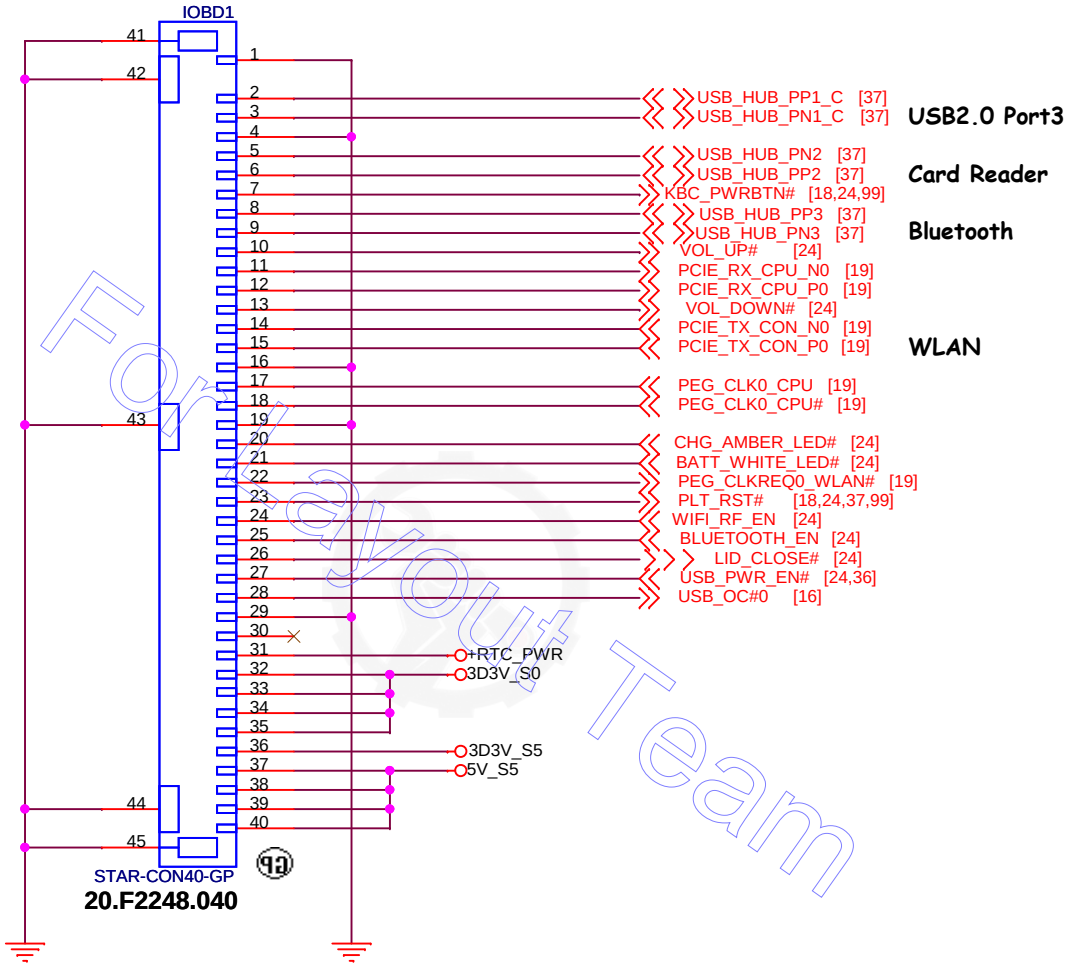

Power Pin Count : 10
GND Pin Count :5

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IO Board CONN*

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

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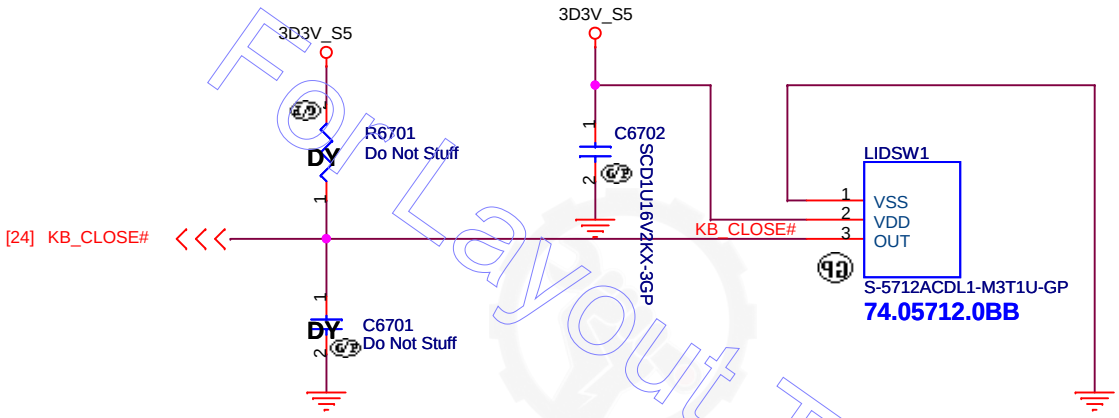

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Redwood BSW 11.6"***	***A00***

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SSID = Debug CONN

Blanking

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved) Debug CONN

Size	Document Number	Rev
A4	Redwood BSW 11.6"	A00

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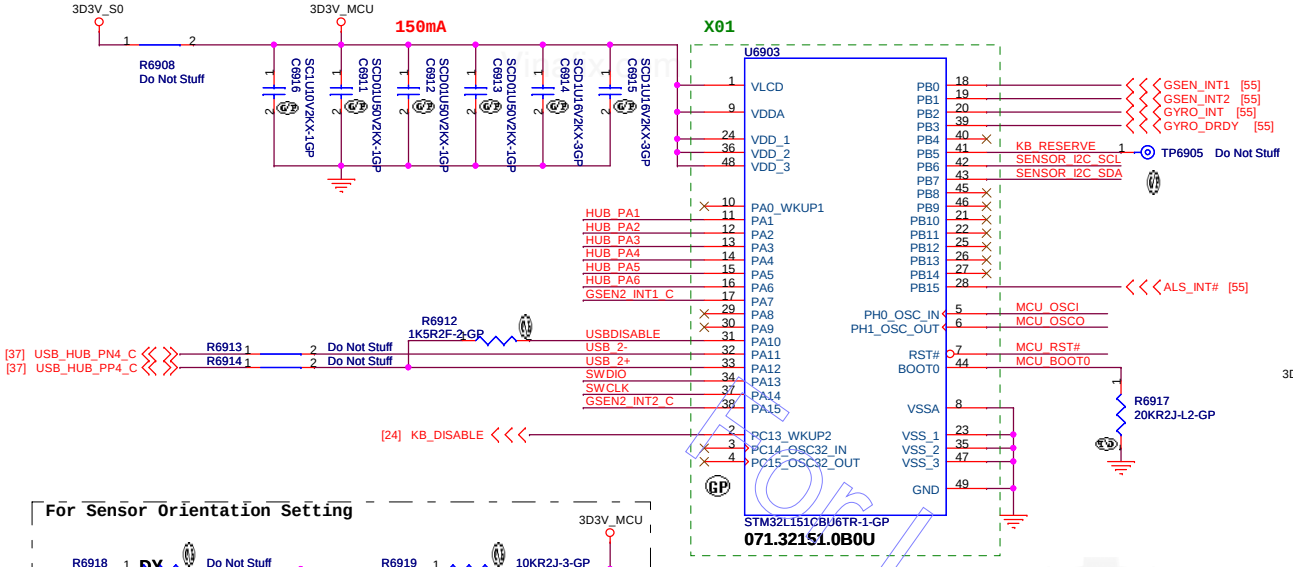
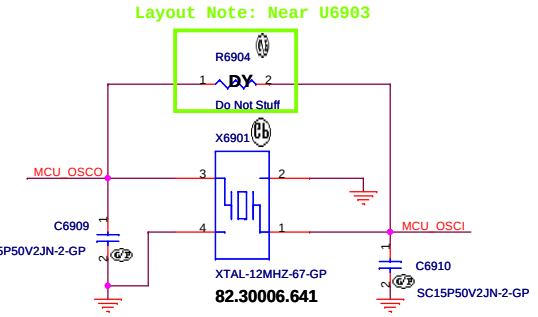
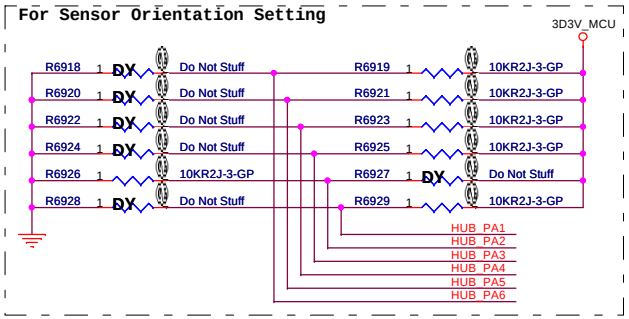
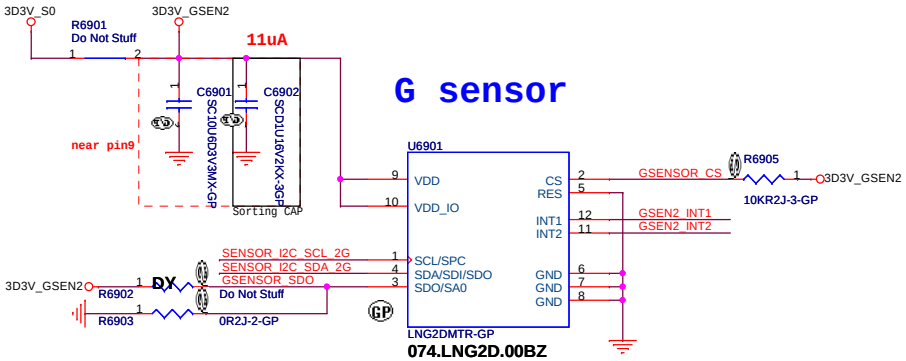
SSID = Sensor

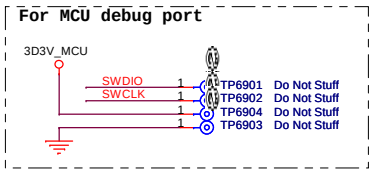
Sensor Hub

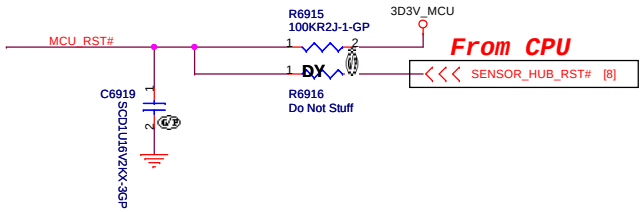


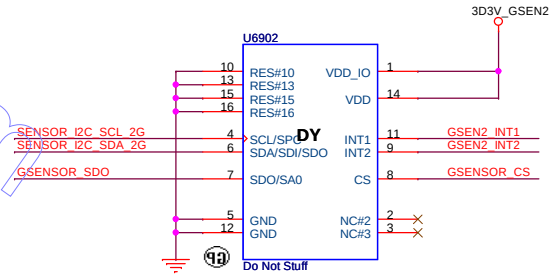


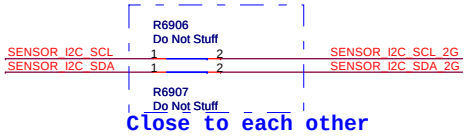


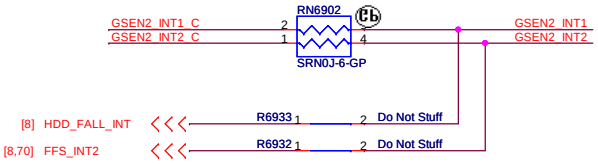












Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor

Size	Document Number	Rev
A3	Redwood BSW 11.6"	A00

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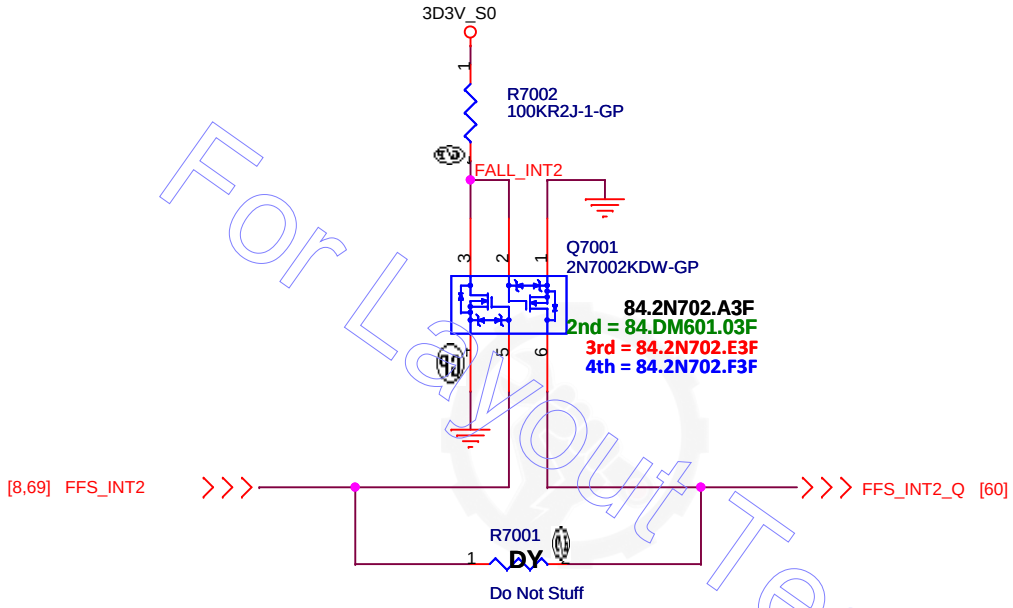
SSID = Free Fall Sensor



Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Free Fall Sensor***

Size	Document Number	Rev
A4	***Redwood BSW 11.6"***	***A00***

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (1/5)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (2/5)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (3/5)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (4/5)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Thunderbolt (5/5)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (1/5) PEG*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (2/5) DIGITAL*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (3/5) VRAM*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)GPU (4/5) GPIO

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)GPU (5/5) PWR/GND*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM1,2 (1/4)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM3,4 (2/4)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)VRAM5,6 (3/4)

Size	Document Number	Rev
A4	***Redwood BSW 11.6"***	***A00***

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)VRAM7,8 (4/4)*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)VGA_CORE*	
Size: A4	Document Number: *Redwood BSW 11.6"*	Rev: *A00*
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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)DISCRETE VGAPOWER*

Size	Document Number	Rev
	Redwood BSW 11.6"	*A00*

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Redwood MLK 1st

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(Reserved)*		
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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***Redwood BSW 11.6"***	***A00***

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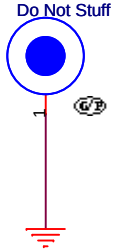
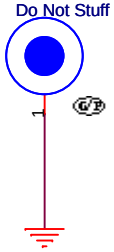
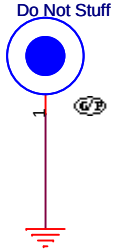
Do Not Stuff
H1
Do Not Stuff



Do Not Stuff
H5
Do Not Stuff



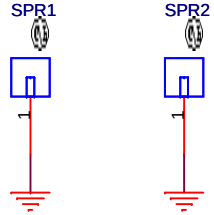
Do Not Stuff
H6
Do Not Stuff



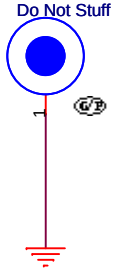
34.4T025.001

SPRING-52-GP
SPR1

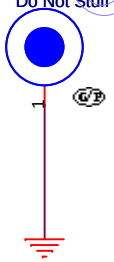
SPRING-52-GP
SPR2



Do Not Stuff
H2
Do Not Stuff

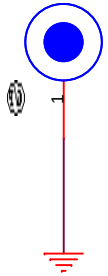


Do Not Stuff
H3
Do Not Stuff



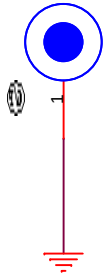
Do Not Stuff
H4
Do Not Stuff

34.4UV01.101
HS1
STF237R128H42-5-GP



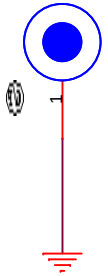
34.4UV28.101

34.4UV01.101
HS2
STF237R128H42-5-GP



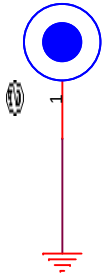
34.4UV28.101

34.4UV01.101
HS3
STF237R128H42-5-GP



34.4UV28.101

34.4UV01.101
HS4
STF237R128H42-5-GP



34.4UV28.101

Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A4	***Redwood BSW 11.6"***	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)NFC Connector*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved) TPM*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Finger Print*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Express Card*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Smart Card Socket*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*(Reserved)SW GFX eDP*	
Size: A4	Document Number: *Redwood BSW 11.6"*	Rev: *A00*
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Redwood MLK 1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)Bottom Docking*

Size	Document Number	Rev
A4	*Redwood BSW 11.6"*	*A00*

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Redwood MLK 1st

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Title	*(Reserved)LAN*	
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Blanking

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Title: *(Reserved)LAN SWITCH*

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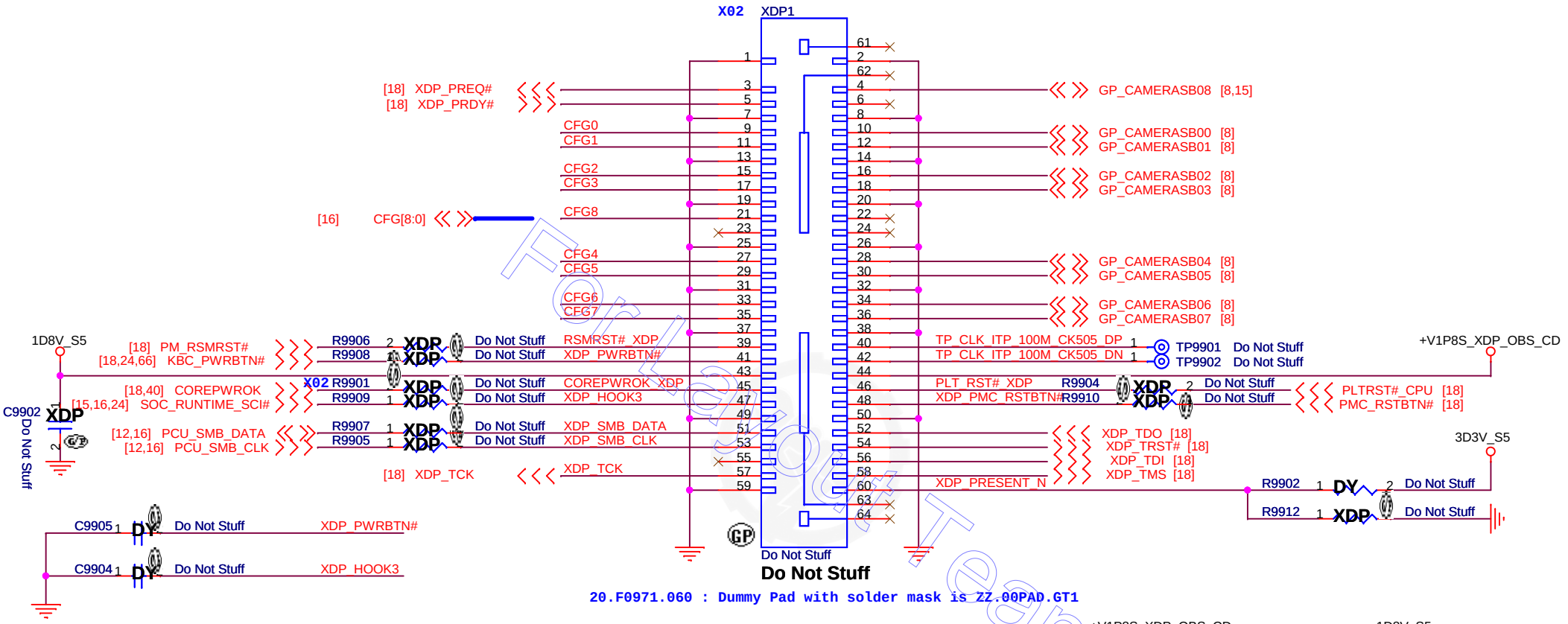
SSID = DEBUG PORT

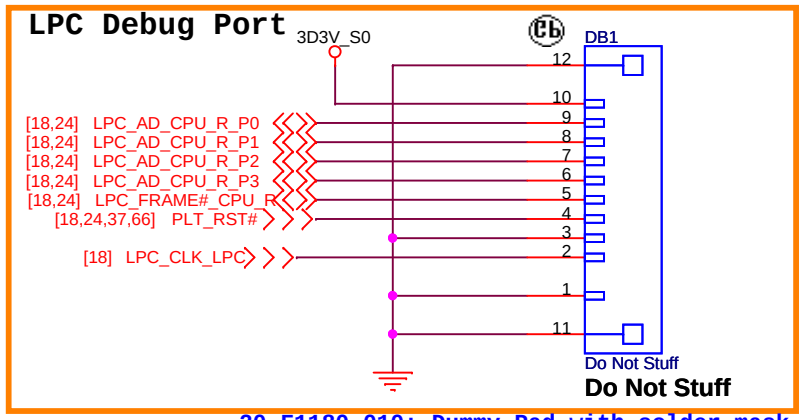
XDP Debug Port



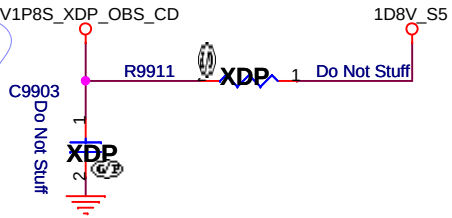
20.F0971.060 : Dummy Pad with solder mask is ZZ.00PAD.GT1

A00

LPC Debug Port



20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1



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Title: CPU_XDP

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Processor Strapping

Braswell Processor Schematic Checklist

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap overdrive	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[8]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.35V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, iCLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

USB2.0 MCP Side

Pair	Device
0	USB port 1 (usb charger)
1	USB port 2
2	USB HUB
3	Touch Panel
4	CAMERA

USH Side

Pair	Device
0	NA
1	NA

USB HUB Side

Pair	Device
1	USB2.0 Port3
2	Card Reader
3	Bluetooth
4	Sensor Hub

USB3.0 MCP Side

Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

PCIE Table

PCIE	
Lane	Device
1	WLAN
2	NA
3	NA
4	NA

SATA Table

SATA	
Pair	Device
0	HDD
1	NA

CHV Straps [CRB] -- strap detect @ RSMRST# assertion

Purpose	CHV Pin Name (refer CHV symbol PIN)	PU/PD (internal - Week)	Options	Default State on board?
DSI Display Detected	GPIO_SUS3	PD	1 - DSI detect, 0 - Disable	Low
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1 - normal, 0 - Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0 - Sus Debug enable	High

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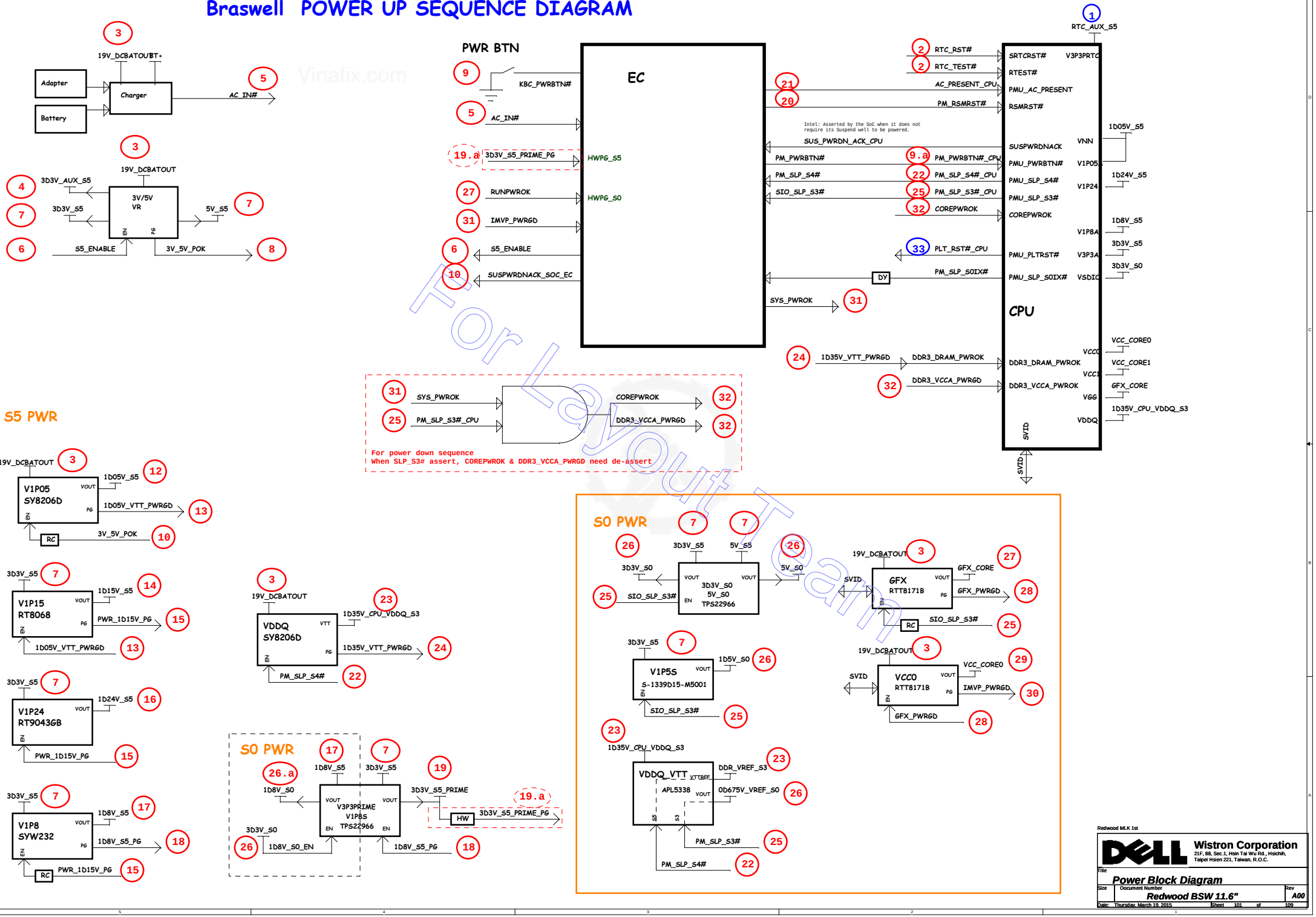
Braswell POWER UP SEQUENCE DIAGRAM



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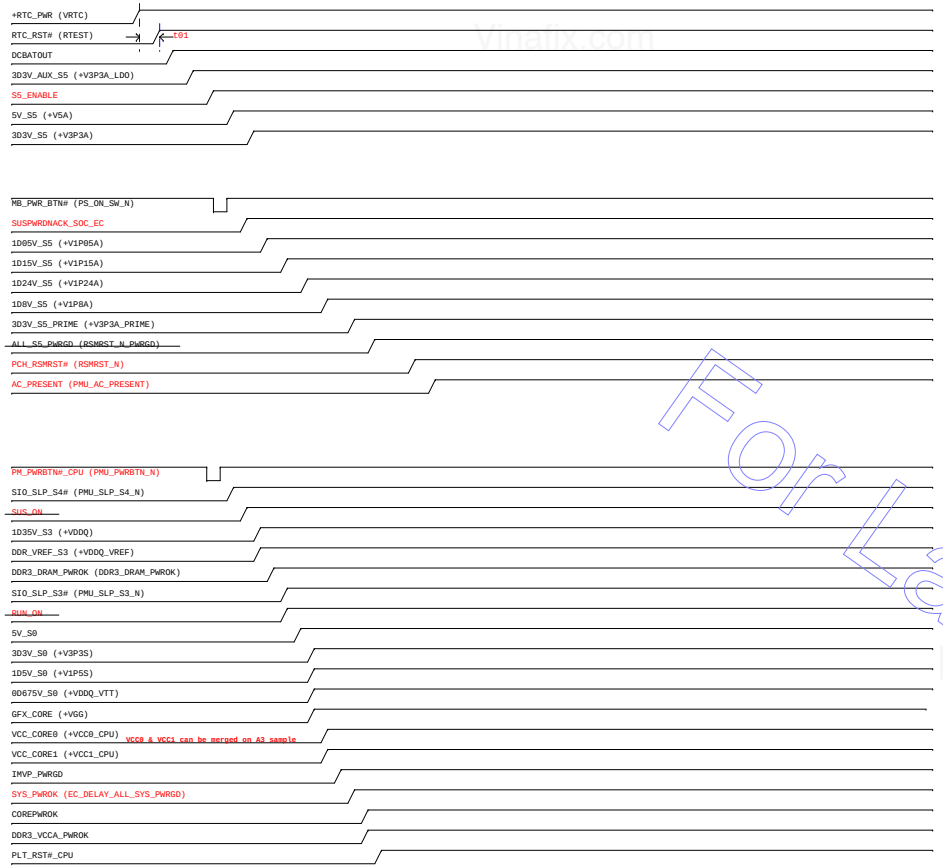
Intel-Power Up Sequence

(AC mode)

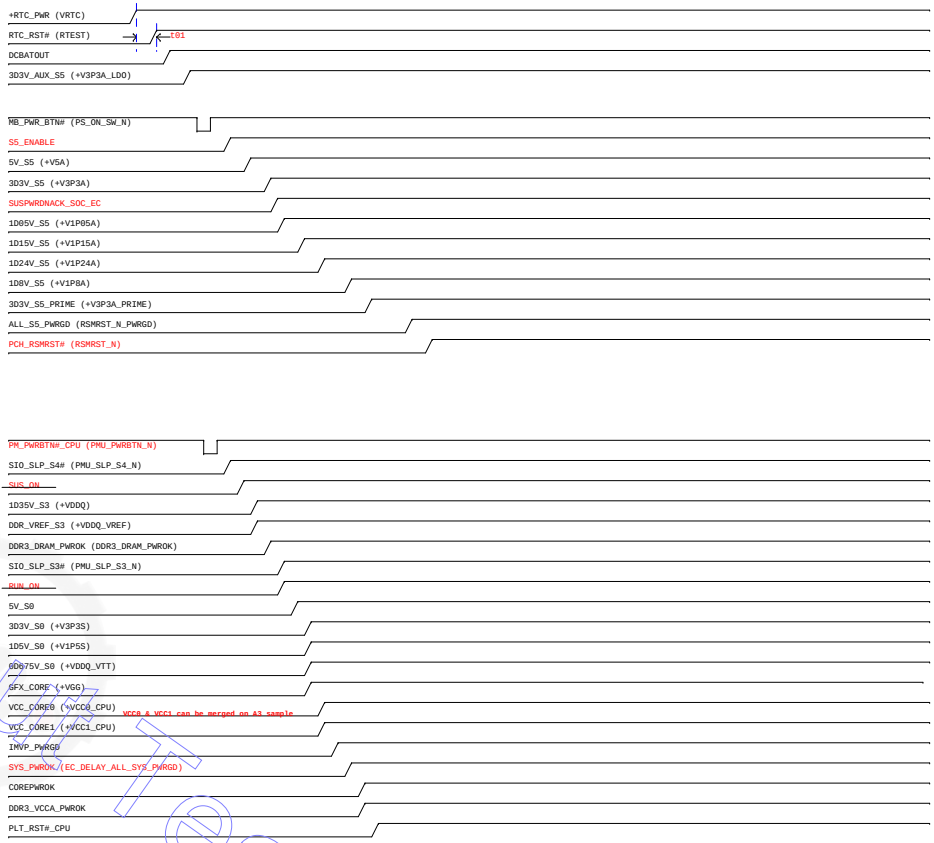
Red word : KBC GPIO



Intel-Power Up Sequence

(DC mode)

Red word : KBC GPIO



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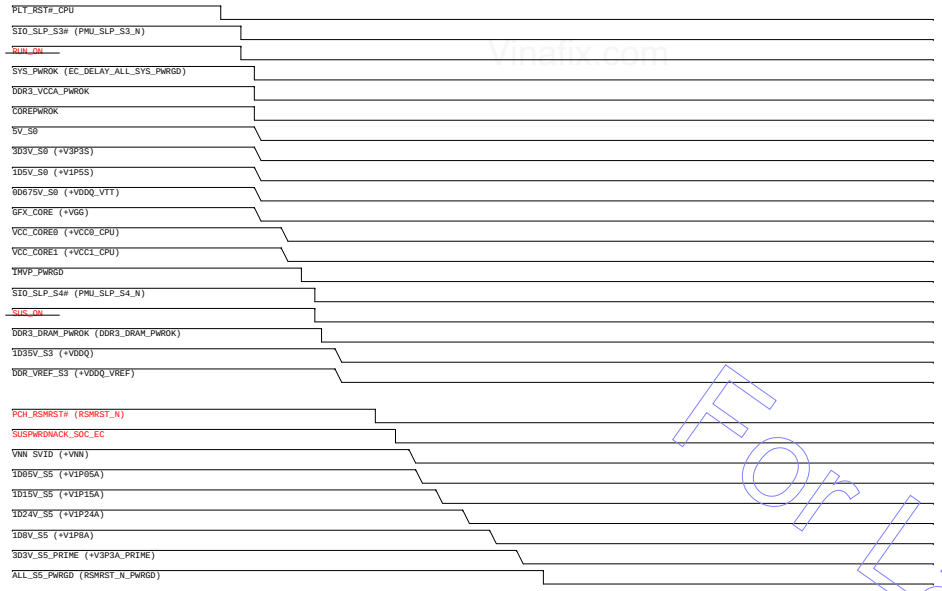
Intel-Power Down Sequence

(AC mode)

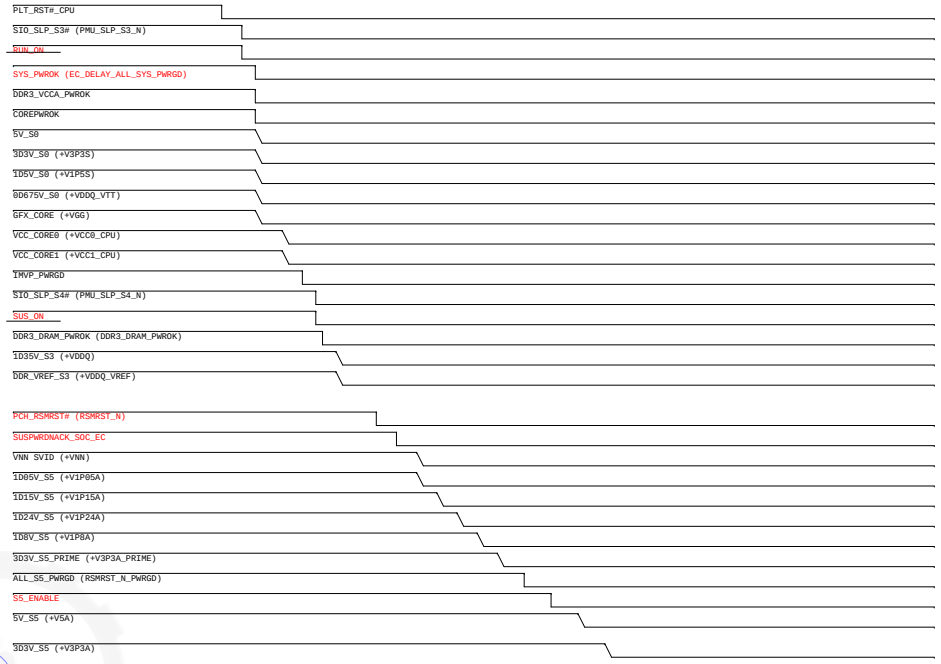
Red word : KBC GPIO



Intel-Power Down Sequence

(DC mode)

Red word : KBC GPIO



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Title: Power Down Sequence

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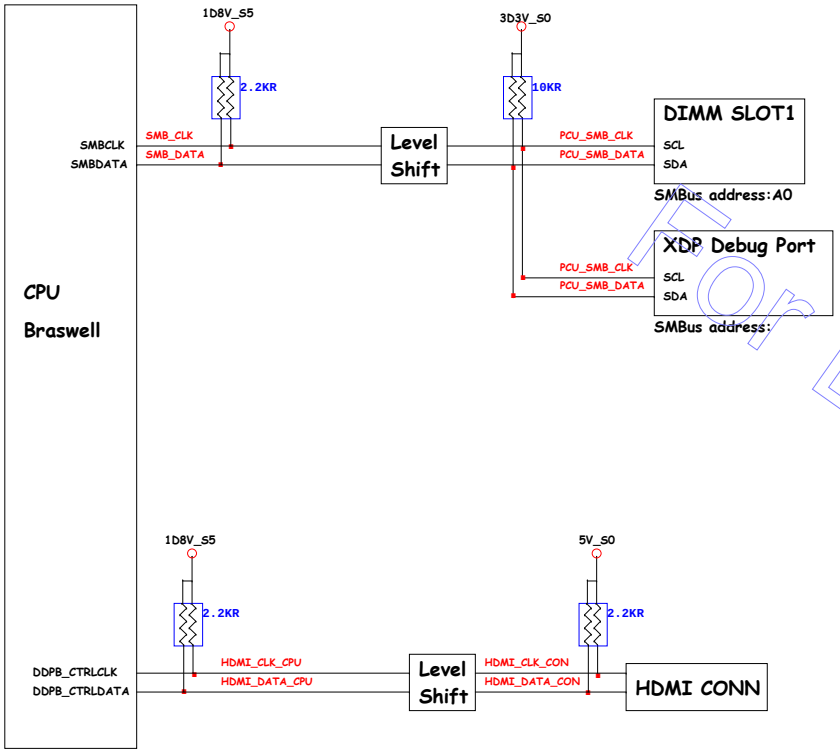
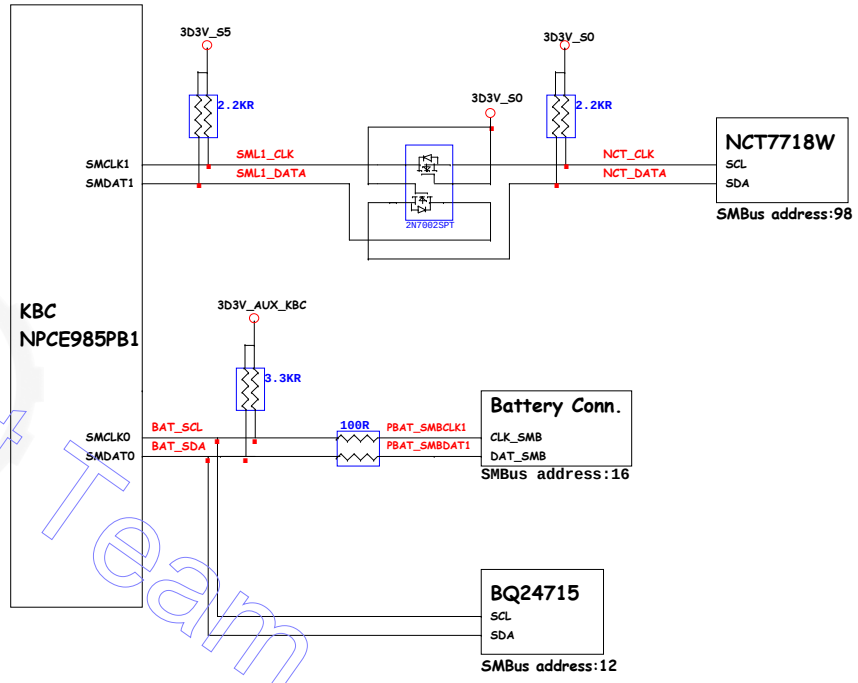
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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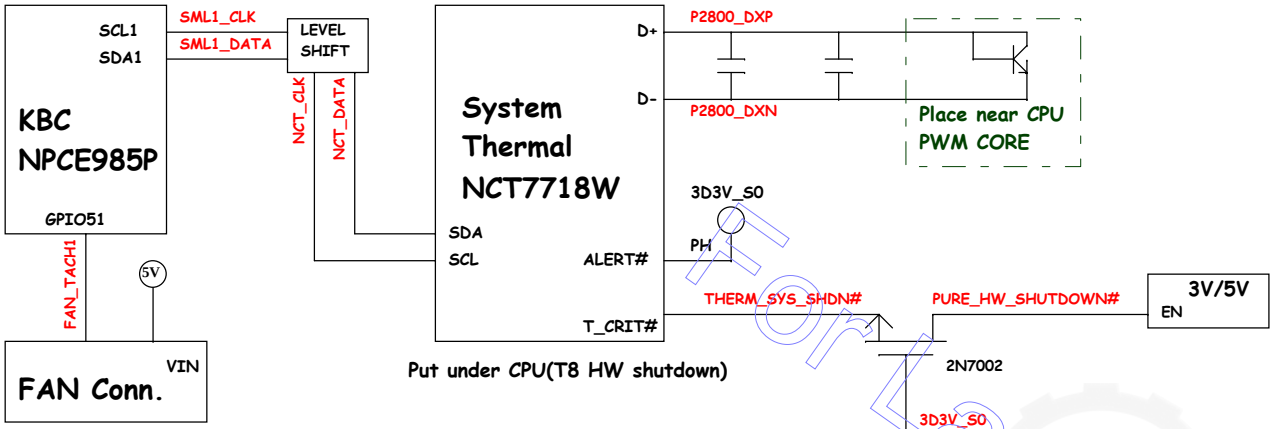
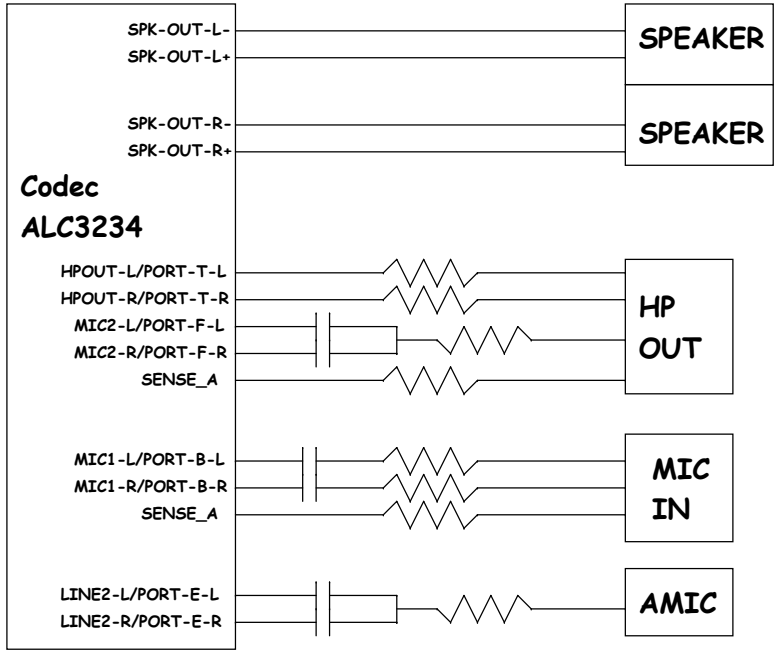
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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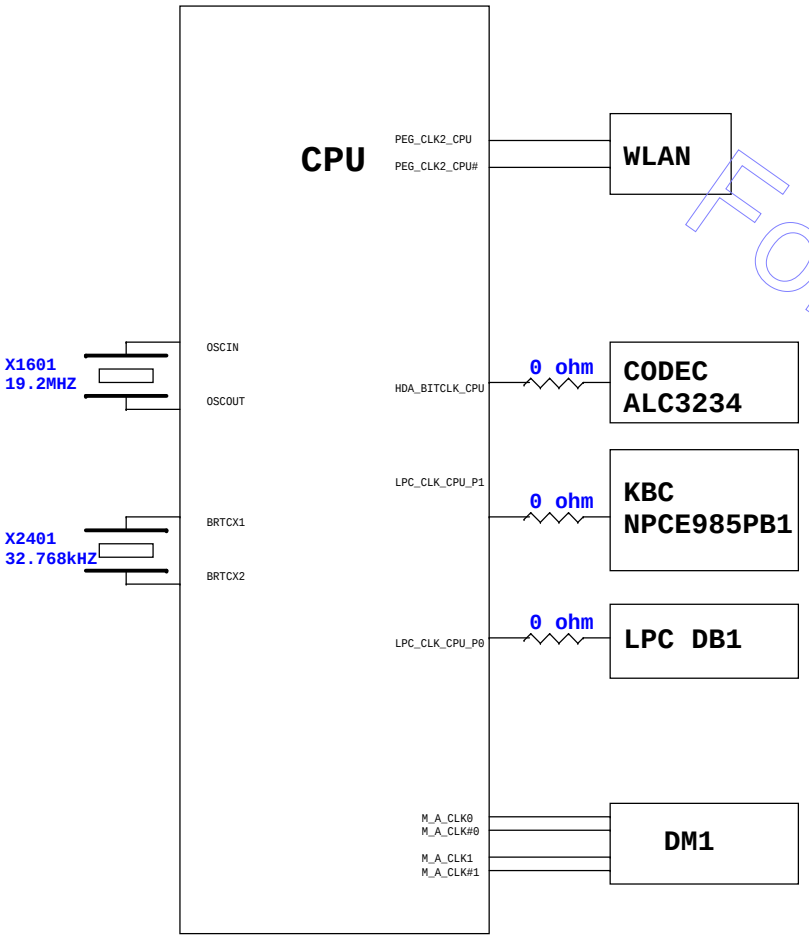
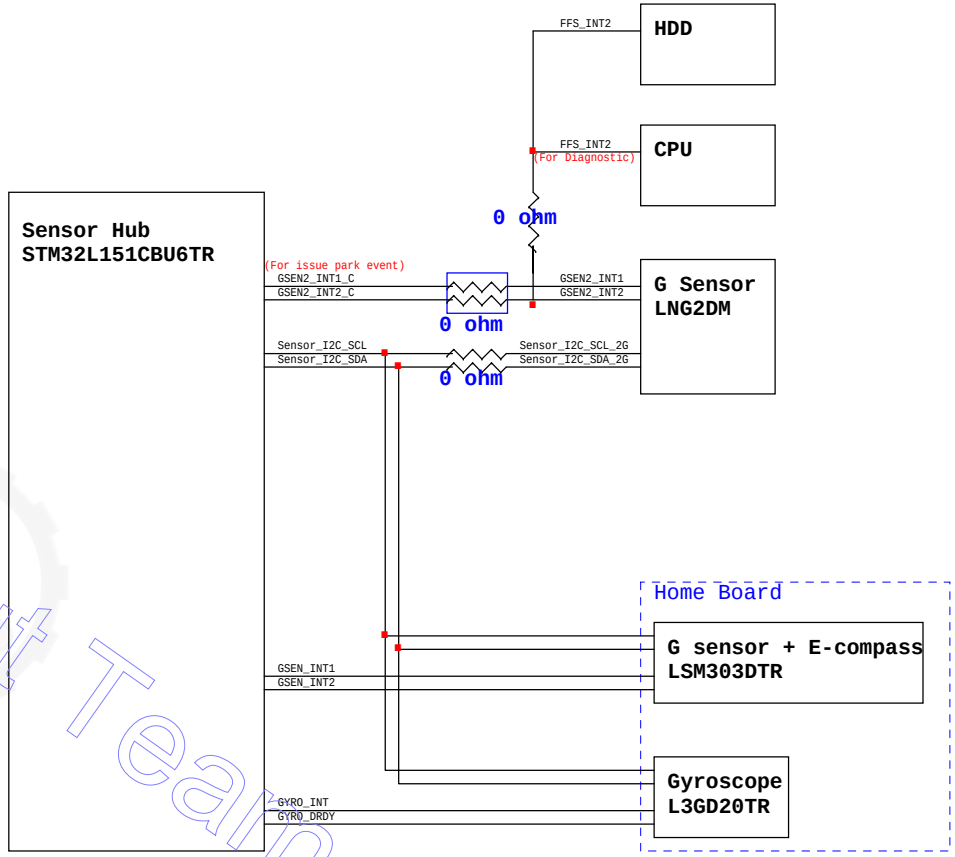
SSID = CLK Block Diagram





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Title: CLK / SENSOR Block

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