GA-970A-D3

Revision : 1.01

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RD980 HT-LINK I/F
11	RD980 PCIE I/F ,SWITCH
12	RD980 SYSTEM I/F
13	RD980 STRAPS ,SPMEM, POWER, GND
14	RTM880T-793
15	SB950 PCIE/PCI/CPU/LPC
16	SB950 ACPI/USB/GPIO/AUDIO
17	SB950 SATA/SPI/IDE/HWM
18	SB950 POWER & GND
19	PCI EXPRESS x16
20	PCI_E x1 SLOT 1,2,3
21	PCI SLOT 1, 2
22	IT8720 JX LPC IO ,Dual-BIOS ,TPM
23	COM, F_USB, R_USB, I_PWR
24	ALC889R CODEC
25	AUDIO JACK

PAGE	TITLE
26	FAN/HWMO KB/MS
27	ATX, FRONT PANEL ,EC
28	VCORE (PWMISL6329+6609)
29	POWER SEQUENCE ,VCC18 ,EUP
30	NB/SB POWER, VCC12HT, VDDA25 ,VCC12_DUAL
31	ETRON EJ168 F_USB30
32	PCIE X4, R_USB
33	REALTEK RTL8111E

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Title: COVER SHEET		
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 1 of 36	

Model Name:GA-970A-D3

Version: 1.01

P-Code: U98094-0

Component value change history

Date	Change Item		Reason
2011.03.10	0.1 9M970AD3-00-01		
2011.03.11	0.1 9M970AD3-00-01A		
2011.05.09	9M970AD3-00-10A	PCB Ver 1.0	
2011.05.10	9M970AD3-00-10B	PCB Ver 1.01	

Circuit or PCB layout change for next version

Date	Change Item	Reason
	0.1	
2011.02.22	Modify from GA-990XA-UD3	
	移除 PCIEx8, 1394, Front USB3	
	增加PCIEx1_3	
	Vcore change 4+1 power pake 6329+6609	
2011.03.11	修改CPU Vcore OCP與RC 電阻值	
	修改超電壓由每格10mV改爲5mV	
2011.03.14	6329 PIN GVOT.PVCC add P-H VCC	
	USB3.0 Fuse 3.0A change 3.5A	
	OPTICAL add 0.1uF(靠近OPTICAL)	
	LAN:8111E LA_VD33 add 0.1uF+4.7uF	
2011.05.09	change M2CPU料號12KRC-04K812-31R_12KRC-04K812-32R]	
	820uF change 560uF	
2011.05.10	cheang ddr dimm文字面順序1.2.3.4->4.2.3.1	

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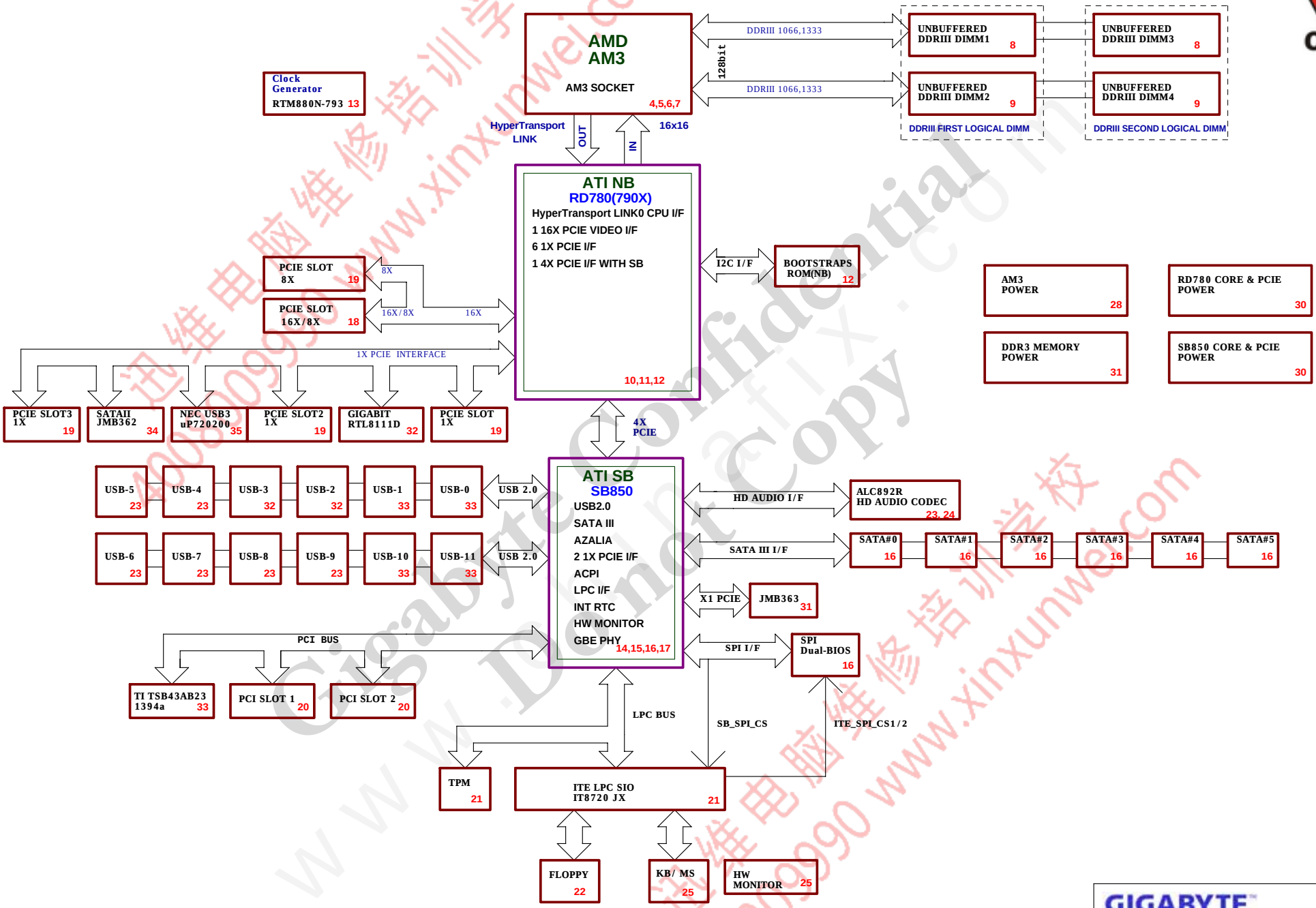
Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.01

Date: Monday, May 16, 2011 | Sheet 2 of 36



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Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 3 of 36

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

L0_CADIN_L[0..15]
L0_CADIN_H[0..15]
L0_CADOUT_L[0..15]
L0_CADOUT_H[0..15]

L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE5	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF4	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AE1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

COUPON1 COUPON1 1 2 COUPON/X VCC
COUPON2 COUPON2 1 2 COUPON/X

M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

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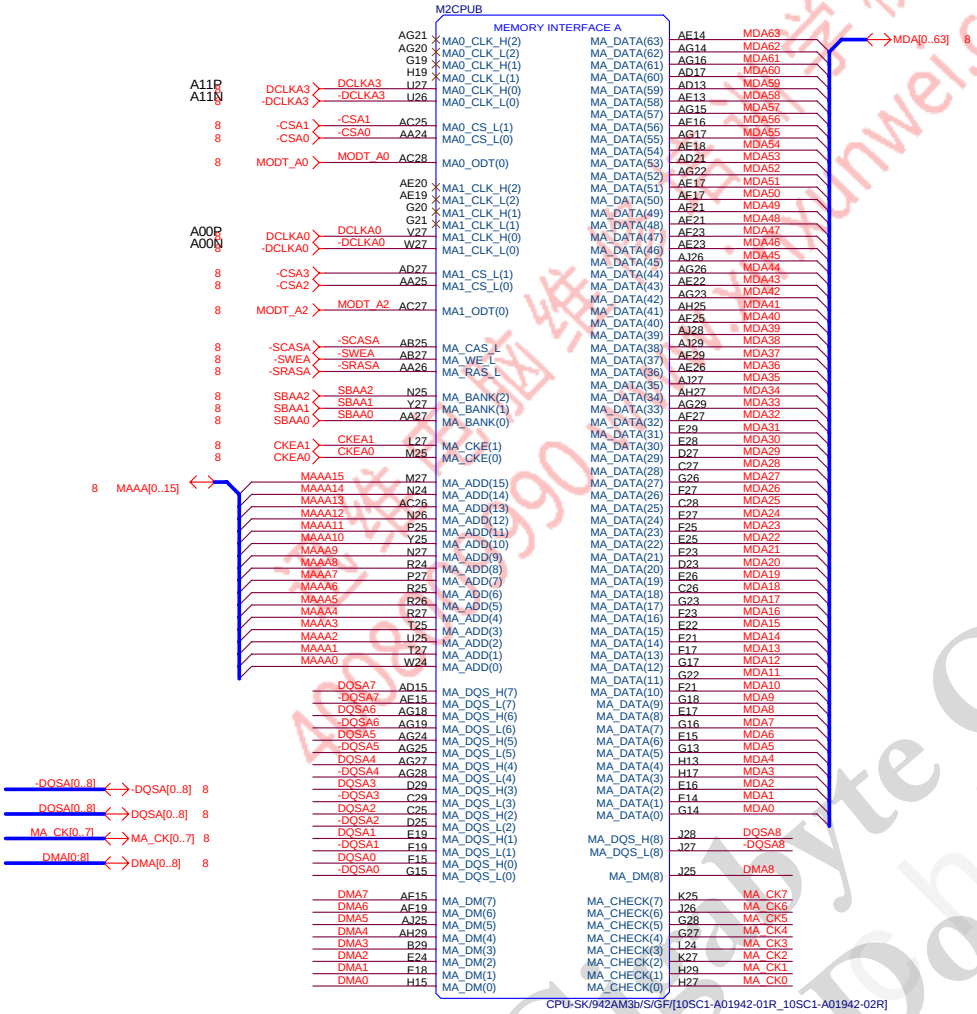
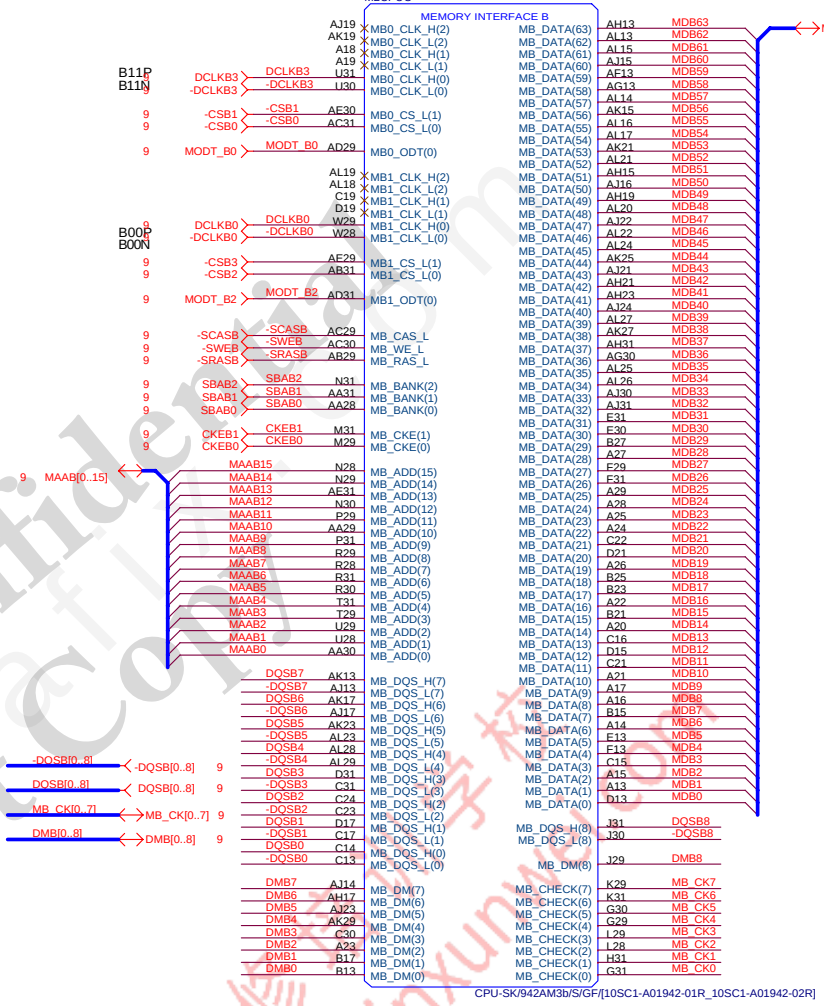
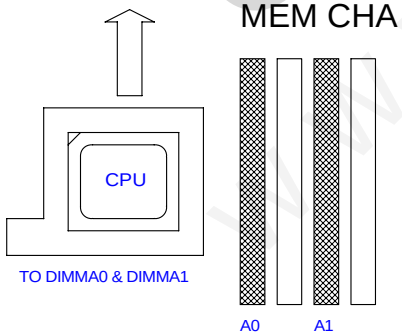
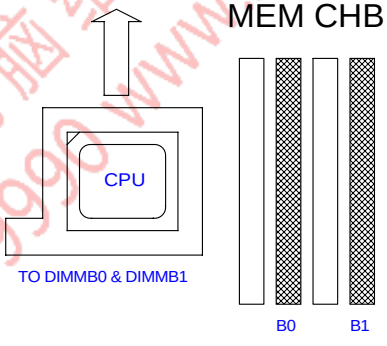
Title	CPU HYPER TRANSPORT	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 4 of 36	

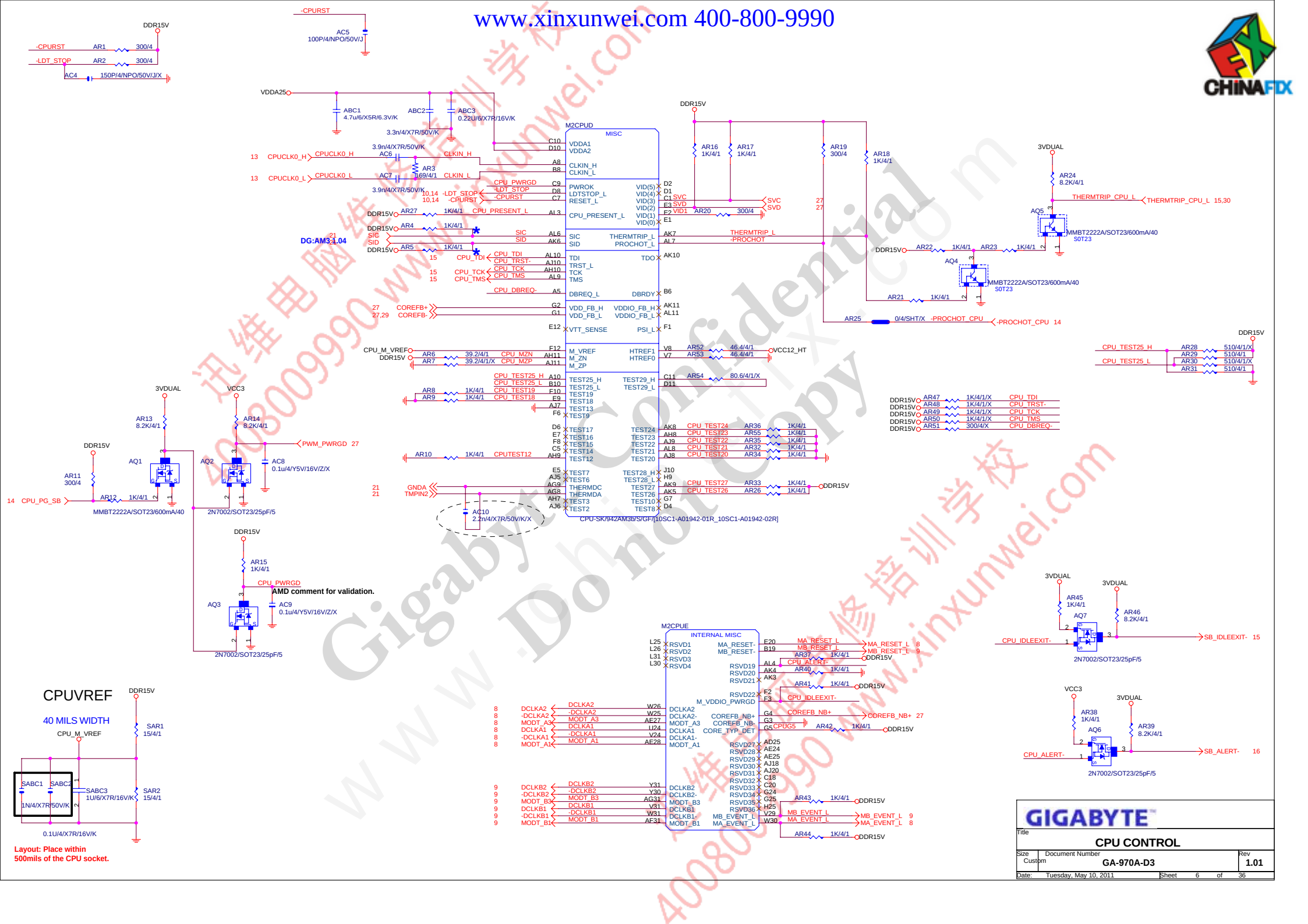








GIGABYTE			
Title: CPU DDRIII MEMORY			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 5 of 36		



VDDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

M2CPUE
VDD1

AE9 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUG
VDD2

H22 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUH
VDD3

AM3 Only

M2CPUI
VDDIO

BUTTOM SIDE

AMD Validation

BUTTOM SIDE

BUTTOM SIDE

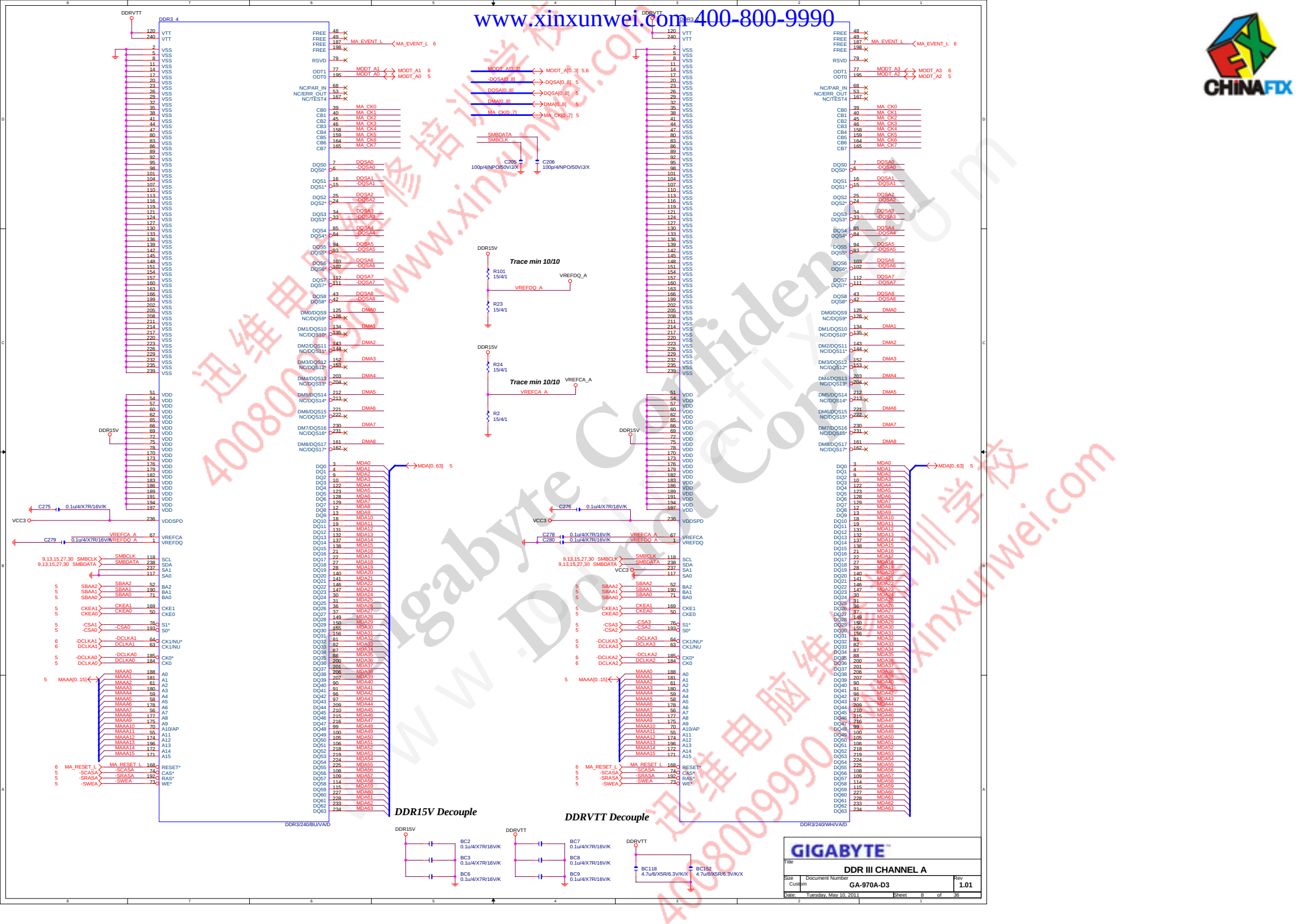
AMD Validation

AMD Validation

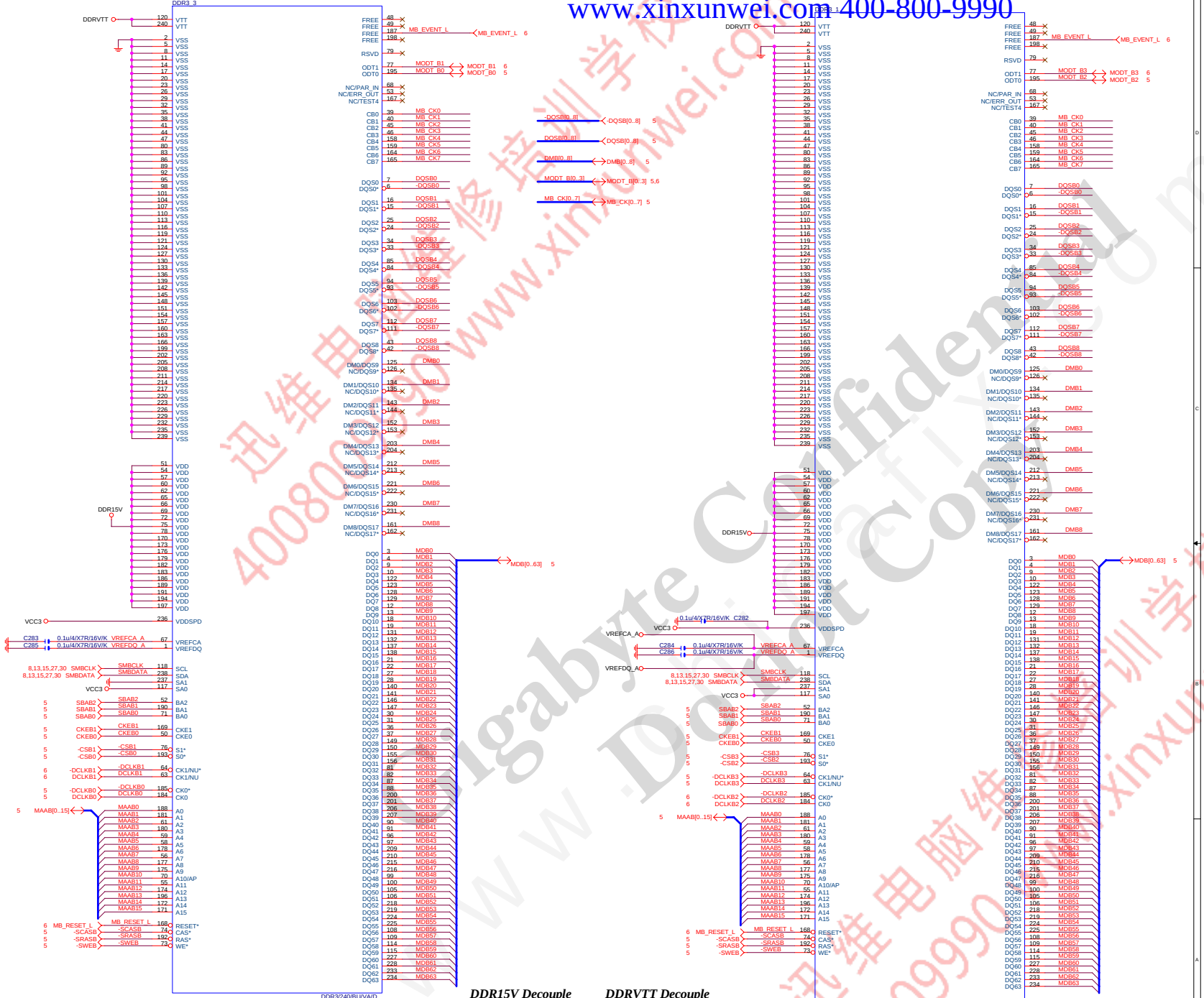
1021 EMI

DDR15V

Title	CPU POWER & GND
Size	Custom
Document Number	GA-970A-D3
Rev	1.01
Date:	Tuesday, May 10, 2011
Sheet	7 of 36



Title	DDR III CHANNEL A
Size	Custom
Document Number	GA-970A-D3
Rev	1.01
Date:	Tuesday, May 10, 2011
Sheet	8 of 36



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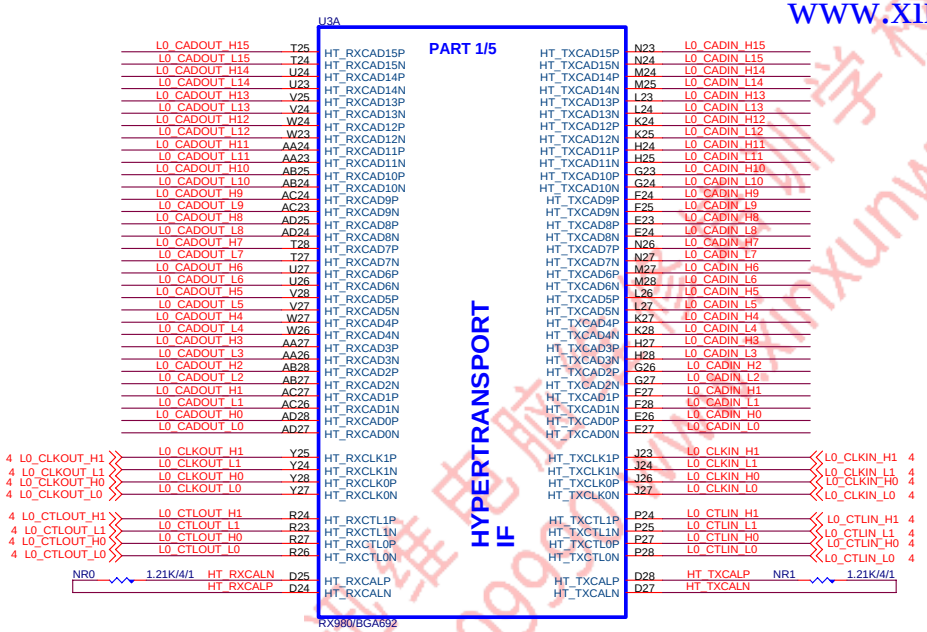
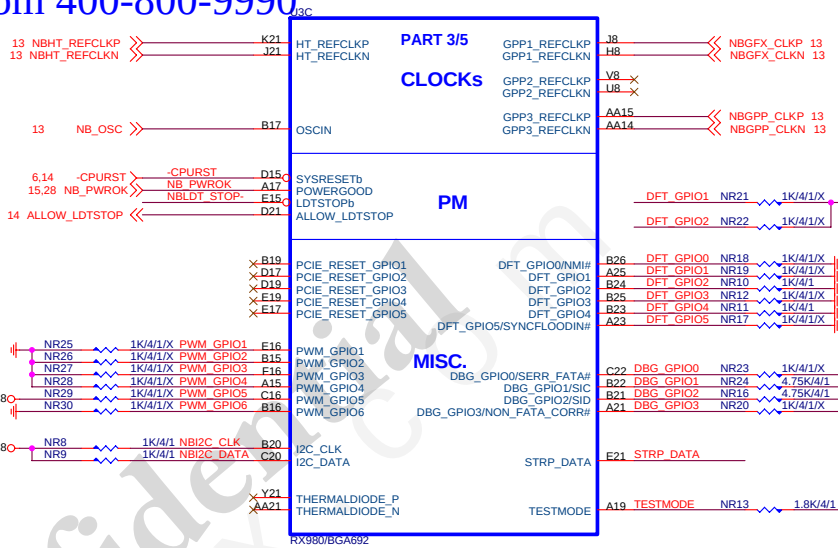
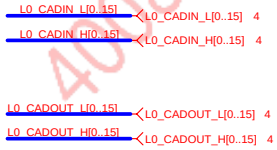
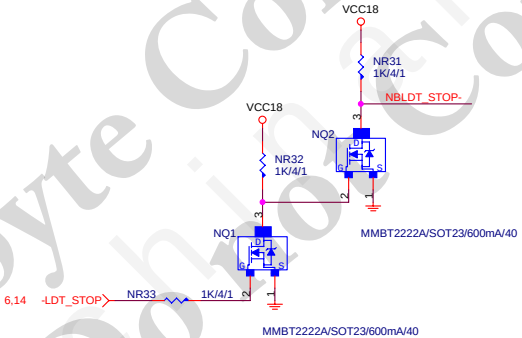
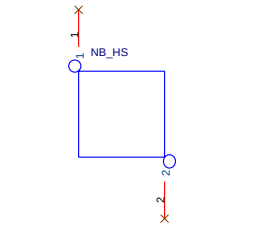
Title	DDR III CHANNEL B	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 9 of 36	











NB_HS/{12SP2-070018-01R_12SP2-070018-02R}

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

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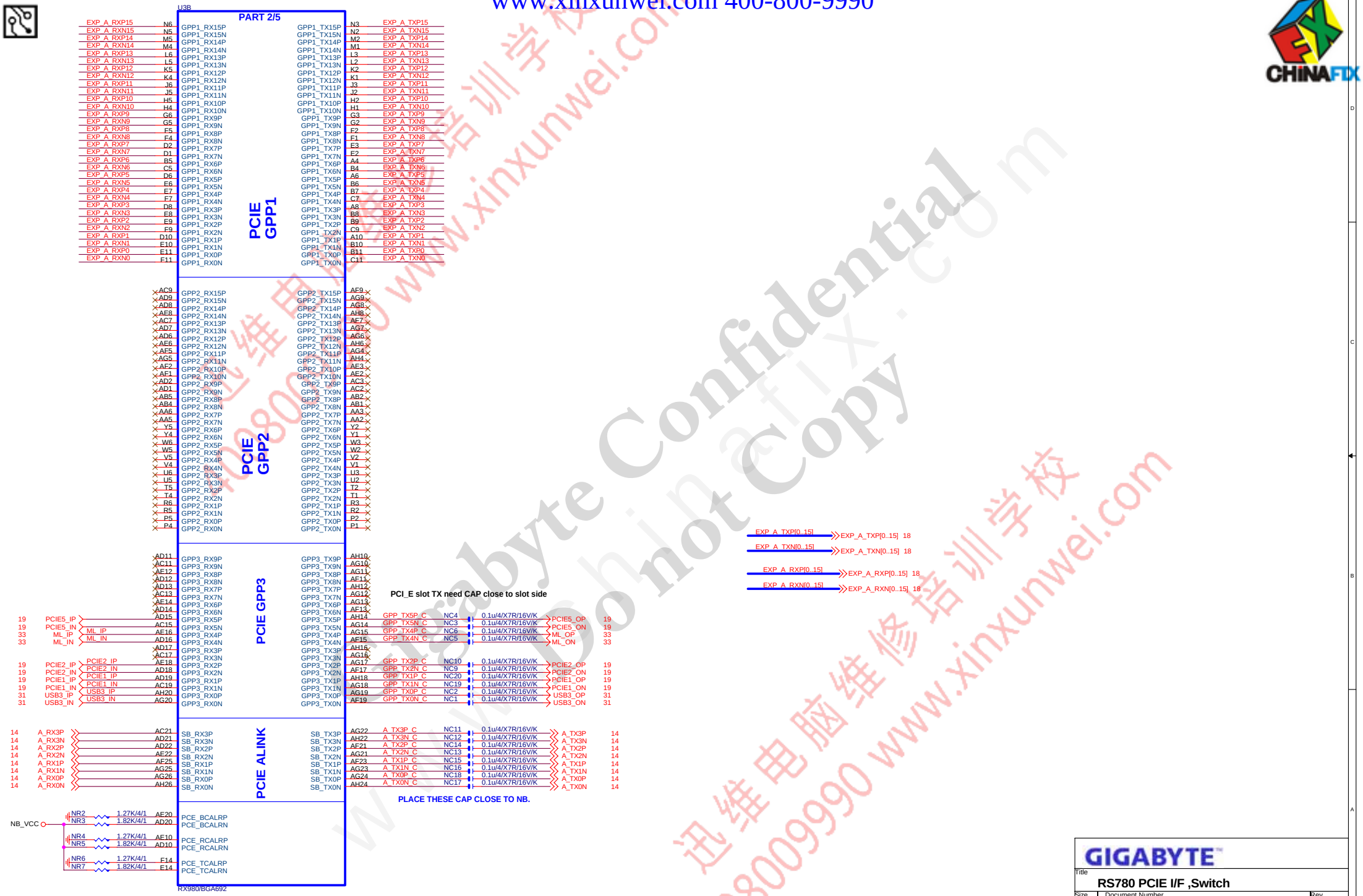
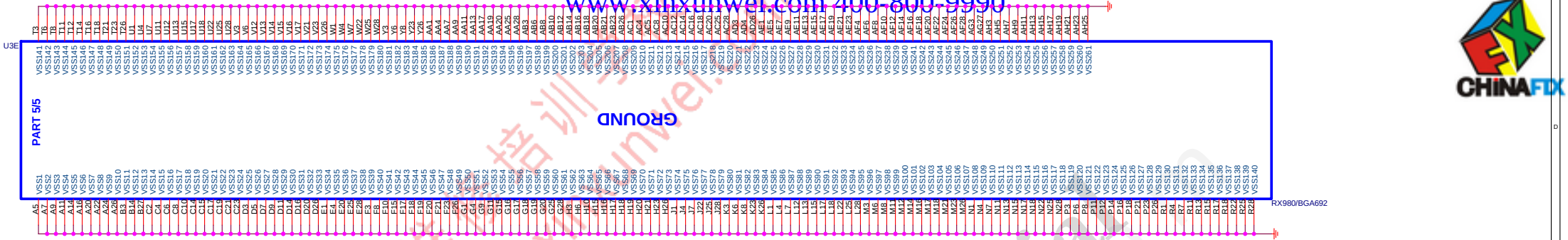
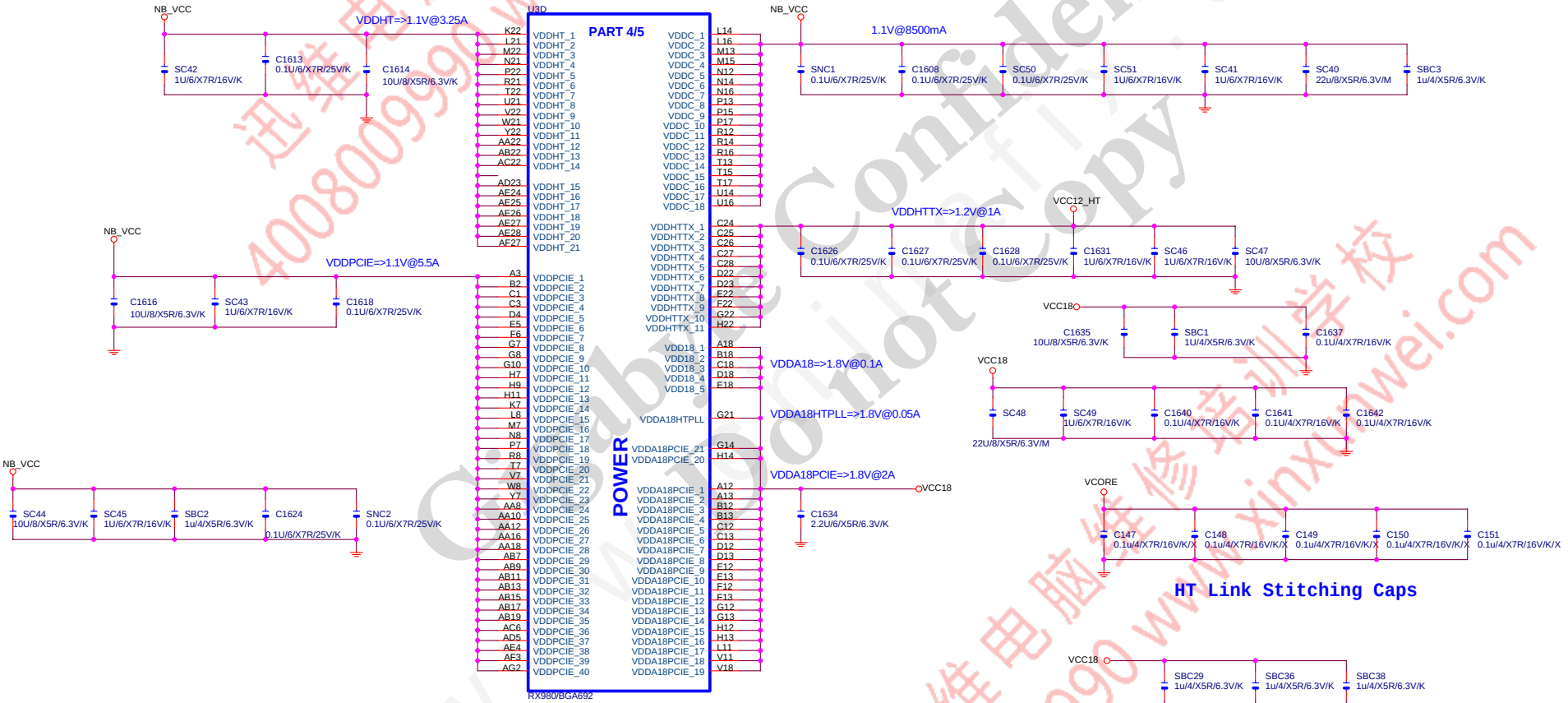
Title: RS780 HT-LINK I/F		
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 10 of 36	

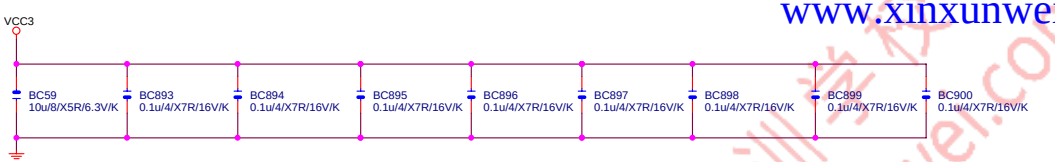


Title	RS780 PCIE I/F ,Switch
Size	Custom
Document Number	GA-970A-D3
Rev	1.01
Date:	Tuesday, May 10, 2011
Sheet	11 of 36





GIGABYTE			
Title: RS780 POWER & GND			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 12 of 36		



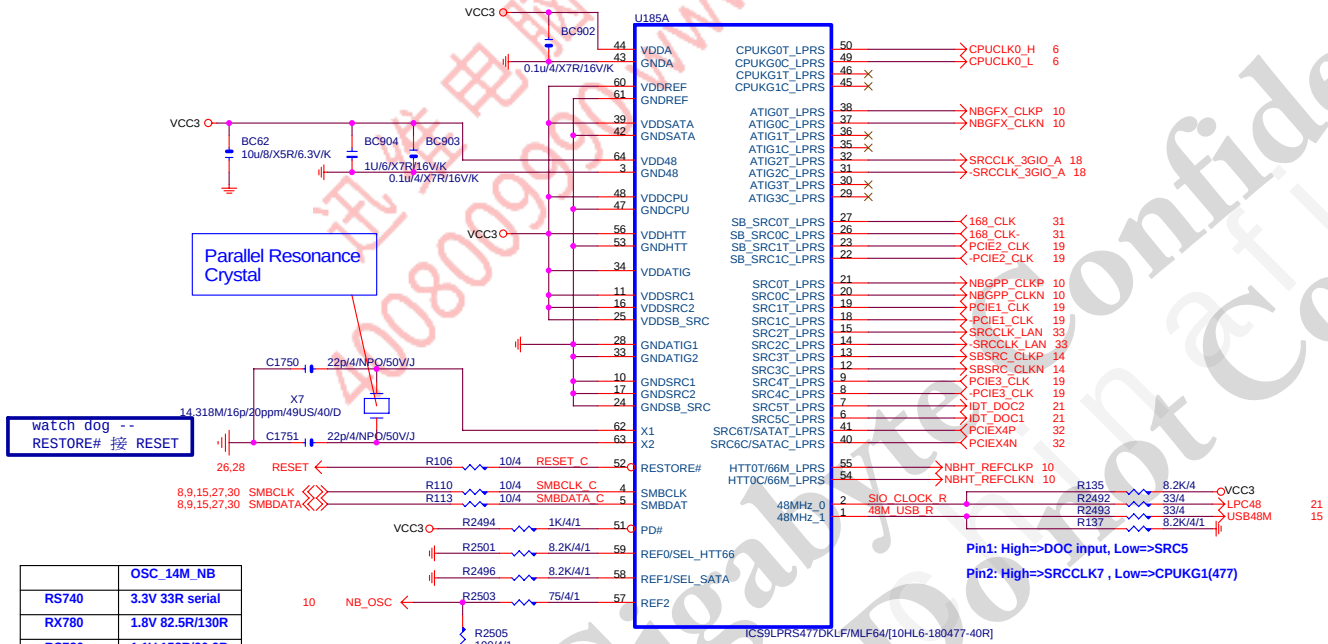
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

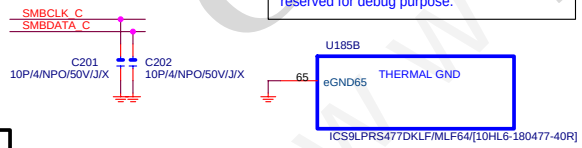
* the GFX_REFCLK input is required for all cases

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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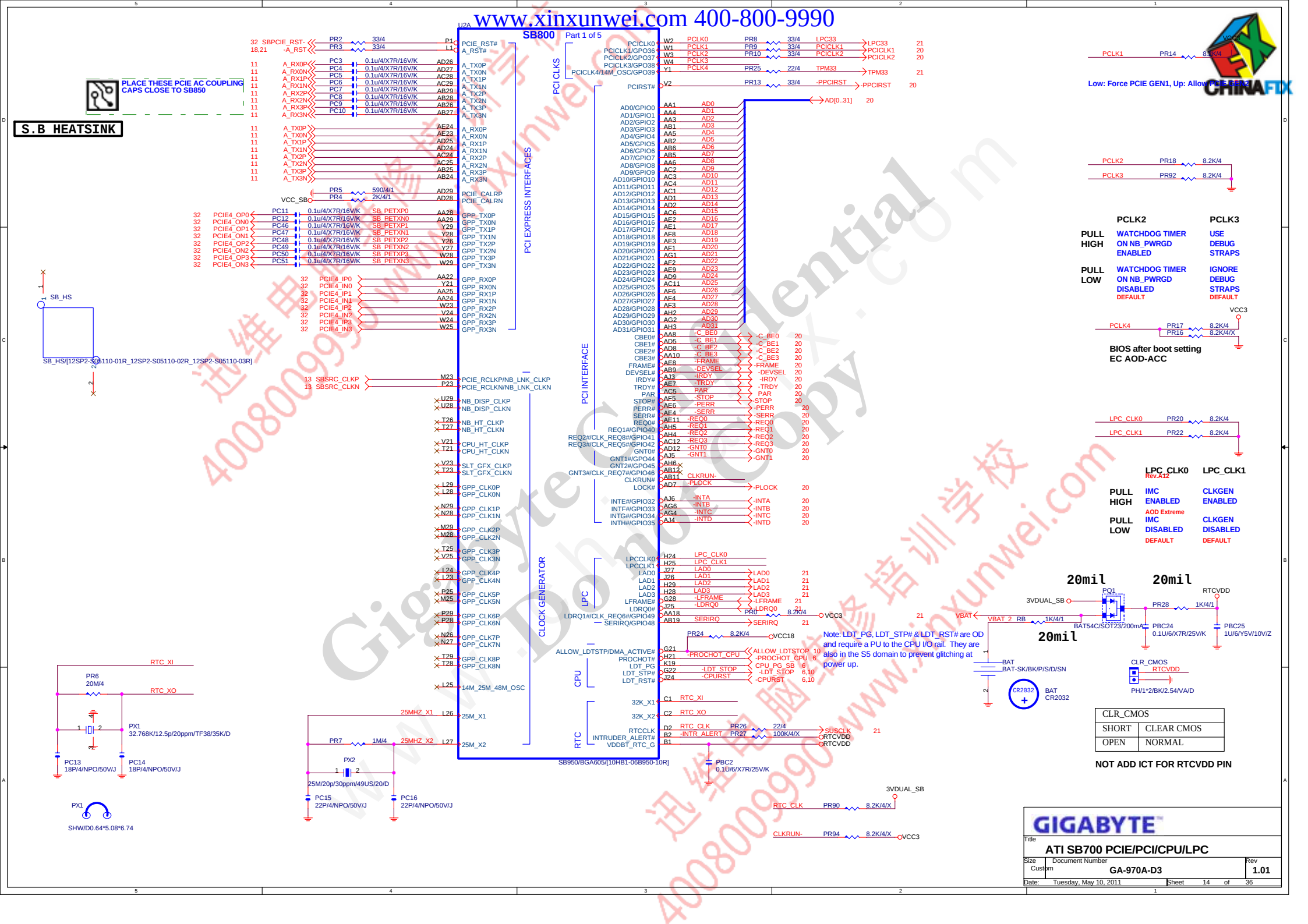
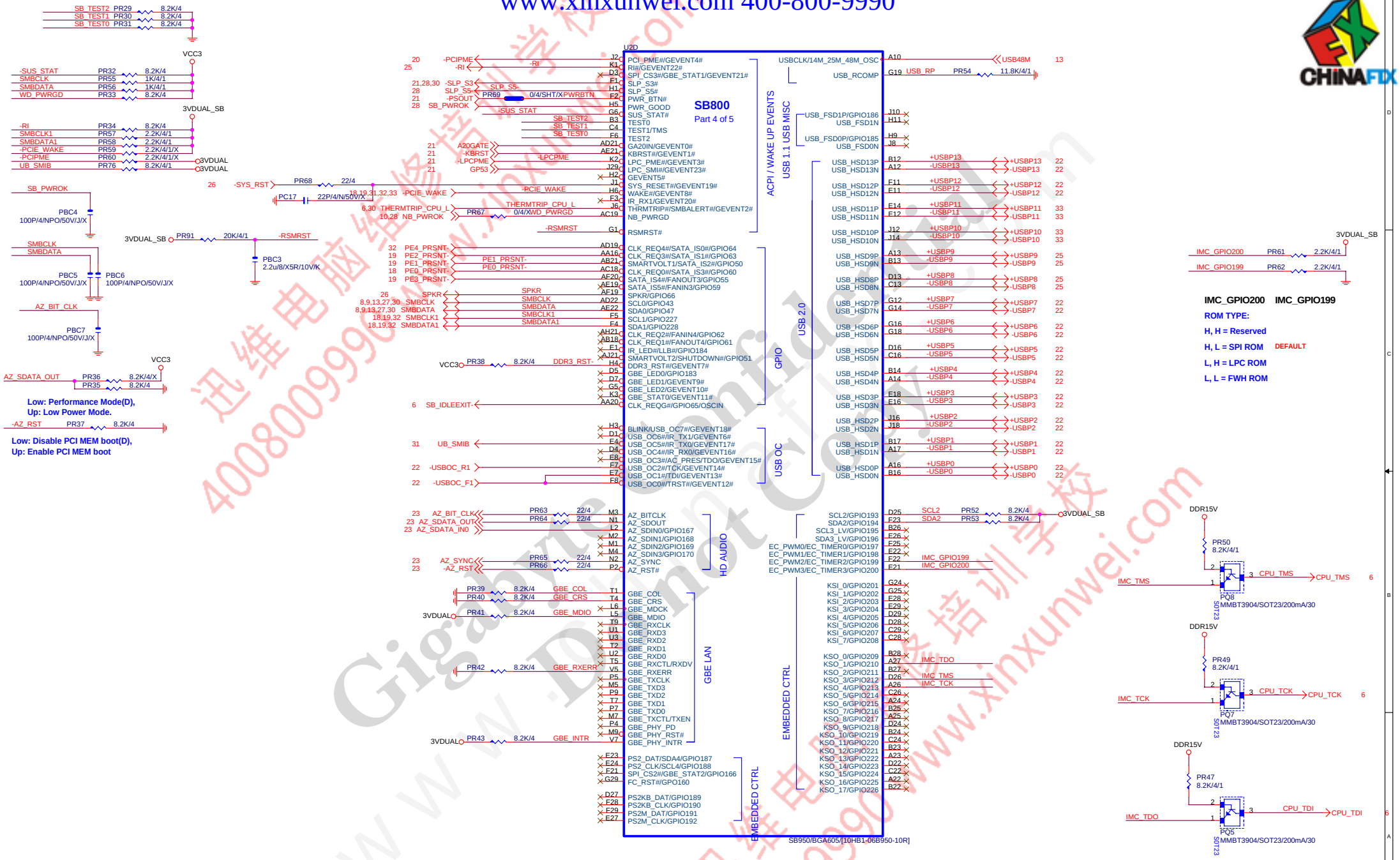
Title: RTM880N-793

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.01

Date: Tuesday, May 10, 2011 | Sheet 13 of 36





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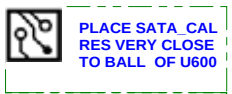
Title: ATI SB700 ACPI/USB/GPIO/AUDIO

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 15 of 36



PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB800

Part 2 of 5

SERIAL ATA

SP_TX0P_C	AH9	SATA_TX0P	
SP_TX0M_C	AJ9	SATA_TX0N	
SP_RX0M_C	AJ8	SATA_RX0N	
SP_RX0P_C	AH8	SATA_RX0P	
SP_TX1P_C	AH10	SATA_TX1P	
SP_TX1M_C	AJ10	SATA_TX1N	
SP_RX1M_C	AG10	SATA_RX1N	
SP_RX1P_C	AE10	SATA_RX1P	
SP_TX2P_C	AG12	SATA_TX2P	
SP_TX2M_C	AF12	SATA_TX2N	
SP_RX2M_C	AJ12	SATA_RX2N	
SP_RX2P_C	AH12	SATA_RX2P	
SP_TX3P_C	AH14	SATA_TX3P	
SP_TX3M_C	AJ14	SATA_TX3N	
SP_RX3M_C	AG14	SATA_RX3N	
SP_RX3P_C	AE14	SATA_RX3P	
SP_TX4P_C	AG17	SATA_TX4P	
SP_TX4M_C	AF17	SATA_TX4N	
SP_RX4M_C	AJ17	SATA_RX4N	
SP_RX4P_C	AH17	SATA_RX4P	
SP_TX5P_C	AJ18	SATA_TX5P	
SP_TX5M_C	AH18	SATA_TX5N	
SP_RX5M_C	AH19	SATA_RX5N	
SP_RX5P_C	AJ19	SATA_RX5P	
PR75 1K/4/1	AB14	SATA_CALRP	
PR74 931/4/1	AA14	SATA_CALRN	
26 -SATA_LED	AD11	SATA_ACT#/GPIO67	
TP5 SATA_X1	AD16	SATA_X1	
TP7 SATA_X2	AC16	SATA_X2	

GPIOD

FC_CLK	AH28
FC_FBCLKOUT	AG29
FC_FBCLKIN	AF26
FC_OE#/GPIOD145	AF28
FC_AVD#/GPIOD146	AG29
FC_WE#/GPIOD148	AG26
FC_CE1#/GPIOD149	AF27
FC_CE2#/GPIOD150	AE29
FC_INT1/GPIOD144	AF29
FC_INT2/GPIOD147	AH27
FC_ADQ0/GPIOD128	AJ27
FC_ADQ1/GPIOD129	AJ26
FC_ADQ2/GPIOD130	AH25
FC_ADQ3/GPIOD131	AH24
FC_ADQ4/GPIOD132	AG23
FC_ADQ5/GPIOD133	AH23
FC_ADQ6/GPIOD134	AJ22
FC_ADQ7/GPIOD135	AG21
FC_ADQ8/GPIOD136	AF21
FC_ADQ9/GPIOD137	AH22
FC_ADQ10/GPIOD138	AJ23
FC_ADQ11/GPIOD139	AF23
FC_ADQ12/GPIOD140	AJ24
FC_ADQ13/GPIOD141	AJ25
FC_ADQ14/GPIOD142	AG25
FC_ADQ15/GPIOD143	AH26

HW MONITOR

FANOUT0/GPIO52	W5
FANOUT1/GPIO53	W6
FANOUT2/GPIO54	Y9
FANIN0/GPIO56	W7
FANIN1/GPIO57	V9
FANIN2/GPIO58	W8
TEMPIN0/GPIO171	B6
TEMPIN1/GPIO172	A6
TEMPIN2/GPIO173	A5
TEMPIN3/TALERT#/GPIO174	B5 → SB_ALERT- 6
TEMP_COMM	C7
VIN0/GPIO175	A3
VIN1/GPIO176	B4
VIN2/GPIO177	A4
VIN3/GPIO178	C5
VIN4/GPIO179	A7
VIN5/GPIO180	B7
VIN6/GBE_STAT3/GPIO181	B8
VIN7/GBE_LED3/GPIO182	A8

SPI ROM

SB_SPI_DI PR70 22/4	SB_SPI_DI_R	J5	SPI_DI/GPIO164
SB_SPI_DO PR71 22/4	SB_SPI_DO_R	E2	SPI_DO/GPIO163
SB_SPI_CLK PR72 22/4	SB_SPI_CLK_R	K4	SPI_CLK/GPIO162
-SB_SPI_CS_ITE PR73 22/4	SB_SPI_CS-	K9	SPI_CS1#/GPIO165
		G2	ROM_RST#/GPIO161
		G27	NC1
		Y2	NC2

21 -SB_SPI_CS_ITE

SB950/BGA605/[10HB1-06B950-10R]

VCC_SB

PR75 1K/4/1 SATA_CALRP

PR74 931/4/1 SATA_CALRN

PLACE SATA AC COUPLING CAPS CLOSE TO SB850

SATA3_0_1

SP_TX0P_C	PC18	0.01u/4/X7R/25V/K	SATA0TXPC	SATA1TXPC	PC30	0.01u/4/X7R/25V/K	SP_TX1P_C
SP_TX0M_C	PC19	0.01u/4/X7R/25V/K	SATA0TXNC	SATA1TXNC	PC31	0.01u/4/X7R/25V/K	SP_TX1M_C
SP_RX0M_C	PC20	0.01u/4/X7R/25V/K	SATA0RXNC	SATA1RXNC	PC32	0.01u/4/X7R/25V/K	SP_RX1M_C
SP_RX0P_C	PC21	0.01u/4/X7R/25V/K	SATA0RXPC	SATA1RXPC	PC33	0.01u/4/X7R/25V/K	SP_RX1P_C

SATA14/BU/H/OP/RA/D/2

SATA3_2_3

SP_TX2P_C	PC22	0.01u/4/X7R/25V/K	SATA2TXPC	SATA3TXPC	PC34	0.01u/4/X7R/25V/K	SP_TX3P_C
SP_TX2M_C	PC23	0.01u/4/X7R/25V/K	SATA2TXNC	SATA3TXNC	PC35	0.01u/4/X7R/25V/K	SP_TX3M_C
SP_RX2M_C	PC24	0.01u/4/X7R/25V/K	SATA2RXNC	SATA3RXNC	PC36	0.01u/4/X7R/25V/K	SP_RX3M_C
SP_RX2P_C	PC25	0.01u/4/X7R/25V/K	SATA2RXPC	SATA3RXPC	PC37	0.01u/4/X7R/25V/K	SP_RX3P_C

SATA14/BU/H/OP/RA/D/2

SATA3_4_5

SP_TX4P_C	PC26	0.01u/4/X7R/25V/K	SATA4TXPC	SATA5TXPC	PC38	0.01u/4/X7R/25V/K	SP_TX5P_C
SP_TX4M_C	PC27	0.01u/4/X7R/25V/K	SATA4TXNC	SATA5TXNC	PC39	0.01u/4/X7R/25V/K	SP_TX5M_C
SP_RX4M_C	PC28	0.01u/4/X7R/25V/K	SATA4RXNC	SATA5RXNC	PC40	0.01u/4/X7R/25V/K	SP_RX5M_C
SP_RX4P_C	PC29	0.01u/4/X7R/25V/K	SATA4RXPC	SATA5RXPC	PC41	0.01u/4/X7R/25V/K	SP_RX5P_C

SATA14/BU/H/OP/RA/D/2

VCC_SB

PBC8 1U/6/Y5V/10V/Z

PBC9 0.1u/4/Y5V/16V/Z

VCC3

PBC10 1U/6/Y5V/10V/Z

PBC11 0.1u/4/Y5V/16V/Z

VCC3

M_BIOS

21 -ITE_SPI_CS

-ITE_SPI_CS	1	CS#	VDD 8 SPC23 0.1U/4/Y5V/16V/Z
SB_SPI_DI	2	SO	HOLD# 7 -SPI_HOLD0
-BIOS_WP	3	WP#	SCK 6 SB_SPI_CLK
	4	VSS	SI 5 SB_SPI_DO

32M/SPI/SO8/200mil/S

B_BIOS

21 -ITE_SPI_CS1

-ITE_SPI_CS1	1	CS#	VDD 8 VCC3
SB_SPI_DI	2	SO	HOLD# 7 -SPI_HOLD0
-BIOS_WP	3	WP#	SCK 6 SB_SPI_CLK
	4	VSS	SI 5 SB_SPI_DO

32M/SPI/SO8/200mil/S

VCC3

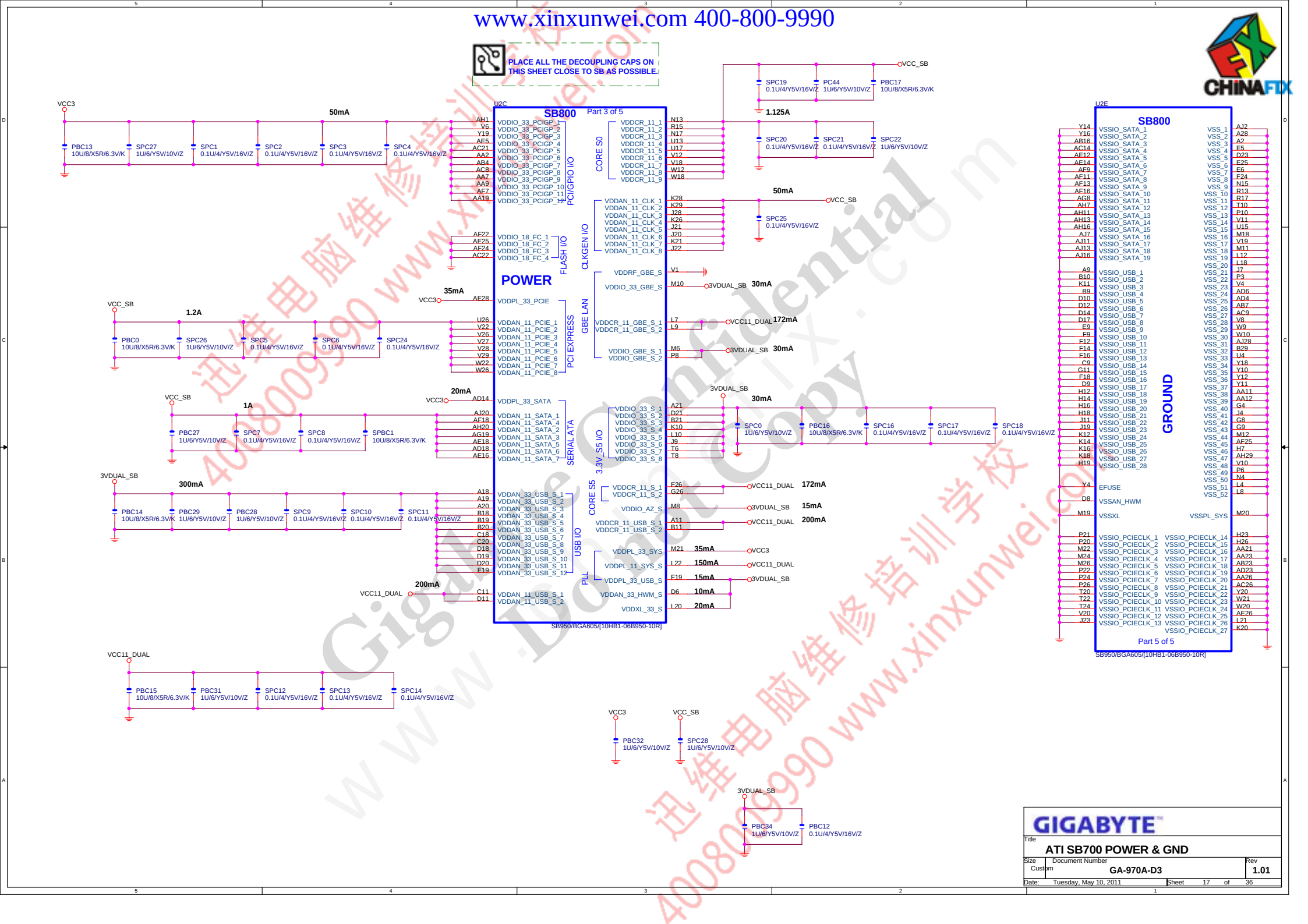
-SPI_HOLD0	PR77	1K/4/1
-BIOS_WP	PR78	1K/4/1
-ITE_SPI_CS	PR79	330/4
-ITE_SPI_CS1	PR80	330/4

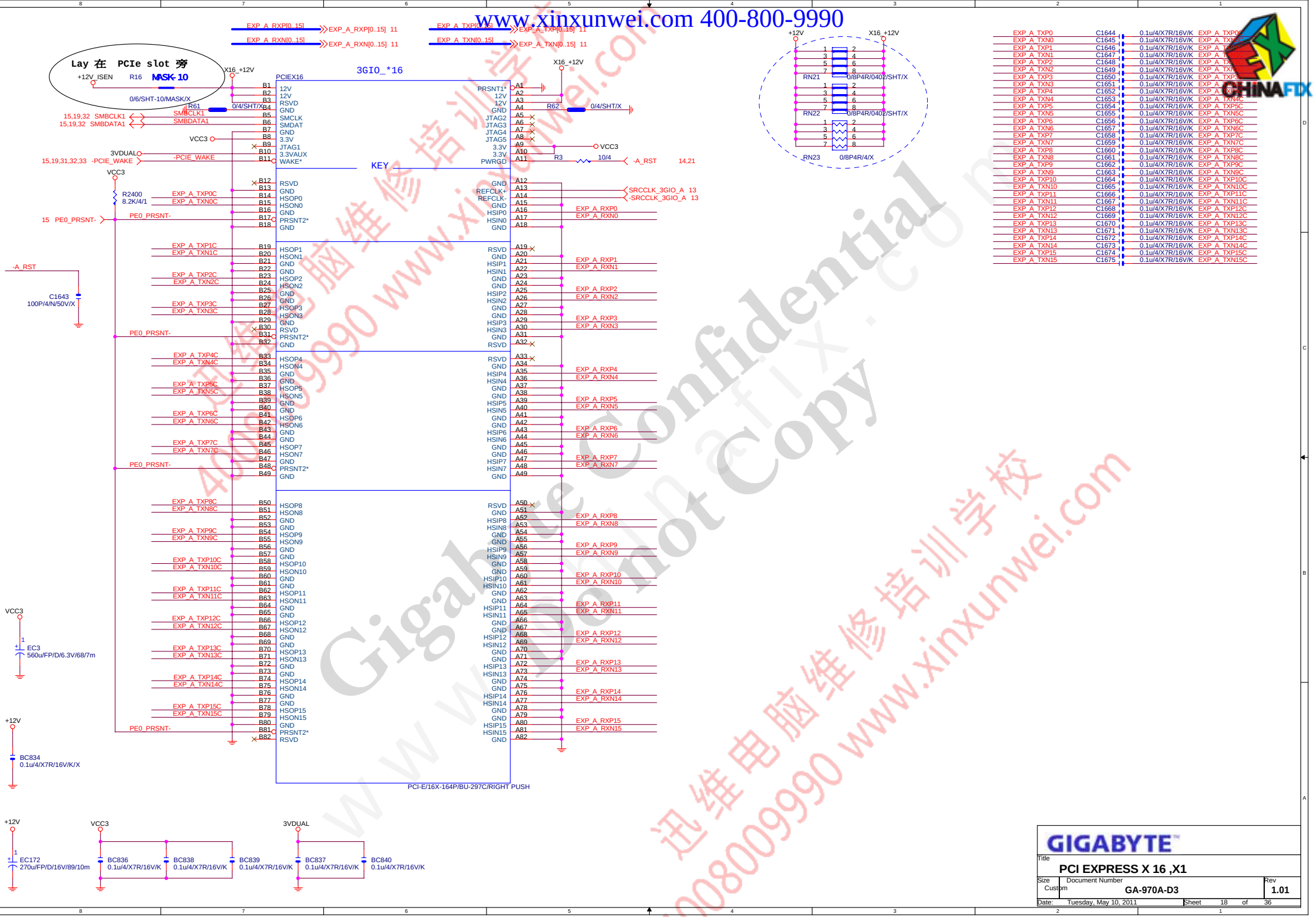
GIGABYTE

Title: ATI SB700 SATA/IDE/HWM/SPI

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 16 of 36





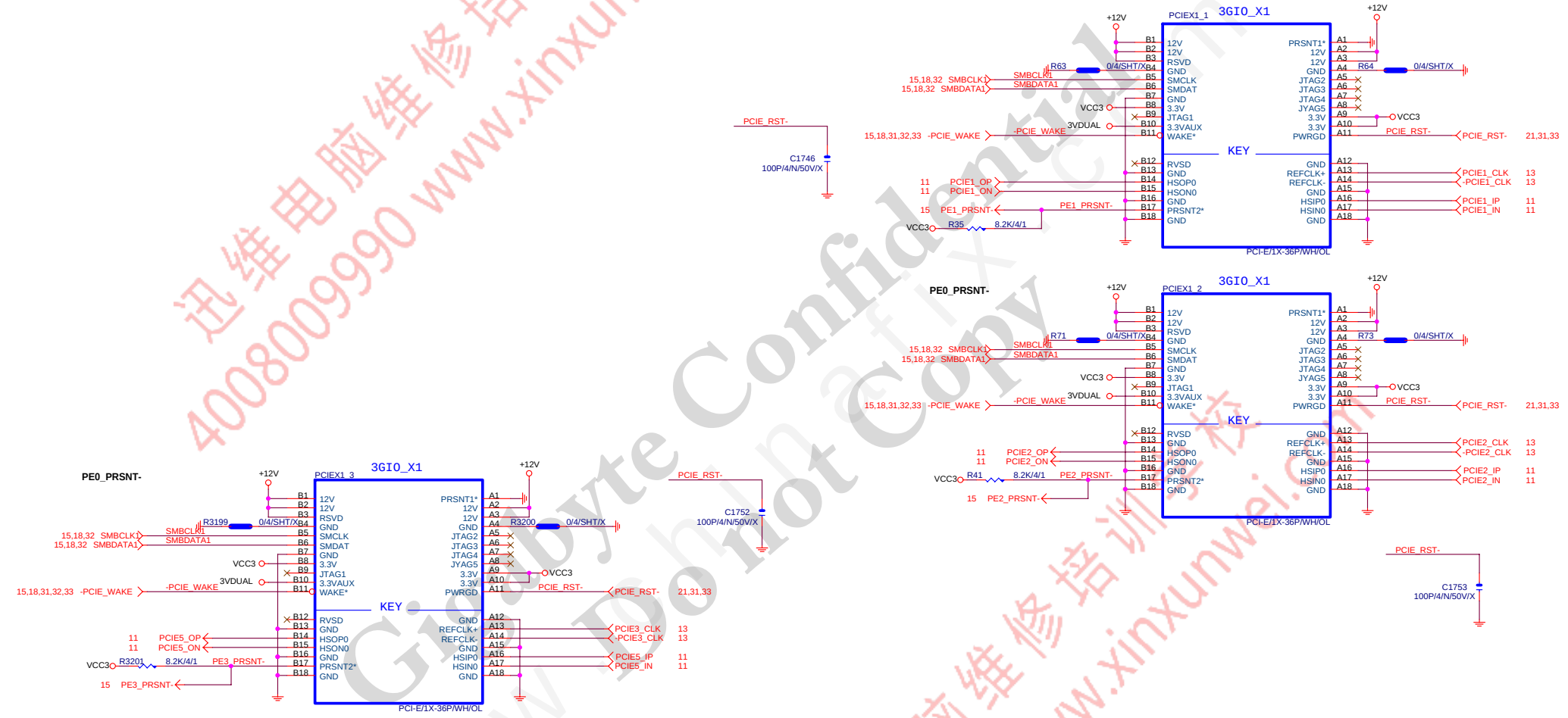
EXP_A_TXP0	C1644	0.1u/4/X7R/16V/K EXP_A_TXP0C
EXP_A_TXN0	C1645	0.1u/4/X7R/16V/K EXP_A_TXN0C
EXP_A_TXP1	C1646	0.1u/4/X7R/16V/K EXP_A_TXP1C
EXP_A_TXN1	C1647	0.1u/4/X7R/16V/K EXP_A_TXN1C
EXP_A_TXP2	C1648	0.1u/4/X7R/16V/K EXP_A_TXP2C
EXP_A_TXN2	C1649	0.1u/4/X7R/16V/K EXP_A_TXN2C
EXP_A_TXP3	C1650	0.1u/4/X7R/16V/K EXP_A_TXP3C
EXP_A_TXN3	C1651	0.1u/4/X7R/16V/K EXP_A_TXN3C
EXP_A_TXP4	C1652	0.1u/4/X7R/16V/K EXP_A_TXP4C
EXP_A_TXN4	C1653	0.1u/4/X7R/16V/K EXP_A_TXN4C
EXP_A_TXP5	C1654	0.1u/4/X7R/16V/K EXP_A_TXP5C
EXP_A_TXN5	C1655	0.1u/4/X7R/16V/K EXP_A_TXN5C
EXP_A_TXP6	C1656	0.1u/4/X7R/16V/K EXP_A_TXP6C
EXP_A_TXN6	C1657	0.1u/4/X7R/16V/K EXP_A_TXN6C
EXP_A_TXP7	C1658	0.1u/4/X7R/16V/K EXP_A_TXP7C
EXP_A_TXN7	C1659	0.1u/4/X7R/16V/K EXP_A_TXN7C
EXP_A_TXP8	C1660	0.1u/4/X7R/16V/K EXP_A_TXP8C
EXP_A_TXN8	C1661	0.1u/4/X7R/16V/K EXP_A_TXN8C
EXP_A_TXP9	C1662	0.1u/4/X7R/16V/K EXP_A_TXP9C
EXP_A_TXN9	C1663	0.1u/4/X7R/16V/K EXP_A_TXN9C
EXP_A_TXP10	C1664	0.1u/4/X7R/16V/K EXP_A_TXP10C
EXP_A_TXN10	C1665	0.1u/4/X7R/16V/K EXP_A_TXN10C
EXP_A_TXP11	C1666	0.1u/4/X7R/16V/K EXP_A_TXP11C
EXP_A_TXN11	C1667	0.1u/4/X7R/16V/K EXP_A_TXN11C
EXP_A_TXP12	C1668	0.1u/4/X7R/16V/K EXP_A_TXP12C
EXP_A_TXN12	C1669	0.1u/4/X7R/16V/K EXP_A_TXN12C
EXP_A_TXP13	C1670	0.1u/4/X7R/16V/K EXP_A_TXP13C
EXP_A_TXN13	C1671	0.1u/4/X7R/16V/K EXP_A_TXN13C
EXP_A_TXP14	C1672	0.1u/4/X7R/16V/K EXP_A_TXP14C
EXP_A_TXN14	C1673	0.1u/4/X7R/16V/K EXP_A_TXN14C
EXP_A_TXP15	C1674	0.1u/4/X7R/16V/K EXP_A_TXP15C
EXP_A_TXN15	C1675	0.1u/4/X7R/16V/K EXP_A_TXN15C

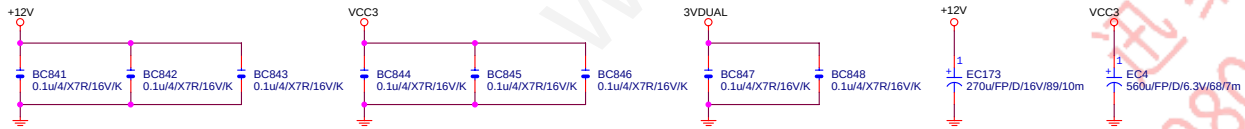
GIGABYTE

Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 18 of 36





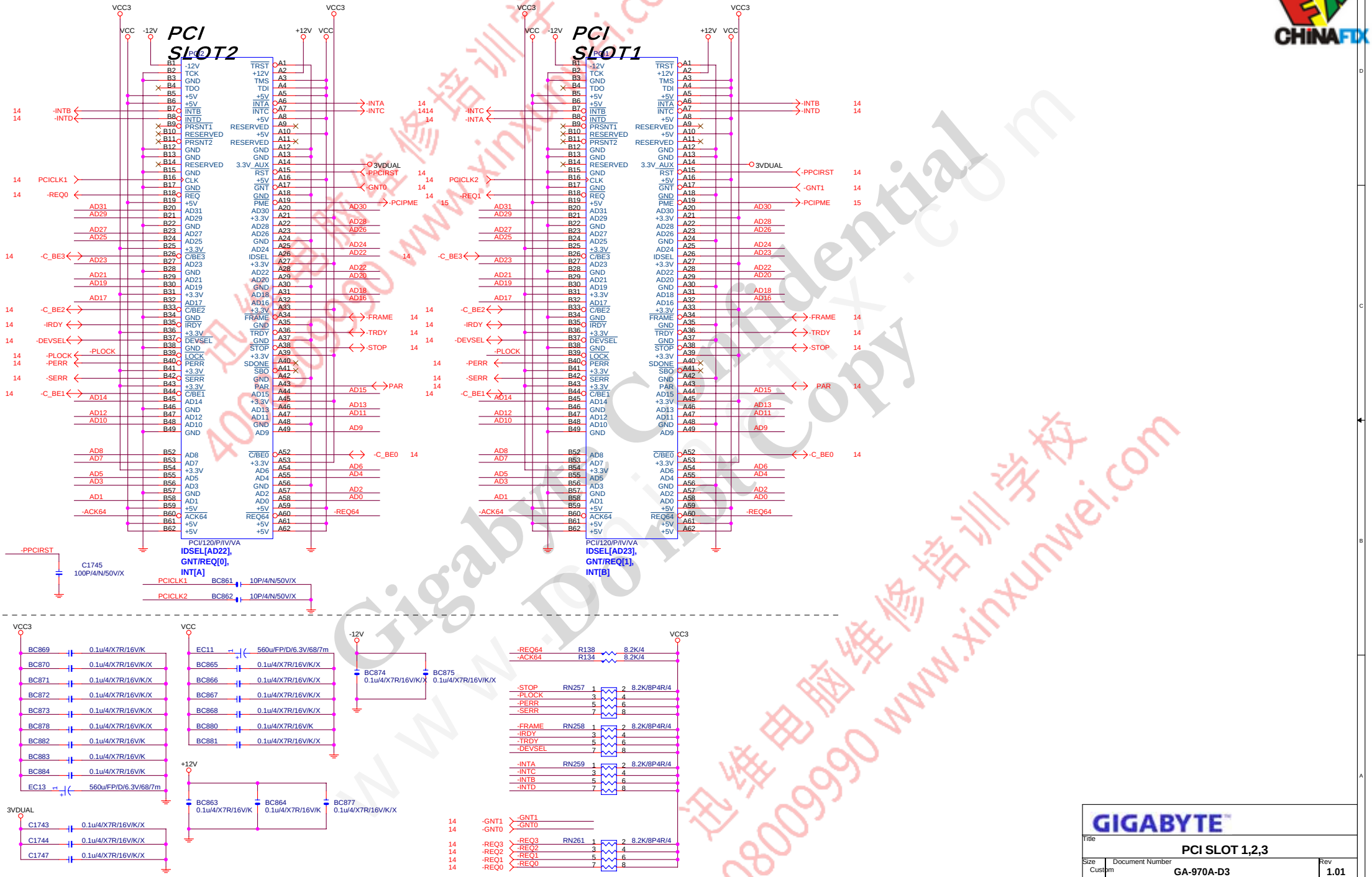
GIGABYTE

Title: PCI_E x8 ,PCI_E x1 SLOT 1,2

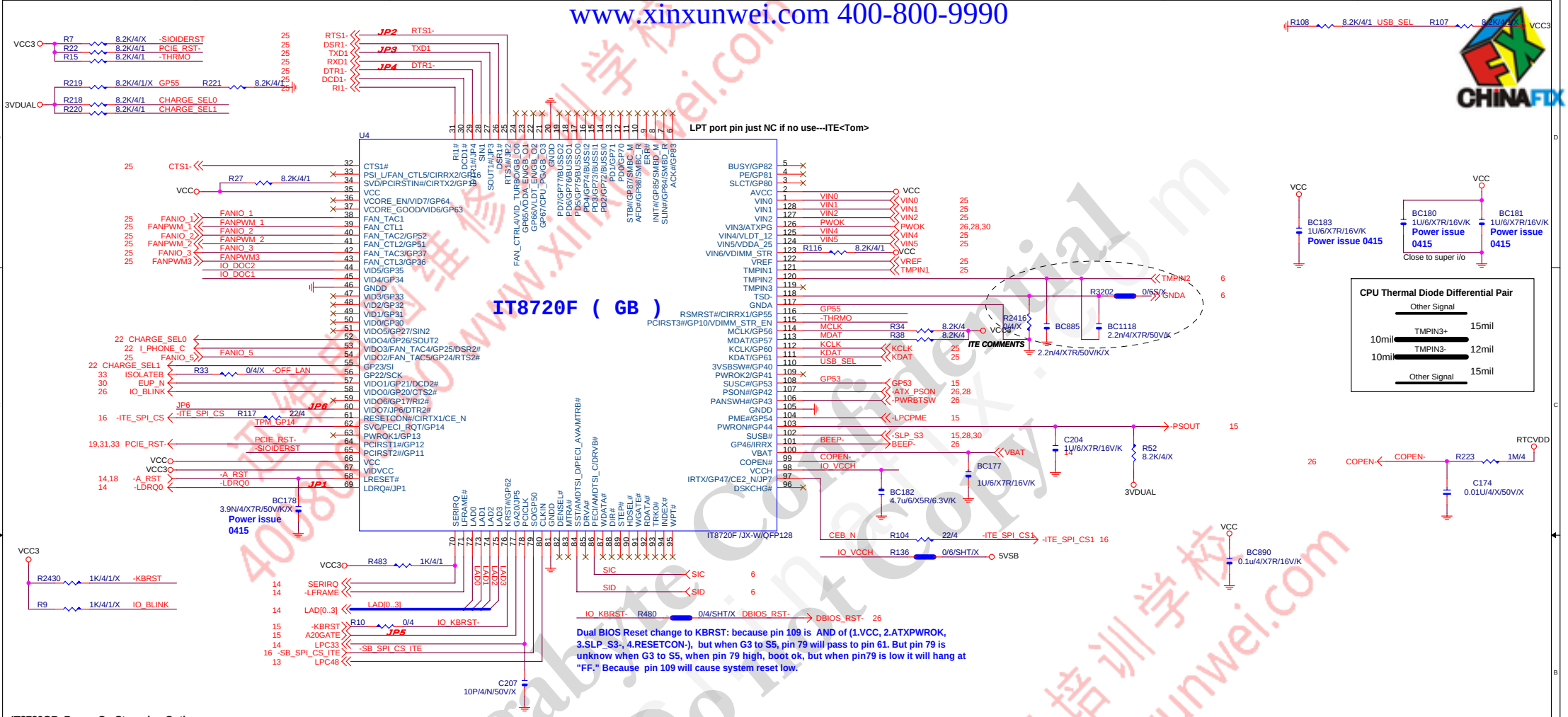
Size	Document Number	Rev
Custom	GA-970A-D3	1.01

Date: Tuesday, May 10, 2011 Sheet 19 of 36

PCI SLOT 1,2



Title	PCI SLOT 1,2,3		
Size: Custom	Document Number: GA-970A-D3		Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 20 of 36		

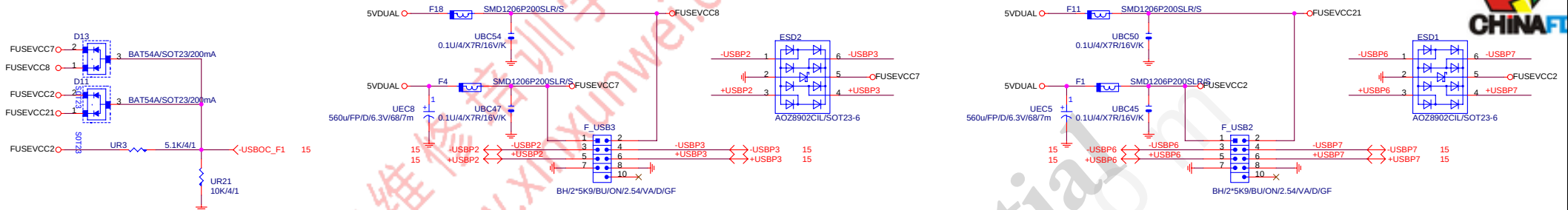


IT8720GB Power On Strapping Options

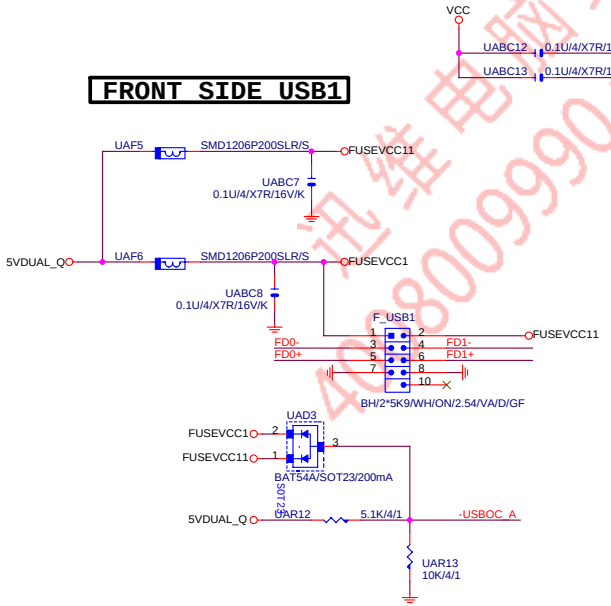
	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

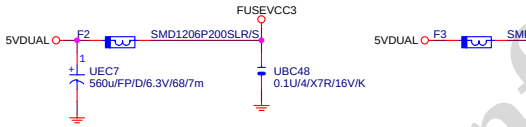
Title	ITE 8720 JX LPC IO ,Dual-BIOS ,TPM
Size	Custom
Document Number	GA-970A-D3
Rev	1.01
Date:	Tuesday, May 10, 2011
Sheet	21 of 36

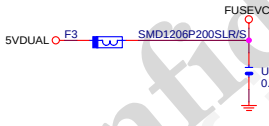
FRONT_SIDE_USB2

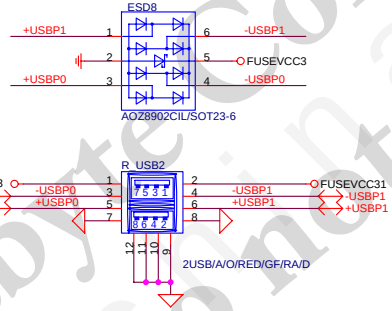


FRONT_SIDE_USB1

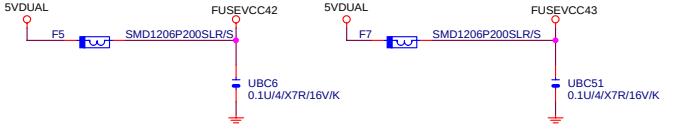


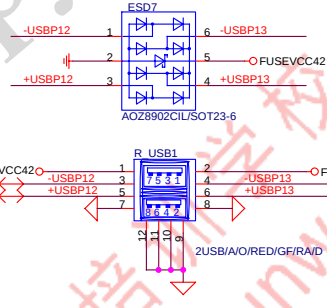


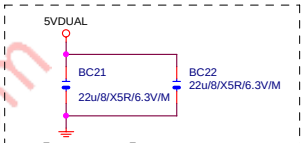


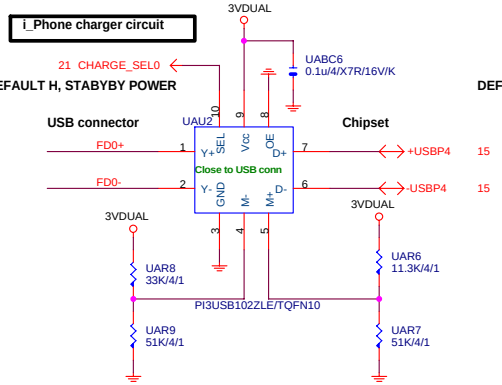


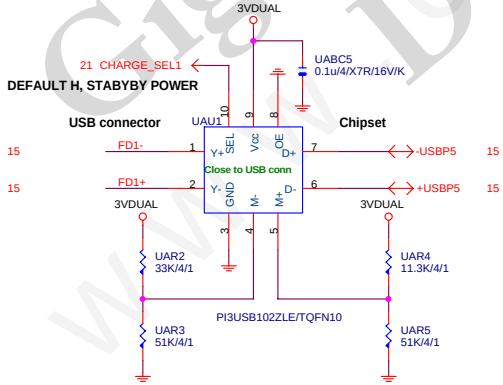
REAR_USB

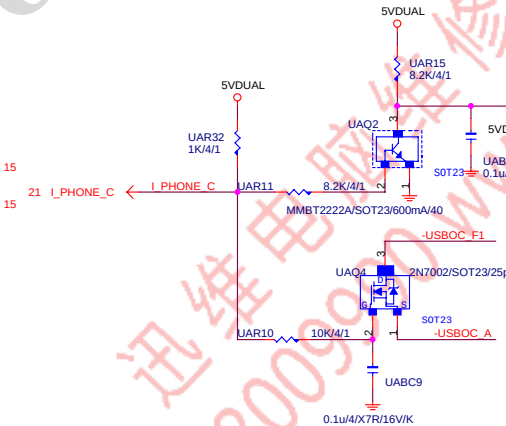


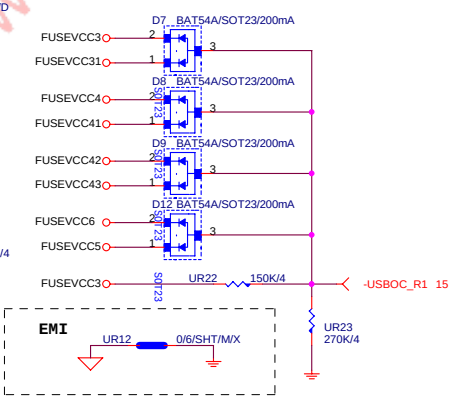








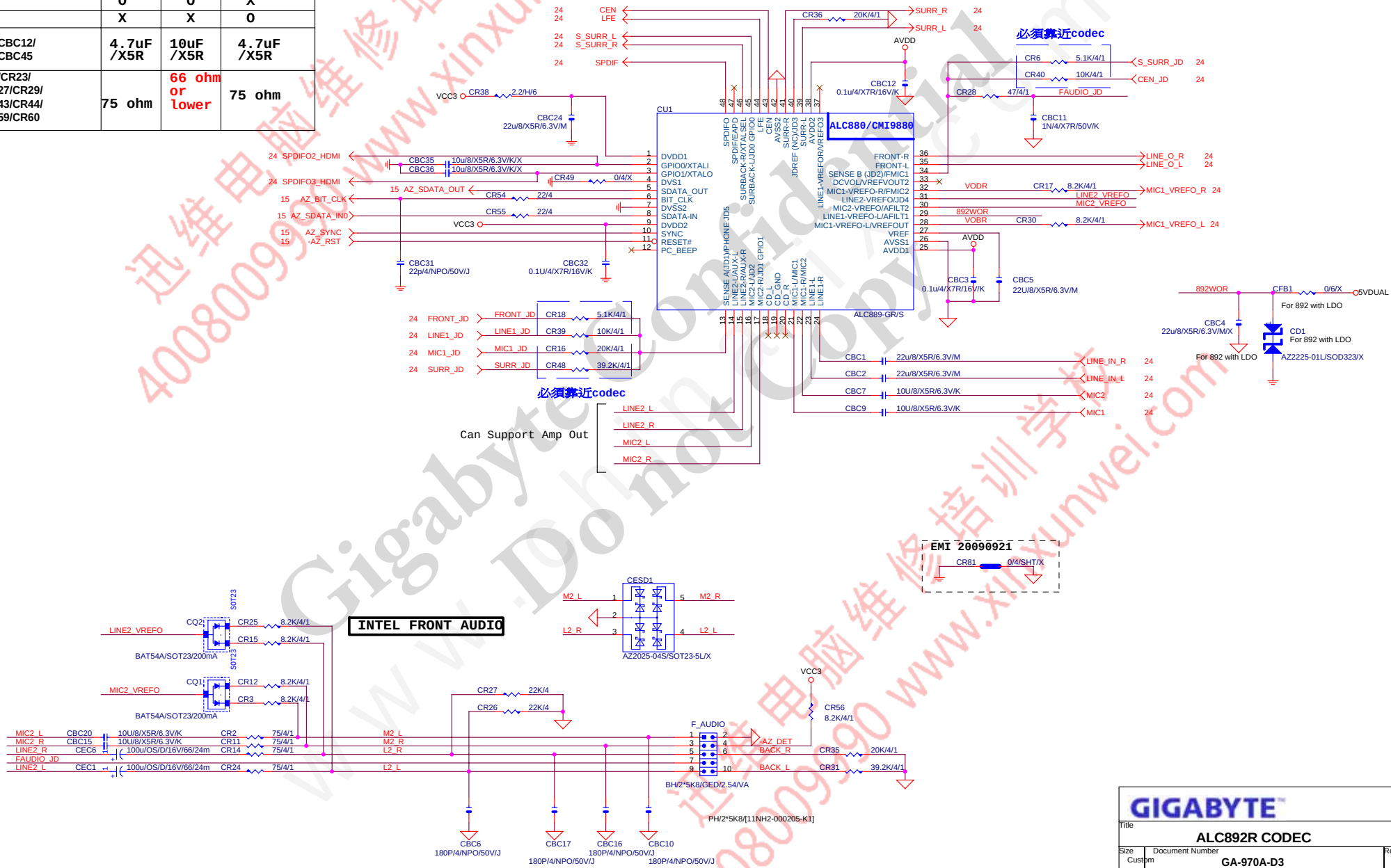




GIGABYTE			
Title: COM/LPT/F_USB/I_PWR			
Size: Custom	Document Number: GA-970A-D3		Rev: 1.01
Date: Tuesday, May 10, 2011		Sheet 22 of 36	

AZALIA CODEC *ALC892/ALC889/ Colay*

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



GIGABYTE

Title: ALC892R CODEC

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.01

Date: Tuesday, May 10, 2011 | Sheet 23 of 36

CR33 0/6/X

For ESD PROTECT DIODE

5VDUAL — CD4 CD4148WP/1206/300mA — AVDD — CBC8 22u/8/X5R/6.3V/M — CD2 AZ2225-01L/SOD323 — CBC21 1U/6/X7R/16V/K

+12V — CD3 CD4148WP/1206/300mA — CQ3 78L05/SOT89/0.1A

SPDIF

23 SPDIFO3_HDMI — CR52 0/4/X
23 SPDIFO2_HDMI — CR53 0/4

For HDMI SPDIF

SPDIF_O — CBC37 100p/4/NPO/50V/J — SPDIF_O — PH/1*2/BK/2.54/VA/D

23 SPDIF — FUSEVCC3 — OPTICAL — FR/5P/BK/T/D/S(GY)

CESD2: AJ_A2, AJ_B2, AJ_C2, AJ_C5 — AZ2025-04S/SOT23-5L/X
CESD4: AJ_B5, AJ_A5, BJ_C2, BJ_A2 — AZ2025-04S/SOT23-5L/X
CESD3: BJ_B5, BJ_A5, BJ_C5, BJ_B2 — AZ2025-04S/SOT23-5L/X
CESD5: SPDIF, SPDIF, SPDIF_O, SPDIF_O — AZ2025-04S/SOT23-5L/X

For Audio precision test

CBC38 2.2/4

USB_LAN — R_USB2 — R_USB1

AUDIOB

23 LINE1_JD — LINE1_JD — AJ_A5 — AJ_A2 — LINE-IN
23 FRONT_JD — FRONT_JD — AJ_B5 — AJ_B2 — LINE-OUT
23 MIC1_JD — MIC1_JD — AJ_C5 — AJ_C2 — MIC-IN

BLUE LINE-IN
GREEN LINE-OUT
PINK MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/B/[11NR6-403006-01_11NR6-403006-02]
3RJ+15F/[11NR6-403004-11]

AUDIOA

23 CEN_JD — CEN_JD — BJ_B5 — BJ_B2 — REAR
23 SURR_JD — SURR_JD — BJ_C5 — BJ_C2 — CEN
23 S_SURR_JD — S_SURR_JD — BJ_A5 — BJ_A2 — FO_SIDE

Orange CEN/LFE

ALC880 - SURROUND
CMI9880 - Back SURR

Black Back side Speaker Azalia Port G

Gray Left & Right Side Speaker

CMI9880 - Side SURR

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

A3RJ/13P/OBG/[11NR6-403006-71]
3RJ+15F/[11NR6-403004-31]

LINE OUT FRONT OUT

23 LINE_O_R — CEC2 100u/OS/D/16V/66/24m — CR7 62/4 — AJ_B5
23 LINE_O_L — CEC3 100u/OS/D/16V/66/24m — CR9 62/4 — AJ_B2

CR10 22K/4 CBC23 180P/4/NPO/50V/J — CR8 22K/4 CBC26 180P/4/NPO/50V/J

LINE-IN

23 LINE_IN_R — CR5 62/4 — AJ_A5
23 LINE_IN_L — CR13 62/4 — AJ_A2

CBC18 180P/4/NPO/50V/J — CBC27 180P/4/NPO/50V/J

MIC

23 MIC2 — CR29 62/4 — AJ_C5
23 MIC1 — CR32 62/4 — AJ_C2
23 MIC1_VREFO_R — CR37 0/4/SHT/X
23 MIC1_VREFO_L — CR34 0/4/SHT/X

CBC19 180P/4/NPO/50V/J — CBC22 180P/4/NPO/50V/J

SURROUND

23 SURR_R — CEC5 100u/OS/D/16V/66/24m — CR46 62/4 — BJ_C5
23 SURR_L — CEC7 100u/OS/D/16V/66/24m — CR19 62/4 — BJ_C2

CR20 22K/4 CBC29 180P/4/NPO/50V/J — CR45 22K/4 CBC28 180P/4/NPO/50V/J

CEN/LFE

23 LFE — CEC9 100u/OS/D/16V/66/24m — CR50 62/4 — BJ_B5
23 CEN — CEC10 100u/OS/D/16V/66/24m — CR41 62/4 — BJ_B2

CR42 22K/4 CBC25 180P/4/NPO/50V/J — CR51 22K/4 CBC34 180P/4/NPO/50V/J

SURR BACK

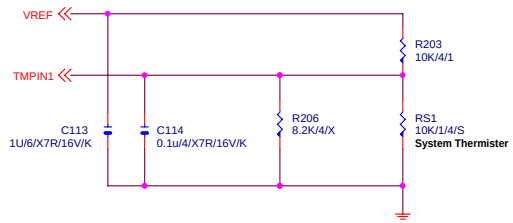
23 S_SURR_R — CEC8 100u/OS/D/16V/66/24m — CR21 62/4 — BJ_A5
23 S_SURR_L — CEC4 100u/OS/D/16V/66/24m — CR47 62/4 — BJ_A2

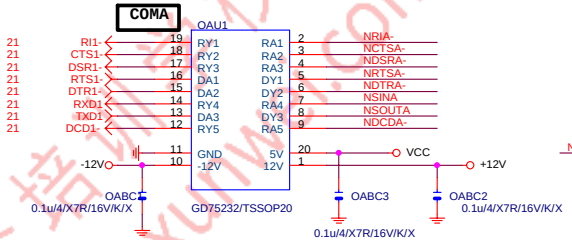
CR43 22K/4 CBC33 180P/4/NPO/50V/J — CR22 22K/4 CBC30 180P/4/NPO/50V/J

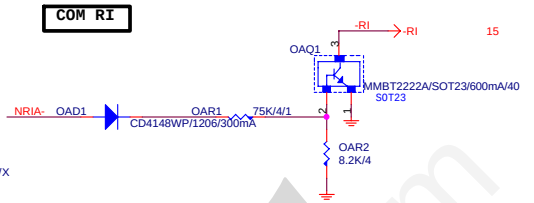
GIGABYTE

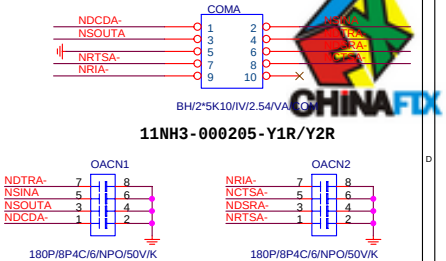
Title: AUDIO JACK
Size: Custom
Document Number: GA-970A-D3
Rev: 1.01
Date: Tuesday, May 10, 2011
Sheet 24 of 36

Hardware Monitor circuits

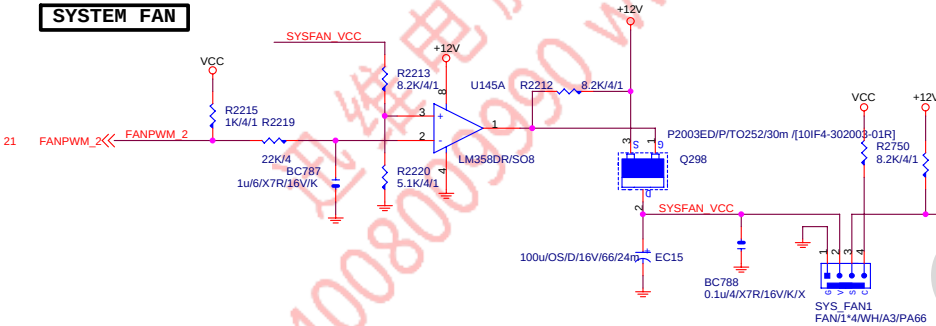


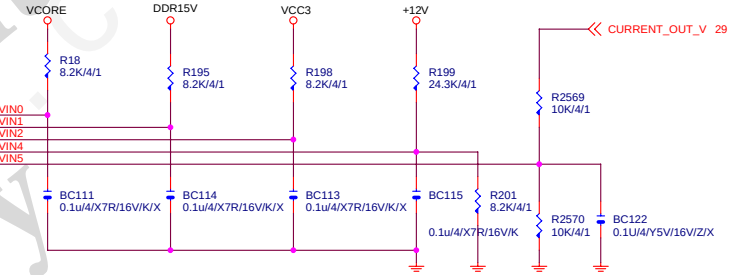




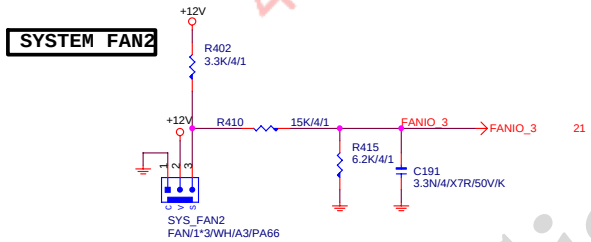


SYSTEM FAN

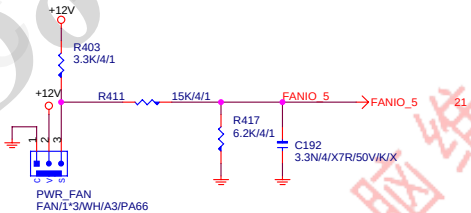




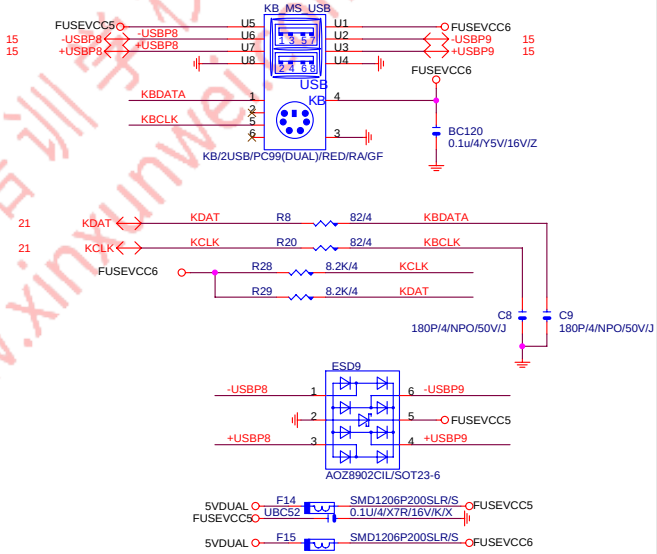
SYSTEM FAN2



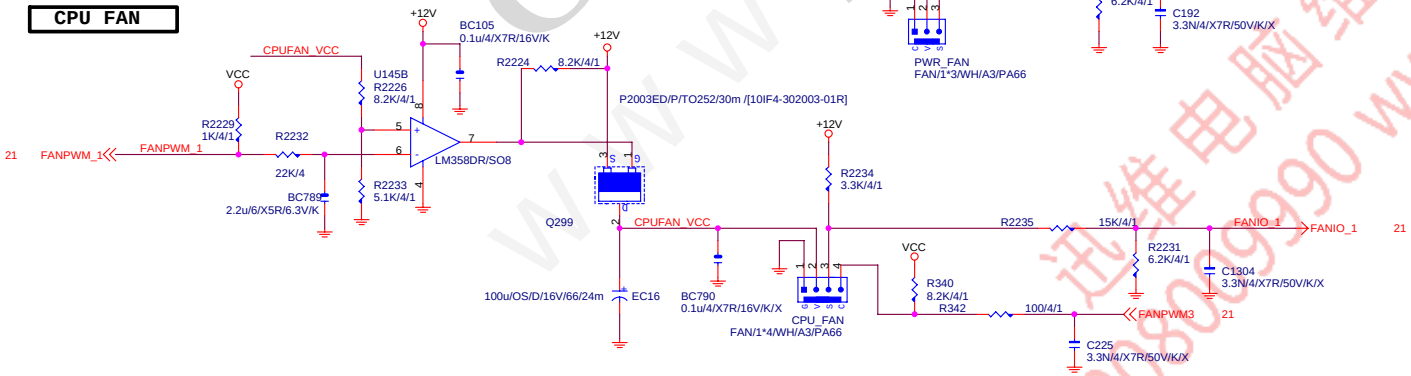
POWER FAN



KB & USB



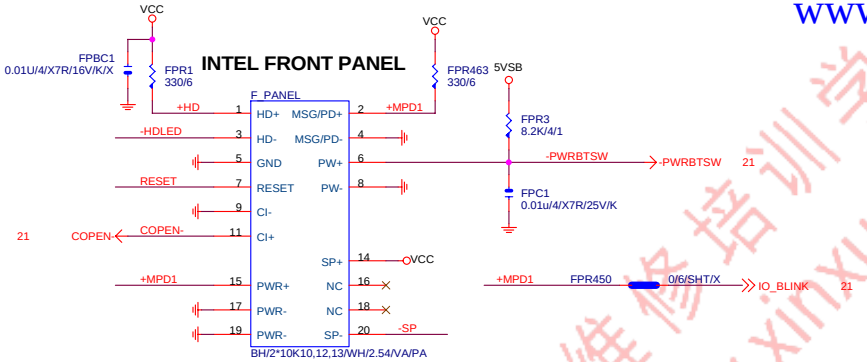
CPU FAN

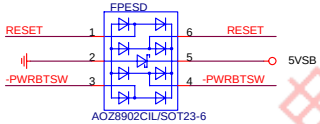


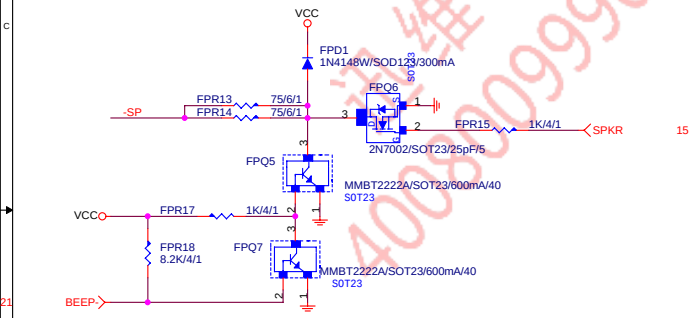
GIGABYTE

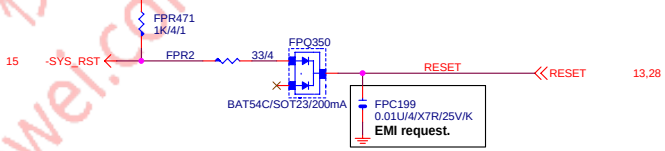
Title	FAN/HWMO KB/MS
Size: Custom	Document Number: GA-970A-D3
Rev	1.01
Date: Tuesday, May 10, 2011	Sheet 25 of 36

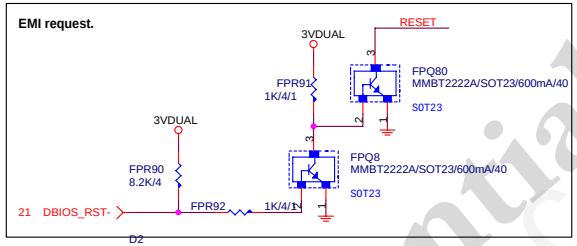
INTEL FRONT PANEL

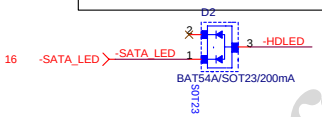


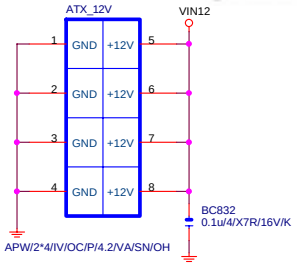




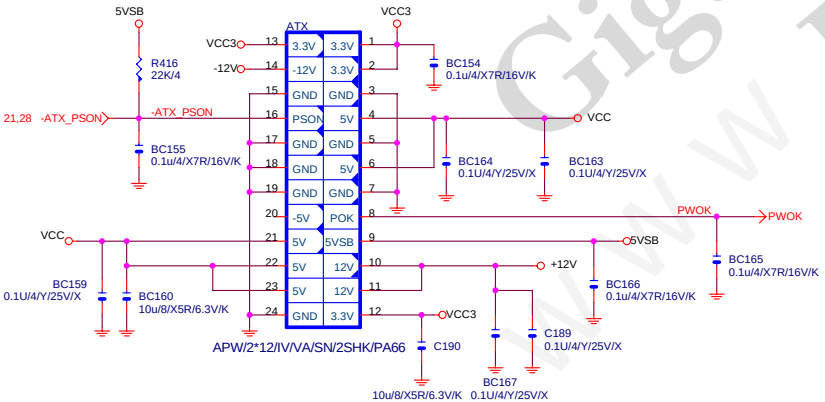


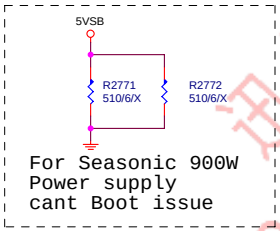


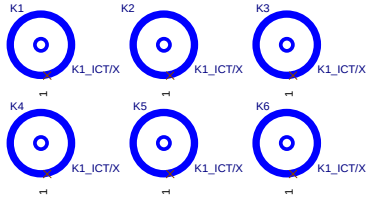


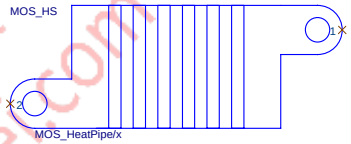


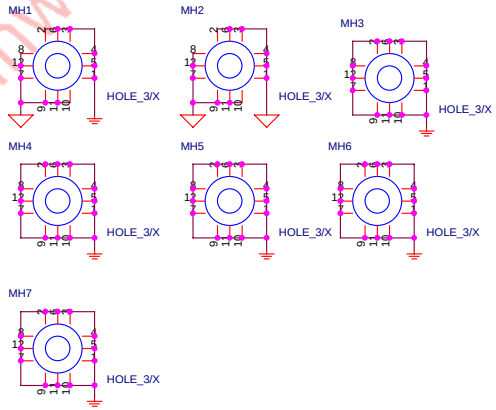
ATX POWER CONNECTOR











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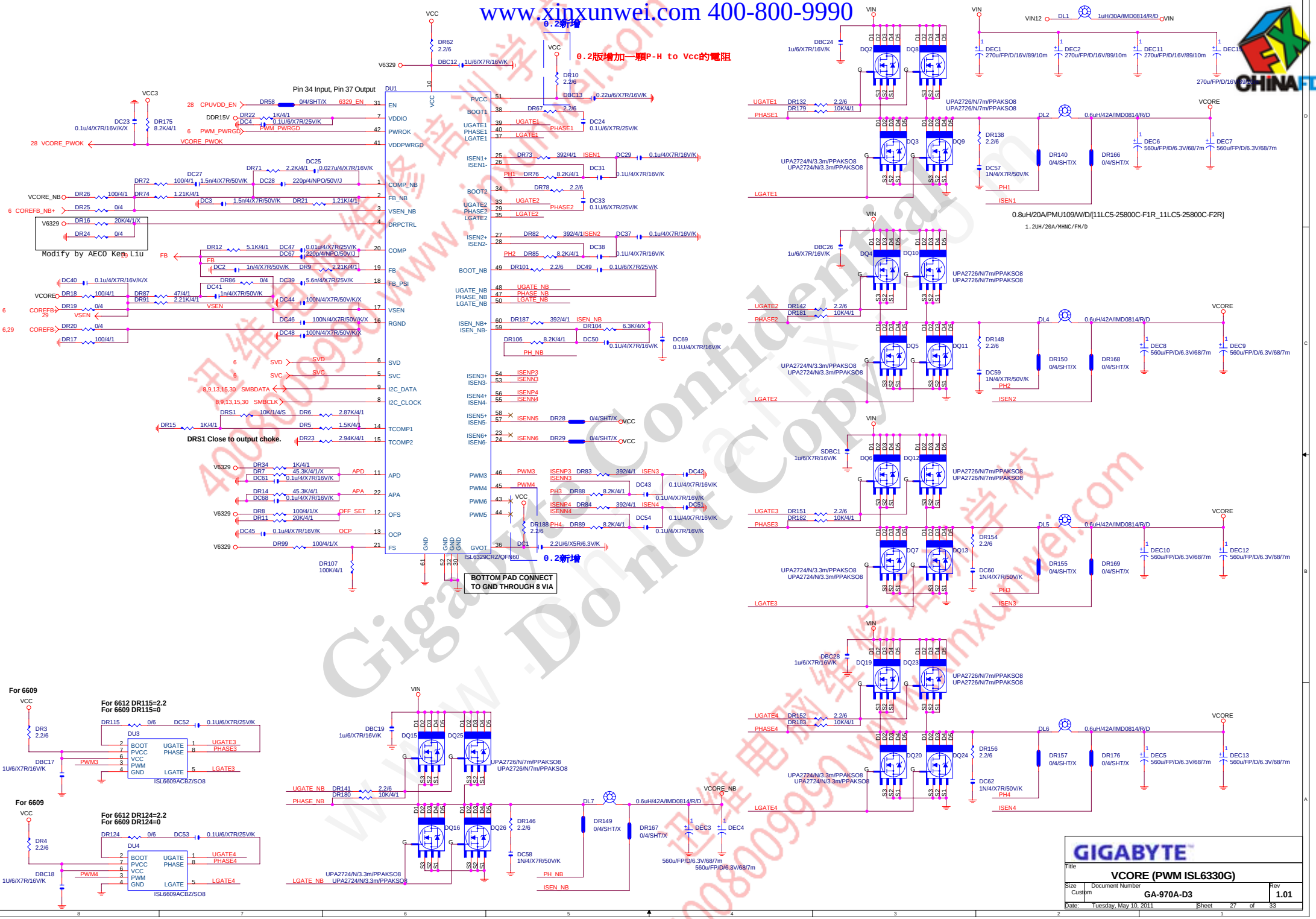
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 26 of 36	



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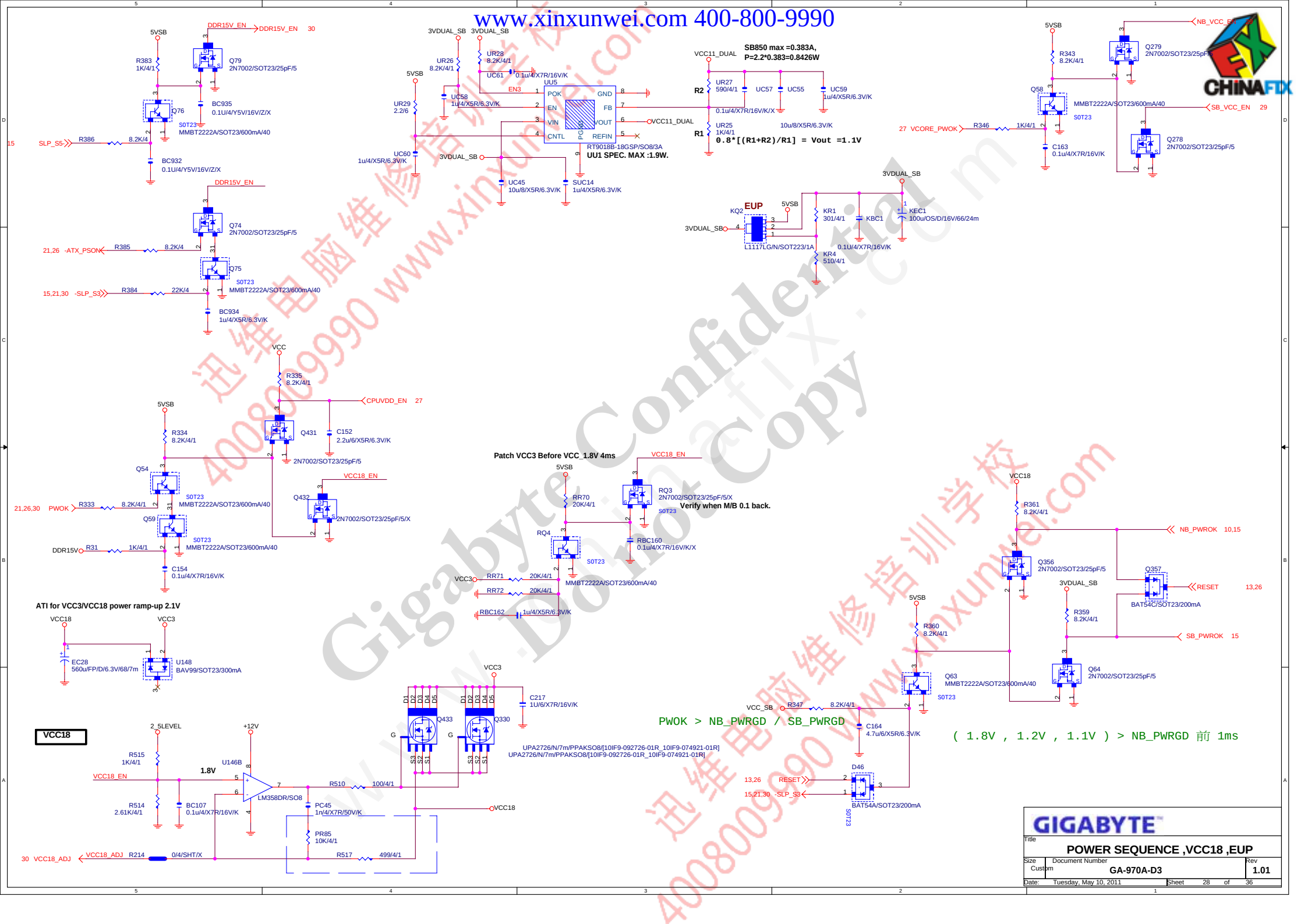
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01	
Date: Tuesday, May 10, 2011	Sheet 27 of 33		



GIGABYTE

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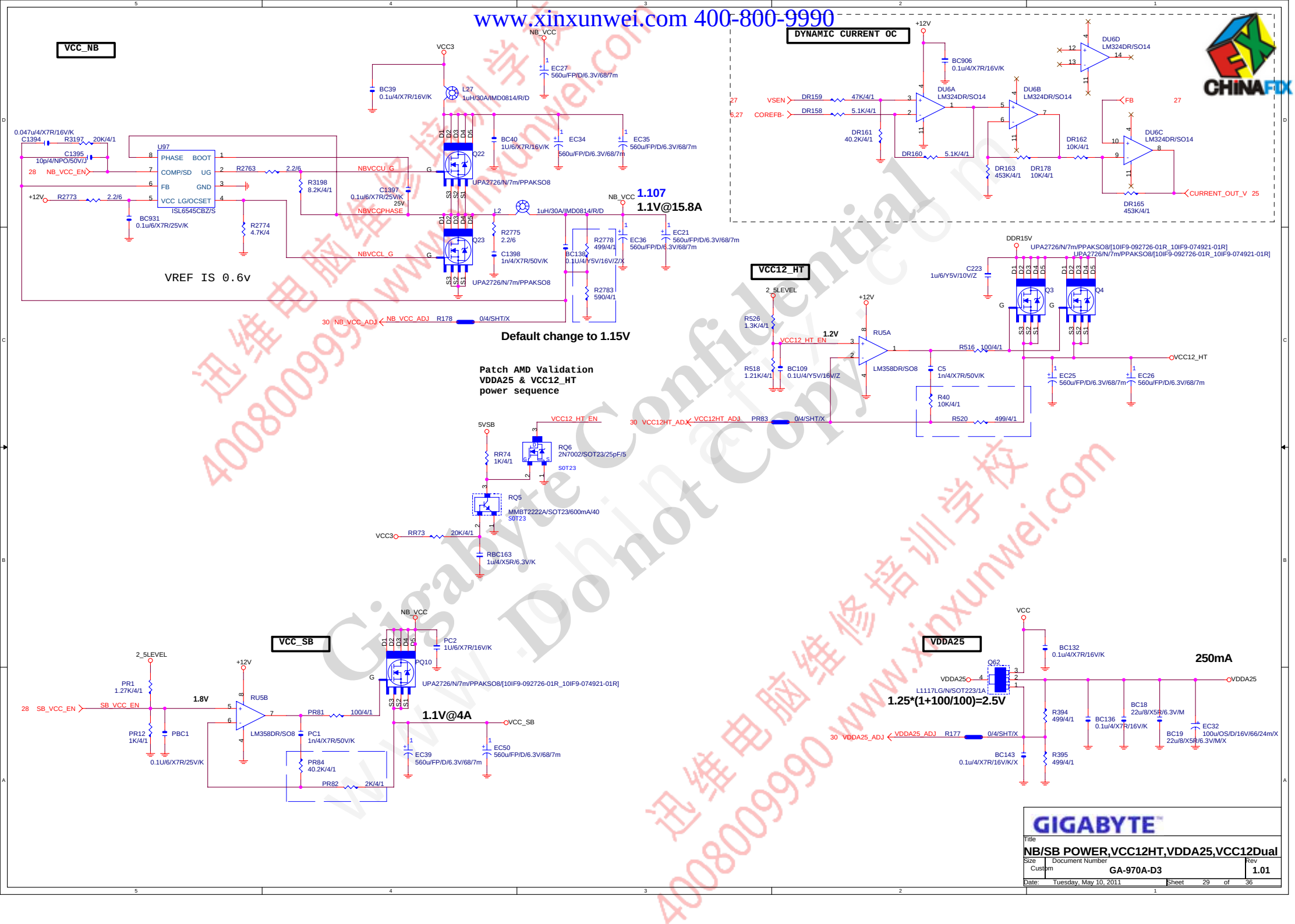
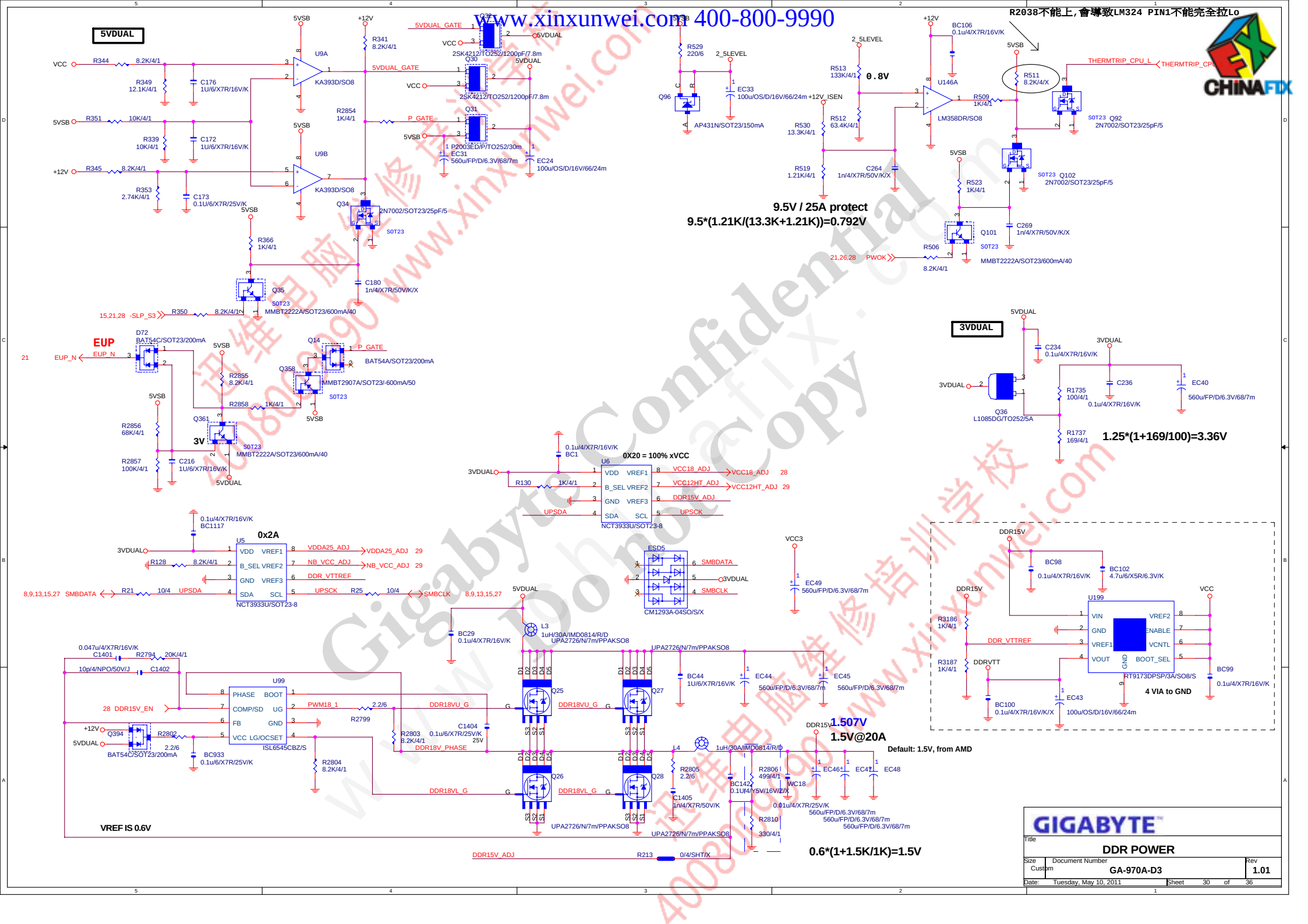
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 28 of 36	



R2038不能上，會導致LM324 PIN1不能完全拉Lo



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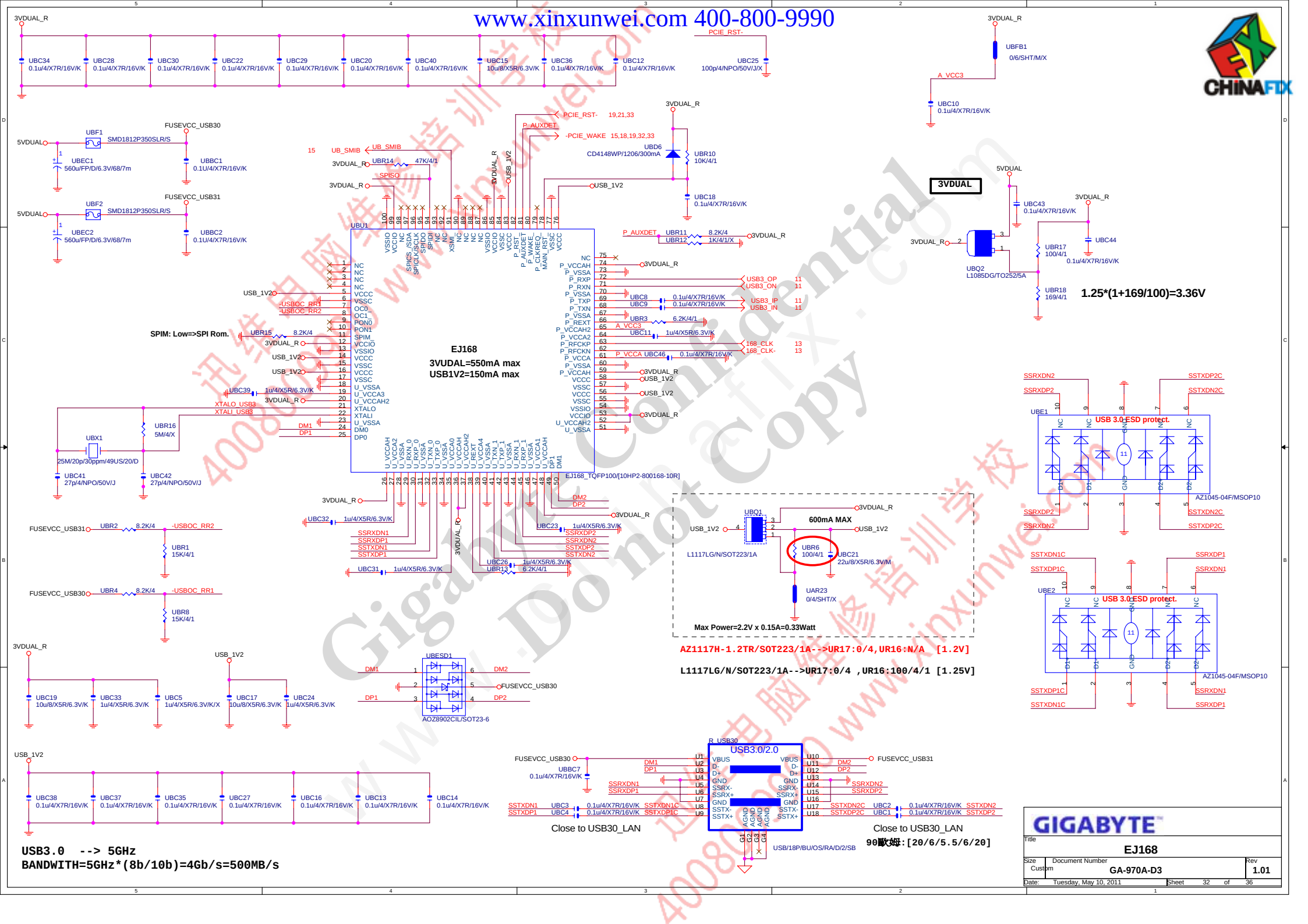
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 30 of 36	



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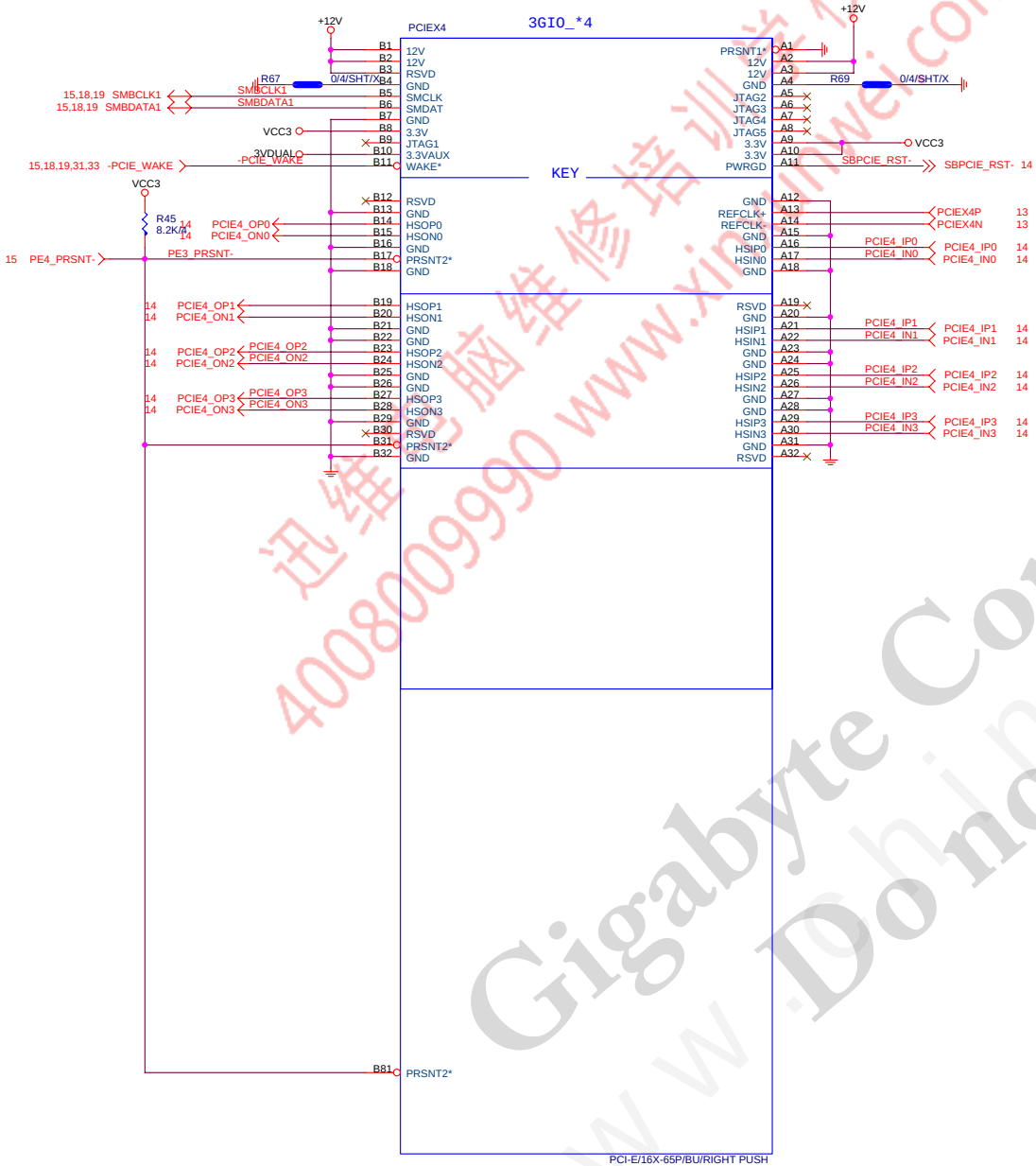
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 32 of 36	



GIGABYTE		
Title	JMB362	
Size: Custom	Document Number: GA-970A-D3	Rev: 1.01
Date: Tuesday, May 10, 2011	Sheet 33 of 36	

PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內

LA_VDD33

LAR10 1K/4/1

LAR12 2.49K/4/1

LAU1

RTL8111E-VL-CG/QFN48/S

Data trace(MDI0~3)的+/-線長需等長,誤差在5mils以內,Pair跟Pair之間線長,最長跟最短data trace請勿超過800 mil

0.2版要修改

XTAL1 XTALO_P

LAX1 25M/20p/30ppm/49US/20/D

LAC5 27p/4/NPO/50V/J

LAC6 27p/4/NPO/50V/J

Pin34/35(VDDREG) 接到3VDUAL的trace 建議寬度大於 40mil

LAR9 1/6

LABC12 LABC13 0.1u/4/X7R/16V/K 4.7u/6/X5R/6.3V/K

LAR7 LAR6 LAR8 8.2K/4

LAR4 1K/4/1

LAR5 15K/4/1

ISOLATEB 21

PCIE_WAKE 15,18,19,31,32

PCIE_RST- 19,21,31

LABC4 100p/4/NPO/50V/J/X

LAR2 LAR1 8.2K/4

ML_OP ML_ON SRCCLK_LAN -SRCCLK_LAN

ML_IP ML_IN LC3 LC4 0.1u/4/X7R/16V/K

CLOSE LAN CHIP 離IC近越好200mil以內

USB_LAN CONNECTOR

P35-152-19W9

YELLOW ORANGE GREEN

3VDUAL_R

LAEC1 560u/FP/D/6.3V/68/7m

LABC6 LABC16 LABC15 LABC5 LABC18 LABC14 0.1u/4/X7R/16V/K

(CLOSE LU1)

VDD10

DVDD10

LABC11 LABC10 LABC9 LABC3 LABC19 LABC17 LABC8 0.1u/4/X7R/16V/K

LAL1 4.7uH/0.8A/3225/S REGOUT

LABC20 4.7u/6/X5R/6.3V/K

LABC21 LABC1 0.1u/4/X7R/16V/K

LABC2 1u/4/X5R/6.3V/K

建議使用X5R電容

USB_LAN

RTL8101E:LR38/LC5/LR43/LC6-->O

RTL8111C:LC6-->O

RTL8102E:LC5/LC6-->O

FOR EMI

LABC22 0.01u/4/X7R/25V/K

LABC25 0.01u/4/X7R/25V/K

USB_LAN

UP

DOWN

USB+LAN/1G/GO,Y/OS/RA/D/1/RED

LED_ACT_TXRX LED_D2 LED_LINK100 LED_LINK1000

LAR13 150/4/1

LAFB2 0/6/SHT/M/X

LABC24 0.1u/4/Y5V/16V/Z/X

-USBP10 +USBP10 -USBP11 +USBP11

FUSEVCC4 FUSEVCC41

5VDUAL UBF3 UBF4 SMD1206P200SLR/S

UEC6 560u/FP/D/6.3V/68/7m

LABC7 LABC23 0.1U/4/X7R/16V/K

UBESD3 AOZ8902CIL/SOT23-6

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

1G :USB+LAN/1G/GO,Y/OS/RA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1

EMI LR1 0/6/SHT/M/X

GIGABYTE

Title: REALTK RTL8111C

Size: Custom | Document Number: GA-970A-D3 | Rev: 1.01

Date: Tuesday, May 10, 2011 | Sheet 34 of 36