MS-7A78

ATX

Ver: 10

Intel -Kabylake plamform Z270

CPU:

kabylake-S

System Chipset:

Z270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:Killer E2400 colay E2500
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X8) Slot *1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 3*
*M2 * 2*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 *2*
*REAR USB2.0 *3*
REAR USB TYPE A+C

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MS-7A78..

Size	Document Description	Rev
Custom	Cover Sheet	10

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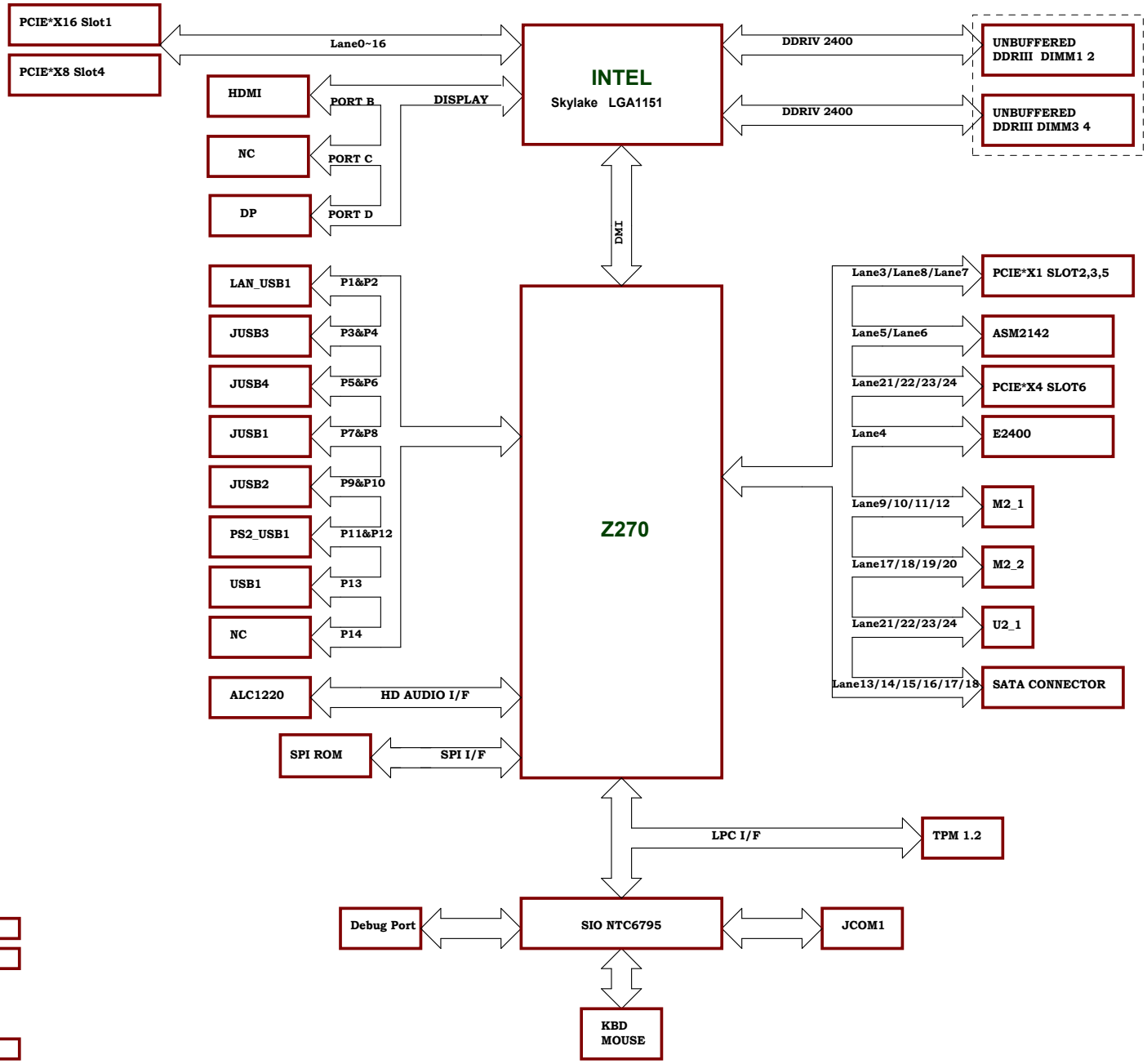
MS-7A78 Block Diagram



Slot Sequence:

- M.2
- PCIE X16
- PCIE X1
- PCIE X1
- PCIE X8
- PCIE X1 / M.2
- PCIE X4

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MS-7A78..		
Size: Custom	Document Description: Block Diagram	Rev: 10
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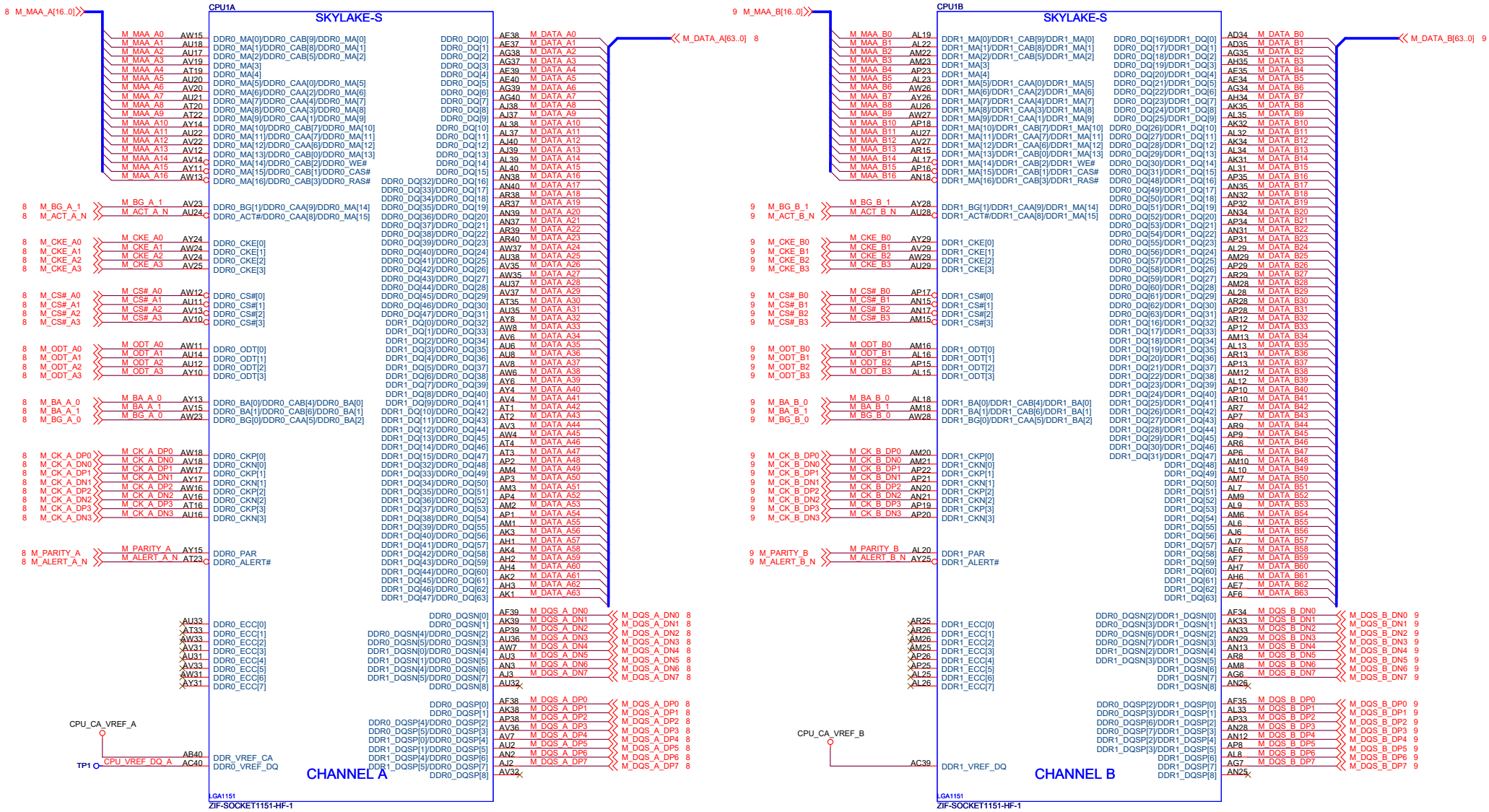

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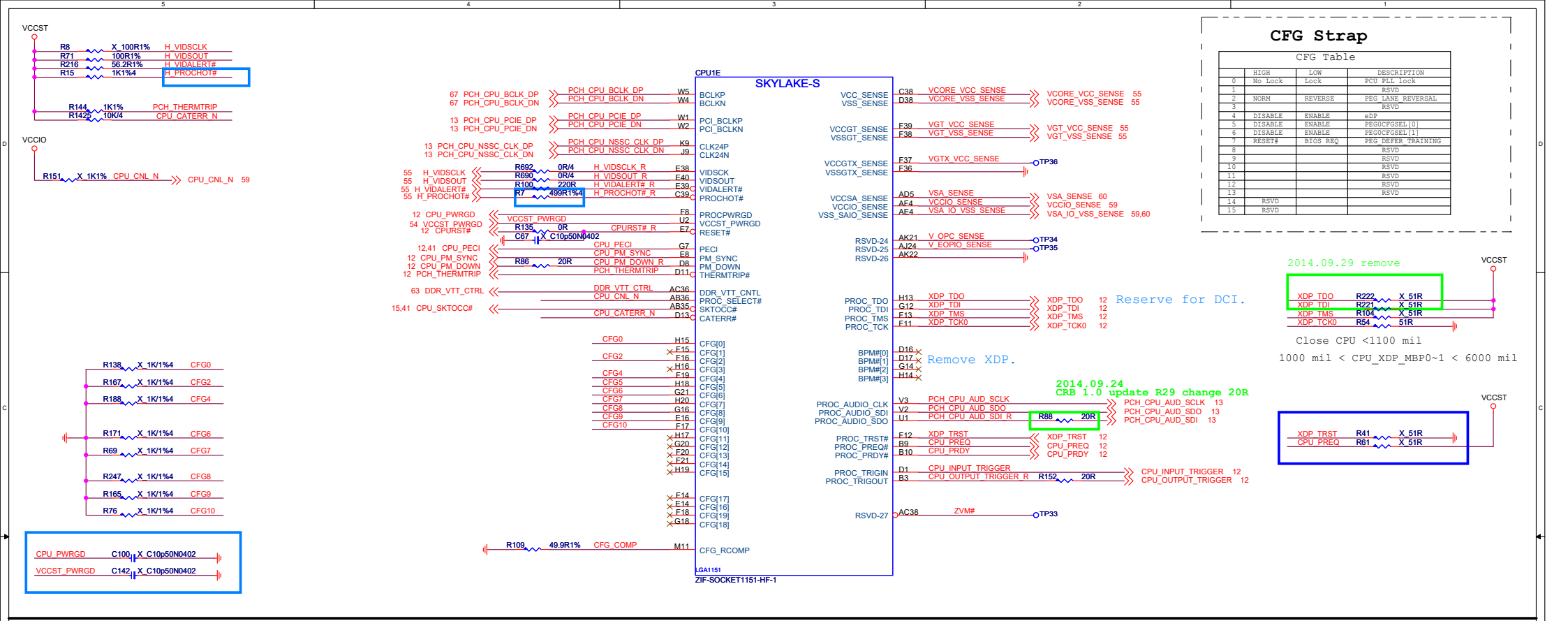
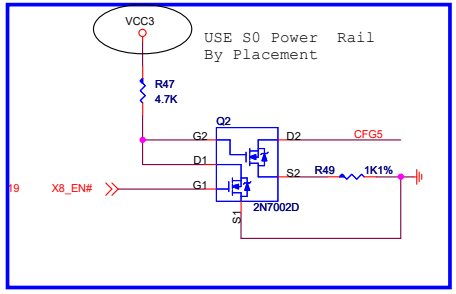
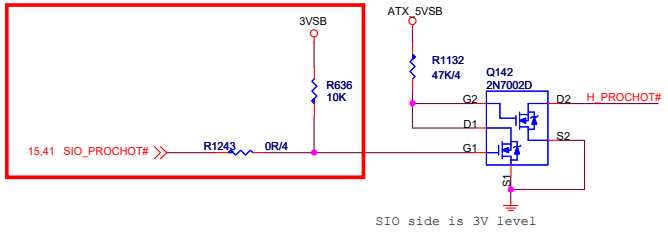


X8 Ctrl

ENABLE# X8	SLOT1	SLOT4
0	X8	X8
1	X16	X0





CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

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Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 10

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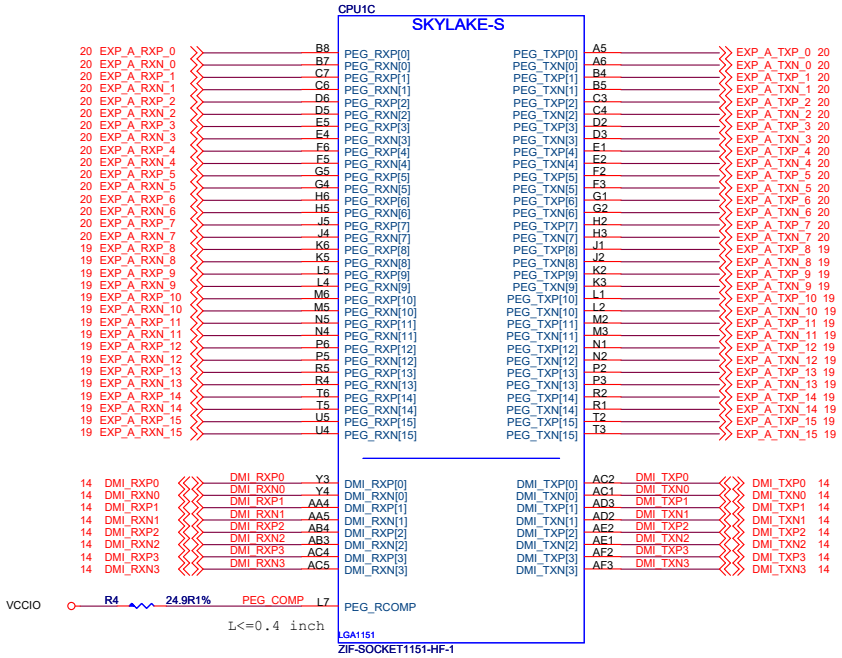

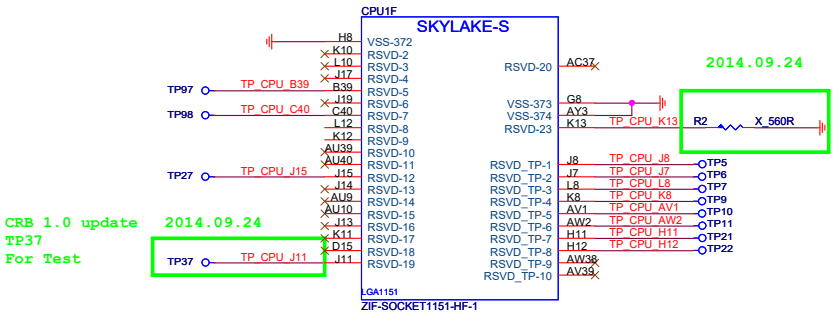

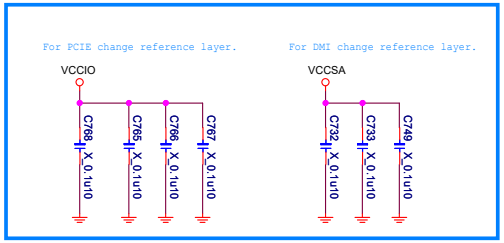

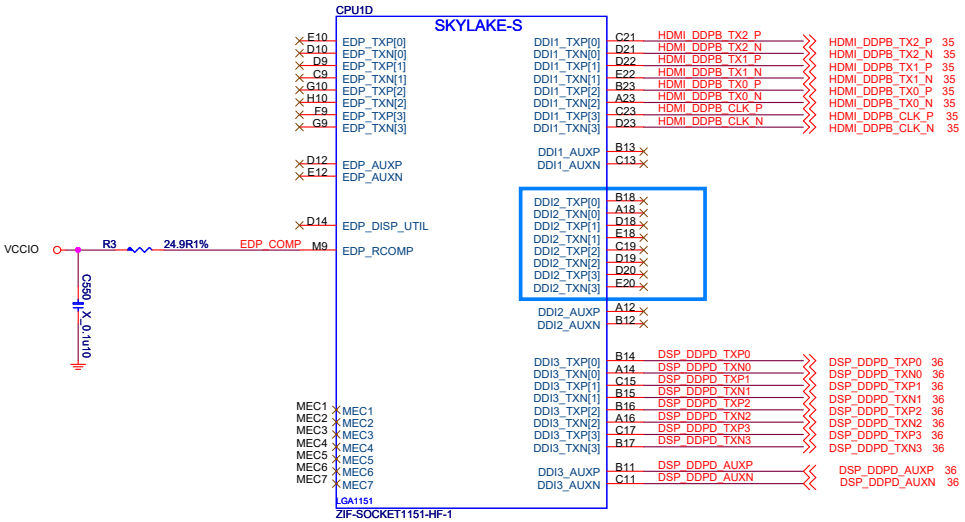

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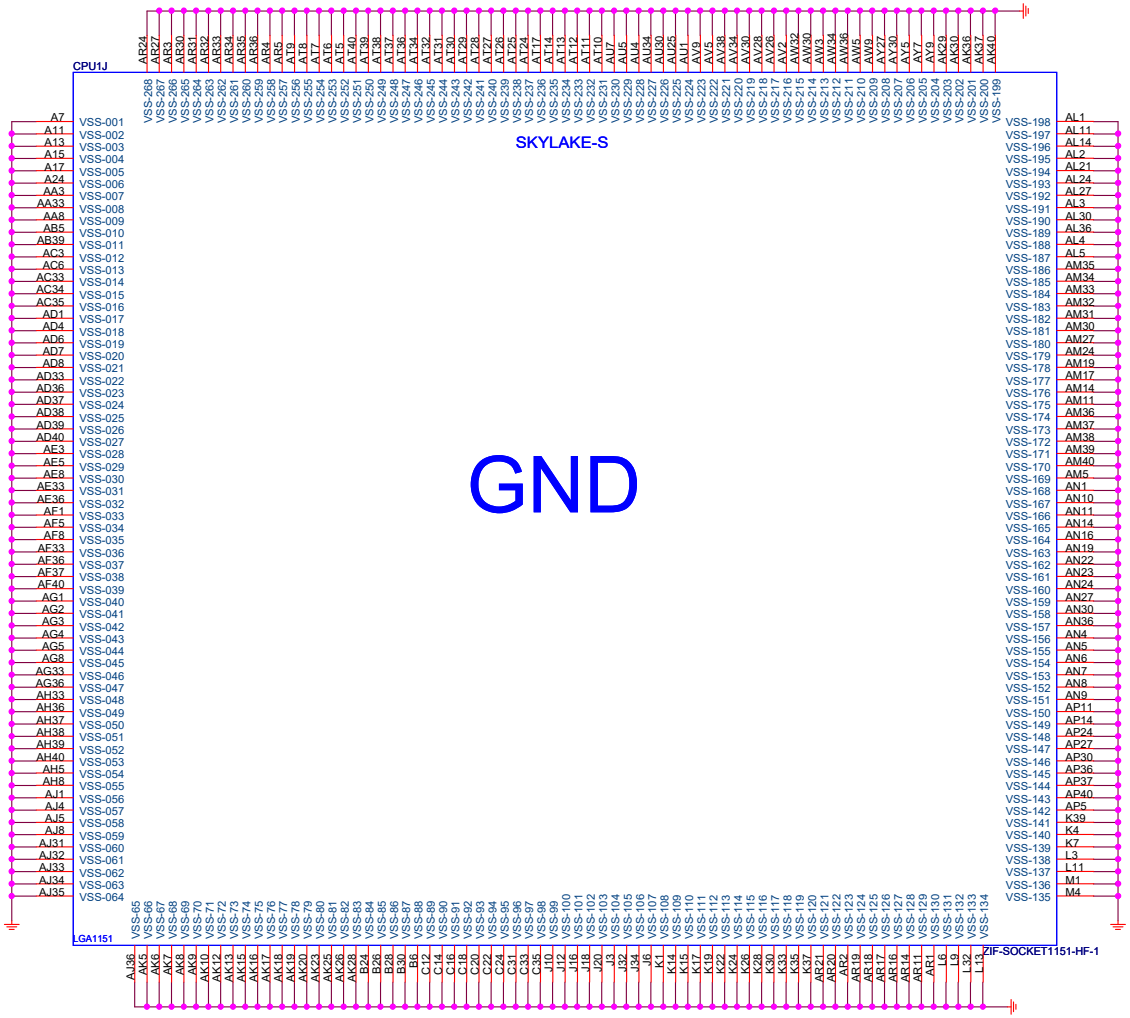
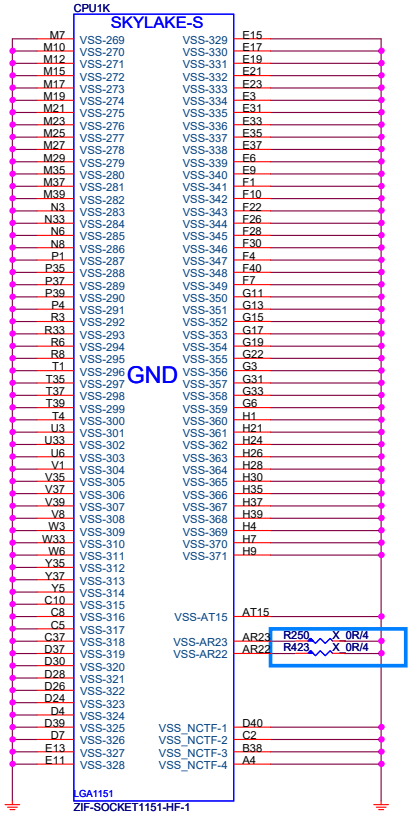
MS-7A78..

Size	Document Description	Rev
Custom	CPU-PEG/Display	10

Date: Friday, September 30, 2016 Sheet 5 of 72





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Size	Document Description	Rev
Custom	CPU-GND	10

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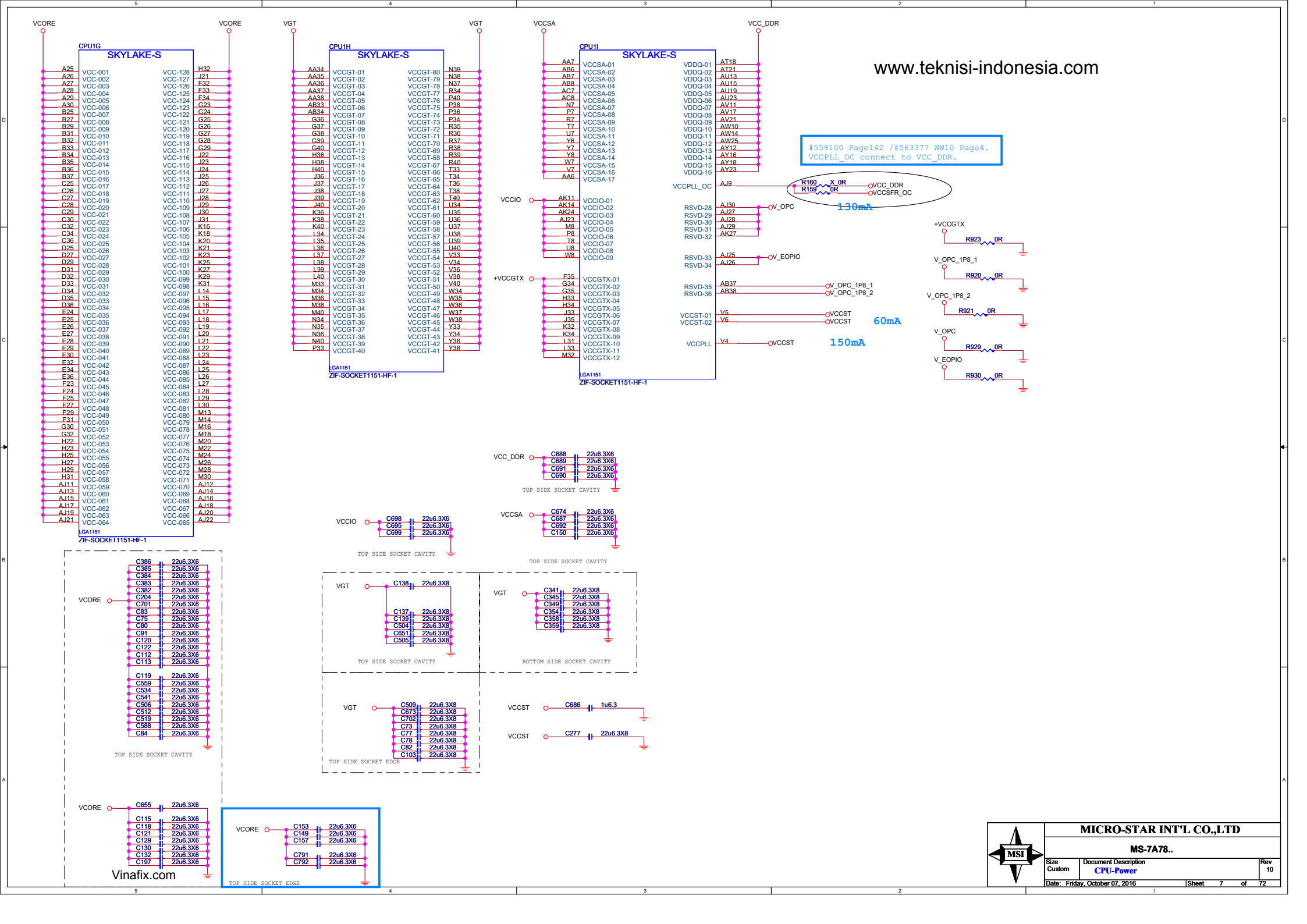
CPU1G
SKYLAKE-S
ZIF-SOCKET1151-HF-1
CPU1H
SKYLAKE-S
ZIF-SOCKET1151-HF-1
CPU1I
SKYLAKE-S
ZIF-SOCKET1151-HF-1
www.teknisi-indonesia.com
#559100 Page142 /#563377 WW10 Page4.
VCCPLL_OC connect to VCC_DDR.
130mA
60mA
150mA
TOP SIDE SOCKET CAVITY
BOTTOM SIDE SOCKET CAVITY
TOP SIDE SOCKET EDGE
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CPU-Power
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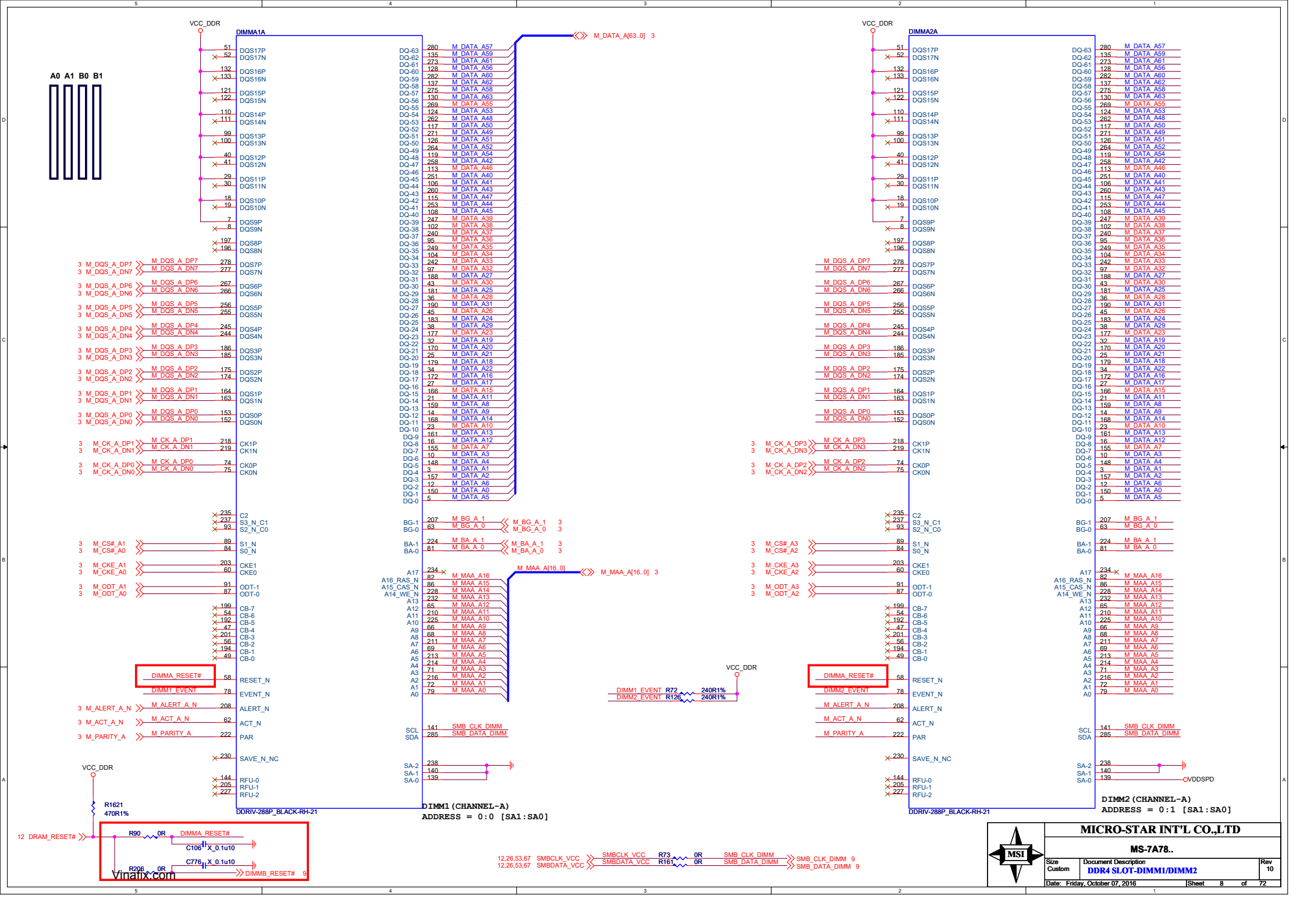
A0 A1 B0 B1
VCC_DDR
DIMMA1A
DIMMA2A
M_DATA_A[63..0] 3
M_MAA_A[16..0]
M_MAA_A[16..0] 3
DIMMA_RESET#
DIMM1_EVENT
DIMM2_EVENT
R72 240R1%
R126 240R1%
R1621 470R1%
12 DRAM_RESET#
R90 0R
R206 0R
C106 X_0.1u10
C776 X_0.1u10
DIMMB_RESET# 9
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DDRIV-288P_BLACK-RH-21
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
VDDSPD
12,26,53,67 SMBCLK_VCC
12,26,53,67 SMBDATA_VCC
SMBCLK_VCC R73 0R SMB_CLK_DIMM
SMBDATA_VCC R161 0R SMB_DATA_DIMM
SMB_CLK_DIMM 9
SMB_DATA_DIMM 9
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MS-7A78..
Size Custom
Document Description DDR4 SLOT-DIMM1/DIMM2
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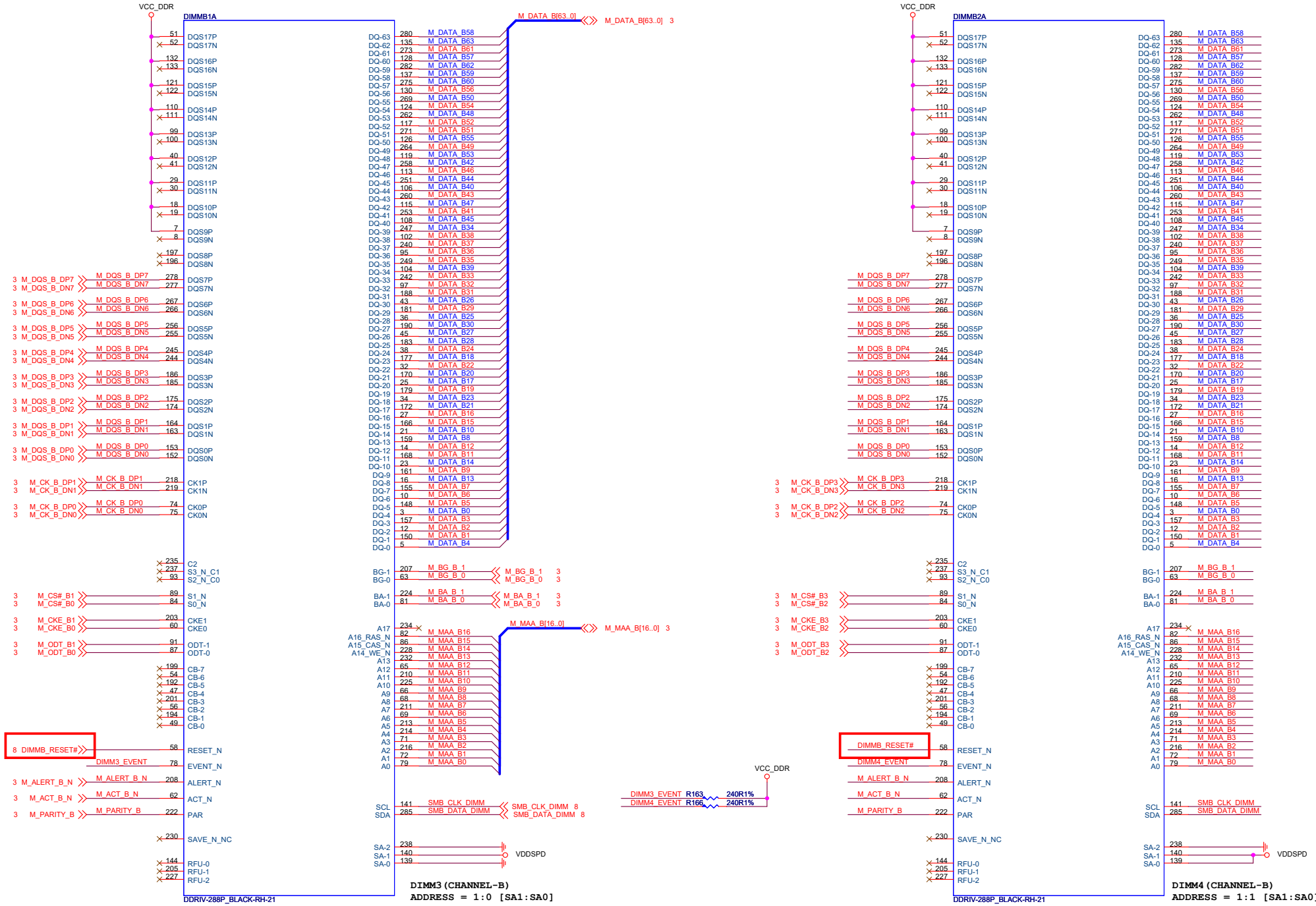

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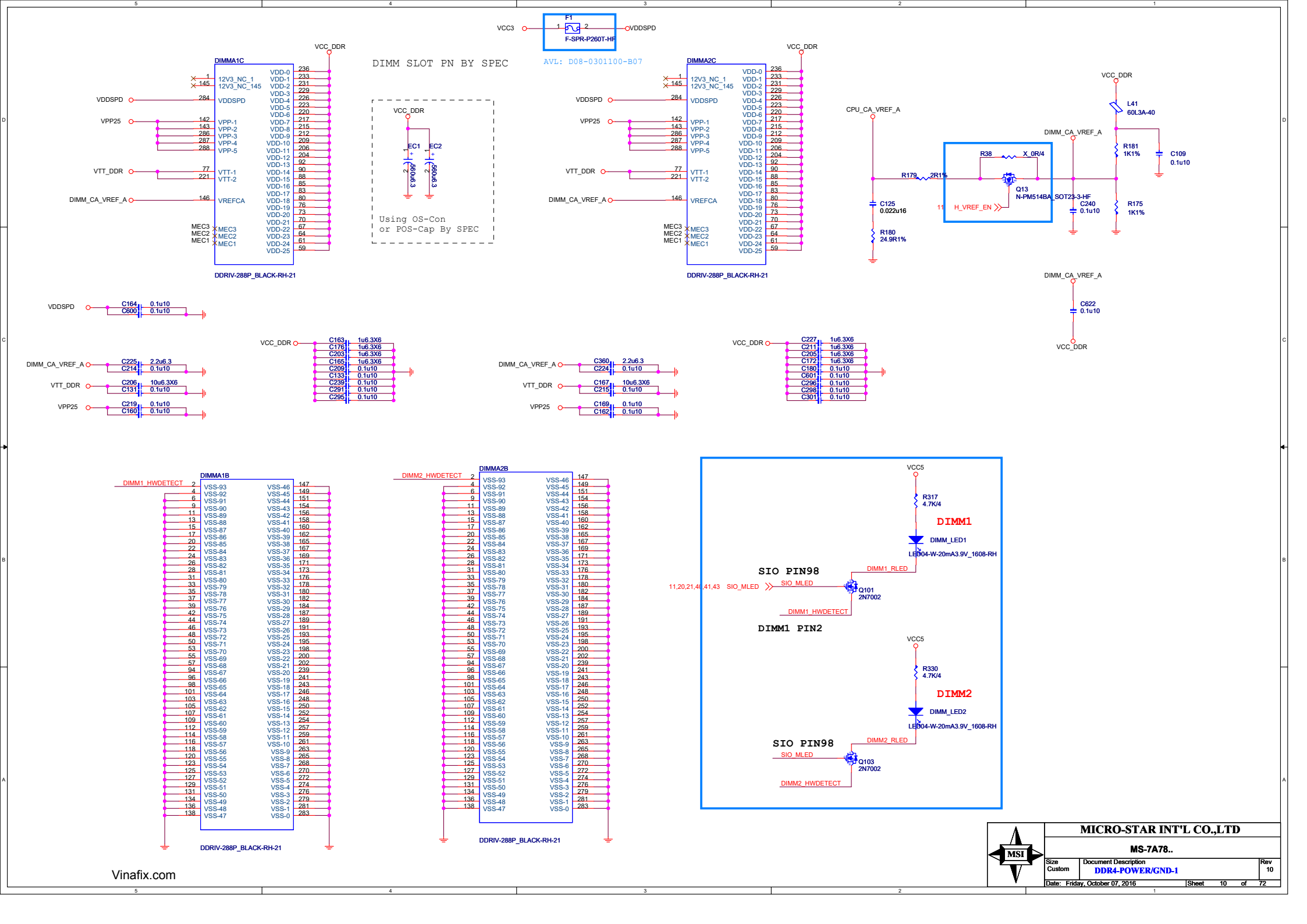
Size: Custom	Document Description: DDR4 SLOT-DIMM3/DIMM4	Rev: 10
Date: Friday, October 07, 2016	Sheet 9 of 72	



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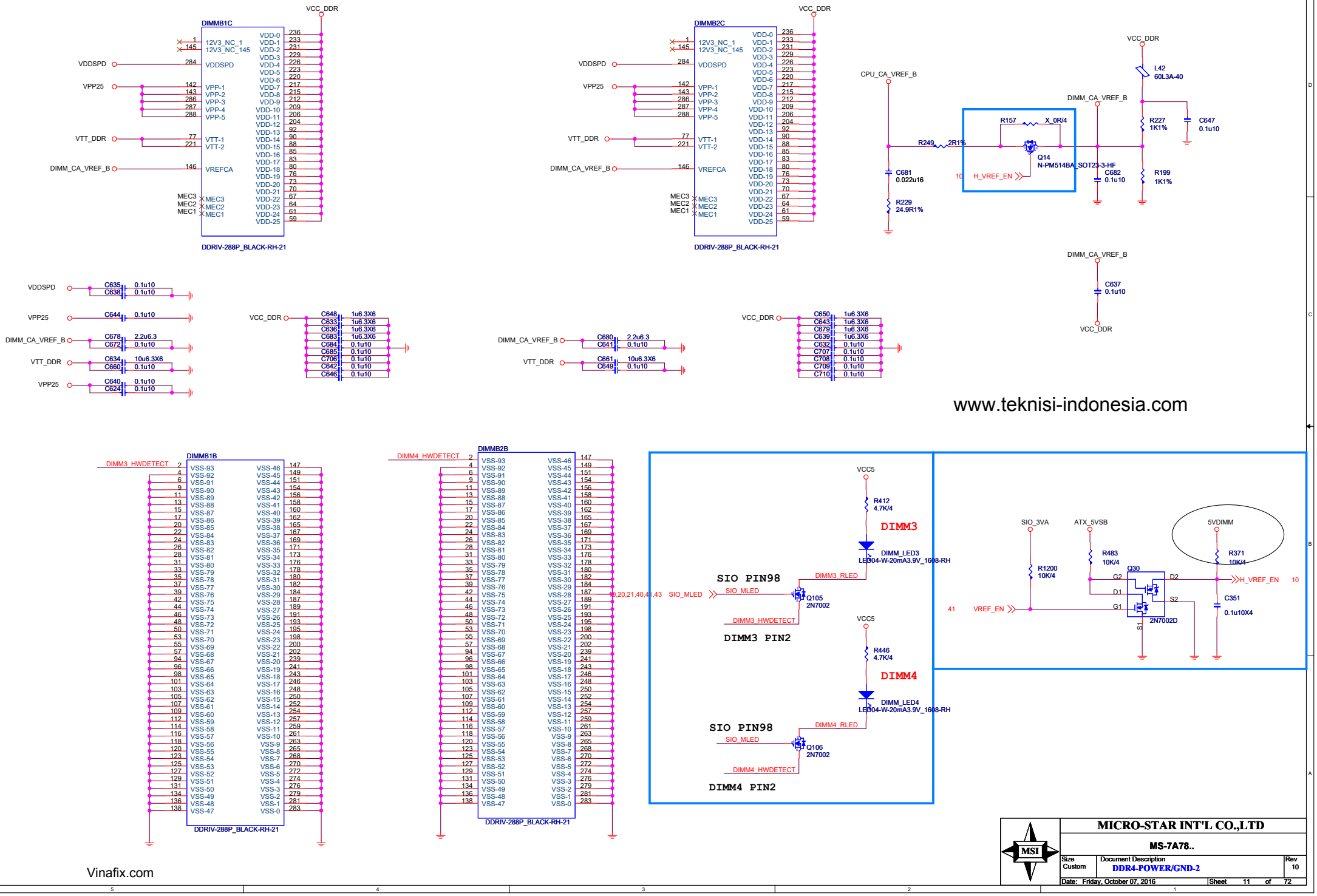
Date: Friday, October 07, 2016	Sheet 10 of 72	


DIMMB1C
DDRIV-288P_BLACK-RH-21
VCC_DDR
VDDSPD
VPP25
VTT_DDR
DIMM_CA_VREF_B
DIMMB2C
CPU_CA_VREF_B
R157 X_0R/4
R249 2R1%
Q14 N-PM514BA_SOT23-3-HF
H_VREF_EN
L42 60L3A-40
R227 1K1%
R199 1K1%
C647 0.1u10
C681 0.022u16
R229 24.9R1%
C682 0.1u10
C635 0.1u10
C638 0.1u10
C644 0.1u10
C678 2.2u6.3
C672 0.1u10
C634 10u6.3X6
C660 0.1u10
C640 0.1u10
C624 0.1u10
C648 1u6.3X6
C633 1u6.3X6
C636 1u6.3X6
C683 1u6.3X6
C684 0.1u10
C685 0.1u10
C706 0.1u10
C642 0.1u10
C646 0.1u10
C680 2.2u6.3
C641 0.1u10
C661 10u6.3X6
C649 0.1u10
C650 1u6.3X6
C643 1u6.3X6
C679 1u6.3X6
C639 1u6.3X6
C632 0.1u10
C707 0.1u10
C708 0.1u10
C709 0.1u10
C710 0.1u10
C637 0.1u10
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DIMMB1B
DIMM3_HWDETECT
DIMMB2B
DIMM4_HWDETECT
SIO PIN98
SIO_MLED
Q105 2N7002
DIMM3_RLED
DIMM3_HWDETECT
DIMM3 PIN2
R412 4.7K/4
DIMM3
DIMM_LED3 LED04-W-20mA3.9V_1608-RH
R446 4.7K/4
DIMM4
DIMM_LED4 LED04-W-20mA3.9V_1608-RH
Q106 2N7002
DIMM4_RLED
DIMM4 PIN2
SIO_3VA
ATX_5VSB
5VDIMM
R1200 10K/4
R483 10K/4
R371 10K/4
Q30
2N7002D
VREF_EN
C351 0.1u10X4
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Size Custom
Document Description DDR4-POWER/GND-2
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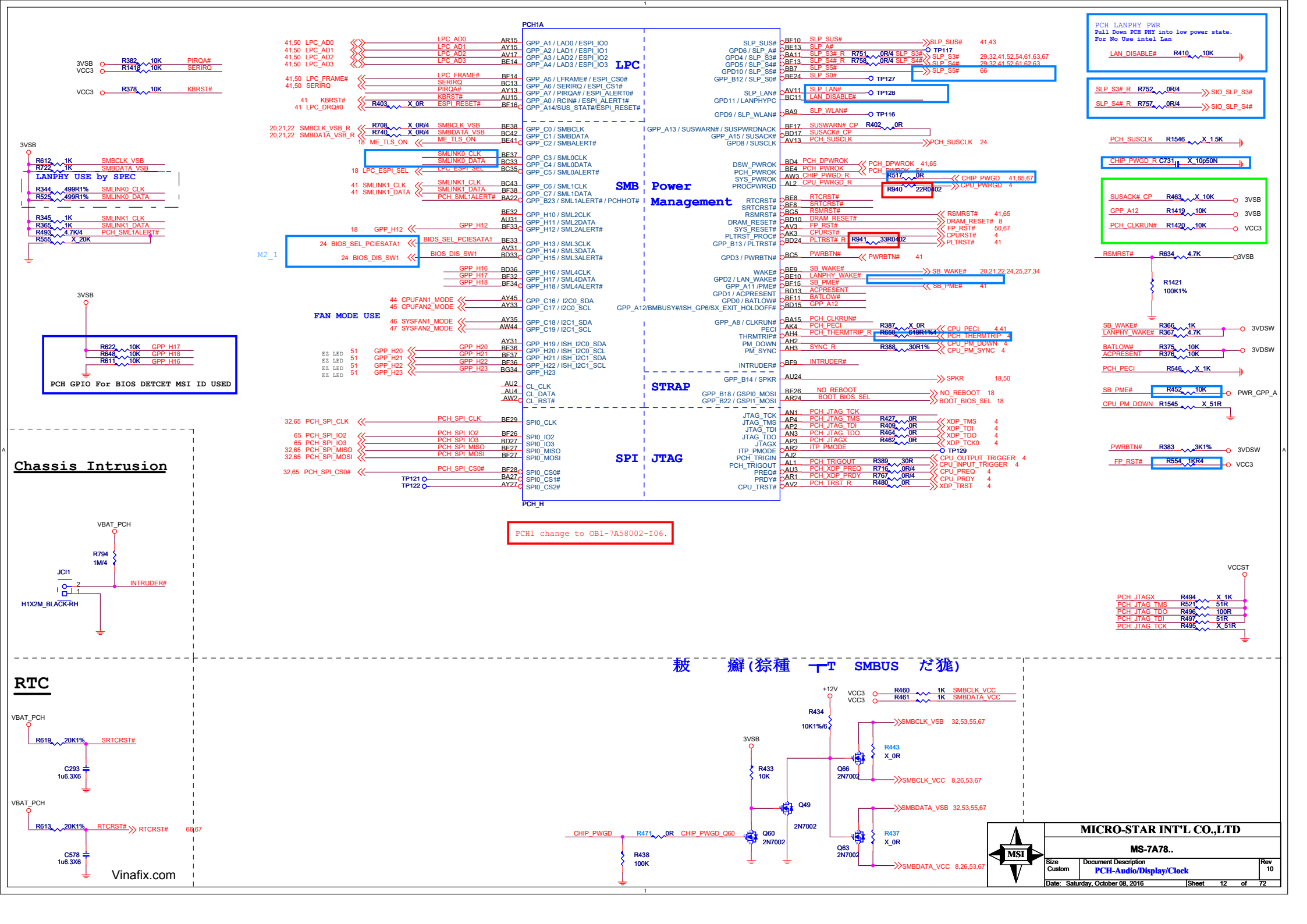
PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
PCH_H
PCH1 change to OB1-7A58002-I06.
LANPHY USE by SPEC
PCH GPIO For BIOS DETCET MSI ID USED
FAN MODE USE
Chassis Intrusion
RTC
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MS-7A78..
PCH-Audio/Display/Clock

PCH_CLK

RTC Block

Close to PCH

C289 12p50N6 — RTCX2
Y2
R481 10M/6 <1 inch
RTCX1 — C292 12p50N6
32.768KHZ12.5p_D-RH-10

AVL: D04-0306001-C11/D04-0306101-T02

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
R445 1MR1%4
R212 0R
R218 0R
24M_OUT
24M_IN
Y1
24MHZ20p_S-HF
C285 C22p50N/4
C284 C22p50N/4

CRB
SRCCLKREQ pull up power change to VCC3.

VCC3
R290 10K LAN_CLKREQ#4
R304 10K M2_CLKREQ#9
R420 10K M2_CLKREQ#10
R311 10K ASM1142_CLKREQ#5

PCH1E

41 CLK_SIO_PCI — R559 22R — CLK_PCH_LPC0 — BE15 — GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
50 TPM_CLK — R468 22R — CLK_PCH_LPC1 — AY17 — GPP_A10 / CLKOUT_LPC1
BC17 — GPP_A16 / CLKOUT_48 — LPC

RTCX1 — BF7 — RTCX1
RTCX2 — BG7 — RTCX2 — RTC

XTAL_24M_PCH_IN — F1 — XTAL24_IN
XTAL_24M_PCH_OUT — A5 — XTAL24_OUT — 24MHZ
C551 0.1u10
PCH_CLK5_1P0 — R346 2.7K1% — XCLK_BIASREF — F1 — XCLK_BIASREF
XCLK_BIASREF < 500 mil

TP123 CLKREQ#0 — BE22 — GPP_B5 / SRCCLKREQ0#
TP124 CLKREQ#1 — BA24 — GPP_B6 / SRCCLKREQ1#
TP125 CLKREQ#2 — BA19 — GPP_B7 / SRCCLKREQ2#
TP126 CLKREQ#3 — BE23 — GPP_B8 / SRCCLKREQ3#
LAN_CLKREQ#4 — BD22 — GPP_B9 / SRCCLKREQ4#
ASM1142_CLKREQ#5 — BF23 — GPP_B10 / SRCCLKREQ5#
LAN: 34 LAN_CLKREQ#4
ASMEDIA: 27 ASM1142_CLKREQ#5

CLK_REQ

TP132 CLKREQ#6 — AR29 — GPP_H0 / SRCCLKREQ6#
TP133 CLKREQ#7 — AU27 — GPP_H1 / SRCCLKREQ7#
TP134 CLKREQ#8 — BG30 — GPP_H2 / SRCCLKREQ8#
M2_CLKREQ#9 — BF30 — GPP_H3 / SRCCLKREQ9#
M2_CLKREQ#10 — BD29 — GPP_H4 / SRCCLKREQ10#
U.2
M.2: 24 M2_CLKREQ#9, 25 M2_CLKREQ#10

BE31 — GPP_H5 / SRCCLKREQ11#
AY29 — GPP_H6 / SRCCLKREQ12#
AV29 — GPP_H7 / SRCCLKREQ13#
BD31 — GPP_H8 / SRCCLKREQ14#
BF31 — GPP_H9 / SRCCLKREQ15#

PCH_H

CLKOUT_CPUBCLK_P — H1 — PCH_IDT_BCLK_DP — PCH_IDT_BCLK_DP 67
CLKOUT_CPUBCLK_N — H2 — PCH_IDT_BCLK_DN — PCH_IDT_BCLK_DN 67
CLKOUT_CPUNSSC_P — G2 — PCH_CPU_NSSC_CLK_DP — PCH_CPU_NSSC_CLK_DP 4
CLKOUT_CPUNSSC_N — G1 — PCH_CPU_NSSC_CLK_DN — PCH_CPU_NSSC_CLK_DN 4
CLKOUT_CPUPCIBCLK_P — J2 — PCH_CPU_PCIE_DP — PCH_CPU_PCIE_DP 4
CLKOUT_CPUPCIBCLK_N — J3 — PCH_CPU_PCIE_DN — PCH_CPU_PCIE_DN 4
CLKOUT_ITPXDP_P — L3
CLKOUT_ITPXDP_N — L2

CLKOUT_PCIE_P0 — P7 — CLK_PE2_DP — CLK_PE2_DP 22 — PCI_E2
CLKOUT_PCIE_N0 — P5 — CLK_PE2_DN — CLK_PE2_DN 22
CLKOUT_PCIE_P1 — M5 — CLK_PE6_DP — CLK_PE6_DP 21 — PCI_E6
CLKOUT_PCIE_N1 — M7 — CLK_PE6_DN — CLK_PE6_DN 21
CLKOUT_PCIE_P2 — G7 — CLK_PE4_DP — CLK_PE4_DP 21 — PCI_E4
CLKOUT_PCIE_N2 — H7 — CLK_PE4_DN — CLK_PE4_DN 21
CLKOUT_PCIE_P3 — K5 — CLK_PE1_DP — CLK_PE1_DP 20 — PCI_E1
CLKOUT_PCIE_N3 — K7 — CLK_PE1_DN — CLK_PE1_DN 20
CLKOUT_PCIE_P4 — E4 — CLK_LAN_DP — CLK_LAN_DP 34 — LAN
CLKOUT_PCIE_N4 — E3 — CLK_LAN_DN — CLK_LAN_DN 34
CLKOUT_PCIE_P5 — C6 — CLK_ASM1142_DP — CLK_ASM1142_DP 27 — ASMEDIA
CLKOUT_PCIE_N5 — C5 — CLK_ASM1142_DN — CLK_ASM1142_DN 27
CLKOUT_PCIE_P6 — T7 — CLK_PE3_DP — CLK_PE3_DP 22 — PCI_E3
CLKOUT_PCIE_N6 — T8 — CLK_PE3_DN — CLK_PE3_DN 22
CLKOUT_PCIE_P7 — V7 — CLK_PE5_DP — CLK_PE5_DP 22 — PCI_E5
CLKOUT_PCIE_N7 — V5 — CLK_PE5_DN — CLK_PE5_DN 22
CLKOUT_PCIE_P8 — Y11 — CK_U.2_DP — CK_U.2_DP 26 — U.2
CLKOUT_PCIE_N8 — Y10 — CK_U.2_DN — CK_U.2_DN 26
CLKOUT_PCIE_P9 — M1 — CLK_M2_1_DP — CLK_M2_1_DP 24 — M.2
CLKOUT_PCIE_N9 — M2 — CLK_M2_1_DN — CLK_M2_1_DN 24
CLKOUT_PCIE_P10 — P2 — CLK_M2_2_DP — CLK_M2_2_DP 25 — M.2
CLKOUT_PCIE_N10 — P3 — CLK_M2_2_DN — CLK_M2_2_DN 25
CLKOUT_PCIE_P11 — T3
CLKOUT_PCIE_N11 — T2
CLKOUT_PCIE_P12 — U2
CLKOUT_PCIE_N12 — U1
CLKOUT_PCIE_P13 — AA5
CLKOUT_PCIE_N13 — Y7
CLKOUT_PCIE_P14 — R2
CLKOUT_PCIE_N14 — R3
CLKOUT_PCIE_P15 — T11
CLKOUT_PCIE_N15 — T13

AZ_BITCLK
C774 X_12p50N6

PCH1D

38 AZ_SDIN0 — AZ_SDIN0 — BA2 — HDA_SDI0
18 AZ_SDOUT_R, 38 AZ_SDOUT — AZ_SDOUT_R — R352 33R — AZ_SDOUT_R — BB1 — HDA_SDI1 — BC3 — HDA_SDO
38 AZ_BITCLK — AZ_BITCLK — R349 33R — AZ_BITCLK_LR — BB3 — HDA_BCLK
38 AZ_RST# — AZ_RST# — R350 33R — AZ_RST#_R — BC1 — HDA_RST#
38 AZ_SYNC — AZ_SYNC — R351 33R — AZ_SYNC_R — BG6 — HDA_SYNC

AUDIO

4 PCH_CPU_AUD_SCLK — R335 30R — PCH_CPU_AUD_SCLK_R — AM2 — DISPA_BCLK
4 PCH_CPU_AUD_SDO — R325 30R — PCH_CPU_AUD_SDO_R — AM3 — DISPA_SDO
4 PCH_CPU_AUD_SDI — PCH_CPU_AUD_SDI — AN2 — DISPA_SDI

AP36 GPP_D5 / I2S0_SFRM
AU43 GPP_D6 / I2S0_TXD
AV44 GPP_D7 / I2S0_RXD
AU42 GPP_D8 / I2S0_SCLK
AP42 GPP_D17 / DMIC_CLK1
AN43 GPP_D18 / DMIC_DATA1
AP38 GPP_D19 / DMIC_CLK0
AM43 GPP_D20 / DMIC_DATA0

PORT B

GPP_I5 / DDPB_CTRLCLK — AW5 — HDMI_DDPB_CTRLCLK — HDMI_DDPB_CTRLCLK 35
GPP_I6 / DDPB_CTRLDATA — AV7 — HDMI_DDPB_CTRLDATA — HDMI_DDPB_CTRLDATA 35
GPP_I0 / DDPB_HPD0 — AP7 — HDMI_DDPB_HPD — HDMI_DDPB_HPD 35

PORT C

GPP_I7 / DDPC_CTRLCLK — AT5 — HDMI_DDPC_CTRLCLK
GPP_I8 / DDPC_CTRLDATA — BA6 — HDMI_DDPC_CTRLDATA
GPP_I1 / DDPC_HPD1 — AT8 — HDMI_DDPC_HPD — R732 10K

PORT D

GPP_I9 / DDPD_CTRLCLK — AY1 — DSP_DDPD_CTRLCLK — DSP_DDPD_CTRLCLK 36
GPP_I10 / DDPD_CTRLDATA — AY2 — DSP_DDPD_CTRLDATA — DSP_DDPD_CTRLDATA 36
GPP_I2 / DDPD_HPD2 — AP8 — DSP_DDPD_HPD — DSP_DDPD_HPD 36

eDP

GPP_F19 / eDP_VDDEN — AC42
GPP_F20 / eDP_BKLTEN — AE35
GPP_F21 / eDP_BKLTCTL — AE36
GPP_I4 / EDP_HPD — BA1 — EDP_HPD — R176 100K
GPP_I3 / DDPE_HPD3 — AT7 — DDPE_HPD3 — R153 10K

PCH_H

VCC3
HDMI_DDPB_CTRLCLK — R347 2.2K
HDMI_DDPB_CTRLDATA — R348 2.2K
HDMI_DDPC_CTRLCLK — R453 X_2.2K
HDMI_DDPC_CTRLDATA — R454 X_2.2K
DSP_DDPD_CTRLCLK — R741 2.2K/4
DSP_DDPD_CTRLDATA — R759 2.2K/4

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Size: Custom
Document Description: PCH-USB/PCIE/DMI/SATA
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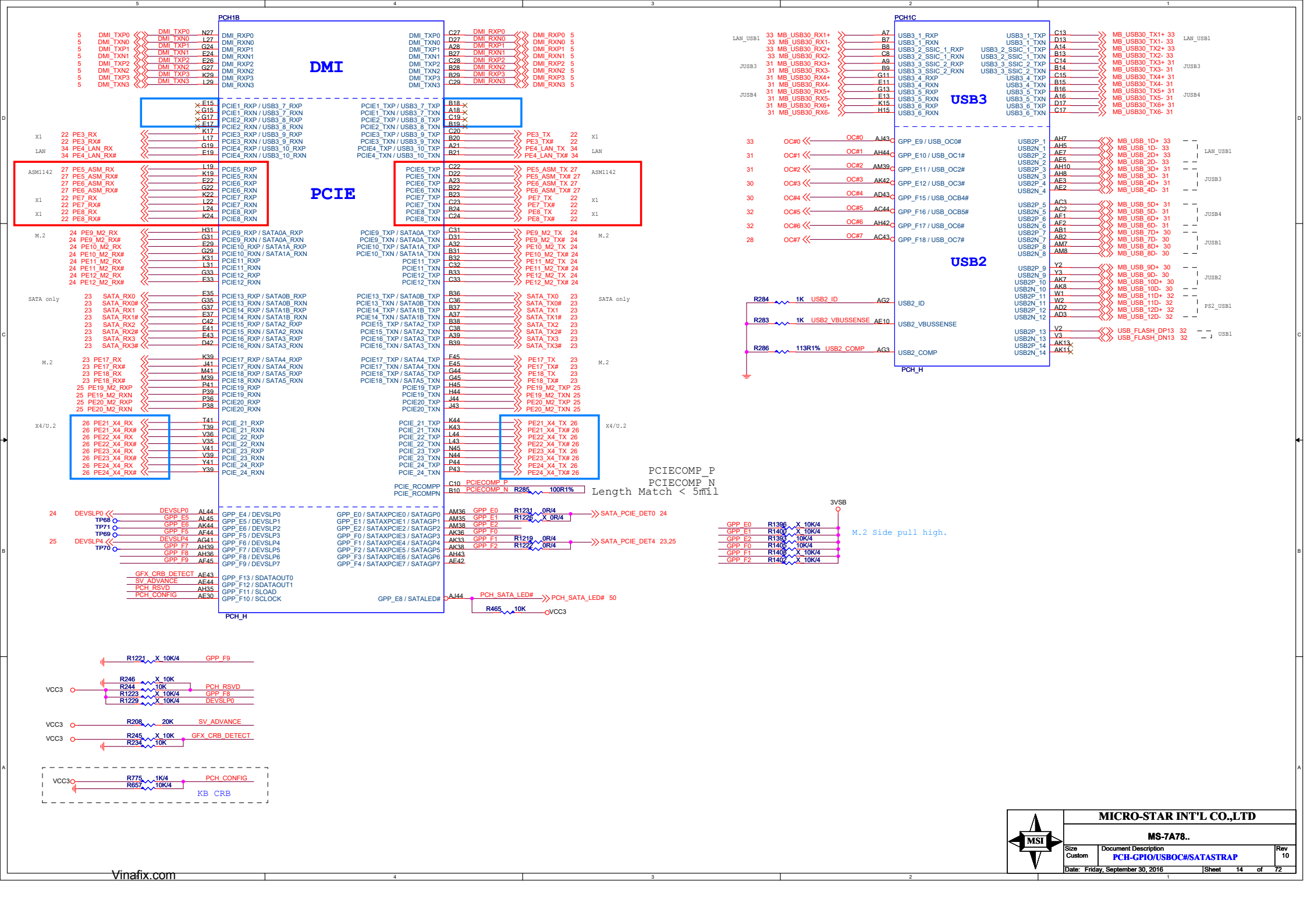
PCH1B
DMI
PCIE
PCH_H
PCH1C
USB3
USB2
PCH_H
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
M.2 Side pull high.
KB CRB
MICRO-STAR INT'L CO.,LTD
MS-7A78..
PCH-GPIO/USBOC#/SATASTRAP
Date: Friday, September 30, 2016
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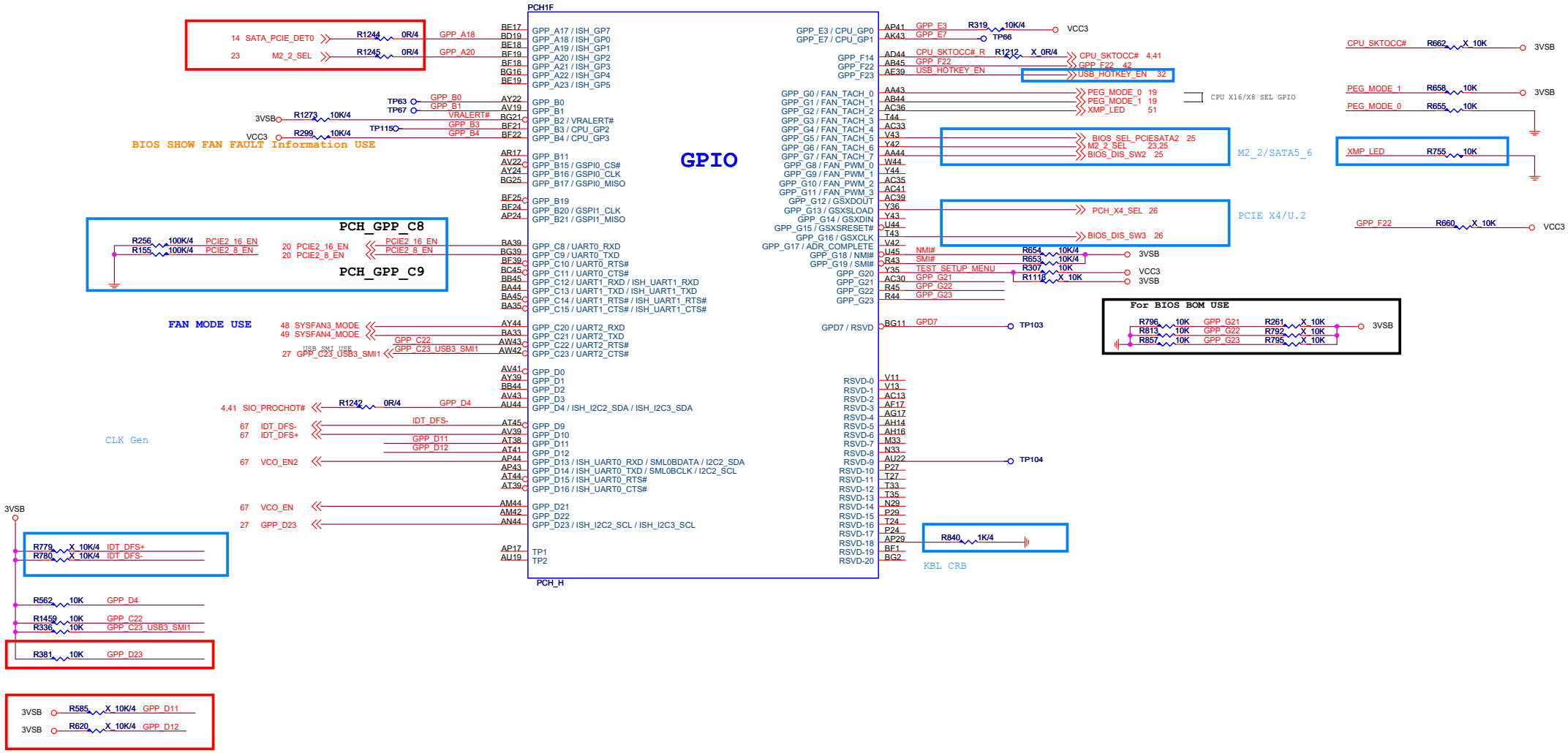

MICRO-STAR INT'L CO.,LTD

MS-7A78..

Size: Custom | Document Description: PCH-LPC/SPI/SMBUS/MISC | Rev: 10

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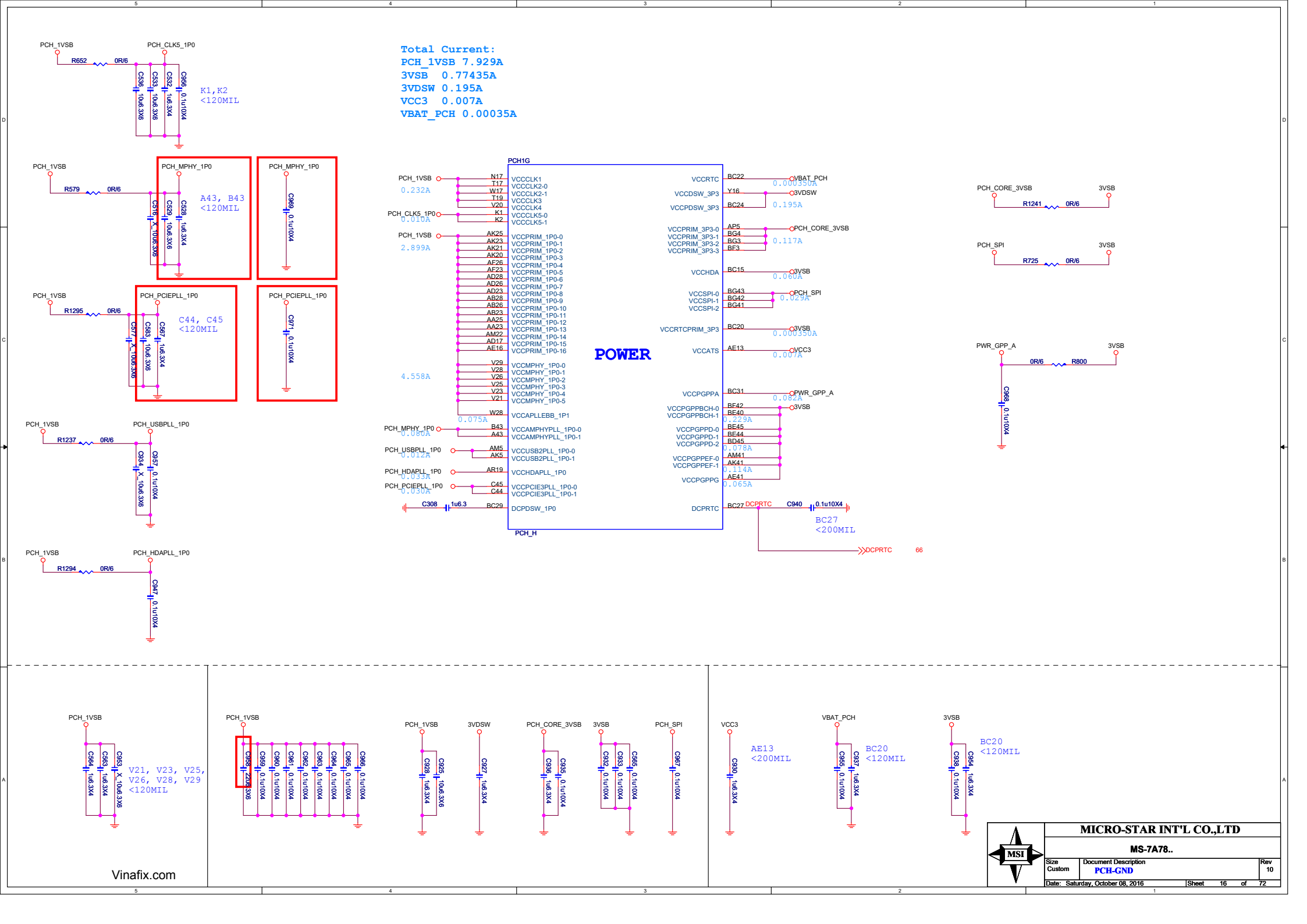
Total Current:
PCH_1VSB 7.929A
3VSB 0.77435A
3VDSW 0.195A
VCC3 0.007A
VBAT_PCH 0.00035A
PCH_1VSB
PCH_CLK5_1P0
R652 0R/6
C536 10u6.3X6
C533 10u6.3X6
C532 1u6.3X4
C986 0.1u10X4
K1,K2
<120MIL
PCH_MPHY_1P0
R579 0R/6
C516 X_10u6.3X6
C529 10u6.3X6
C528 1u6.3X4
A43, B43
<120MIL
C969 0.1u10X4
PCH_PCIEPLL_1P0
R1295 0R/6
C577 X_10u6.3X6
C583 10u6.3X6
C587 1u6.3X4
C44, C45
<120MIL
C971 0.1u10X4
PCH_USBPLL_1P0
R1237 0R/6
C934 X_10u6.3X6
C957 0.1u10X4
PCH_HDAPLL_1P0
R1294 0R/6
C947 0.1u10X4
PCH1G
POWER
PCH_H
PCH_1VSB 0.232A
PCH_CLK5_1P0 0.010A
PCH_1VSB 2.899A
4.558A
0.075A
PCH_MPHY_1P0 0.080A
PCH_USBPLL_1P0 0.012A
PCH_HDAPLL_1P0 0.033A
PCH_PCIEPLL_1P0 0.030A
C308 1u6.3
N17 VCCCLK1
T17 VCCCLK2-0
W17 VCCCLK2-1
T19 VCCCLK3
V20 VCCCLK4
K1 VCCCLK5-0
K2 VCCCLK5-1
AK25 VCCPRIM_1P0-0
AK23 VCCPRIM_1P0-1
AK21 VCCPRIM_1P0-2
AK20 VCCPRIM_1P0-3
AF26 VCCPRIM_1P0-4
AF23 VCCPRIM_1P0-5
AD28 VCCPRIM_1P0-6
AD26 VCCPRIM_1P0-7
AD23 VCCPRIM_1P0-8
AB28 VCCPRIM_1P0-9
AB26 VCCPRIM_1P0-10
AB23 VCCPRIM_1P0-11
AA25 VCCPRIM_1P0-12
AA23 VCCPRIM_1P0-13
AM22 VCCPRIM_1P0-14
AD17 VCCPRIM_1P0-15
AE16 VCCPRIM_1P0-16
V29 VCCMPHY_1P0-0
V28 VCCMPHY_1P0-1
V26 VCCMPHY_1P0-2
V25 VCCMPHY_1P0-3
V23 VCCMPHY_1P0-4
V21 VCCMPHY_1P0-5
W28 VCCAPLLEBB_1P1
B43 VCCAMPHYPLL_1P0-0
A43 VCCAMPHYPLL_1P0-1
AM5 VCCUSB2PLL_1P0-0
AK5 VCCUSB2PLL_1P0-1
AR19 VCCHDAPLL_1P0
C45 VCCPCIE3PLL_1P0-0
C44 VCCPCIE3PLL_1P0-1
BC29 DCPDSW_1P0
VCCRTC BC22 VBAT_PCH 0.000350A
VCCDSW_3P3 Y16 3VDSW
VCCPDSW_3P3 BC24 0.195A
VCCPRIM_3P3-0 AP5
VCCPRIM_3P3-1 BG4
VCCPRIM_3P3-2 BG3
VCCPRIM_3P3-3 BF3
PCH_CORE_3VSB 0.117A
VCCHDA BC15 3VSB 0.060A
VCCSPI-0 BG43
VCCSPI-1 BG42
VCCSPI-2 BG41
PCH_SPI 0.029A
VCCRTCPRIM_3P3 BC20 3VSB 0.000350A
VCCATS AE13 VCC3 0.007A
VCCPGPPA BC31 PWR_GPP_A 0.082A
VCCPGPPBCH-0 BF42
VCCPGPPBCH-1 BE40 3VSB 0.229A
VCCPGPPD-0 BE45
VCCPGPPD-1 BE44
VCCPGPPD-2 BD45 0.078A
VCCPGPPEF-0 AM41
VCCPGPPEF-1 AK41 0.114A
VCCPGPPG AE41 0.065A
DCPRTC BC27 DCPRTC C940 0.1u10X4
BC27
<200MIL
DCPRTC 66
PCH_CORE_3VSB R1241 0R/6 3VSB
PCH_SPI R725 0R/6 3VSB
PWR_GPP_A 0R/6 R800 3VSB
C968 0.1u10X4
PCH_1VSB
C564 1u6.3X4
C563 1u6.3X4
C953 X_10u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
C958 220u6.3X6
C959 0.1u10X4
C960 0.1u10X4
C961 0.1u10X4
C962 0.1u10X4
C963 0.1u10X4
C964 0.1u10X4
C965 0.1u10X4
C966 0.1u10X4
3VDSW
C928 1u6.3X4
C925 10u6.3X6
C927 1u6.3X4
PCH_CORE_3VSB
C936 1u6.3X4
C935 0.1u10X4
3VSB
C932 0.1u10X4
C933 0.1u10X4
C565 0.1u10X4
PCH_SPI
C967 0.1u10X4
VCC3
C930 1u6.3X4
AE13
<200MIL
VBAT_PCH
C955 0.1u10X4
C937 1u6.3X4
BC20
<120MIL
3VSB
C938 0.1u10X4
C954 1u6.3X4
BC20
<120MIL
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MICRO-STAR INT'L CO.,LTD
MS-7A78..
Size Custom
Document Description PCH-GND
Rev 10
Date: Saturday, October 08, 2016
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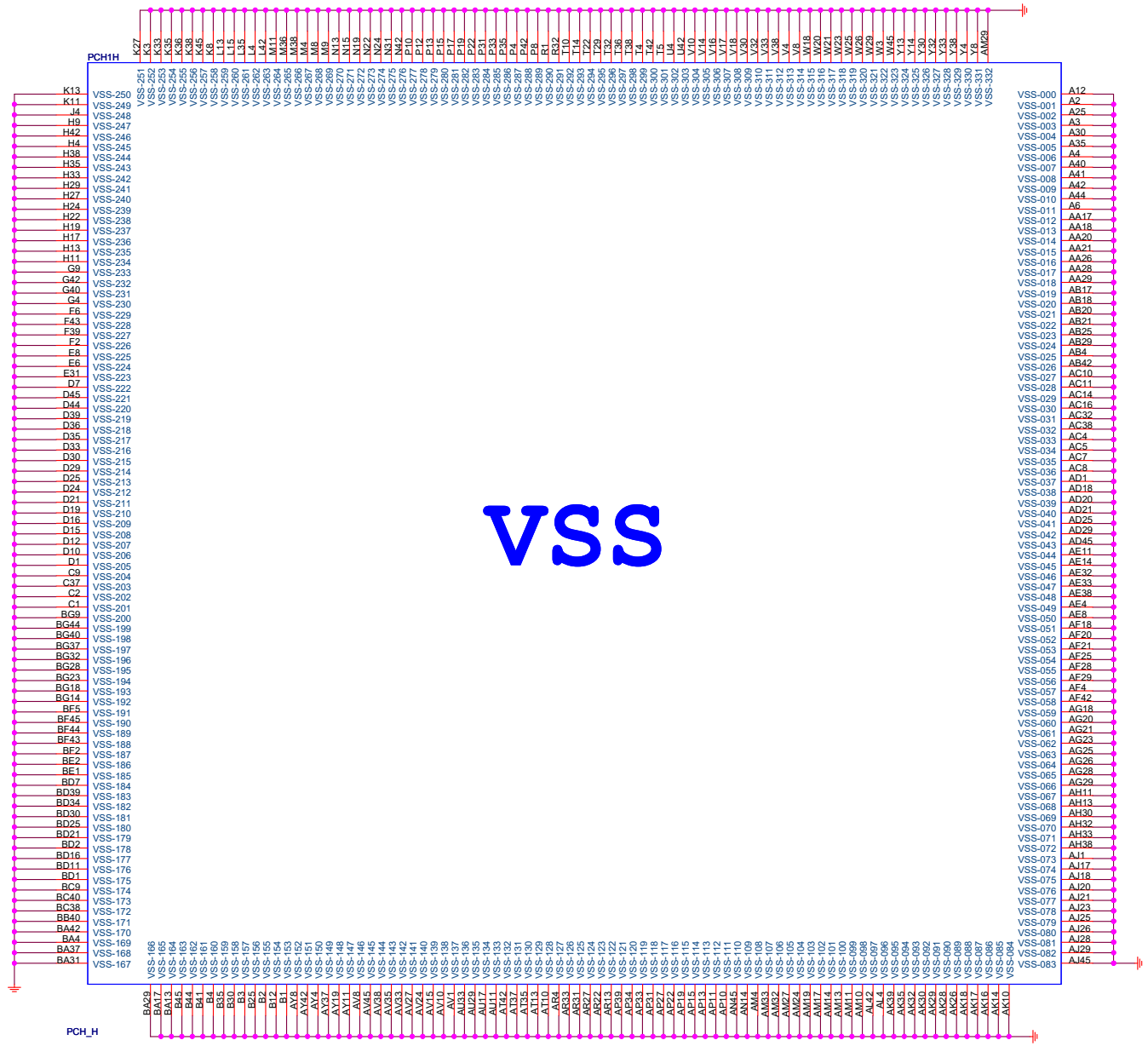

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Custom	PCH-Power	10

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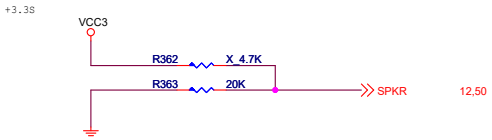
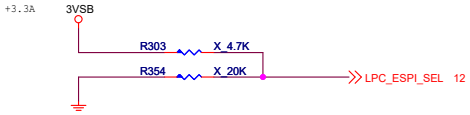
TOP Swap



Internal pull-down is disabled after PLTRST#

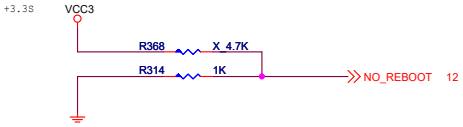
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

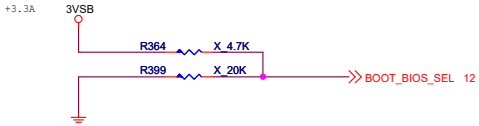
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

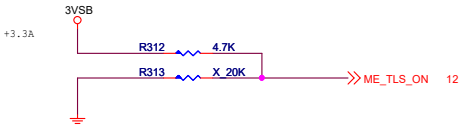
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

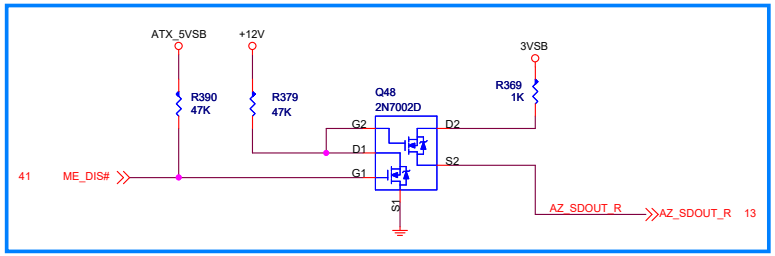
AMT and SBA with confidentiality



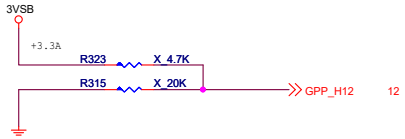
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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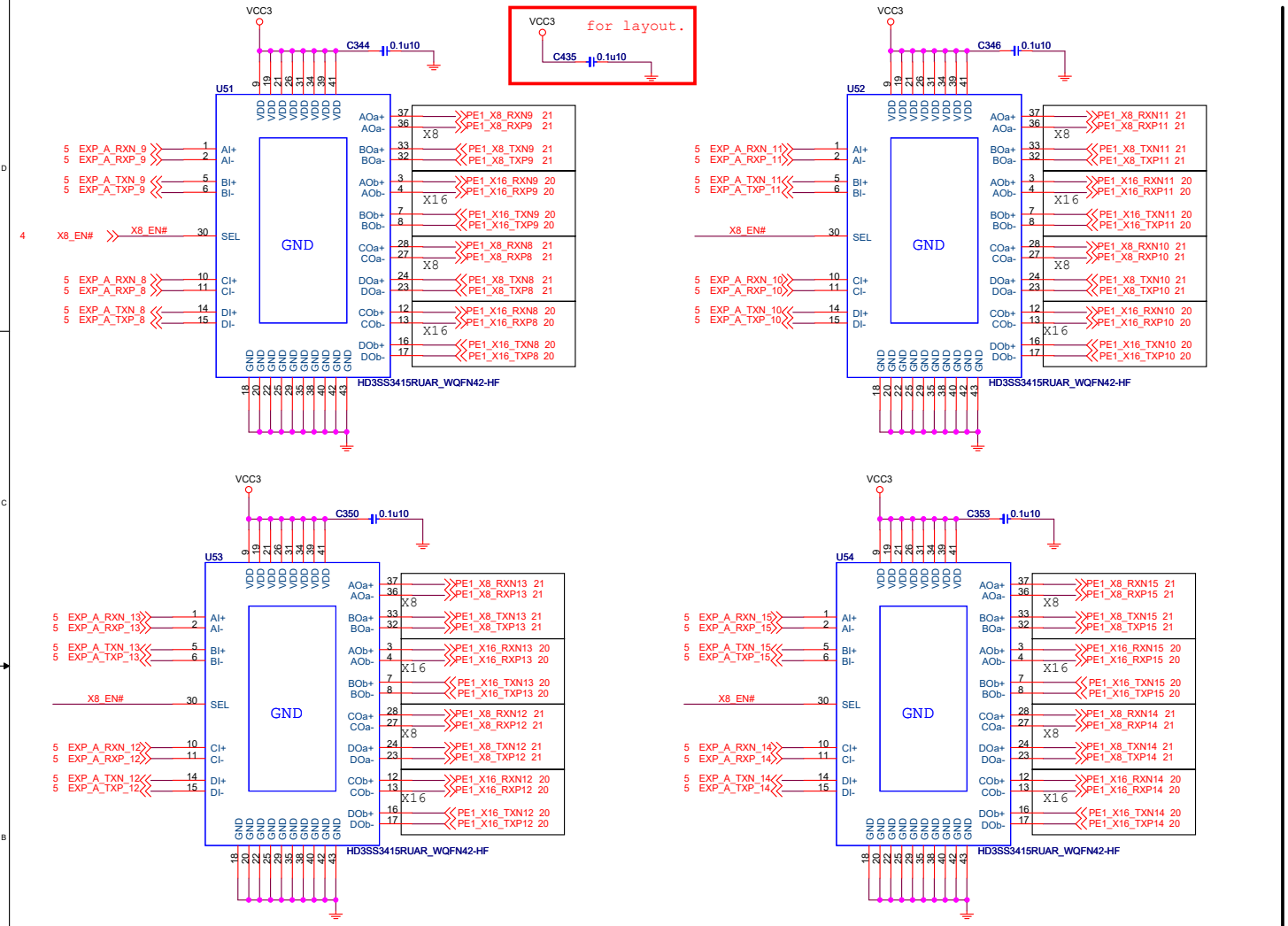

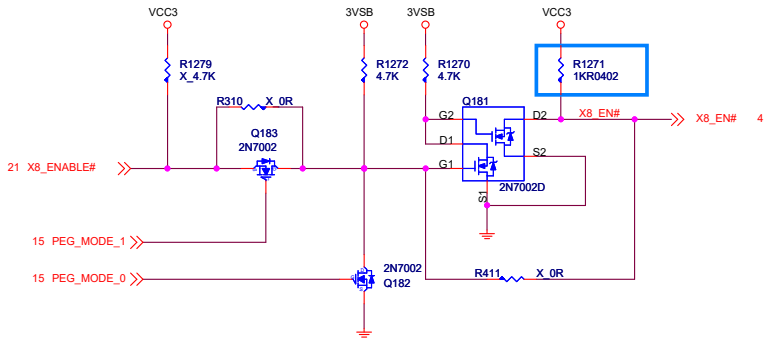

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MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0/2	MODE_1
AUTO	0	1

MICRO-STAR INT'L CO.,LTD

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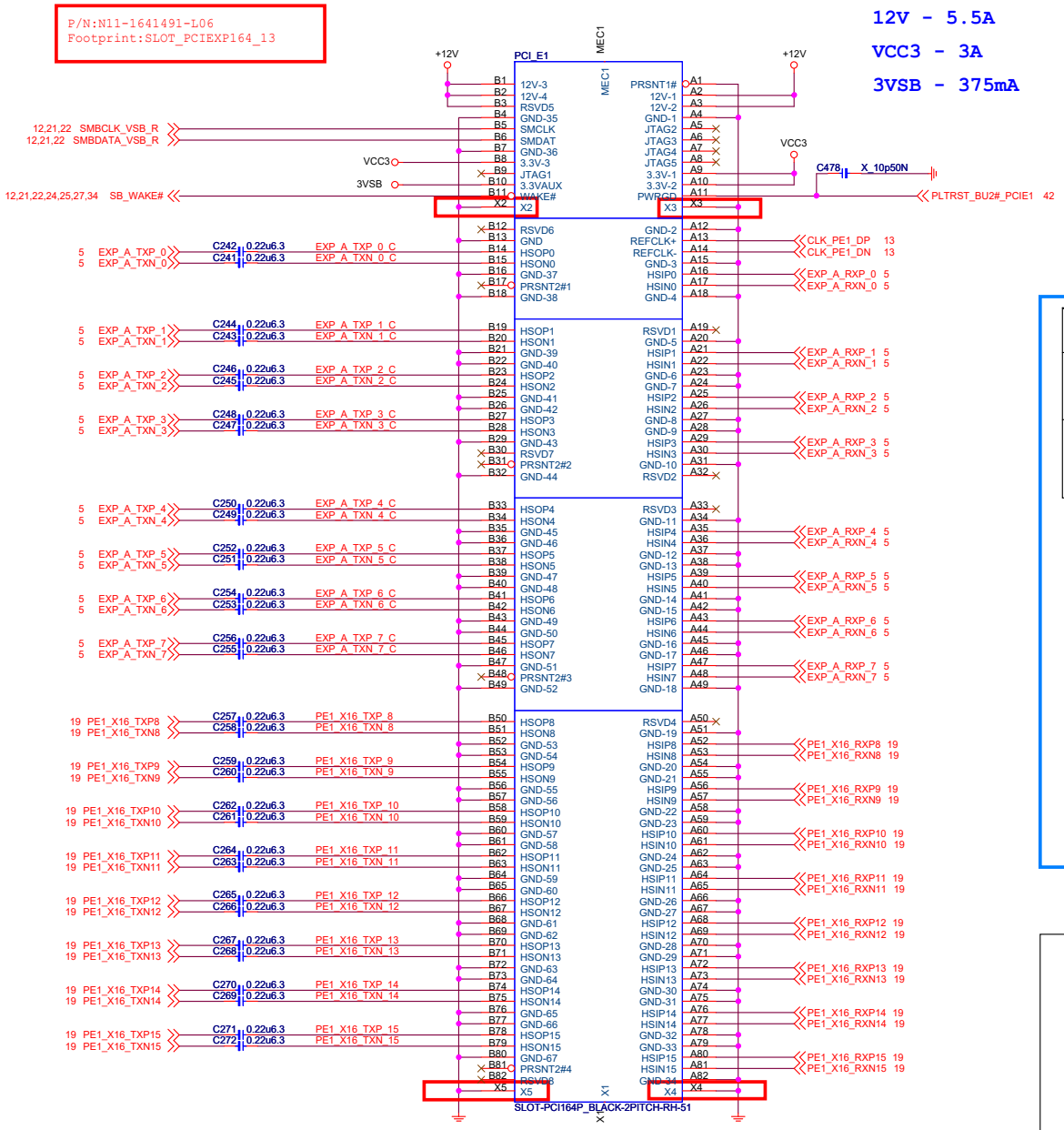
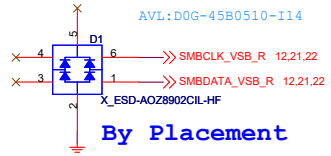
P/N:N11-1641491-L06
Footprint:SLOT_PCIEXP164_13

12V - 5.5A
VCC3 - 3A
3VSB - 375mA



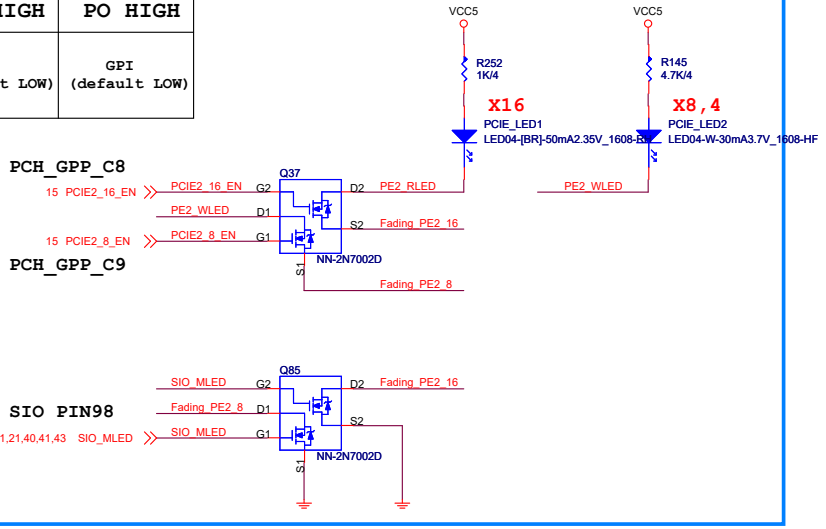
SMBUS ESD

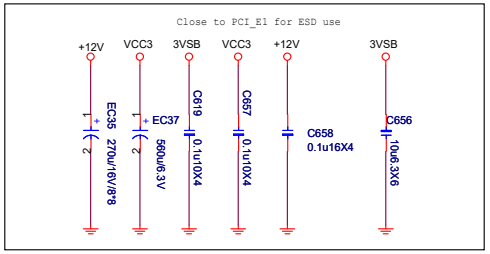


By Placement

GPIO / LED	GPP_C8	GPP_C9
獾	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

PCIE SLOT LED





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Size: Custom
Document Description: PCIE SLOT (X16)
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PCI Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSB- 375mA

P/N:N11-1000221-L06
Footprint:SLOT_PCIEXP100_5

P/N:N11-1000151-L06
Footprint:SLOT_PCIEXP100_3

SLOT-PCI100P_BLACK-2PITCH-RH-5

SLOT-PCI100P_BLUE-2PITCH-RH

Close to PCI_E4 for ESD use

Close to PCI_E6 for ESD use

X8 , 4

X4

VF:2.7~3.7V

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MS-7A78..	
Size: Custom	Document Description: PCIE SLOT (X4)
Rev: 10	
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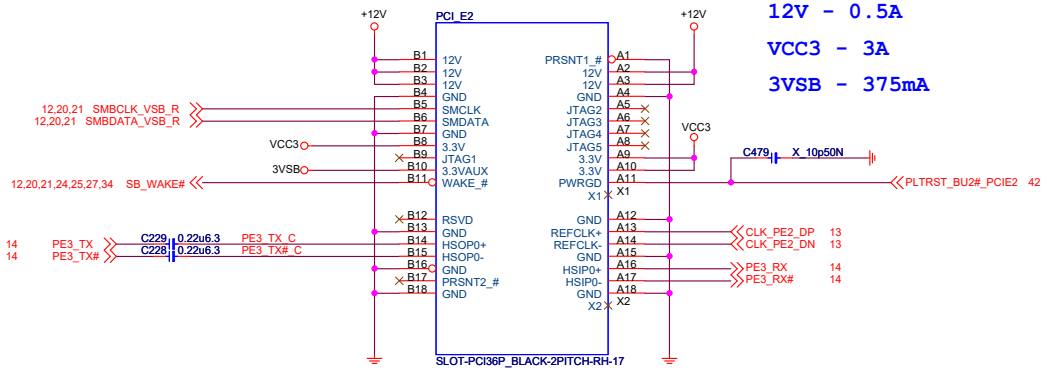

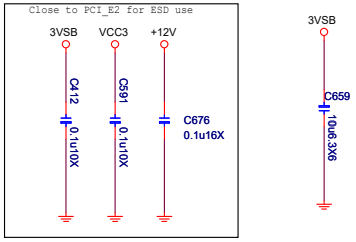

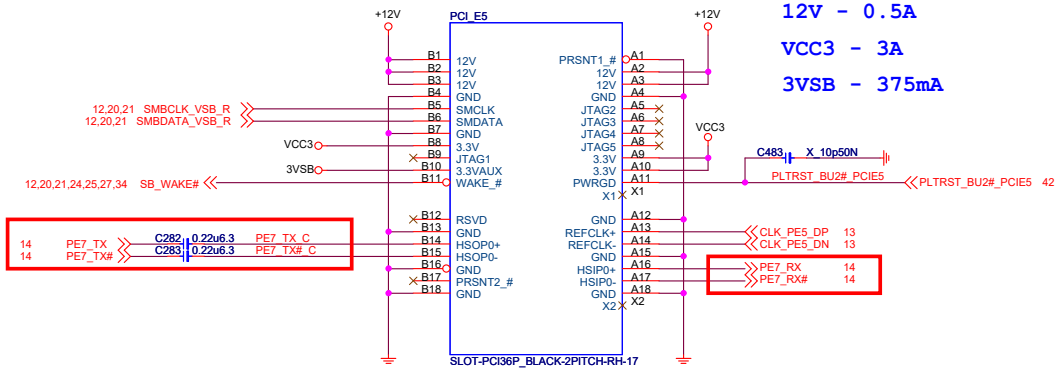

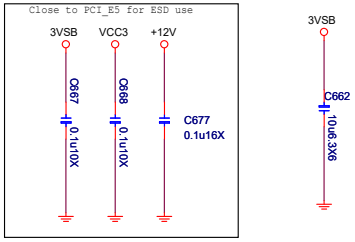

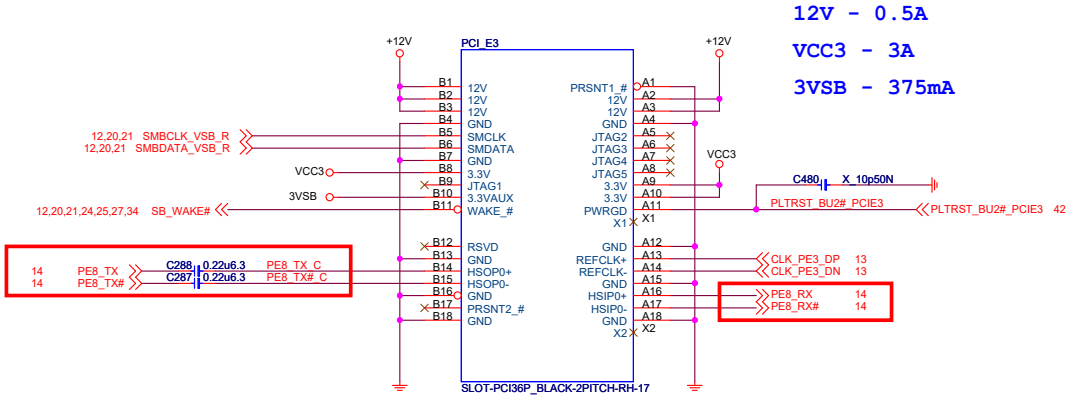

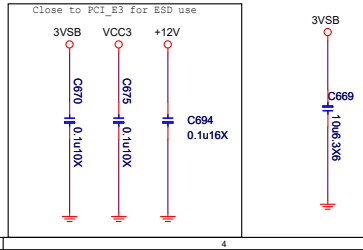

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Size	Document Description	Rev
Custom	PCIE SLOT (X1)	10

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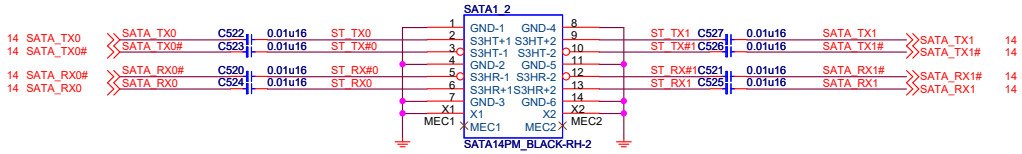
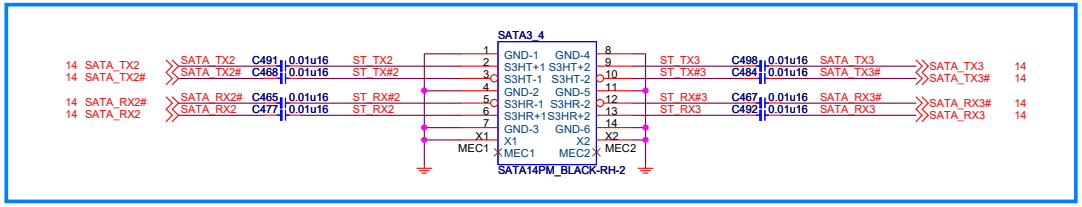
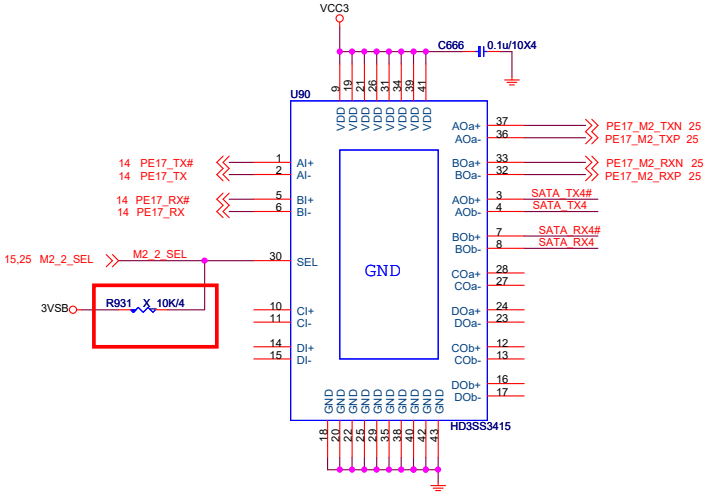
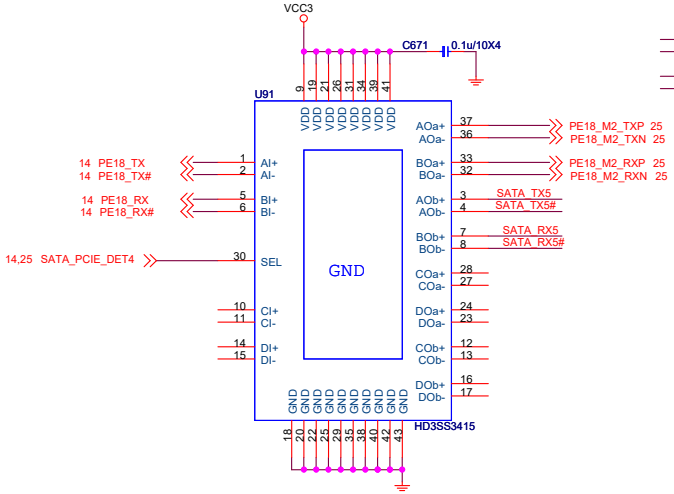
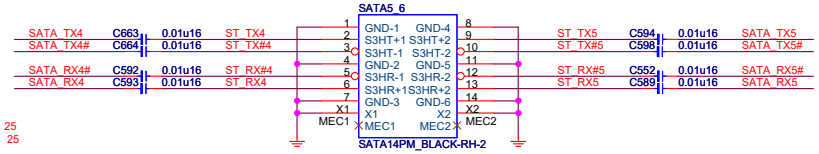




M2_2_SEL
0:to m2_2
1:to SATA







MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SATA Connector	10

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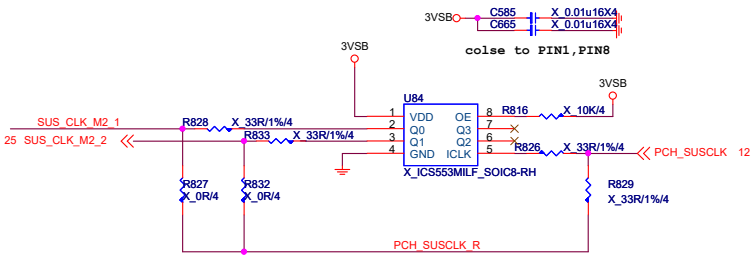
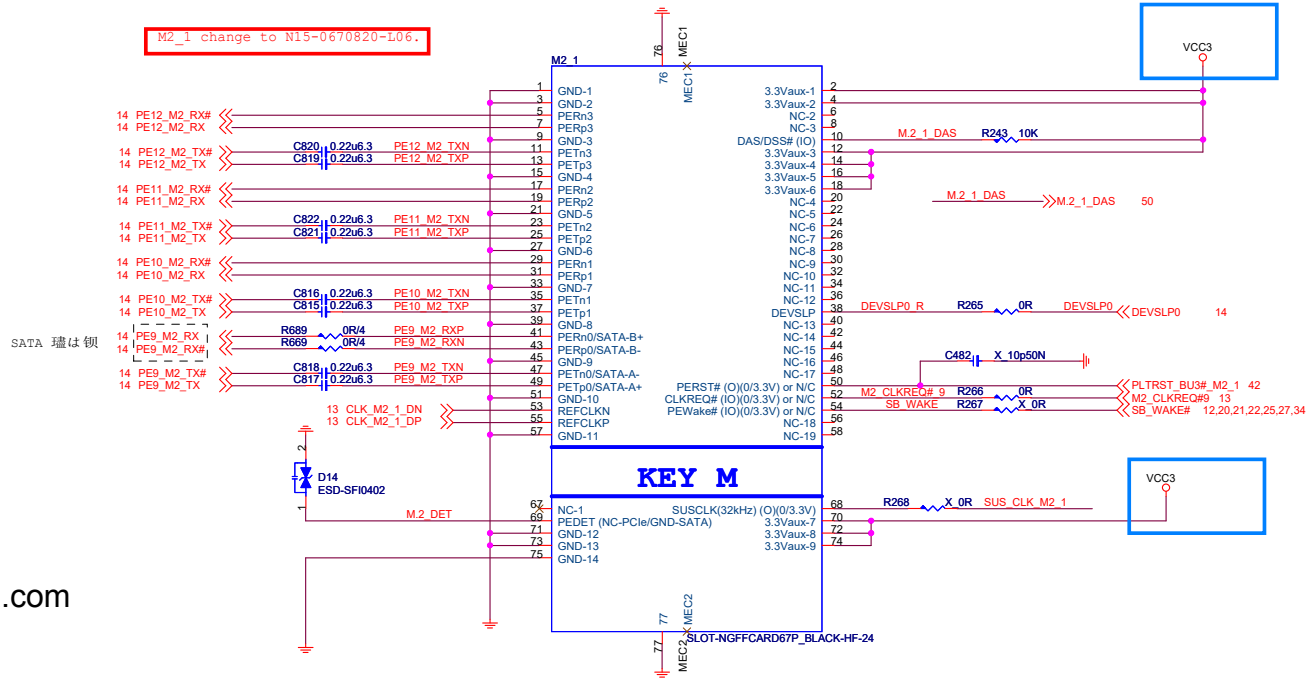
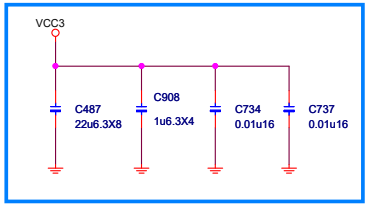


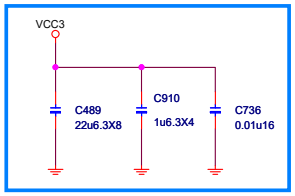


M.2 VCC3>=2.5A

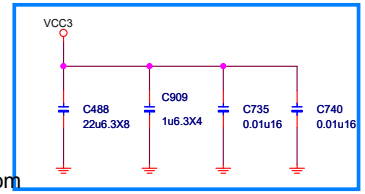
Near Pin2,Pin4

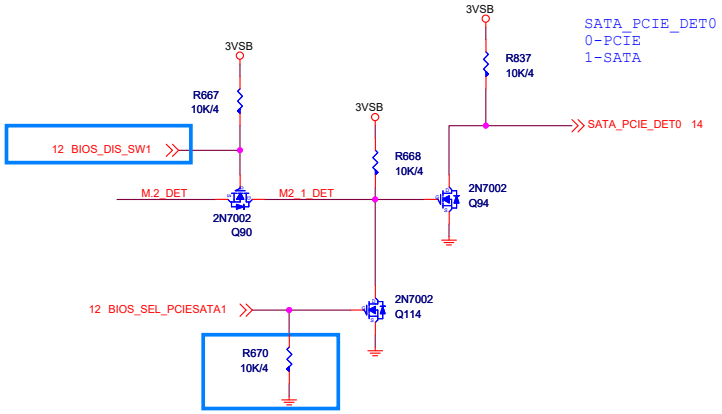


Near Pin12,Pin14,Pin16,Pin18



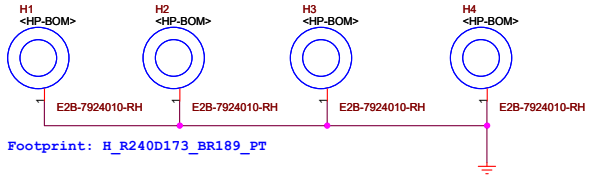
Near Pin70,Pin72,Pin74





BIOS_MODE

BIOS_DIS_SW	*BIOS_SEL_PCIESATA1*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI	*GPI*	*AUTO*



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Custom	M.2-SLOT1	10

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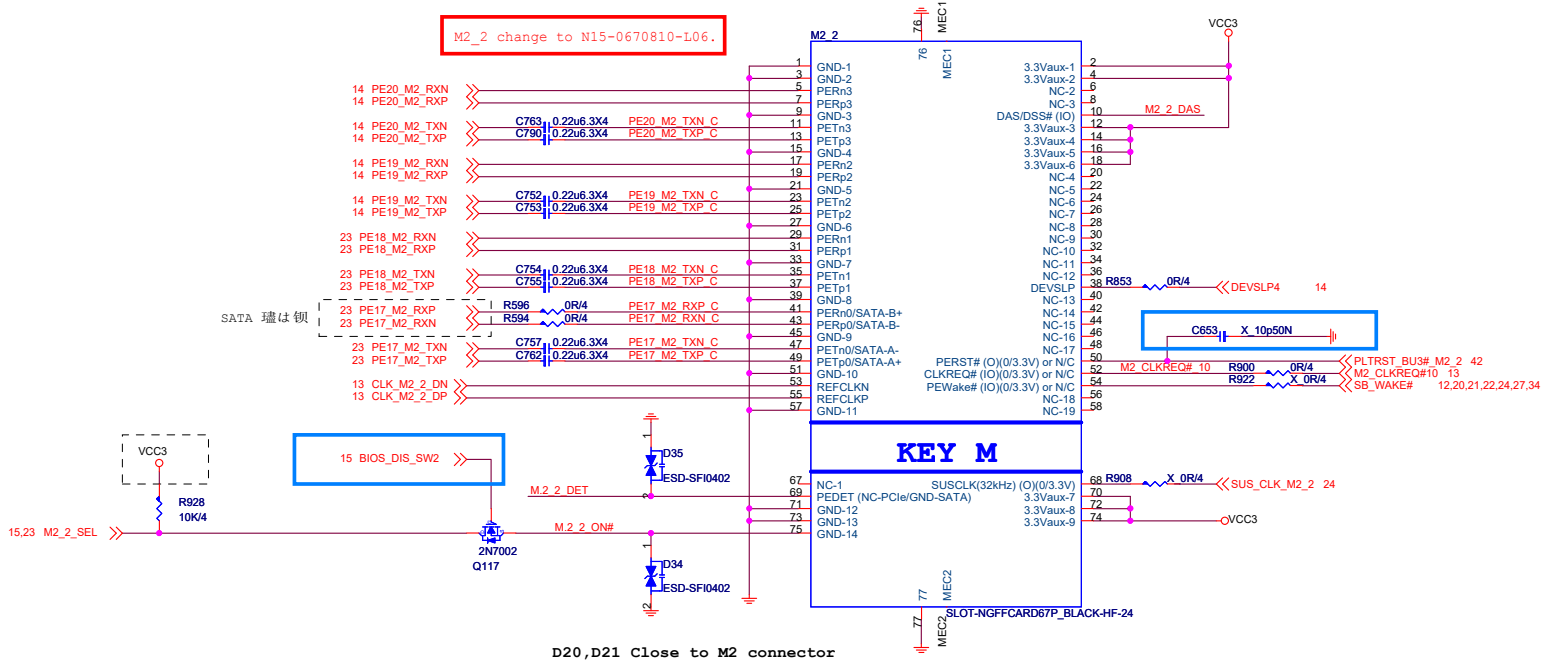
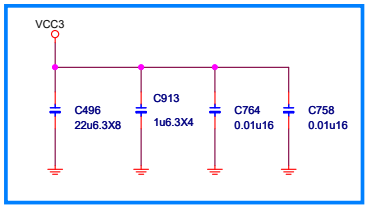
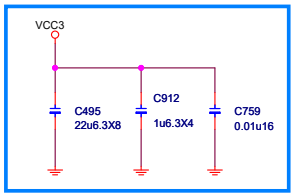


M.2 VCC3>=2.5A

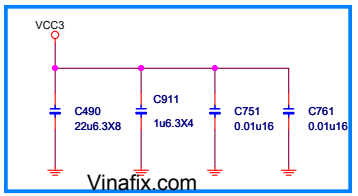
Near Pin2,Pin4



Near Pin12,Pin14,Pin16,Pin18



Near Pin70,Pin72,Pin74



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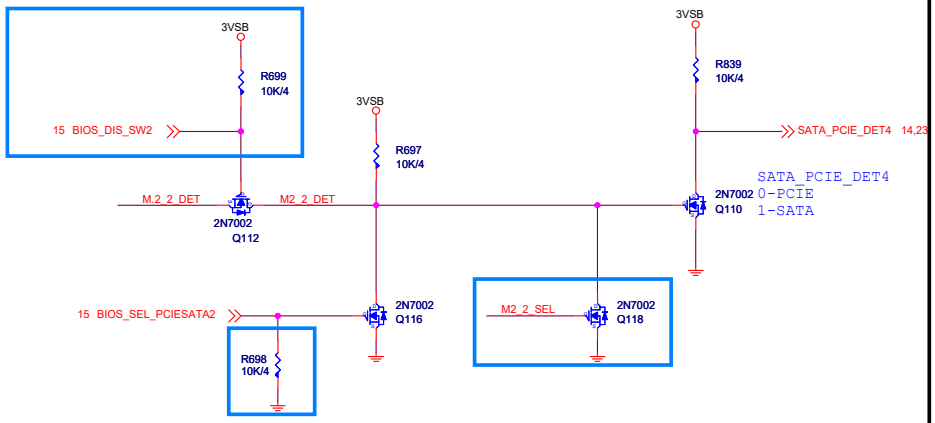
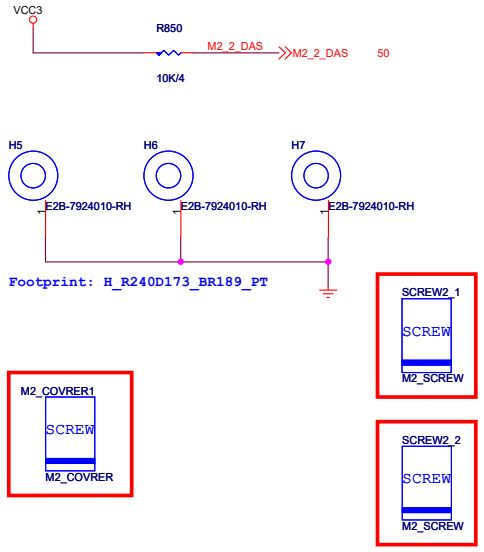


BIOS_MODE

BIOS_DIS_SW	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
0	*0*	*1*	***M2-SATA***
0	*0*	*0*	***M2-PCIE***
GPI	*GPI*	*GPI*	*AUTO*



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	M.2-SLOT2	10

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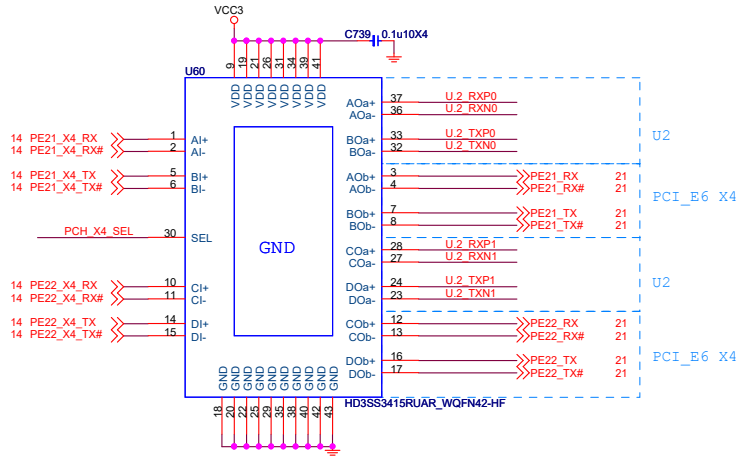
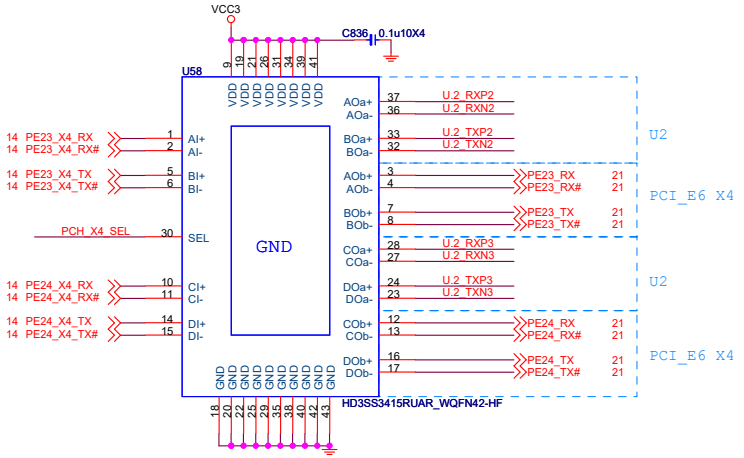
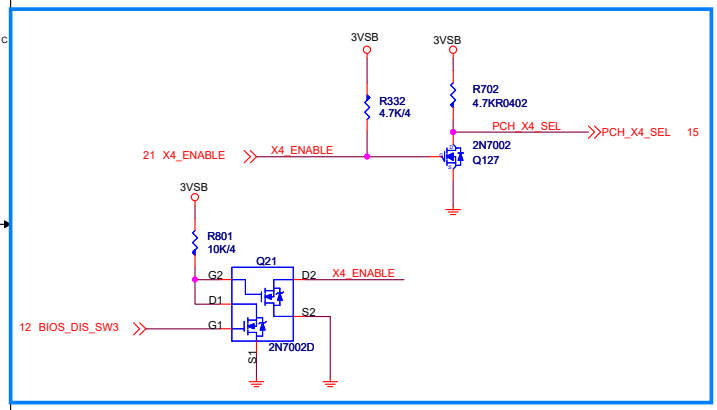
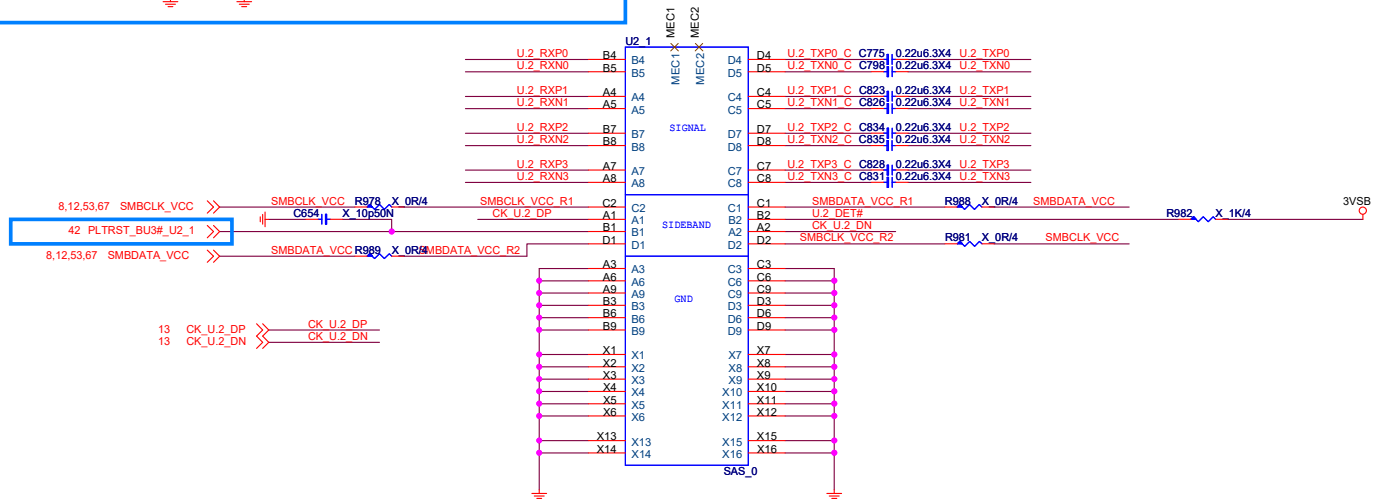


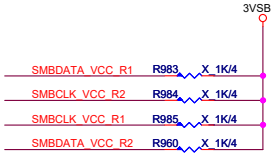




Default U.2 Working, PCIE X4 First.

MODE	BIOS_DIS_SW3	PCH_X4_SEL
AUTO	GPI	GPI
U.2 X4	GPO Low	GPO Low
PCIE X4	GPO Low	GPO High





MICRO-STAR INT'L CO.,LTD

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Custom	U.2 Connector	10

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Minimun gap should be greater of
>15mil with other signal.

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

USB HS (90Ohm-Diff)

Chip to Connector <1.5 inch.

USB SS (80Ohm-Diff)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

P/N:B02-021421C-AD0

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

ASM1142 RU29 stuff RU28 unstuff
ASM2142 RU29 unstuff RU28 stuff

ASM1142 RU14 stuff RU16 unstuff
ASM2142 RU14 unstuff RU16 stuff

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

ASM2142 UU8 stuff RU6 unstuff
ASM1142 UU8 unstuff RU6 stuff

Reset control for ASM2142 only.

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

ASM1142 RU3/RU4 100K/93.12K 1.24V
ASM2142 RU3/RU4 100K/100K 1.2V
ASM1042AE RU3/RU4 196K/261K 1.05V

ASM1142 1.2 VSB Power

ASM1142 RU33 18K 1.24V
ASM2142 RU33 19.6K 1.2V
ASM1042AE RU33 31.6K 1.05V

ASM1142/ASM1042 unstuff
ASM2142 stuff

EEPROM

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-25L1022-M24(1M bit)

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Custom	ASM 1142	10

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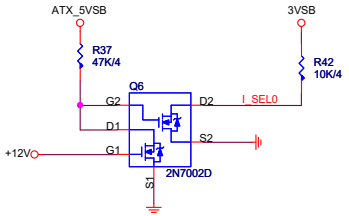
Current Mode

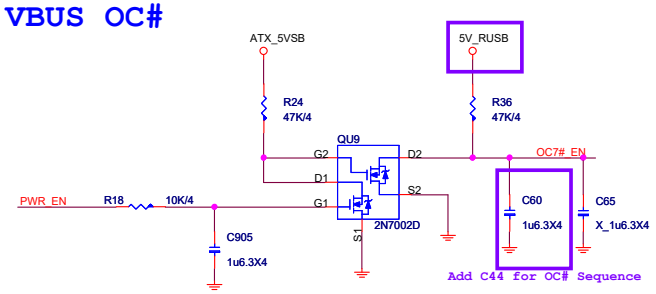


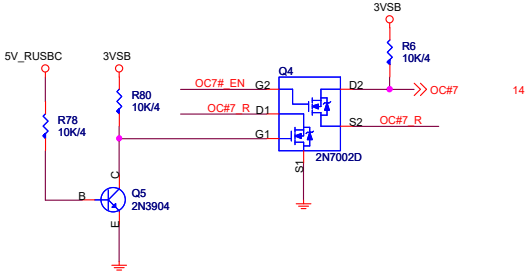
I_SEL0 : I_SEL1

X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

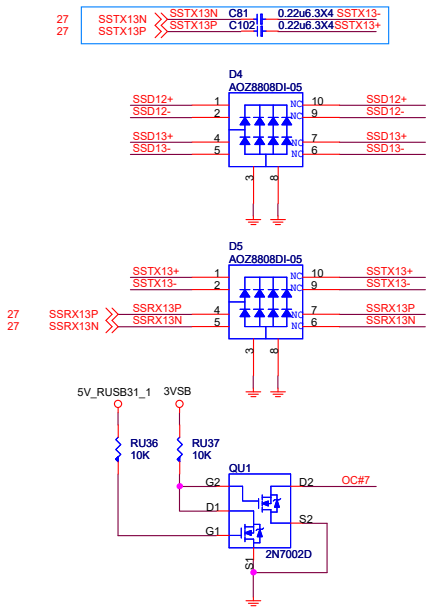
1.5A under S3 mode
3A under S0 mode

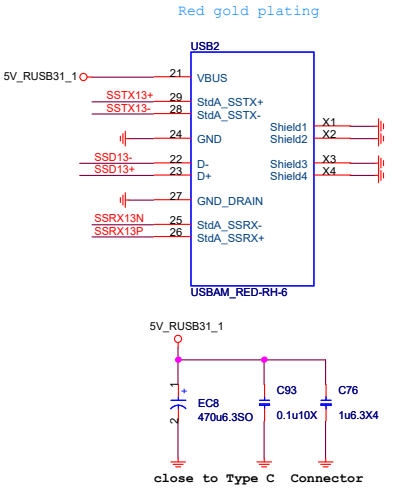
VBUS OC#



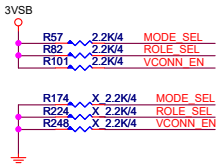


TYPE-A





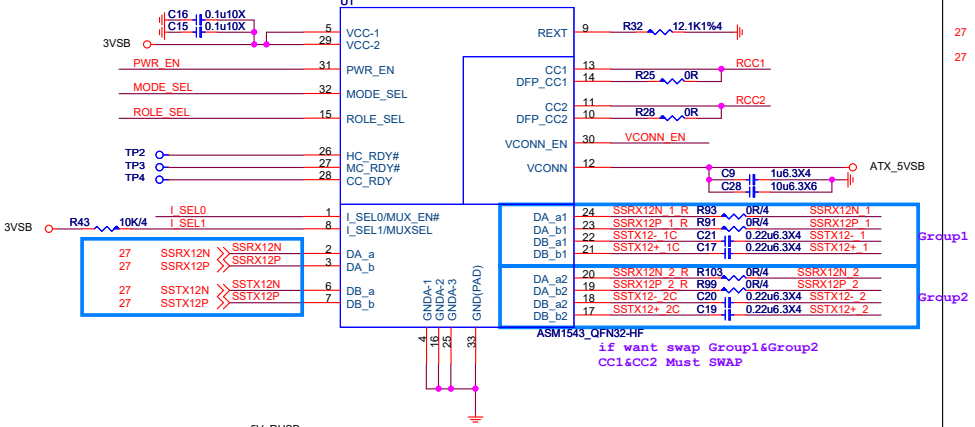
USB Type-C MUX with Configuration Channel (CC)

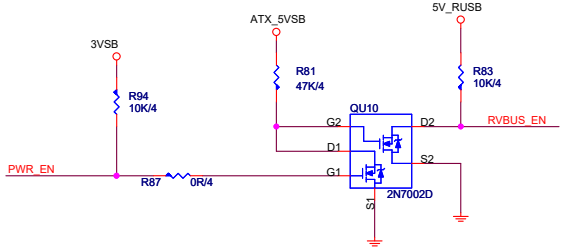


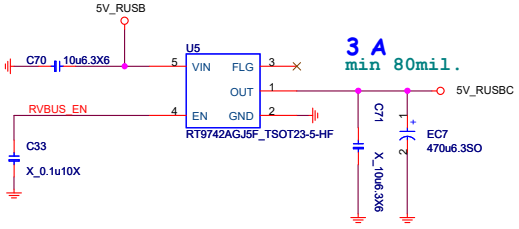
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable







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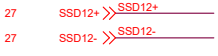
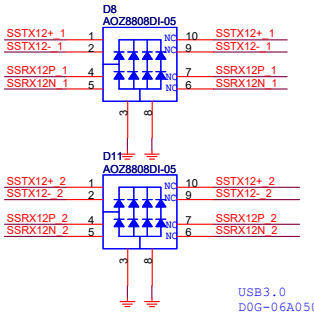
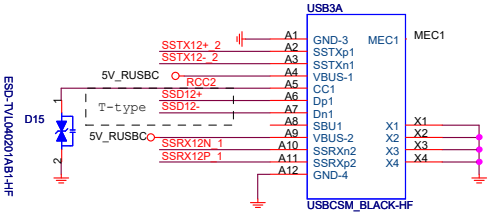
TYPE-C

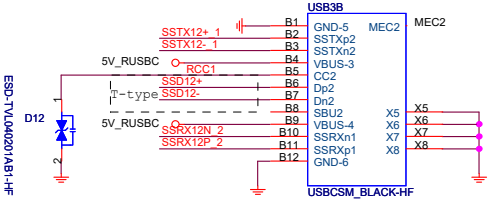




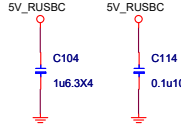
ESD Protection
NEAR CONNECTOR



T-type だや惠 140mils



close to Type C Connector



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL

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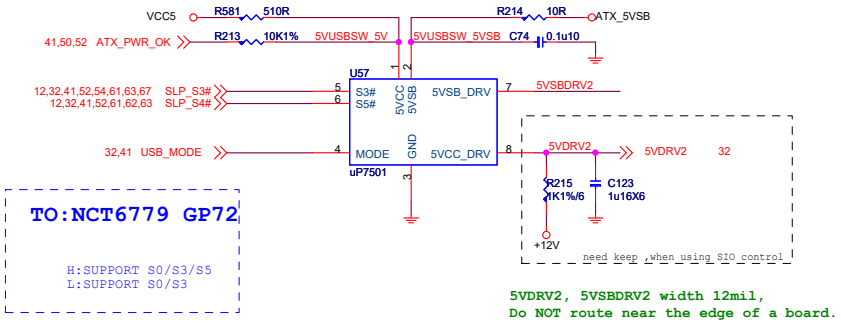
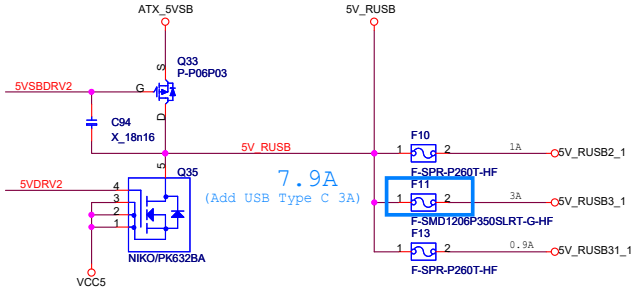
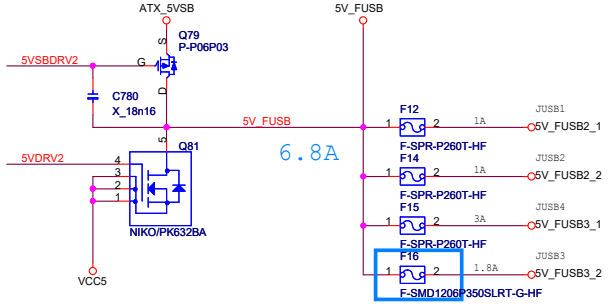
USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



need confirm C780 value



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-005
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

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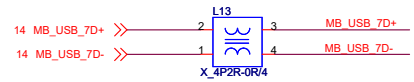

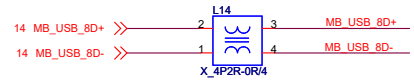

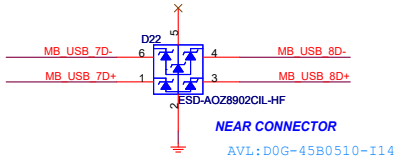

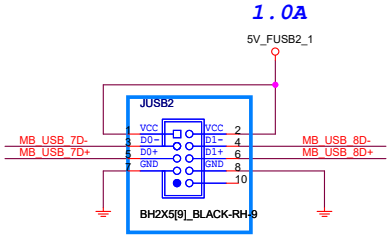

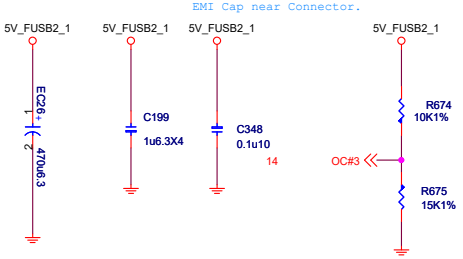

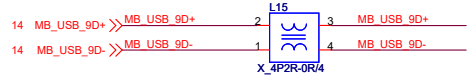

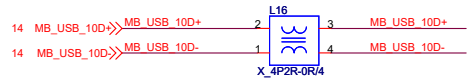

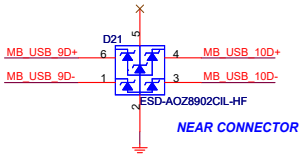

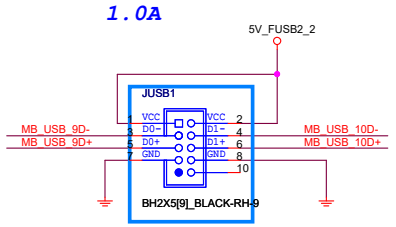

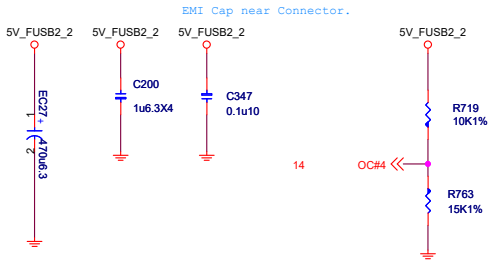

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MSI	MICRO-STAR INT'L CO.,LTD	
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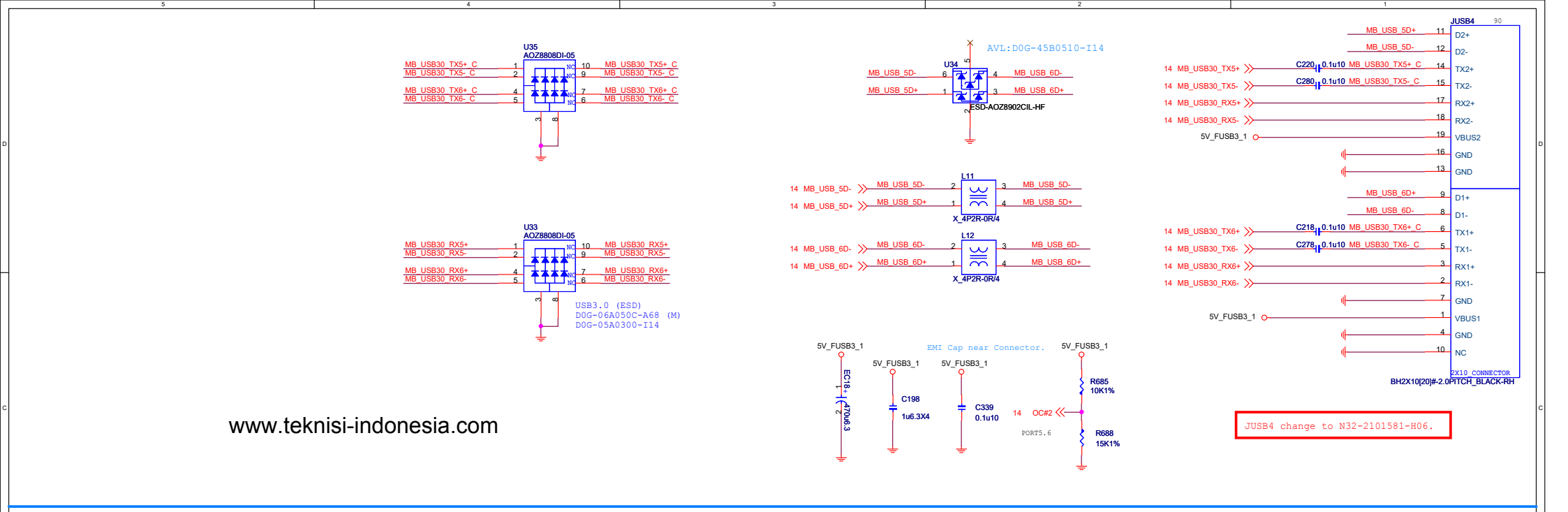
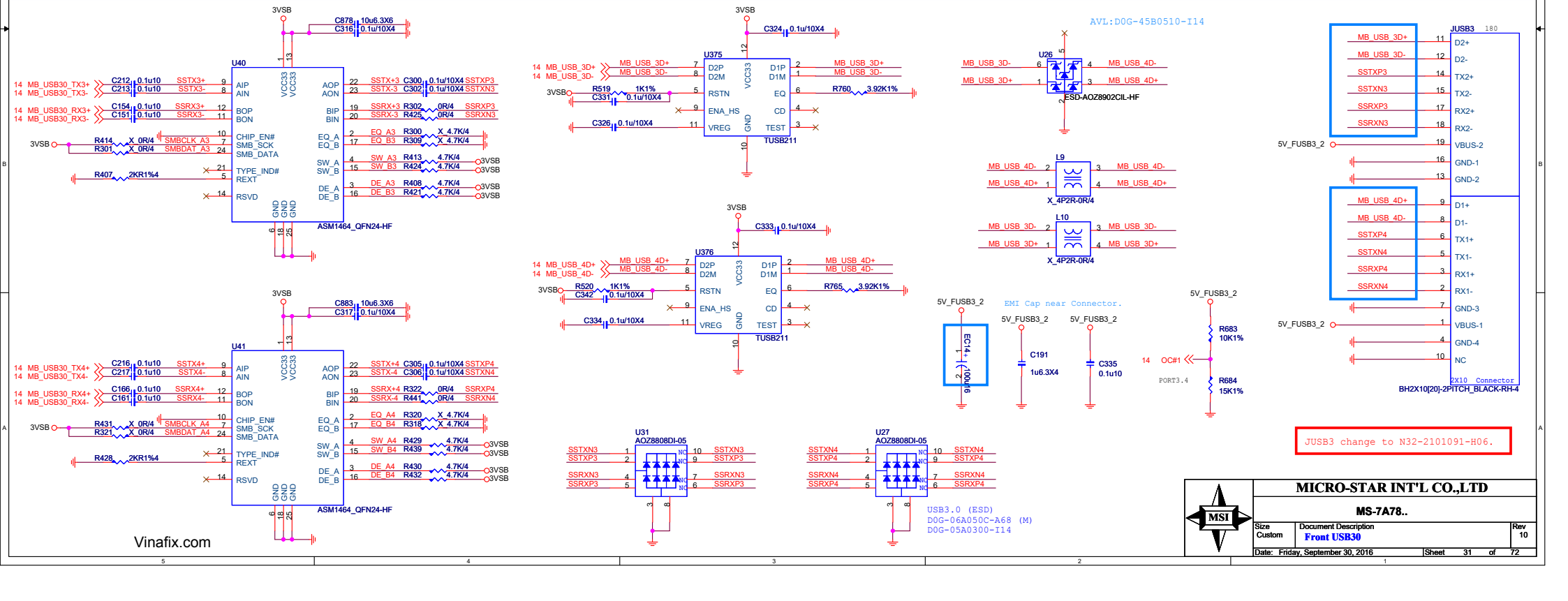

U35
AOZ8808DI-05
MB_USB30_TX5+_C
MB_USB30_TX5-_C
MB_USB30_TX6+_C
MB_USB30_TX6-_C
U33
AOZ8808DI-05
MB_USB30_RX5+
MB_USB30_RX5-
MB_USB30_RX6+
MB_USB30_RX6-
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
AVL:D0G-45B0510-I14
U34
MB_USB_5D-
MB_USB_5D+
MB_USB_6D-
MB_USB_6D+
ESD-AOZ8902CIL-HF
L11
X_4P2R-0R/4
L12
X_4P2R-0R/4
JUSB4
90
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS2
GND
D1+
D1-
TX1+
TX1-
RX1+
RX1-
VBUS1
NC
2X10_CONNECTOR
BH2X10[20]#-2.0PITCH_BLACK-RH
5V_FUSB3_1
EMI Cap near Connector.
EC18
470u6.3
C198
1u6.3X4
C339
0.1u10
OC#2
PORT5.6
R685
10K1%
R688
15K1%
JUSB4 change to N32-2101581-H06.
www.teknisi-indonesia.com


3VSB
U40
ASM1464_QFN24-HF
U41
ASM1464_QFN24-HF
U375
TUSB211
U376
TUSB211
AVL:D0G-45B0510-I14
U26
ESD-AOZ8902CIL-HF
L9
L10
X_4P2R-0R/4
JUSB3
180
D2+
D2-
TX2+
TX2-
RX2+
RX2-
VBUS-2
GND-1
GND-2
D1+
D1-
TX1+
TX1-
RX1+
RX1-
GND-3
VBUS-1
GND-4
NC
2X10_Connector
BH2X10[20]-2PITCH_BLACK-RH-4
5V_FUSB3_2
EMI Cap near Connector.
EC14
C191
1u6.3X4
C335
0.1u10
OC#1
PORT3.4
R683
10K1%
R684
15K1%
U31
AOZ8808DI-05
U27
AOZ8808DI-05
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
JUSB3 change to N32-2101091-H06.
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Size
Custom
Document Description
Front USB30
Rev
10
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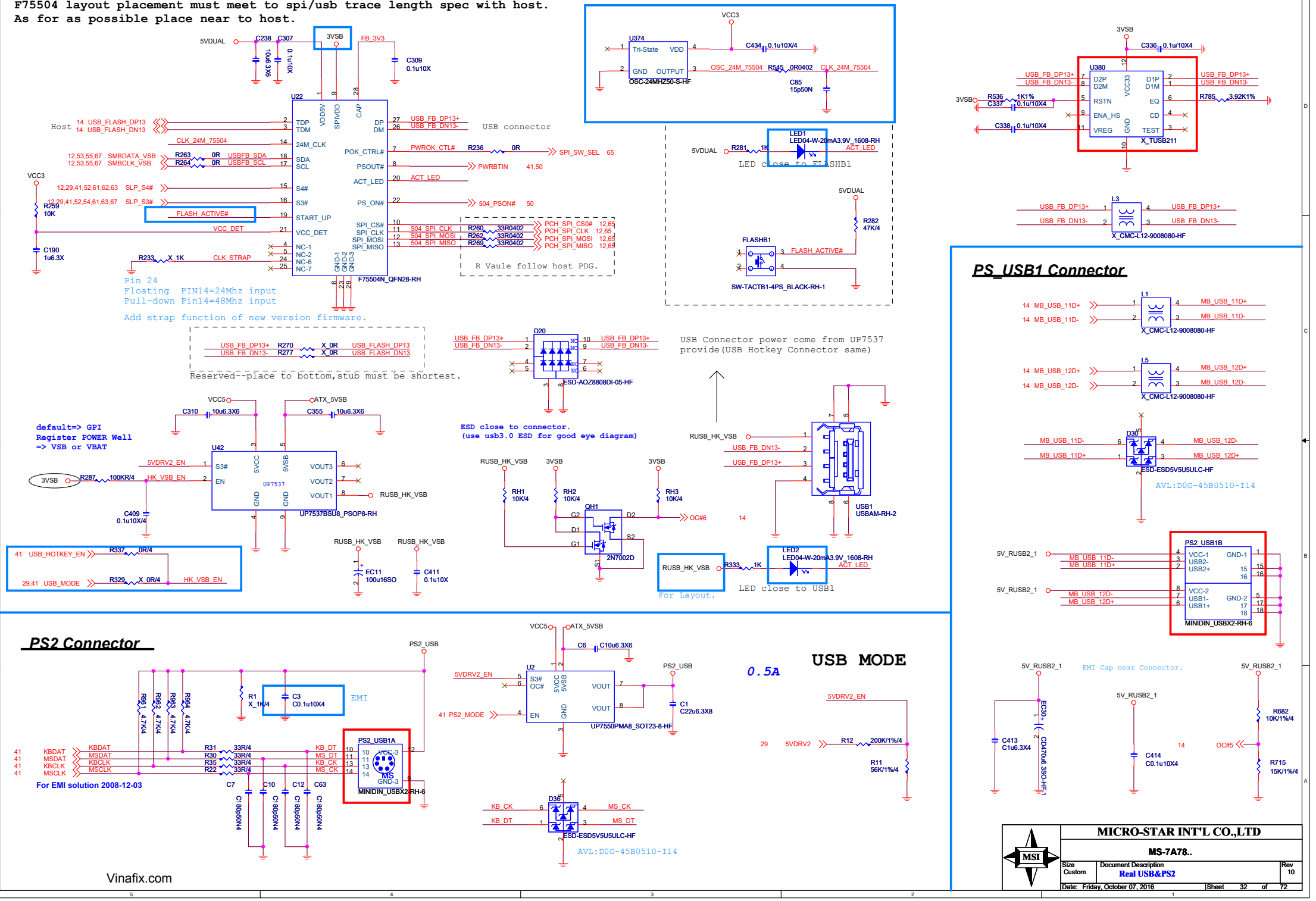
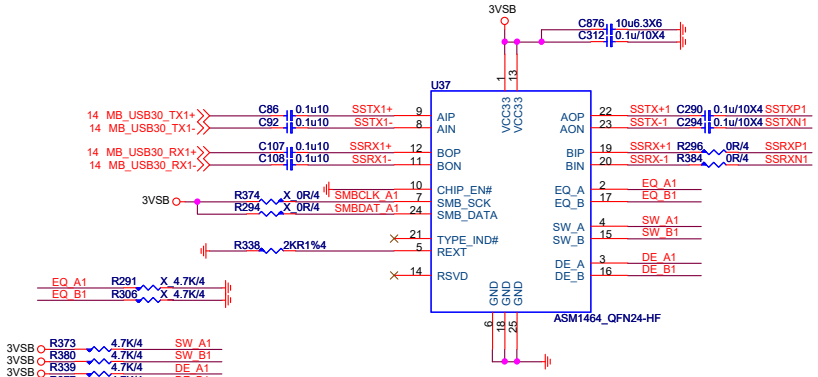
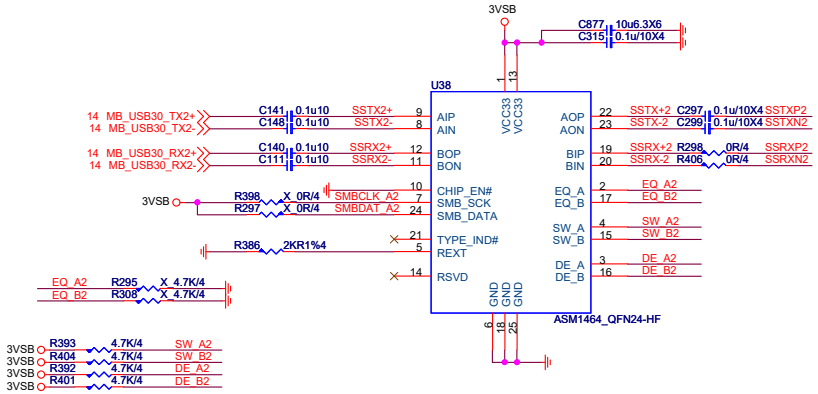
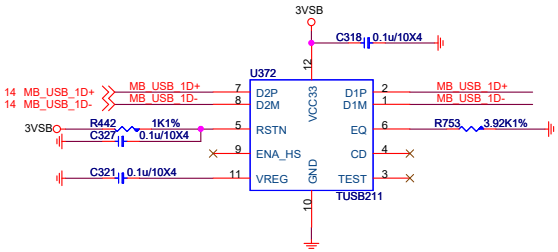
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

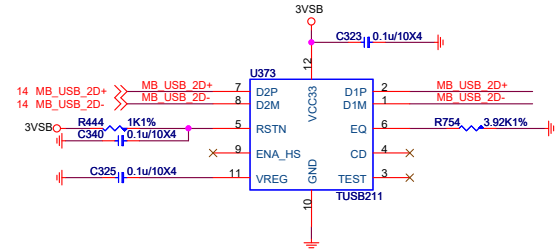


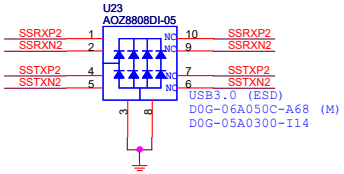
LAN USB3.0

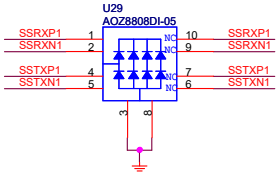


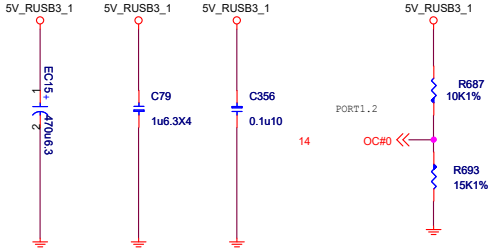


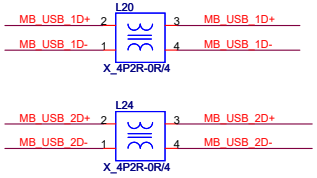


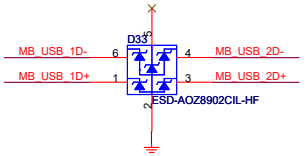




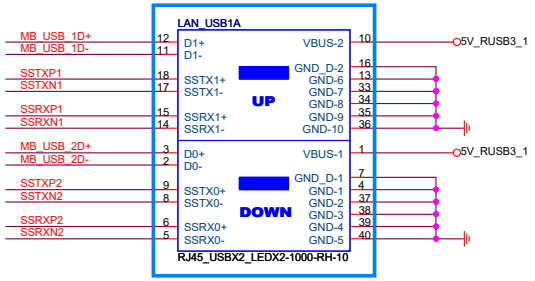








AVL:D0G-45B0510-I14



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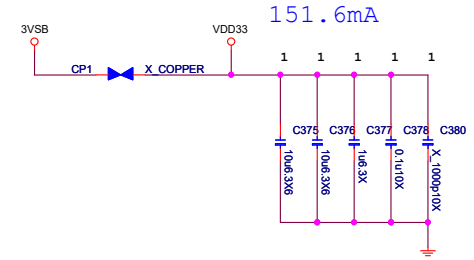
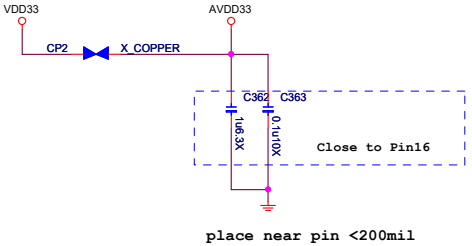
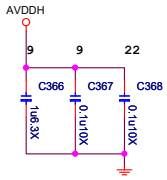
E2400 GIGA LAN

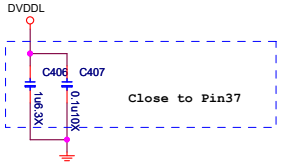




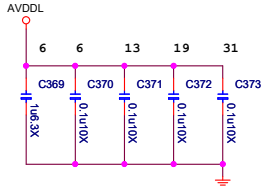
place near pin <200mil



place near pin <200mil



place near pin <200mil



place near pin <200mil

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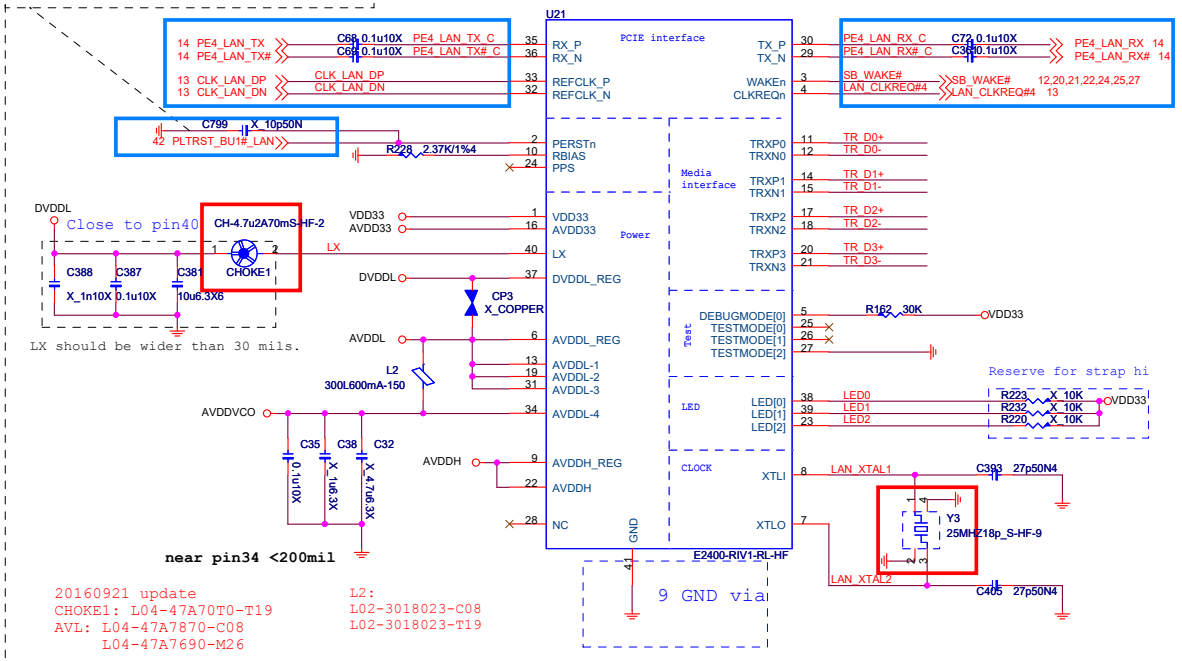
PIN2:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#,

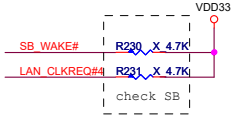
E2500:B06-E25000C-R54
E2400:B06-E24000C-R54



near pin34 <200mil

20160921 update
CHOKE1: L04-47A70T0-T19
AVL: L04-47A7870-C08
L04-47A7690-M26

L2:
L02-3018023-C08
L02-3018023-T19



note:

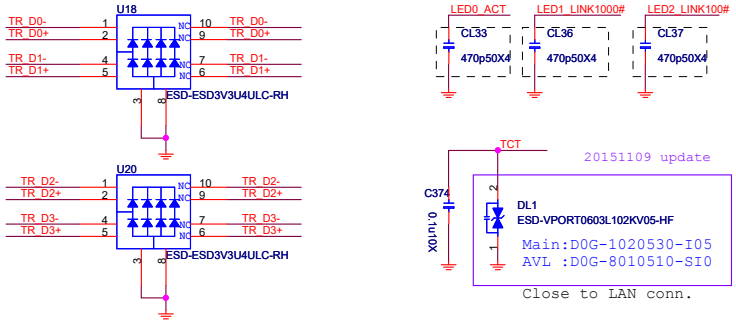
LED0:
1=High core voltage
0=Low core voltage

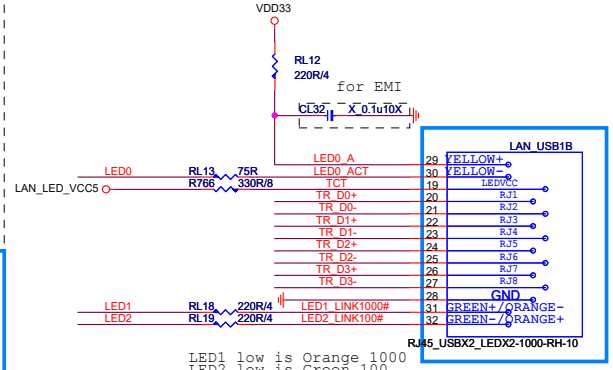
LED1:
1=SWR mode
0=LDO mode

LED2:
1=25MHz clock
0=48MHz clock

VDD33 >= 30mils;
AVDD33 >= 30mils;
AVDDH >= 20mils;
AVDDL >= 20mils.
DVDDL >= 20mils.
Pin LX to L1 >= 30mils.

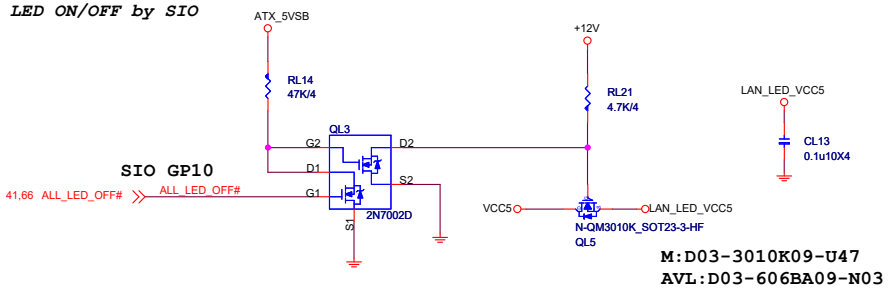
EMC





LED1 low is Orange 1000
LED2 low is Green 100

LED ON/OFF by SIO



M:D03-3010K09-U47
AVL:D03-606BA09-N03

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MS-7A78..

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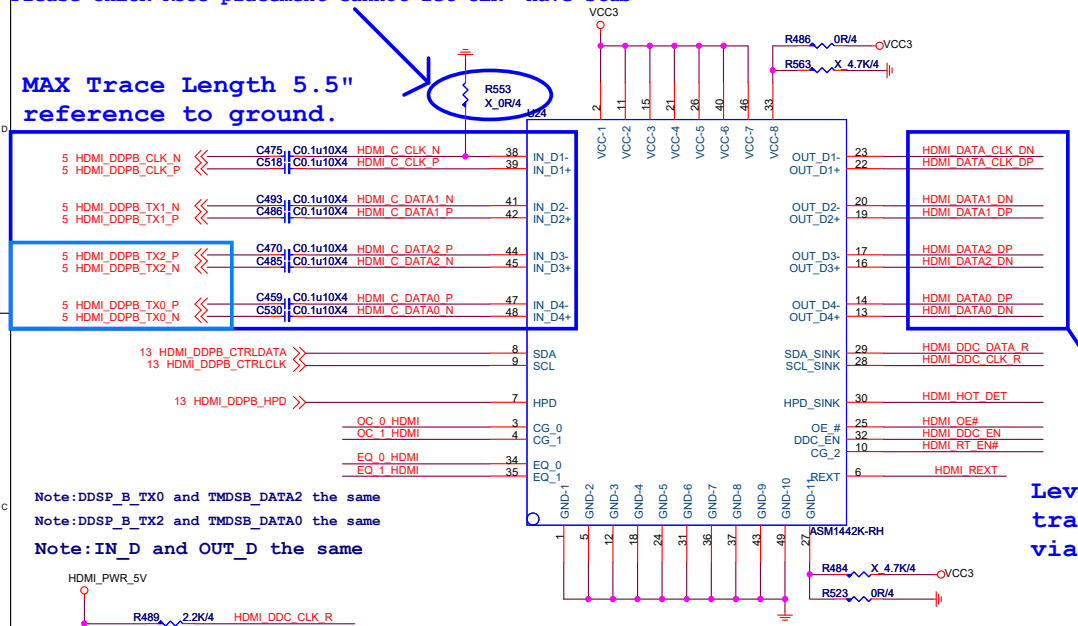
HDMI level shifter

Please CHECK R553 placement cannot let CLK- have stub

MAX Trace Length 5.5" reference to ground.



Note:DDSP_B_TX0 and TMDSB_DATA2 the same

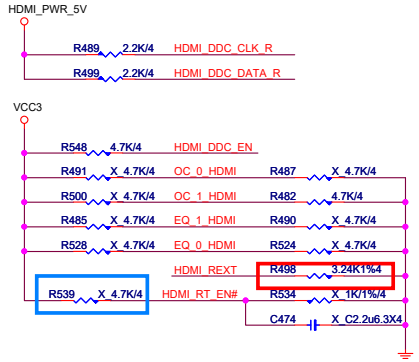
Note:DDSP_B_TX2 and TMDSB_DATA0 the same

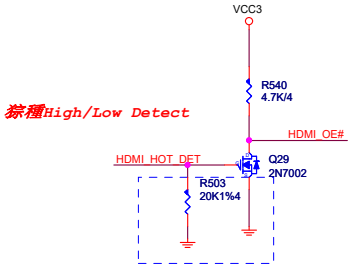
Note:IN_D and OUT_D the same

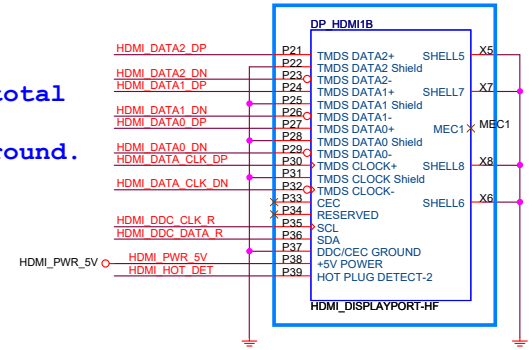
Level Shift to HDMI connector total trace length > 0.9〞 ; < 1〞 via count ∝ 2 ,reference to ground.

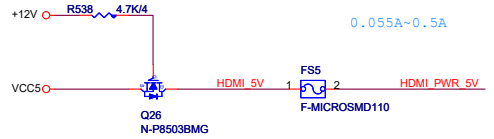
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	







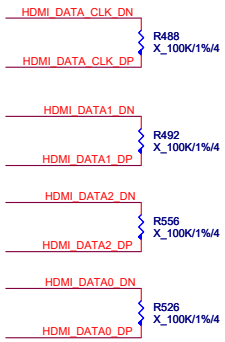


	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

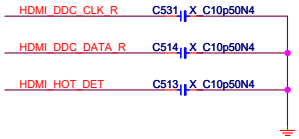
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

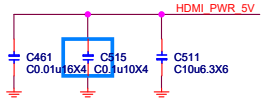
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

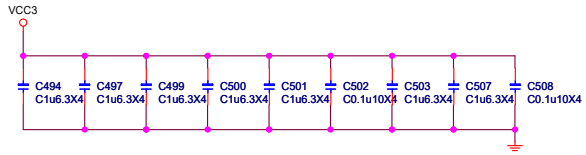
EMI



EMI cap.







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MS-7A78..		
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MS-7A78..		
Size: Custom	Document Description: HDMI Connector	Rev: 10
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ALC1220

P/N:B05-012201C-R09

UA1

ALC1220-CG-RH

follow PCH power well

all of JD resistors should be placed as close as possible to the sense pin of codec.

AUDIO1E

AUDIO1B

AUDIO1D

AUDIO1A

AUDIO1F

AUDIO1C

near JACK

CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

CPVDD:150mA

Closed Codec

EMI

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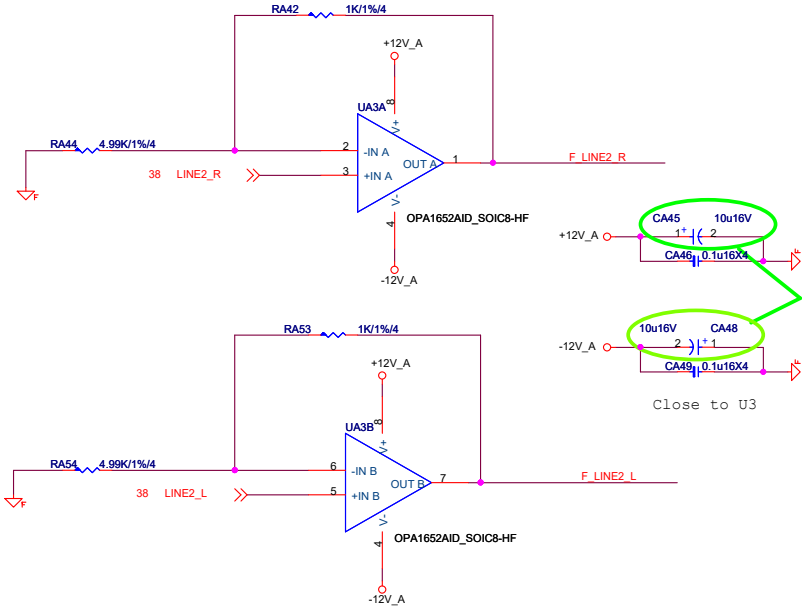
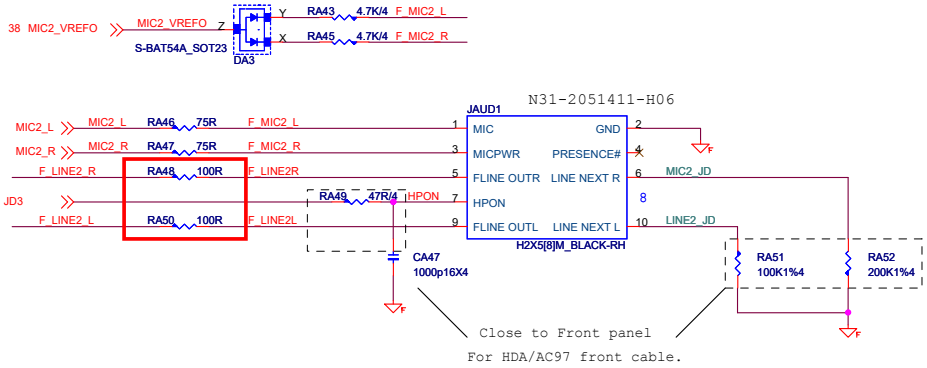
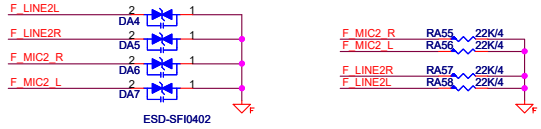




Close to Jack

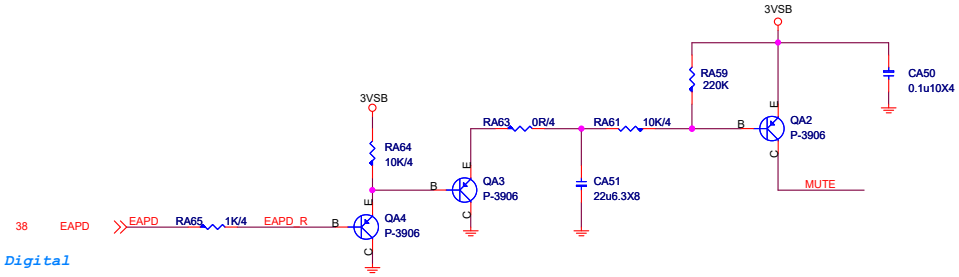
ESD protect

D0G-2950500-SI0
D0G-3010510-I05

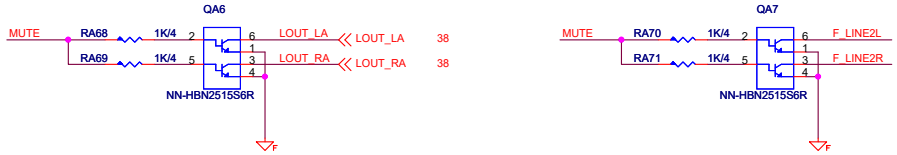


Rear Line OUT De-POP circuit

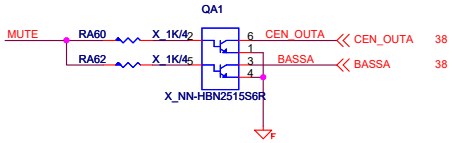
(De-pop circuit for Rear Line out & Front Headphone out)

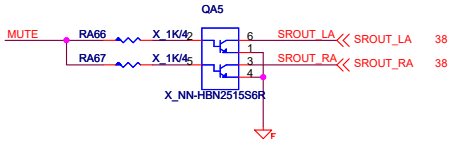


Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)





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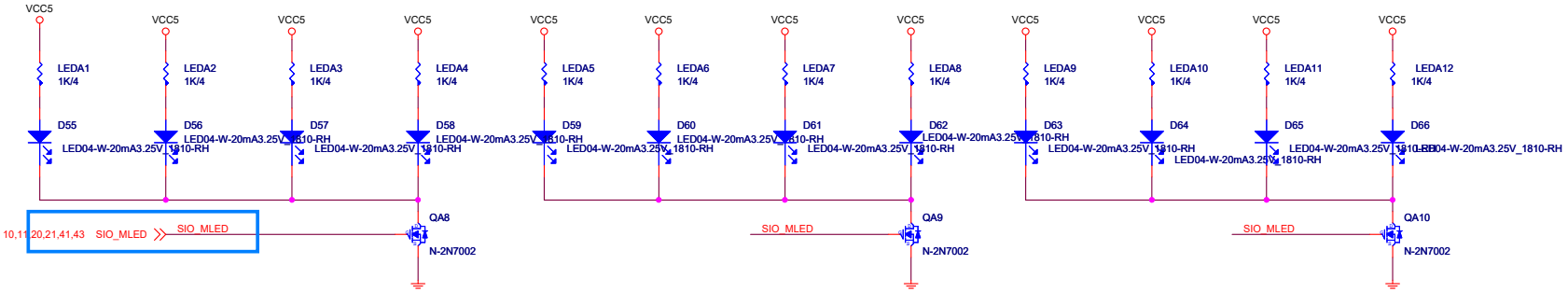
Audio moat is transparent and width 40mil



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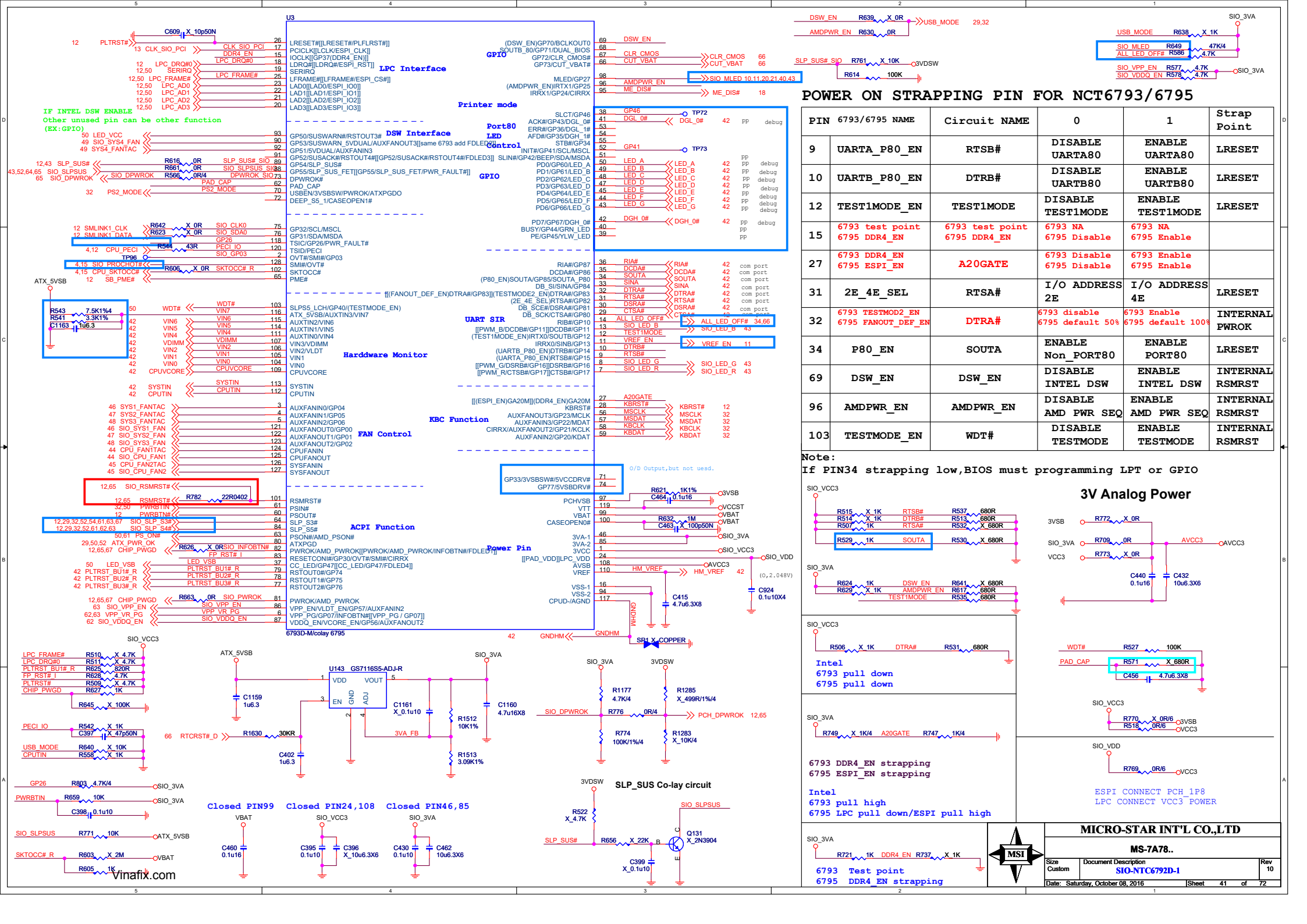
U3
6793D-M/colay 6795
LPC Interface
DSW Interface
GPIO
Printer mode
Port80
LED
Control
UART SIR
Harddware Monitor
FAN Control
KBC Function
ACPI Function
Power Pin
IF INTEL DSW ENABLE
Other unused pin can be other function
(EX:GPIO)
POWER ON STRAPPING PIN FOR NCT6793/6795
PIN | 6793/6795 NAME | Circuit NAME | 0 | 1 | Strap Point
9 | UARTA_P80_EN | RTSB# | DISABLE UARTA80 | ENABLE UARTA80 | LRESET
10 | UARTB_P80_EN | DTRB# | DISABLE UARTB80 | ENABLE UARTB80 | LRESET
12 | TEST1MODE_EN | TEST1MODE | DISABLE TEST1MODE | ENABLE TEST1MODE | LRESET
15 | 6793 test point 6795 DDR4_EN | 6793 test point 6795 DDR4_EN | 6793 NA 6795 Disable | 6793 NA 6795 Enable |
27 | 6793 DDR4_EN 6795 ESPI_EN | A20GATE | 6793 Disable 6795 Disable | 6793 Enable 6795 Enable |
31 | 2E_4E_SEL | RTSA# | I/O ADDRESS 2E | I/O ADDRESS 4E | LRESET
32 | 6793 TESTMOD2_EN 6795 FANOUT_DEF_EN | DTRA# | 6793 disable 6795 default 50% | 6793 Enable 6795 default 100% | INTERNAL PWROK
34 | P80_EN | SOUTA | ENABLE Non_PORT80 | ENABLE PORT80 | LRESET
69 | DSW_EN | DSW_EN | DISABLE INTEL DSW | ENABLE INTEL DSW | INTERNAL RSMRST
96 | AMDPWR_EN | AMDPWR_EN | DISABLE AMD PWR SEQ | ENABLE AMD PWR SEQ | INTERNAL RSMRST
103 | TESTMODE_EN | WDT# | DISABLE TESTMODE | ENABLE TESTMODE | INTERNAL RSMRST
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO
3V Analog Power
Intel
6793 pull down
6795 pull down
6793 DDR4_EN strapping
6795 ESPI_EN strapping
Intel
6793 pull high
6795 LPC pull down/ESPI pull high
6793 Test point
6795 DDR4_EN strapping
Closed PIN99
Closed PIN24,108
Closed PIN46,85
SLP_SUS Co-lay circuit
ESPI CONNECT PCH_1P8
LPC CONNECT VCC3_POWER
MICRO-STAR INT'L CO.,LTD
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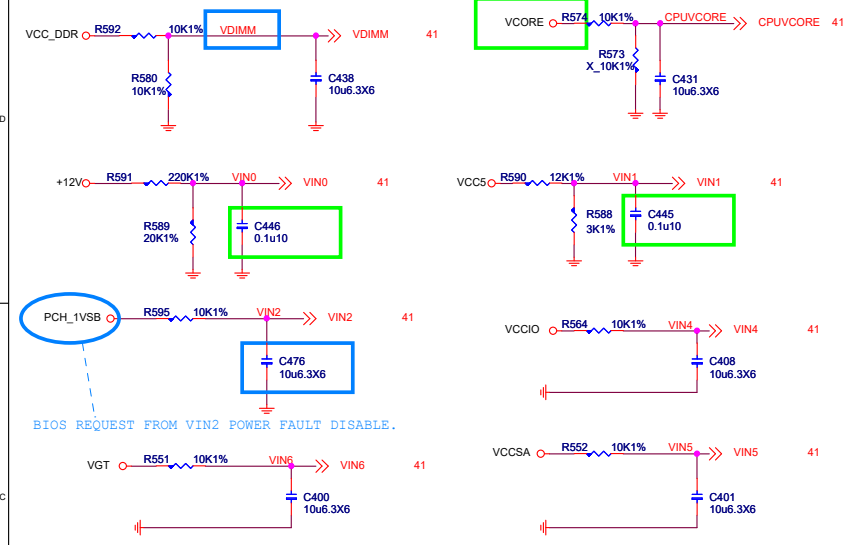
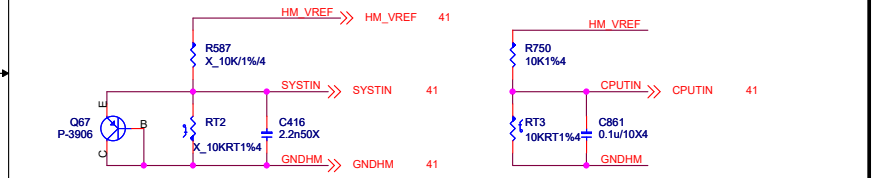
HW Monitor - Voltage

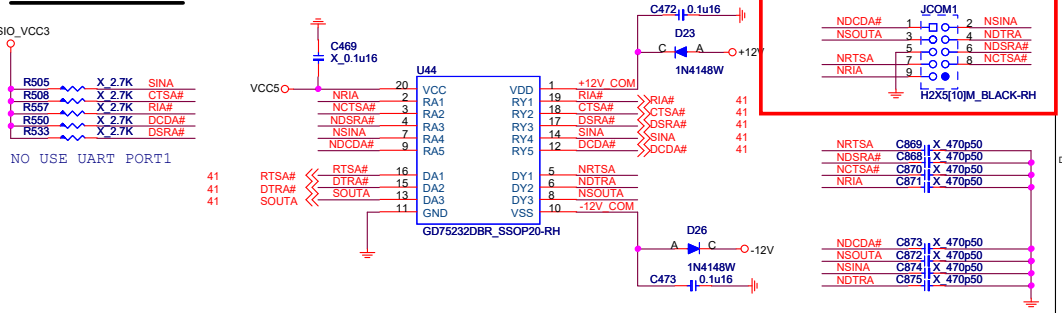
SIO HM Voltage voer 2V will not detect



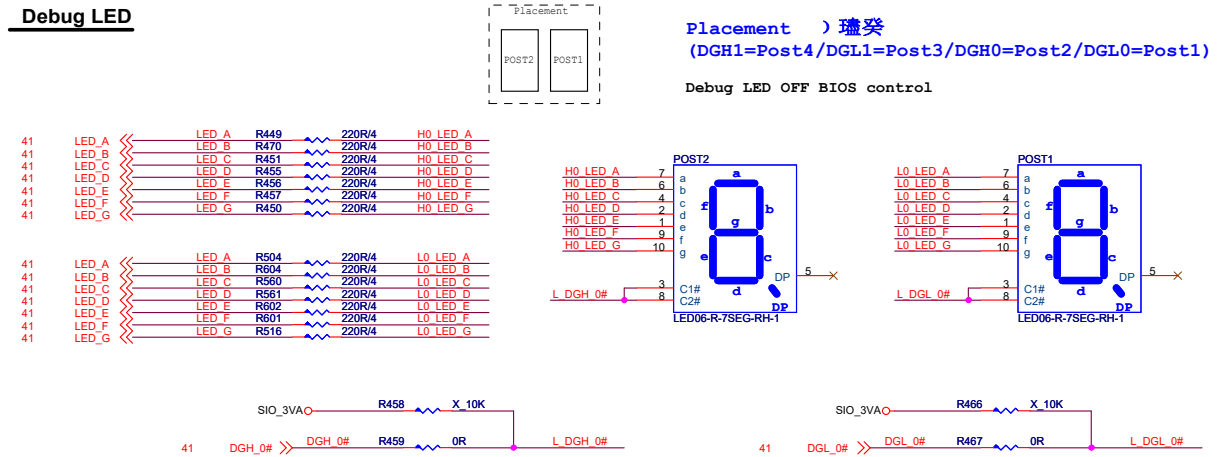
Thermal Monitor

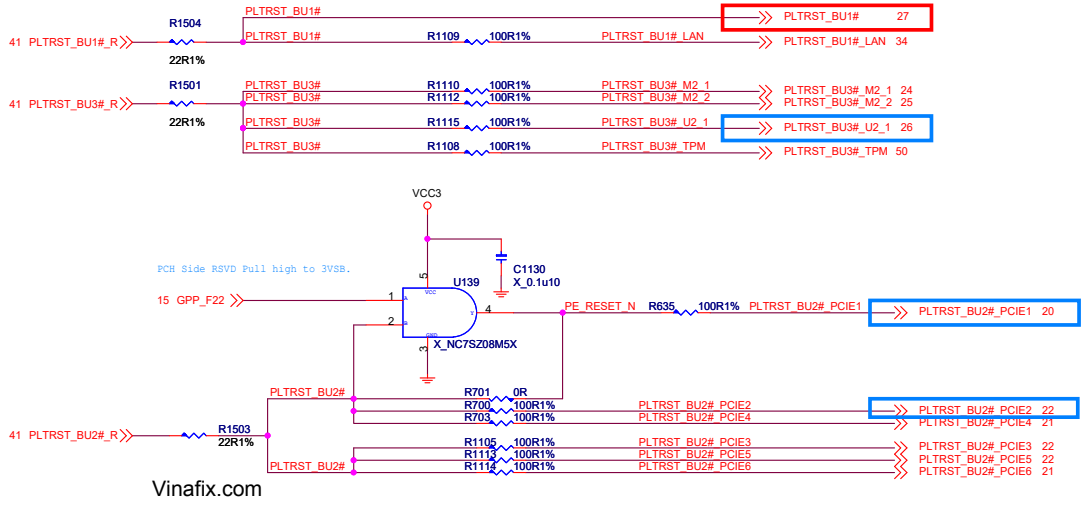


SERIAL PORT 1



Debug LED





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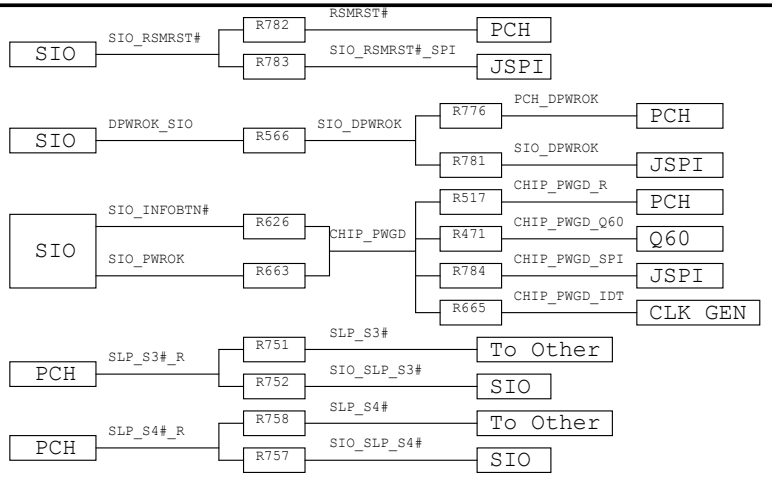

For Signals Monotonic

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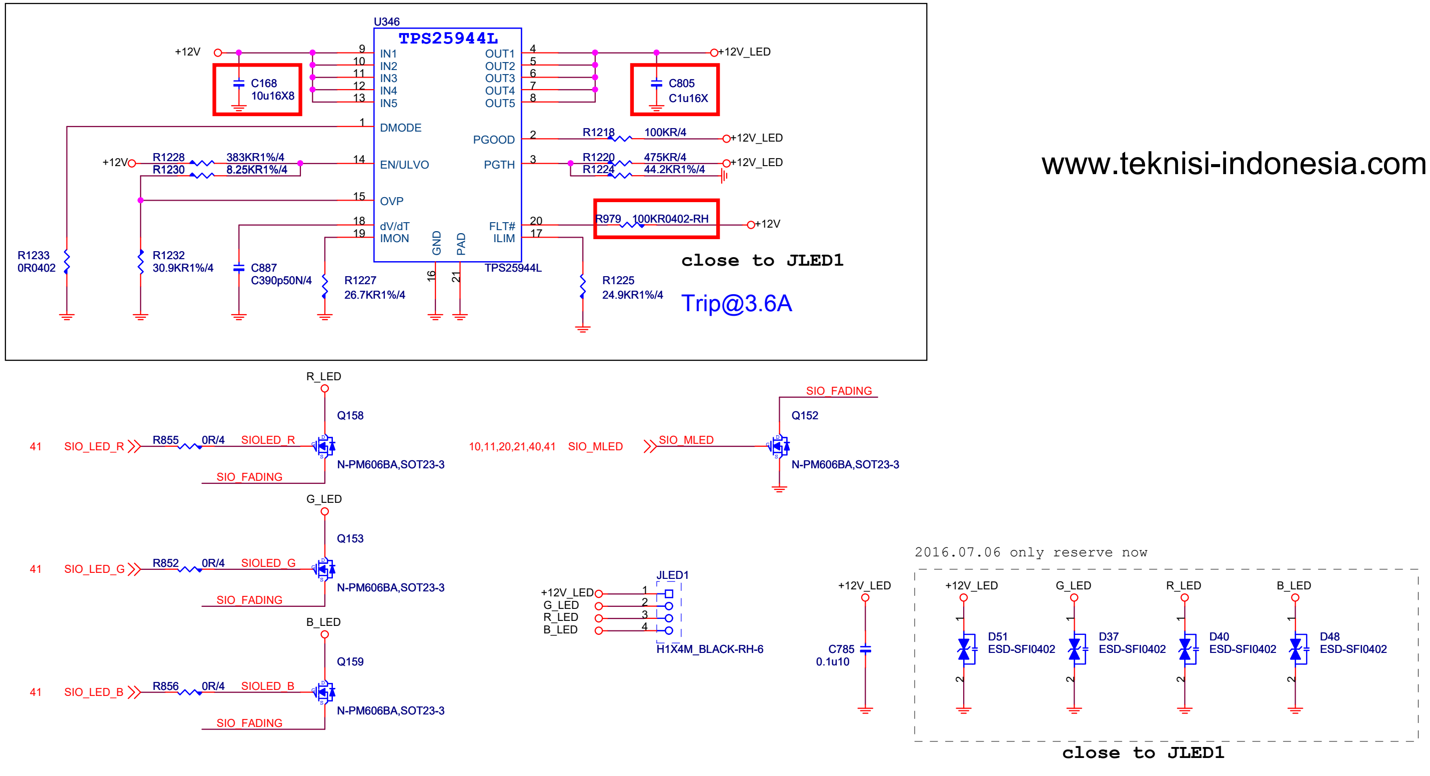
LED Control by SIO

2016.07.06 Use TPS25944L



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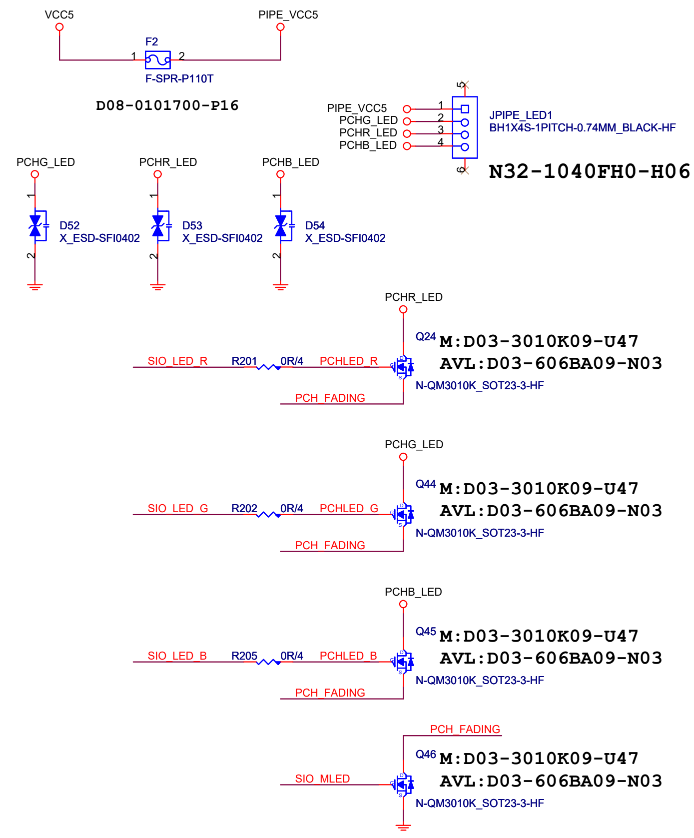
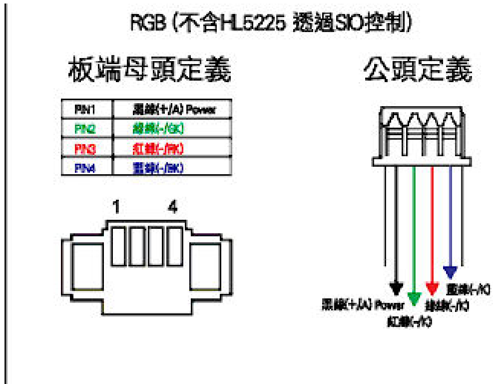
PCH Heatsink RGB LED

PIPE_VCC5 > 40mil

PIPE_VCC5 please check your Heatsink LED USE

RGB = 粲球0.06A x 顆縊计





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Size: Custom | Document Description: SIO-NTC6792D-2 | Rev: 10

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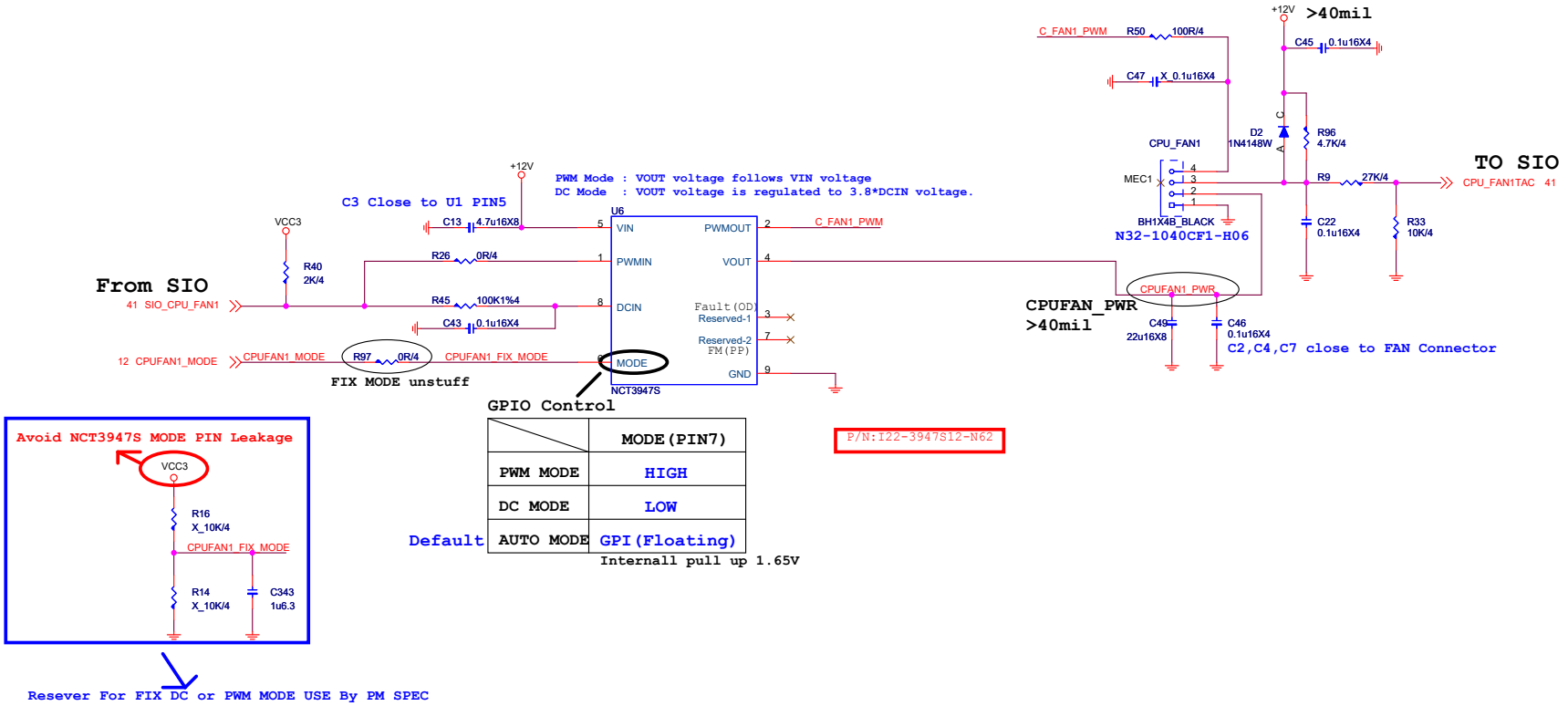
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE



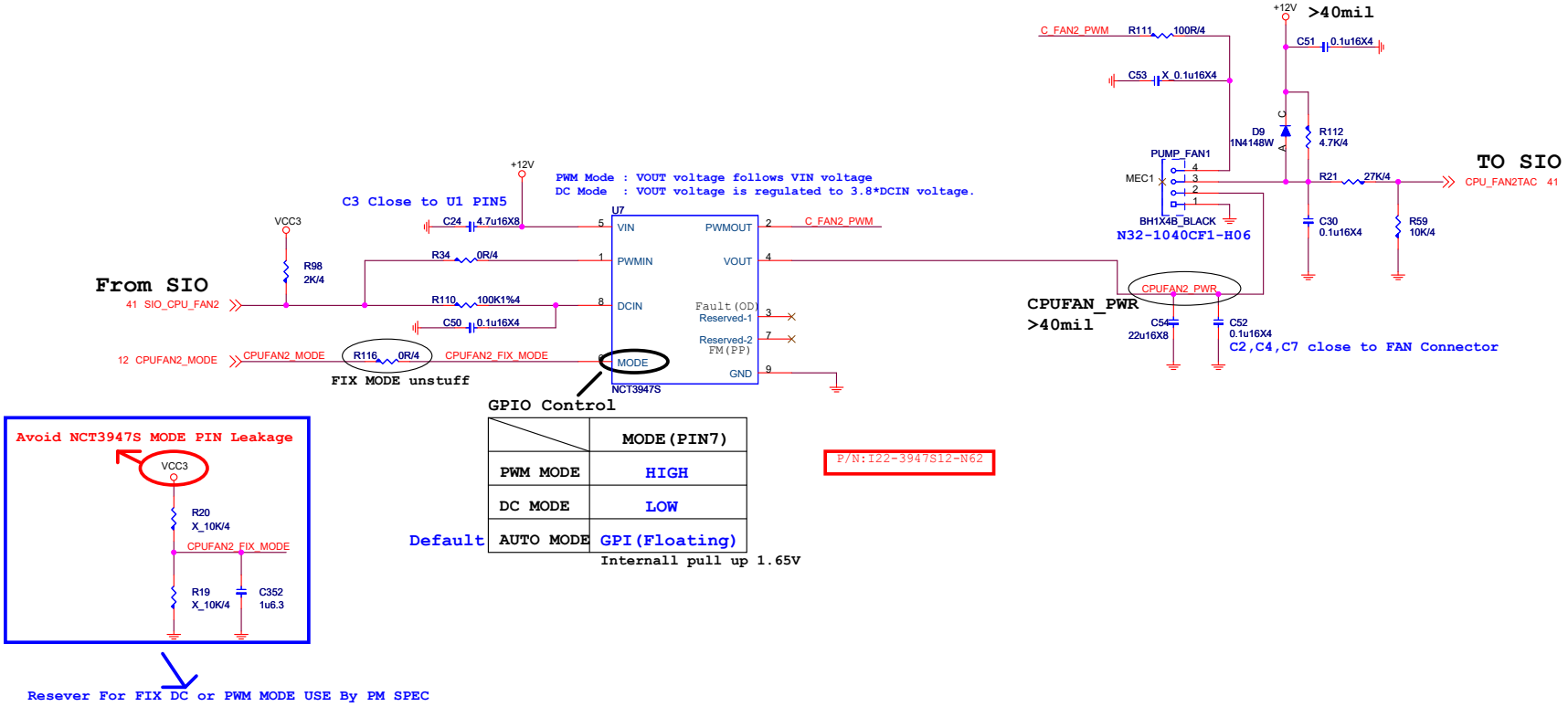
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD	
MS-7A78..	
Size: Custom	Document Description: CPU FAN1
Rev: 10	
Date: Monday, September 26, 2016	Sheet 44 of 72

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

P/N:I22-3947S12-N62

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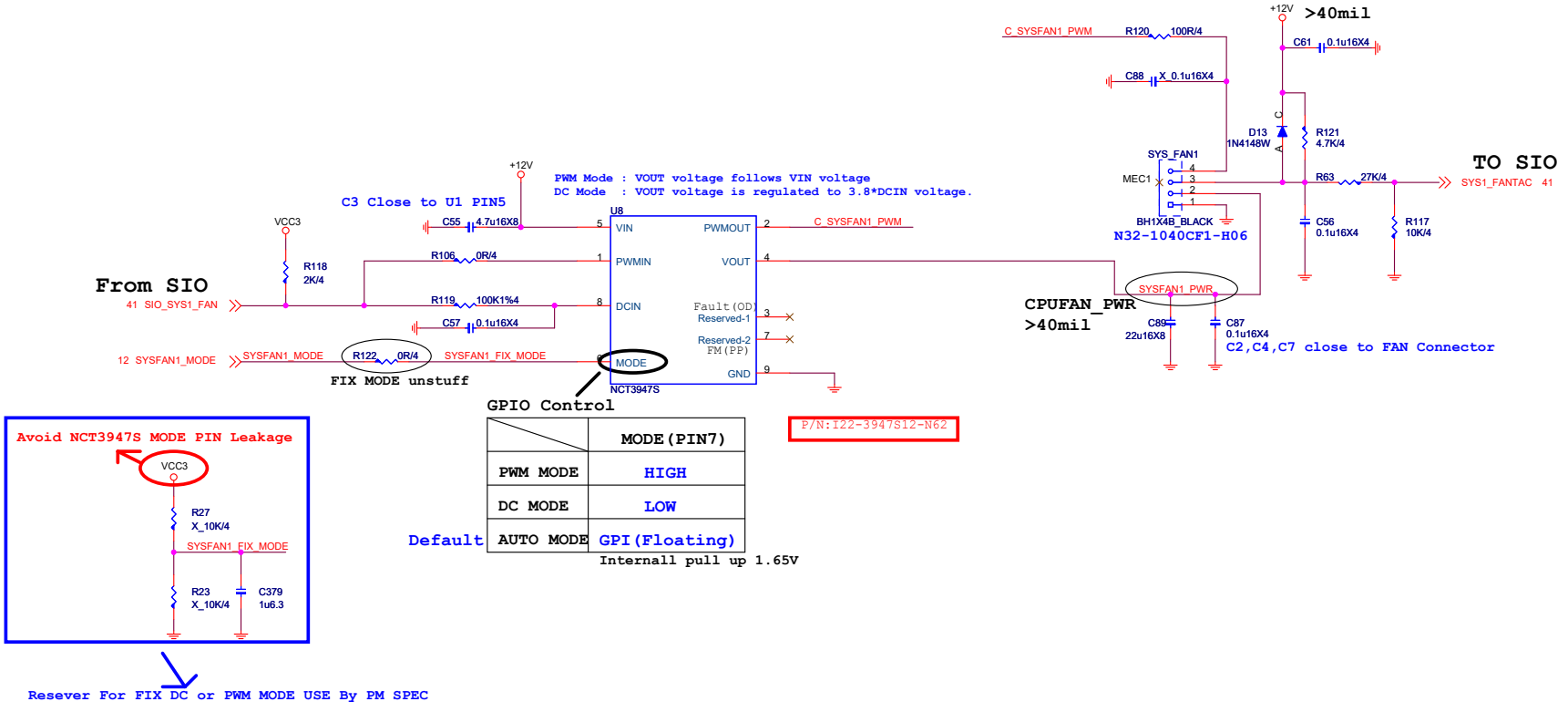
MS-7A78..		
Size: Custom	Document Description: CPU FAN2	Rev: 10
Date: Monday, September 26, 2016	Sheet 45 of 72	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE



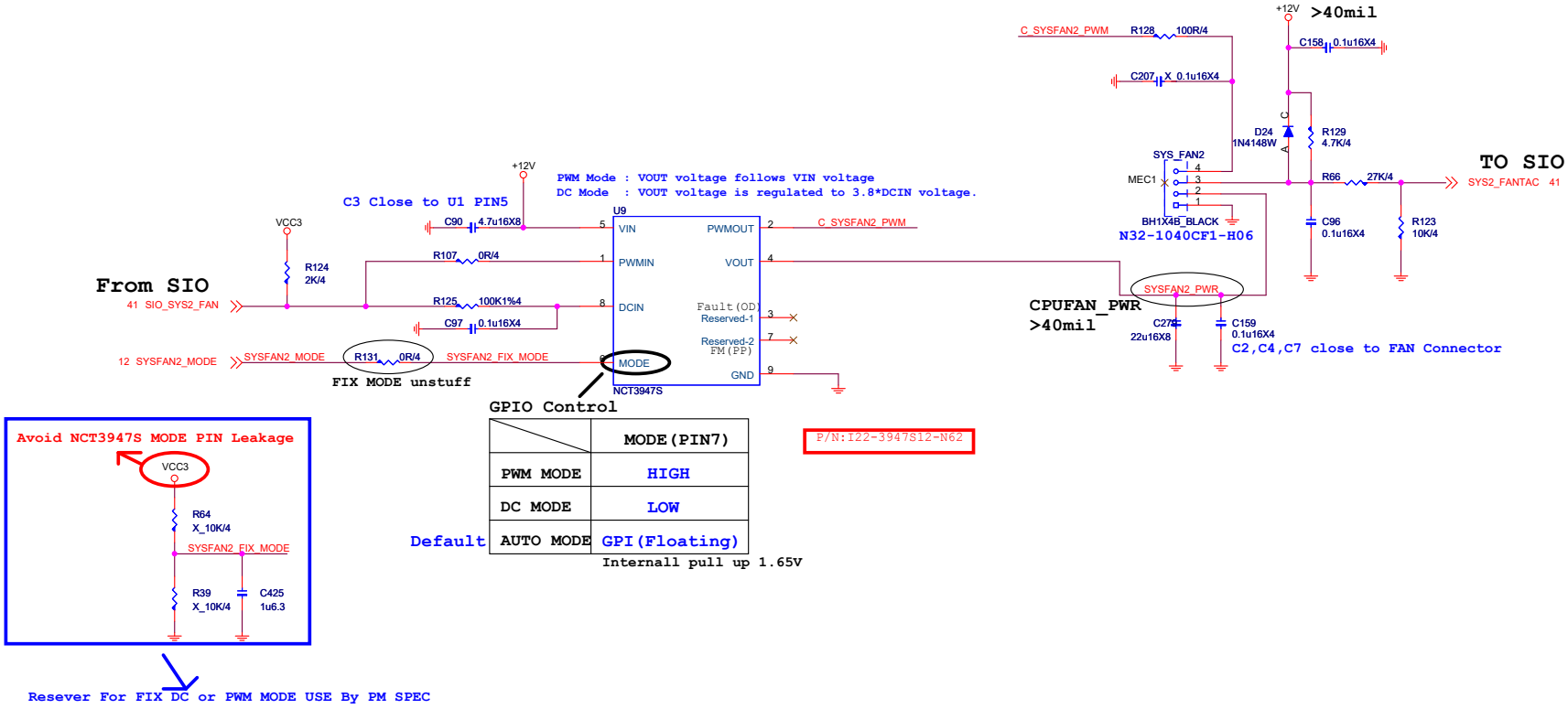
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

MICRO-STAR INT'L CO.,LTD		
MS-7A78..		
Size: Custom	Document Description: SYSTEM FAN1	Rev: 10
Date: Monday, September 26, 2016	Sheet 46 of 72	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE



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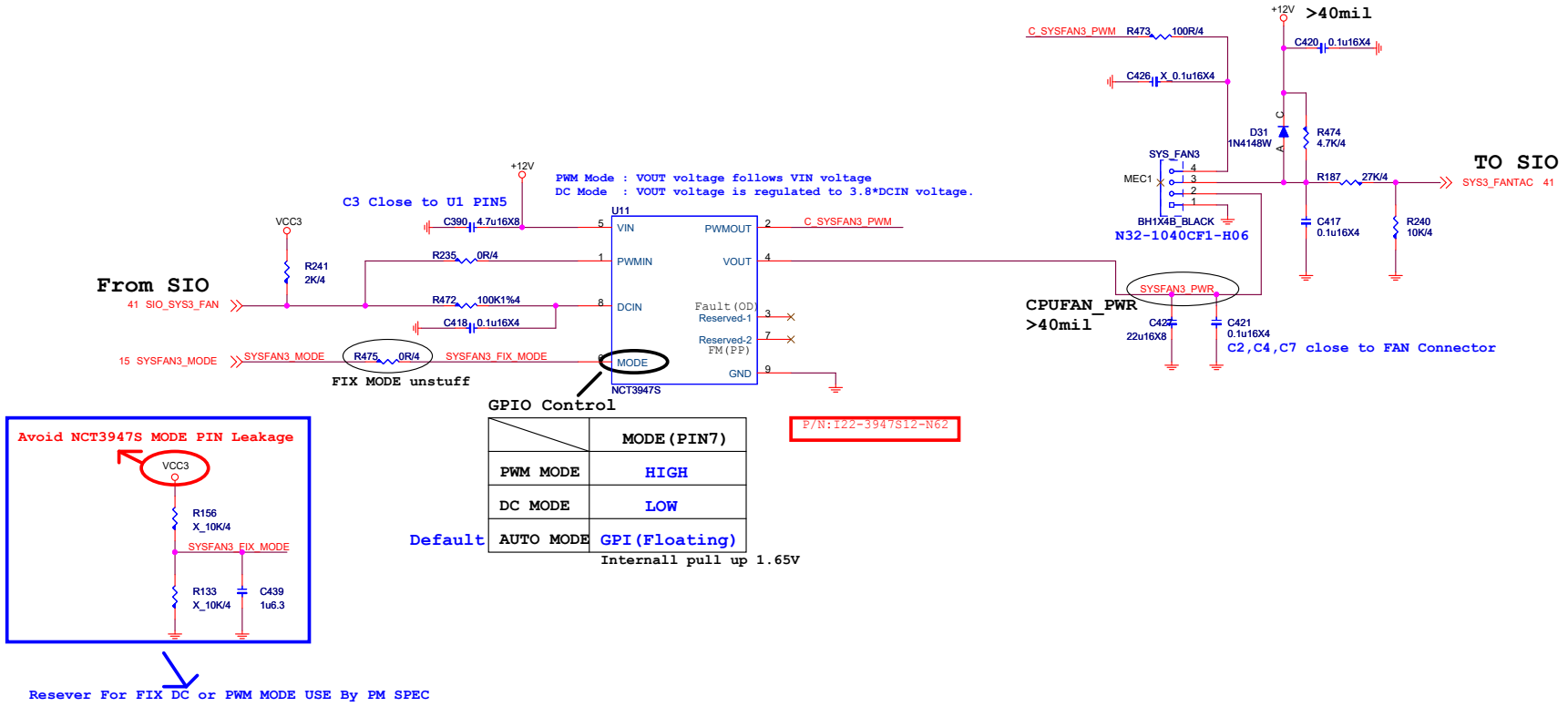
MS-7A78..	
Size: Custom	Document Description: SYSTEM FAN2
Rev: 10	
Date: Monday, September 26, 2016	Sheet 47 of 72

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　パBIOSち传 PWM/DC MODE



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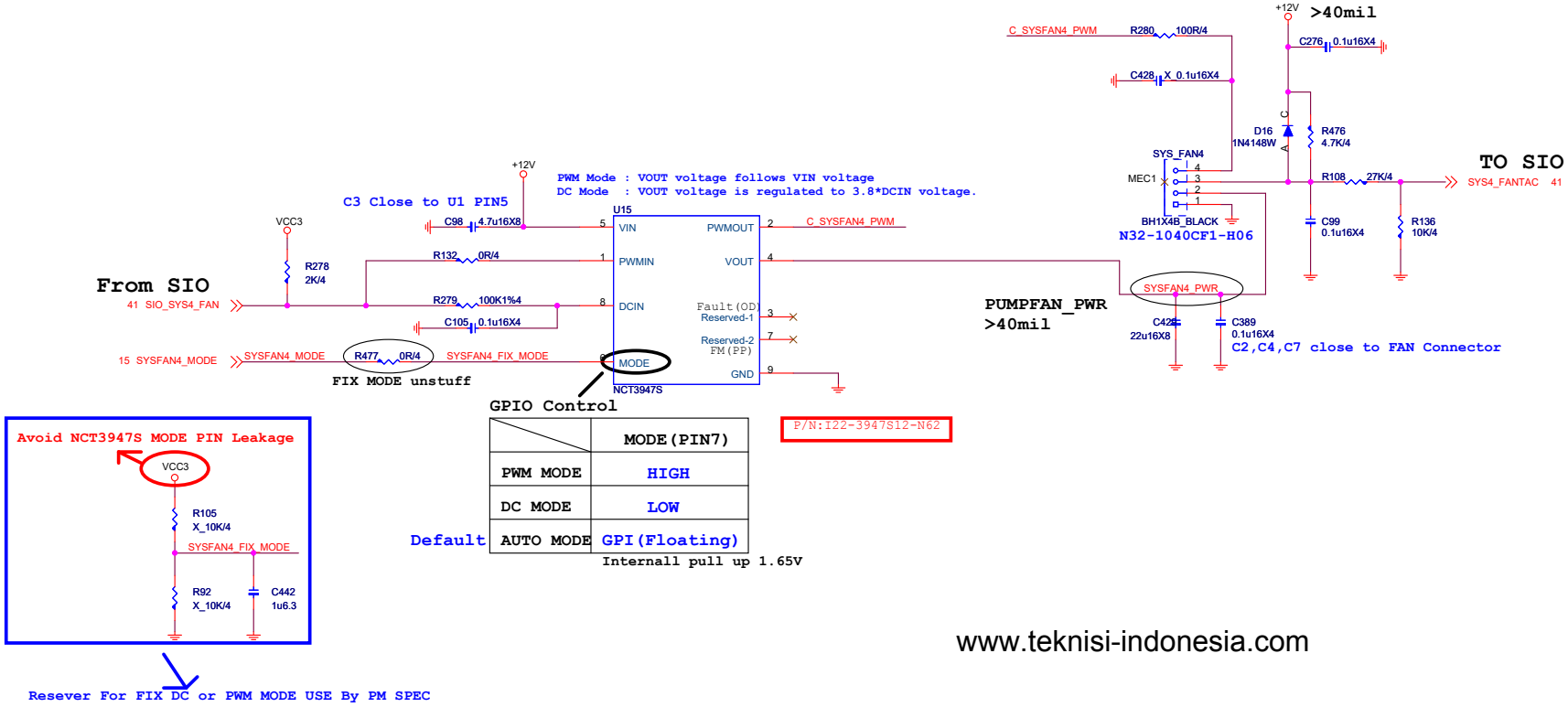
MS-7A78..	
Size: Custom	Document Description: SYSTEM FAN3
Rev: 10	
Date: Monday, September 26, 2016	Sheet 48 of 72

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　　パBIOSち传 PWM/DC MODE



	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

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Size: Custom | Document Description: SYSTEM FAN4 | Rev: 10

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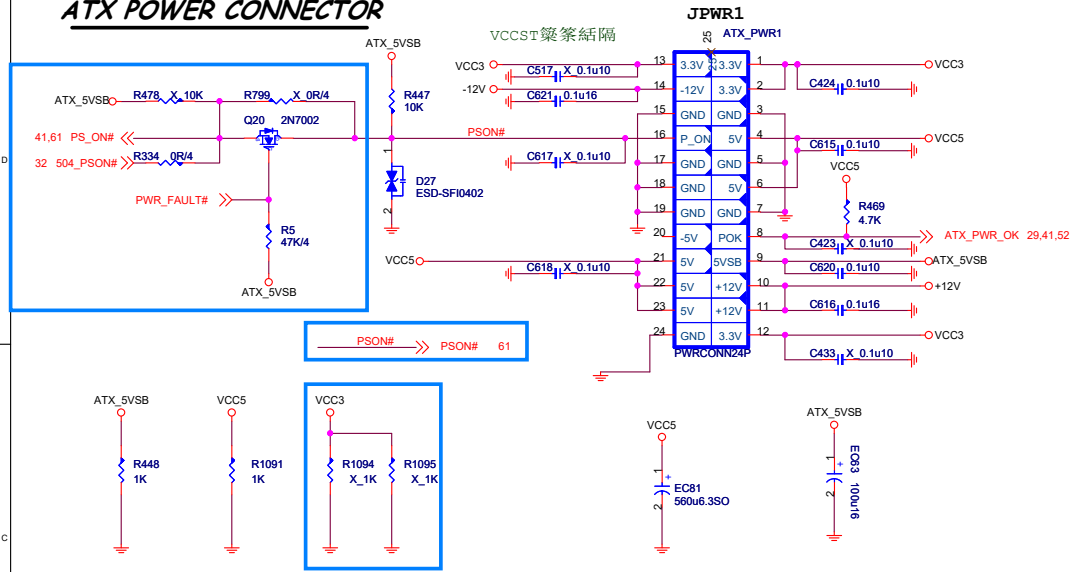
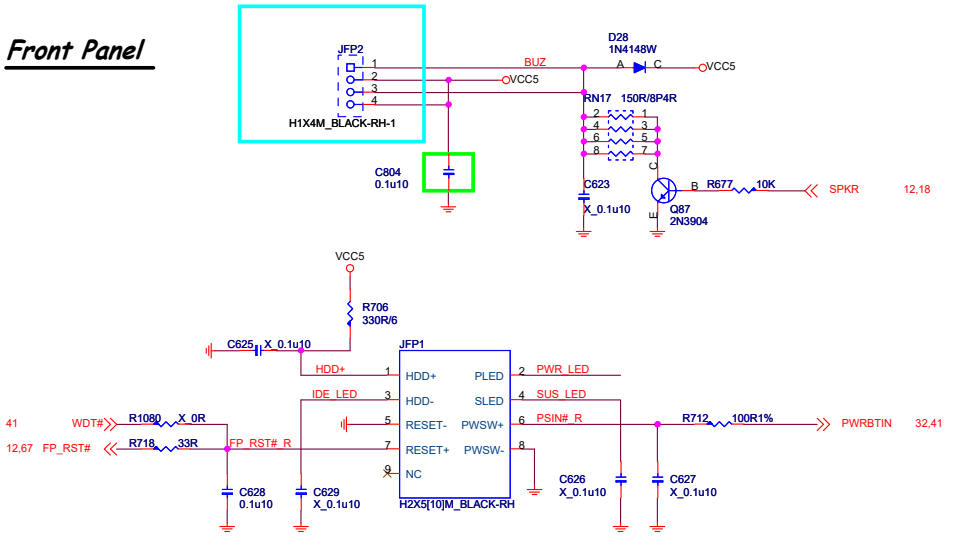
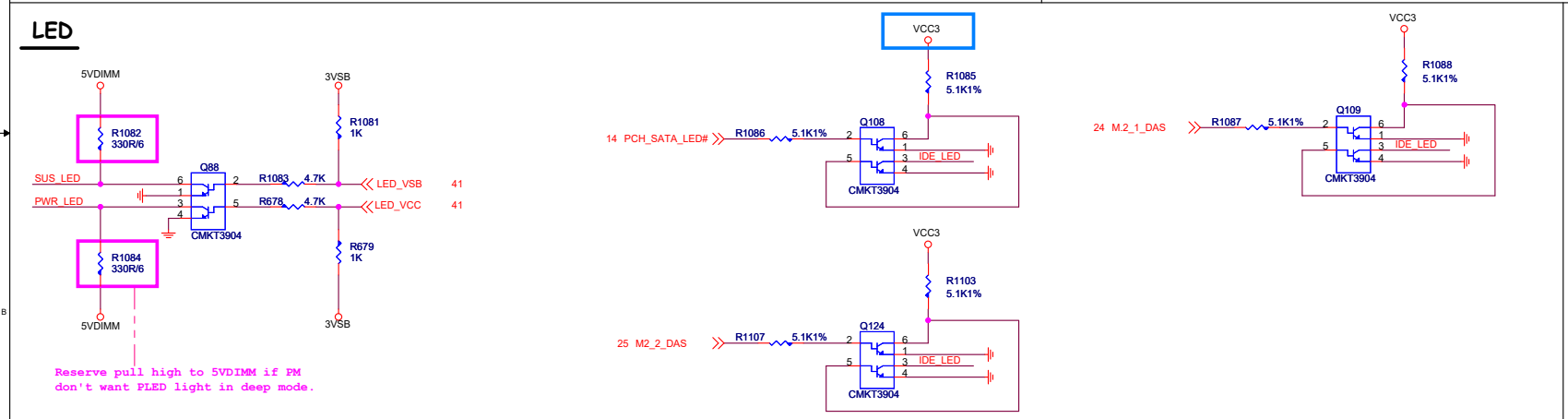
ATX POWER CONNECTOR



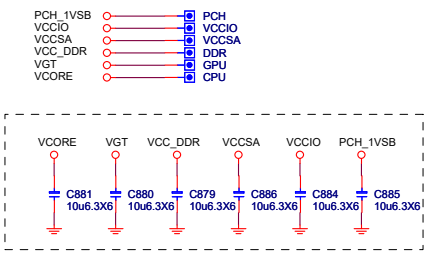
Front Panel



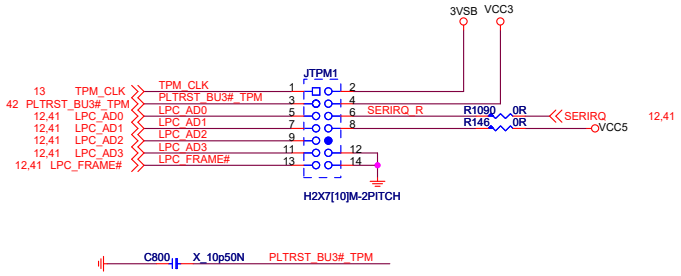
LED

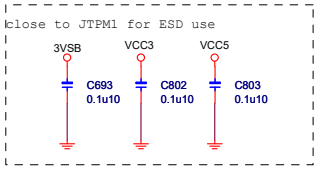


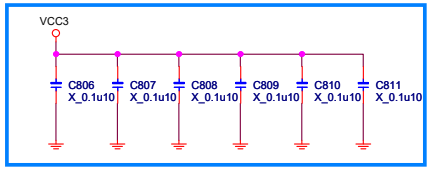
Voltage test point

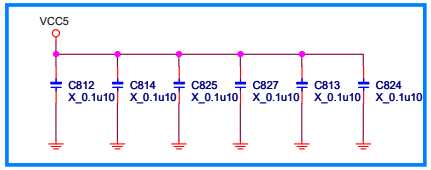


TPM









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Custom	ATX Power/F_Panel	10

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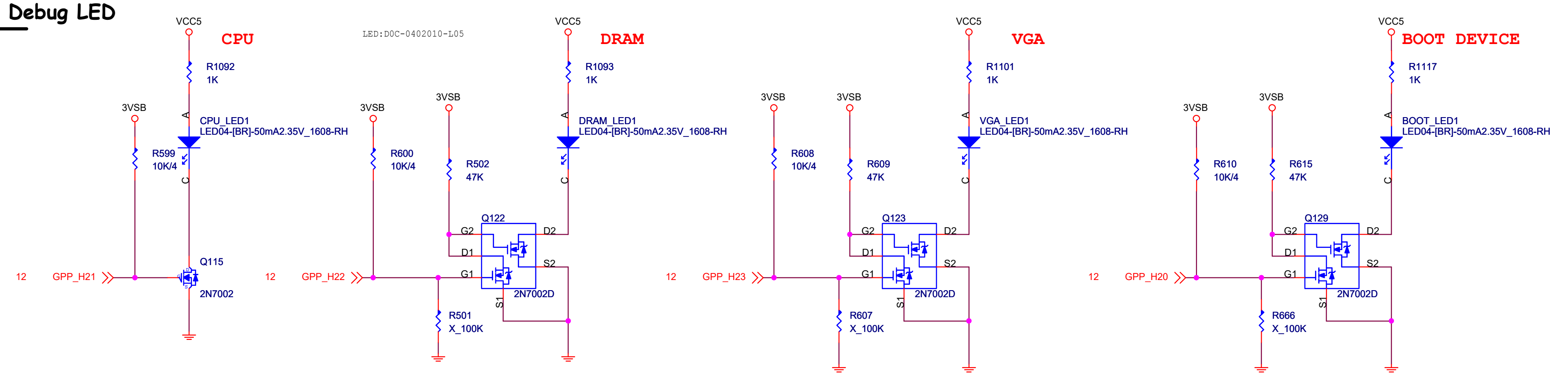
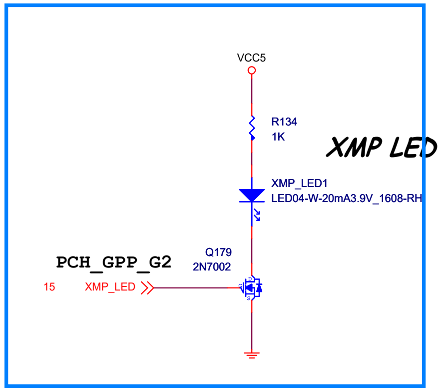
EZ Debug LED



LED
翱 : DOC-040S500-E07
フ : DOC-040S200-E07

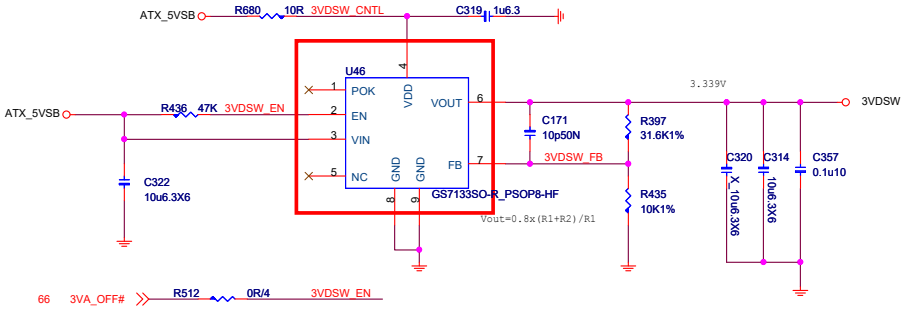
闰诀耞案 釪 4滗LED 蝴烃default 稭 柞诀硑案诀
1.楗 秈︽CPU checkCPU LED 獹 check PASS诀玥CPU LED防奔
2.钡帝ゎ 秈︽Memory /memory LED獹check PASS诀玥memory LED防奔
3.VGA check/VGA LED獹 check PASS诀玥VGA LED防奔
4. 程诀タ眭抖 柞诀诀 滗LED縊常琌防奔
╰参骈币┫ 亢 锊 硏⊙ ╰参骈柞诀 玥LEDご邪 瑂︽戕笆

GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
獹	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



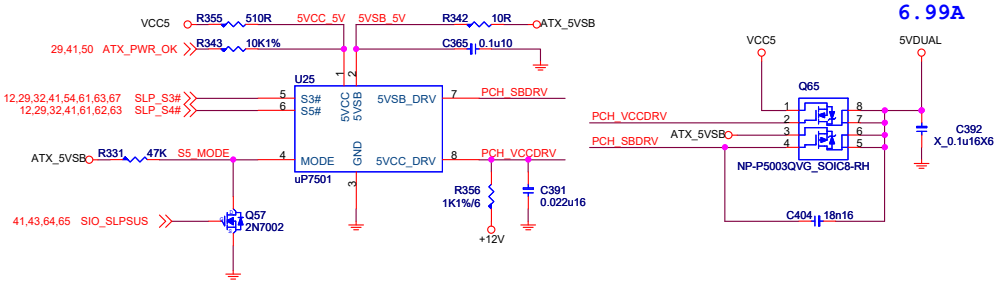
LED
翱 : DOC-040S500-E07
フ : DOC-040S200-E07

3VDSW

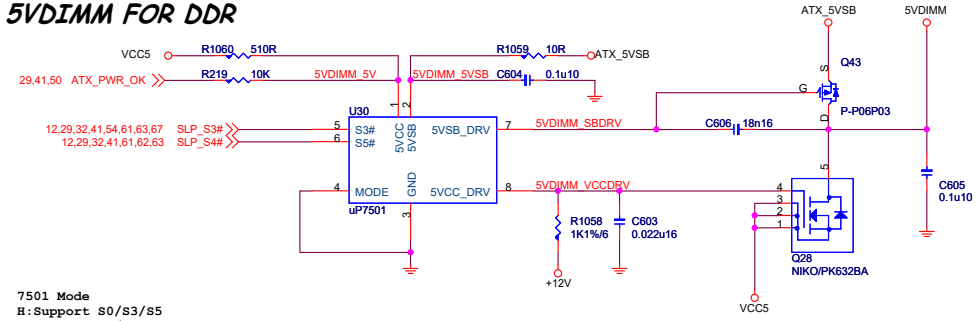


5VDUAL

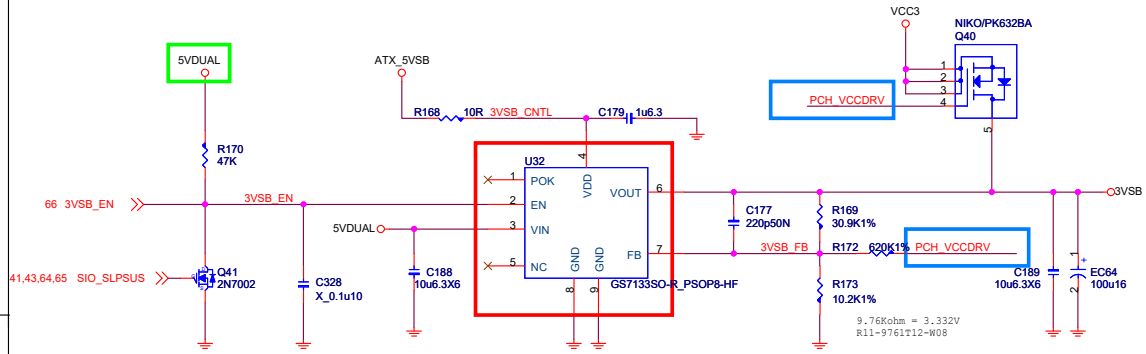
5VDUAL is power source of 1P0SB



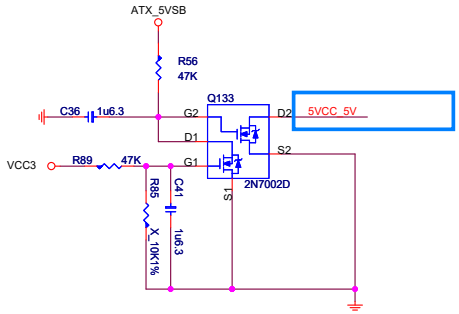
5VDIMM FOR DDR



3VSB cost down



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.



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MS-7A78..		
Size: Custom	Document Description: ACPI UPI	Rev: 10
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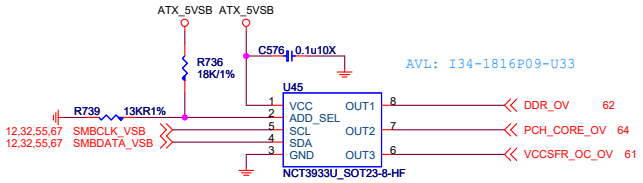
UPI VOLTAGE CONSOLE

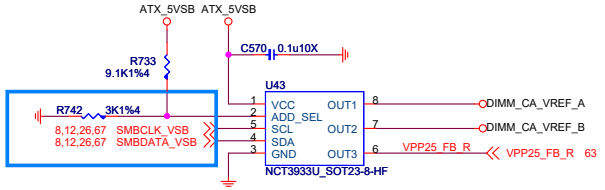
0x26:RH=18K,RL=13K



VCC_DDR
PCH_1VSB
VCCSFR_OC

UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K

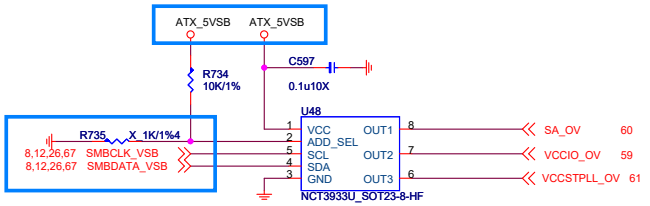


CHA_VREF
CHB_VREF
VPP25

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN



VCCSA
VCCIO

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Size: Custom | Document Description: OV-NCT3933/GPIO-NCT5605 | Rev: 10

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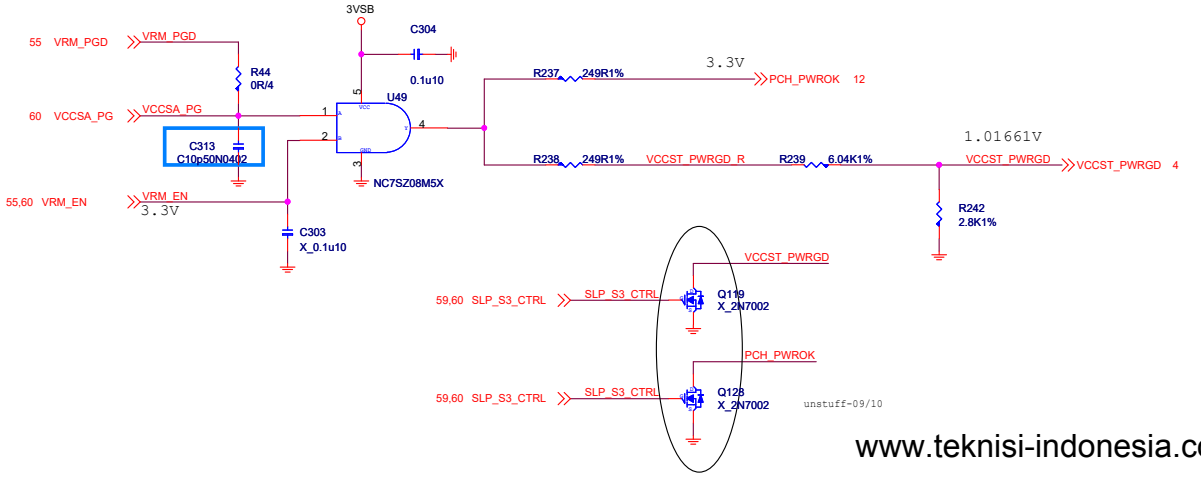
PCH_PWROK Control from VCCIO_PG&VCCSA

VCCST_PWRGD Control from VRM_PGD

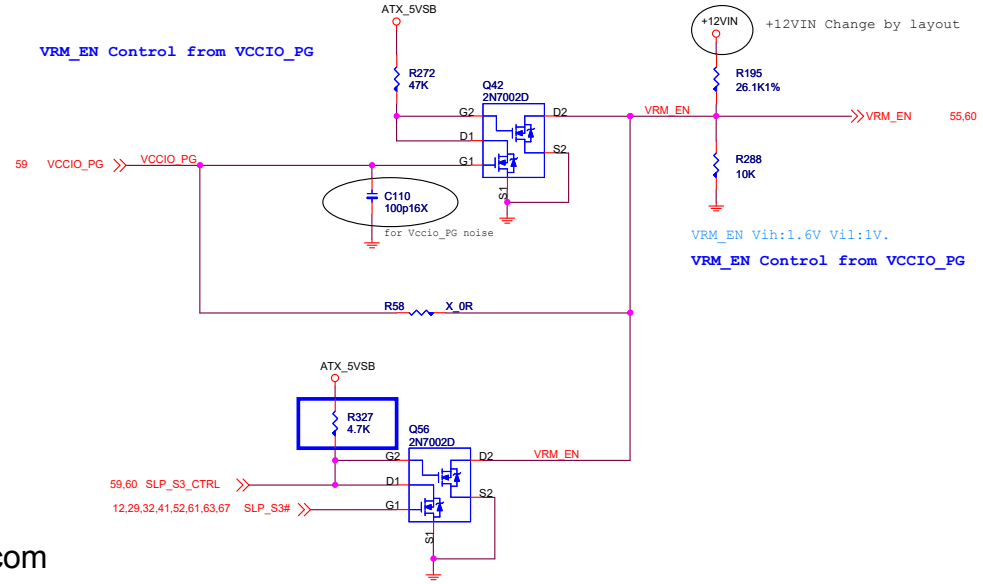
VCCSA&Vcore use same PWM IC, pull up VCC3

VCCSA&Vcore use different PWM IC,pull up VCCSA

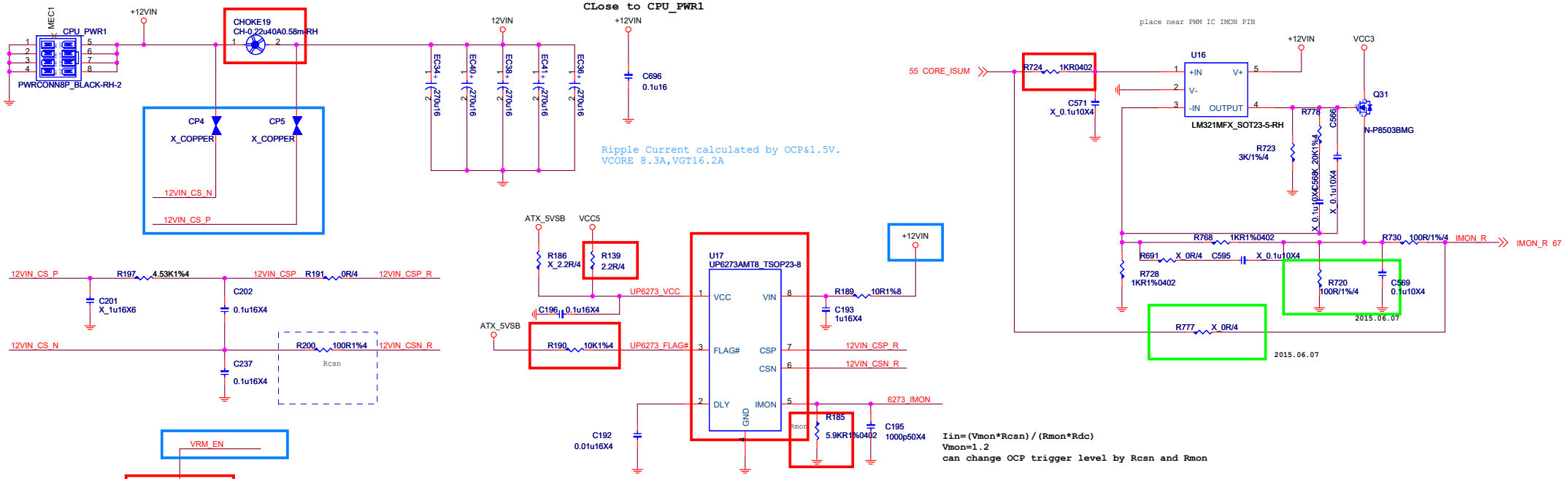
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



VRM_EN Control from VCCIO_PG



CLose to CPU_PWR1



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Size: Custom | Document Description: Rear I/O PS2 | Rev: 10

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Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A
VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A

VU1 change to I32-9508Q0C-U33.

Close IC

VR13=48.7K,for VGT ICCMAX=48A.
VR17=100K,for VCORE ICCMAX=100A.

PROG1: For 4+1 Setting
PROG2: Vboot 0V, SMBUS Adress 8Ah.
PROG3: For Phase Extension Enable.

SMBus address=8Ah
VR32=16.5K,R225=38.3K,Vboot:1.05V.
VR32=16.5K,R225 unstuff,Vboot 0V.

Diff pair

Diff pair

Close Phase1 CHOKE

Close Phase1 MOS

Close Phase1 CHOKE

Close Phase1 MOS

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Size: Custom | Document Description: PWM-UP9508 VCORE+VGT | Rev: 10

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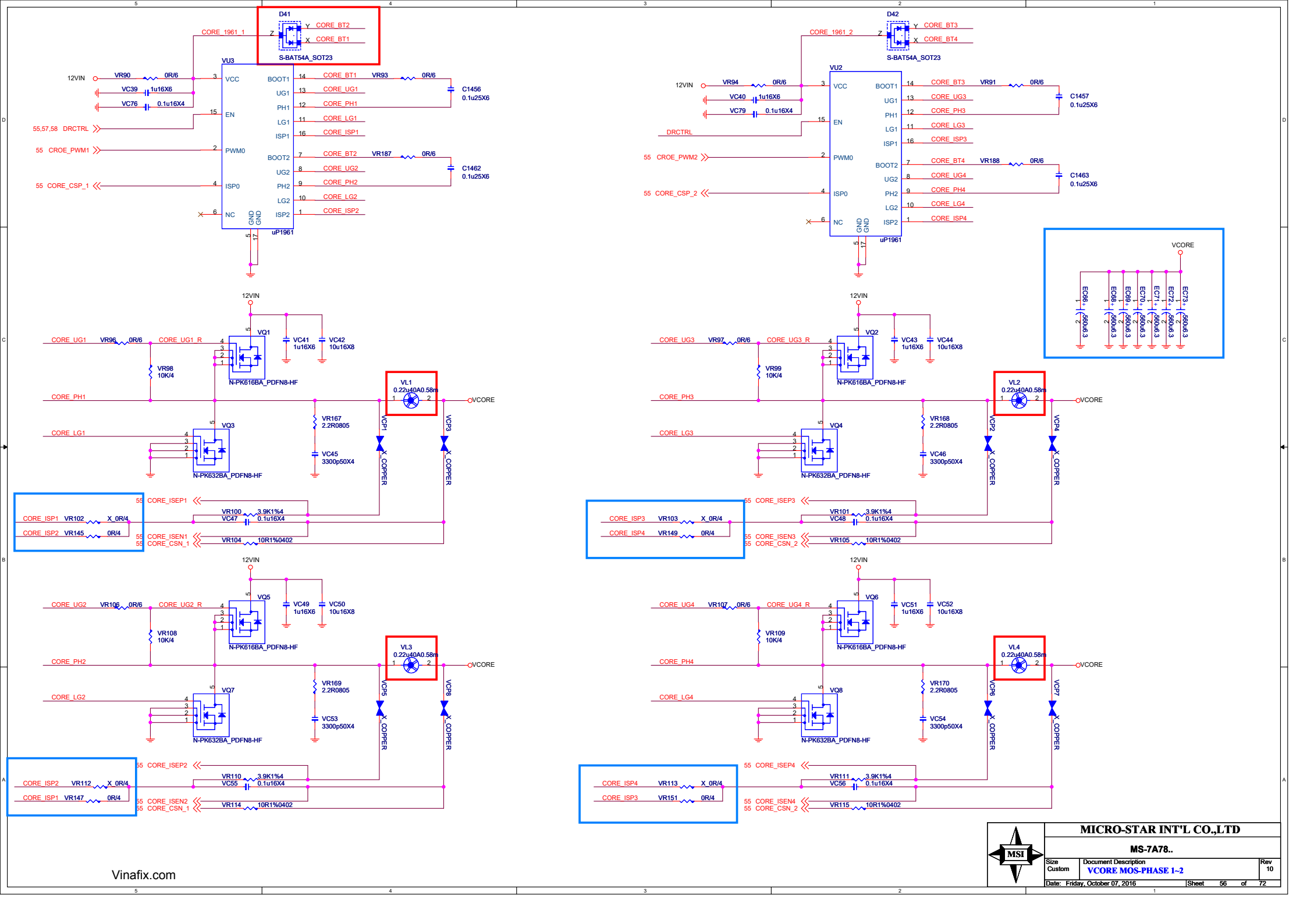
D41
S-BAT54A_SOT23
CORE_1961_1
CORE_BT2
CORE_BT1
VU3
uP1961
12VIN
VR90 0R/6
VC39 1u16X6
VC76 0.1u16X4
55,57,58 DRCTRL
55 CROE_PWM1
55 CORE_CSP_1
VCC
EN
PWM0
ISP0
NC
GND
BOOT1
UG1
PH1
LG1
ISP1
BOOT2
UG2
PH2
LG2
ISP2
CORE_BT1
CORE_UG1
CORE_PH1
CORE_LG1
CORE_ISP1
CORE_BT2
CORE_UG2
CORE_PH2
CORE_LG2
CORE_ISP2
VR93 0R/6
VR187 0R/6
C1456 0.1u25X6
C1462 0.1u25X6
D42
S-BAT54A_SOT23
CORE_1961_2
CORE_BT3
CORE_BT4
VU2
VR94 0R/6
VC40 1u16X6
VC79 0.1u16X4
DRCTRL
55 CROE_PWM2
55 CORE_CSP_2
CORE_BT3
CORE_UG3
CORE_PH3
CORE_LG3
CORE_ISP3
CORE_BT4
CORE_UG4
CORE_PH4
CORE_LG4
CORE_ISP4
VR91 0R/6
VR188 0R/6
C1457 0.1u25X6
C1463 0.1u25X6
VCORE
EC66+ 560u6.3
EC68+ 560u6.3
EC69+ 560u6.3
EC70+ 560u6.3
EC71+ 560u6.3
EC72+ 560u6.3
EC73+ 560u6.3
VQ1
VQ3
VQ5
VQ7
N-PK616BA_PDFN8-HF
N-PK632BA_PDFN8-HF
CORE_UG1
CORE_UG1_R
VR96 0R/6
VR98 10K/4
CORE_PH1
CORE_LG1
VC41 1u16X6
VC42 10u16X8
VL1 0.22u40A0.58m
VR167 2.2R0805
VC45 3300p50X4
VCP1 X_COPPER
VCP3 X_COPPER
CORE_ISP1 VR102 X_0R/4
CORE_ISP2 VR145 0R/4
55 CORE_ISEP1
55 CORE_ISEN1
55 CORE_CSN_1
VR100 3.9K1%4
VC47 0.1u16X4
VR104 10R1%0402
CORE_UG2
CORE_UG2_R
VR106 0R/6
VR108 10K/4
CORE_PH2
CORE_LG2
VC49 1u16X6
VC50 10u16X8
VL3 0.22u40A0.58m
VR169 2.2R0805
VC53 3300p50X4
VCP5 X_COPPER
VCP8 X_COPPER
CORE_ISP2 VR112 X_0R/4
CORE_ISP1 VR147 0R/4
55 CORE_ISEP2
55 CORE_ISEN2
55 CORE_CSN_1
VR110 3.9K1%4
VC55 0.1u16X4
VR114 10R1%0402
VQ2
VQ4
VQ6
VQ8
CORE_UG3
CORE_UG3_R
VR97 0R/6
VR99 10K/4
CORE_PH3
CORE_LG3
VC43 1u16X6
VC44 10u16X8
VL2 0.22u40A0.58m
VR168 2.2R0805
VC46 3300p50X4
VCP2 X_COPPER
VCP4 X_COPPER
CORE_ISP3 VR103 X_0R/4
CORE_ISP4 VR149 0R/4
55 CORE_ISEP3
55 CORE_ISEN3
55 CORE_CSN_2
VR101 3.9K1%4
VC48 0.1u16X4
VR105 10R1%0402
CORE_UG4
CORE_UG4_R
VR107 0R/6
VR109 10K/4
CORE_PH4
CORE_LG4
VC51 1u16X6
VC52 10u16X8
VL4 0.22u40A0.58m
VR170 2.2R0805
VC54 3300p50X4
VCP6 X_COPPER
VCP7 X_COPPER
CORE_ISP4 VR113 X_0R/4
CORE_ISP3 VR151 0R/4
55 CORE_ISEP4
55 CORE_ISEN4
55 CORE_CSN_2
VR111 3.9K1%4
VC56 0.1u16X4
VR115 10R1%0402
MICRO-STAR INT'L CO.,LTD
MS-7A78..
Size Custom
Document Description
VCORE MOS-PHASE 1~2
Rev 10
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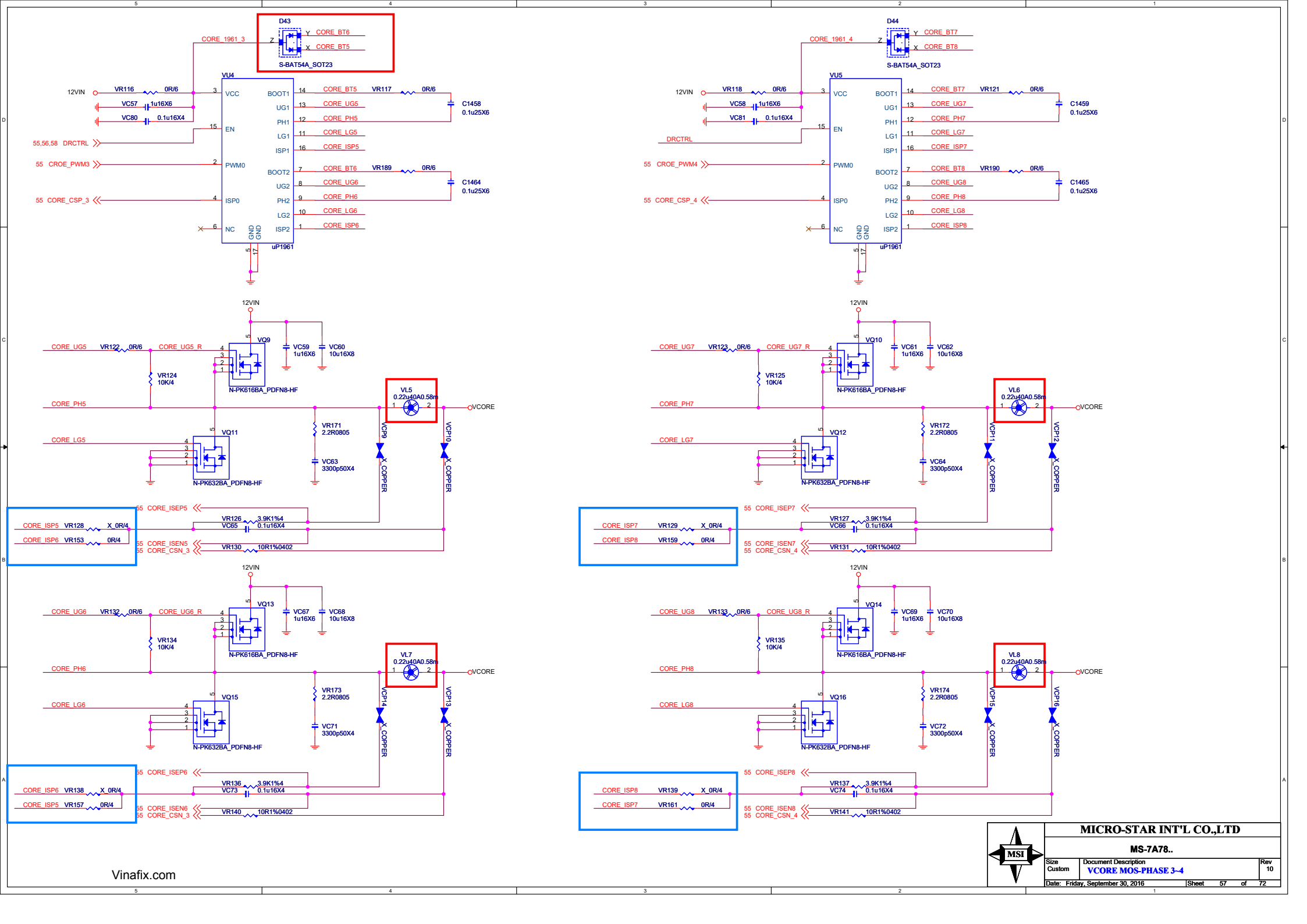
D43
S-BAT54A_SOT23
CORE_1961_3
CORE_BT6
CORE_BT5
VU4
uP1961
12VIN
VR116 0R/6
VC57 1u16X6
VC80 0.1u16X4
55,56,58 DRCTRL
55 CROE_PWM3
55 CORE_CSP_3
VR117 0R/6
VR189 0R/6
C1458 0.1u25X6
C1464 0.1u25X6
CORE_UG5
CORE_PH5
CORE_LG5
CORE_ISP5
CORE_ISP6
VR122 0R/6
VR124 10K/4
VR128 X_0R/4
VR153 0R/4
VQ9
VQ11
N-PK616BA_PDFN8-HF
N-PK632BA_PDFN8-HF
VC59 1u16X6
VC60 10u16X8
VR171 2.2R0805
VC63 3300p50X4
VL5 0.22u40A0.58m
VCORE
VCP9 X_COPPER
VCP10 X_COPPER
55 CORE_ISEP5
55 CORE_ISEN5
55 CORE_CSN_3
VR126 3.9K1%4
VC65 0.1u16X4
VR130 10R1%0402
CORE_UG6
CORE_PH6
CORE_LG6
CORE_ISP6
CORE_ISP5
VR132 0R/6
VR134 10K/4
VR138 X_0R/4
VR157 0R/4
VQ13
VQ15
VC67 1u16X6
VC68 10u16X8
VR173 2.2R0805
VC71 3300p50X4
VL7 0.22u40A0.58m
VCP13 X_COPPER
VCP14 X_COPPER
55 CORE_ISEP6
55 CORE_ISEN6
55 CORE_CSN_3
VR136 3.9K1%4
VC73 0.1u16X4
VR140 10R1%0402
D44
S-BAT54A_SOT23
CORE_1961_4
CORE_BT7
CORE_BT8
VU5
uP1961
VR118 0R/6
VC58 1u16X6
VC81 0.1u16X4
DRCTRL
55 CROE_PWM4
55 CORE_CSP_4
VR121 0R/6
VR190 0R/6
C1459 0.1u25X6
C1465 0.1u25X6
CORE_UG7
CORE_PH7
CORE_LG7
CORE_ISP7
CORE_ISP8
VR123 0R/6
VR125 10K/4
VR129 X_0R/4
VR159 0R/4
VQ10
VQ12
VC61 1u16X6
VC62 10u16X8
VR172 2.2R0805
VC64 3300p50X4
VL6 0.22u40A0.58m
VCP11 X_COPPER
VCP12 X_COPPER
55 CORE_ISEP7
55 CORE_ISEN7
55 CORE_CSN_4
VR127 3.9K1%4
VC66 0.1u16X4
VR131 10R1%0402
CORE_UG8
CORE_PH8
CORE_LG8
CORE_ISP8
CORE_ISP7
VR133 0R/6
VR135 10K/4
VR139 X_0R/4
VR161 0R/4
VQ14
VQ16
VC69 1u16X6
VC70 10u16X8
VR174 2.2R0805
VC72 3300p50X4
VL8 0.22u40A0.58m
VCP15 X_COPPER
VCP16 X_COPPER
55 CORE_ISEP8
55 CORE_ISEN8
55 CORE_CSN_4
VR137 3.9K1%4
VC74 0.1u16X4
VR141 10R1%0402
MICRO-STAR INT'L CO.,LTD
MS-7A78..
Size Custom
Document Description
VCORE MOS-PHASE 3-4
Rev 10
Date: Friday, September 30, 2016
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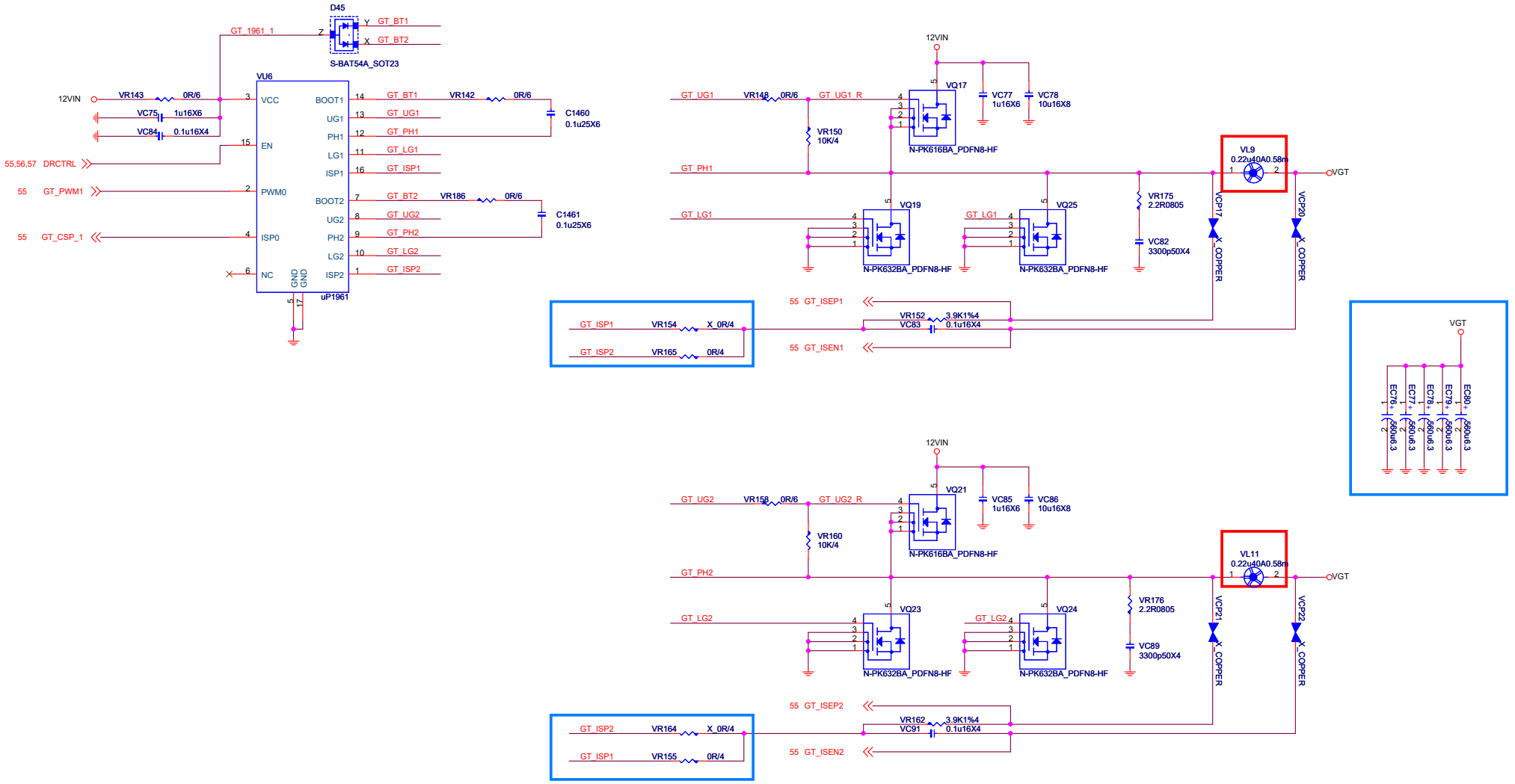

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MS-7A78..

Size	Document Description	Rev
Custom	VGT MOS-PHASE 1~2	10

Date: Friday, October 07, 2016 Sheet 58 of 72

VCCIO

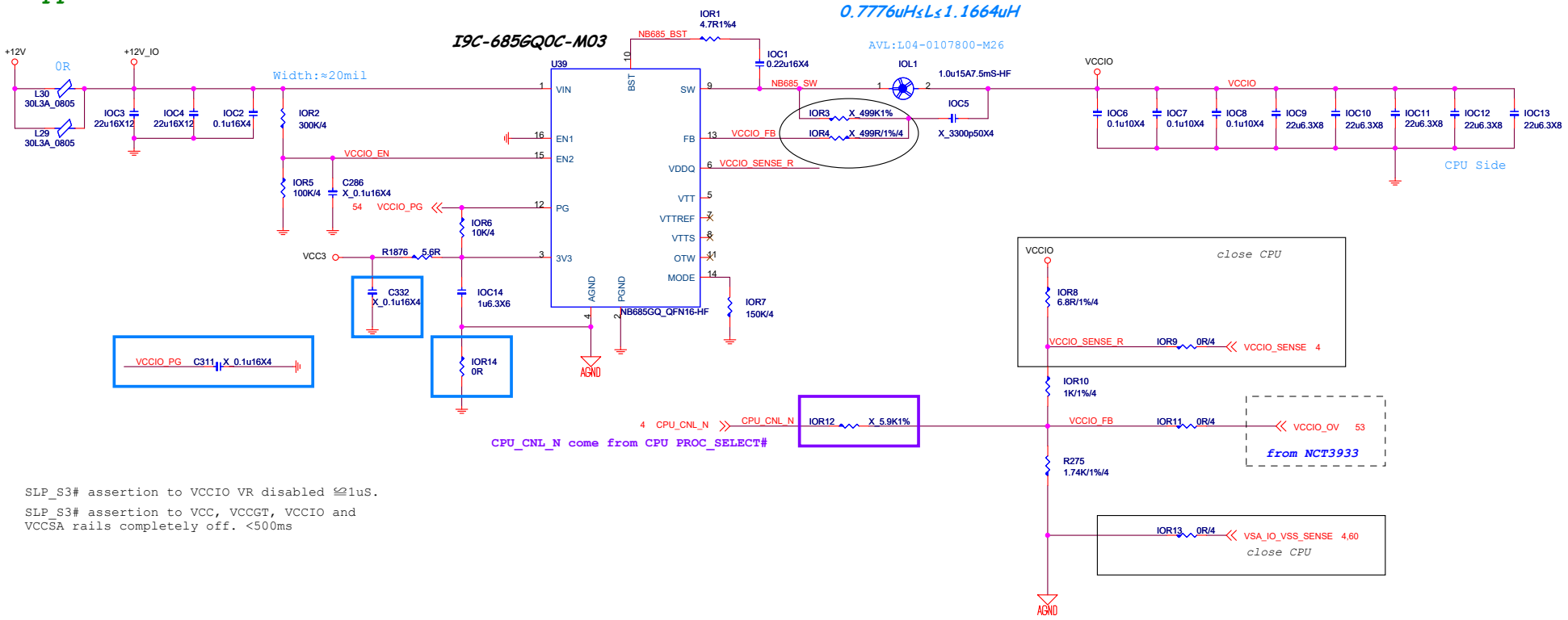
0.95V; 5.5A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685

I9C-685GQ0C-M03

0.7776uH≤L≤1.1664uH

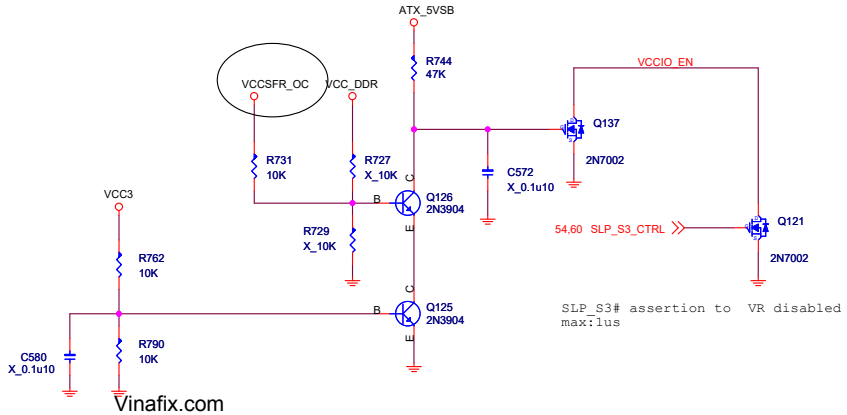


4 CPU_CNL_N >> CPU_CNL_N IOR12 X_5.9K1%

CPU_CNL_N come from CPU PROC_SELECT#

SLP_S3# assertion to VCCIO VR disabled ≦1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



SLP_S3# assertion to VR disabled max:1us

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MS-7A78..

Size	Document Description	Rev
Custom	CPU PWR_VCCIO	10

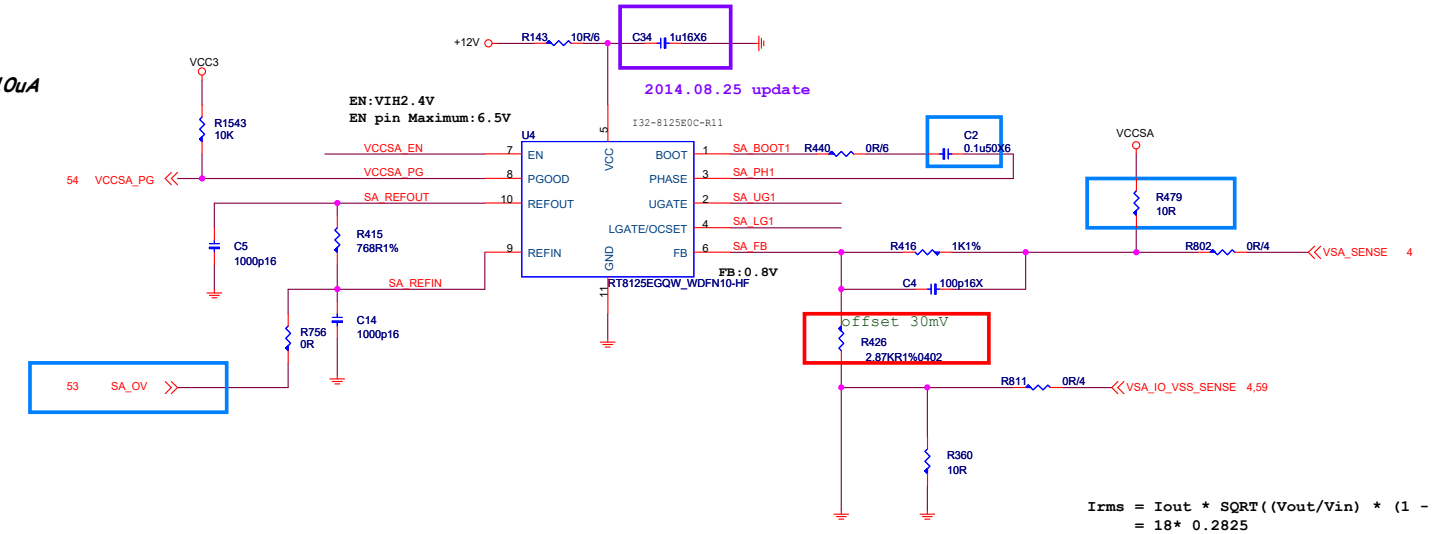
Date: Friday, October 07, 2016 Sheet 59 of 72

SA Power:1.05V,11.1A

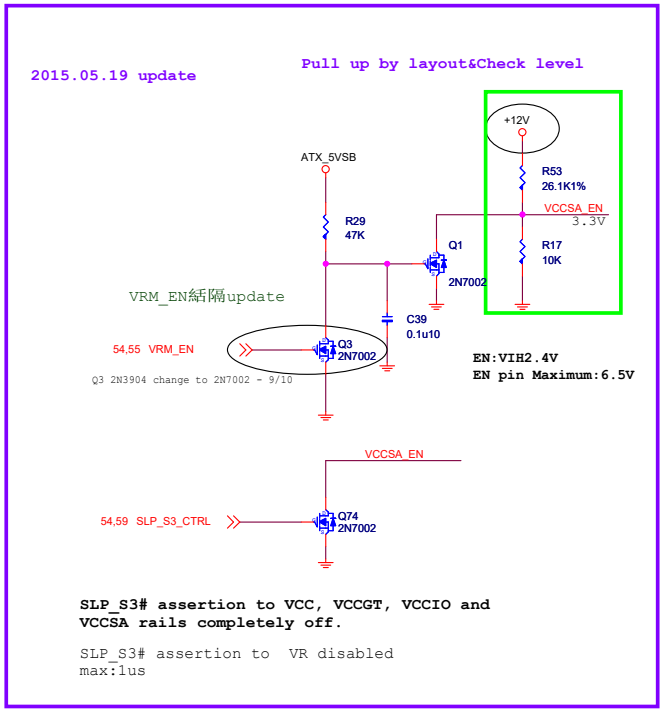
*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.3mohm]/10uA*
=15.54(3.3)mohm/10uA*
=5.1282Kohm

Rocs:5.23K,OCP:
D03-632BA0C-N03 : 15.848A

Rdson(low)10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

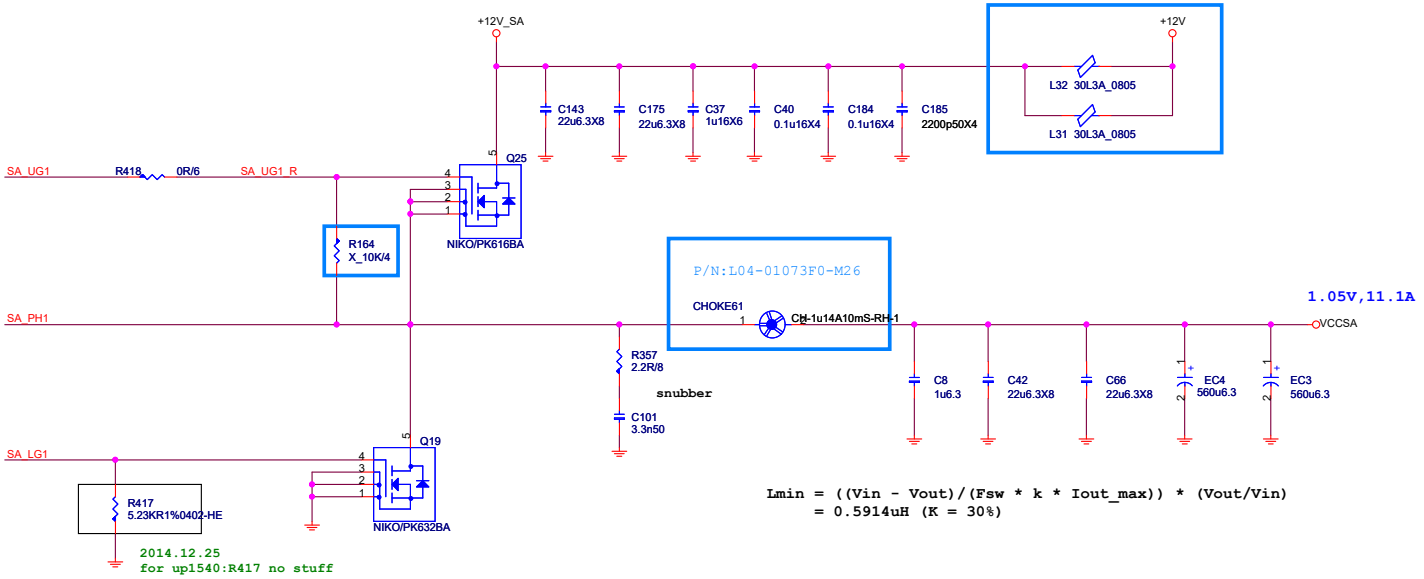


Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 18* 0.2825
= 5.086A

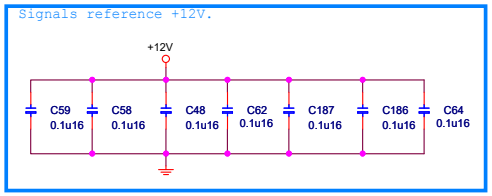


SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.5914uH (K = 30%)



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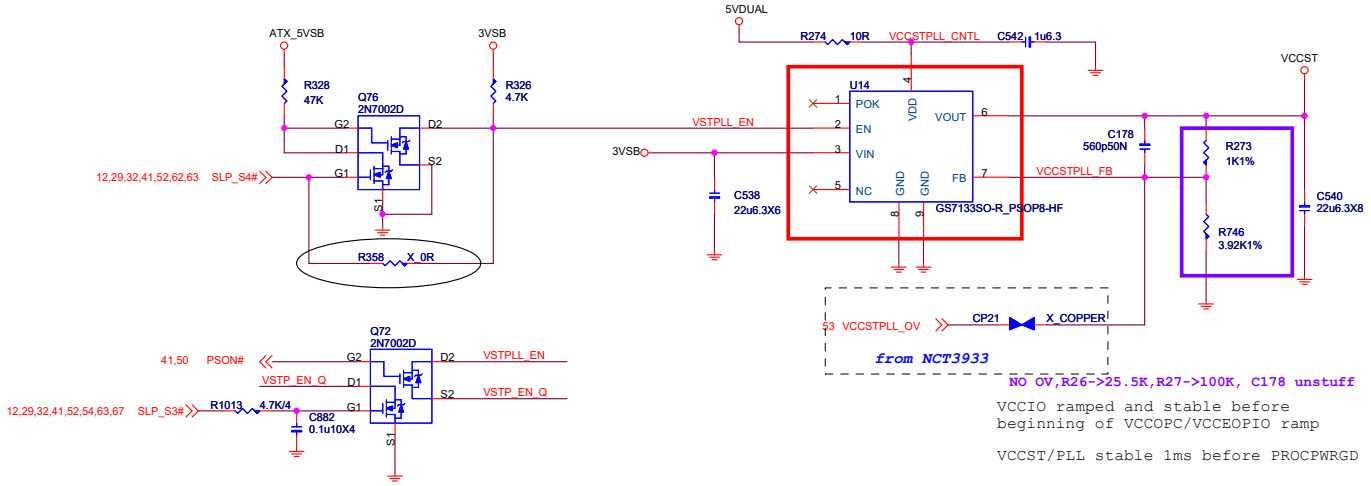
VCCST

for Gaming3/5, Classic, ECO and H110

1.0V; 250mA

For Cost down VCCST&VCCPLL merge



NO OV,R26->25.5K,R27->100K, C178 unstuff

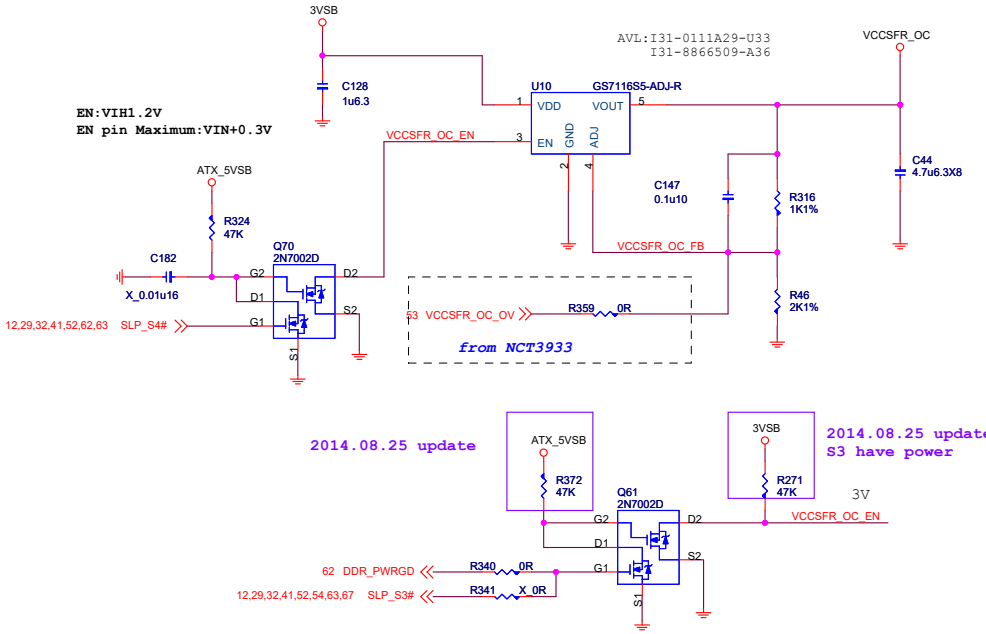
VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

VCCPLL_OC

1.2V; 110mA

2014.08.21 update



2014.08.25 update
S3 have power

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MS-7A78..		
Size: Custom	Document Description: CPU PWR_ST/PLL	Rev: 10
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DDR4_1.2V 2.8A+9.2A+1.2A=13.2A

2.8A FOR CPU

9.2A FOR 4DIMM

1.2A FOR DDR VTT

OCP =13.2A*1.5=19.8A

Rocs(R3)=OCP*[Rdson(Low side)/2]/10uA

=19.8A*(4.6/2)mohm/10uA

=4.554Kohm < 5K ohm

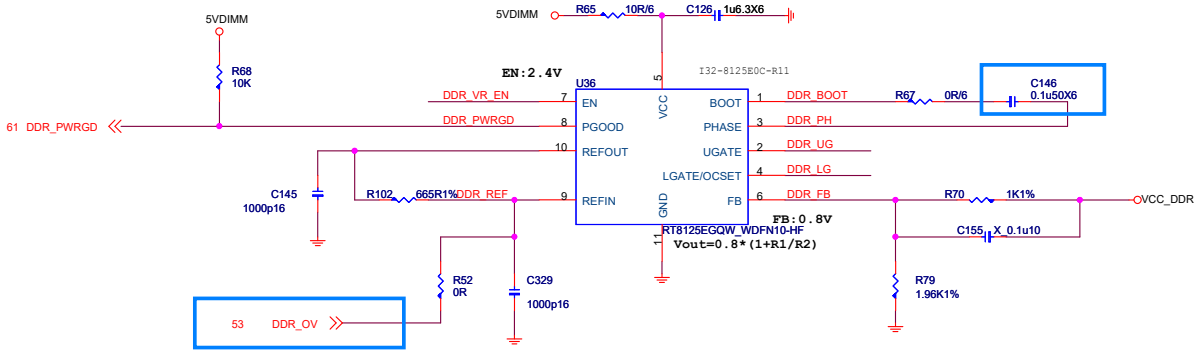
Rocpset:5.1K

OCP=Rocset/[Rdson(Low side)/2]*10uA

=5.1K/2.3mohm*10uA

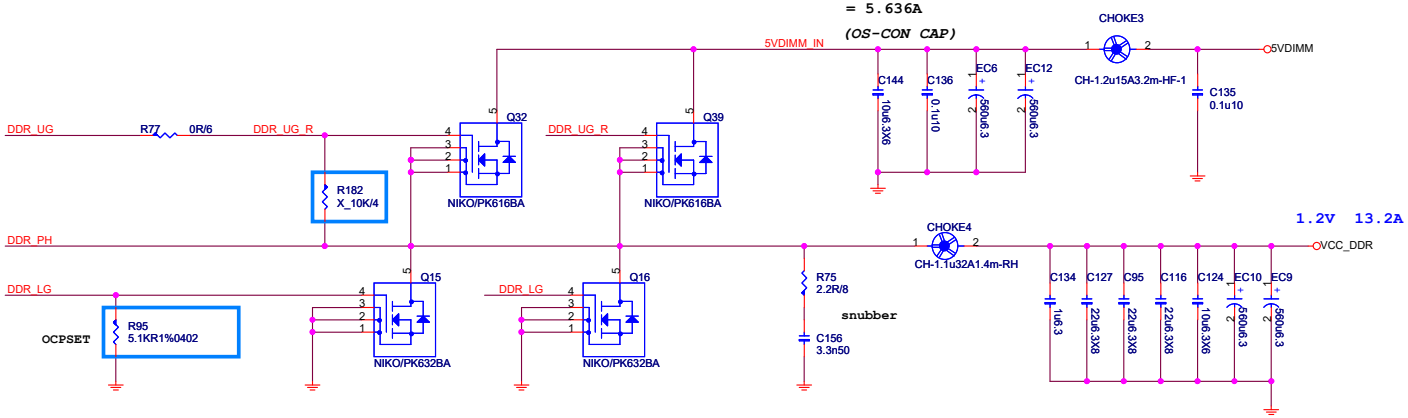
=22.1A

Rdson(low)4.5V	
D03-4C05N03-O05	: 5 mohm
D03-632BA0C-N03	: 4.6mohm
D03-3056M00-U47	: 6.2mohm



Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A

(OS-CON CAP)

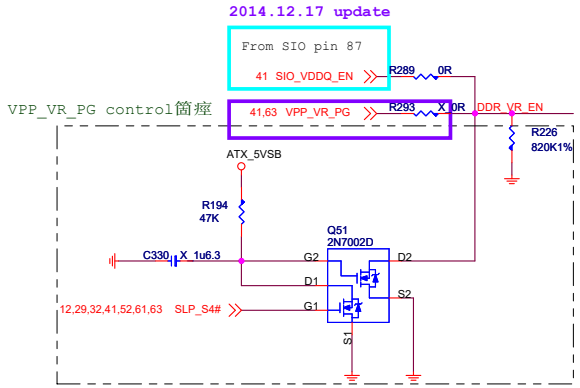


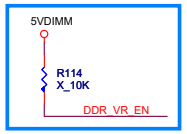
MOS PPK(1/1)→(2/2)

依Datasheet計算:Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

依CAP ESR計算:0.2432uH≤ L ≤1.2897uH

2014.12.17 update





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MS-7A78..		
Size: Custom	Document Description: DDR4 Power-RT8125C	Rev: 10
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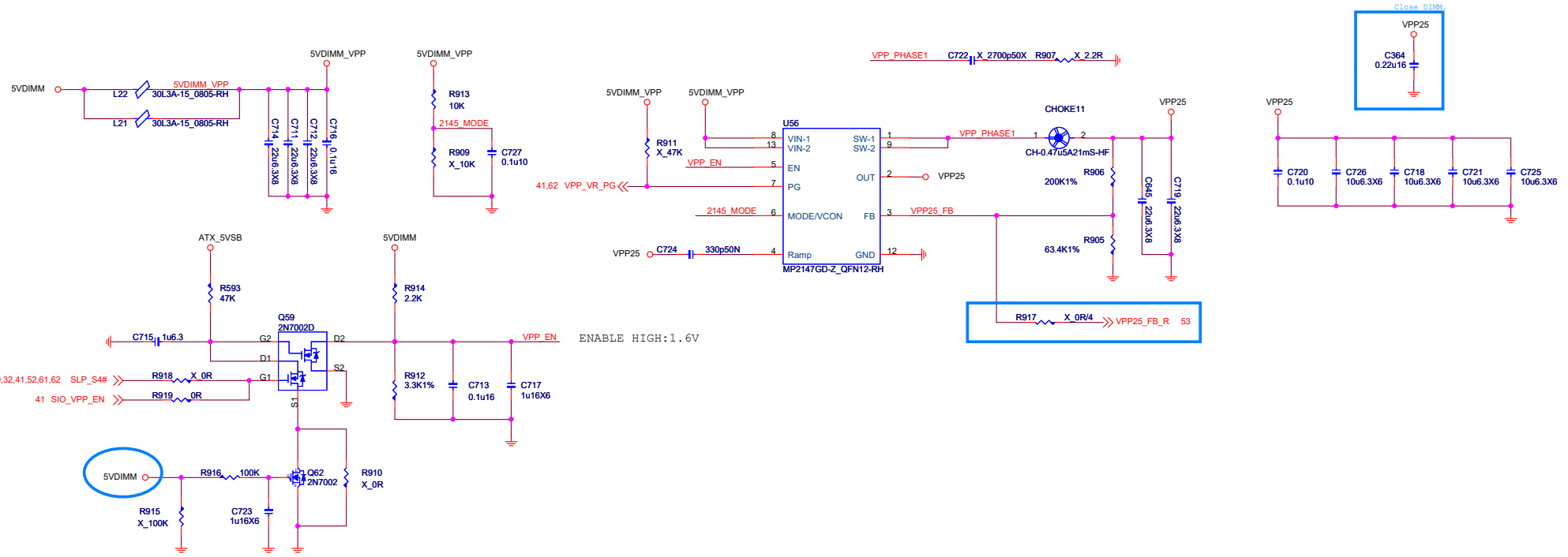
4DIMM :2.84A FOR DDR VPP2.5V

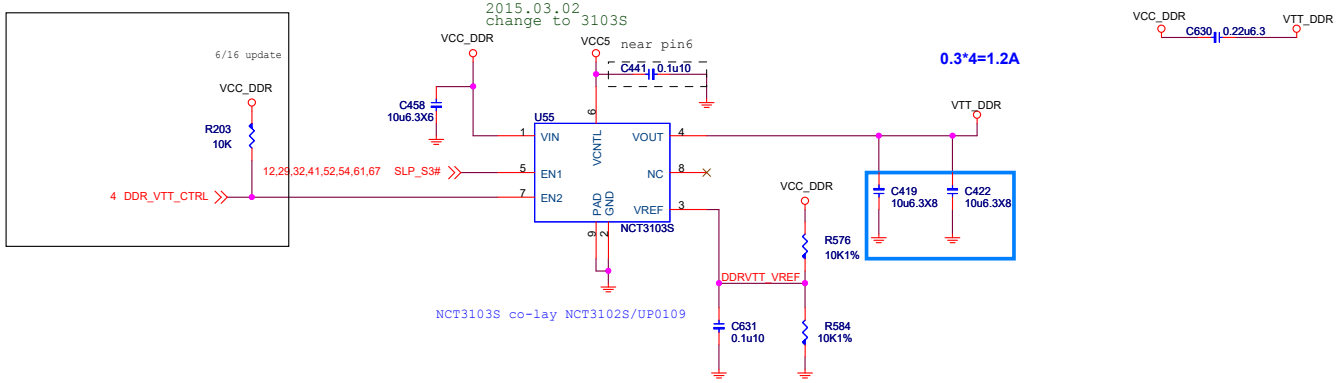
VPP25 Power

2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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MS-7A78..

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Custom	DDR4 Power-VPP25	10

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PCH 1VSB

1.0V; 10A(7.929A)

OCP = 15A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 15A * 4.6mohm / 10uA
= 6.9K

Rocs:6.81K,OCP:
D03-632BA0C-N03 : 14.8A

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

1504 change to 8125 I32-8125E0C-R11

2014.08.25:Change 1u/0603

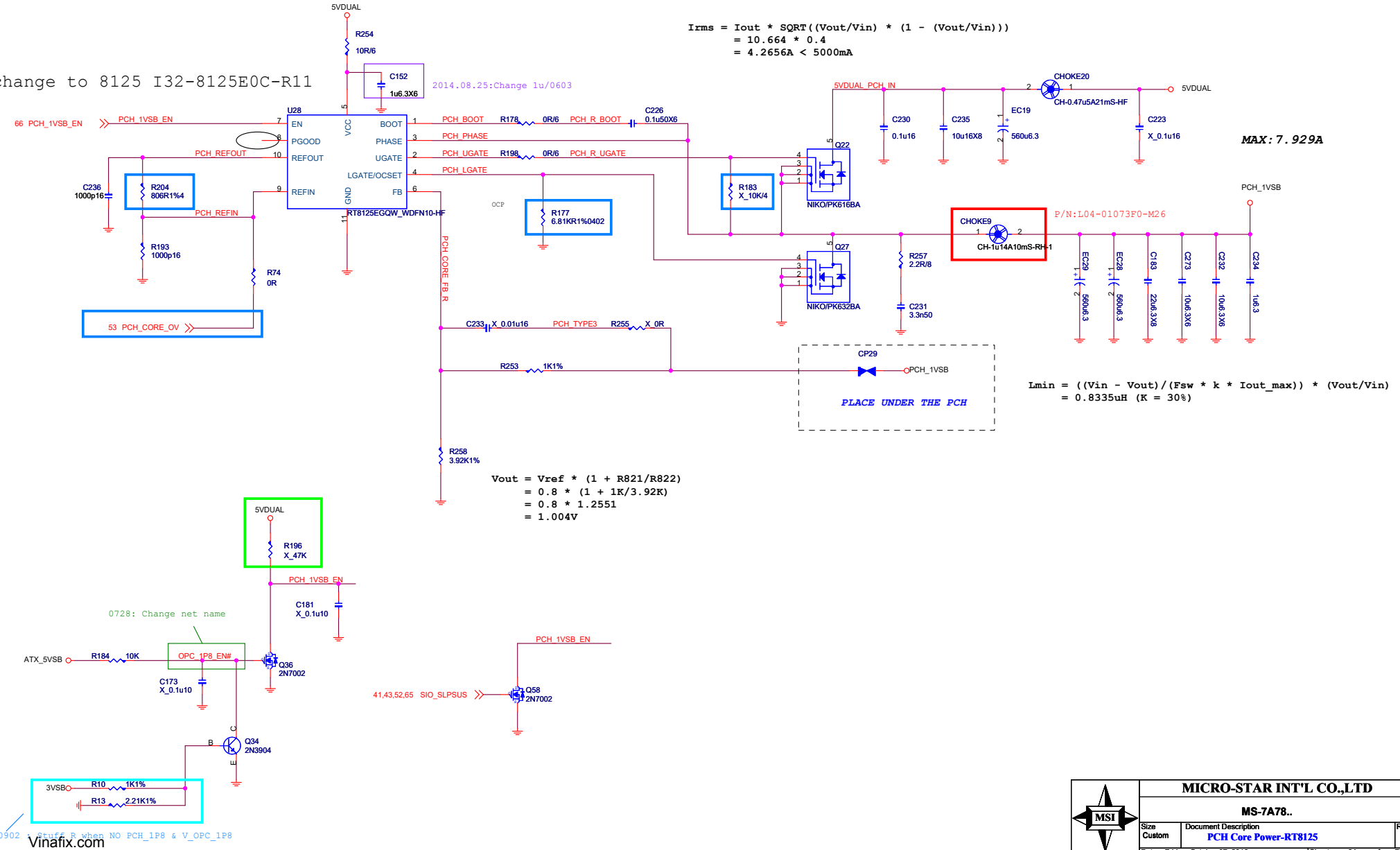
MAX:7.929A

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

0728: Change net name

0902 : Stuff R when NO PCH_1P8 & V_OPC_1P8



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MS-7A78..

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Custom	PCH Core Power-RT8125	10

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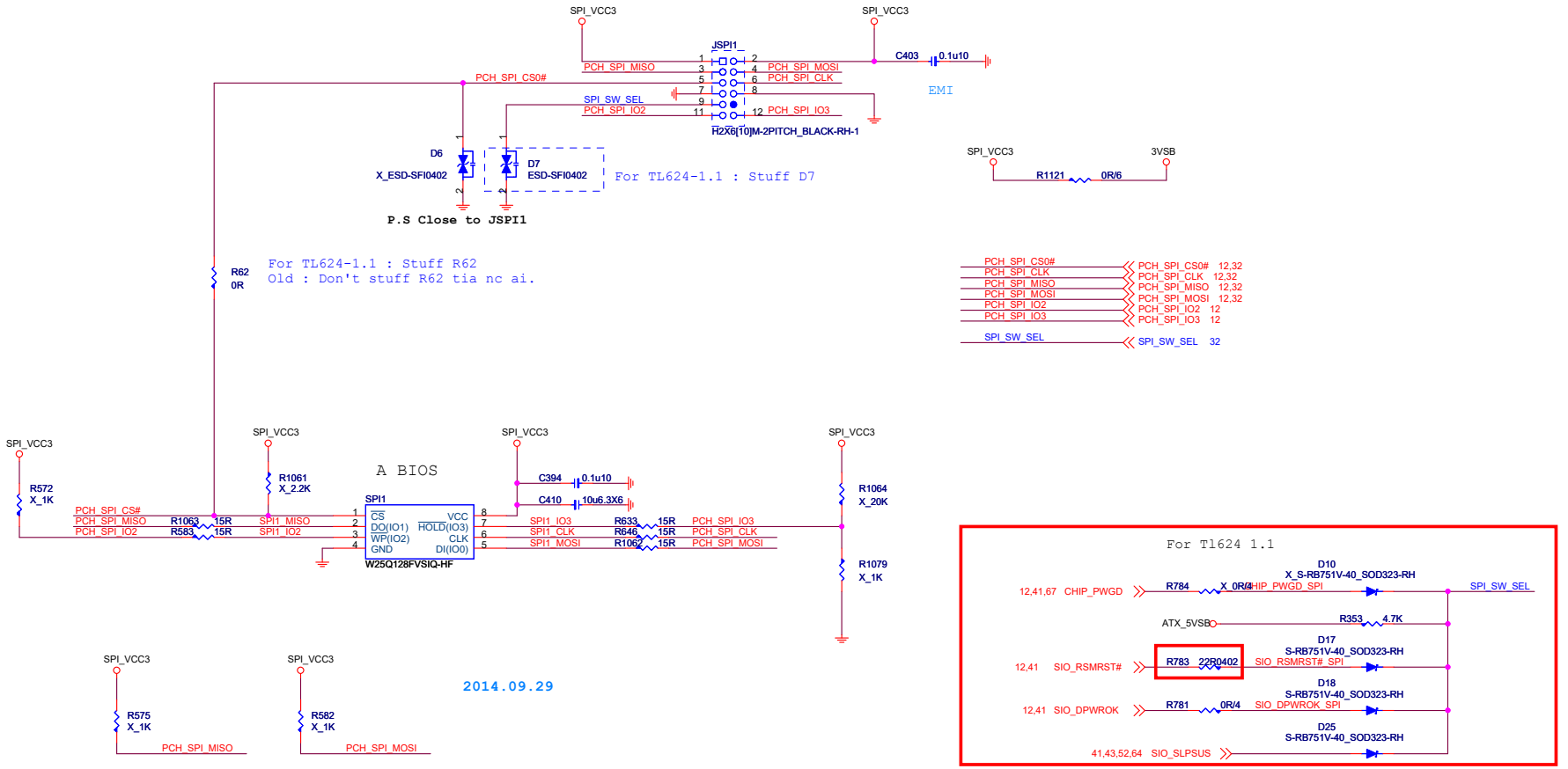
JSPI1 change to N31-2061451-H06.



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272

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MS-7A78..	
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Rev: 10	
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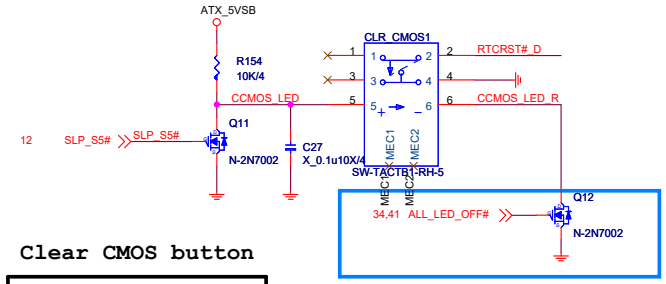
Clear CMOS HW MODE



Clear CMOS button

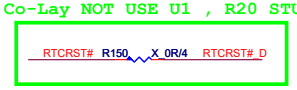
LED LIGHTING RULE
S0/S3/S4 : LED OFF
S5 : LED ON

By PM SPEC

Function 1			
IN		OUT	
INPUT1	INPUT2	OUTPUT1	
0	1	1	Default
1	0	0	
1	1	0	
0	0	0	

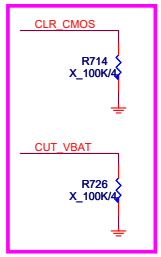
Function 2					
IN		OUT			
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT	
0	0	0	1	1	Default
1	0	1	1	0 (discharge)	
0	1	1	0	0 (discharge)	
1	1	1	0	0 (discharge)	

Co-Lay NOT USE U1 , R20 STUFF



If STUFF R20 Please Check RTCRST# Double Pull High

20160629



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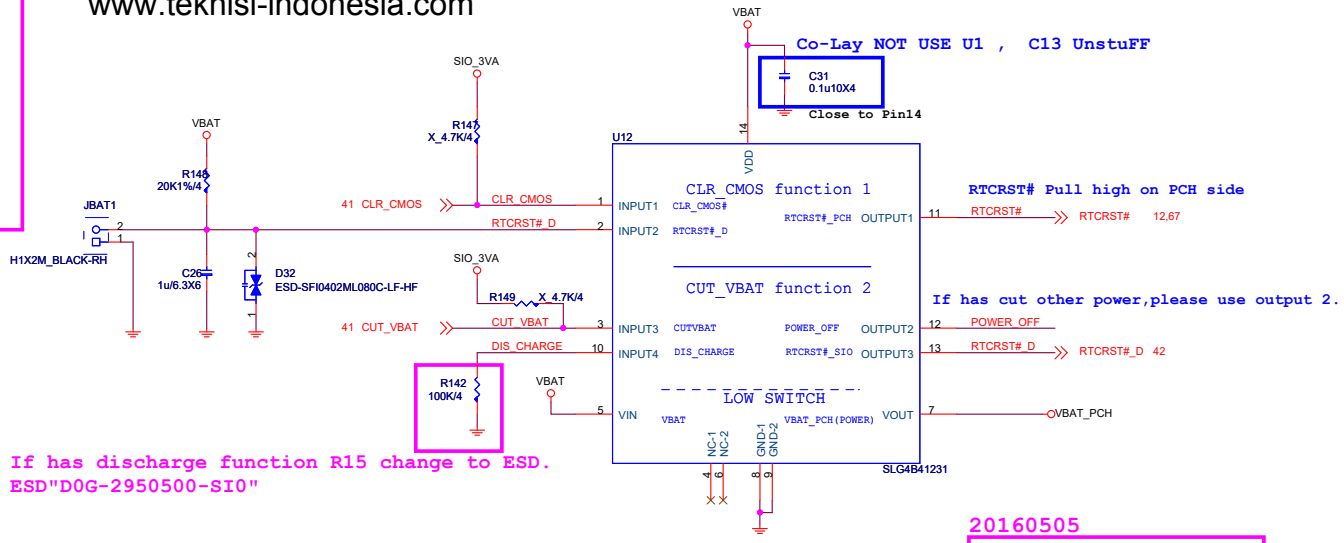
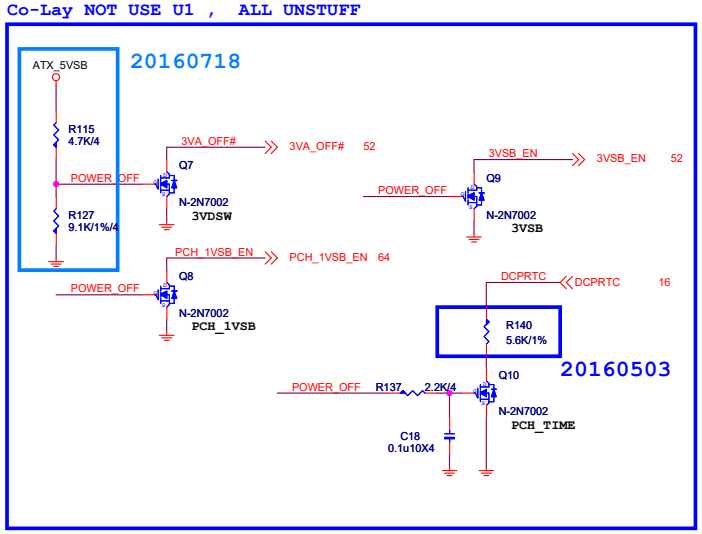
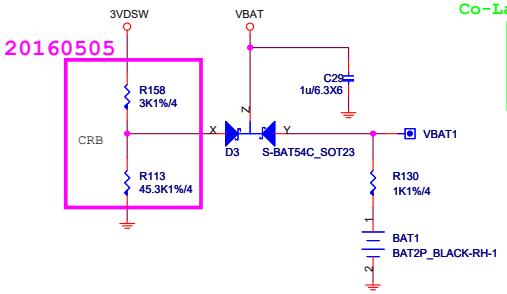


If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"

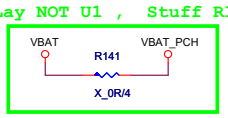
Co-Lay NOT USE U1 , C13 UnstuFF

Co-Lay NOT USE U1 , ALL UNSTUFF





Co-Lay NOT U1 , Stuff R18



20160505

Remove

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MS-7A78..		
Size: Custom	Document Description: Clear CMOS	Rev: 10
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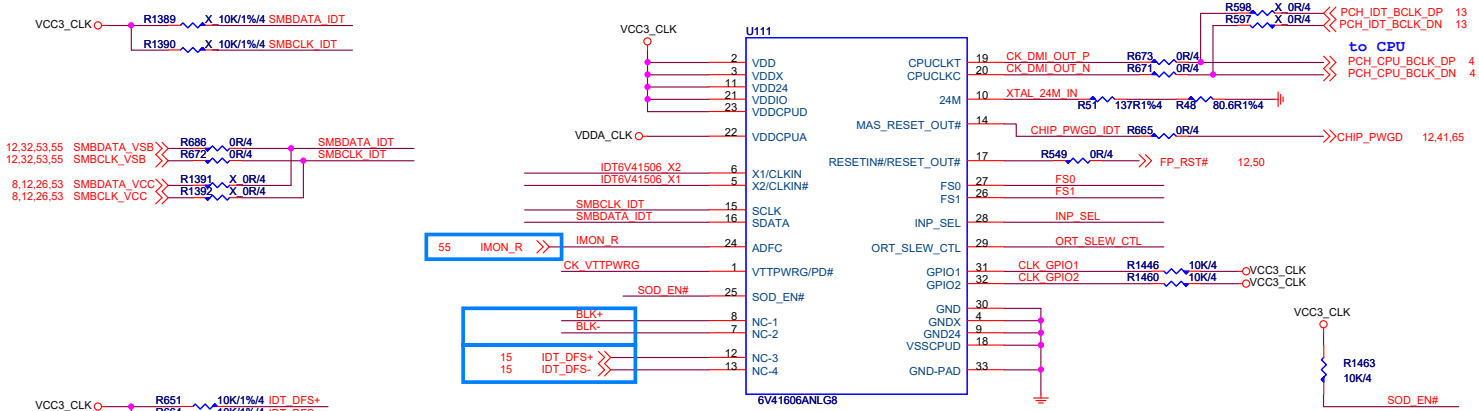
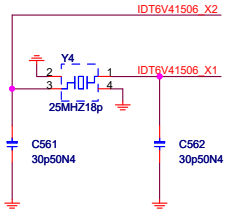
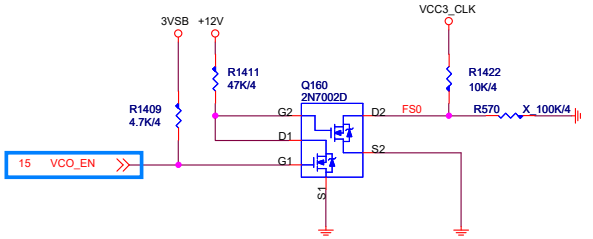
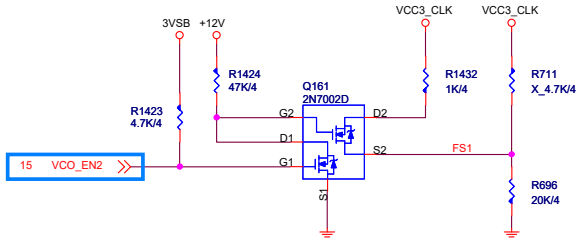


SMBUS adress:D2

Remove VDDA_CLK 0V.

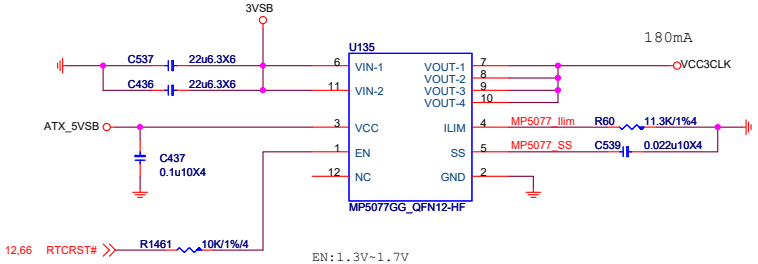


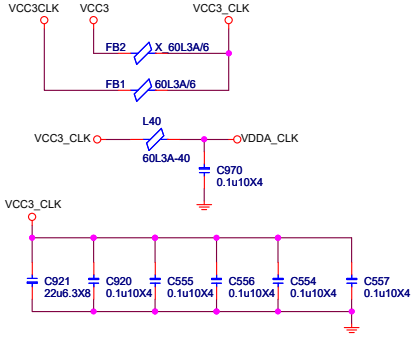


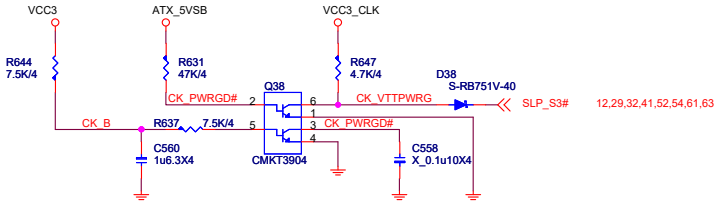


FS1	FS0	VCO Frequency
0	0	VCO 200MHz
0	1	VCO 400MHz (default)
1	0	VCO 1000MHz
1	1	VCO 100MHz

INP_SEL	
0	25MHz crystal input
1	100MHz differential input







To POWER 2015/02/03

MICRO-STAR INT'L CO.,LTD

MS-7A78..

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PCB

PCB1

7a78_0A

PD0-07A7810-G37
PD0-07A7810-E48

CPU_H1

CPU 顺帆

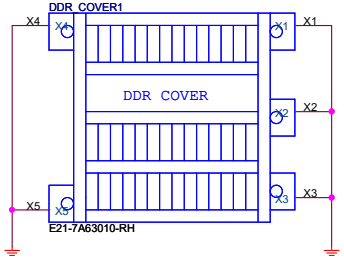
CPU_H1

BAT1_X1

BAT-BCR2032P-RH

DIMM Cover

DDR_COVER1



E21-7A63010-RH

VR Cover

VR_COVER1

E21-7A63020-RH

MKT_LA1 — LABEL — X_MKT_LABEL

CFOS_LA1 — LABEL — CFOS_LABEL

U31_LA1 — LABEL — U31_LABEL

NAH_LA1 — LABEL — NAH_LABEL

BIOS_LA1 — LABEL — BIOS_LABEL

SLI_LA1 — LABEL — SLI_LABEL

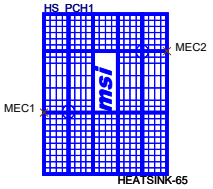
HDMI_LA1 — LABEL — HDMI_LABEL

XSPLIT_LA1 — LABEL — XSPLIT_LABEL

SSE_LA1 — LABEL — SSE_LABEL

PCH Heatsink

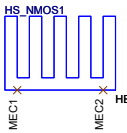
HS_PCH1



HEATSINK-65

North MOS Heatsink

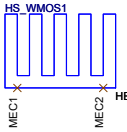
HS_NMOS1



HEATSINK-23

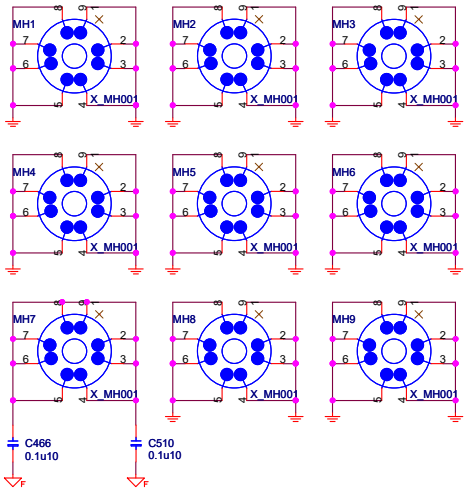
West MOS Heatsink

HS_WMOS1



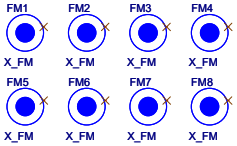
HEATSINK-23

Mounting Holes



Simulation

Optical Fiducial Marks-120



To POWER 2015/02/03

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