MS-7A39 Ver:1.0

CPU:
AMD AM4

System Chipset:
Promontory A320
(Value DIY or System Builder)

Main Memory:
DDR IV * 2 MAX:64 GB

VRM
RT8894 3+2

On Board Chipset:
LPC Super I/O --NCT6795
LAN RTL8111H

Azalia CODEC - Realtek
ALC887

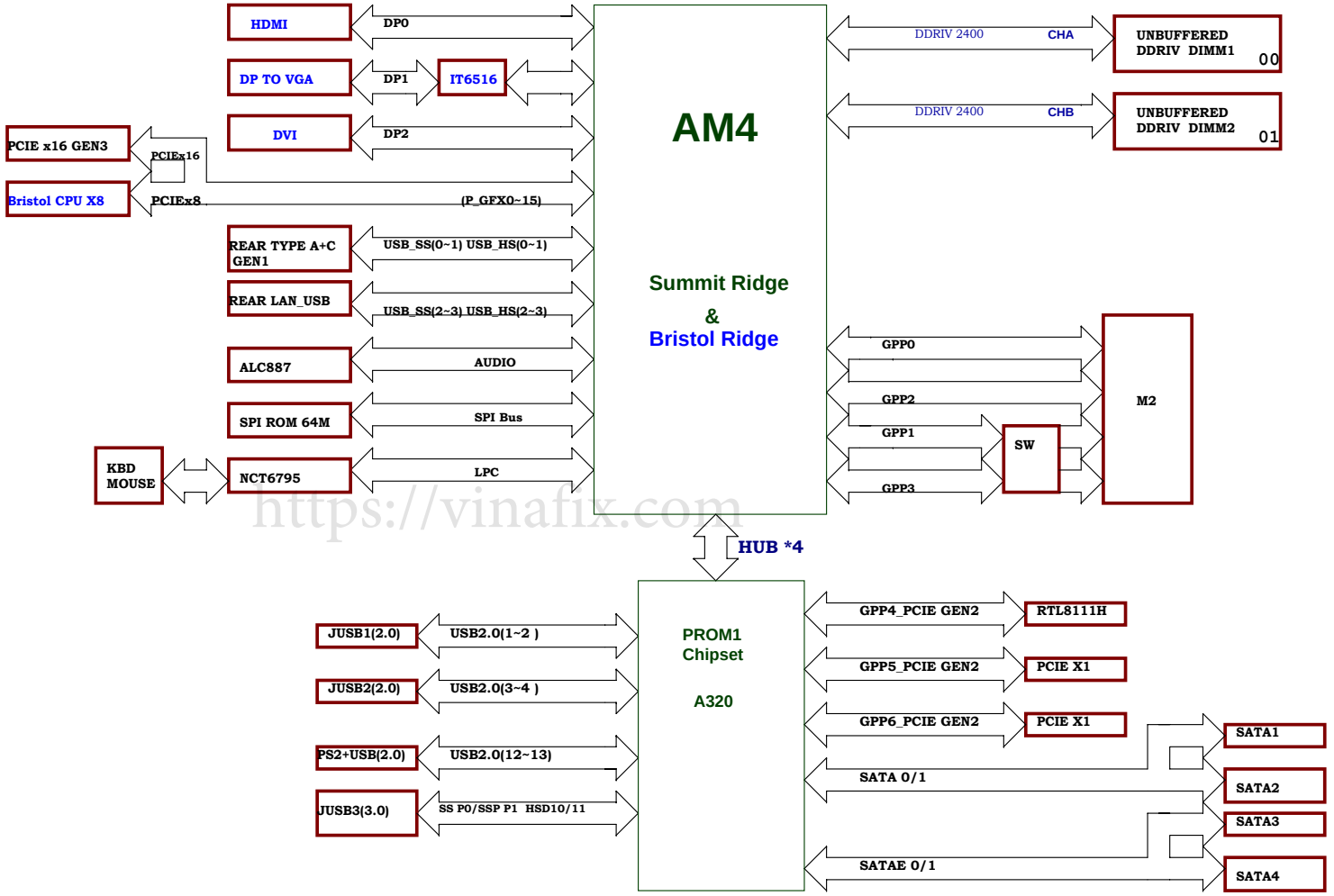
Expansion Slots:

From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1

OCP IC:

UP6273

FUSION BLOCK DIAGRAM



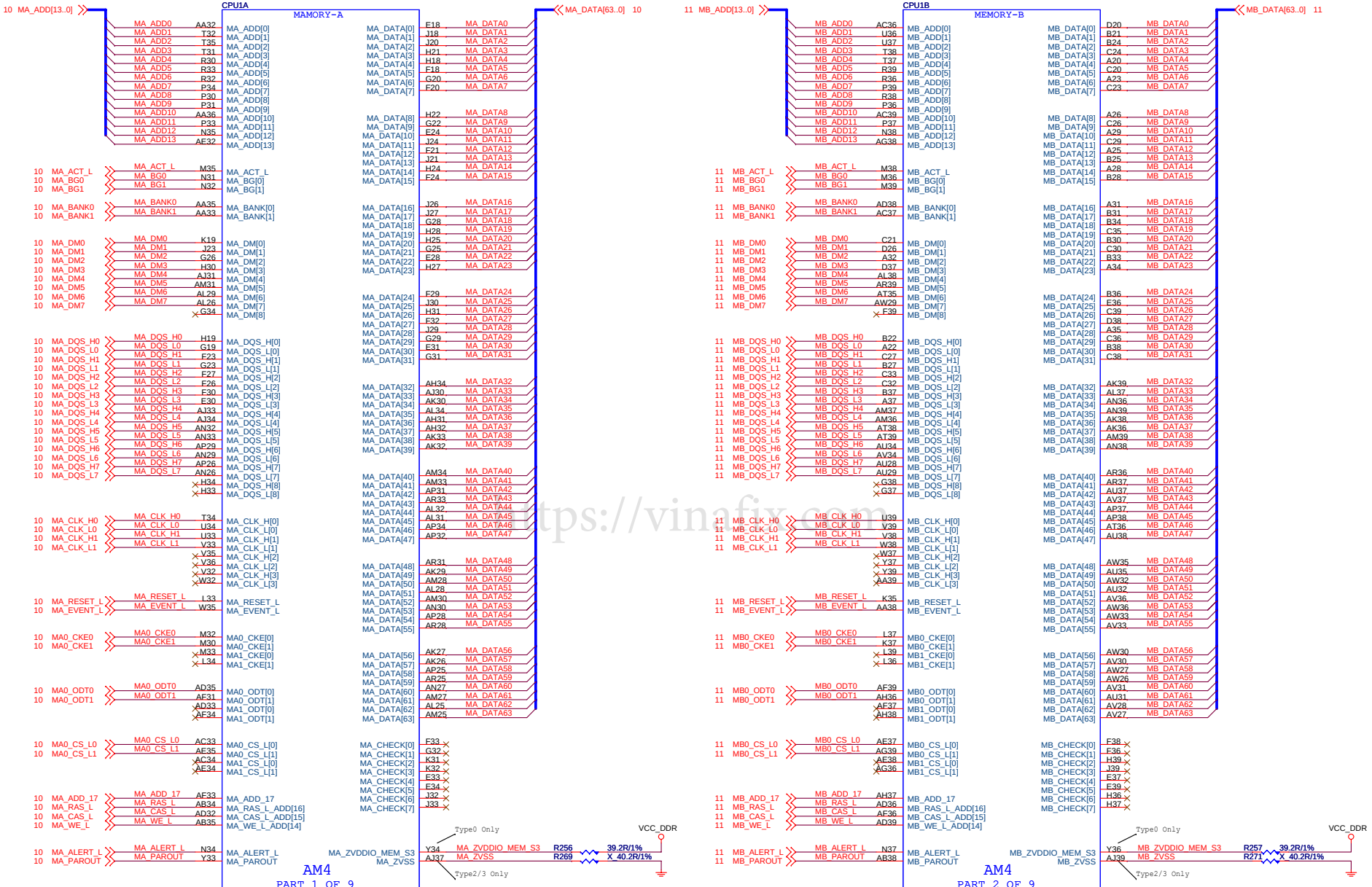
MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Tuesday, January 03, 2017	Sheet 1 of 55	

AMD AM4

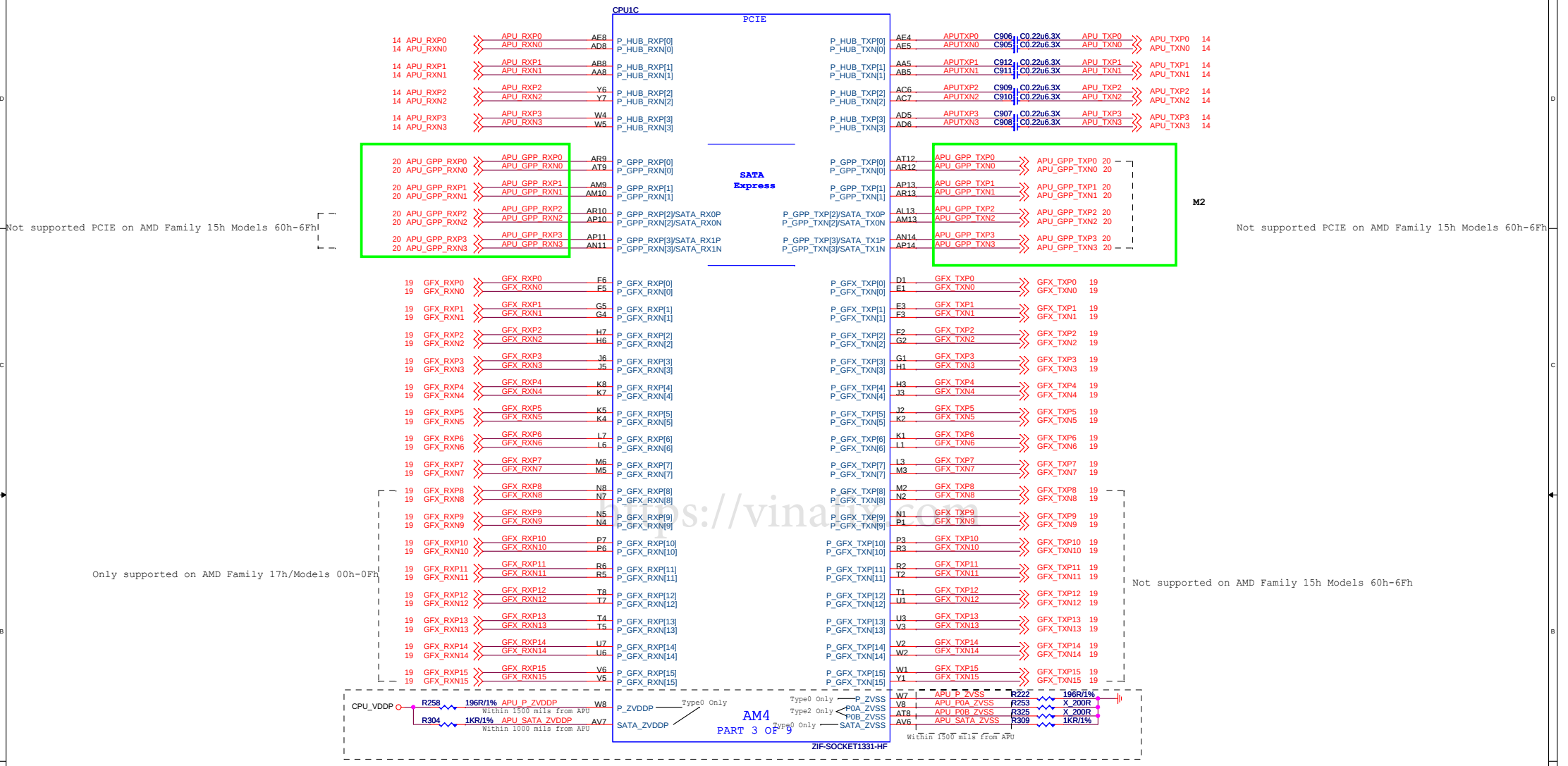
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: AM4 DDR4 I/F		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Tuesday, January 03, 2017	Sheet 2 of 55	



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

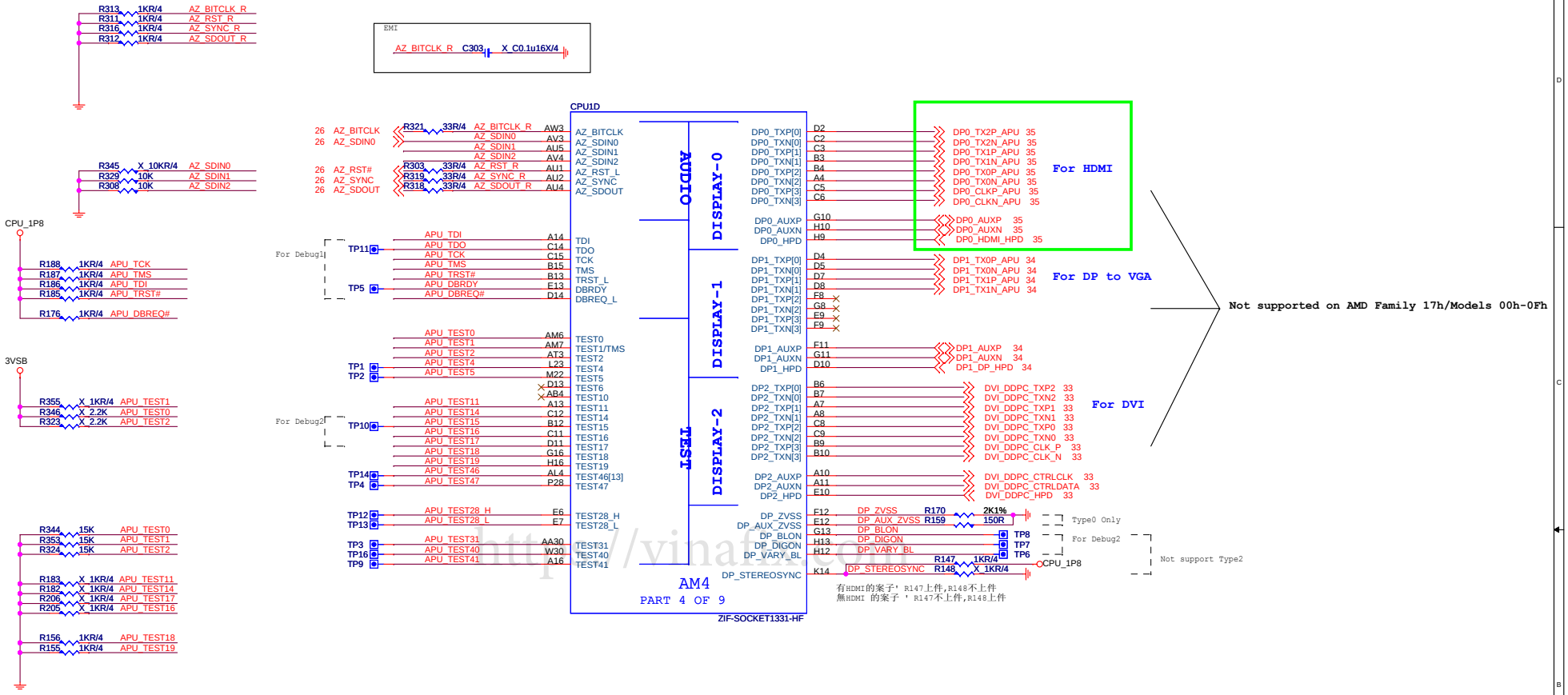
Title	AM4 DDR4 I/F	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 3 of 55	



Vinafix.com

MSI MICRO-START INT'L CO.,LTD.

Title: AM4 PCIE/SATAE		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 4 of 55	

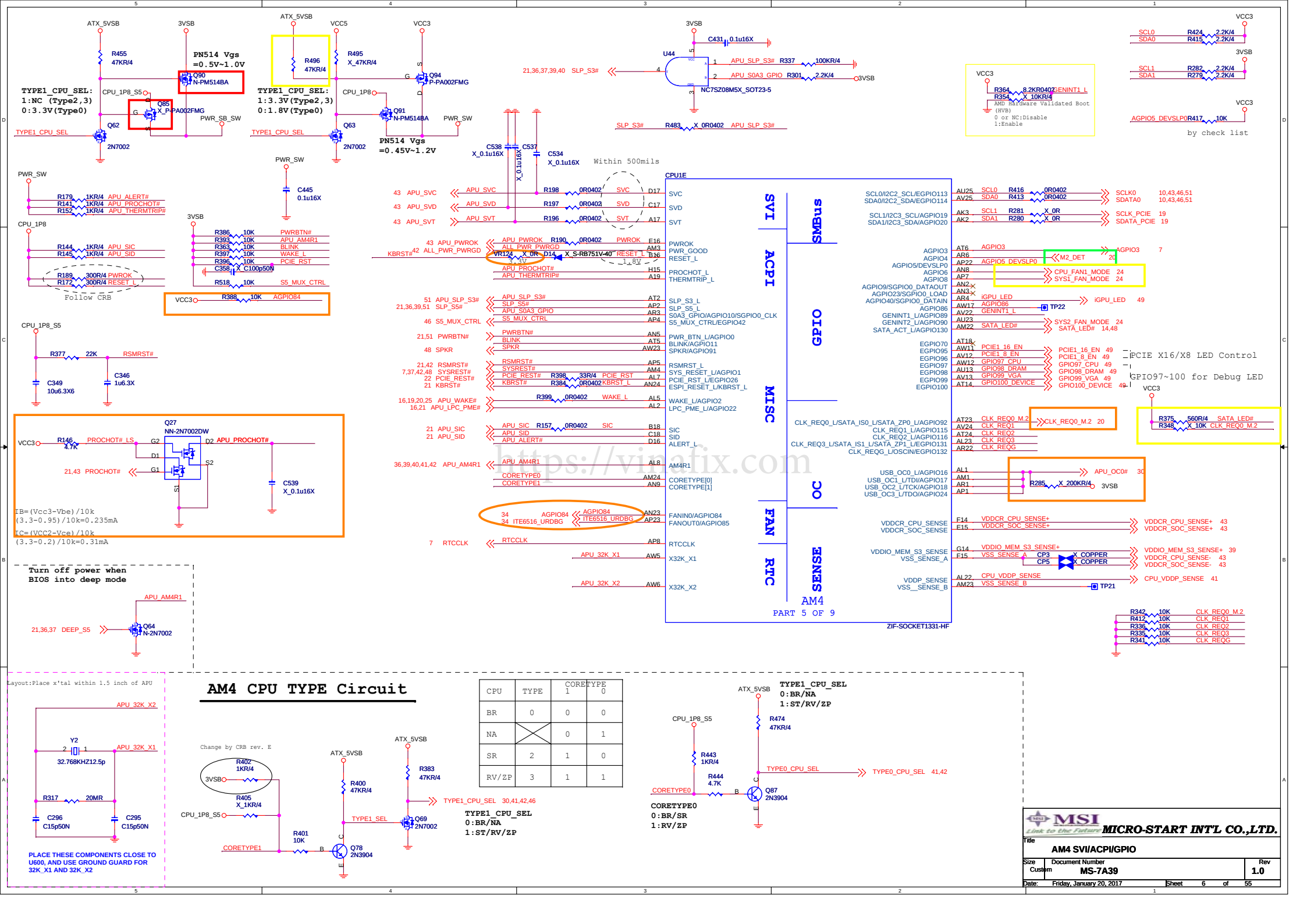


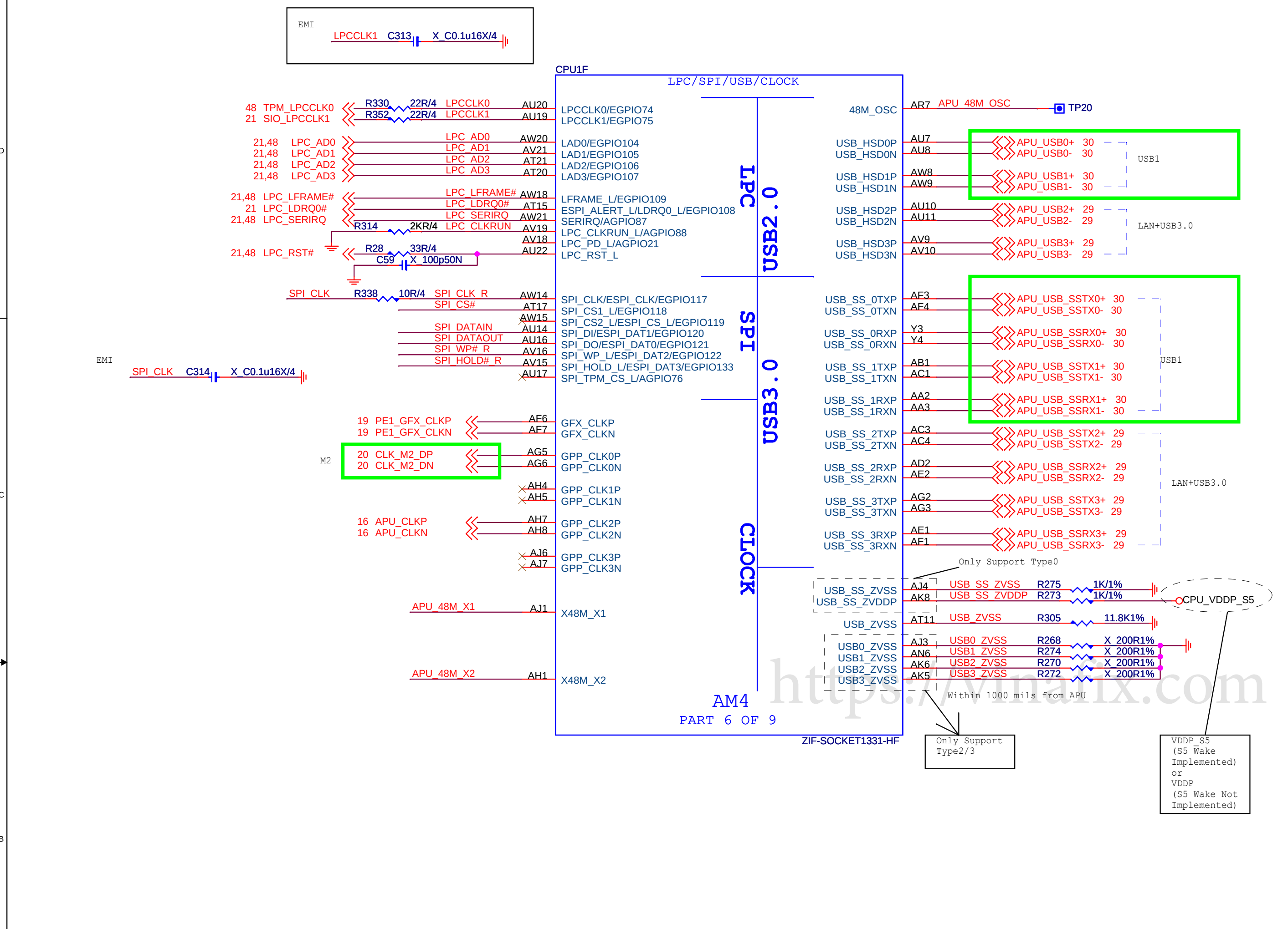
MSI MICRO-START INT'L CO.,LTD.

Title: AM4 DISPLAY/AUDIO

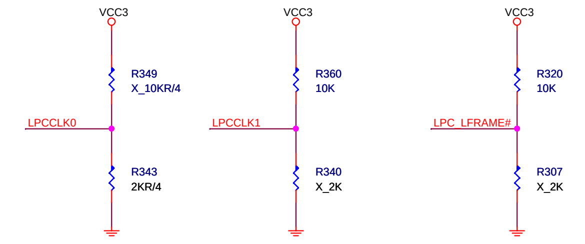
Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 5 of 55

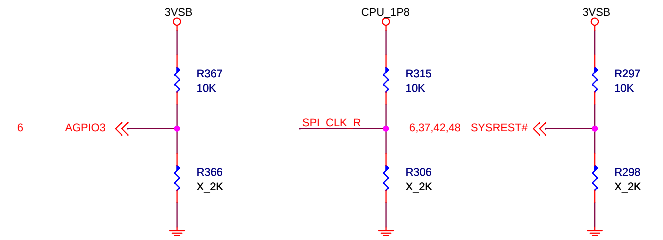

AM4 CPU TYPE Circuit
AM4 SVI/ACPI/GPIO
MICRO-START INT'L CO.,LTD.
MS-7A39
1.0
Friday, January 20, 2017
Sheet 6 of 55
PART 5 OF 9
ZIF-SOCKET1331-HF
TYPE1_CPU_SEL
1:NC (Type2,3)
0:3.3V(Type0)
PN514 Vgs
=0.5V~1.0V
TYPE1_CPU_SEL
1:3.3V(Type2,3)
0:1.8V(Type0)
0:1.8V(Type1)
PN514 Vgs
=0.45V~1.2V
Within 500mils
Follow CRB
Turn off power when
BIOS into deep mode
PLACE THESE COMPONENTS CLOSE TO
U600, AND USE GROUND GUARD FOR
32K_X1 AND 32K_X2
Layout:Place x'tal within 1.5 inch of APU
Change by CRB rev. E
CORETYPE0
0:BR/SR
1:RV/ZP
TYPE1_CPU_SEL
0:BR/NA
1:ST/RV/ZP
iPCIE X16/X8 LED Control
GPIO97~100 for Debug LED
by check list
SVI
ACPI
GPIO
SMBus
MISC
OC
FAN
RTC
SENSE
CPU1E
https://vinafix.com



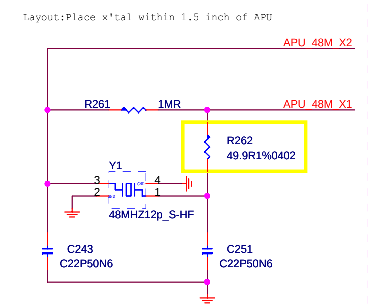
Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator **(Default)**	SPI ROM **(Default)**
PULL LOW	LPC device Boot Fail Timer Disabled **(Default)**	Configured for External clock generator ?????	LPC ROM

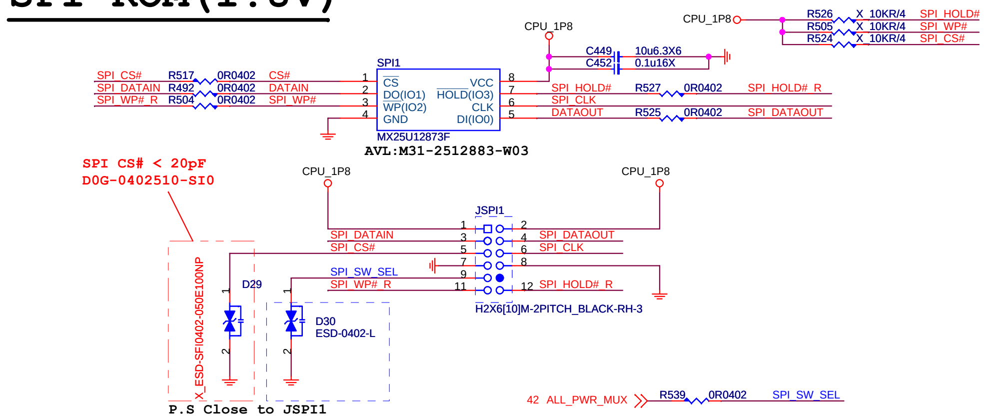


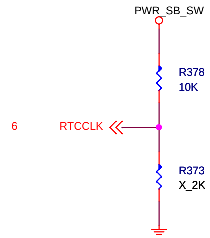
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	Normal reset mode **(Default)**
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

SPI ROM(1.8V)



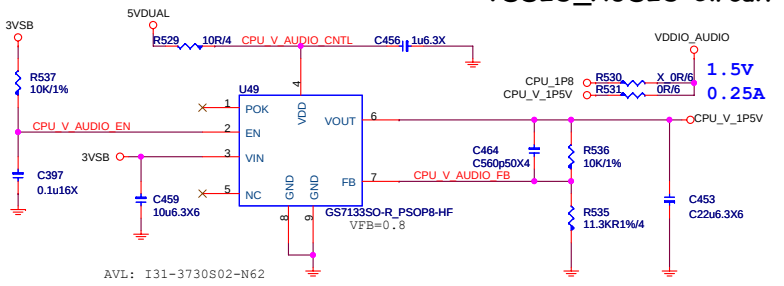


	RTCCLK
PULL HIGH	RTC Coin Battery is on board **(Default)**
PULL LOW	RTC Coin Battery is not on board

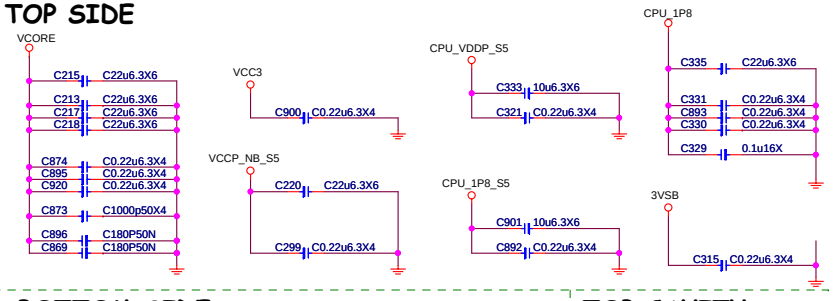
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	AM4 LPC/SPI/USB/CLK/STRAP	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 7 of 55	

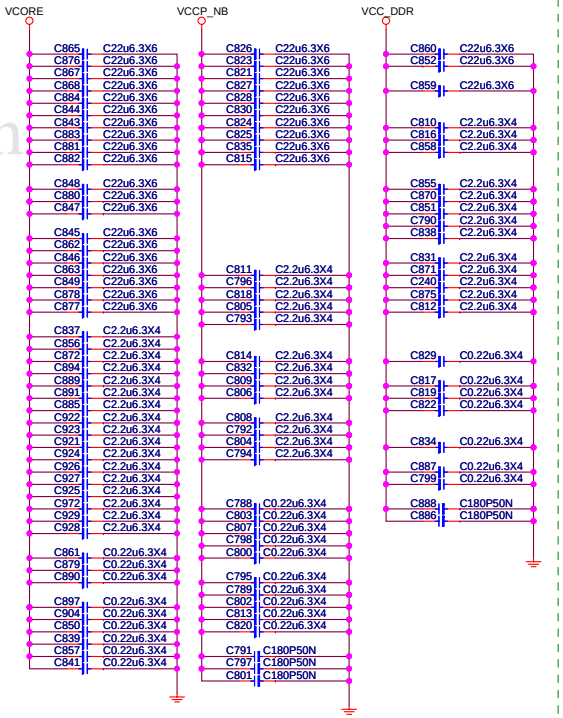
VDDIO_AUDIO Circuit



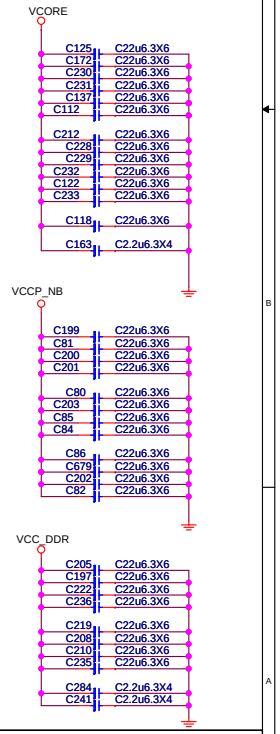
TOP SIDE

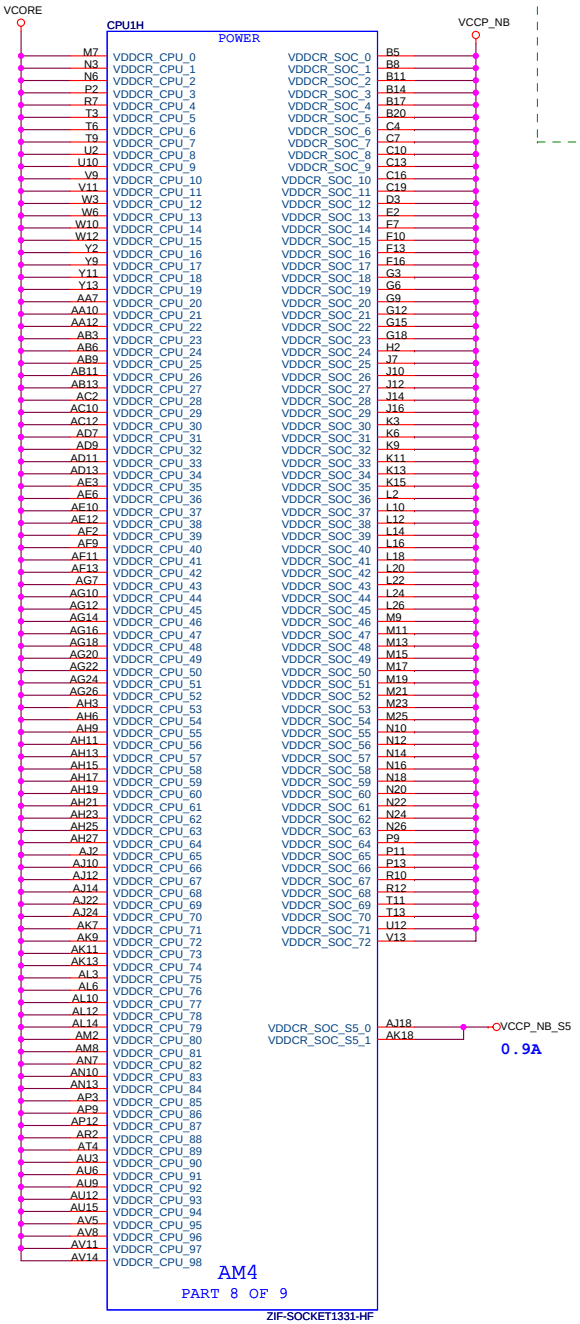


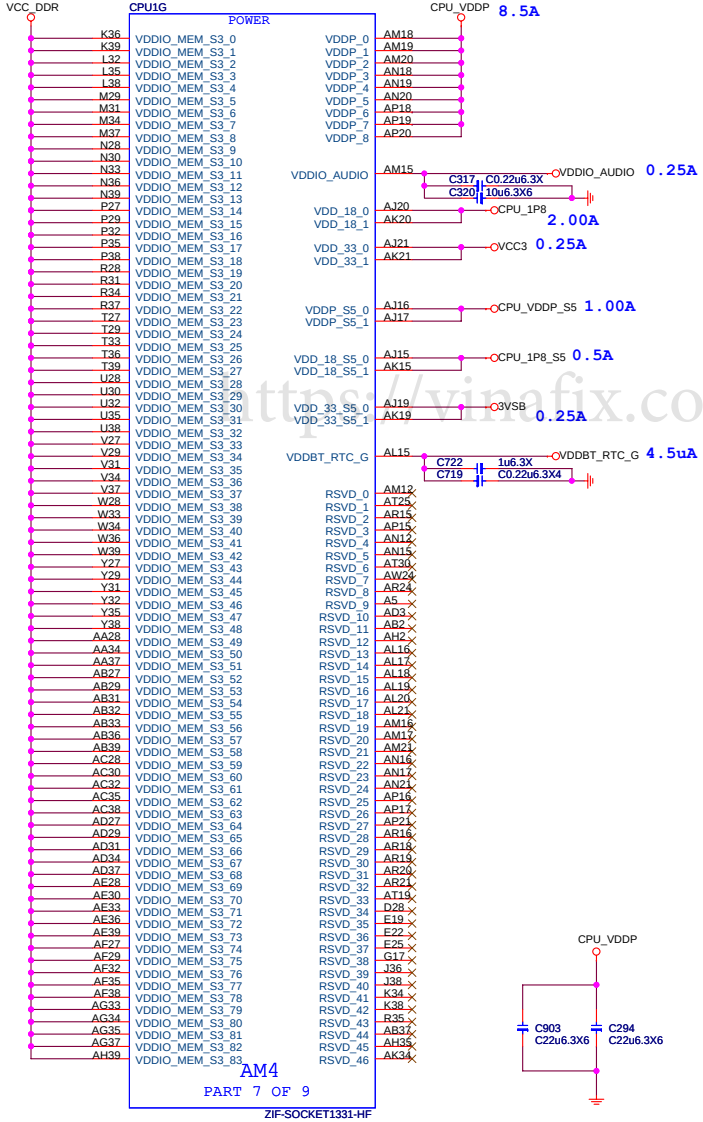
BOTTOM SIDE



TOP CAVITY

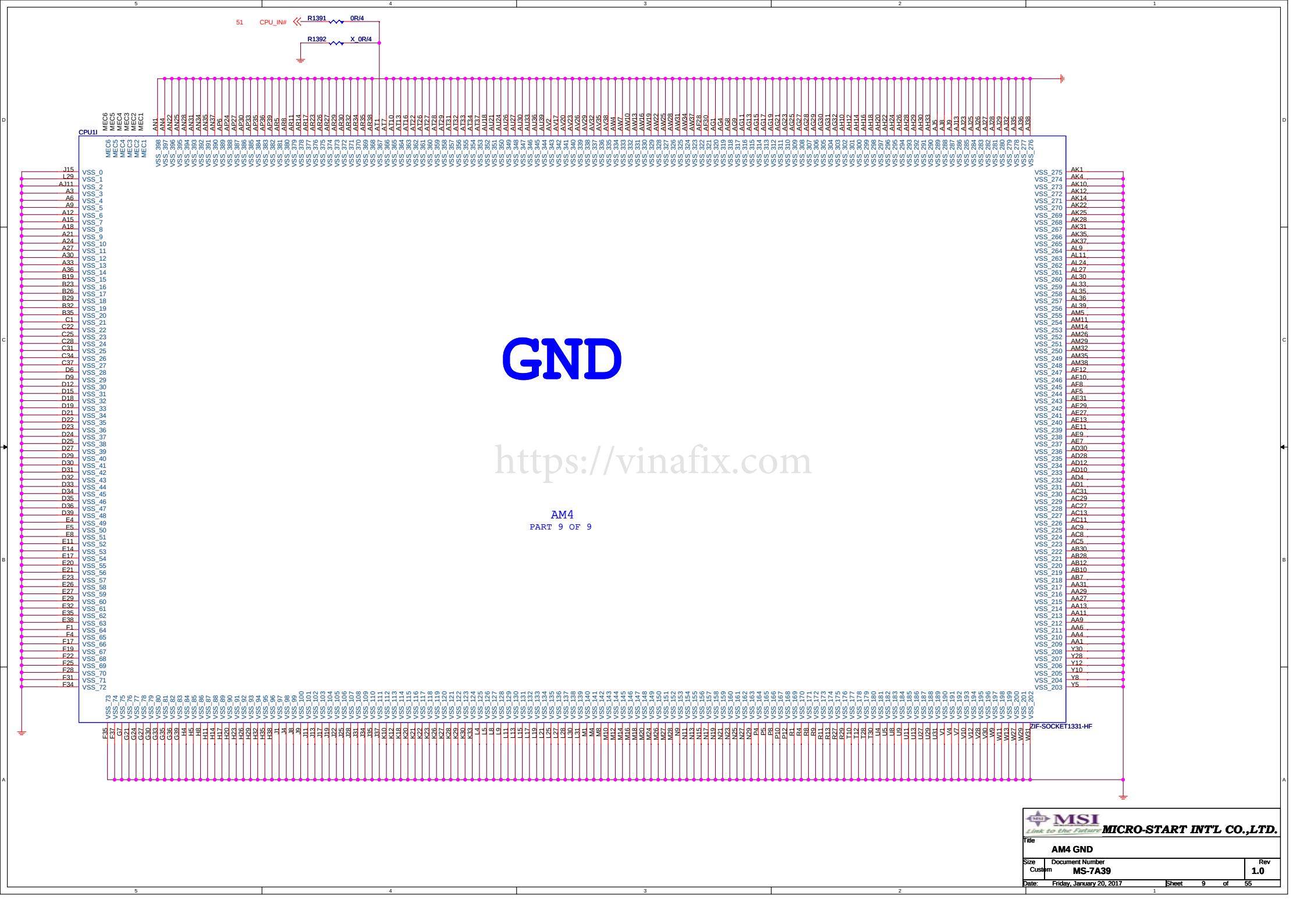






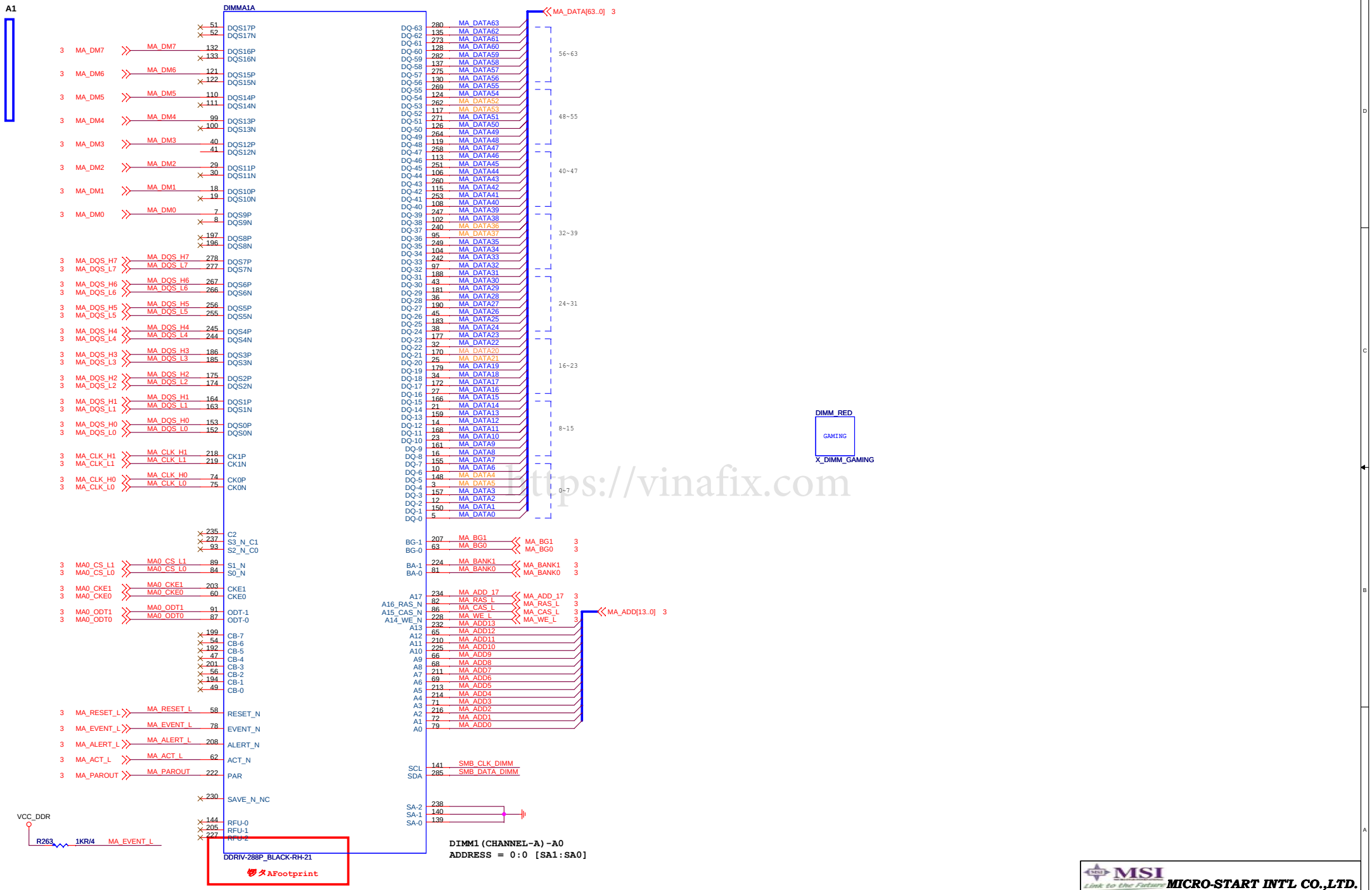
MSI MICRO-START INT'L CO.,LTD.

Title: AM4 Power/RTC Power		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 8 of 55	



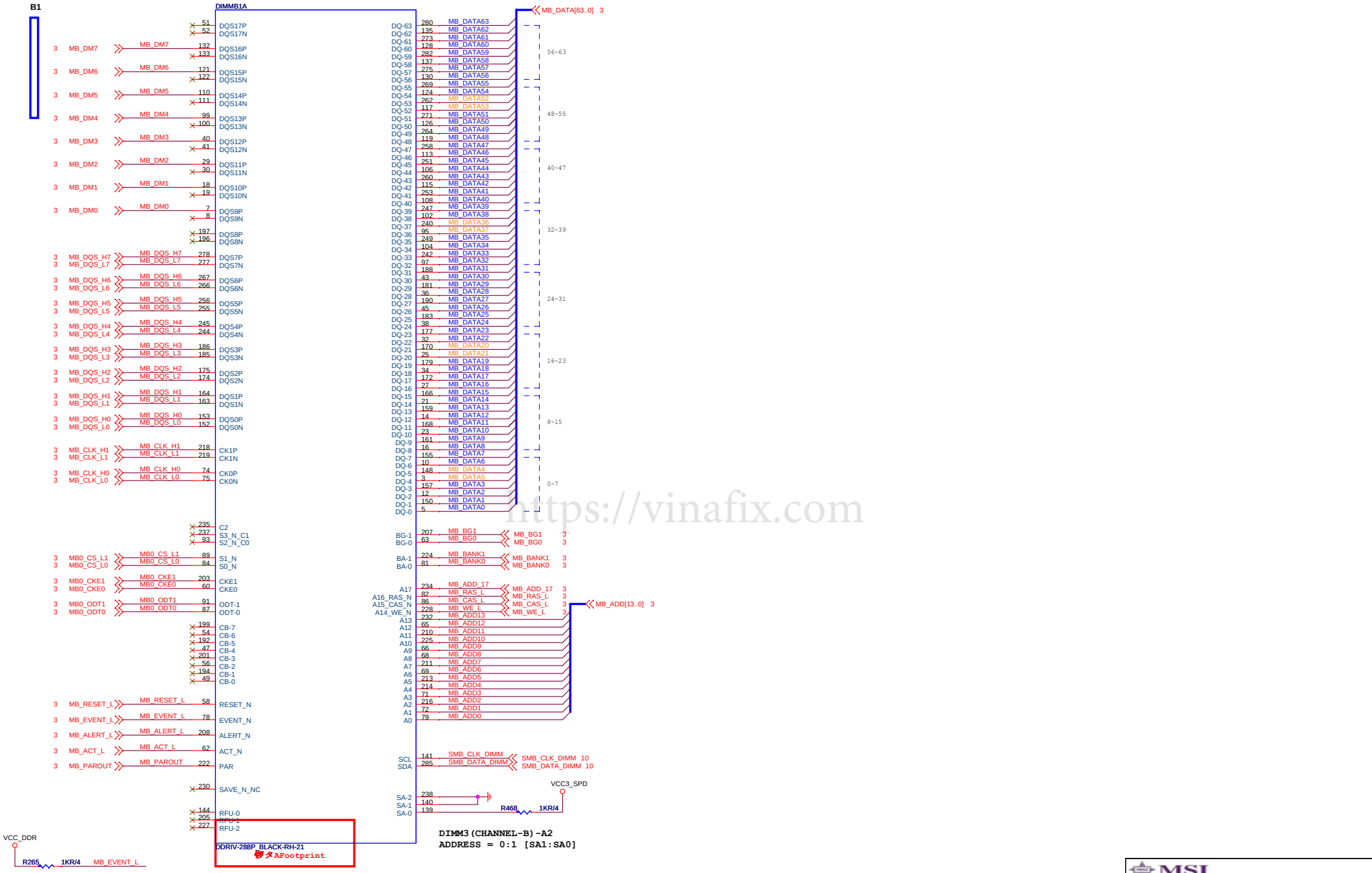
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	AM4 GND	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 9 of 55	



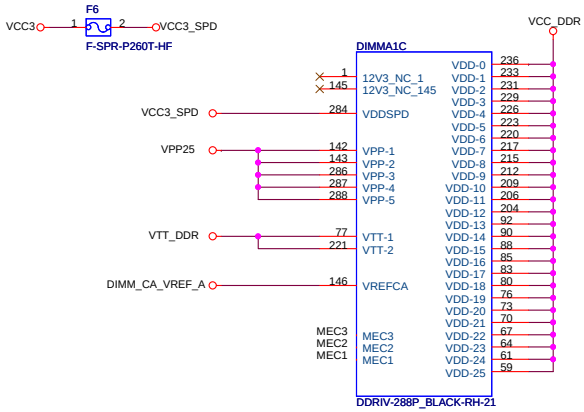
MICRO-START INT'L CO.,LTD.

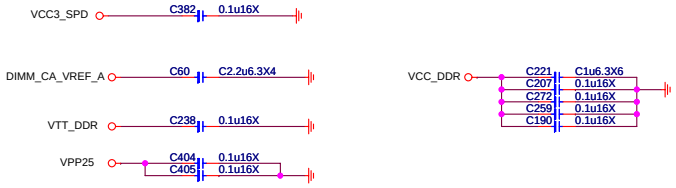
Title	DDR4 DIMM CH-A		
Size: Custom	Document Number: MS-7A39		Rev: 1.0
Date: Friday, January 20, 2017	Sheet 10 of 55		

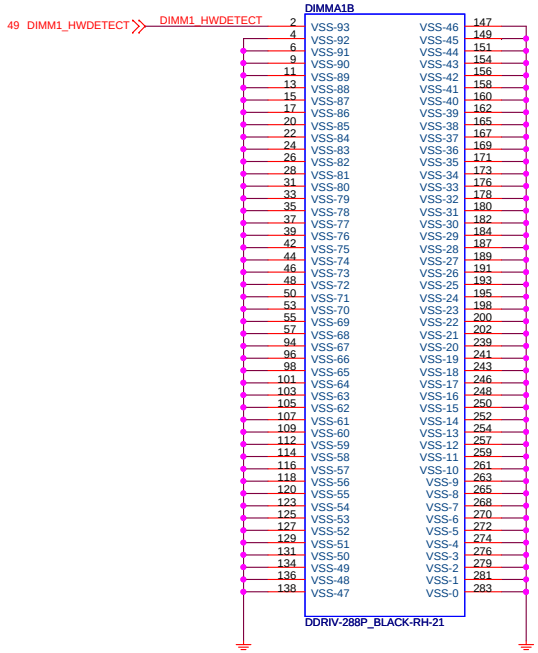


MICRO-START INT'L CO.,LTD.

Title	DDR4 DIMM CH-B	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 11 of 55	

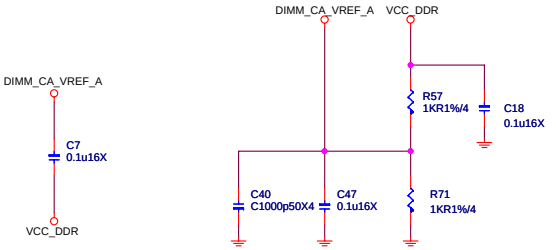






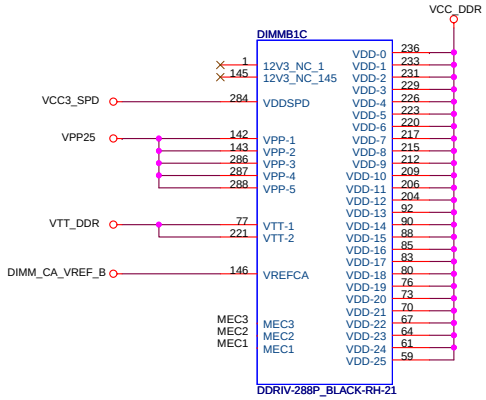
DDR VREF

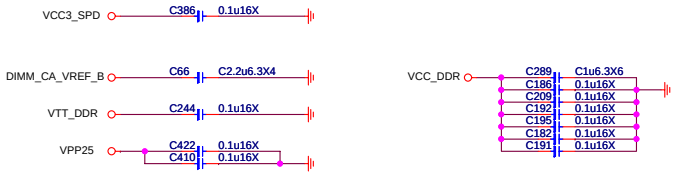
(place resistors close to DIMMs)

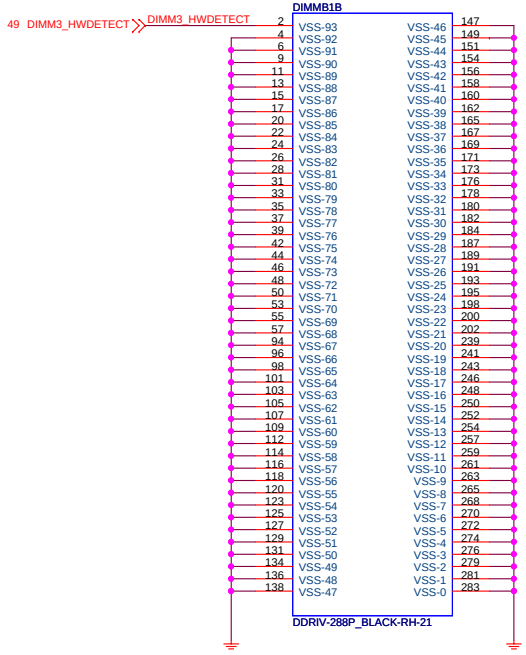


MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	DDR4-POWER/GND-1	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 12 of 55	

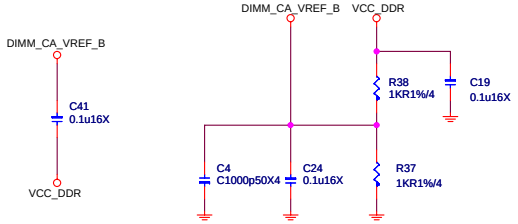






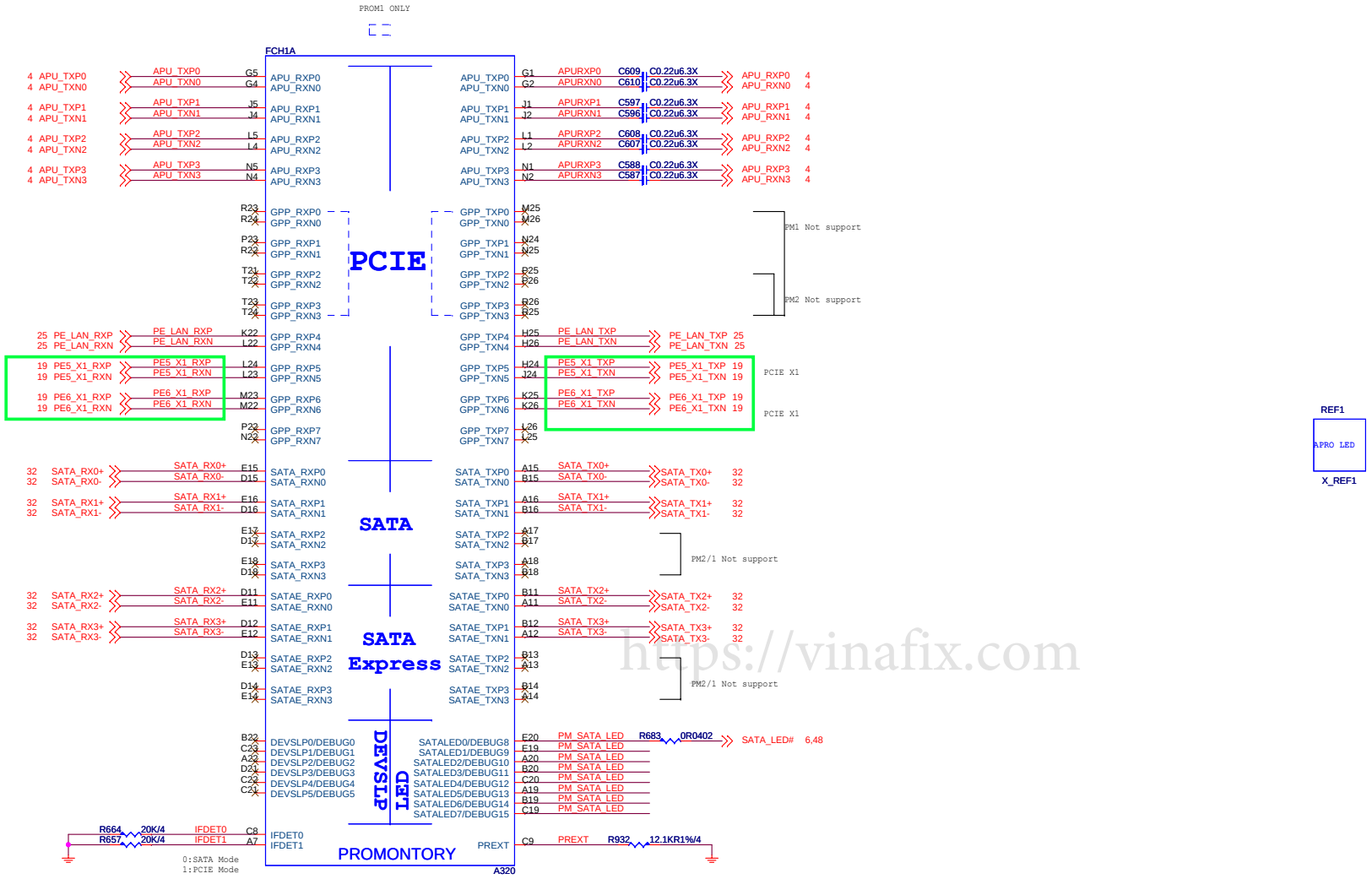
DDR VREF

(place resistors close to DIMMs)



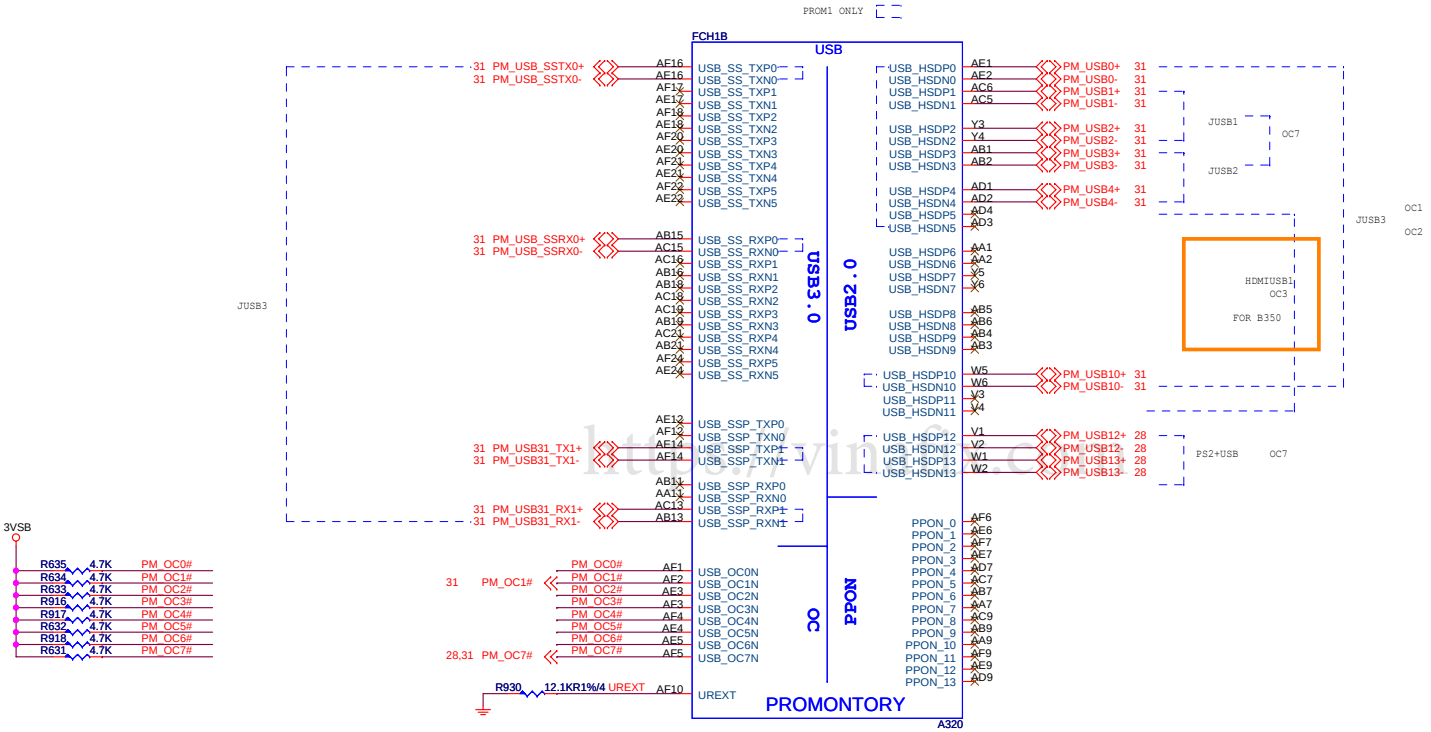
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: DDR4-POWER/GND-2		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 13 of 55	



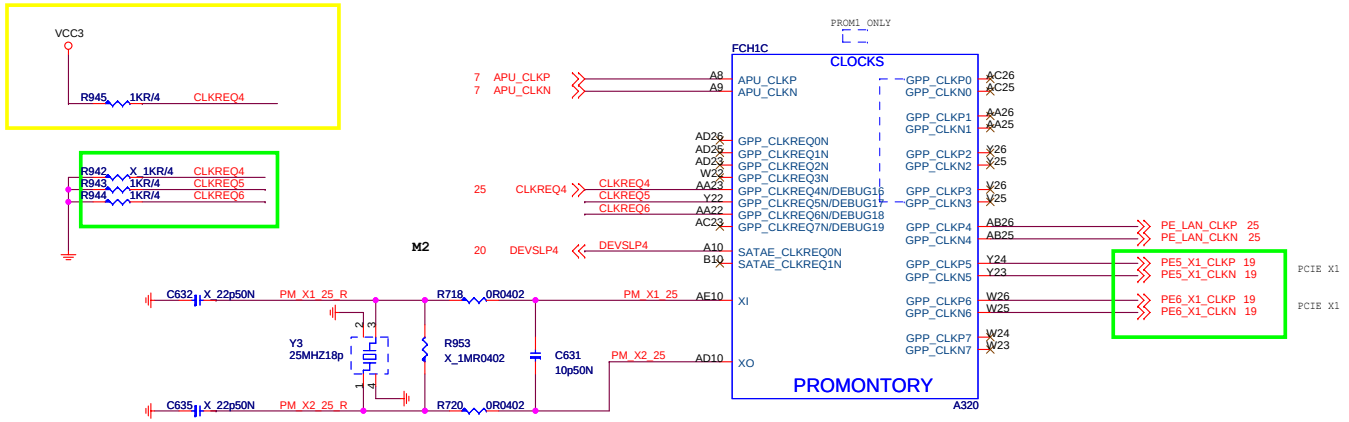
MSI MICRO-START INT'L CO.,LTD.

Title: Promontory-PCIE/SATA/SATAE		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 14 of 55	

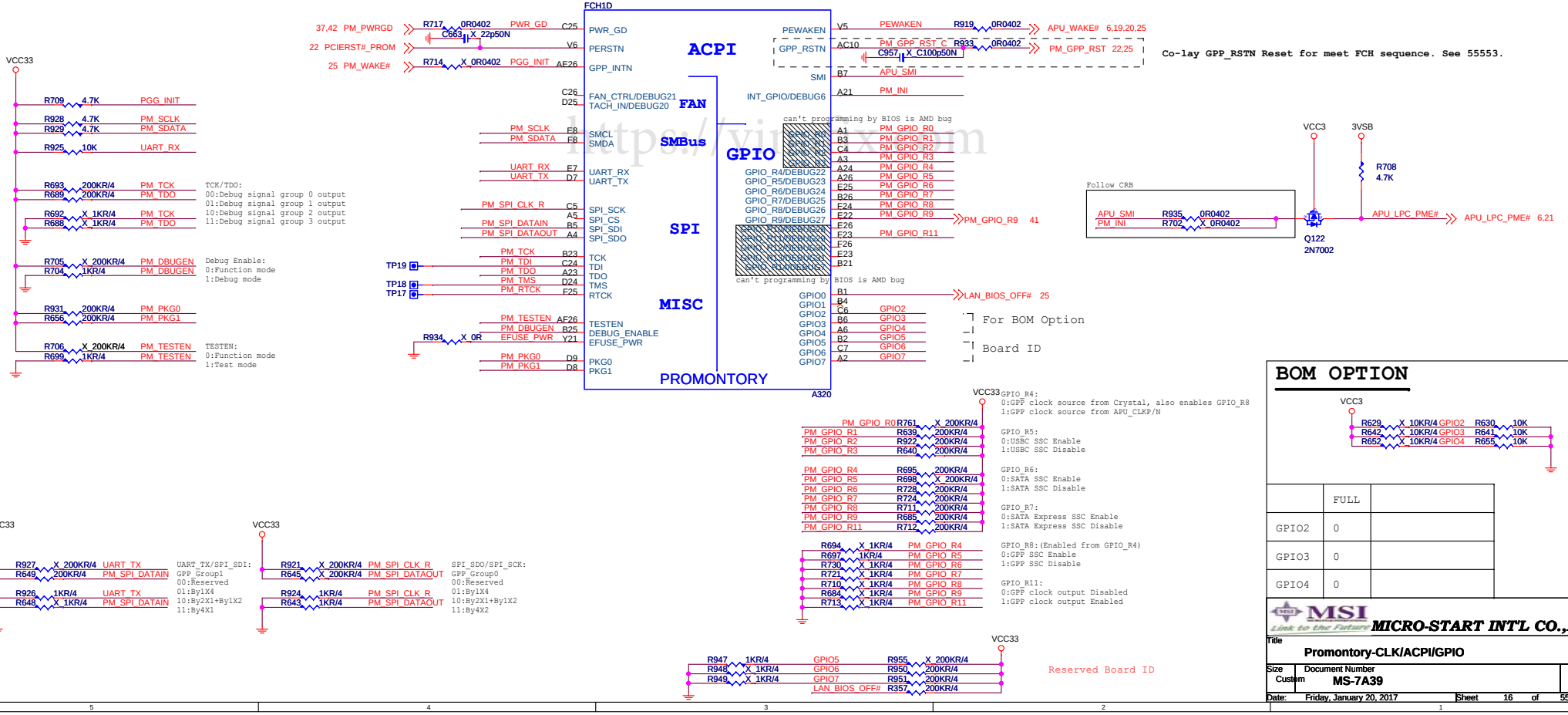


MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Promontory-USB/OC		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 15 of 55	



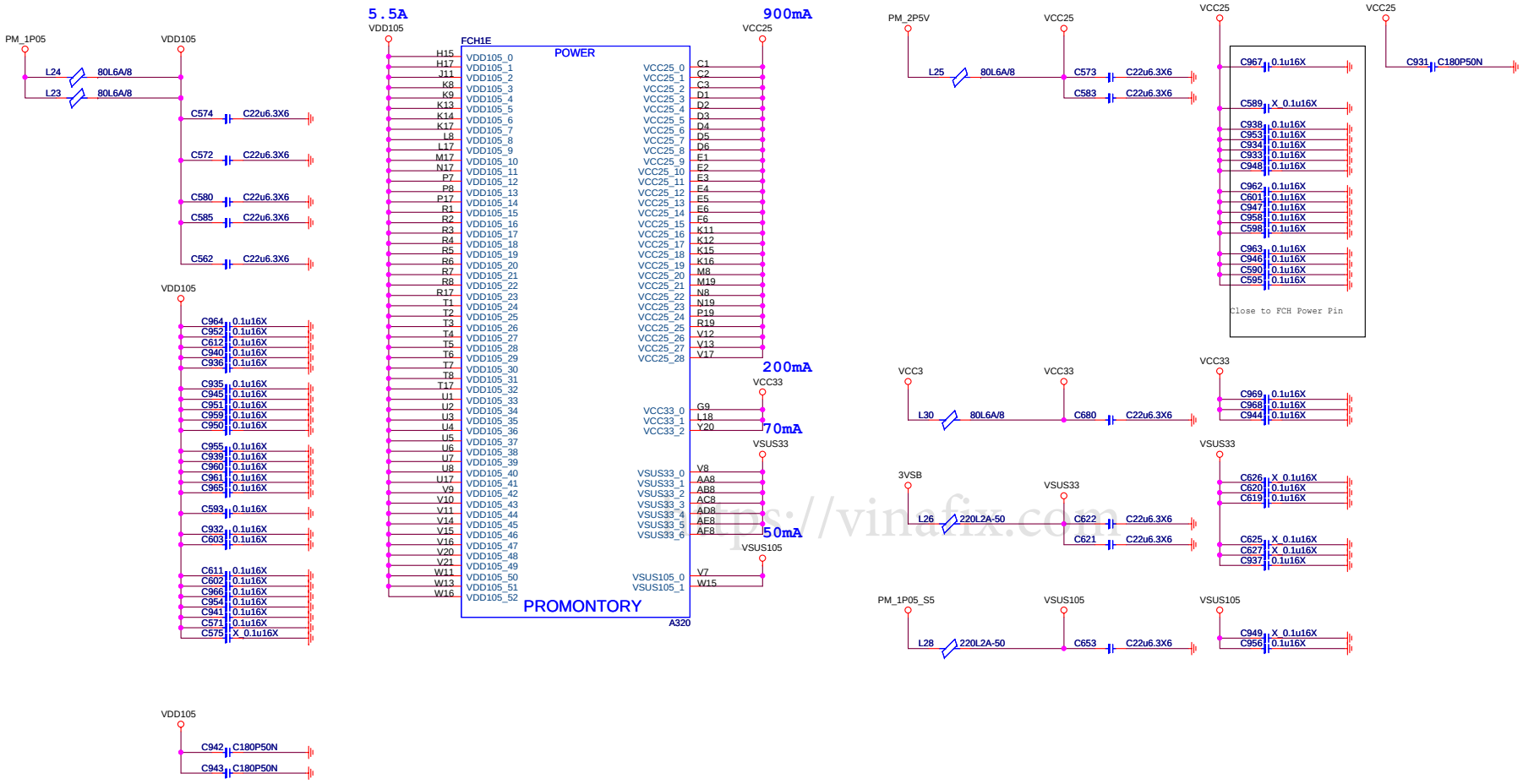
Vinafix.com



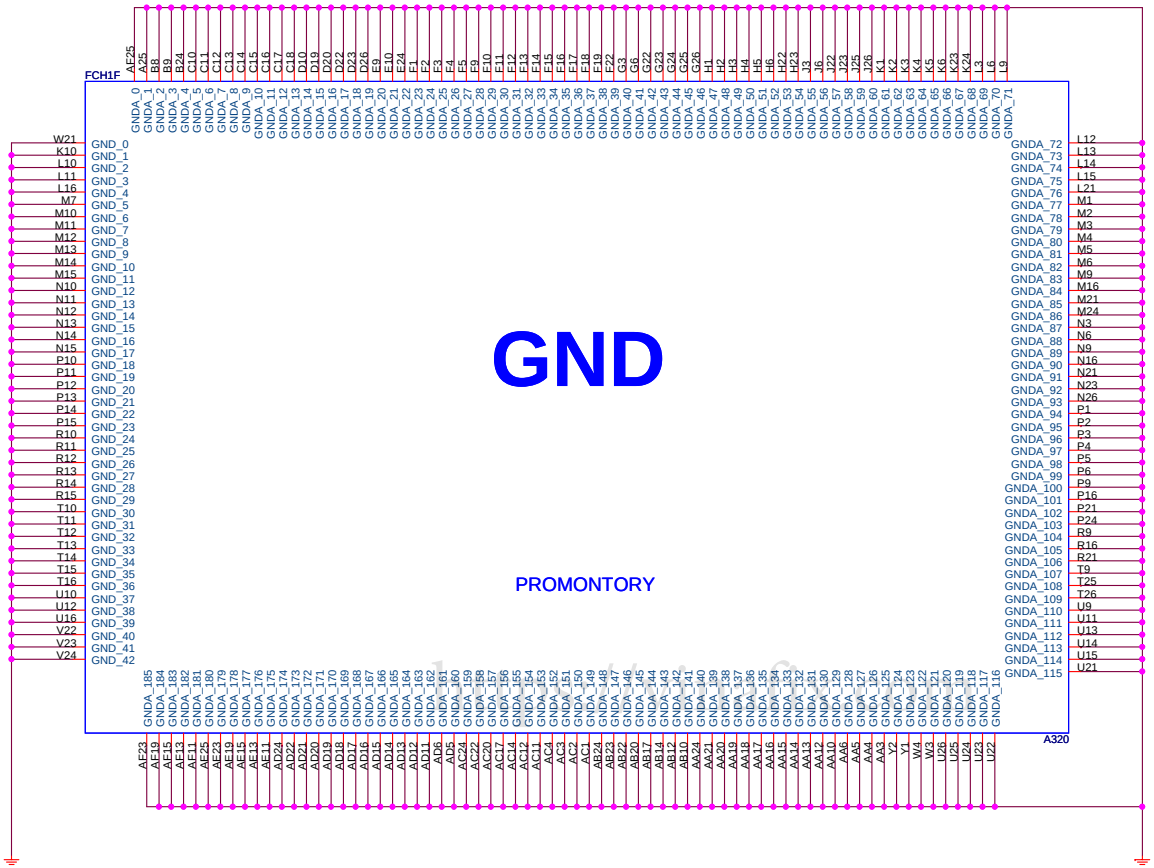
	FULL	
GPIO2	0	
GPIO3	0	
GPIO4	0	

MICRO-START INTL CO.,LTD.

Title	Promontory-CLK/ACPI/GPIO	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 16 of 55	



MSI Link to the Future	MICRO-START INT'L CO.,LTD.	
Title: Promontory-Power		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 17 of 55	



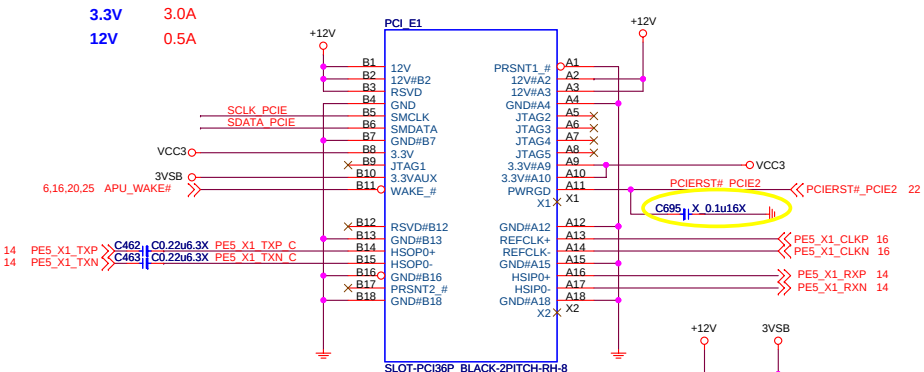
MSI	MICRO-START INT'L CO.,LTD.
Title	Promontory-GND
Size	Custom
Document Number	MS-7A39
Rev	1.0
Date:	Friday, January 20, 2017
Sheet	18 of 55

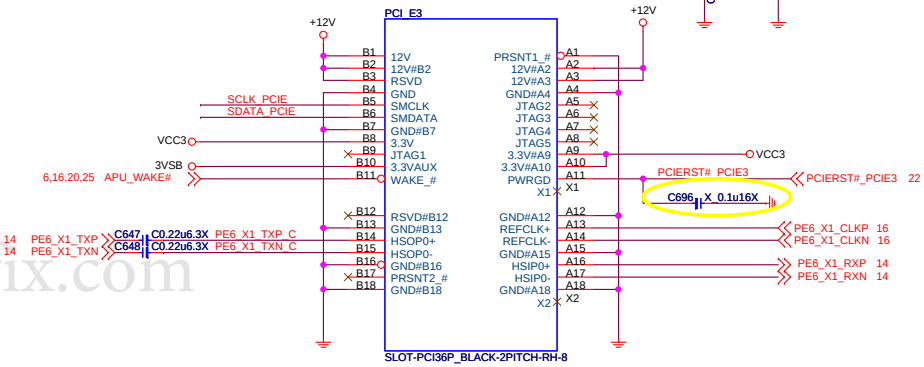
PCI EXPRESS x16 Slot

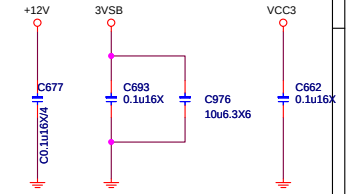
3.3V 3.0A
12V 5.5A

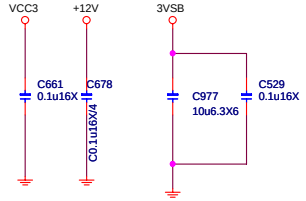
PCIEX1 12V 0.5A
3.3V weak 375mA

3.3V 3.0A
12V 0.5A

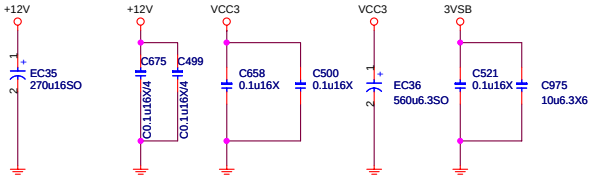




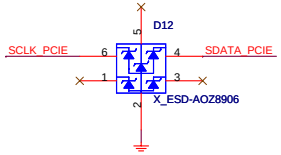




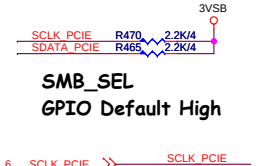
PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



PCIE2_16
GAMING
X_PCIE X16



SMBus separate circuit



MSI MICRO-START INT'L CO.,LTD.

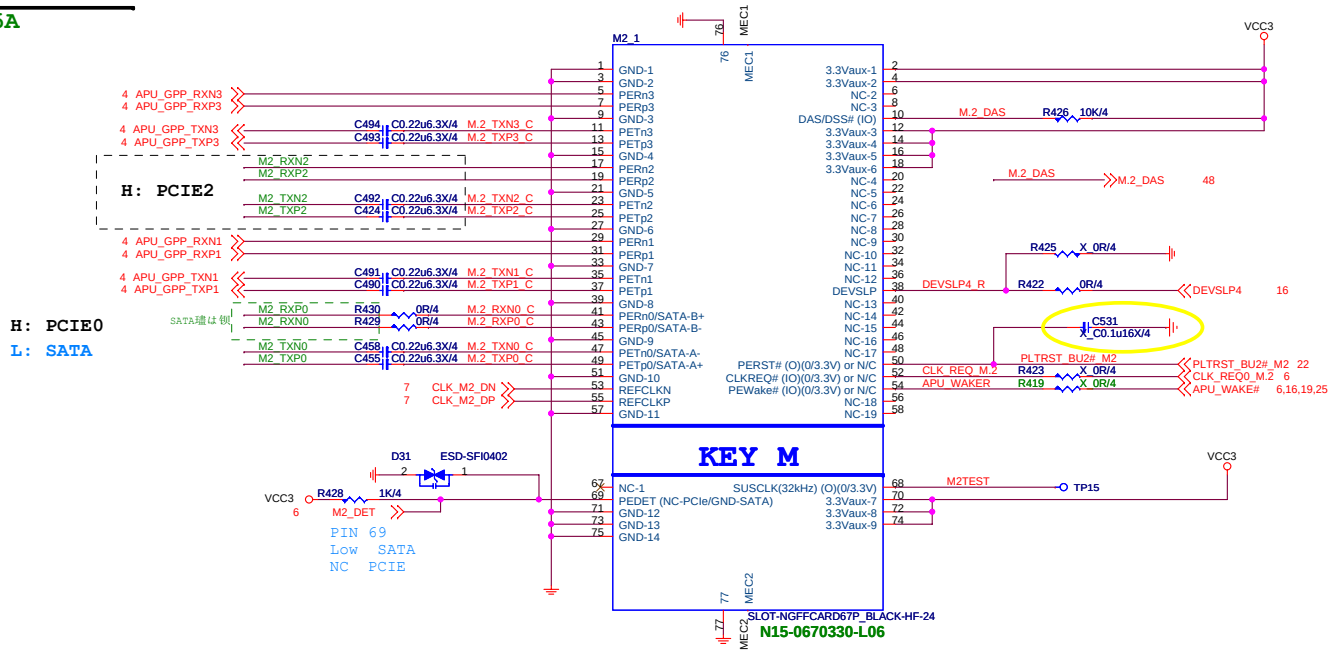
Title: PCIE X16(X1*2) SLOT

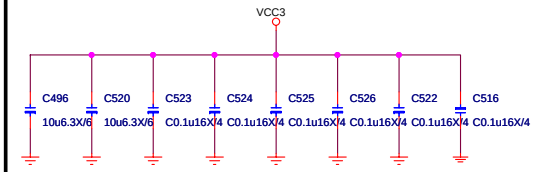
Size: Custom | Document Number: MS-7A39 | Rev: 1.0

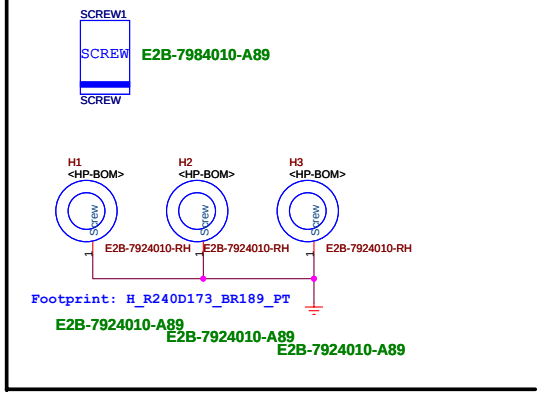
Date: Friday, January 20, 2017 | Sheet 19 of 55

M.2 Connector

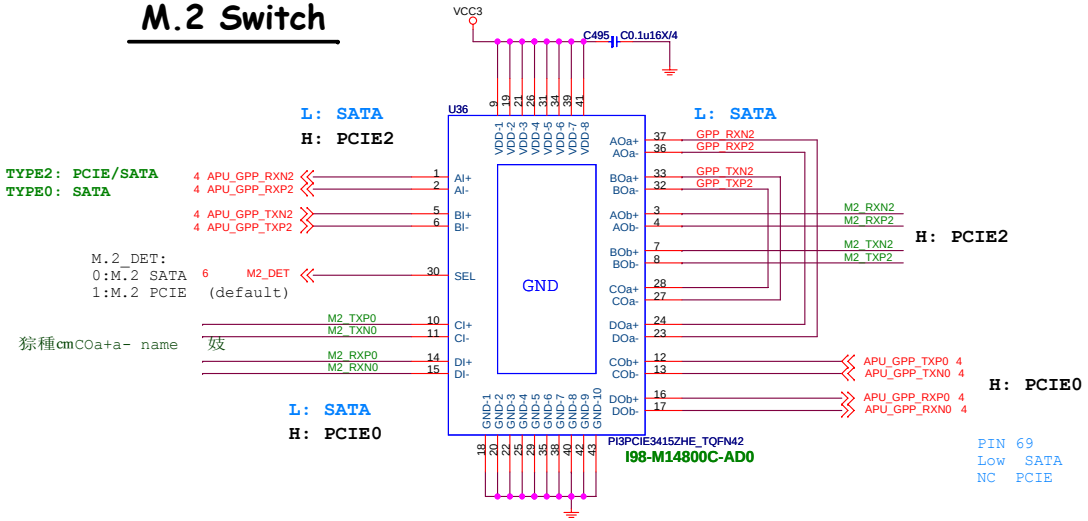
3.3V@2.5A



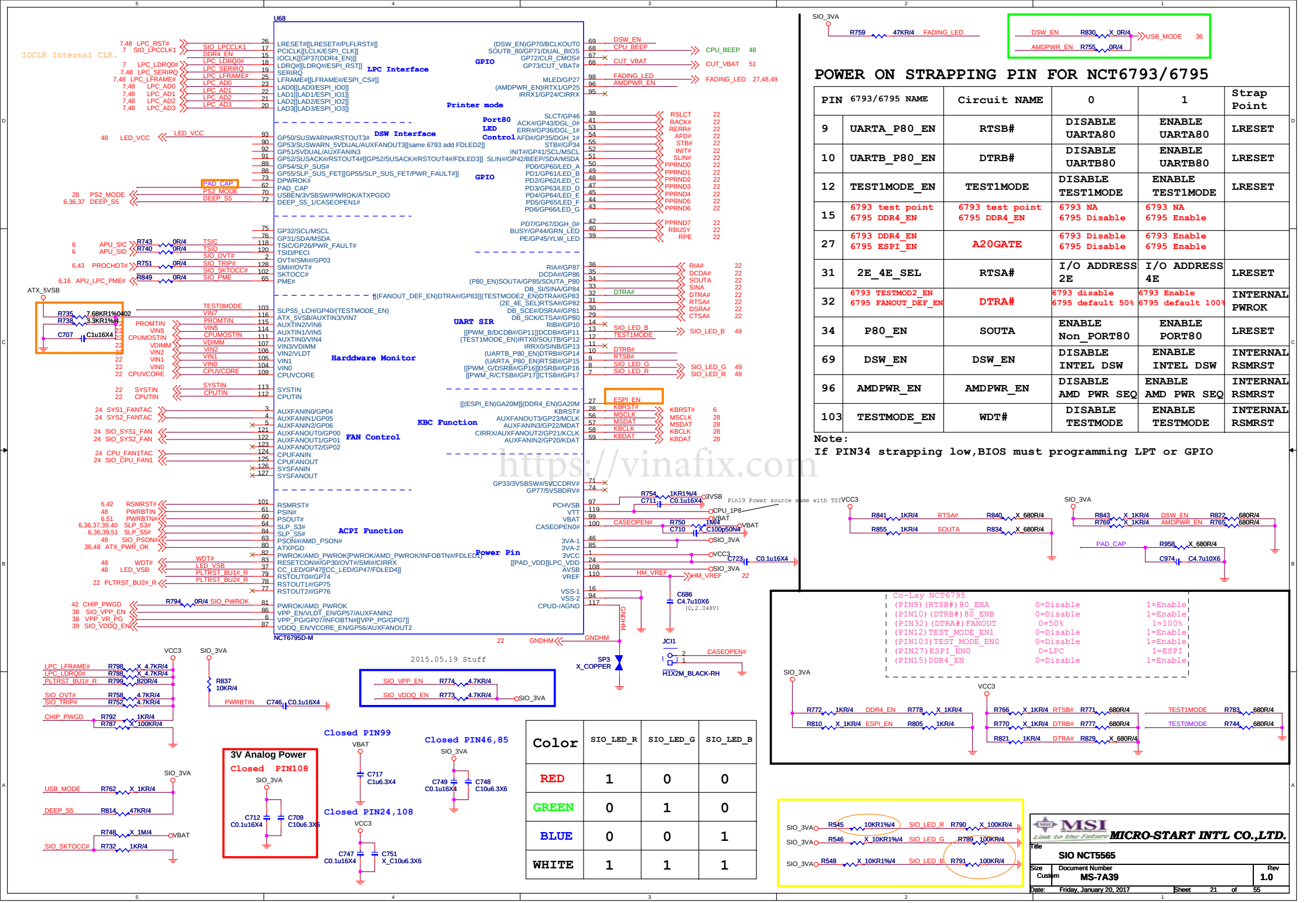




M.2 Switch



MSI MICRO-START INT'L CO.,LTD.			
Title: M2			
Size: Custom	Document Number: MS-7A39		Rev: 1.0
Date: Friday, January 20, 2017		Sheet 20 of 55	



POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

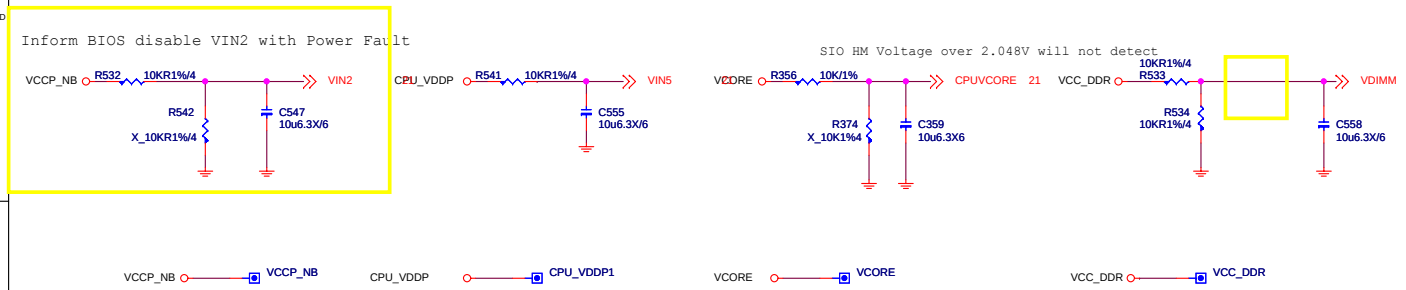
Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

Co-Lay NCT6795
(PIN9)(RTSB#)80_ENA 0=Disable 1=Enable
(PIN10)(DTRB#)80_ENB 0=Disable 1=Enable
(PIN32)(DTRA#)FANOUT 0=50% 1=100%
(PIN12)TEST_MODE_EN1 0=Disable 1=Enable
(PIN103)TEST_MODE_EN0 0=Disable 1=Enable
(PIN27)ESPI_EN0 0=LPC 1=ESPI
(PIN15)DDR4_EN 0=Disable 1=Enable

Title	SIO NCT5565
Size / Document Number	Custom / MS-7A39
Rev	1.0
Date:	Friday, January 20, 2017
Sheet	21 of 55

MICRO-START INT'L CO.,LTD.

HW Monitor - Voltage



VCCP_NB → VCCP_NB

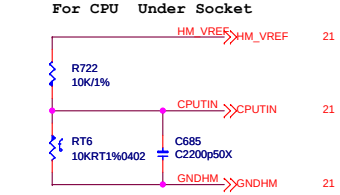
CPU_VDDP → CPU_VDDP1

VCORE → VCORE

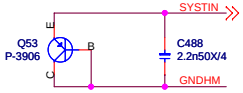
VCC_DDR → VCC_DDR

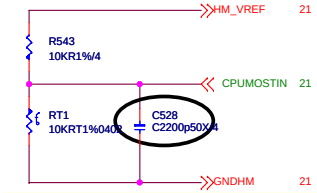
Thermal Monitor

For CPU Under Socket

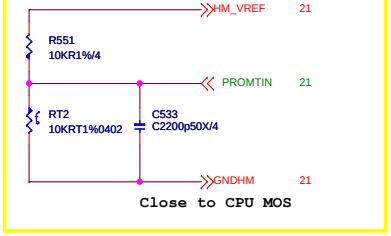


For System Close to SIO



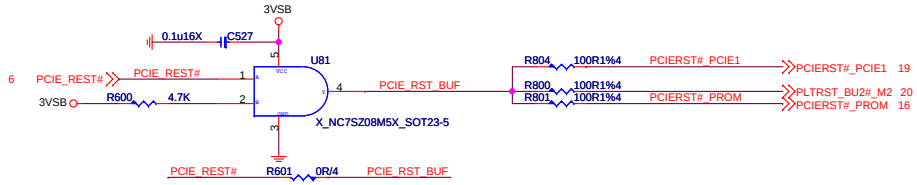


Close to CPU MOS

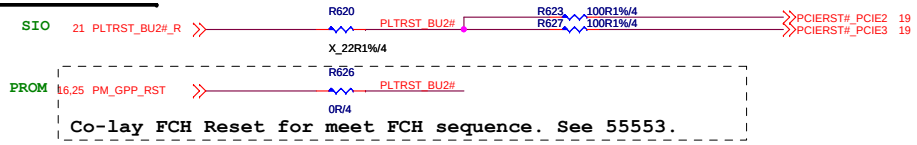


Close to CPU MOS

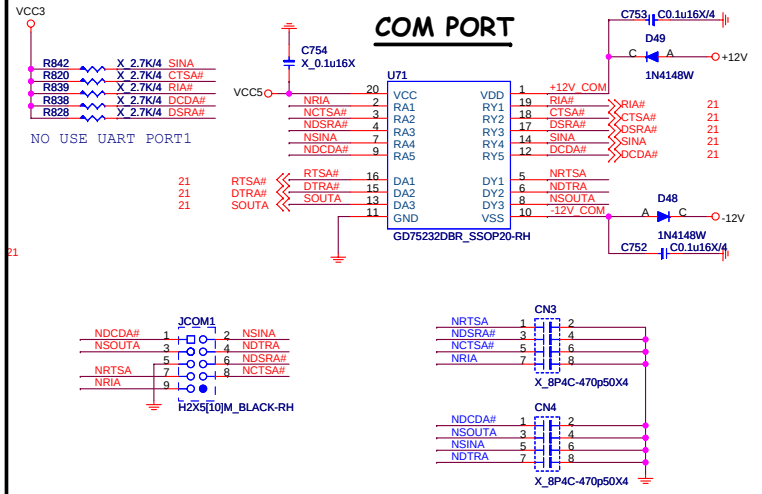
CPU RST



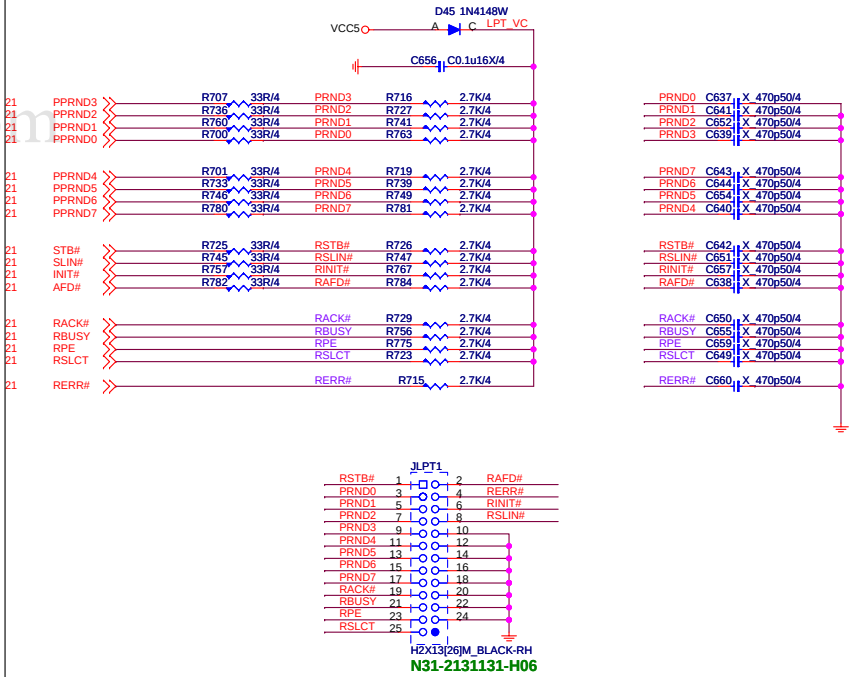
PROM RESET



COM PORT



PARALLAL PORT



N31-2131131-H06

MICRO-START INT'L CO.,LTD.

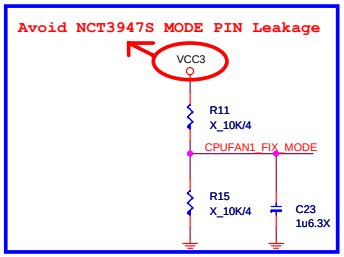
Title	SIO NCT6793D	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 22 of 55	

MSI Link to the Future MICRO-START INT'L CO.,LTD.

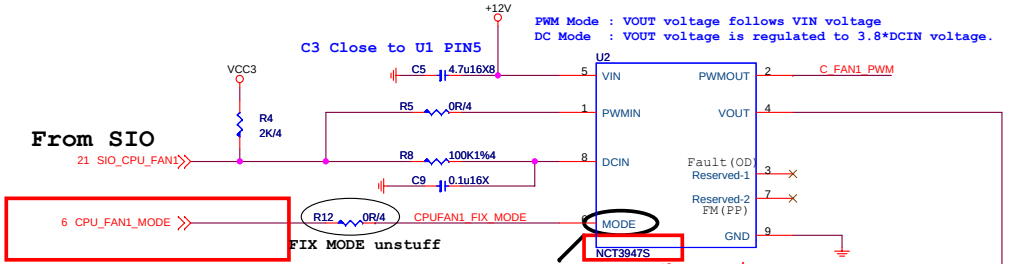
Title: Manual parts		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Tuesday, January 03, 2017	Sheet 23 of 55	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO　　パBIOSち传 PWM/DC MODE



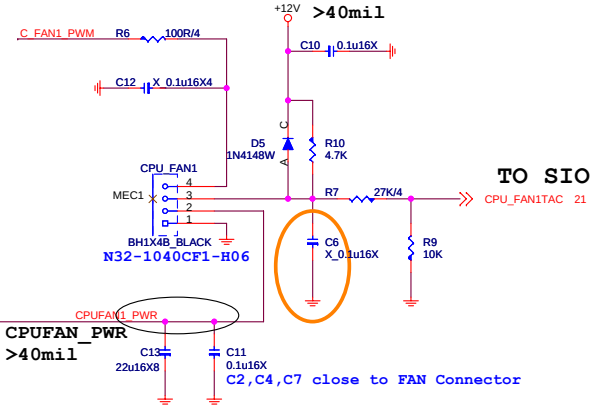
Resever For FIX DC or PWM MODE USE By PM SPEC

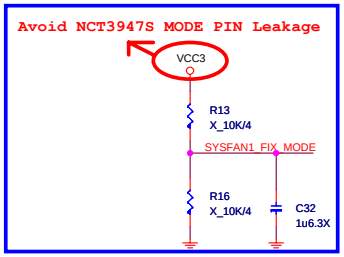


GPIO Control

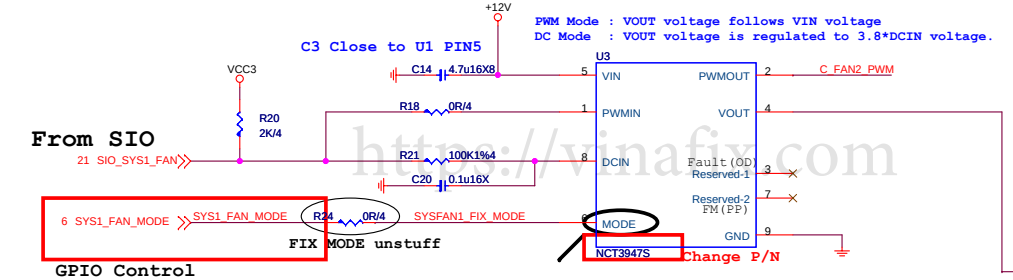
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





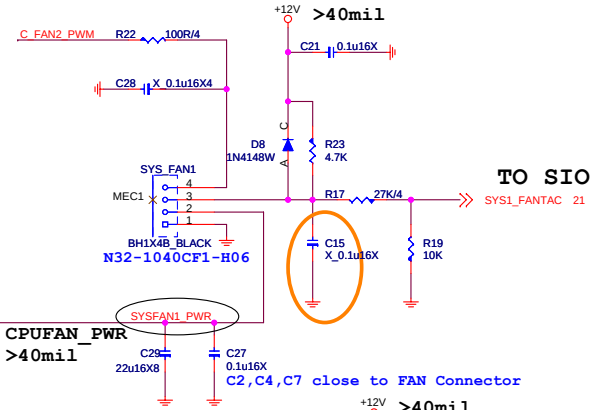
Resever For FIX DC or PWM MODE USE By PM SPEC

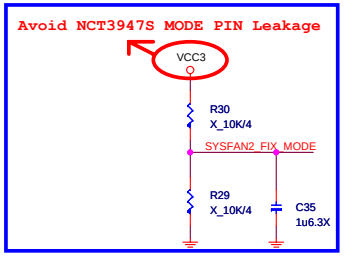


GPIO Control

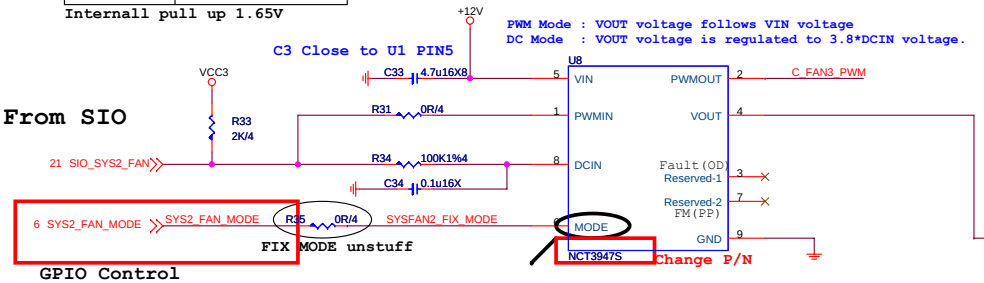
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V





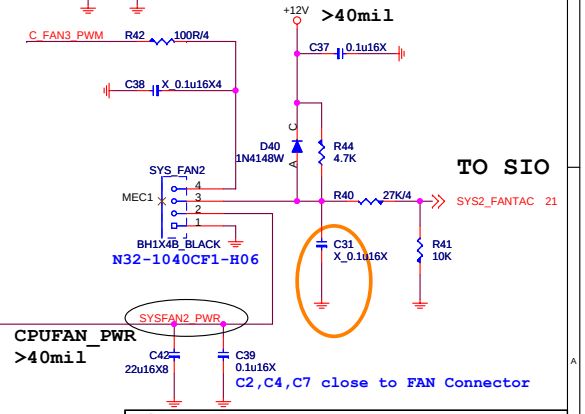
Resever For FIX DC or PWM MODE USE By PM SPEC



GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



MICRO-START INTL CO.,LTD.

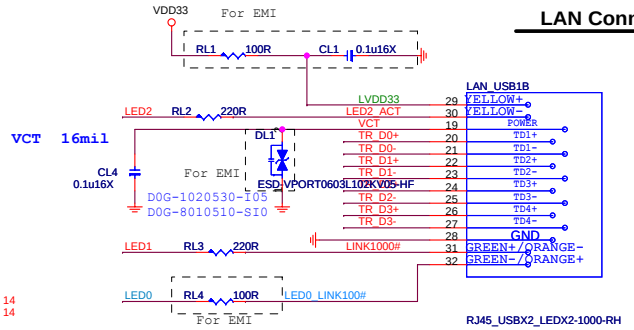
Title: CPU FAN Control

Size: Custom | Document Number: MS-7A39 | teknisi indonesia | Rev: 1.0

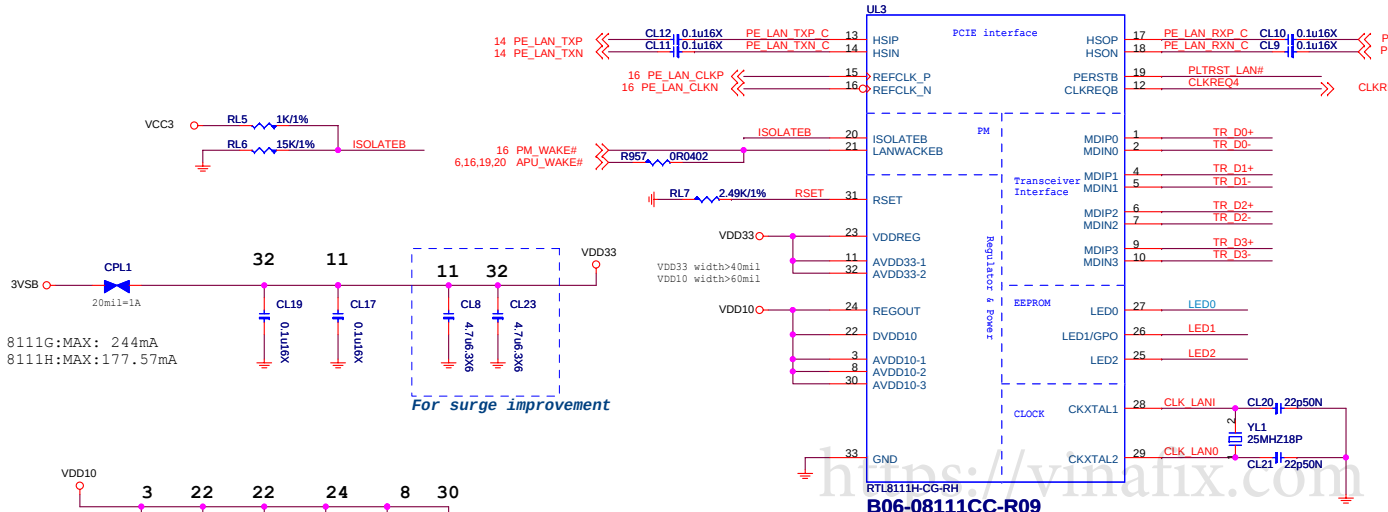
Date: Friday, January 20, 2017 | Sheet 24 of 55

RTL8111G/RTL8111H Giga LAN

LAN Connector

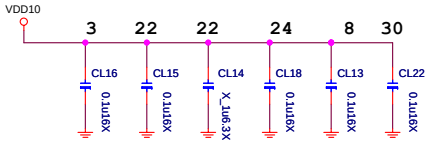


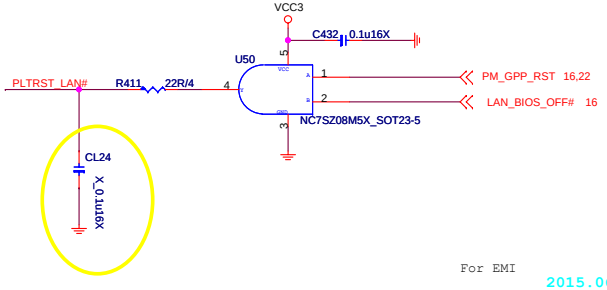
8111H:B06-08111CC-R09
8111G:B06-081116C-R09

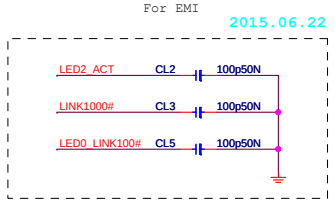


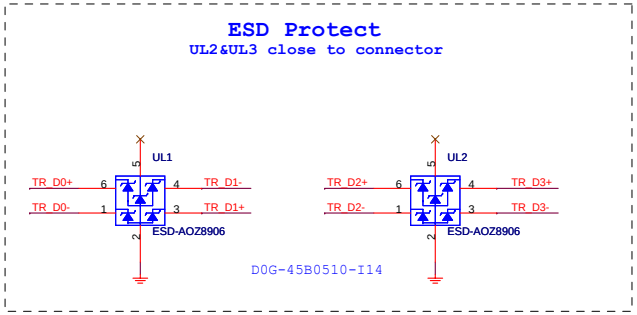
B06-08111CC-R09

Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.









8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

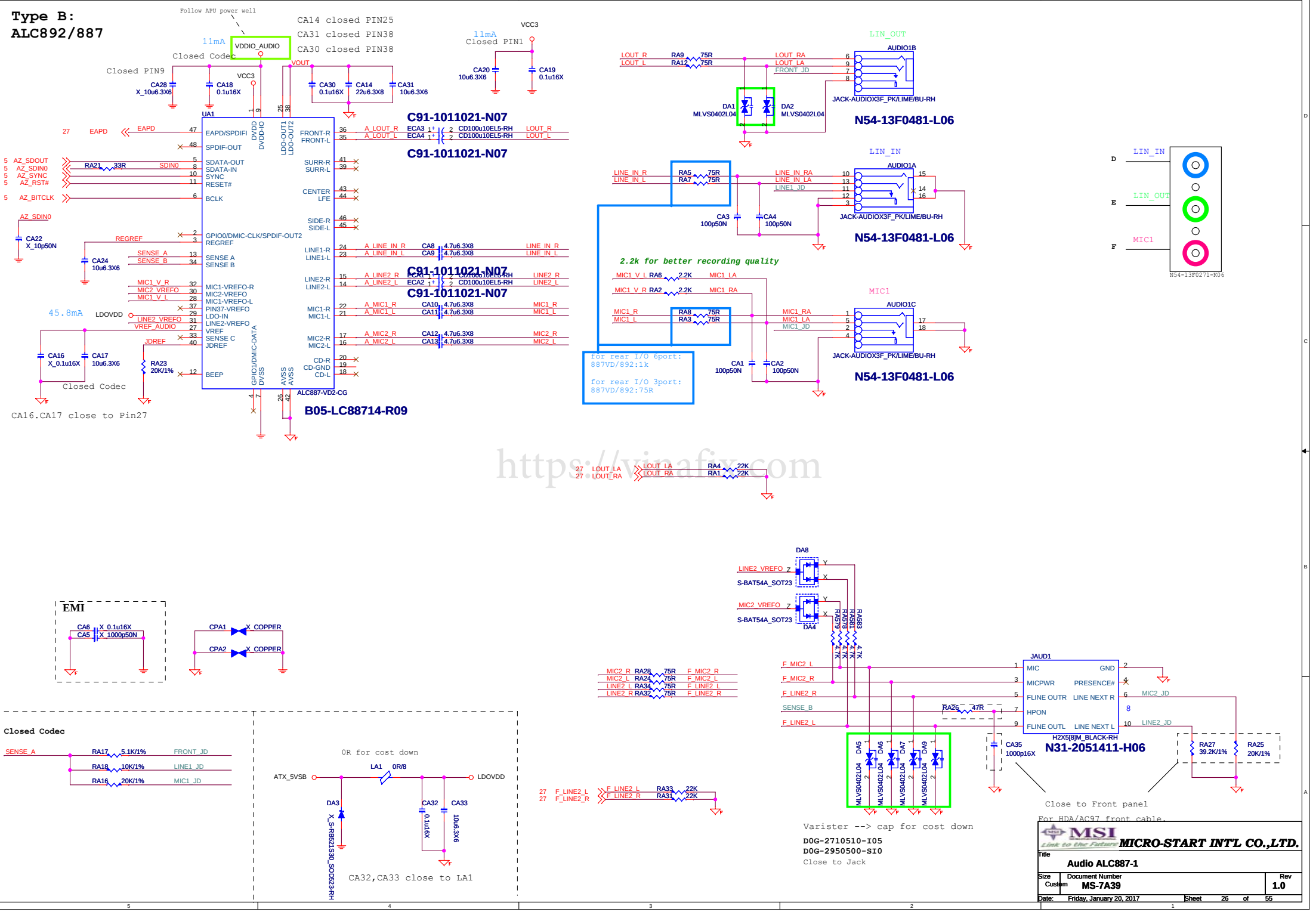
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: LAN-RTL8111H		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 25 of 55	

Type B:
ALC892/887

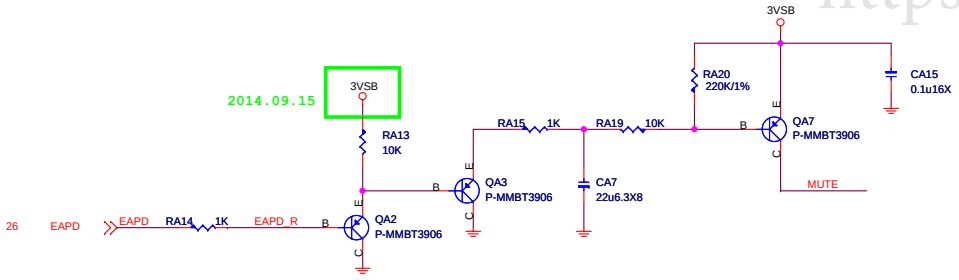


MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	Audio ALC887-1	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 26 of 55	

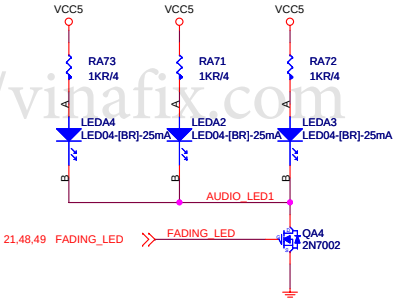
Rear Line OUT De-POP circuit

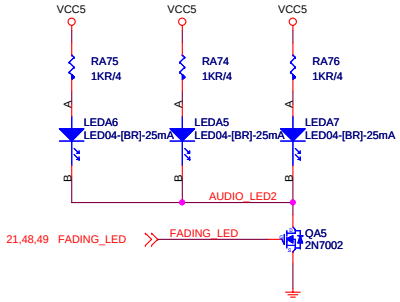
De-pop circuit for Rear Line out & Front Headphone out)

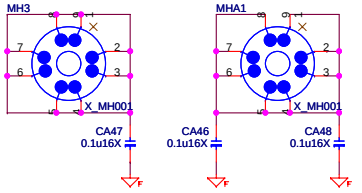


Digital

Analog







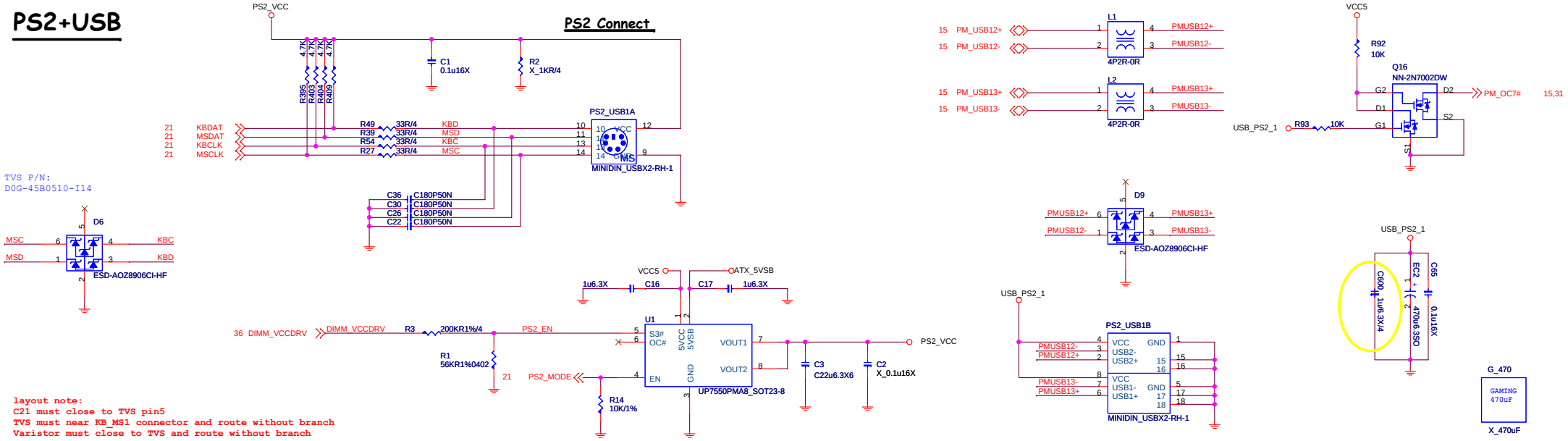
MICRO-START INT'L CO.,LTD.

Title: Audio ALC887-2

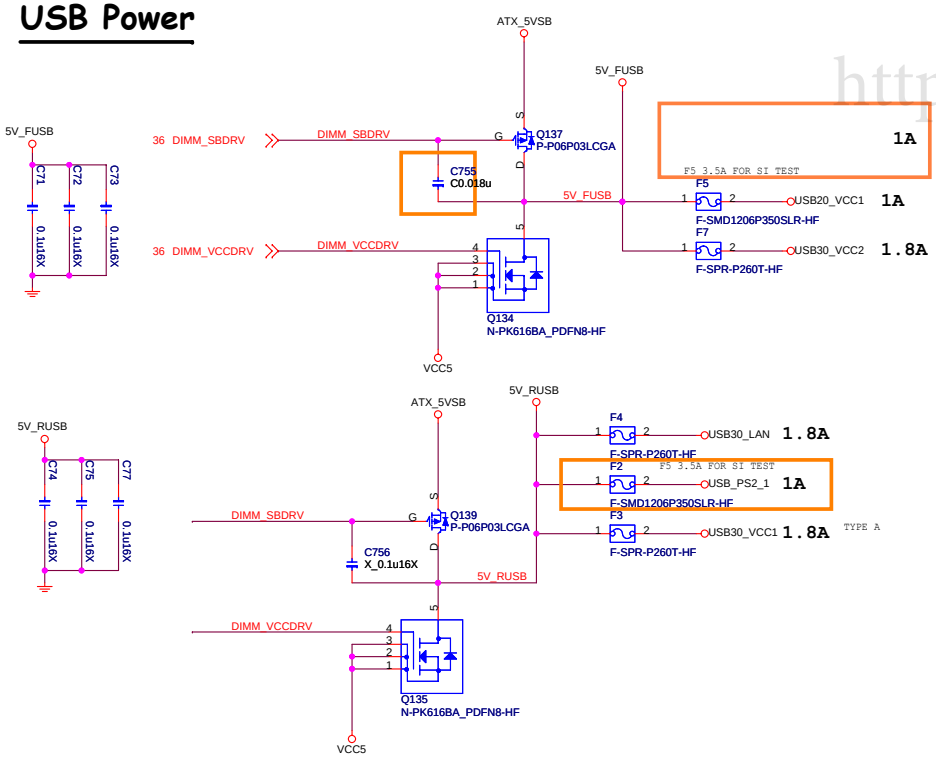
Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 27 of 55

PS2+USB



USB Power



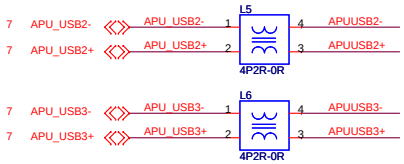
Vinafix.com

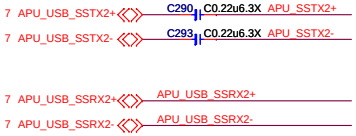
MSI MICRO-START INT'L CO.,LTD.

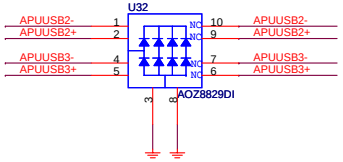
Title: USB Rear PS2+USB2.0		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 28 of 55	

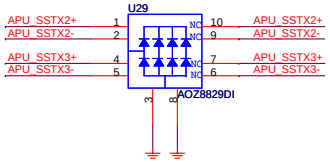
USB3.1 GEN1

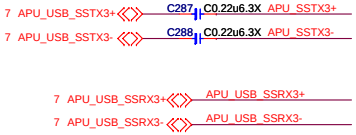
VR Sloution U2 redriver

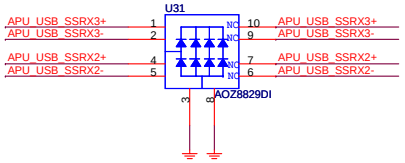




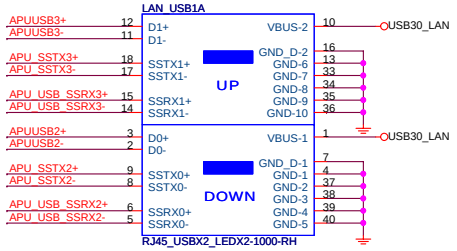


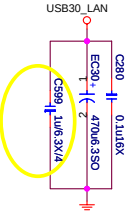






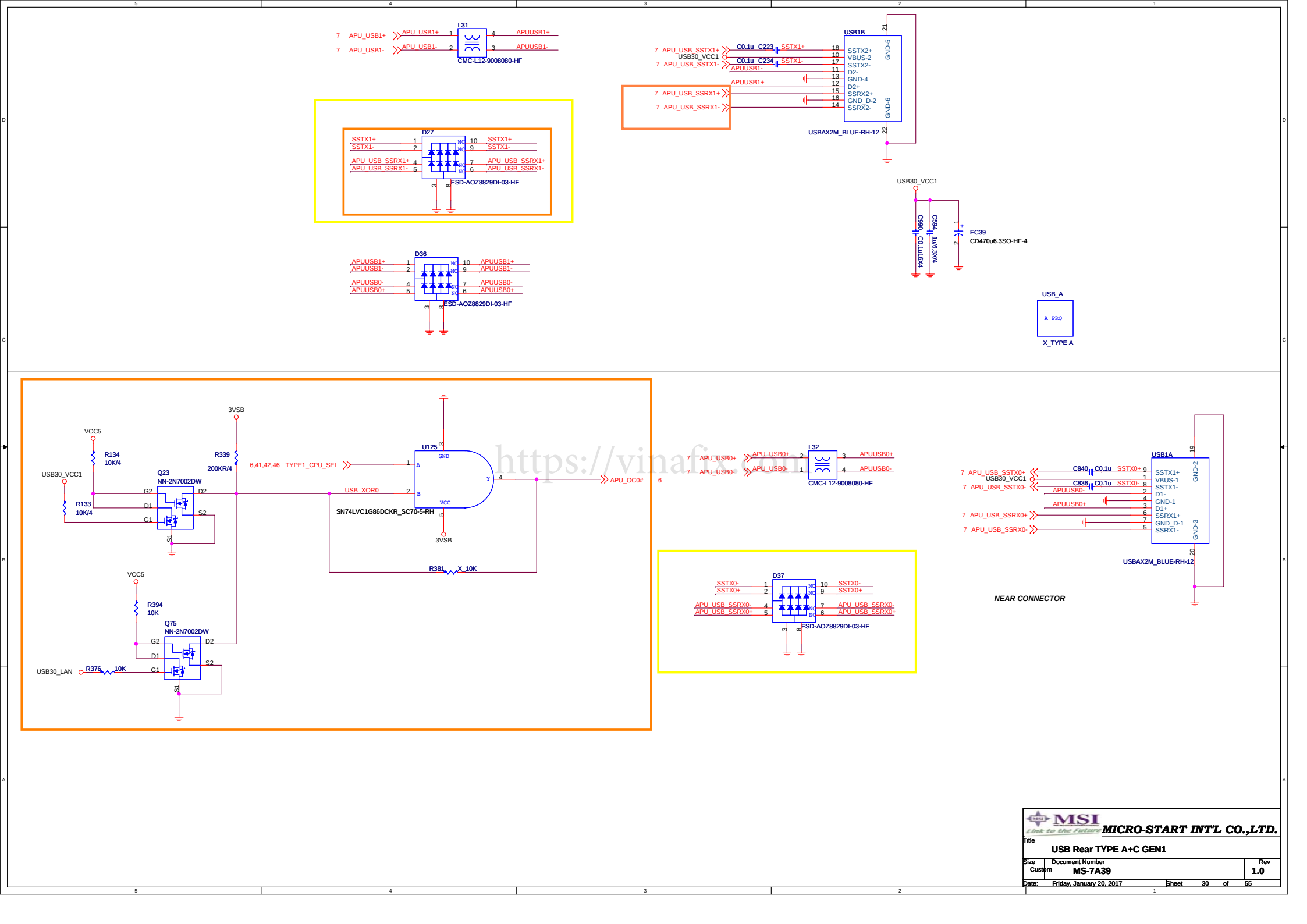
LAN+USB





MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: USB Rear LAN+USB3.1 GEN1		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 29 of 55	



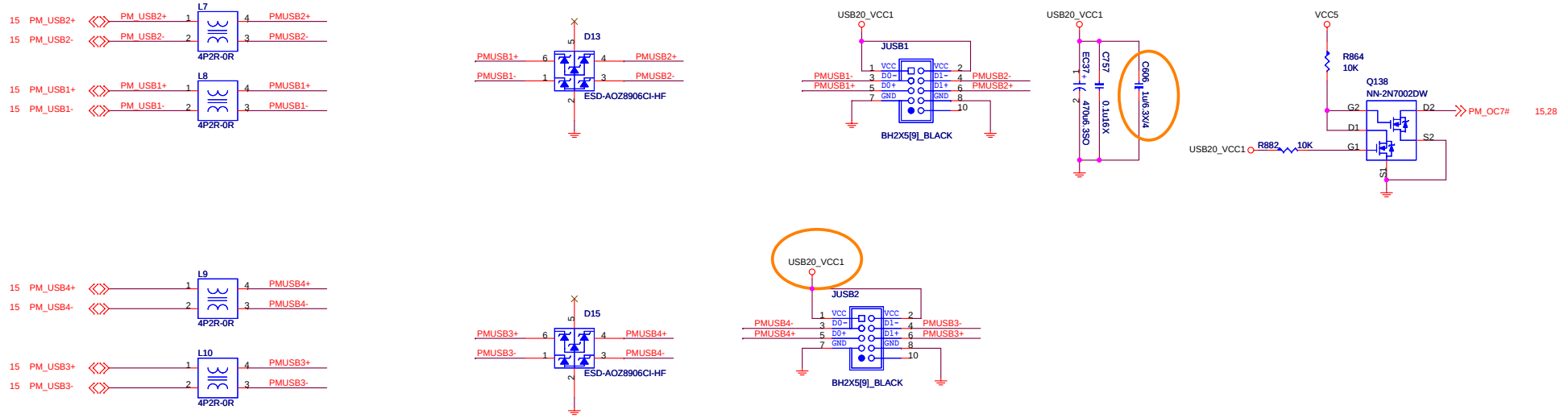
MICRO-START INT'L CO.,LTD.

Title: USB Rear TYPE A+C GEN1

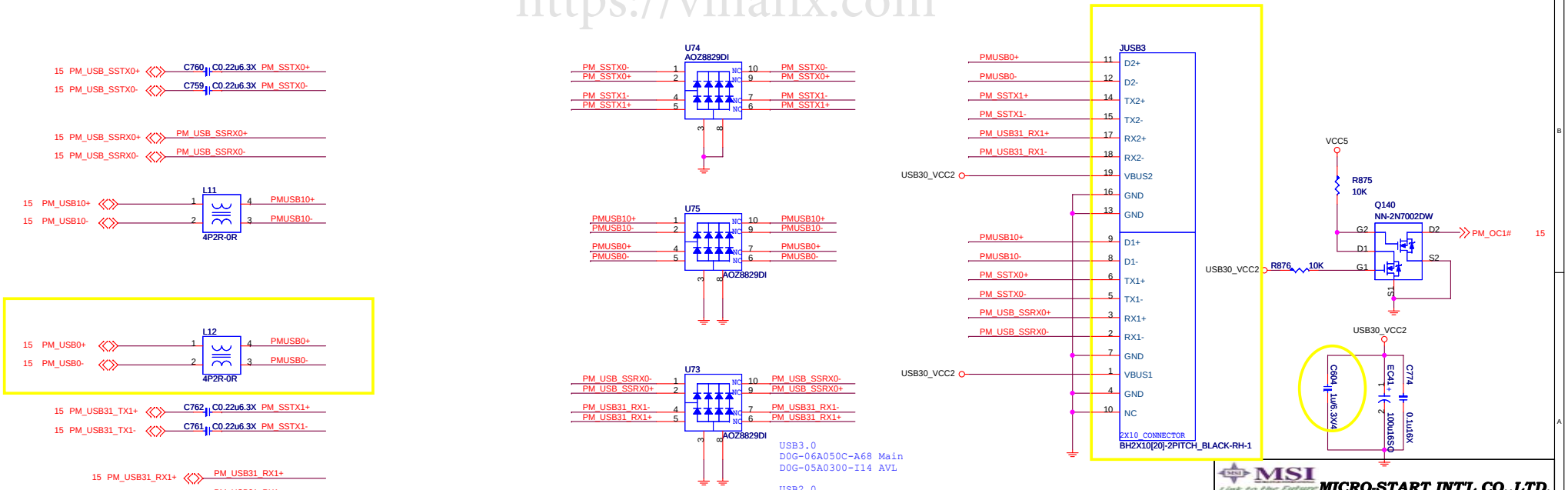
Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 30 of 55

Front USB2.0



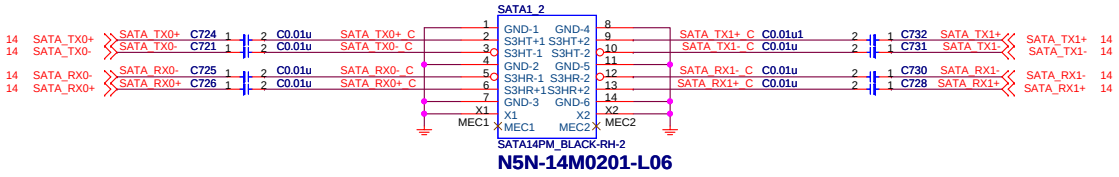
Front USB3.1 GEN1

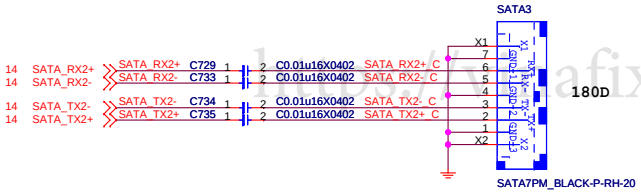


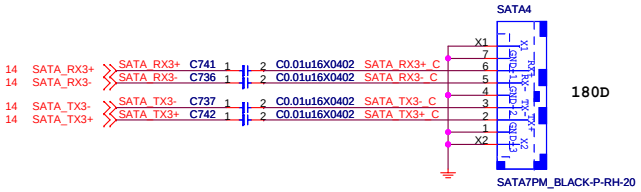
MSI MICRO-START INTL CO.,LTD.

Title: USB Front Side		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 31 of 55	

SATA Connector





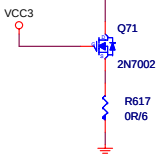


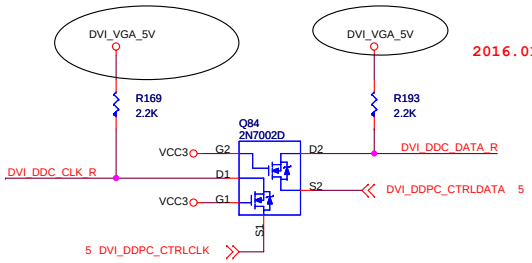
MSI MICRO-START INT'L CO.,LTD.

Title: SATA Connector		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 32 of 55	

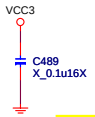
DVI level shifter

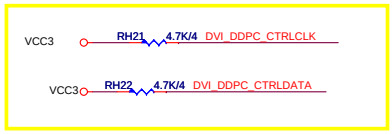
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

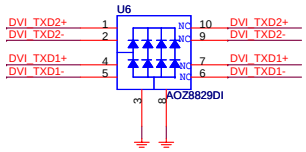


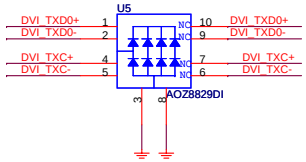


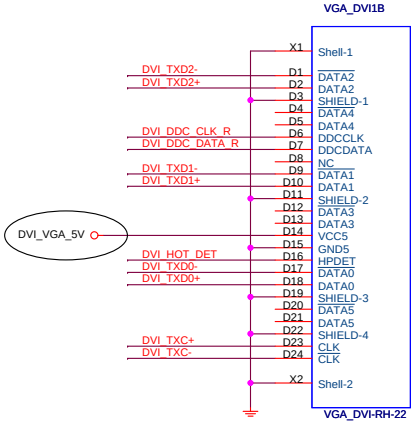
2016.01.11 Dual MOS change to single MOS,reduce CM noise by EMI Suggestion

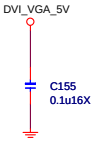


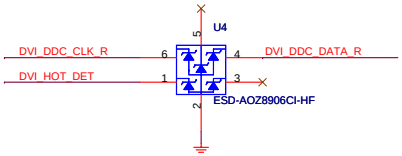


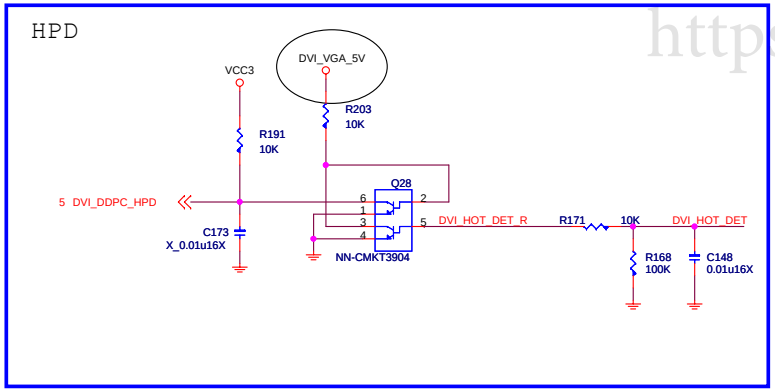


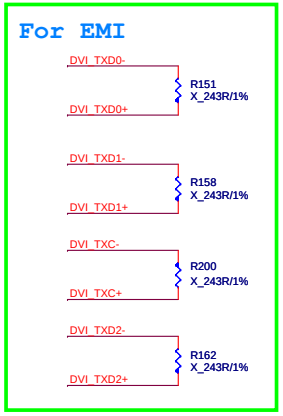


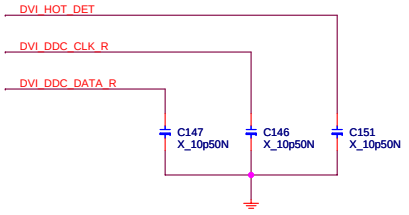










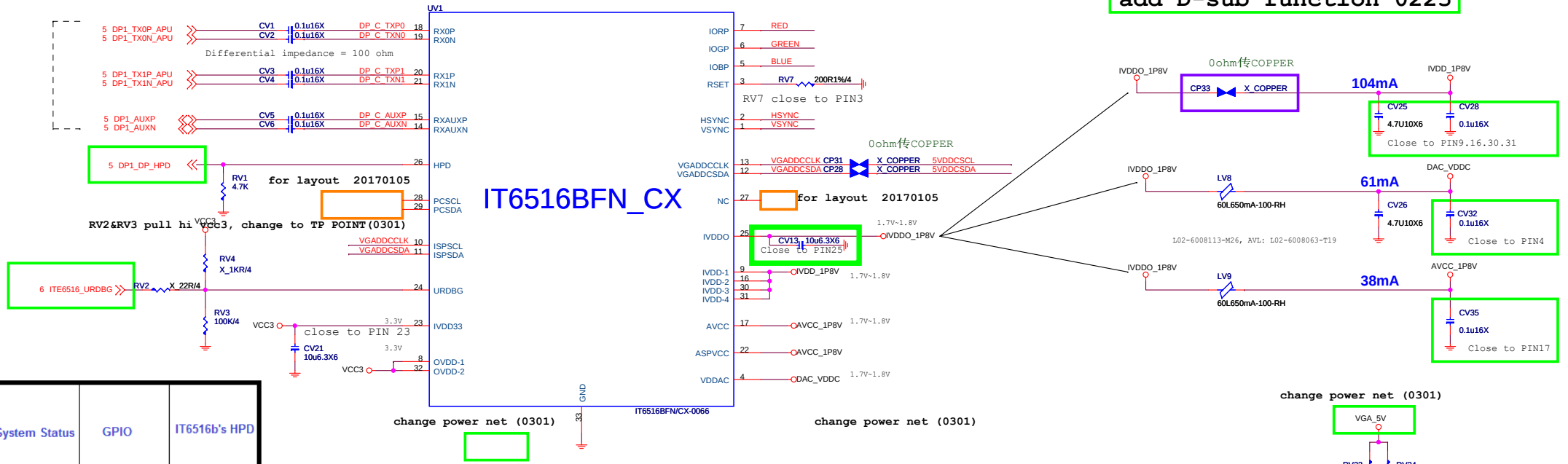


MICRO-START INT'L CO.,LTD.

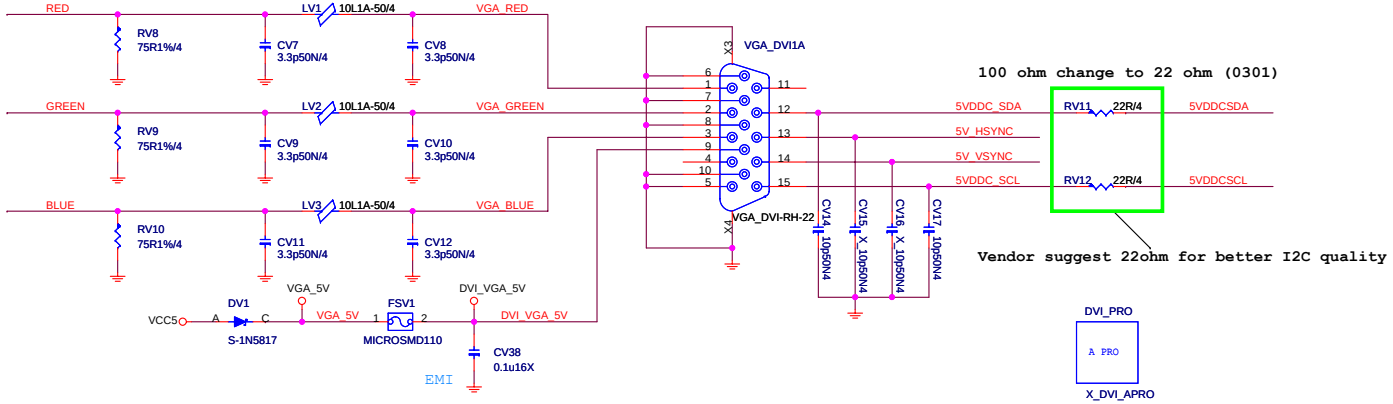
Title: DVI Connector		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 33 of 55	

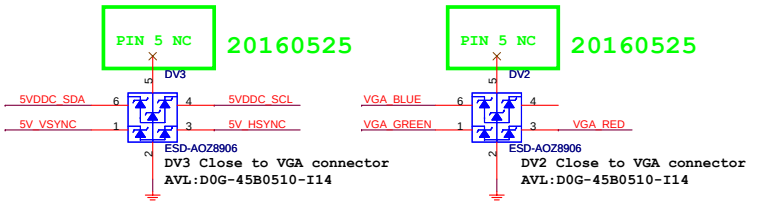
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS MOde	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug





MSI MICRO-START INTL CO.,LTD.

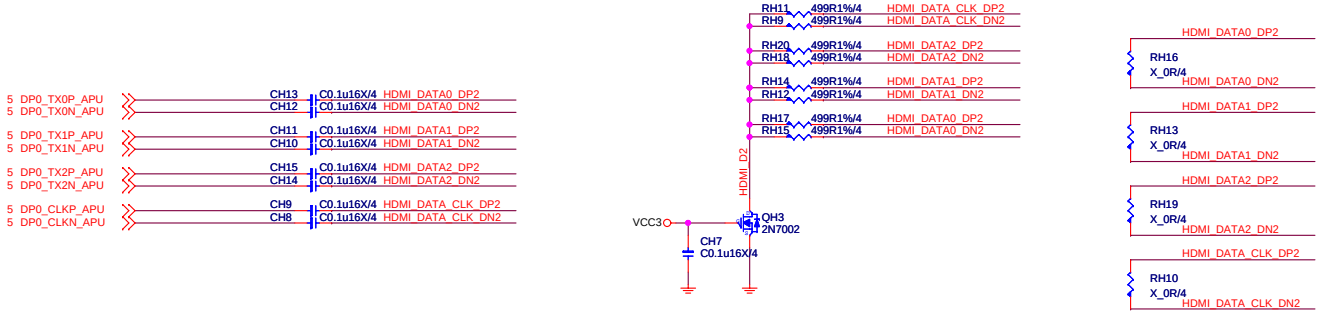
Title: DP to VGA ITE6516

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

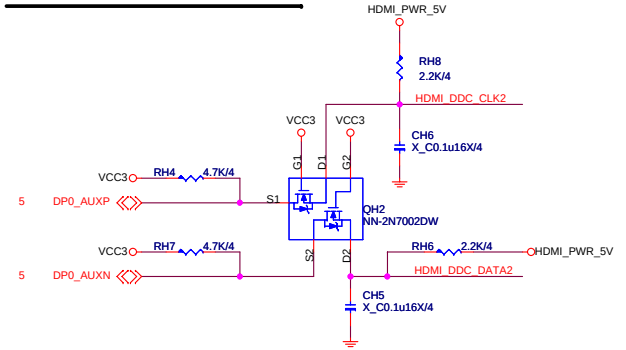
Date: Friday, January 20, 2017 | Sheet 34 of 55

HDMI CONNECTOR

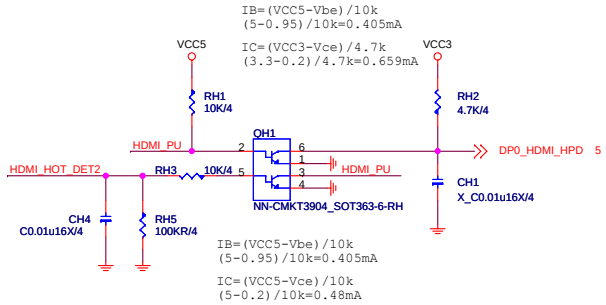
For HDMI 1.4



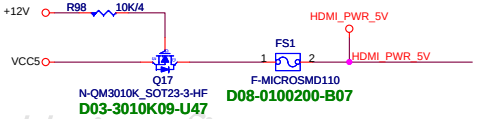
AUX Level Shifter



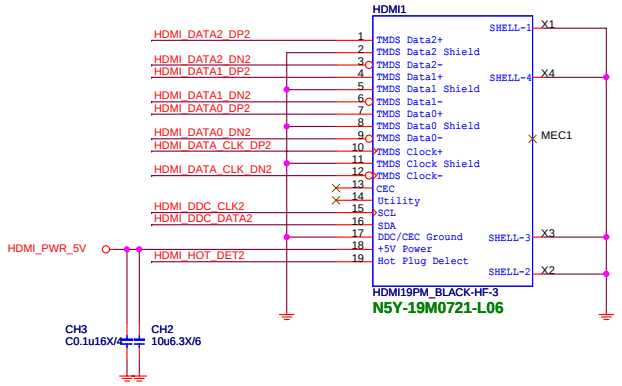
HPD Circuit



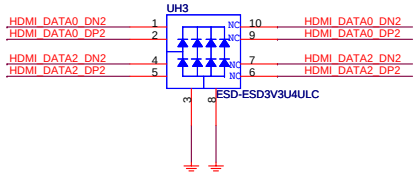
Connector Power

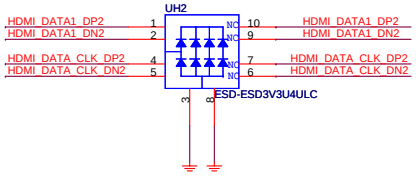


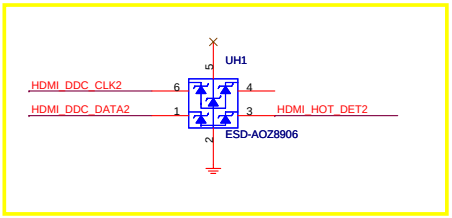
Connector



For EMI







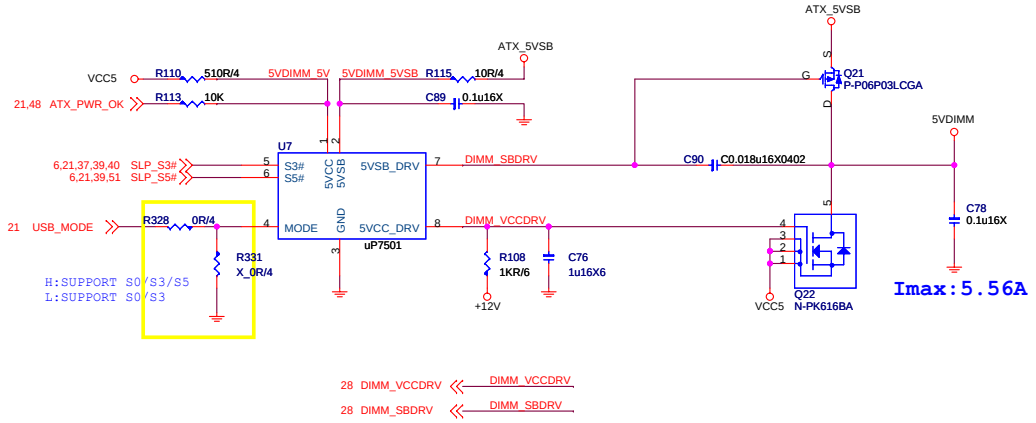
MSI MICRO-START INT'L CO.,LTD.

Title: HDMI 1.4

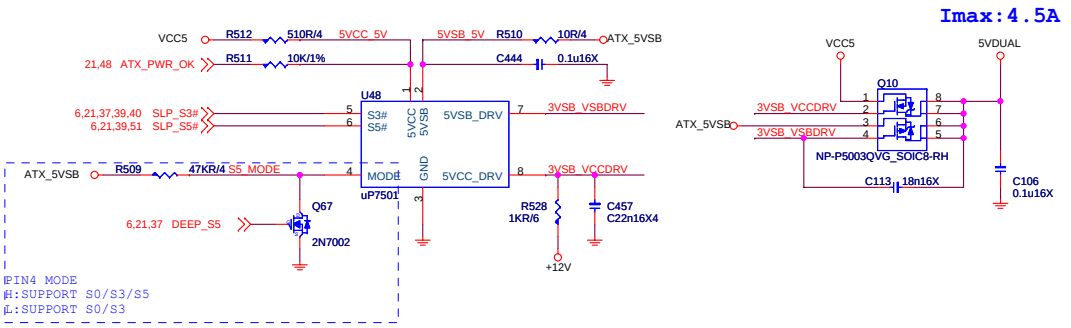
Size: Custom | Document Number: MS-7A39 | Rev: 1.0

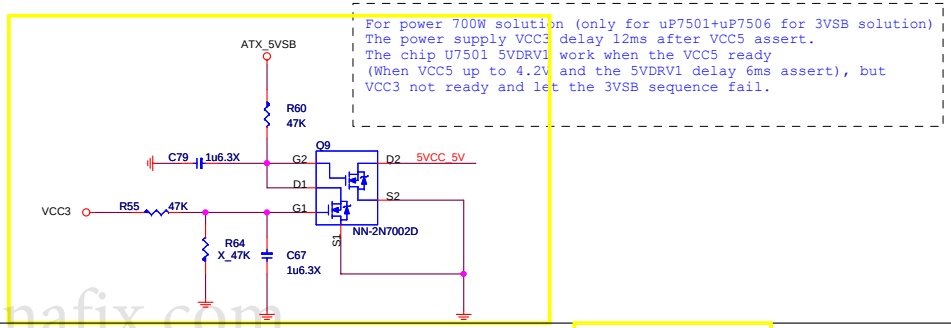
Date: Friday, January 20, 2017 | Sheet 35 of 55

5VDIMM FOR DDR

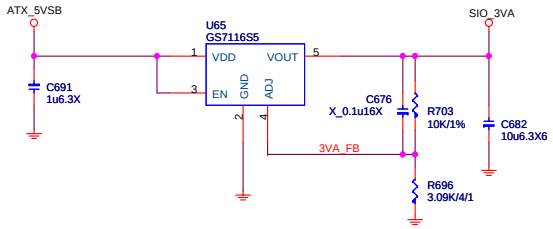


5VDUAL For 3VSB CPU 1.8V VDDP

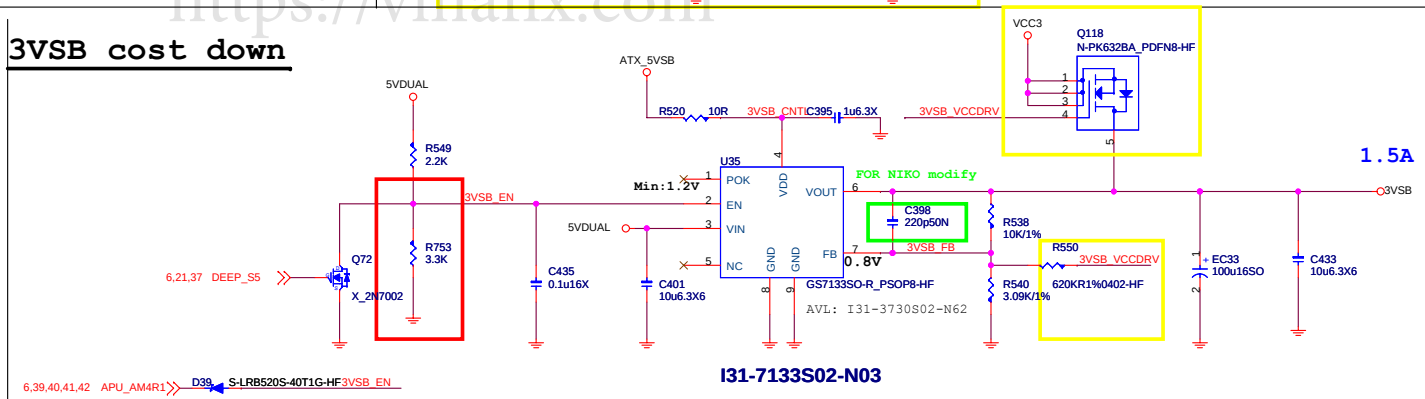




SIO_3VA



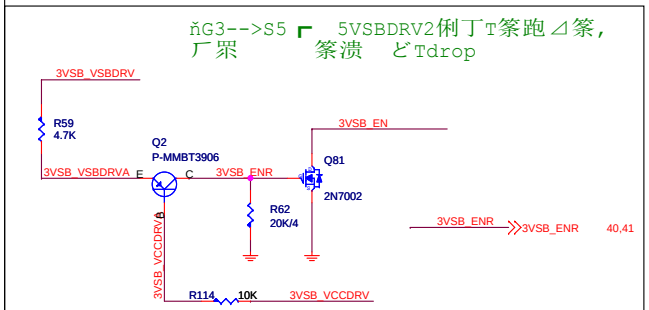
3VSB cost down



3VSB cost down

3.3V@1.4959A

1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
*PCIE*3 @1.125A*
USB TYPE-C @0.9mA



MSI MICRO-START INT'L CO.,LTD.

Title: ACPI uPI-5VDIMM&3VSB		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 36 of 55	

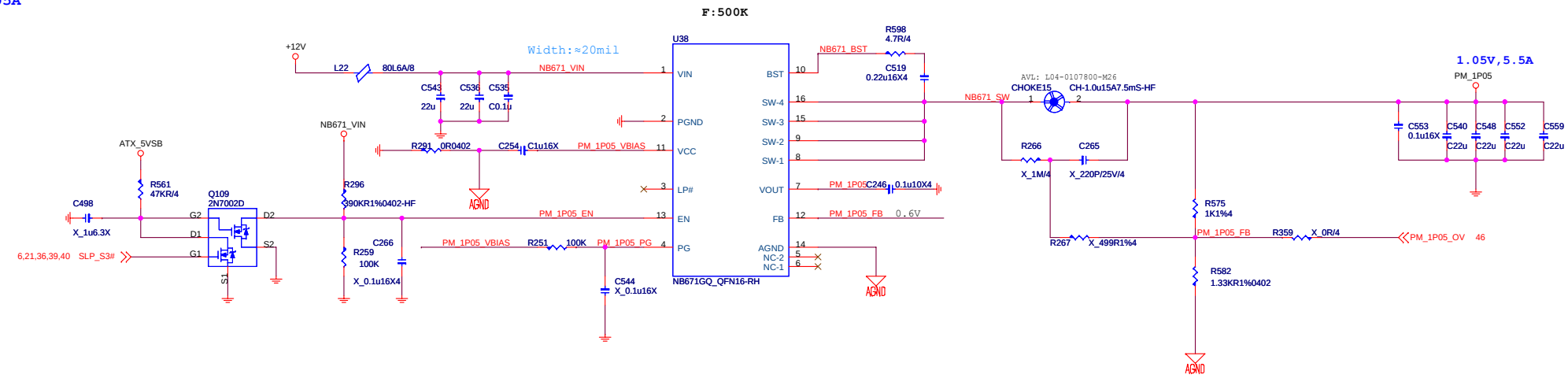
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A

support OV=>NB685
not support OV=> NB681

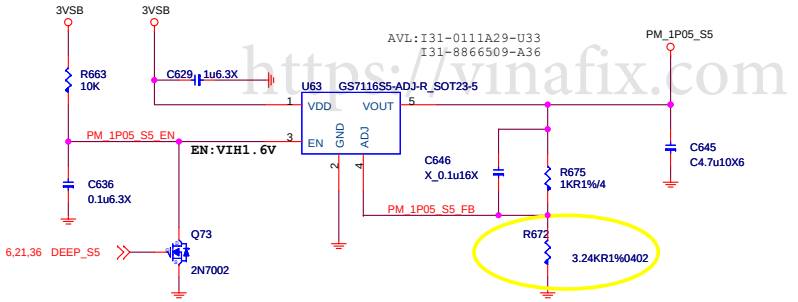
IMAX 10A
ILIMIT=10A~12A
*IOC=ILIMIT+40%*IMAX/2=12A~14A.*

0.7776uH≦L≦1.1664uH



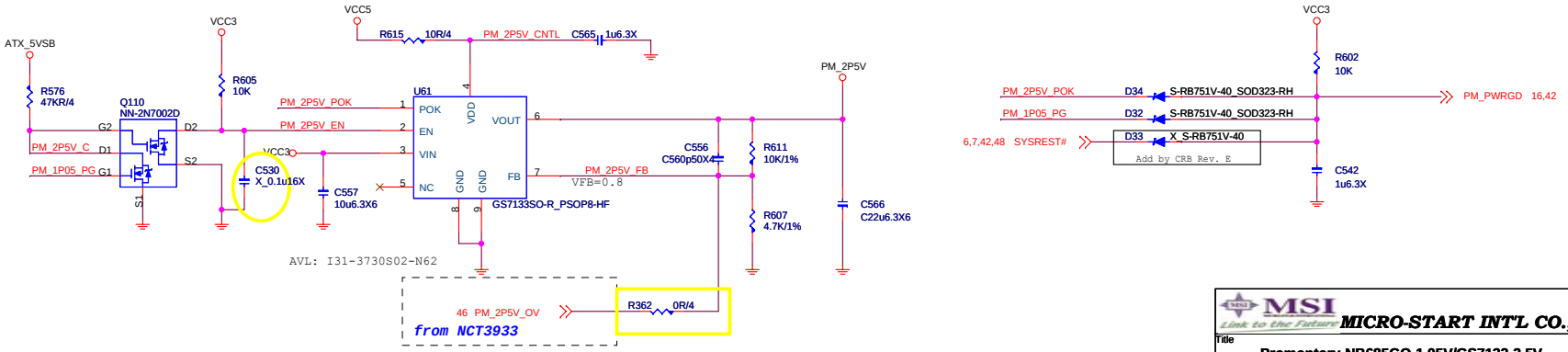
FOR Promontory 1.05V_S5

0.05A



Promontory-2.5V

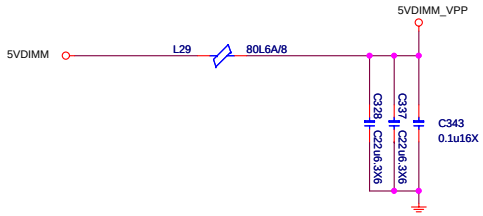
2.5V; 900mA

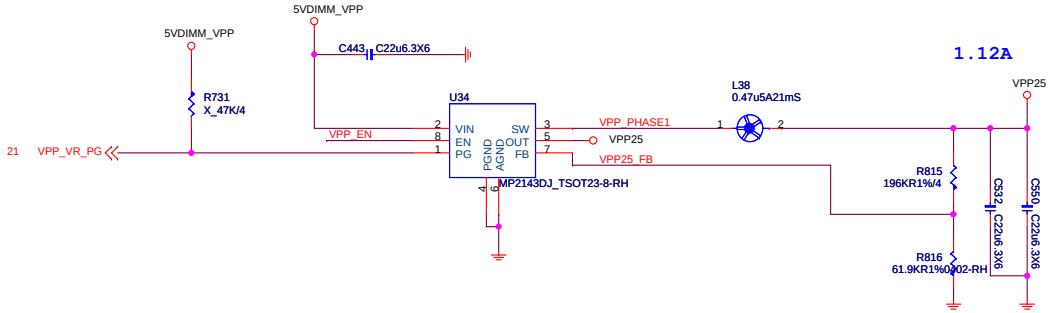


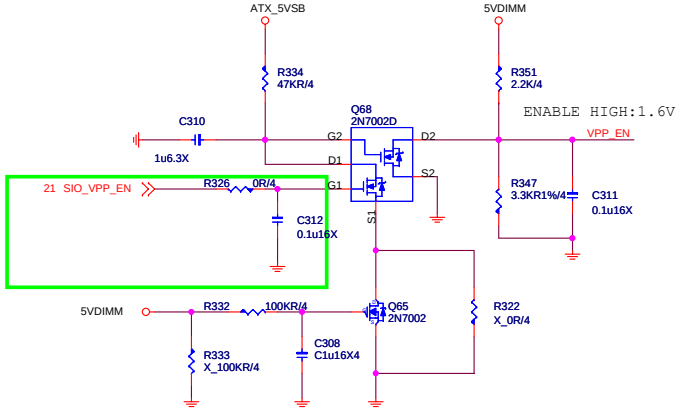
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Promontory-NB685GQ-1.05V/GS7133-2.5V		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 37 of 55	

2DIMM :1.12A FOR DDR VPP2.5V







MICRO-START INT'L CO.,LTD.

Title: DDR PWR VPP25/VTT-MP2143		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 38 of 55	

DDR4_1.2V 15.5A+4.75A+0.6A=20.85A

15.5A FOR CPU

4.75A FOR 2DIMM

0.3*2=0.6A FOR DDR VTT

OCP =7.925A*1.5=11.8875A

Current limit= 110K(R178)*5uA/10/4mohm)=33A

Irms = Iout * SQRT{D/N- (D)^2]}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A

VID	Reference Voltage (V)
H	0.675
L	0.75

OCP:27.5A

Imax: 20.85A

By layout modify

f:400KHz

27.5A

FB:0.75V

I32-8231A0C-R11

MAX:20.85A

1.2V

0.1uFx1 per dimm

Close to PIN19

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K

MICRO-START INT'L CO.,LTD.

Title: DDR Power-RT8231AGQW

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 39 of 55

FOR CPU 1.8V S5

0.5A

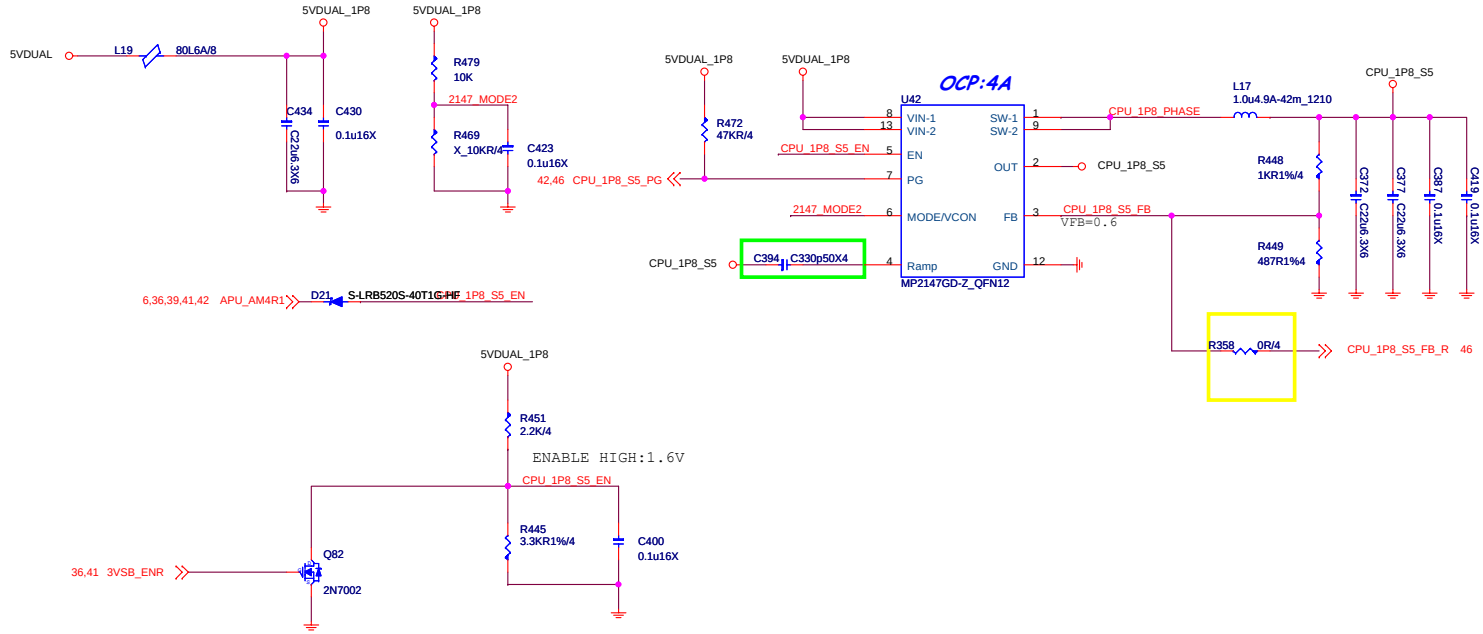
FOR VCCP_SOC_S5

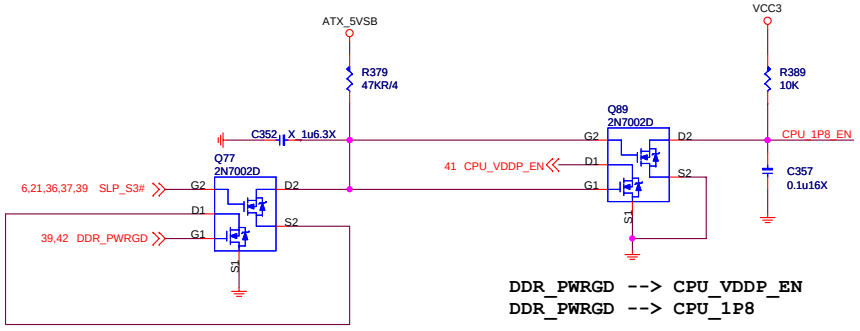
0.9A

FOR CPU 1.8V S0

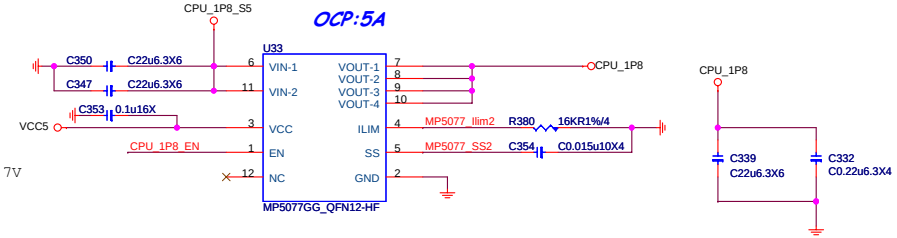
2.0A

0.5A + 2.0A + 0.9A =3.4A





DDR_PWRGD --> CPU_VDDP_EN
DDR_PWRGD --> CPU_1P8



ENABLE HIGH:1.7V

Ilimit=(1/Rlimit)*S,S=80000,when VIN=1.8V
=(1/16)*80000=5.0375A

Tss=(1/3)*((Vout*Css)/Iss),Iss=9uA
Tss=(1/3)*((1.8*15n)/9uA)=1mS

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: CPU Power 1P8V-MP2147		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 40 of 55	

CPU_VDDP_S0

1.05V/0.9
S0:8.5A
OCP=12A

by layout

+12V
R406 100K1%4
EN:VIH1.6V
CPU_VDDP_EN
R418 33K/1%
C389 0.1u16X

VCC5
R437 10K
42 CPU_VDDP_PG

EN:VIH1.6V
EN pin Maximum:6.5V

by layout
+12V
R494 10R/8
U6_VCC
C429 C1u16X6

6,36,39,40,42 APU_AM4R1
D20 S-LRB520S-40T1G-HF
VDDP_EN

U41
EN
PGOOD
REFOUT
REFIN
VCC
GND
BOOT
PHASE
UGATE
LGATE/OCSET
FB
RT8125EGQW_WDFN10-HF

CPU_VDDP_BOOT1
R484 0R/6
C440 0.1u16X25
CPU_VDDP_PH1
CPU_VDDP_UG1
CPU_VDDP_LG1
CPU_VDDP_FB
FB:0.8V

CPU_VDDP_REFOUT
C426 C1000p50X4
R453 768R1%4
CPU_VDDP_REFIN
0.8V
0.684V
C374 C1000p50X4
R463 4.53KR1%4

CPU_VDDP
R420 10R1%4
R438 1KR1%/4
CPU_VDDP_SENSE_R
R421 0R/4
CPU_VDDP_SENSE 6
C399 X_0.1u16X
R450 3.16K/1%

AM4_CPU_SEL
0:Type 0/1 1.05V
1:Type 2/3 0.9V

Q86
NN-2N7002DW
6,30,42,46 TYPE1_CPU_SEL
16 PM_GPIO_R9
46 CPU_VDDP_OV
CP25 X_COPPER

PM_GPIO_R9
1:Type 0/1 1.05V
0:Type 2/3 0.9V

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.1* 0.8 * 0.282566
= 3.46A

TYPE0_CPU_SEL:
1:TYPE 0
0:TYPE 2

CPU_VDDP_EN:
0:TYPE 2
1:TYPE 0

Q92
NN-2N7002DW
6,42 TYPE0_CPU_SEL
VDDP_SEL
6,30,42,46 TYPE1_CPU_SEL
CPU_VDDP_EN
CPU_VDDP_EN 40

TYPE1_CPU_SEL:
0:TYPE 0
1:TYPE 2

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

12VCC_IN
CHOKE14
CH-0.47u5A21mS-HF
+12V
C461 C1u16X6
C460 22u16X8
EC11 270u16SO
C446 0.1u16X

CPU_VDDP_UG1
R508 0R/6
CPU_VDDP_UG1_R
R500 X_10KR/4
N-PK616BA_PDFN8-HF
Q97

CPU_VDDP_PH1
CHOKE13
1.0u15A7.5mS-HF
CPU_VDDP
OCP=12A
1.05V,8.5A

CPU_VDDP_LG1
R482 X_2.2R/8
snubber
C437 X_C3300p50X4
C334 1u6.3X
C425 C22u6.3X6
EC31 560u6.3SO
EC32 560u6.3SO
N-PK632BA_PDFN8-HF
Q96

OCPSET:min 5Kohm
OCP
=(R475*10uA)/DCR
=(5.1k*10uA)/3.3m
=15.45A
R475 5.1K/1%/4

CPU_VDDP_S5

VDDP_S5 1.05V/0.9
S5:1A

5VDUAL
3VSB
3VSB
L20 80L6A/8
R501 X_10KR/4
R502 10K
C439 C22u6.3X6
U45
VDDP_VSB_VIN
VDDP_VSB_EN
VDDP_VSB_PG
VIN
EN
PG
PGND
AGND
SW
OUT
FB
MP2143DJ
VDDP_VSB_PHASE
L18 1.0u6.3A_1210-HF
CPU_VDDP_S5
42 VDDP_VSB_PG
Internal Pull-Up 500K
R489 1KR1%/4
R488 2KR1%/4
C412 C22u6.3X6
C421 C22u6.3X6
C427 C0.22u6.3X4
VDDP_VSB_FB

6,36,39,40,42 APU_AM4R1
D28 S-LRB520S-40T1G-HF
VDDP_VSB_EN
C390 X_0.1u16X
36,40 3VSB_ENR
Q98
2N7002

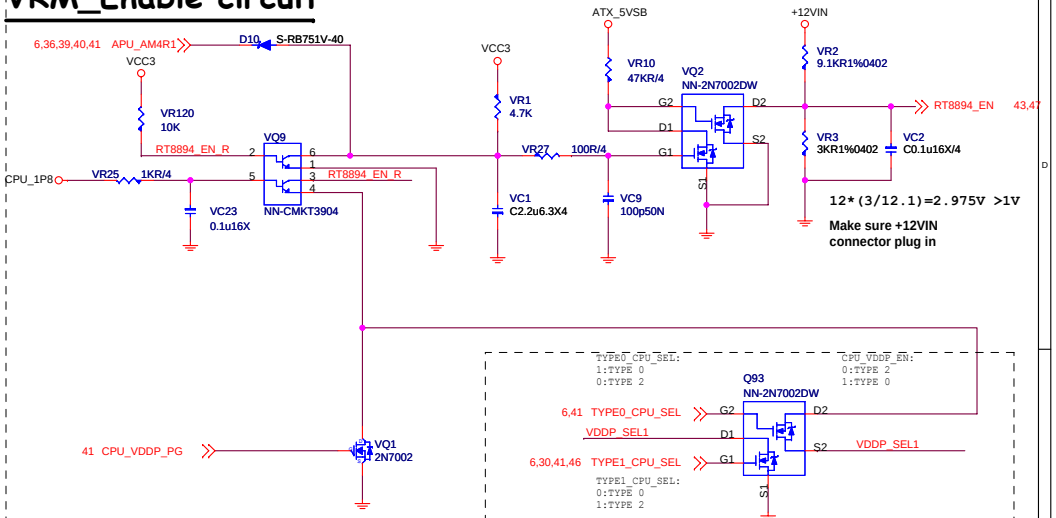
ATX_5VSB
R490 47KR/4
Q95
NN-2N7002DW
C436 0.1u16X
R464 3.83KR1%4
6,30,42,46 TYPE1_CPU_SEL
AM4_CPU_SEL
0:Type 0/1
1:Type 2/3

R488///R464=1.3139K, Vout=1.056V
R488=8.06K, Vout=0.9V

MSI
MICRO-START INTL CO.,LTD.

Title: CPU Power VDDP-RT8125E
Size: Custom
Document Number: MS-7A39
Rev: 1.0
Date: Friday, January 20, 2017
Sheet 41 of 55

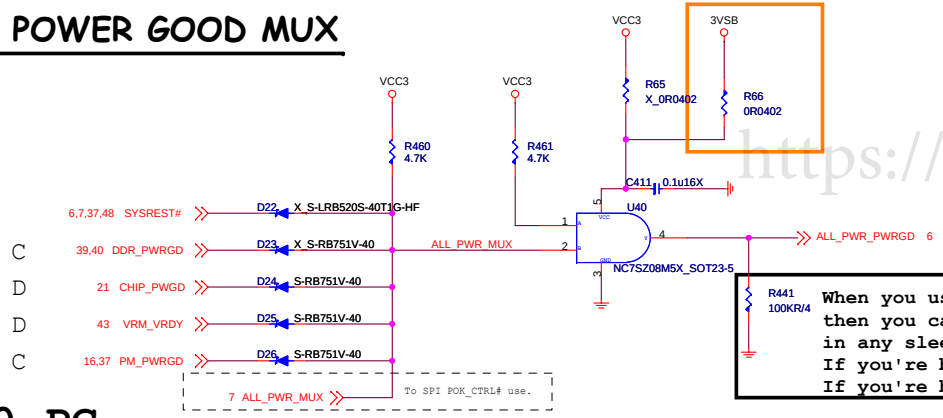
VRM_Enable circuit



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

ALL POWER GOOD MUX

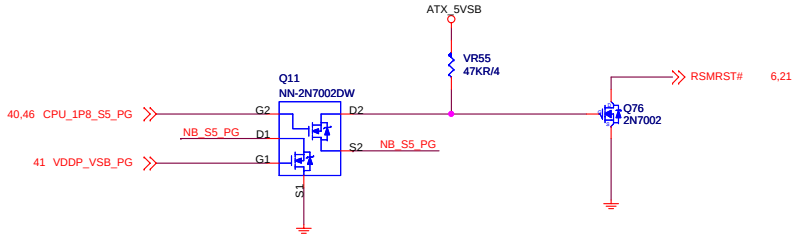


R441 100KR/4

When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

S0 PG

S5 PG



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

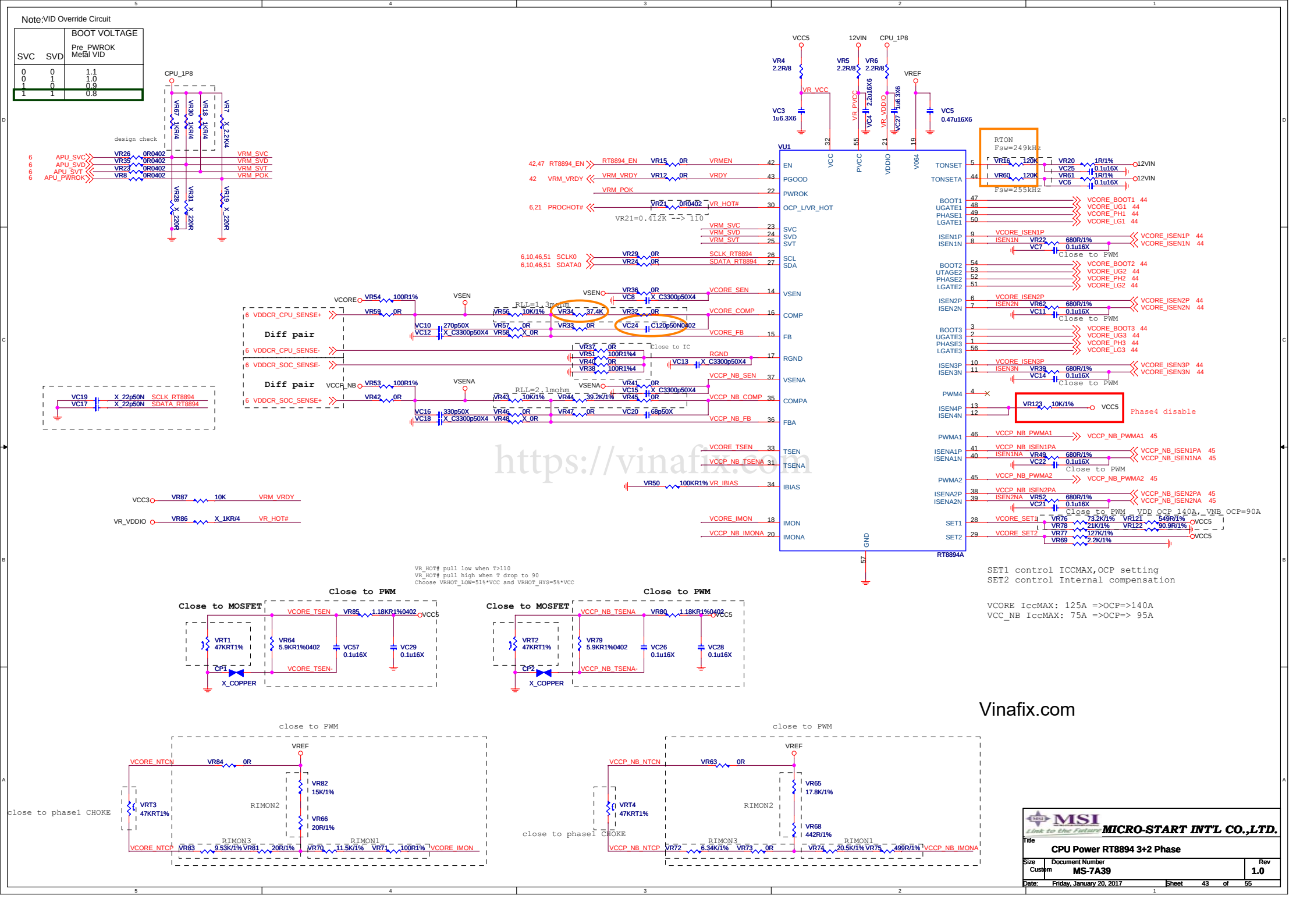
Title: CPU PWR-IR3599

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 42 of 55

Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



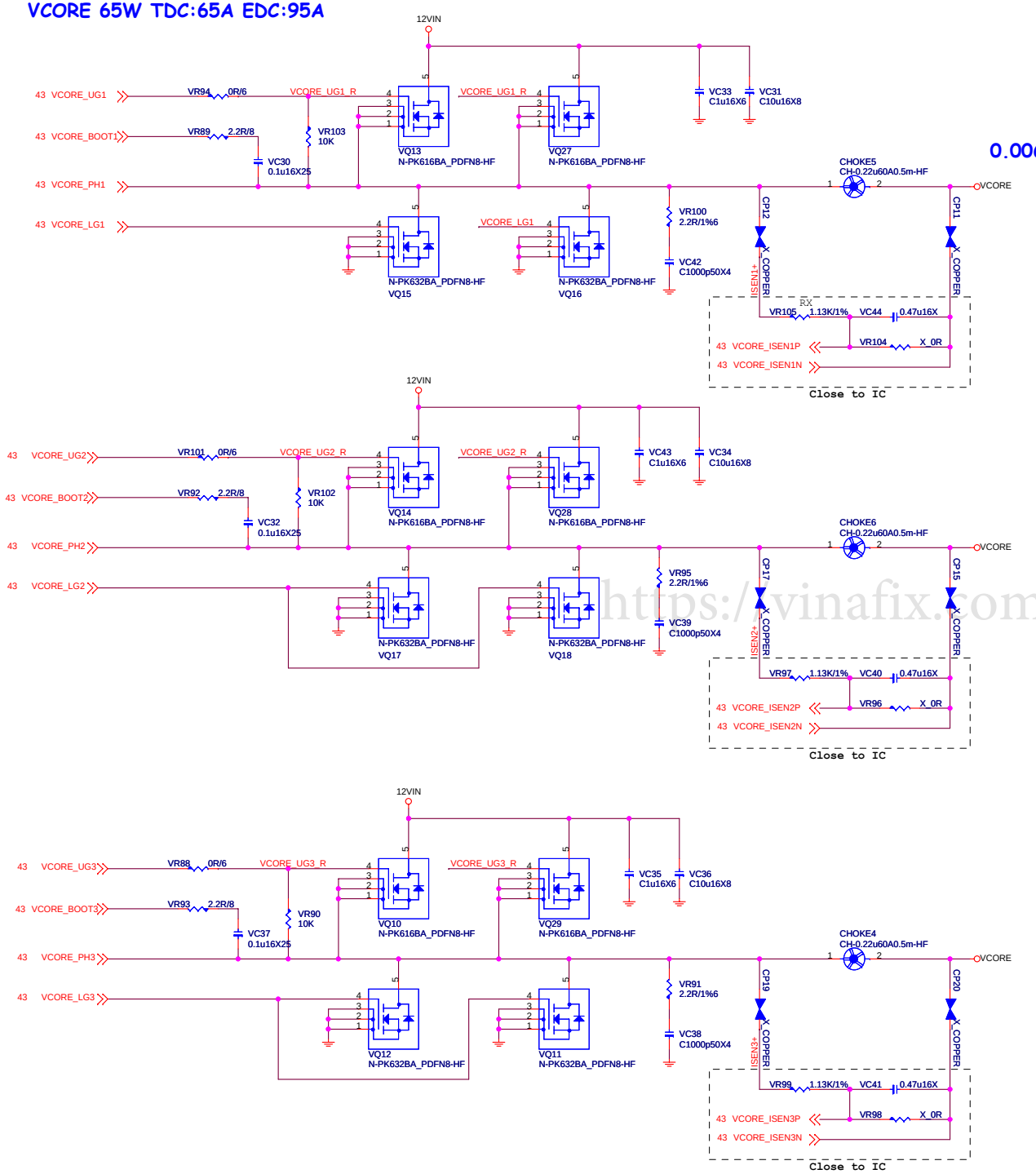
MSI MICRO-STAR INT'L CO.,LTD.

Title: CPU Power RT8894 3+2 Phase

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 43 of 55

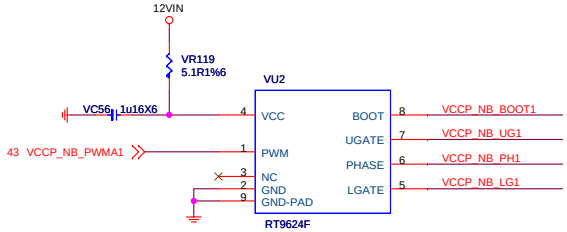
VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A

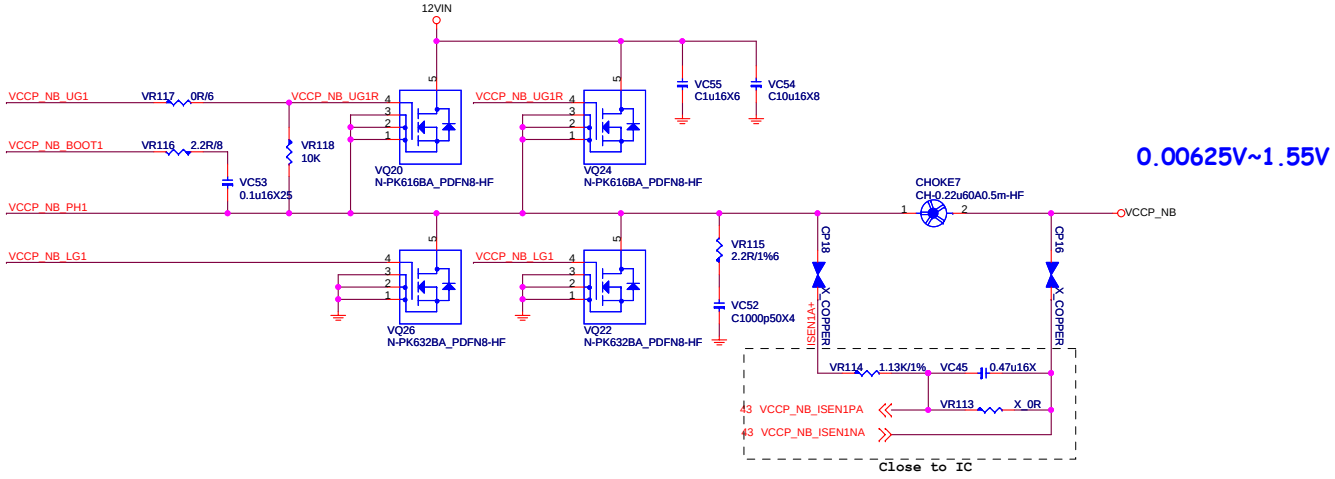


MICRO-START INT'L CO.,LTD.

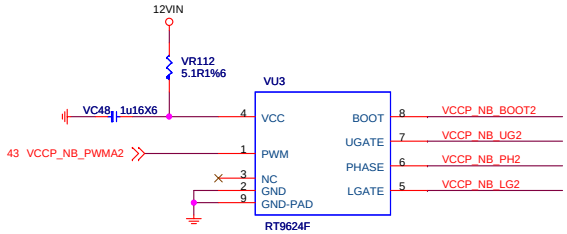
Title	CPU Power Phase 1-3	
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 44 of 55	

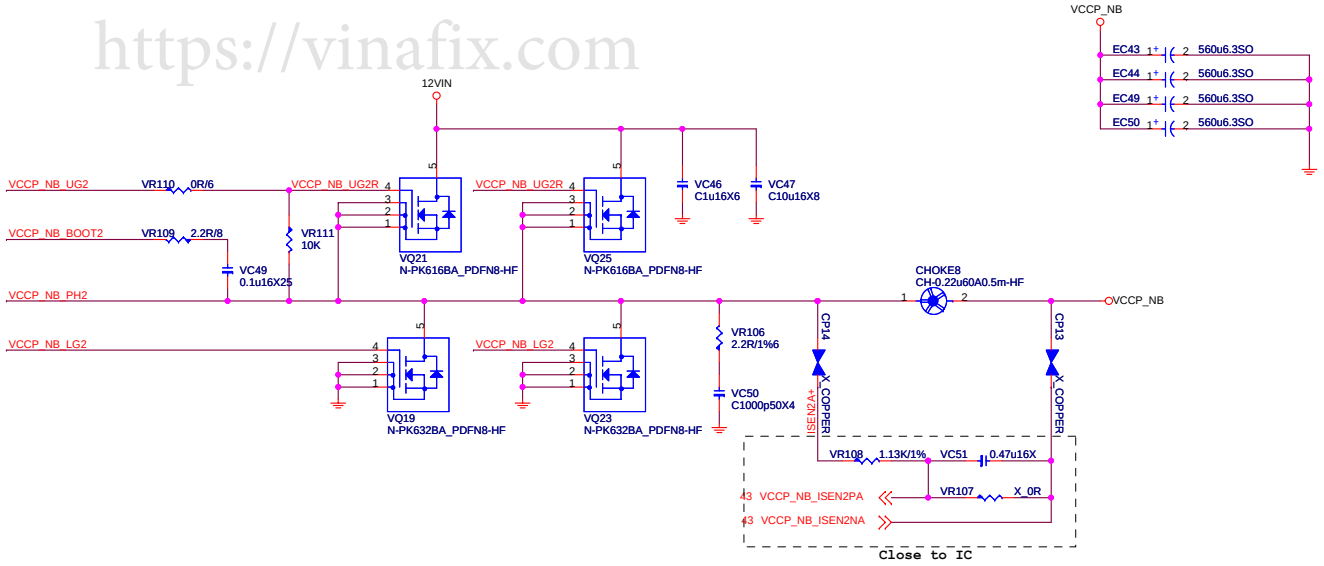
VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A





0.00625V~1.55V





MICRO-START INT'L CO.,LTD.

Title: CPU Power NB Phase 1-2		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 45 of 55	

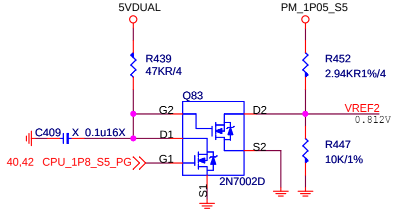
FOR VCCP_SOC_s5
0.9A

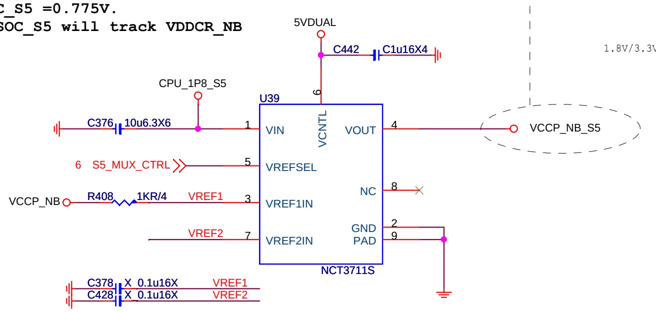
TYPE0 Only

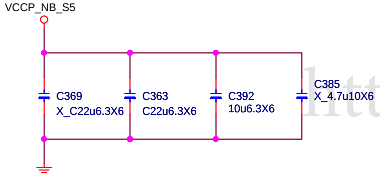
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

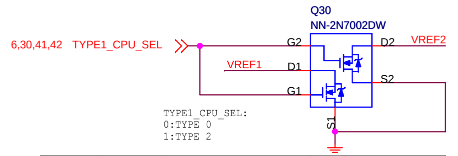
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0









CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

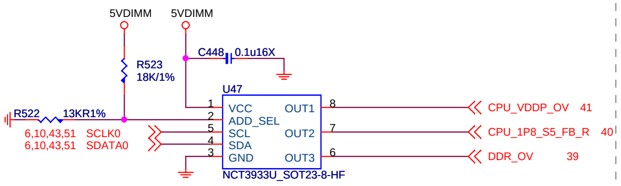
Over Voltage Control IC

UPI VOLTAGE CONSOLE

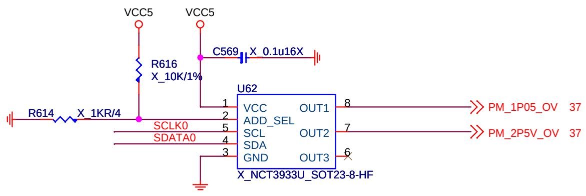
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

埃獲襘渍癸　ፕヴ：腊　，　玥ぃ　NCT3933籔柞襘渍匡兜

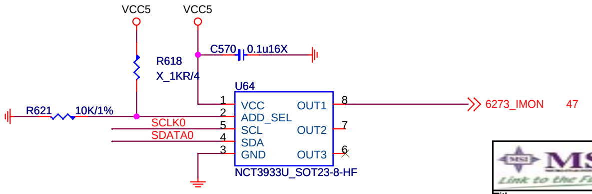
0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



0x2A:RH=OPEN,RL=10K



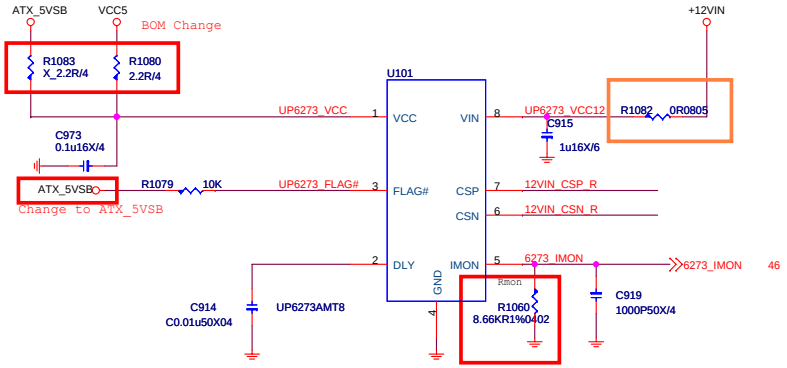
MICRO-STAR INT'L CO.,LTD.

Title	CPU Power NB Switch / NCT3933 OV
Size	Custom
Document Number	MS-7A39
Rev	1.0
Date:	Friday, January 20, 2017
Sheet	46 of 55

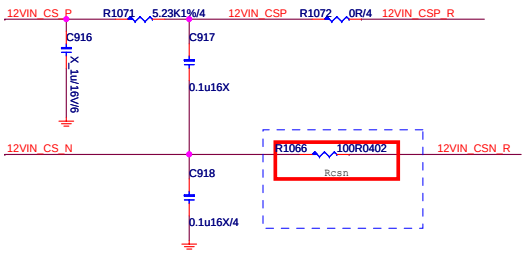
uP6273 CURRENT SENSE

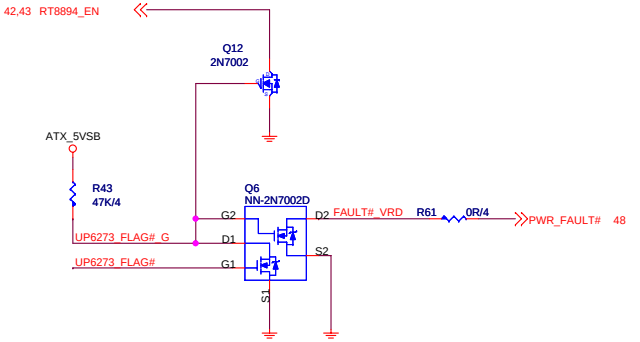
VCORE EDC MAC 125A

NB EDC MAX75A

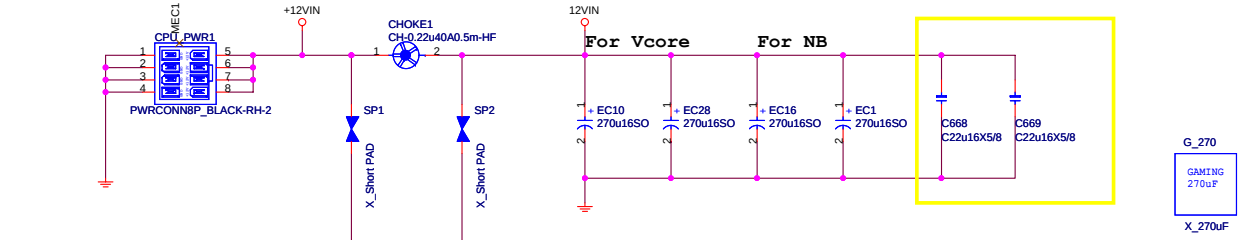


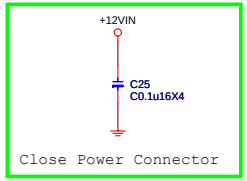
OCP = 26A(default)





CPU POWER CONNECTOR





Irms = Iout * SQRT{D/N- (D)^2]}

CORE:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=3
=125A*SQRT(0.0388-0.0136)
=19.8A

NB:
D=Vout/Vin=1.4/12=0.1166
N=Phase number=2
=75A*SQRT(0.0583-0.0136)
=15.8A

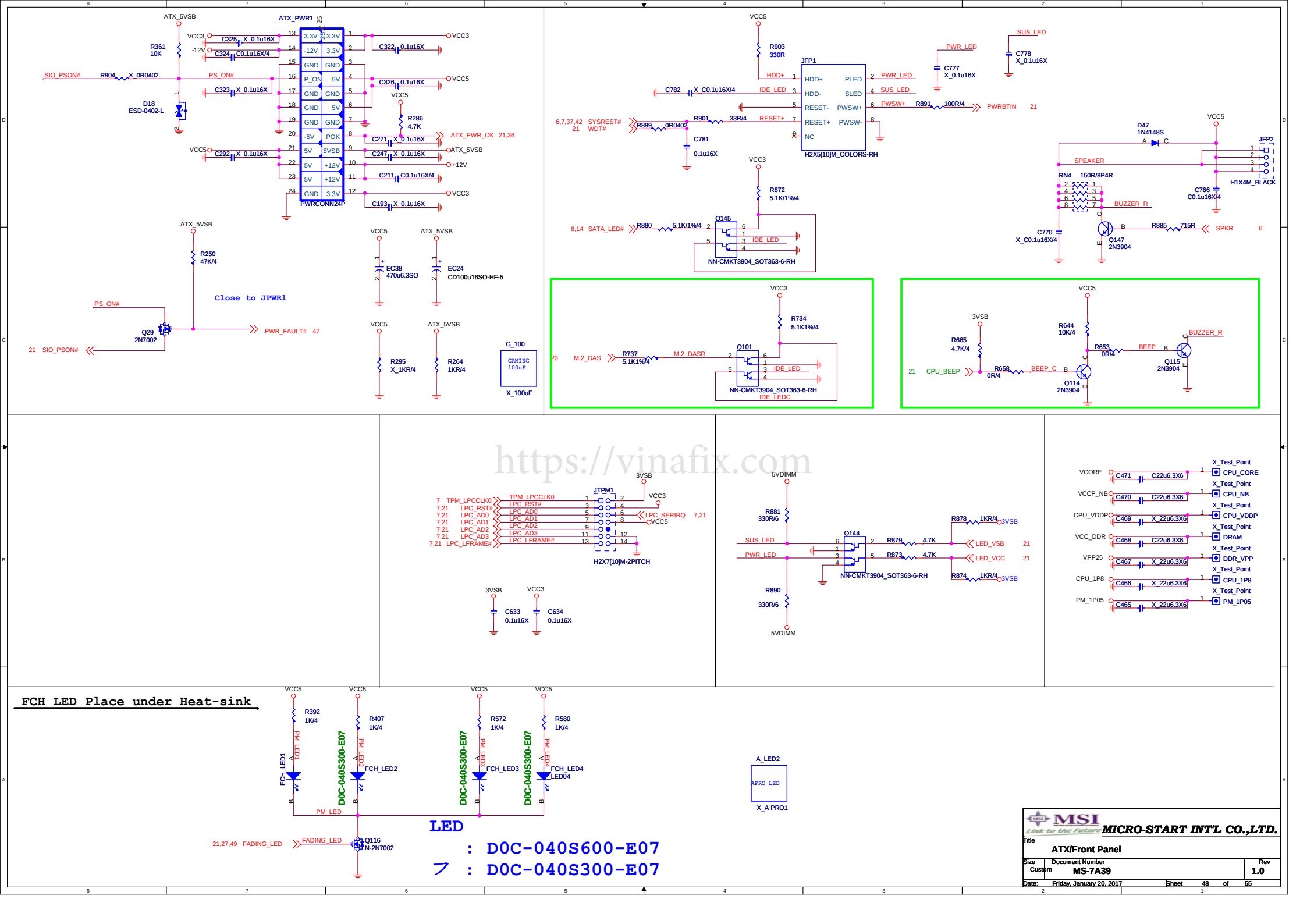
uP6273 CURRENT SENSE

VCORE EDC MAC 125A

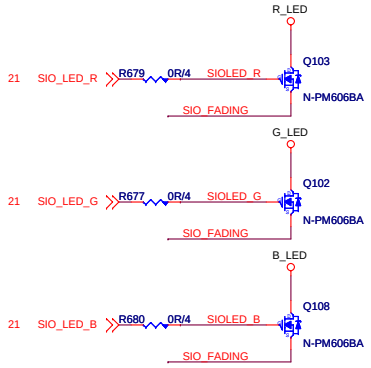
NB EDC MAX75A

MICRO-START INT'L CO.,LTD.

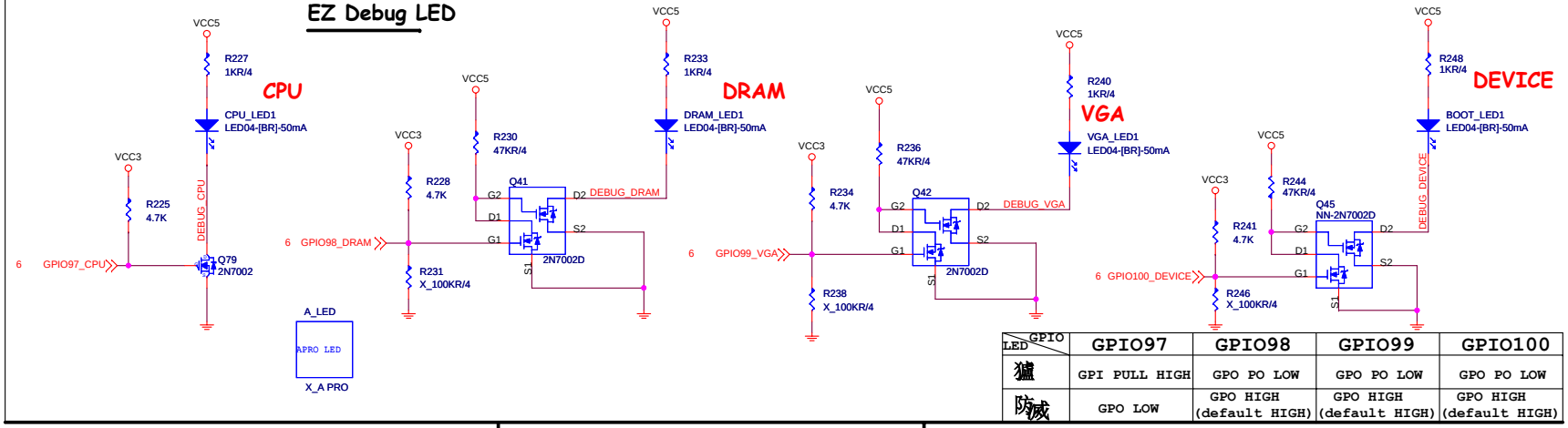
Title: uP6273 CURRENT SENSE		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 47 of 55	



LED Control by SIO

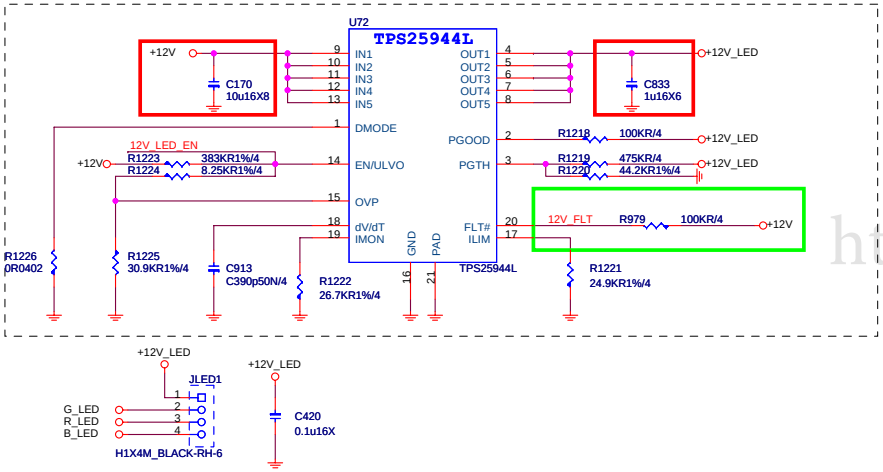


EZ Debug LED

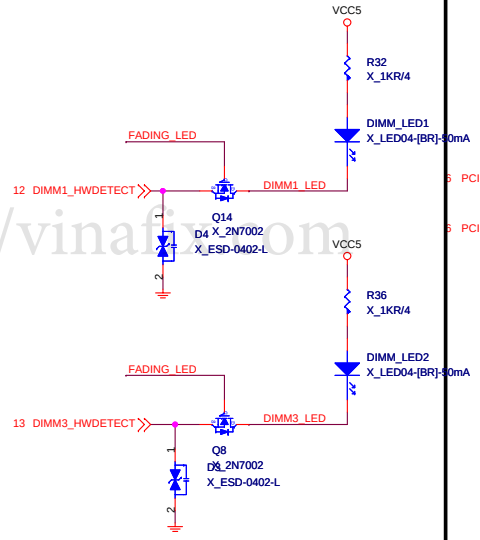


LED \ GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獨	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

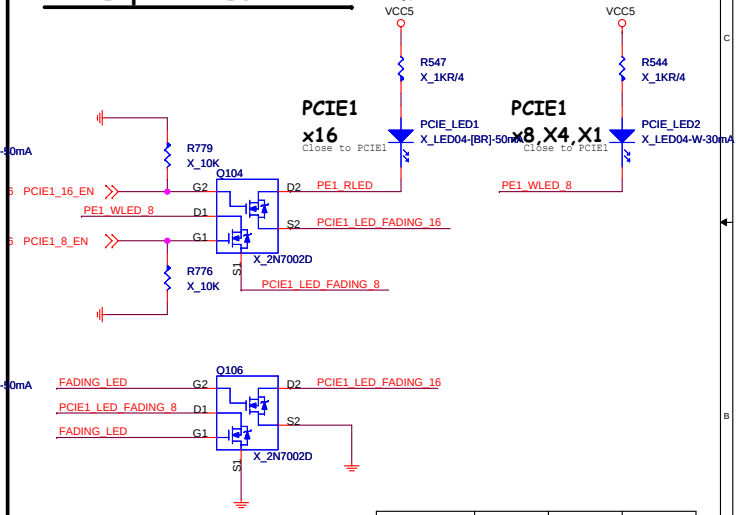
2016.07.06 Use TPS25944L



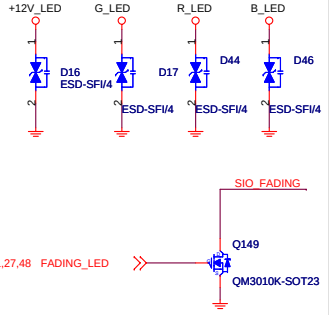
DDR LED REMOVE



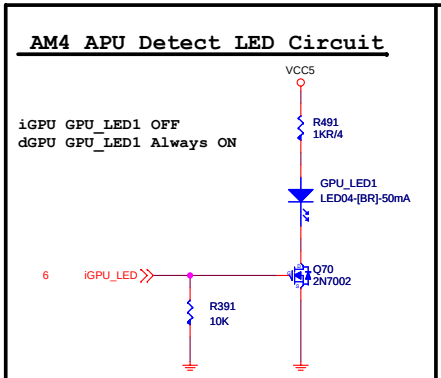
PCI Express LED Control remove



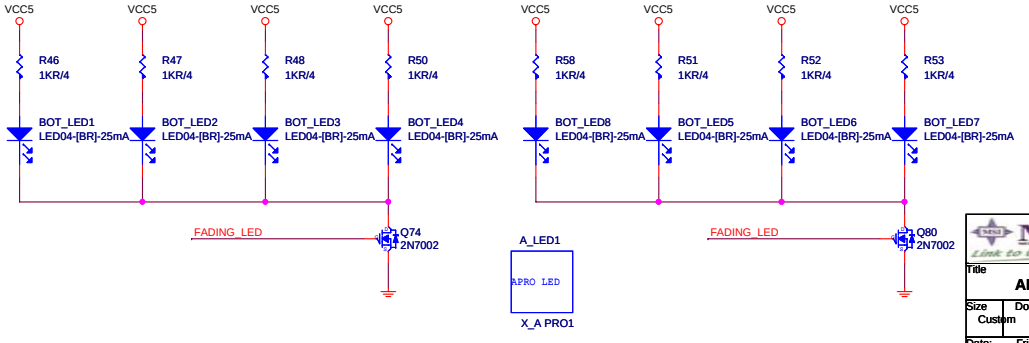
LED	x16	x8	x4
PCIE2	Red	White	White



AM4 APU Detect LED Circuit



Bottom LED



LED \ GPIO	EGPIO95	EGPIO96
獨	GPO PO HIGH	GPO PO HIGH
防	GPI (default LOW)	GPI (default LOW)

MSI Link to the Future MICRO-START INTL CO.,LTD.

Title: ALL LED Control

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 49 of 55

HEAT SINK

PM_HS1
MEC2
MEC1
HS-0408790-RH

MOS_HS1
MEC2
MEC1
MOS_HS1
E31-0504740-K08

CPU Socket

CPU2
E95-0000021-C22
RETENTION MODULE

Simulation

X_JS3
SIM1
X_PIN1*2

X_JS4
SIM2
X_PIN1*2

MANUAL PART

HDMI_LA1
Y01-RHDMI03-000

SSE_LA1
Y02-MA00101-SSE

XSP_LA1
Y02-MA00401-XSP

CFOS_LA1
Y02-MU00170-CFO

MKT2
G51-M1SPK31-Q13

MKT1
G51-M1SPK31-Q13

BIOS_LABEL
G51-M1SPXXA-A09

REF2
APRO LED
X_REF2

PCB1
7A36-0A
PK0-07A360A-E48,腦地,腳　吹邻紅(MSIS)
PK0-07A360A-G37,弘e-裏　,腳　吹邻紅(MSIS)

BAT1_X1
BAT-CR2032-RH

Optics Orientation Holes

MH4
X_MH001

MH6
X_MH001

MH1
X_MH001

MH2
X_MH001

5010
FM1
FM2
X_FM120
X_FM120

5020
FM3
FM4
X_FM120
X_FM120

FM5
FM6
X_FM120
X_FM120

FM7
FM8
X_FM120
X_FM120

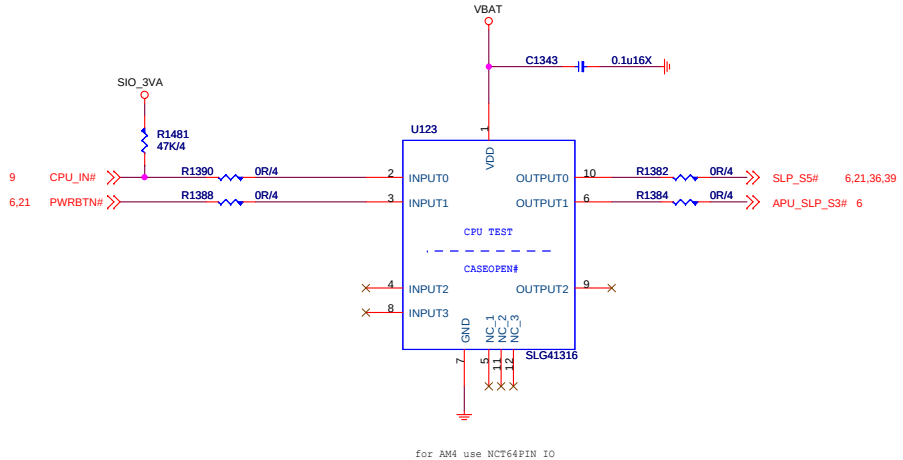
OPT	Configure	BOM	Function
		601-7A36-A01	XXXX

MSI Link to the Future MICRO-START INT'L CO.,LTD.

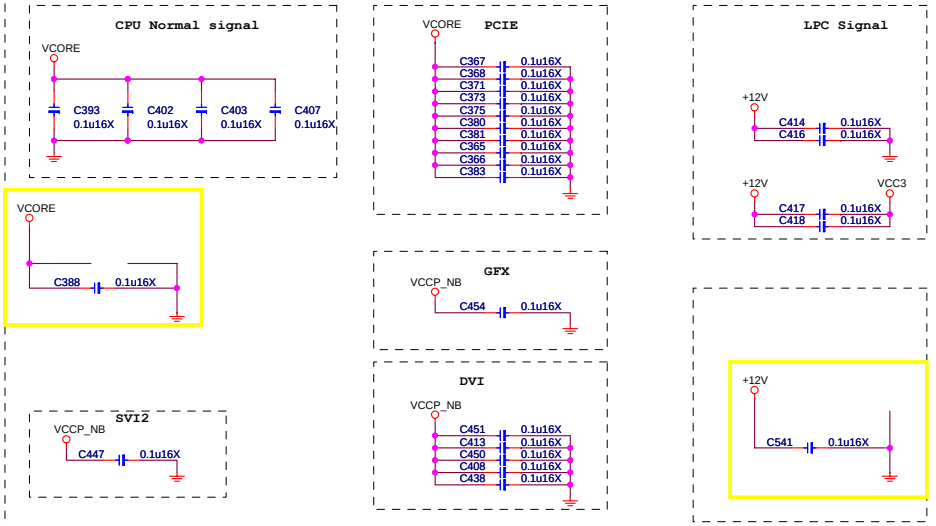
Title: BOM OPTION

Size: Custom | Document Number: MS-7A39 | Rev: 1.0

Date: Friday, January 20, 2017 | Sheet 50 of 55

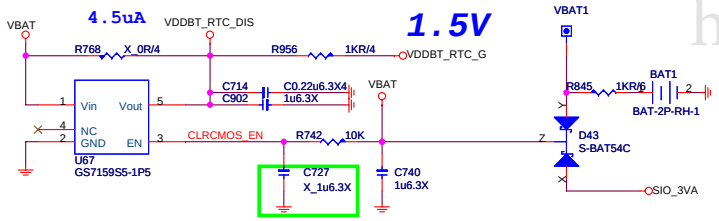


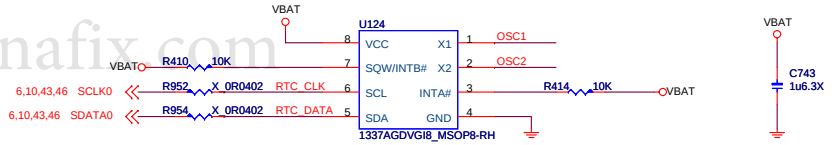
Moat Cap



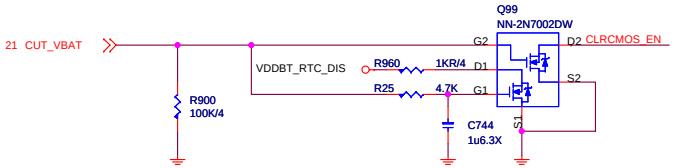
RTC & Clear CMOS Circuit

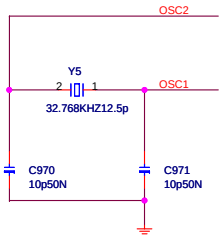
Placement Bottom Side

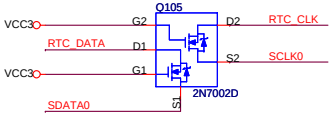


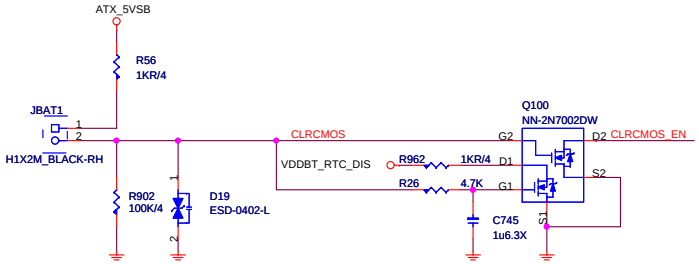


Slave Address:
11010000 , Wite , E0
11010001 , Read , E1









MICRO-START INT'L CO.,LTD.

Title: RTC Circuit		
Size: Custom	Document Number: MS-7A39	Rev: 1.0
Date: Friday, January 20, 2017	Sheet 51 of 55	