MS-7817

mATX
Ver: 10

Intel Sharkbay plamform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL892

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Other:

DVI*1
VGA*1
SATA2*2
SATA3*2
FRONT USB2.0 *2
REAL USB2.0 *4
REAL USB3.0 *2

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1

MICRO-STAR INT'L CO.,LTD

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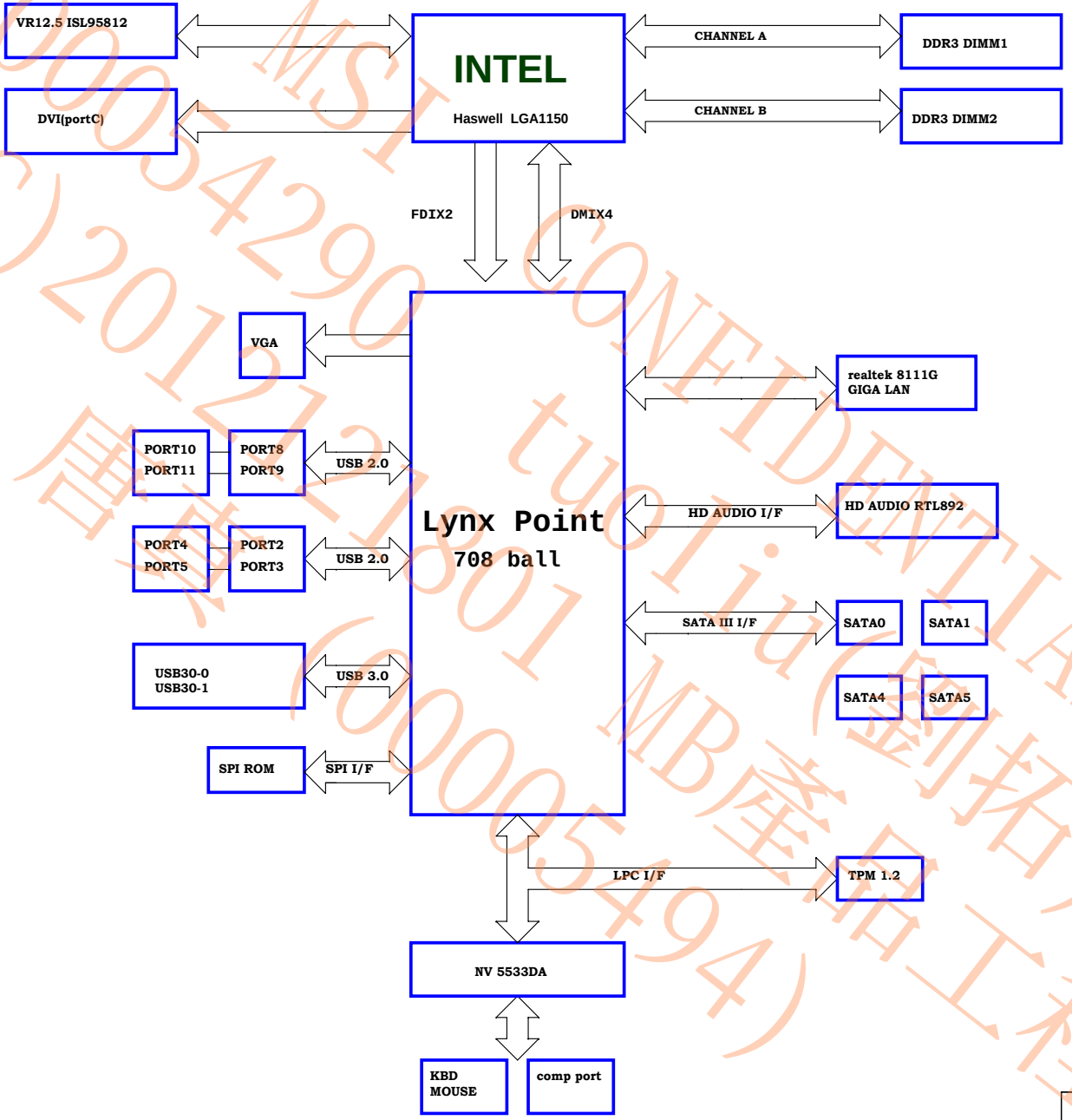
Date: Tuesday, December 04, 2012	Sheet 1 of 36	

MS-7817 Block Diagram



MICRO-STAR INT'L CO.,LTD		
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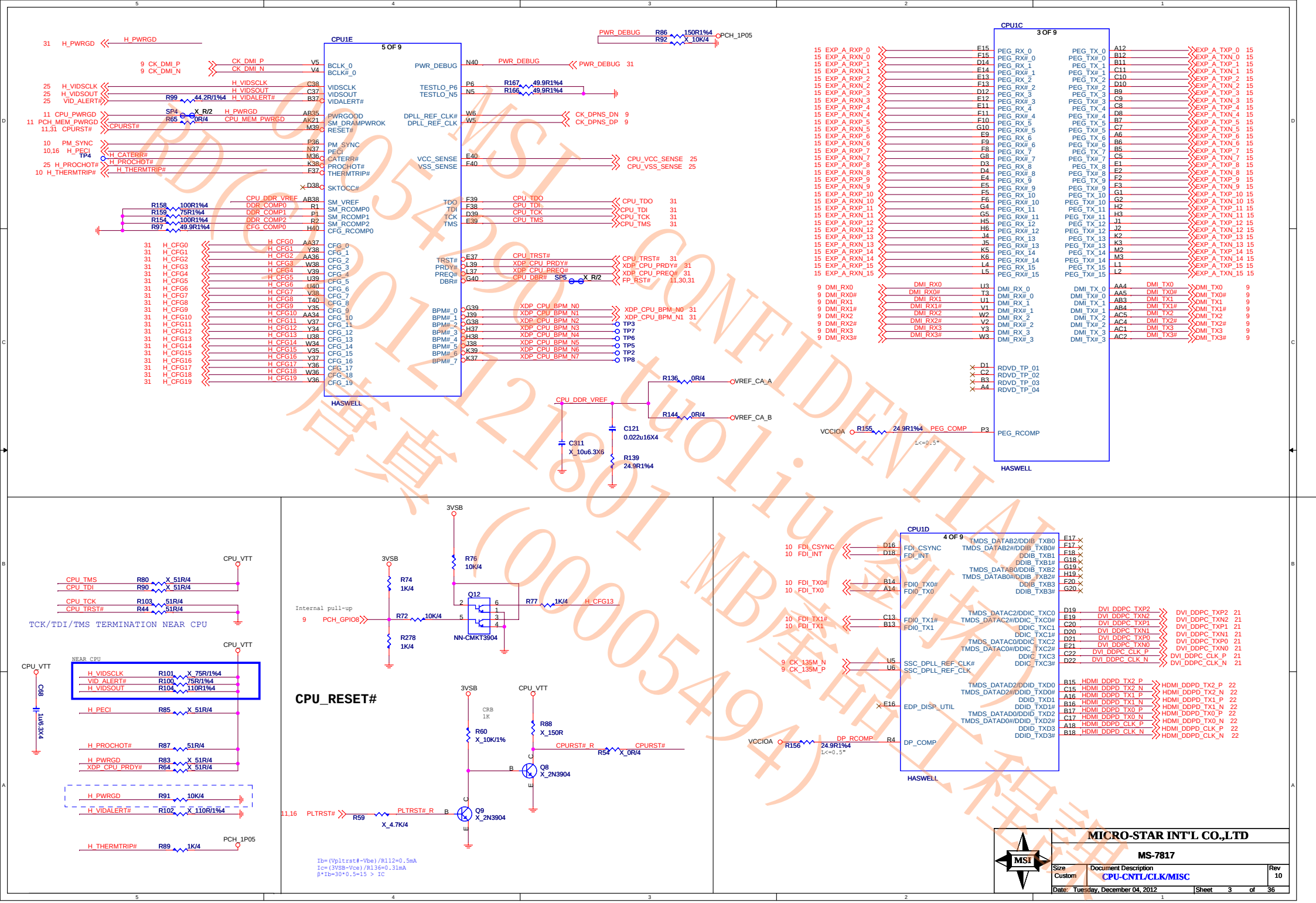
CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
HASWELL
CPU1D
4 OF 9
HASWELL
TCK/TDI/TMS TERMINATION NEAR CPU
CPU_RESET#
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CPU-CNTL/CLK/MISC
Size
Custom
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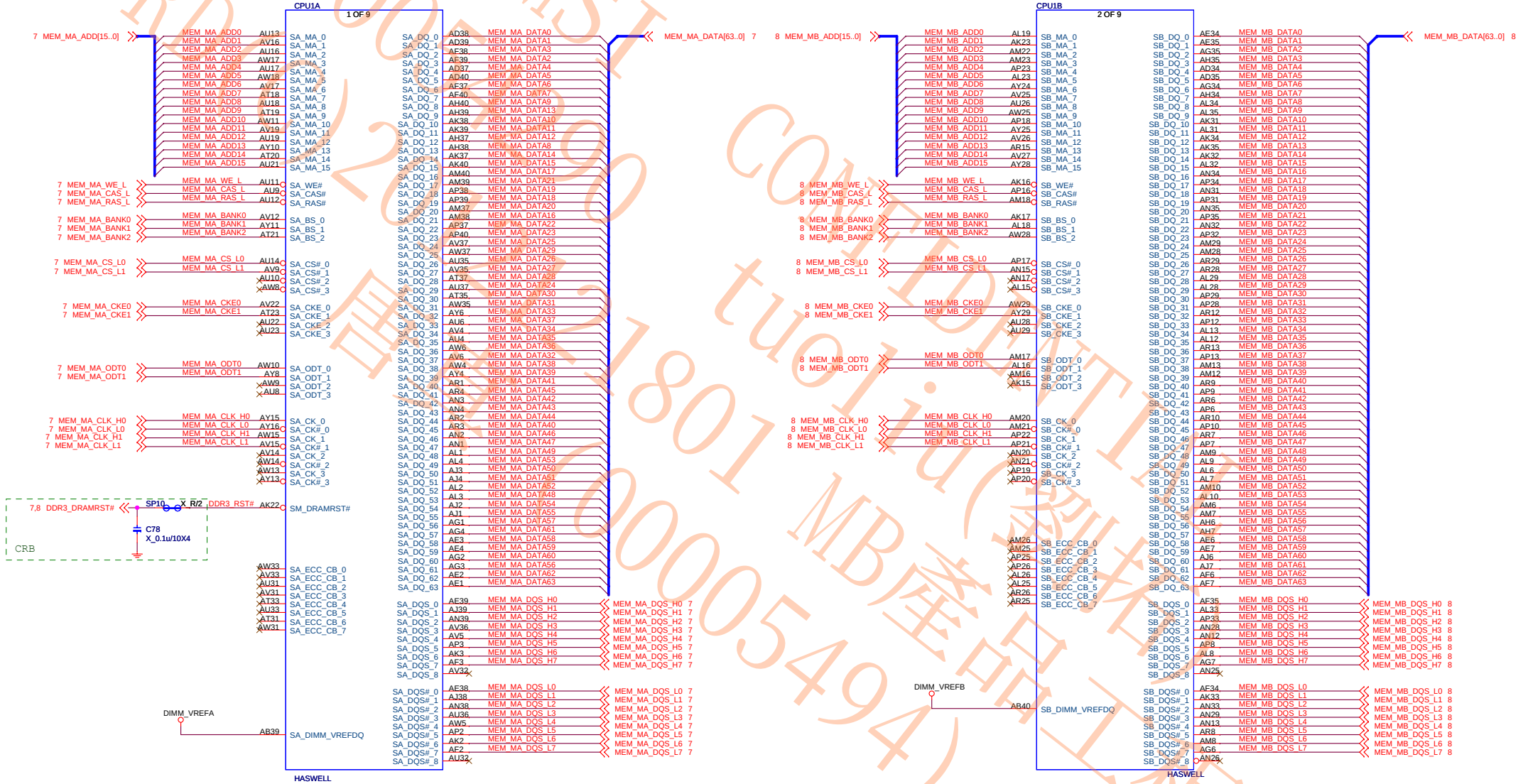

MICRO-STAR INT'L CO.,LTD			
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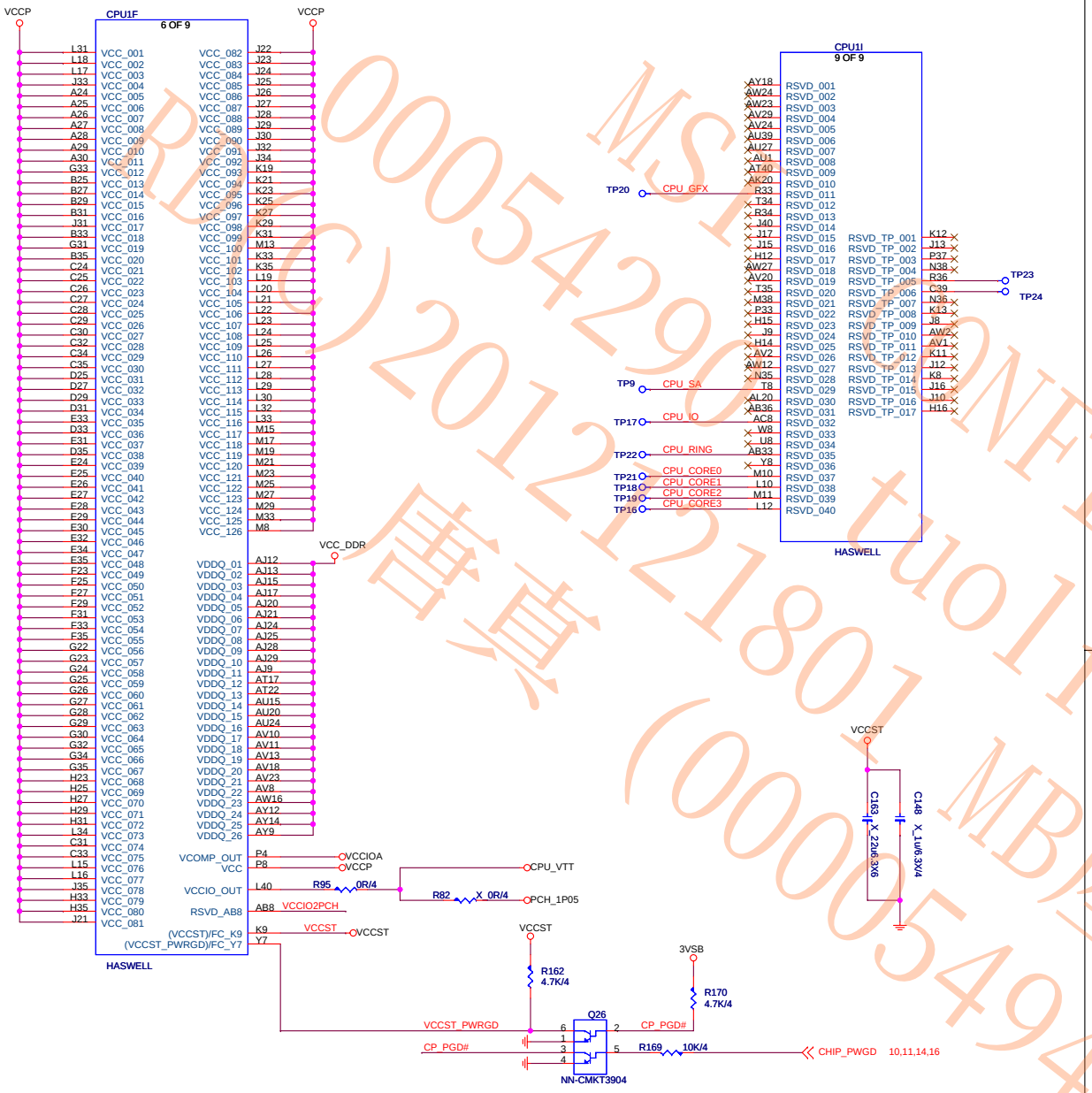
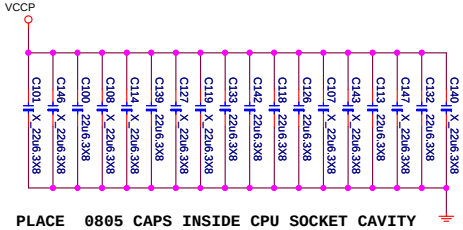
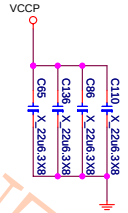


+CPU_VCCP-Decoupling

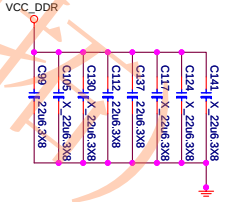


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805 CAPS Near CPU SOCKET edge



+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS

MICRO-STAR INT'L CO.,LTD		
MS-7817		
Size: Custom	Document Description: CPU-Power	Rev: 10
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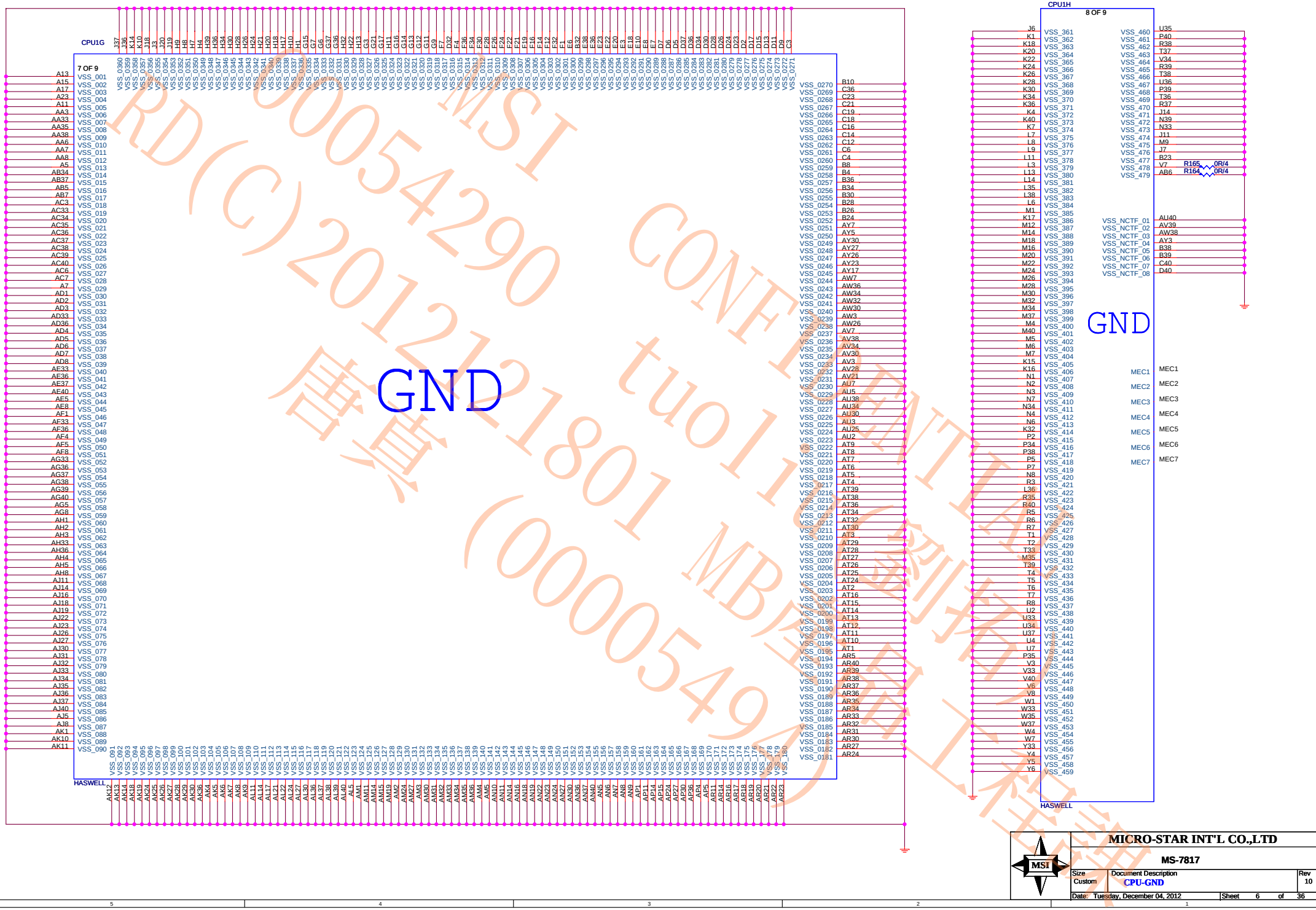

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU-GND	10

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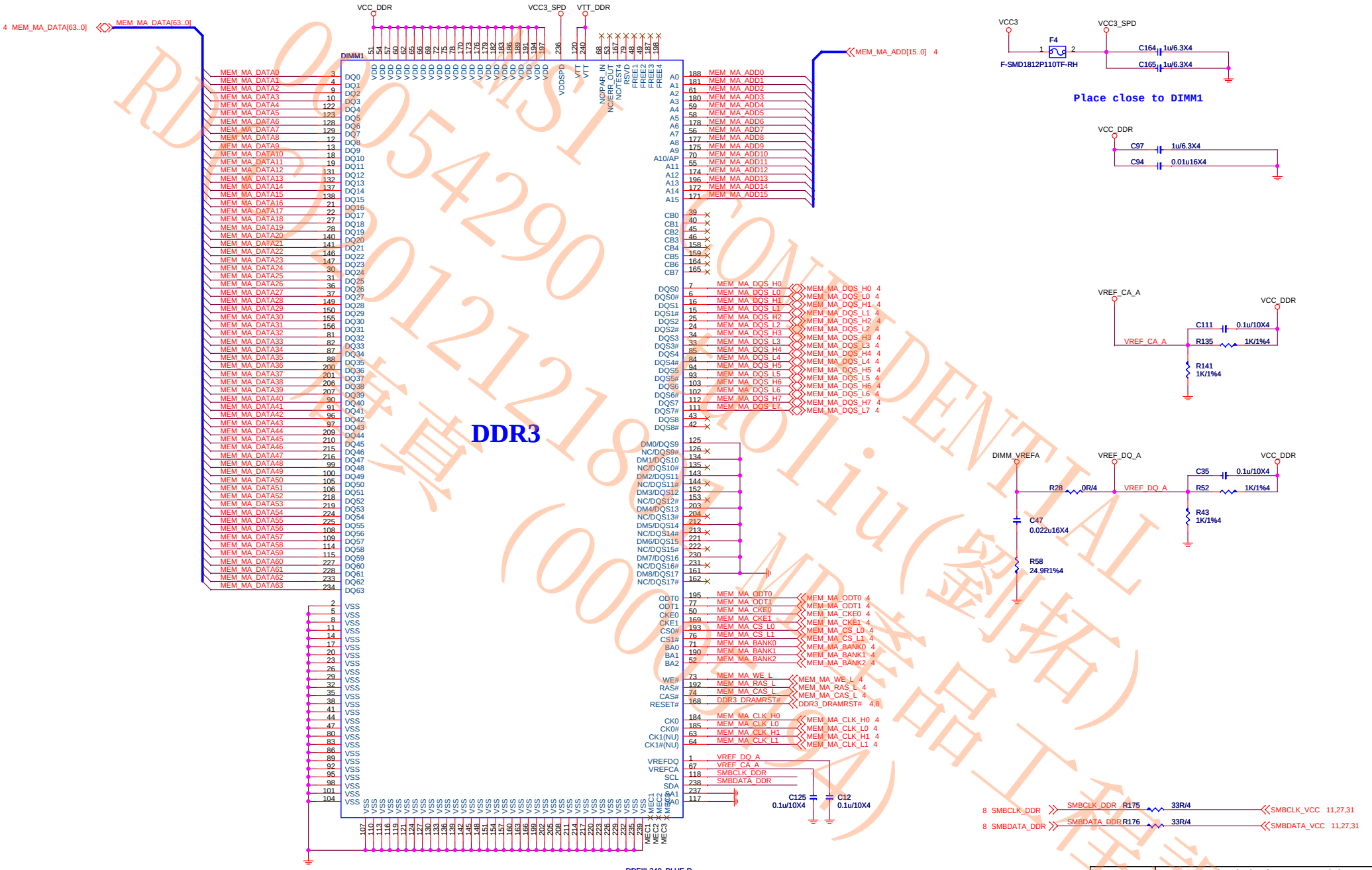

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Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
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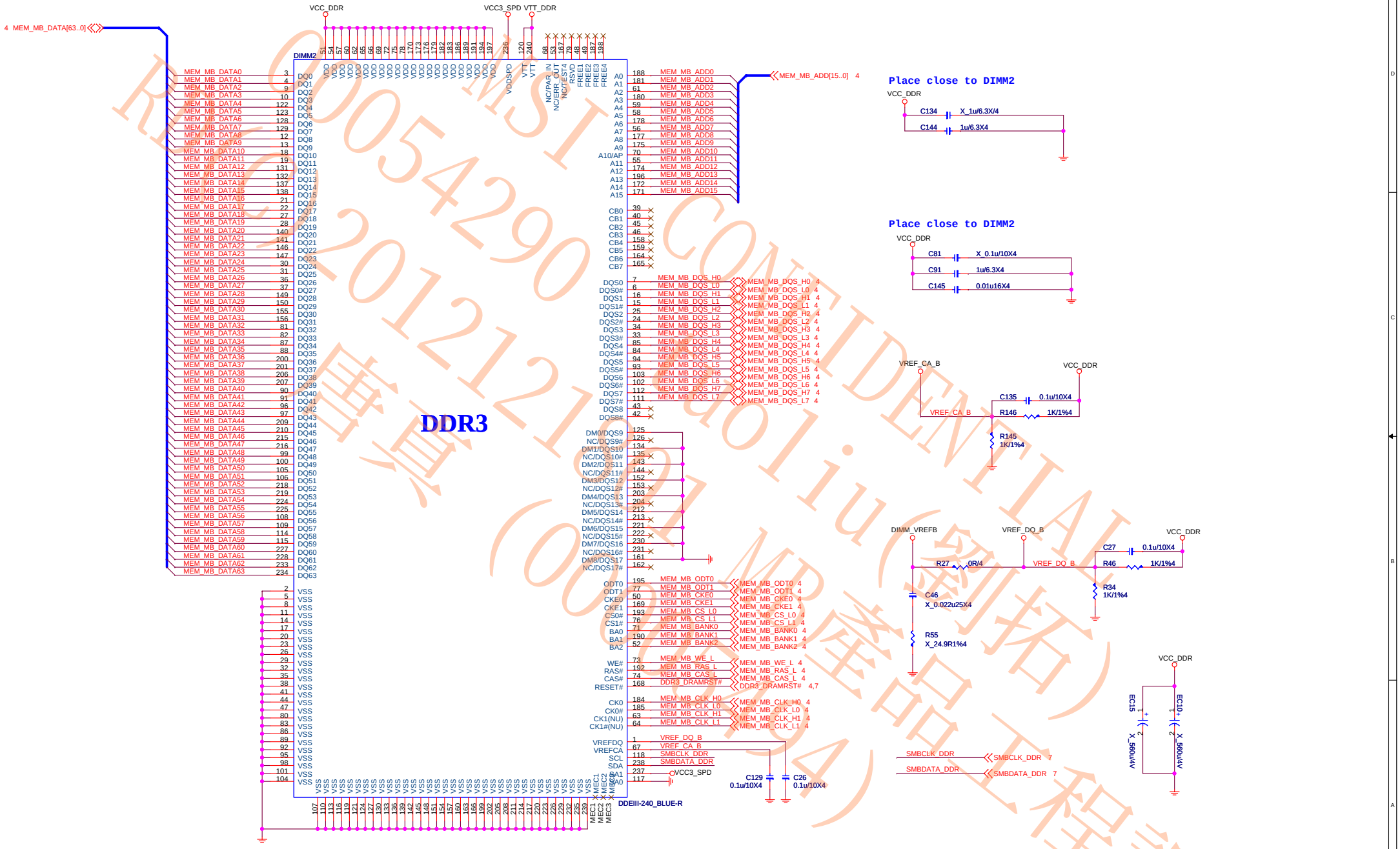
DDRIII DIMM_B0



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4	Rev: 10
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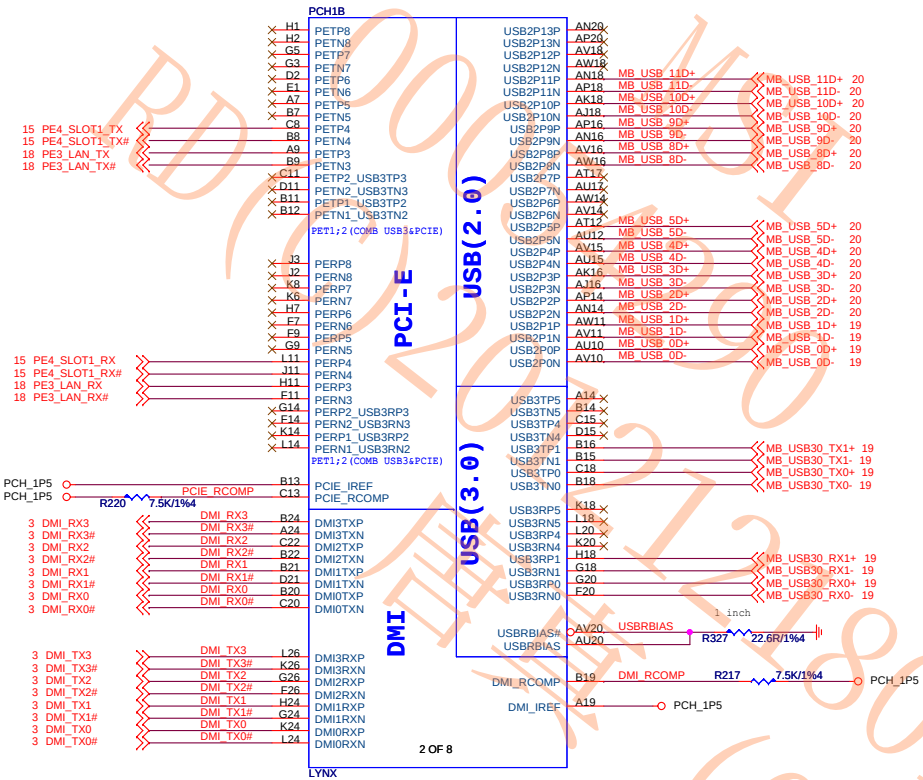
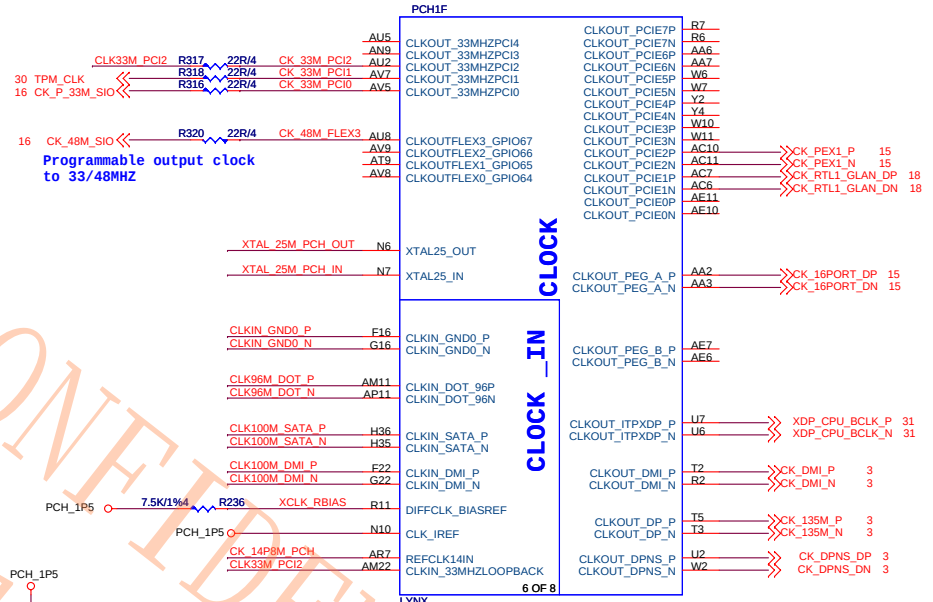
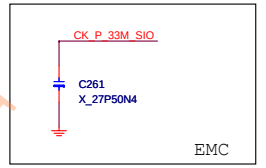
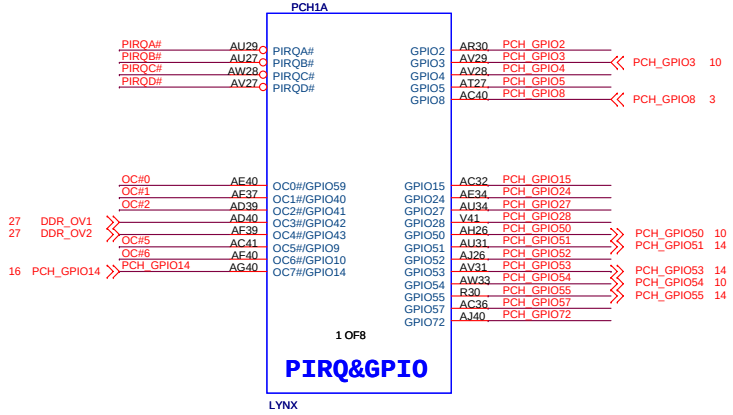
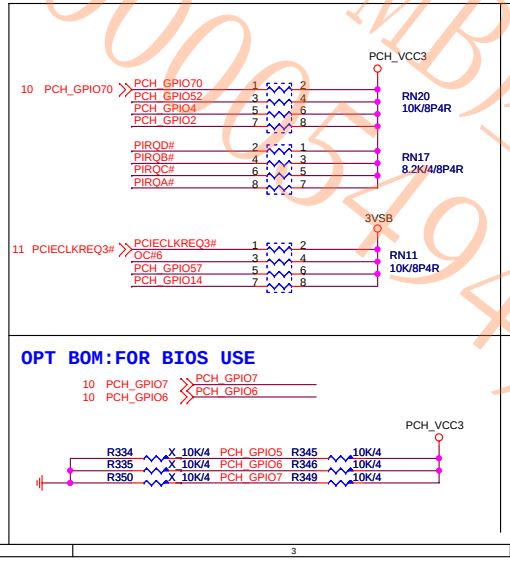
USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
Only USB 3.0 ports 1 and 2 are enabled.
pcie port7,8 NA

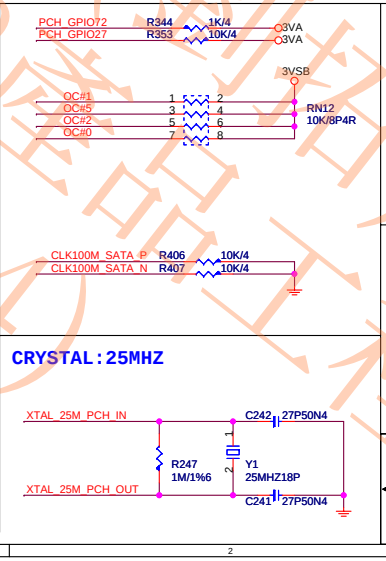


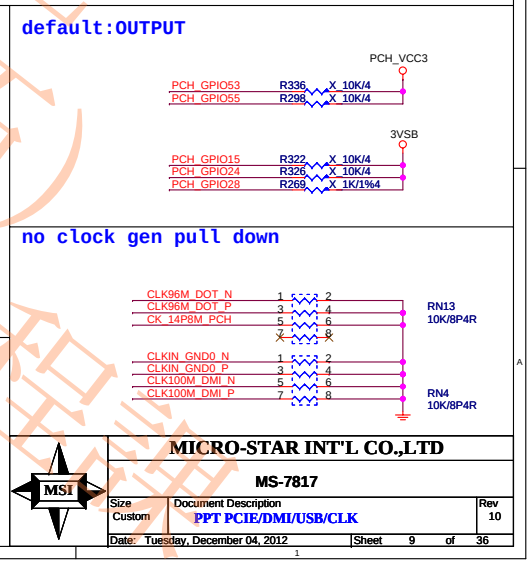












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Size: Custom
Document Description: PPT PCIE/DMI/USB/CLK
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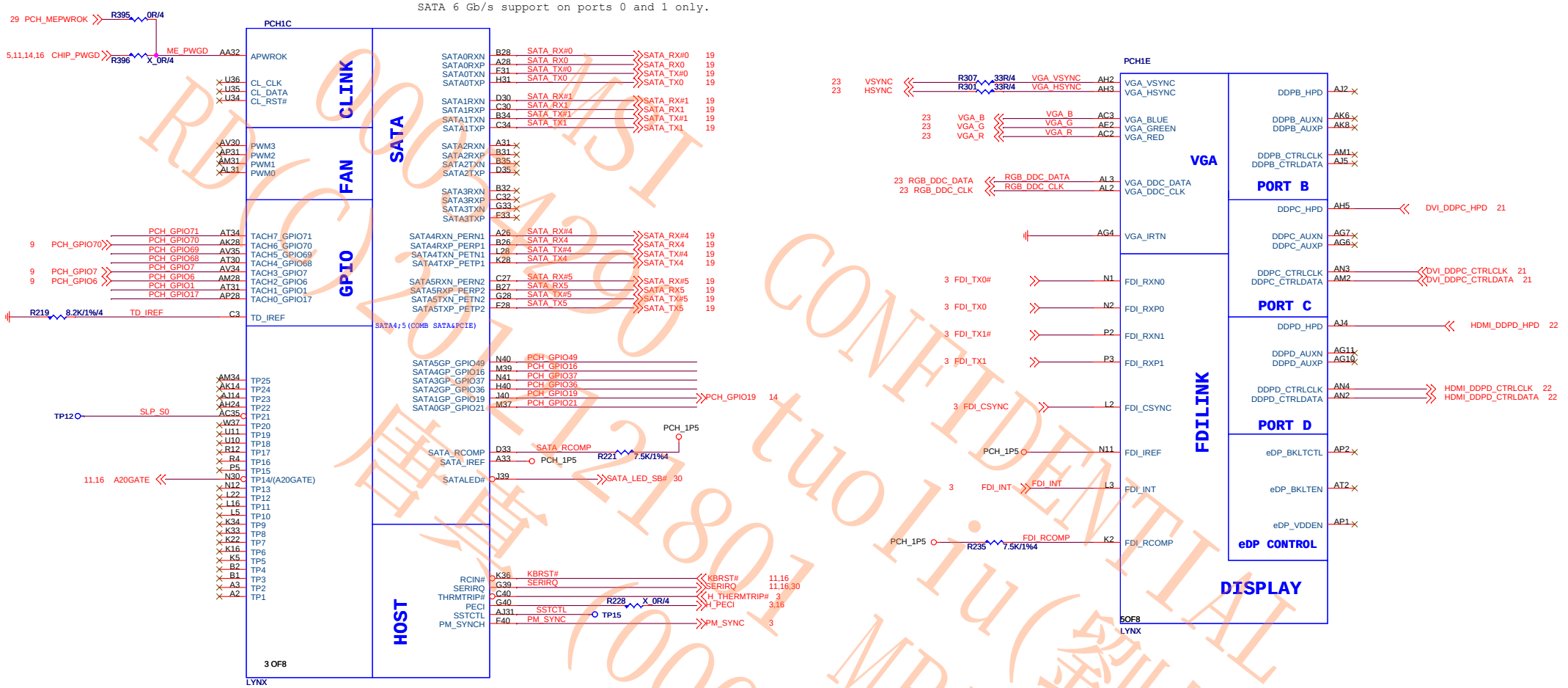
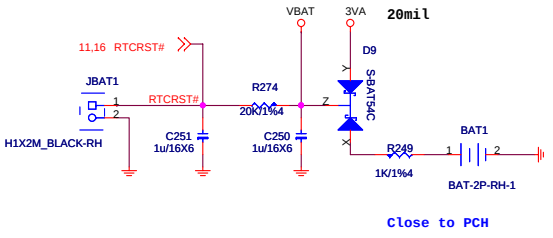
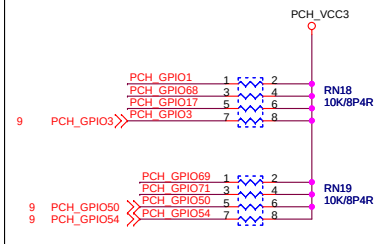
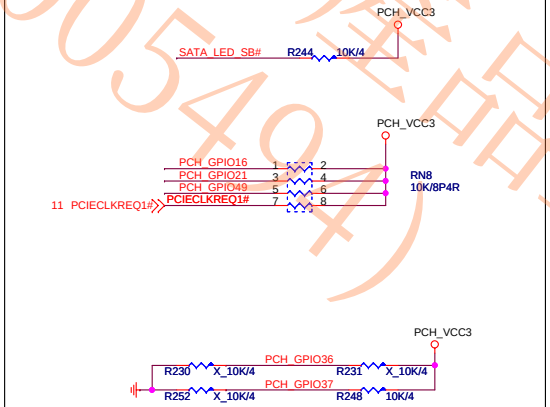
SATA ports 2 and 3 are disabled on 4 port SKUs.
SATA 6 Gb/s support on ports 0 and 1 only.



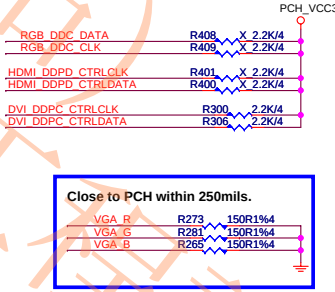
RTC and CLR_CMOS







Enable VGA(CTRLCLK/DATA Pull High)



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MS-7817	
Size: Custom	Document Description: PPT SATA/HOST/FAN/GPIO/VGA
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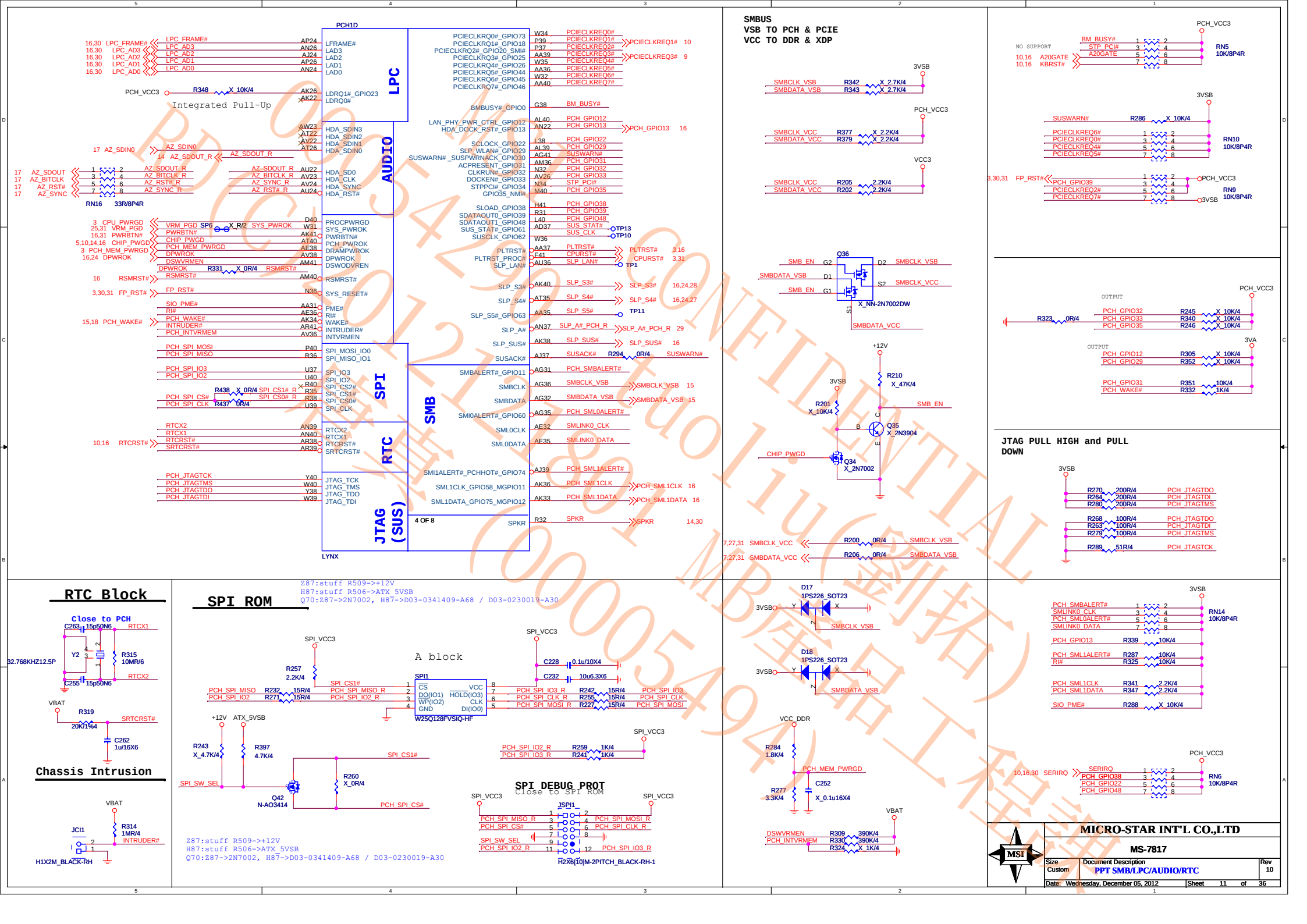
PCH1D
LPC
AUDIO
SPI
SMB
RTC
JTAG (SUS)
LYNX
4 OF 8
Integrated Pull-Up
SMBUS
VSB TO PCH & PCIE
VCC TO DDR & XDP
JTAG PULL HIGH and PULL DOWN
RTC Block
Close to PCH
Chassis Intrusion
SPI ROM
A block
SPI DEBUG PROT
Close to SPI ROM
Z87:stuff R509->+12V
H87:stuff R506->ATX_5VSB
Q70:Z87->2N7002, H87->D03-0341409-A68 / D03-0230019-A30
MICRO-STAR INT'L CO.,LTD
MS-7817
PPT SMB/LPC/AUDIO/RTC
Rev 10
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VCC3	0.21A
3VA	0.015A
VBAT	6uA
3VSB	0.261A
VCC1_5	0.249A
PCH_1P05	5.747A

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

POWER

PCH1G

PCH_1P05 — T20 T19 P28 P26 P25 P23 P22 P17 P16 P14 M14 AF23 AF22 AF20 AE19 AC12 — VCCIO_016 VCCIO_015 VCCIO_014 VCCIO_013 VCCIO_012 VCCIO_011 VCCIO_010 VCCIO_009 VCCIO_007 VCCIO_006 VCCIO_005 VCCIO_004 VCCIO_003 VCCIO_002 VCCIO_001

W25 W23 W19 W17 V25 V23 V22 V20 V19 V17 AD16 AB20 AB18 AB17 AB16 AA20 AA19 AB1 — VCCCORE_018 VCCCORE_017 VCCCORE_016 VCCCORE_015 VCCCORE_014 VCCCORE_013 VCCCORE_012 VCCCORE_011 VCCCORE_010 VCCCORE_009 VCCCORE_008 VCCCORE_007 VCCCORE_006 VCCCORE_005 VCCCORE_004 VCCCORE_003 VCCCORE_002 VCCCORE_001 — V_1P05_XCK_R

SPI_VCC3 — R41 — VCCSPI

3VSB — AP35 — VCCSUS3_3
VBAT — AP33 — VCCRTC_01

PCH_1P5 — T14 C1 C2 A4 B4 A40 A39 B39 K1 A38 B37 — VCCVRM_11 VCCVRM_10 VCCVRM_09 VCCVRM_08 VCCVRM_07 VCCVRM_06 VCCVRM_05 VCCVRM_04 VCCVRM_03 VCCVRM_02 VCCVRM_01

PCH_1P05 — AP22 — VCCUSBPLL

C279 0.1u/10X4 — C266 0.1u/10X4 — AH28 AW35 — DCPSST DCPRTC

P19 AE30 — DCPSUS_02 DCPSUS_01

C265 1u/16X6 — R321 5.1R1%4 — C264 0.1u16X4 — DCPSUSBYP — AU41 AU40 — DCPSUSBYP_02 DCPSUSBYP_01

500mil

R285 649R1%4 — DAC_IREF — AF5 — DAC_IREF

PCH_1P05 — V16 — VCCCLK

1.5_DAC_FB_R — AF2 — VCCADAC

V_PROC_IO — C39 — V_PROC_IO

C223 — X_1uF/6.3V/X/4

VCCADACBG3_3 — AE1
VCC3_3_01 — AW21
VCC3_3_02 — V30
VCC3_3_03 — W30
VCC3_3_04 — AE28
VCC3_3_05 — AG1
VCC3_3_06 — B6

VCCDSW3_3_01 — AV39
VCCDSW3_3_02 — AW38
VCCDSW3_3_03 — AW39

DCPSUS2 — AJ22

VCCSUS3_3_009 — AK20
VCCSUS3_3_008 — AJ20
VCCSUS3_3_007 — AH22
VCCSUS3_3_006 — AH20
VCCSUS3_3_005 — AH18
VCCSUS3_3_004 — P20
VCCSUS3_3_003 — AW33
VCCSUS3_3_002 — AW32
VCCSUS3_3_001 — AW28

LYNX

PCH_VCC3 — 3VA — TP14 — 3VSB

7OF 8

PCH_VCC3 HAVE SEQENCING

PCH_VCC3

VCCCLK3_3_13 AW3
VCCCLK3_3_12 AV3
VCCCLK3_3_11 AK11
VCCCLK3_3_10 AG12
VCCCLK3_3_09 AW9
VCCCLK3_3_08 AW4
VCCCLK3_3_07 AV4
VCCCLK3_3_06 AT5
VCCCLK3_3_05 AR4
VCCCLK3_3_04 AP7
VCCCLK3_3_03 AP5
VCCCLK3_3_02 AM9
VCCCLK3_3_01 AM7

PCH_1P05

VCCCLK_07 T16
VCCCLK_06 W16
VCCCLK_05 AA16
VCCCLK_04 AB2
VCCCLK_03 W14
VCCCLK_02 V14
VCCCLK_01 U12

+1P05V_ME

VCCASW_015 AF25
VCCASW_014 AD25
VCCASW_013 W26
VCCASW_012 AD23
VCCASW_011 AD22
VCCASW_010 AD20
VCCASW_009 AD19
VCCASW_008 AD17
VCCASW_007 AB26
VCCASW_006 AB25
VCCASW_005 AB23
VCCASW_004 AB22
VCCASW_003 AA26
VCCASW_002 AA25
VCCASW_001 AA23

H81->Stuff
H87->un-Stuff

+1P05V_ME — R416 X_0R/8 — R417 X_0R/8 — PCH_1P05

PCH_1P05 — R253 0R/8 — V_1P05_XCK_DCB_FB — R441 0R/4 — V_1P05_XCK_R
C247 X_10u6.3X6
C249 1u/6.3X4

PCH_1P5 — R442 0R/6 — 1.5_DAC_FB — R291 1R/4 — 1.5_DAC_FB_R
C347 0.01u16X4

PCH decoupling cap

close V14,U12,T16,V16

PCH_1P05 — C305 X_1u6.3X/4 — C306 X_1u6.3X/4

PCH_1P05 — C312 0.01u16X4 — C248 X_1u6.3X4 — C309 1u6.3X4 — C308 X_10u6.3X6 — C304 X_10u6.3X6 — C318 10u6.3X6

VBAT — C313 X_0.1u/10X4 — C277 1u6.3X4

3VSB — C274 1u6.3X4 — C301 1u6.3X4 — C314 X_0.1u/10X4 — C315 X_0.1u/10X4

SPI_VCC3 — C244 1u6.3X4

PCH_VCC3 — C307 X_1u6.3X/4 — C253 0.1u/10X4 — C310 X_0.1u/10X4

+1P05V_ME — C303 X_1u6.3X/4

PCH_VCC3 — C288 1u6.3X4 — C229 0.1u/10X4

T14
PCH_1P5 — C302 X_0.1u/10X4

3VA — C257 1u6.3X4

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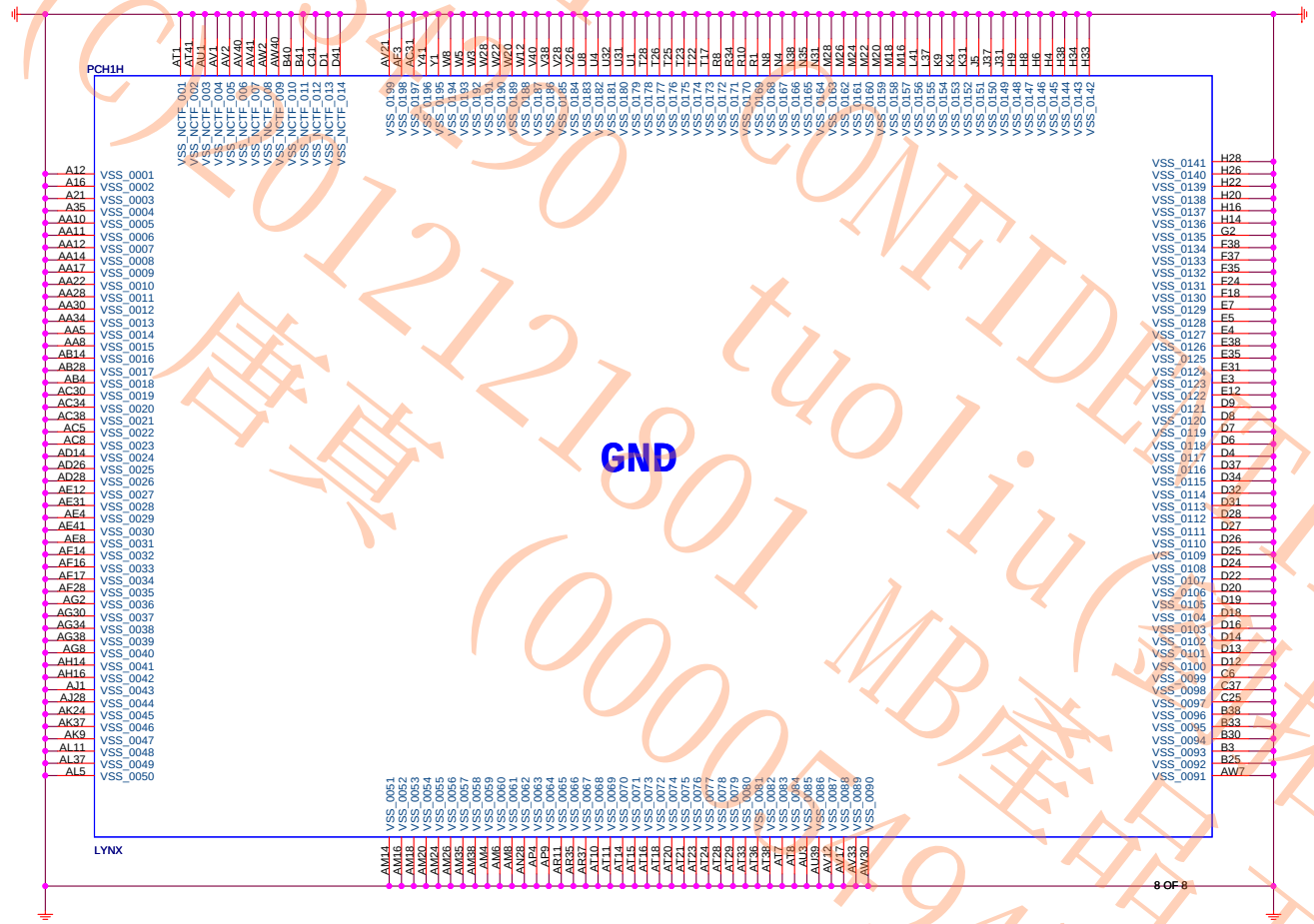

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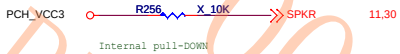
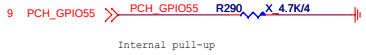
PCH Straps



SPKR

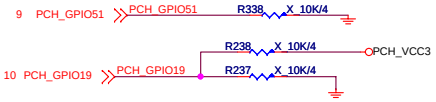
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



GPIO55

Default Mode:
Internal pull-up.
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

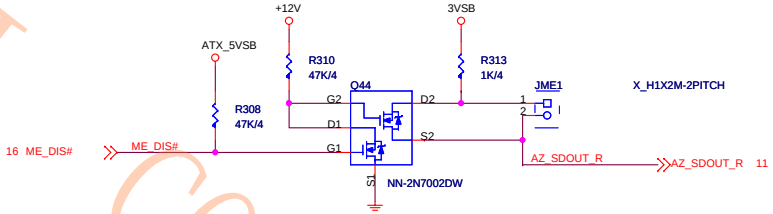


SATA1GP/GPIO19, GPIO51

Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



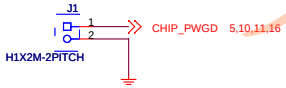
HDA_SDO

Default:
Do not pull high.
Disable ME in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

For test cpu voltage



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PPT STRAPS	Rev: 10
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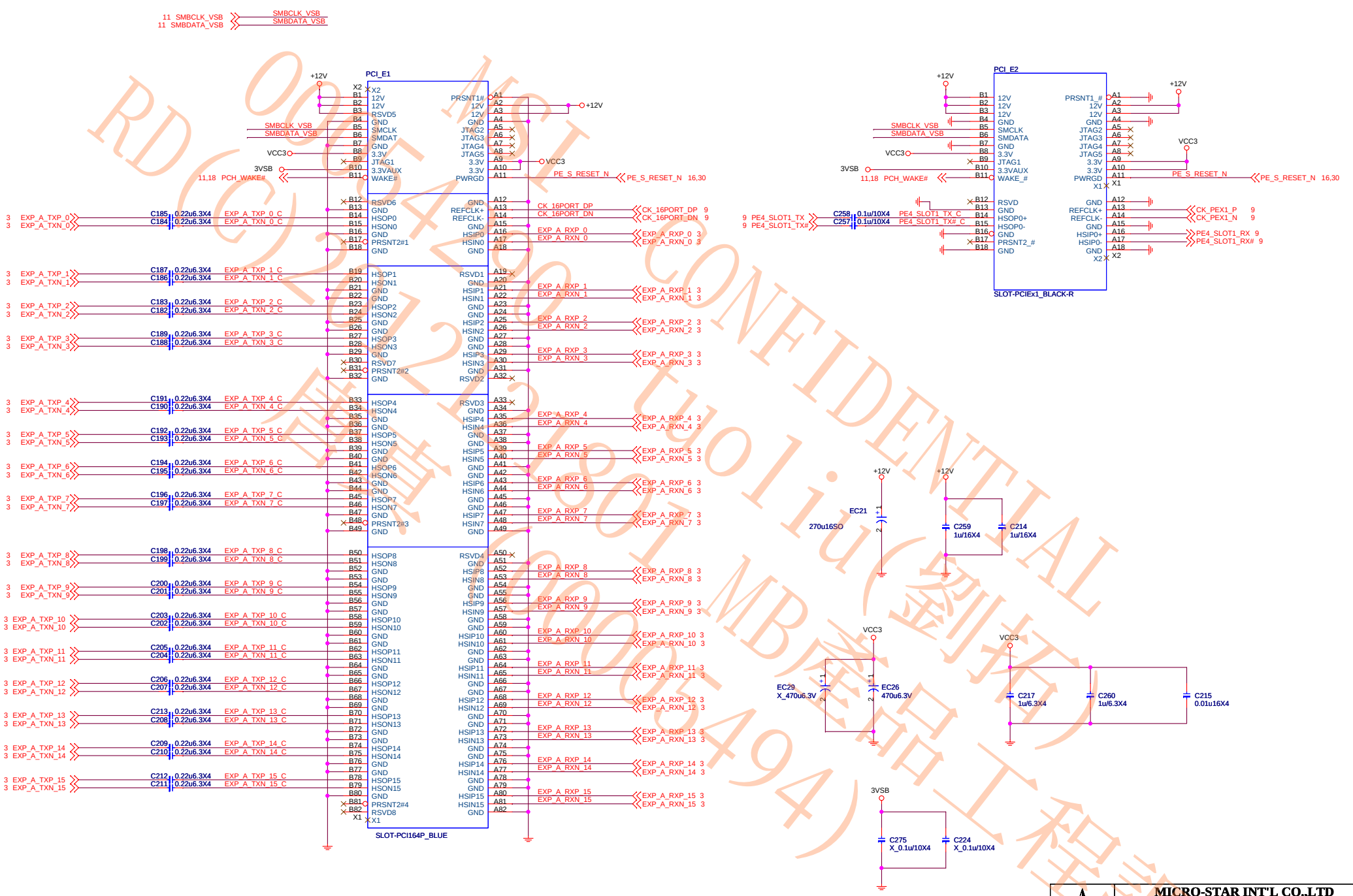

MICRO-STAR INT'L CO.,LTD	
MS-7817	
Size: Custom	Document Description: PCIE1(X1) & PCIE2(X16) Slots
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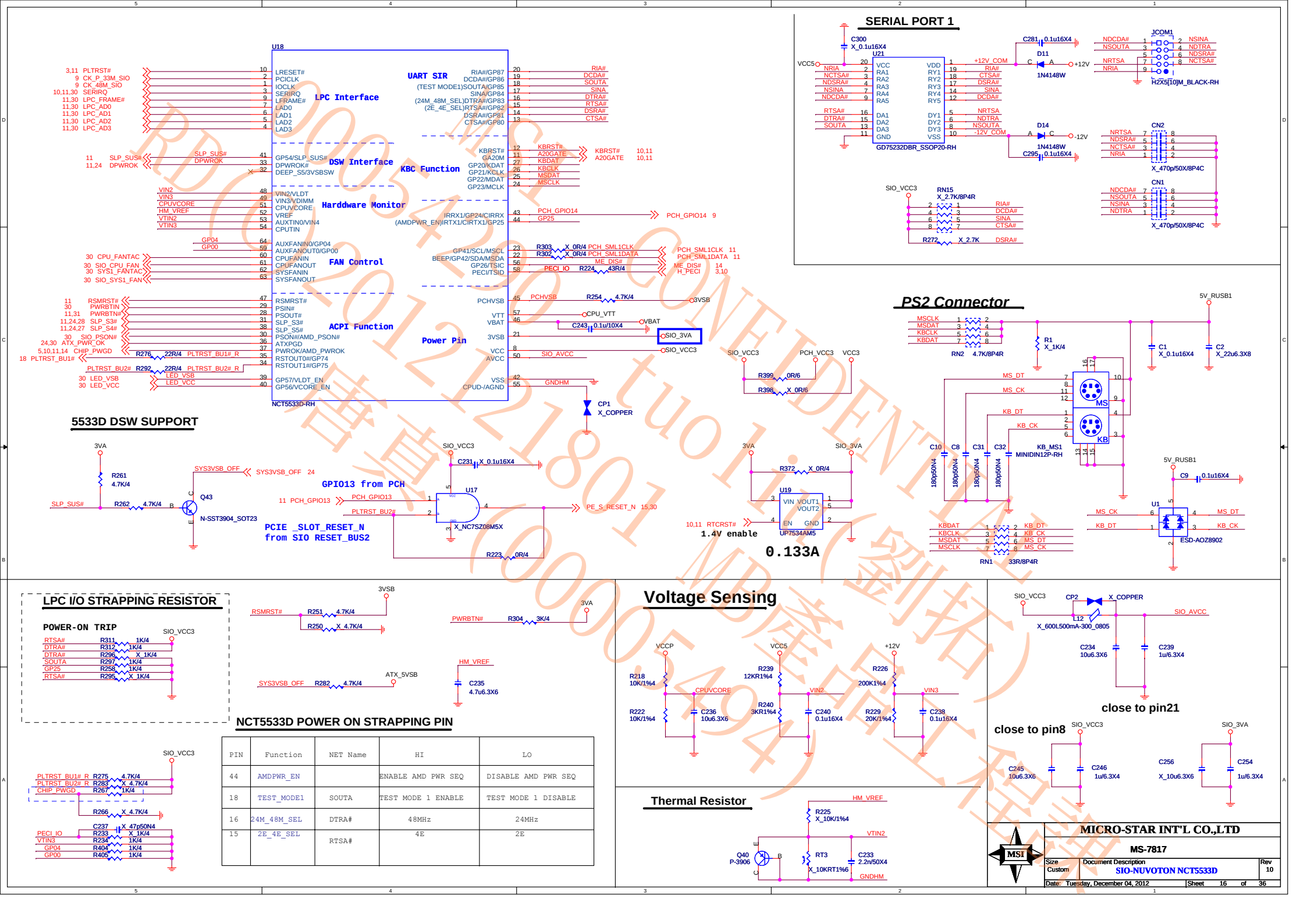
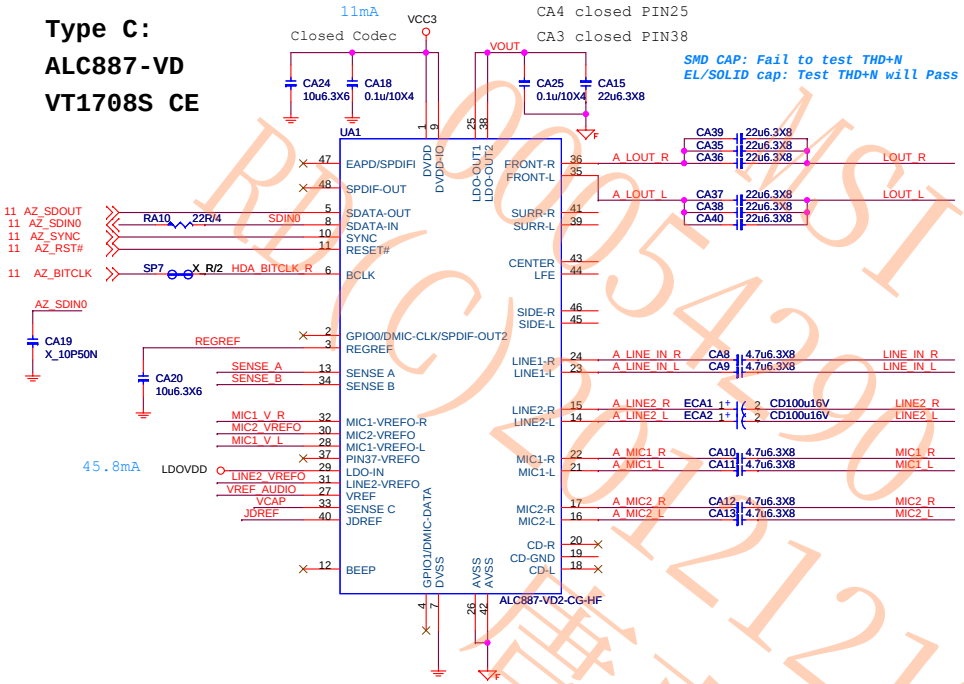
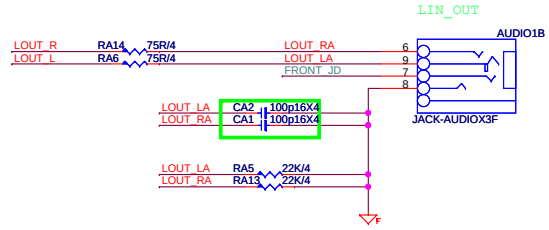
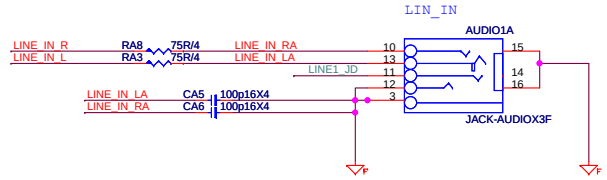


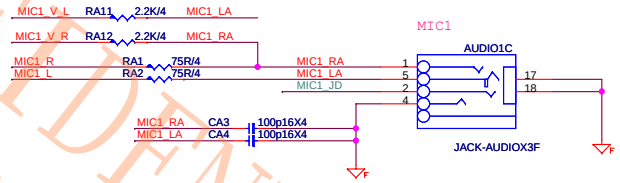
PIN	Function	NET Name	HI	LO
44	AMDPWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODE1	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

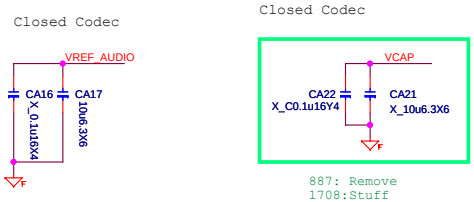
Type C:
ALC887-VD
VT1708S CE

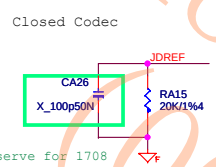


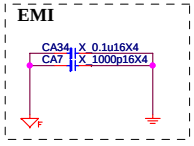


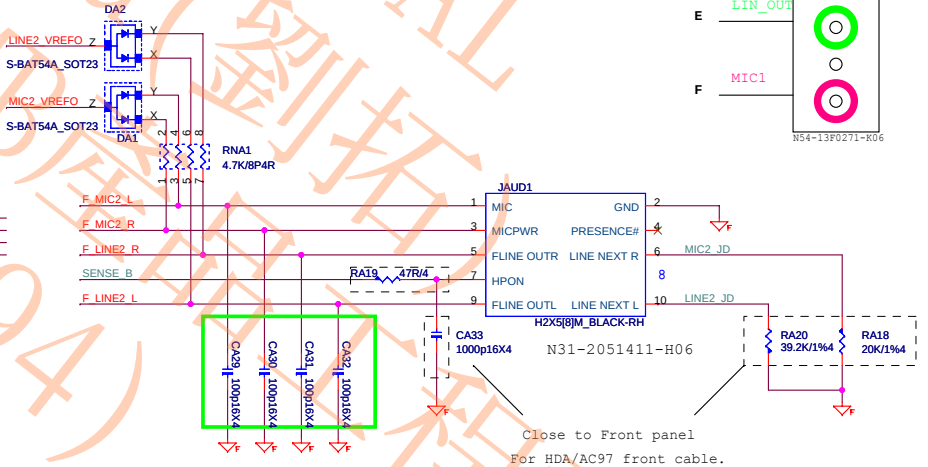


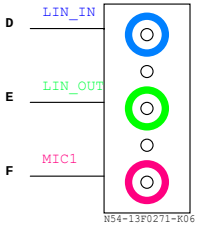


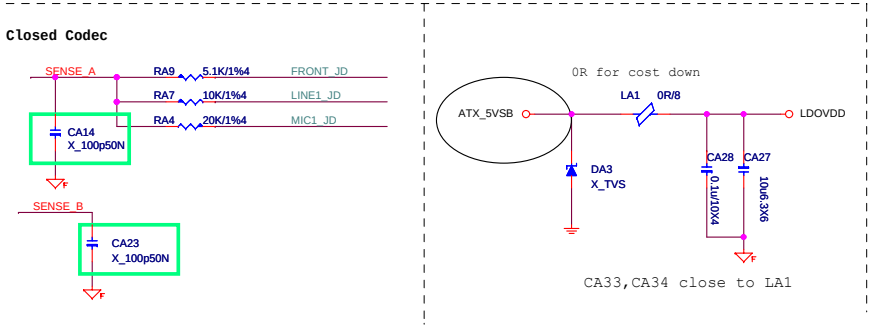












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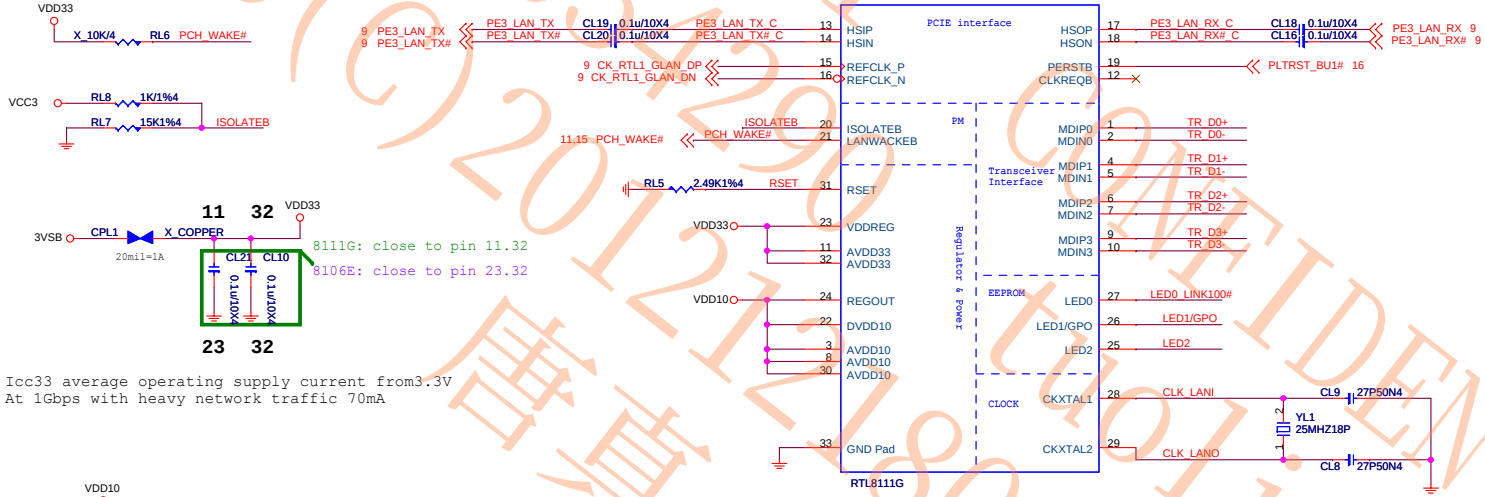
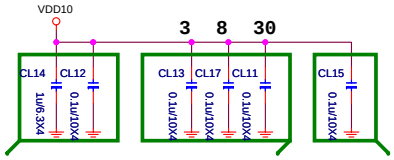
RTL8111G Giga LAN
RTL8106E 10/100M LAN



8111G: close to pin 11.32
8106E: close to pin 23.32

Icc33 average operating supply current from3.3V
At 1Gbps with heavy network traffic 70mA



22

8111G: close to pin 22
8106E: close to pin 30

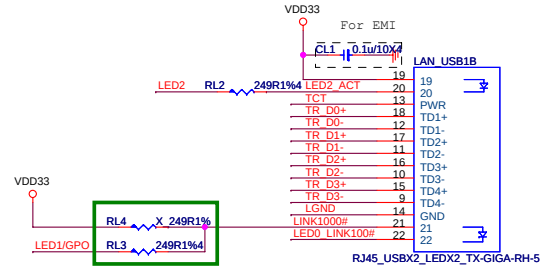
8111G: close to pin 3.8.30
8106E: close to pin 8.30

8111G: LDO mode close to pin 24
8106E: unstuff

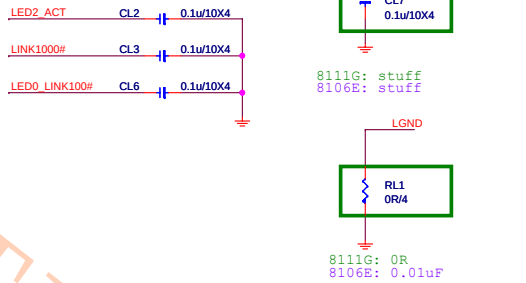
30

Icc10 average operating supply current from1.0V
At 1Gbps with heavy network traffic 300mA

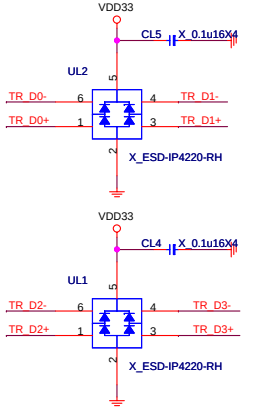
LAN Connector



8111G: Keep RL6 and Remove RL5 for RTL8111G
8106E: Keep RL5 and Remove RL6 for RTL8106E
Support R>= 249 ohm Resister For Single Color LED.
Support R>= 125 ohm Resister For Dual Color LED.



Reserve ESD Protect



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7817	
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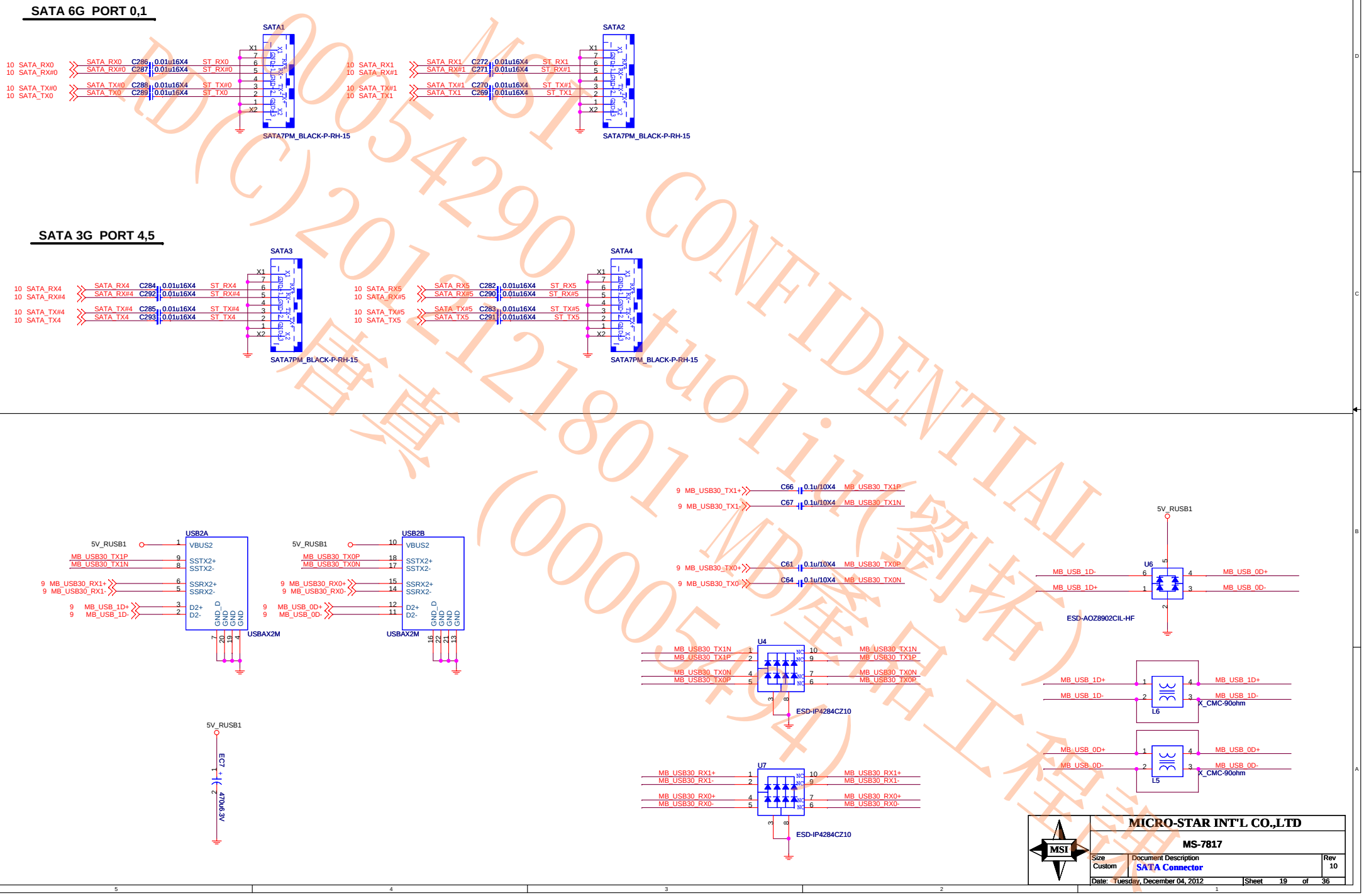
SATA 6G PORT 0,1
SATA1
SATA2
SATA7PM_BLACK-P-RH-15
SATA 3G PORT 4,5
SATA3
SATA4
USB2A
USB2B
USBAX2M
5V_RUSB1
ESD-IP4284CZ10
ESD-AOZ8902CIL-HF
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SATA Connector
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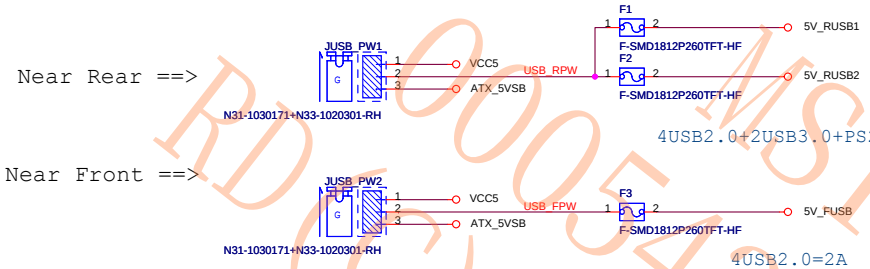
Type C: jumper +Fuse

PCH/FCH side: OC# pull high to +3VSB

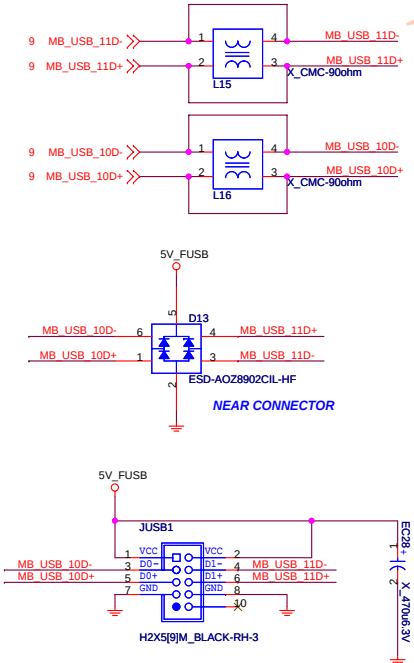


Default VCC5 (PIN1-2)

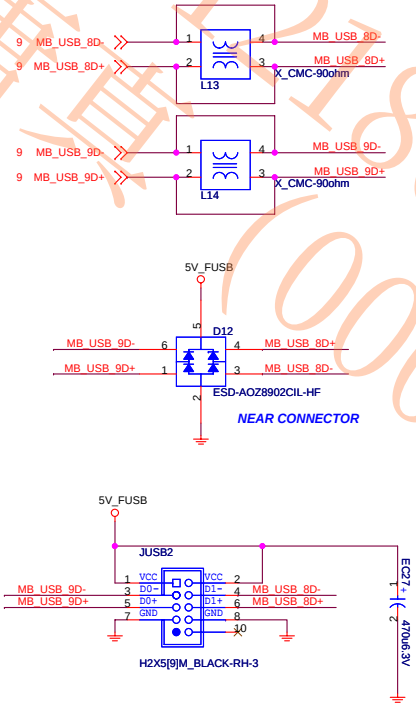
JUSB_PW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	
2-3	EUP Enable	Not support
	EUP Disable	support

D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

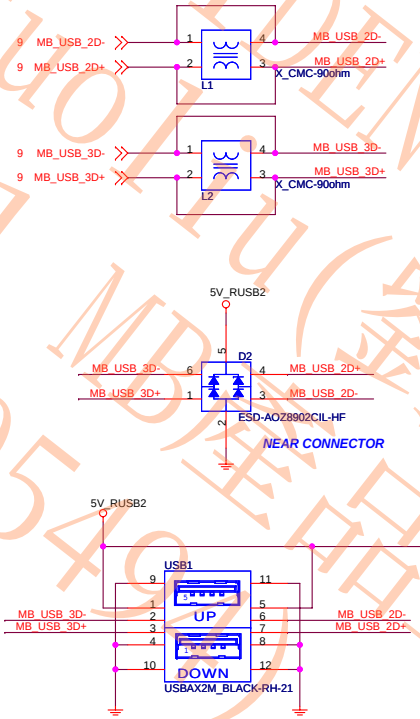
FRONT USB PORT 8,9



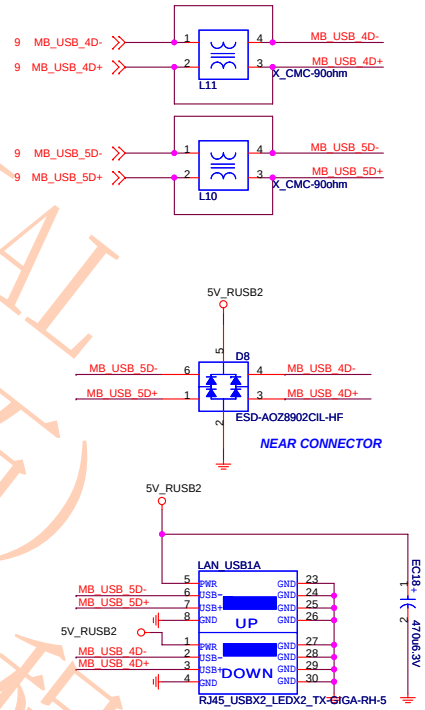
FRONT USB PORT 10.11



FRONT USB PORT 10.11



FRONT USB PORT 10.11



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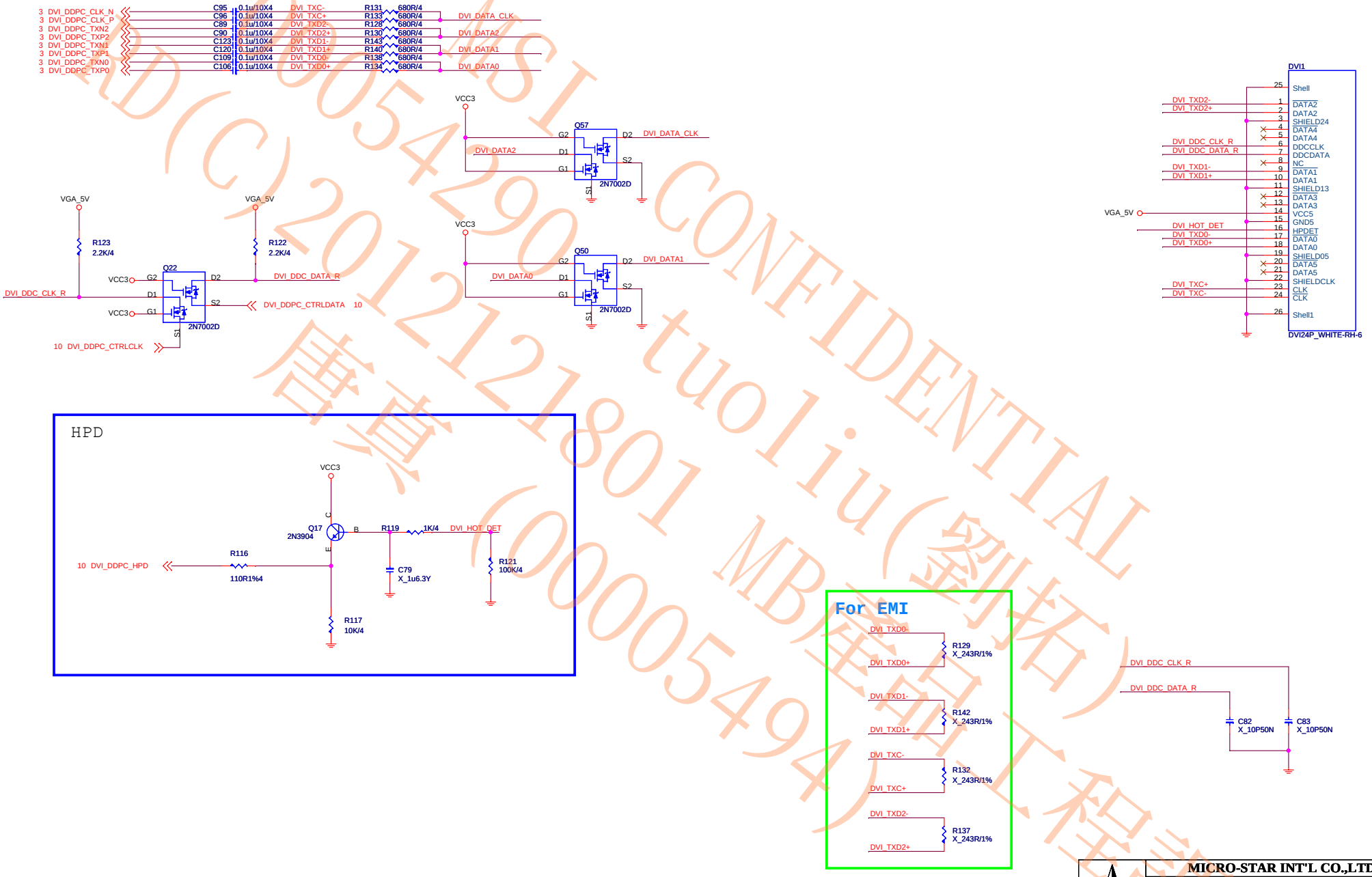
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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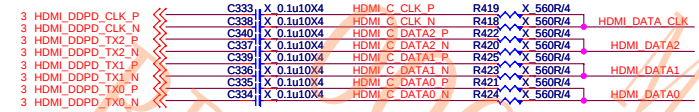
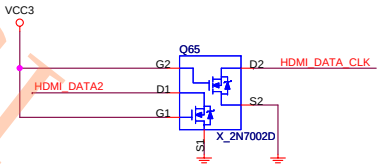
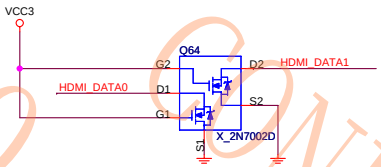
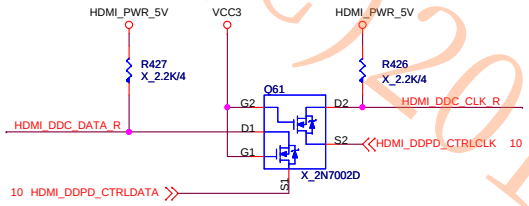
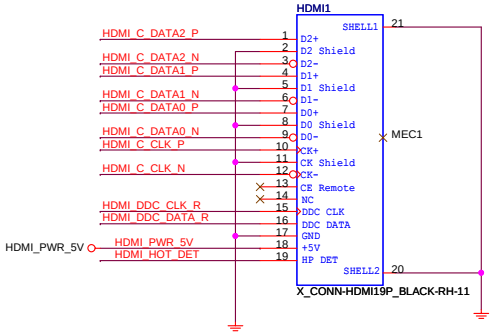
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

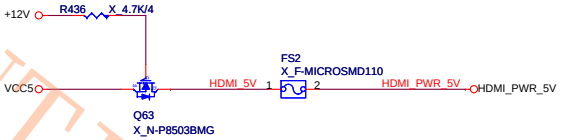


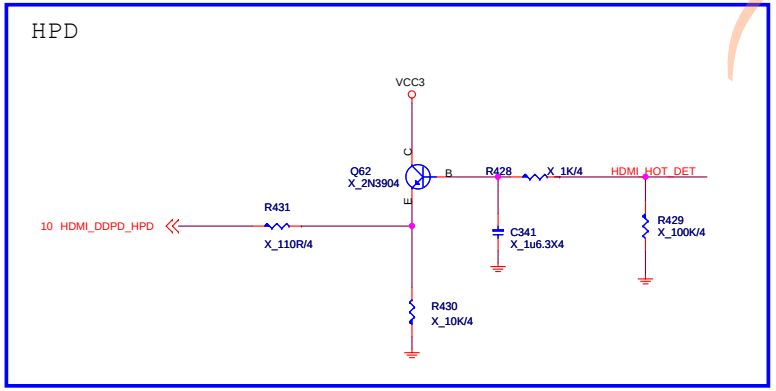


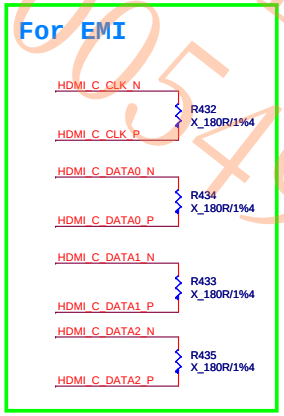


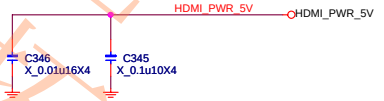




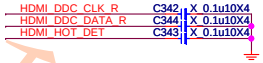








EMI



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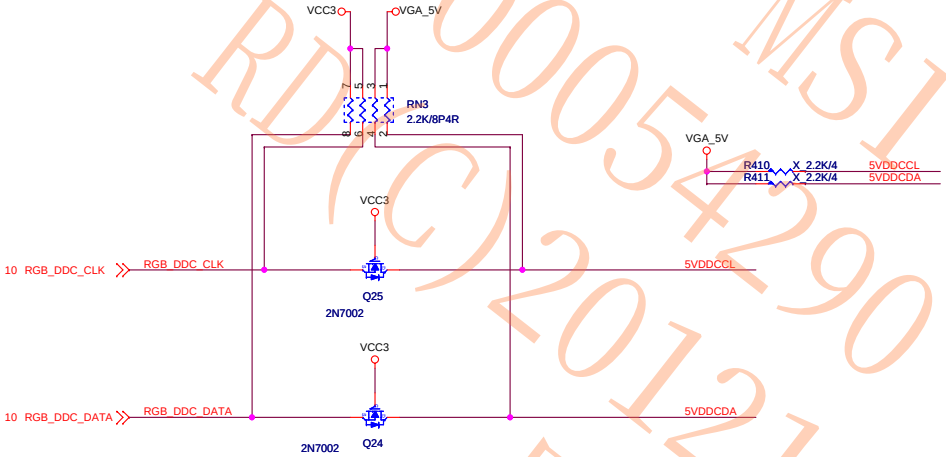
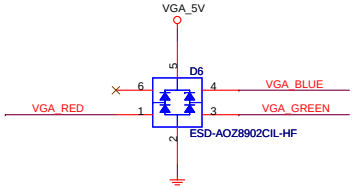
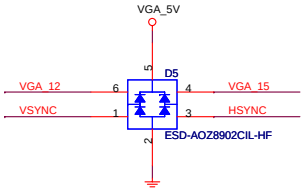
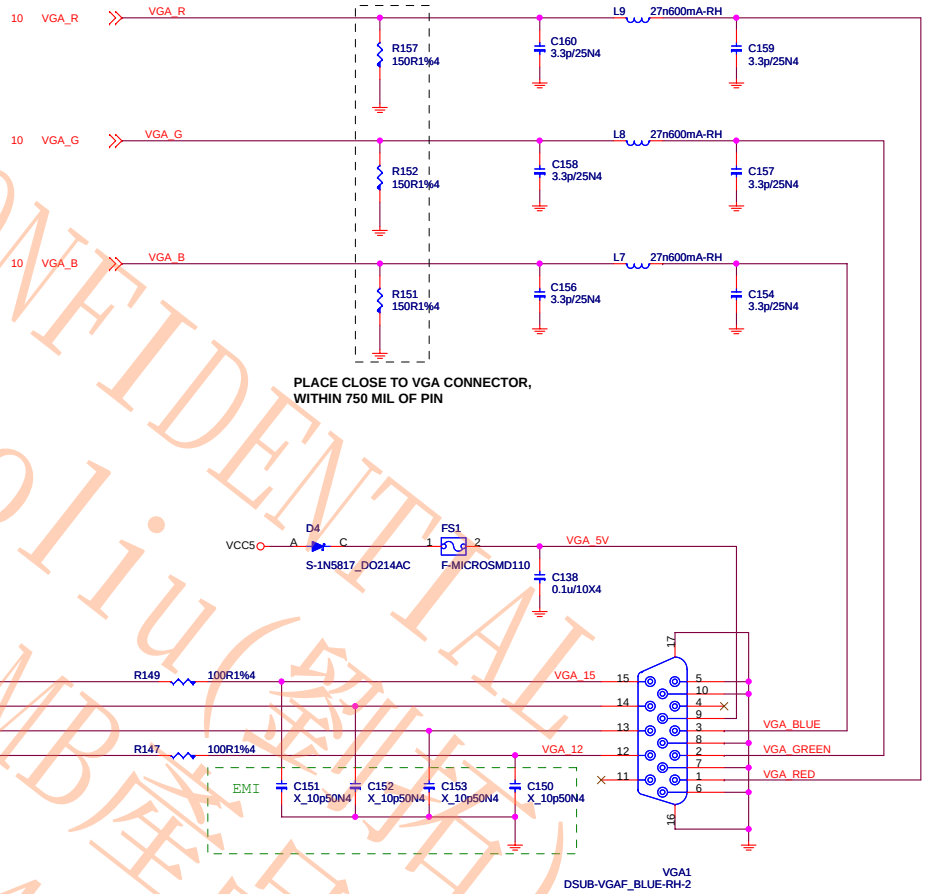
D-Sub

Level shift









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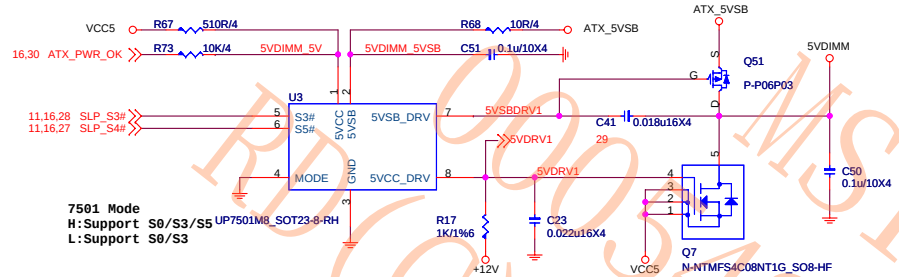
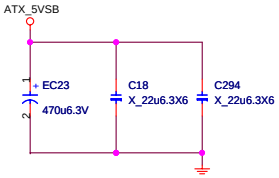
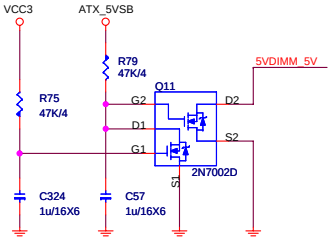
5VDIMM FOR DDR





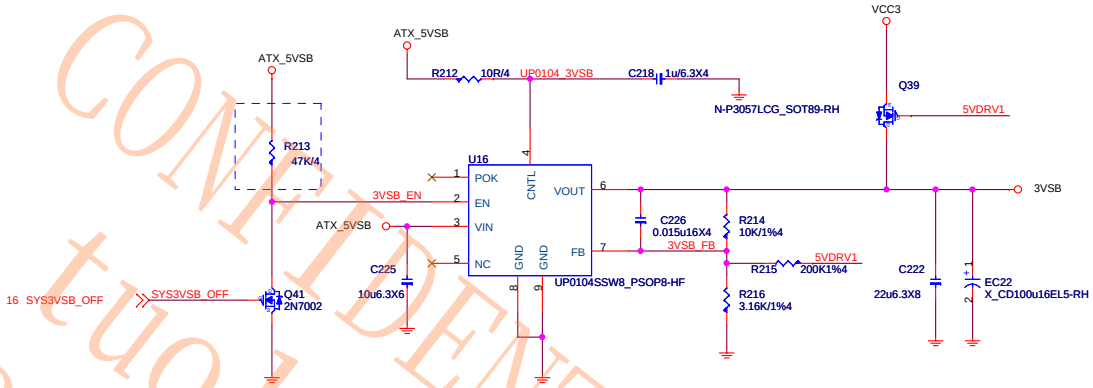
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



Patch coolermaster 700w power sequence

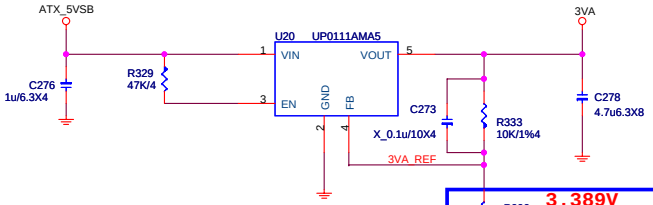
3VSB

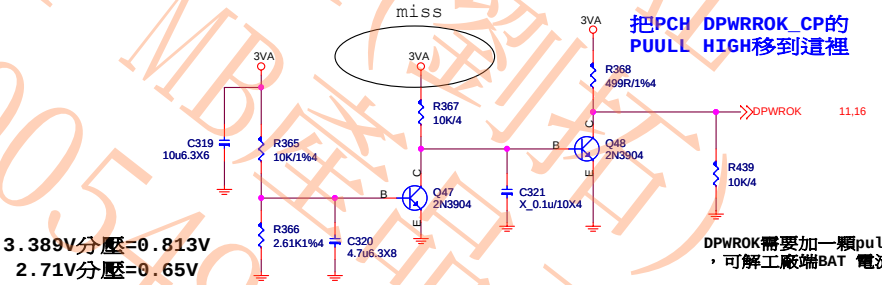
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



3VA

20mA





3.389V分壓=0.813V
2.71V分壓=0.65V

DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題

FOR DPWROK跟3VA的POWER
DOWN的時序(S5-->G3)

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VCORE power on by s3 and 12v

HIGH:0.7V
LOW:0.3V

+12VIN
R29 9.1KR1%4
VRD_EN
28 SLP_S3_CTRL
Q4 2N7002
R26 1K/1%4
C17 X_0.1u16X4
28 PCH1P05_CTRL
Q5 2N7002

CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT

VCCP
3VSB
VCC3
R9 1K/4
R7 10K/4
R19 4.7K/4
VRM_PGD_R
R10 4.7K/4
Q1
NN-CMKT3904
R18 100K/4
VRM_PGD 11,31
C16 100p16X4
R293 X_0R/4
VRM_PGD_R
28 SLP_S3_CTRL
Q2 2N7002
CRB

CPU_VTT
VID_ALERT# R35 X_110R/1%4
H_VIDSCLK R36 54.9R1%4
H_VIDSOUT R38 110R1%4
C28 1u/6.3X4

VCC5
+12VIN
R53 2.2R/8
V95812
C38 0.1u16X4
R61 2.2R/8
C42 0.1u16X4
R63 2.2R/8
C45 0.1u16X4

U2
VDD
VIN
3 VID_ALERT#
3 H_VIDSOUT
3 H_VIDSCLK
ALERT#
SDA
SCLK
VRM_PGD_R
VRD_EN
VR_HOT#
PGOOD
VR_ON
VR_HOT#
3 H_PROCHOT#
R25 0R/4
R5 9.1K/1%4
C4 2200p50N4
C14 33p/50N4
COMP
VCCP
C3 2200p50N4
R16 2.2KR1%4
C6 220p50N4
R15 3.83KR1%4
R30 3.4KR1%4
R22 100R1%4
FB
3 CPU_VCC_SENSE
C21 X_330p50N
R378 8.06KR1%4
SLOPE
C5 X_1000p16X4
3 CPU_VSS_SENSE
C22 X_330p50N/4
R31 100R1%4
RTN
C15 0.022u16X4
R8 95.3KR1%4
R45 42.2K/1%4
R49 21KR1%4
R48 3.24KR1%4
IMON
PROG1
PROG2
PROG3
THERMAL PAD
ISL95812HRZ-T_QFN32-HF

VDDP
BOOT1
BO1
R62 0R/8
C44 0.22u16X4
PHASE1
VCORE_PHASE1 26
UGATE1
VCORE_UG1 26
LGATE1
VCORE_LG1 26
BOOT2
BO2
R56 0R/8
C40 0.22u16X4
PHASE2
VCORE_PHASE2 26
UGATE2
VCORE_UG2 26
LGATE2
VCORE_LG2 26
PWM3
R57 0R/4
V95812
ISEN1
ISEN2
ISEN3
ISPHASE1_R
ISPHASE2_R
R21 10K/1%4
R32 10K/1%4
ISPHASE1 26
ISPHASE2 26
ISUNP
ISUMN
VSUMP
R20 3.65K/1%4 ISPHASE1
R41 3.65K/1%4 ISPHASE2
R446 X_2MR/4
NTC
RT2 100KRT1%4
R24 24.9K/1%4
R13 11.5KR1%4
R39 866R1%4
C25 X_330p50N4
R37 X_110R1%4
C29 0.1u16X4
C33 0.33u6.3X4
C34 0.33u6.3X4
R47 11KR1%4
R50 2.26KR1%4
RT1 10KRT1%4
VSUMN

OCP=110A

ISPHASE1_R
R33 10K/1%4
ISVCORE2
ISVCORE2 26
C11 0.22u16X4
VSUMN
R23 X_20KR1%4
R14 2.2R/4
ISVCORE1
ISVCORE1 26

ISPHASE2_R
R6 10K/1%4
ISVCORE1
C7 0.22u16X4
VSUMN
R12 X_20KR1%4
R42 2.2R/4
ISVCORE2

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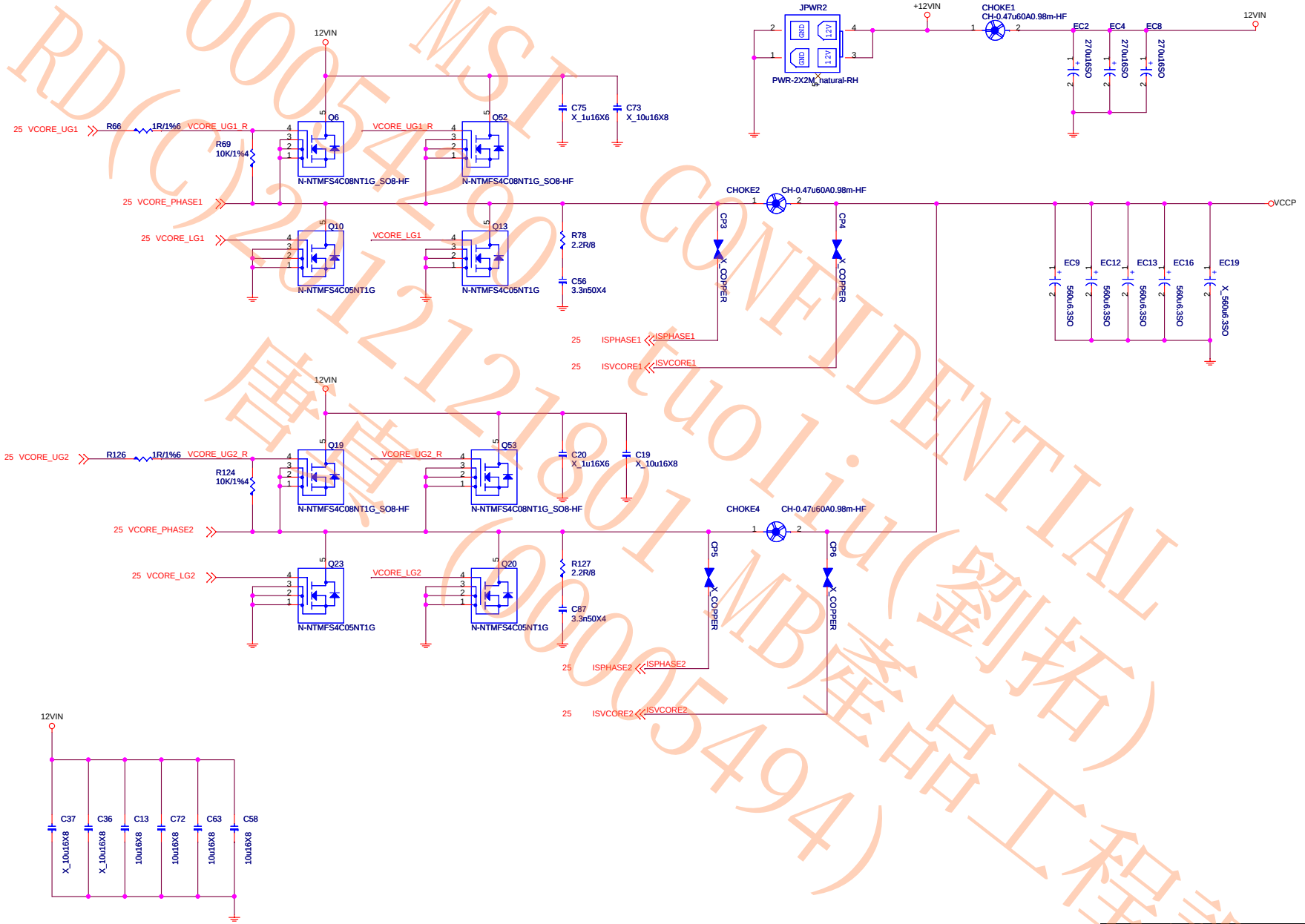
VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm



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DDR Power:1.5V

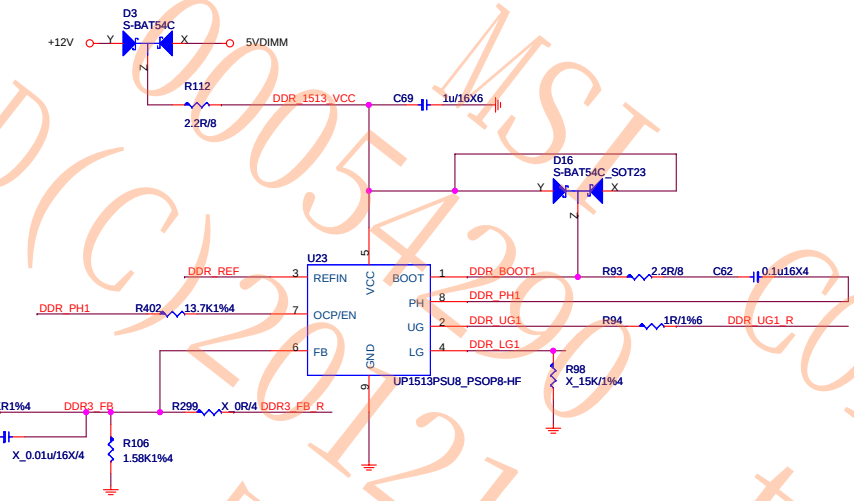
DDR3_1.5V 4.2A+6A+0.5A+7.661=18.361A

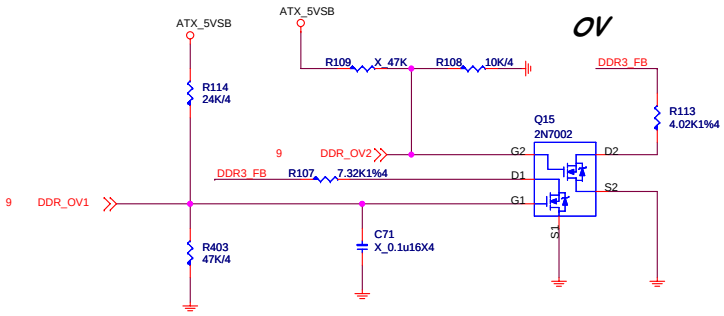
OCP:66.7A

4.2A FOR CPU
6A FOR 2DIMM
0.5A FOR DDR VTT
7.661A FOR PCH

OCP:16.447*1.5=24.6705A
OCPXRdson(Low side)=(40uA*Rocs(R122)-0.4V)
Rocs(R122)=13.75K

2012.03.22 Modify Pull hi (47K)to ATX_5VSB

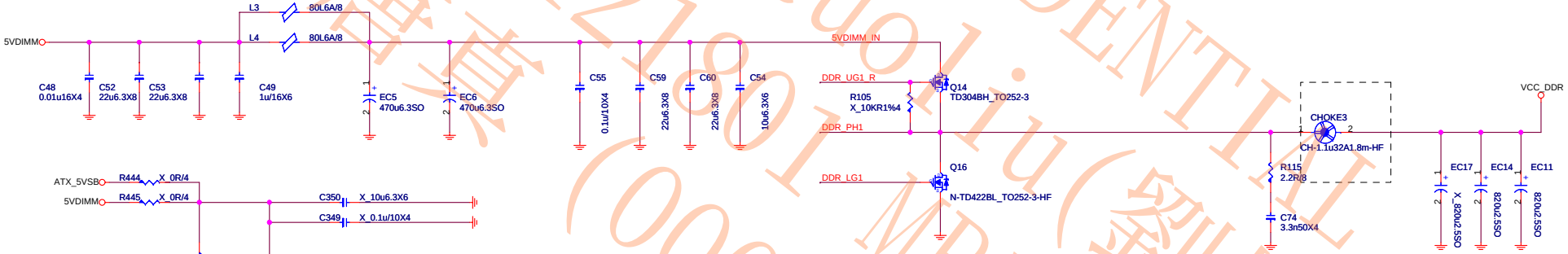


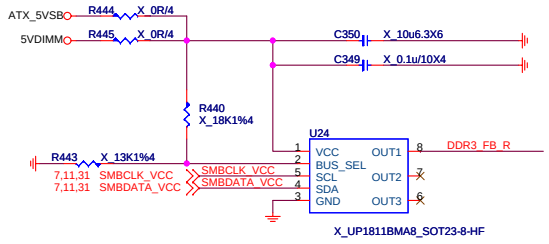


*Default 1.5V

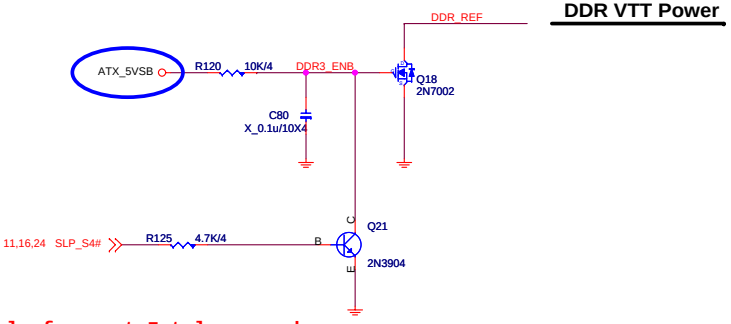
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)





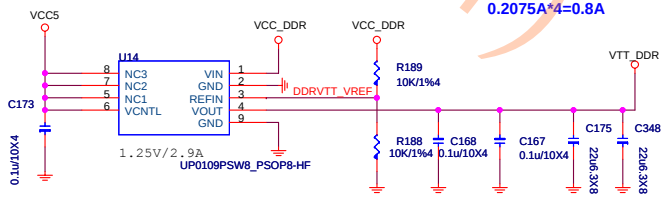
DDR VTT Power

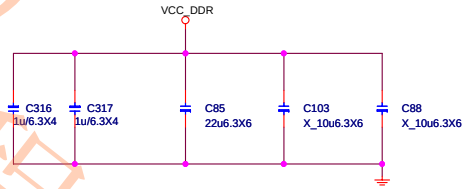


P.S. Only for meet Intel power down sequence.

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A





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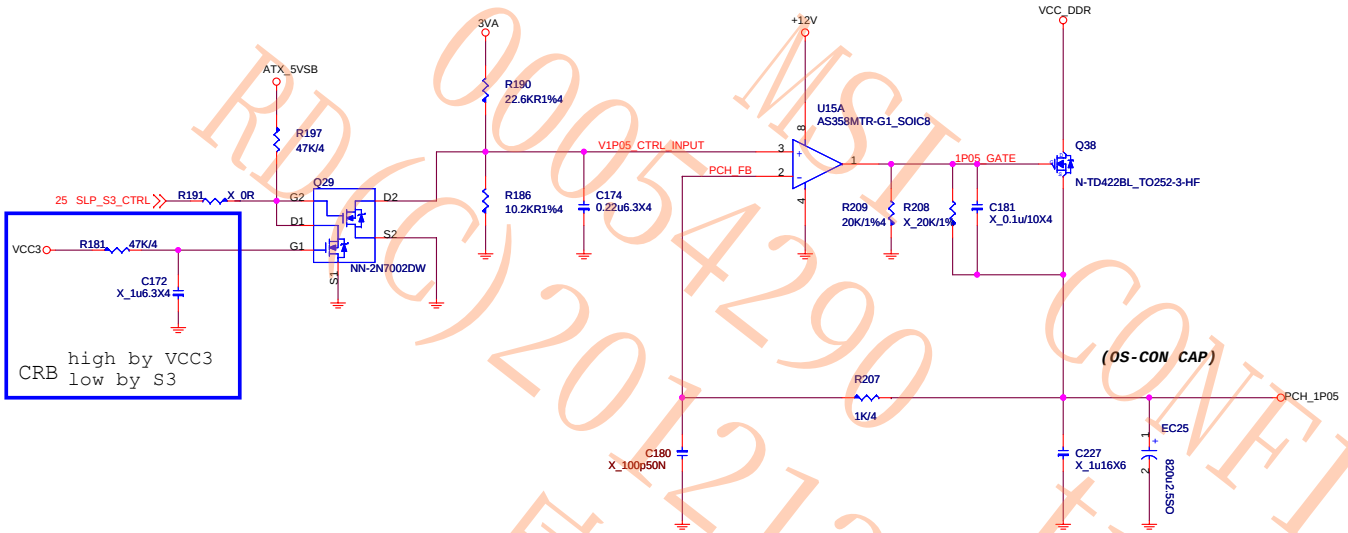
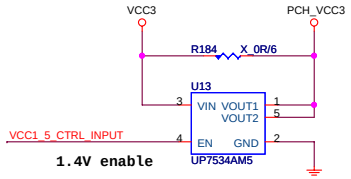
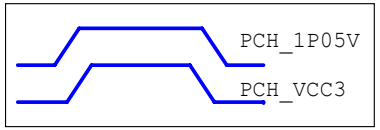
PCH Power:1.05V 5.747A

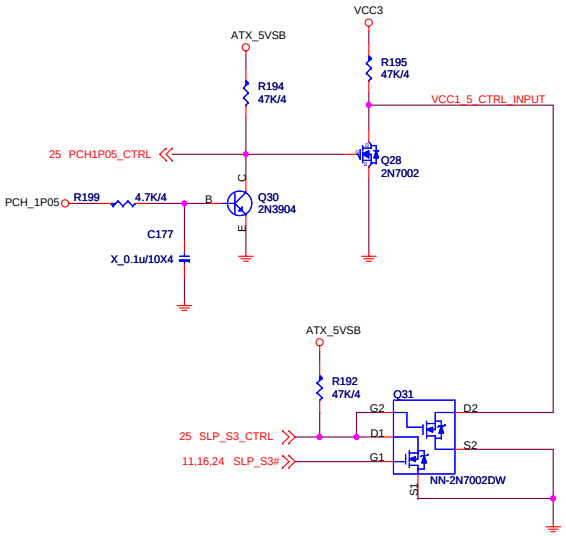


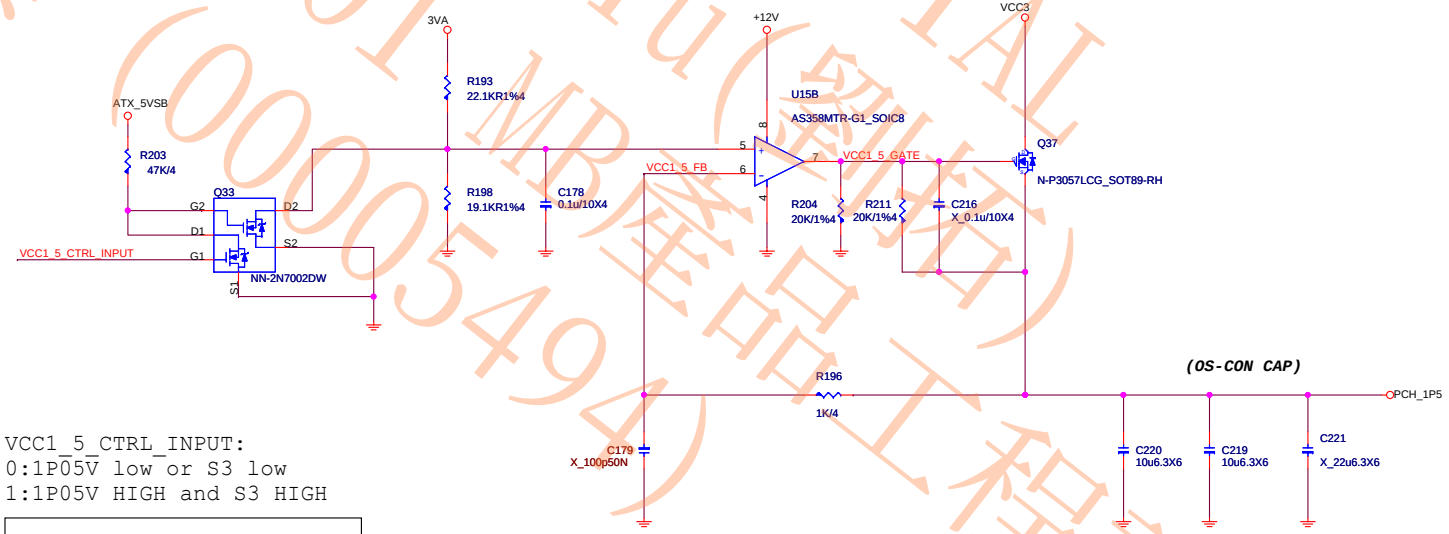
0.133A



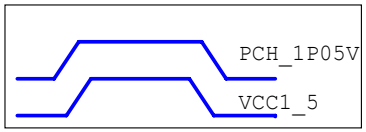


PCH Power:1.5V 0.183A





VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



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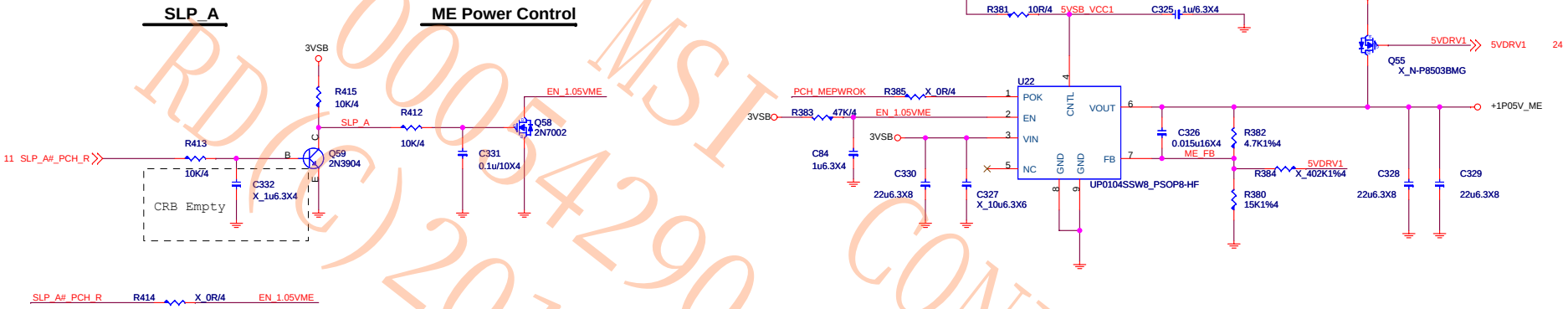
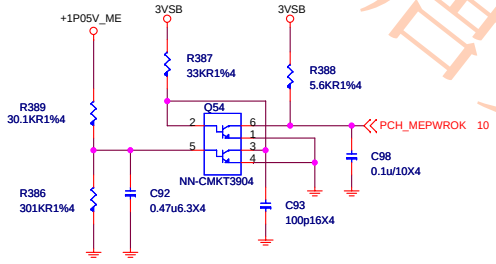
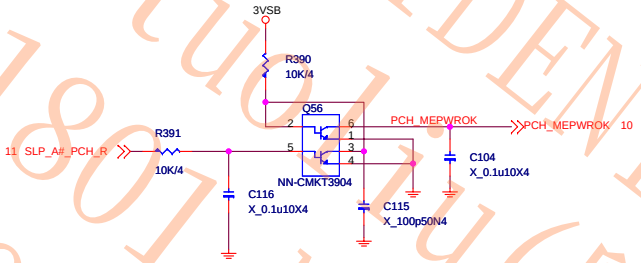
PCH ME Power:1.05V 0.670A



PCH_MEPWROK

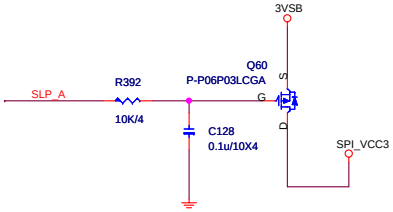


VccASW active to APWROK high 1ms



APWROK falling to VccASW falling 40ns

+3.3V_ME



+3.3V_ME

For INTEL ME

287->Stuff R366
H87->Stuff R354

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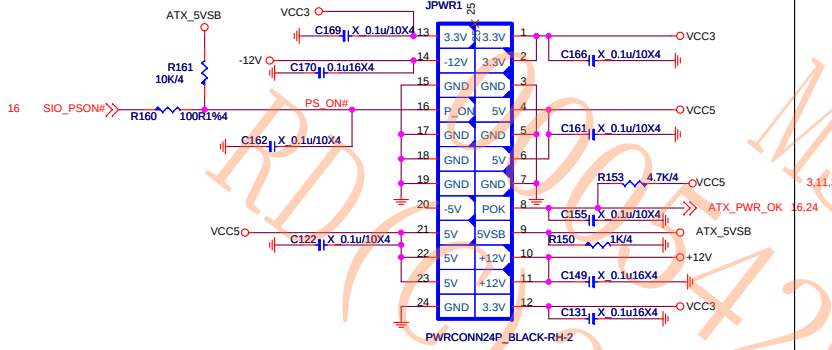
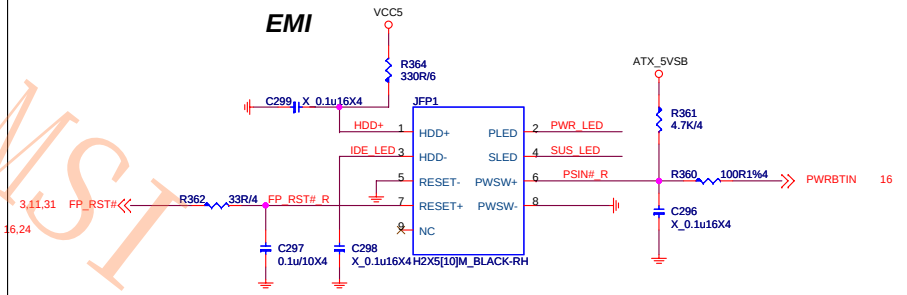
ATX POWER CONNECTOR

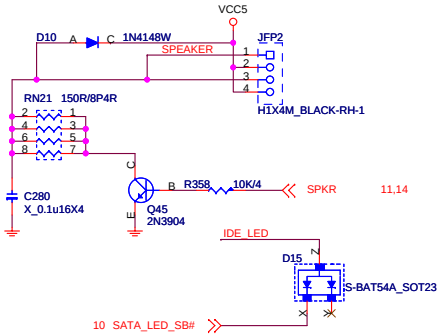


FRONT PANNEL

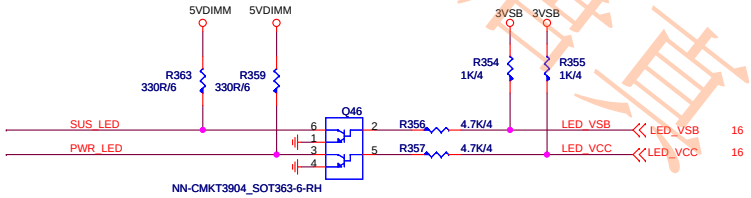
EMI



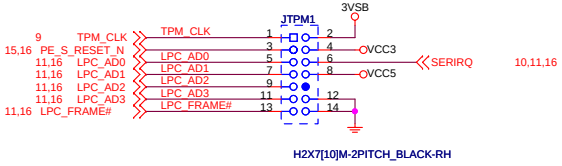
Speaker Pin Header



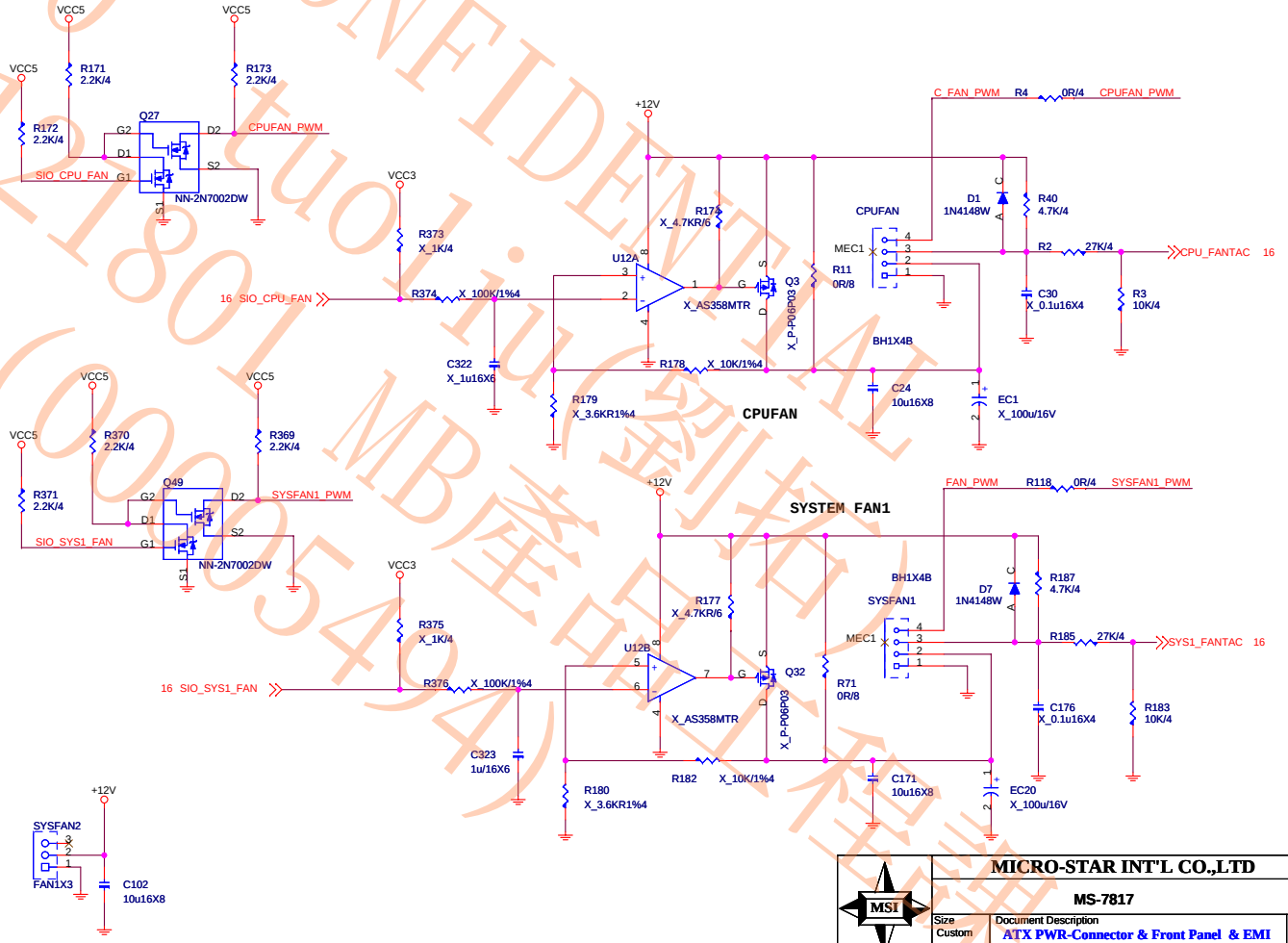
LED (for NV5533)



TPM/JLPC



FAN-COUNTROL CIRCUIT



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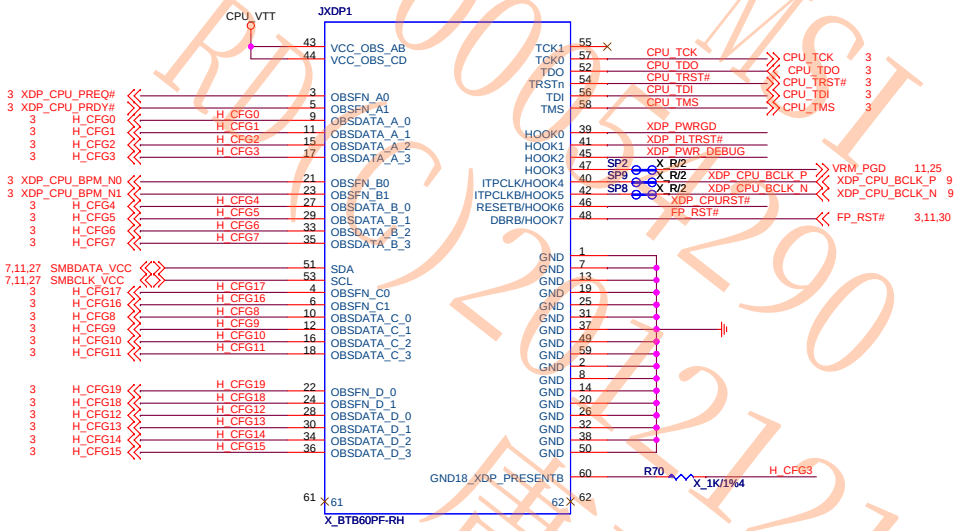
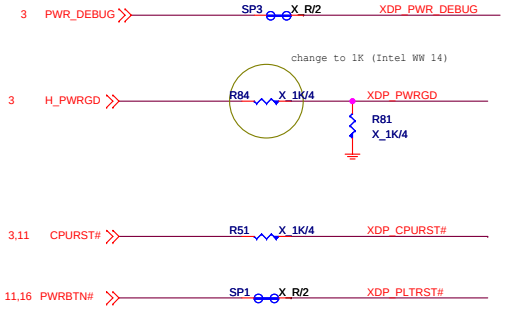
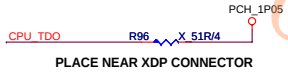
Reserve debug port 5020







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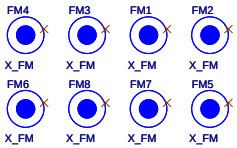
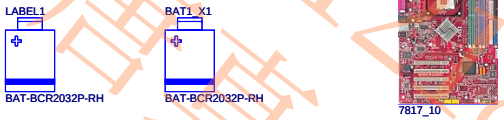
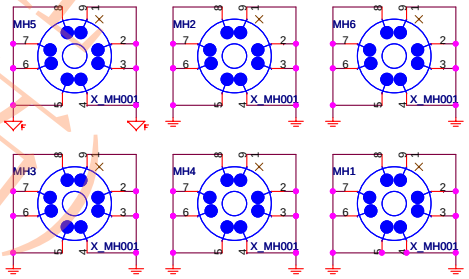
Optical Fiducial Marks-120



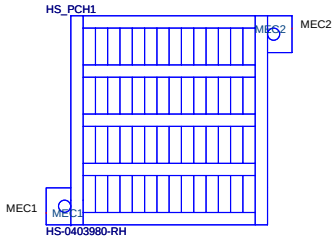


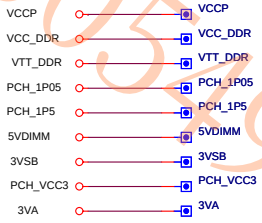
Simulation

Mounting Holes



PCH XDP PWRGD/RESET





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