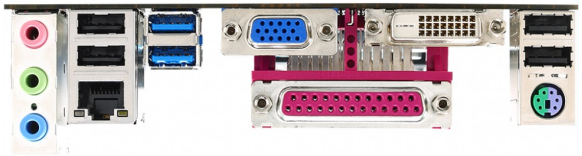
MS-7846

mATX

Ver: 2.1

Intel Sharkbay plamform H81 COLAY B85 H87



CPU:

INTEL-Haswell LGA1150

System Chipset:

H81,B85,H87

Memory:

*DDRIII (1333/1666MHz) * 2 (Dual Channel)*

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-realtek8111G

SIO:NUVOTON 6779D

SPI ROM: 64 MB & 128MB

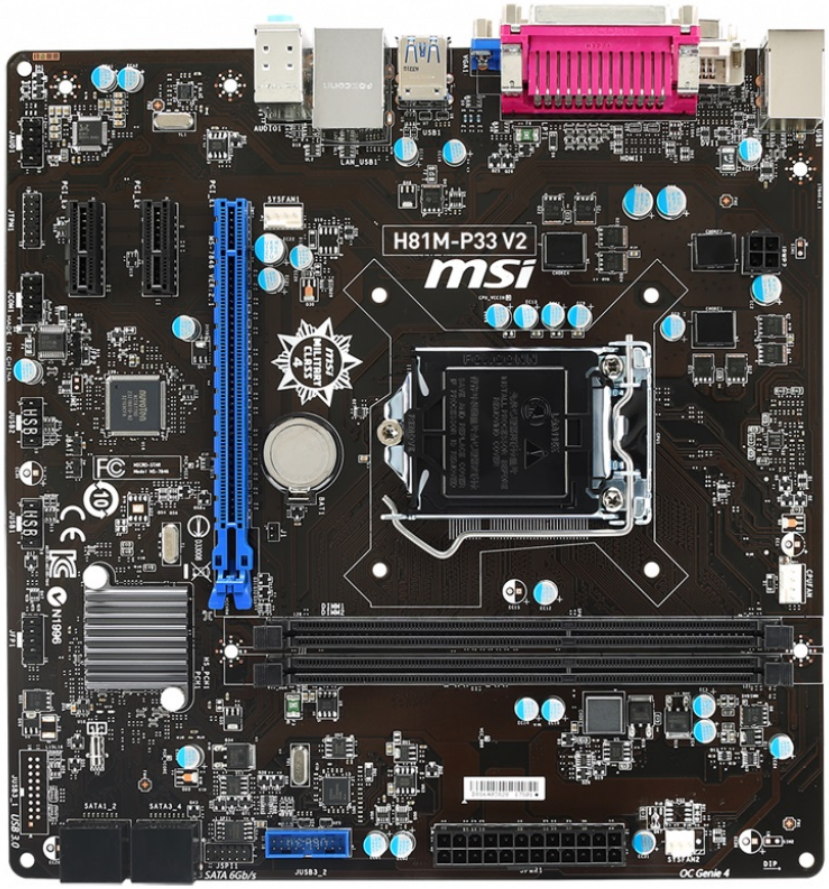
Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

Other:

*VGA*1*
*SATA2*2*
*SATA3*2*
*FRONT USB2.0 *4*
*FRONT USB3.0 *2*
*REAL USB2.0 *2*
*REAL USB3.0 *2*
*PS2*1*
*FRONT COM PORT*1*
*REAL PRINT PORT*1*



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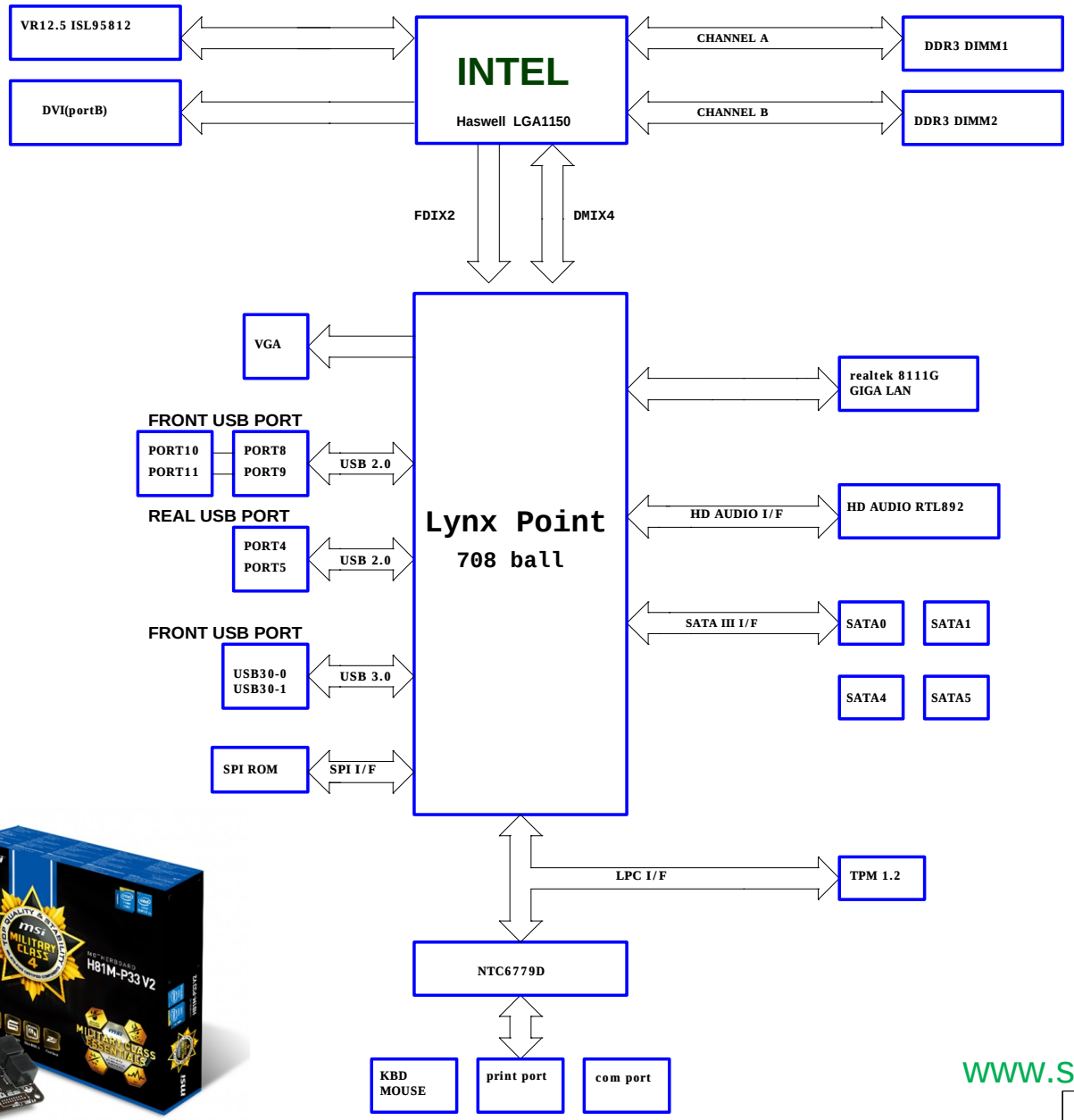
MS-7846 Block Diagram



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Block Diagram	2.1

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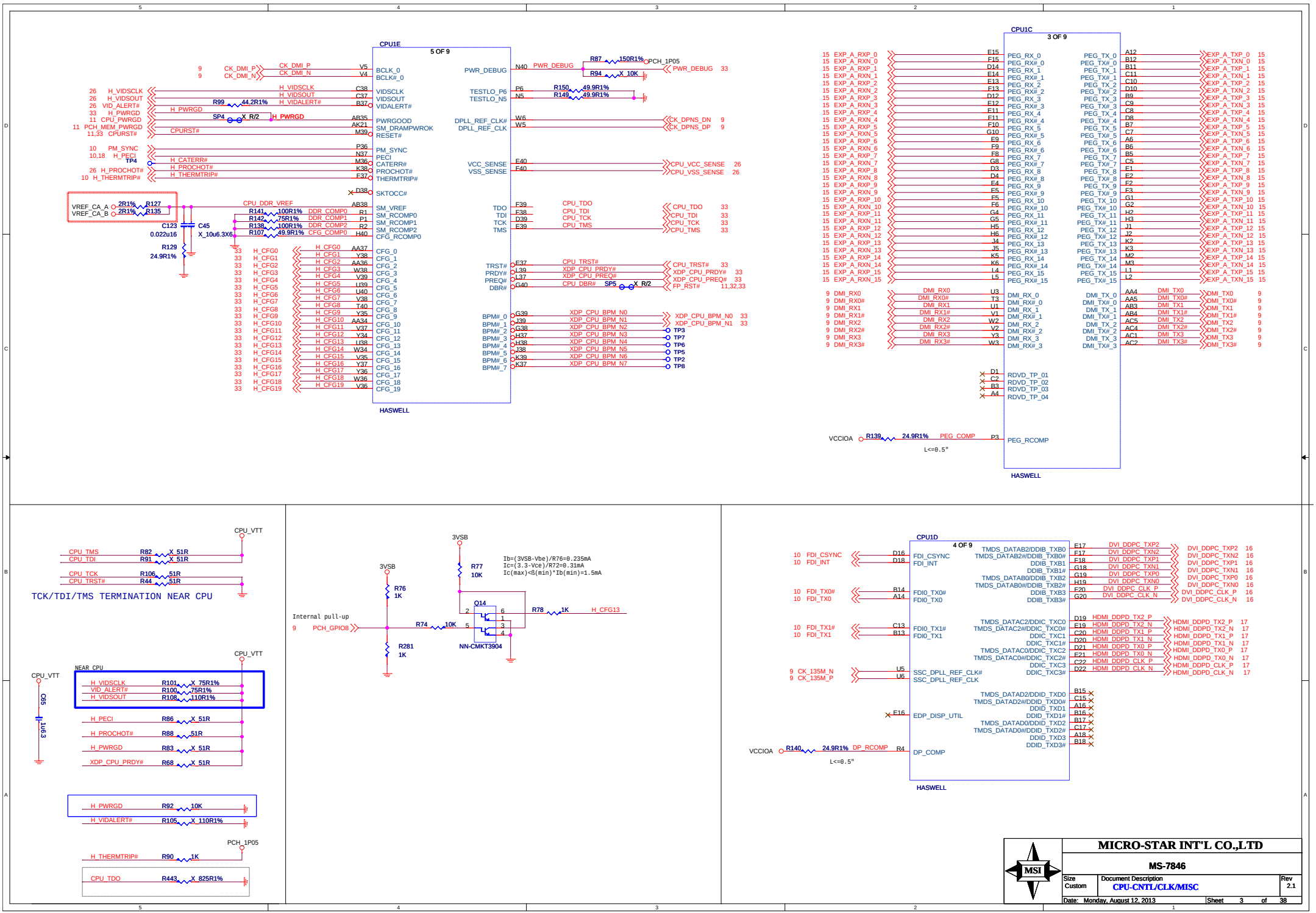
CPU1E
5 OF 9
HASWELL
CPU1C
3 OF 9
HASWELL
CPU1D
4 OF 9
HASWELL
TCK/TDI/TMS TERMINATION NEAR CPU
NEAR CPU
Internal pull-up
NN-CMKT3904
MICRO-STAR INT'L CO.,LTD
MS-7846
CPU-CNTL/CLK/MISC
Size
Custom
Rev
2.1
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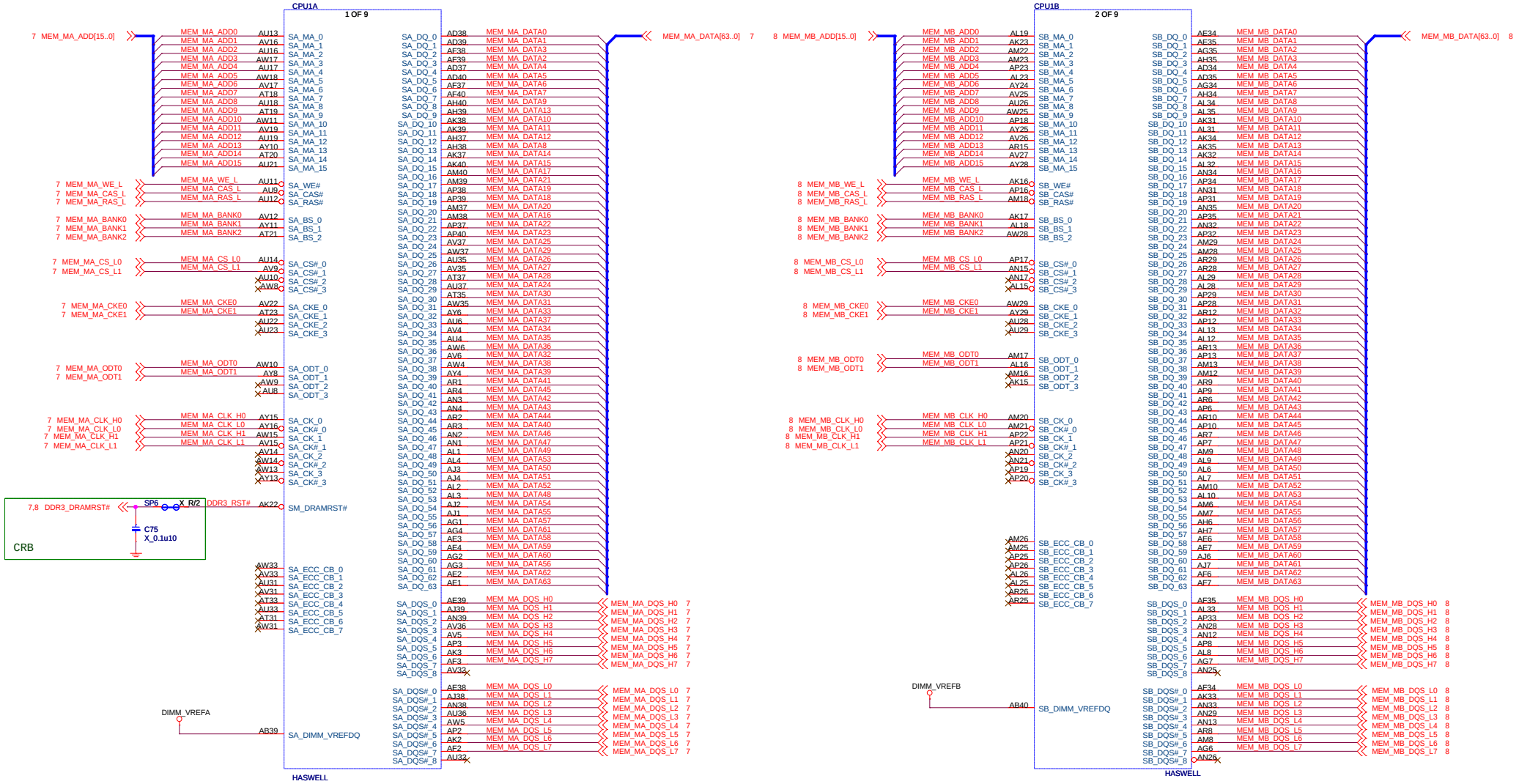

MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size: Custom	Document Description: CPU-Memory	Rev: 2.1
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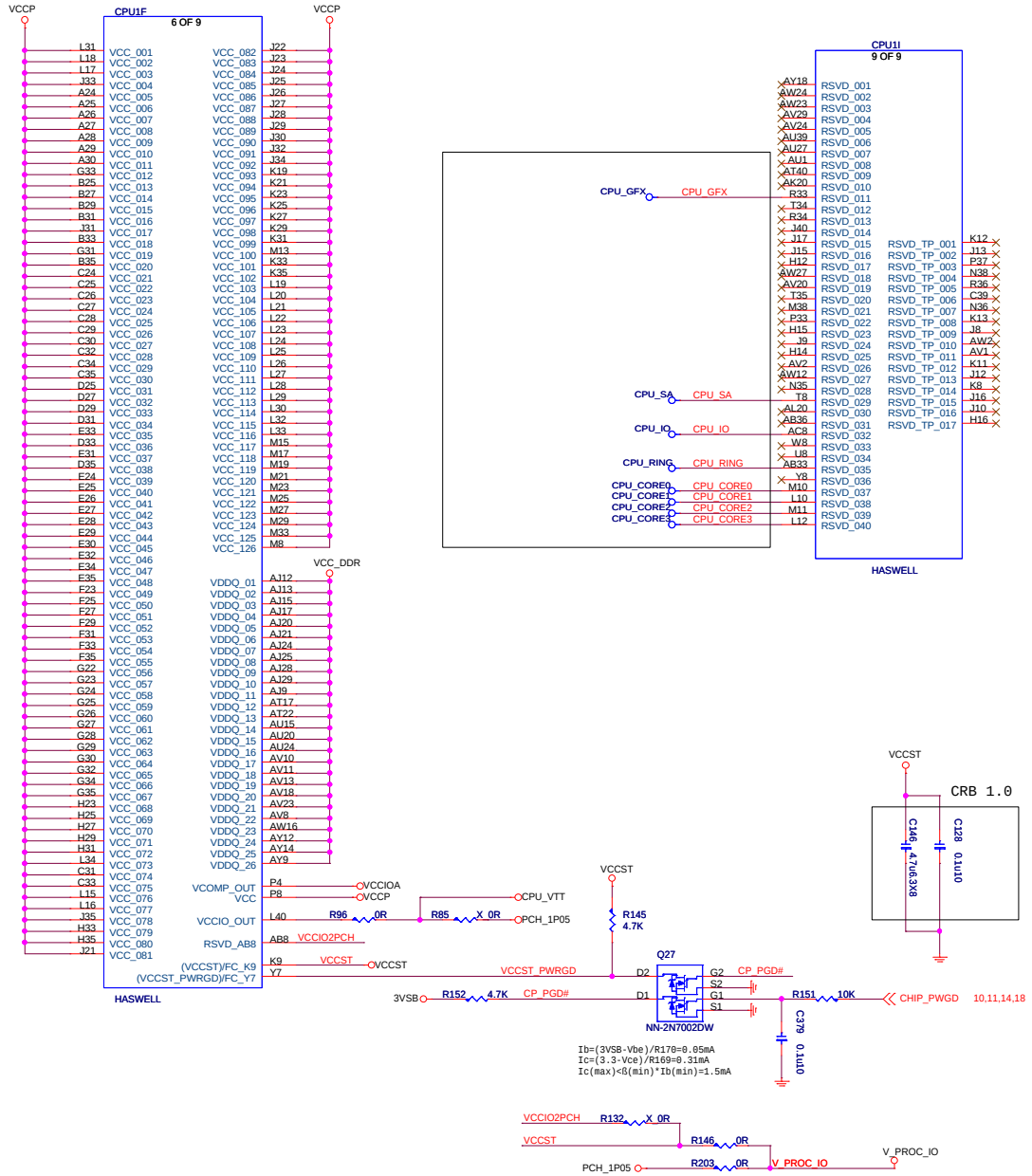
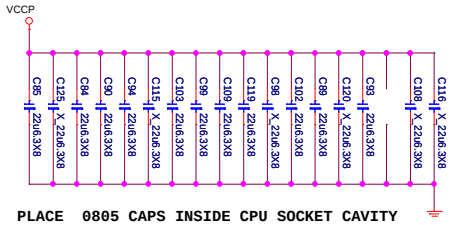
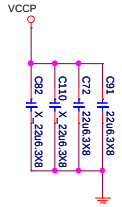


+CPU_VCCP-Decoupling

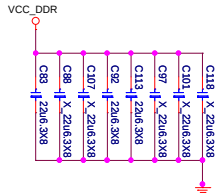


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

PLACE 0805 CAPS Near CPU SOCKET edge



+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS

MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size: Custom	Document Description: CPU-Power	Rev: 2.1
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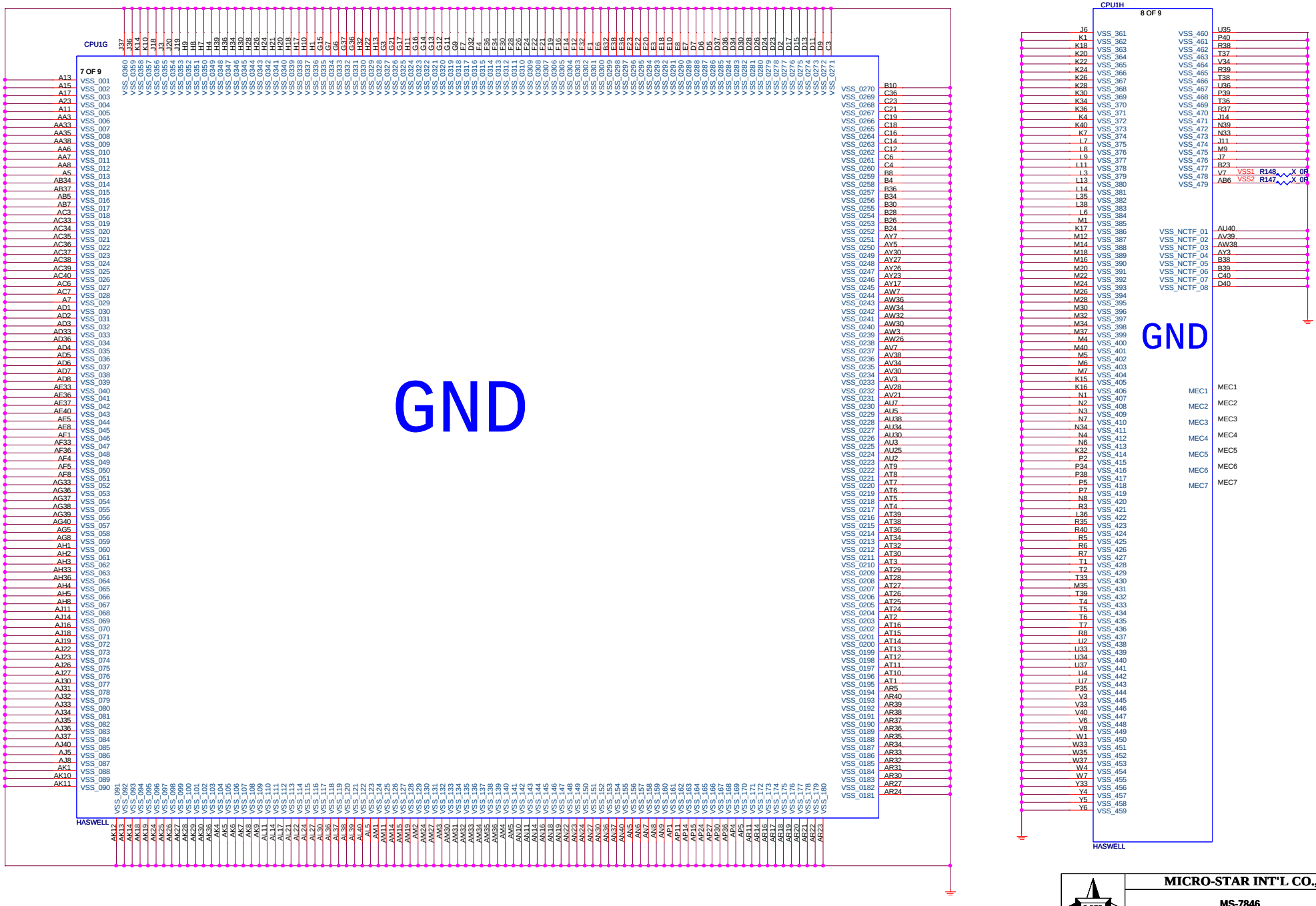
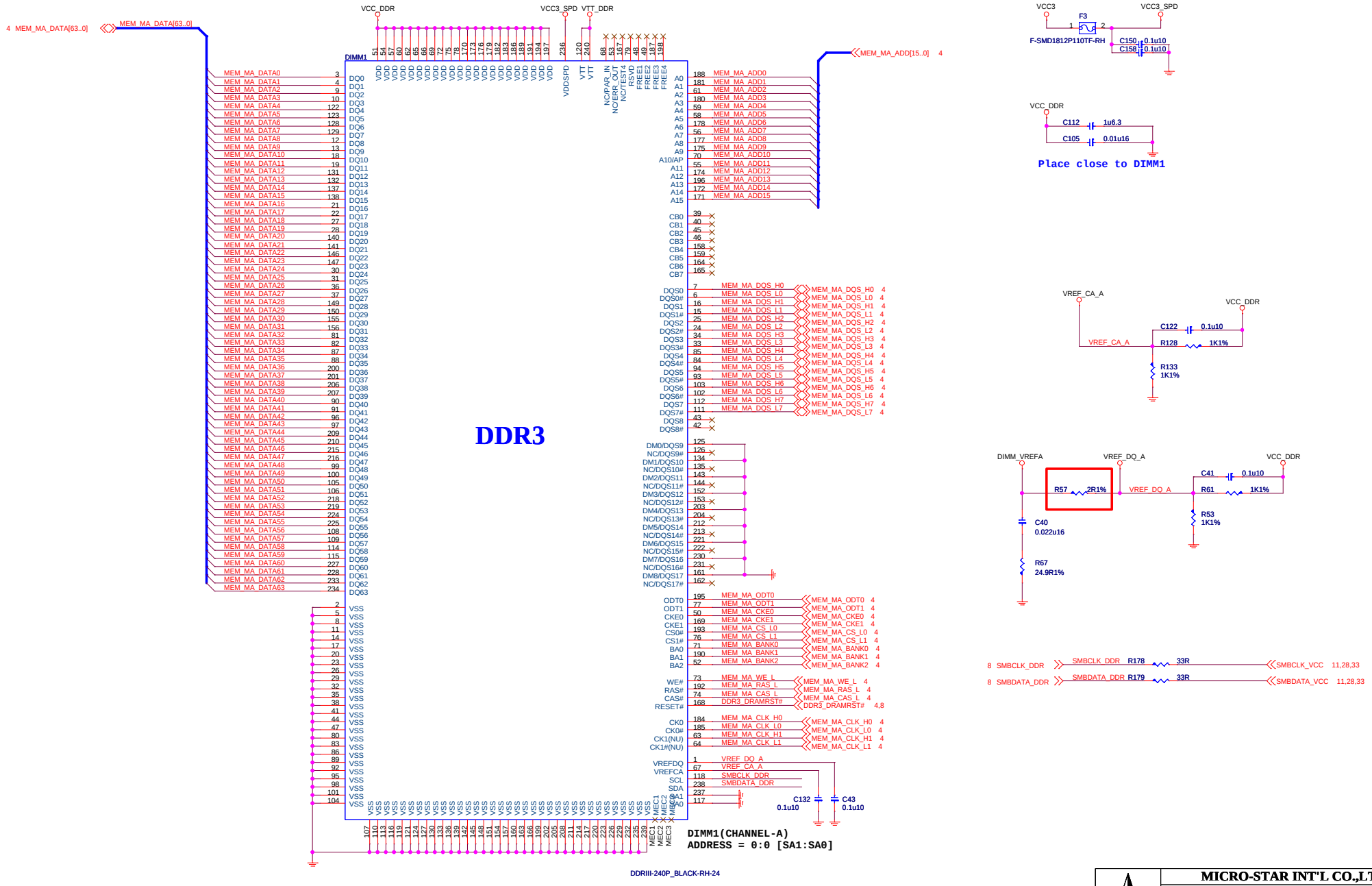


MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size: Custom	Document Description: CPU-GND	Rev: 2.1
Date: Monday, August 12, 2013	Sheet 6 of 38	



MICRO-STAR INT'L CO.,LTD	
MS-7846	
Size: Custom	Document Description: DDR3 Chanel-A DIMM1/2
Rev: 2.1	
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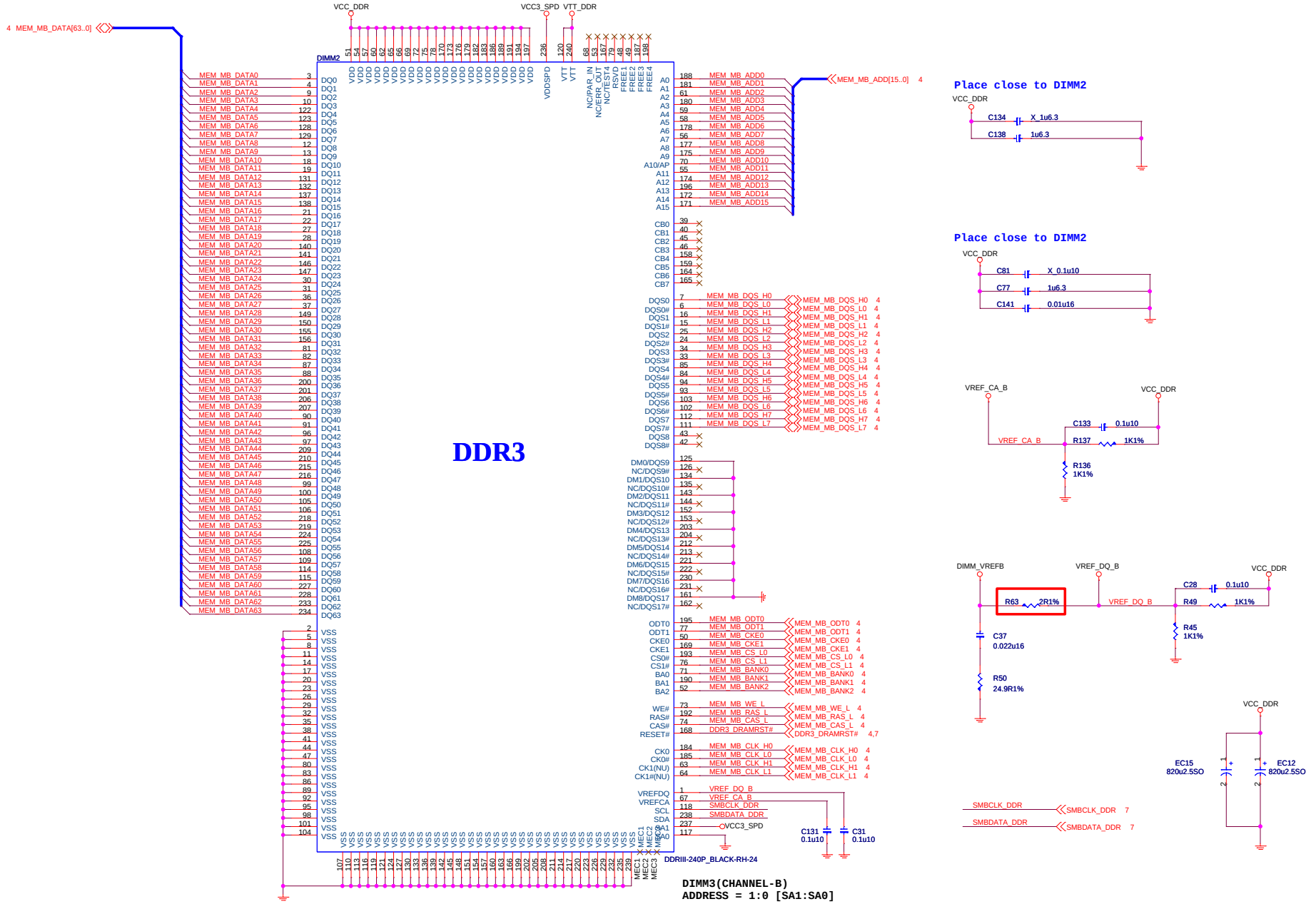
DDRIII DIMM_B0



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Custom	DDR3 Chanel-B DIMM3/4	2.1

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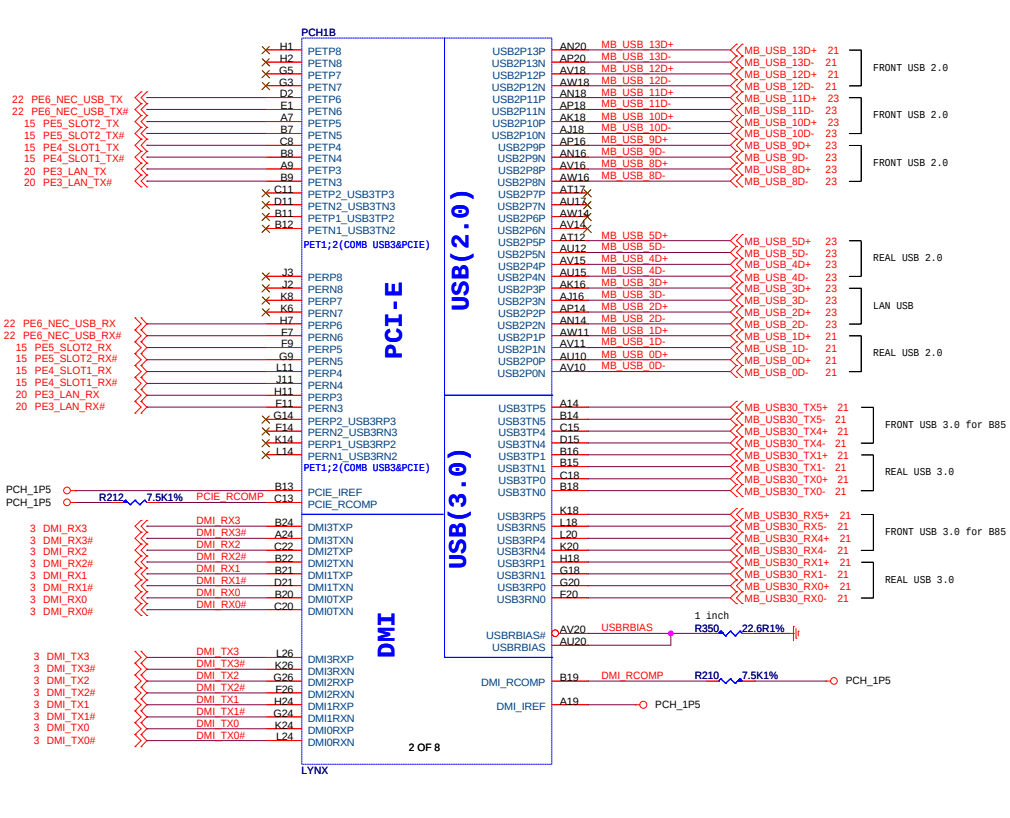
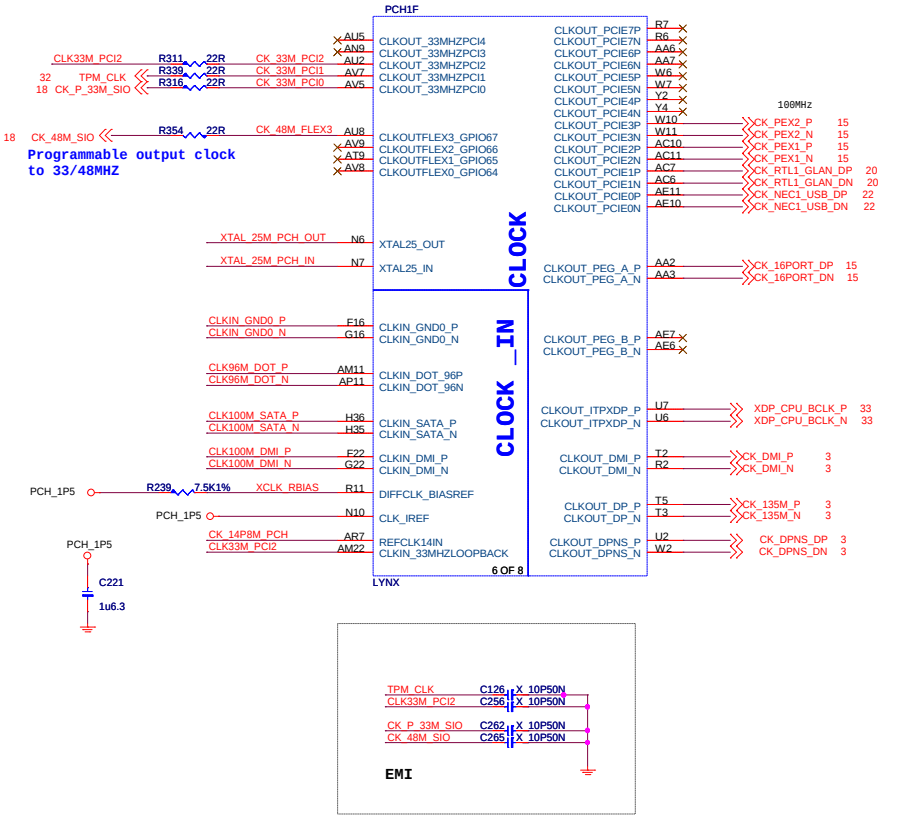
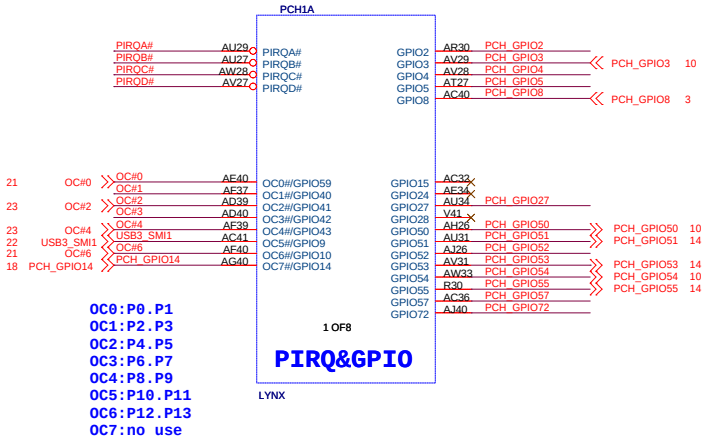
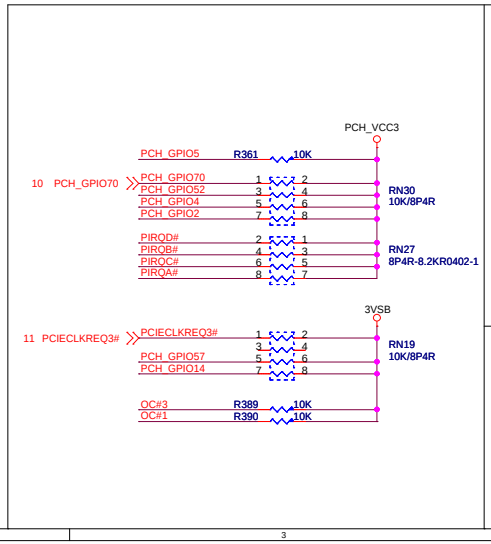
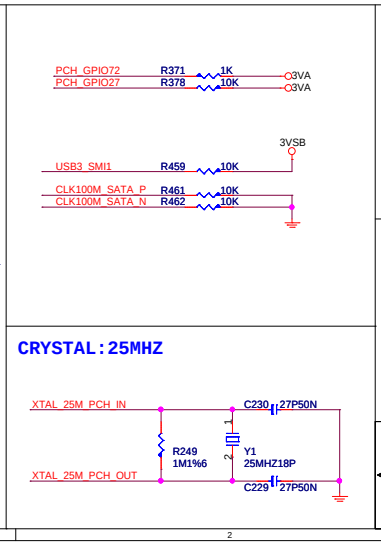
USB 2.0 ports 6,7,12 and 13 are disabled on 10 port SKUs.
Only USB 3.0 ports 1 and 2 are enabled.
pcie port7,8 NA

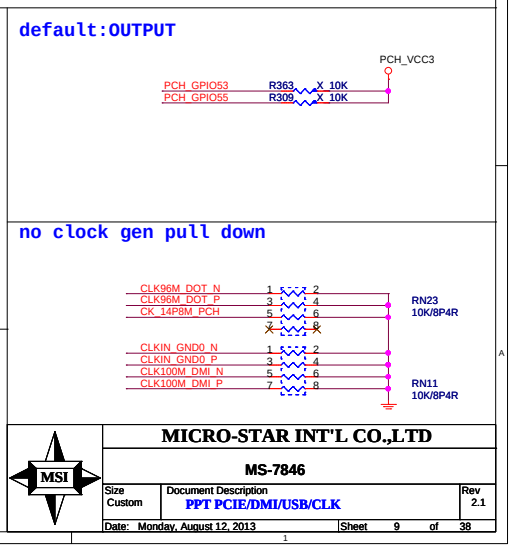




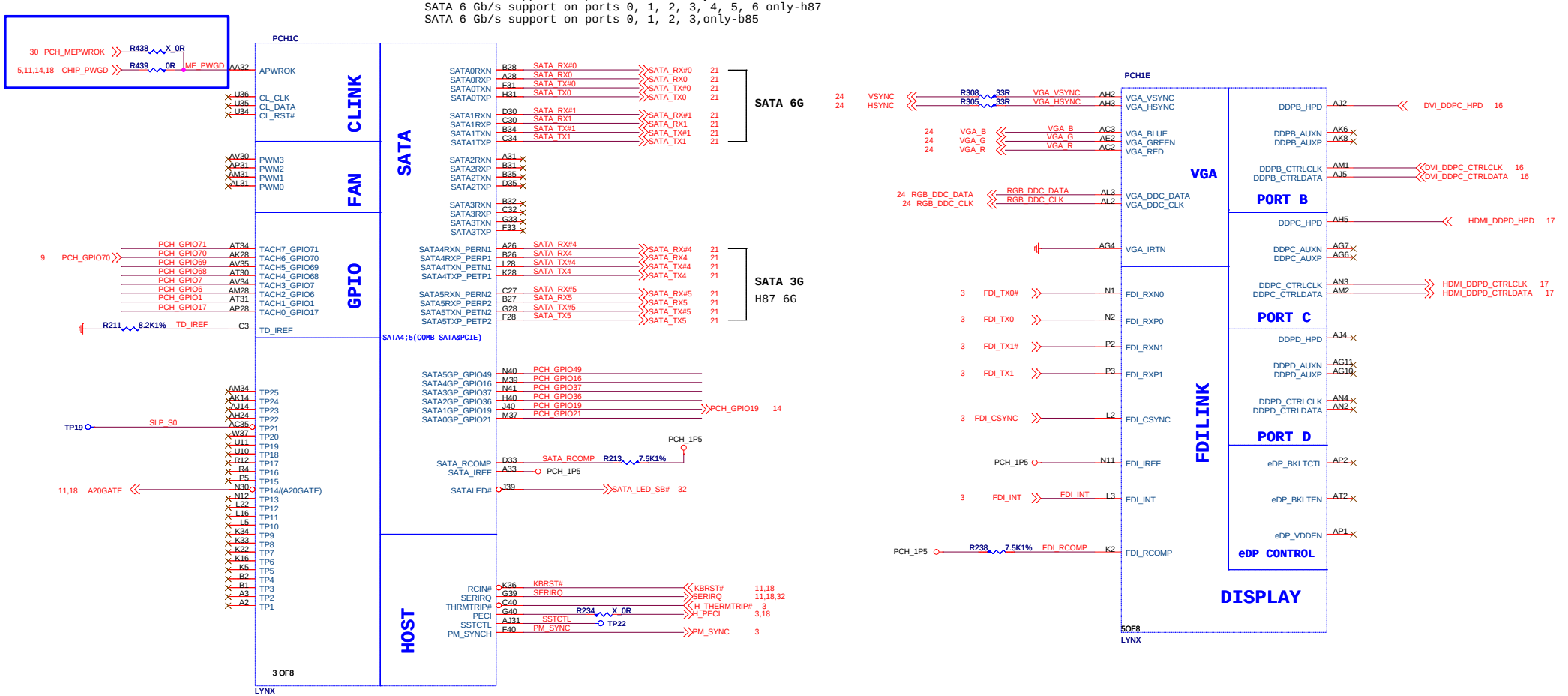




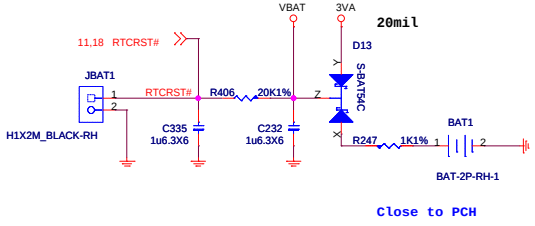


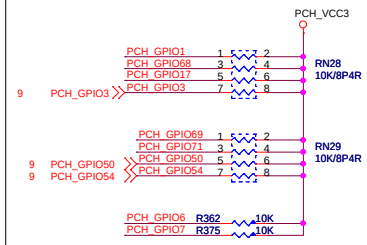


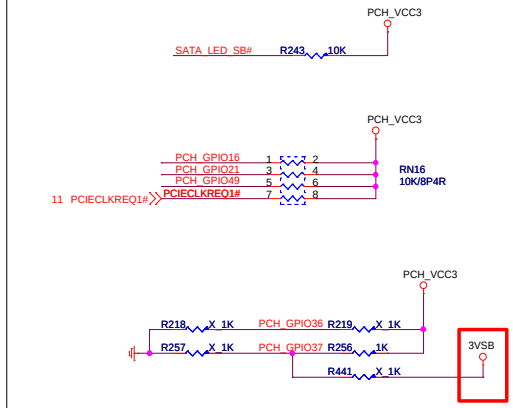
SATA 6 Gb/s support on ports 0 and 1 only.-h81
SATA 6 Gb/s support on ports 0, 1, 2, 3, 4, 5, 6 only-h87
SATA 6 Gb/s support on ports 0, 1, 2, 3,only-b85



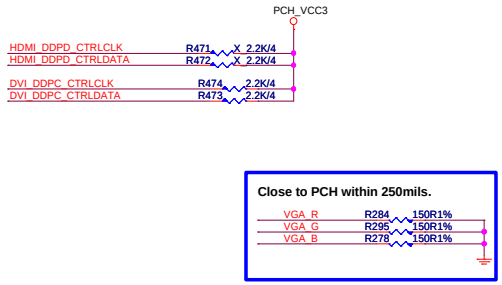
RTC and CLR_CMOS







Enable VGA(CTRLCLK/DATA Pull High)



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Size	Document Description	Rev
Custom	PPT SATA/HOST/FAN/GPIO/VGA	2.1

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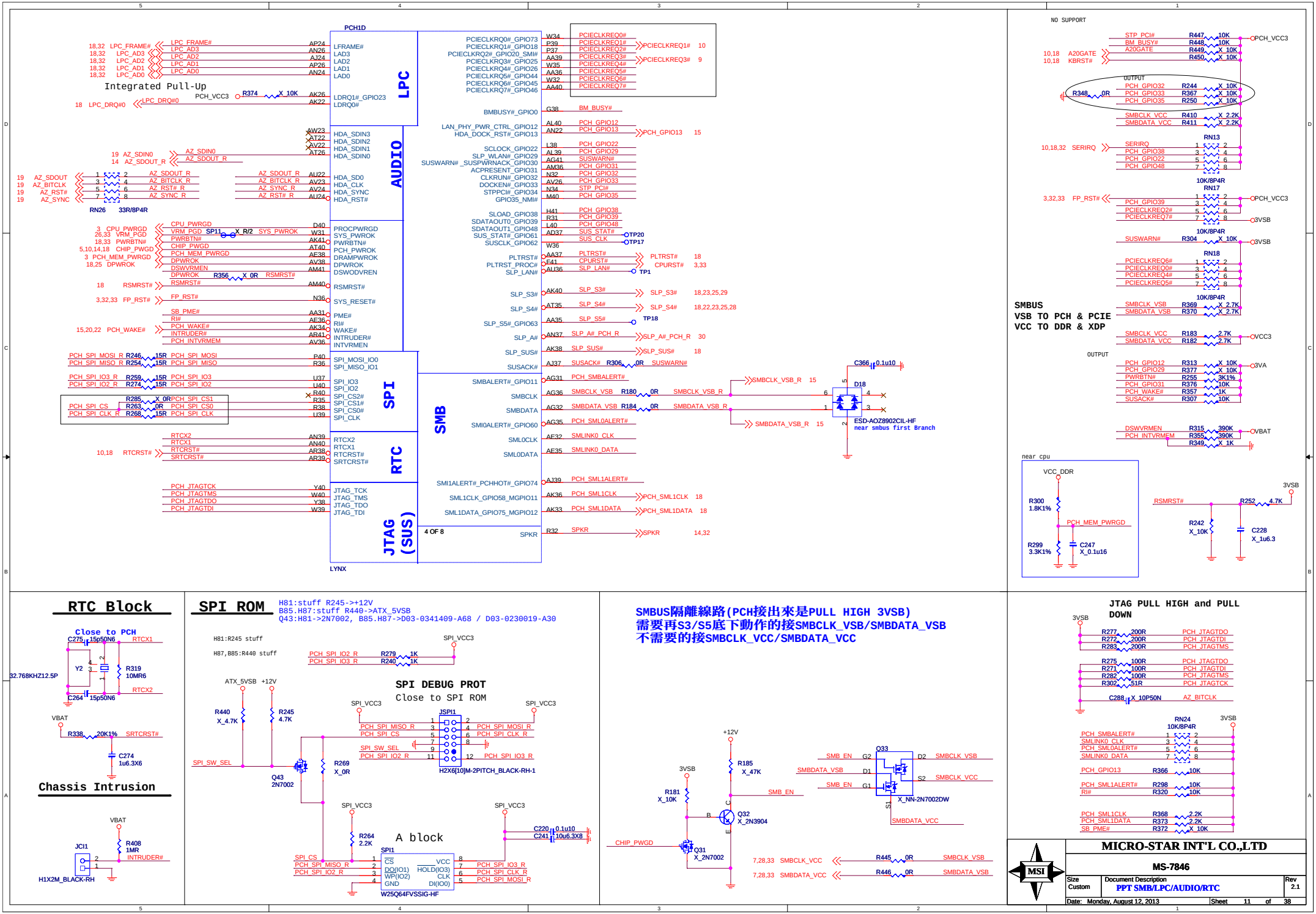

RTC Block

Close to PCH

Chassis Intrusion

SPI ROM

H81:stuff R245->+12V
B85.H87:stuff R440->ATX_5VSB
Q43:H81->2N7002, B85.H87->D03-0341409-A68 / D03-0230019-A30

SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC

JTAG PULL HIGH and PULL DOWN

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Size	Document Description	Rev
Custom	PPT SMB/LPC/AUDIO/RTC	2.1

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VCC3 (PCH_VCC3) 0.21A

3VA 0.015A

VBAT 6uA

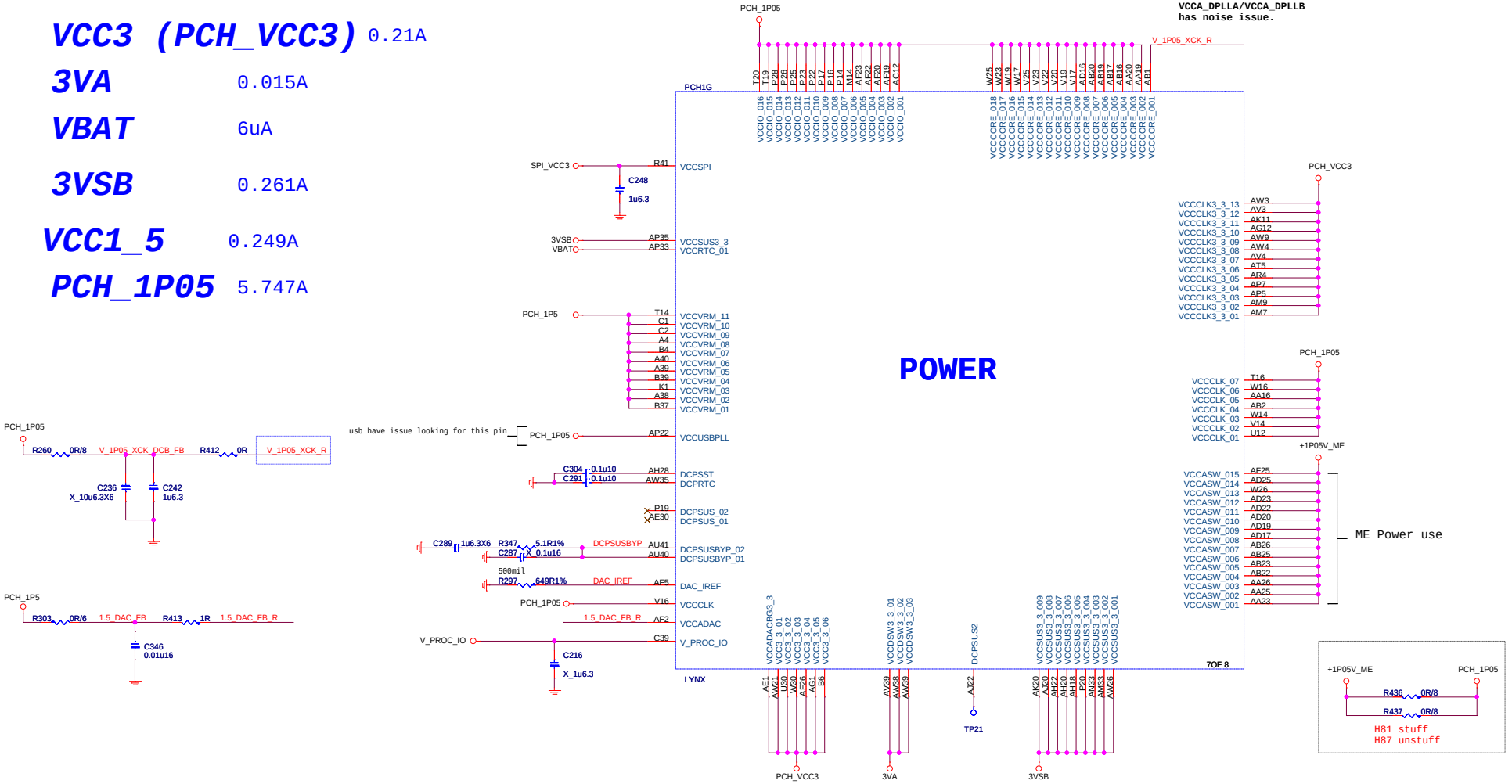
3VSB 0.261A

VCC1_5 0.249A

PCH_1P05 5.747A

Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.

POWER

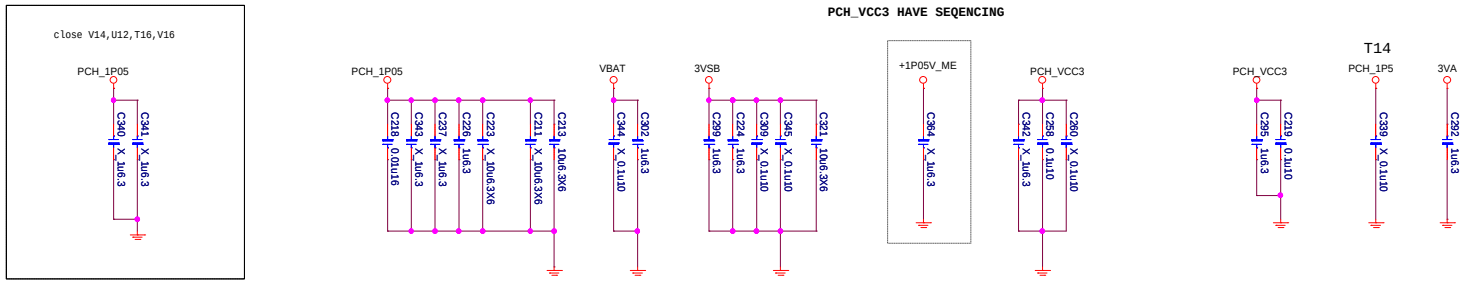


PCH decoupling cap

close V14,U12,T16,V16

PCH_VCC3 HAVE SEQENCING

T14



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: LYNX -POWER PIN
Rev: 2.1	
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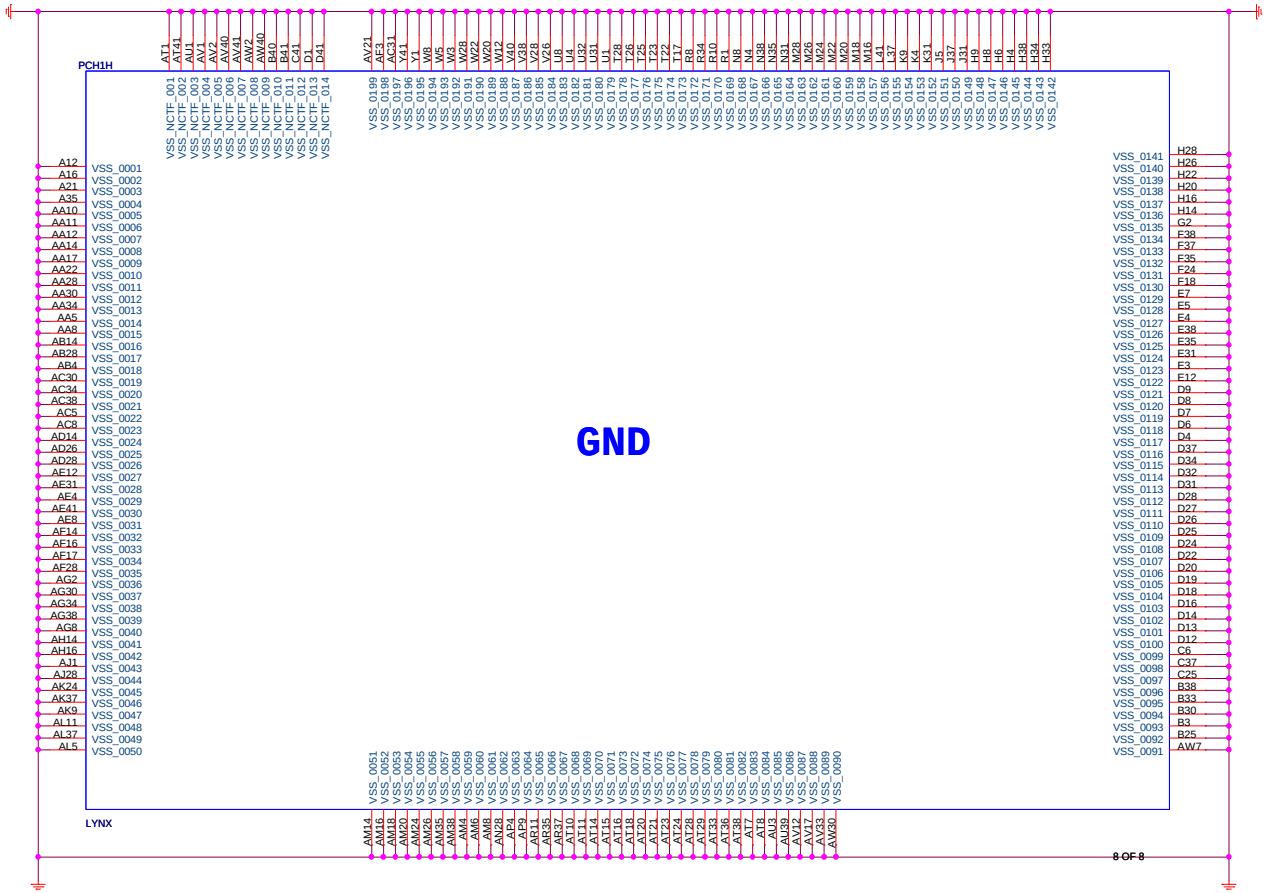

MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PPT GND/NVRAM
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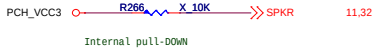
PCH Straps



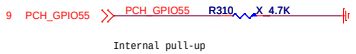
SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



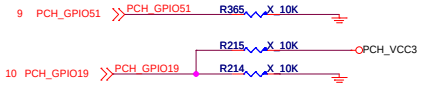
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GP/GPIO19, GPIO51

Default (SPI):

Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

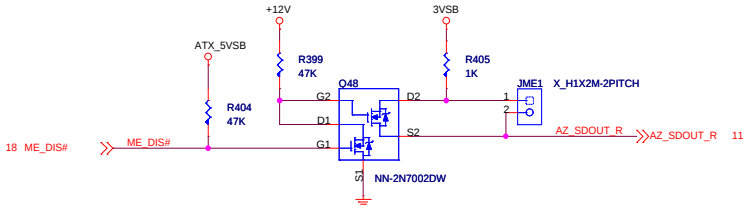
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

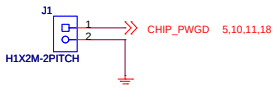
Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

For test cpu voltage



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Size	Document Description	Rev
Custom	PPT STRAPS	2.1

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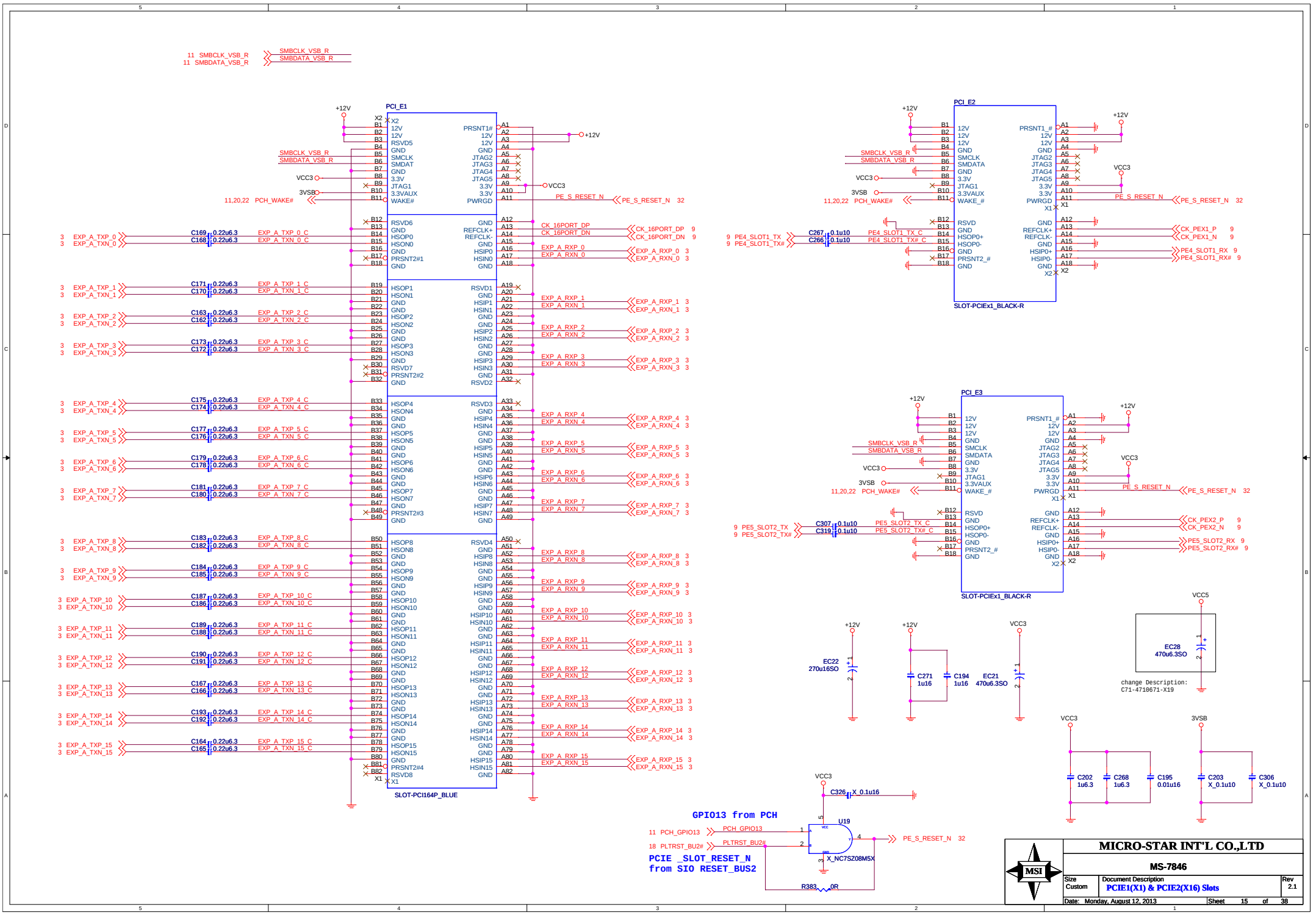
PCI_E1
PCI_E2
PCI_E3
SLOT-PCIE164P_BLUE
SLOT-PCIEx1_BLACK-R
SLOT-PCIEx1_BLACK-R
SMBCLK_VSB_R
SMBDATA_VSB_R
PCH_WAKE#
PE_S_RESET_N
GPIO13 from PCH
PCIE _SLOT_RESET_N
from SIO RESET_BUS2
PCH_GPIO13
PLTRST_BU2#
X_NC7SZ08M5X
R383 0R
EC22 270u16SO
C271 1u16
C194 1u16
EC21 470u6.3SO
EC28 470u6.3SO
change Description:
C71-4710671-X19
C202 1u6.3
C268 1u6.3
C195 0.01u16
C203 X_0.1u10
C306 X_0.1u10
MICRO-STAR INT'L CO.,LTD
MS-7846
PCIE1(X1) & PCIE2(X16) Slots
Size Custom
Rev 2.1
Date: Monday, August 12, 2013
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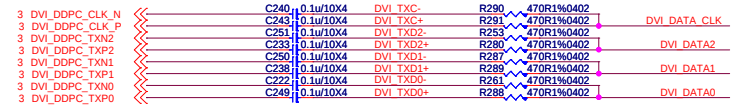
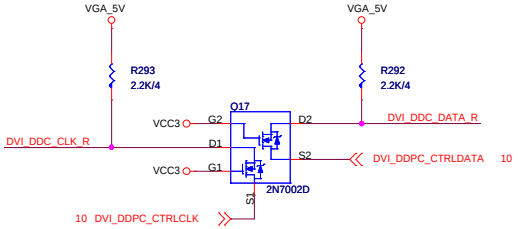
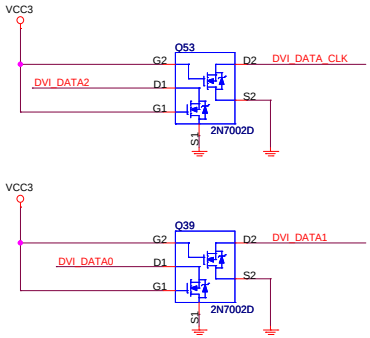
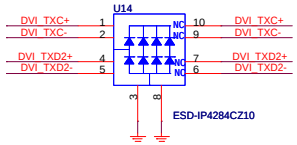
DVI level shifter

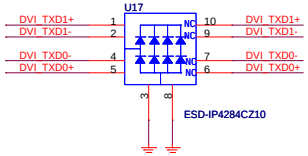
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

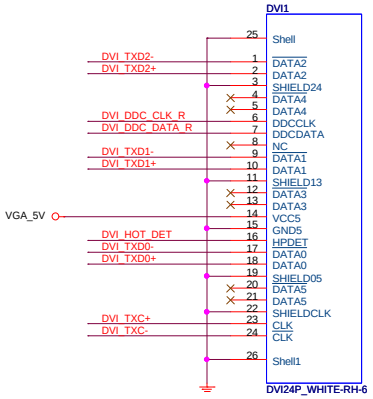


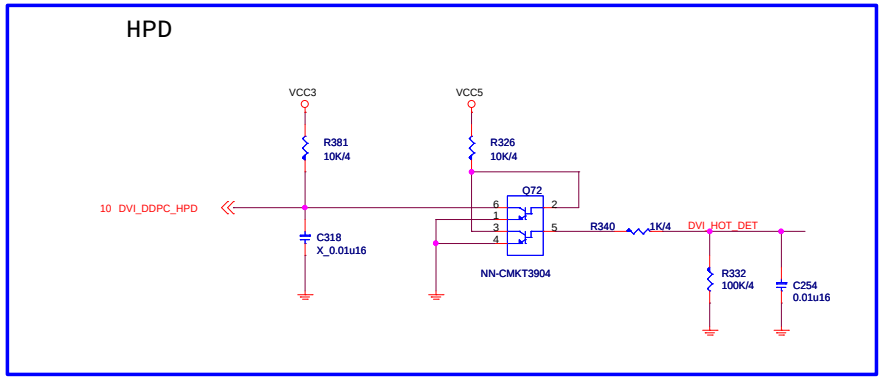


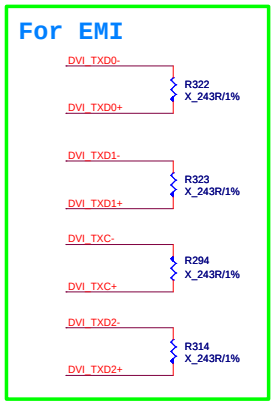


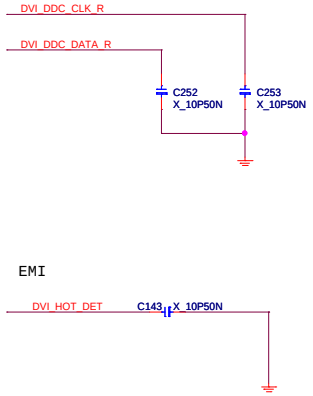


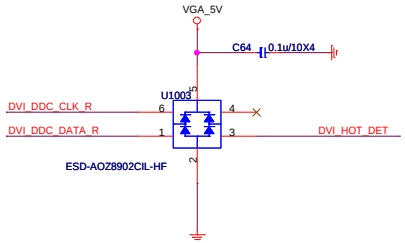












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Size	Document Description	Rev
Custom	DVI	2.1

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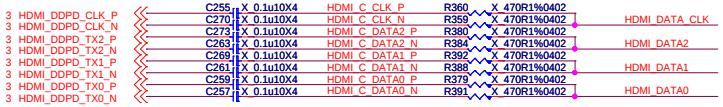
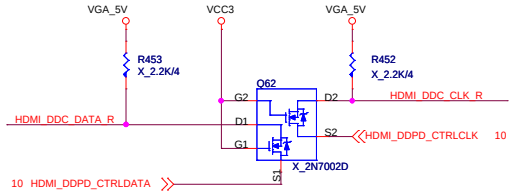
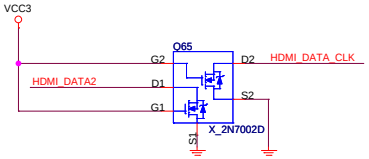
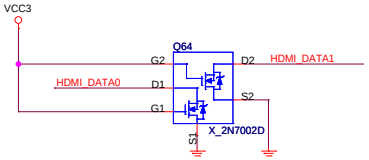
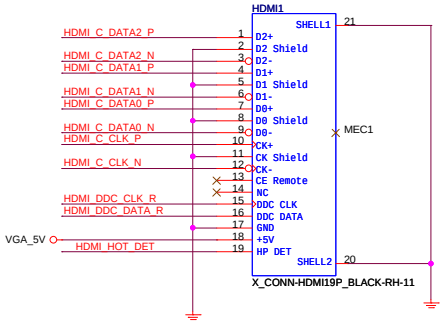
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



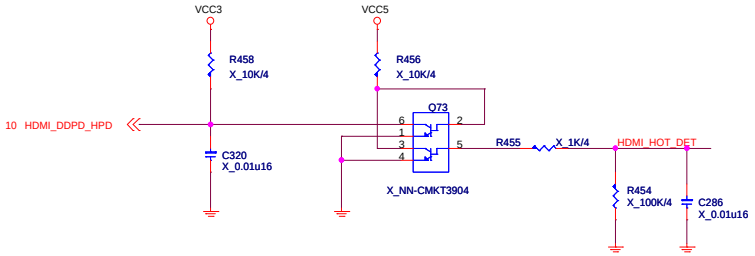


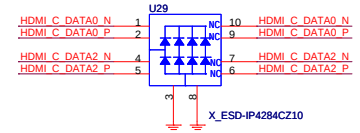


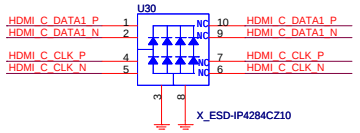


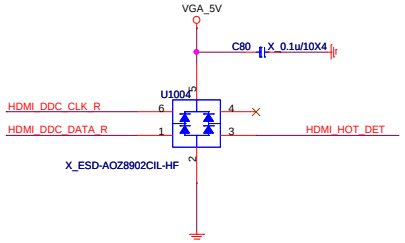


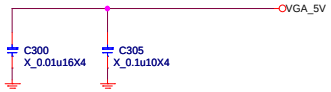
HPD



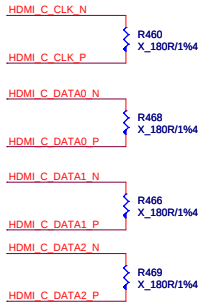




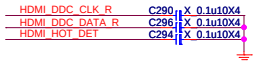




For EMI



EMI



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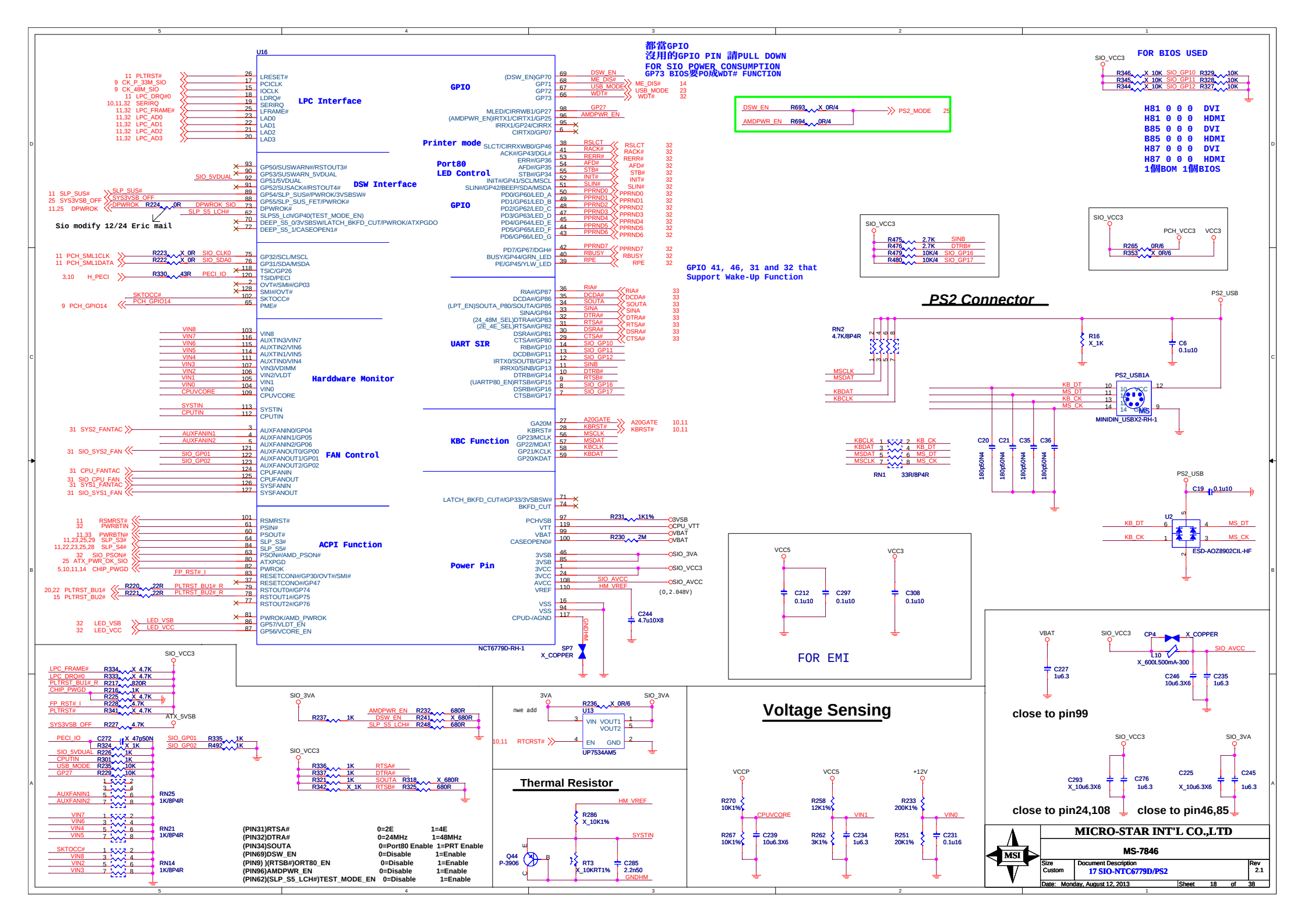
都當GPIO
沒用的GPIO PIN 請PULL DOWN
FOR SIO POWER CONSUMPTION
GP73 BIOS要PO成WDT# FUNCTION
FOR BIOS USED
H81 0 0 0 DVI
H81 0 0 0 HDMI
B85 0 0 0 DVI
B85 0 0 0 HDMI
H87 0 0 0 DVI
H87 0 0 0 HDMI
1個BOM 1個BIOS
U16
LPC Interface
GPIO
Printer mode
Port80
LED Control
DSW Interface
Sio modify 12/24 Eric mail
Harddware Monitor
UART SIR
FAN Control
KBC Function
ACPI Function
Power Pin
GPIO 41, 46, 31 and 32 that
Support Wake-Up Function
NCT6779D-RH-1
PS2 Connector
MINIDIN_USBX2-RH-1
ESD-AOZ8902CIL-HF
FOR EMI
Voltage Sensing
Thermal Resistor
UP7534AM5
close to pin99
close to pin24,108
close to pin46,85
(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable
MICRO-STAR INT'L CO.,LTD
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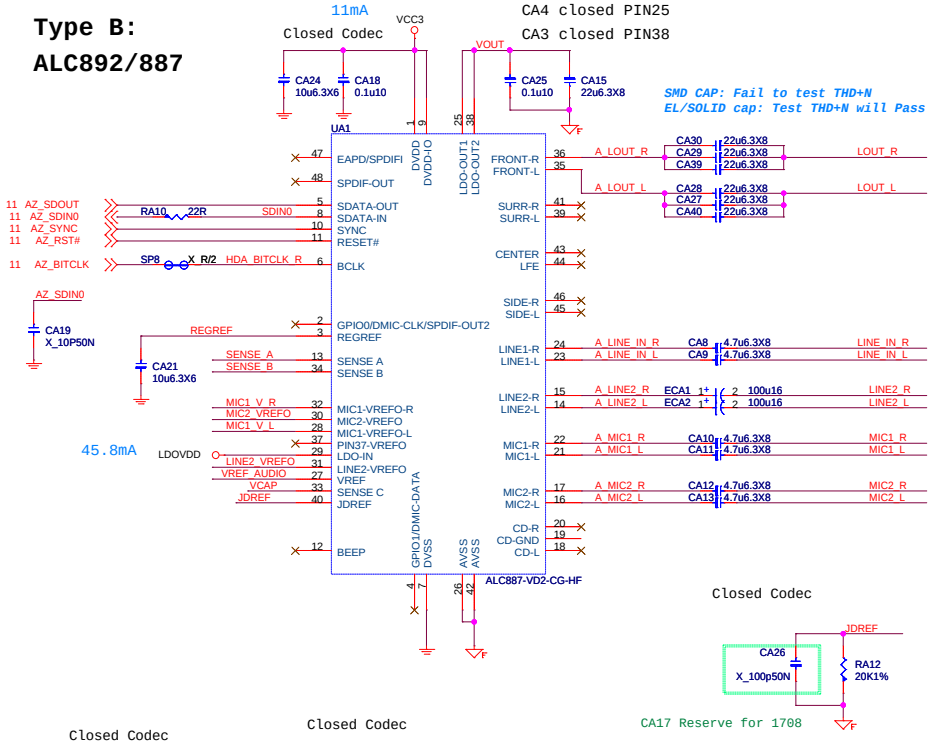
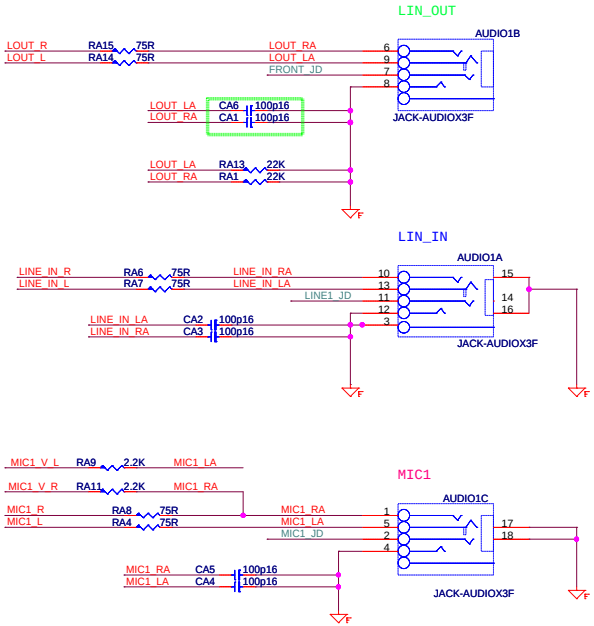
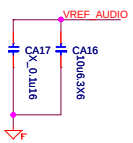
Type B:
ALC892/887

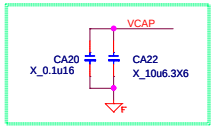




Closed Codec

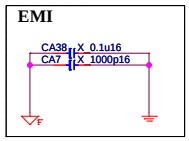


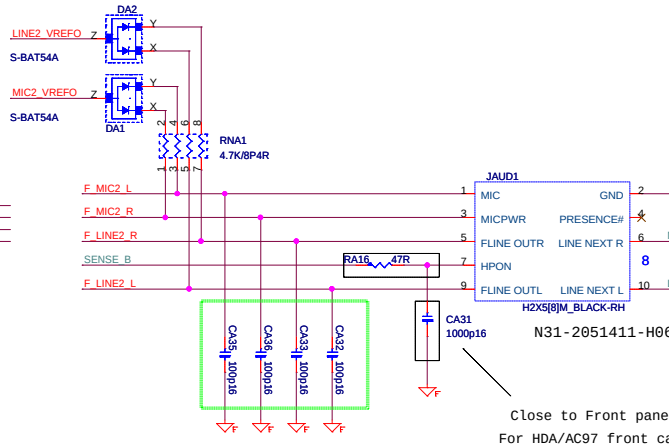
Closed Codec

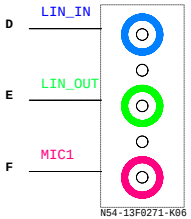


887: Remove
1708:Stuff

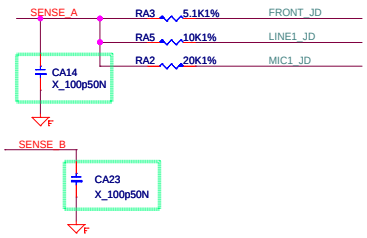
EMI

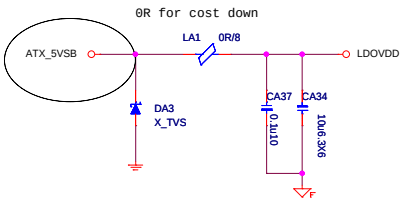






Closed Codec





CA37,CA34 close to LA1

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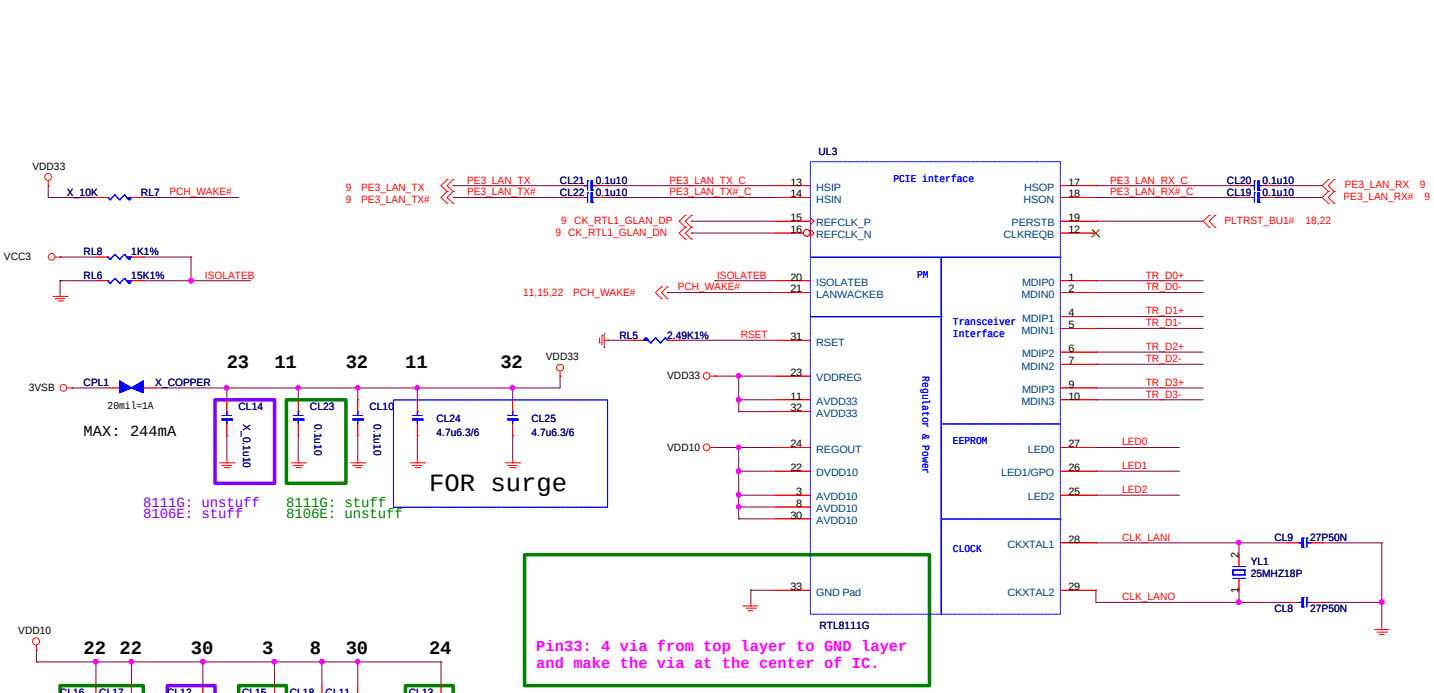
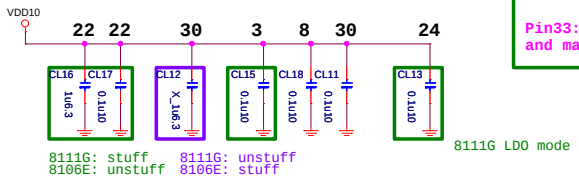
RTL8111G Giga LAN

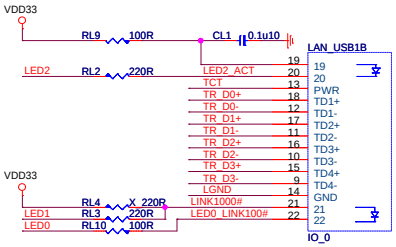
RTL8106E 10/100M LAN



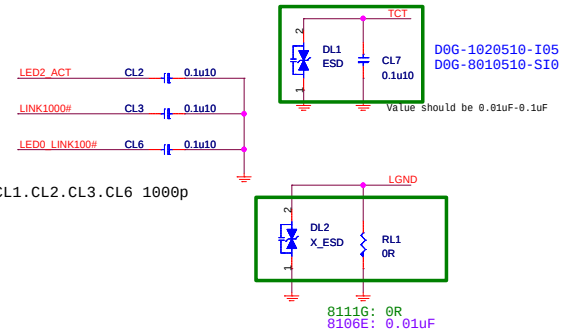


Icc10 average operating supply current from1.0V
At 1Gbps with heavy network traffic 300mA

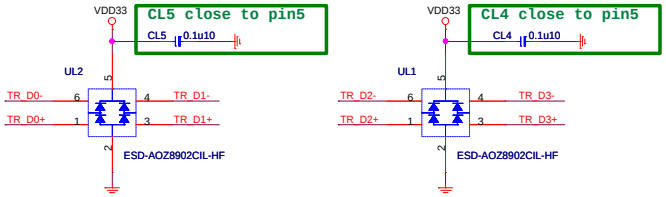
LAN Connector



8111G: Keep RL3 and Remove RL4 for RTL8111G
8106E: Keep RL4 and Remove RL3 for RTL8106E



Reserve ESD Protect



MSI P/N : D0G-0200529-A68、Vender P/N : AOZ8902CI
MSI P/N : D0G-0100619-I05、Vender P/N : TVLST2304AD0

8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

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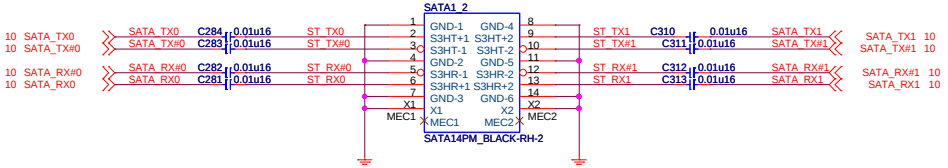
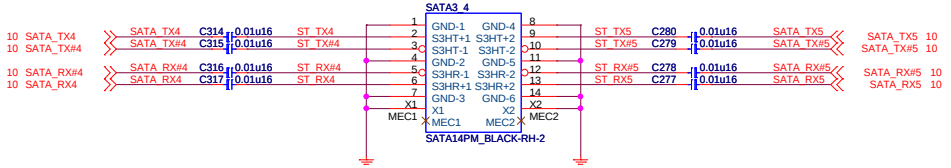
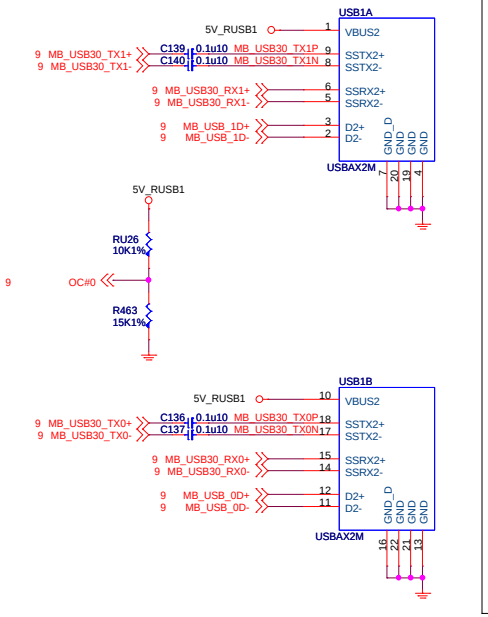
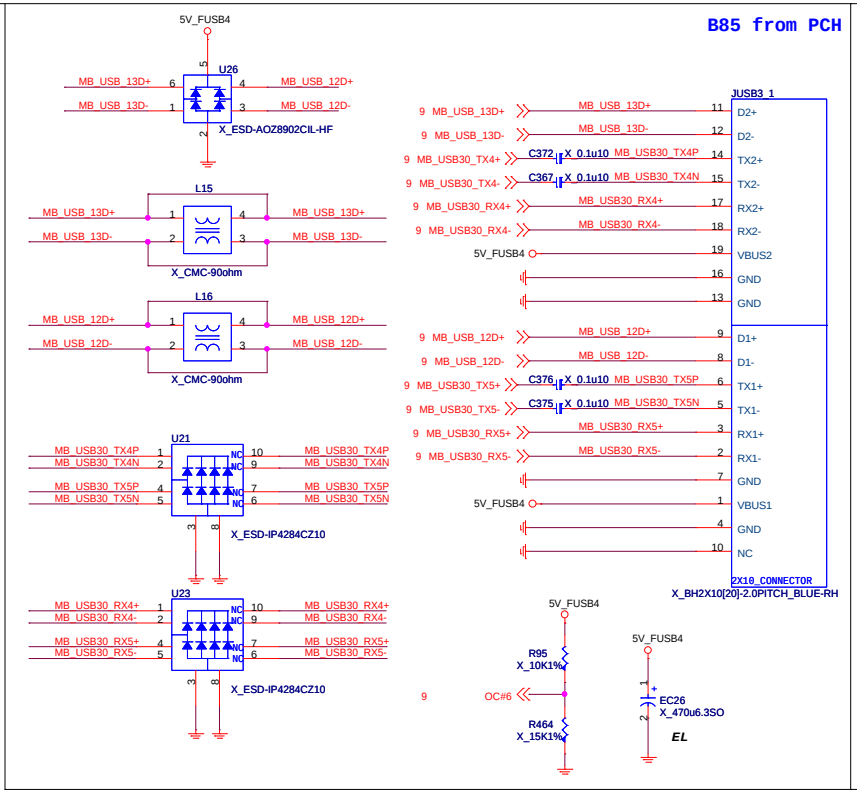
SATA 6G PORT 0,1

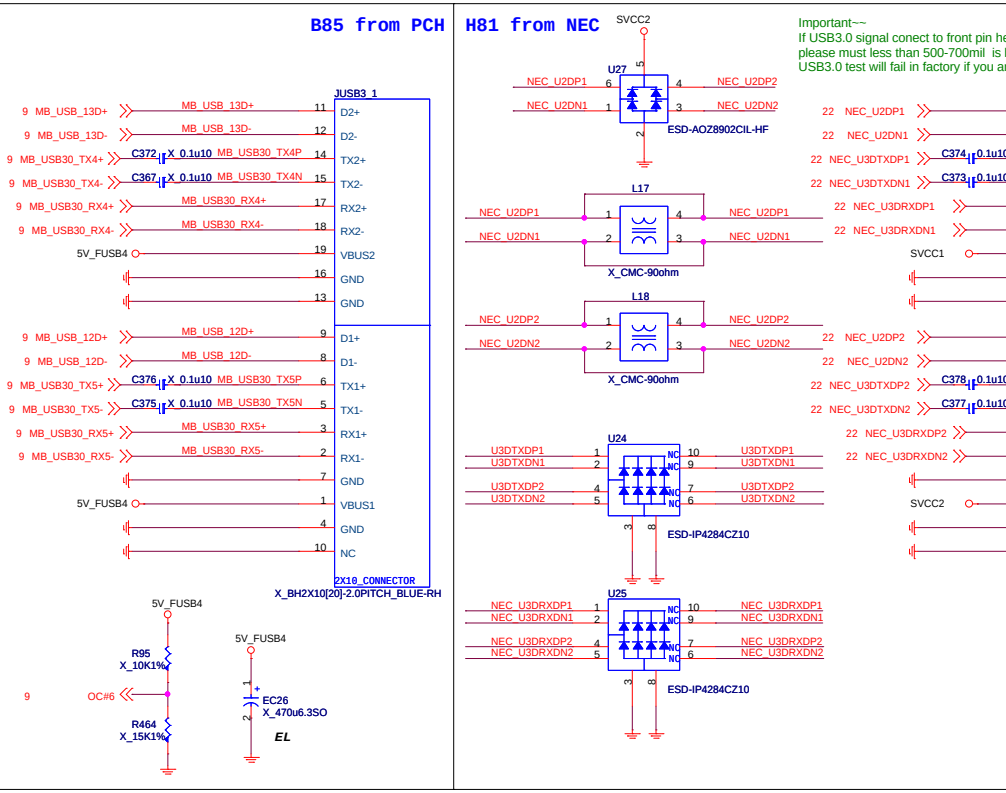


SATA 3G PORT 4,5

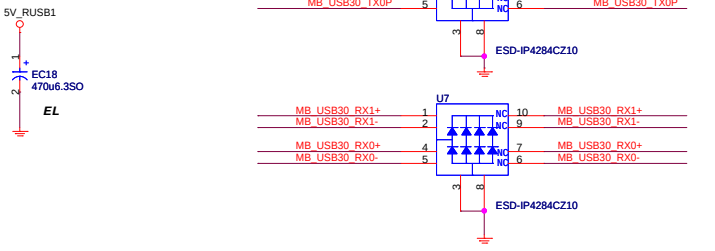








Important~~
If USB3.0 signal conect to front pin header,
please must less than 500-700mil is better.
USB3.0 test will fail in factory if you aren't follow this rule.



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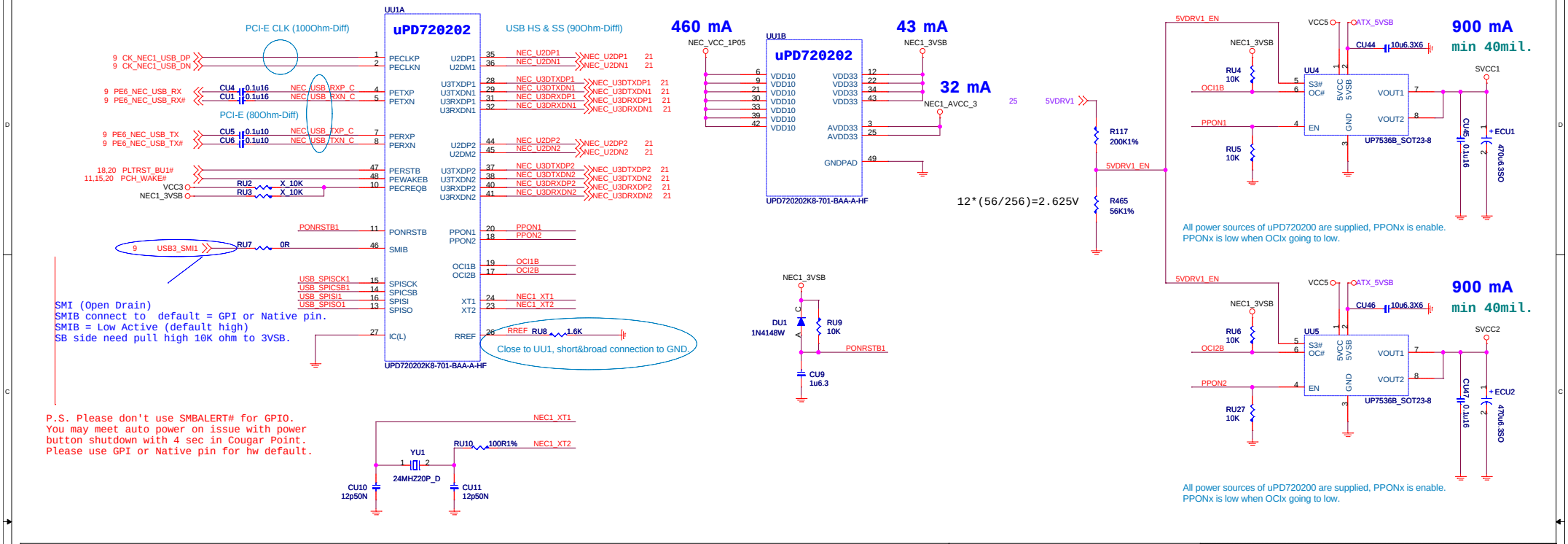
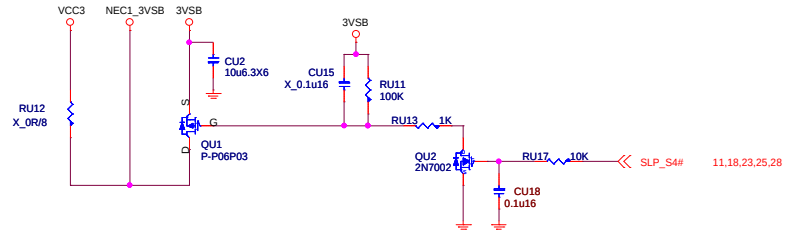
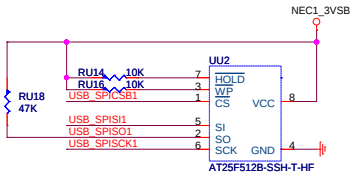


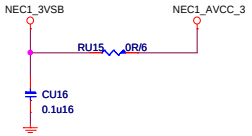
3V_Dual Circuit

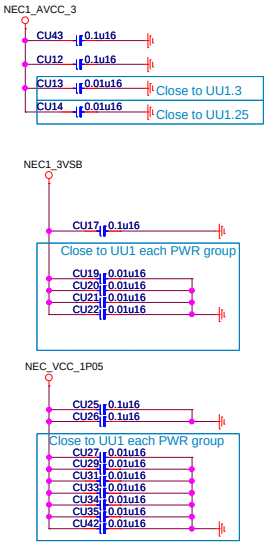


EEPROM

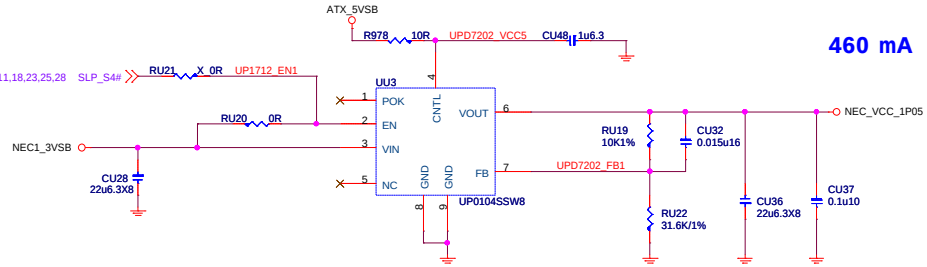


AVCC3 STB Power





uPD720200 core Power



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MS-7815		
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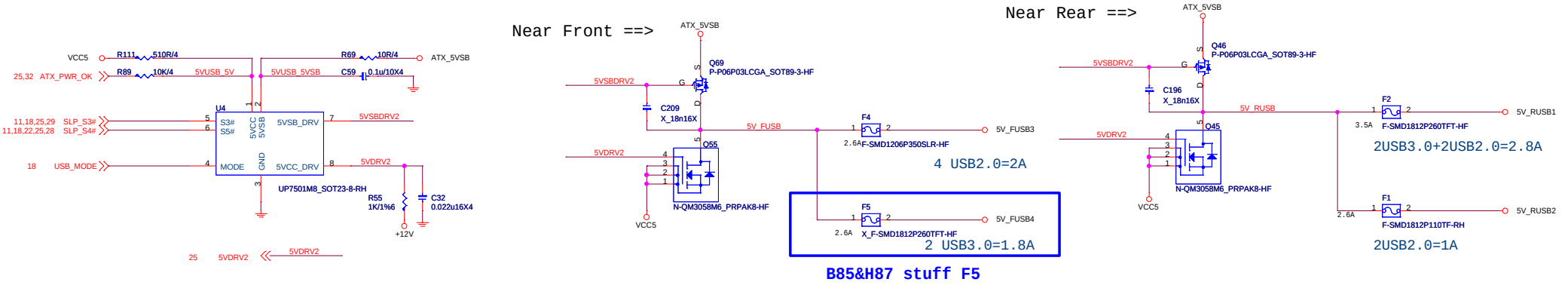
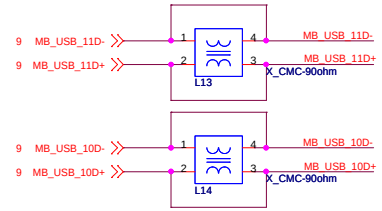
Type A: UP7501+MOS+Fuse

PCH/FCH side: OC# pull high to +3VSB

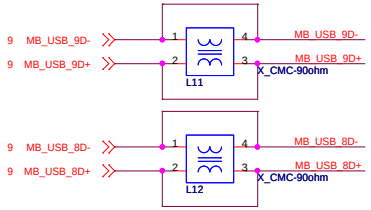
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)
D08-2000200-P16 (Itrip=3.5A; 0.003ohm) MINISMD050



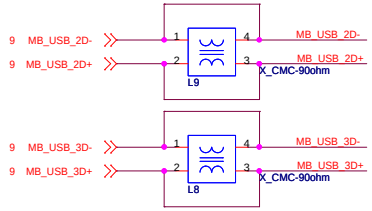
FRONT USB PORT 10,11

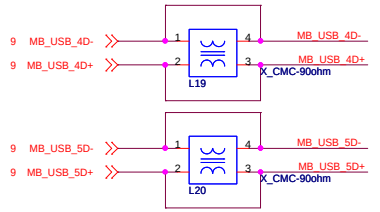


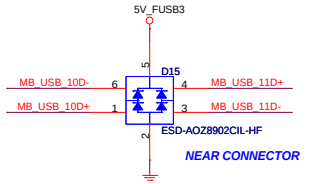
FRONT USB PORT 8,9

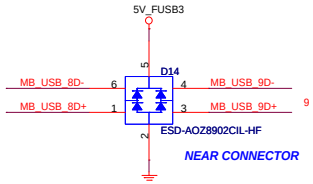


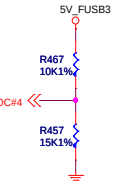
REAL USB PORT 12.13

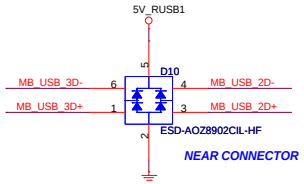


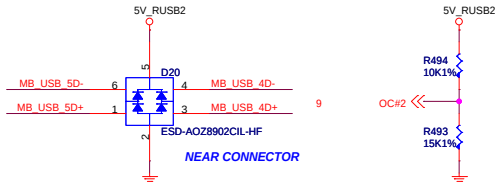


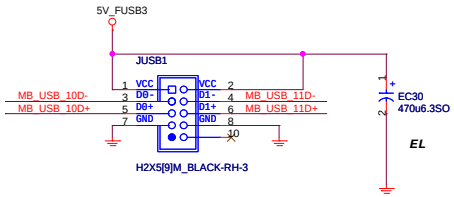


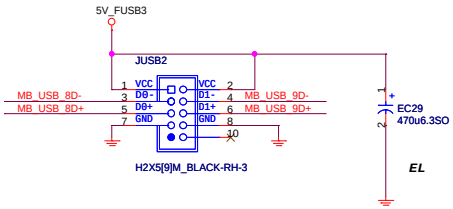


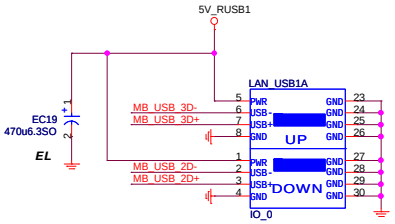


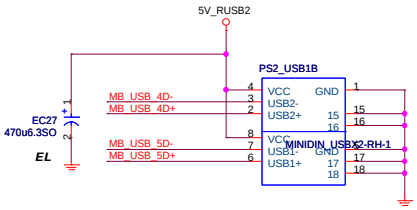












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	MS-7846	
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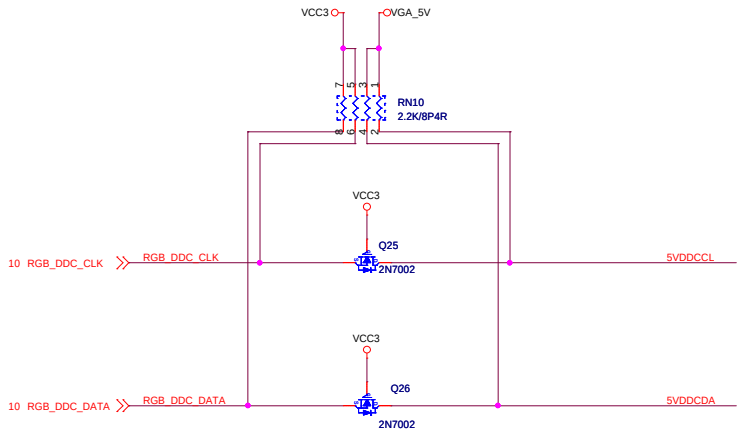
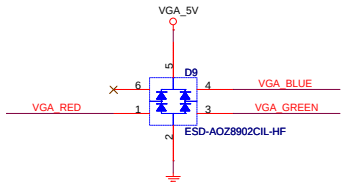
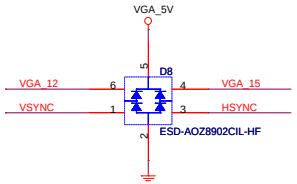
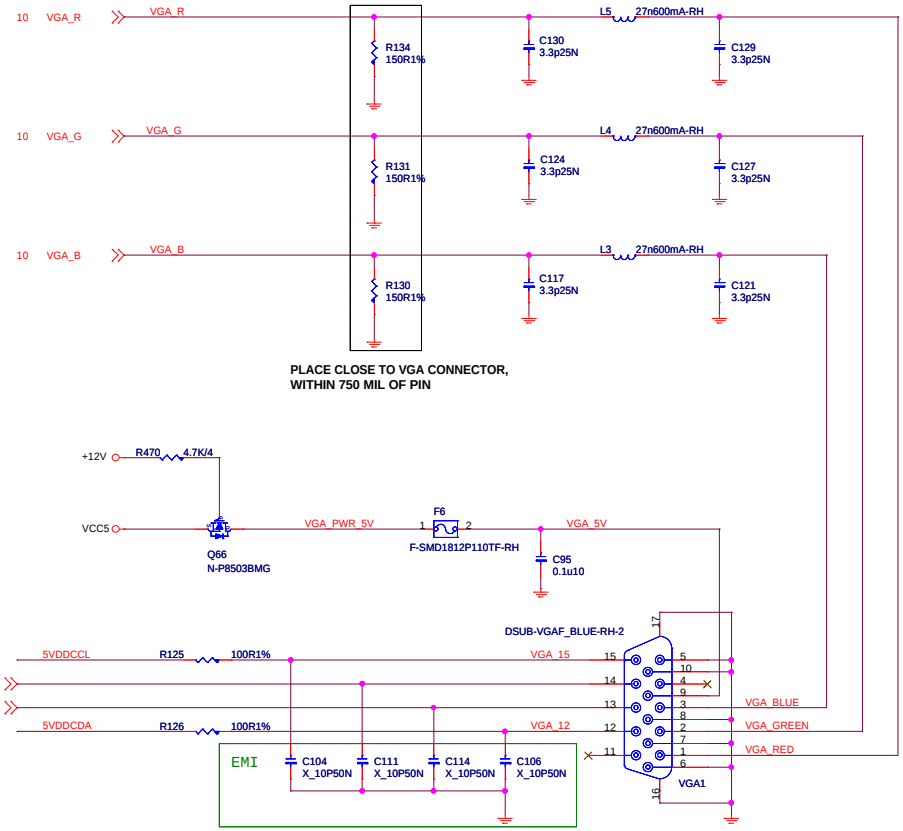
D-Sub

Level shift









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	MS-7846	
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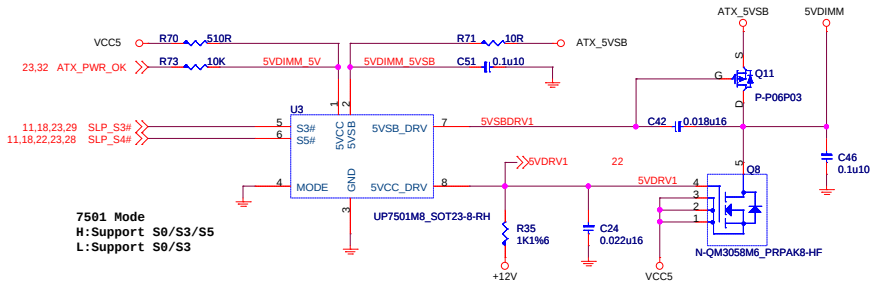
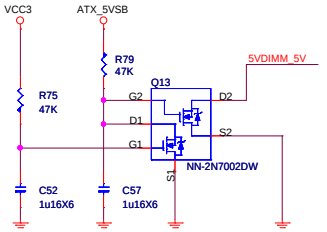
5VDIMM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

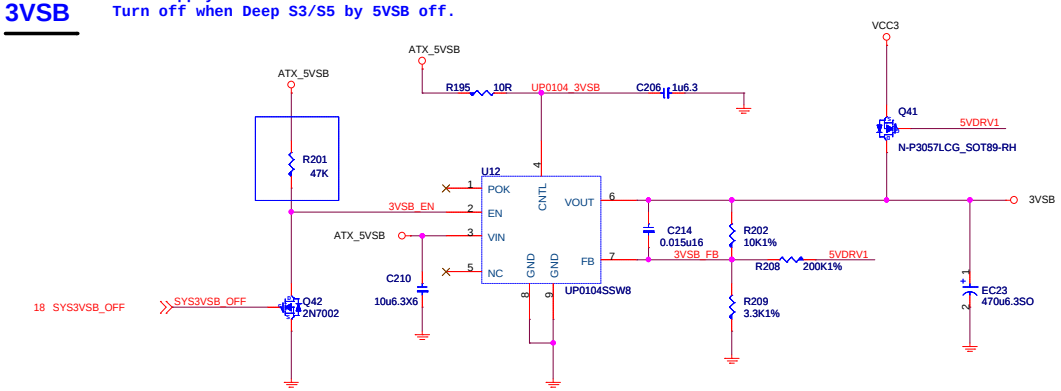
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



Patch coolermaster 700w power sequence

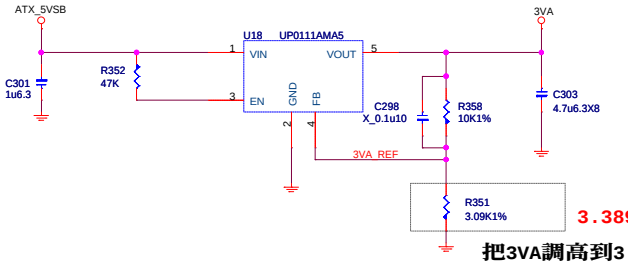
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



3VA

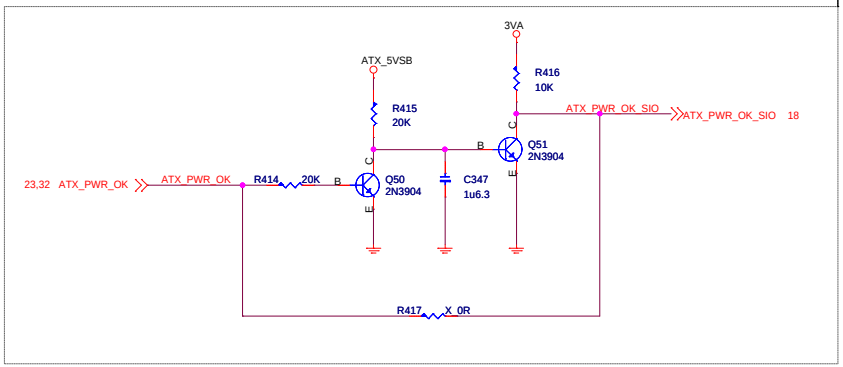
20mA



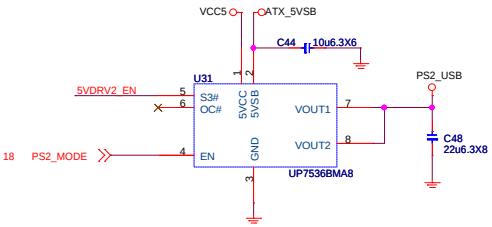
3.389V

把3VA調高到3.389V

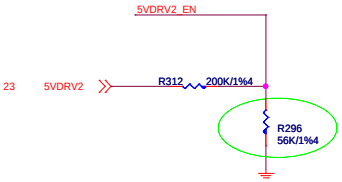
DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題



PS2 Power



USB MODE



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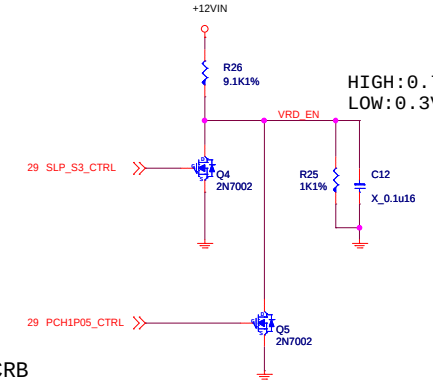
VCORE power on by s3 and 12v

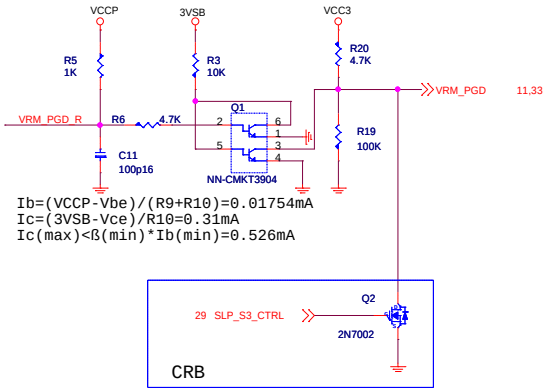


HIGH:0.7V
LOW:0.3V

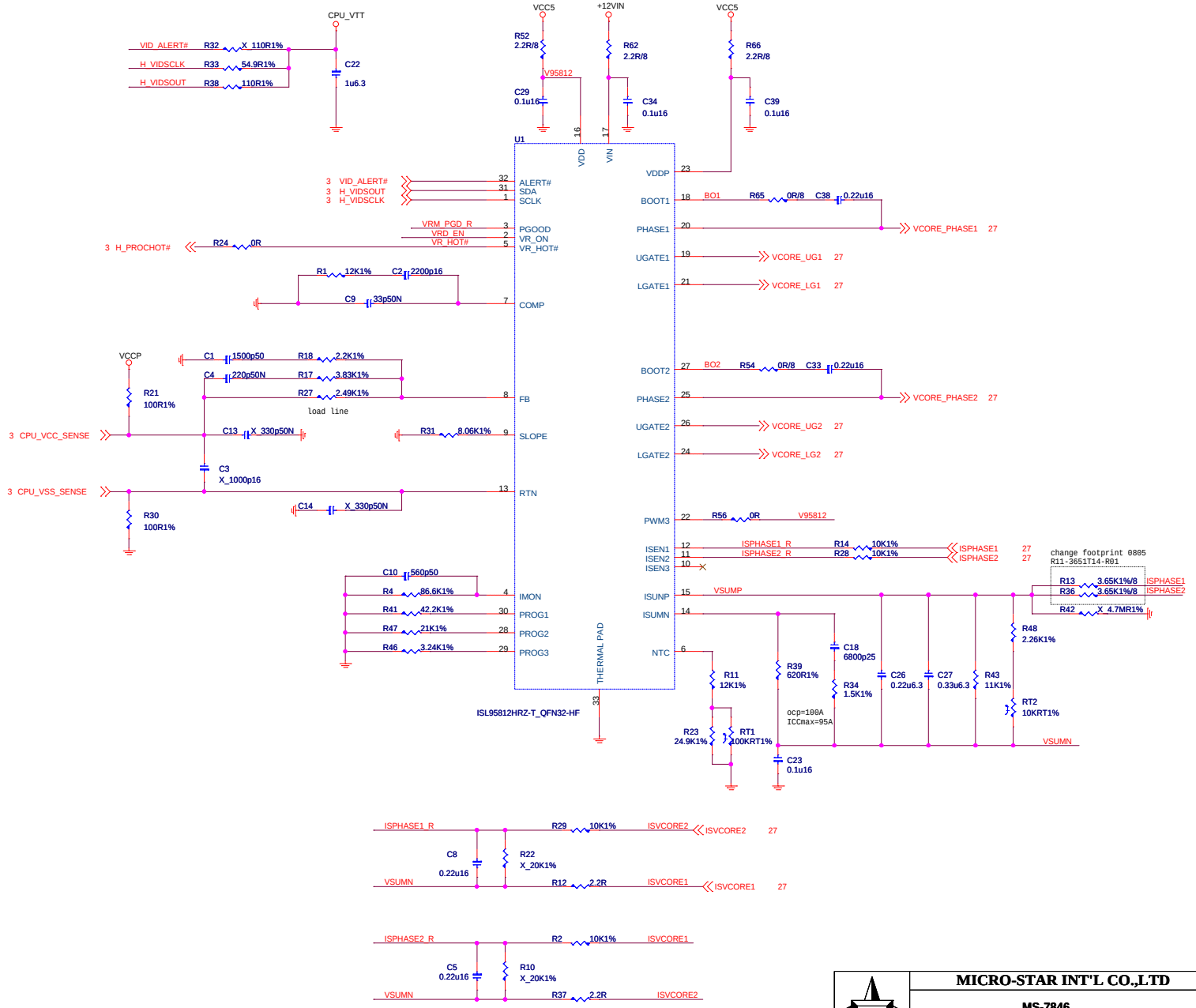
CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT



Ib=(VCCP-Vbe)/(R9+R10)=0.01754mA
Ic=(3VSB-Vce)/R10=0.31mA
Ic(max)<ß(min)*Ib(min)=0.526mA



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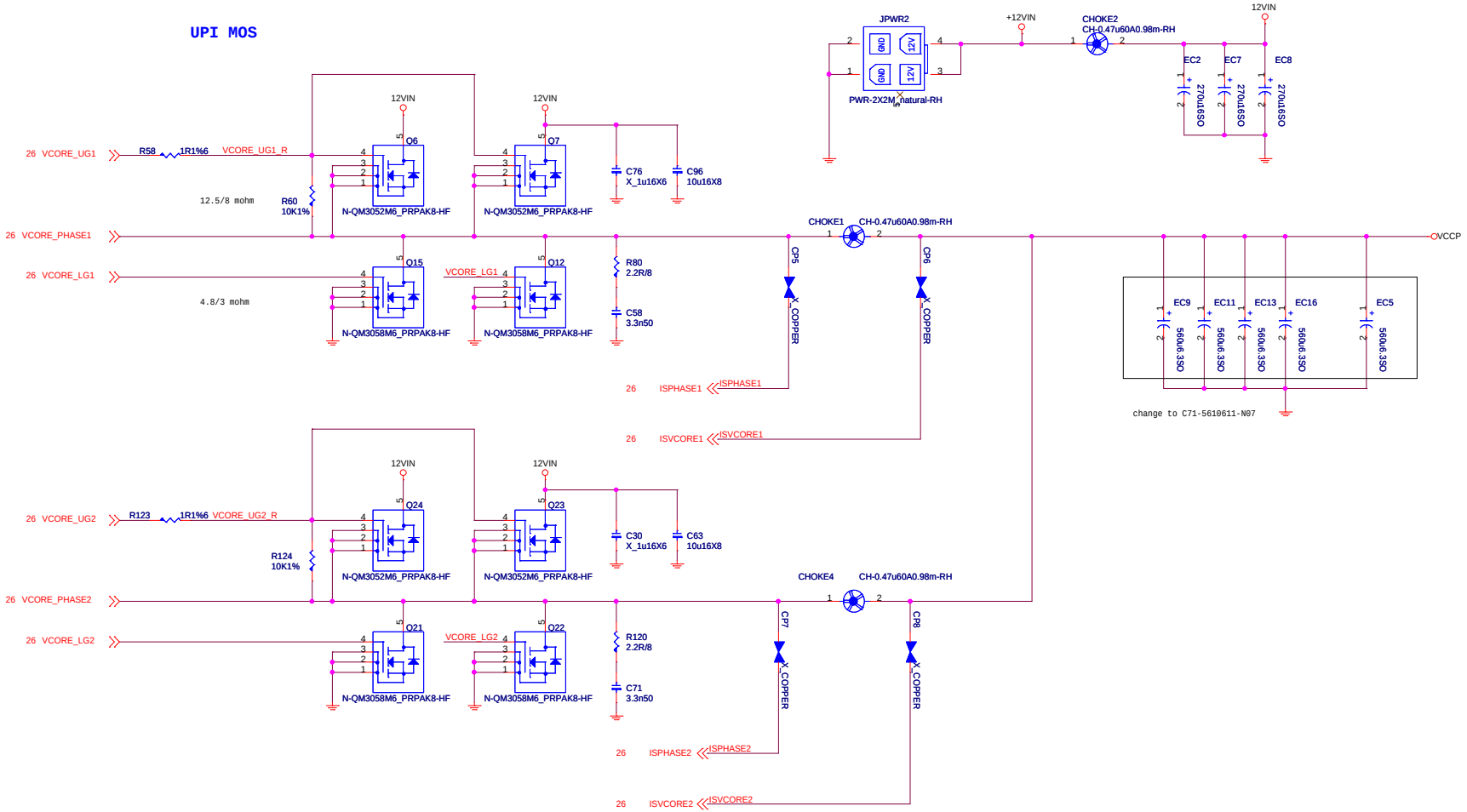
VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

Irms_input=17.5A



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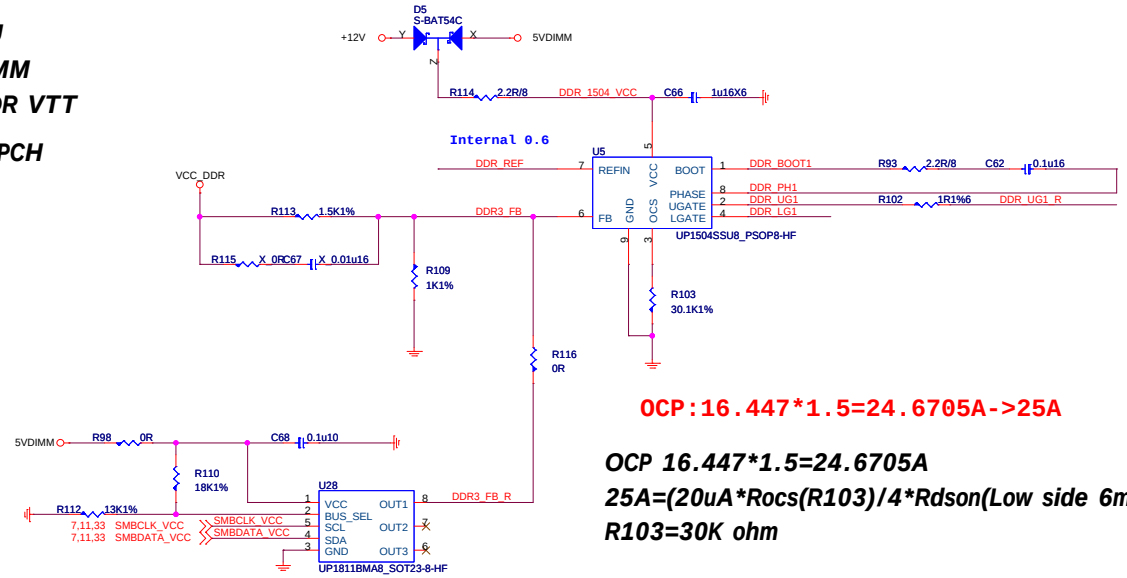
DDR Power:1.5V

DDR3_1.5V 4.2A+6A+0.5A+5.747=16.447A

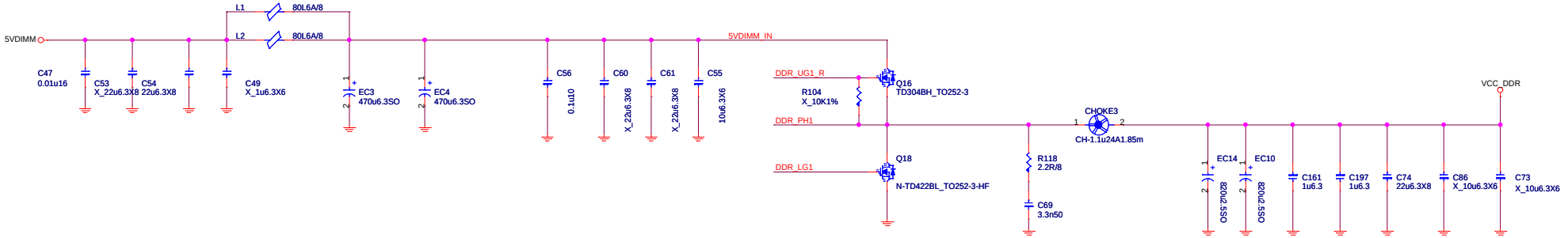
4.2A FOR CPU
6A FOR 2DIMM
0.5A FOR DDR VTT

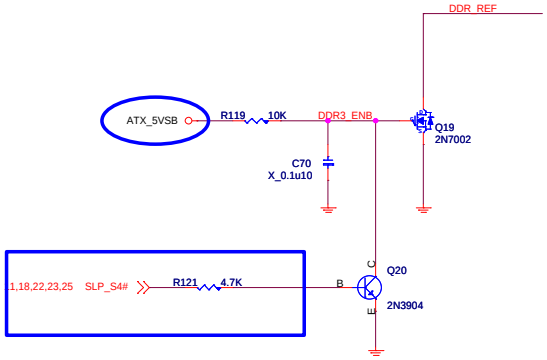
5.747A FOR PCH



OCP:16.447*1.5=24.6705A->25A

OCP 16.447*1.5=24.6705A
25A=(20uA*Rocs(R103)/4*Rdson(Low side 6mohm)
R103=30K ohm



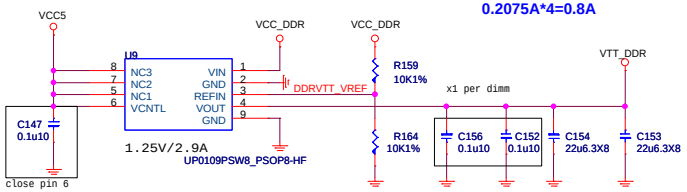


P.S. Only for meet Intel power down sequence.

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.2075A*4=0.8A



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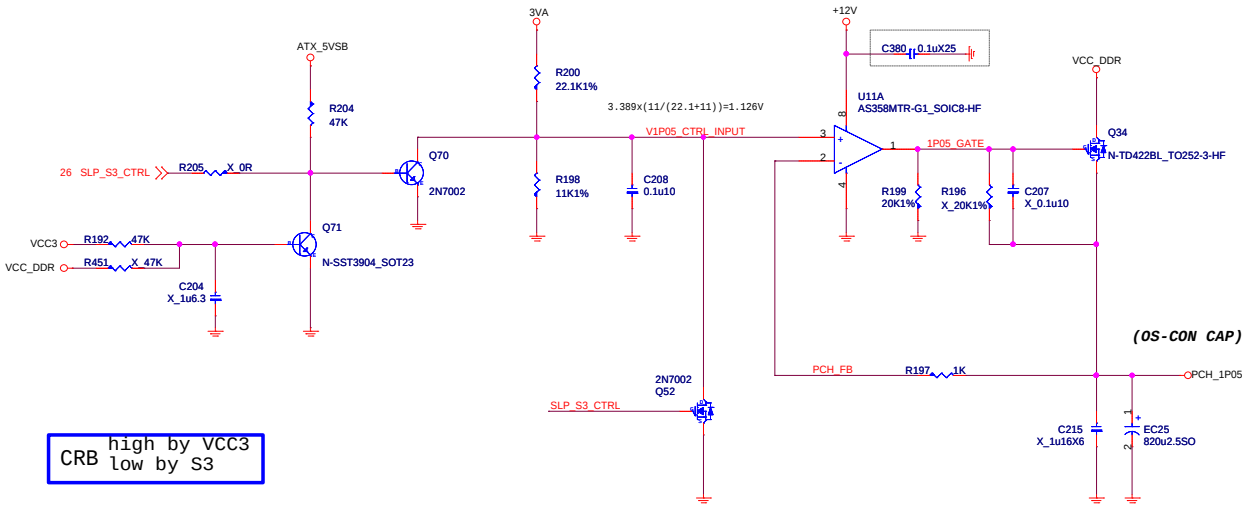
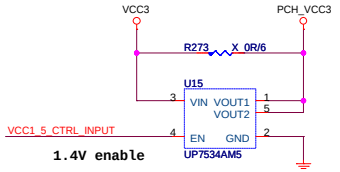
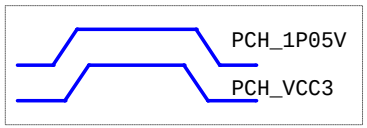
PCH Power:1.05V 5.747A



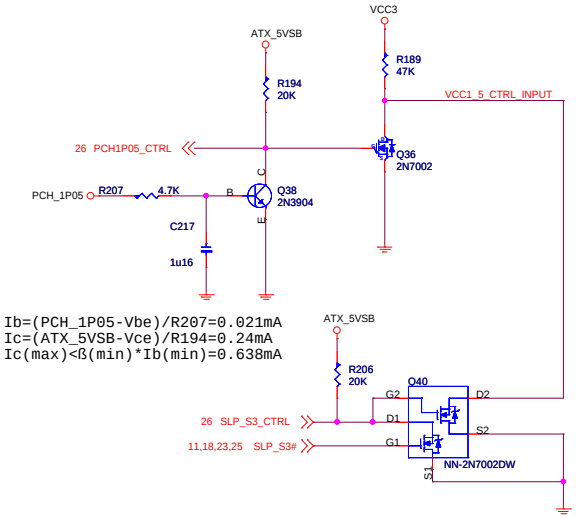
CRB high by VCC3
low by S3

0.133A

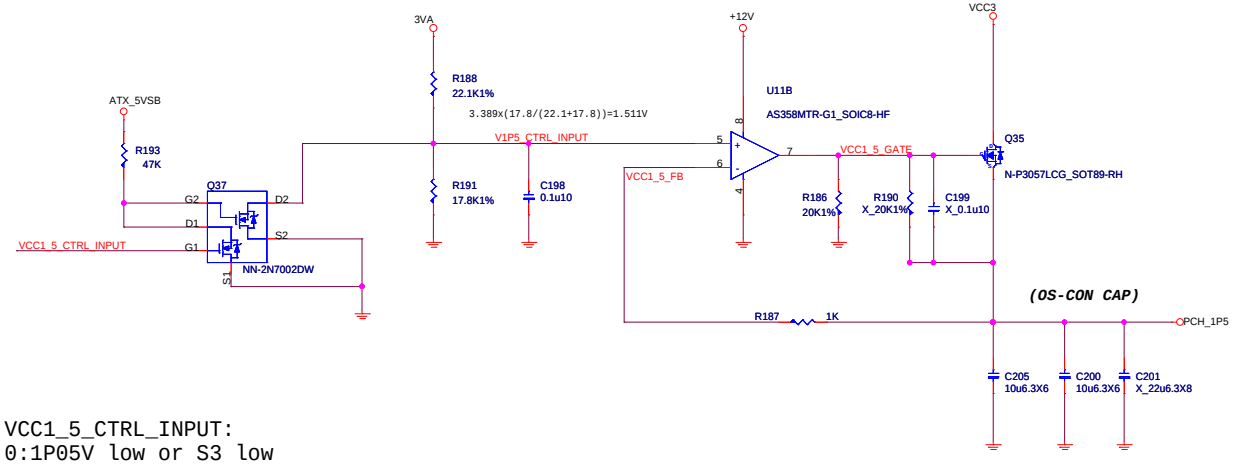




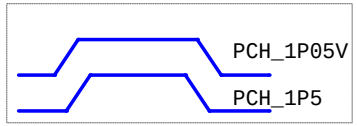
PCH Power:1.5V 0.183A



Ib=(PCH_1P05-Vbe)/R207=0.021mA
Ic=(ATX_5VSB-Vce)/R194=0.24mA
Ic(max)<ß(min)*Ib(min)=0.638mA



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



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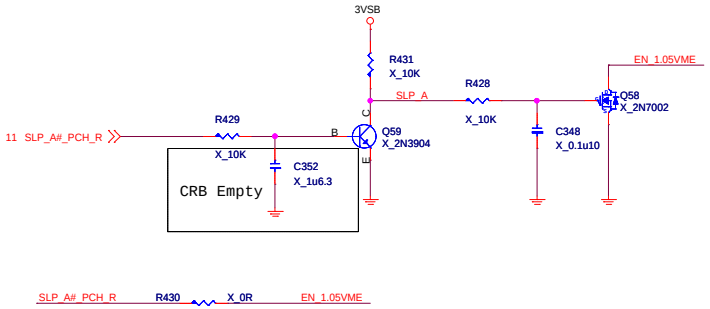
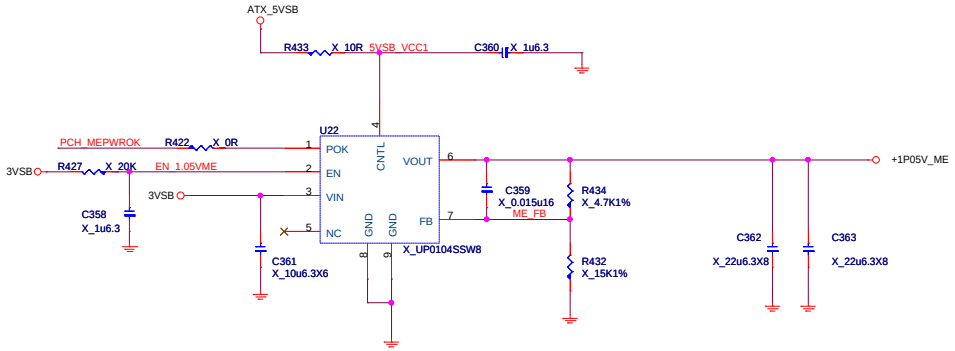
PCH ME Power:1.05V 0.670A

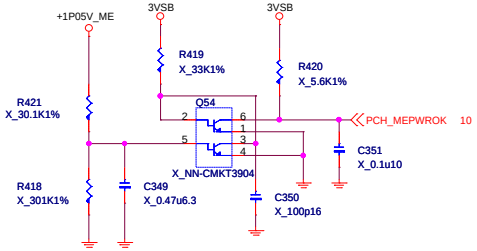
SLP_A

ME Power Control

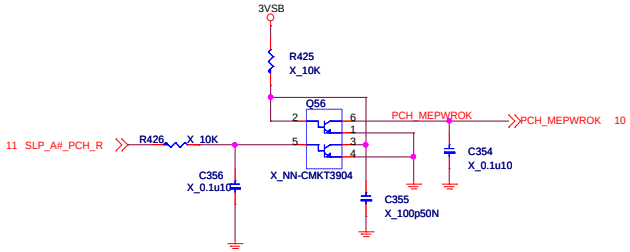




PCH_MEPWROK

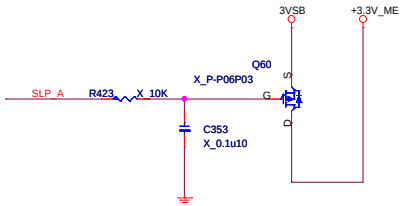


VccASW active to APWROK high 1ms

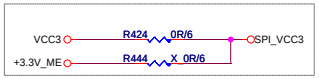


APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME



H81 stuff R424
B85 stuff R444

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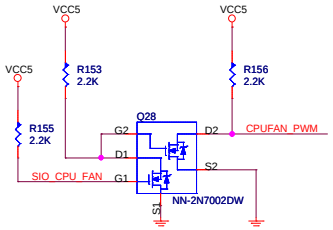
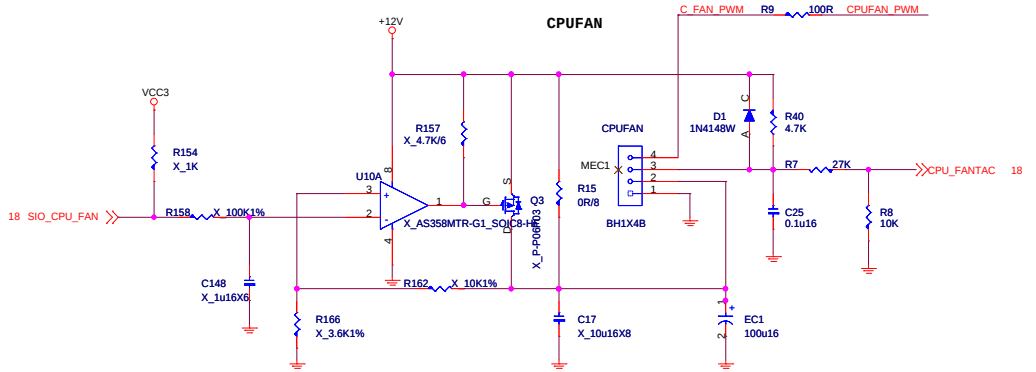
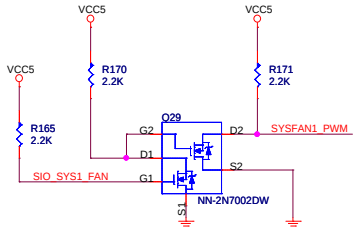
FAN-COUNTROL CIRCUIT

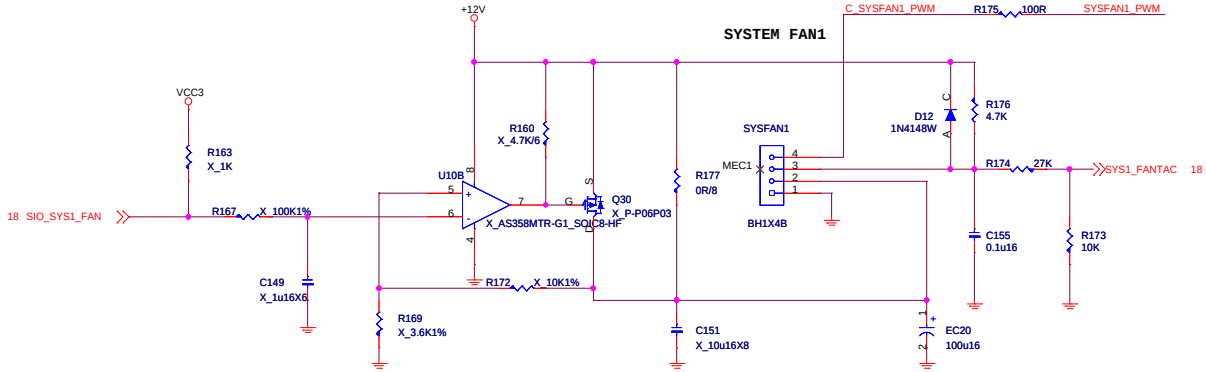


FAN TYPE E

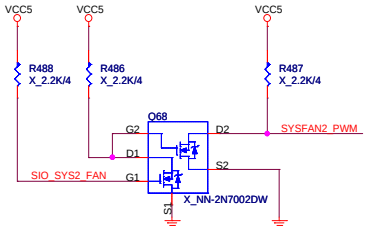


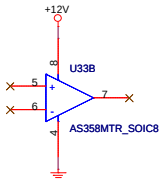
FAN TYPE E

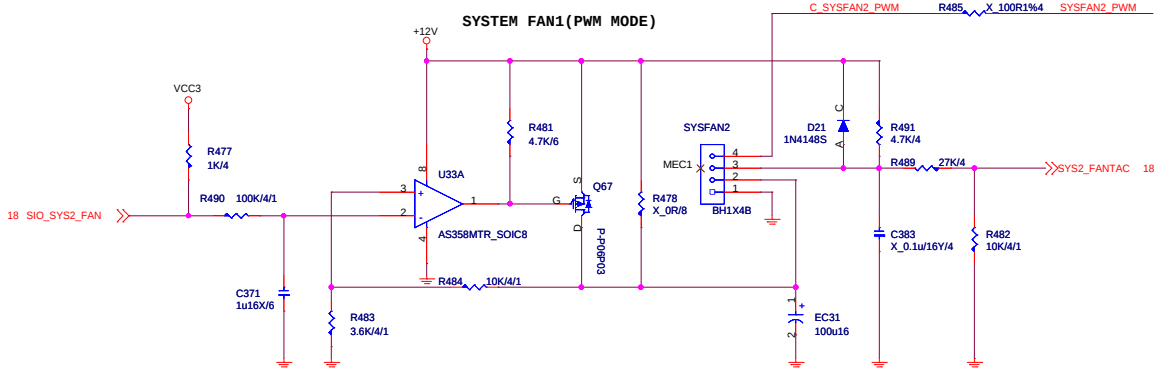




FAN TYPE F







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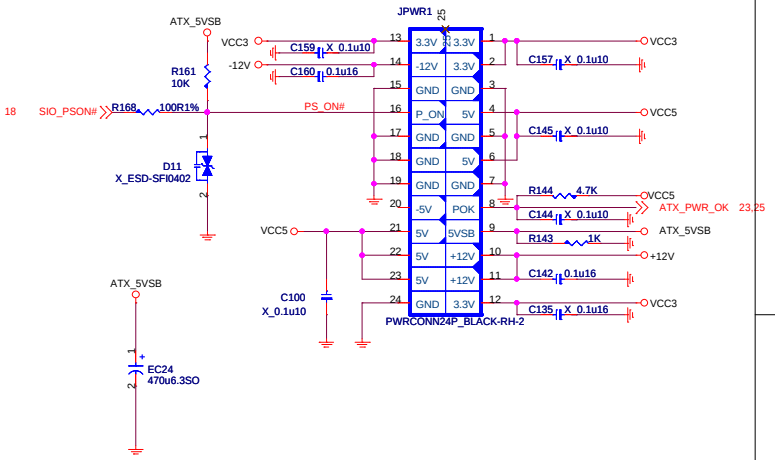
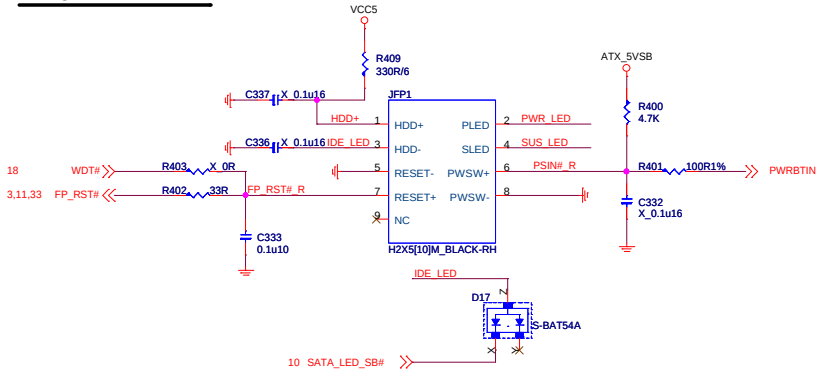
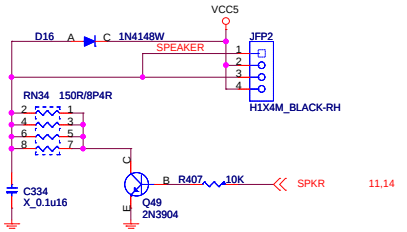
ATX POWER CONNECTOR



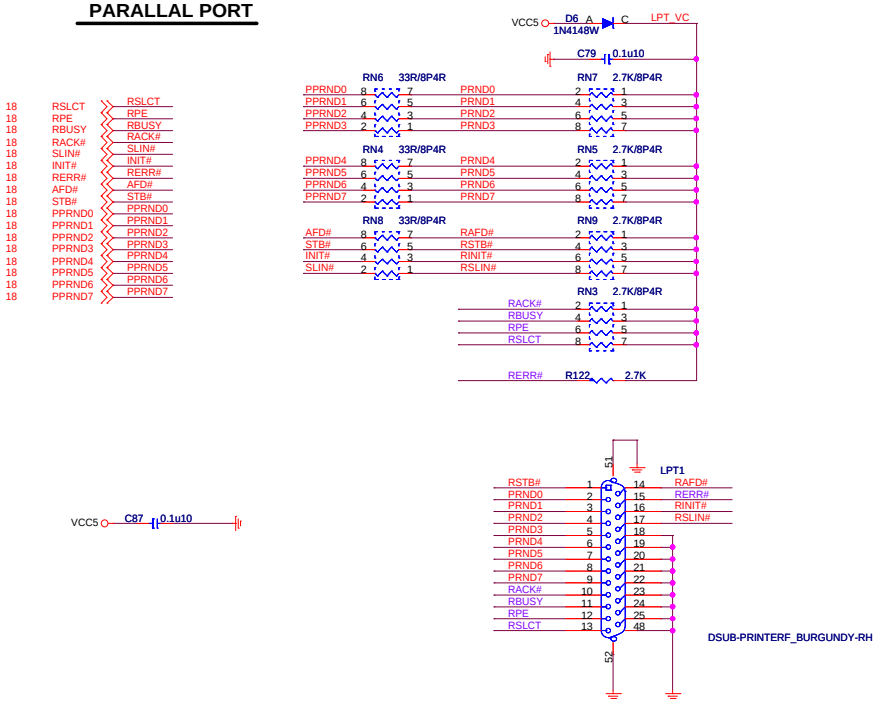
FRONT PANNEL

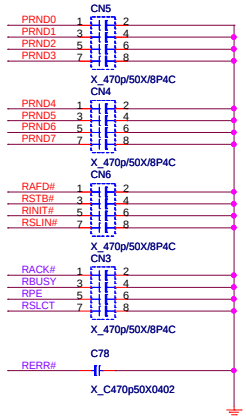


Speaker Pin Header

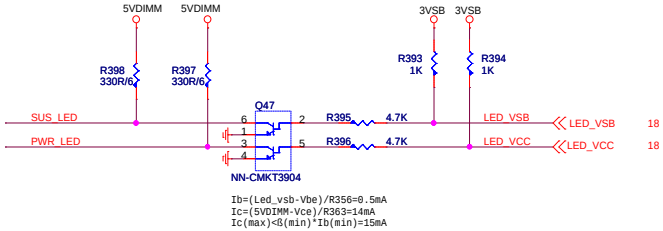


PARALLAL PORT

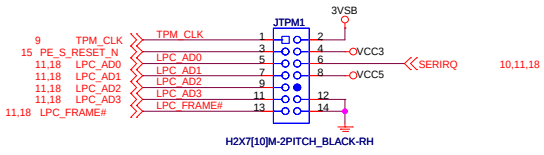




LED (for NV5533)



TPM/JLPC



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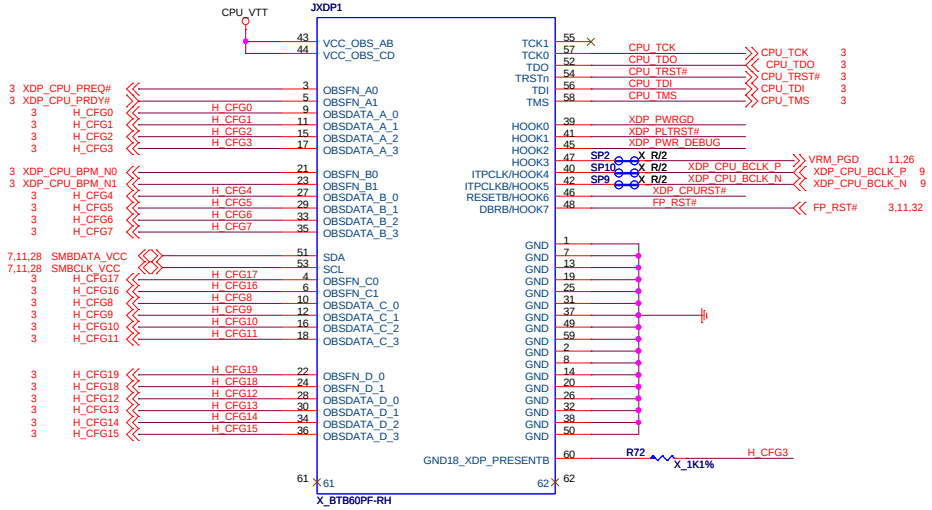
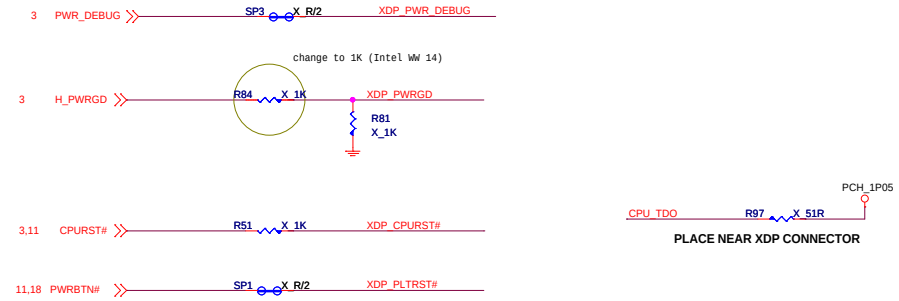
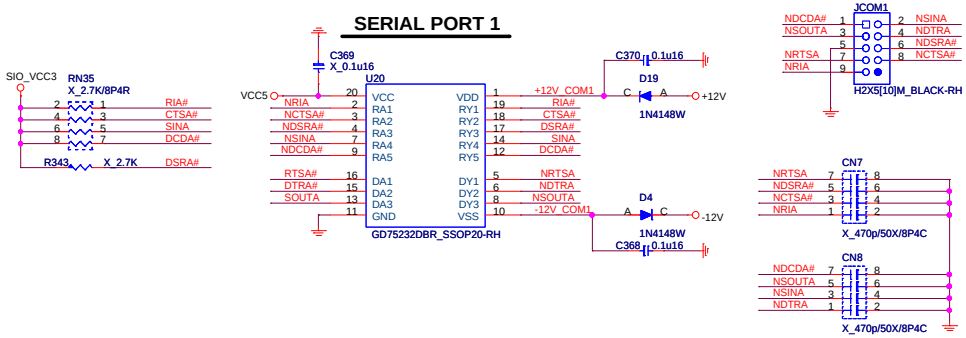
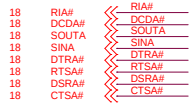
Reserve debug port 5020





SERIAL PORT 1





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SPI OPT.

SPI10
SPI
16M
X_W25Q128FVSIQ-HF

D1000
MOS
X_N-AO3414

CHIPSET OPT.

U1001
H87
X_H87 QS

U1002
B85
X_B85 QS

F100
FAN 3PIN
X_FAN

LABEL OPT.

LABEL100
H87DVI
X_LABEL

LABEL101
H87HDMI
X_LABEL

LABEL103
B85DVI
X_LABEL

LABEL104
B85HDMI
X_LABEL

LABEL105
H81HDMI
X_LABEL

MK1
G51-M1SPE13-Q13

LABEL106
H81DVI_MCJ
X_LABEL

LA3
AMI_BIOS LABLE
X_BIOS_LABLE

BAT1_X1
BAT-BCR2032P-RH

PCB1
7846_21

CPU_H1
CPU
鐵座
CPU_H1

PK0-0784621-G37
PK0-0784621-E48

Simulation

SIM1
VCC5
SIM1
X_PIN1*2

SIM2
SIM2
X_PIN1*2

PCH XDP PWRGD/RESET

HS_PCH1
MEC2
MEC1
HS-0406120-RH

VCCP — CPU_VCCIN
VCC_DDR — VCC_DDR
VTT_DDR — VTT_DDR
PCH_1P05 — PCH_VCORE
PCH_1P5 — PCH_VCCVRM
5VDIMM — 5VDIMM
3VSB — 3VSB
PCH_VCC3 — PCH_VCC3
3VA — 3VA

Optical Fiducial Marks-120

FM1 FM2 FM3 FM4
FM5 FM6 FM7 FM8
X_FM

Mounting Holes

MH1 MH2 MH3 MH4 MH5
X_MH001

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