First International Computer,Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : **MR056B**

Version : 0.1

Initial Date : May. 04 , 2007

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2. PCI & IRQ & DMA Description :
3. Block Diagram :
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Manager Sign by: AVERY

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Total confirm by:

LAN Circuit check by:

Audio Circuit check by:

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1. Schematic Page Description :

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2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI (Wireless LAN)
AD27	X
AD29	Lan (Realtek RTL8101L)

BUSMASTER

REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	LAN (Realtek RTL8101L)
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	~~Serial Port~~
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	~~LPT~~
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	~~Cardbus~~
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	~~ECP~~
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (VIA VT6311S)
IRQB	LAN (Realtek RTL8101L)
IRQC	X
IRQD	X
IRQE / GPIO2	LAN (Realtek RTL8101L)
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

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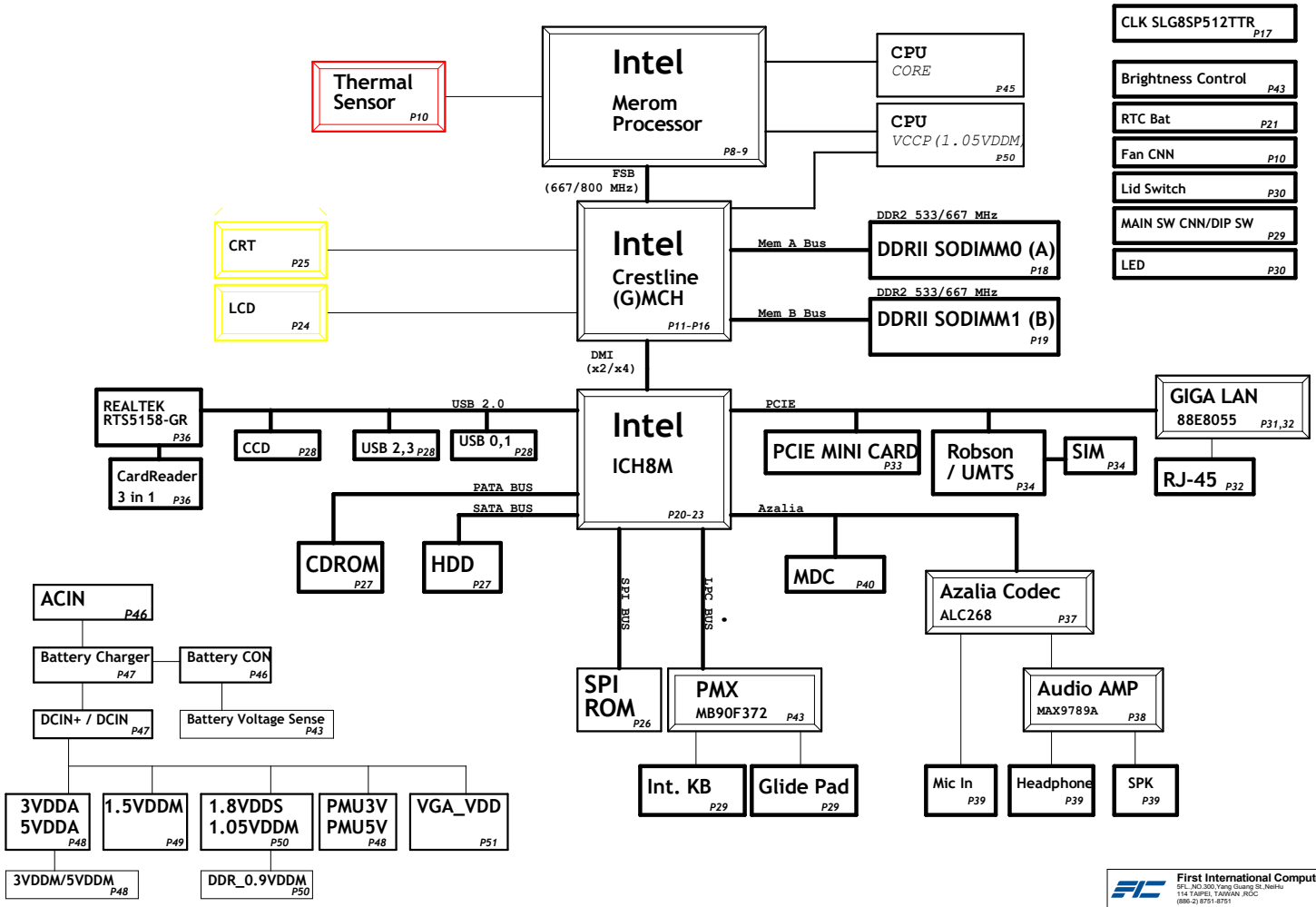
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer(High Speed)
Layer 4	Stripline Layer(High Speed)
Layer 5	Power Plane
Layer 6	Solder Side,Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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6.Schematic modify Item and History :

Power Rail	Ball Name	Destination	Voltage	S0 Current
VCC_CORE		Merom HFM: LFM:	1.0375V~?~1.3000V TBD~TBD	44A TBD
1.05VDDM	VCCP VTT(VCCP) VCC VCC_PEG VCCR_RX_DMI VCC_AXM VCC1_05 VCCSUS1_05 VCCCL1_05 VCCLAN1_05	Merom: AGTL+ termination Crestline: AGTL+ termination Crestline: Core chipset Crestline: PCI Express BasedGraphics Crestline: Rx and I/O Logic forDMI Crestline: Controller Link/ME voltage supply ICH8M: ICH8 Core ICH8M: ICH8M: ICH8M:	1.00V~1.05V~1.10V 0.9975V~1.05V~1.1025V 0.9975V~1.05V~1.1025V	4.5A 0.8A 1.3A
1.25VDDM	VCCA_SM VCCA_SM_CK VCCA_PEG_PLL VCCD_PEG_PLL VCC_DMI VCCA_HPLL VCCD_HPLL VCCA_MPLL VCCA_DPLLA VCCA_DPLLB VCC_AXG VCC_AXF VCC_DMI	Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: Crestline: ICH8M:		
1.5VDDM	VCCA VCCD_QDAC VCCD_TVDAC VCCD_CRT VCCD_QDAC VCC1_5_A VCC1_5_B VCCSUS1_5 VCCGLAN1_5 VCCCL1_5 VCCUSBPLL VCCDMIPLL VCCSATAPLL VCCGLANPLL +1.5V TBD	Merom PLL Crestline: TV DAC Crestline: TV DAC Crestline: CRT Crestline: CRT ICH8M: I/O ICH8M: I/O ICH8M: Resume well I/O ICH8M: Integrated Gigabit LAN I/O ICH8M: Controller Link ICH8M: USB PLL ICH8M: DMI PLL ICH8M: SATA PLL ICH8M: Integrated Gigabit LANPLL Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.7V~1.8V~1.9V	130mA 1.5A 60mA 24mA 320mA
1.8VDDS:	VCC_SM VCC_SM_CK VCCD_LVDS VCC_TX_LVDS VCCA_LVDS 1.8VDDS:	Crestline: I/O Voltage Crestline: Clock I/O Votage Crestline: Crestline: Crestline: SO-DIMM:		3.1A
0.9VDDT_DDRII:		DDRII Terminator:	0.855V~0.9V~0.945V	1.0A

Need Modify

Power Rail	Ball Name	Destination	Voltage	S0 Current
2.5VDDM		945GM: PCIE analog 945GM: LVDS analog 945GM: LVDS I/O 945GM: CRT DAC CH7307:	2.32V~2.5V~2.625V 2.375V~2.5V~2.625V 2.375V~2.5V~2.625V 2.32V~2.5V~2.625V	2mA 10mA 60mA 70mA
3VDDM	VCCA_PEG_BG VCC_HV VCC_SYNC VCCA_CRT_DAC VCCA_TVA_DAC VCCA_TVB_DAC VCCA_TVC_DAC VCCA_DAC_BG	Crestline: PCI Express BaseGraphics Crestline: HV buffer power Crestline: H/VSYNC power Crestline: CRT DAC Crestline: TV Out Crestline: TV Out Crestline: TV Out Crestline: TV DAC ICH7m: Mini Card: Express Card: CLK Generator: ICS954226 KBC: KB3886 Flash ROM: BIOS Azalia Codec: ALC260 Azalia MDC: HDD: SATA	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V	40mA 120mA 400mA
3VDDS		Lan: Broadcom BCM4401 Card Reader: SD/MMC/MS Azalia MDC: For wake up	3.0V~3.3V~3.6V	
3VDDA		ICH7m: ICH7m: ICH7m: LCD:	 3.0V~3.3V~3.6V	 1.0A
5VDDM		Azalia Codec: ALC260 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1420 Inverter:	3.0V~3.3V~3.6V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	 Max: 1.0A ; R/W Max: 1.8A ; R/W: 900mA
5VDDS		USB: x 4 ports	5V	2.0A
PMU3V		EC: PMU08 ICH7m: RTC		

Page22 RF_ON# change to RF_ON
Page22 UMTS_ON change to UMTS_OFF#
Page43 VOR0 change to VOR#

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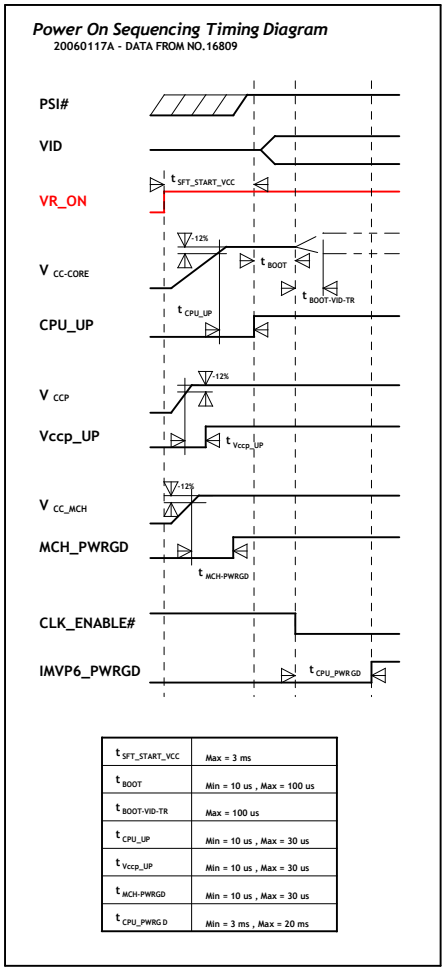
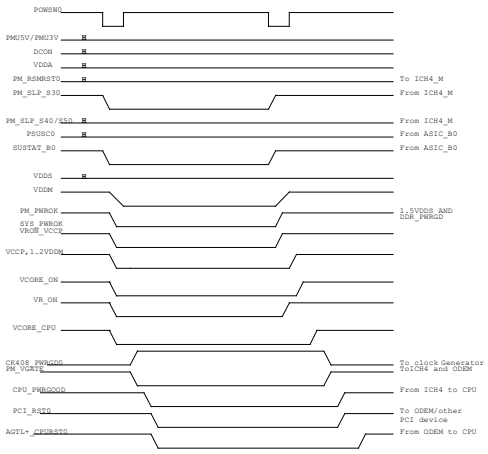
7. power on & off & S3 Sequence :

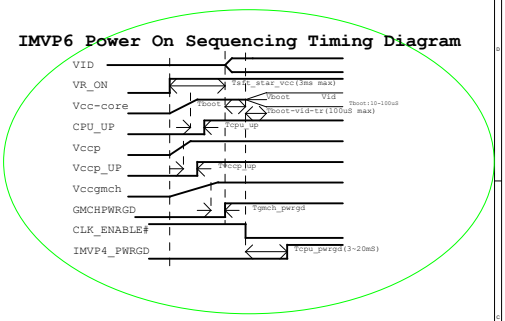


$t_{SFT\_START\_VCC}$	Max = 3 ms
t_{BOOT}	Min = 10 us , Max = 100 us
$t_{BOOT-VID-TR}$	Max = 100 us
t_{CPU_UP}	Min = 10 us , Max = 30 us
t_{Vccp_UP}	Min = 10 us , Max = 30 us
$t_{MCH-PWRGD}$	Min = 10 us , Max = 30 us
t_{CPU_PWRGD}	Min = 3 ms , Max = 20 ms

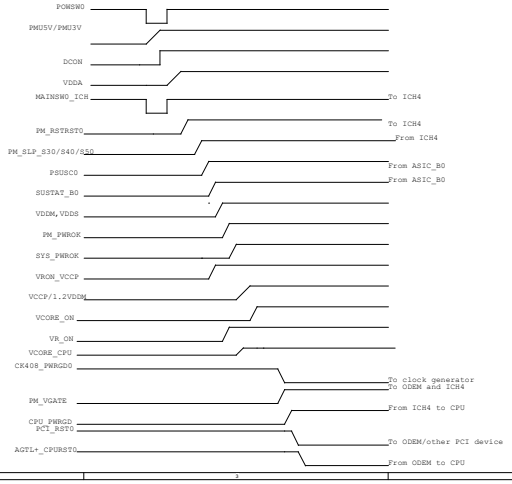
S3 SUSPEND AND RESUME TIMING



IMVP6 Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



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8. Layout Guideline :

Crestline DDRII Layout Guidelines

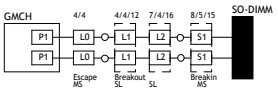
DDRII Signal Groups

Group	Signal Name
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SA_DQS#[7..0] SB_DQS[7..0]/SB_DQS#[7..0]
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#
Control	SM_CS#[3..0] SM_CKE[3..0] SM_ODT[3..0]
Clock	SM_CK[3..0] SM_CK#[3..0]
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : SM_CK[3..0],SM_CK#[3..0]

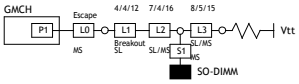


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA_RCVENIN#,SA_RCVENOUT#,SB_RCVENIN#,B_RCVENOUT#

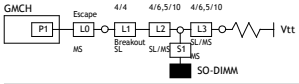
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



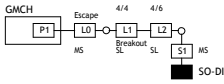
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



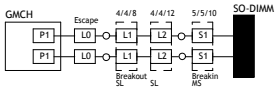
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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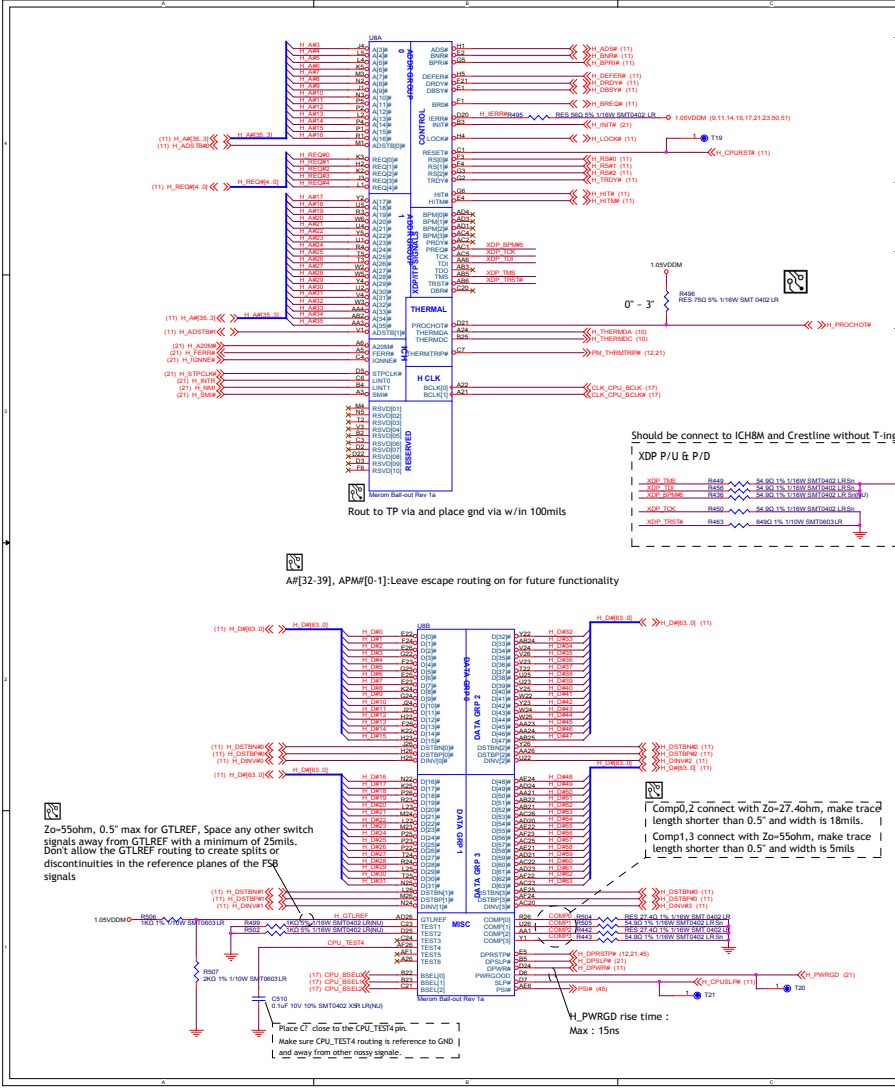
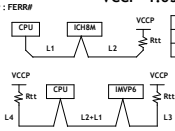


VCCP=1.05VDDM

Topology : FERR#



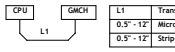
L1	L2	Rtt	Transmission Line
0.5" ~ 12"	0" ~ 3.0"	56 +/-5%	Microstrip
0.5" ~ 12"	0" ~ 3.0"	56 +/-5%	Stripline

L1	L2	L3	L4	Rtt	Transmission Line
0.5" ~ 6.5"	0.5" ~ 6.5"	0" ~ 3.0"	0" ~ 3.0"	75 +/-5%	Micro-strip
0.5" ~ 6.5"	0.5" ~ 6.5"	0" ~ 3.0"	0" ~ 3.0"	75 +/-5%	Strip-line

Topology : PWRGOOD

L1	Transmission Line
0.5" ~ 12"	Micro-strip
0.5" ~ 12"	Strip-line

Topology : CPUSLP#

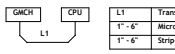


L1	Transmission Line
0.5" ~ 12"	Micro-strip
0.5" ~ 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SM# , STPCLK#

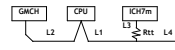
L1	Transmission Line
0.5" ~ 12"	Micro-strip
0.5" ~ 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" ~ 6"	Micro-strip
1" ~ 6"	Strip-line

Topology : THERMTRIP#



L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" ~ 12"	1" ~ 6"	1" ~ 12"	0" ~ 3.0"	0" ~ 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" ~ 12"	1" ~ 6"	1" ~ 12"	0" ~ 3.0"	0" ~ 3.0"	24 +/-5%	56 +/-5%	Strip-line

Processor ITP Signal Default Strapping When ITP-XDP & ITP700FLEX Dedbug Port Not Used.

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

FSB Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#,			
Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	4 & 8 mils
Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 8 mils	N/A
DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils
DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	4 & 12 mils	4 & 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 200 mils
A#[31..17]	+/- 200 mils	ADSTB1#	+/- 200 mils

*** No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#[31..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils
ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	4 & 8 mils

(9,11,14,15,17,21,23,50,51) 1.05VDDM → 1.05VDDM

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Size	Document Number	Rev
C	Merom Processor (1/ 2)	0.1

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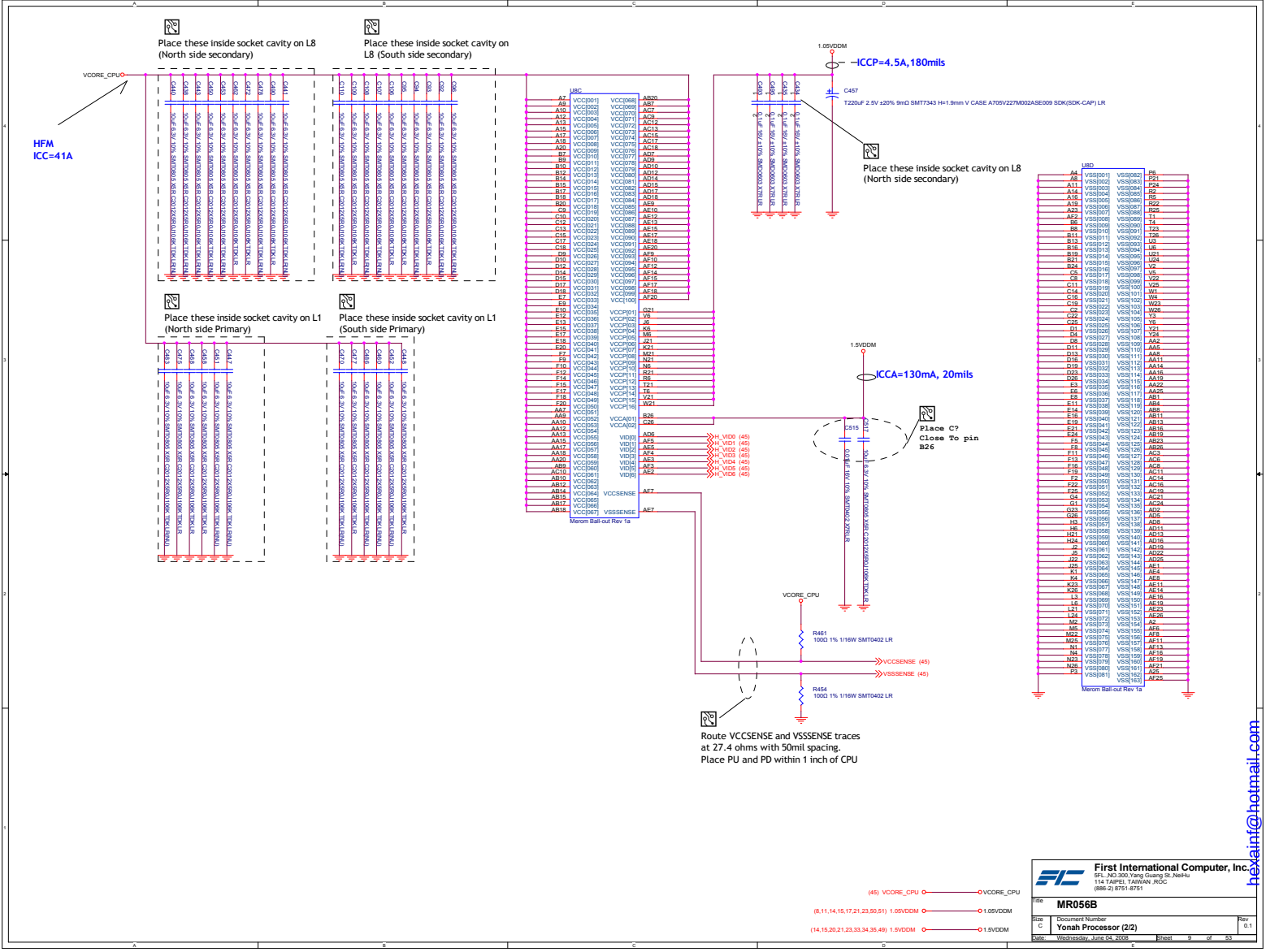

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Size: C	Document Number: Yonah Processor (2/2)	Rev: 0.1
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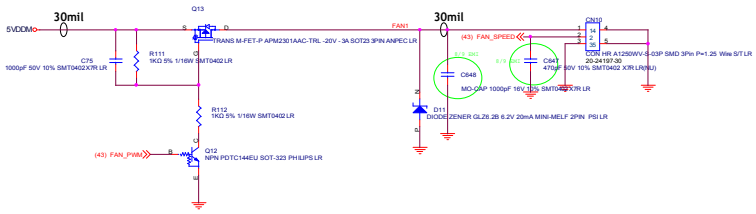
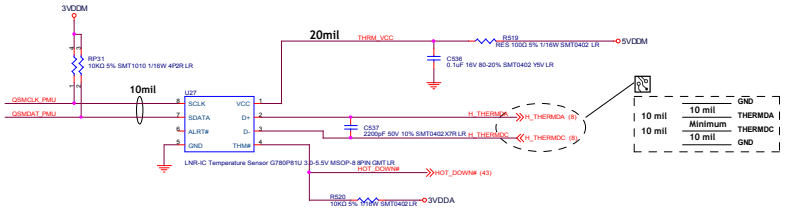
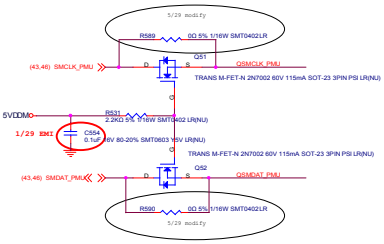


THERMAL SENSOR





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Size	Document Number	Rev
C	CPU Thermal	0.1

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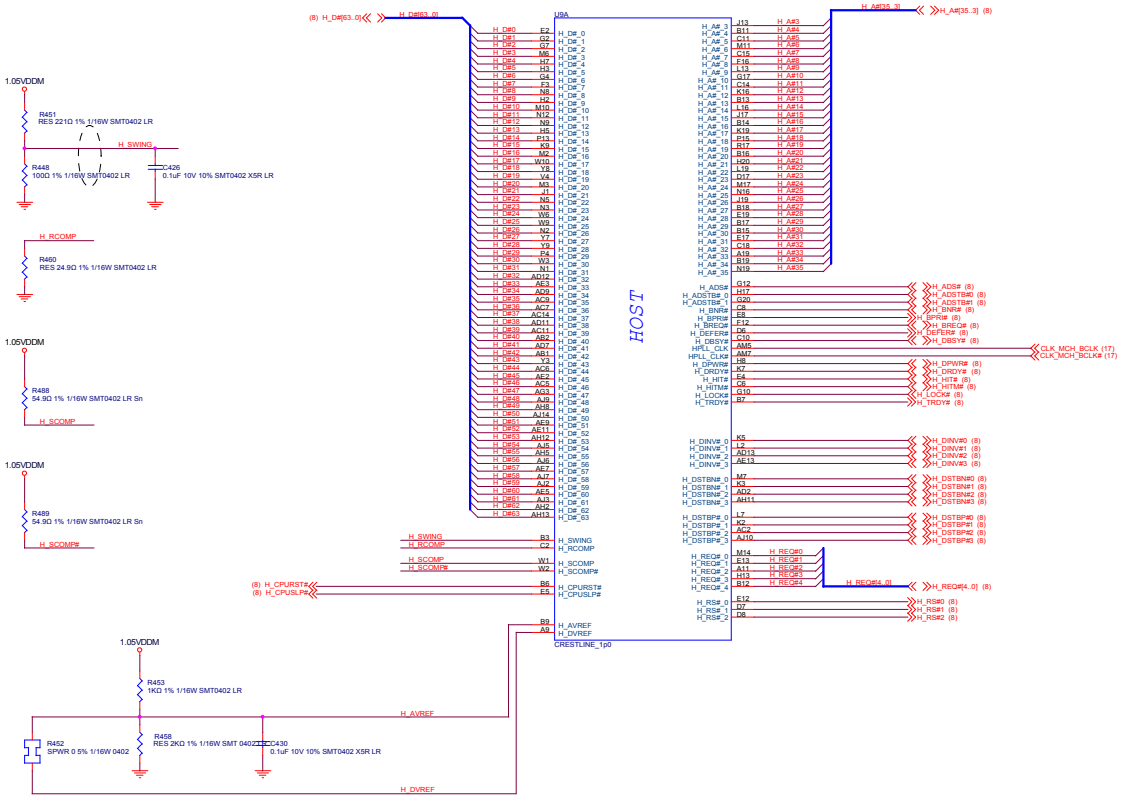
NB GL960 : 05-23843-01
NB GM965 : 05-23798-01 (REV. C0)



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Size: C | Document Number: Crestline Host (1/6) | Rev: 0.1

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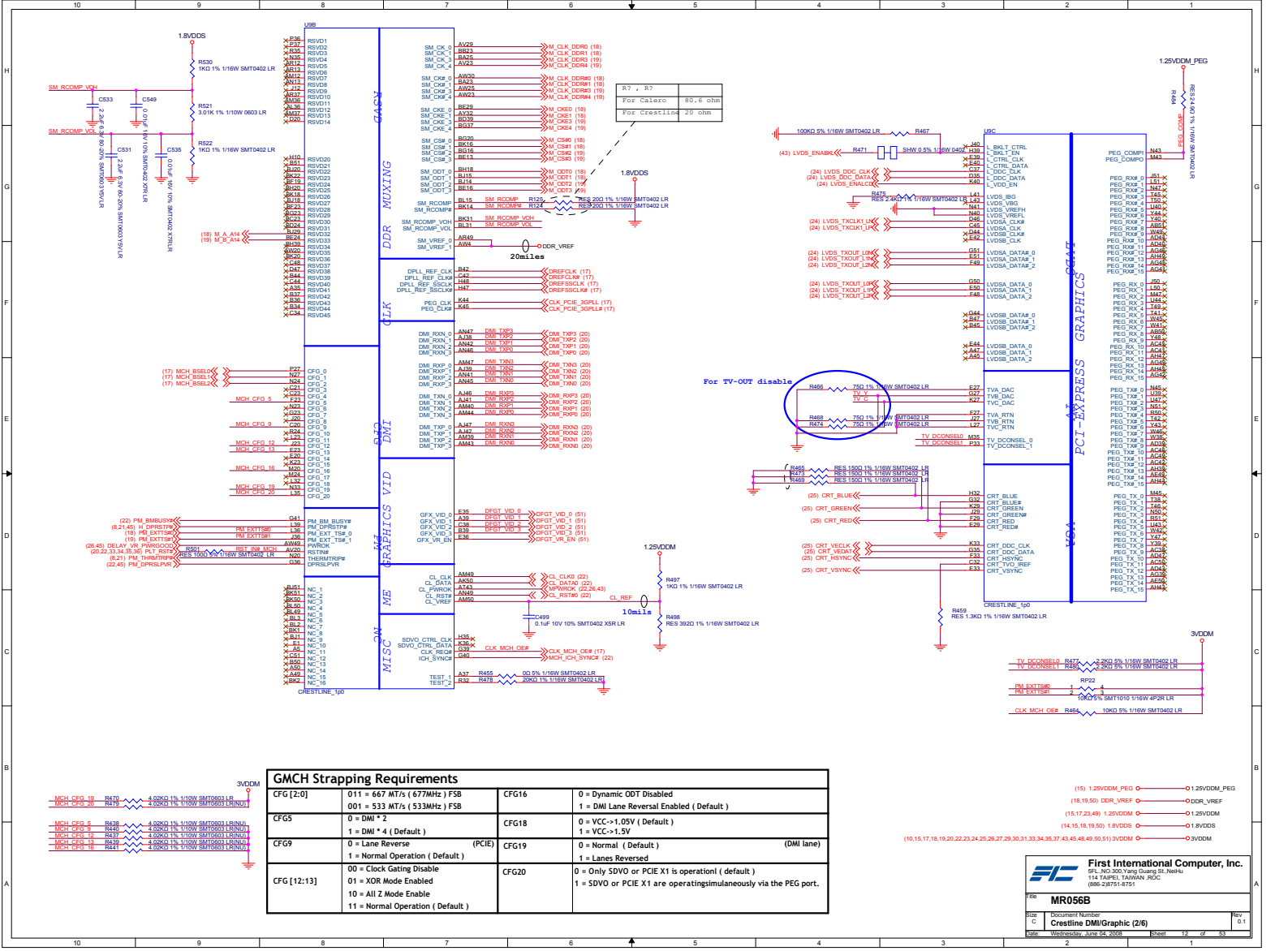

GMCH Strapping Requirements

CFG [2:0]	011 = 667 MT/s (677MHz) FSB 001 = 533 MT/s (533MHz) FSB	CFG16	0 = Dynamic ODT Disabled 1 = DMI Lane Reversal Enabled (Default)
CFG5	0 = DMI * 2 1 = DMI * 4 (Default)	CFG18	0 = VCC->1.05V (Default) 1 = VCC->1.5V
CFG9	0 = Lane Reverse (PCIE) 1 = Normal Operation (Default)	CFG19	0 = Normal (Default) (DMI lane) 1 = Lanes Reversed
CFG [12:13]	00 = Clock Gating Disable 01 = XOR Mode Enabled 10 = All Z Mode Enable 11 = Normal Operation (Default)	CFG20	0 = Only SDVO or PCIE X1 is operation! (default) 1 = SDVO or PCIE X1 are operatingsimulaneously via the PEG port.

(15) 1.25VDDM_PEG → 1.25VDDM_PEG
(18,19,50) DDR_VREF → DDR_VREF
(15,17,23,49) 1.25VDDM → 1.25VDDM
(14,15,18,19,50) 1.8VDDS → 1.8VDDS
(10,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM → 3VDDM

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Size	Document Number	Rev
C	Crestline DMI/Graphic (2/6)	0.1

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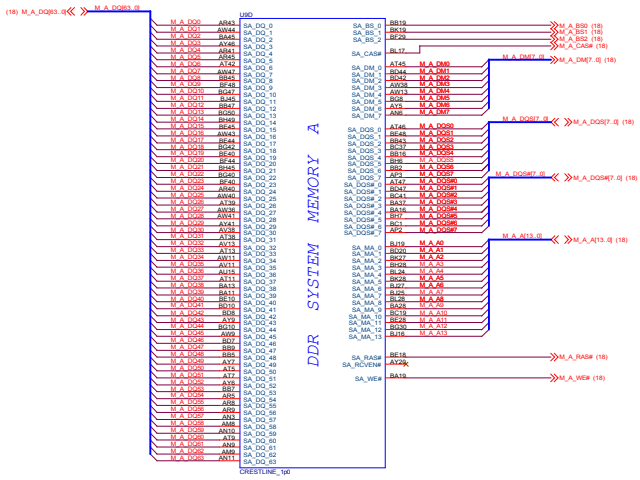
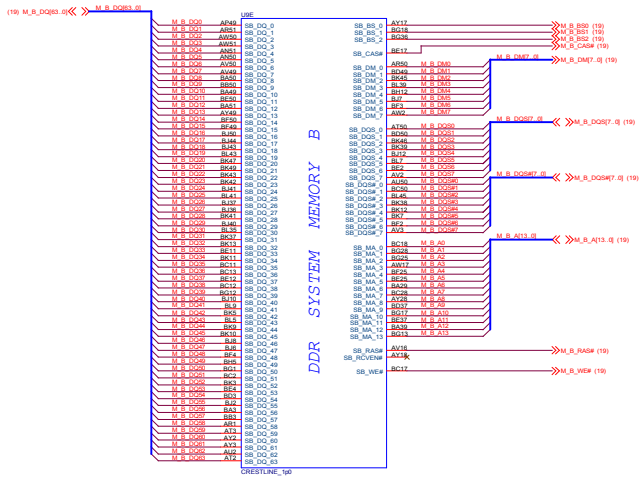
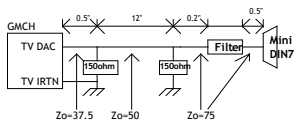




TV DAC Routing Guideline

1. The minimum spacing between each RGB is 40-mils while 50-mils is preferred
2. RGB signals should be routed on the same layer, have a similar number of bends, same number of vias
3. All routing should be done with ground referencing as well
4. TV DAC route lengths should be lenght match to within 200 mils



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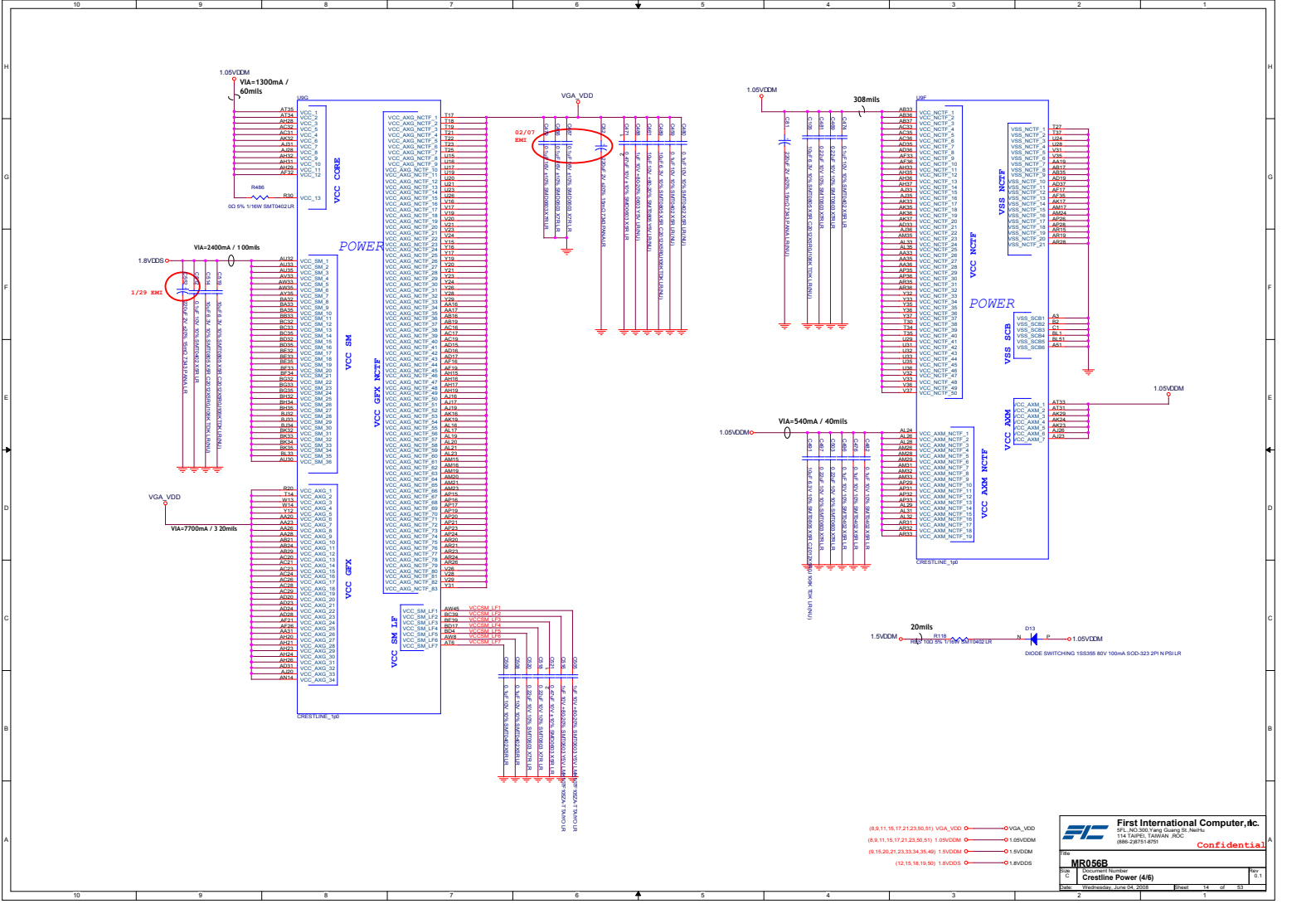
1.05VDDM
VIA=1300mA / 60mils
U9G
VCC_CORE
R486
00 5% 1/16W SMT0402 LR
VIA=2400mA / 100mils
1.8VDDS
1/29 EMI
VCC_SM
VCC_GFX_NCTF
VGA_VDD
VIA=7700mA / 320mils
VCC_GFX
VCC_SM_LF
CRESTLINE_1p0
POWER
02/07 EMI
1.05VDDM
308mils
U9F
VCC_NCTF
VSS_NCTF
VSS_SCB
VCC_AXM_NCTF
VCC_AXM
VIA=540mA / 40mils
20mils
R118
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PI N PSI LR
(8,9,11,15,17,21,23,50,51) VGA_VDD
(8,9,11,15,17,21,23,50,51) 1.05VDDM
(9,15,20,21,23,33,34,35,49) 1.5VDDM
(12,15,18,19,50) 1.8VDDS
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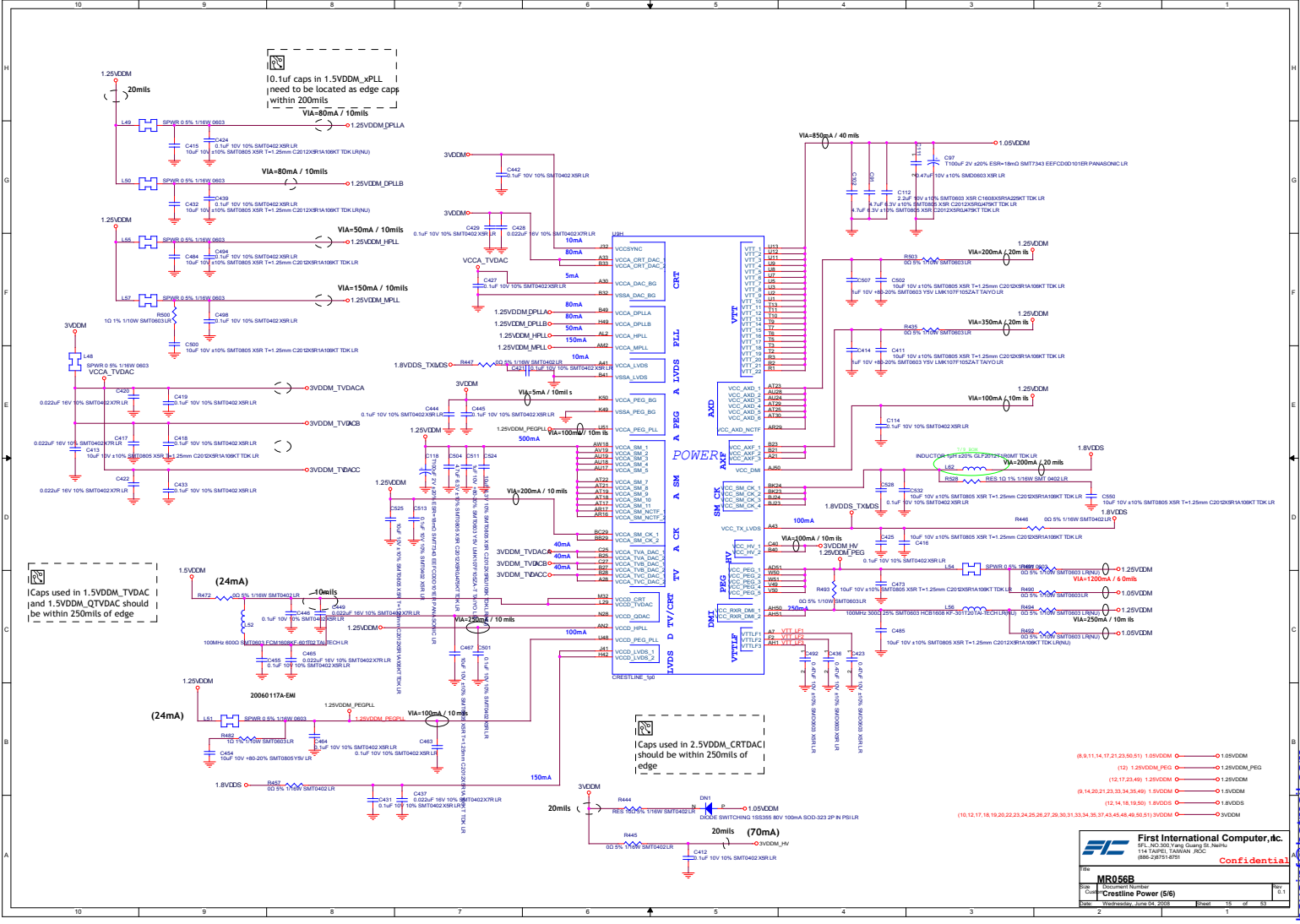

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Size: A3	Document Number: Crestline Power (5/6)	Rev: 0.1
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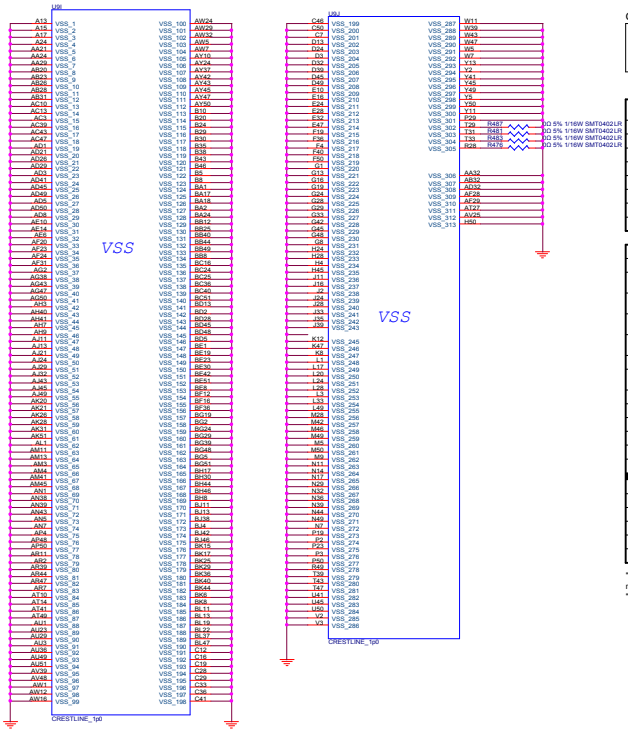
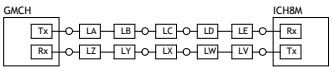


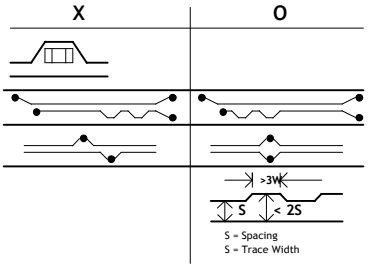
DMI Routing Guideline



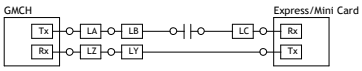
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over Voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



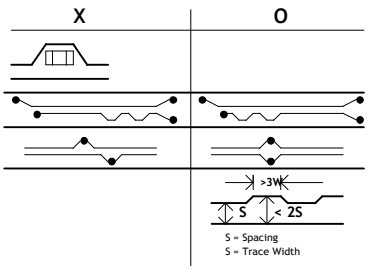
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



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C	Crestline Ground (6/6)	0.1

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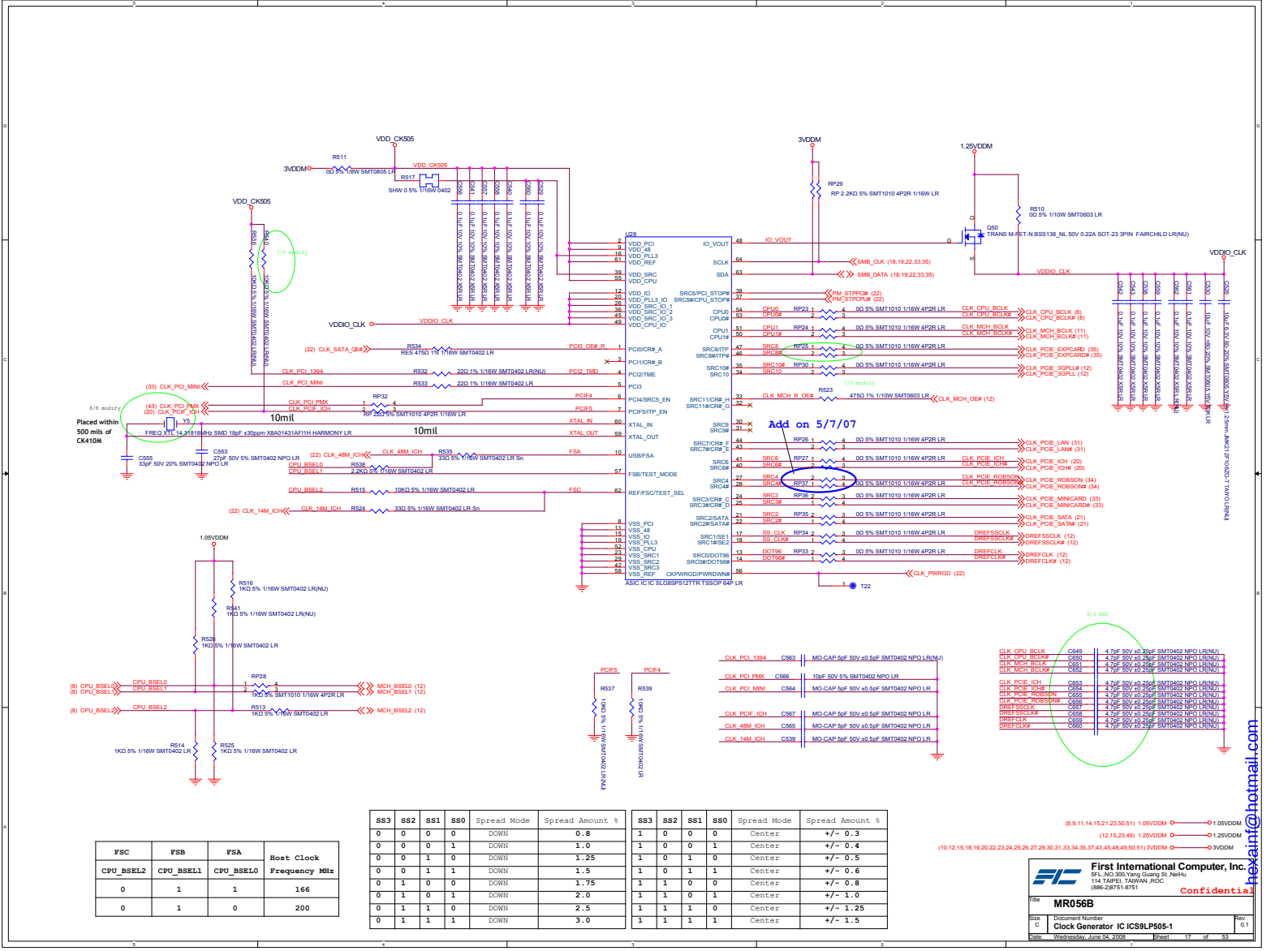
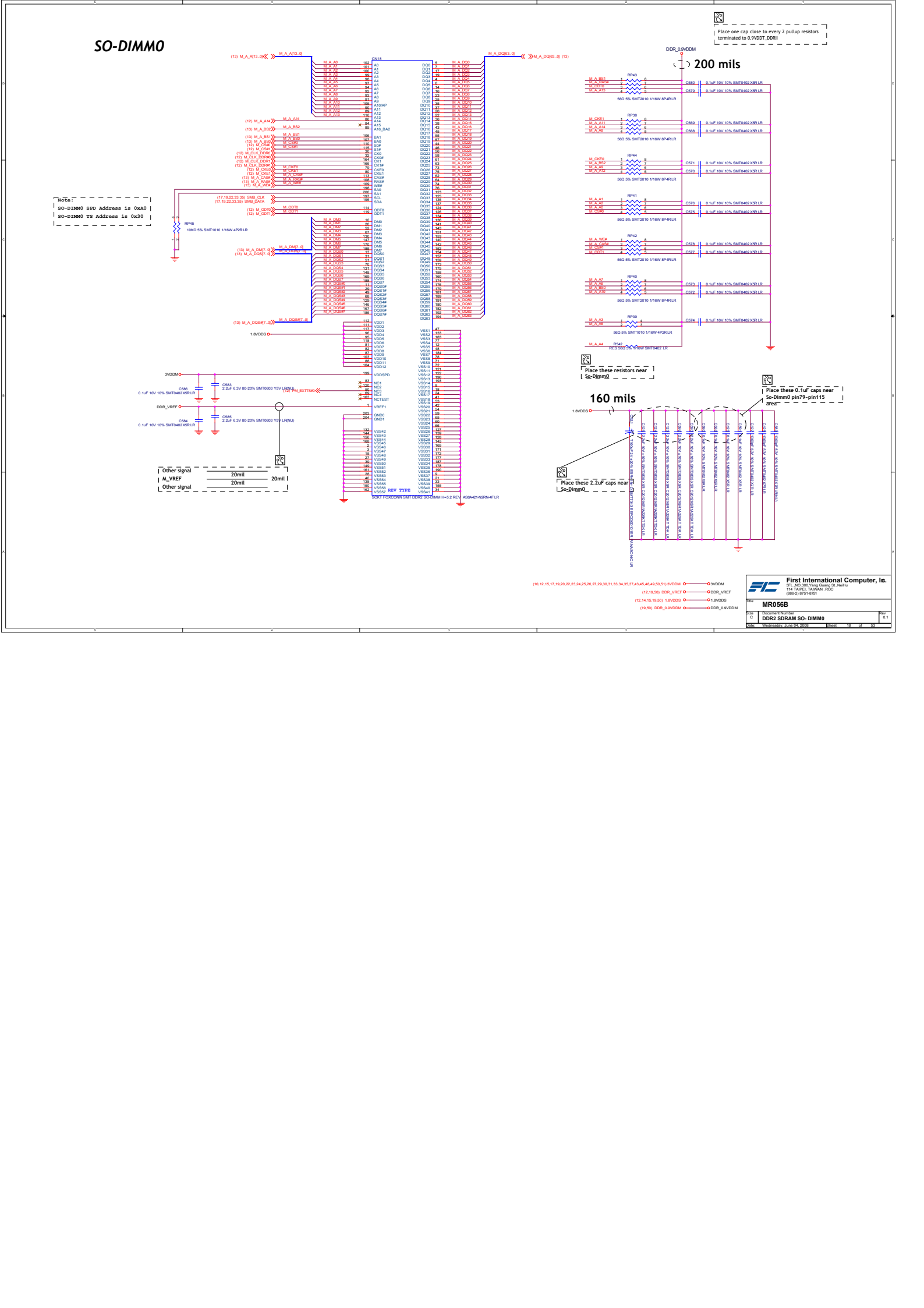


FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHz
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

SO-DIMM0


Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII
DDR_0.9VDDM
200 mils
Note:
SO-DIMM0 SPD Address is 0xA0
SO-DIMM0 TS Address is 0x30
Place these resistors near So-Dimm0
Place these 0.1uF caps near So-Dimm0 pin79-pin115 area
160 mils
Place these 2.2uF caps near So-Dimm0
Other signal
M_VREF
Other signal
20mil
20mil
SCKT FOXCONN SMT DDR2 SO-DIMM H=5.2 REV: AS9A421-N2RN-4F LR
REV TYPE
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MR056B
DDR2 SDRAM SO- DIMM0
Size C
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Rev 0.1
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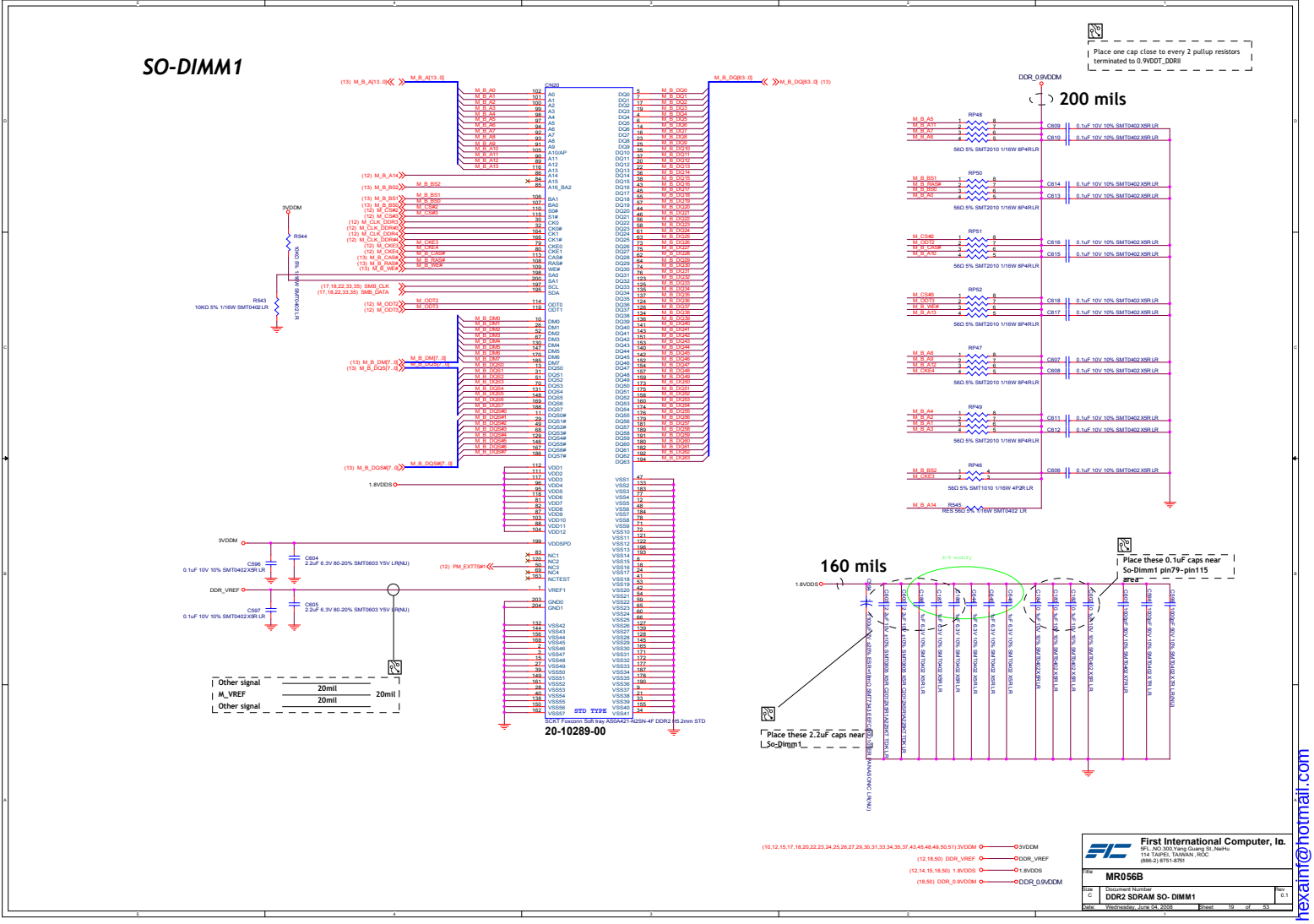
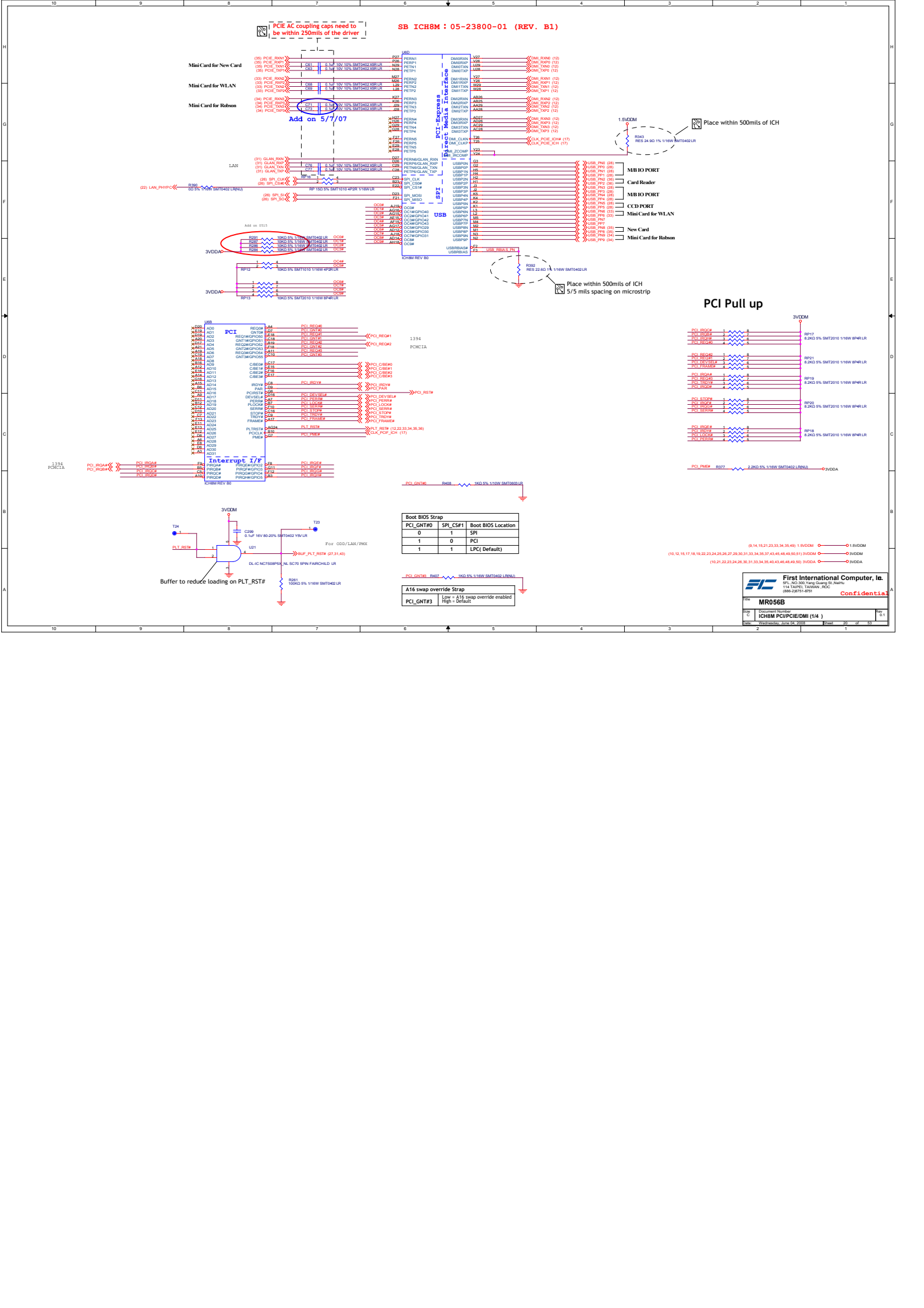
SO-DIMM1




SB ICH8M：05-23800-01 (REV. B1)
PCIE AC coupling caps need to be within 250mils of the driver
Mini Card for New Card
Mini Card for WLAN
Mini Card for Robson
Add on 5/7/07
LAN
PCI-Express Interface
SPI Interface
USB
ICH8M REV B0
Place within 500mils of ICH
1.5VDDM
M/B IO PORT
Card Reader
M/B IO PORT
CCD PORT
Mini Card for WLAN
New Card
Mini Card for Robson
3VDDAO
Place within 500mils of ICH
5/5 mils spacing on microstrip
PCI Pull up
PCI
Interrupt I/F
1394
PCMCIA
Buffer to reduce loading on PLT_RST#
For ODD/LAN/PMX
Boot BIOS Strap
PCI_GNT#0 PCI_CS#1 Boot BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override Strap
PCI_GNT#3 Low = A16 swap override enabled High = Default
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MR056B
ICH8M PCI/PCIE/DMI (1/4)
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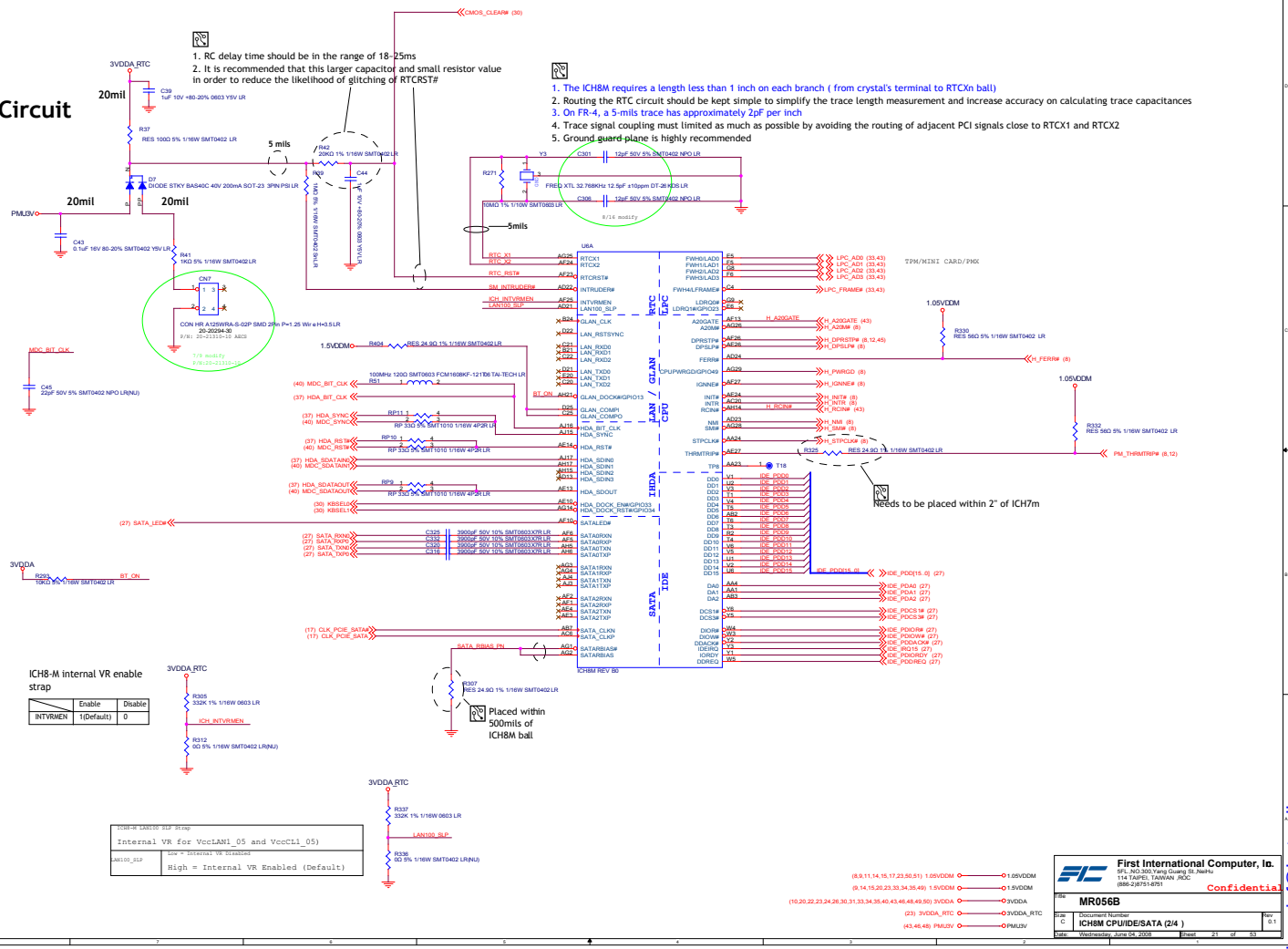
RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH8M requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



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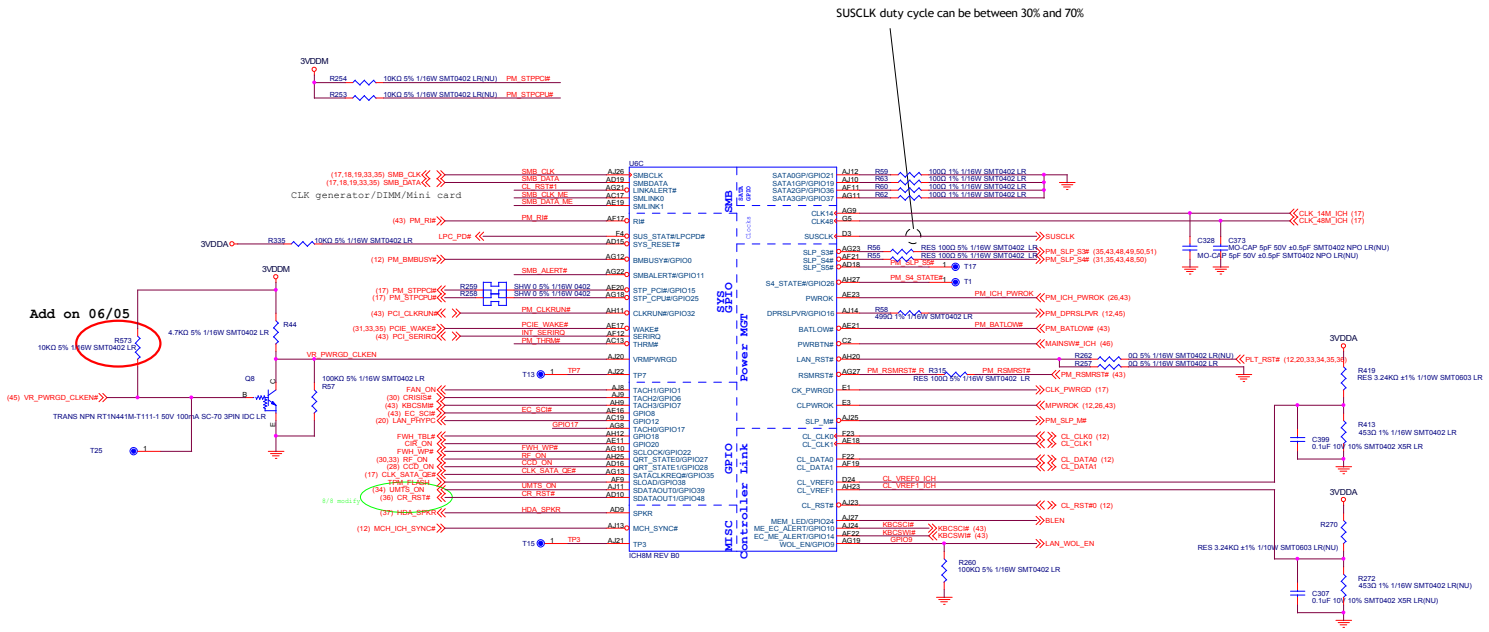
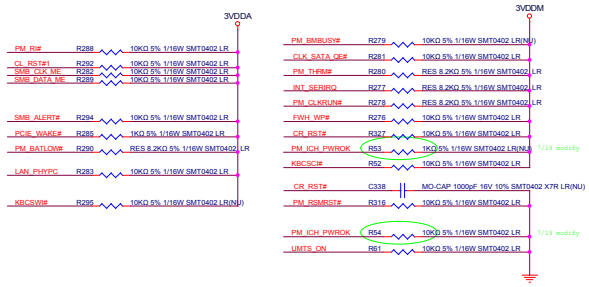


ACZ_SPKR	No stuff : by default Stuff : For NO reboot

HDA_SPKR R275 1KΩ 5% 1/16W SMT0402 LR(NU)

ICH8-M Pullups



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	MR056B			
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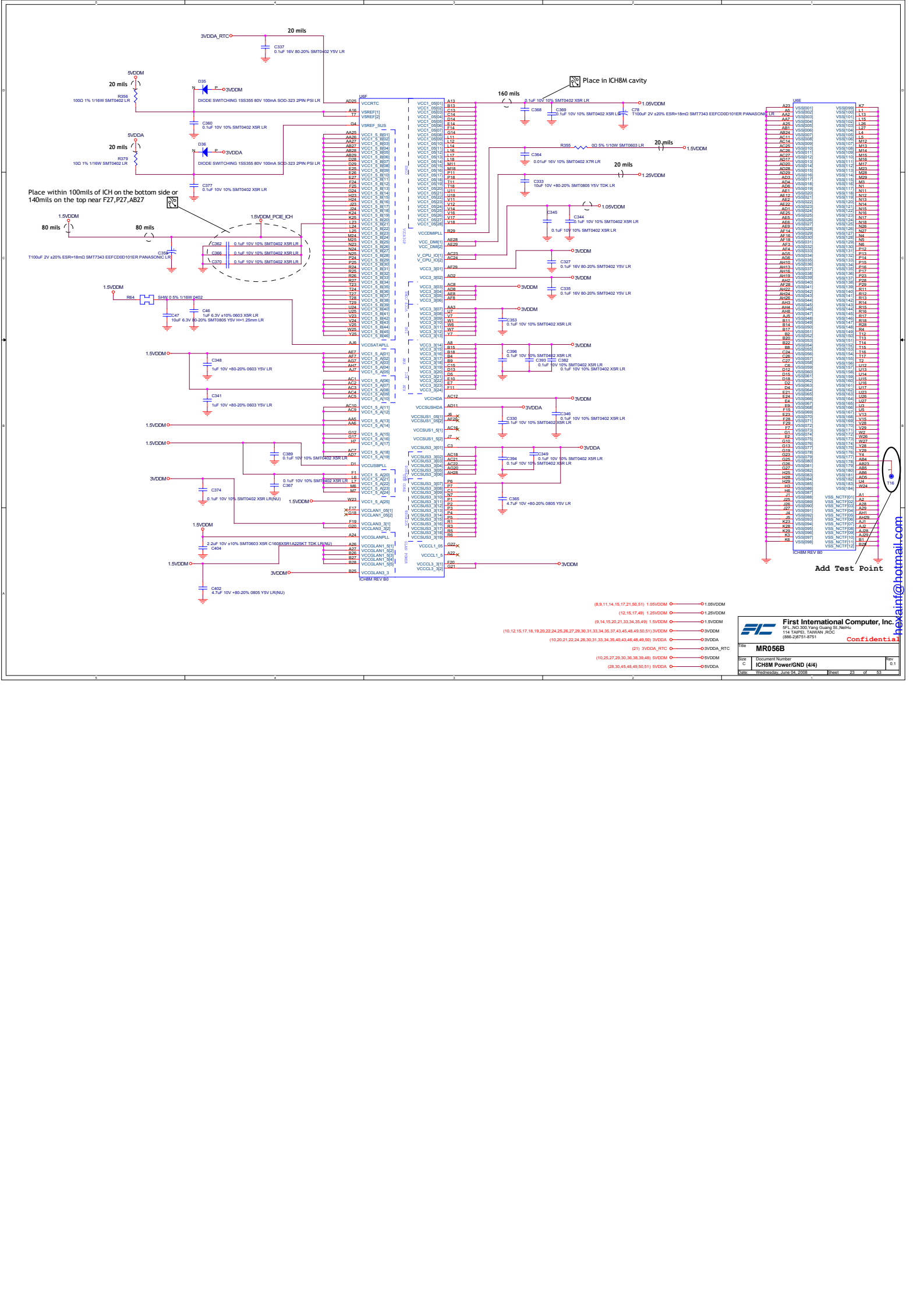
3VDDA_RTC
20 mils
C337
0.1uF 16V 80-20% SMT0402 Y5V LR
5VDDM
20 mils
R356
100Ω 1% 1/16W SMT0402 LR
D35
3VDDM
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
C360
0.1uF 10V 10% SMT0402 X5R LR
5VDDA
20 mils
R379
10Ω 1% 1/16W SMT0402 LR
D36
3VDDA
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR
C377
0.1uF 10V 10% SMT0402 X5R LR
Place within 100mils of ICH on the bottom side or
140mils on the top near F27,P27,AB27
1.5VDDM
80 mils
80 mils
1.5VDDM_PCIE_ICH
C358
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR
C362
C366
C370
0.1uF 10V 10% SMT0402 X5R LR
R64
SHW 0.5% 1/16W 0402
C47
10uF 6.3V 80-20% SMT0805 Y5V H=1.25mm LR
C46
1uF 6.3V ±10% 0603 X5R LR
C348
1uF 10V +80-20% 0603 Y5V LR
C341
1uF 10V +80-20% 0603 Y5V LR
C389
0.1uF 10V 10% SMT0402 X5R LR
C374
0.1uF 10V 10% SMT0402 X5R LR(NU)
C367
0.1uF 10V 10% SMT0402 X5R LR
C404
2.2uF 10V ±10% SMT0603 X5R C1608X5R1A225KT TDK LR(NU)
C402
4.7uF 10V +80-20% 0805 Y5V LR(NU)
U8F
ICH8M REV B0
Place in ICH8M cavity
160 mils
C368
0.1uF 10V 10% SMT0402 X5R LR
C369
0.1uF 10V 10% SMT0402 X5R LR
1.05VDDM
C78
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR
R355
0Ω 5% 1/10W SMT0603 LR
20 mils
1.5VDDM
C364
0.01uF 16V 10% SMT0402 X7R LR
20 mils
1.25VDDM
C333
10uF 10V +80-20% SMT0805 Y5V TDK LR
C345
C344
0.1uF 10V 10% SMT0402 X5R LR
0.1uF 10V 10% SMT0402 X5R LR
C327
0.1uF 16V 80-20% SMT0402 Y5V LR
C335
0.1uF 16V 80-20% SMT0402 Y5V LR
C353
0.1uF 10V 10% SMT0402 X5R LR
C396
0.1uF 10V 10% SMT0402 X5R LR
C393
C382
0.1uF 10V 10% SMT0402 X5R LR
0.1uF 10V 10% SMT0402 X5R LR
C346
0.1uF 10V 10% SMT0402 X5R LR
C330
0.1uF 10V 10% SMT0402 X5R LR
C394
0.1uF 10V 10% SMT0402 X5R LR
C349
0.1uF 10V 10% SMT0402 X5R LR
C365
4.7uF 10V +80-20% 0805 Y5V LR
U8E
T16
Add Test Point
(8,9,11,14,15,17,21,50,51) 1.05VDDM
(12,15,17,49) 1.25VDDM
(9,14,15,20,21,33,34,35,49) 1.5VDDM
(10,12,15,17,18,19,20,22,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM
(10,20,21,22,24,26,30,31,33,34,35,40,43,46,48,49,50) 3VDDA
(21) 3VDDA_RTC
(10,25,27,29,30,36,38,39,48) 5VDDM
(28,30,45,48,49,50,51) 5VDDA
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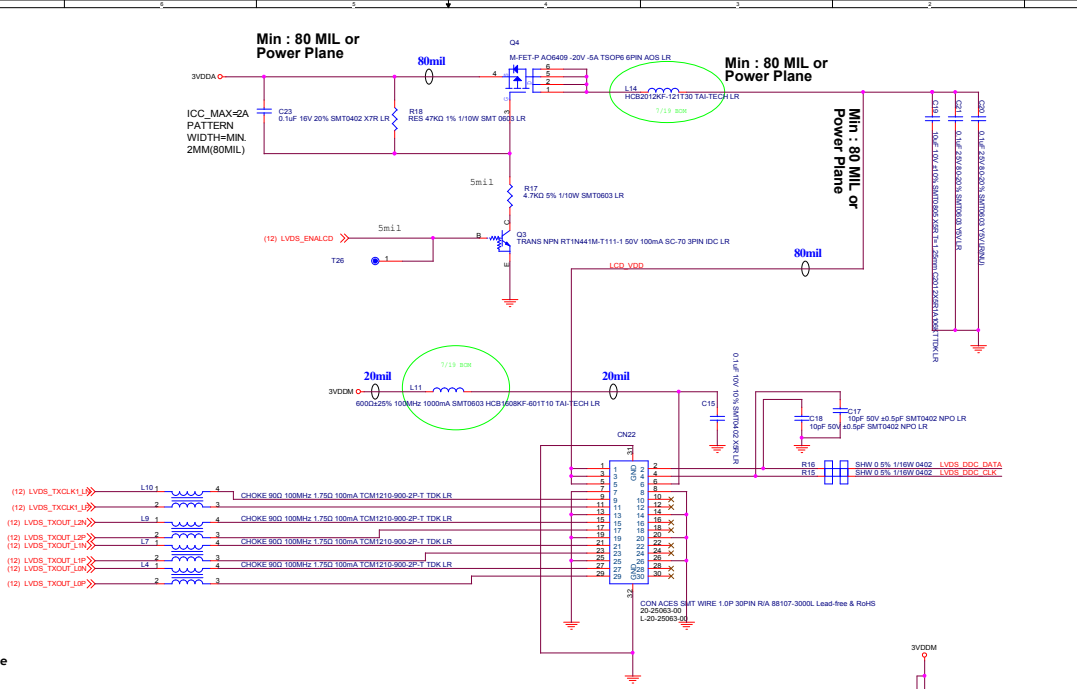
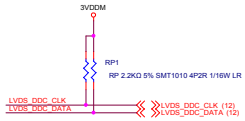
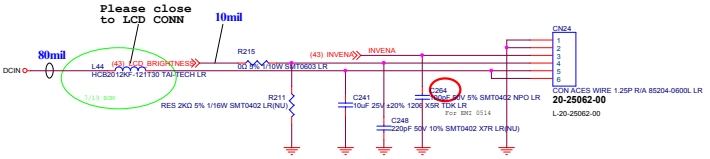
LVDS Interface







LVDS Signal Group Routing Guideline

GMCH

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	**4 mils**
Nominal Pair Spacing (Edge to edge)	**7 mils**
Minimum Pair-to-Pair Spacing	**20 mils**
Minimum Serpentine Spacing	**20 mils**
Minimum Spacing to Other LVDS	**20 mils**
Minimum Isolation Spacing to non-LVDS	**20 mils**
Maximim Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

***Cable Length must be less than 16"**

(10,20,21,22,23,26,30,31,33,34,35,40,43,46,48,49,50) 3VDDA — 3VDDA
(10,12,15,17,18,19,20,22,23,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM — 3VDDM
(45,46,47,48,49,50,51) DCIN — DCIN

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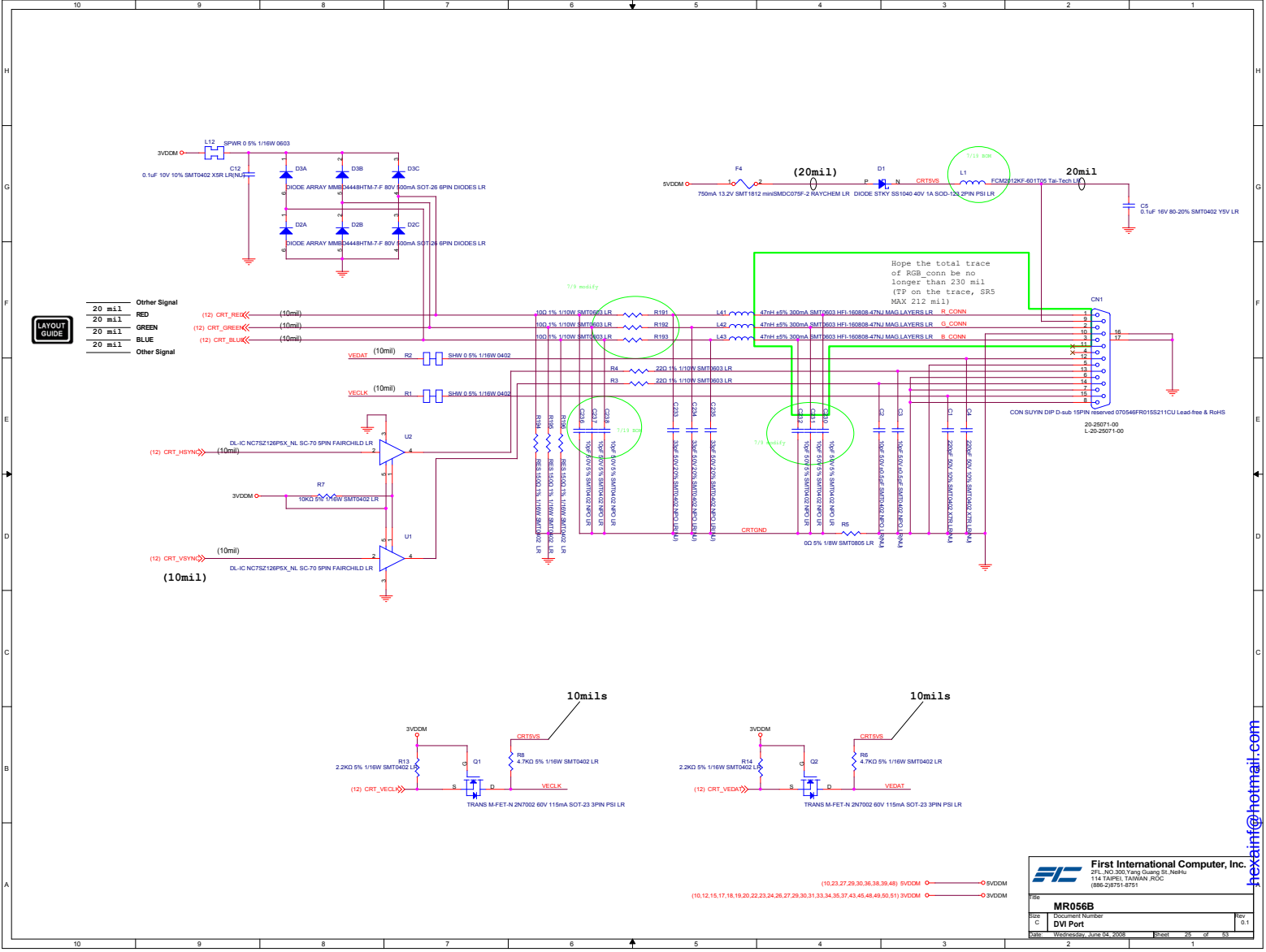

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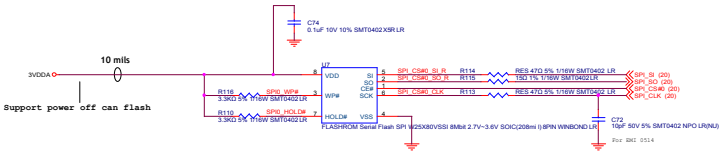
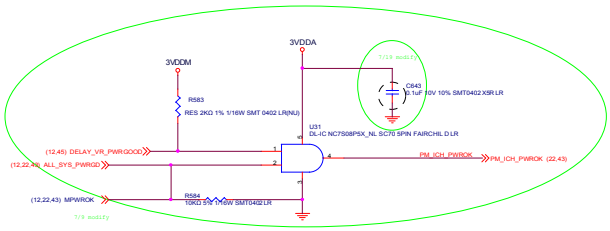
SPI Interface





(10,12,15,17,18,19,20,22,23,24,25,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM — 3VDDM

(10,20,21,22,23,24,30,31,33,34,35,40,43,46,48,49,50) 3VDDA — 3VDDA

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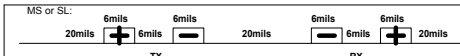
NOTE

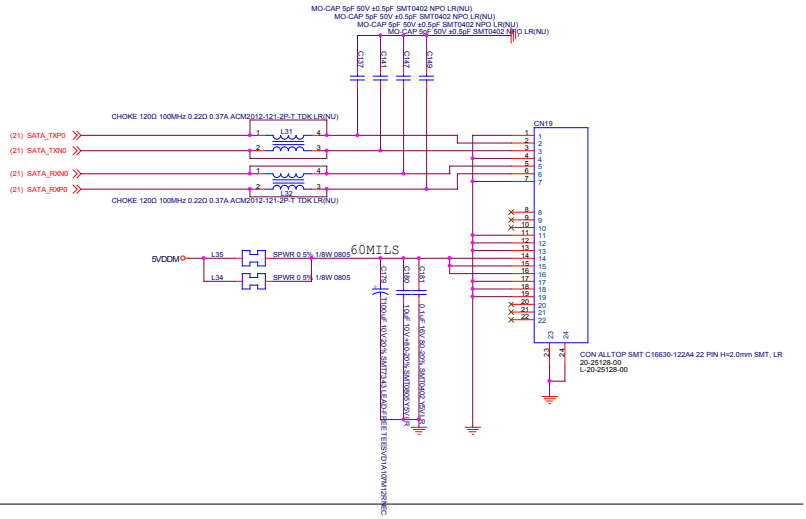
SATA differential stripline 20:5:6:5:20
SATA differential mircostripline 20:6:6:6:20
請包GROUND

SATA Layout Note:

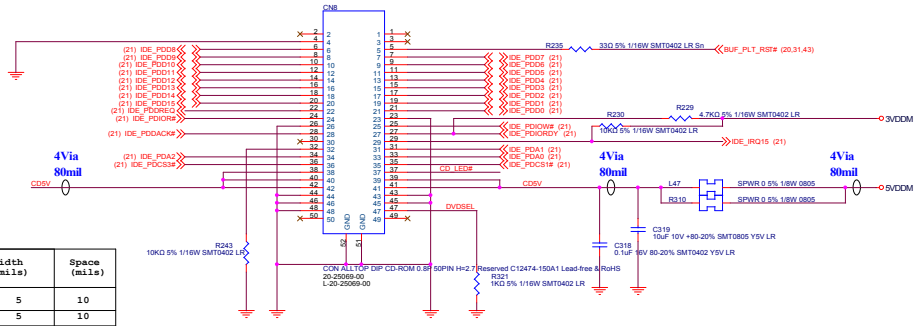
MS or SL:



* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.

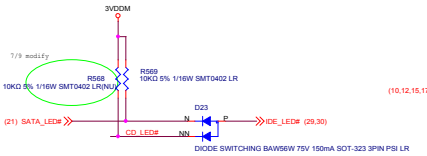


CD-ROM CNN



IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_PDCS 10-30#	8	5	10
IDE_PDDREQ	8	5	10
IDE_SDDREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_PATADET	8	5	10
IDE_SATADET	8	5	10
IDE_PDDACK#	8	5	10
IDE_SDDACK#	8	5	10



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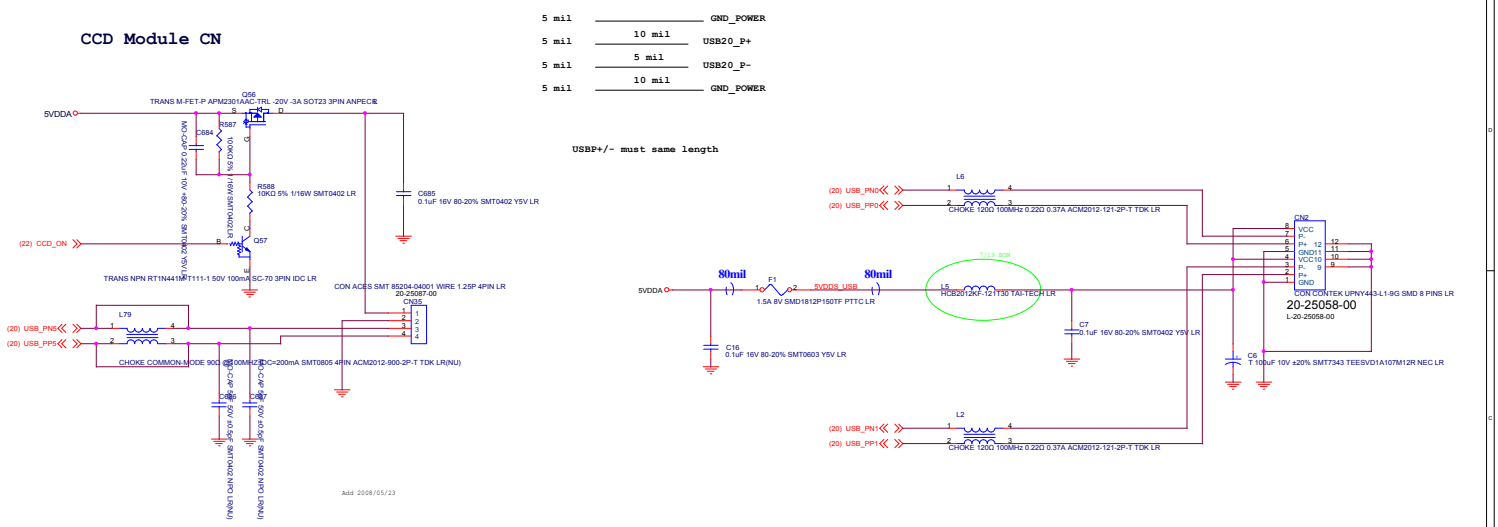
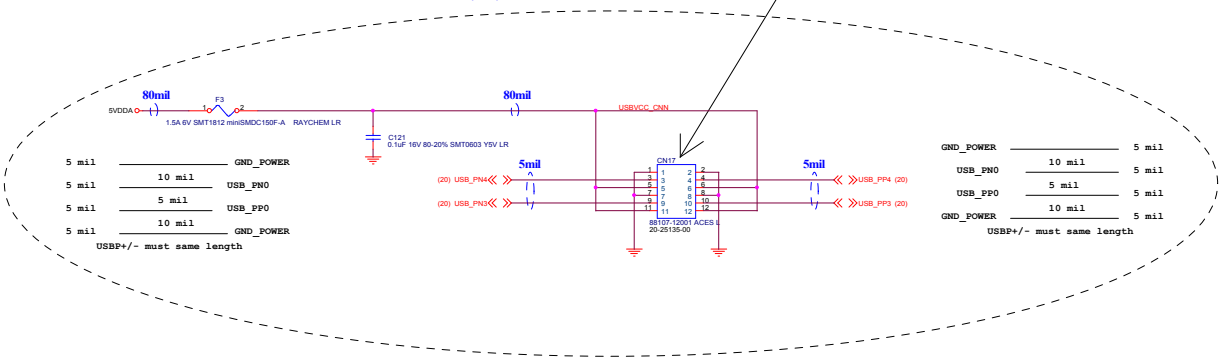
CCD Module CN



Add on 5/4/07

X,Y follow PA354 CN12



(23,30,45,48,49,50,51) 5VDDA — 5VDDA

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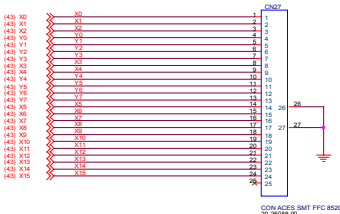
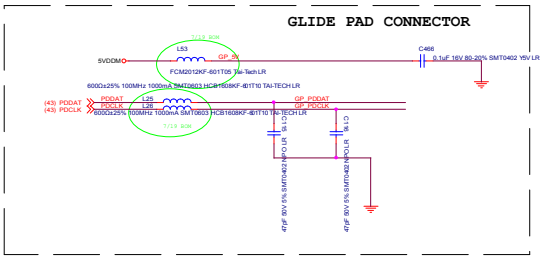
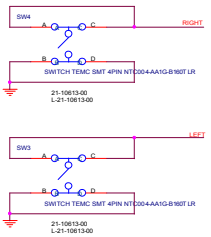
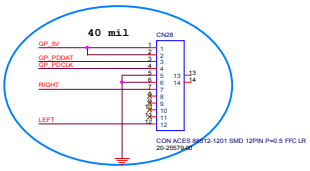
INT KB CNN



GLIDE PAD CONNECTOR

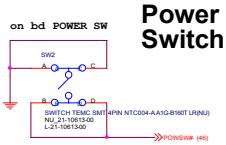




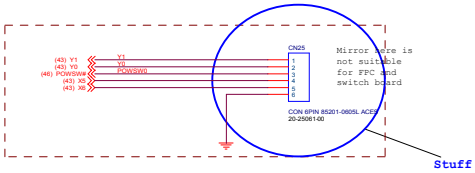


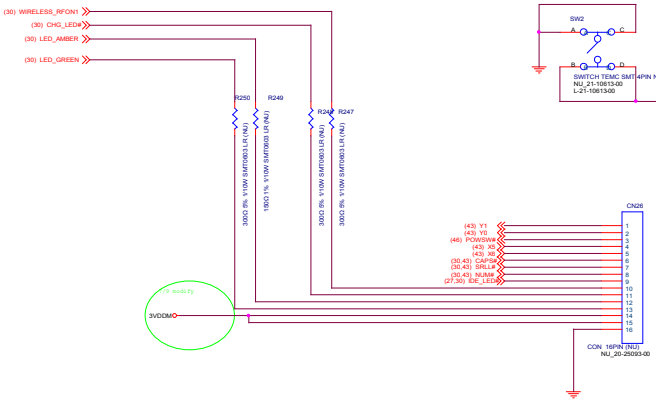
modify on 20080318 to follow XY670 for ME require

Power Switch



switch board con ID2





switch board con ID3

(10,12,15,17,18,19,20,22,23,24,25,26,27,30,31,33,34,35,37,43,45,48,49,50,51) 5VDDM → 5VDDM

(10,23,25,27,30,36,38,39,48) 5VDDM → 5VDDM

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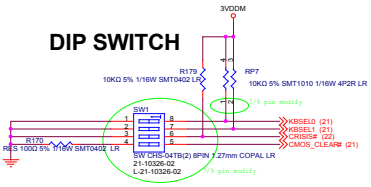
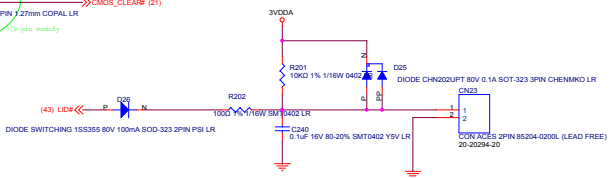
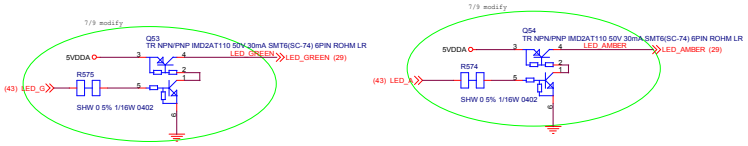
DIP SWITCH



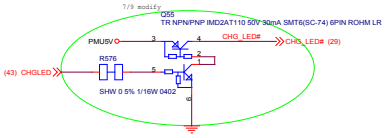
LID Switch



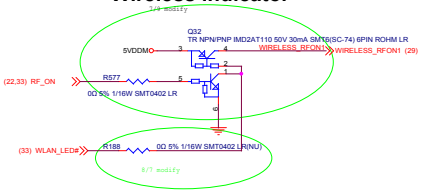
Power indicator



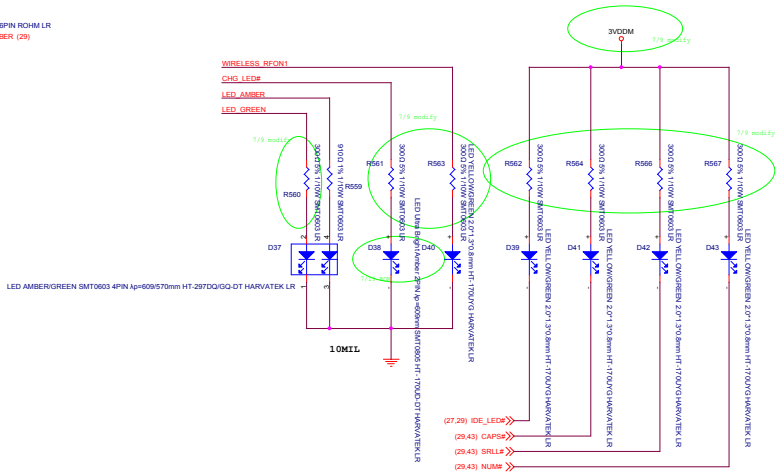
Charge indicator



Wireless indicator



LED indicator control logic



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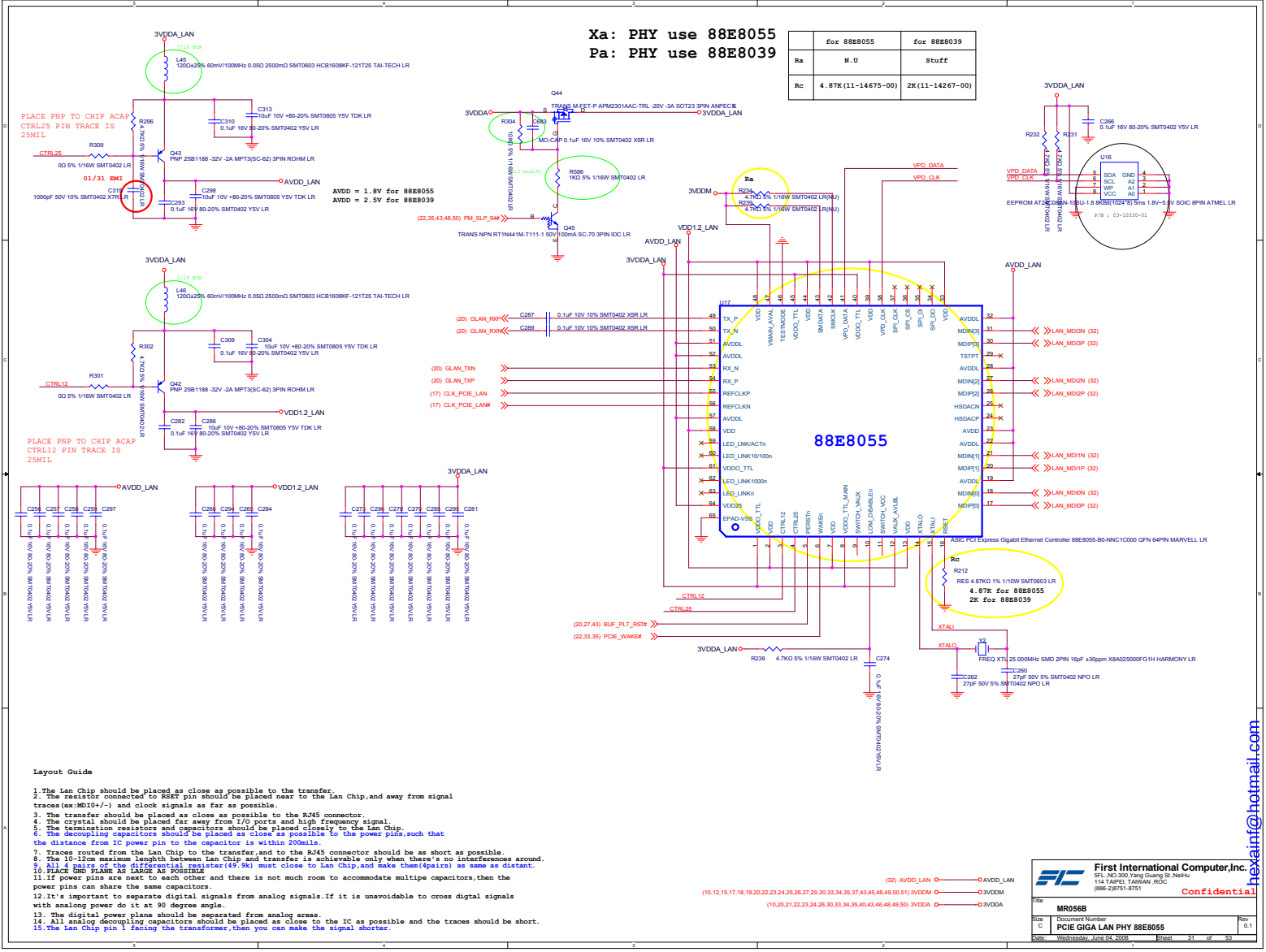

Layout Guide

1.The Lan Chip should be placed as close as possible to the transfer.
2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.
3. The transfer should be placed as close as possible to the RJ45 connector.
4. The crystal should be placed far away from I/O ports and high frequency signal.
5. The termination resistors and capacitors should be placed closely to the Lan Chip.
6. The decoupling capacitors should be placed as close as possible to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.
7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.
8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.
9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.
10.PLACE GND PLANE AS LARGE AS POSSIBLE
11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.
12.It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analog power do it at 90 degree angle.
13. The digital power plane should be separated from analog areas.
14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
15.The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

(32) AVDD_LAN → AVDD_LAN
(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,33,34,35,37,43,45,48,49,50,51) 3VDDM → 3VDDM
(10,20,21,22,23,24,26,30,33,34,35,40,43,46,48,49,50) 3VDDA → 3VDDA

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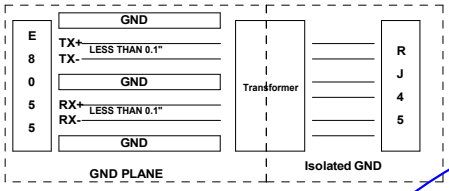
MR056B			
Size: C	Document Number: PCIE GIGA LAN PHY 88E8055		Rev: 0.1
Date: Wednesday, June 04, 2008	Sheet 31 of 53		

hexainf@hotmail.com

TX
RX

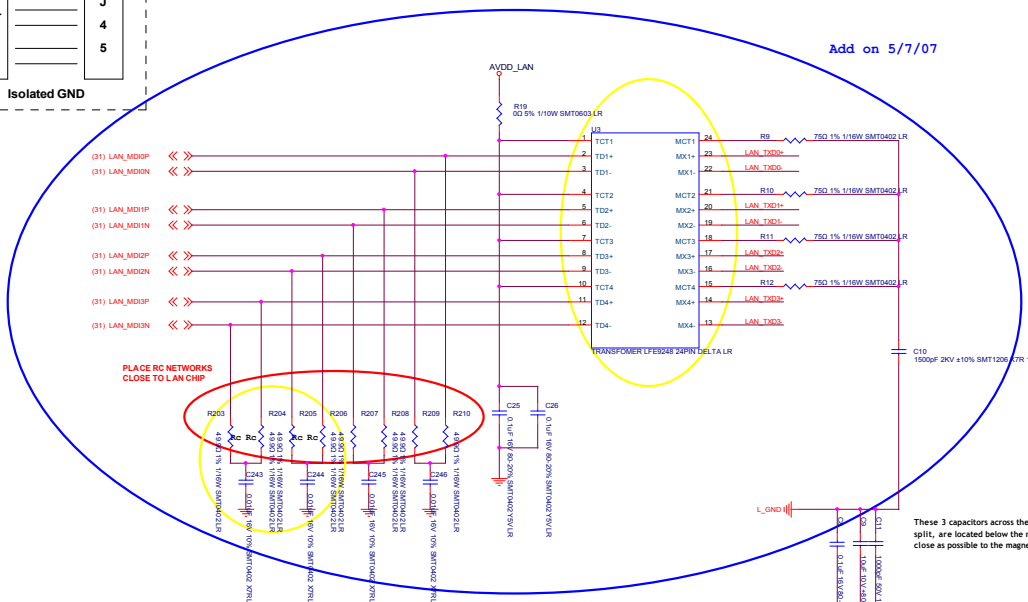
100 ohm ---> trace 4 mil , space 10 mil
50 mil space from other signals
Total Tace Length no more thans 4.8"
2 Differential pairs must have the same length



Xa: Transformer use LFE9248(12-01904-01)

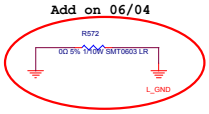
Pa: Transformer use LFE8466(12-02109-01)

Add on 5/7/07



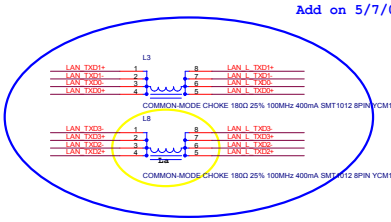
These 3 capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.

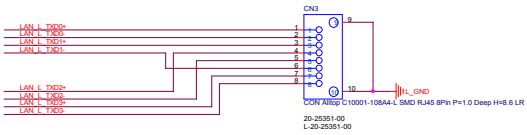
Add on 06/04



	for 88E8055	for 88E8039
Rc	STUFF	NU
La	STUFF	NU

Add on 5/7/07





(31) AVDD_LAN — AVDD_LAN

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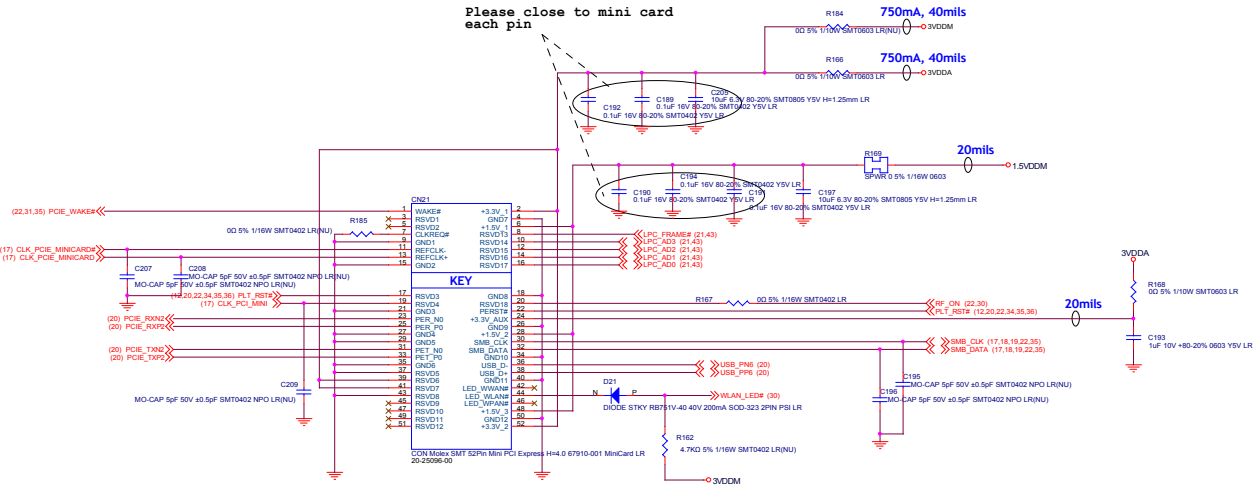
PCIE Mini Card for Wireless Lan



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Title	MR056B	
Size: C	Document Number: PCIE Mini Card	Rev: 0.1
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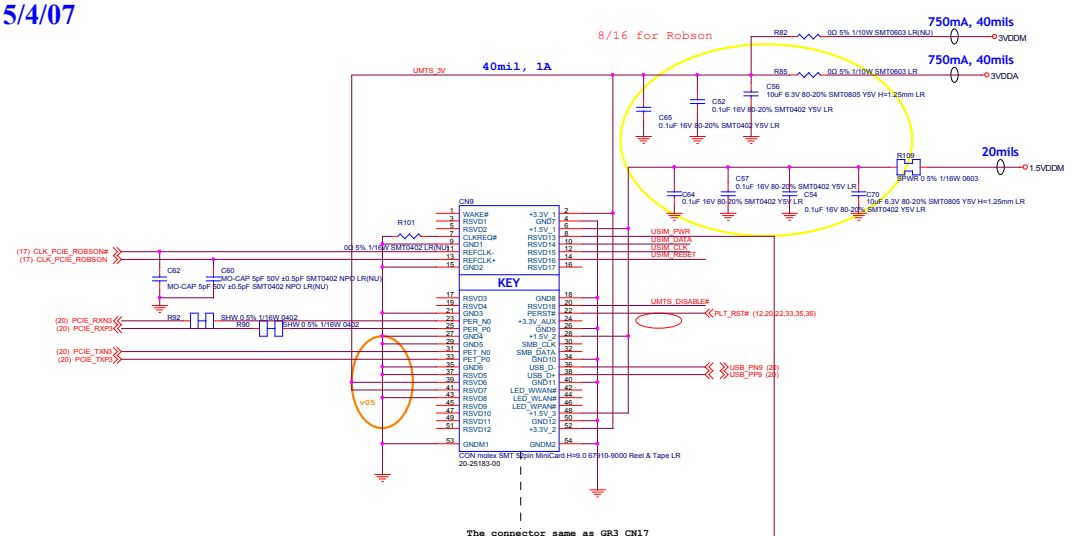
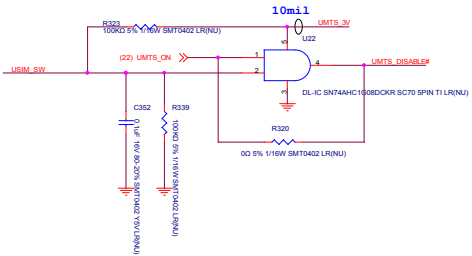
Robson / UMTS
Add on 5/4/07

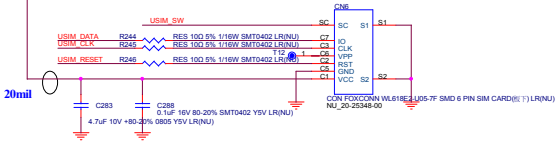


The connector same as GR3 CN17

SIM Card Switch



SIM Card CN



(9,14,15,20,21,23,33,35,49) 1.5VDDM
(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,35,37,43,45,48,49,50,51) 3VDDM
(10,20,21,22,23,24,26,30,31,33,35,40,43,46,48,49,50) 3VDDA
(23,28,30,45,48,49,50,51) 5VDDA

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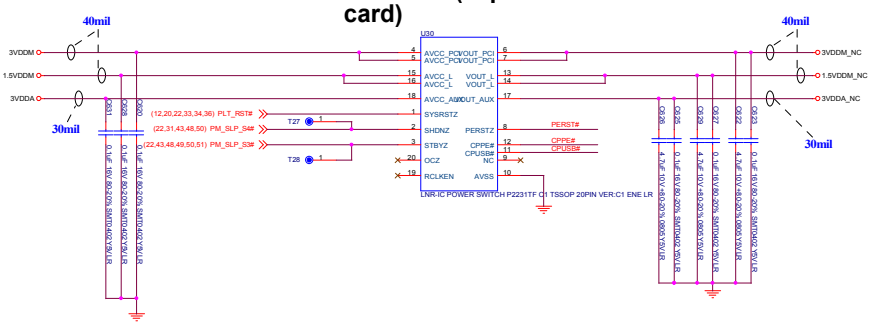
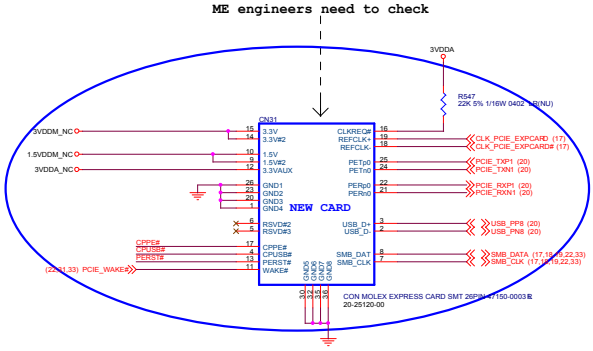
New Card(express card)



X,Y follow LM10W ME drawing 5/10

ME engineers need to check



(10,20,21,22,23,24,26,30,31,33,34,40,43,46,48,49,50) 3VDDA — 3VDDA

(9,14,15,20,21,23,33,34,49) 1.5VDDM — 1.5VDDM

(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,37,43,45,48,49,50,51) 3VDDM — 3VDDM

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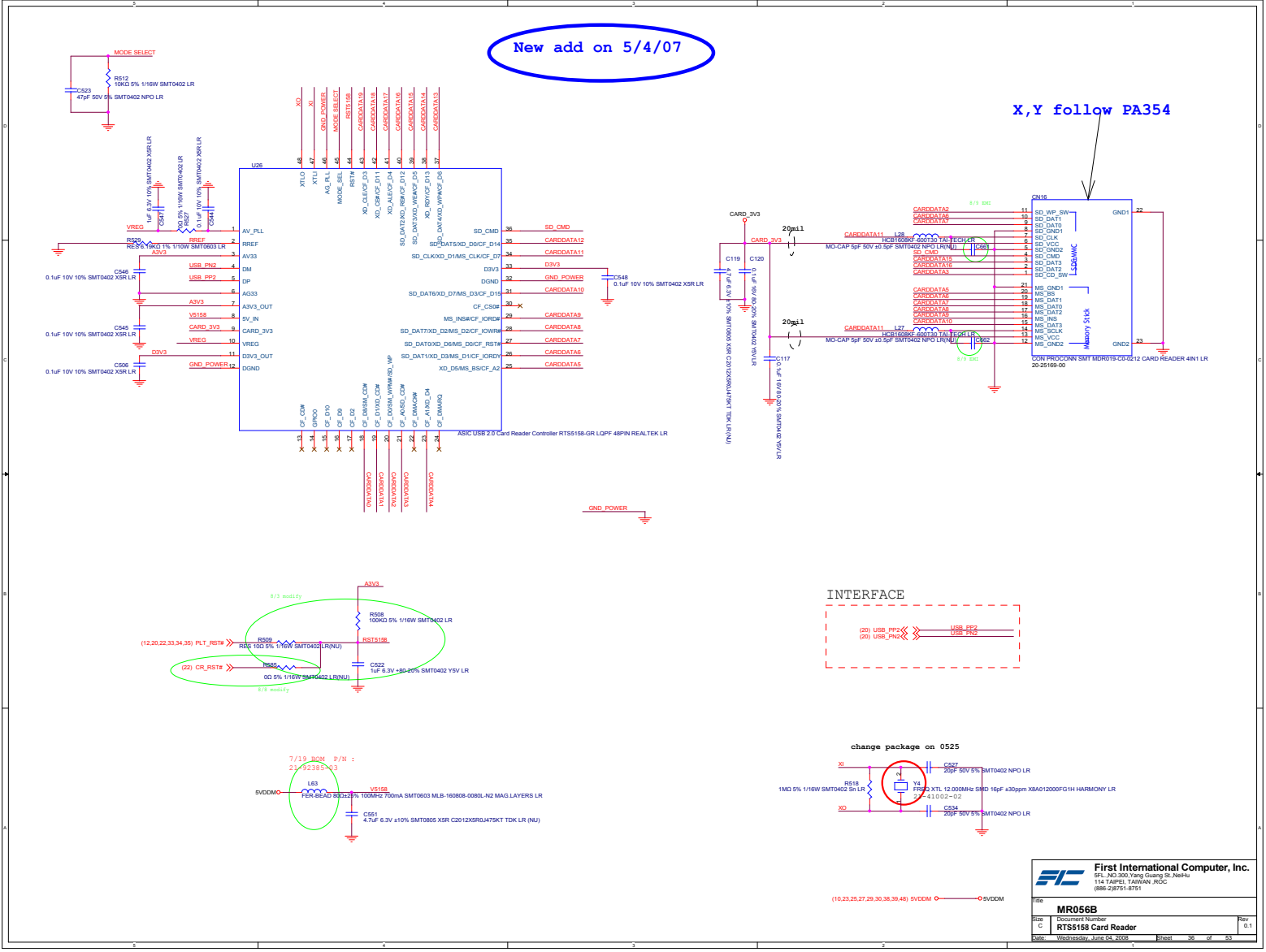
New add on 5/4/07
X,Y follow PA354
MODE SELECT
R512
10KΩ 5% 1/16W SMT0402 LR
C523
47pF 50V 5% SMT0402 NPO LR
U26
ASIC USB 2.0 Card Reader Controller RTS5158-GR LQFP 48PIN REALTEK LR
AV_PLL
RREF
AV33
DM
DP
AG33
A3V3_OUT
5V_IN
CARD_3V3
VREG
D3V3_OUT
DGND
SD_CMD
CARDDATA12
CARDDATA11
D3V3
GND_POWER
CARDDATA10
CARDDATA9
CARDDATA8
CARDDATA7
CARDDATA6
CARDDATA5
GND_POWER
CN16
CON PROCONN SMT MDR019-C0-0212 CARD READER 4IN1 LR
20-25169-00
INTERFACE
USB_PP2
USB_PN2
change package on 0525
R518
1MΩ 5% 1/16W SMT0402 Sn LR
Y4
FREQ XTL 12.000MHz SMD 16pF ±30ppm X8A012000FG1H HARMONY LR
C527
20pF 50V 5% SMT0402 NPO LR
C534
20pF 50V 5% SMT0402 NPO LR
R508
100KΩ 5% 1/16W SMT0402 LR
R509
RES 10Ω 5% 1/16W SMT0402 LR(NU)
R585
0Ω 5% 1/16W SMT0402 LR(NU)
C522
1uF 6.3V +80-20% SMT0402 Y5V LR
L63
FER-BEAD 600Ω±25% 100MHz 700mA SMT0603 MLB-160808-0080L-N2 MAG.LAYERS LR
C551
4.7uF 6.3V ±10% SMT0805 X5R C2012X5R0J475KT TDK LR (NU)
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(886-2)8751-8751
MR056B
RTS5158 Card Reader
Wednesday, June 04, 2008

AC97/AZALIA CODEC DUAL LAYOUT

USE AL883 GR / AZALIA

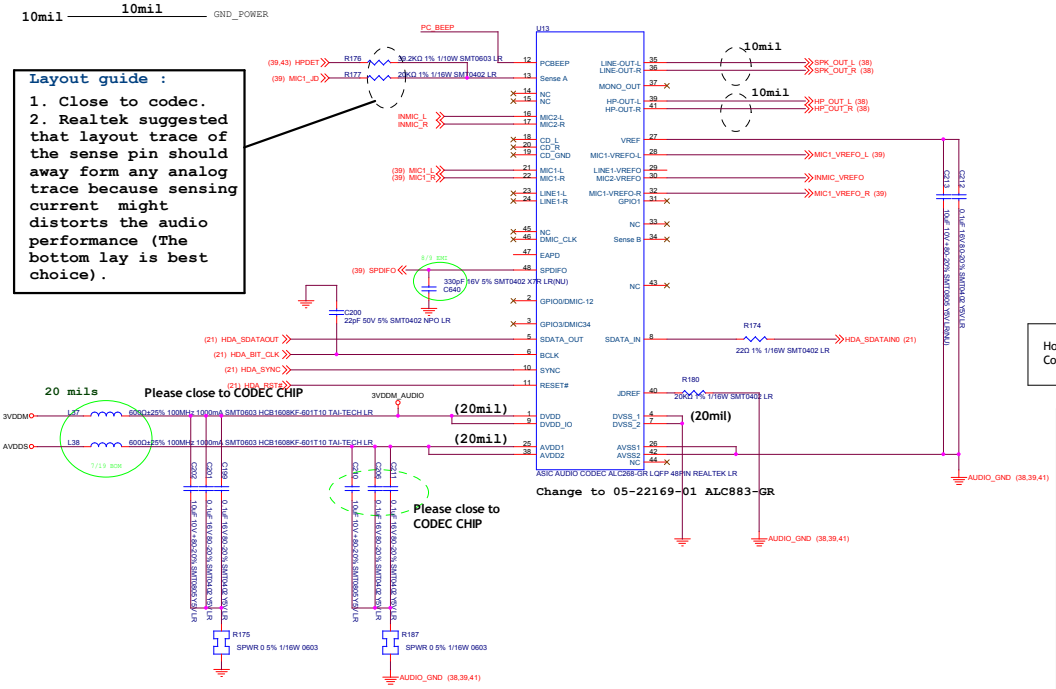
10mil — GND_POWER
10mil — 10mil — AZALIA_PCBEEP
10mil — 10mil — GND_POWER

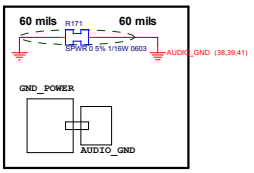
10mil — GND_POWER
10mil — 10mil — AZALIA_BITCLK
10mil — 10mil — GND_POWER

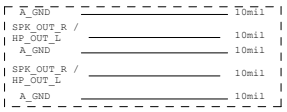
10mil — GND_POWER
10mil — 10mil — 14MCLK_AZALIA
10mil — 10mil — GND_POWER

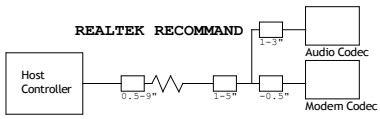
Layout guide :

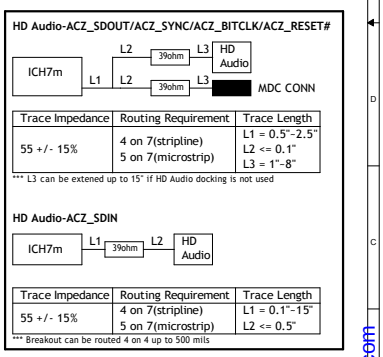
1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away form any analog trace because sensing current might distorts the audio performance (The bottom lay is best choice).

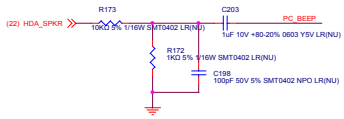












Layout guide :

1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry form quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.

(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,43,45,48,49,50,51) 3VDDM — 3VDDM
(38) AVDDS — AVDDS

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File: MR056B
Size: C
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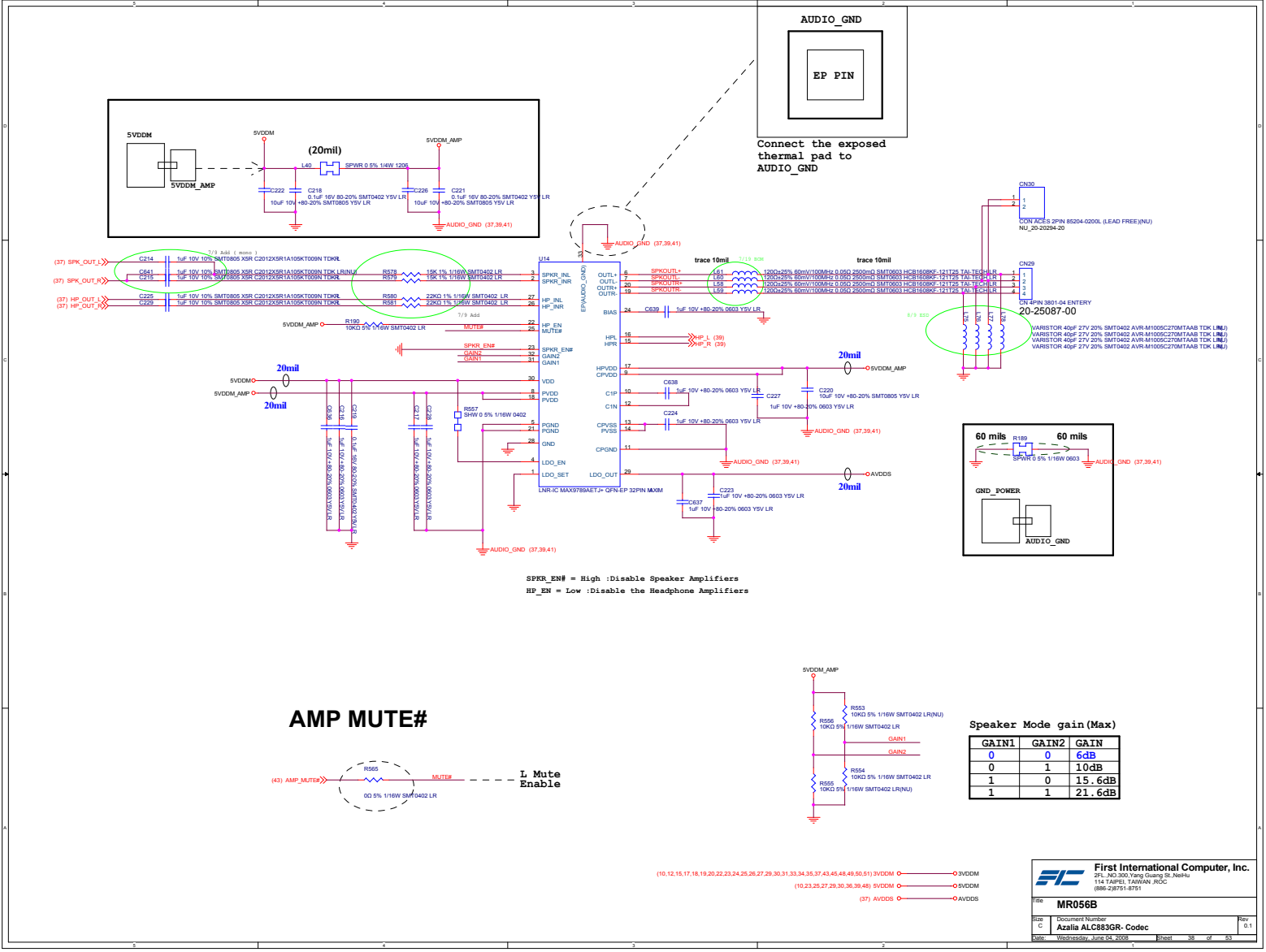

SPKR_EN# = High :Disable Speaker Amplifiers
HP_EN = Low :Disable the Headphone Amplifiers

AMP MUTE#

L Mute Enable

Speaker Mode gain(Max)

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM
(10,23,25,27,29,30,36,39,48) 5VDDM
(37) AVDDS

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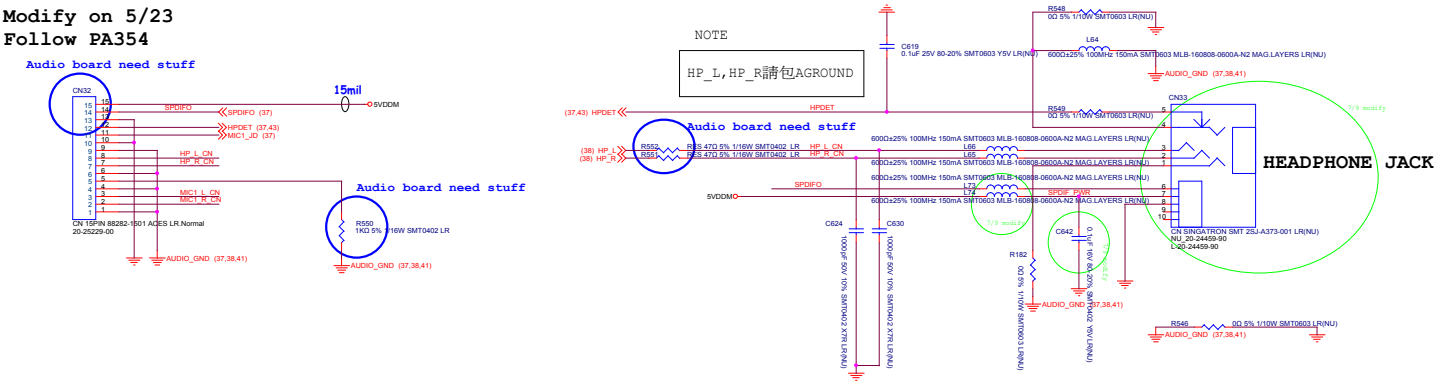
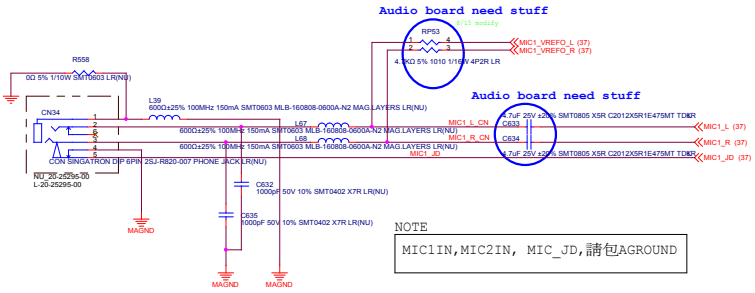
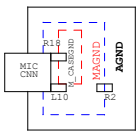
Size C	Document Number: Azalia ALC883GR- Codec	Rev 0.1
Date: Wednesday, June 04, 2008	Sheet 38 of 53	

Modify on 5/23
Follow PA354



MIC IN





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Size: C
Document Number: HP / MIC IN JACK
Rev: 0.1
Date: Wednesday, June 04, 2008
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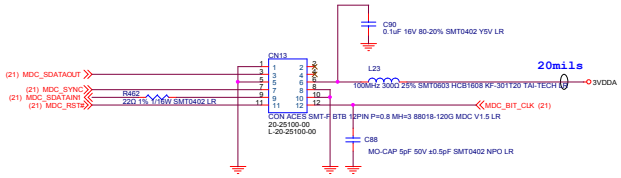
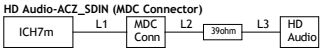
MDC 1.5 CNN

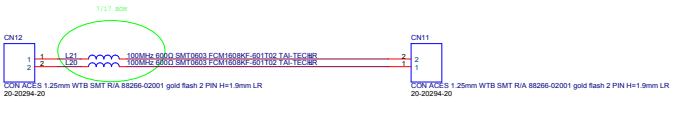


HD Audio-ACZ_SDIN (MDC Connector)



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"-15" L2 = 0.5"-1.5" L3 = 0.5"

*** Breakout can be routed 4 on 4 up to 400 mils



(10,20,21,22,23,24,26,30,31,33,34,35,43,46,48,49,50) 3VDDA — 3VDDA

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Title: MR056B

Size	Document Number	Rev
C	MDC CNN	0.1

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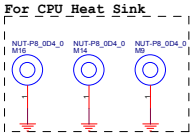
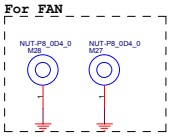
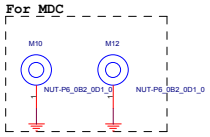
stuff
P/N:24-10966-51
For CPU_Heat_Sink



stuff
P/N:24-10966-51
For FAN



stuff
P/N:24-10732-21
For MDC



stuff
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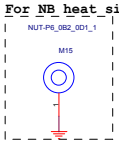
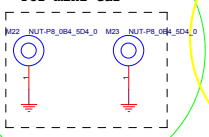
For NB_heat_sink

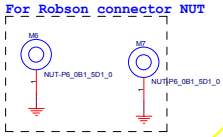


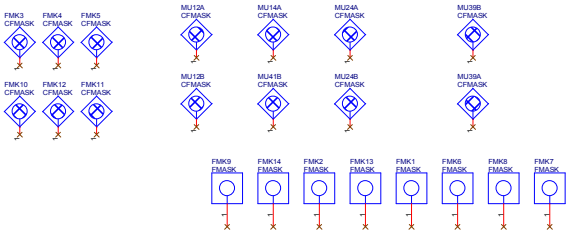
7/9 modify

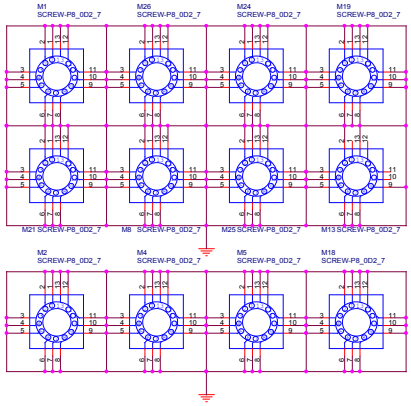
stuff
P/N:24-11743-50
For mini car

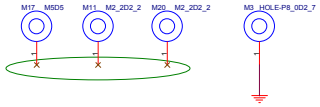


Add on 5/7/07
Not stuff 8/16 for Robson
P/N:24-11618-50
For Robson connector NUT

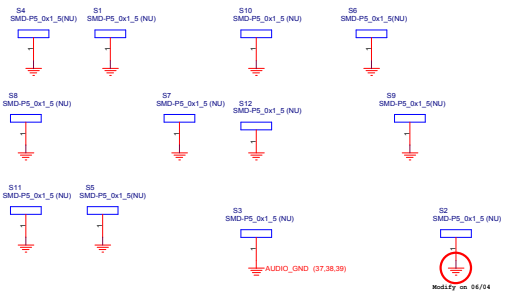




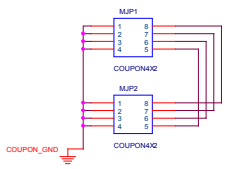




9/26 Change not connect to GND



COUPON4X2



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hexainf@hotmail.com

EMI Solution

C682 : VGA_VDD ---- P.51
C681 : Q19 pin4 --- P.45
C680 : R200 pin 1 -- P.46
C679 : 3VDDA ------- P.48
C678 : DCIN -------- P.47
C677 : DCIN -------- P.47
C676 : DCIN -------- P.47
C675 : DCIN -------- P.47
C674 : 3VDDA ------- P.48

C673 : 1.5VDDM ----- P.49
C672 : 1.25VDDM ---- P.49
C671 : 1.5VDDM ----- P.49
C670 : 1.5VDDM ----- P.49
C669 : DCIN -------- P.47
C668 : ADPIN ------- P.46
C667 : 1.05VDDM ---- P.50

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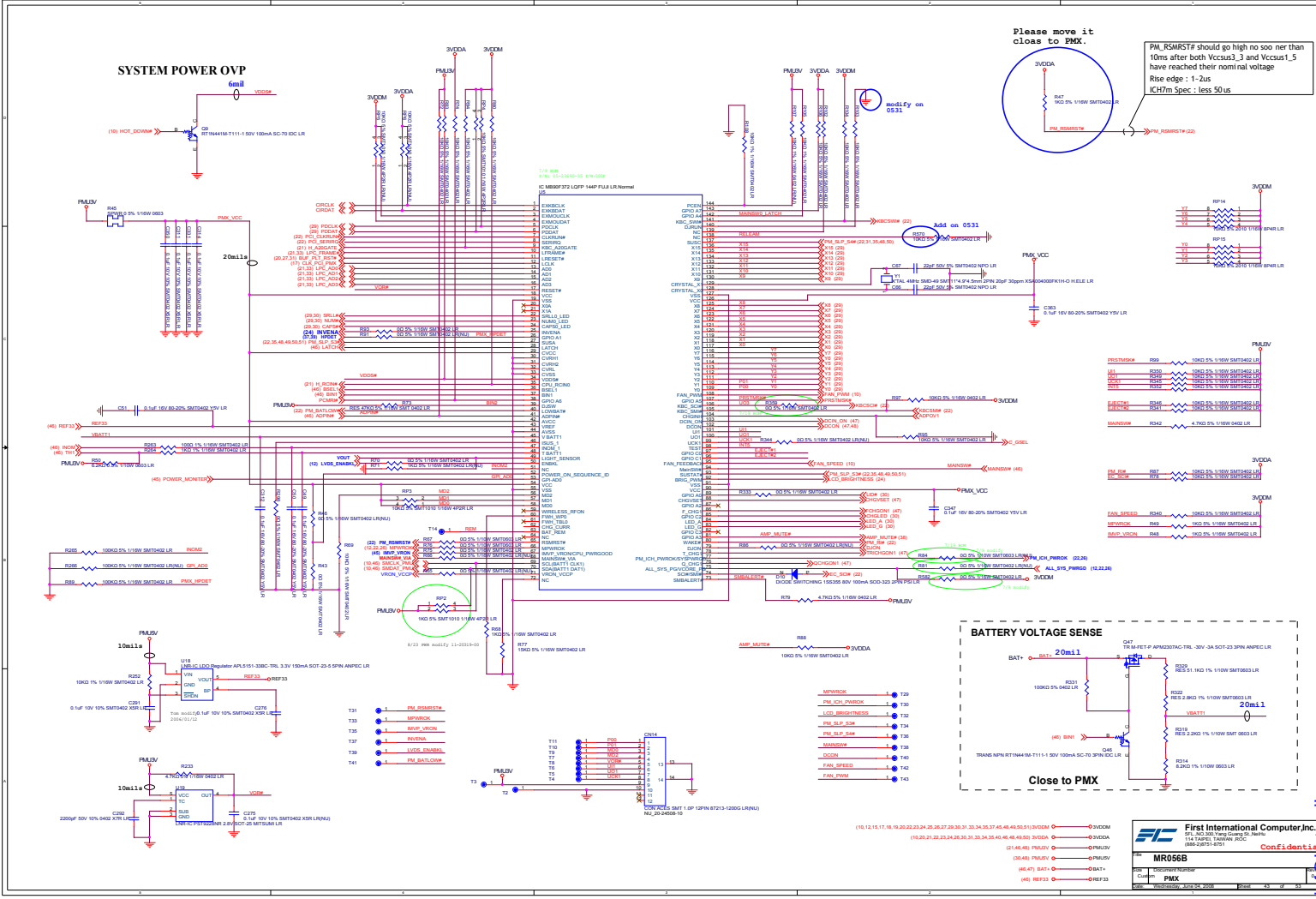
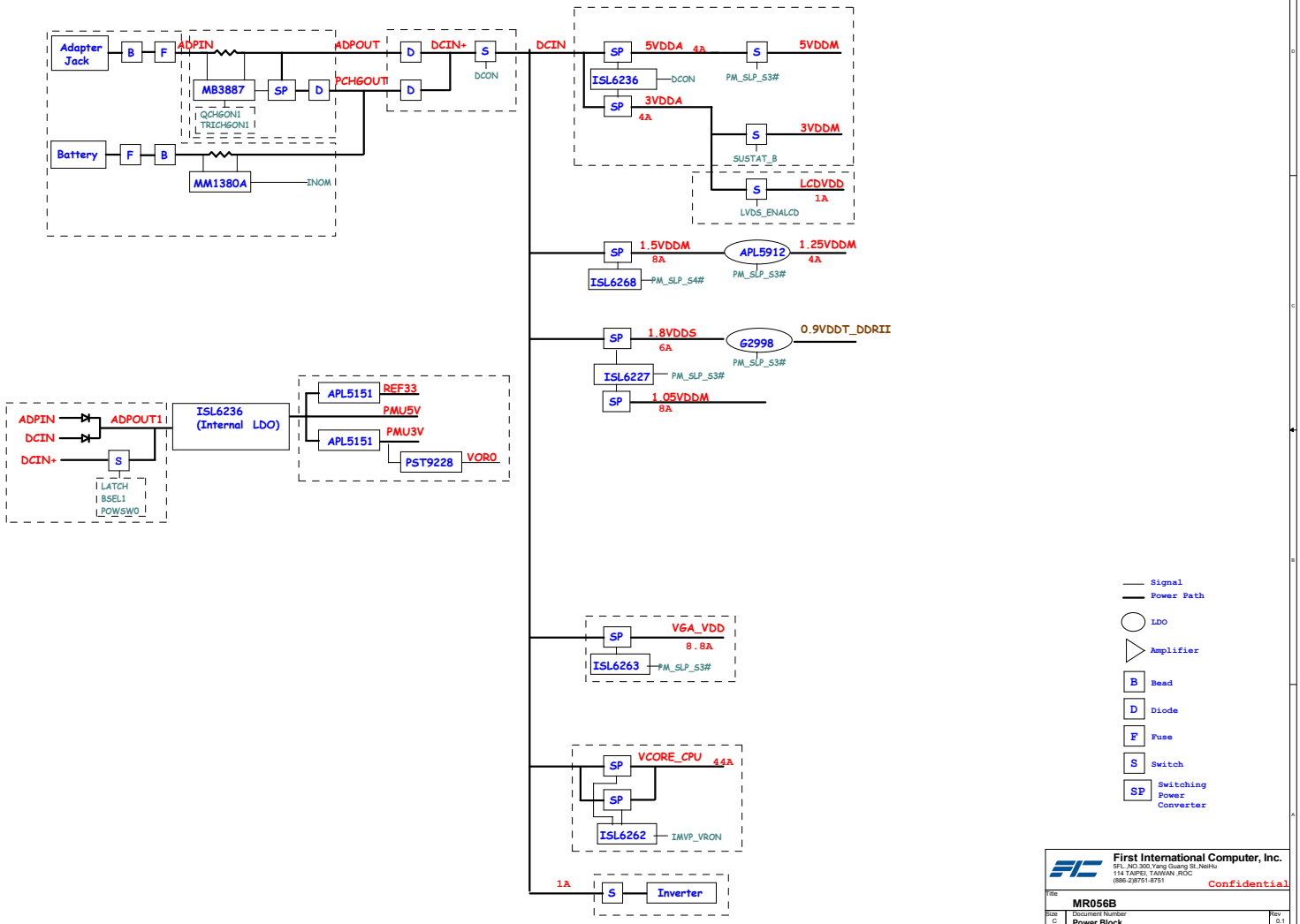


MR055/MR056 Power Block



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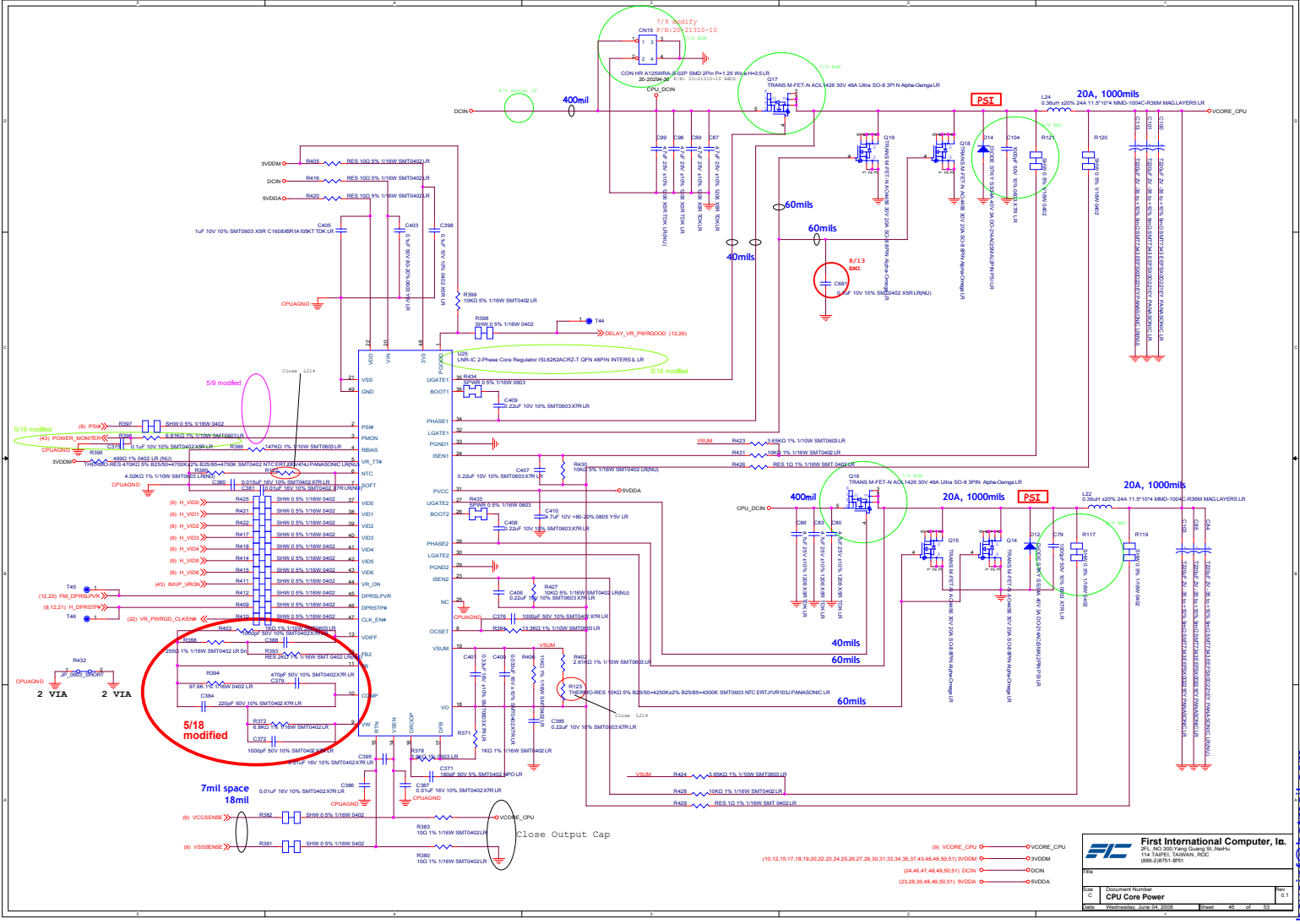
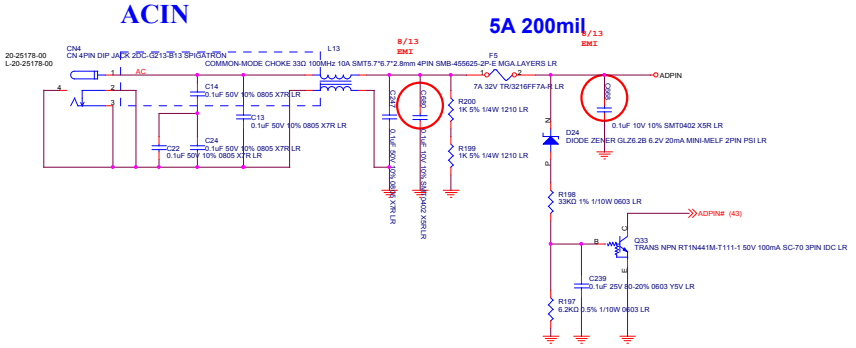
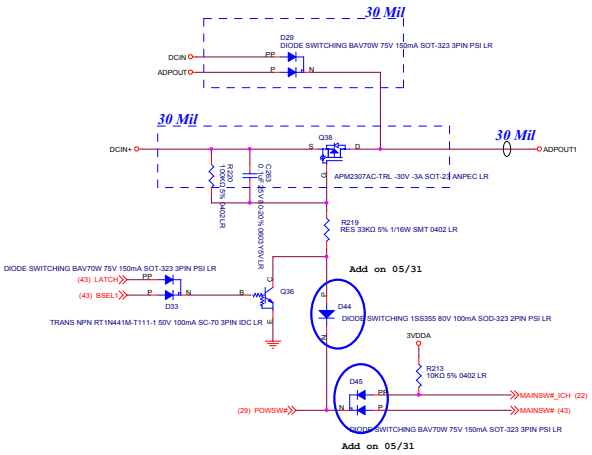


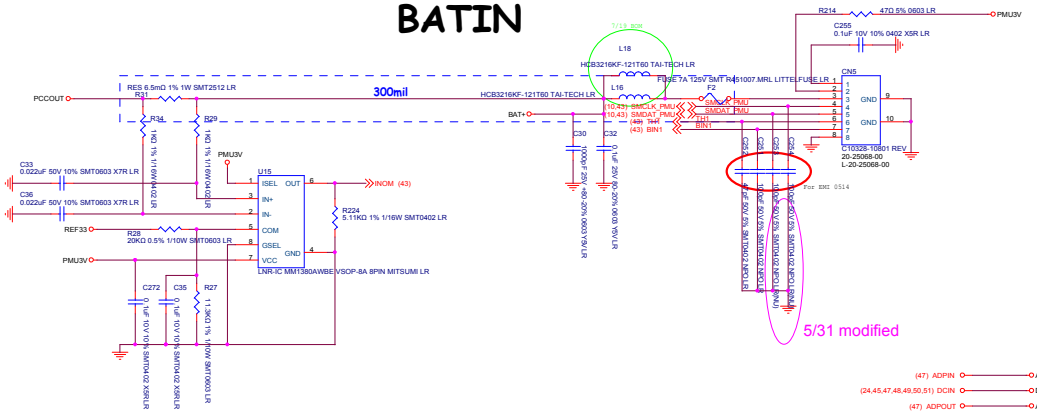
ACIN



ADPOUT1



BATIN



(47) ADPIN → ADPIN
(24,45,47,48,49,50,51) DCIN → DCIN
(47) ADPOUT → ADPOUT
(48) ADPOUT1 → ADPOUT1
(10,20,21,22,23,24,26,30,31,33,34,35,40,43,48,49,50) 3VDDA → 3VDDA
(21,43,48) PMU3V → PMU3V
(47) PCCOUT → PCCOUT
(47) DCIN+ → DCIN+
(43,47) BAT+ → BAT+
(43) REF33 → REF33

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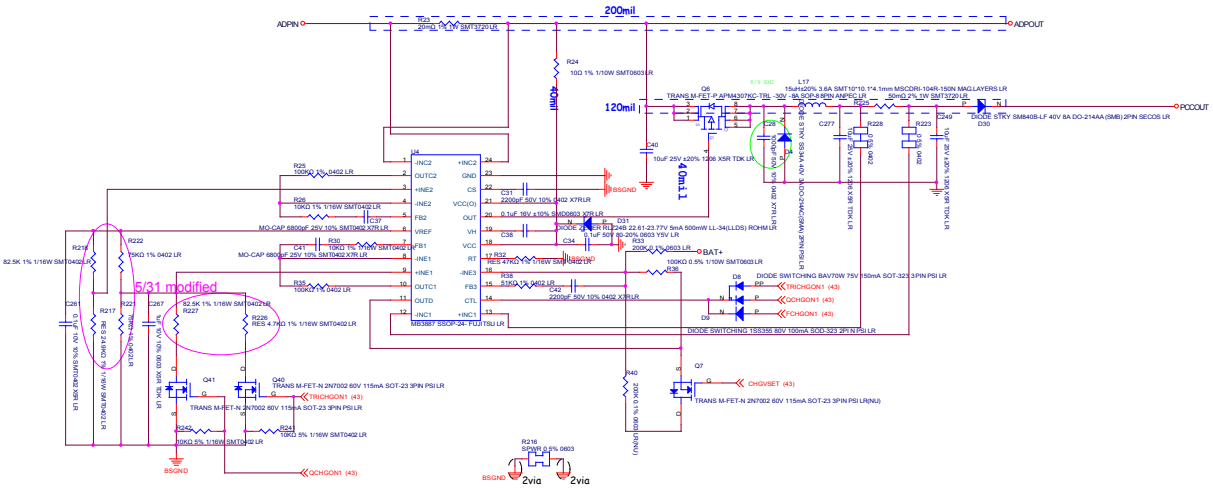
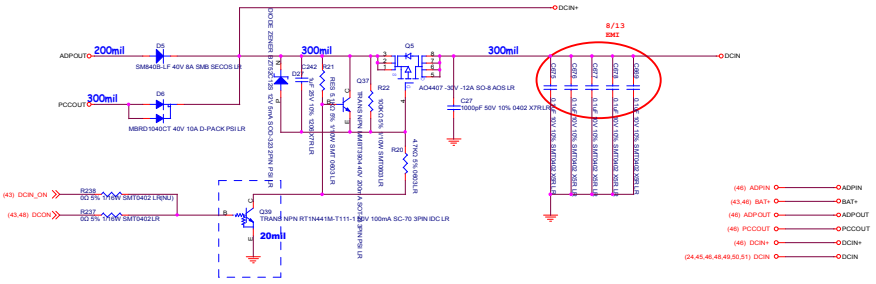
Charger



DCIN



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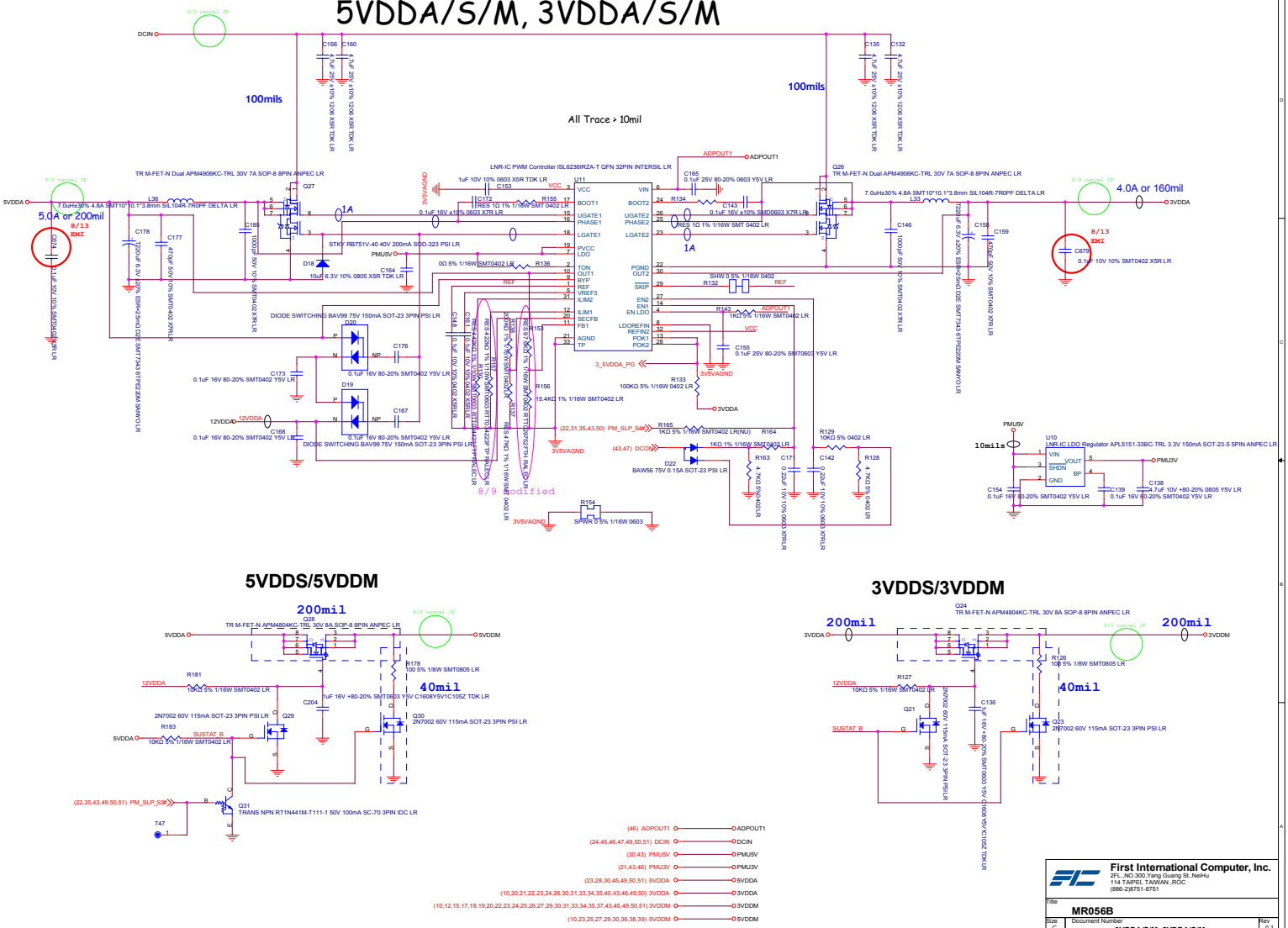
5VDDA/S/M, 3VDDA/S/M



5VDDS/5VDDM

3VDDS/3VDDM

(46) ADPOUT1 → ADPOUT1
(24,45,46,47,49,50,51) DCIN → DCIN
(30,43) PMU5V → PMU5V
(21,43,46) PMU3V → PMU3V
(23,28,30,45,49,50,51) 5VDDA → 5VDDA
(10,20,21,22,23,24,26,30,31,33,34,35,40,43,46,49,50) 3VDDA → 3VDDA
(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,49,50,51) 3VDDM → 3VDDM
(10,23,25,27,29,30,36,38,39) 5VDDM → 5VDDM

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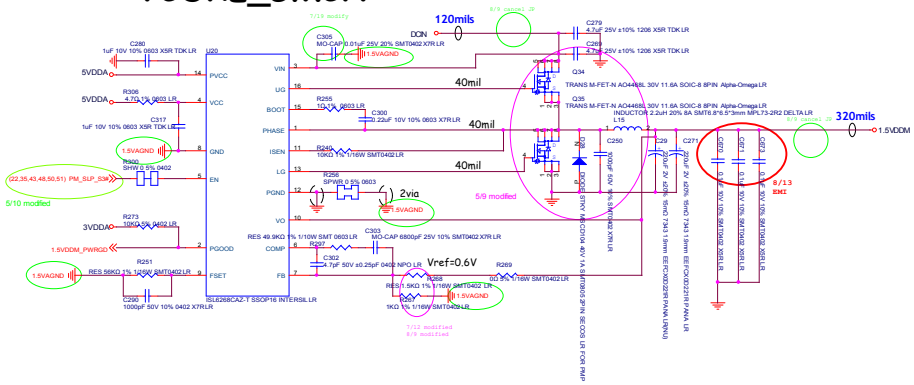
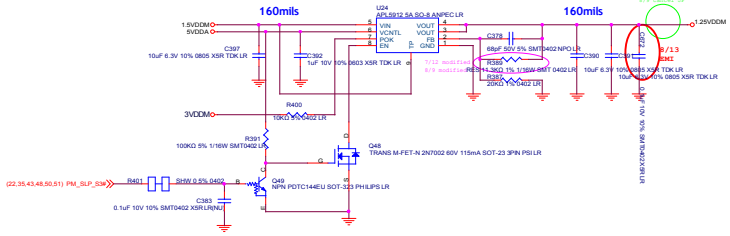
VCORE_GMCH



1.25VDDM



(24,45,46,47,48,50,51) DCIN — DCIN
(23,28,30,45,48,50,51) 5VDDA — 5VDDA
(10,20,21,22,23,24,26,30,31,33,34,35,40,43,46,48,50) 3VDDA — 3VDDA
(9,14,15,20,21,23,33,34,35) 1.5VDDM — 1.5VDDM
(12,15,17,23) 1.25VDDM — 1.25VDDM
(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,50,51) 3VDDM — 3VDDM

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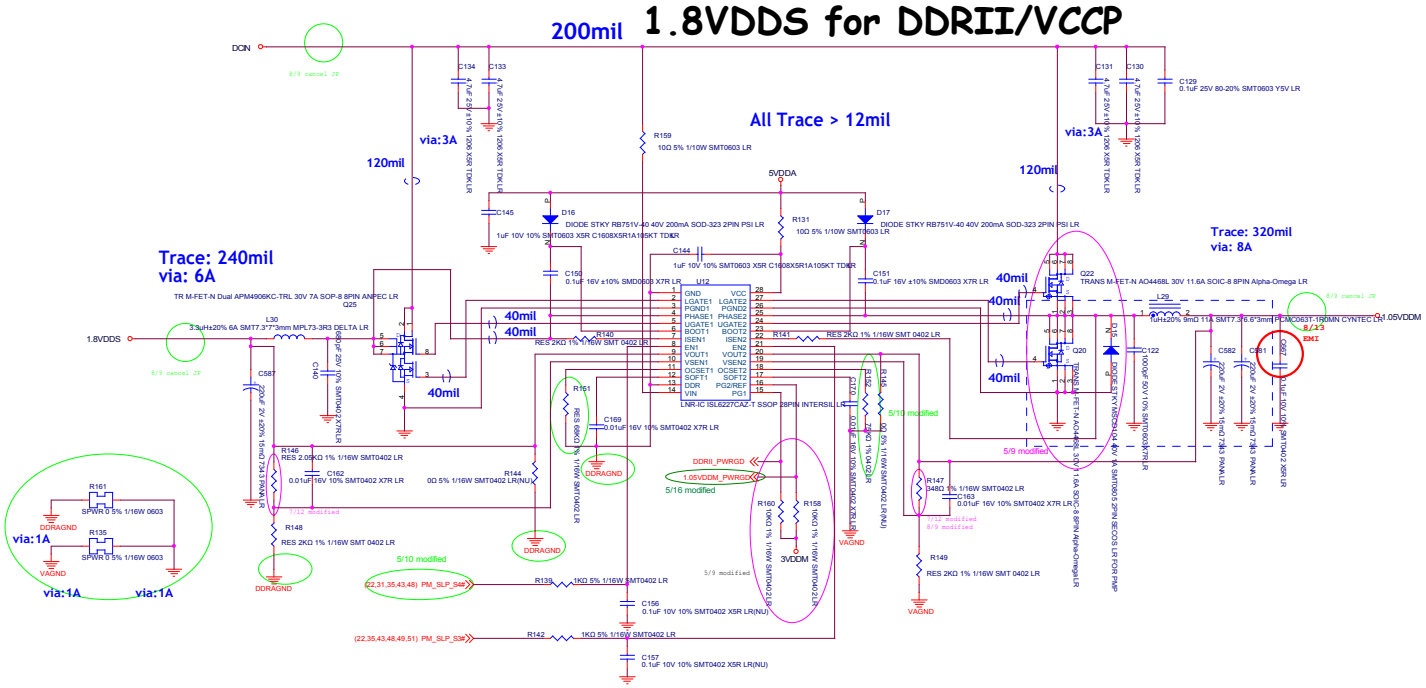
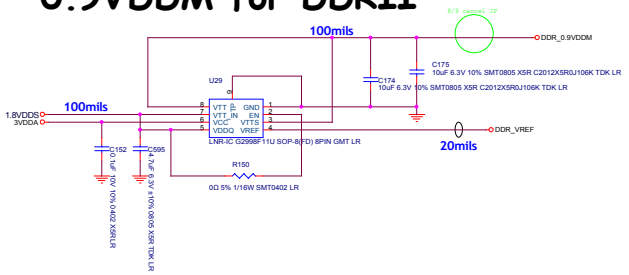
1.8VDDS for DDRII/VCCP



0.9VDDM for DDRII



(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,51) 3VDDM → 3VDDM
(8,9,11,14,15,17,21,23,51) 1.05VDDM → 1.05VDDM
(10,20,21,22,23,24,26,30,31,33,34,35,40,43,46,48,49) 3VDDA → 3VDDA
(23,28,30,45,48,49,51) 5VDDA → 5VDDA
(24,45,46,47,48,49,51) DCIN → DCIN
(12,18,19) DDR_VREF → DDR_VREF
(18,19) DDR_0.9VDDM → DDR_0.9VDDM
(12,14,15,18,19) 1.8VDDS → 1.8VDDS

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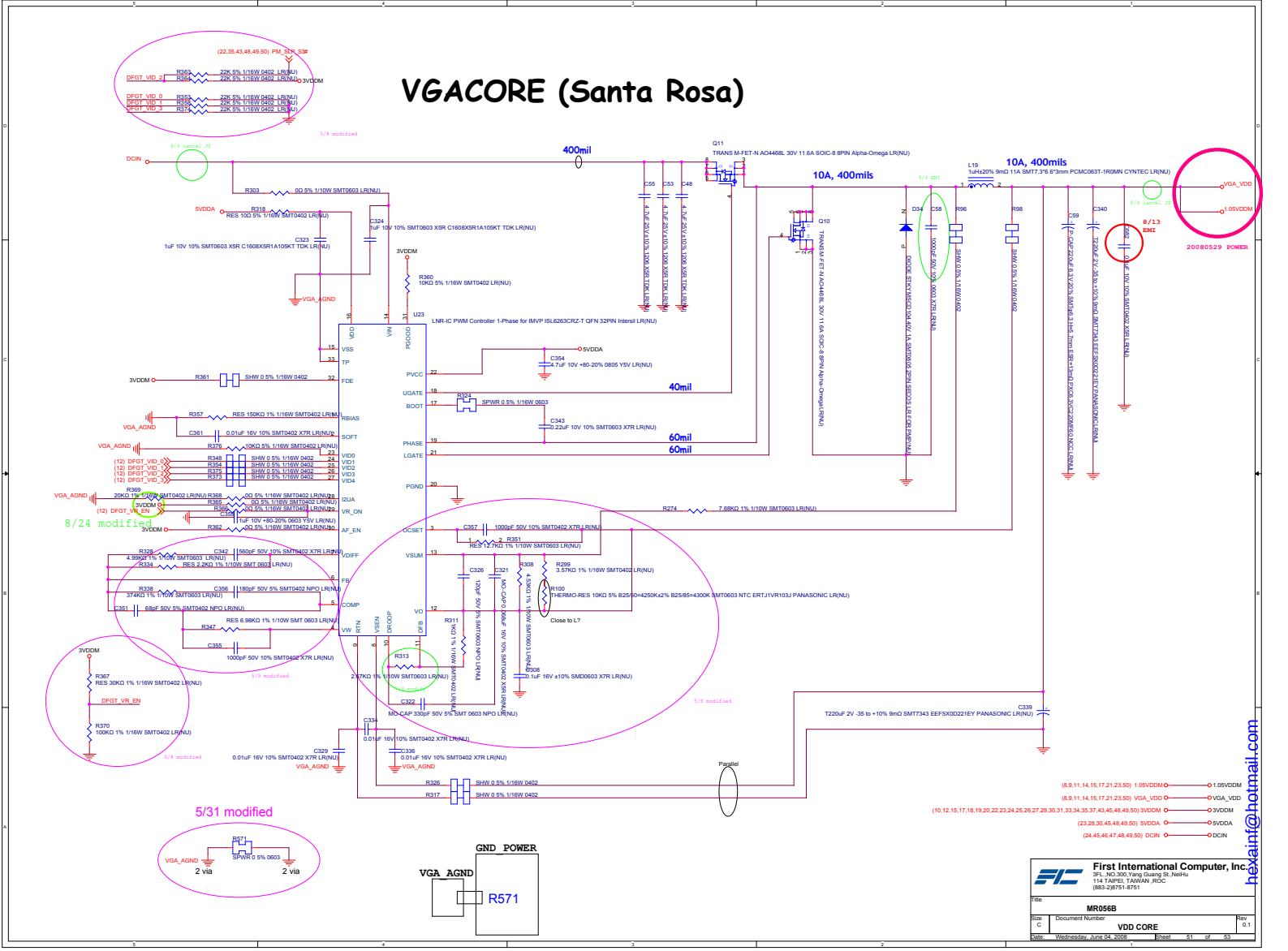
VGACORE (Santa Rosa)



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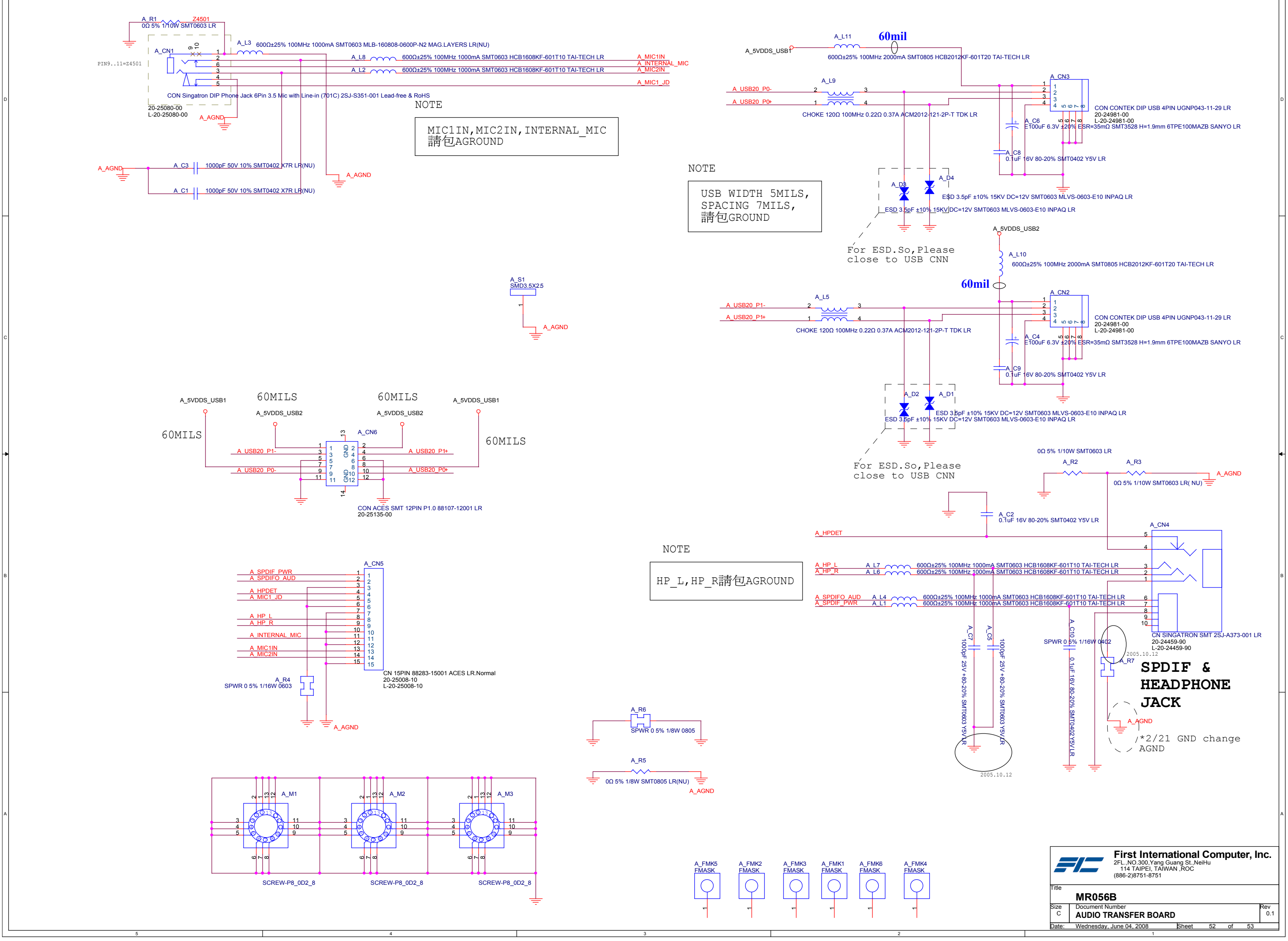

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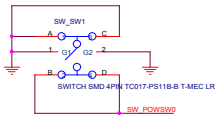
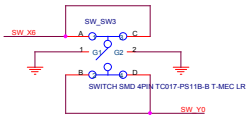
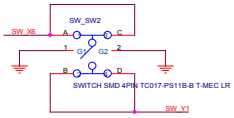
POWER SW



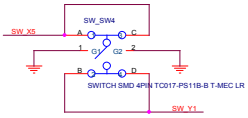
INTERNET SW

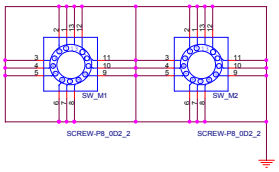


RF SW



SILEN SW





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