MANTIS_CML Schematic

2019/06/04

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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Title	Cover Page		
Size A4	Document Number: Mantis_CML		Rev A00
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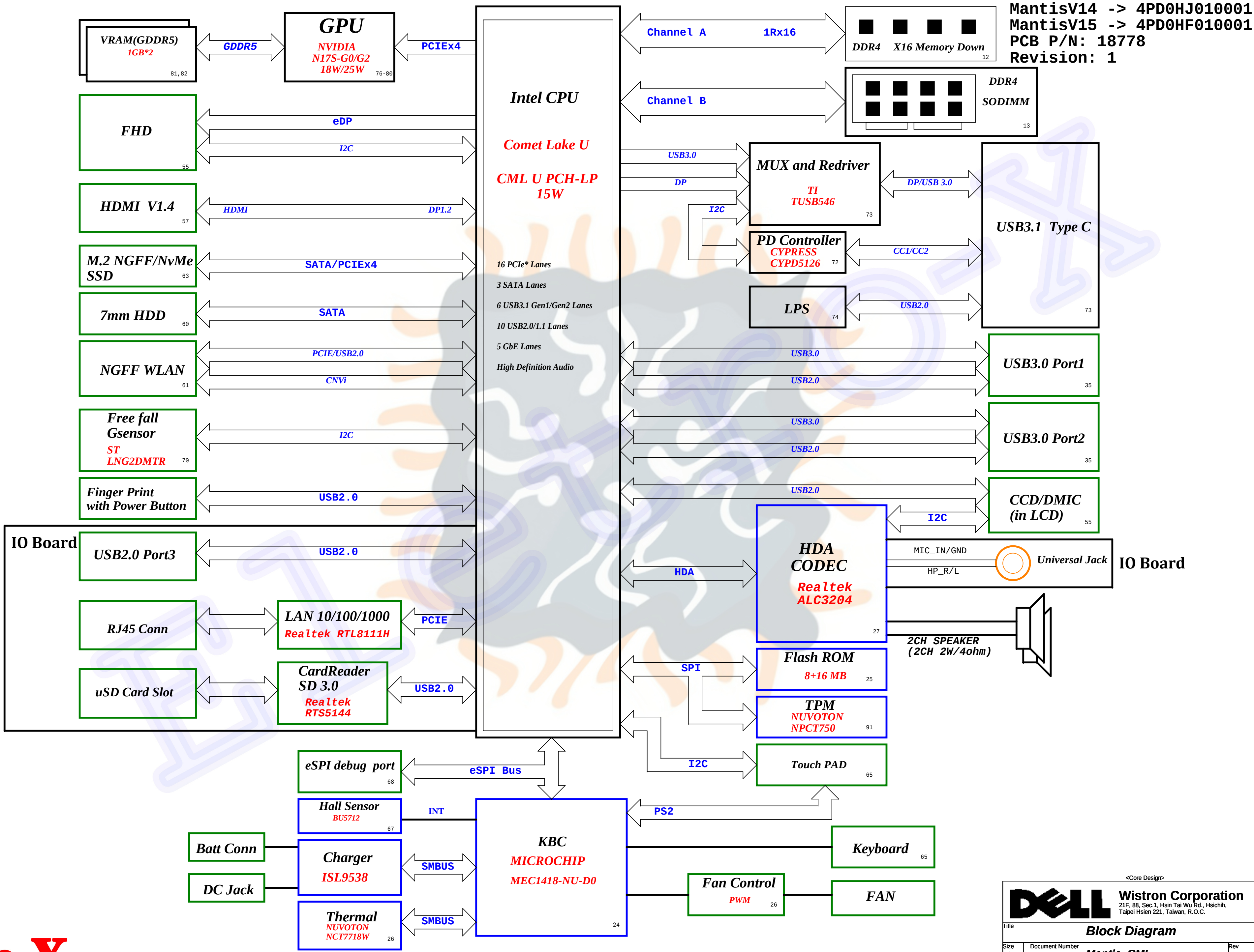
Mantis CML Block Diagram

Project code:
MantisN14 -> 4PD0HH010001
MantisN15 -> 4PD0HG010001
MantisV14 -> 4PD0HJ010001
MantisV15 -> 4PD0HF010001
PCB P/N: 18778
Revision: 1



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Title	Block Diagram	
Size C	Document Number Mantis_CML	Rev A00
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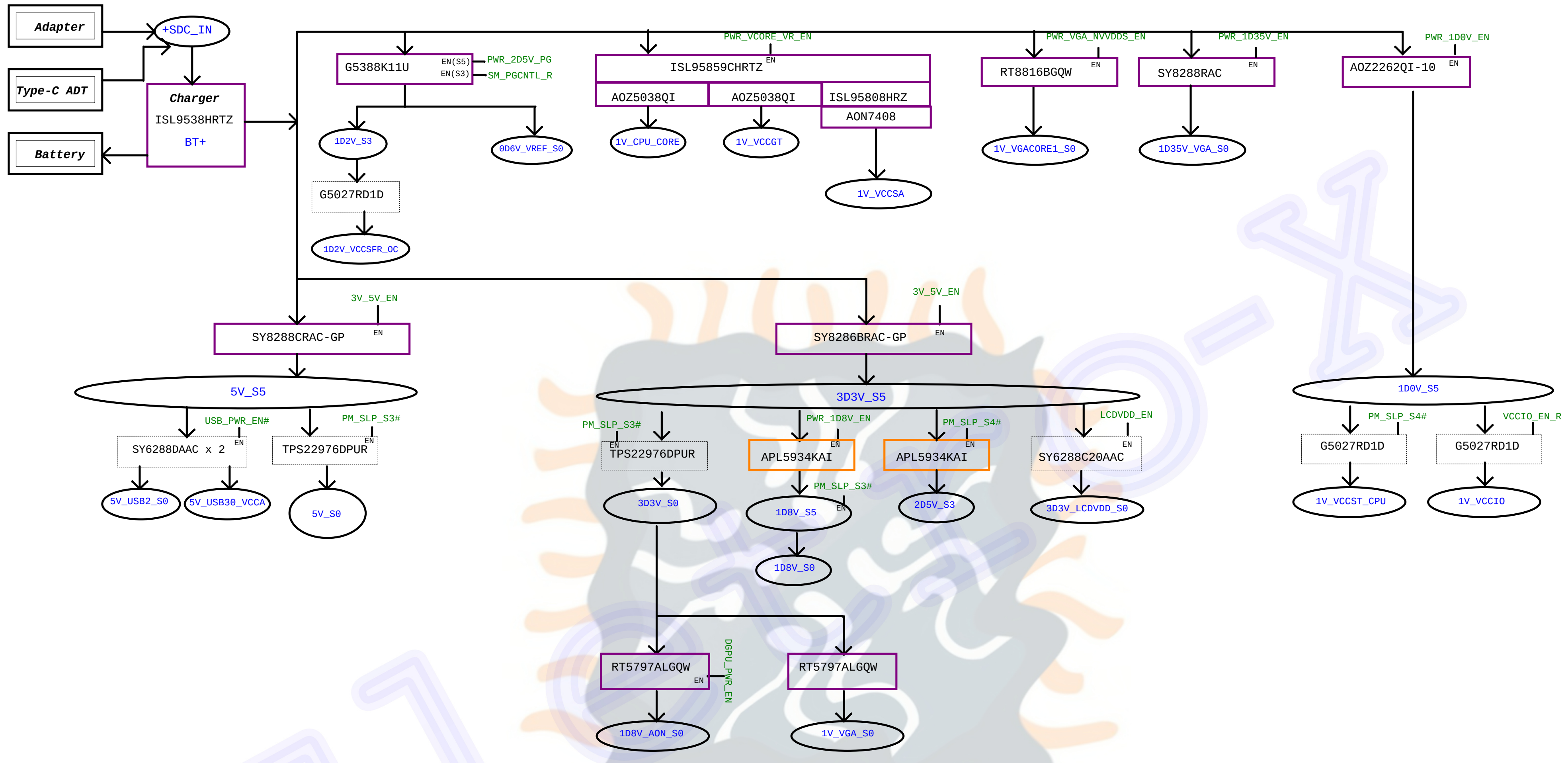
Eletro-X



Power Shape

Regulator | LDO | Switch

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Title: **Power Block Diagram**

Size: A2 | Document Number: **Mantis_CML** | Rev

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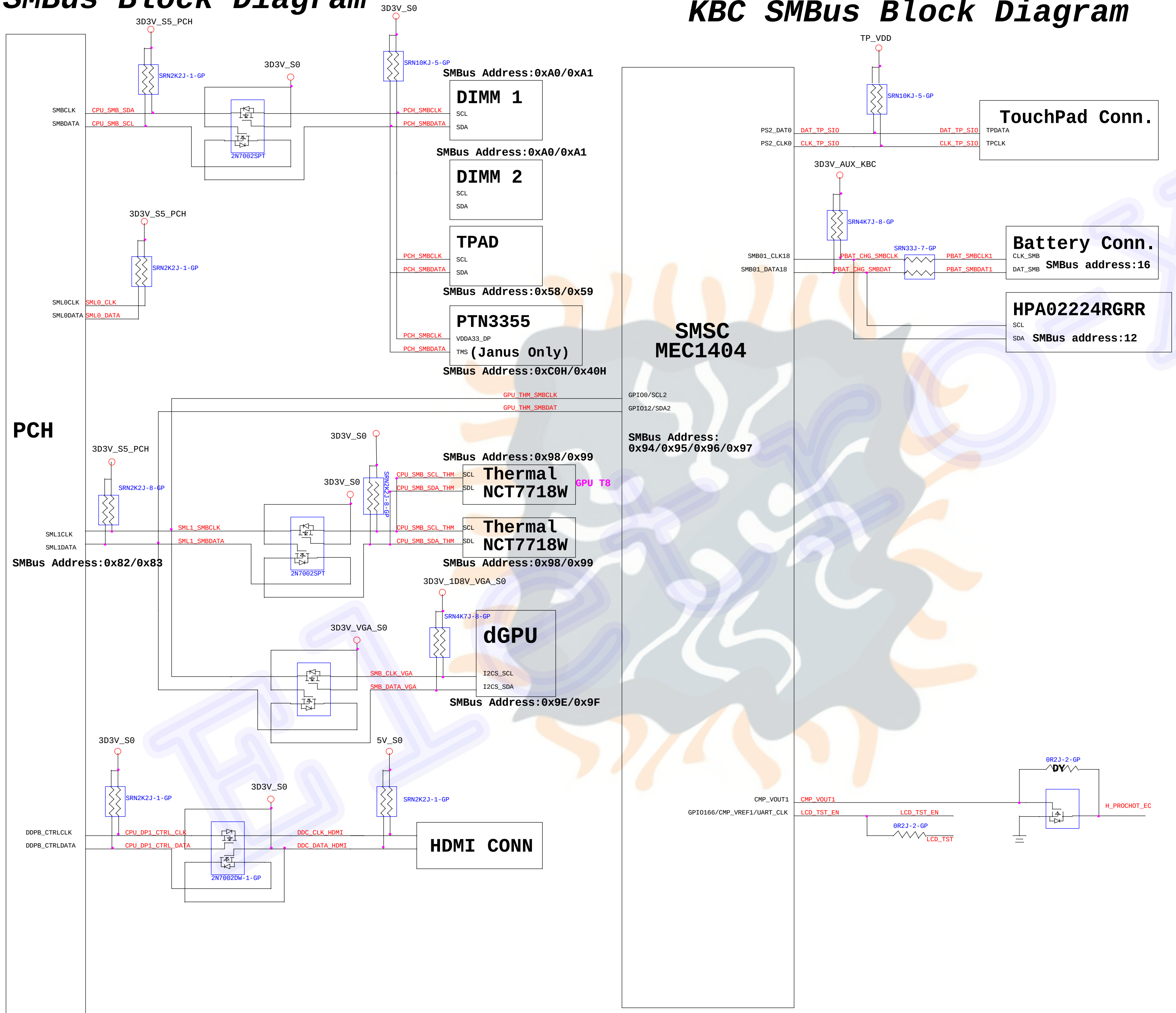
PCH SMBus Block Diagram

KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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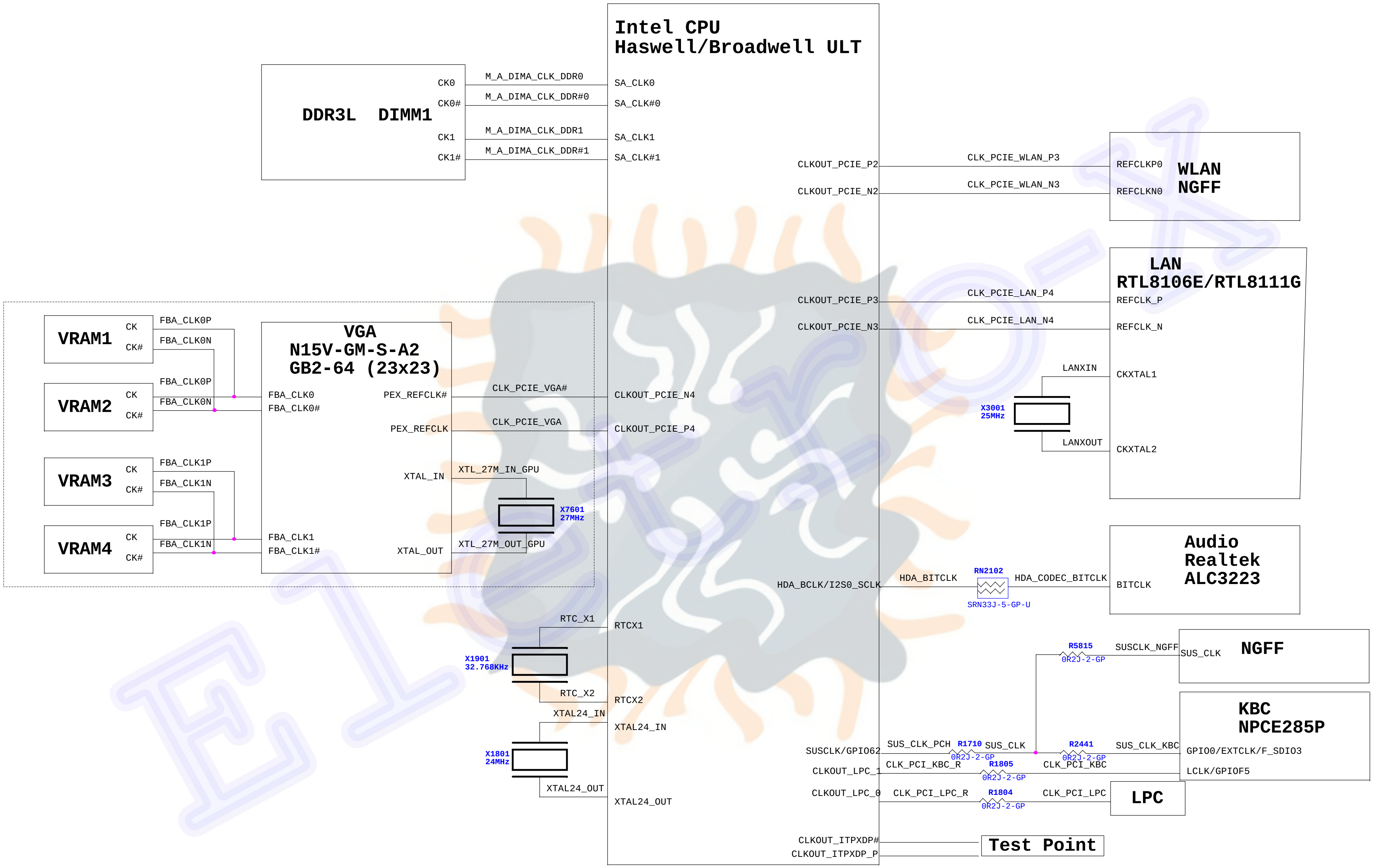
CLK Block Diagram



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Title: CLK Block Diagram

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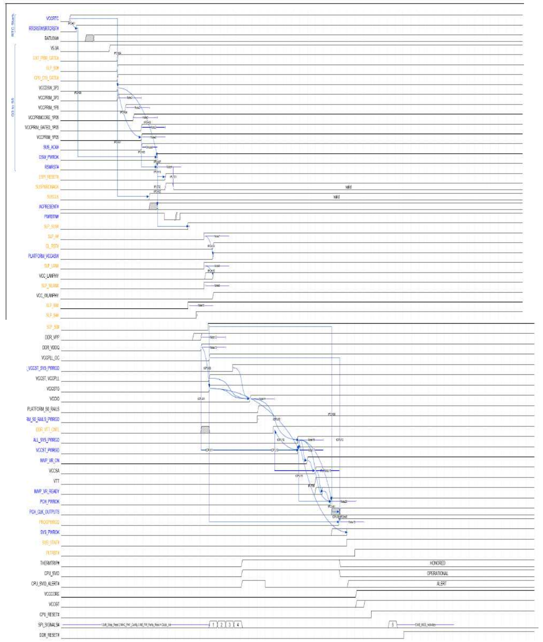
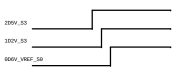
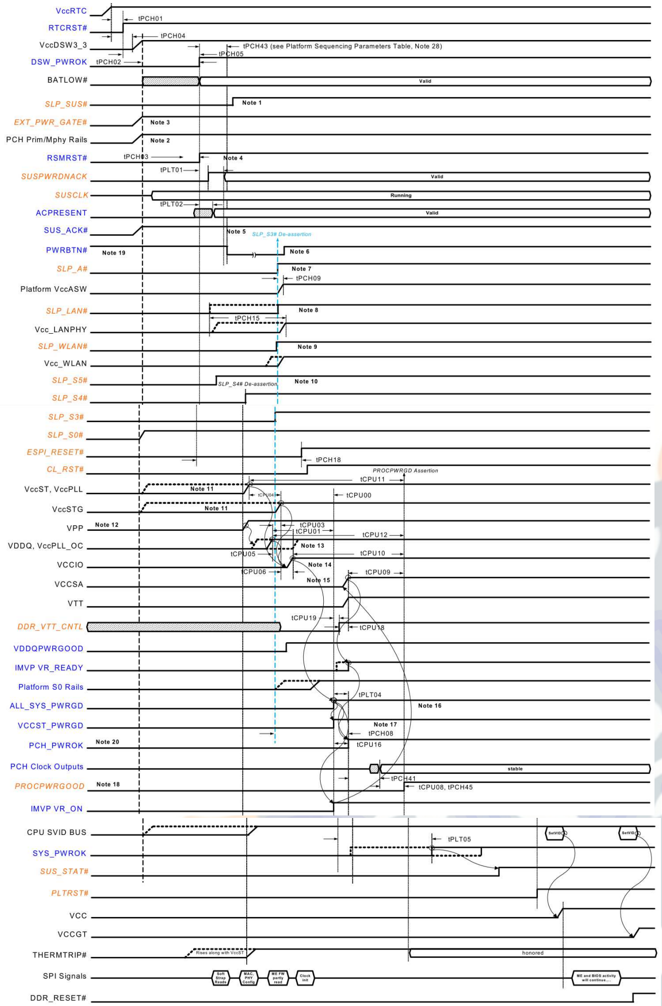
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



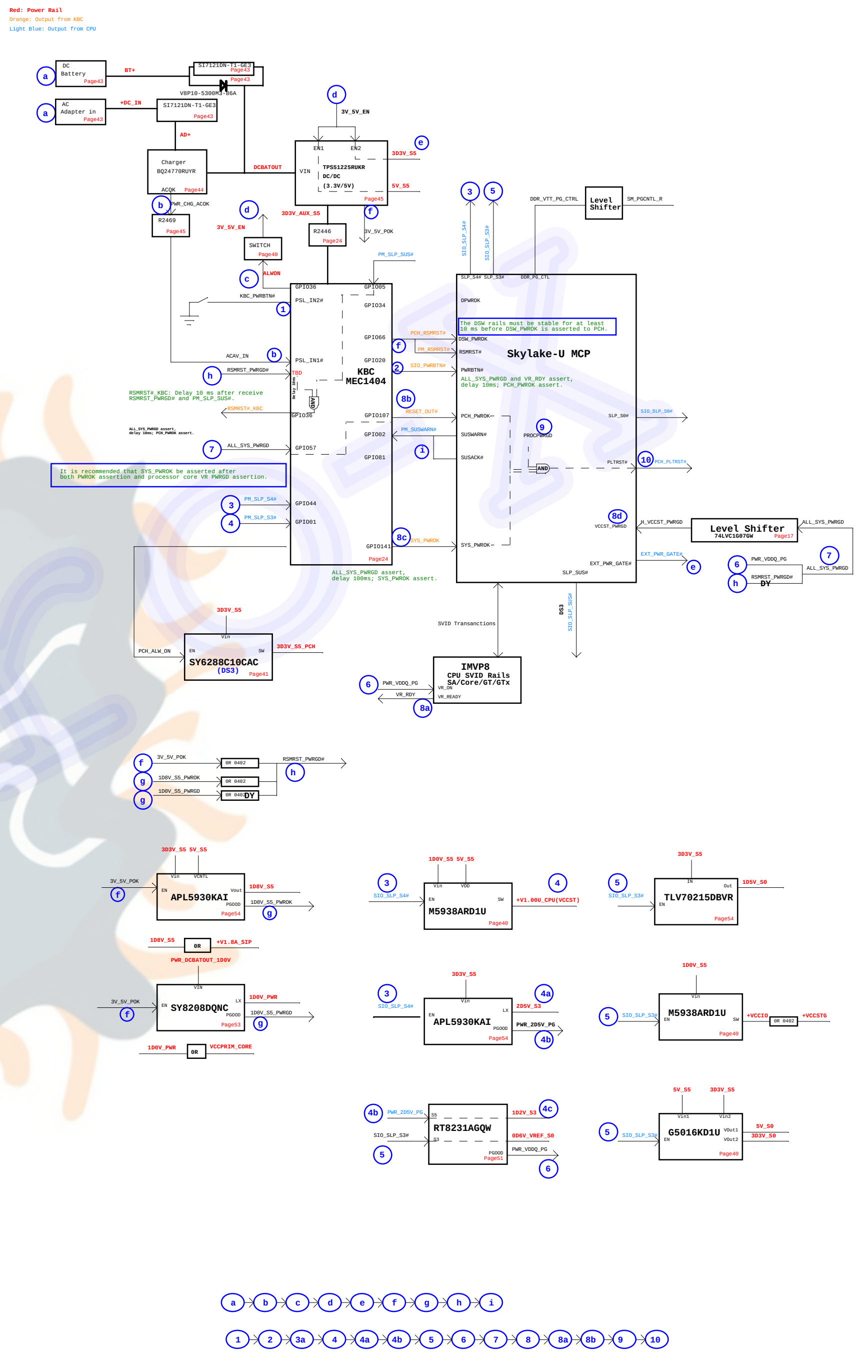
For DDR4 power sequence



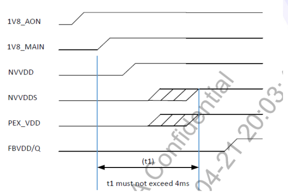
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



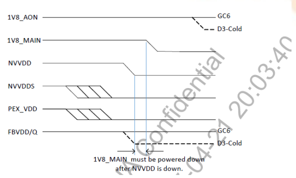
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



NV N17S GPU Power ON sequence



NV N17S GPU Power Down sequence



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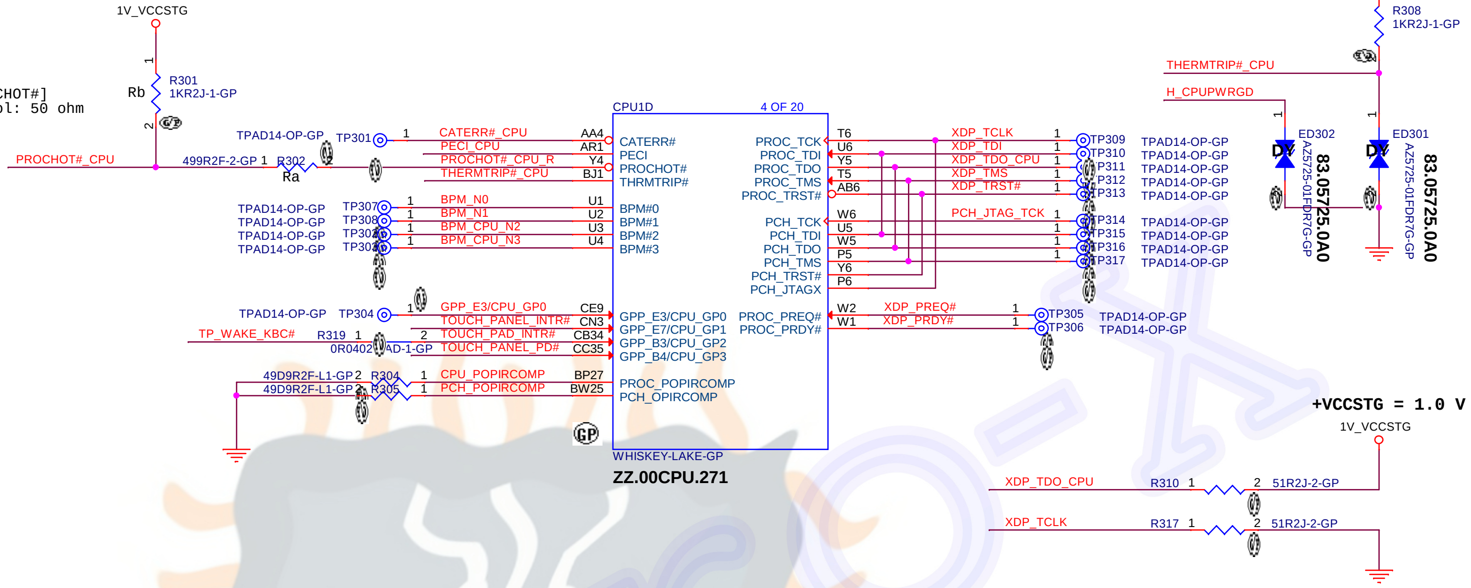
Power Sequence
Mantis_CML

SSID = CPU

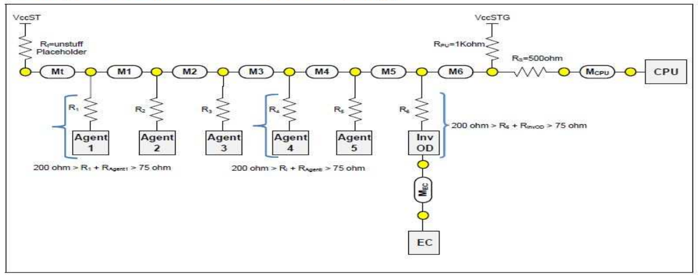
[24] PECI_CPU
[24,44,46] PROCHOT#_CPU
[55] TOUCH_PANEL_INTR#
[24,65] TP_WAKE_KBC#
[17] H_CPUPWRGD
[55] TOUCH_PANEL_PD#

[PECI] and [PROCHOT#]
Impedance control: 50 ohm



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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Title	CPU (THML/JTAG)	
Size A3	Document Number Mantis_CML	Rev A00
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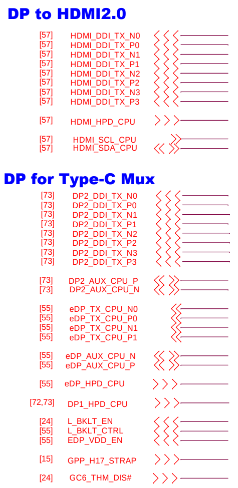
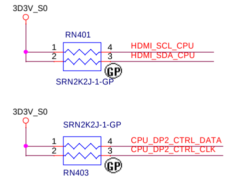
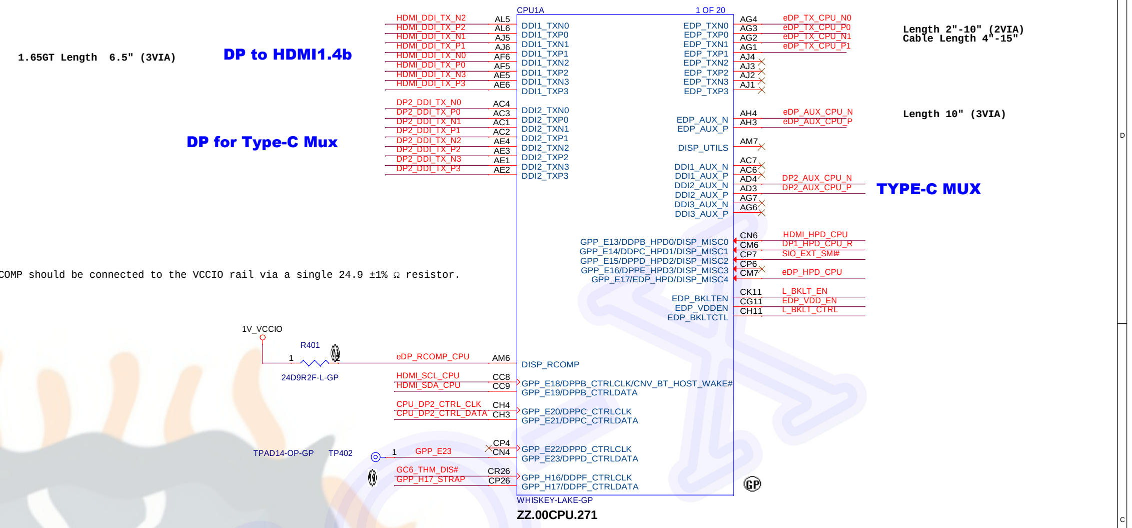
Eletro-X

SSID = CPU







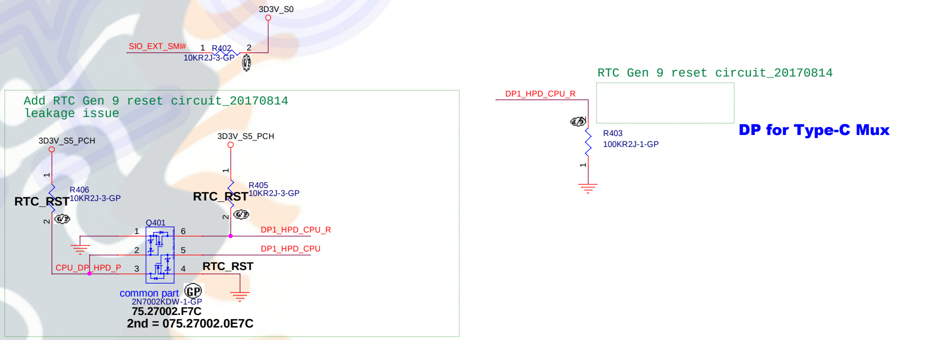
Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



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Title	CPU (DDI/EDP/TBT/TPC/)	
Size A2	Document Number: Mantis_CML	Rev
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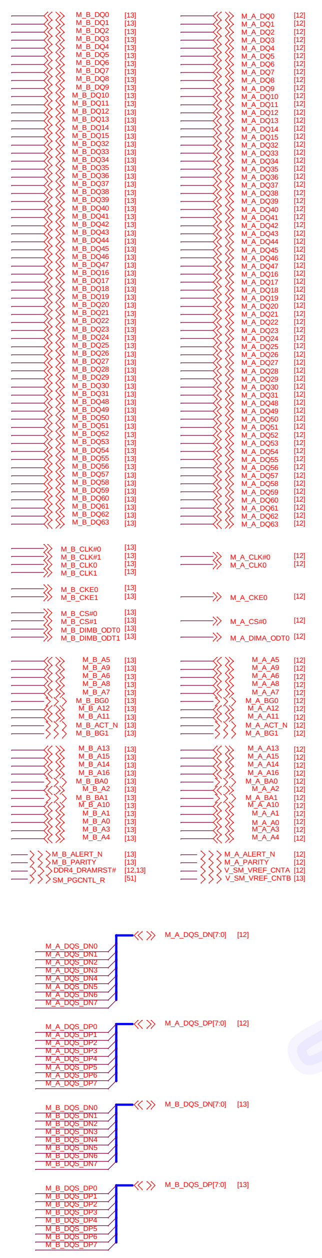
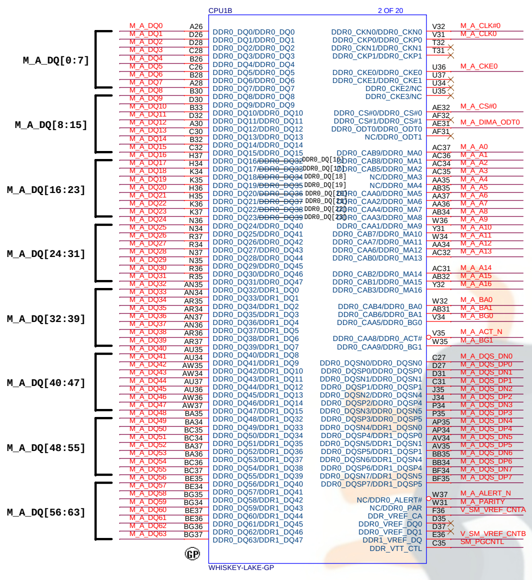
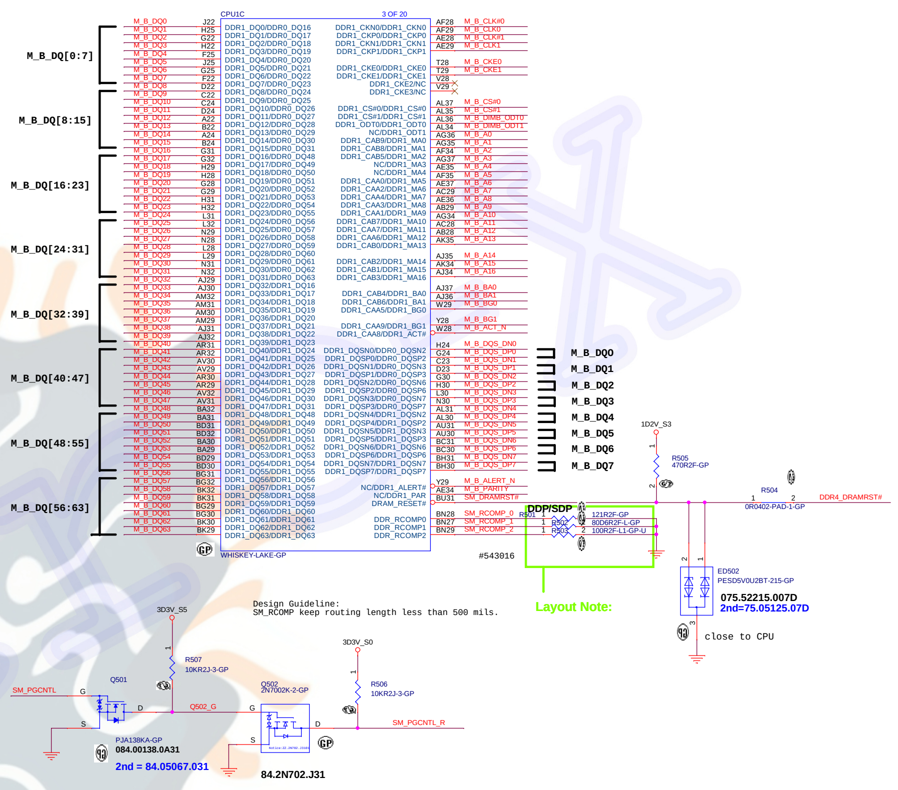
Main Func = CPU

DDR4 ball type: Interleaved Type







DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

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Title	CPU (DDR)
Size: Custom	Document Number: Mantis_CML
Rev	A00
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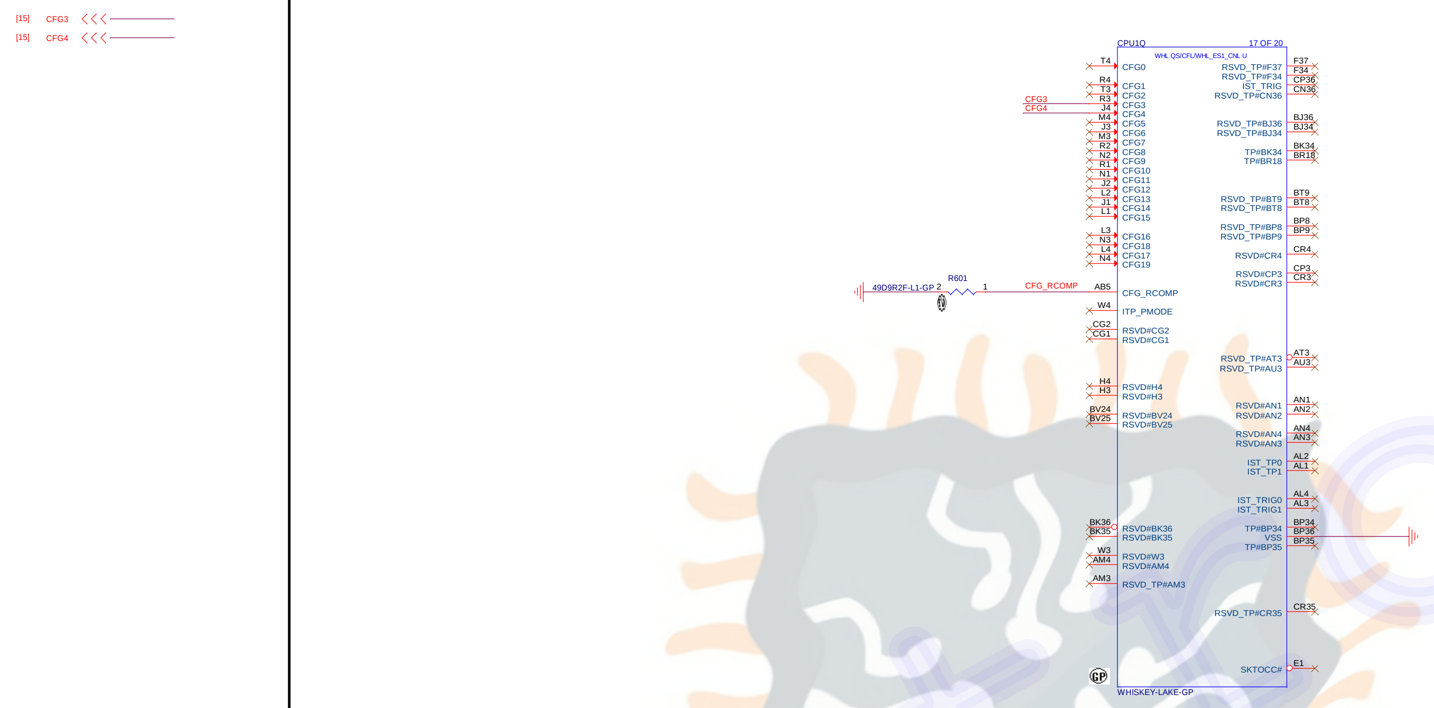
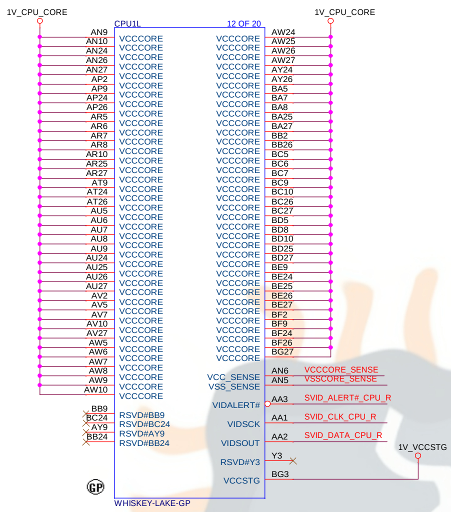
SSID = CPU



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

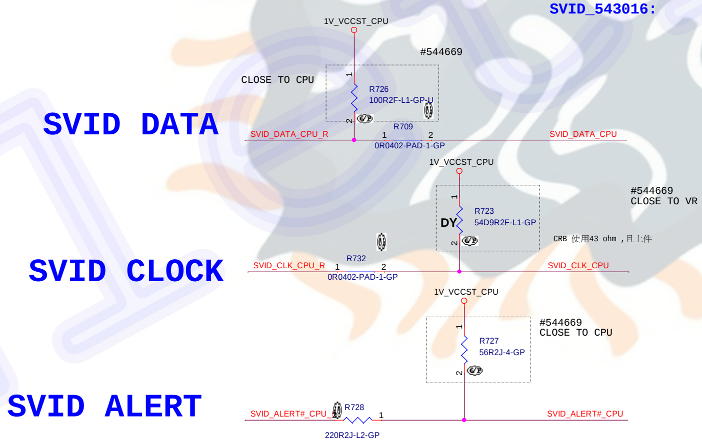
SSID = CPU

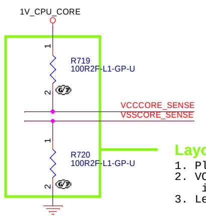
[46] VCCCORE_SENSE
[46] VSSCORE_SENSE
[46] SVID_DATA_CPU
[46] SVID_CLK_CPU
[46] SVID_ALERT#_CPU



Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:





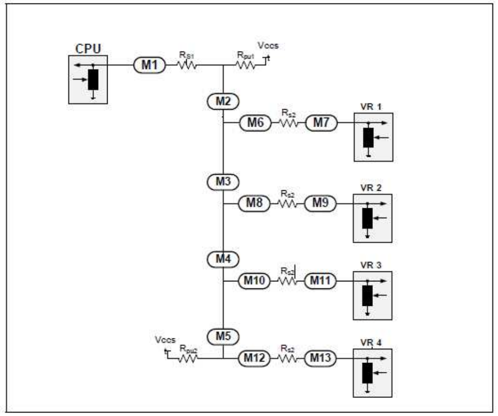
Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE
impedance=50 ohm
3. Length match<25mil

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

Topology Guidelines	
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

. Routing Illustration for SVID Topology



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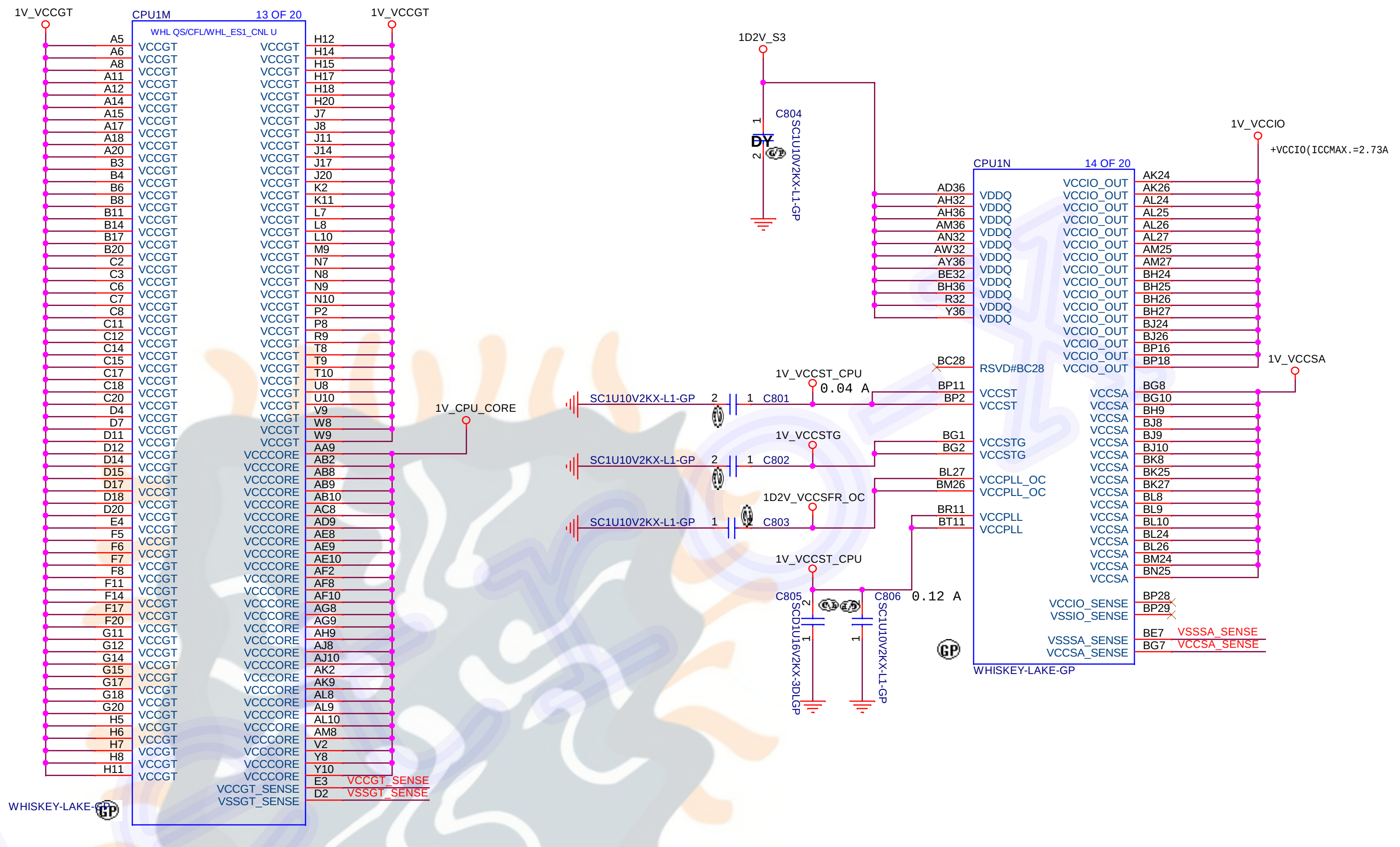
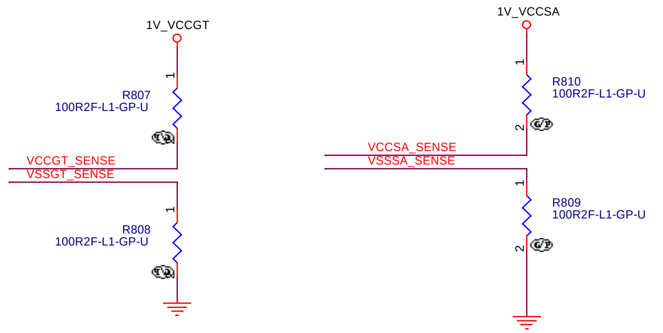
Title	CPU (VCCIN/VID)
Size A2	Document Number Mantis_CML
Date: Tuesday, May 28, 2019	Sheet 7

[46] VSSSA_SENSE
[46] VCCSA_SENSE
[46] VCCGT_SENSE
[46] VSSGT_SENSE



Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



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Title: CPU (VDDQ/VCC/VCCST/VCCSTG)

Size: A3 | Document Number: Mantis_CML | Rev: A00

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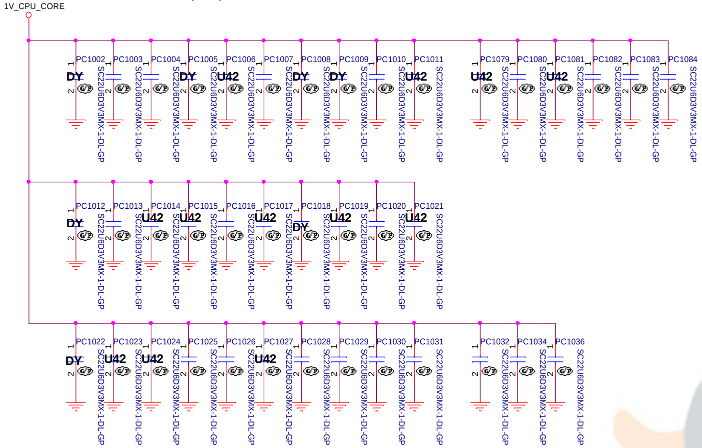
SSID = CPU

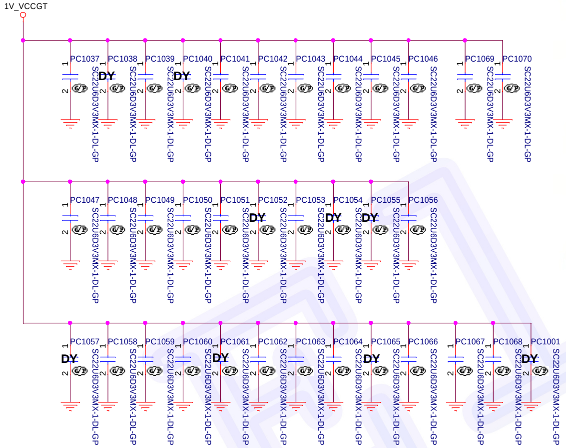
1V_CPU_CORE

22U 0603 x 39 (7DY)



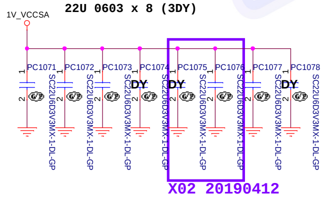
VCCGT

22U 0603 x 35 (9 DY)



VCCSA

22U 0603 x 8 (3DY)



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{GT}	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{ST} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps >Power source.

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DELL

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Title: CPU(CORE Power Cap1)

Size: A2 | Document Number: Mantis_CML

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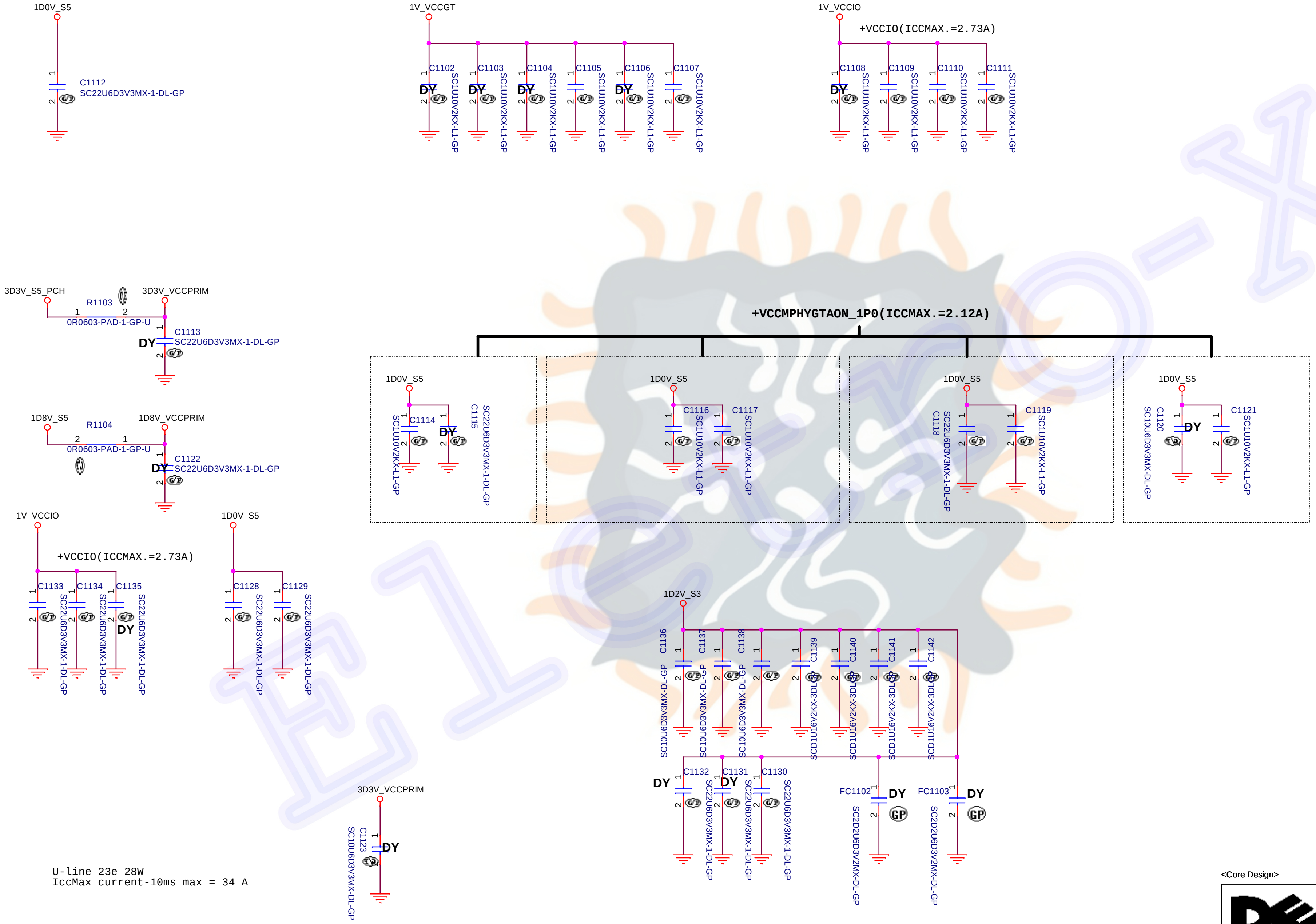
SSID = CPU

PCH DERIVED RAILS

UNSLICED GT

VCCIO



Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

U-line 23e 28W
IccMax current-10ms max = 34 A

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Title	CPU (Power CAP2)
Size A3	Document Number: Mantis_CML
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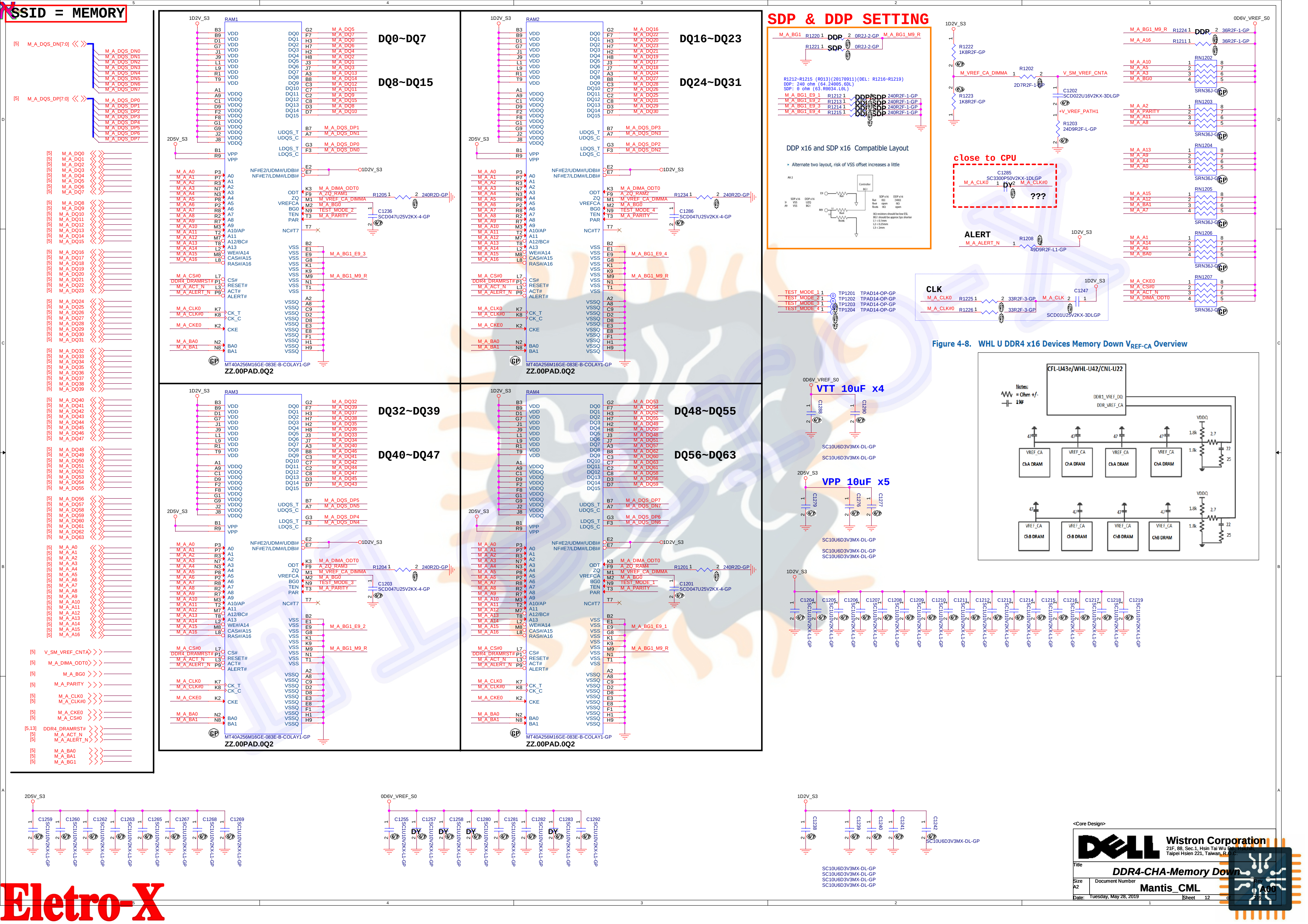
SSID = MEMORY
RAM1
DQ0~DQ7
DQ8~DQ15
RAM2
DQ16~DQ23
DQ24~DQ31
RAM3
DQ32~DQ39
DQ40~DQ47
RAM4
DQ48~DQ55
DQ56~DQ63
MT40A256M16GE-083E-B-COLAY1-GP
ZZ.00PAD.0Q2
SDP & DDP SETTING
DDP
SDP
DDP x16 and SDP x16 Compatible Layout
close to CPU
???
ALERT
CLK
Figure 4-8. WHL U DDR4 x16 Devices Memory Down VREF-CA Overview
CFL-U43e/WHL-U42/CNL-U22
VTT 10uF x4
VPP 10uF x5
<Core Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4-CHA-Memory Down
Size A2
Document Number
Mantis_CML
Rev A00
Date: Tuesday, May 28, 2019
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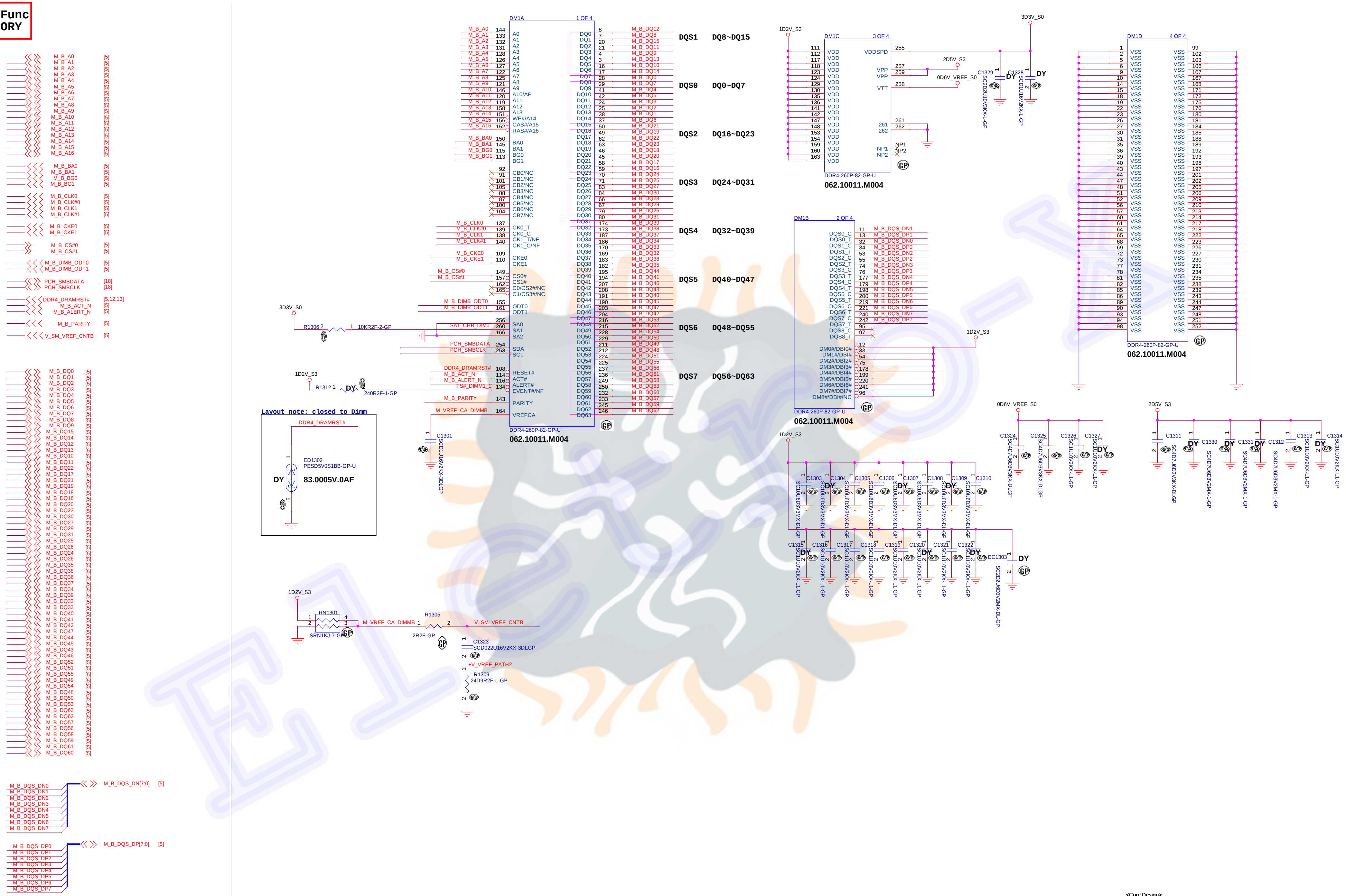
Eletro-X

Main Func = MEMORY



<Core Design>
DELL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR4-CHB-SODIMM
Size A2
Document Number Mantis_CML
Rev A00
Date: Tuesday, May 28, 2019
Sheet 13

Main Func = PCH

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.

GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

PCH strap pin:

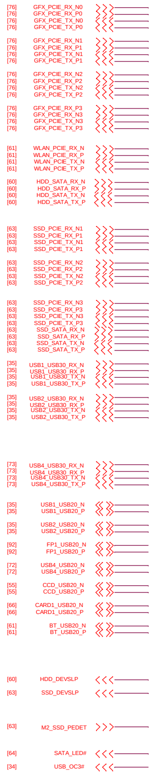
(#543016)

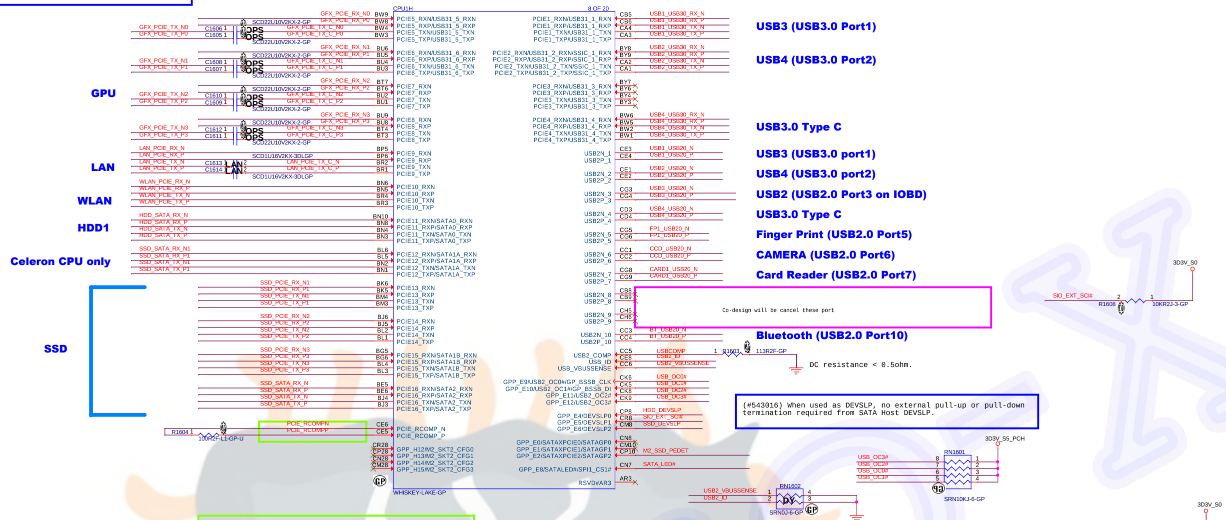
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

Main Func = PCH

(#543016):
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.





(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

	BUCKY	Rogue
USB_OC0#	TYPEC PD	NC
USB_OC1#	Power share	USB3.0 Power
USB_OC2#	USB3.0 Power	NC
USB_OC3#	USB2.0 Power	TYPEC PD

Layout Note:

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

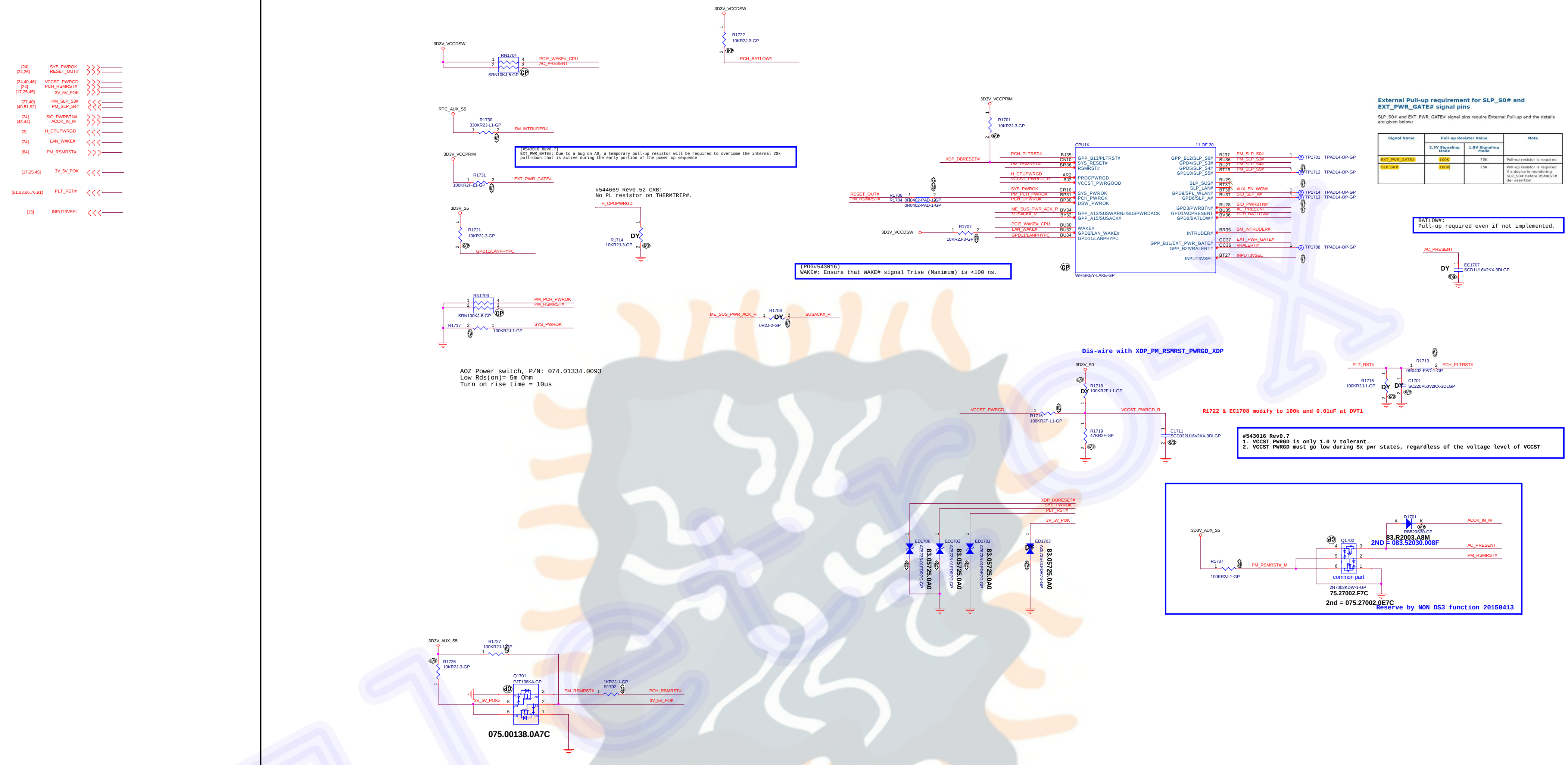
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

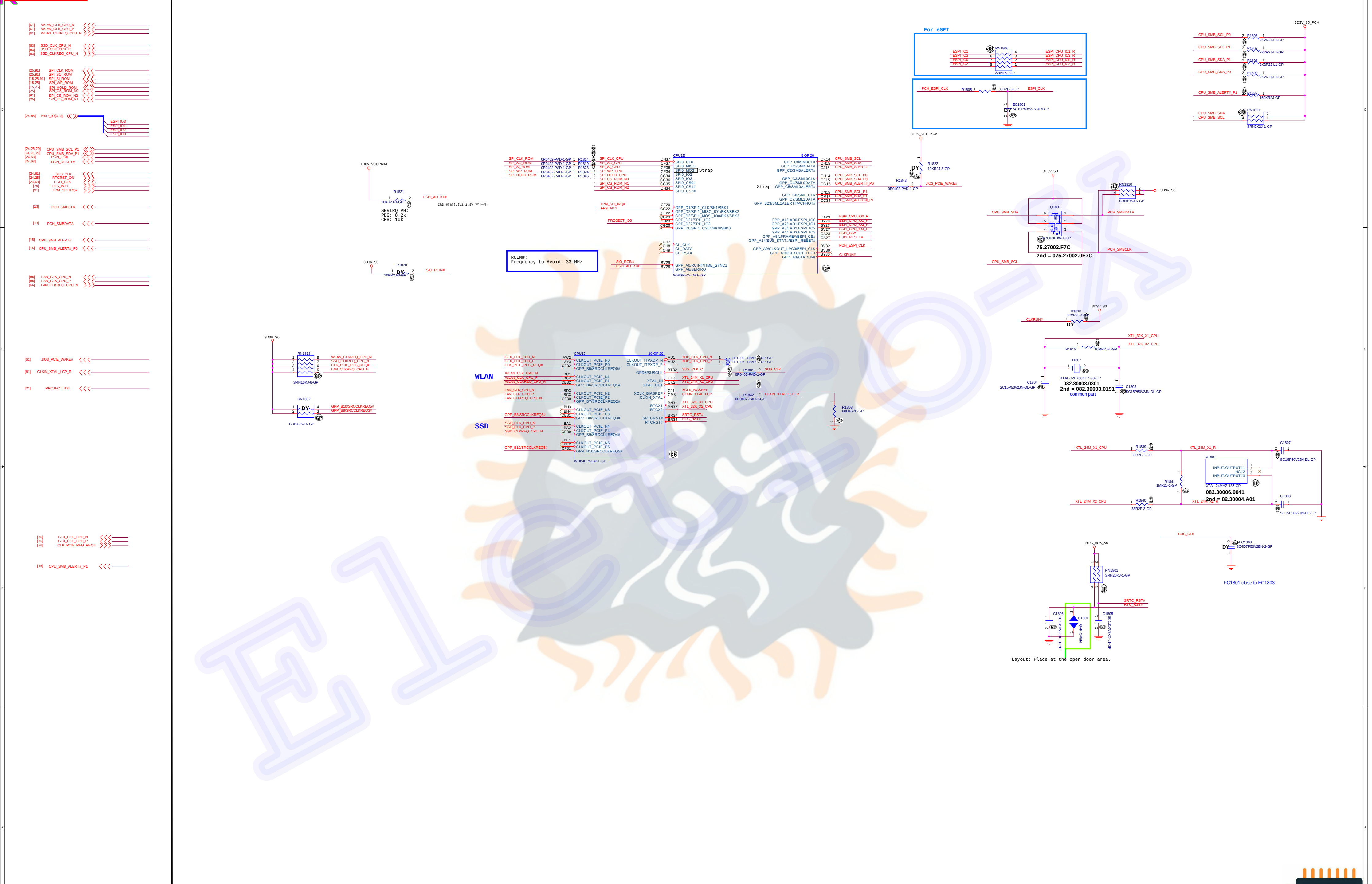
PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

SSID = PCH



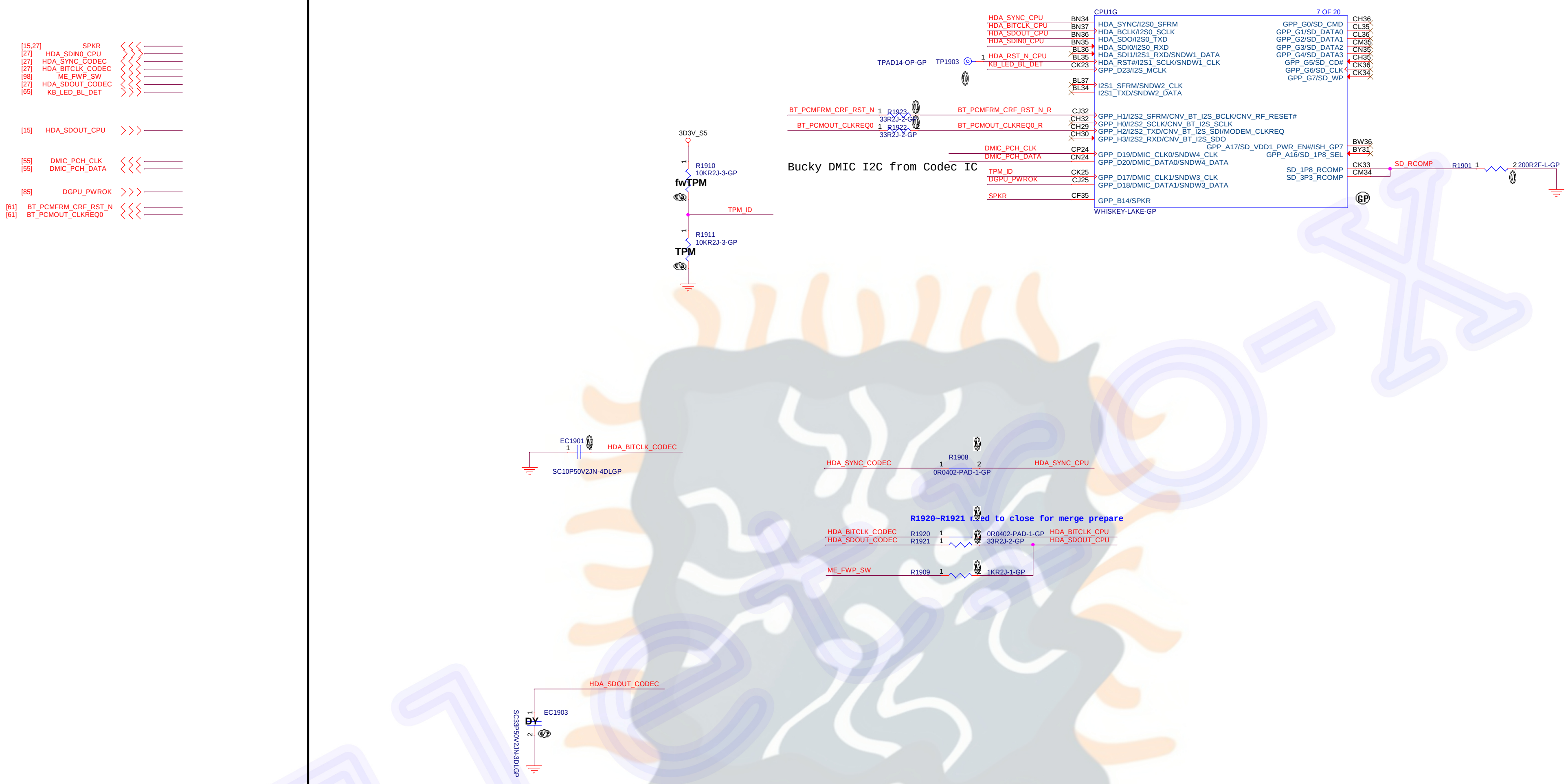
<Core Design>
Wistron Corporation
Title: PCH_(PMU)
Size: A1
Document Number: Mantis_CML
Rev: A00
Date: Tuesday, May 28, 2019

SSID = PCH



<Core Design>
Wistron Corporation
CPU (SPI/ESPI/SMBS/XTAL/CLK)
Mantis_CML
Date: Tuesday, May 28, 2019

SSID = PCH



<Core Design>

Wistron Corporation
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Title	CPU (HAD/I2S/SD/DMIC)
Size	A2
Document Number	Mantis_CML
Date:	Tuesday, May 28, 2019
Sheet	19

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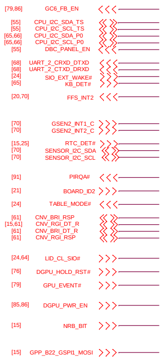
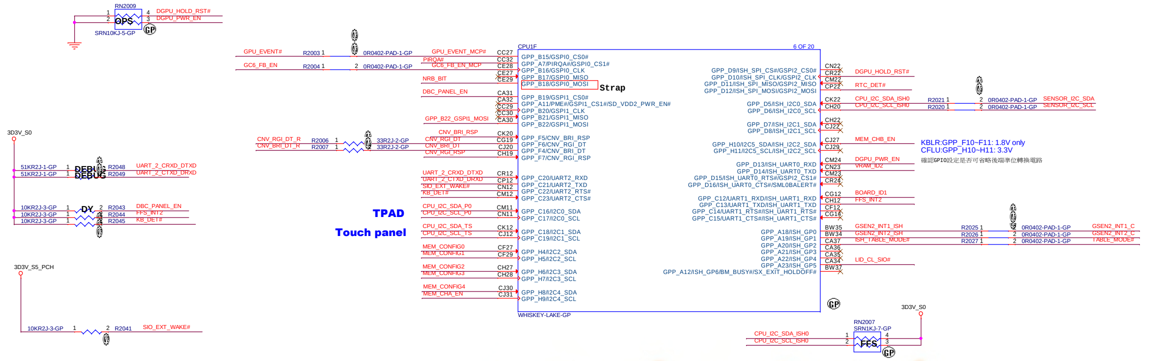
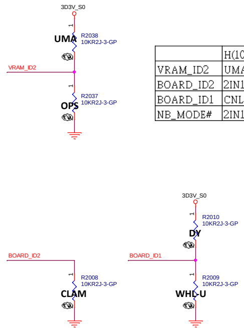




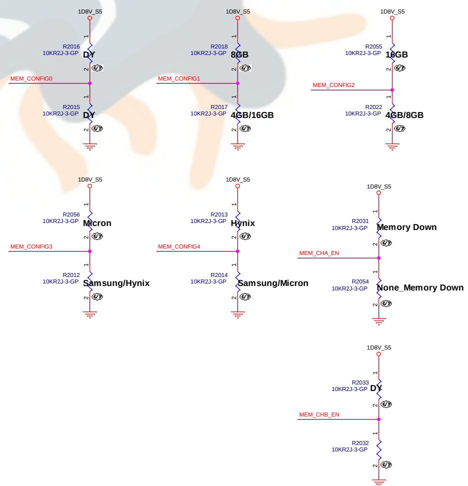
(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.



	H(10K)	L(10K)
VRAM_ID2	UMA	OPS
BOARD_ID2	2IN1	CLAM
BOARD_ID1	CNL	WHL-U
NB_MODE#	2IN1	CLAM

RAM ID

Vendor	MEM_CONFIG[0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Wistron P/N	Capacity
Hynix	NA	00	01	H5AN8G6NCJR-VKC	WDFJW$BA	4GB
Micron	NA	00	10	MT40A512M16LY-075:E	WDFJW$CA	4GB
Samsung	NA	00	00	K4A8G165WC-BCTD	WDFJW$AA	4GB
Hynix	NA	10	01	H5ANAG6NCMR-VKC	6K9H9$BA	8GB
Micron	NA	10	10	MT40A1G16KNR-075:E	6K9H9$CA	8GB
Samsung	NA	10	00	K4AAG165WB-MCTD	6K9H9$AA	8GB



Wistron Corporation

CPU (UART/I2C/ISH)

Mantis_CML

Tuesday, May 28, 2019

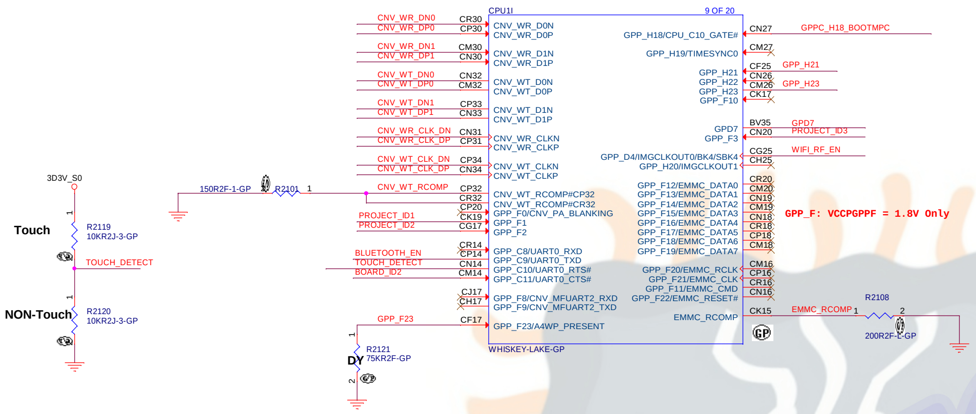
SSID = PCH

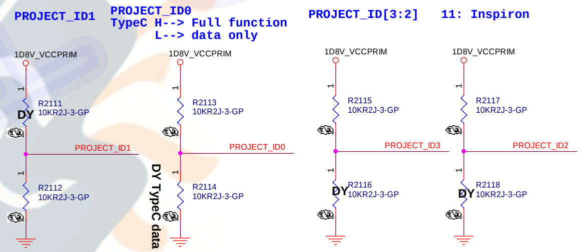
SSID = PCH

[40] GPPC_H18_BOOTMPC
[61] WIFI_RF_EN
[61] BLUETOOTH_EN
[20] BOARD_ID2
[15] GPP_H23
[15] GPP_H21

[61] CNV_WT_CLK_DN
[61] CNV_WT_CLK_DP
[61] CNV_WT_DP0
[61] CNV_WT_DN0
[61] CNV_WT_DP1
[61] CNV_WT_DN1
[61] CNV_WR_CLK_DN
[61] CNV_WR_CLK_DP
[61] CNV_WR_DP0
[61] CNV_WR_DN0
[61] CNV_WR_DP1
[61] CNV_WR_DN1

[18] PROJECT_ID0
[15] GPD7





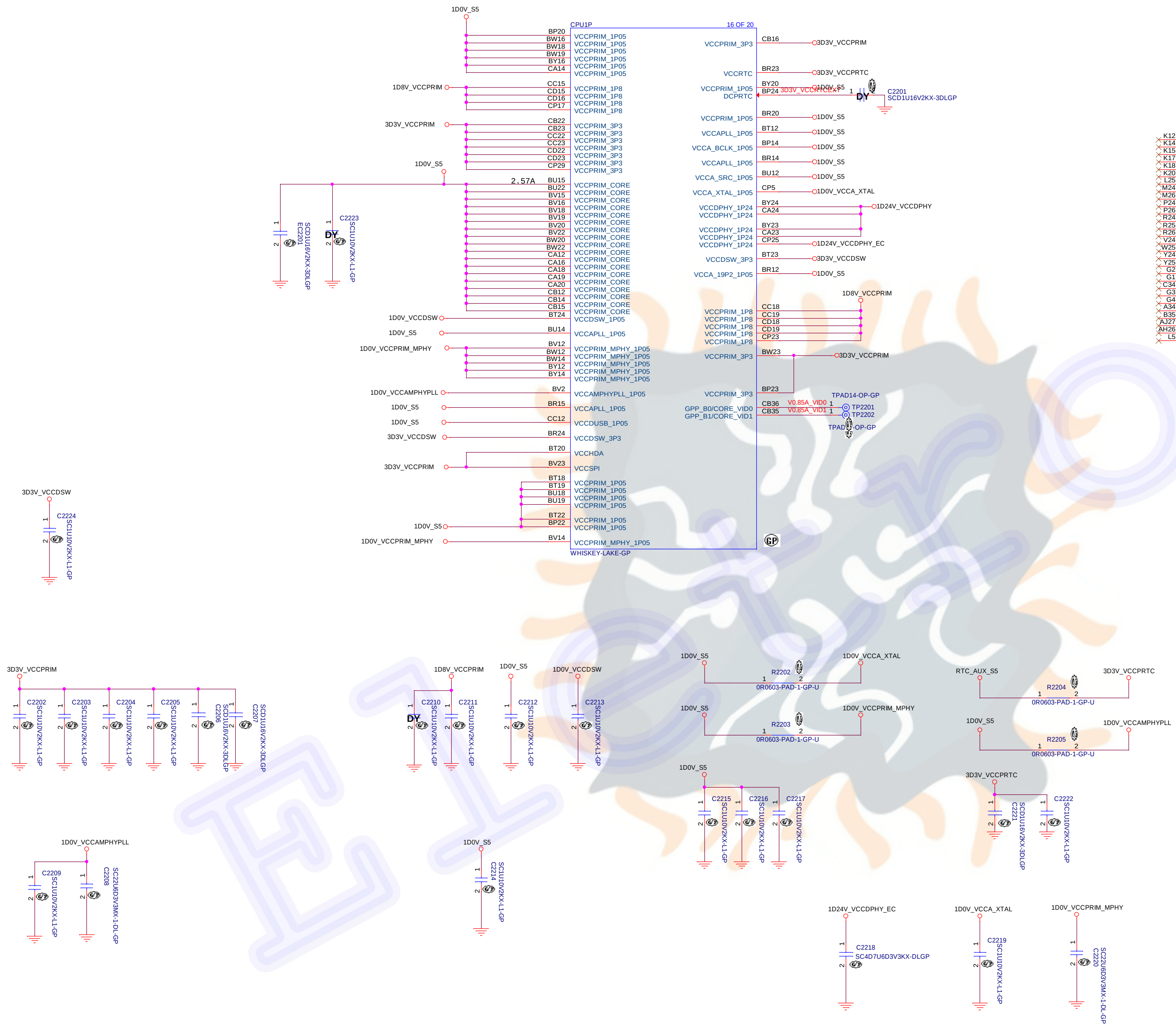
	H(10K)	L(10K)	Note
PROJECT_ID0	TypeC full	TypeC data	TypeC function det
PROJECT_ID1	Non	Non	follow Rogue define
PROJECT_ID2	Non	Non	
PROJECT_ID3	Non	Non	

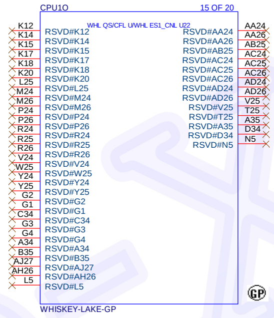
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CSI/EMMC/CNVI)
Size: A2 Document Number: Mantis_CML Rev: A00
Date: Tuesday, May 28, 2019 Sheet 21

SSID = PCH





Layout Note:

1. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP22, BP20, BW16, BW18, BW19, BY16, CA14, BR20, BY20, BT18, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BY12, BY14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.0A / V0.85A	VCCPRIM_CORE	BU15, BU22, BV15, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23,CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29,BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BY24, CA24	4.7uF	0402	1	E	CP25

Notes:
1. Placeholder only. Does not need to be stuffed.
2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
4. For description of (R)unway, and (E)dge decoupling capacitor placement, refer to "Loop Inductance Reduction Decoupling".
5. Refer to Electromagnetic Interference chapter for recommended placement
6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.

<Core Design>

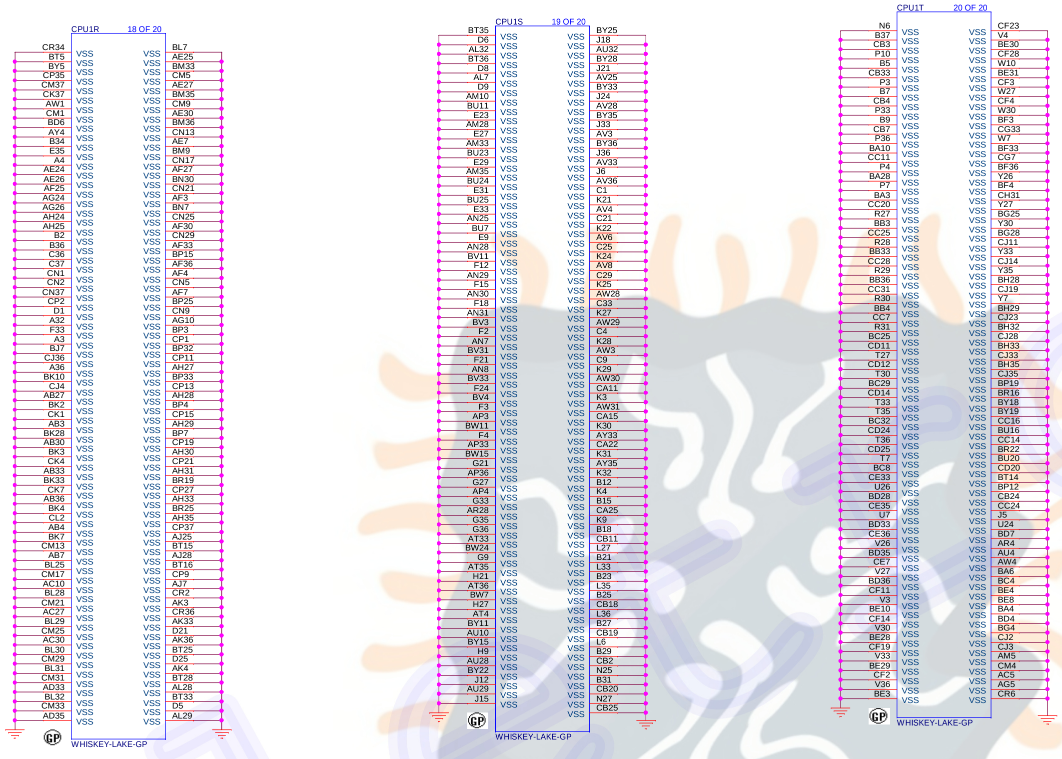
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

Size: A2 | Document Number: Mantis_CML

Date: Tuesday, May 28, 2019 | Sheet 22

SSID = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

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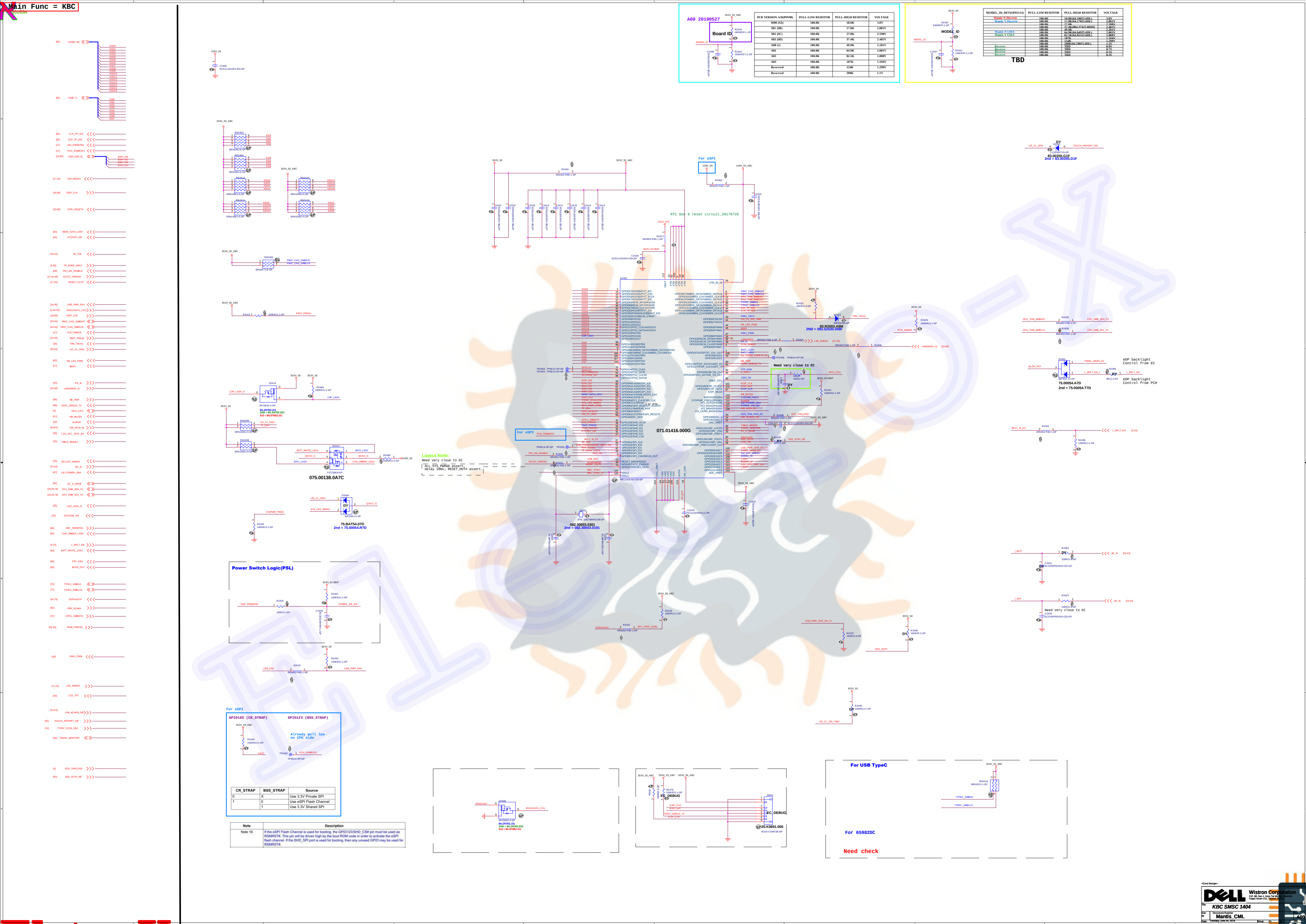
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH_(VSS)

Size: A2 | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, May 28, 2019 | Sheet 23

Main Func = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X01 (SB)	100.0K	17.8K	2.801V
X02 (SC)	100.0K	27.0K	2.598V
X03 (SD)	100.0K	37.4K	2.402V
A00 (1)	100.0K	49.9K	2.201V
A01	100.0K	64.9K	2.001V
A02	100.0K	82.5K	1.808V
A03	100.0K	107K	1.594V
Reserved	100.0K	154K	1.299V
Reserved	100.0K	200K	1.1V

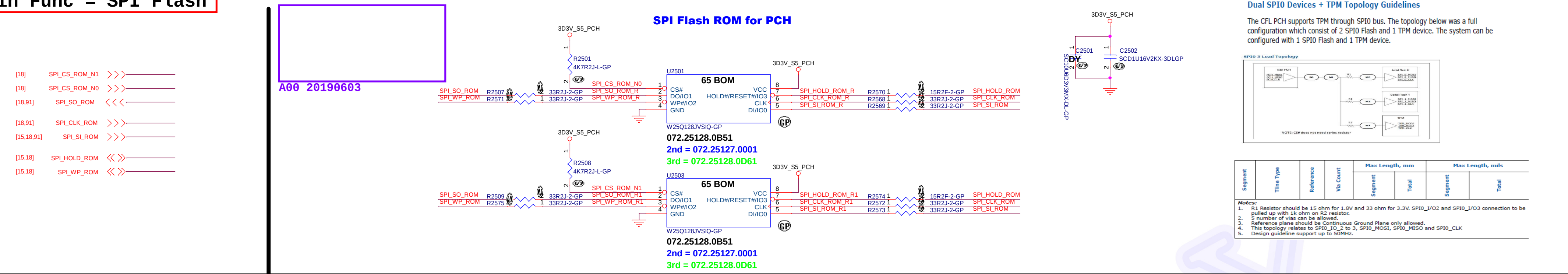
MODEL_ID_DET(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Mantis N Discrete	100.0K	10.0K(64.10025.6DL)	3.0V
Mantis V Discrete	100.0K	17.8K(64.17825.6DL)	2.801V
	100.0K	27.0K	2.598V
	100.0K	37.4K(064.37425.06DS)	2.402V
	100.0K	49.9K	2.201V
Mantis N UMA	100.0K	64.9K(64.64925.6DL)	2.001V
Mantis V UMA	100.0K	82.5K(64.82525.6DL)	1.808V
	100.0K	107K	1.594V
	100.0K	154K	1.299V
	100.0K	200K(64.20035.6DL)	1.1V
Reserve	100.0K	TBD	0.9V
Reserve	100.0K	TBD	0.7V
Reserve	100.0K	TBD	0.5V
Reserve	100.0K	TBD	0.3V

TBD

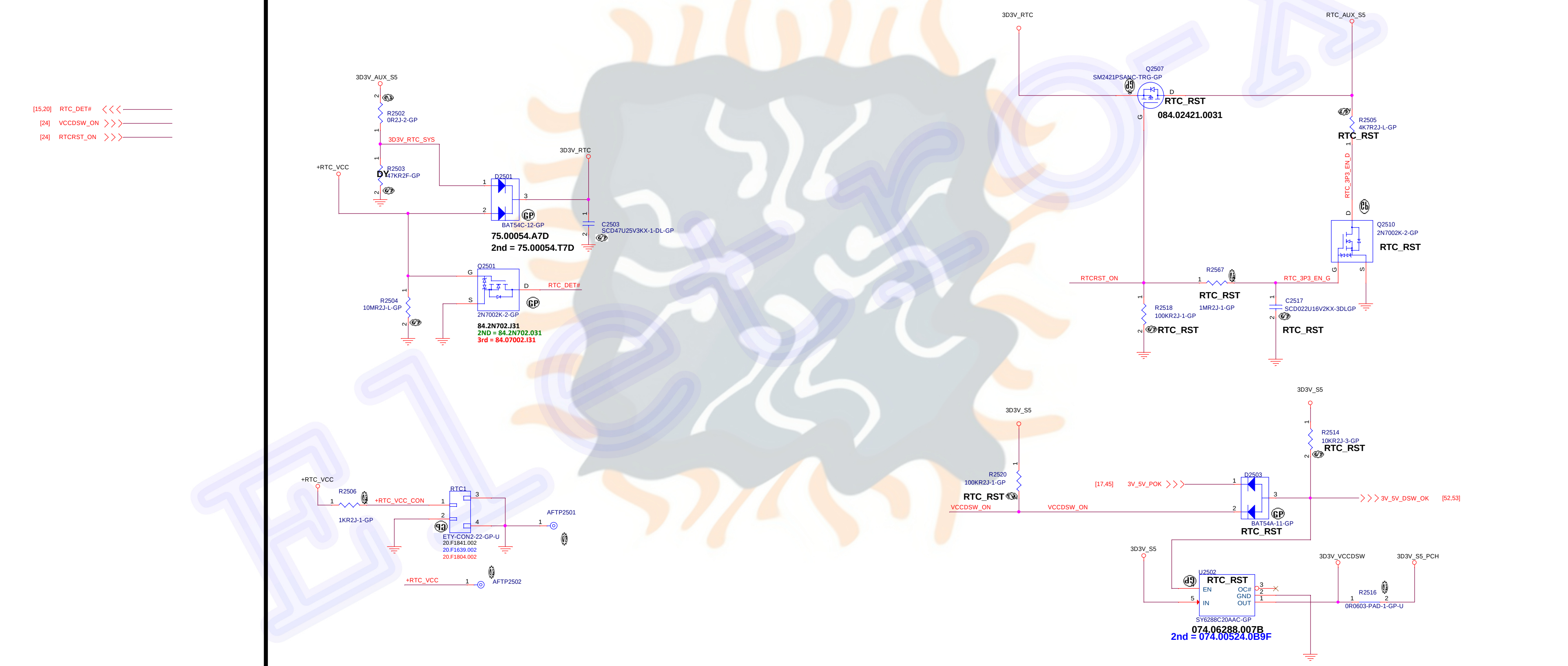
CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Main Func = SPI Flash



Main Func = RTC



<Core Design>

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Title: Flash

Size A2 | Document Number: Mantis_CML | Rev A00

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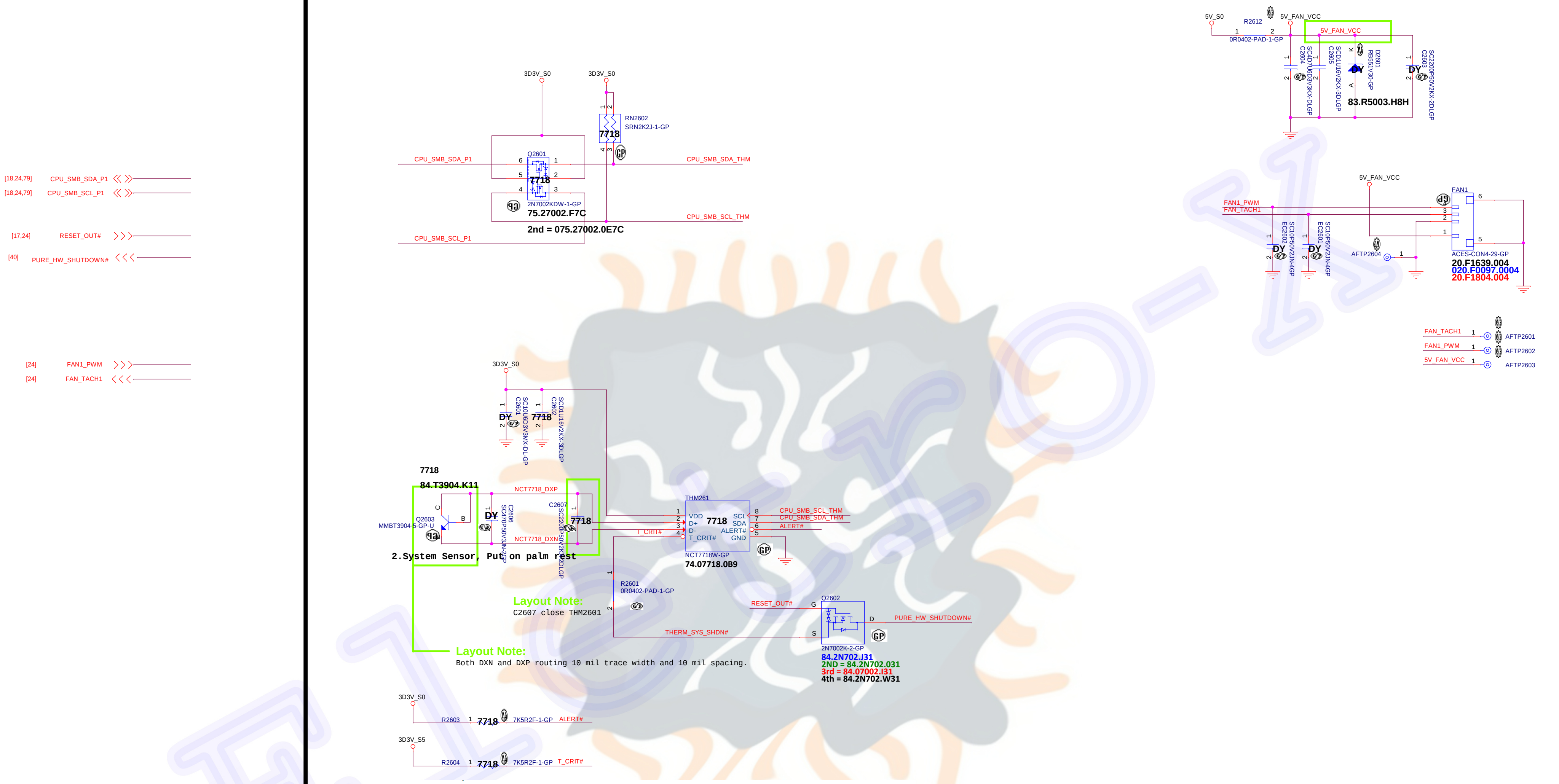
Eletro-X

Main Func = Thermal Sensor

PWM FAN1



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size A2 | Document Number: Mantis_CML | Rev A00

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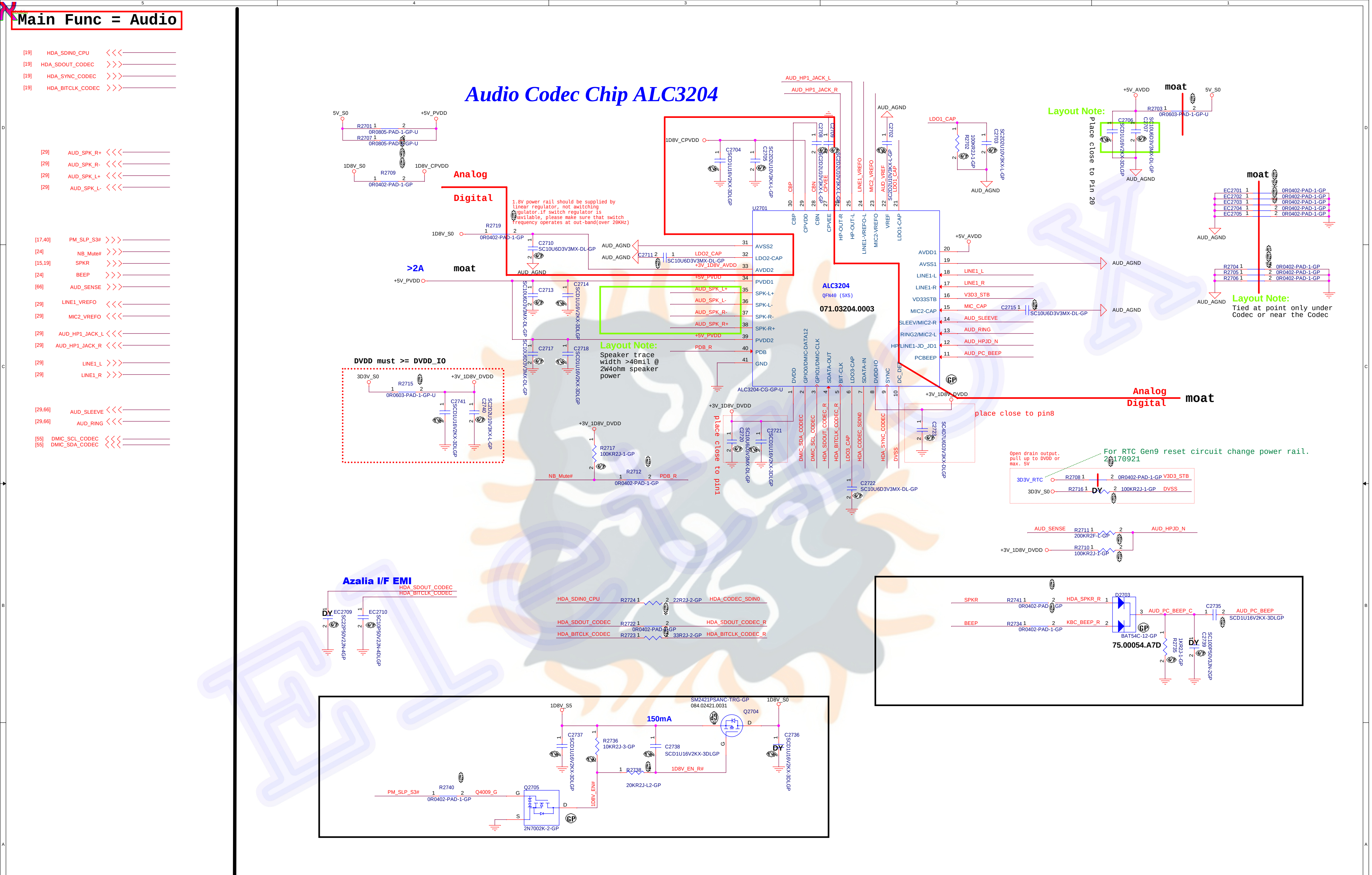

<Core Design>

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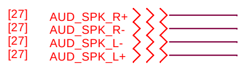
Title: Audio Codec ALC3204

Size: A2 | Document Number: Mantis_CML | Rev: A00

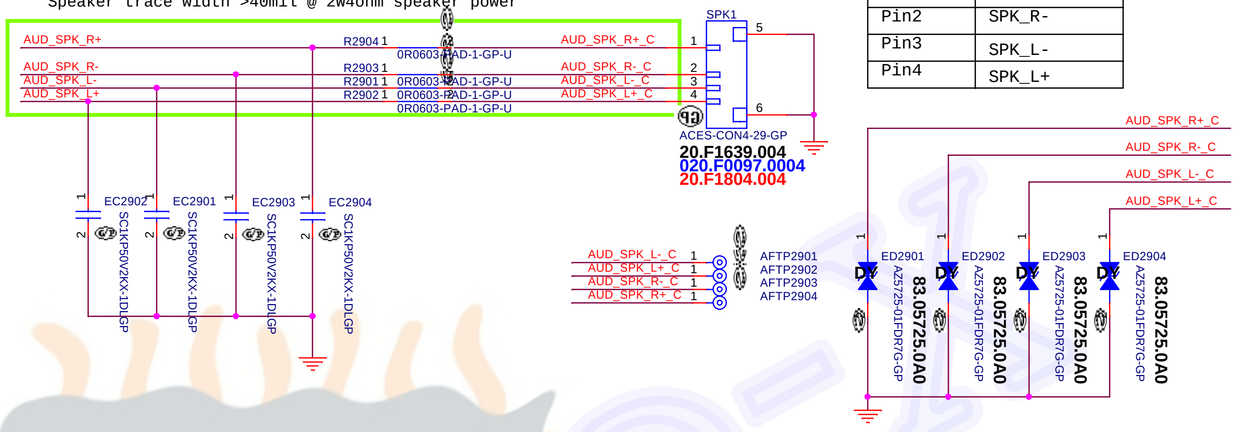
Date: Tuesday, May 28, 2019 | Sheet 27

Main Func = Audio



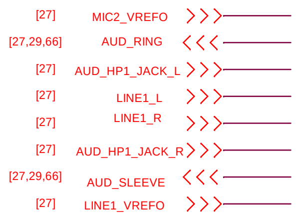
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

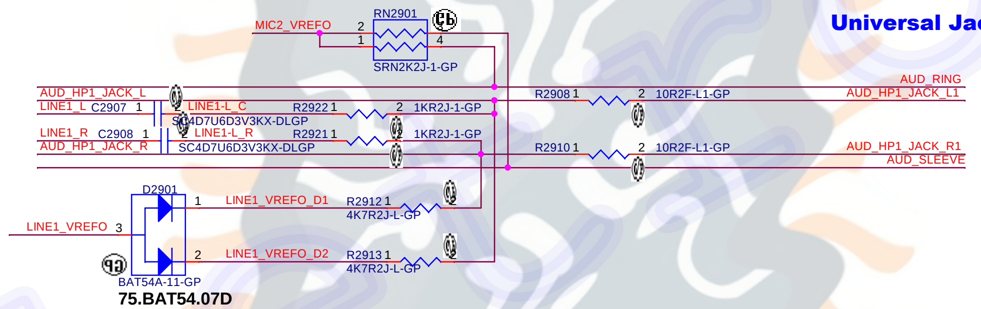


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L-
Pin4	SPK_L+

From Codec



Universal Jack (Moved to I/O Board)



To IO Board

<Core Design>

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Title	Audio IO	
Size A3	Document Number: Mantis_CML	Rev A00
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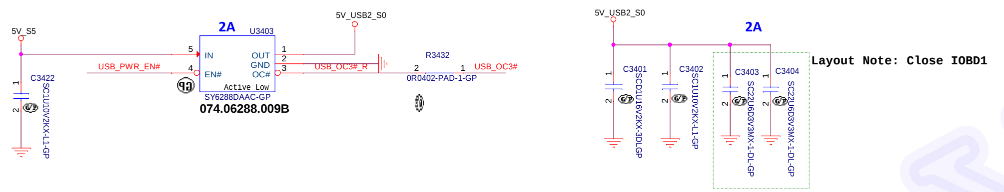
Eletro-X

Main Func = USB2.0

[16] USB_OC3#
[24,35] USB_PWR_EN#

USB2.0 Port3 (IO Board)



<Core Design>

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Title	USB2.0 CONN
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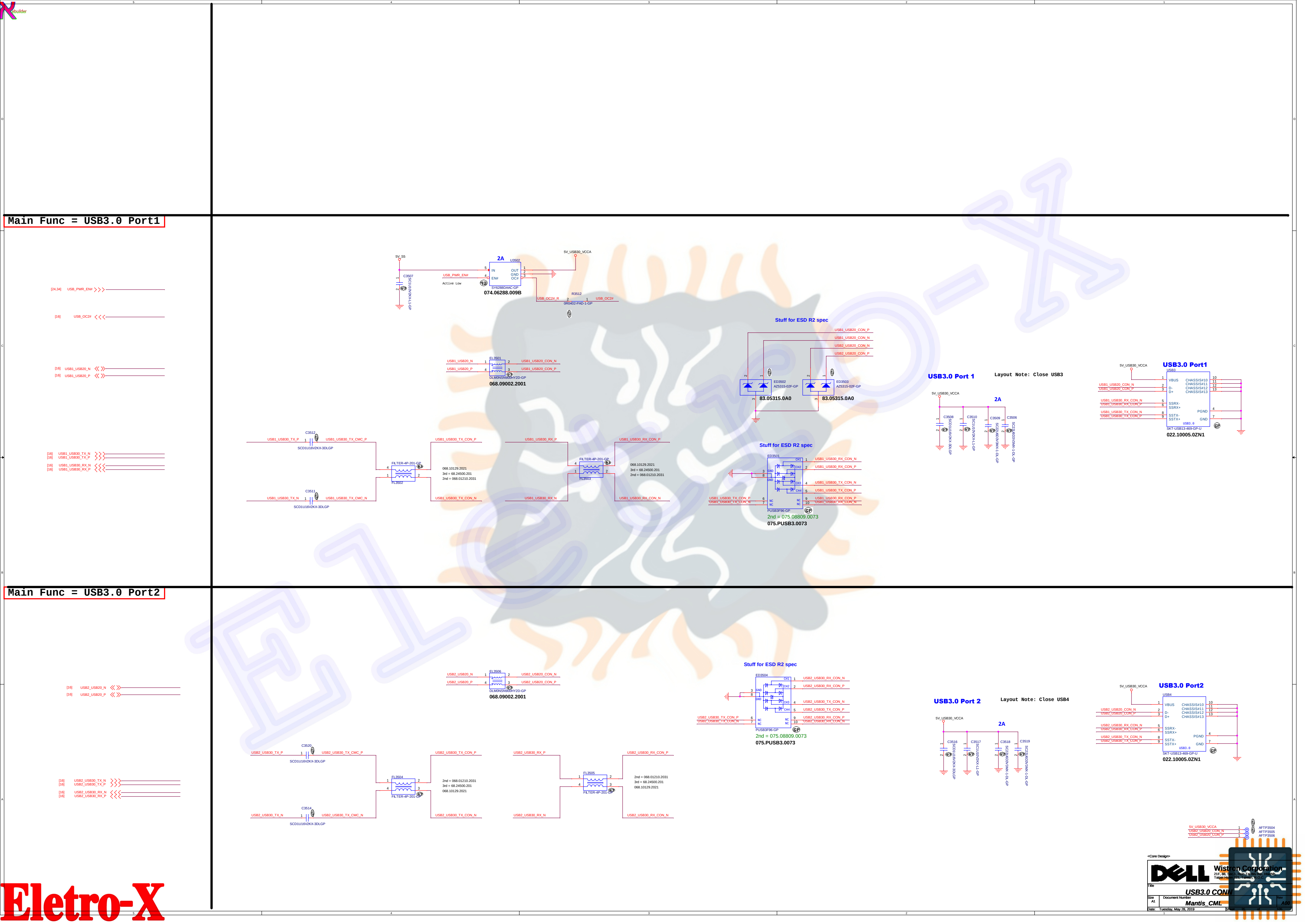

Main Func = USB3.0 Port1
Main Func = USB3.0 Port2
2A
U3502
5V_S5
5V_USB30_VCCA
USB_PWR_EN#
Active Low
SY6288D4AC-GP
074.06288.009B
R3512
USB_OC2#_R
USB_OC2#
0R0402-PAD-1-GP
C3507
Stuff for ESD R2 spec
EL3501
DLM0NSN900HY2D-GP
068.09002.2001
ED3502
AZ5315-02F-GP
83.05315.0A0
ED3503
AZ5315-02F-GP
83.05315.0A0
USB3.0 Port 1
Layout Note: Close USB3
USB3.0 Port1
USB3
SKT-USB13-469-GP-U
022.10005.0ZN1
C3512
SCD1U16V2KX-3DLGP
C3511
FILTER-4P-201-GP
FL3502
FL3503
068.10129.2021
3rd = 68.24500.201
2nd = 068.01210.2031
ED3501
PUSB3F96-GP
2nd = 075.08809.0073
075.PUSB3.0073
EL3506
ED3504
USB3.0 Port 2
Layout Note: Close USB4
USB3.0 Port2
USB4
C3520
C3514
FL3504
FL3505
Eletro-X
Wistron Corporation
USB3.0 CONN
Mantis_CML
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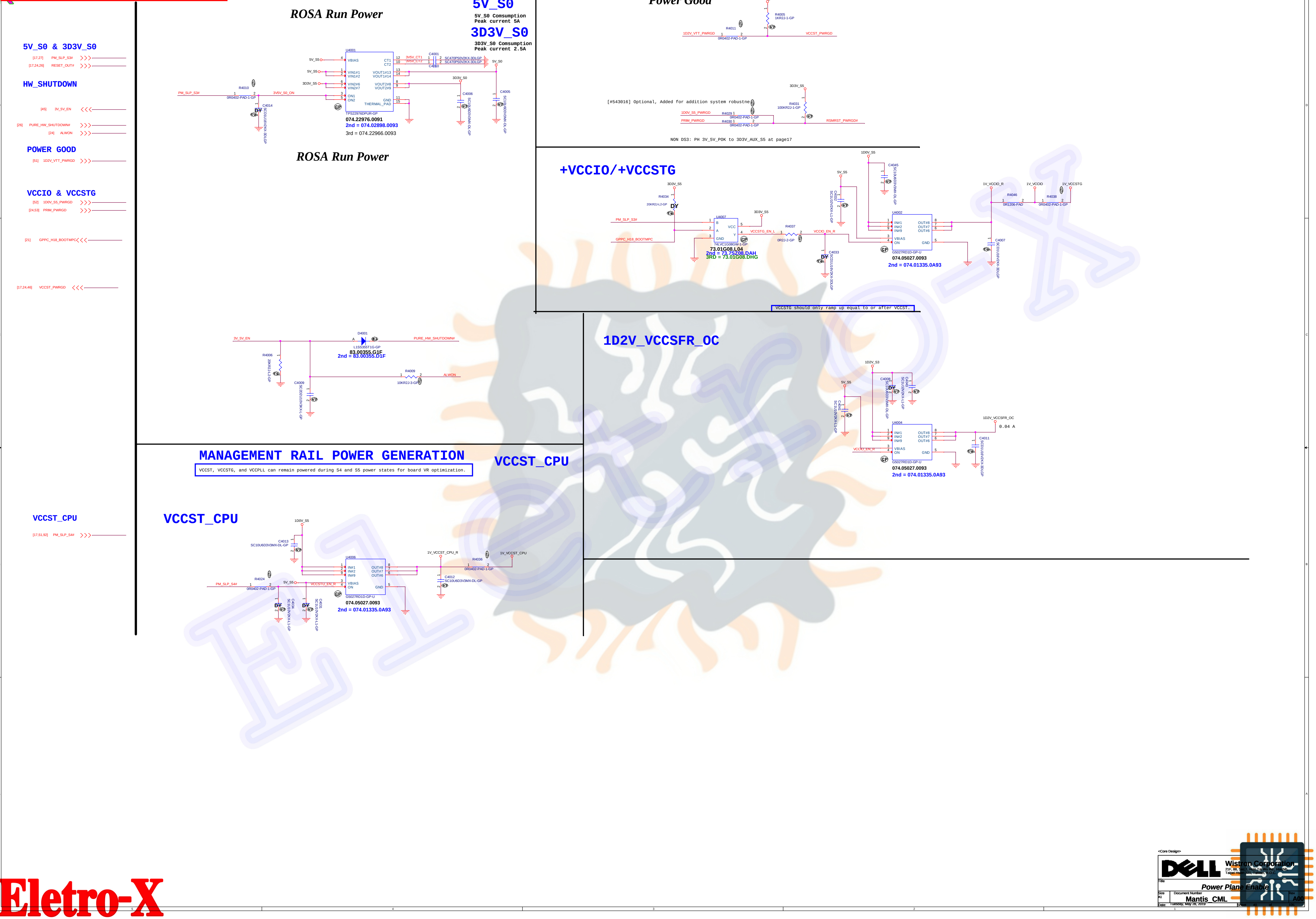
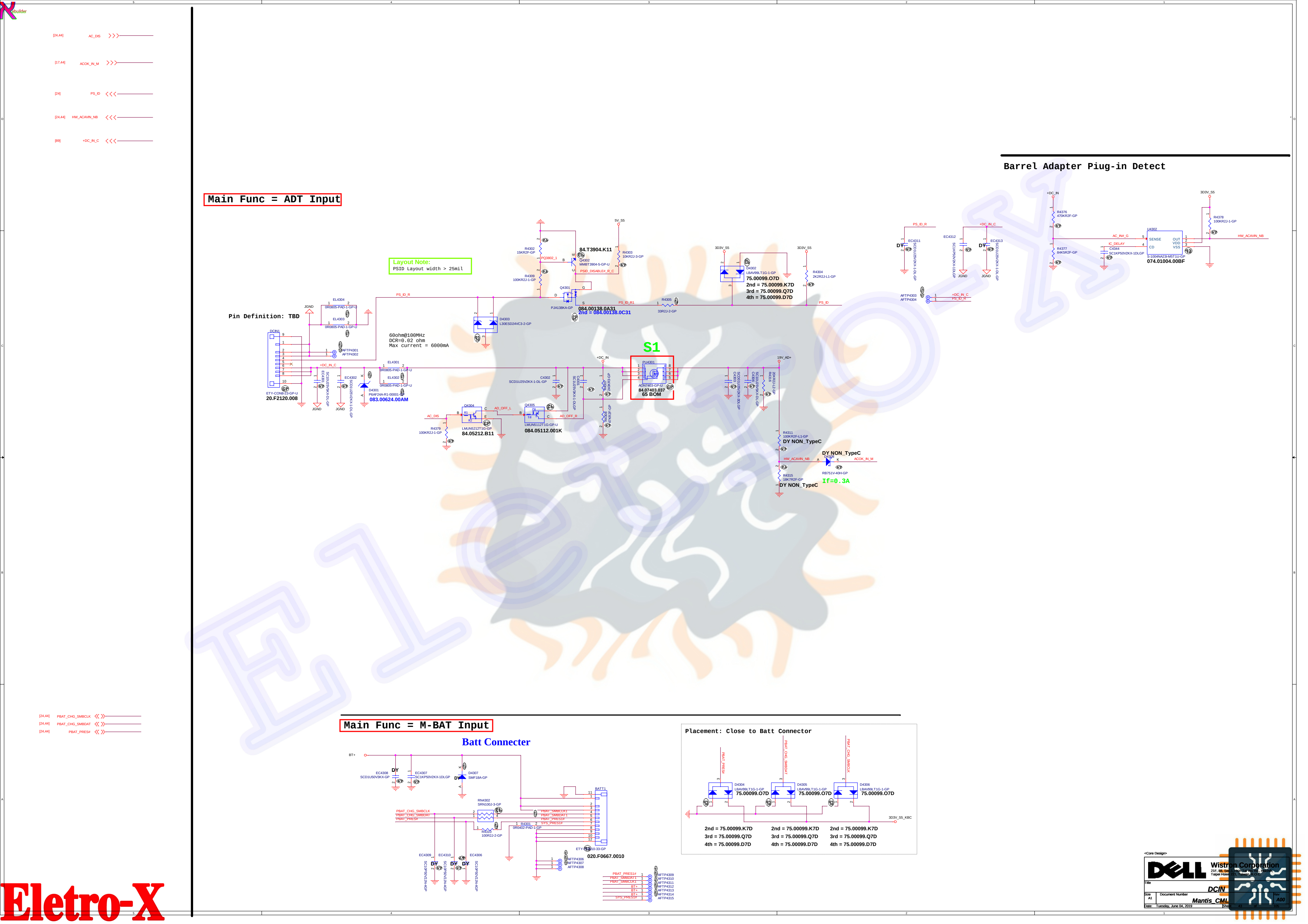
Main Func = Power Plane & Sequence





[24,44] AC_DIS
[17,44] ACOK_IN_M
[24] PS_ID
[24,44] HW_ACAVIN_NB
[89] +DC_IN_C
Main Func = ADT Input
Layout Note:
PSID Layout width > 25mil
Pin Definition: TBD
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA
84.T3904.K11
084.00138.0A31
2nd = 084.00138.0C31
75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.Q7D
4th = 75.00099.D7D
S1
84.07403.037
65 BOM
20.F2120.008
083.00624.00AM
84.05212.B11
084.05112.001K
DY NON_TypeC
If=0.3A
Barrel Adapter Piug-in Detect
074.01004.00BF
[24,44] PBAT_CHG_SMBCLK
[24,44] PBAT_CHG_SMBDAT
[24,44] PBAT_PRES#
Main Func = M-BAT Input
Batt Connecter
020.F0667.0010
Placement: Close to Batt Connector
75.00099.O7D
2nd = 75.00099.K7D
3rd = 75.00099.Q7D
4th = 75.00099.D7D
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DCIN
Mantis_CML
Date: Tuesday, June 04, 2019
Eletro-X

Main Func = Charger

OFFPAGE

EE needs check it!!

[24,43] PBAT_CHG_SMBDAT
[24,43] PBAT_CHG_SMBCLK
[24,64] HW_ACAV_IN
[17,43] ACOK_IN_M
[24,79] DGPUHOT#
[24] AD_IA
[24,43] PBAT_PRES#
[74] VCCPD_VBUS_ACK
From NXP ACK
[24,43] AC_DIS
[24,43] HW_ACAVIN_NB
[3,24,46] PROCHOT#_CPU
[66] PWR_CHG_CSOP_R
[66] PWR_CHG_CSON_R
[46] PWR_CORE_PSYS

ISL9538H For Charger

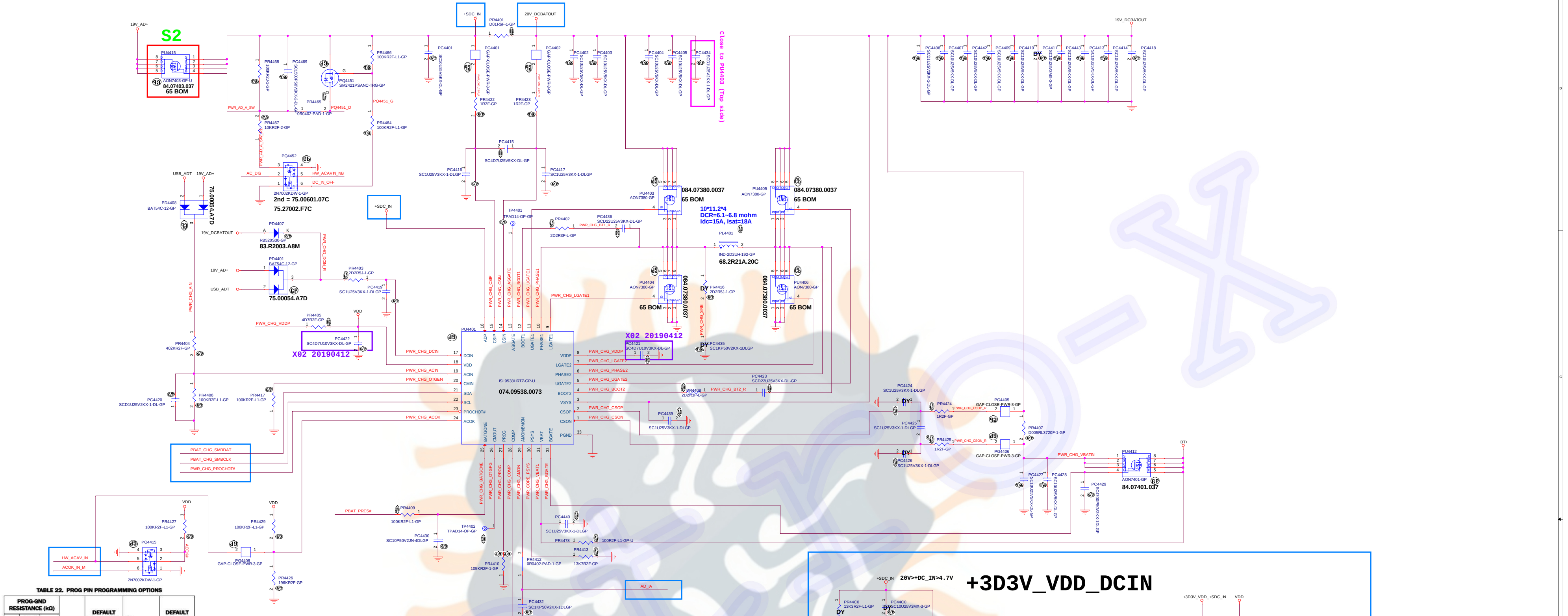
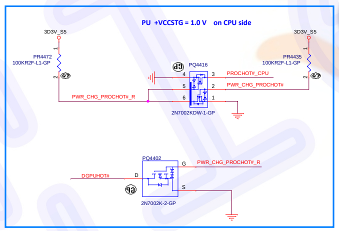


TABLE 22. PROG PIN PROGRAMMING OPTIONS

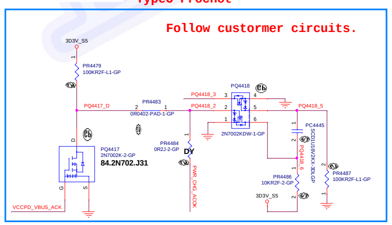
PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLimit1 Reg(A)
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

PU +VCCSTG = 1.0 V on CPU side



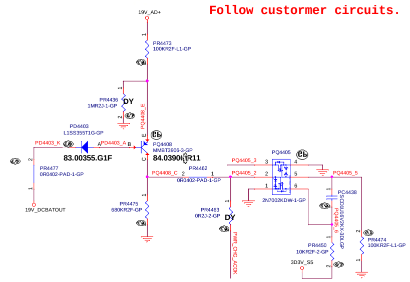
TypeC Prochot

Follow custormer circuits.



Barrel Prochot

Follow customer circuits.



+3D3V_VDD_DCIN

20V>+DC_IN>4.7V

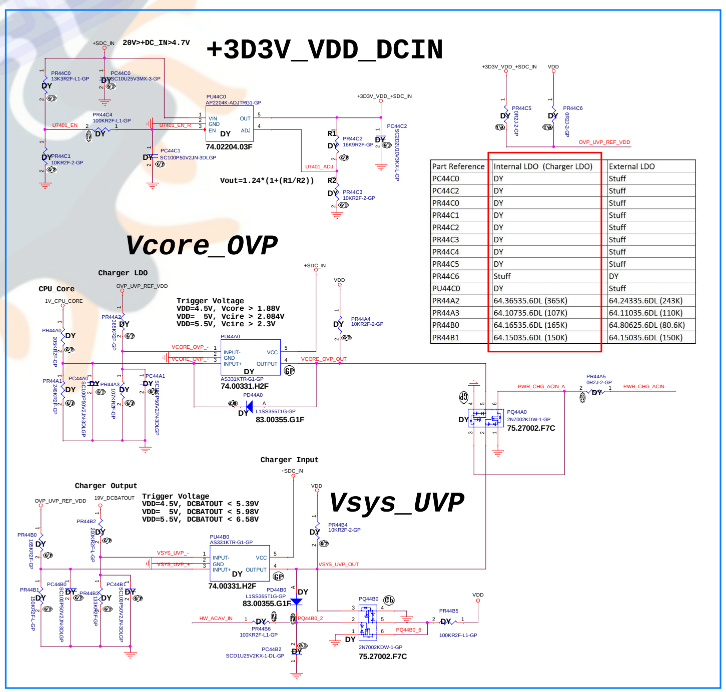
Vout=1.24*(1+(R1/R2))

Vcore_OVP

Trigger Voltage
VDD=4.5V, Vcore > 1.88V
VDD= 5V, Vcore > 2.084V
VDD=5.5V, Vcore > 2.3V

Vsys_UVP

Trigger Voltage
VDD=4.5V, DCBATOUT < 5.39V
VDD= 5V, DCBATOUT < 5.98V
VDD=5.5V, DCBATOUT < 6.58V



Part Reference	Internal LDO (Charger LDO)	External LDO
PC44C0	DY	Stuff
PC44C2	DY	Stuff
PR44C0	DY	Stuff
PR44C1	DY	Stuff
PR44C2	DY	Stuff
PR44C3	DY	Stuff
PR44C4	DY	Stuff
PR44C5	DY	Stuff
PR44C6	Stuff	DY
PU44C0	DY	Stuff
PR44A2	64.36535.6DL (365K)	64.24335.6DL (243K)
PR44A3	64.10735.6DL (107K)	64.11035.6DL (110K)
PR44B0	64.16535.6DL (165K)	64.80625.6DL (80.6K)
PR44B1	64.15035.6DL (150K)	64.15035.6DL (150K)

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Power (Charger_ISL9538)
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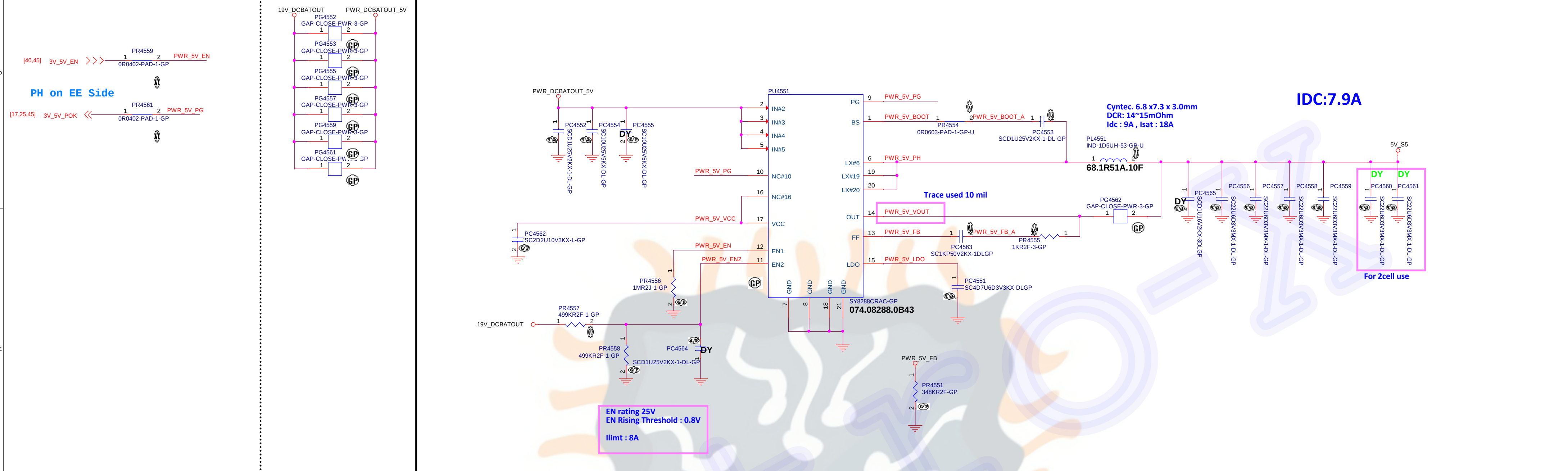
Tuesday, June 04, 2019

SSID = PWR.Plane.Regulator_5V

SY8288C For 5V

OFFPAGE-Signal

OFFPAGE-GAP

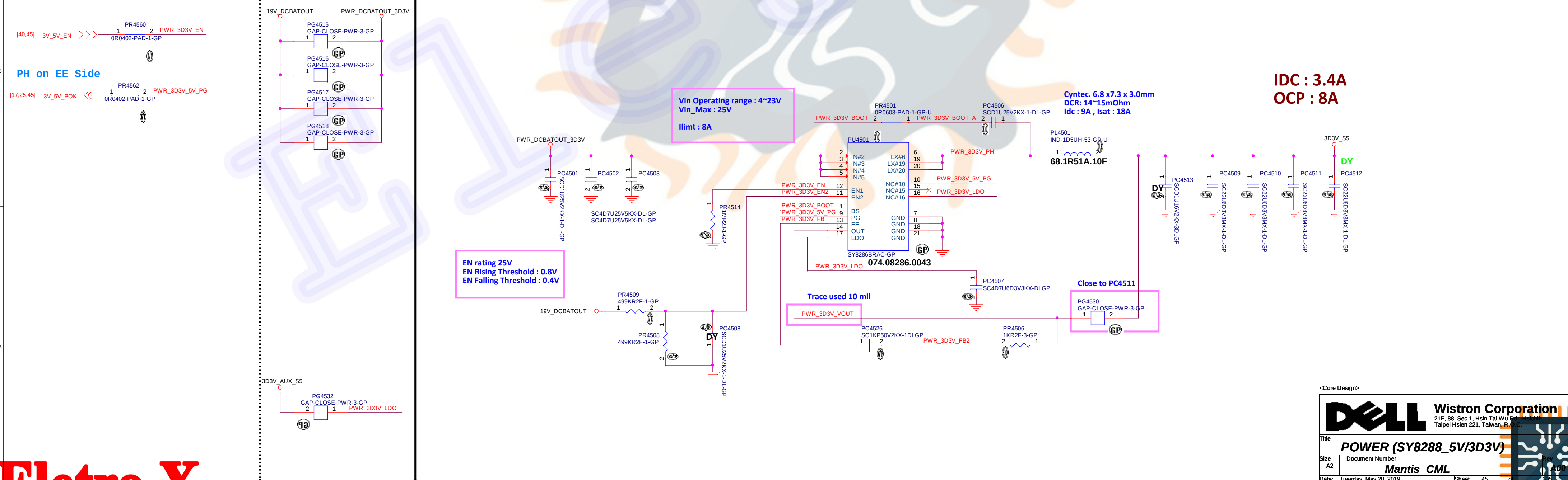


SSID = PWR.Plane.Regulator_3D3V

SY8286B For 3D3V

OFFPAGE-Signal

OFFPAGE-GAP



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Title	POWER (SY8288_5V/3D3V)
Size	A2
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Main Func = CPU_CORE

OFFPAGE

PH on CPU side

[3,24,44] PROCHOT#_CPU
[7] SVID_ALERT#_CPU
[7] SVID_CLK_CPU
[7] SVID_DATA_CPU
[44] PWR_CORE_PSYS
[17,24,40] VCCST_PWRGD

For VCCGT Sense

[8] VSSGT_SENSE
[8] VCCGT_SENSE

For Vcore Sense

[7] VCCCORE_SENSE
[7] VSSCORE_SENSE

For Vccsa Sense

[8] VSSSA_SENSE
[8] VCCSA_SENSE

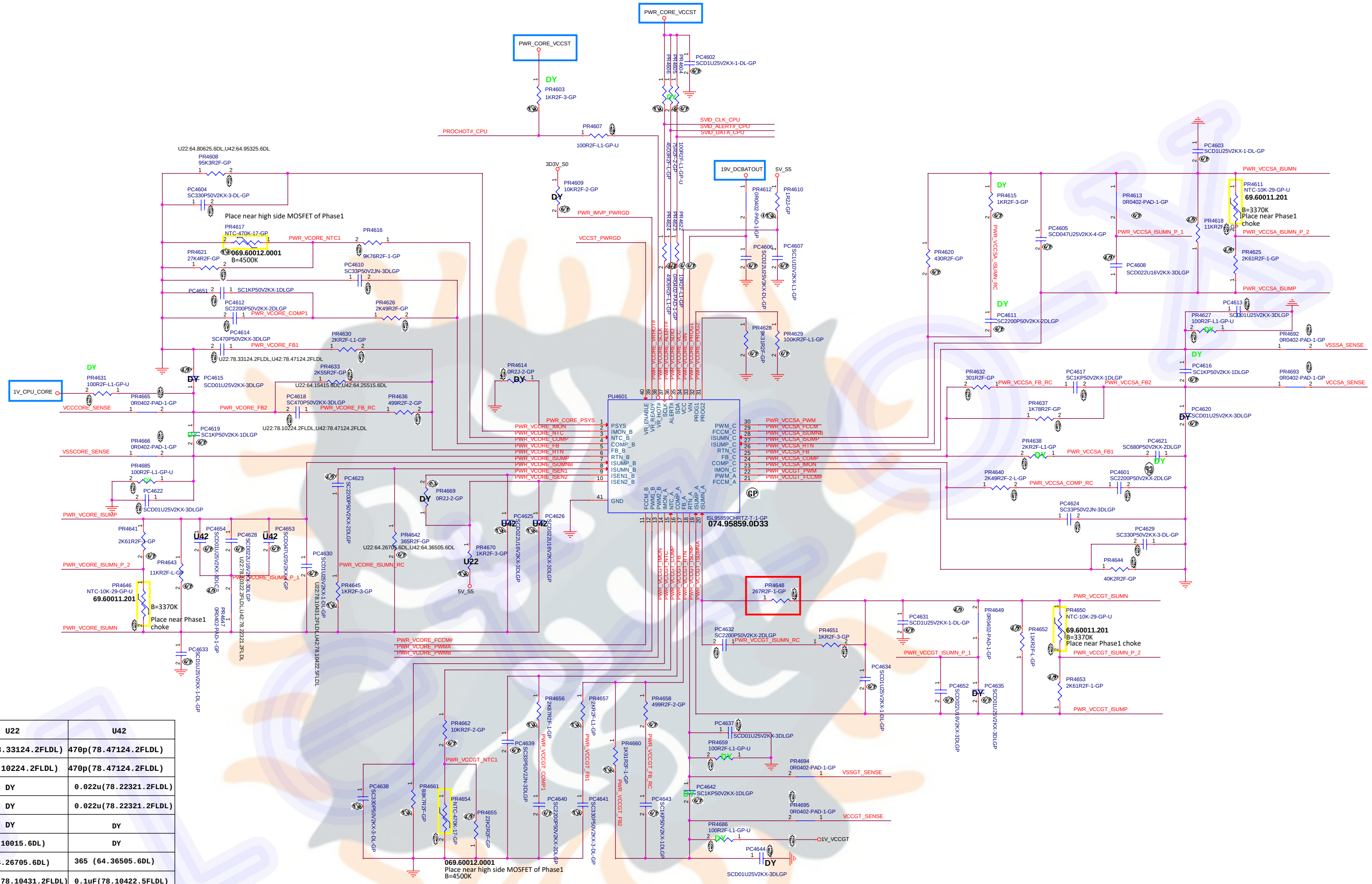
EE side Link
SVID Pull High V

1V_VCCST_CPU
PG4601
GAP-CLOSE-PWR-3-GP
PWR_CORE_VCCST

[47] PWR_VCORE_PWMB
[47] PWR_VCORE_ISUMN
[47] PWR_VCORE_ISUMP
[47] PWR_VCORE_FCCM#
[47] PWR_VCORE_PWMA
[48] PWR_VCCGT_PWM
[48] PWR_VCCGT_FCCM#
[48] PWR_VCCGT_ISUMN
[48] PWR_VCCGT_ISUMP
[50] PWR_VCCSA_ISUMP
[50] PWR_VCCSA_ISUMN
[50] PWR_VCCSA_PWM
[50] PWR_VCCSA_FCCM

[47] PWR_VCORE_ISEN1
[47] PWR_VCORE_ISEN2

ISL95859C For CPUCORE



	U22	U42
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)
PC4625	DY	0.022u(78.22321.2FLDL)
PC4626	DY	0.022u(78.22321.2FLDL)
PR4669	DY	DY
PR4670	1K(64.10015.6DL)	DY
PR4642	267(64.26705.6DL)	365 (64.36505.6DL)
PC4630	0.1uF(78.10431.2FLDL)	0.1uF(78.10422.5FLDL)
PC4628	0.01uF(78.10322.2FLDL)	22nF(78.22321.2FLDL)
PC4654	DY	0.01u(78.10322.2FLDL)
PC4653	DY	47nF(078.47322.02FD)
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)
PR4608	80.6K(64.80625.6DL)	95.3K (64.95325.6DL)

A00 20190530

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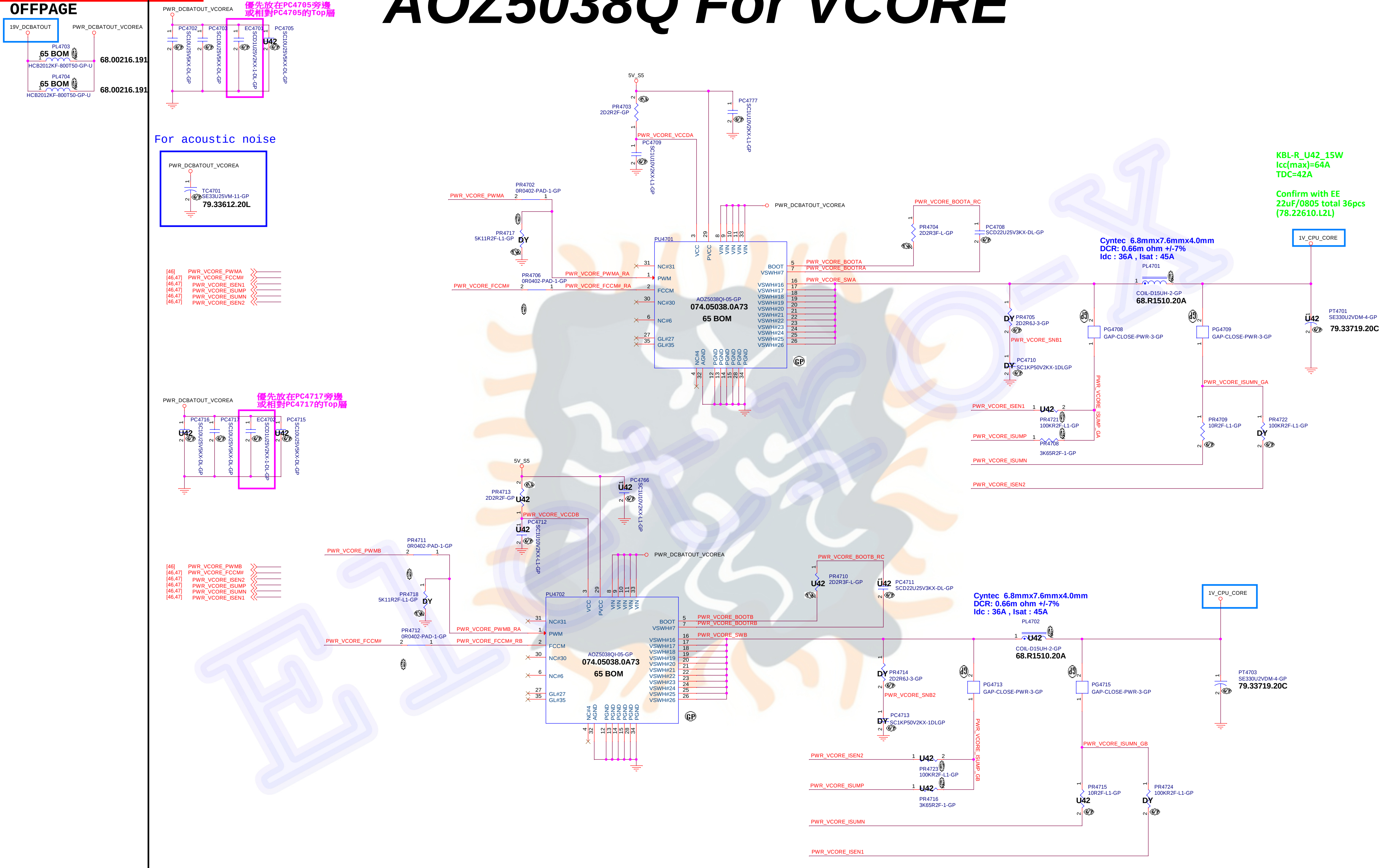
Title: POWER (95859_CPUCORE(1/3))

Size: A1 | Document Number: Mantis_CML | Rev: A00

Date: Monday, June 03, 2019 | Sheet 46 of 105

Main Func = CPU_CORE

AOZ5038Q For VCORE



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Title: POWER (5038_CPU_VCORE(2/3))

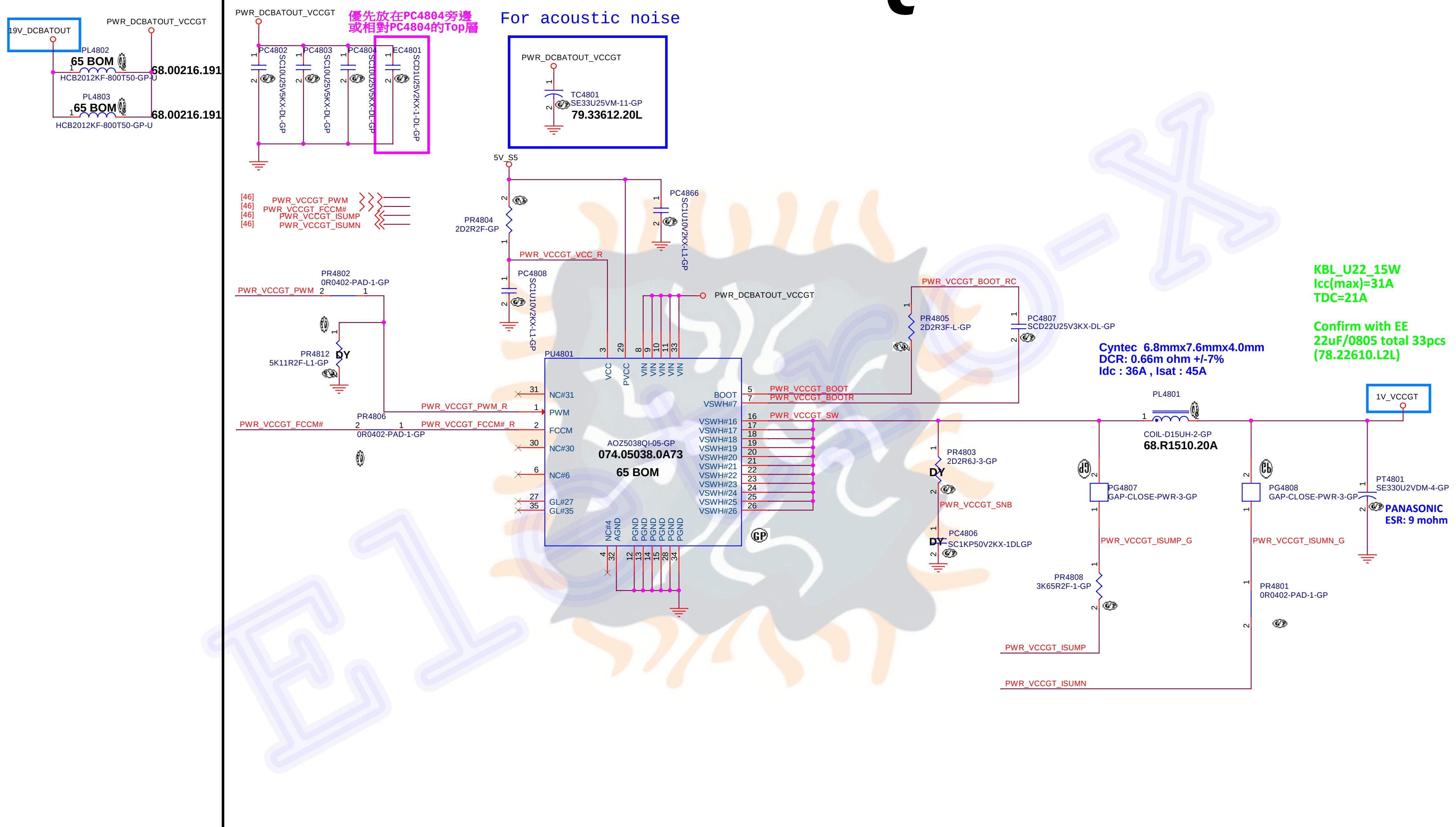
Size: A2 | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, June 04, 2019 | Sheet 47

Main Func = CPU_CORE

Offpage-Signal

AOZ5038Q For VCCGT



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Taipei Hsien 221, Taiwan, R.O.C.

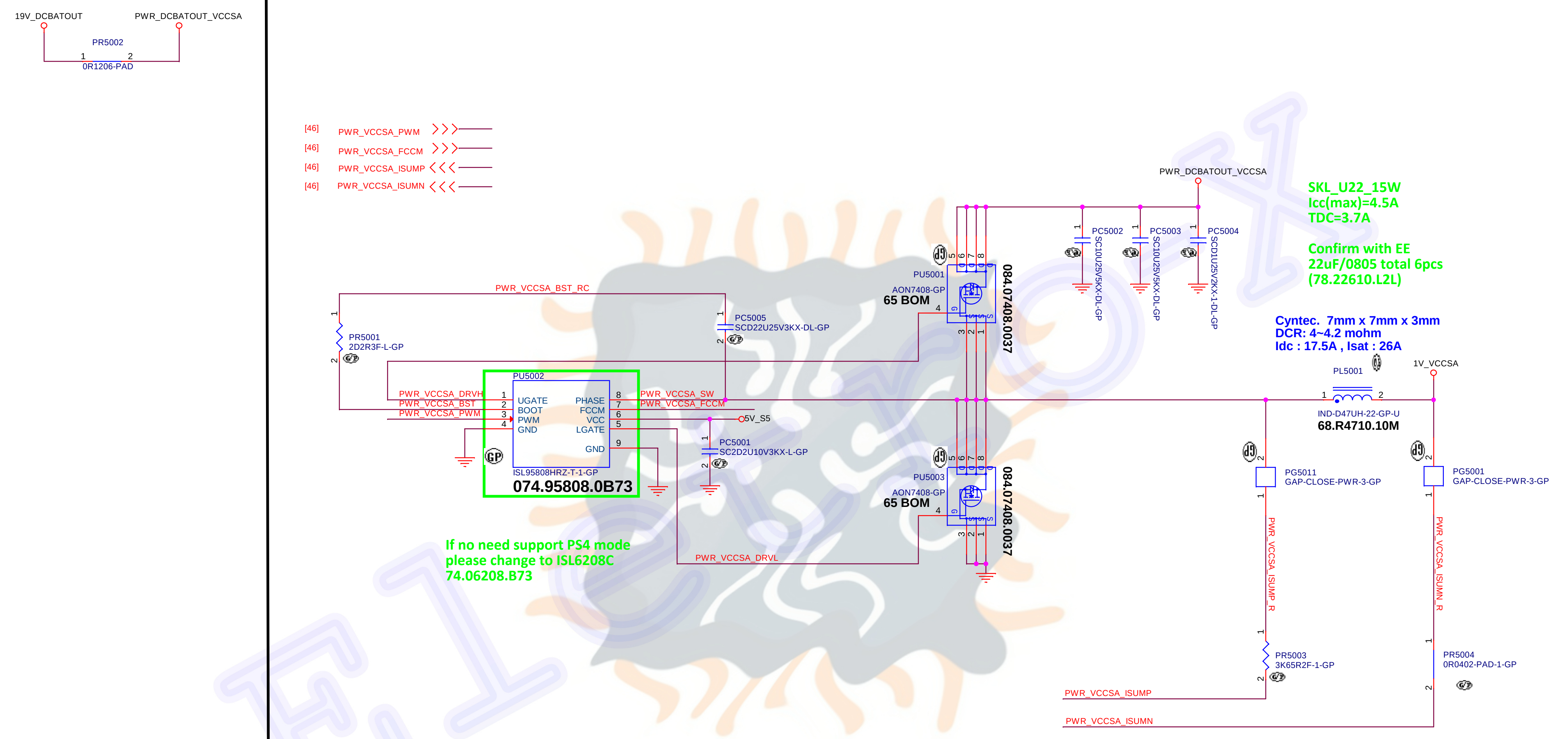
Title: POWER (5038_CPU_VCORE(3/3))

Size: A3 | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, June 04, 2019 | Sheet 48 of 105

Main Func = CPU_CORE

ISL95808 For VCCSA



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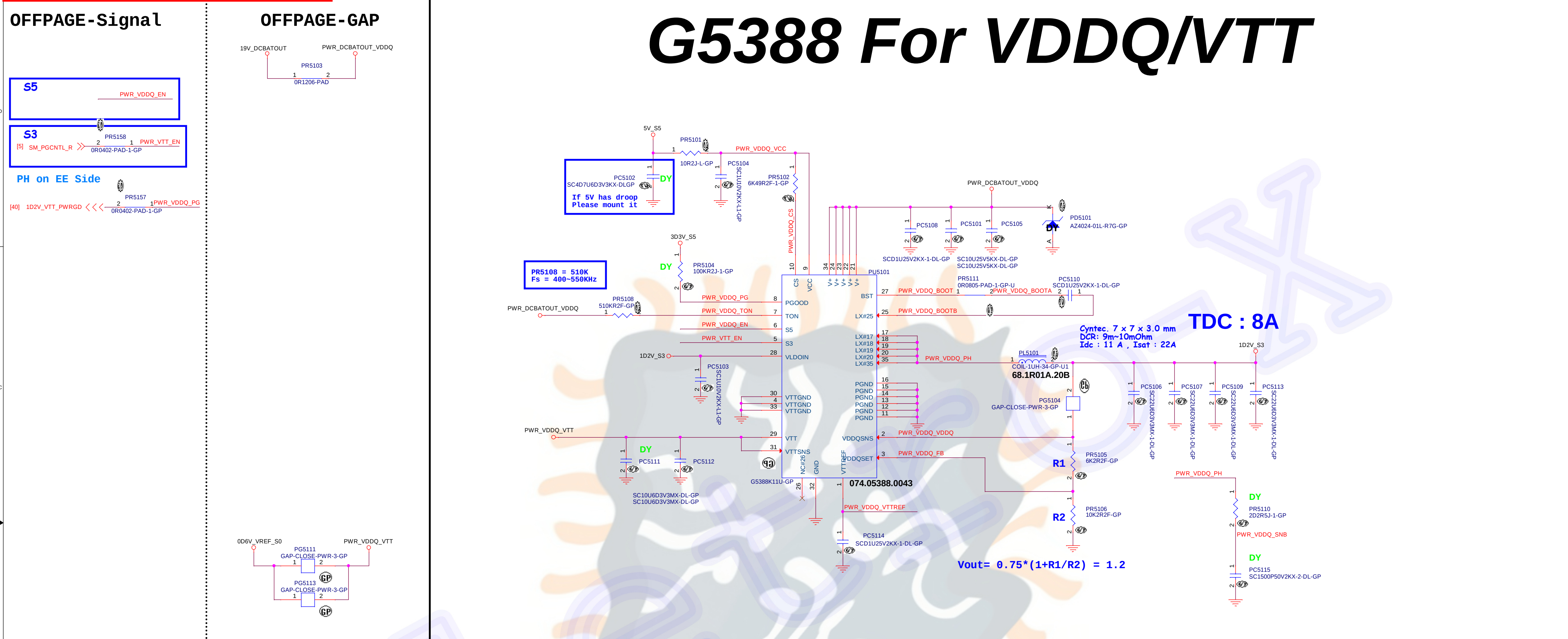
Title: POWER (ISL95808_VCCSA)

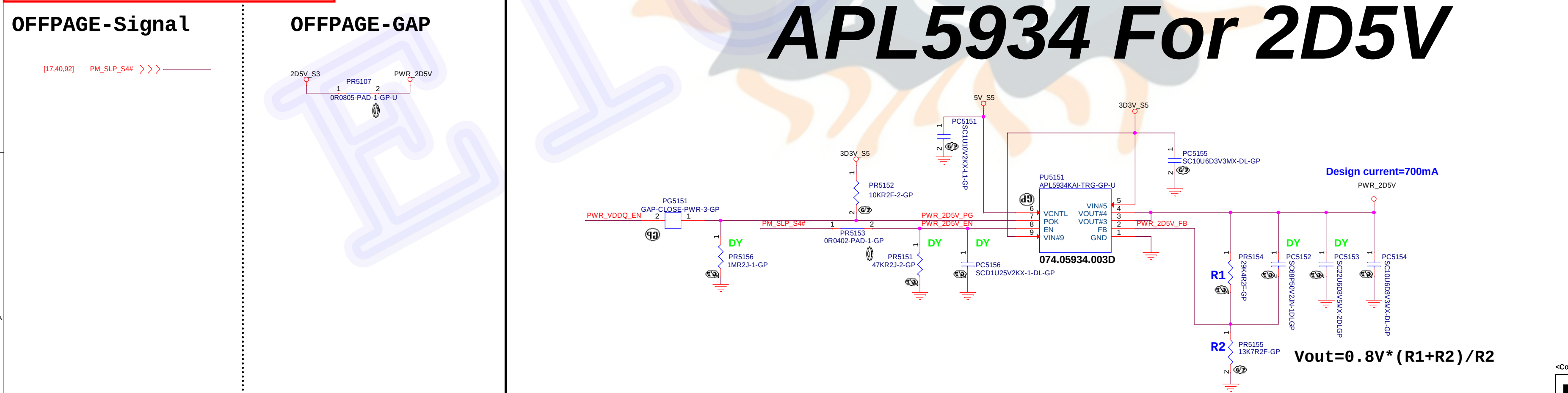
Size: A3 | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, June 04, 2019 | Sheet 50 of 105

SSID = PWR.Plane.Regulator_1D2V/0D6V



SSID = PWR.Plane.Regulator_2D5V



<Core Design>

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Title	Power (G5388_VDDQ_VTT_VPP)
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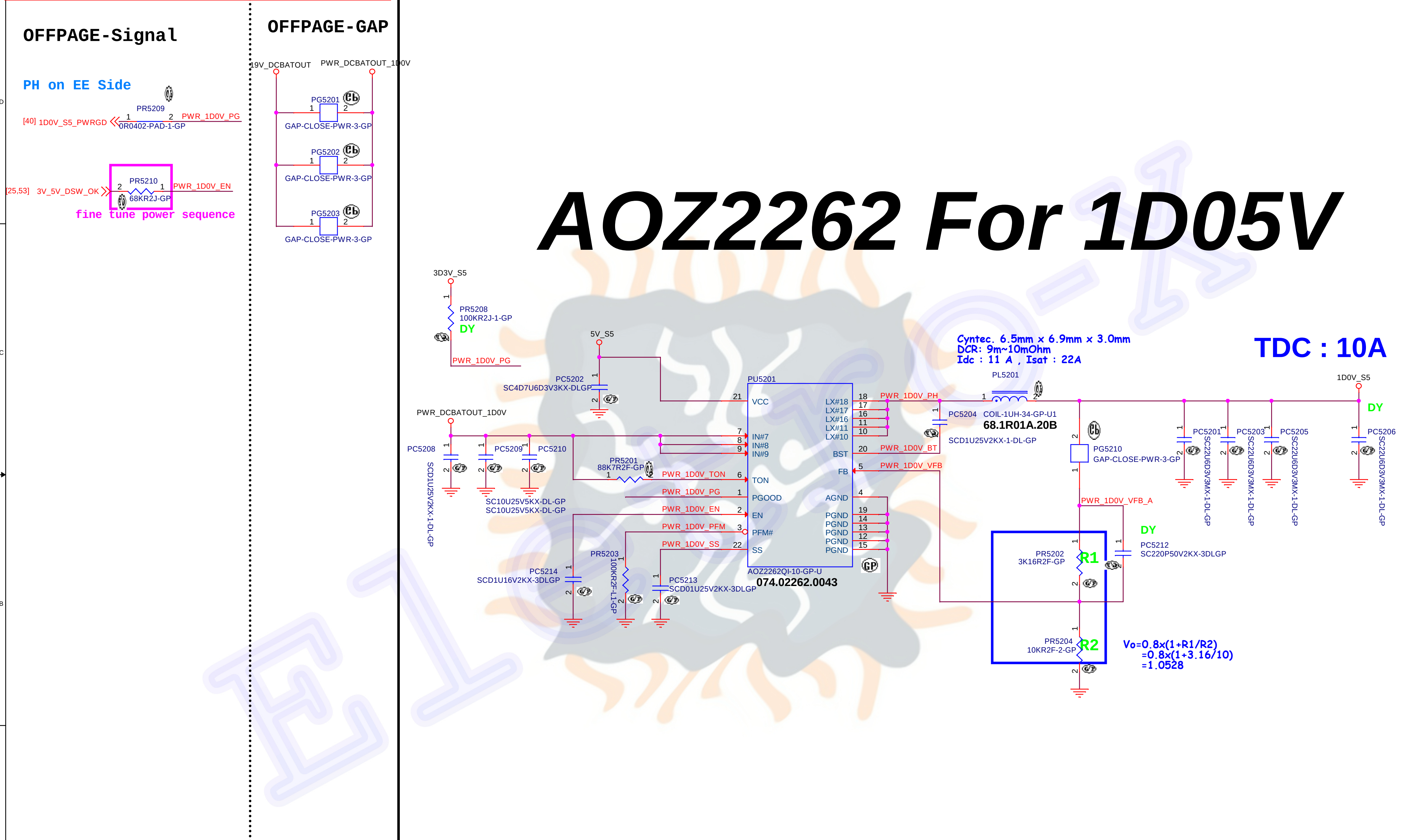
Eletro-X

SSID = PWR.Plane.Regulator_1D0V



<Core Design>

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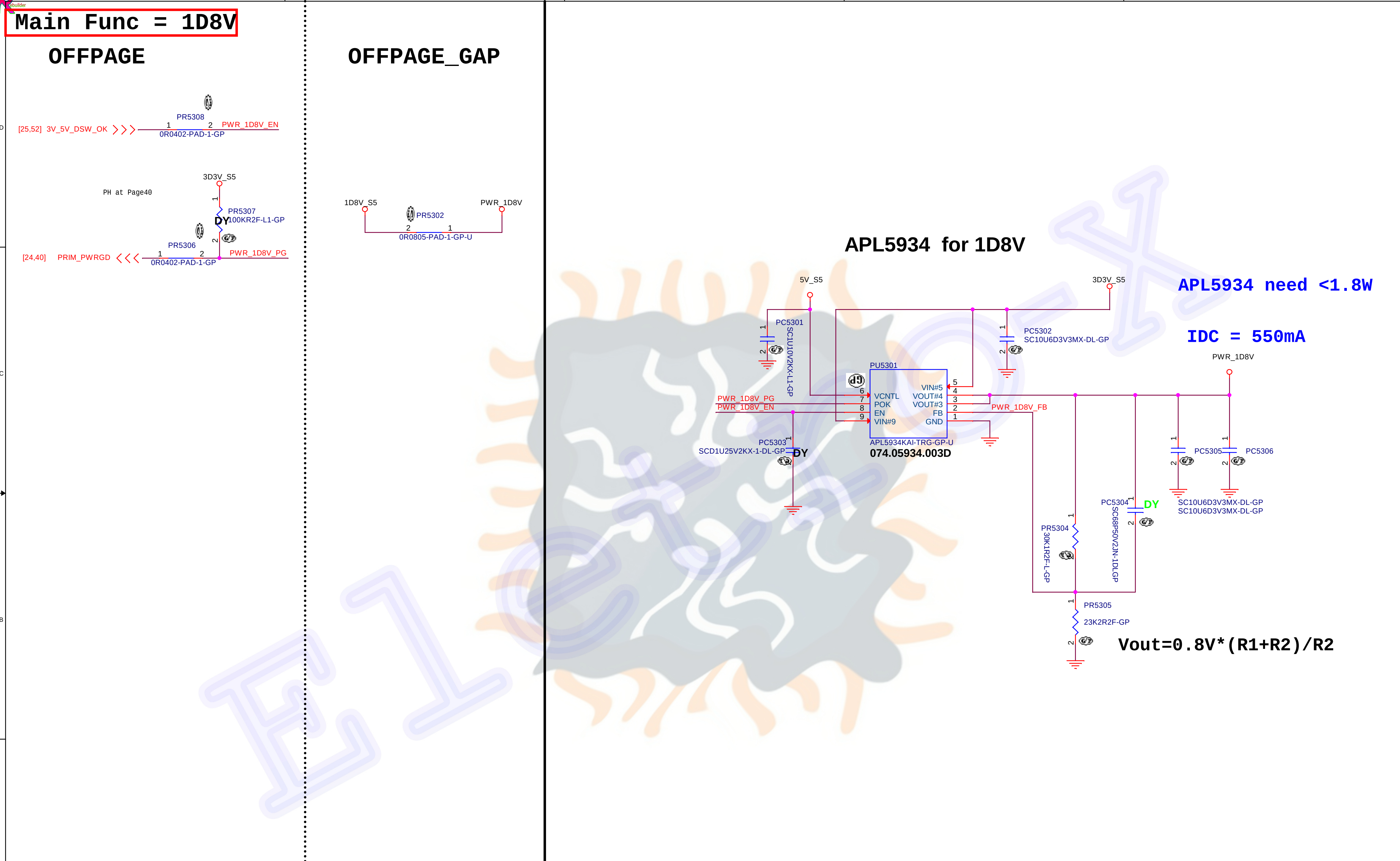
Title	POWER (AOZ2262Q_1D0V)
Size A3	Document Number: Mantis_CML
Date: Tuesday, May 28, 2019	Sheet 52 of 105

Eletro-X



<Core Design>

DELL

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Title: **POWER (APL5934_1D8V)**

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A3	Mantis_CML	A00

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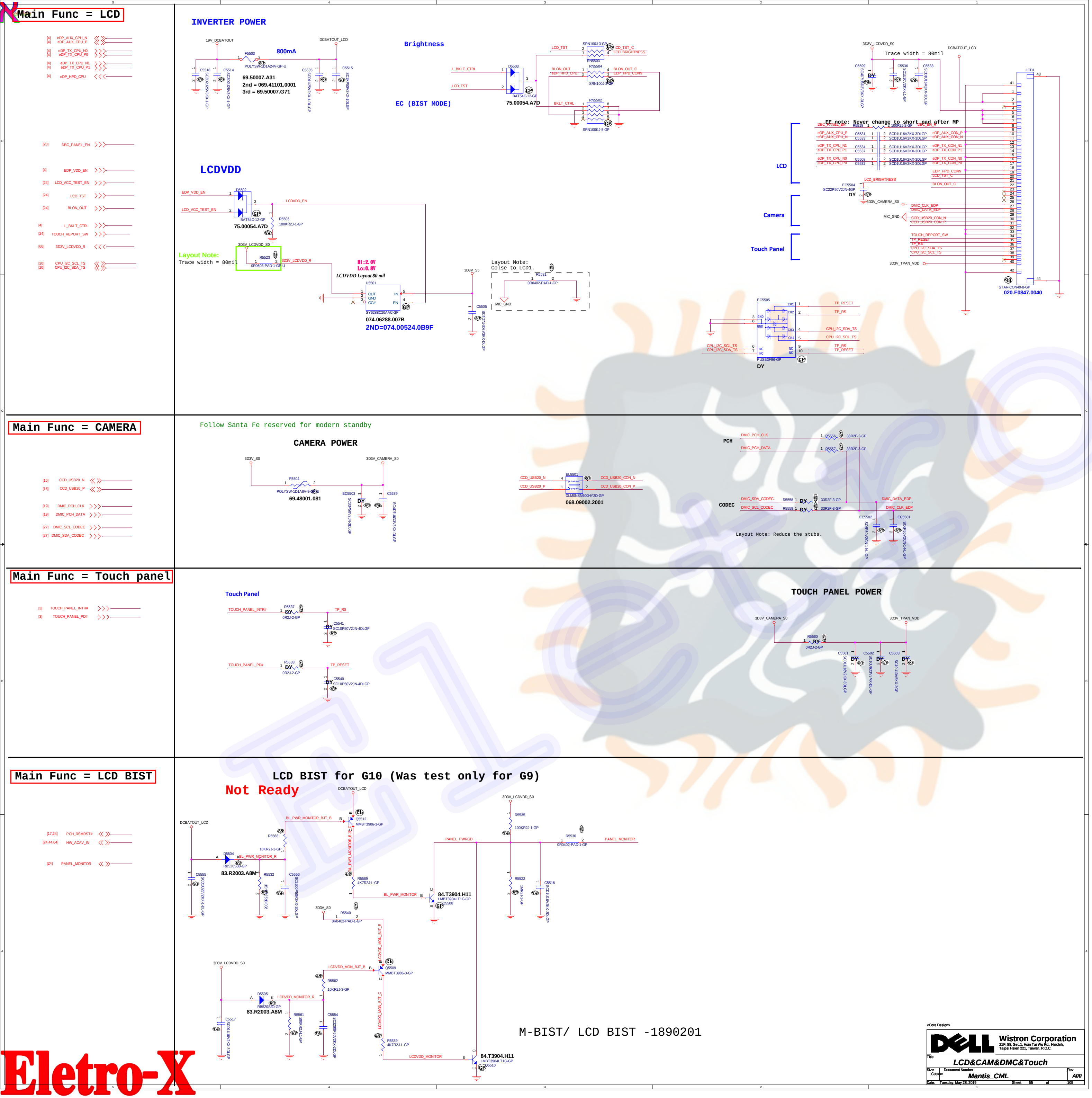
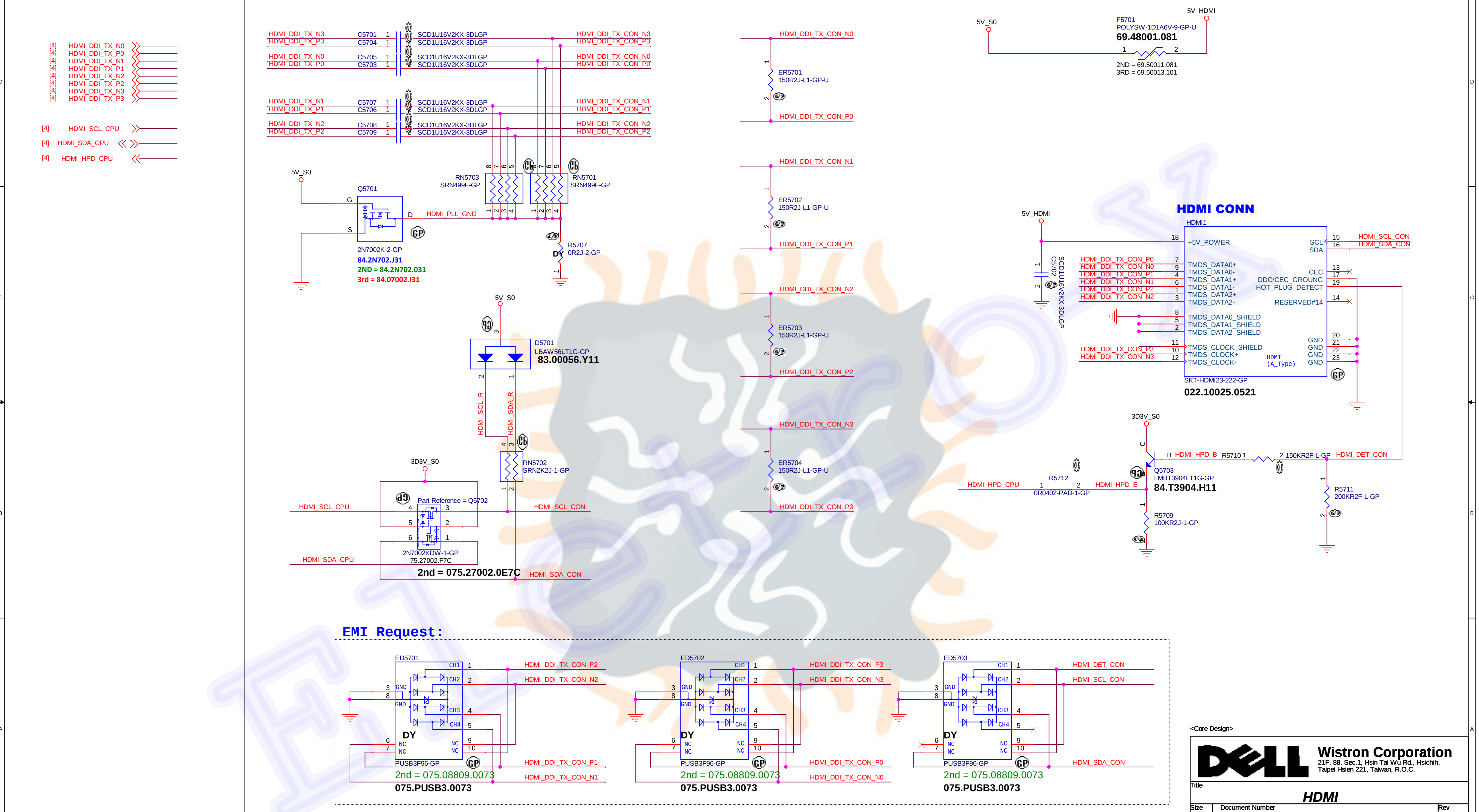

Main Func = LCD
INVERTER POWER
800mA
69.50007.A31
2nd = 069.41101.0001
3rd = 69.50007.G71
Brightness
EC (BIST MODE)
75.00054.A7D
LCDVDD
Layout Note:
Trace width = 80mil
LCDVDD Layout 80 mil
Hi:2.0V
Lo:0.8V
074.06288.007B
2ND=074.00524.0B9F
Layout Note:
Colse to LCD1.
Trace width = 80mil
EE note: Never change to short pad after MP
LCD
Camera
Touch Panel
020.F0847.0040
Main Func = CAMERA
Follow Santa Fe reserved for modern standby
CAMERA POWER
69.48001.081
068.09002.2001
PCH
CODEC
Layout Note: Reduce the stubs.
Main Func = Touch panel
Touch Panel
TOUCH PANEL POWER
Main Func = LCD BIST
LCD BIST for G10 (Was test only for G9)
Not Ready
83.R2003.A8M
84.T3904.H11
M-BIST/ LCD BIST -1890201
Wistron Corporation
LCD&CAM&DMC&Touch
Mantis_CML
A00
Eletro-X

SSID = HDMI Level Shifter/Connector



<Core Design>

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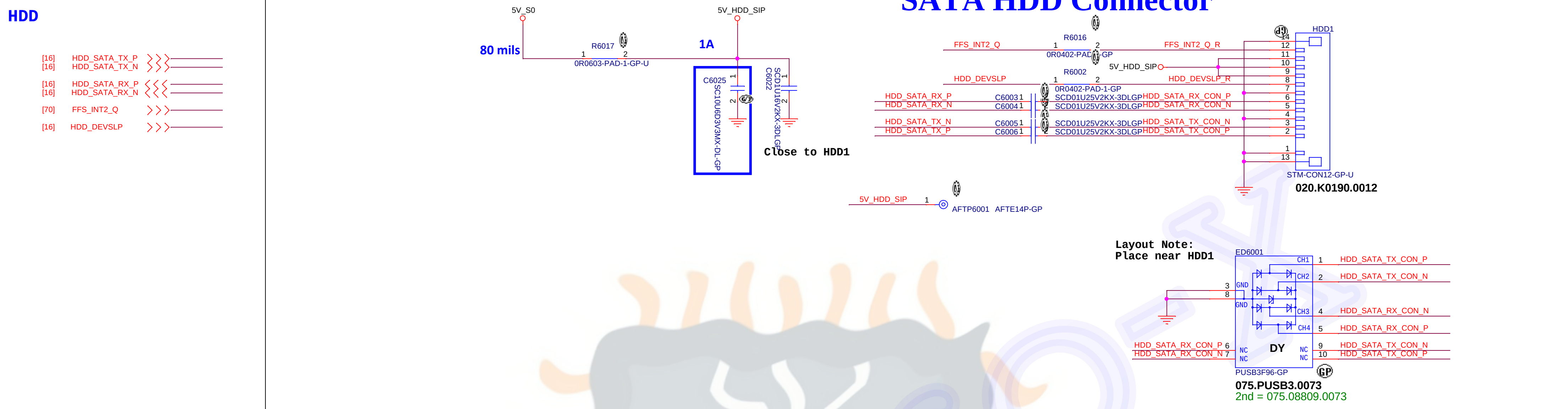
Title	HDMI	
Size: Custom	Document Number: Mantis_CML	Rev: A00
Date: Tuesday, May 28, 2019	Sheet 57 of 105	

Eletro-X

Main Func = HDD



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Title	SATA IF_HDD/ODD	
Size: Custom	Document Number: Mantis_CML	Rev: A00
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Eletro-X

Main Func = WLAN

PCIE

[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P

PCIE_CLK

[18] WLAN_CLK_CPU_N
[18] WLAN_CLK_CPU_P
[18,61] WLAN_CLKREQ_CPU_N

USB2.0

[16] BT_USB20_P
[16] BT_USB20_N

Single end

[21] BLUETOOTH_EN
[21] WIFI_RF_EN
[17,63,66,76,91] PLT_RST#
[18,24] SUS_CLK

Power EN (Madesimo)

[19] BT_PCMOUT_CLKREQ0
[19] BT_PCMFRM_CRF_RST_N

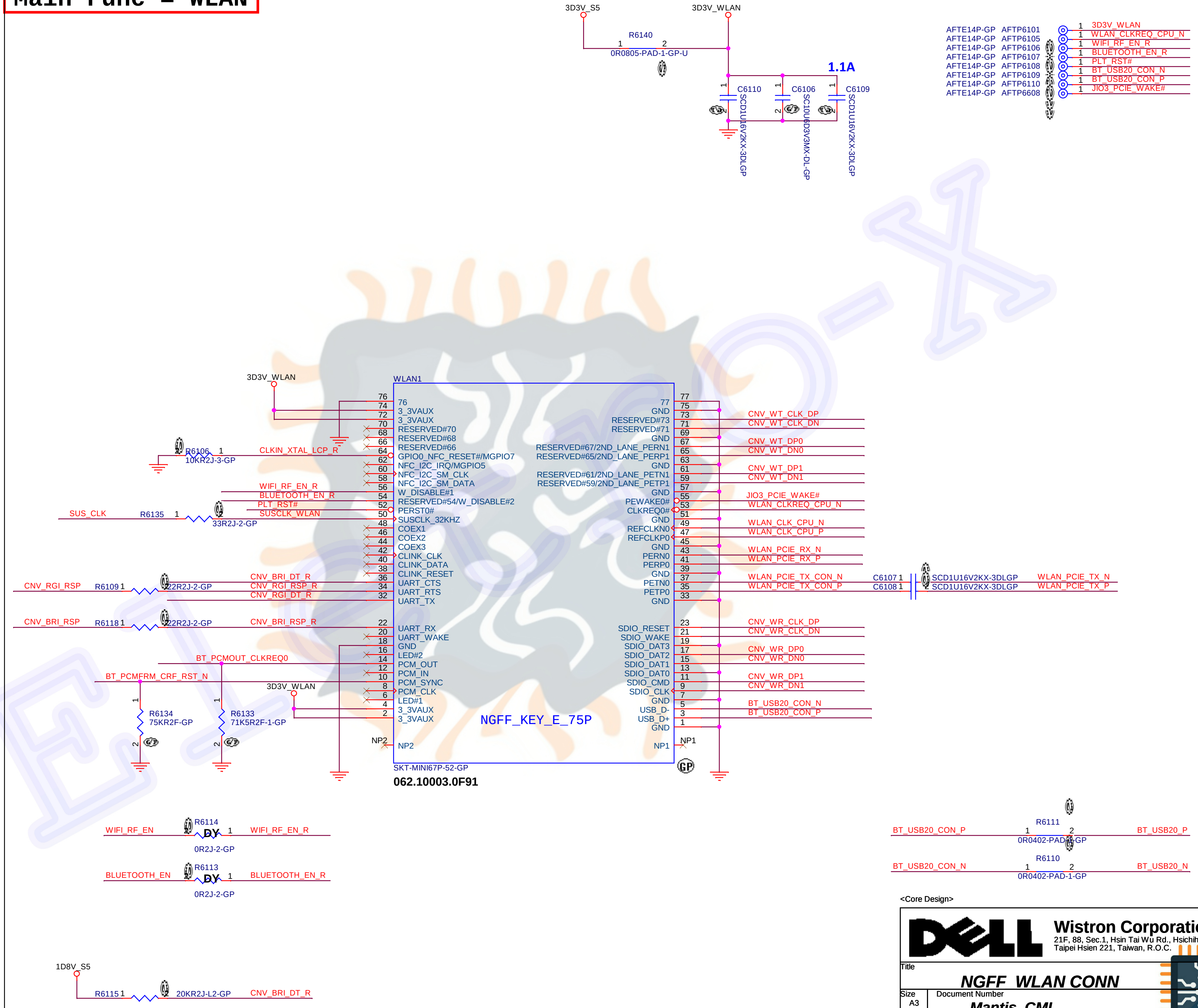
[21] CNV_WT_DN0
[21] CNV_WT_DP0
[21] CNV_WT_DN1
[21] CNV_WT_DP1
[21] CNV_WT_CLK_DN
[21] CNV_WT_CLK_DP

[21] CNV_WR_DN0
[21] CNV_WR_DP0
[21] CNV_WR_DN1
[21] CNV_WR_DP1
[21] CNV_WR_CLK_DN
[21] CNV_WR_CLK_DP

[15,20] CNV_RGI_DT_R
[20] CNV_BRI_DT_R

[20] CNV_BRI_RSP
[20] CNV_RGI_RSP

[18] JIO3_PCIE_WAKE#
[18] CLKIN_XTAL_LCP_R



<Core Design>

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Title	NGFF_WLAN CONN
Size	A3
Document Number	Mantis_CML
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Date	Monday, June 03, 2019
Sheet	61 of 105

Main Func = M.2 SSD

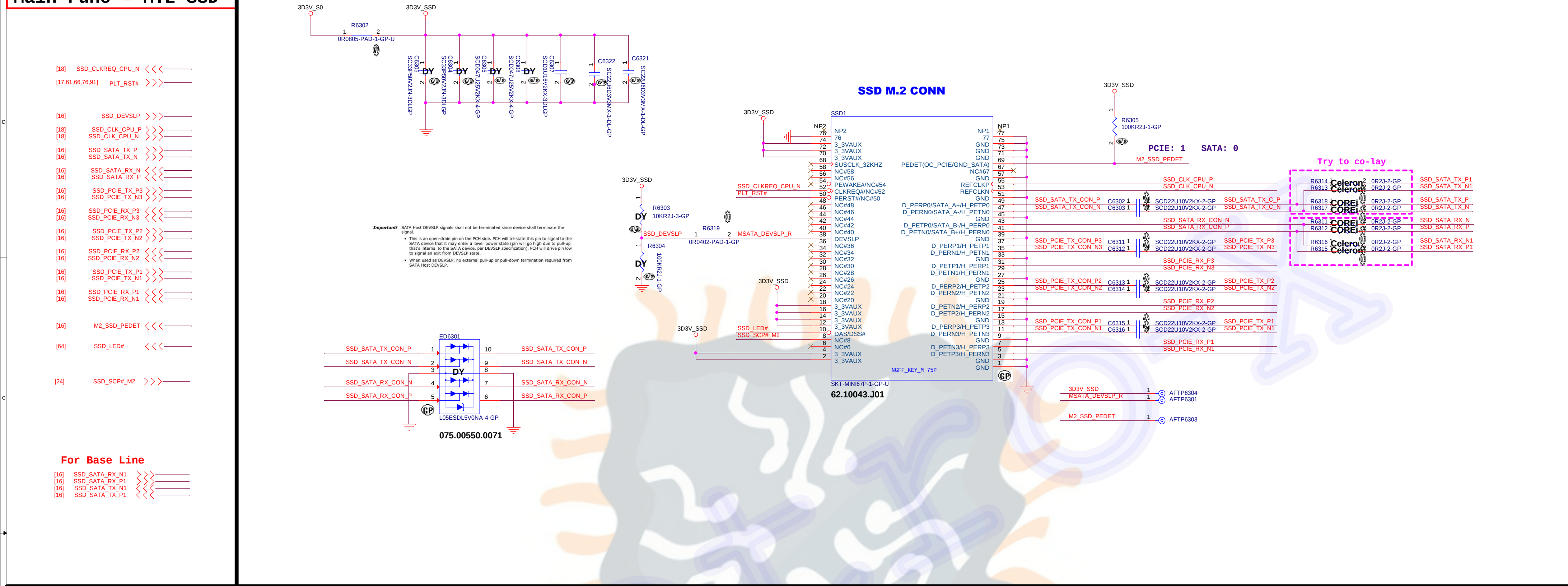

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

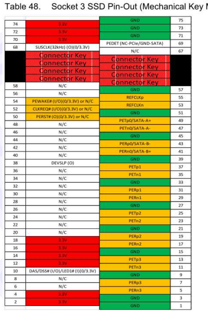

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title	mSATA
Size A2	Document Number: Mantis_CML
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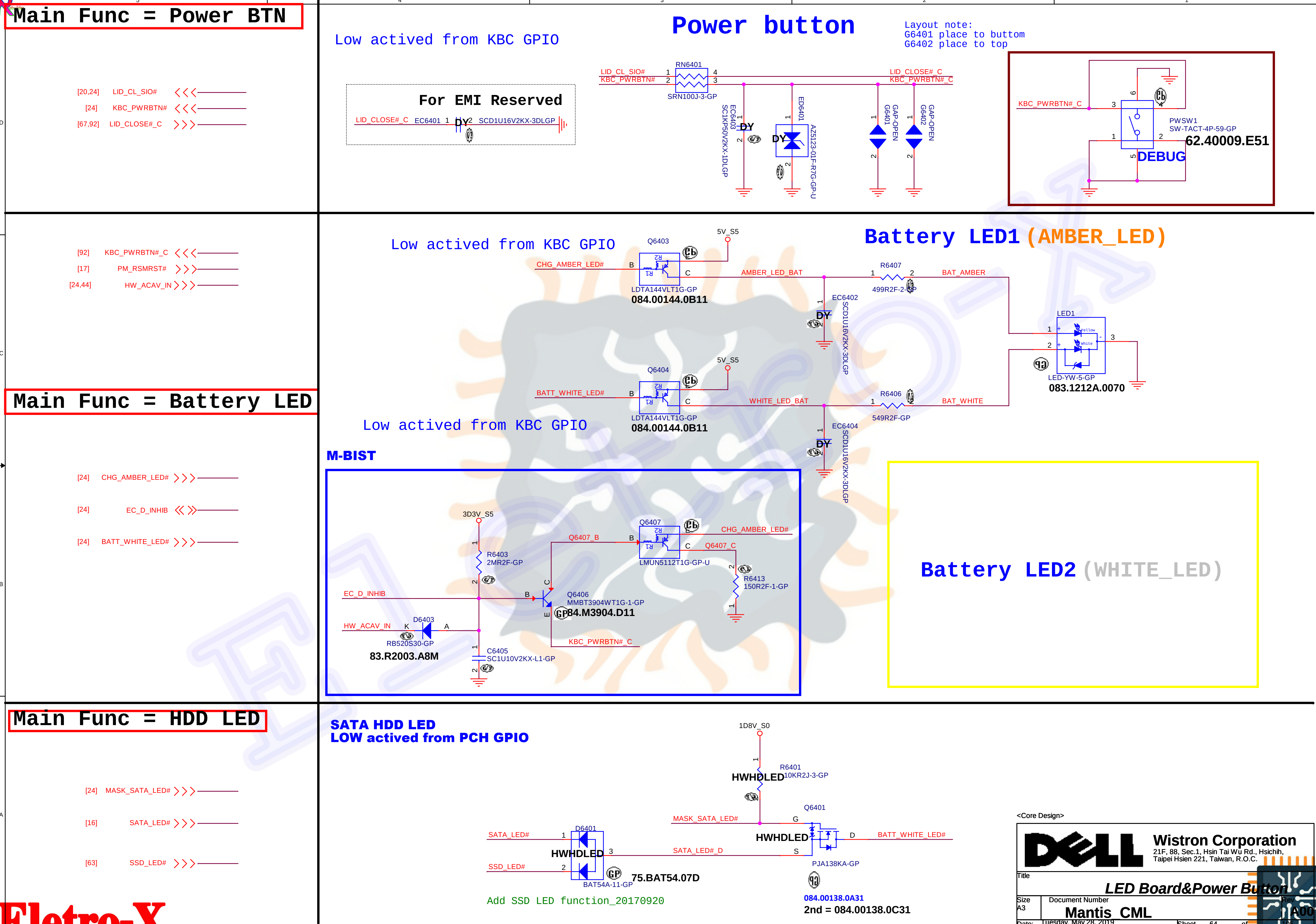

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Title: LED Board&Power Button

Size: A3 | Document Number: Mantis_CML | Rev: A00

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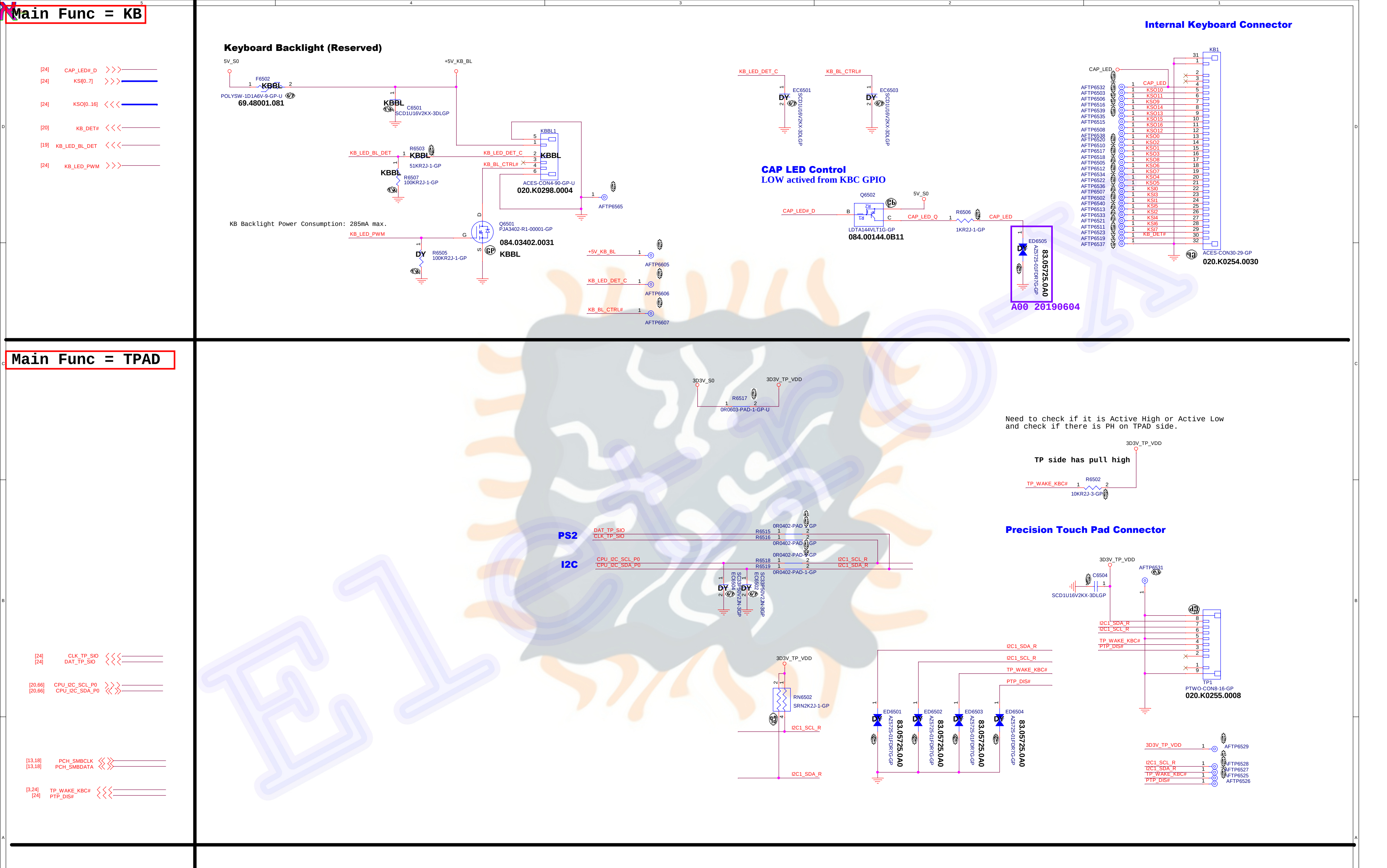

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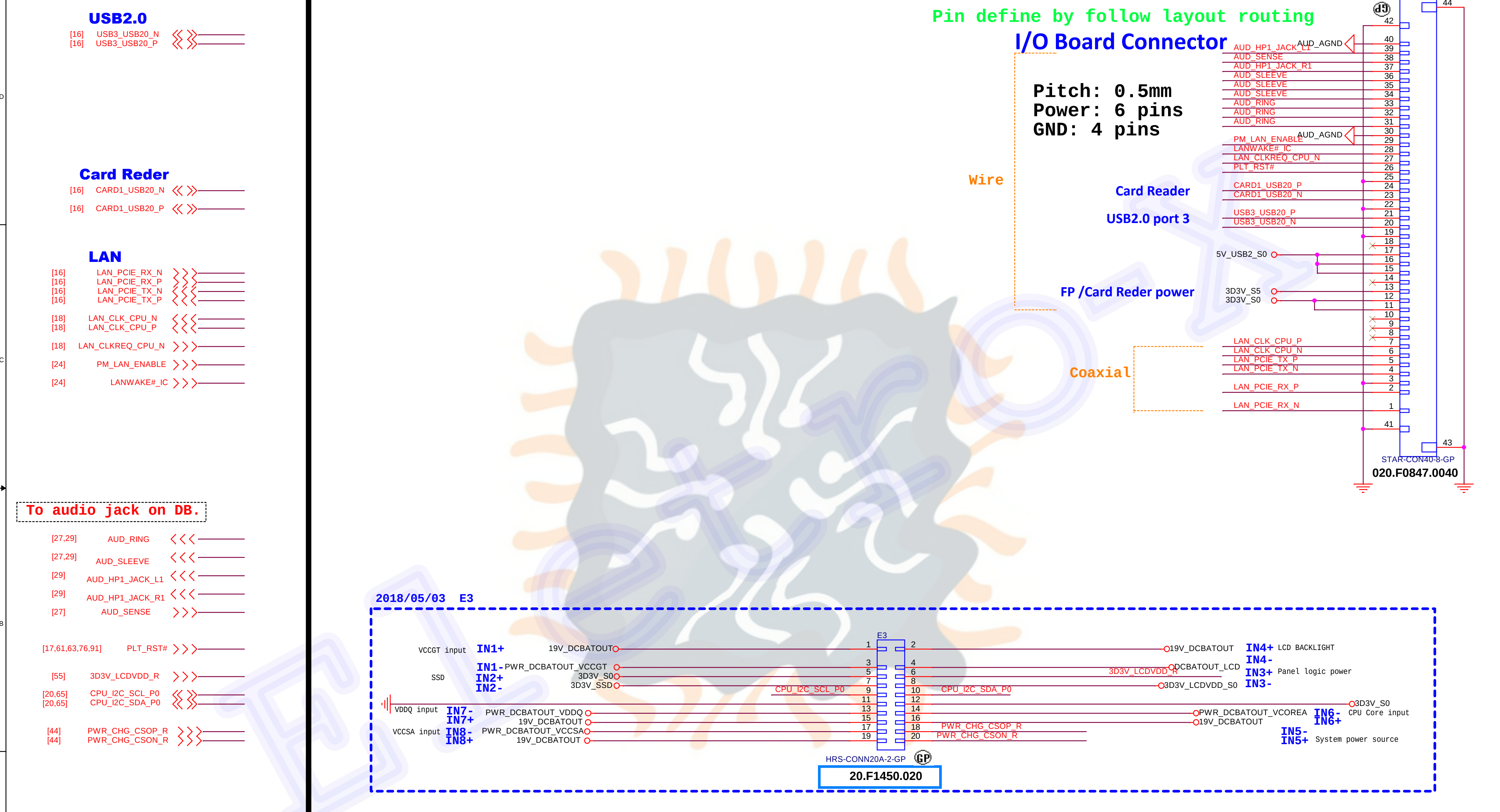
Title: Key Board&Touch Pad

Size: A2 | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, June 04, 2019 | Sheet 65

Main Func = IO Connector



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Title: IO Board Connector

Size: A3 | Document Number: Mantis_CML | Rev: A00

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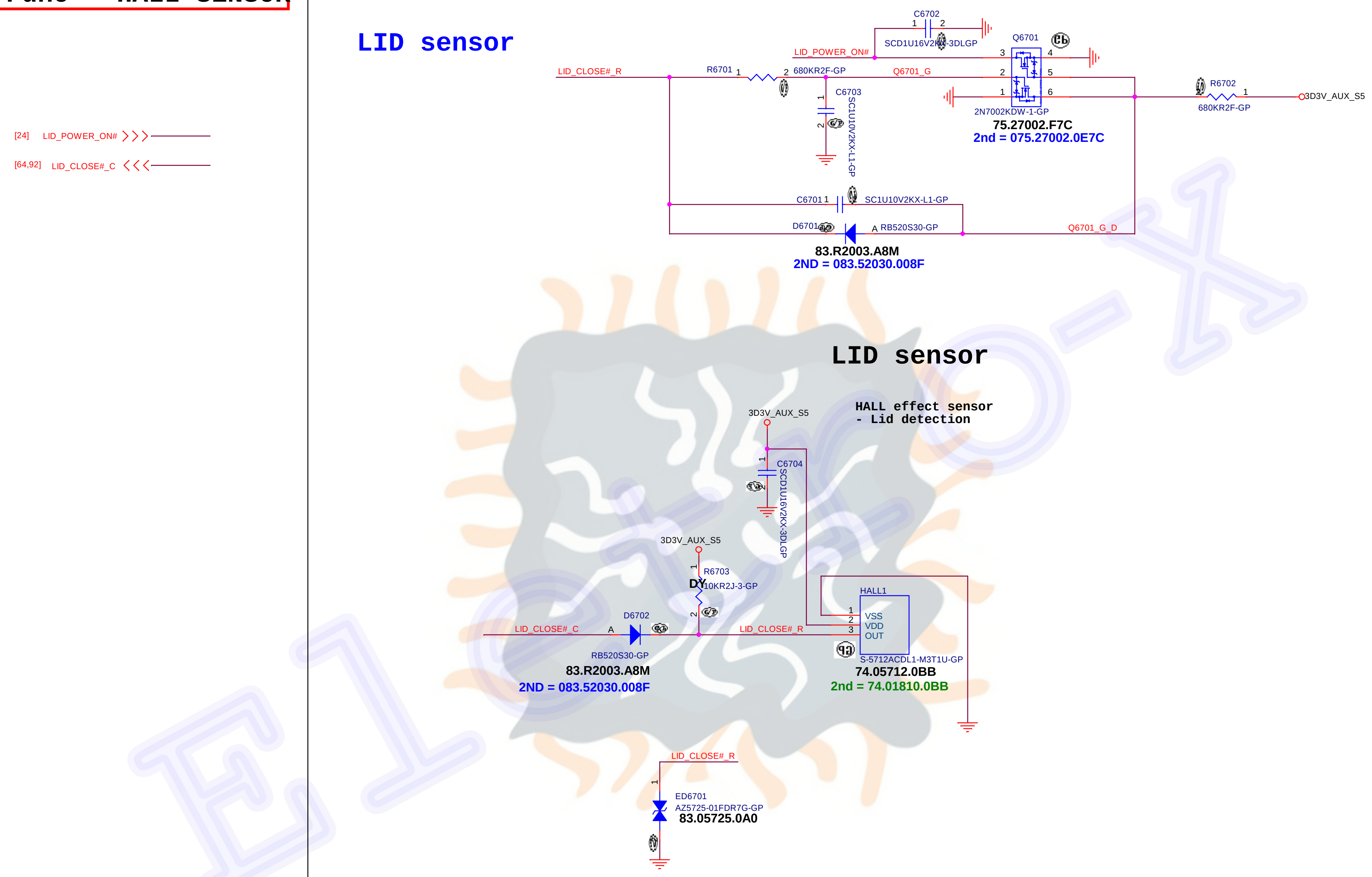
Eletro-X

Main Func = HALL SENSOR



<Core Design>

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Title	Reserved	
Size A3	Document Number Mantis_CML	Rev A00
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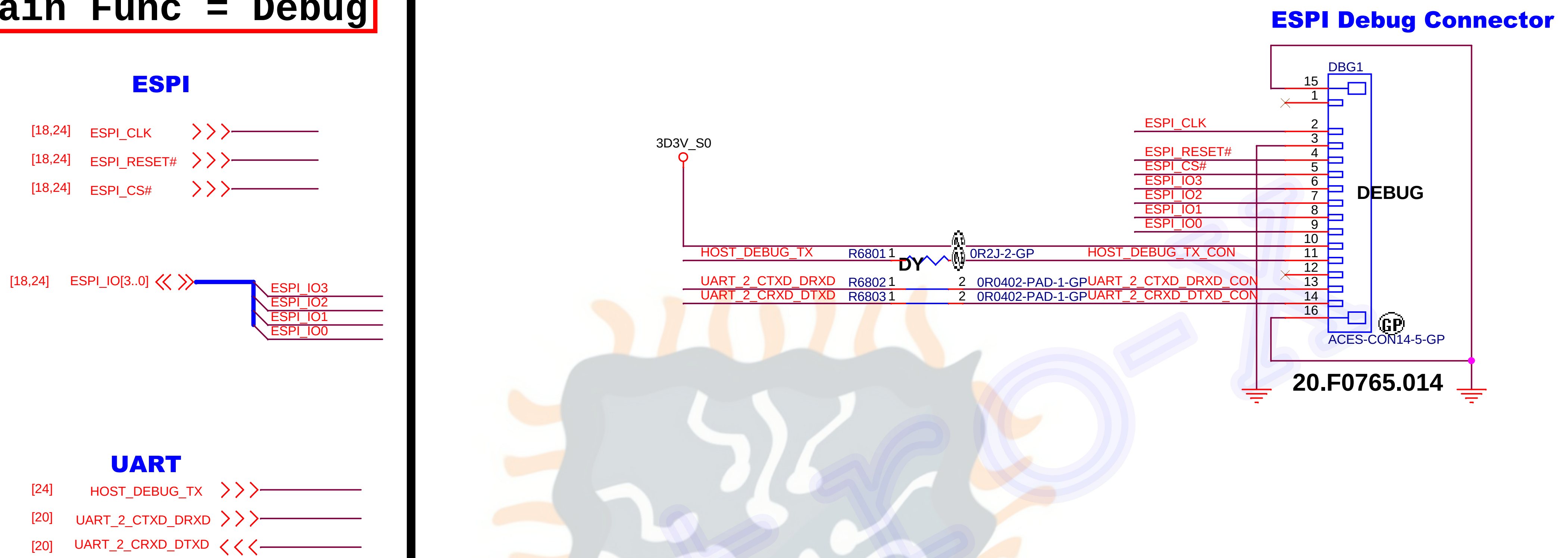
Main Func = Debug



<Core Design>

DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Dubug connector*
Size A4	Document Number *Mantis_CML* Rev A00
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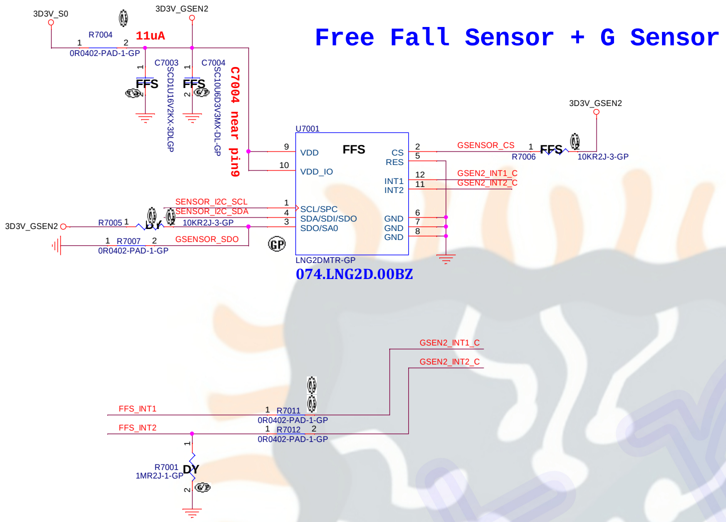
SSID = User.interface

Mantis Accelerometer for adaptive thermal and HDD protection

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I^2C lines.

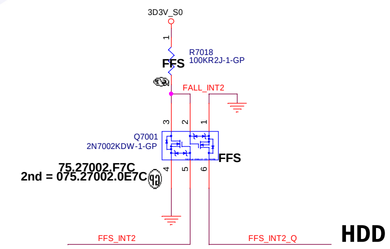
[20] GSEN2_INT1_C
[20] GSEN2_INT2_C
[20] SENSOR_I2C_SCL
[20] SENSOR_I2C_SDA
[18] FFS_INT1
[20] FFS_INT2
[60] FFS_INT2_Q

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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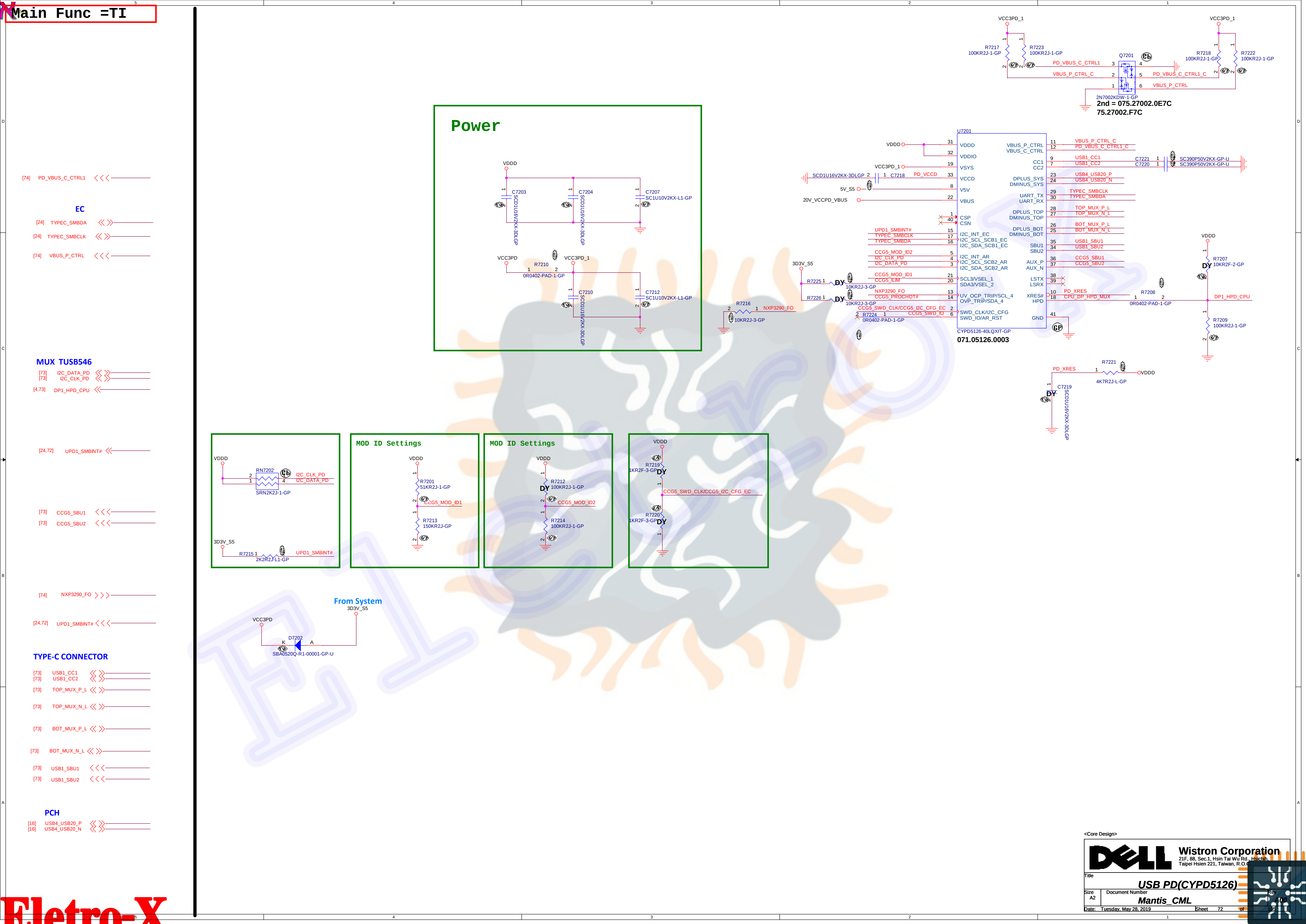
Title	Free Fall Sensor
Size A2	Document Number: Mantis_CML
Date: Tuesday, May 28, 2019	Sheet 70

Main Func =TI



<Core Design>

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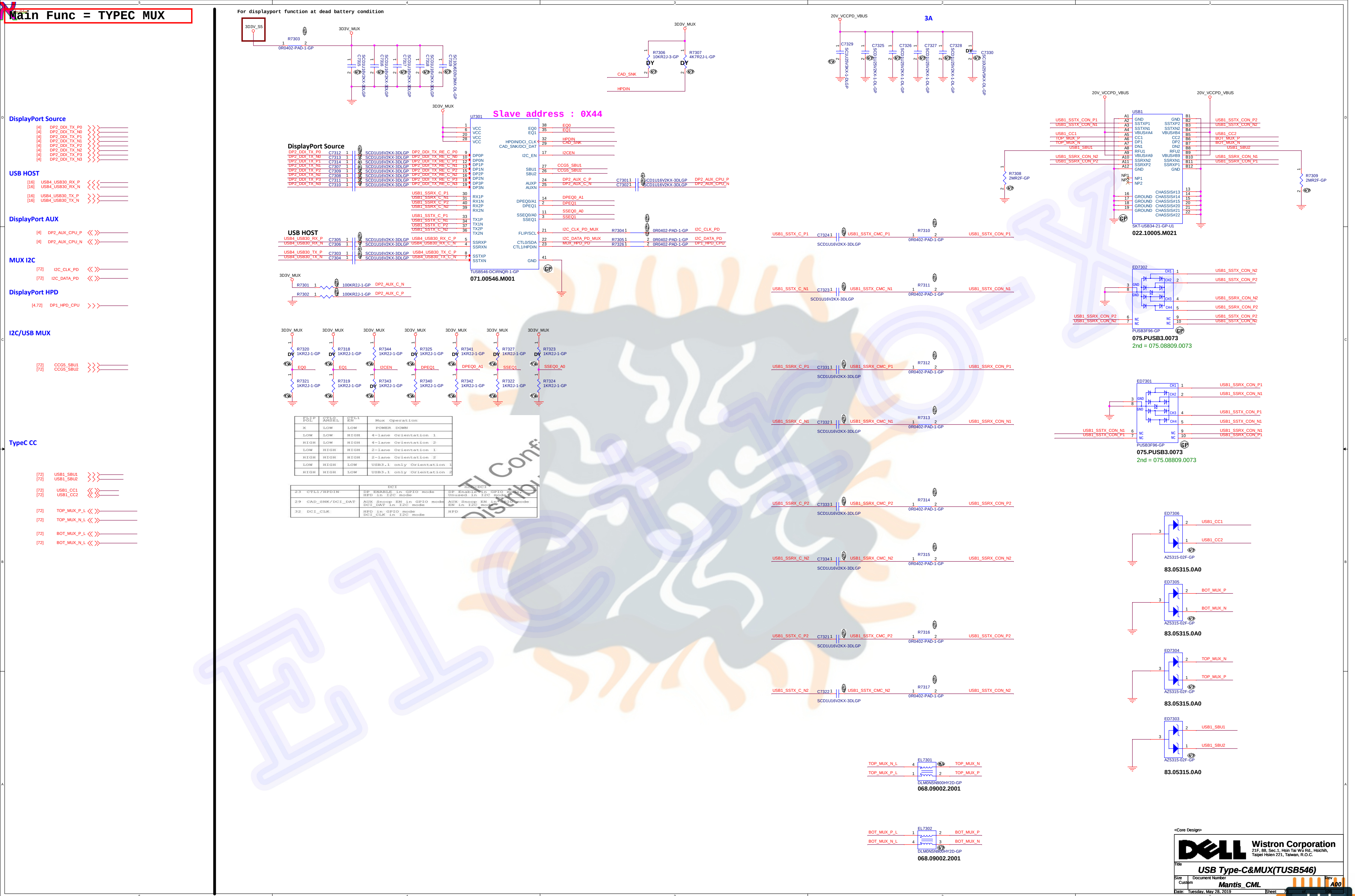
Title: USB PD(CYPD5126)

Size: A2 | Document Number: Mantis_CML

Date: Tuesday, May 28, 2019 | Sheet 72

Main Func = TYPEC MUX



FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

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Title: USB Type-C&MUX(TUSB546)

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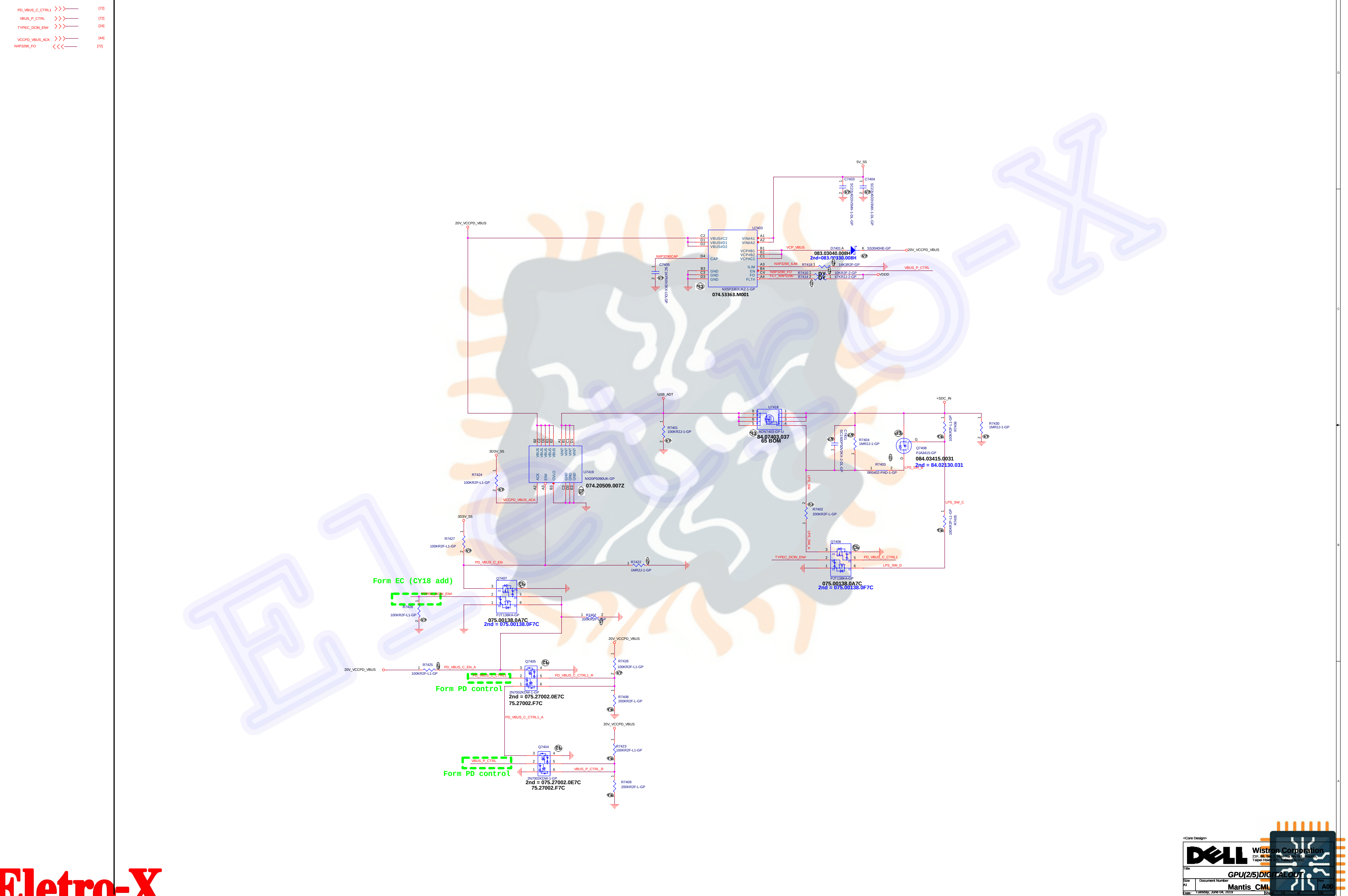
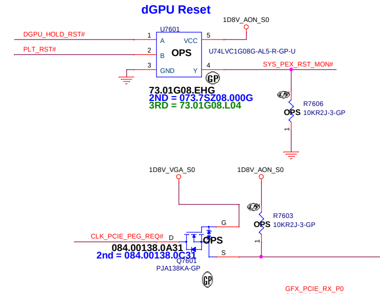
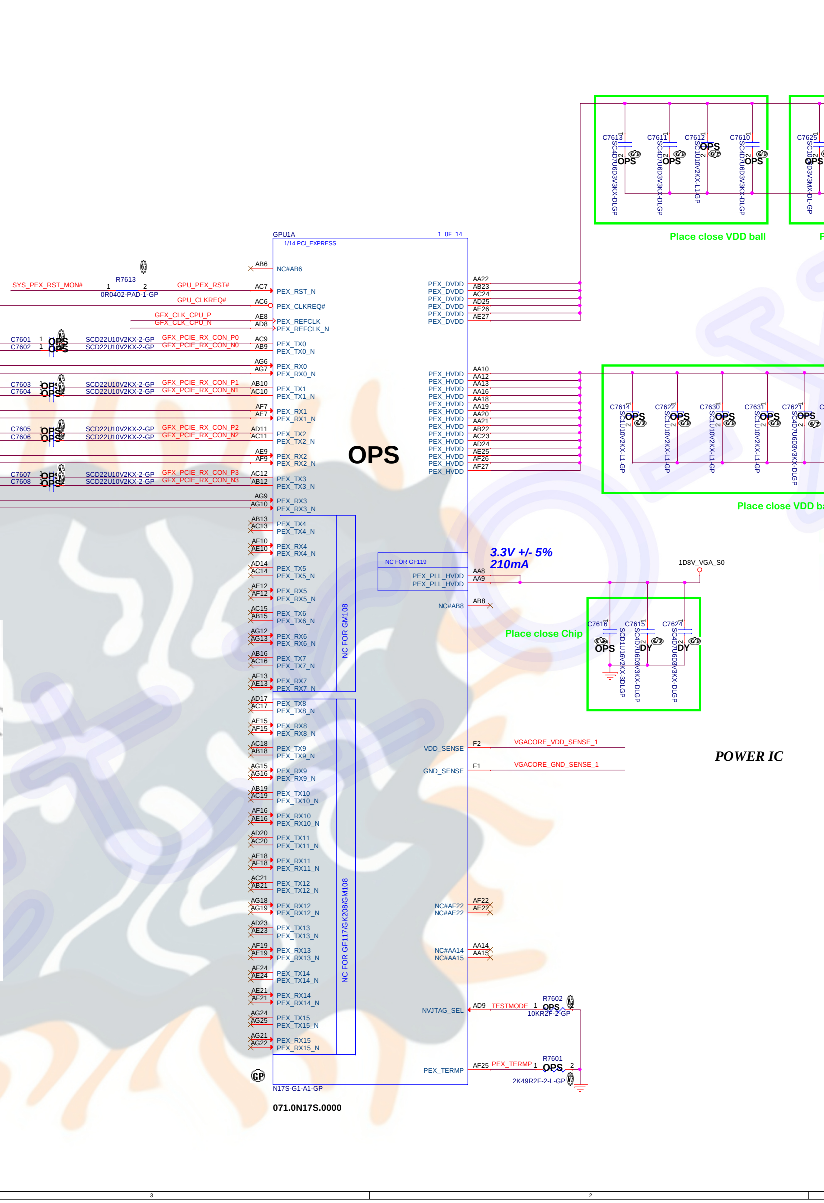

PD_VBUS_C_CTRL1 [72]
VBUS_P_CTRL [72]
TYPEC_DCIN_EN# [24]
VCCPD_VBUS_ACK [44]
NXP3290_FO [72]
5V_S5
C7403
C7404
20V_VCCPD_VBUS
U7403
NXP3290CAP
C7405
VCP_VBUS
D7401
SS3040HE-GP
083.03040.008H
2nd=083.00330.008H
NXP3290_ILIM
R7418
14K3R2F-GP
VBUS_P_CTRL
NXP3290_FO
R7410
10KR2F-2-GP
R7414
47KR2J-2-GP
NX5P3363UKZ-1-GP
074.53363.M001
USB_ADT
R7401
100KR2J-1-GP
U7418
AON7403-GP-U
84.07403.037
65 BOM
+SDC_IN
R7406
R7430
1MR2J-1-GP
R7404
1MR2J-1-GP
Q7408
PJA3415-GP
084.03415.0031
2nd = 84.02130.031
R7403
0R0402-PAD-1-GP
3D3V_S5
R7424
100KR2F-L1-GP
U7419
NX20P5090UK-GP
074.20509.007Z
VCCPD_VBUS_ACK
LPS_SW
LPS_SW_C
R7402
200KR2F-L-GP
R7405
100KR2F-L1-GP
Q7406
TYPEC_DCIN_EN#
PD_VBUS_C_CTRL1
LPS_SW_D
PJT138KA-GP
075.00138.0A7C
2nd = 075.00138.0F7C
3D3V_S5
R7427
100KR2F-L1-GP
PD_VBUS_C_EN
R7422
1MR2J-1-GP
Form EC (CY18 add)
Q7407
R7428
100KR2F-L1-GP
PJT138KA-GP
075.00138.0A7C
2nd = 075.00138.0F7C
R7402
200KR2F-GP
20V_VCCPD_VBUS
R7426
100KR2F-L1-GP
20V_VCCPD_VBUS
R7425
100KR2F-L1-GP
PD_VBUS_C_EN_A
Q7405
PD_VBUS_C_CTRL1_R
Form PD control
2N7002KDW-1-GP
2nd = 075.27002.0E7C
75.27002.F7C
R7408
200KR2F-L-GP
PD_VBUS_C_CTRL1_A
20V_VCCPD_VBUS
R7423
100KR2F-L1-GP
Q7404
VBUS_P_CTRL
VBUS_P_CTRL_R
Form PD control
2N7002KDW-1-GP
2nd = 075.27002.0E7C
75.27002.F7C
R7409
200KR2F-L-GP
<Core Design>
Wistron Corporation
GPU(2/5)DIGITALOUT
Mantis_CML
A00
Tuesday, June 04, 2019
Eletro-X

Main Func = dGPU





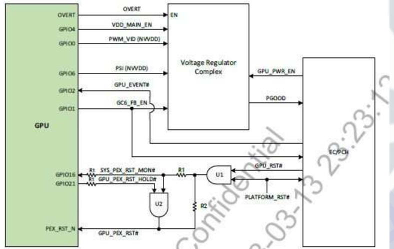


Figure 11. GC6 2.1 High-Level Signal Connections Concept (w/o GPIO Swizzling)

Note: It is critical that the GPU's OVERT output be routed directly to the voltage regulator complex enable (EN) input so that the GPU can trigger a shutdown.

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population		Location
				N16	N17	
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

GPU	Capacitor Type		Footprint	Population		Location
				N16	N17	
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU

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Title: GPU(1/5)PEG

Size: Custom | Document Number: Mantis_CML | Rev: A00

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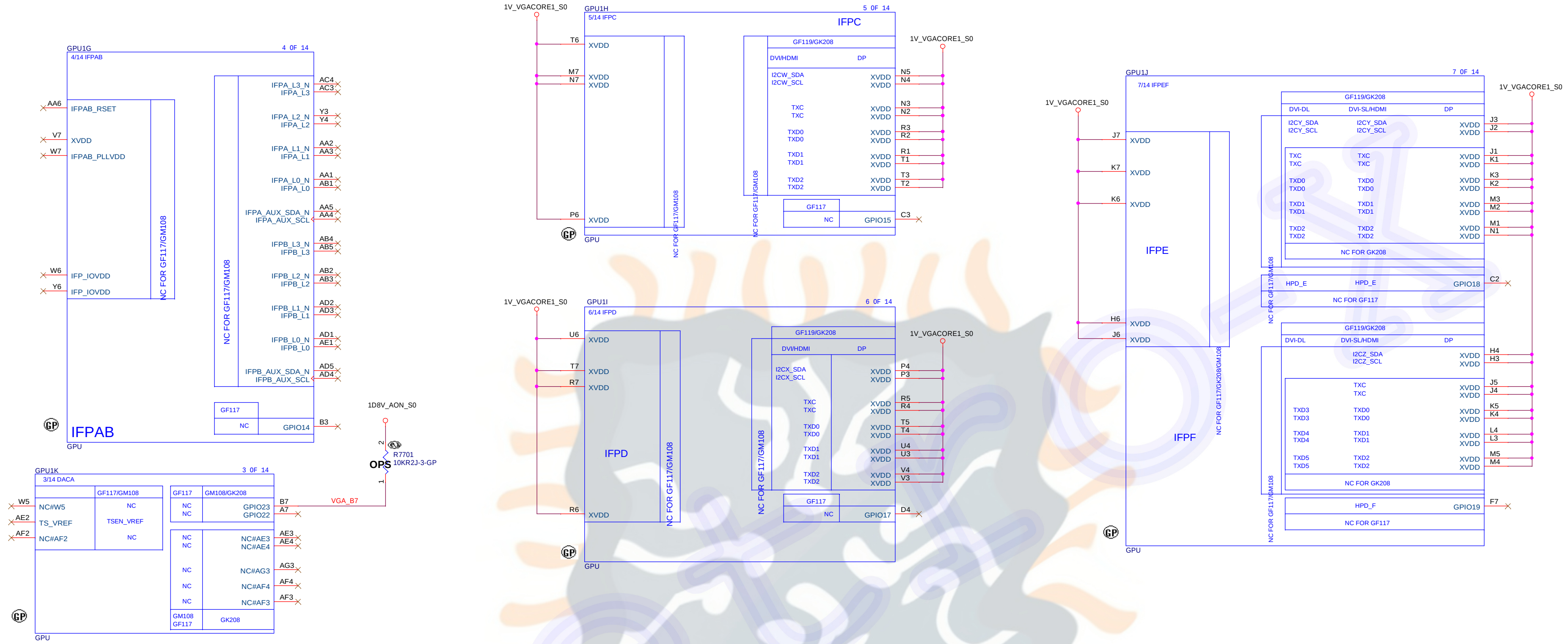
Main Func = dGPU



<Core Design>

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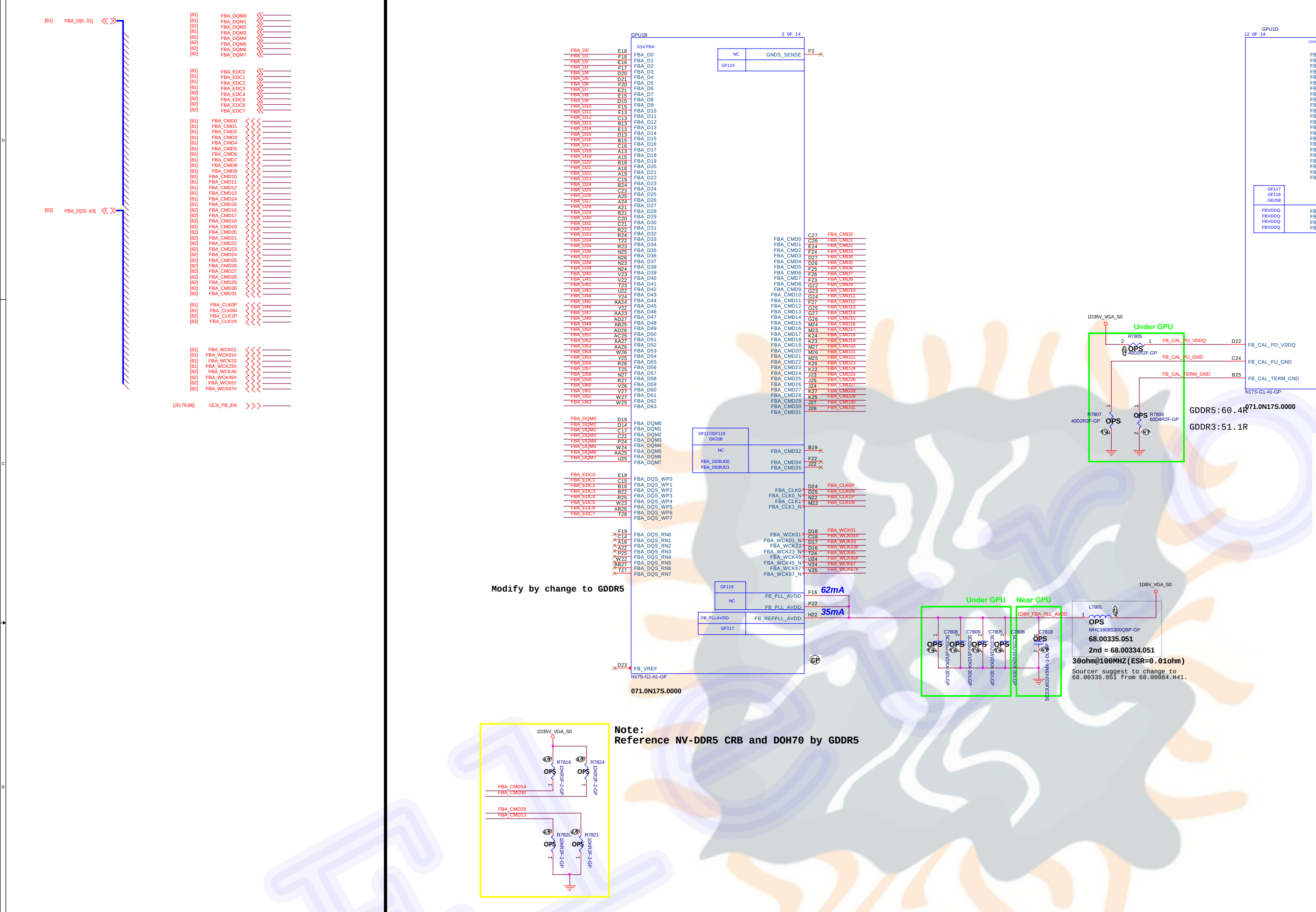
Title
GPU(2/5)DIGITALOUT

Size A2 | Document Number Mantis_CML | Rev A00

Date: Tuesday, May 28, 2019 | Sheet 77

Main Func = dGPU



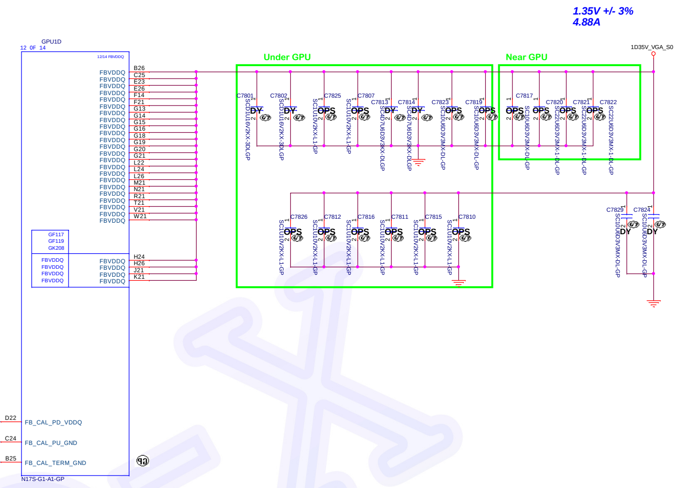


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

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GPU(3/5)VRAM/IF
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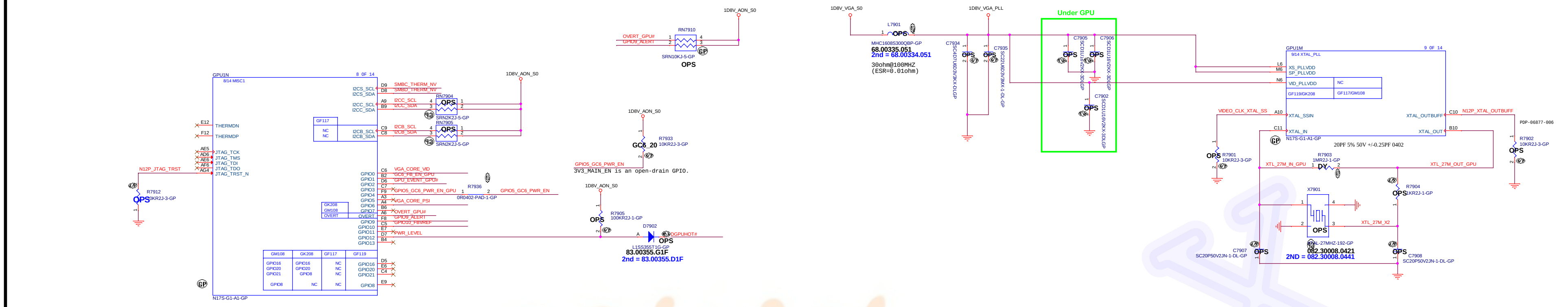
A00



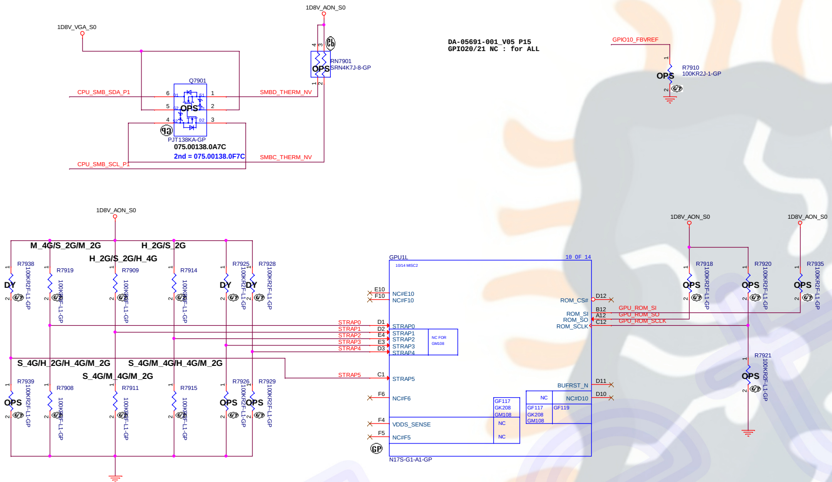


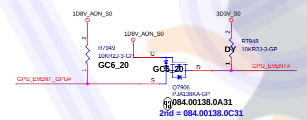
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

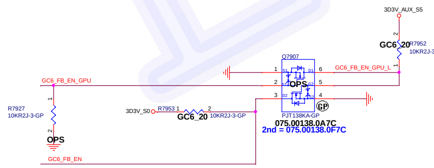
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

20161215 N17

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0





64 bits	
GDDR5 @ 1.35V	
2GB	4GB
2pcs x 8Gb(256M x 32)	4pcs x 8Gb(512Mx 16)
Hynix - H5GC8H24MJR-R0C (029XX)	Hynix - H5GC8H24MJR-R0C (029XX)
Micron - MT51J256M32HF-70:A (V15MH)	Micron - MT51J256M32HF-70:A (V15MH)
Samsung - K4G80325FB-HC28 (N1MMH)	Samsung - K4G80325FB-HC28 (N1MMH)

Table 4. N17S-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
4 Gb	128Mx32 256Mx16	1.35V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready

Notes:

1. For N17S-G1, the maximum allowable memory case temperature is 85 °C.
2. Higher-speed grade memory devices can be used on N17x GPU designs in accordance with written waivers from the memory vendors. An acceptable waiver should indicate that the higher speed grade memory can be used as a substitute for lower-speed grade memory without any changes to spec parameters, including but not limited to timing, BIOS, and voltage.

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	Samsung 4G 2G
L	L	H	1 (0x0001)	Micron 4G 2G
L	H	L	2 (0x0002)	Hynix 4G 2G
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	

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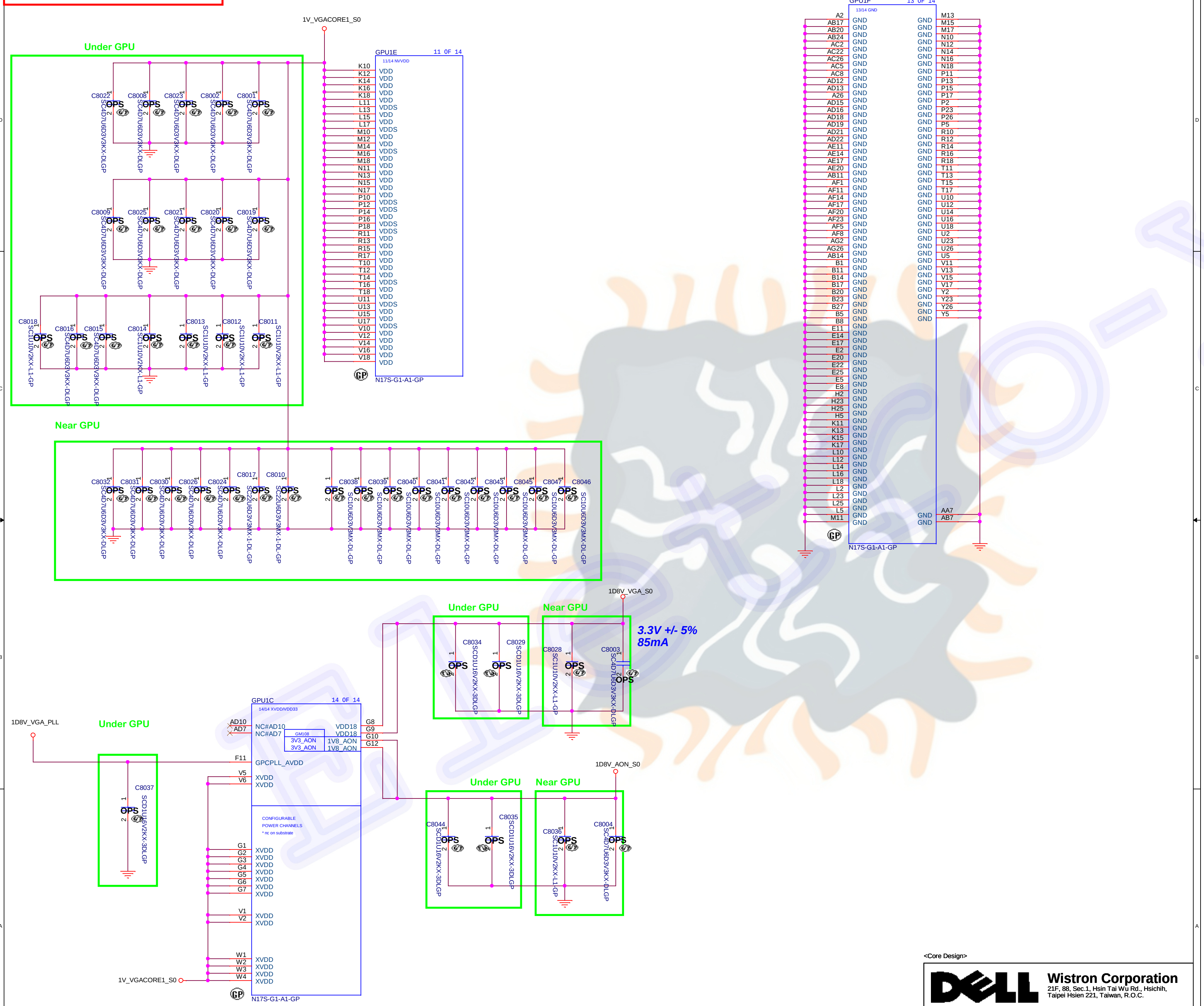
Title	GPU(4/5)GPIO/STRAP
Size Custom / Document Number	Mantis_CML
Rev	A00
Date	Tuesday, May 28, 2019
Sheet	79 of 105

Main Func = dGPU



<Core Design>

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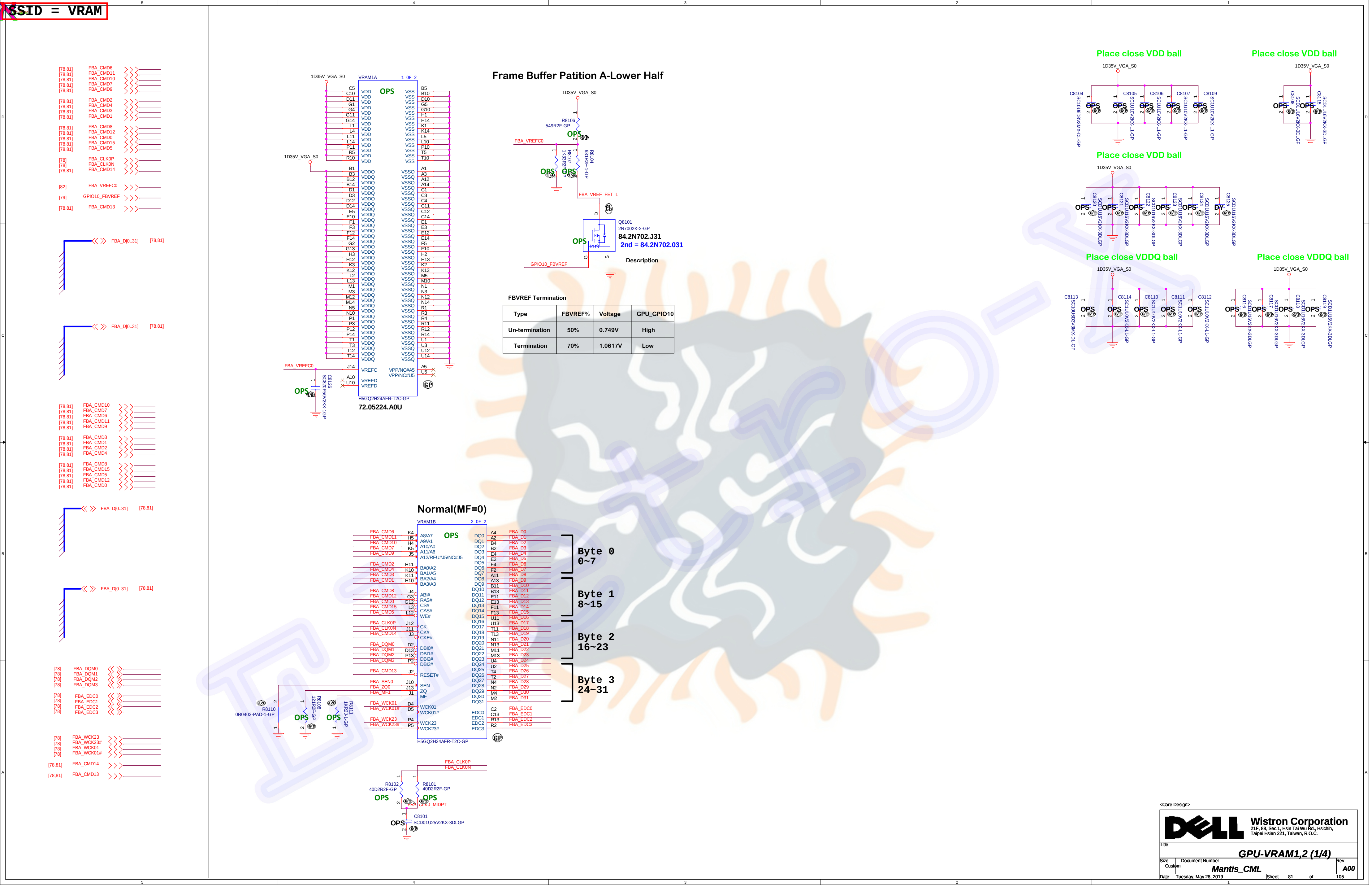
Title	GPU(5/5)PWR/GND	
Size Custom	Document Number Mantis_CML	Rev A00
Date: Tuesday, May 28, 2019	Sheet 80 of 105	

SSID = VRAM



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

<Core Design>

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Title: GPU-VRAM1,2 (1/4)

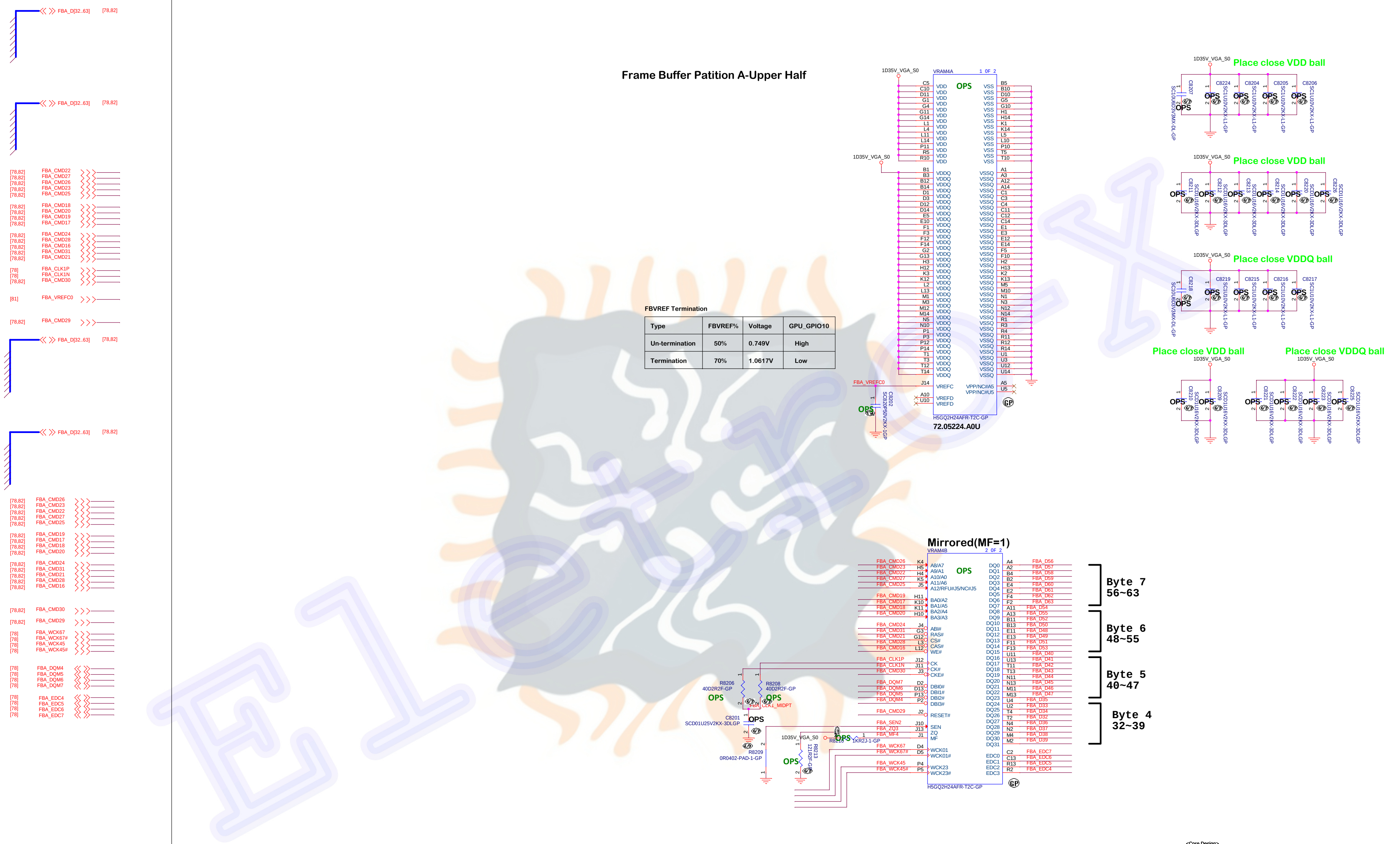
Size: Custom | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, May 28, 2019 | Sheet 81 of 105

Eletro-X

SSID = VRAM

Frame Buffer Patition A-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

Place close VDD ball

Place close VDDQ ball

Mirrored(MF=1)

Byte 7 56~63

Byte 6 48~55

Byte 5 40~47

Byte 4 32~39

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Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Mantis_CML | Rev: A00

Date: Tuesday, May 28, 2019 | Sheet 82 of 105

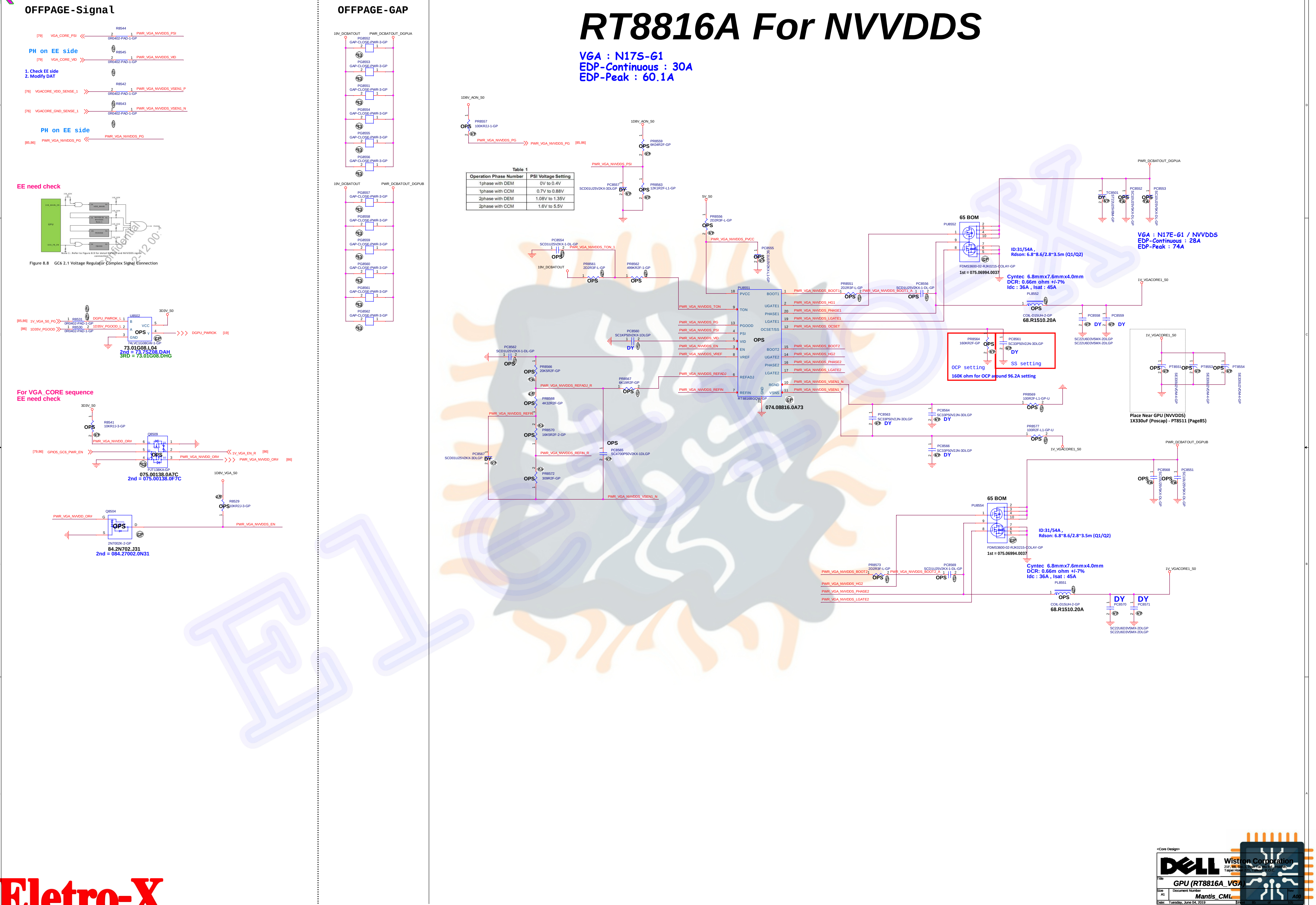
Eletro-X

RT8816A For NVVDDS

VGA : N17S-G1
EDP-Continuous : 30A
EDP-Peak : 60.1A

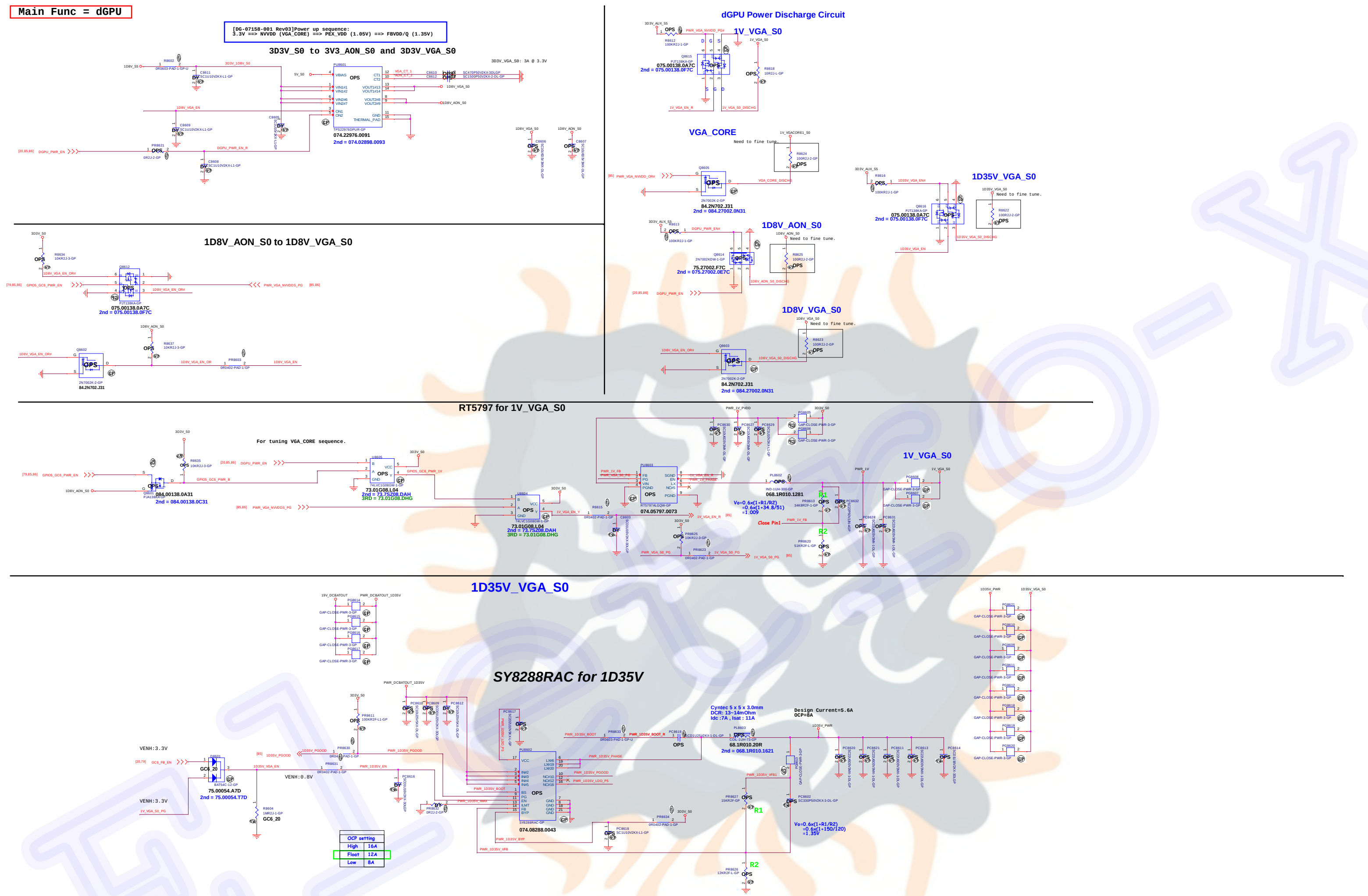
Table 1

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V



Wistron Corporation
GPU (RT8816A_VGA)
Mantis_CML
Date: Tuesday, June 04, 2019

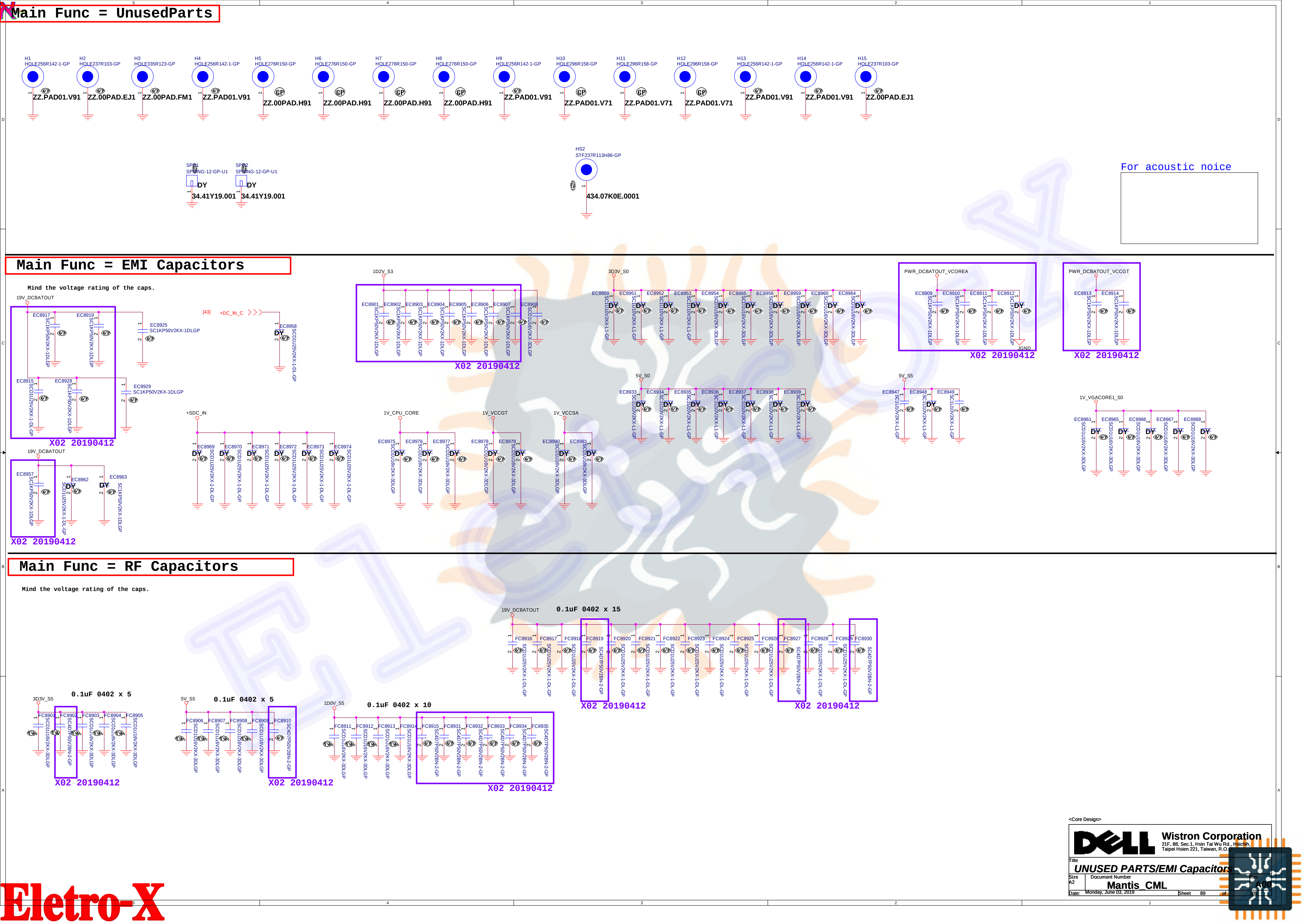
Main Func = dGPU



Wistron Corporation

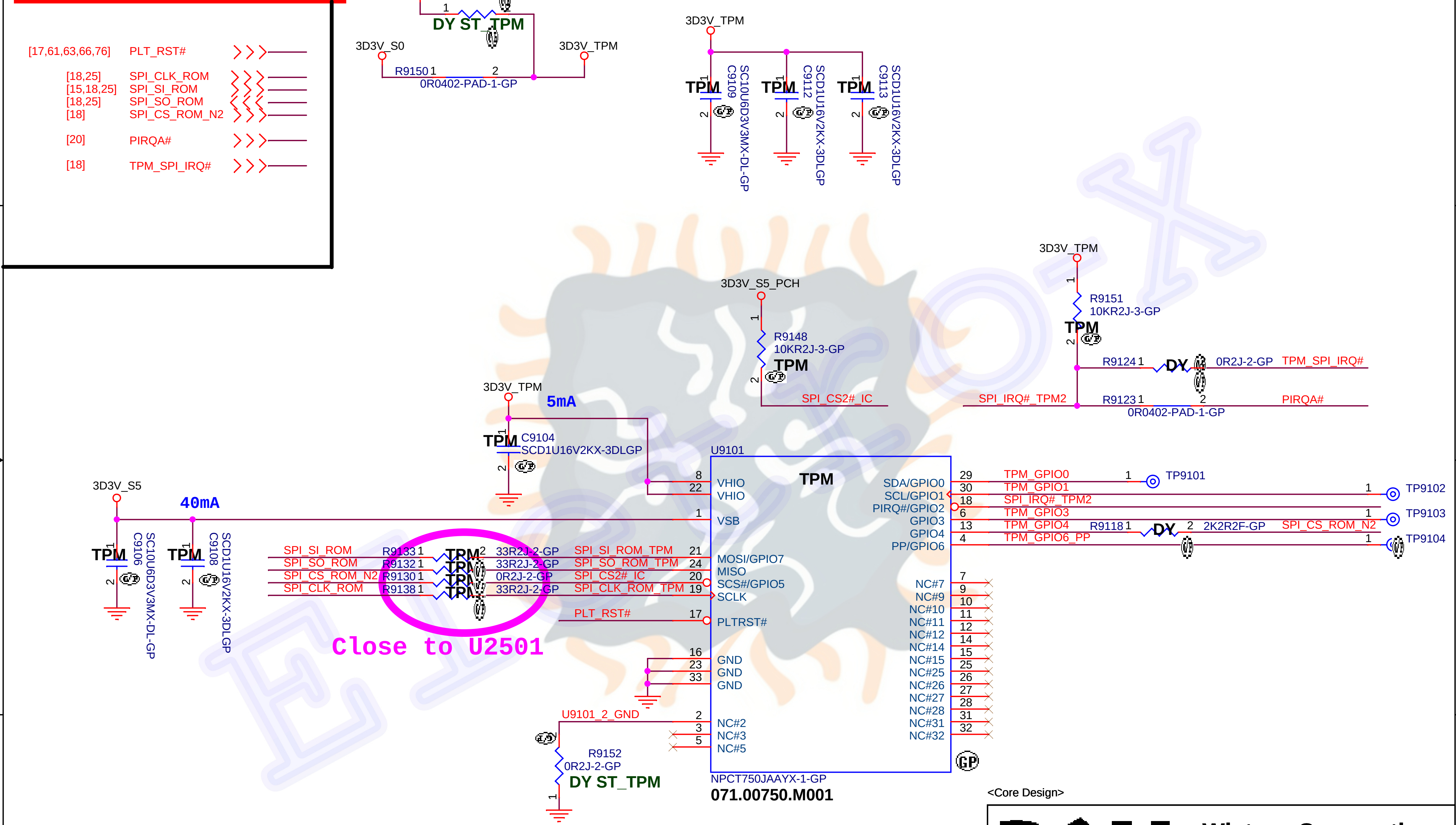
DISCRETE VGA POWER

Mantis_CML



Main Func = UnusedParts
H1 HOLE256R142-1-GP ZZ.PAD01.V91
H2 HOLE237R103-GP ZZ.00PAD.EJ1
H3 HOLE335R123-GP ZZ.00PAD.FM1
H4 HOLE256R142-1-GP ZZ.PAD01.V91
H5 HOLE276R150-GP ZZ.00PAD.H91
H6 HOLE276R150-GP ZZ.00PAD.H91
H7 HOLE276R150-GP ZZ.00PAD.H91
H8 HOLE276R150-GP ZZ.00PAD.H91
H9 HOLE256R142-1-GP ZZ.PAD01.V91
H10 HOLE296R158-GP ZZ.PAD01.V71
H11 HOLE296R158-GP ZZ.PAD01.V71
H12 HOLE296R158-GP ZZ.PAD01.V71
H13 HOLE256R142-1-GP ZZ.PAD01.V91
H14 HOLE256R142-1-GP ZZ.PAD01.V91
H15 HOLE237R103-GP ZZ.00PAD.EJ1
SPR1 SPRING-12-GP-U1 DY 34.41Y19.001
SPR2 SPRING-12-GP-U1 DY 34.41Y19.001
HS2 STF237R113H86-GP 434.07K0E.0001
For acoustic noice
Main Func = EMI Capacitors
Mind the voltage rating of the caps.
19V_DCBATOUT
EC8917 SC1KP50V2KX-1DLGP
EC8919 SC1KP50V2KX-1DLGP
EC8925 SC1KP50V2KX-1DLGP
EC8915 SCD1U25V2KX-1-DL-GP
EC8928 SC1KP50V2KX-1DLGP
EC8929 SC1KP50V2KX-1DLGP
[43] +DC_IN_C
EC8958 SCD1U25V2KX-1-DL-GP DY
X02 20190412
EC8957 SC1KP50V2KX-1DLGP
EC8962 SCD1U25V2KX-1-DL-GP DY
EC8963 SC1KP50V2KX-1DLGP DY
1D2V_S3
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908
3D3V_S0
EC8950 EC8951 EC8952 EC8953 EC8954 EC8955 EC8956 EC8959 EC8960 EC8964
PWR_DCBATOUT_VCOREA
EC8909 EC8910 EC8911 EC8912
PWR_DCBATOUT_VCCGT
EC8913 EC8914
5V_S0
EC8933 EC8934 EC8935 EC8936 EC8937 EC8938 EC8939
5V_S5
EC8947 EC8948 EC8949
1V_VGACORE1_S0
EC8961 EC8965 EC8966 EC8967 EC8968
+SDC_IN
EC8969 EC8970 EC8971 EC8972 EC8973 EC8974
1V_CPU_CORE
EC8975 EC8976 EC8977
1V_VCCGT
EC8978 EC8979
1V_VCCSA
EC8980 EC8981
Main Func = RF Capacitors
Mind the voltage rating of the caps.
19V_DCBATOUT 0.1uF 0402 x 15
FC8916 FC8917 FC8918 FC8919 FC8920 FC8921 FC8922 FC8923 FC8924 FC8925 FC8926 FC8927 FC8928 FC8929 FC8930
3D3V_S5 0.1uF 0402 x 5
FC8901 FC8902 FC8903 FC8904 FC8905
5V_S5 0.1uF 0402 x 5
FC8906 FC8907 FC8908 FC8909 FC8910
1D0V_S5 0.1uF 0402 x 10
FC8911 FC8912 FC8913 FC8914 FC8915 FC8931 FC8932 FC8933 FC8934 FC8935
X02 20190412
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size A2
Document Number
Mantis_CML
Date: Monday, June 03, 2019
Sheet 89
Eletro-X

Main Func = TPM



<Core Design>

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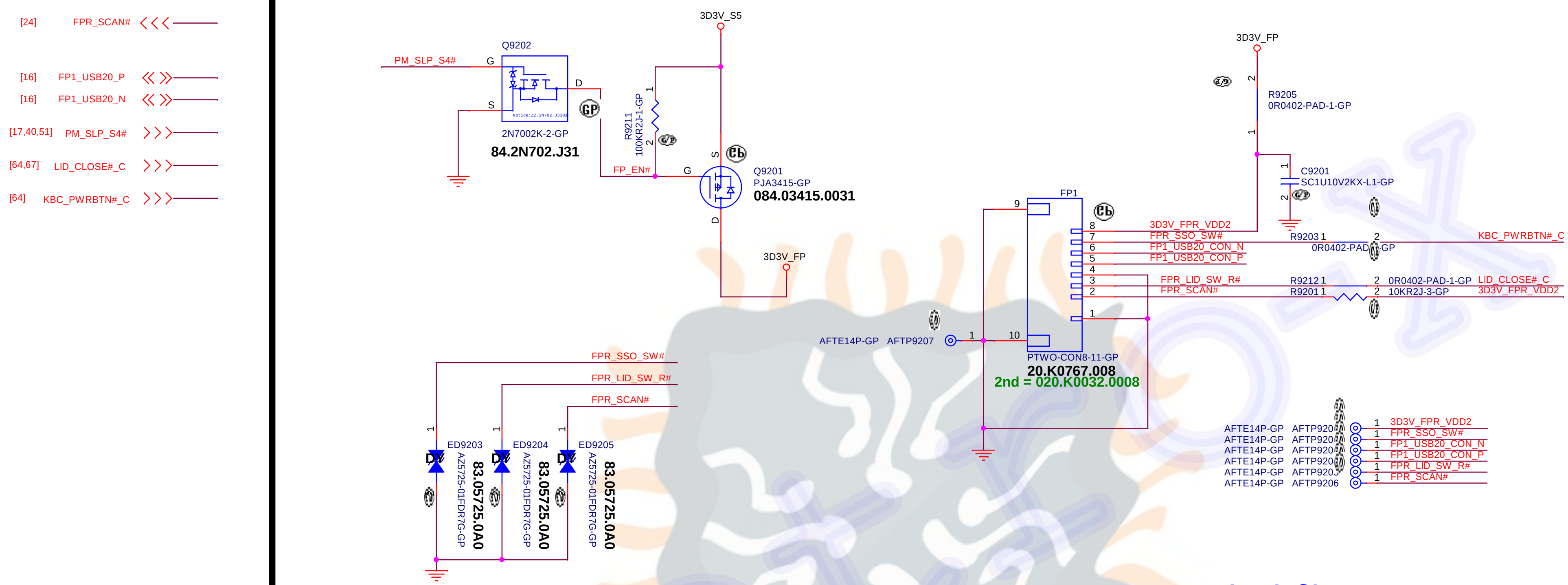
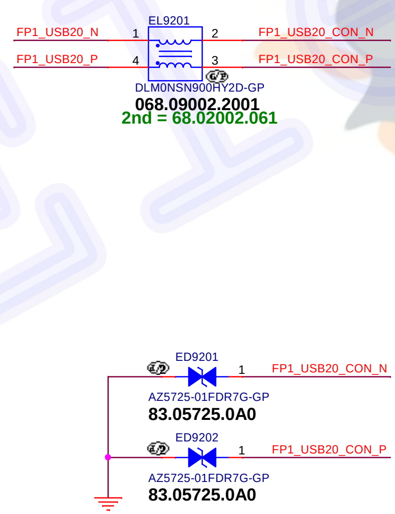
Title	INT IO (TPM)	
Size A4	Document Number Mantis_CML	Rev A00
Date: Tuesday, May 28, 2019	Sheet 91 of 105	

SSID = Finger Print



FP_Pin_define

PIN 序号	PIN 名	说明
1	VBUS	AVDD(3.3V)
2	Power button	Power button signal
3	USB_DN	USB_N
4	USB_DP	USB_P
5	GND	系统地
6	LID closed	LID closed signal
7	GPIO_key	GPIO
8	ID(GND)	ID 检测脚



<Core Design>

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Title: **Finger Print**

Size: A3 | Document Number: **Mantis_CML** | Rev: A00

Date: Tuesday, May 28, 2019 | Sheet 92 of 105

Main Func = Firmware SW

[19] ME_FWP_SW
[24] ME_FWP

R9806
ME_FWP 2 1 ME_FWP_SW
0R0402-PAD-1-GP
INSTALL after MP

Firmware SW

Default setting:pull LOW
DY for MP

	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

<Core Design>

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Title	CRT_Switch	
Size A3	Document Number Mantis_CML	Rev A00
Date: Tuesday, May 28, 2019	Sheet 98 of 103	

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

<Core Design>

DELL

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Title: *Change History*

Size: A3
Document Number: *Mantis_CML*
Rev: A00
Date: Tuesday, May 28, 2019
Sheet 101 of 101