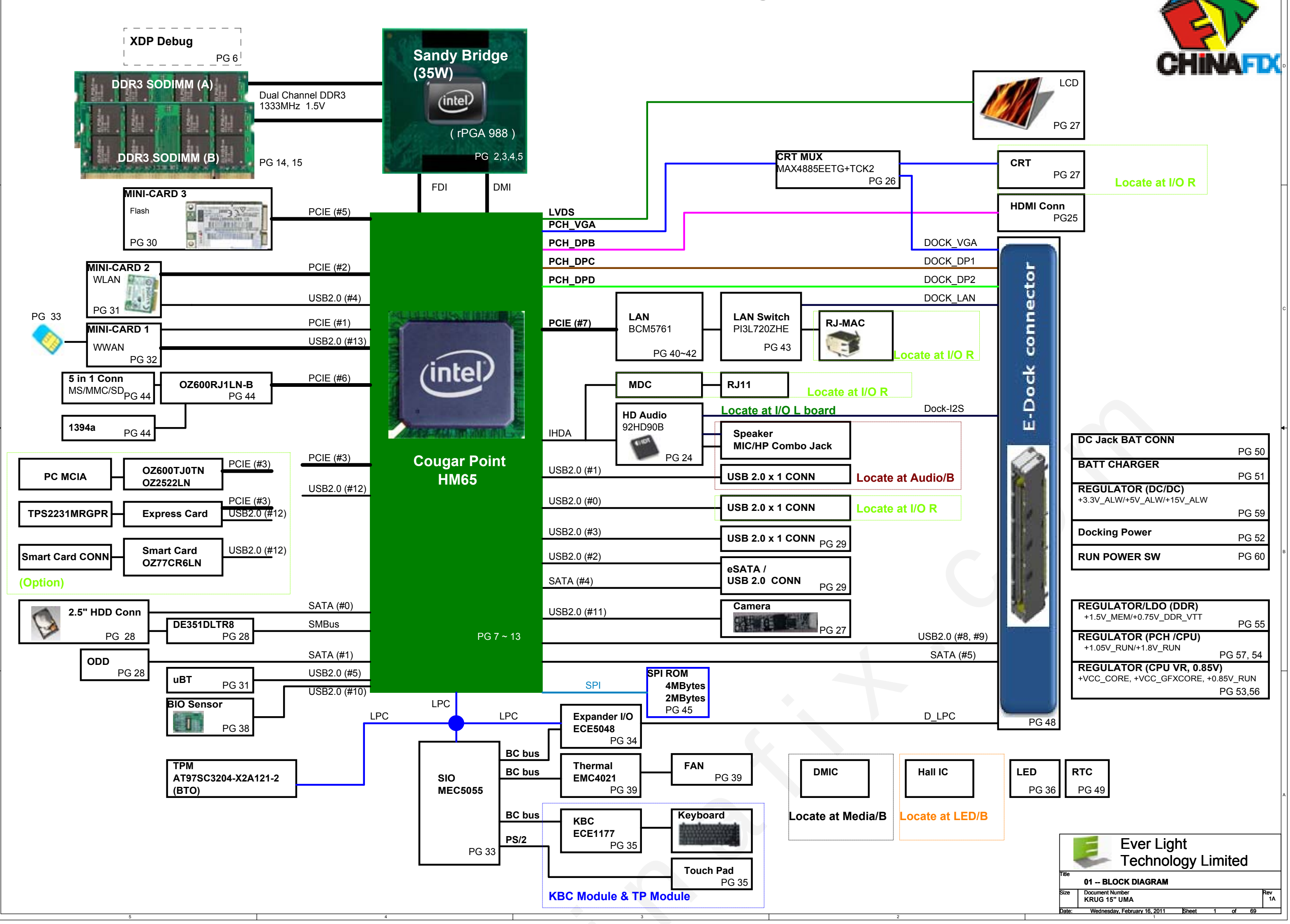
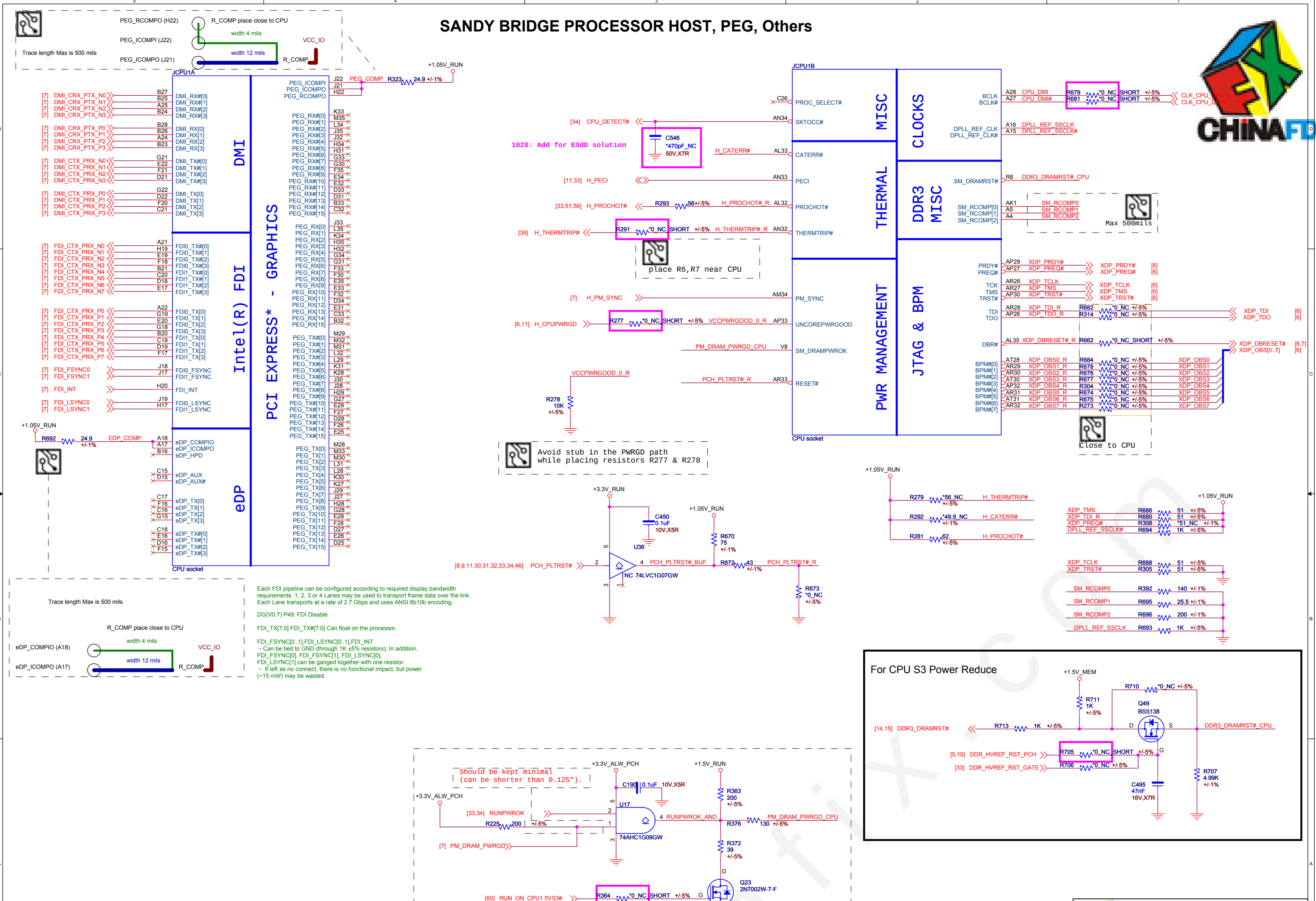
KRUG 15" UMA Block Diagram

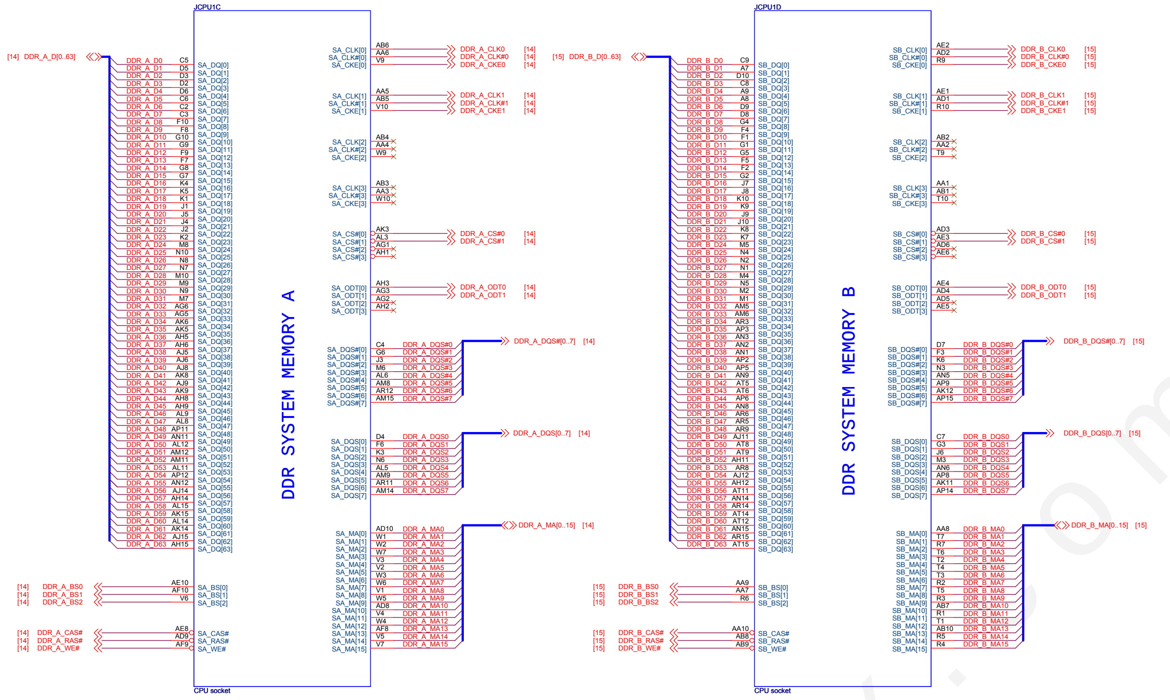


SANDY BRIDGE PROCESSOR HOST, PEG, Others



Ever Light Technology Limited		
Title: 02 -- SNB (rPGA) 1/4 HOST, PEG		
Size	Document Number: KRUG 15" UMA	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 2 of 69	

SANDY BRIDGE PROCESSOR (DDR3)



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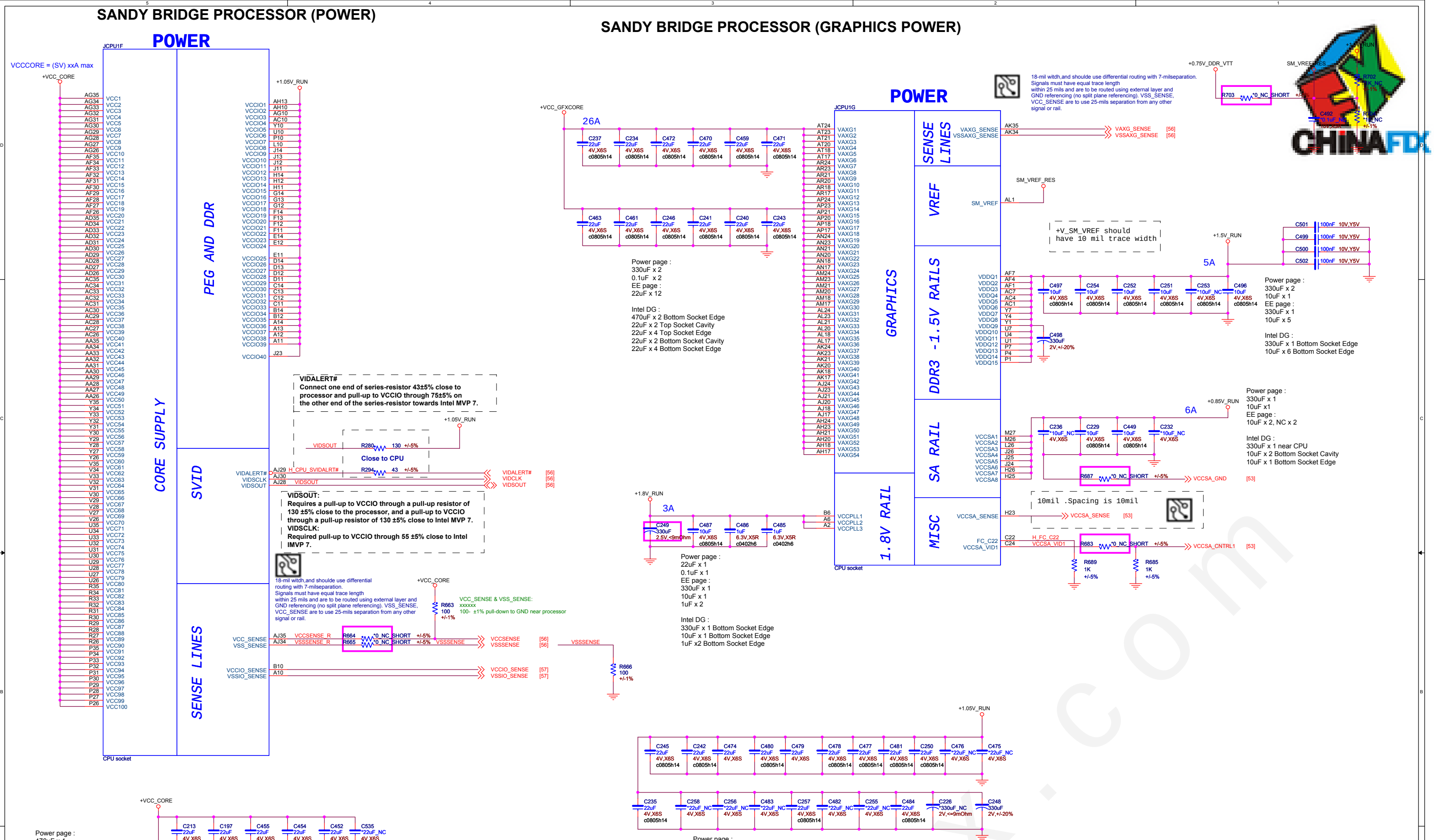
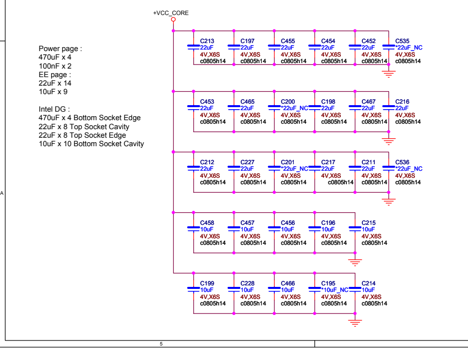
Title	03 -- SNB (rPGA) 2/4 DDR		
Size	Document Number: KRUG 15" UMA		Rev: 1A
Date:	Wednesday, February 16, 2011	Sheet 3 of 69	

SANDY BRIDGE PROCESSOR (POWER)

SANDY BRIDGE PROCESSOR (GRAPHICS POWER)





CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

* Description
5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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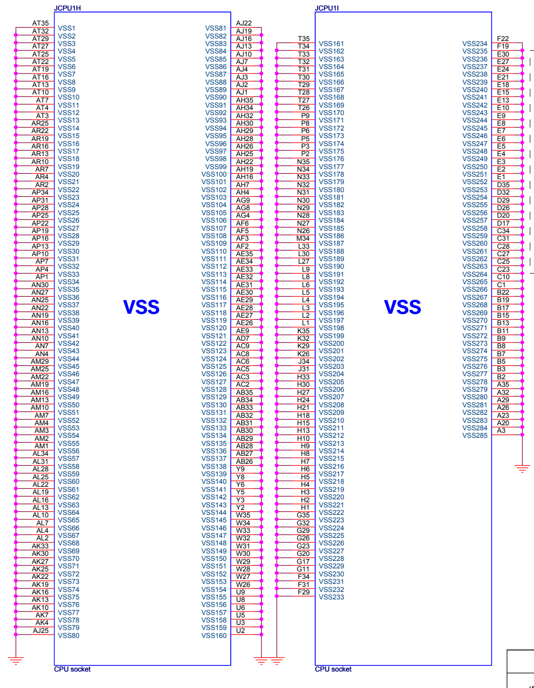
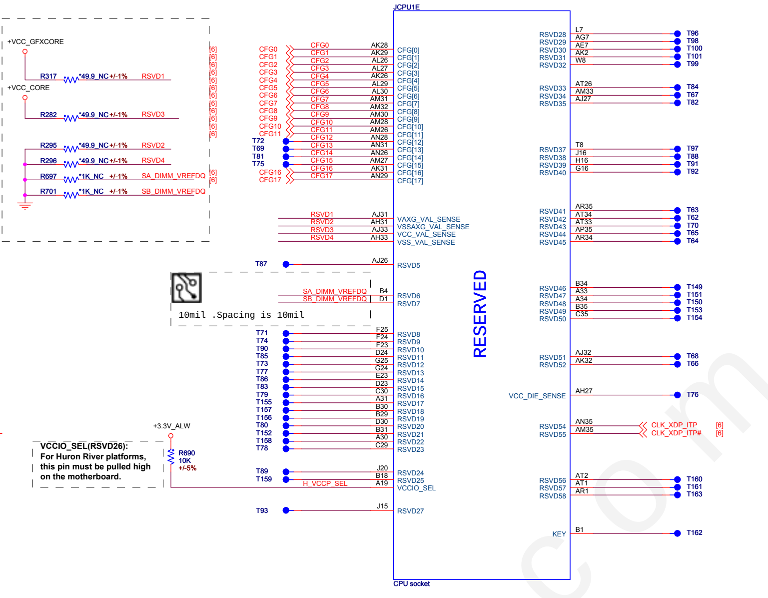
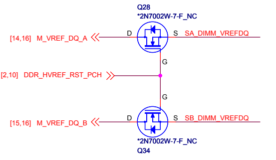
Title	04 -- SNB (rPGA) 3/4 POWER
Size	Document Number: KRUG 15" UMA — Rev 1A
Date:	Wednesday, February 16, 2011 — Sheet 4 of 69

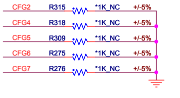
SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)

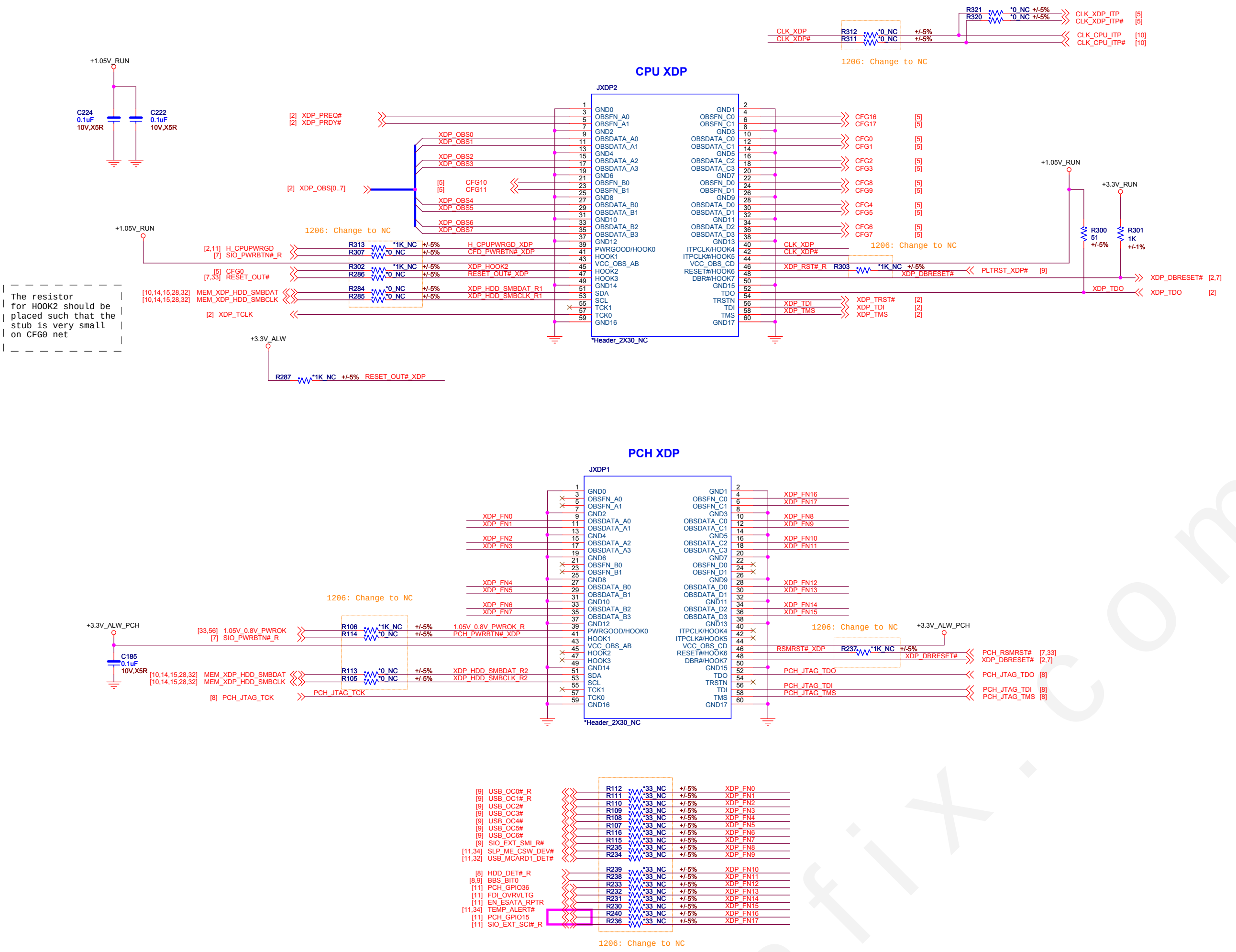






	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Diplay Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 (PEG Defer Training)	PEG Train immediately following xxRESETB de assertion (Default Value)	PEG Wait for BIOS for training

CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable(Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable



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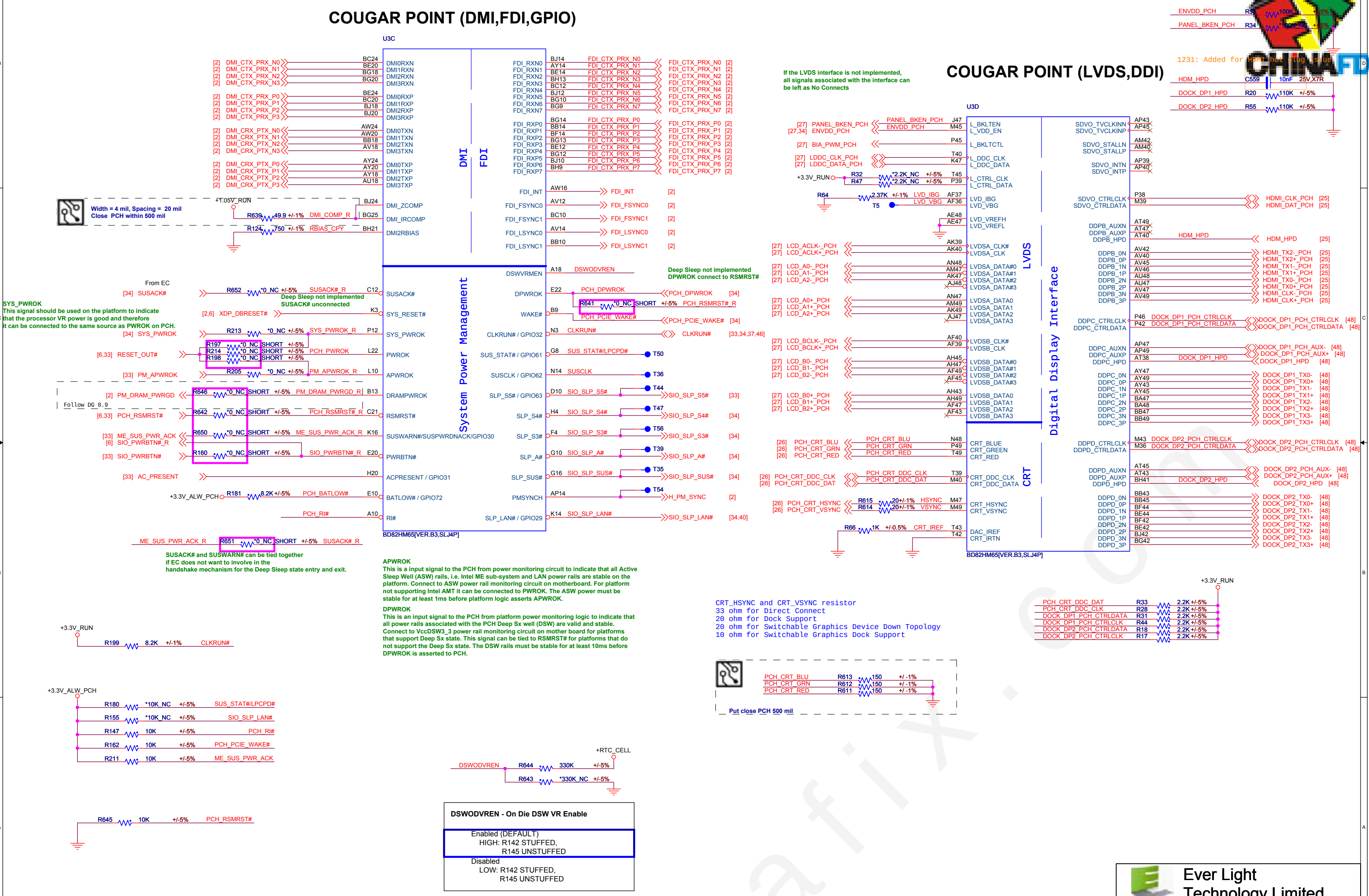
Title	06 -- XDP Connector	
Size	Document Number: Thunder	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 6 of 69	



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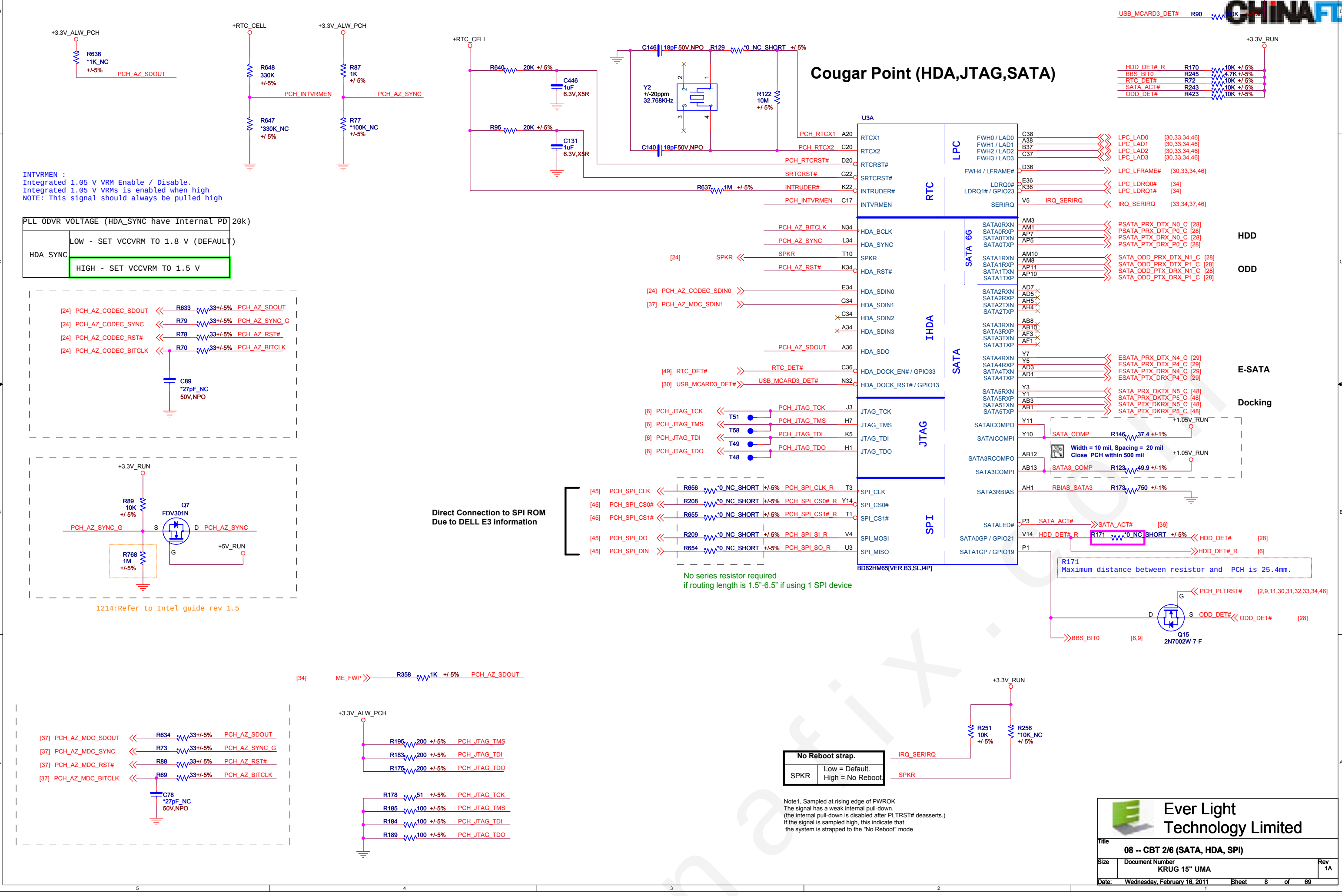
Title	07 -- CBT 1/6 (DMI&VIDEO)		
Size	Document Number: KRUG 15" UMA		Rev 1A
Date:	Wednesday, February 16, 2011	Sheet 7 of 69	



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Title		
08 -- CBT 2/6 (SATA, HDA, SPI)		
Size	Document Number: KRUG 15" UMA	Rev: 1A
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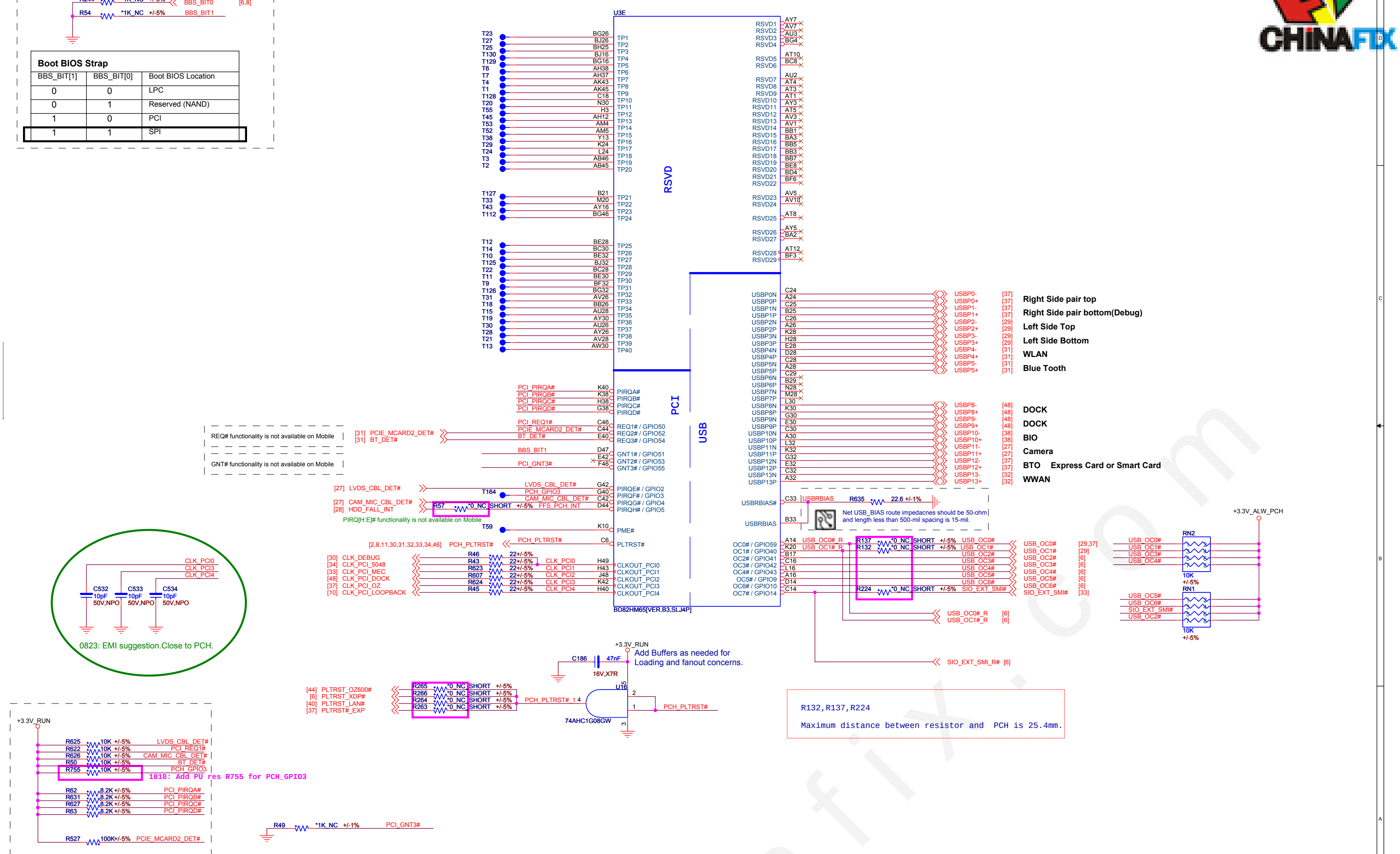
Cougar Point (PCI,USB,NVRAM)



Boot BIOS Strap

BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title	09 -- CBT 3/6 (USB, PCI, NVRAM)		
Size	Document Number KRUG 15" UMA		Rev 1A
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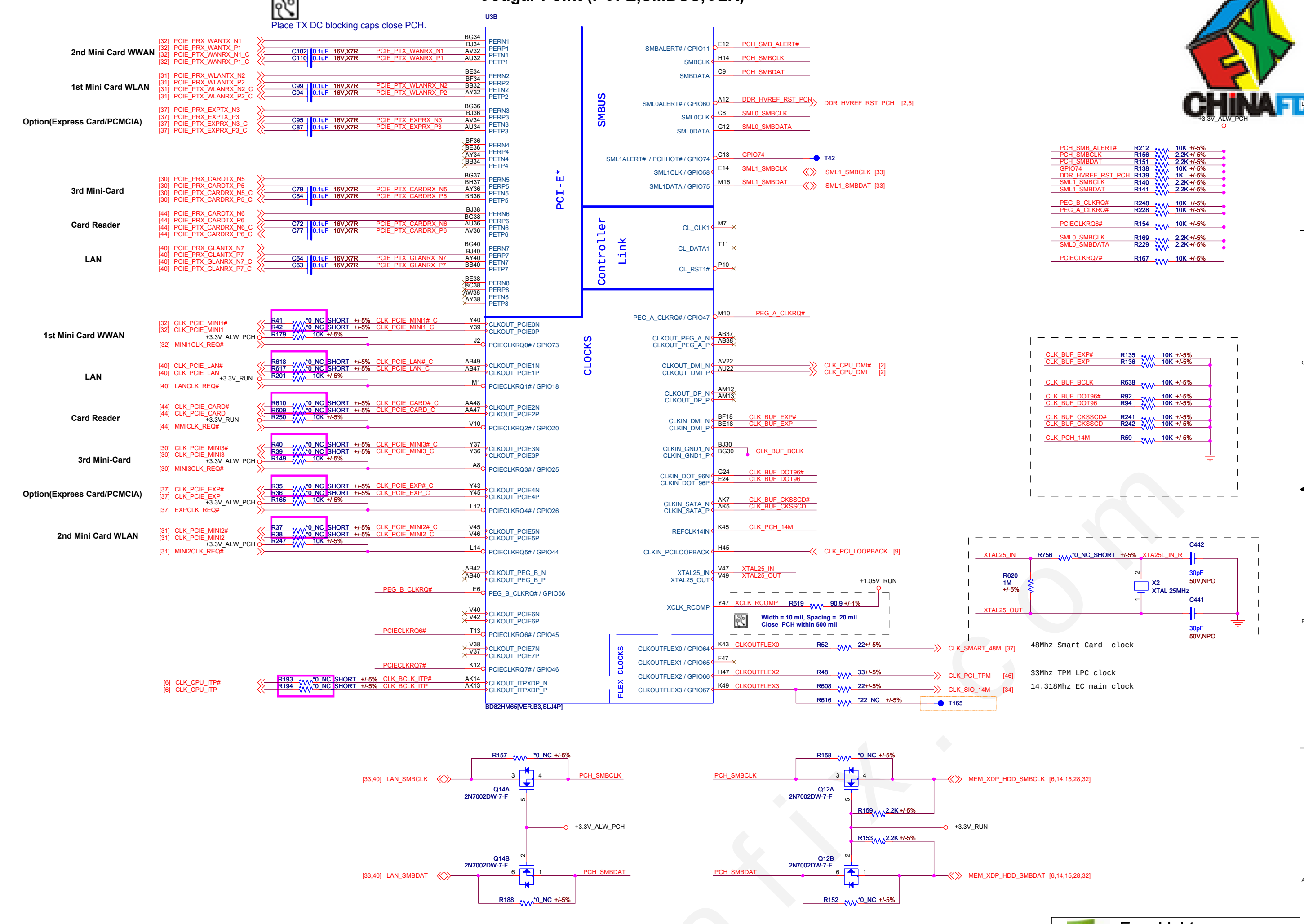
Cougar Point (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



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Title	10 -- CBT 4/7 (PCIE, CLK)
Size / Document Number	KRUG 15" UMA
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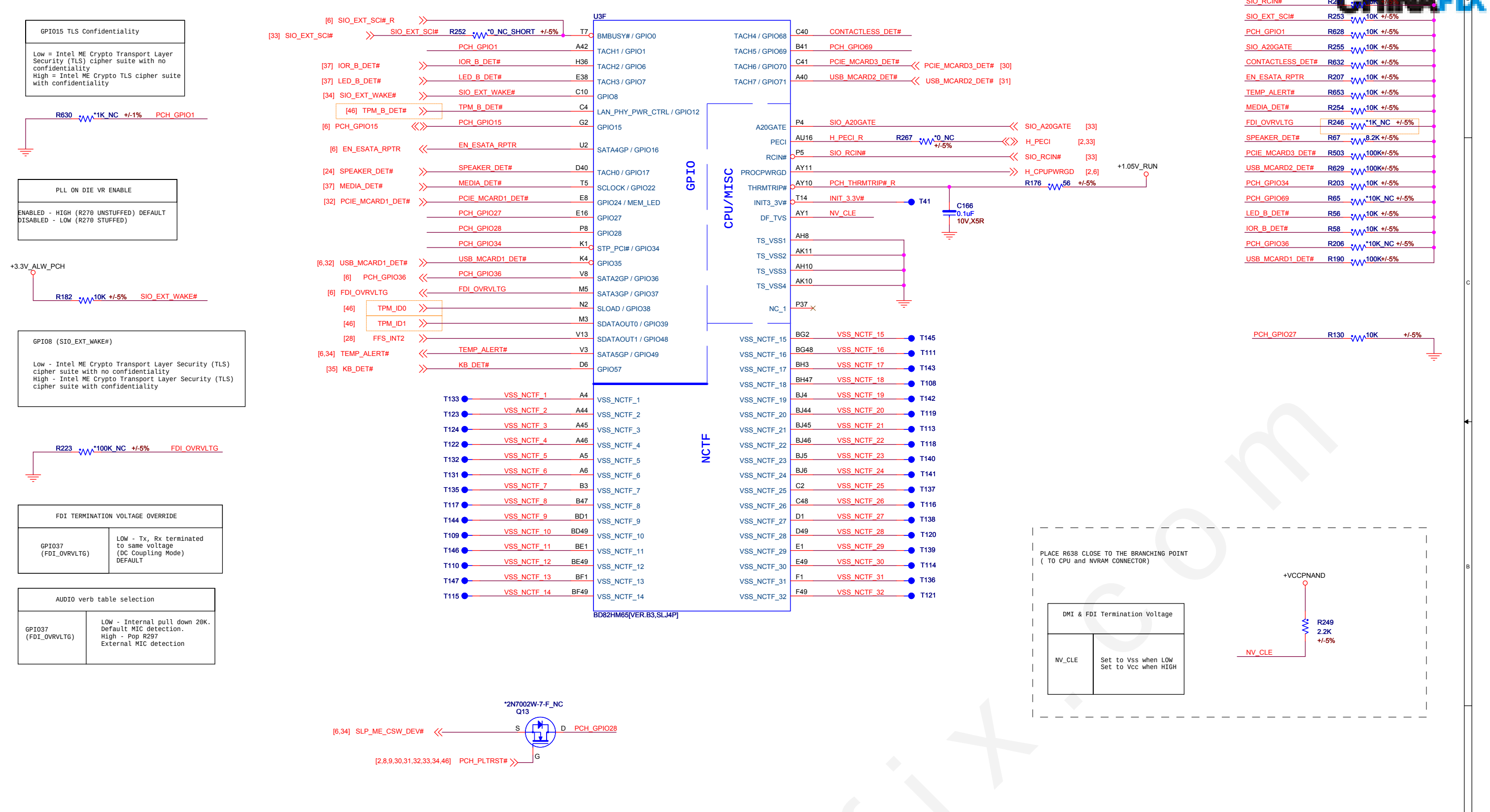
COUGAR POINT (GPIO,VSS_NCTF,RSVD)

R252
Maximum distance between resistor and PCH is 25.4mm.

1227: Pop R196 for Intel ME setting



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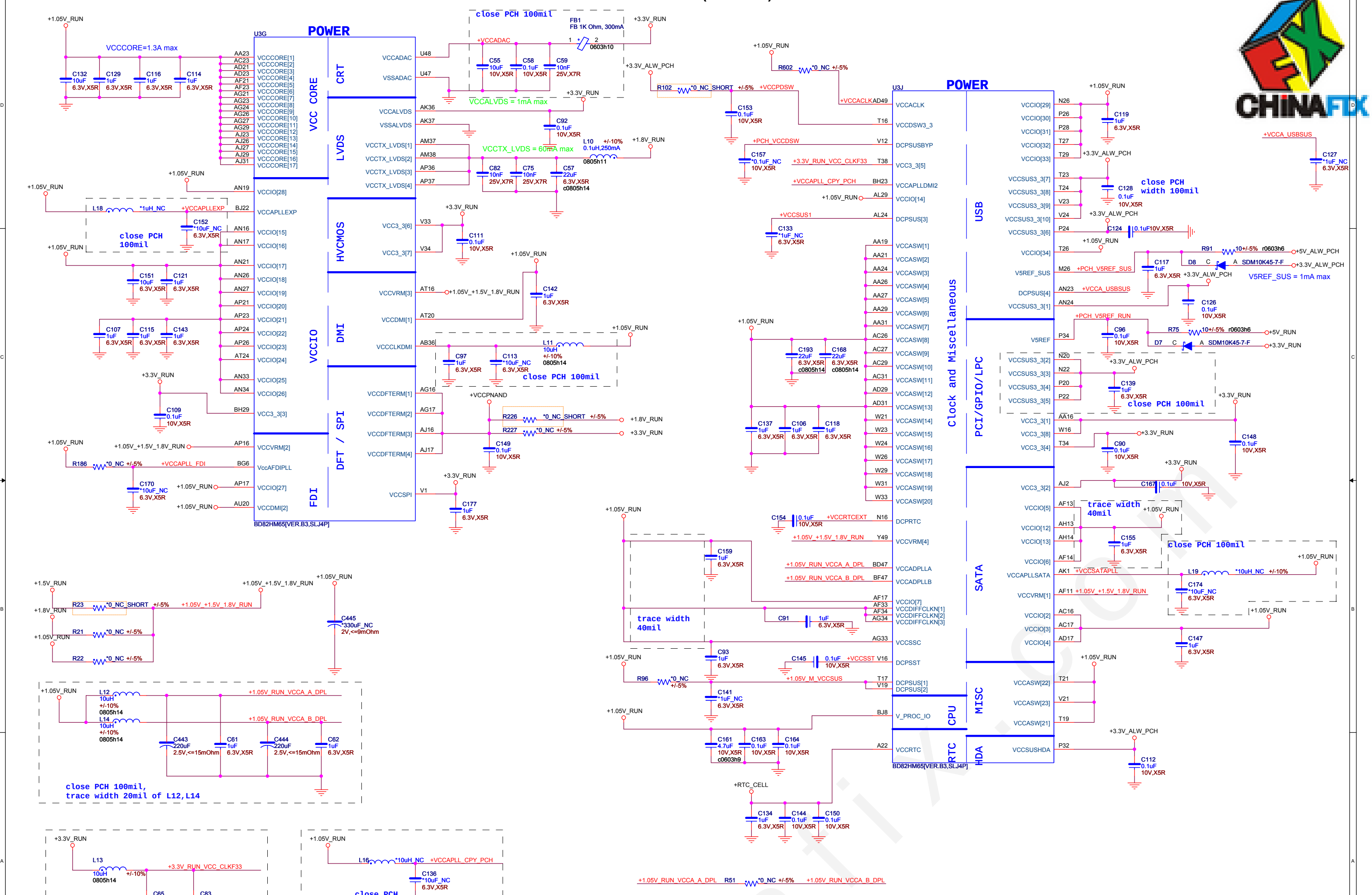
Title	11 -- CBT 5/7 (GPIO, CPU)	
Size	Document Number: KRUG 15" UMA	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 11 of 69	

COGAR POINT (POWER)



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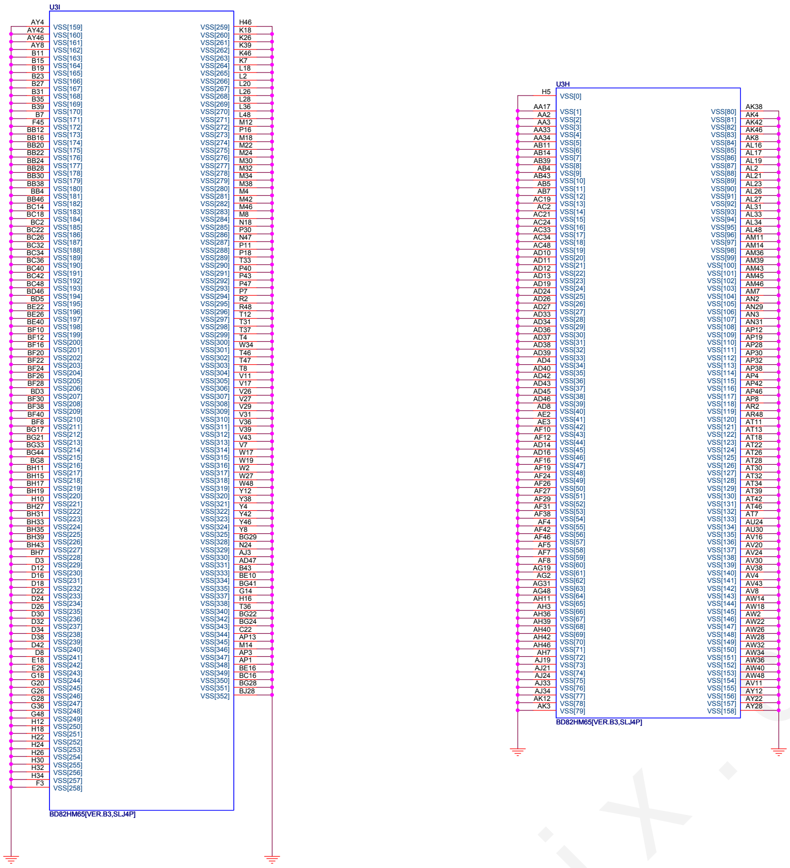
Title	12 -- CBT 6/7 (POWER)
Size	Document Number	Rev 1A
Date: Wednesday, February 16, 2011	Sheet 12 of 69

Cougar Point (GND)



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Title	13 -- CBT 7/7 (GND)	
Size	Document Number: KRUG 15" UMA	Rev: 1A
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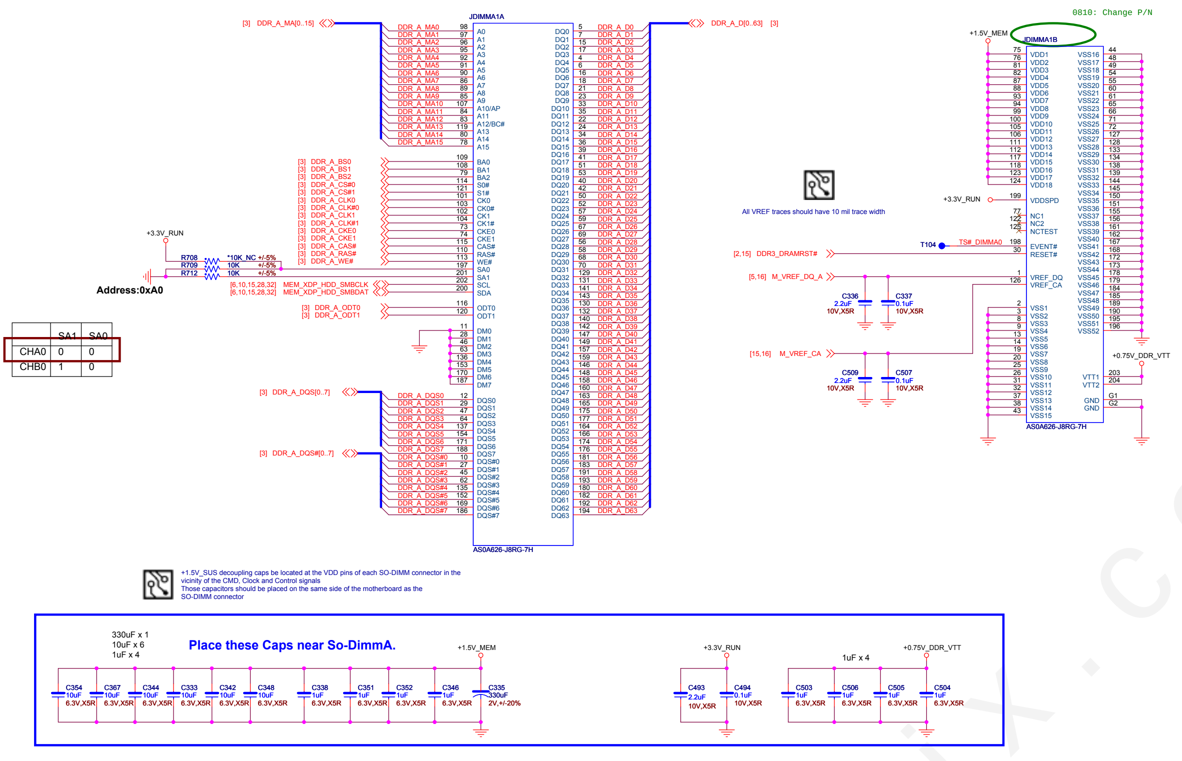
DDR3 Length Matching Formulas		
Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



	SA1	SA0
CHA0	0	0
CHB0	1	0

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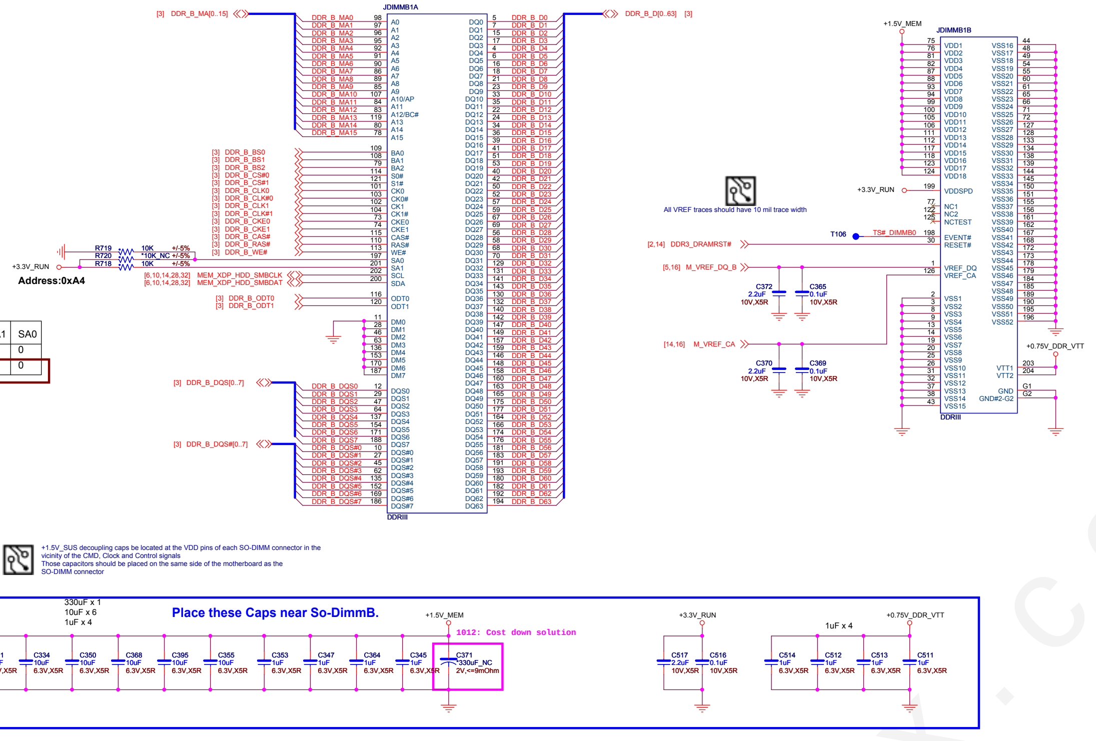
Title: 14 -- SODIMM-204P_JDIMM A

Size | Document Number: KRUG 15" UMA | Rev: 1A

Date: Wednesday, February 16, 2011 | Sheet 14 of 69

DDR3 Length Matching Formulas

Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



	SA1	SA0
CHA0	0	0
CHB0	1	0

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Title	15 -- SODIMM-204P_JDIMMB	
Size	Document Number: KRUG 15" UMA	Rev: 1A
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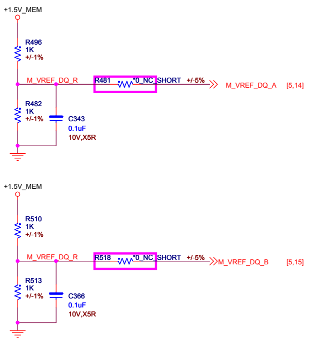
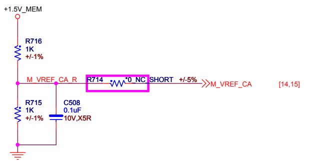
M1: Fixed SO-DIMM VREF_DQ (Default)

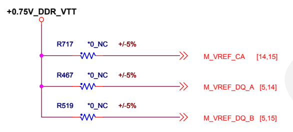


For SO-DIMM VREF_DQ

M2: Programmable SODIMM VREFDQ



For SO-DIMM VREF_CA



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Title	16 -- DDR3 VREF	
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Blank Page

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Title: 17 -- Blank Page (GPU)		
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Blank Page

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Title	19 -- Blank Page (GPU)	
Size	Document Number KRUG 15" UMA	Rev 1A
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Blank Page

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Title	20 -- Blank Page (GPU)
Size	Document Number: KRUG 15" UMA — Rev: 1A
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Blank Page

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Title	22 -- Blank Page (GPU)
Size	Document Number: KRUG 15" UMA — Rev 1A
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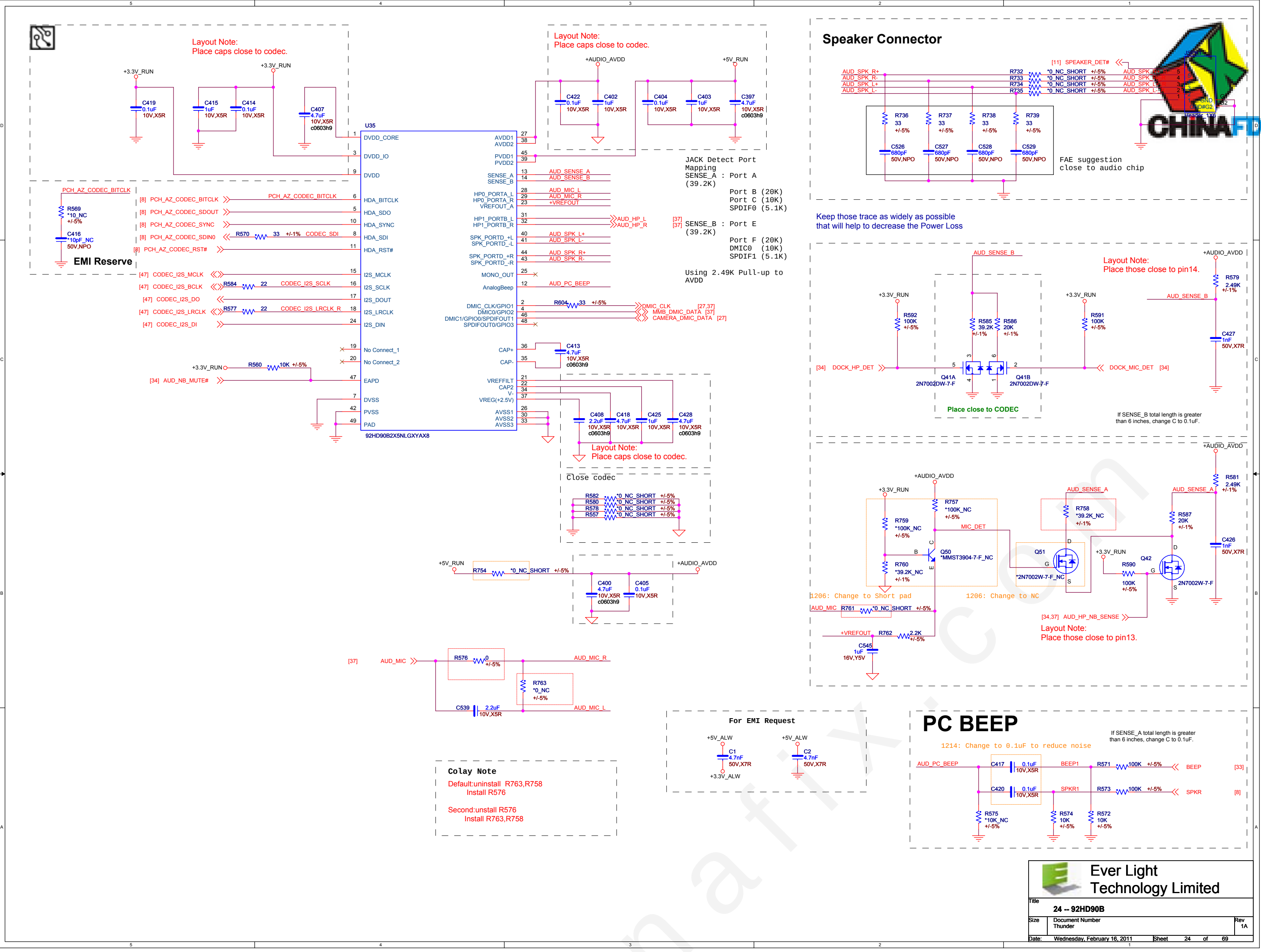
Blank Page


Layout Note:
Place caps close to codec.
EMI Reserve
U35
92HD90B2X5NLGXYAX8
JACK Detect Port Mapping
SENSE_A : Port A (39.2K)
Port B (20K)
Port C (10K)
SPDIF0 (5.1K)
SENSE_B : Port E (39.2K)
Port F (20K)
DMIC0 (10K)
SPDIF1 (5.1K)
Using 2.49K Pull-up to AVDD
Close codec
Speaker Connector
FAE suggestion close to audio chip
Keep those trace as widely as possible that will help to decrease the Power Loss
Layout Note:
Place those close to pin14.
Place close to CODEC
If SENSE_B total length is greater than 6 inches, change C to 0.1uF.
1206: Change to Short pad
1206: Change to NC
Layout Note:
Place those close to pin13.
For EMI Request
PC BEEP
1214: Change to 0.1uF to reduce noise
If SENSE_A total length is greater than 6 inches, change C to 0.1uF.
Colay Note
Default:uninstall R763,R758
Install R576
Second:unstall R576
Install R763,R758
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24 -- 92HD90B
Thunder
Wednesday, February 16, 2011
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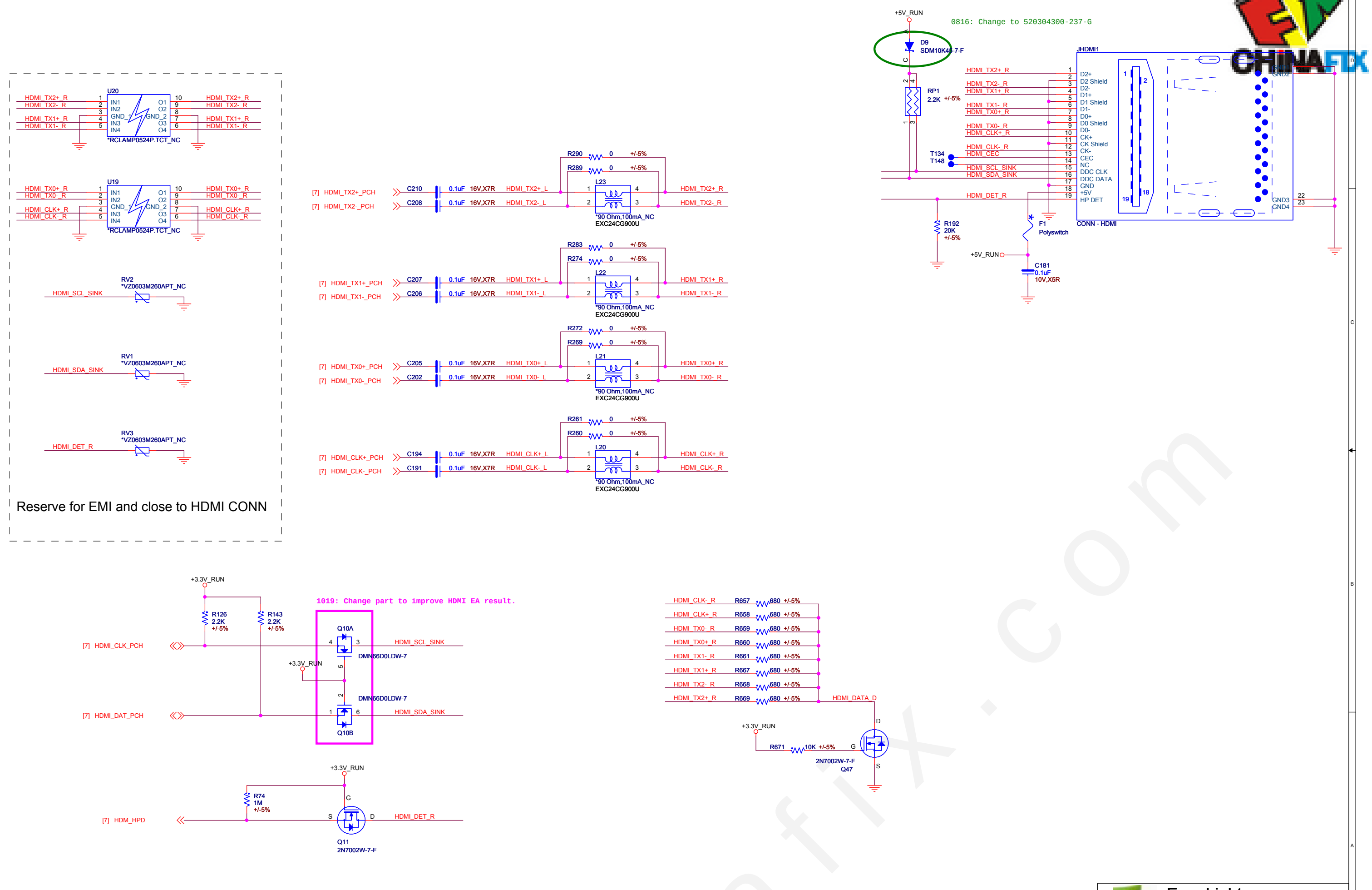
1A

HDMI CONN



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Title	25 -- HDMI		
Size	Document Number: KRUG 15" UMA		Rev: 1A
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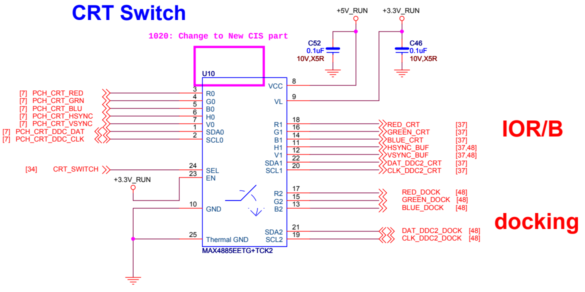
CRT Switch



CRT Switch table

SEL	VGA signals	Switch
L	RGB[0] = RGB[1] SDA[0] = SDA[1] SCL[0] = SCL[1]	IOR/B
H	RGB[0] = RGB[2] SDA[0] = SDA[2] SCL[0] = SCL[2]	DOCK

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Title: 26 -- CRT & MUX

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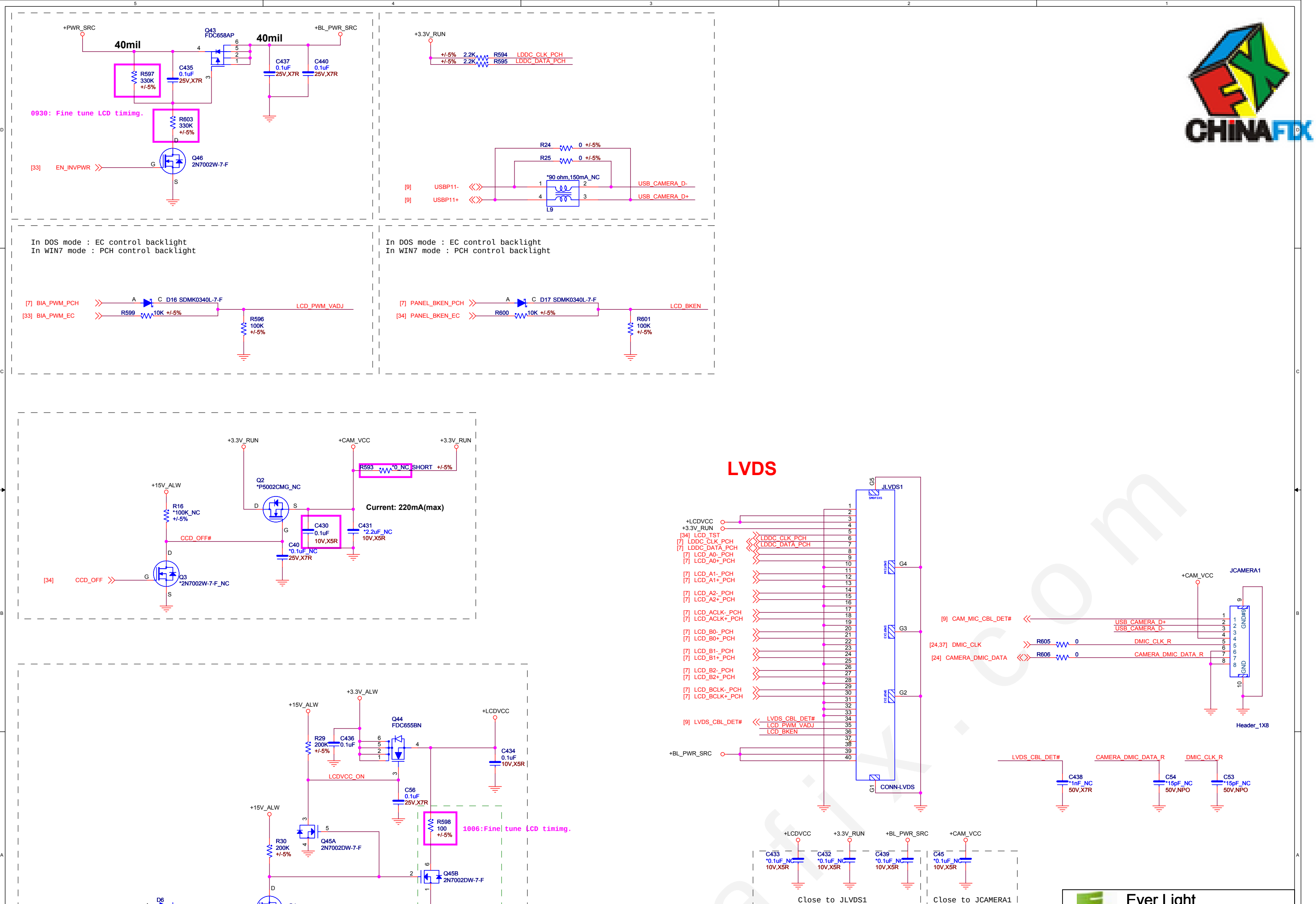

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Title	29 -- LCD,Camera,Touch Conn	
Size	Document Number: Thunder	Rev: 1A
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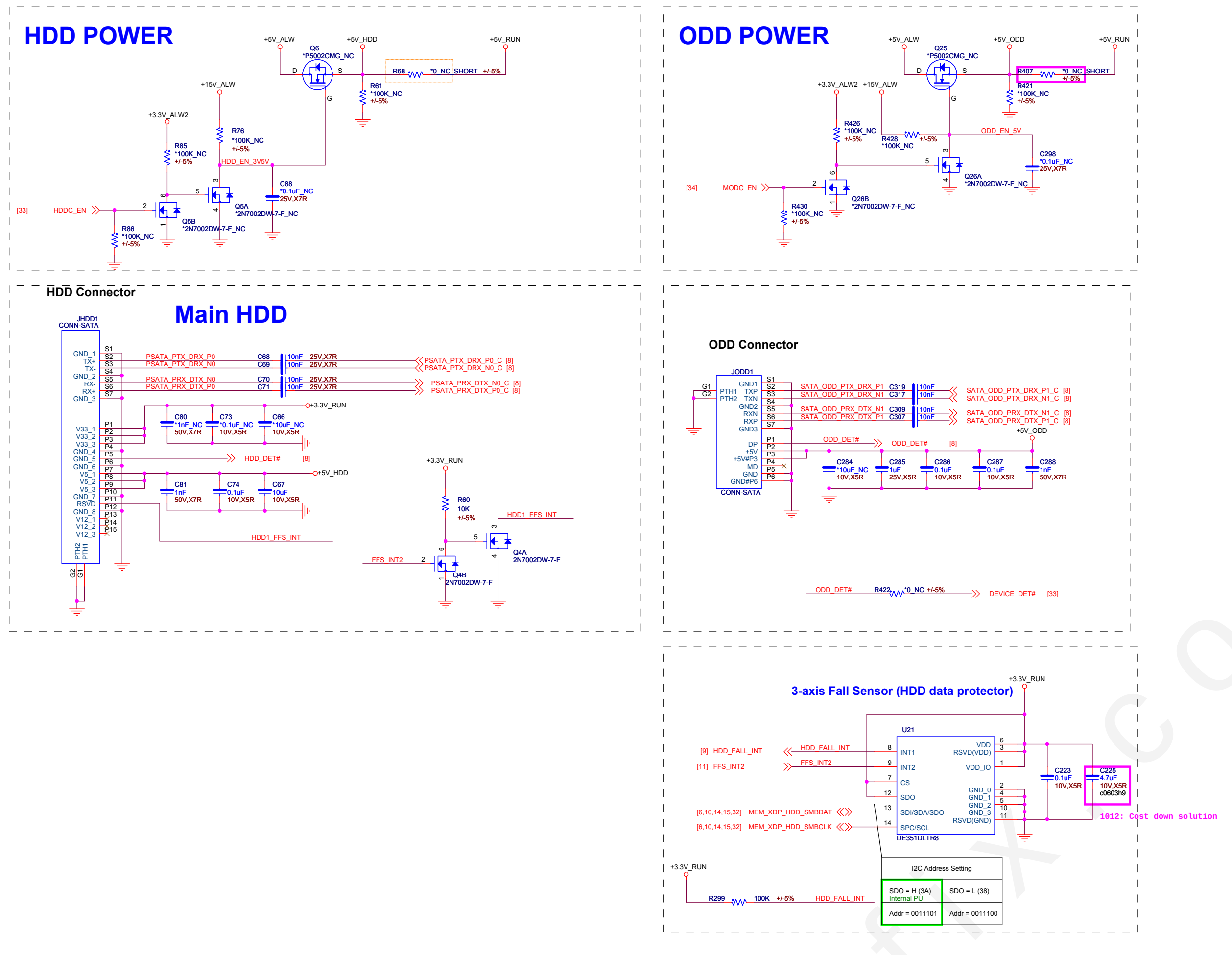

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Title	28 -- HDD, ODD, G-SENSOR	
Size	Document Number: KRUG 15" UMA	Rev: 1A
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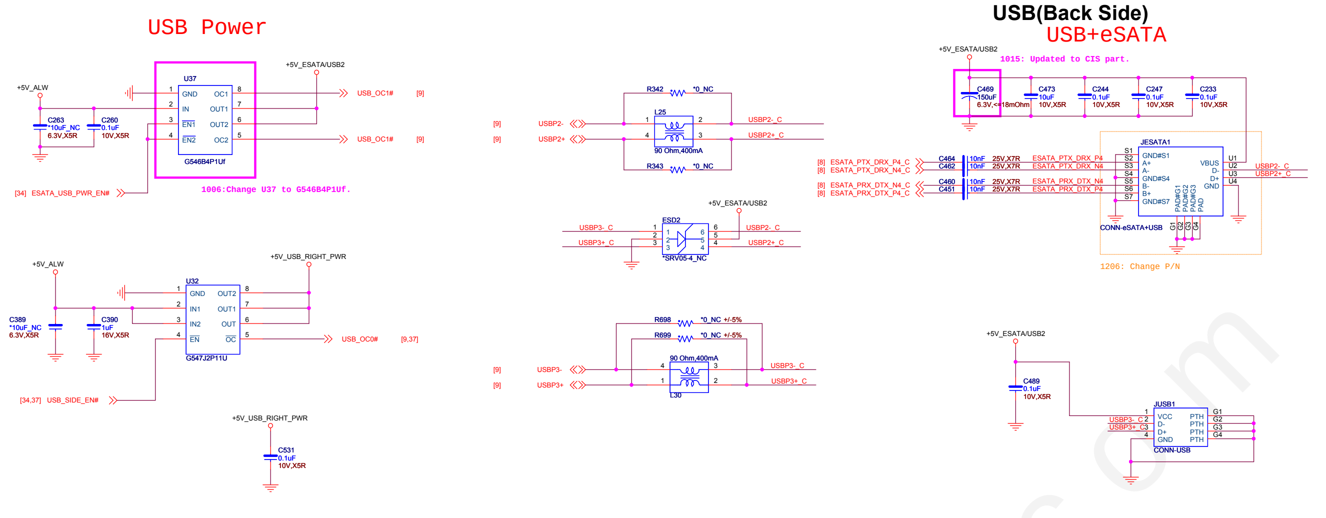

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Title	29 -- eSATA/USB, USB x 1
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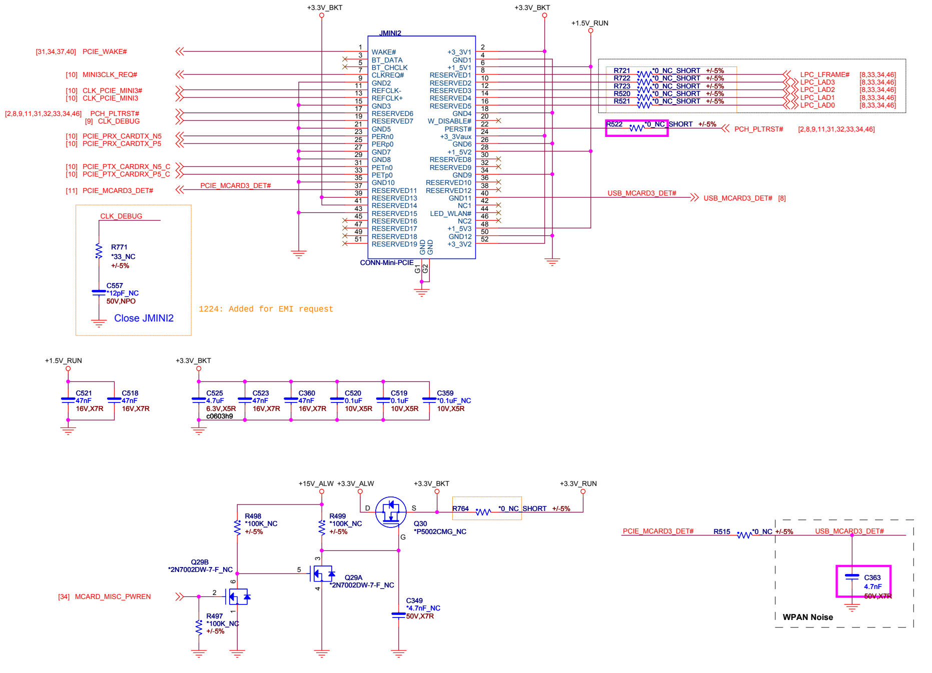
3rd MiniCard connector (Flash, half size)

MiniCard connector



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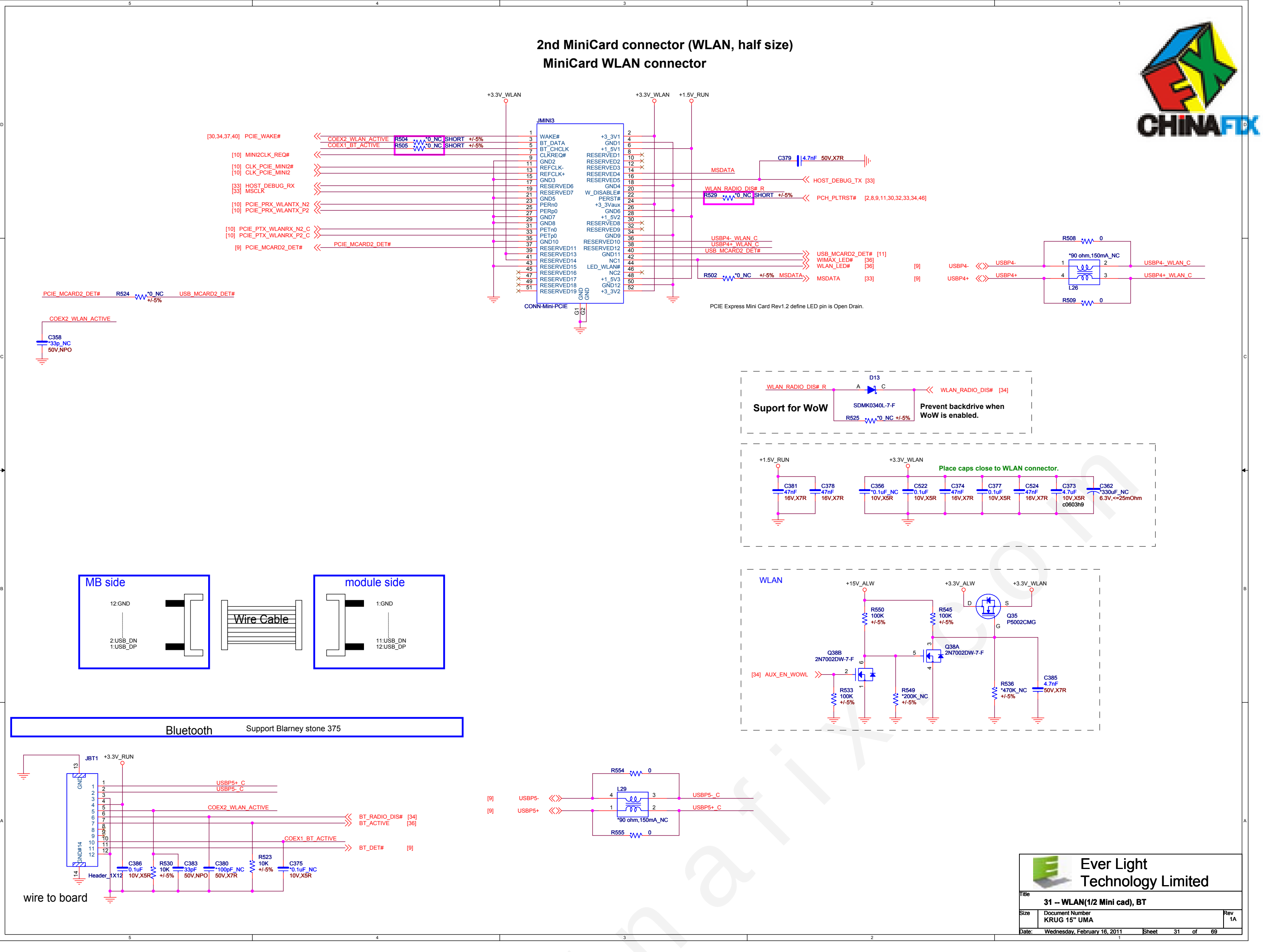
Title	30 -- Flash /PP(1/2Mini cad)		
Size	Document Number KRUG 15" UMA		Rev 1A
Date: Wednesday, February 16, 2011	Sheet 30 of 69		


2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector
JMINI3
CONN-Mini-PCIE
PCIE Express Mini Card Rev1.2 define LED pin is Open Drain.
Suport for WoW
Prevent backdrive when WoW is enabled.
Place caps close to WLAN connector.
WLAN
MB side
module side
Wire Cable
Bluetooth
Support Blarney stone 375
wire to board
JBT1
Header_1X12
Ever Light Technology Limited
Title
31 -- WLAN(1/2 Mini cad), BT
Size
Document Number
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1A
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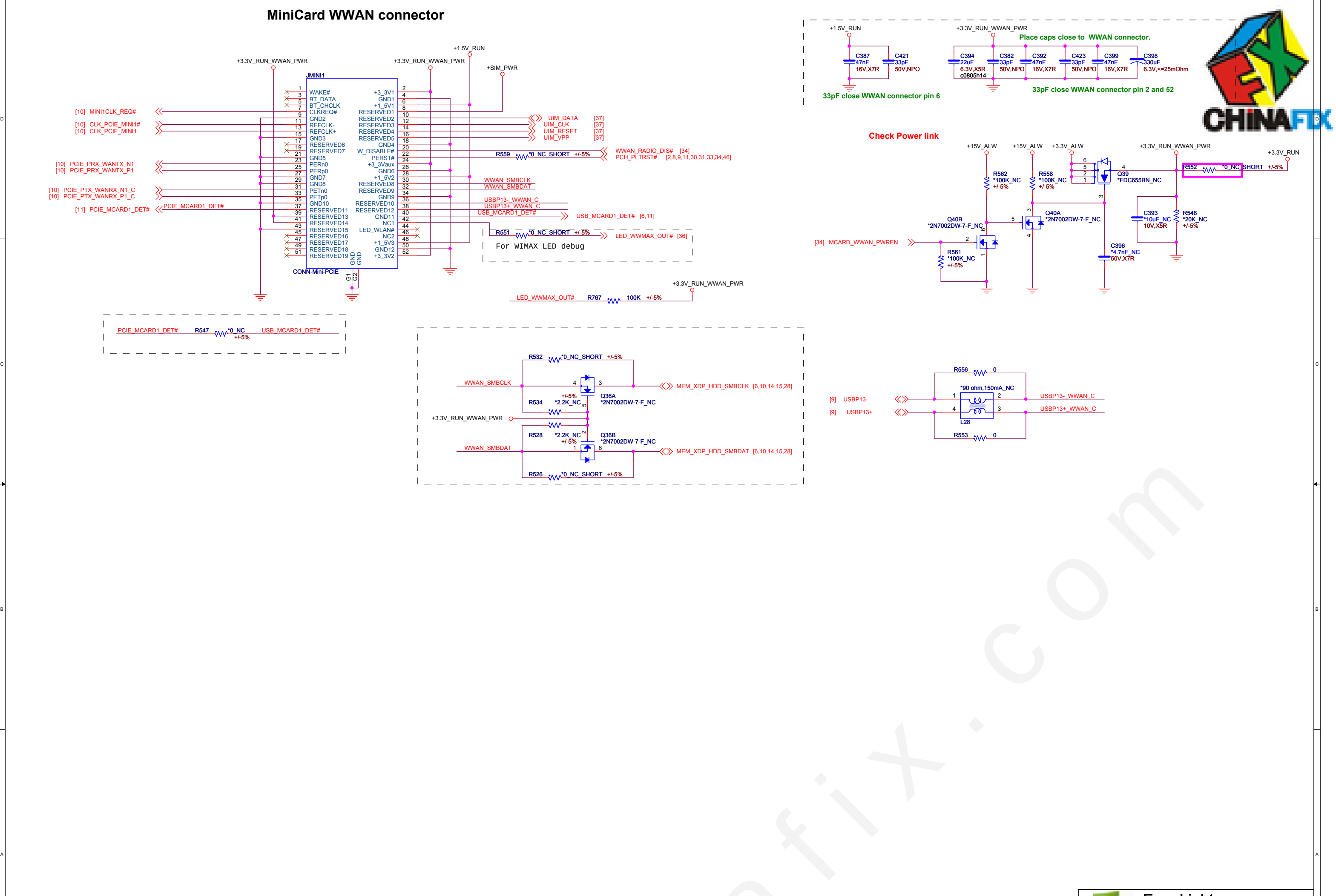
MiniCard WWAN connector



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Title	32 -- WWAN+ SIM+MUX
Size	Document Number: KRUG 15" UMA
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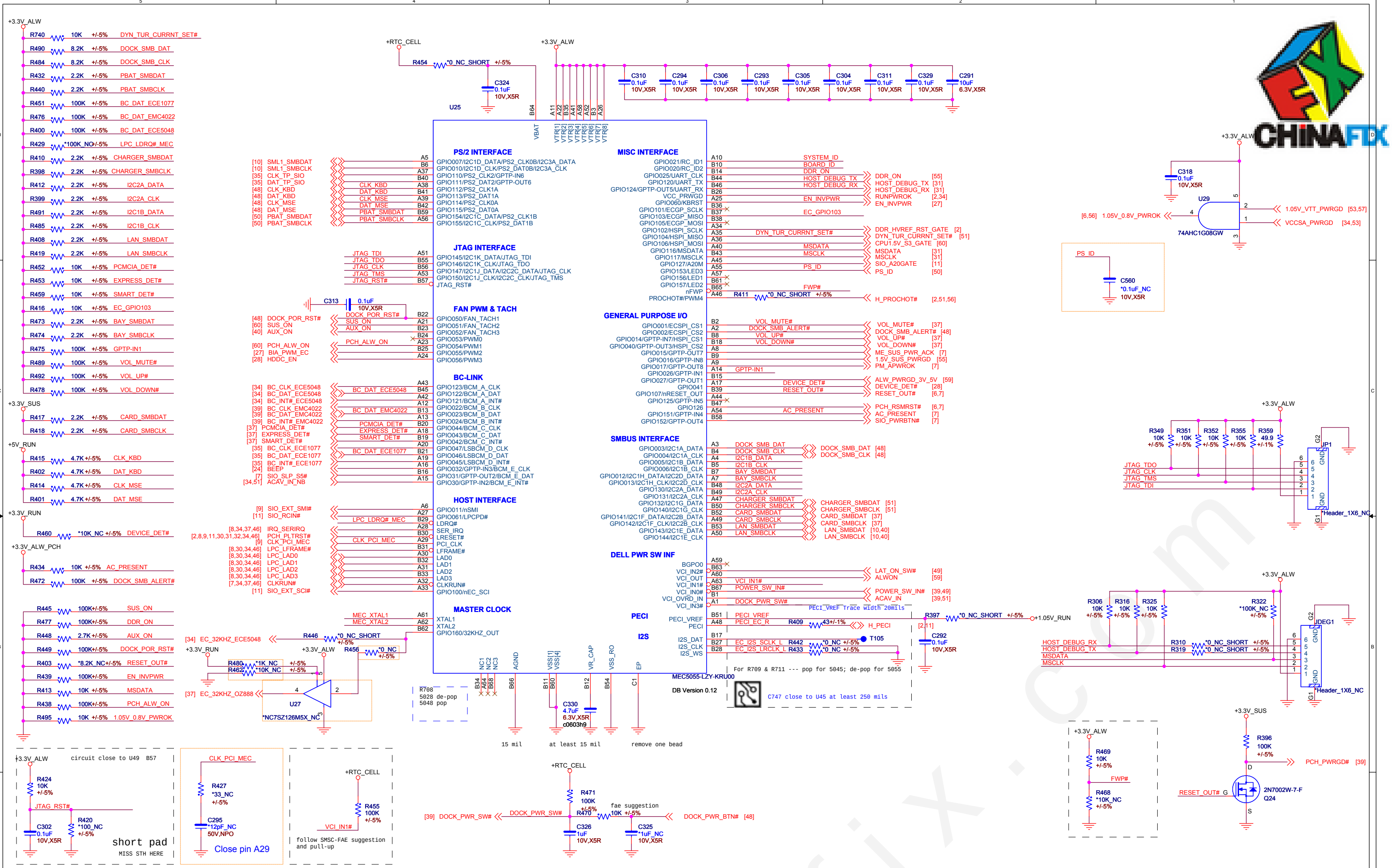
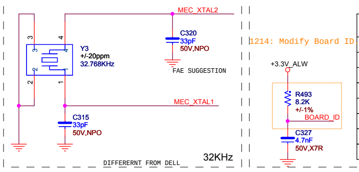
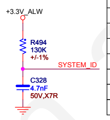




Cap Value (C327)	Resistor Value (R493) +/- 5%	Board Ver
4700PF	240K	SSI (X00)
4700PF	130K	PT (X01)
4700PF	62K/33K	ST (X02)
4700PF	8.2K/4.3K	QT(A00)
4700PF	2K	(X04)
4700PF	1K	(A00)



Cap Value (C328)	Resistor Value (R494) +/- 5%	System ID
4700PF	240K	Krug 14
4700PF	130K	Krug 15
4700PF	62K	System 3
4700PF	33K	System 4
4700PF	8.2K	System 5
4700PF		
4700PF		
4700PF		

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Title	33 – SIO (MEC5055)	
Size	Document Number Thunder	Rev 1A
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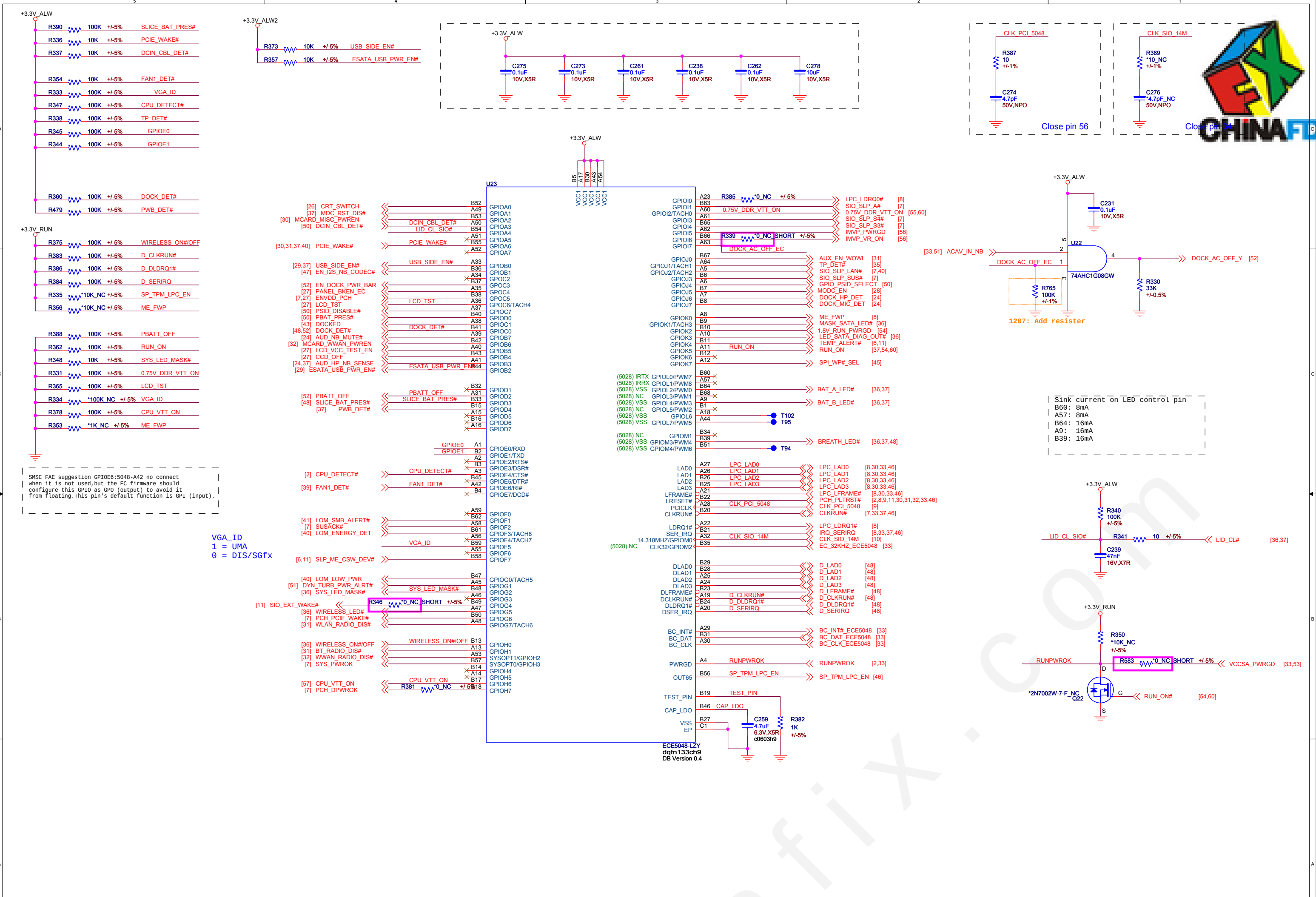

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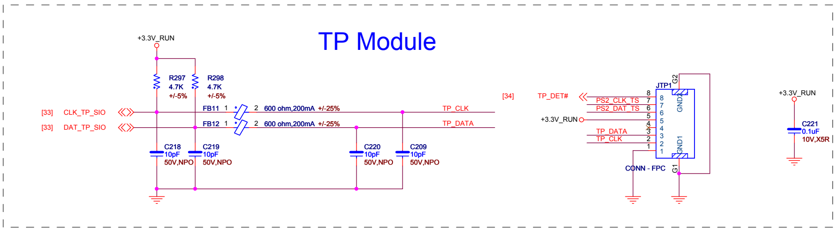
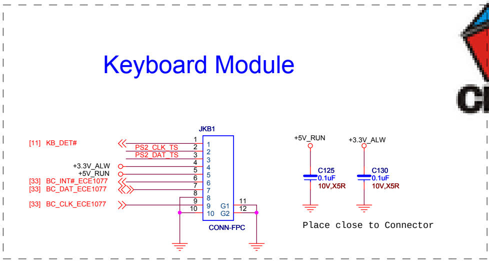
Title
34 -- SIO (ECE5048)

Size	Document Number	Rev
	Thunder	1A

Date: Wednesday, February 16, 2011 Sheet 34 of 69





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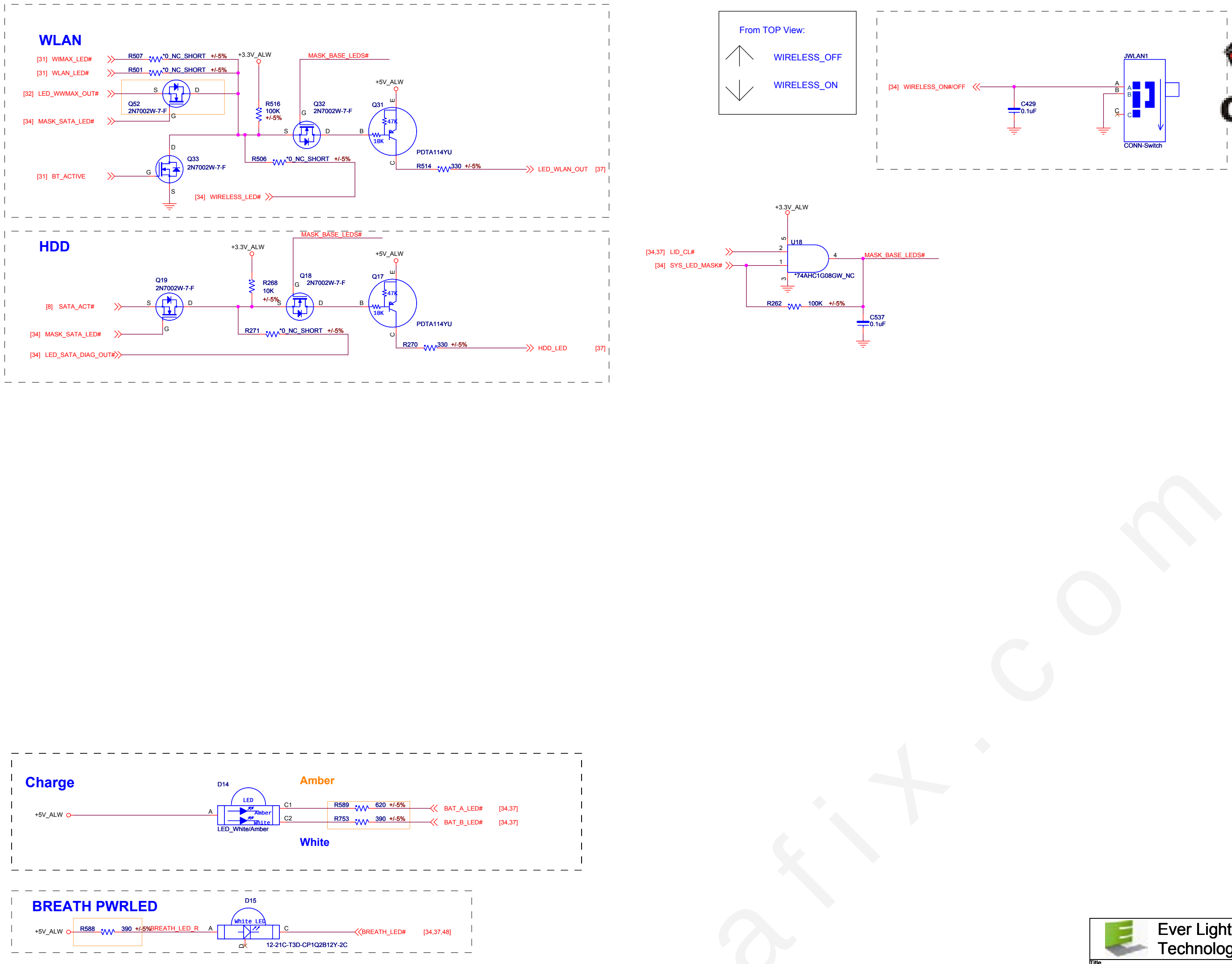
Title	35 -- KB+TP	
Size	Document Number KRUG 15" UMA	Rev 1A
Date:	Wednesday, February 16, 2011	Sheet 35 of 69



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Title	36 -- LED+Control, Wirele
Size	Document Number: Thunder
Rev	1A
Date:	Wednesday, February 16, 2011
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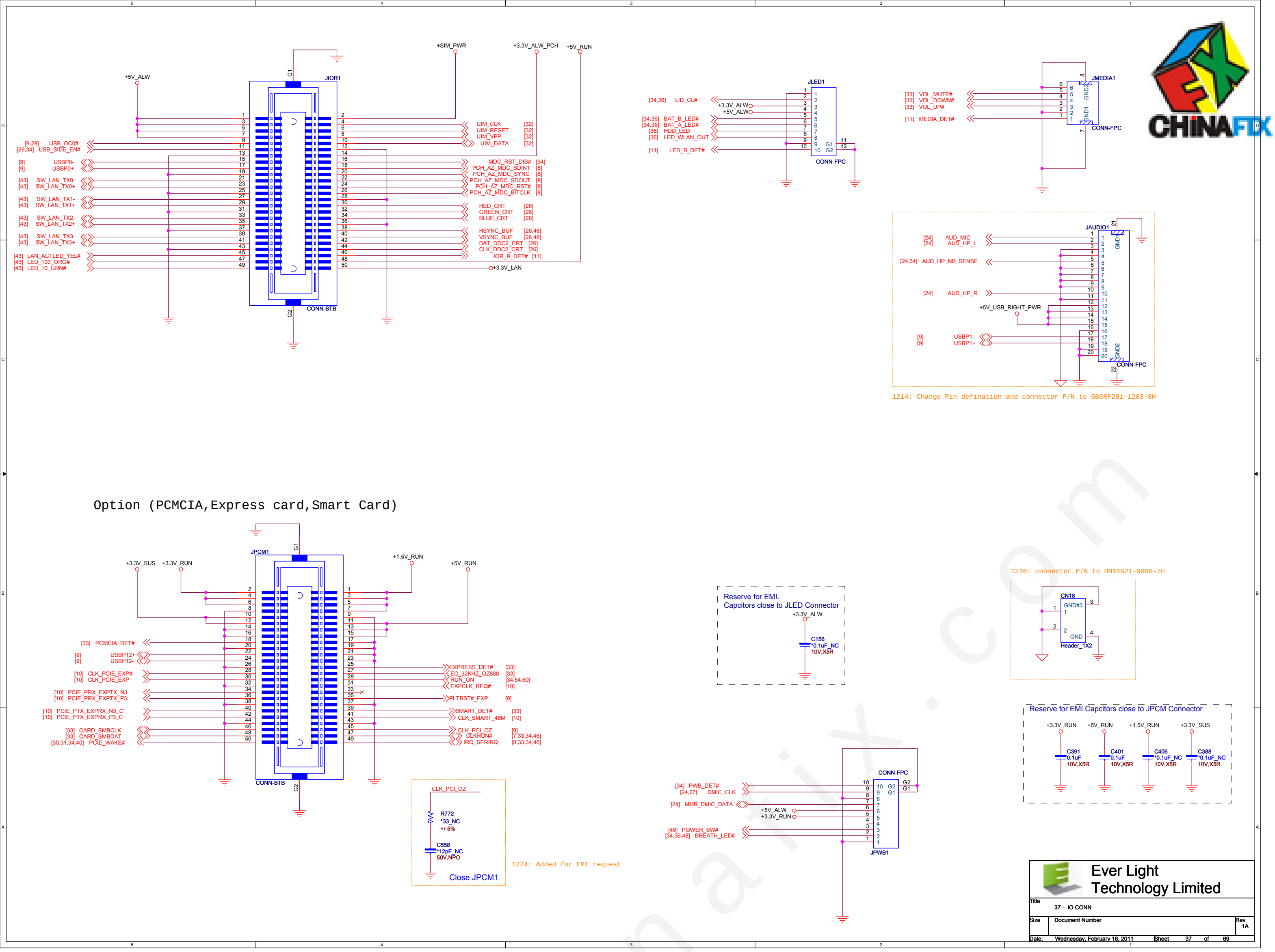
JIOR1
CONN-BTB
+5V_ALW
+SIM_PWR
+3.3V_ALW_PCH
+5V_RUN
USB_OC0#
USB_SIDE_EN#
USBP0-
USBP0+
SW_LAN_TX0-
SW_LAN_TX0+
SW_LAN_TX1-
SW_LAN_TX1+
SW_LAN_TX2-
SW_LAN_TX2+
SW_LAN_TX3-
SW_LAN_TX3+
LAN_ACTLED_YEL#
LED_100_ORG#
LED_10_GRN#
UIM_CLK
UIM_RESET
UIM_VPP
UIM_DATA
MDC_RST_DIS#
PCH_AZ_MDC_SDIN1
PCH_AZ_MDC_SYNC
PCH_AZ_MDC_SDOUT
PCH_AZ_MDC_RST#
PCH_AZ_MDC_BITCLK
RED_CRT
GREEN_CRT
BLUE_CRT
HSYNC_BUF
VSYNC_BUF
DAT_DDC2_CRT
CLK_DDC2_CRT
IOR_B_DET#
+3.3V_LAN
JLED1
CONN-FPC
LID_CL#
BAT_B_LED#
BAT_A_LED#
HDD_LED
LED_WLAN_OUT
LED_B_DET#
JMEDIA1
VOL_MUTE#
VOL_DOWN#
VOL_UP#
MEDIA_DET#
JAUDIO1
AUD_MIC
AUD_HP_L
AUD_HP_NB_SENSE
AUD_HP_R
+5V_USB_RIGHT_PWR
USBP1-
USBP1+
1214: Change Pin defination and connector P/N to GB5RF201-1203-8H
Option (PCMCIA,Express card,Smart Card)
JPCM1
+3.3V_SUS
+3.3V_RUN
+1.5V_RUN
PCMCIA_DET#
USBP12+
USBP12-
CLK_PCIE_EXP#
CLK_PCIE_EXP
PCIE_PRX_EXPTX_N3
PCIE_PRX_EXPTX_P3
PCIE_PTX_EXPRX_N3_C
PCIE_PTX_EXPRX_P3_C
CARD_SMBCLK
CARD_SMBDAT
PCIE_WAKE#
EXPRESS_DET#
EC_32KHZ_OZ888
RUN_ON
EXPCLK_REQ#
PLTRST#_EXP
SMART_DET#
CLK_SMART_48M
CLK_PCI_OZ
CLKRUN#
IRQ_SERIRQ
R772
*33_NC
+/-5%
C558
*12pF_NC
50V,NPO
Close JPCM1
1224: Added for EMI request
Reserve for EMI.
Capcitors close to JLED Connector
C156
*0.1uF_NC
10V,X5R
1216: connector P/N to HN14021-0000-7H
CN18
Header_1X2
Reserve for EMI.Capcitors close to JPCM Connector
C391
C401
C406
C388
JPWB1
PWB_DET#
DMIC_CLK
MMB_DMIC_DATA
POWER_SW#
BREATH_LED#
Ever Light
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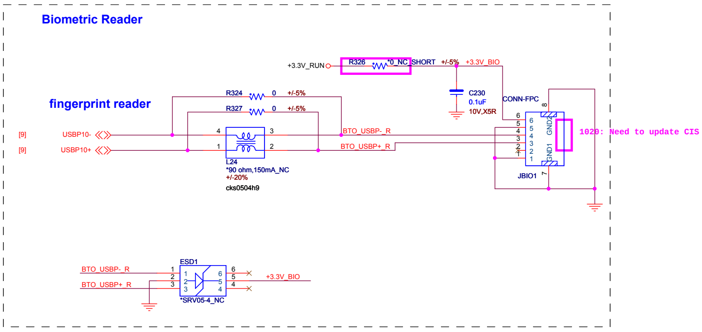
Title
37 -- IO CONN
Size
Document Number
Rev
1A
Date: Wednesday, February 16, 2011
Sheet 37 of 69



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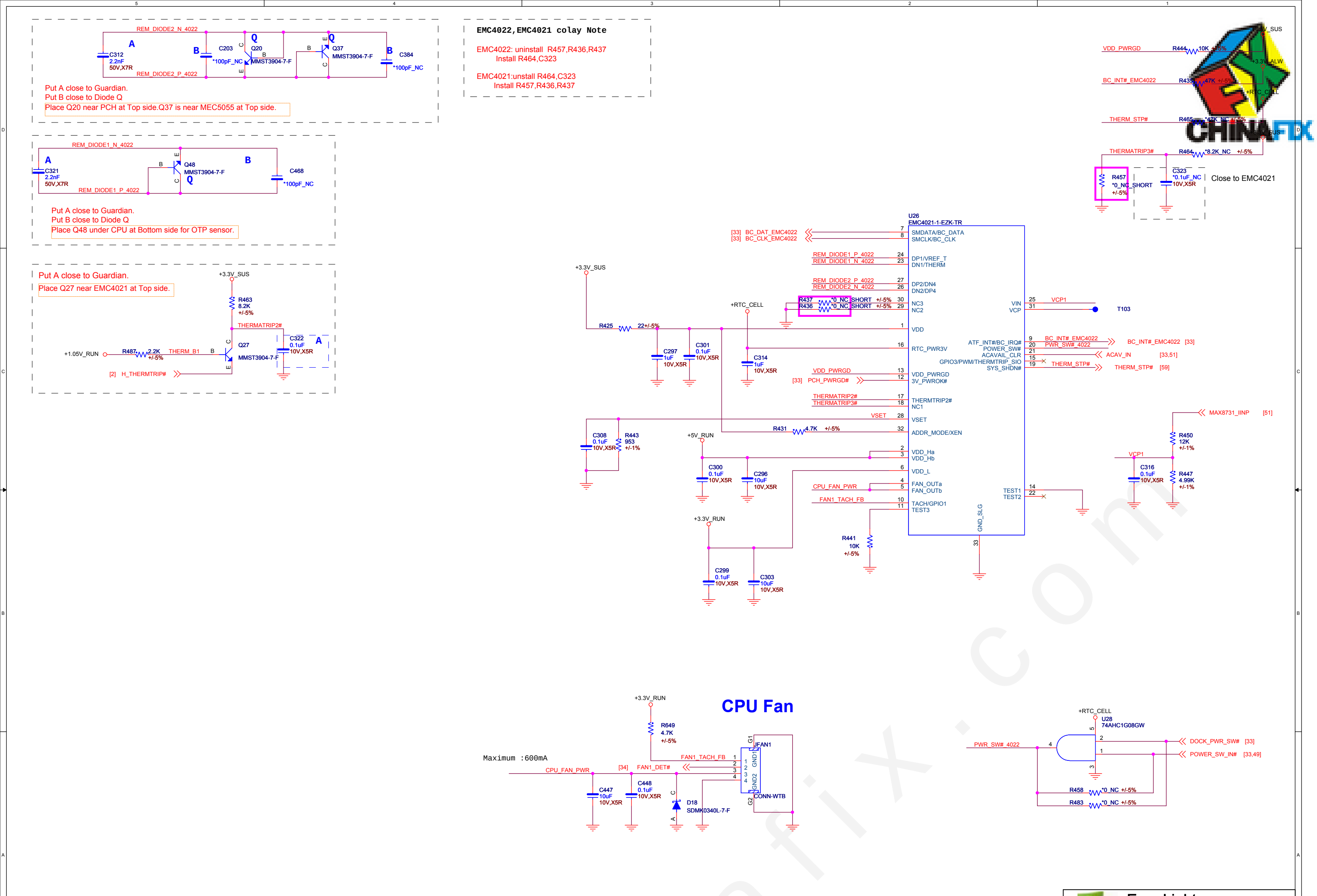
Title	41 -- BIO reader	
Size	Document Number	Rev 1A
Date: Wednesday, February 16, 2011	Sheet 38 of 69	



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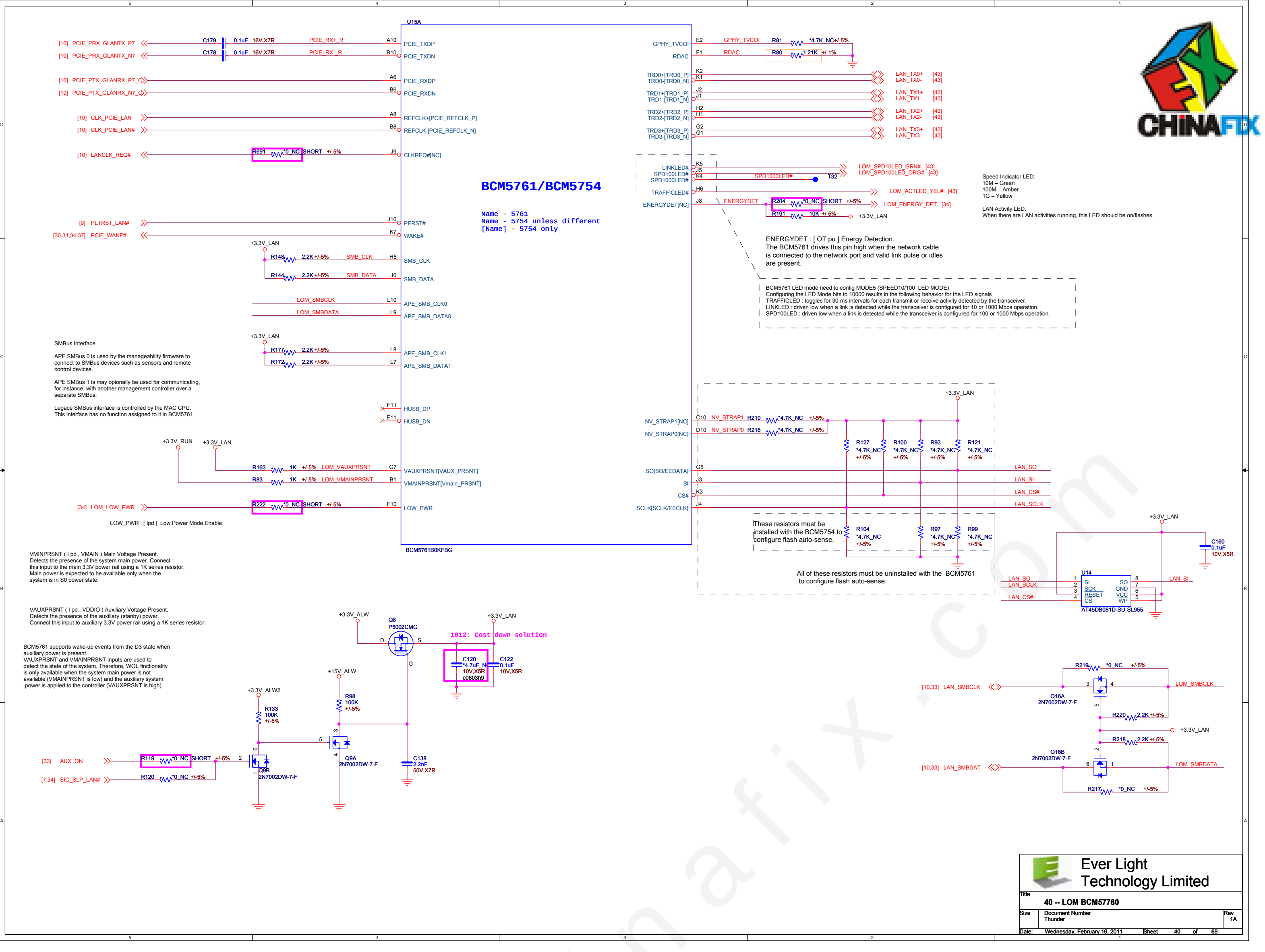
Title: 39 -- Thermal 4021 & FAN x 1

Size | Document Number: Thunder | Rev: 1A

Date: Wednesday, February 16, 2011 | Sheet 39 of 69


BCM5761/BCM5754
Name - 5761
Name - 5754 unless different
[Name] - 5754 only
U15A
BCM5761B0KFBG
PCIE_TXDP
PCIE_TXDN
PCIE_RXDP
PCIE_RXDN
REFCLK+[PCIE_REFCLK_P]
REFCLK-[PCIE_REFCLK_N]
CLKREQ#[NC]
PERST#
WAKE#
SMB_CLK
SMB_DATA
APE_SMB_CLK0
APE_SMB_DATA0
APE_SMB_CLK1
APE_SMB_DATA1
HUSB_DP
HUSB_DN
VAUXPRSNT[VAUX_PRSNT]
VMAINPRSNT[Vmain_PRSNT]
LOW_PWR
GPHY_TVCOI
RDAC
TRD0+[TRD0_P]
TRD0-[TRD0_N]
TRD1+[TRD1_P]
TRD1-[TRD1_N]
TRD2+[TRD2_P]
TRD2-[TRD2_N]
TRD3+[TRD3_P]
TRD3-[TRD3_N]
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
ENERGYDET[NC]
NV_STRAP1[NC]
NV_STRAP0[NC]
SO[SO/EEDATA]
SI
CS#
SCLK[SCLK/EECLK]
[10] PCIE_PRX_GLANTX_P7
[10] PCIE_PRX_GLANTX_N7
[10] PCIE_PTX_GLANRX_P7_C
[10] PCIE_PTX_GLANRX_N7_C
[10] CLK_PCIE_LAN
[10] CLK_PCIE_LAN#
[10] LANCLK_REQ#
[9] PLTRST_LAN#
[30,31,34,37] PCIE_WAKE#
[34] LOM_LOW_PWR
C179 0.1uF 16V,X7R PCIE_RX+_R
C178 0.1uF 16V,X7R PCIE_RX-_R
R691 *0_NC SHORT +/-5%
R222 *0_NC SHORT +/-5%
R148 2.2K +/-5% SMB_CLK
R144 2.2K +/-5% SMB_DATA
LOM_SMBCLK
LOM_SMBDATA
R177 2.2K +/-5%
R172 2.2K +/-5%
R163 1K +/-5% LOM_VAUXPRSNT
R83 1K +/-5% LOM_VMAINPRSNT
+3.3V_LAN
+3.3V_RUN
GPHY_TVCOI R81 *4.7K_NC +/-5%
RDAC R80 1.21K +/-1%
LAN_TX0+ [43]
LAN_TX0- [43]
LAN_TX1+ [43]
LAN_TX1- [43]
LAN_TX2+ [43]
LAN_TX2- [43]
LAN_TX3+ [43]
LAN_TX3- [43]
LOM_SPD10LED_GRN# [43]
LOM_SPD100LED_ORG# [43]
SPD1000LED# T32
LOM_ACTLED_YEL# [43]
ENERGYDET R204 *0_NC SHORT +/-5% LOM_ENERGY_DET [34]
R191 10K +/-5% +3.3V_LAN
Speed Indicator LED:
10M -- Green
100M -- Amber
1G -- Yellow
LAN Activity LED:
When there are LAN activities running, this LED should be on/flashes.
ENERGYDET : [OT pu] Energy Detection.
The BCM5761 drives this pin high when the network cable is connected to the network port and valid link pulse or idles are present.
BCM5761 LED mode need to config MODE5 (SPEED10/100 LED MODE)
Configuring the LED Mode bits to 10000 results in the following behavior for the LED signals
TRAFFICLED : toggles for 30-ms intervals for each transmit or receive activity detected by the transceiver.
LINKLED : driven low when a link is detected while the transceiver is configured for 10 or 1000 Mbps operation.
SPD100LED : driven low when a link is detected while the transceiver is configured for 100 or 1000 Mbps operation.
SMBus Interface
APE SMBus 0 is used by the manageability firmware to connect to SMBus devices such as sensors and remote control devices.
APE SMBus 1 is may opionally be used for communicating, for instance, with another management controller over a separate SMBus.
Legace SMBus interface is controlled by the MAC CPU. This interface has no function assigned to it in BCM5761.
NV_STRAP1 R210 *4.7K_NC +/-5%
NV_STRAP0 R216 *4.7K_NC +/-5%
R127 *4.7K_NC +/-5%
R100 *4.7K_NC +/-5%
R93 *4.7K_NC +/-5%
R121 *4.7K_NC +/-5%
R104 *4.7K_NC +/-5%
R97 *4.7K_NC +/-5%
R99 *4.7K_NC +/-5%
LAN_SO
LAN_SI
LAN_CS#
LAN_SCLK
These resistors must be installed with the BCM5754 to configure flash auto-sense.
All of these resistors must be uninstalled with the BCM5761 to configure flash auto-sense.
U14
AT45DB081D-SU-SL955
SI SO SCK GND RESET VCC CS WP
C160 0.1uF 10V,X5R
LOW_PWR : [Ipd] Low Power Mode Enable
VMINPRSNT (I pd , VMAIN) Main Voltage Present.
Detects the presence of the system main power. Connect this input to the main 3.3V power rail using a 1K series resistor.
Main power is expected to be available only when the system is in S0 power state.
VAUXPRSNT (I pd , VDDIO) Auxiliary Voltage Present.
Detects the presence of the auxiliary (stanby) power.
Connect this input to auxiliary 3.3V power rail using a 1K series resistor.
BCM5761 supports wake-up events from the D3 state when auxiliary power is present.
VAUXPRSNT and VMAINPRSNT inputs are used to detect the state of the system. Therefore, WOL finctionality is only available when the system main power is not available (VMAINPRSNT is low) and the auxiliary system power is applied to the controller (VAUXPRSNT is high).
+3.3V_ALW
Q8 P5002CMG
1012: Cost down solution
C120 *4.7uF_NC 10V,X5R c0603h9
C122 0.1uF 10V,X5R
+15V_ALW
R98 100K +/-5%
+3.3V_ALW2
R133 100K +/-5%
Q9A 2N7002DW-7-F
Q9B 2N7002DW-7-F
C138 2.2nF 50V,X7R
[33] AUX_ON R119 *0_NC SHORT +/-5%
[7,34] SIO_SLP_LAN# R120 *0_NC +/-5%
[10,33] LAN_SMBCLK
[10,33] LAN_SMBDAT
R219 *0_NC +/-5%
Q16A 2N7002DW-7-F
Q16B 2N7002DW-7-F
R220 2.2K +/-5%
R218 2.2K +/-5%
R217 *0_NC +/-5%
LOM_SMBCLK
LOM_SMBDATA
Ever Light Technology Limited
Title
40 -- LOM BCM57760
Size
Document Number
Thunder
Rev
1A
Date: Wednesday, February 16, 2011
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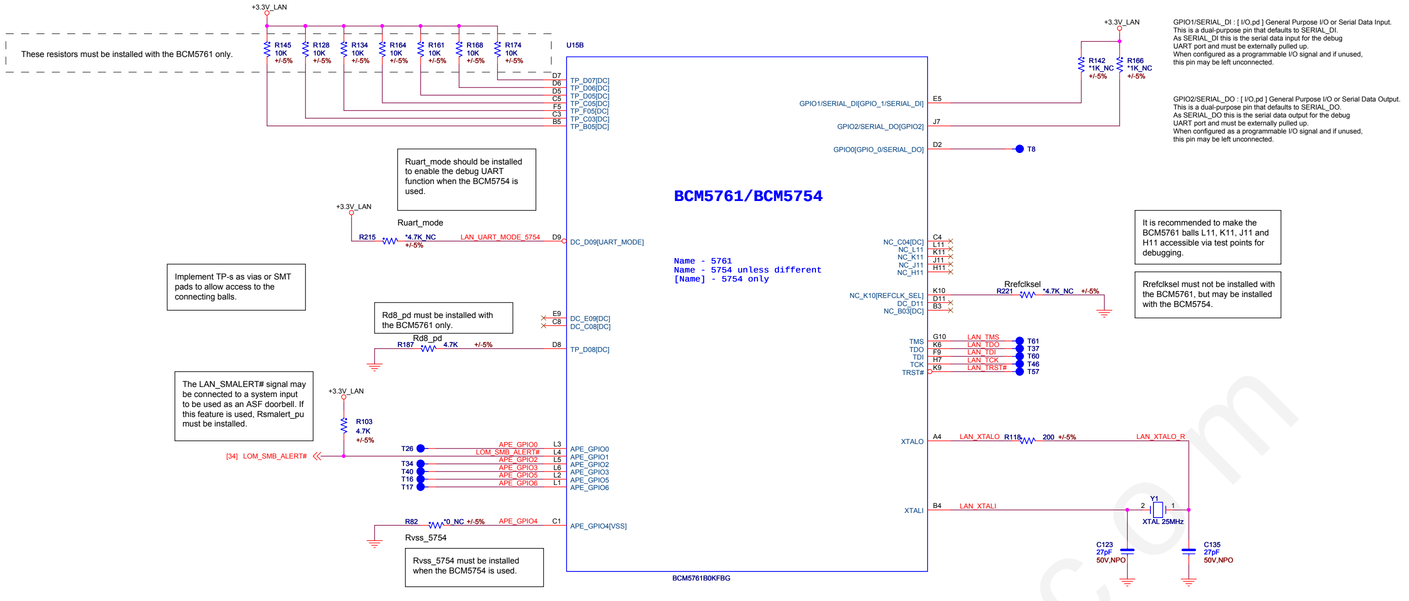
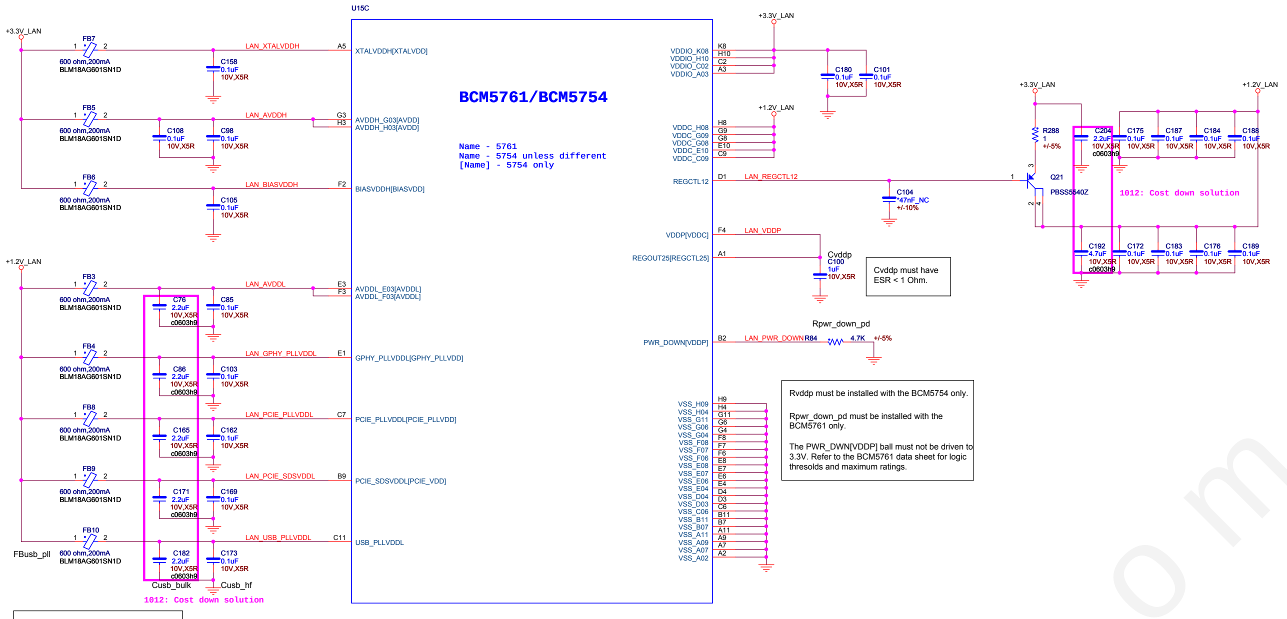


	Ever Light Technology Limited
Title	41 -- BCM5761_TPM/GPIO
Size / Document Number	KRUG 15" UMA
Rev	1A
Date:	Wednesday, February 16, 2011
Sheet	41 of 69



If the BCM5761 is installed, Fusb_pll, Cusb_bulk and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, Fusb_pll, Cusb_bulk and Cusb_hf may be uninstalled.

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Title	42 -- BCM5761_Power	
Size	Document Number: KRUG 15" UMA	Rev 1A
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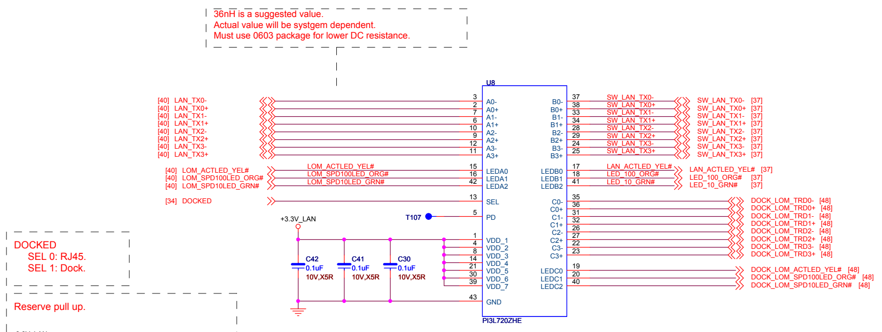

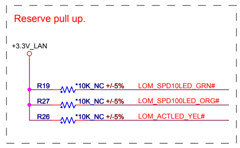

LAN Switch table

DOCKED(SEL)	LOM signals	LED SIGNALS	Switch
L	Ax to Bx	LEDAx to LEDBx	MB
H	Ax to Cx	LEDAx to LEDCx	DOCK

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Title	43 -- RJ45 MUX Switch
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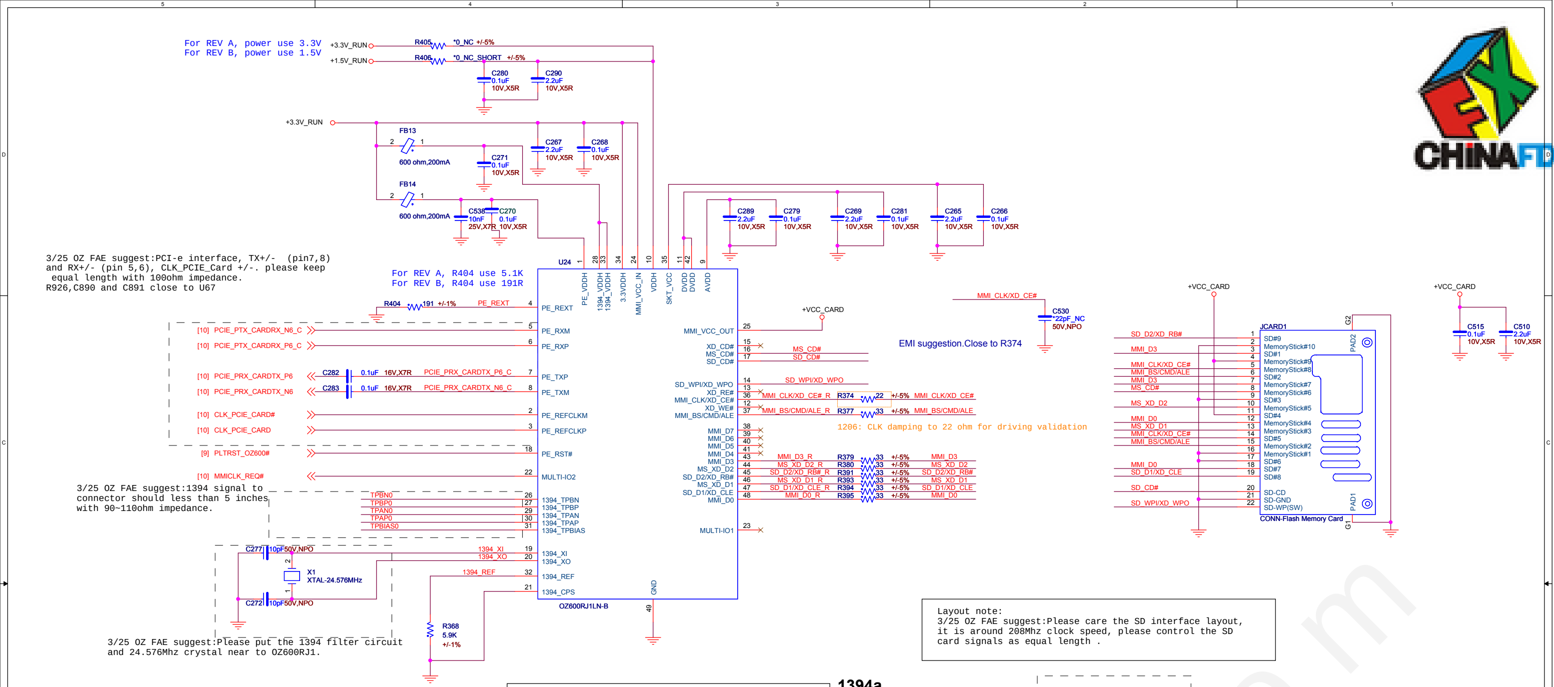
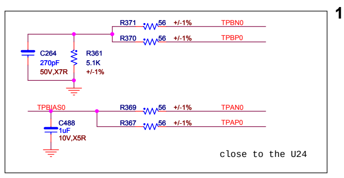
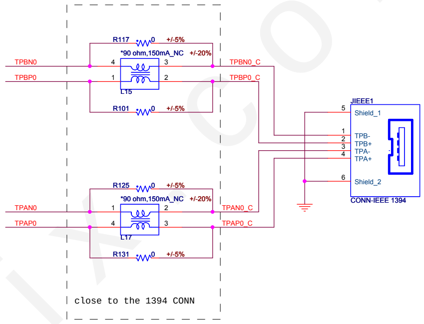
Sheet	43 of 69



1394a





Card Reader Conn Pin definition

NO	FOR	Pin Assign	Function
01	SD	#9	SD-DAT2
02	MemoryStick	#10	MS-VSS
03	SD/MMC	#1	SD-CD/DAT3 MMC-RSV
04	MemoryStick	#9	MS-VCC
05	MemoryStick	#8	MS-SCLK
06	SD/MMC	#2	SD-CMD MMC--CMD
07	MemoryStick	#7	MS-DATA3
08	MemoryStick	#6	MS-INS
09	SD/MMC	#3	SD-VSS MMC-VSS1
10	MemoryStick	#5	MS-DATA2
11	SD/MMC	#4	SD-VDD MMC-VDD
12	MemoryStick	#4	MS-DATA0
13	MemoryStick	#3	MS-DATA1
14	SD/MMC	#5	SD-CLK MMC-CLK
15	MemoryStick	#2	MS-BS
16	MemoryStick	#1	MS-VSS
17	SD/MMC	#6	SD-VSS MMC-VSS2
18	SD/MMC	#7	SD-DAT0 MMC-DAT
19	SD	#8	SD-DAT1
20	SD	CD	SD-CD
21	SD	GND	SD-GND
22	SD	SW.WP	SD-WP(SW)

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Title: 44 -- MMI & 1394(OZ600RJ1)

Size | Document Number: KRUG 15" UMA | Rev: 1A

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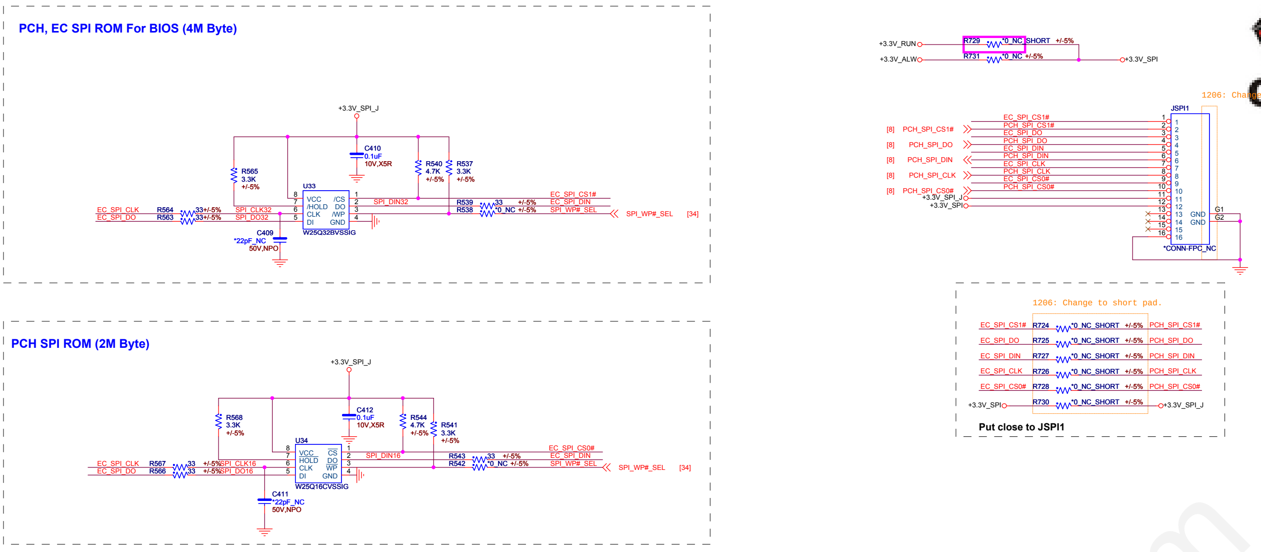

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Title	45 -- BIOS ROM(4M+8M)
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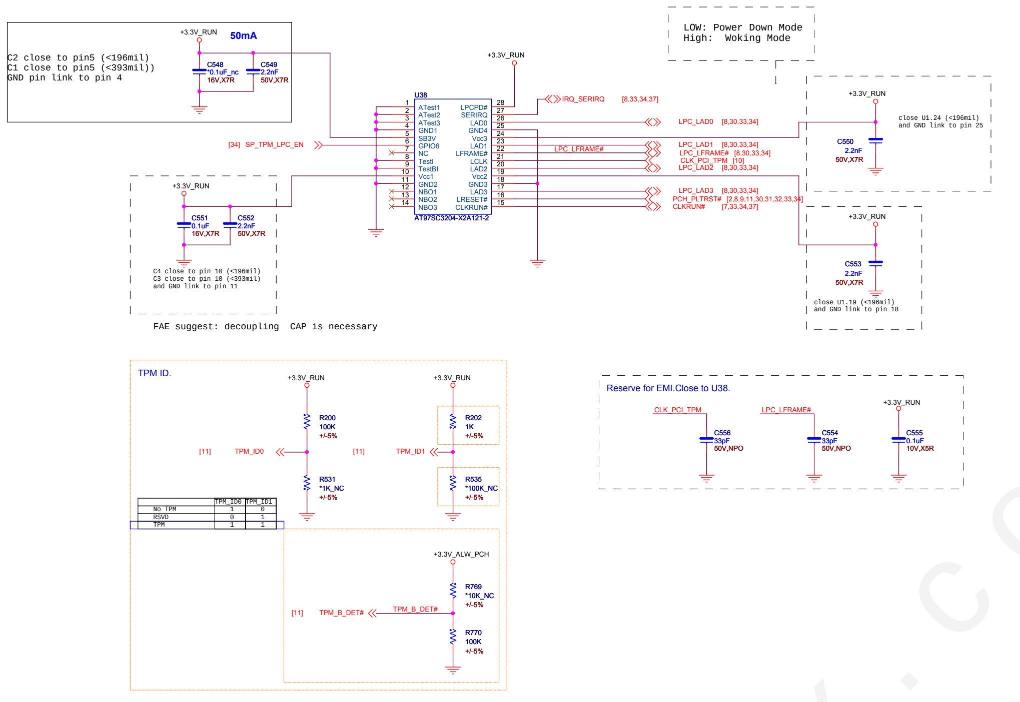
China TPM : ATMEL (TEMP SYMBOL)



	TPM_ID0	TPM_ID1
No TPM	1	0
RSVD	0	1
TPM	1	1

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Title: 46 -- TPM/TCM

Size | Document Number: KRUG 15" UMA | Rev: 1A

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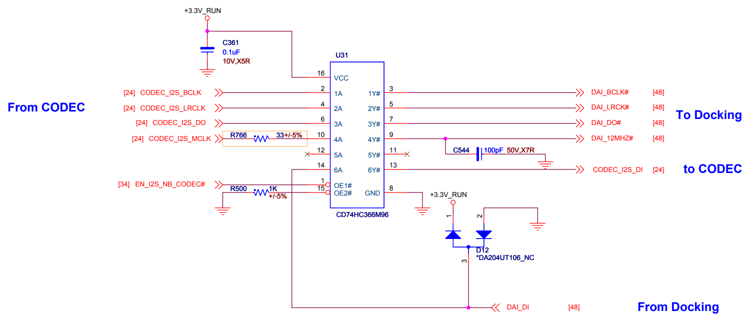

CD74HC366M96 table

INPUTS			OUTPUTS(Y)
OE1#	OE2#	A	HC366
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

NOTE:
Z=High impedance (OFF) state

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Title: 47 -- Audio Buffer for Docking

Size | Document Number: KRUG 15" UMA | Rev: 1A

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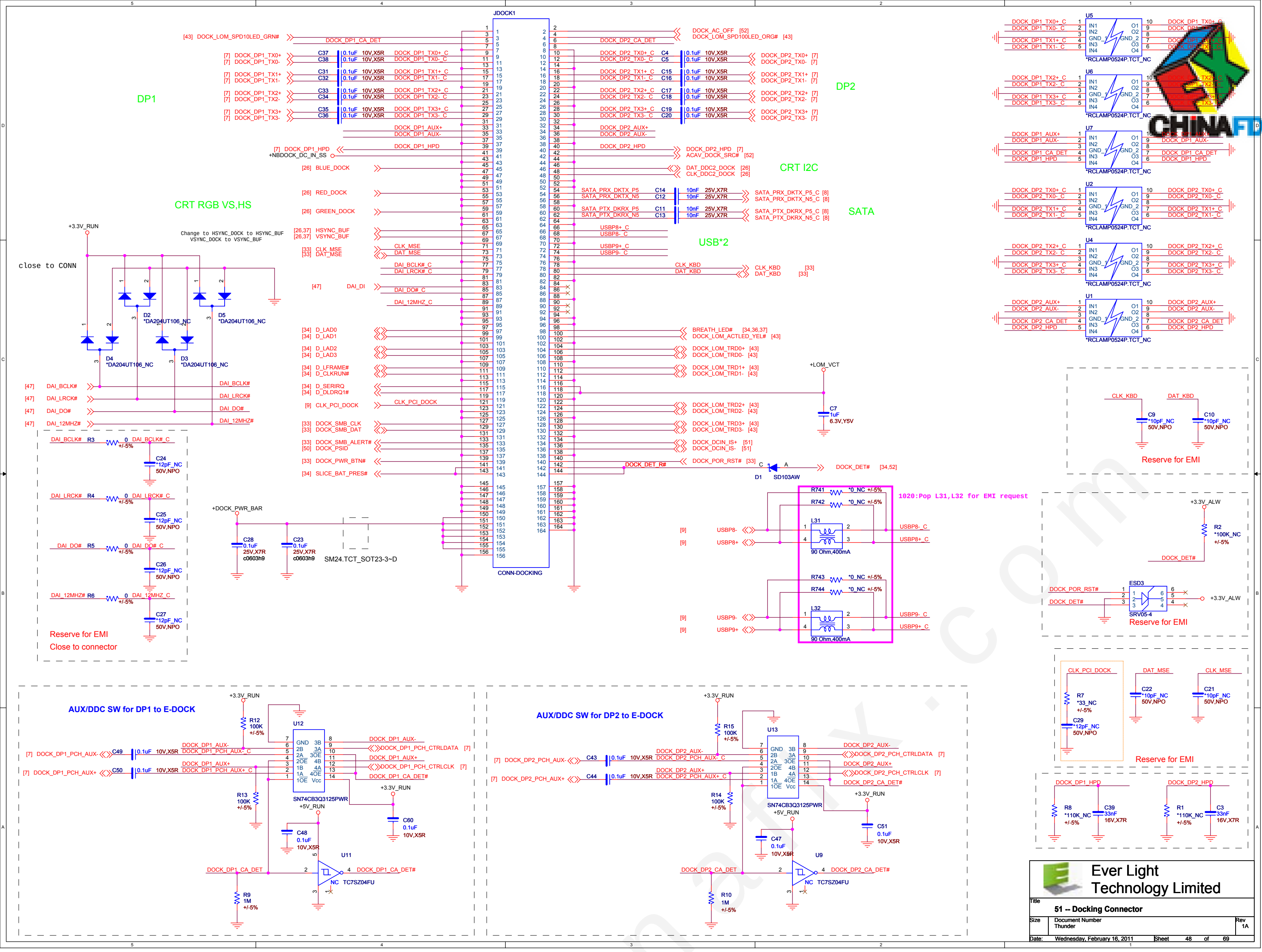
JDOCK1
DP1
DP2
CRT RGB VS,HS
CRT I2C
SATA
USB*2
close to CONN
Change to HSYNC_DOCK to HSYNC_BUF
VSYNC_DOCK to VSYNC_BUF
CONN-DOCKING
SM24.TCT_SOT23-3~D
*RCLAMP0524P.TCT_NC
1020:Pop L31,L32 for EMI request
90 Ohm,400mA
SD103AW
SRV05-4
Reserve for EMI
Close to connector
AUX/DDC SW for DP1 to E-DOCK
AUX/DDC SW for DP2 to E-DOCK
SN74CB3Q3125PWR
TC7SZ04FU
Ever Light
Technology Limited
Title
51 -- Docking Connector
Size
Document Number
Thunder
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1A
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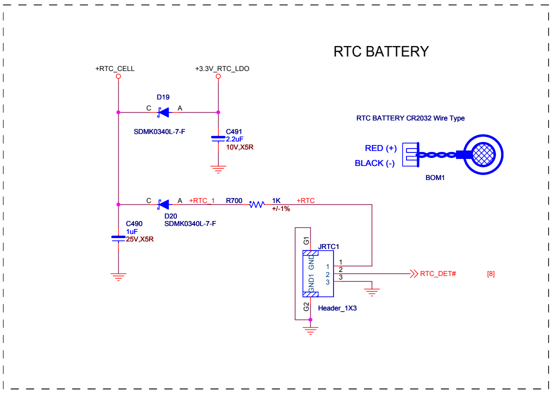
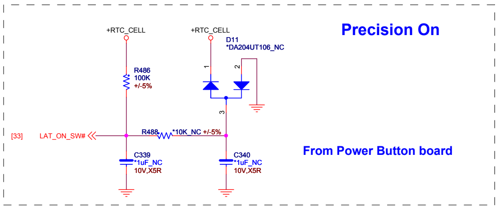
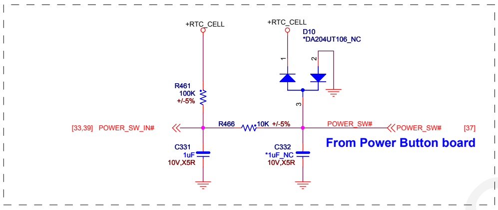
Sheet 48 of 69







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Title: 49 -- System Reset & RTC&UI		
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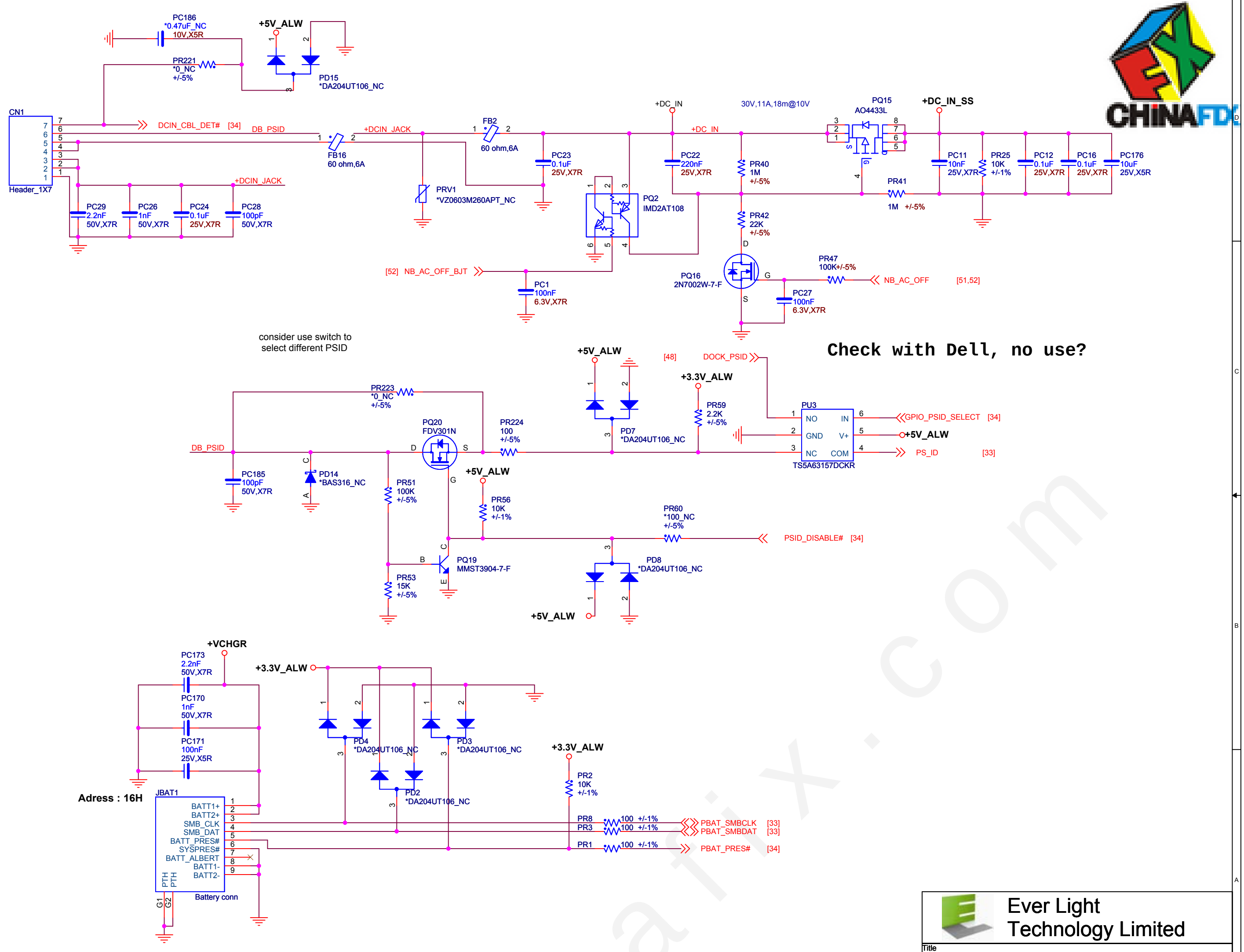

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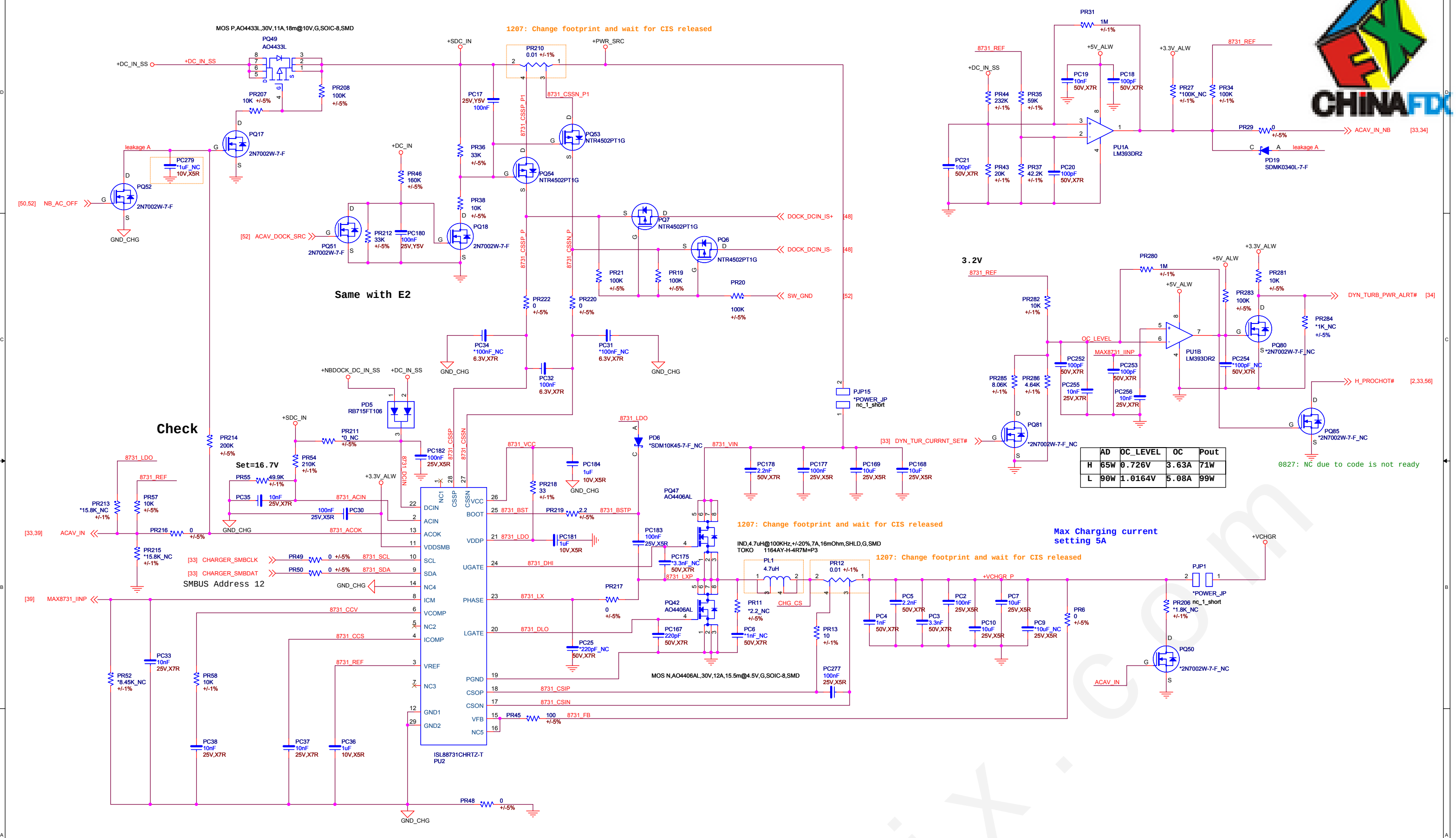
Title	50 -- PW_DCin & Batt
Size	Document Number: KRUG 15" UMA — Rev 1A
Date:	Wednesday, February 16, 2011 — Sheet 50 of 69



AD	OC_LEVEL	OC	Pout
H 65W	0.726V	3.63A	71W
L 90W	1.0164V	5.08A	99W

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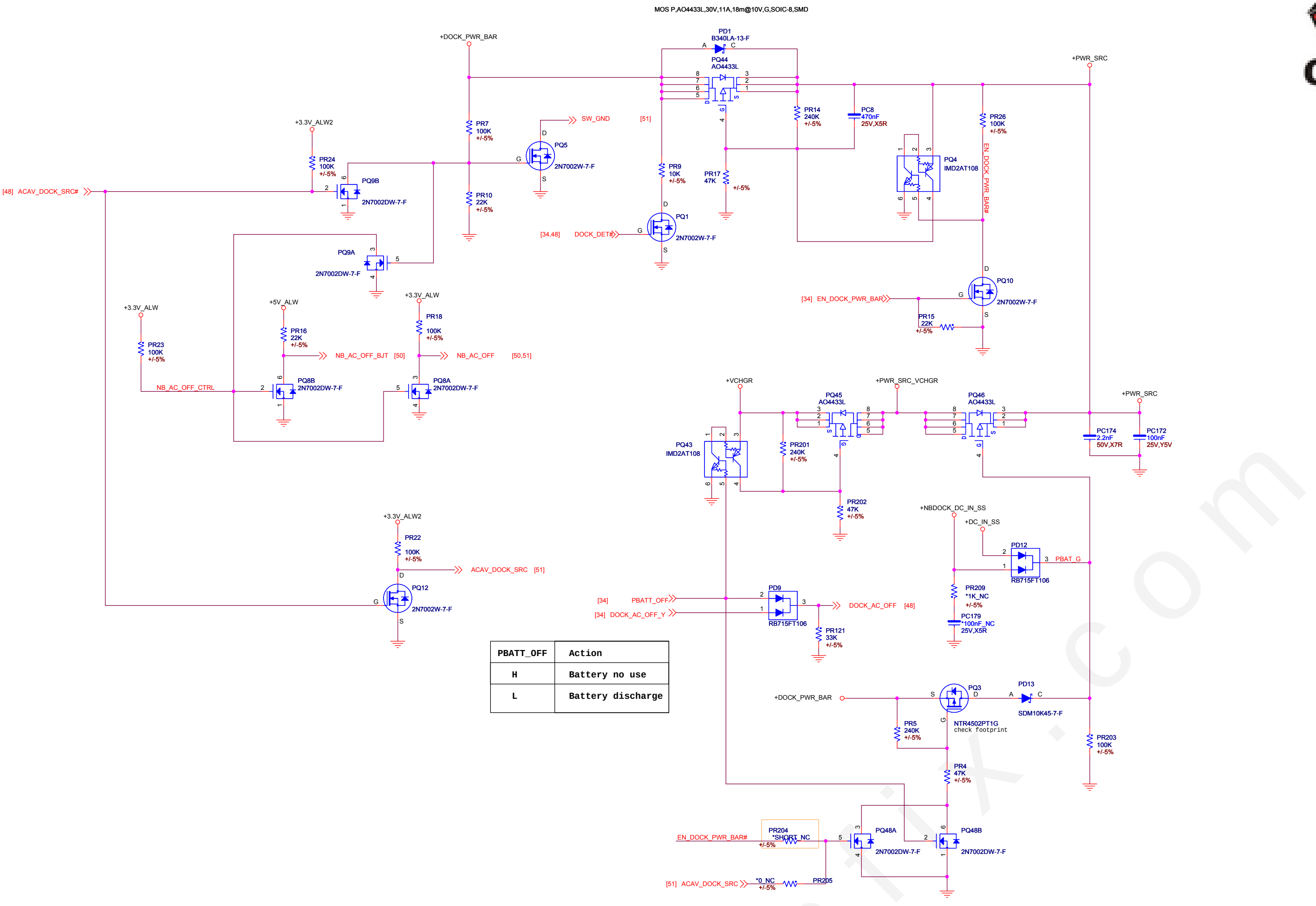
Title: Charger (ISL88731C)

Size | Document Number: B3_14" UMA | Rev: 1A

Date: Wednesday, February 16, 2011 | Sheet 51 of 69



PBATT_OFF	Action
H	Battery no use
L	Battery discharge

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Title	52 -- PW_Dock_Selector(Dis)	
Size	Document Number: KRUG 15" UMA	Rev: 1A
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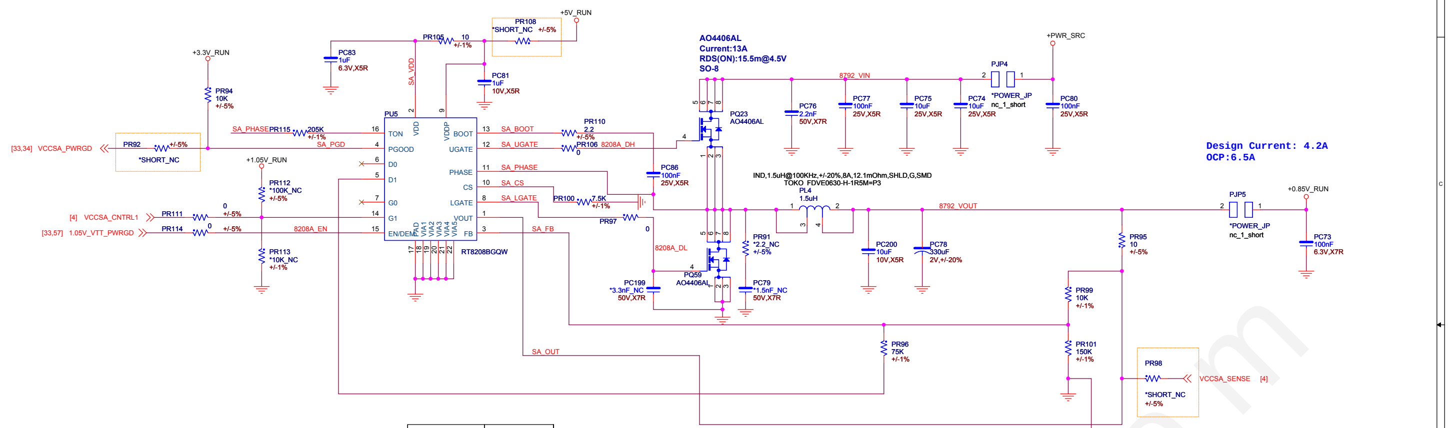

VCCSA_CNTRL1	VOUT(SPEC)
0	0.90V
1	0.80V

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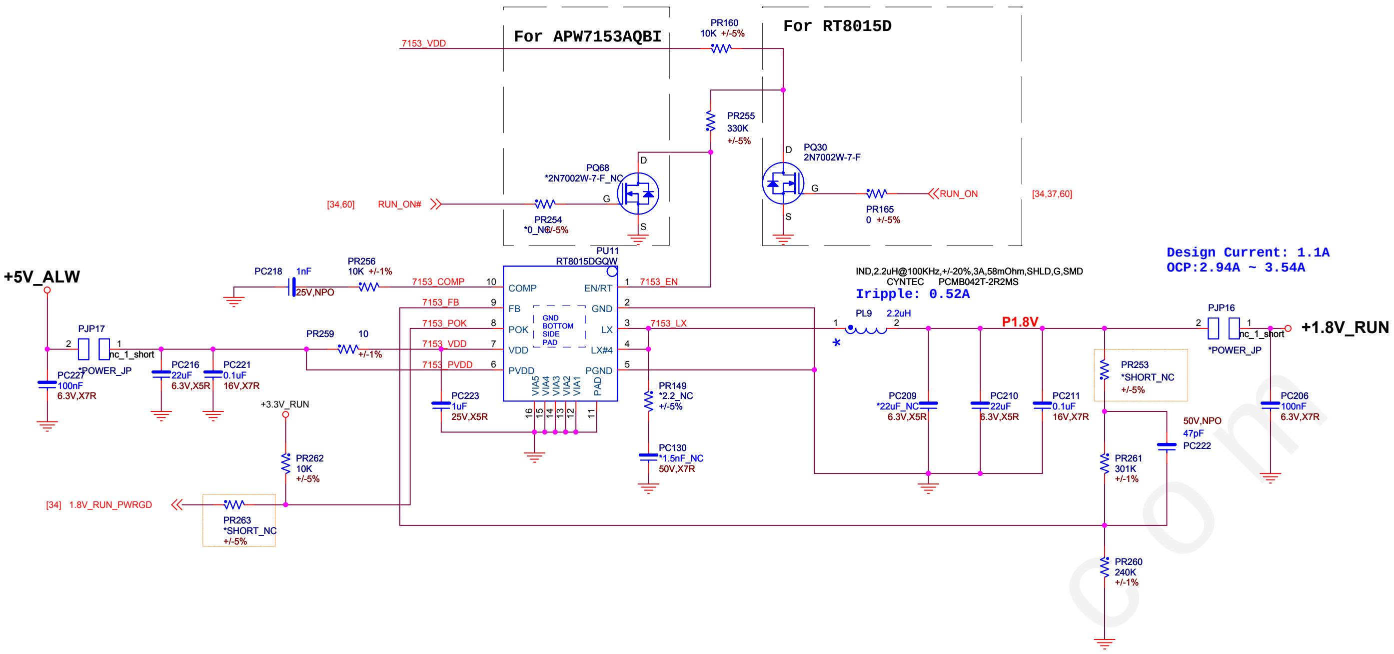
Title: 53 -- PW_+0.85V(MAX8792)

Size | Document Number: KRUG 15" UMA | Rev: 1A

Date: Wednesday, February 16, 2011 | Sheet 53 of 69



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Title	54 -- PW_SW_+1.8V(APW7153QBI)
Size / Document Number	KRUG 15" UMA
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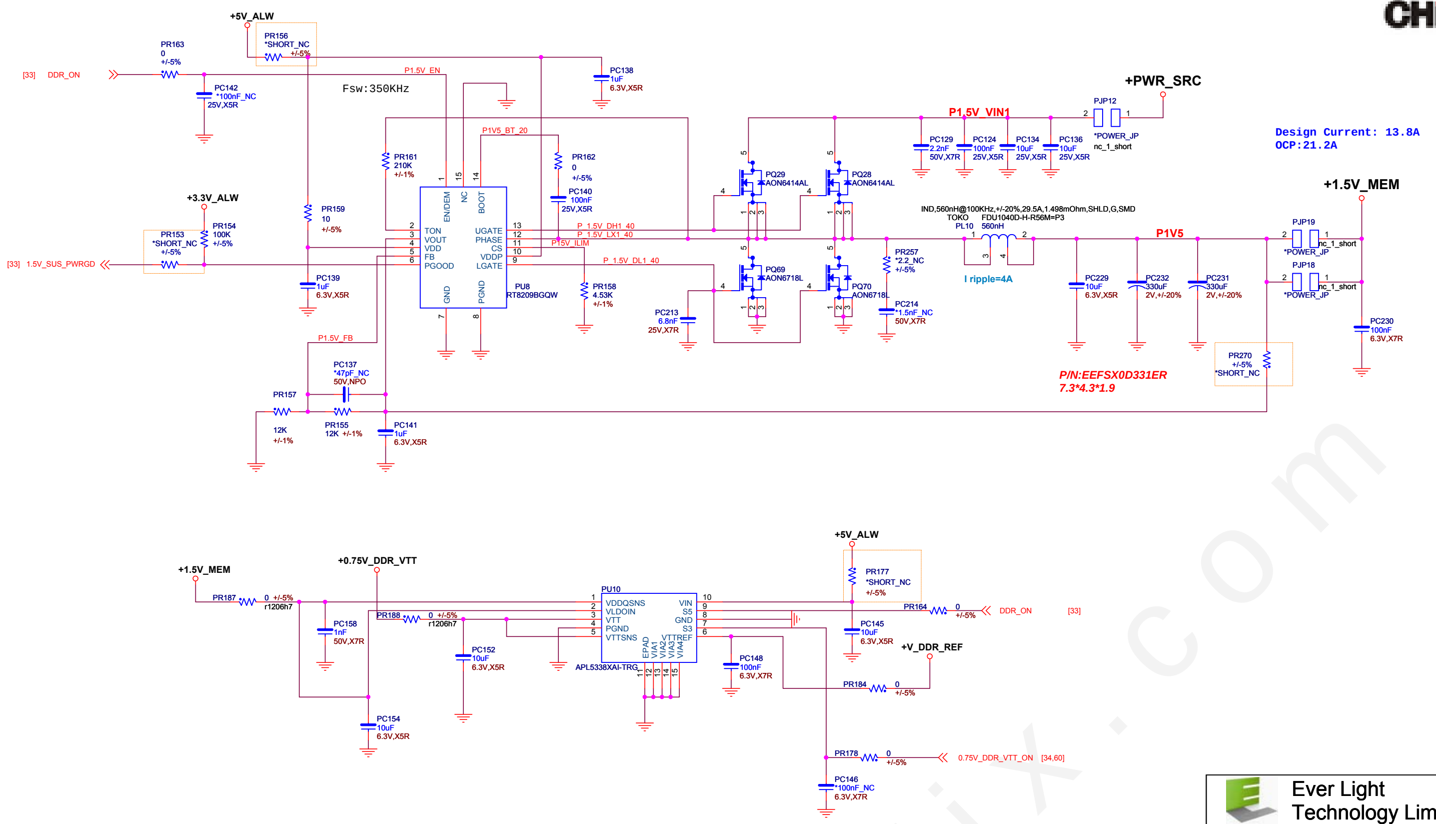
Sheet	54 of 69



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Title	55 -- PW_DDR(RT8209B/APL5338AI)
Size	Document Number: KRUG 15" UMA
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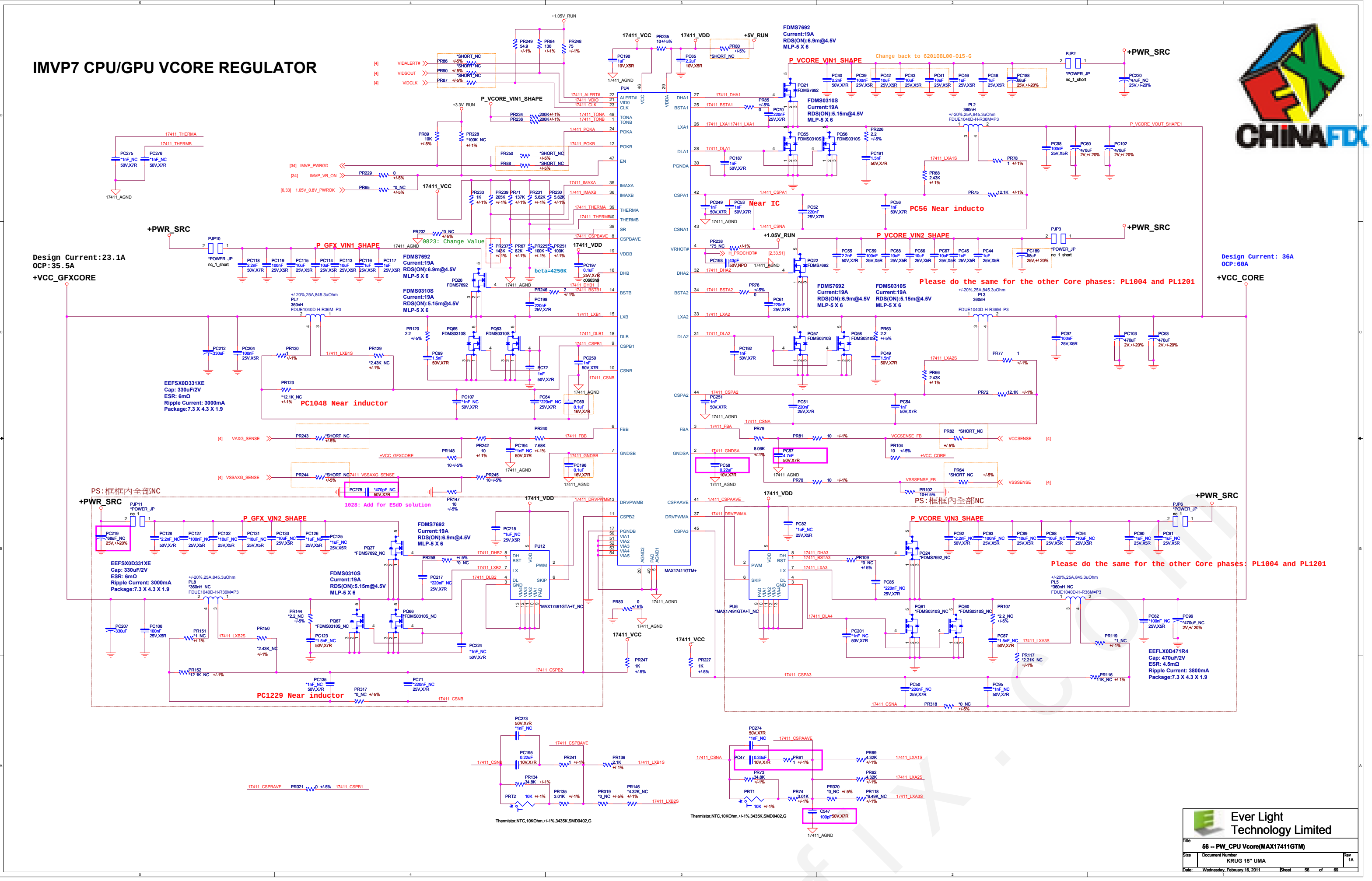
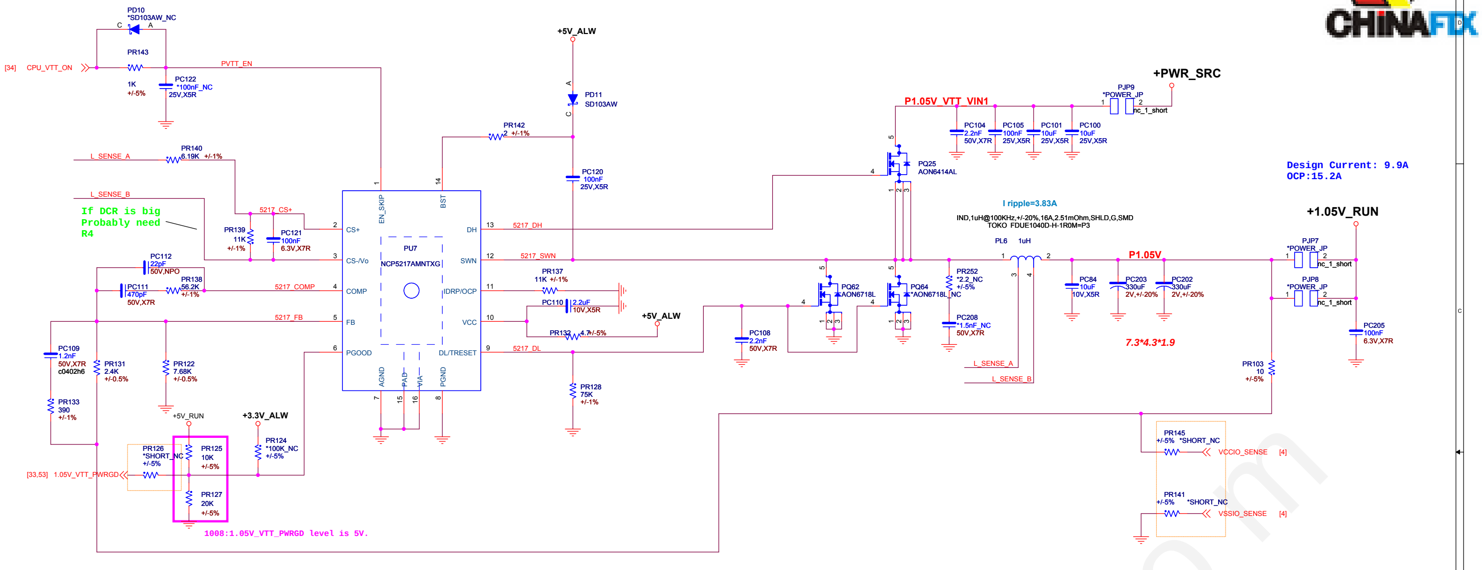
Date:	Wednesday, February 16, 2011
Sheet	55 of 69


IMVP7 CPU/GPU VCORE REGULATOR
Design Current:23.1A
OCP:35.5A
+VCC_GFXCORE
+PWR_SRC
Design Current: 36A
OCP:60A
+VCC_CORE
P_VCORE_VIN1_SHAPE
P_VCORE_VIN2_SHAPE
P_VCORE_VIN3_SHAPE
P_GFX_VIN1_SHAPE
P_GFX_VIN2_SHAPE
PC56 Near inductor
PC1048 Near inductor
PC1229 Near inductor
Near IC
Please do the same for the other Core phases: PL1004 and PL1201
PS:框框内全部NC
MAX17411GTM+
MAX17491GTA+T_NC
Ever Light Technology Limited
56 -- PW_CPU Vcore(MAX17411GTM)
KRUG 15" UMA
Wednesday, February 16, 2011



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Title	57 -- PW_1.05V(RT8209B)
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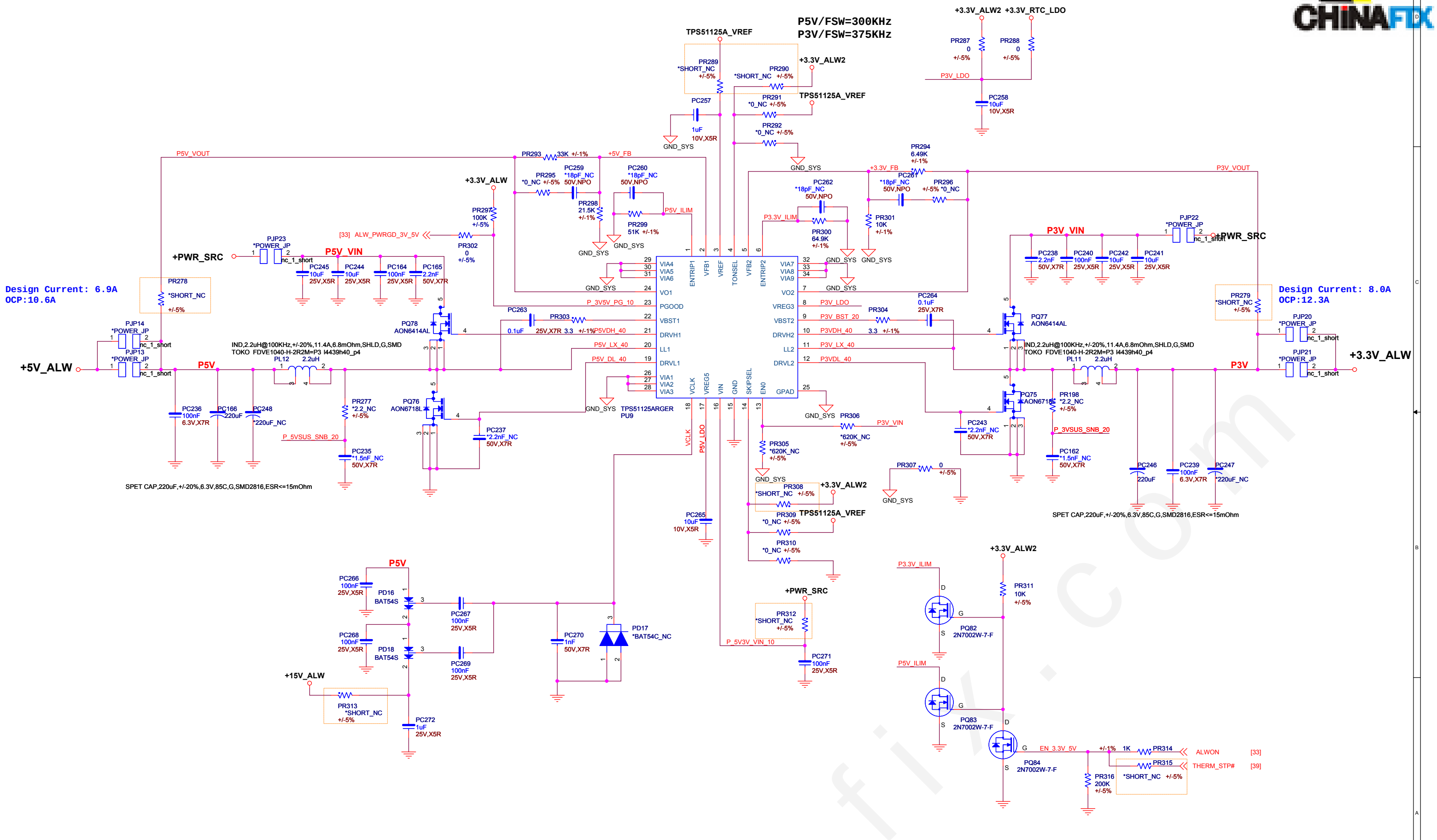
Ever Light Technology Limited		
Title: 58 -- PW_Blank for Ext.GPU		
Size	Document Number: KRUG 15" UMA	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 58 of 69	



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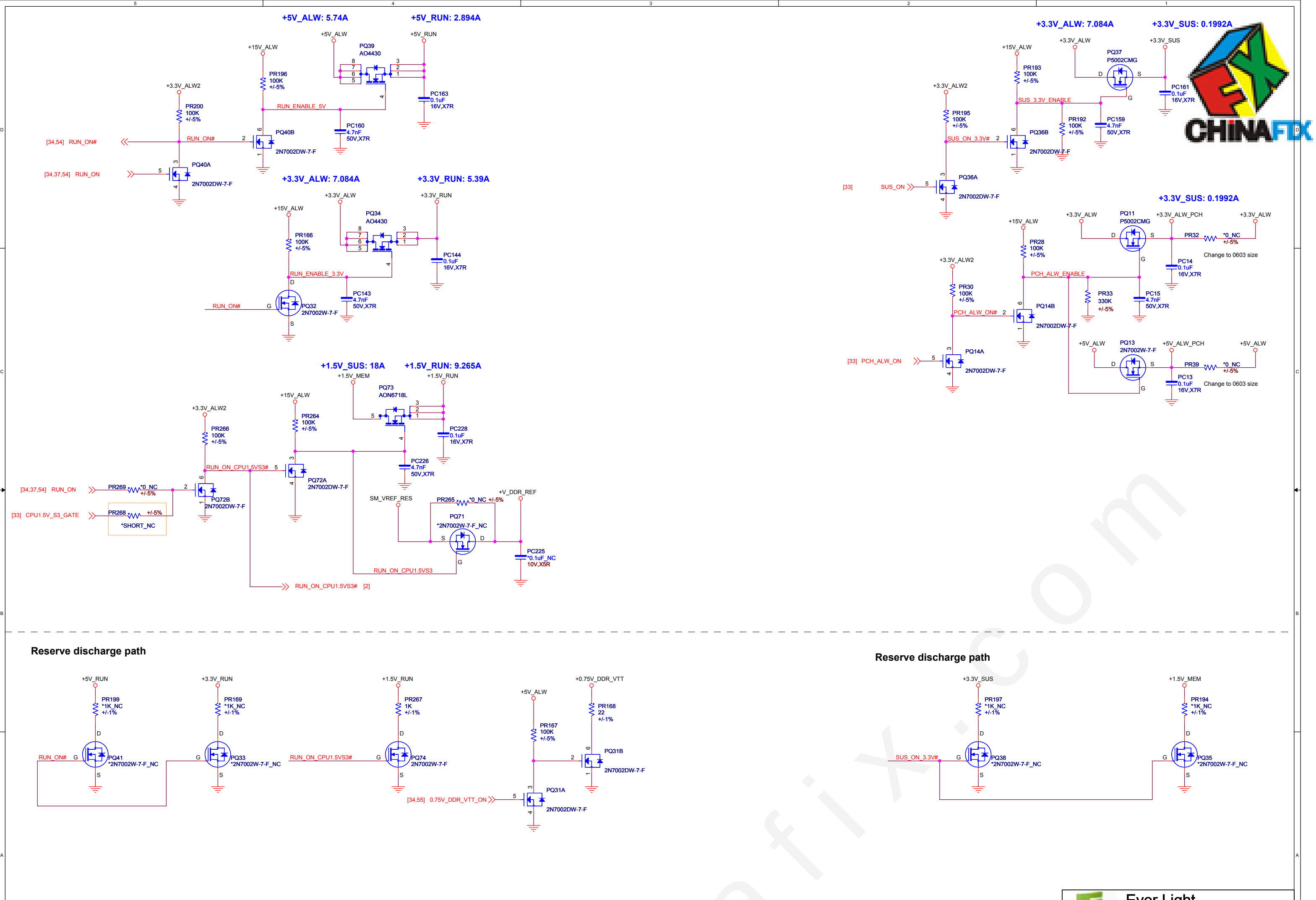
Title	59 -- PW_SYSTEM(TPS51125A)	
Size	Document Number: KRUG 15" UMA	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 59 of 69	



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Title	60 -- PW_Run Power Switch	
Size	Document Number KRUG 15" UMA	Rev 1A
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Title
61 -- PW_Blank

Size	Document Number	Rev
	KRUG 15" UMA	1A

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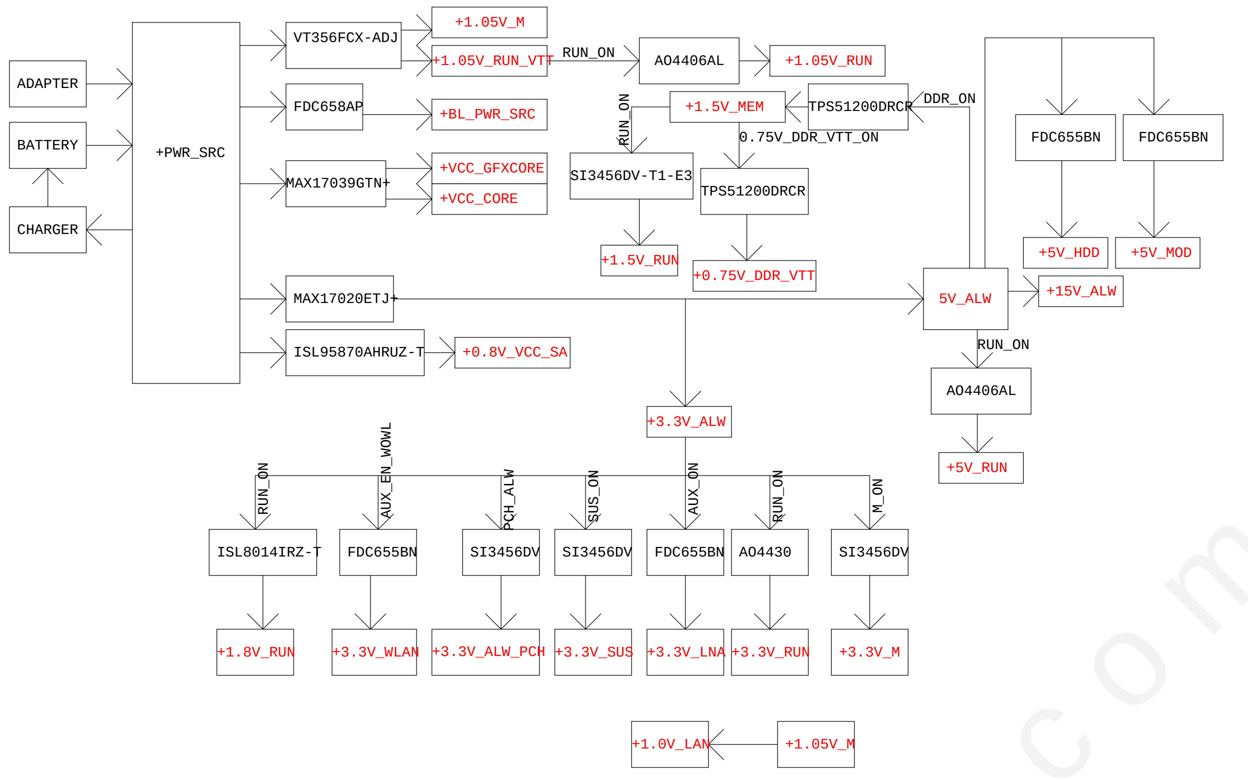
Title	62 -- PW_Blank	
Size	Document Number KRUG 15" UMA	Rev 1A
Date:	Wednesday, February 16, 2011	Sheet 62 of 69



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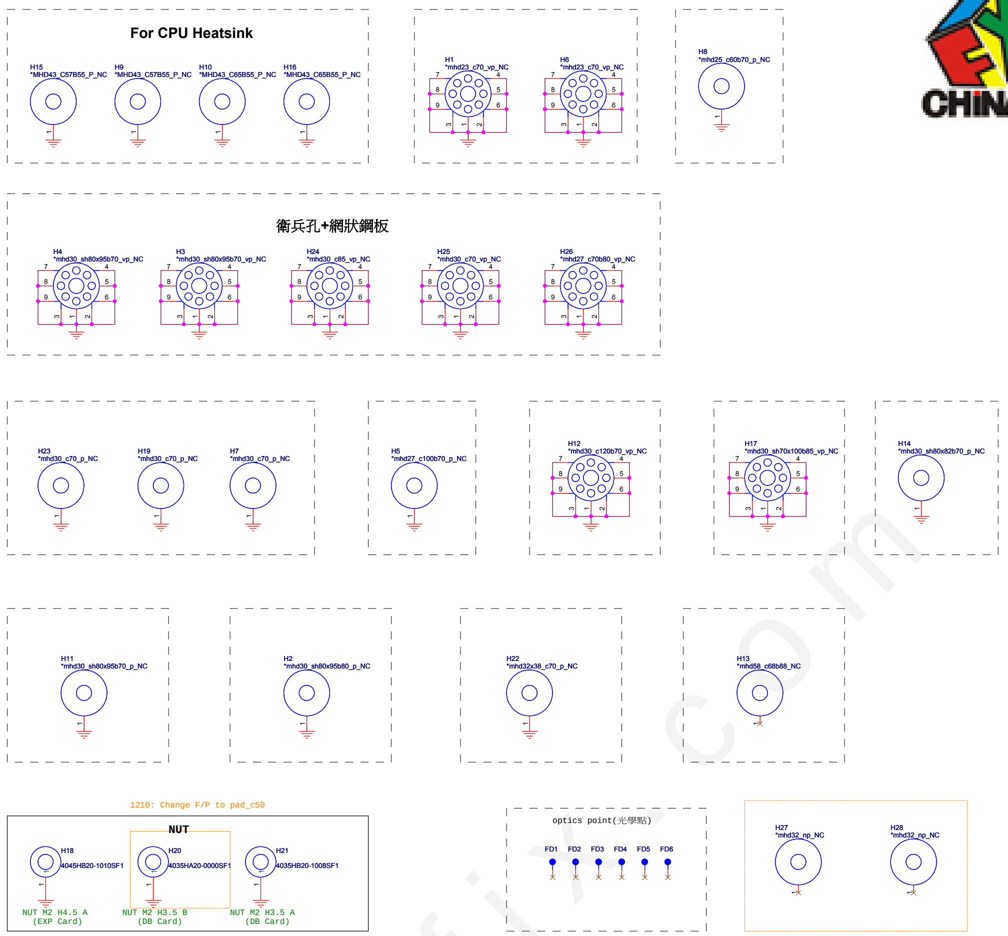
Title	63 -- power flow	
Size	Document Number: KRUG 15" UMA	Rev: 1A
Date: Wednesday, February 16, 2011	Sheet 63 of 69	



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Title	64 -- PAD,SCREW & Stiching CAPs	
Size	Document Number KRUG 15" UMA	Rev 1A
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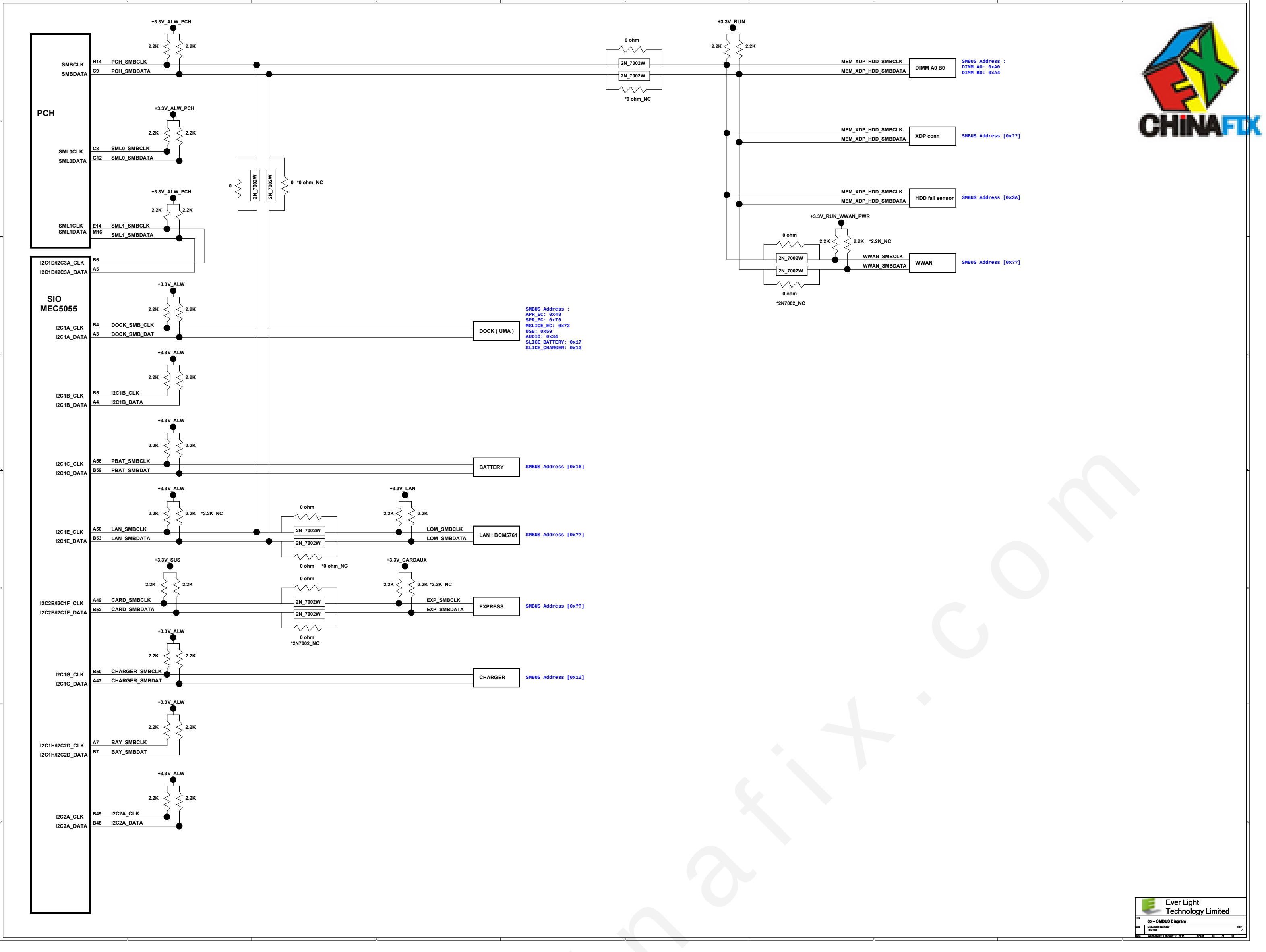

PCH
SMBCLK
SMBDATA
H14 PCH_SMBCLK
C9 PCH_SMBDATA
SML0CLK
SML0DATA
C8 SML0_SMBCLK
G12 SML0_SMBDATA
SML1CLK
SML1DATA
E14 SML1_SMBCLK
M16 SML1_SMBDATA
+3.3V_ALW_PCH
2.2K
0 ohm
*0 ohm_NC
2N_7002W
0
*0 ohm_NC
+3.3V_RUN
MEM_XDP_HDD_SMBCLK
MEM_XDP_HDD_SMBDATA
DIMM A0 B0
SMBUS Address :
DIMM A0: 0xA0
DIMM B0: 0xA4
XDP conn
SMBUS Address [0x??]
HDD fall sensor
SMBUS Address [0x3A]
+3.3V_RUN_WWAN_PWR
*2.2K_NC
WWAN_SMBCLK
WWAN_SMBDATA
WWAN
*2N7002_NC
SIO
MEC5055
I2C1D/I2C3A_CLK
I2C1D/I2C3A_DATA
B6
A5
+3.3V_ALW
I2C1A_CLK
I2C1A_DATA
B4 DOCK_SMB_CLK
A3 DOCK_SMB_DAT
DOCK (UMA)
SMBUS Address :
APR_EC: 0x48
SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13
I2C1B_CLK
I2C1B_DATA
B5 I2C1B_CLK
A4 I2C1B_DATA
I2C1C_CLK
I2C1C_DATA
A56 PBAT_SMBCLK
B59 PBAT_SMBDAT
BATTERY
SMBUS Address [0x16]
I2C1E_CLK
I2C1E_DATA
A50 LAN_SMBCLK
B53 LAN_SMBDATA
*2.2K_NC
+3.3V_LAN
LOM_SMBCLK
LOM_SMBDATA
LAN : BCM5761
+3.3V_SUS
+3.3V_CARDAUX
I2C2B/I2C1F_CLK
I2C2B/I2C1F_DATA
A49 CARD_SMBCLK
B52 CARD_SMBDATA
EXP_SMBCLK
EXP_SMBDATA
EXPRESS
*2N7002_NC
I2C1G_CLK
I2C1G_DATA
B50 CHARGER_SMBCLK
A47 CHARGER_SMBDAT
CHARGER
SMBUS Address [0x12]
I2C1H/I2C2D_CLK
I2C1H/I2C2D_DATA
A7 BAY_SMBCLK
B7 BAY_SMBDAT
I2C2A_CLK
I2C2A_DATA
B49 I2C2A_CLK
B48 I2C2A_DATA
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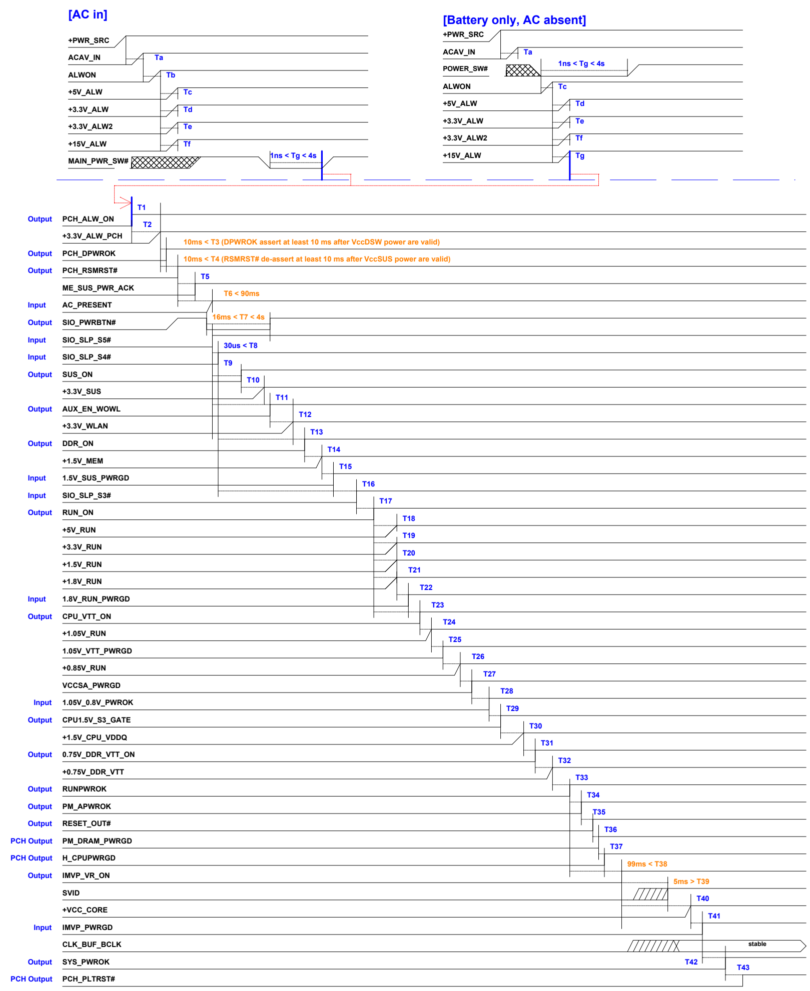
65 -- SMBUS Diagram

UMA Power On Sequence

EC pay attention timing



[AC in]

ITEM	Measure Point			Time
Ta	+PWR_SRC	To	ACAV_IN	
Tb	ACAV_IN	To	ALWON	
Tc	ALWON	To	+5V_ALW	
Td	ALWON	To	+3.3V_ALW	
Te	ALWON	To	+3.3V_ALW2	
Tf	ALWON	To	+15V_ALW	
Tg	MAIN_PWR_SW#		Low pluse width	N/A

[Battery only, AC absent]

ITEM	Measure Point			Time
Ta	+PWR_SRC	To	ACAV_IN	
Tb	POWER_SW#_MB		Low pluse width	N/A
Tc	POWER_SW#_MB	To	ALWON	
Td	ALWON	To	+5V_ALW	
Te	ALWON	To	+3.3V_ALW	
Tf	ALWON	To	+3.3V_ALW2	
Tg	ALWON	To	+15V_ALW	

ITEM	Measure Point			Time
T1	MAIN_PWR_SW#	To	PCH_ALW_ON	
T2	PCH_ALW_ON	To	+3.3V_ALW_PCH	
T3	+3.3V_ALW_PCH	To	PCH_DPWROK	
T4	+3.3V_ALW_PCH	To	PCH_RSMRST#	
T5	PCH_RSMRST#	To	ME_SUS_PWR_ACK	
T6	PCH_RSMRST#	To	AC_PRESENT	
T7	SIO_PWRBTN#	To	Low pluse width	
T8	SIO_SLP_S5#	To	SIO_SLP_S4#	
T9	SIO_SLP_S4#	To	SUS_ON	
T10	SUS_ON	To	+3.3V_SUS	
T11	+3.3V_SUS	To	AUX_EN_WOWL	
T12	AUX_EN_WOWL	To	+3.3V_WLAN	
T13	SIO_SLP_S4#	To	DDR_ON	
T14	DDR_ON	To	+1.5V_MEM	
T15	+1.5V_MEM	To	1.5V_SUS_PWRGD	
T16	SIO_SLP_S4#	To	SIO_SLP_S3#	
T17	SIO_SLP_S3#	To	RUN_ON	
T18	RUN_ON	To	+5V_RUN	
T19	RUN_ON	To	+3.3V_RUN	
T20	RUN_ON	To	+1.5V_RUN	
T21	RUN_ON	To	+1.8V_RUN	
T22	+1.8V_RUN	To	+1.8V_RUN_PWRGD	
T23	RUN_ON	To	CPU_VTT_ON	
T24	CPU_VTT_ON	To	+1.05V_RUN	
T25	+1.05V_RUN	To	1.05V_VTT_PWRGD	
T26	1.05V_VTT_PWRGD	To	+0.85V_RUN	
T27	+0.85V_RUN	To	VCCSA_PWRGD	
T28	1.05V_0.8V_PWROK	To	CPU1.5V_S3_GATE	
T29	CPU1.5V_S3_GATE	To	+1.5V_CPU_VDDQ	
T30	+1.5V_CPU_VDDQ	To	0.75V_DDR_VTT_ON	
T31	0.75V_DDR_VTT_ON	To	+0.75V_DDR_VTT	
T32	+0.75V_DDR_VTT	To	RUNPWROK	
T33	RUNPWROK	To	PM_APWROK	
T34	PM_APWROK	To	RESET_OUT#	
T35	RESET_OUT#	To	PM_DRAM_PWRGD	
T36	PM_DRAM_PWRGD	To	H_CPUPWRGD	
T37	H_CPUPWRGD	To	IMVP_VR_ON	
T38	IMVP_VR_ON	To	SVID	
T39	IMVP_VR_ON	To	+VCC_CORE	
T40	IMVP_VR_ON	To	+VCC_GFXCORE	
T41	+VCC_CORE	To	IMVP_PWRGD	
T42	IMVP_PWRGD	To	SYS_PWROK	
T43	SYS_PWROK	To	PCH_PLTRST#	

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Title	67 -- Power Sequency Timing
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Change List

Item	Date	T	Page#	Issue Description	Solution Description
				A00	
01		PWR		Delete Power Jump.	Change Power Jump to short pad.
02			P39	Edit thermal diode note.	
03			P40	IEEE test fail.	Change R80 to 1.2K.
04		EE	P45	SCH Changed	Change R724~R728,R730 to shortpad.De pop JSPI1.
05			P29	Change eSATA connector part number.	Change eSATA connector part number.
06			P02	SCH Changed	De pop R273,R304,R314,R674~R678,R682,R684
07			P06	SCH Changed	Remove XDP component.Change R107~R112,R115,R116,R230~R236,RR238~R240 to NC
08			P06	SCH Changed	Change R284~R286,R302,R303,,R307,R311~R313,R105,R106,R113,R114,R237 to NC
09		EE	P24	SCH Changed	Change R761 to Short pad
10			P24	SCH Changed	Change R757,R759,R760,Q50,Q51 to NC
11			P44	Design Changed	CLK damping to 22 ohm (R374) for driving validation
12		PWR	P51	Design Changed	Change P/N and FP for PR12,PR210,PL1 and wait for CIS released.
13			P34	Design Changed	ADD R765 100K ohm for power request
14			P49	Delete Power switch SW1.	Delete Power switch SW1.
15			P11	TPM only	Pop R202 and De-pop R535
16			P37	TPM only	Delete JTPM1,C541~C543,C376
17			P46	Change TPM SCH to MB	Add U38,C548~C556 for TPM SCH changed.
18		EE	P47	SCH Changed	Add R766 between U31 and Singal "CODEC_I2S_MCLK"
19			P64	Design Changed	Change H20 to new f/p mhd11_c50b_paste
20			P46	TPM only	Move TPM ID table to Page46.
21			P51	Power Changed	Reserve 1uF(PC279) at leakage A,let it will be low after +3.3V_ALW turn on.
22			P36, P32	Wlan LED is lighting when WWAN module insert after AC-IN.	Add mosfet (Q52) and Res 100K (R767) to control LED .
23			P37	Add 2 pin connector (CN18)	Add 2 pin connector (CN18)
24			P36	LED Current & Brightness adjust	Change R588 & R753 to 130 ohm, R589 to 180 ohm.
25		PWR	P56	De-rating thermal issue	Change PC41,42,43 to 62011HS00-015-G
26			P64	Design Changed	Change H20 to new f/p pad_c50
27			P24	Reduce noise	Change C417 and c420 to 0.uF
28			P43	IEEE test fail.	Delete R745~R752
29		EE	P43	Refer Intel guide rev 1.5	Add R768
30			P32	Pin 42 of WWAN module is open drain .Add PU resistor at LED_WWAN_OUT# .	Add R767(100K ohm) and PU to "+3.3V_RUN_WWAN_PWR" for net"LED_WWAN_OUT#"
31			P37	Modify Audio board pin define.	Modify Audio board pin define.
32			P33	Change board ID.	Change board ID R493 to 8.2K.
33			P33	Design Changed	Depop R456,R480,R462,U27
34			P52~P60	Cost down	Change 0 ohm to short pad for power portion P52~P60.
35		PWR	P56	Acoustic test result.	Change PC188,PC189 to 68uF(62110VQ00-024-G)
36			P56	De-rating thermal issue	Change PC41,42,43 to 620108L00-015-G
37		EE	P37	P/N Changed	Change JAudio1 to GB5RF201-1203-8H and CN18 to HN14021-0000-7H
38			P11	Design Changed	Change R246 to 1K. modify GPIO37 table.
39		PWR	P33	P/N Changed	Change MEC5055 mfg PN to MEC5055-LZY-KRU00 .
40			P51	P/N Changed	Add PL1 Foxconn PN .
41			P51	P/N Changed	Change PL1 part number to 1164AY-H-4R7M=P3 and keep footprint.
42			P46	Add pull down resistor R770 at TPM_B_DET#. Modified TPM selection table.	Add pull down resistor R770 at TPM_B_DET#. Modified TPM selection table.
43			P33	Add MEC5055 Foxconn part number which the same in ST stage.	Add MEC5055 Foxconn part number which the same in ST stage.
44			P07~P13	P/N Changed	Update PCH P/N to 21011EG00-187-G
45			P64	Add H27,H28	Add H27,H28
46		EE	P36	LED Current & Brightness adjust	Change LED RES R753,R588 to 390 ohm and R589 to 620 ohm
47			P07~P13	P/N Changed	Update PCH P/N to 21011EG00-187-G
48			P04	P/N Changed	Change C249 part number to 622203J00-022-G because part number is error .
49			P30,P37	EMI Request	Reserve R771,C557 for "CLK_DEBUG" and R772,C558 for "CLK_PCI_OZ"
50			P11	Intel feedback	Pop R196 for Intel ME setting.
51			P07	HDMI Hot plug detect issue	Add C559 (620103600-011-G) to fix
52			P56	Solve overshoot issue	Change PC69 and PC196 to 62010JC00-026-G
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Rev
A00

POWER SATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN/WIMAX
	5	MUX: Intel port to WWAN or Blacktop port to WWAN
	6	Bluetooth
	7	USH2-Host port
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera1/Camera2
	12	
	13	Mini CARD3

PM TABLE

	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW_PCH	+3.3V_SUS +1.5V_ME M	+5V_RUN +1.5V_RUN +1.8V_RUN +3.3V_RUN +0.75V_DDR_VT T +VCC_CORE +1.05V_RUN_VT	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exis	OFF	OFF	OFF	OFF	OFF

USH	USB PORT#	DESTINATOPN
	0	BIO
	1	None

SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	MINI CARD
SATA3	None
SATA4	ESATA
SATA5	DOCK

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WWAN
	CLKOUT_PCIE1	10/100/1G LAN
	CLKOUT_PCIE2	PCMCIA
	CLKOUT_PCIE3	MiniWPAN (Mini Card 3)
	CLKOUT_PCIE4	EXPRESS CARD
	CLKOUT_PCIE5	MINI CARD-2 WLAN
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	USB3.0
	CLKOUT_PEG8	CARD READER
	CLKOUTFLEX0	SIO_14M
	CLKOUTFLEX1	PCI_TCM
	CLKOUTFLEX2	PCI_TPM
	CLKOUTFLEX3	JETWAY_14M

PCI EXPRESS	DESTINATION
Lane1	MINI CARD-1 WWAN
Lane2	MINI CARD-2 WLAN
Lane3	CARD READER
Lane4	EXPRESS CARD
Lane5	MINI CARD-3 PCIE
Lane6	USB3.0
Lane7	
Lane8	PCMCIA

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