BOHOL LB720 Schematics

Kabylake-U

U22 / U2+3e / U42

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DY	***DUMMY***
DY-EMC	***Follow EMC team request (DY)***
EMC-TVS	***SDV : ASM*** ***FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)***
EMC-TEST	***Follow EMC team request (ASM)***

23e	***U2+3e only***
U42	***U42 only***
NON-U42	***U22 or U2+3e***
UMA	***UMA only***
PX	***Discrete only***

BOM1

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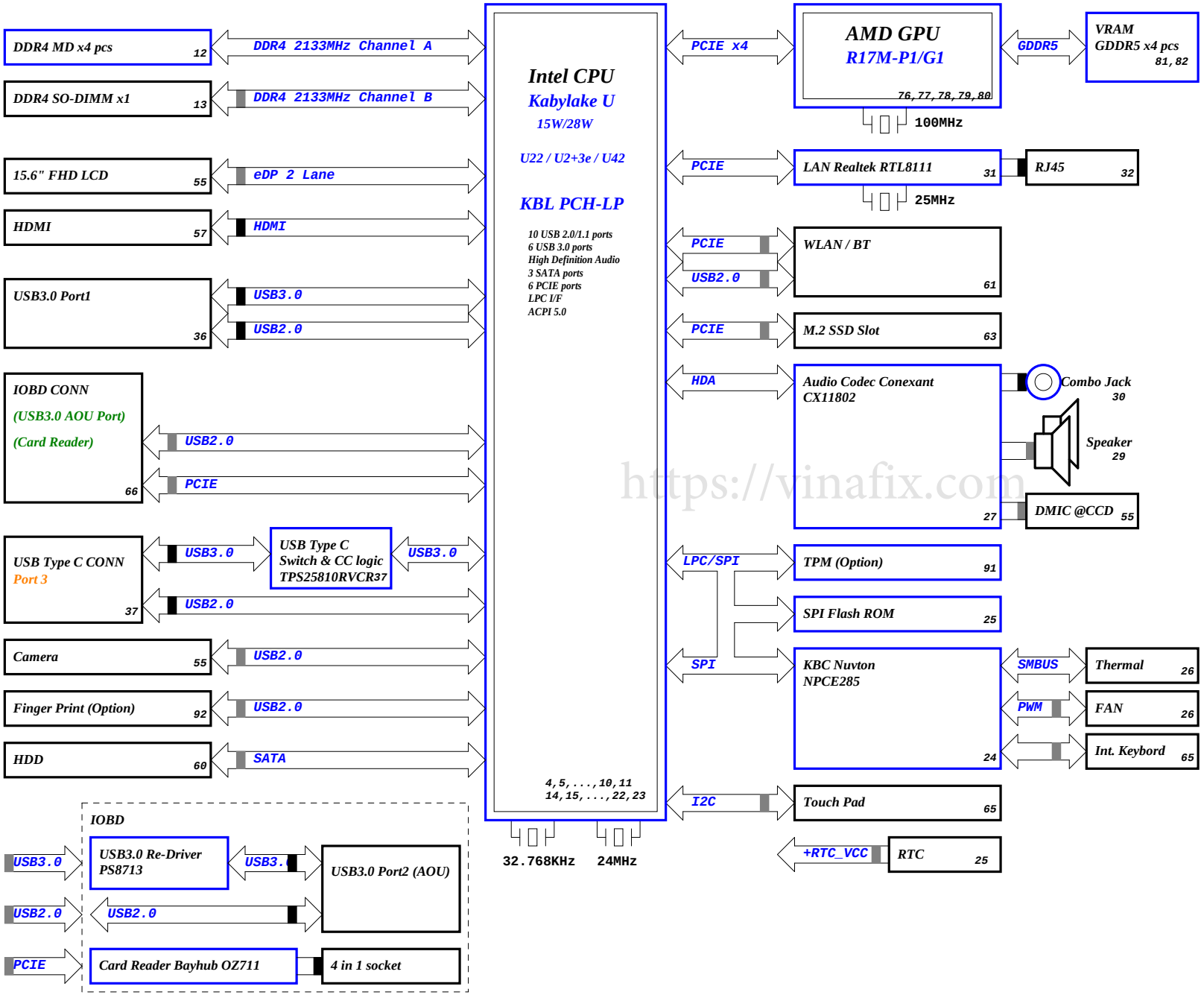
Title: ***COVER PAGE***

Size: A3 | Document Number: BOHOL | Rev: -1

Date: Tuesday, May 02, 2017 | Sheet 1 of 105

Project code: LB720: 4PD0CJ010001
LB721: 4PD0CJ01A001
PCB P/N: 16877
Revision: -1

LB720/LB721 KBL-U Block Diagram



PCB LAYER

L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket
Internal Connector/Socket

CHARGER HPA02224RGRR 44

INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT6575DGQW 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power ISL95829AHRTZ 46~50
AOZ5049QI x 2 (U42)
AOZ5049QI x 2 (23e)
ISL6208BCRZ

INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA

DDR4 SUS RT8231AGQW 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0

CPU DC/DC 1D0V_S5 RT8237CZQW 52

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

EOPIO/EDRAM (23e) APE8939GN3 53

INPUTS	OUTPUTS
1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

CPU VCCIO TPS22961DNYT 53

INPUTS	OUTPUTS
1D0V_S5	+VCCIO

LDO V1D8V RT9025-25ZSP 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

G5016KD1U RT9025-25ZSP 40

INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0

VCCST AOZ1335DI 40

INPUTS	OUTPUTS
1D0V_S5	1V_VCCST

DGPU CORE ISL6277AHRZ 85

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

DGPU VDDCI & 0.8V ISL6208BCRZ 86

INPUTS	OUTPUTS
DCBATOUT	0D8V_VGA_S0

DGPU GDDR5 AOZ2260QI 86

INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

DGPU 1D8V APL5930KAI 86

INPUTS	OUTPUTS
3D3V_S5	1D8V_VGA_S0

BOM1

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Title: BLOCK DIAGRAM
Size: Custom | Document Number: BOHOL | Rev: -1
Date: Tuesday, May 02, 2017 | Sheet 2 of 105

Main Func = CPU

(Blank)

BOM1

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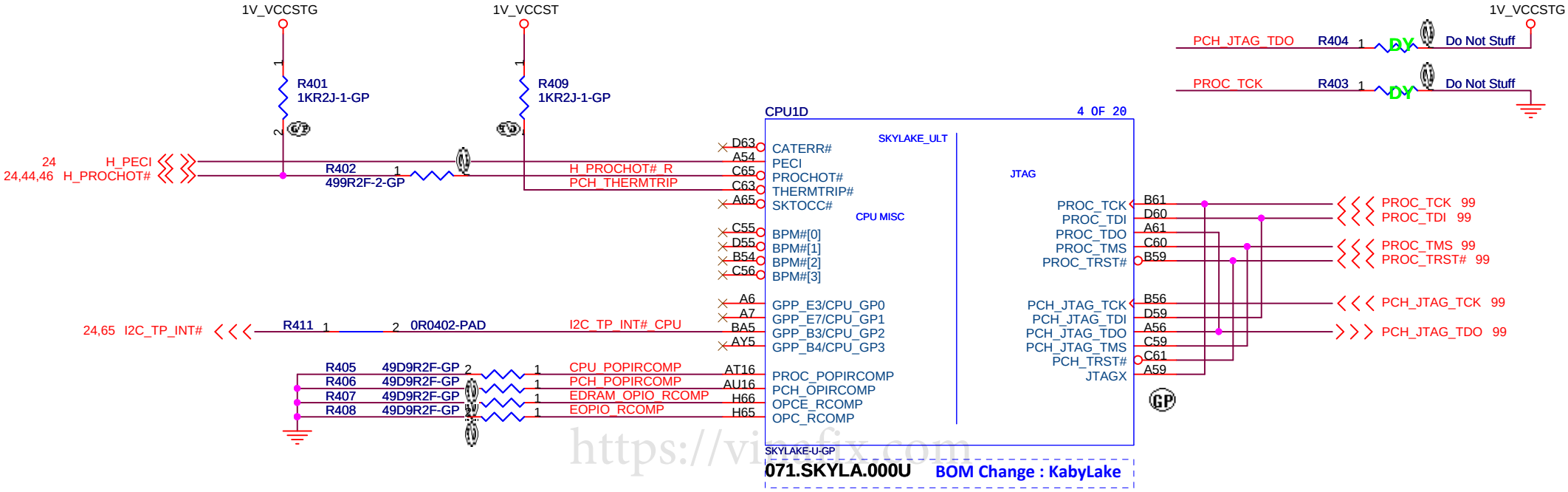
Title: ***RESERVED***	
Size: A4	Document Number: **BOHOL** Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 3 of 105

Main Func = CPU



BOM1

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Title: ***CPU (JTAG/CPU SIDE BAND)***

Size	Document Number	Rev
A4	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 4 of 105

Main Func = CPU

DDR4 ball type: Interleaved Type

M_A_BG1, M_VREF_DQ_DIMM0
Reserve Testpoint only

CPU1B — 2 OF 20 — SKYLAKE_ULT

CPU1C — 3 OF 20 — SKYLAKE_ULT

M_B_DQ[8:15] M_B_DQ[0:7]
M_B_DQ[16:23] M_B_DQ[24:31]
M_B_DQ[32:39] M_B_DQ[40:47]
M_B_DQ[48:55] M_B_DQ[56:63]

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

TP502 TPAD14-OP-GP
TP501 TPAD14-OP-GP

Q501
DMN5L06K-7-GP
84.05067.031

AFTP501
R506 220KR2F-GP

R505 470R2F-GP
R501 121R2F-GP
R502 80D6R2F-L-GP
R503 100R2F-L1-GP-U
R504 0R0402-PAD
C501 DY

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

2017/03/05
SIT 504 change to short pad.

close to CPU
close to DIMM1

	DDR4
M_B_A14	AY44
M_B_A15	AY43
M_B_A16	AW44
M_B_BG1	AN52
M_B_BG0	AP52
M_B_PARITY	AP43
M_B_ALERT_N	AN43
M_B_ACT_N	AN53

071.SKYLA.000U BOM Change : KabyLake

BOM1

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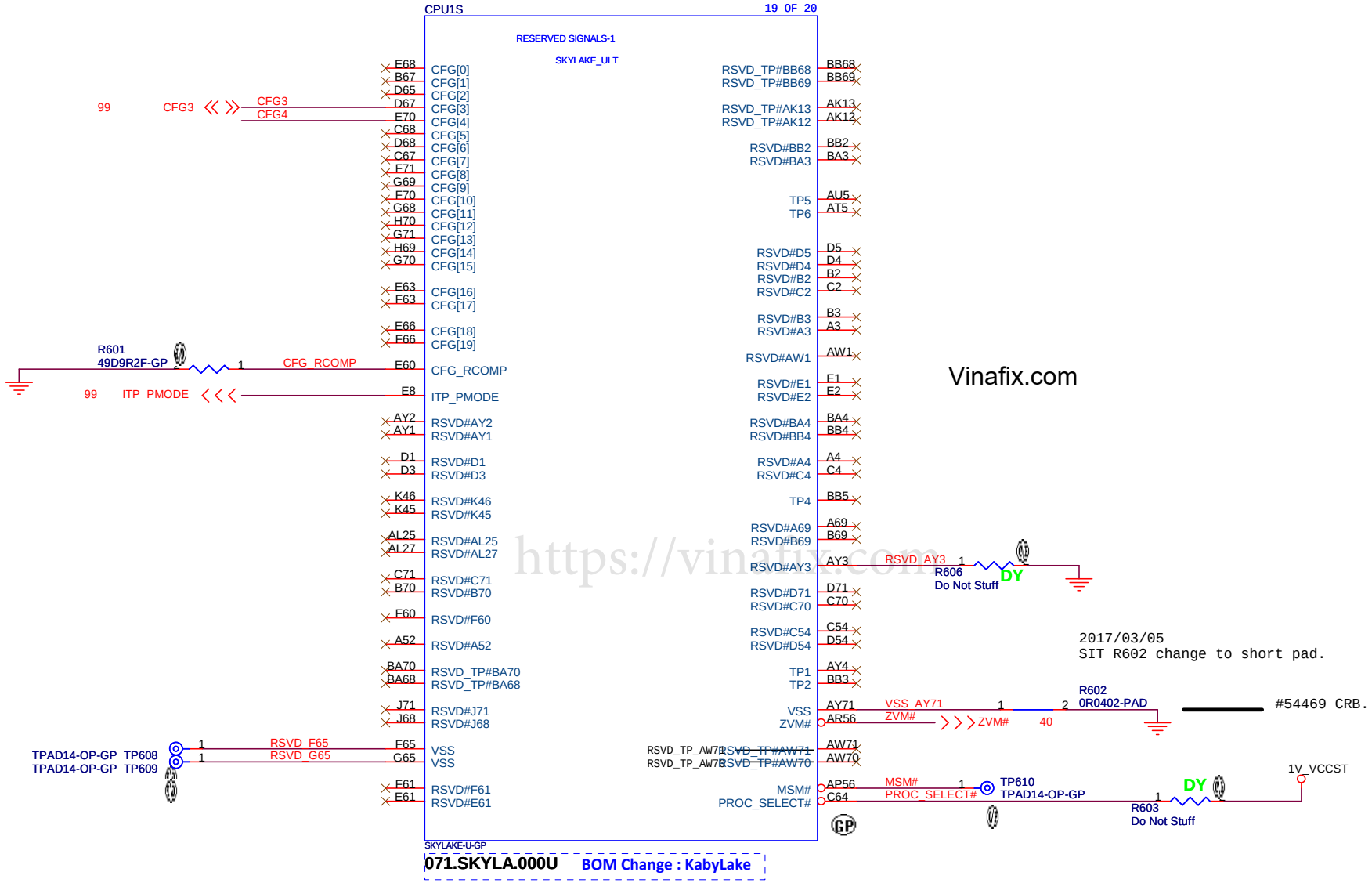
Title: CPU (DDR)

Size: Custom | Document Number: BOHOL | Rev: -1

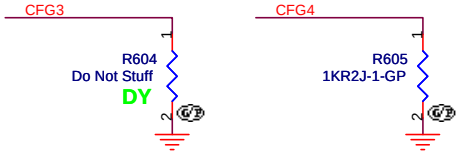
Date: Tuesday, May 02, 2017 | Sheet 5 of 105

Main Func = CPU



2017/03/05
SIT R602 change to short pad.

#54469 CRB.



[559100]
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.

BOM1

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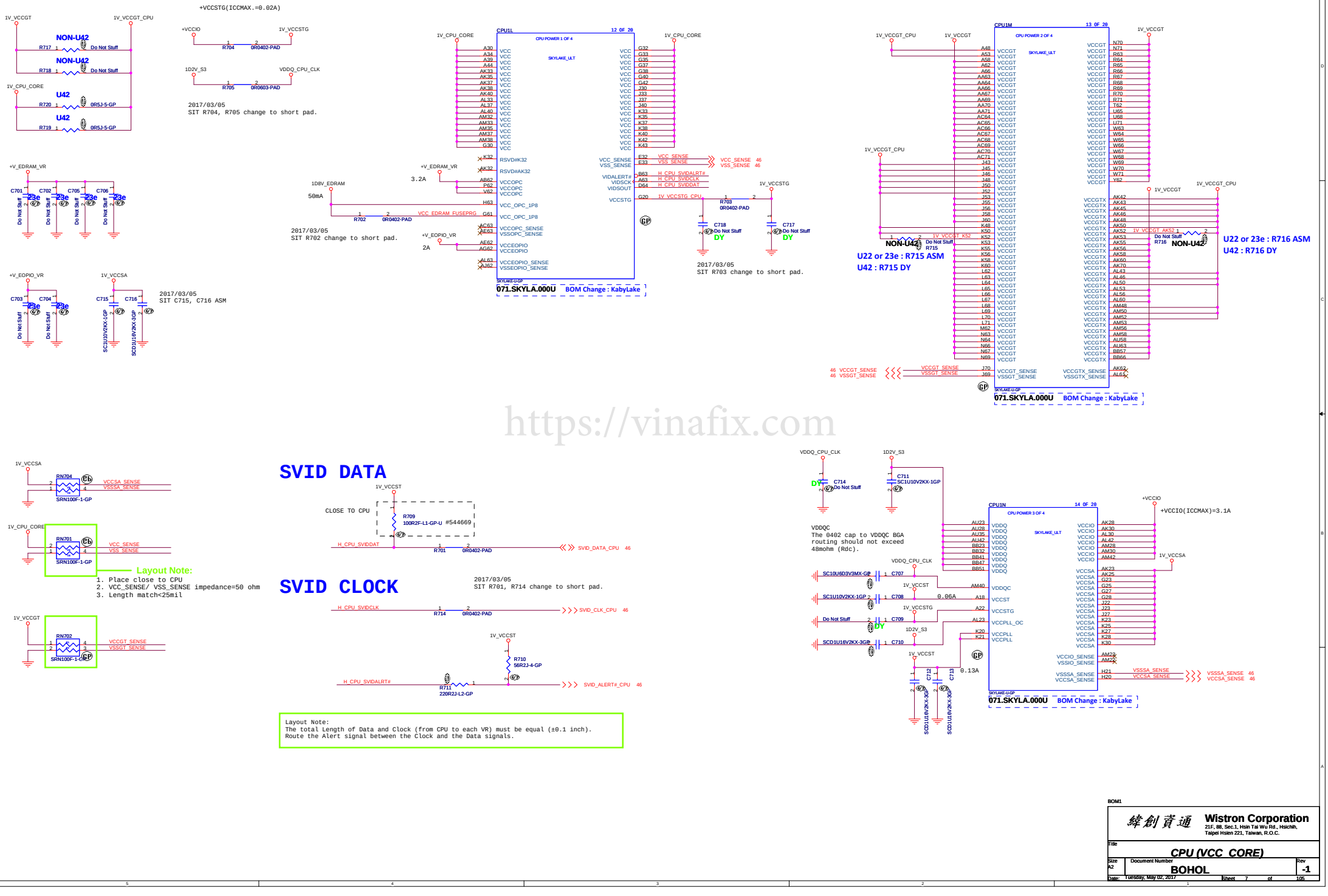
Title: CPU (CFG)

Size	Document Number	Rev
Custom	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 6 of 105

Main Func = CPU



BOM1

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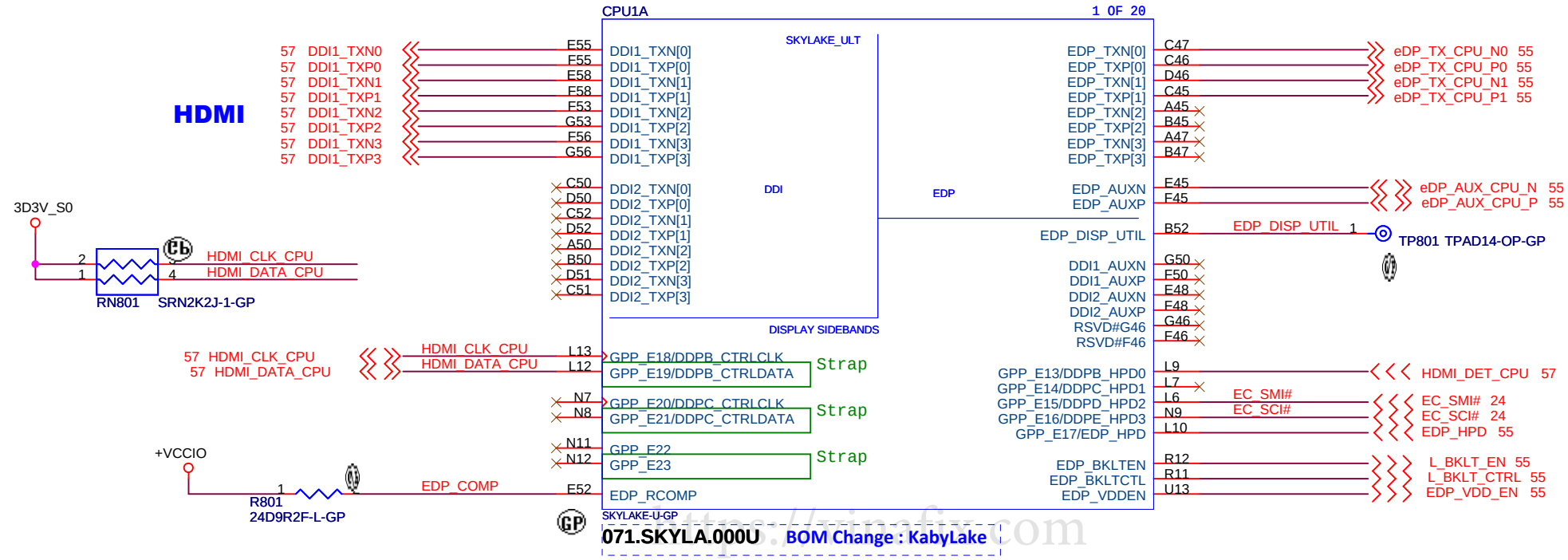
Title: CPU (VCC_CORE)

Size	Document Number	Rev
A2	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 7 of 105

Main Func = CPU

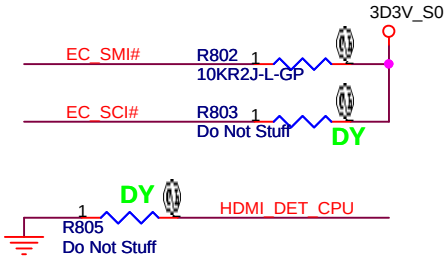


[561280] eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

[561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



BOM1

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Title: **CPU (DDI/EDP)**

Size	Document Number	Rev
A4	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 8 of 105

Main Func = CPU

(Blank)

BOM1

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Title	*CPU (RESERVED)*
Size: A4	Document Number: BOHOL
Rev: -1	
Date: Tuesday, May 02, 2017	Sheet 9 of 105

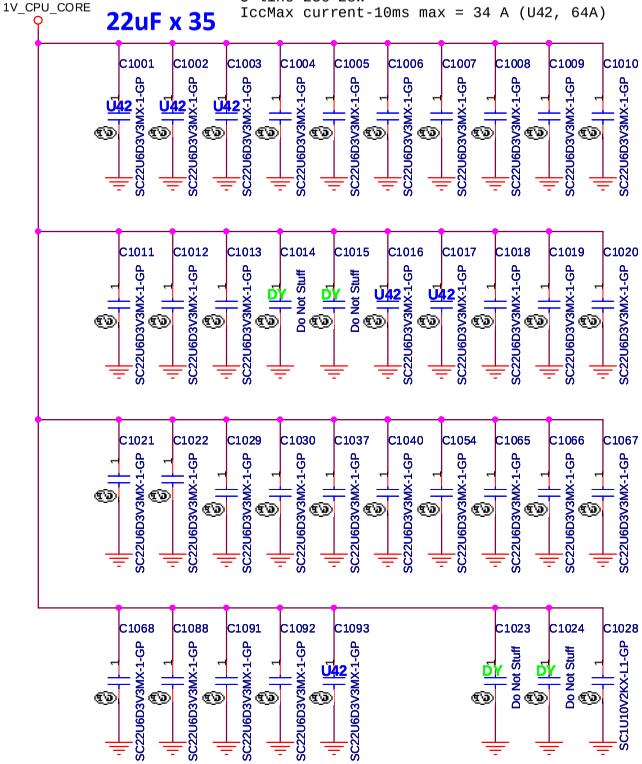
Main Func = CPU

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A (U42, 64A)

1V_CPU_CORE

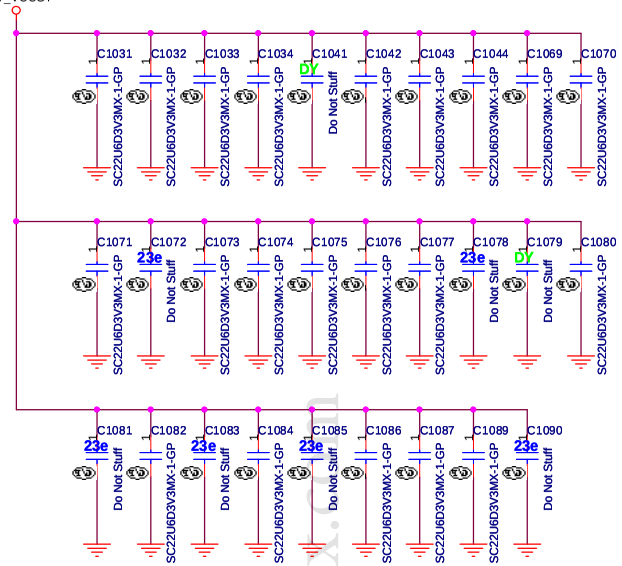
22uF x 35



SLICED GT

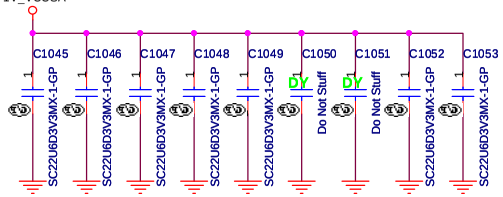
U-line 23e 28W
IccMax current-10ms max[A] = 67 A

1V_VCCGT



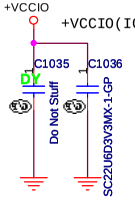
VCCSA

1V_VCCSA

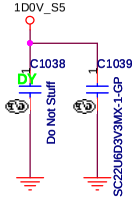


+VCCIO

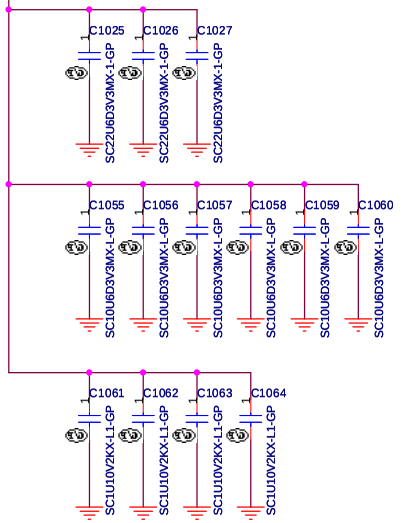
+VCCIO(ICCMAX.=2.73A)



1D0V_S5



1D2V_S3



BOM1

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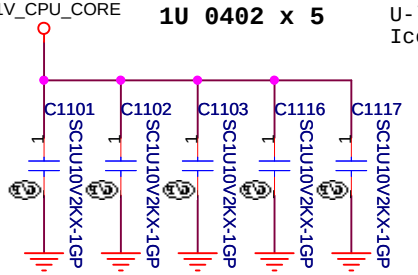
Title	CPU (POWER CAP1)	
Size A3	Document Number BOHOL	Rev -1
Date: Tuesday, May 02, 2017	Sheet 10 of 105	

Main Func = CPU

1V_CPU_CORE

1U 0402 x 5

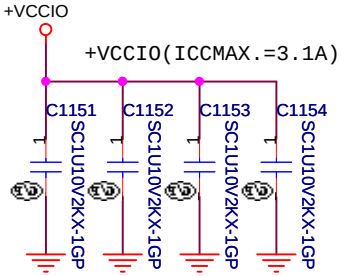
U-line 23e 28W
IccMax current-10ms max = 34 A



VCCIO

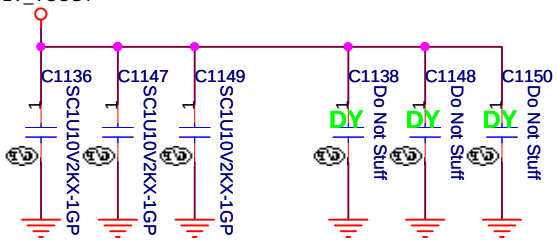
+VCCIO

+VCCIO(ICCMAX.=3.1A)



1V_VCCGT

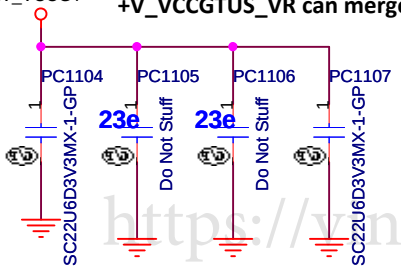
1U 0402 x 3



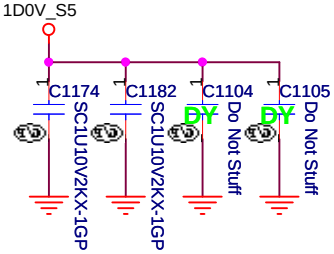
GTUS

1V_VCCGT

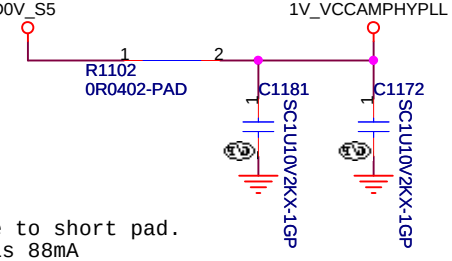
+V_VCCGTUS_VR can merge to +VCCGT



1D0V_S5



1D0V_S5 — 1V_VCCAMPHYPLL



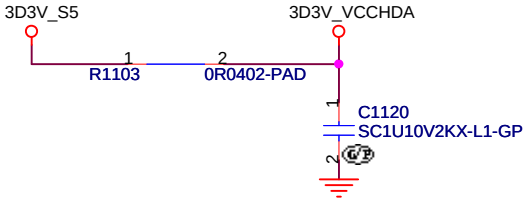
2017/03/05
SIT R1102 change to short pad.
1V_VCCAMPHYPLL is 88mA

c1181 place to far, change to 1uf_10v_0402

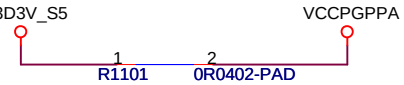
PCH DERIVED RAILS

VCCPGPPA(ICCMAX.=0.05A)

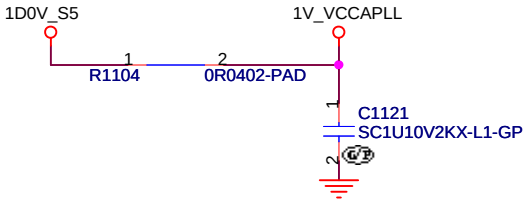
3D3V_S5 — 3D3V_VCCHDA



3D3V_S5 — VCCPGPPA



1D0V_S5 — 1V_VCCAPLL



2017/03/05
SIT R1101, R1103, R1104 change to short pad.

BOM1

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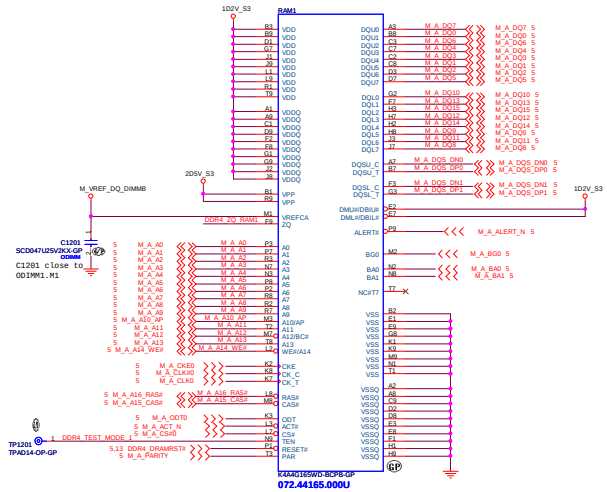
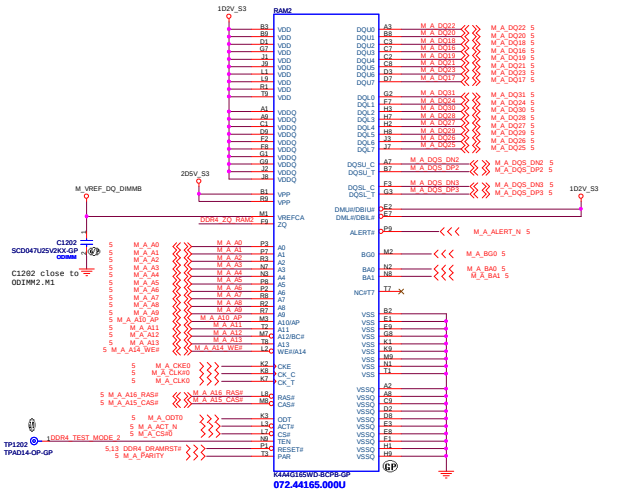
Title: *CPU (POWER CAP2)*

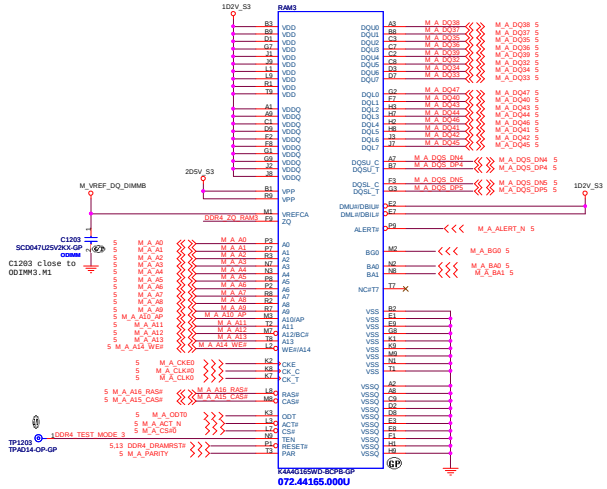
Size	Document Number	Rev
A4	BOHOL	-1

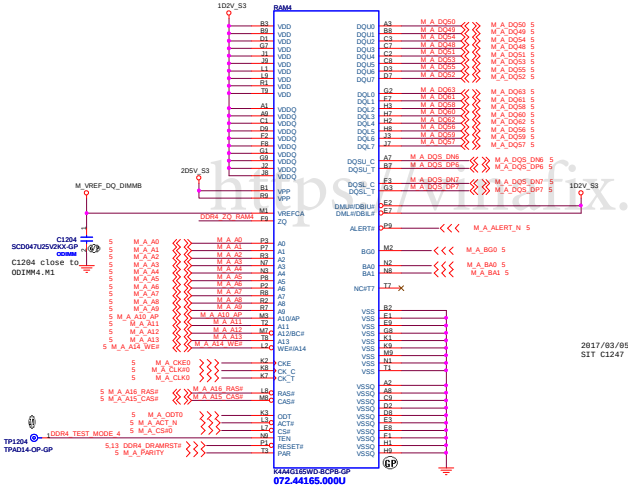
Date: Tuesday, May 02, 2017 Sheet 11 of 105

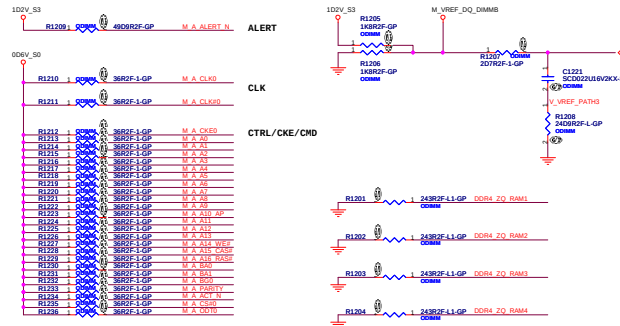
Main Func = DDR4 On Board with Single Rank

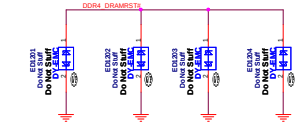








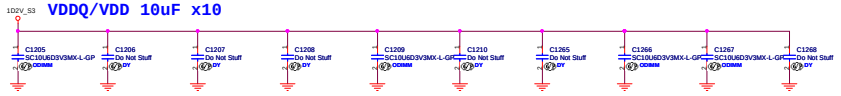




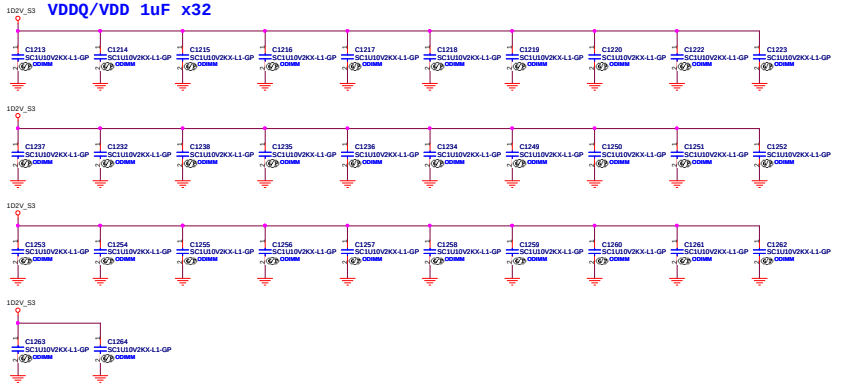
ED1202~ED1204 close to ODIMM1~ODIMM4

DDR4 On Board RAM Power Decouple Cap

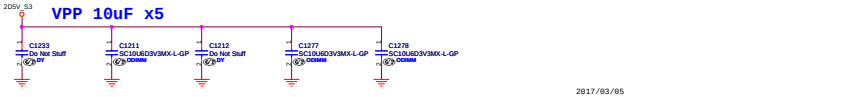
VDDQ/VDD 10uF x10



VDDQ/VDD 1uF x32

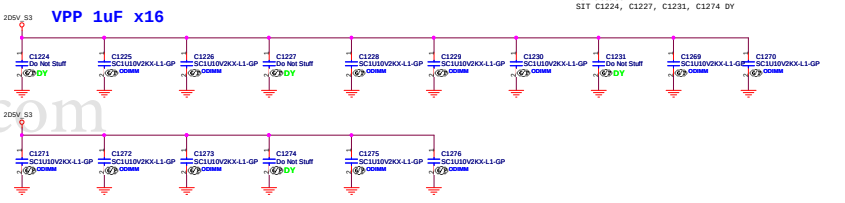


VPP 10uF x5



2017/03/05
SIT C1224, C1227, C1231, C1274 DY

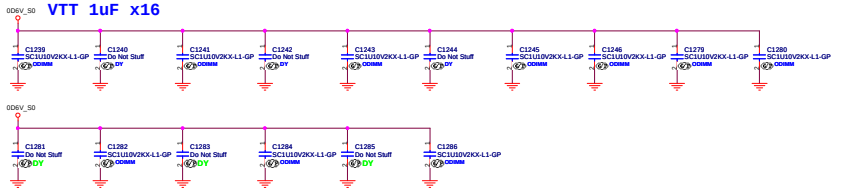
VPP 1uF x16



VTT 10uF x4

2017/03/05
SIT C1247 DY

VTT 1uF x16



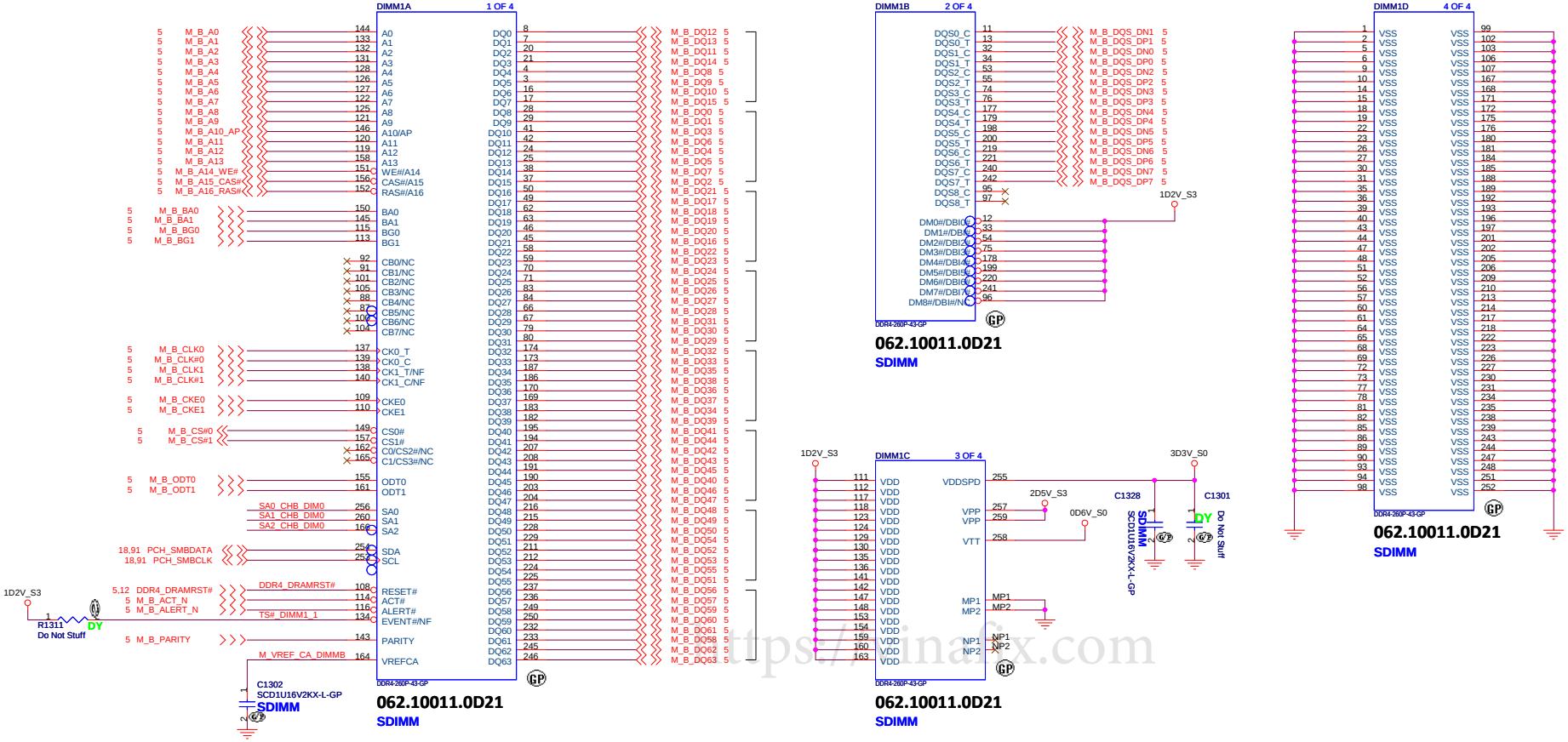
BOM1

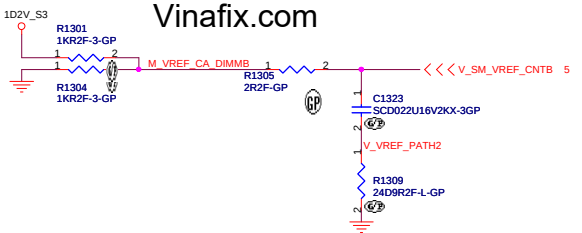
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

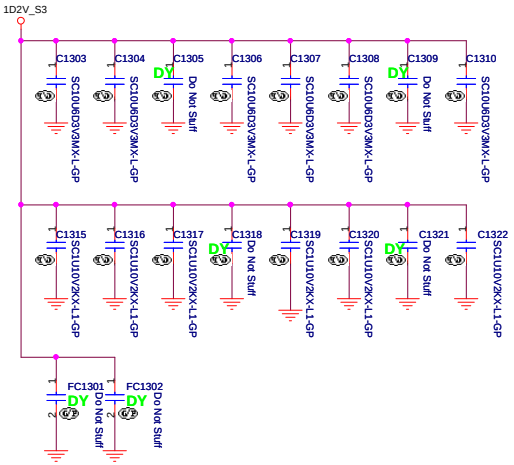
Title: DDR4 MEMORY DOWN

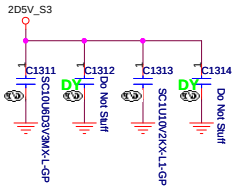
Size	Document Number	Rev
Custom	BOHOL	-1

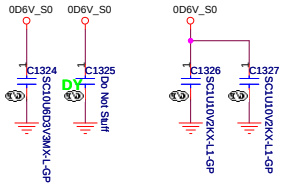
Date: Tuesday, May 02, 2017 Sheet 12 of 105

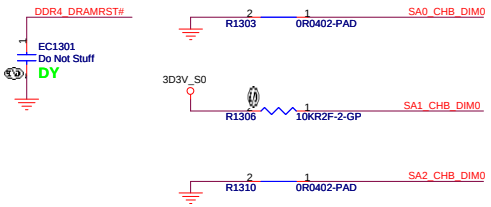












2017/03/05
SIT R1303, R1310 change to short pad.

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR4_SODIMM

Size	Document Number	Rev
Custom	BOHOL	-1

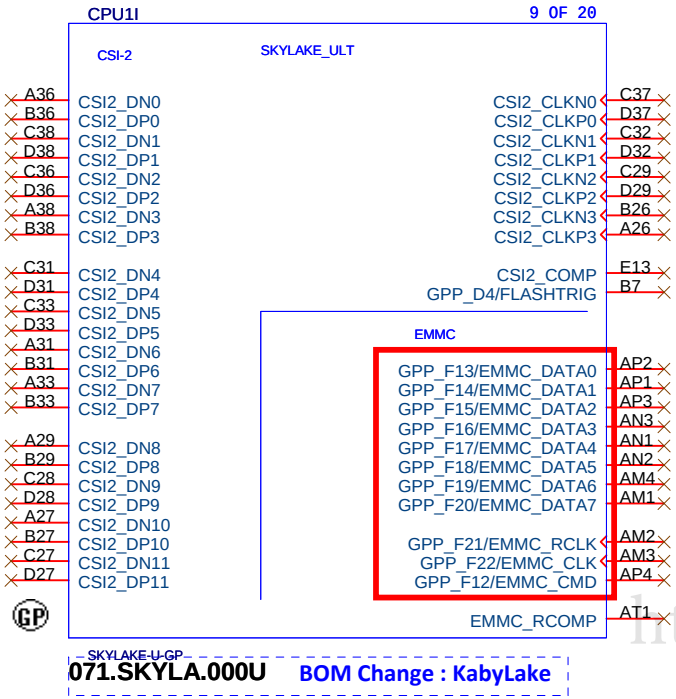
Date: Tuesday, May 02, 2017 Sheet 13 of 105

(Blank)

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 14 of 105	

Main Func = PCH



GPP_F: VCCPGPPF = 1.8V Only

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CPU (CSI2/EMMC)*		
Size: A4	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 15 of 105	

Main Func = PCH

[561280]
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

4 x 1 **GPU**

4 x 1 **M.2 SSD Optane PCIE only**

inform SW team
P / N swap
SSD : PETP0 pin
SSD : PETN0 pin

1 x 1 **LAN**

1 x 1 **WLAN**

1 x 1 **Card Reader**

SATA **HDD (SATA GEN.3)**

ED1601 Do Not Stuff
Do Not Stuff
DY-EMC
close to CPU

[561280] Both RCOMP & RCOMPN need to matched to less than 1%.

CPU1H 8 OF 20
SKYLAKE_ULT
SKYLAKE-U-GP
071.SKYLA.000U
BOM Change : KabyLake

[561280] The xHCI controller provides a USB 3.0 debug port capability on all SuperSpeed ports.

USB1 (USB3.0 Port1)
USB2 (USB3.0 Port2-AOU)
USB3 (USB3.0 Port3-TypeC)
1/18 For TYPEC Solution Change
USB1 (USB2.0 port1)
USB2 (USB2.0 Port2-AOU)
USB3 (TpyeC Port3)
CAMERA (USB2.0 Port5)
Bluetooth (USB2.0 Port8)
Finger Print

USBCOMP DC resistance < 0.5ohm.

[561280] When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

RN1601 SRN10KJ-6-GP
RN1602 SRN10KJ-6-GP
R1601 DY Do Not Stuff
ED1602 Do Not Stuff DY-EMC

PCIE Table

Port	PCIE Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0 (SSD)
8	M.2 SSD	SATA1A (SSD)
9	LAN	
10	WLAN	
11	Card Reader	N/A
12	N/A	HDD

SATA Table

Pair	SATA Device	Share BUS
0	N/A	PCIE7 (M.2 SSD)
1A	N/A	PCIE8 (M.2 SSD)
1B	N/A	PCIE11 (Card Reader)
2	HDD	N/A

USB 3.0 Table

Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Debug Port)	
2	USB3.0 Port2 (IOBD - AOU)	
3	USB3.0 Port3 (Type C)	
4	N/A	
5	N/A	PCIE1 (GPU)
6	N/A	PCIE2 (GPU)

USB 2.0 Table

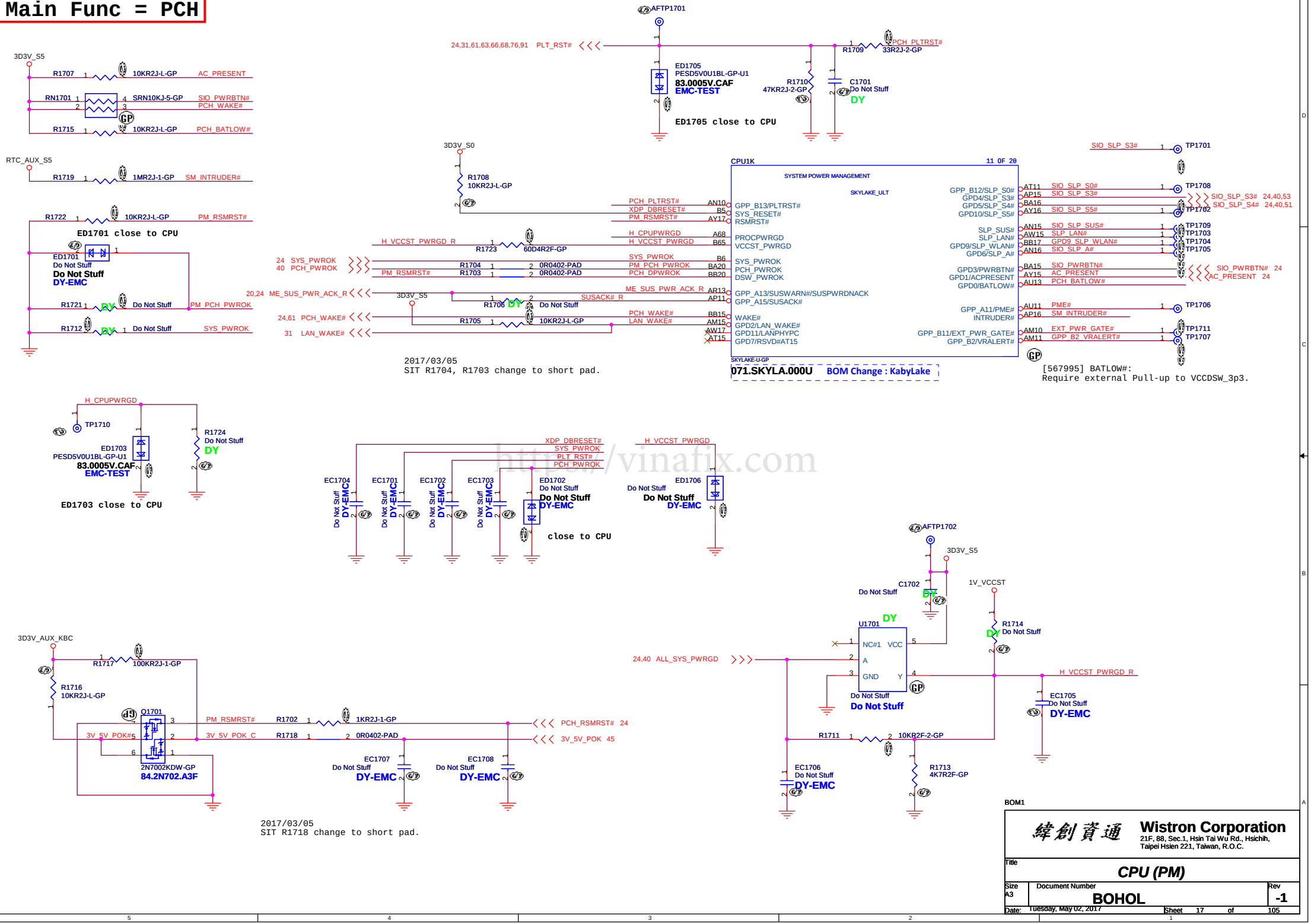
Pair	USB2.0 Device
1	USB3.0 port1 (Debug Port)
2	USB3.0 Port2 (IOBD - AOU)
3	USB3.0 Port3 (Type C)
4	N/A
5	CAMERA
6	N/A
7	N/A
8	Bluetooth
9	Finger Print
10	N/A

BOM1

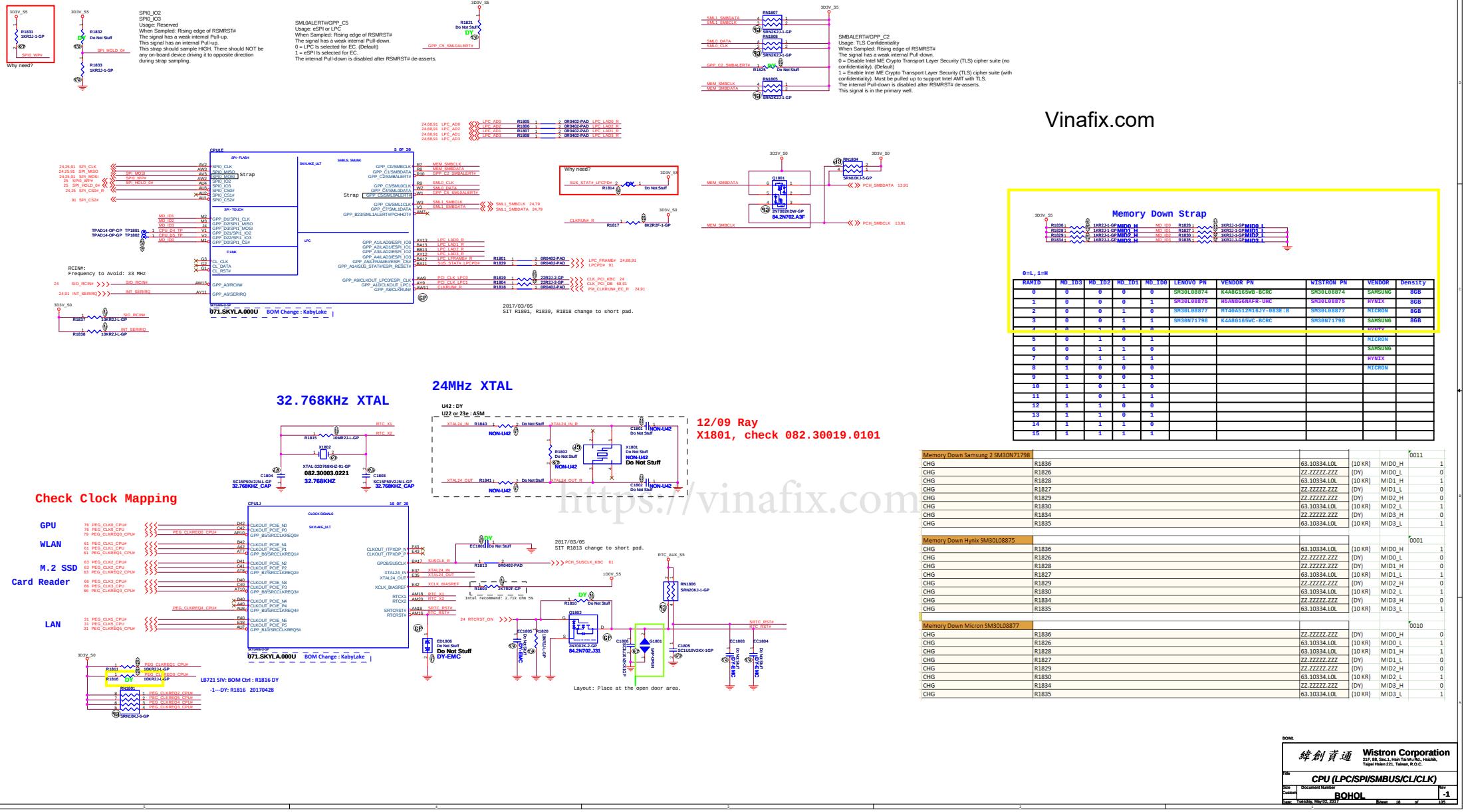
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)
Size: Custom | Document Number: BOHOL | Rev: -1
Date: Tuesday, May 02, 2017 | Sheet 16 of 105

Main Func = PCH



Main Func = PCH



Vinafix.com

Memory Down Strap

0=L, 1=H

RAMID	MD_ID3	MD_ID2	MD_ID1	MD_ID0	LENOVO PN	VENDOR PN	WISTRON PN	VENDOR	Density
0	0	0	0	0	SM30L08874	K4A8G165WB-BCRC	SM30L08874	SAMSUNG	8GB
1	0	0	0	1	SM30L08875	H5ANBG6NAFR-UHC	SM30L08875	HYNIX	8GB
2	0	0	1	0	SM30L08877	MT40A512M16JY-083E:B	SM30L08877	MICRON	8GB
3	0	0	1	1	SM30N71798	K4A8G165WC-BCRC	SM30N71798	SAMSUNG	8GB
4	0	1	0	0				HYNIX	
5	0	1	0	1				MICRON	
6	0	1	1	0				SAMSUNG	
7	0	1	1	1				HYNIX	
8	1	0	0	0				MICRON	
9	1	0	0	1					
10	1	0	1	0					
11	1	0	1	1					
12	1	1	0	0					
13	1	1	0	1					
14	1	1	1	0					
15	1	1	1	1					

Memory Down Samsung 2 SM30N71798				0011
CHG	R1836	63.10334.L0L	(10 KR)	MID0_H 1
CHG	R1826	ZZ.ZZZZZ.ZZZ	(DY)	MID0_L 0
CHG	R1828	63.10334.L0L	(10 KR)	MID1_H 1
CHG	R1827	ZZ.ZZZZZ.ZZZ	(DY)	MID1_L 0
CHG	R1829	ZZ.ZZZZZ.ZZZ	(DY)	MID2_H 0
CHG	R1830	63.10334.L0L	(10 KR)	MID2_L 1
CHG	R1834	ZZ.ZZZZZ.ZZZ	(DY)	MID3_H 0
CHG	R1835	63.10334.L0L	(10 KR)	MID3_L 1
Memory Down Hynix SM30L08875				0001
CHG	R1836	63.10334.L0L	(10 KR)	MID0_H 1
CHG	R1826	ZZ.ZZZZZ.ZZZ	(DY)	MID0_L 0
CHG	R1828	ZZ.ZZZZZ.ZZZ	(DY)	MID1_H 0
CHG	R1827	63.10334.L0L	(10 KR)	MID1_L 1
CHG	R1829	ZZ.ZZZZZ.ZZZ	(DY)	MID2_H 0
CHG	R1830	63.10334.L0L	(10 KR)	MID2_L 1
CHG	R1834	ZZ.ZZZZZ.ZZZ	(DY)	MID3_H 0
CHG	R1835	63.10334.L0L	(10 KR)	MID3_L 1
Memory Down Micron SM30L08877				0010
CHG	R1836	ZZ.ZZZZZ.ZZZ	(DY)	MID0_H 0
CHG	R1826	63.10334.L0L	(10 KR)	MID0_L 1
CHG	R1828	63.10334.L0L	(10 KR)	MID1_H 1
CHG	R1827	ZZ.ZZZZZ.ZZZ	(DY)	MID1_L 0
CHG	R1829	ZZ.ZZZZZ.ZZZ	(DY)	MID2_H 0
CHG	R1830	63.10334.L0L	(10 KR)	MID2_L 1
CHG	R1834	ZZ.ZZZZZ.ZZZ	(DY)	MID3_H 0
CHG	R1835	63.10334.L0L	(10 KR)	MID3_L 1

BOM1

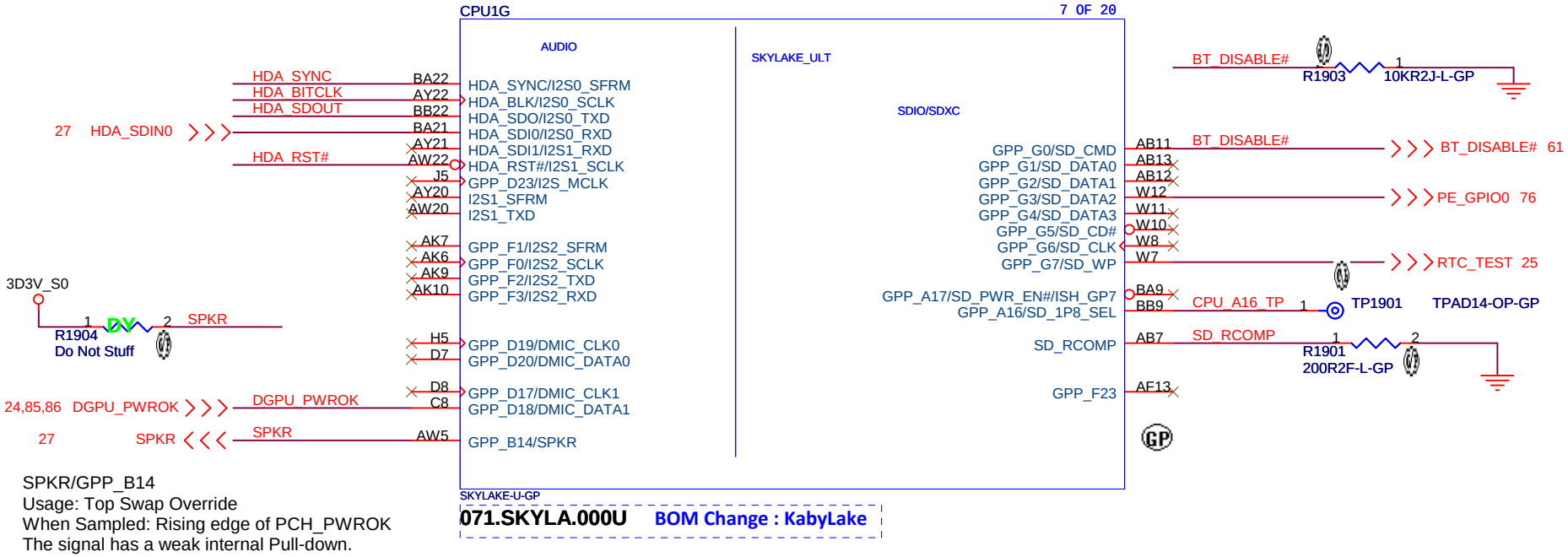
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPC/SPI/SMBUS/CL/CLK)

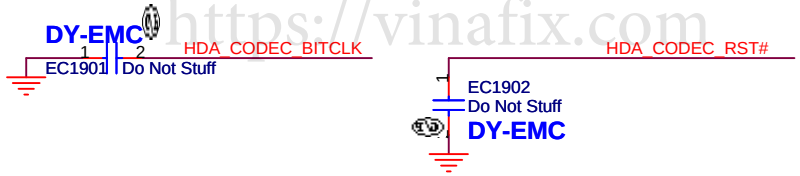
Size: Custom | Document Number: BOHOL | Rev: -1

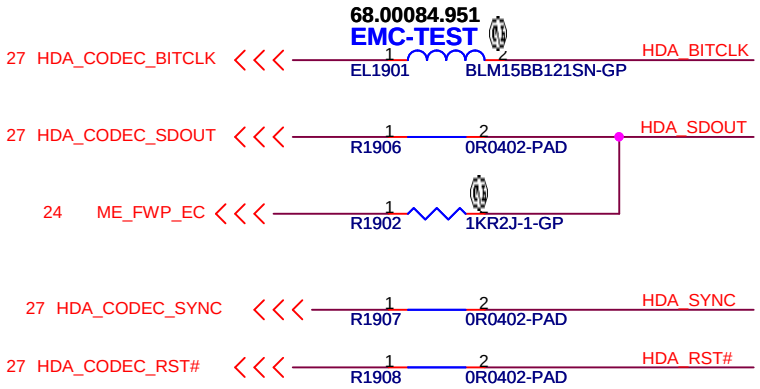
Date: Tuesday, May 02, 2017 | Sheet 18 of 105

Main Func = PCH



SPKR/GPP_B14
Usage: Top Swap Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable “Top Swap” mode. (Default)
1 = Enable “Top Swap” mode.
The internal Pull-down is disabled after
PCH_PWROK de-asserts.
This signal is in the primary well.





HDA_SDO /I2S_TXD0
Usage: Flash Descriptor Security Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Enable security measures defined in the Flash
Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This
strap should only be asserted high using external
Pull-up in manufacturing/debug environments
ONLY.
The internal Pull-down is disabled after PCH_PWROK de-asserts.

2017/03/05
SIT R1906, R1907, R1908 change to short pad.

BOM1

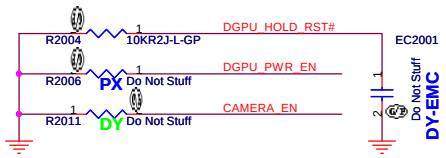
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (HDA/SDIO/SDXC)***

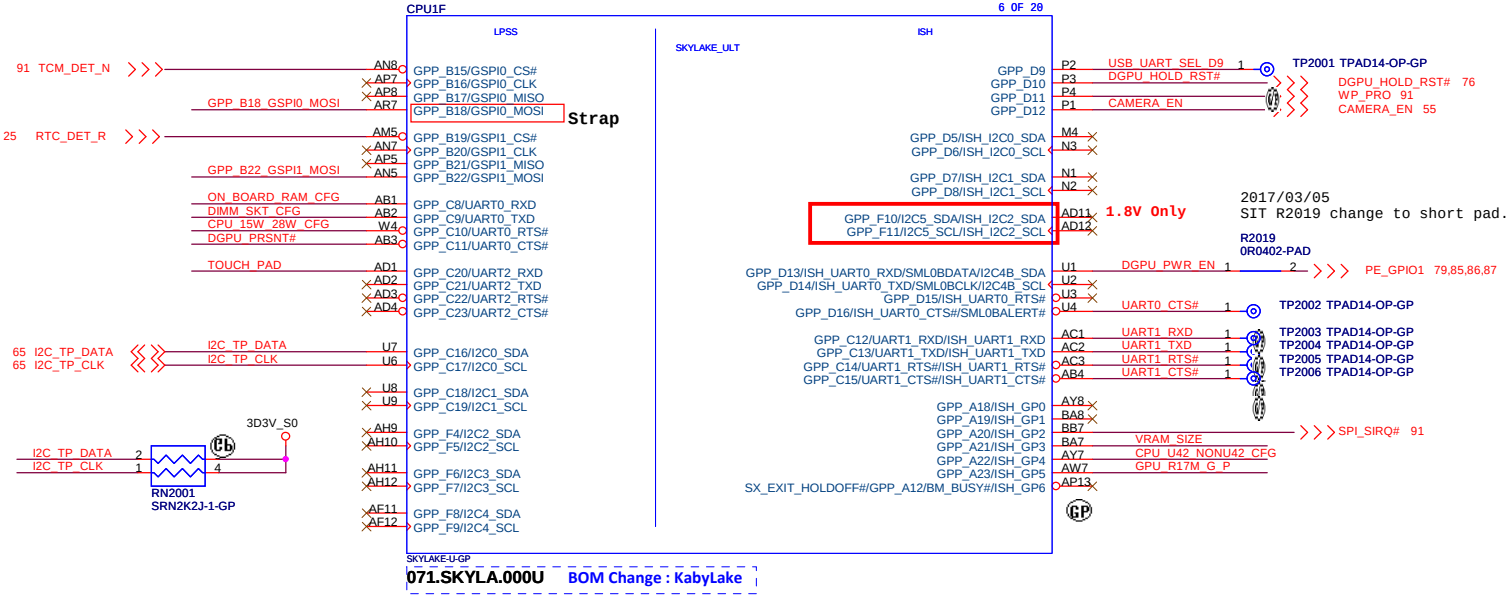
Size	Document Number	Rev
A4	BOHOL	-1

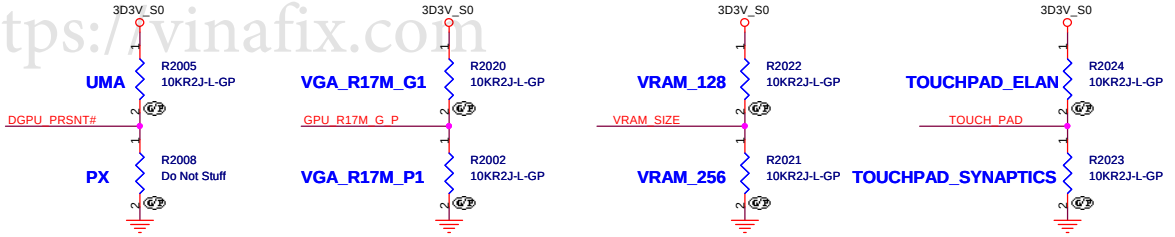
Date: Tuesday, May 02, 2017 Sheet 19 of 105

Main Func = PCH

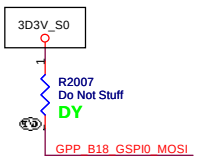


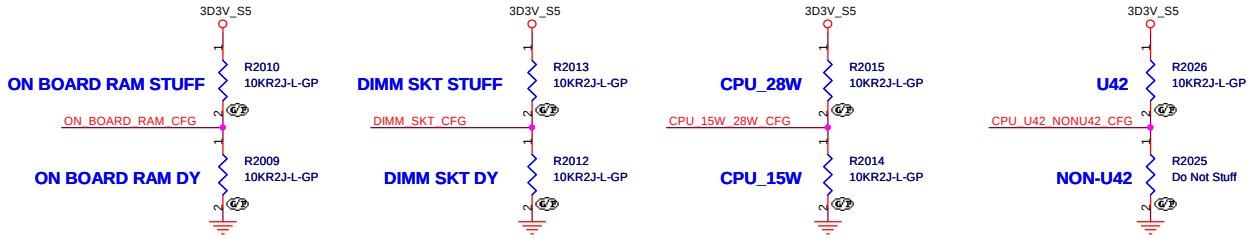
GSPI1_MOSI/GPP_B22
Usage: Boot BIOS Strap Bit BBS
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC
The internal Pull-down is disabled after PCH_PWROK de-asserts.





GSPI0_MOSI/GPP_B18
Usage: No Reboot
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable “No Reboot” mode. (Default)
1 = Enable “No Reboot” mode (PCH will disable the
TCO Timer system reboot feature). This function is useful when running ITP/XDP.
The internal Pull-down is disabled after PCH_PWROK de-asserts.





BOM1

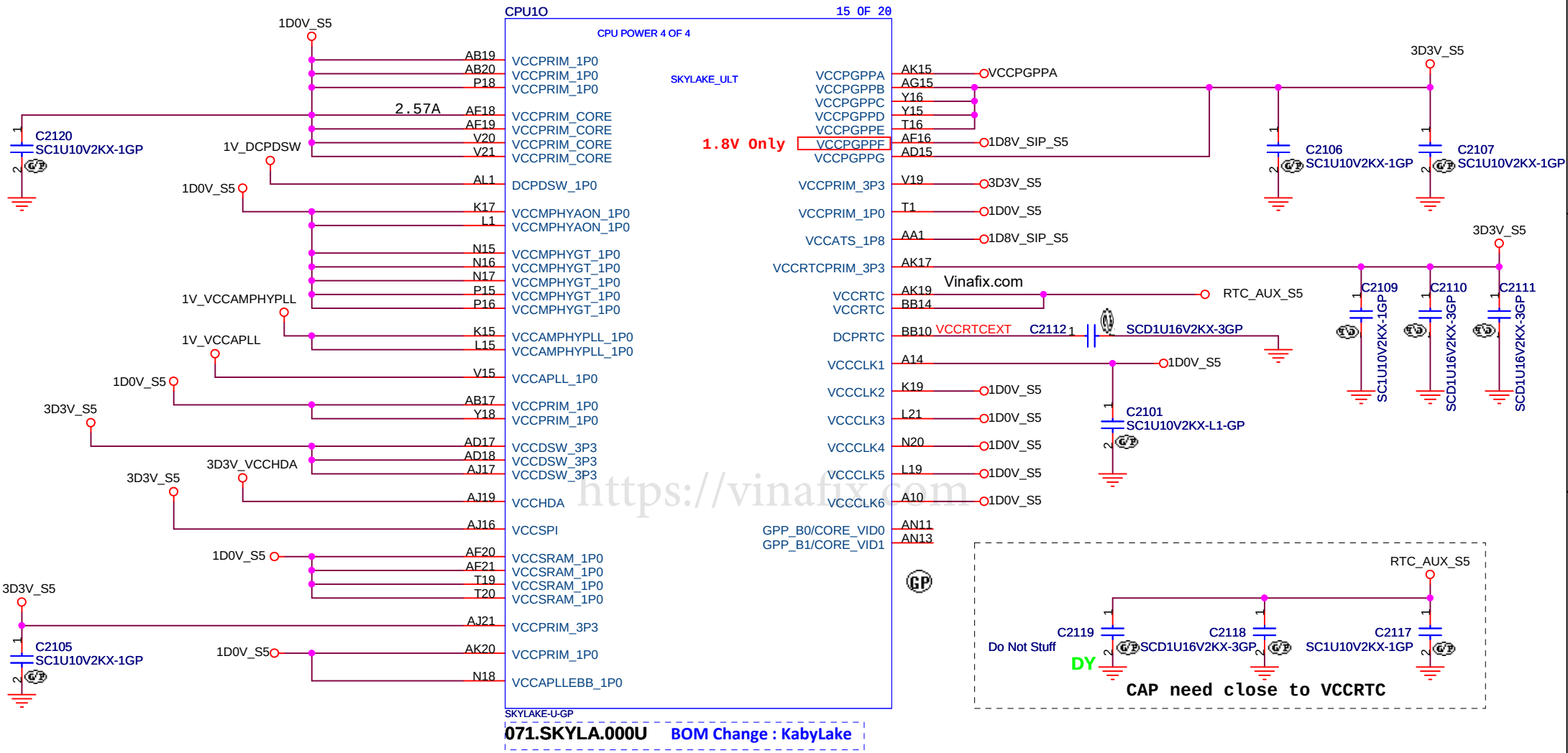
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

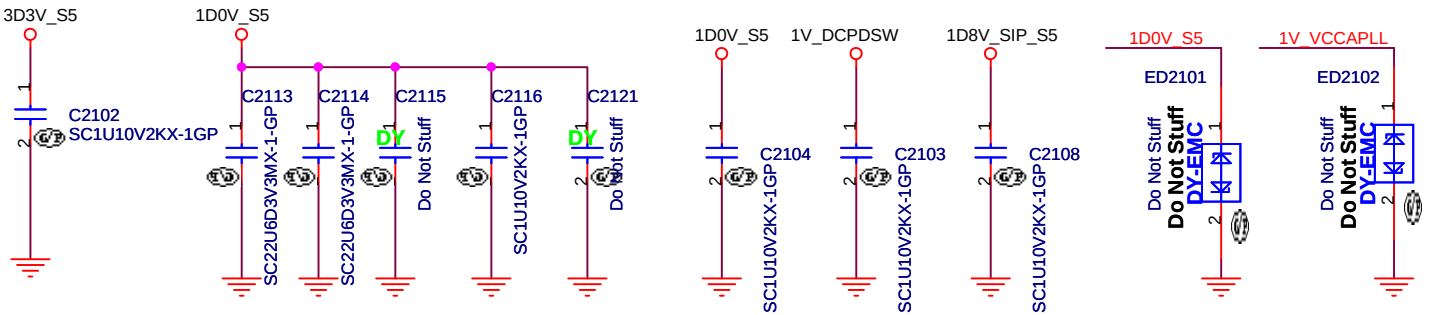
Title: CPU (LPSS/UART/ISH)

Size: A3 | Document Number: BOHOL | Rev: -1

Date: Tuesday, May 02, 2017 | Sheet 20 of 105

Main Func = PCH





BOM1

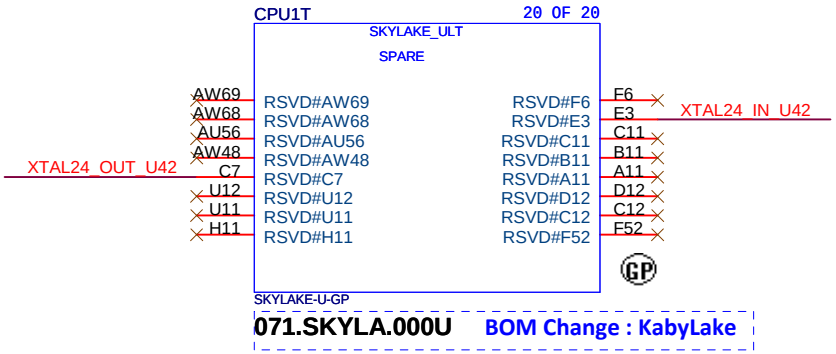
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

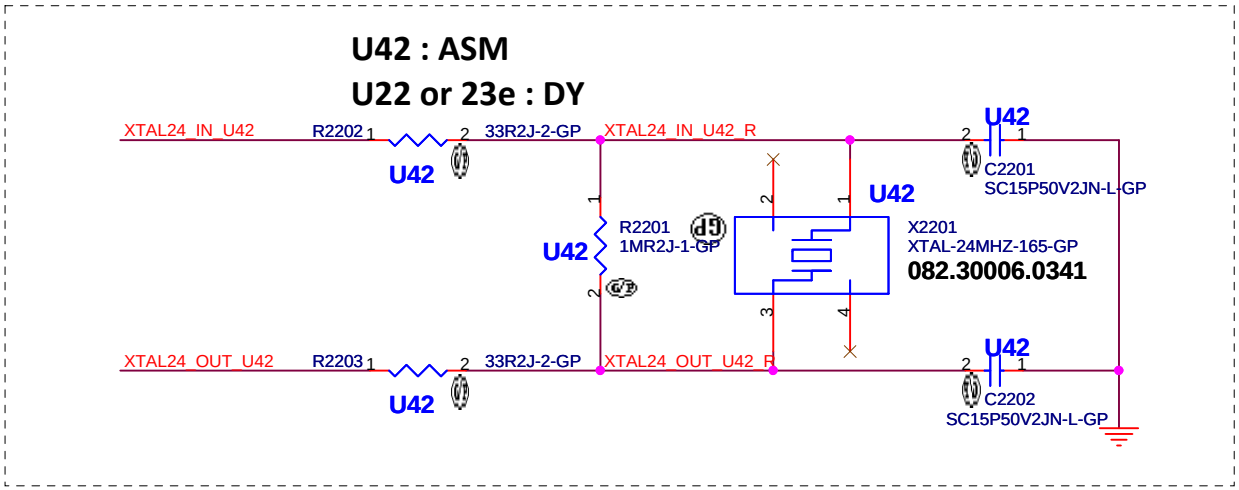
Size	Document Number	Rev
A4	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 21 of 105

Main Func = PCH



24MHz XTAL



BOM1

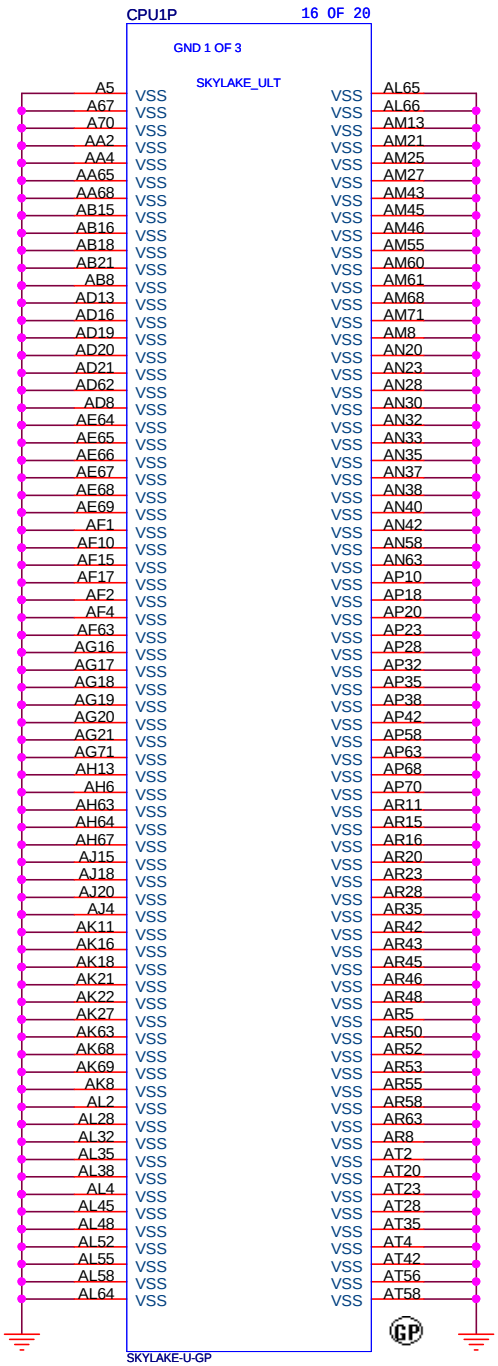
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

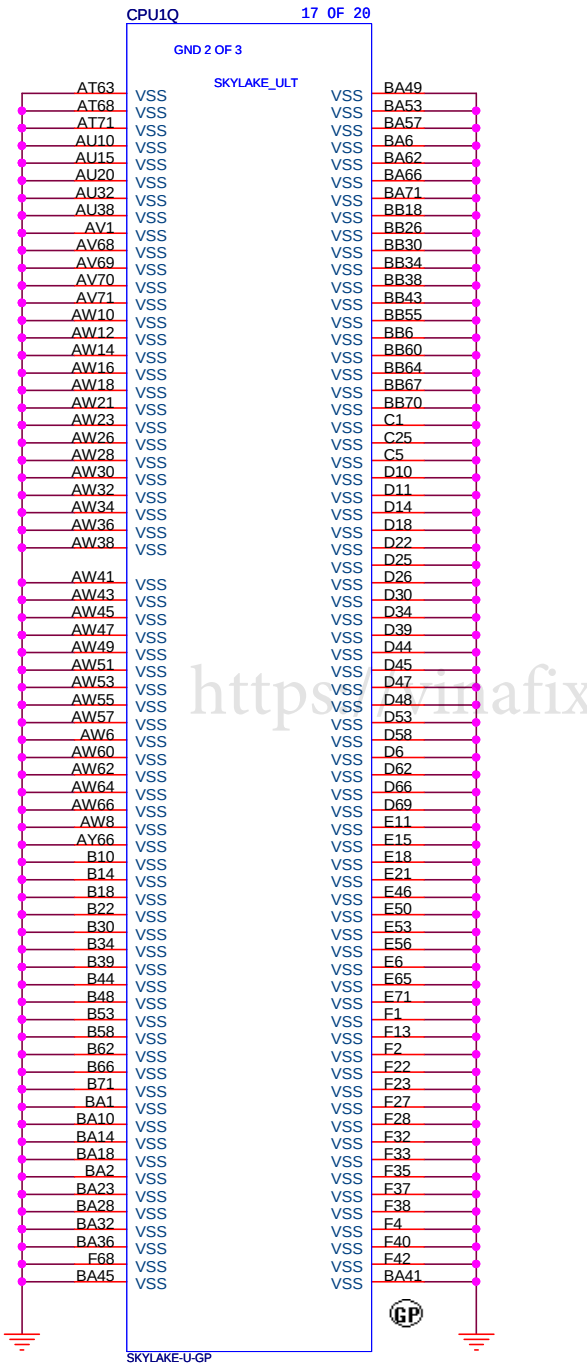
Title: ***CPU (RSVD)***

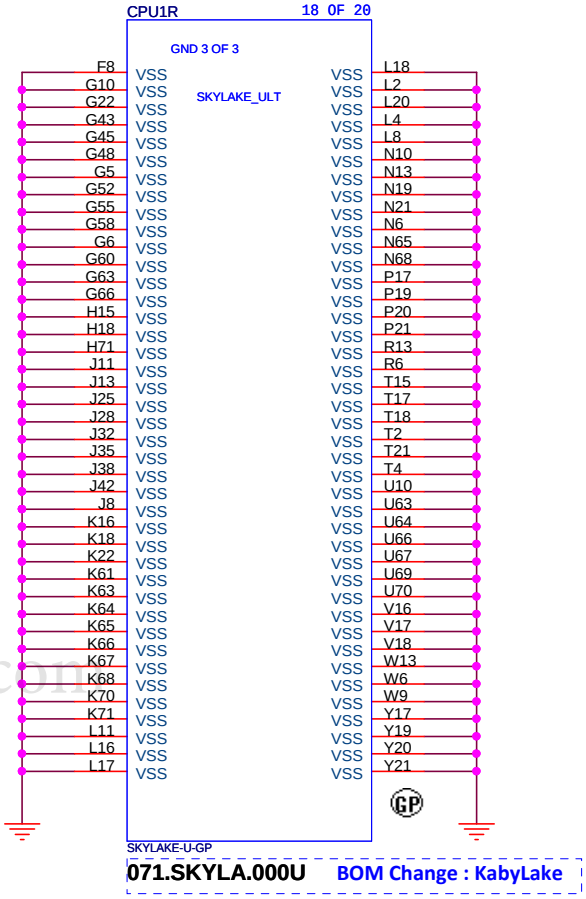
Size	Document Number	Rev
A4	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 22 of 105

Main Func = PCH







BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
Custom	**BOHOL**	-1

Date: Tuesday, May 02, 2017 Sheet 23 of 105

SSID = KBC

2017/03/05
SIT R2425 change to 0402 size
R2415 change to 0402 short pad.

NPCE285G

U2402
NPCE285PA0DX-2-GP
071.00285.0C0G

2016/11/18 U2402 Change Part Number to 071.00285.0C0G(285P)

2017/03/05
SIT R2423 change to short pad.

Thermal VD

BATTERY / CHARGER ---->

TP---->

2017/03/05
SIT ADD R2458, ADU Status pin is OD.

2017/03/05
SIT R2448, R2434, R2403 change to short pad.

Thermal VD

EMI
R2436
0R0402-PAD

2017/03/05
SIT R2436, R2430 change to short pad.

NOTE:
Locate resistors R2415 and R2417 close to the U2401.

close to U2402 KBC

NOTE:
Please be aware that the SPI interface trace length between PCH and EC should not exceed 650mils.. The mismatch of SPI interface signals between EC and SPI flash should not exceed 500mils.

KBC PWR supply at PSL mode.

2017/03/05
SIT R2454, R2414, R2419
R2418 change to short pad.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

NOTE:
PWM Signal :
1. If unused, select alternative GPIO function and enable internal pull-down.
2. Please measure and make sure that the rise time of VCC_POR is less than 10us.

R2431 close to Pin103

2017/03/05
SIT R2431 change to short pad.

Model_ID_BOM Ctrl

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LB720 IntelKabylake U	100.0K	10.0K 64.10025.6DL	3.0V
LB721 IntelKabylake U	100.0K	20.0K 64.20025.1.0L	2.75V
NA	100.0K	33.0K 64.33025.1.0L	2.48V
NA	100.0K	47.0K 64.47025.6DL	2.24V
NA	100.0K	64.9K 64.64925.6DL	2.0V
NA	100.0K	76.8K 64.76825.6DL	1.87V
NA	100.0K	215.0K 64.21535.6DL	1.048V

SPEC: ADT PWR Detection Function V1 3

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-1M	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

DELTA Model:ADP65FD BB-PD03 ADP

PIN 3 PIN 1 PIN 2

TABLE	
PIN 1	SIGNAL 287~ohm(1% TOLERANCE)
PIN 3	------
PIN 2	

ADP internal Resis 287ohm
3.3*287/1037=0.91V (65W)

45W_65W#
High: 45W / Low 65W
DISCRETE#
High: UMA / Low: Discrete

AC Adapter	ADT_TYPE	System Power Limit
130W	1.683V < ID <= 2.109V	90W
90W	1.172V < ID <= 1.618V	90W
SA 65W	0.693V < ID <= 1.134V	65W
45W	0.234V < ID <= 0.663V	45W

Prevent BIOS data loss solution

EC GPIO PH

EC GPIO PL

Nuvoton KBC PSL Power Switched Logic

1.Enter PSL mode (Entry S5 after 10sec) :
3D3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)

PSL mode(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Hi	Low	OFF

PSL Wake(AC or DC):		
EC_ENABLE#_G	S5_ENABLE	3D3V_AUX_KBC
Low	Hi	ON

EC_GPIO47 High Active

NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.		
KBC_NOVO_BTN#	KBC_PWRBTN_EC#	
Low	Low	

KBC_PWRBTN_EC#:Low
(1) 4sec: PWR Button shut down
(2) 8sec: KBC reset

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC NPCE285

Size	Document Number	Rev
A1	BOHOL	-1

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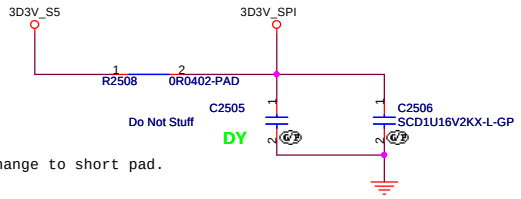
SSID = Flash.ROM

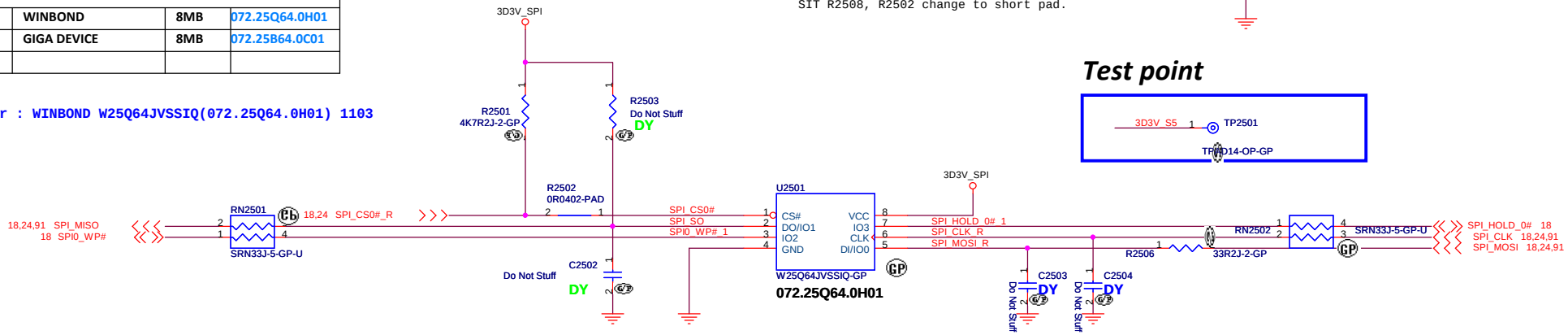
SPI ROM Equal length need to less than 500mil

U2502			
1ST	WINBOND	8MB	072.25Q64.0H01
2ND	GIGA DEVICE	8MB	072.25B64.0C01
3RD			

vendor : WINBOND W25Q64JVSSIQ(072.25Q64.0H01) 1103

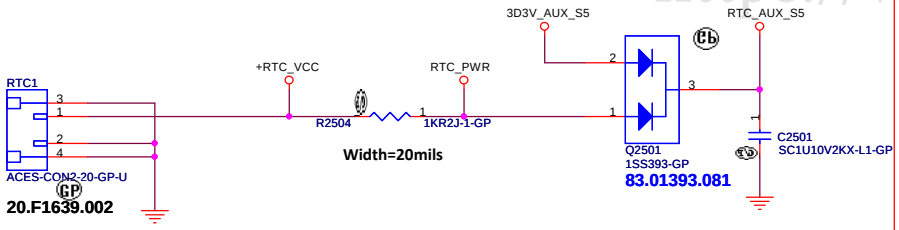
2017/03/05
SIT R2508, R2502 change to short pad.



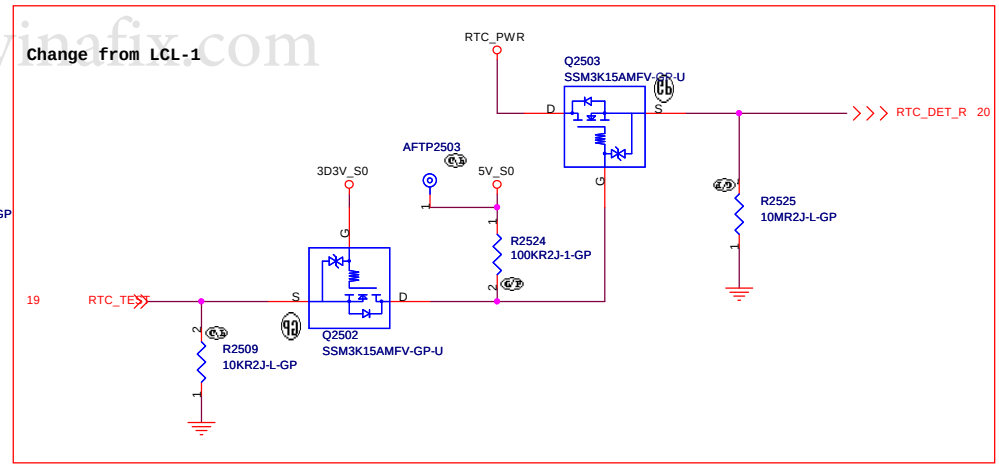


Test point

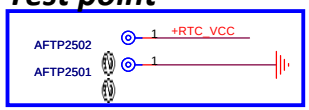
SSID = RBATT



Change from LCL-1



Test point



High Detect
Need to Check whether to PD in PCH Side

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPI/RTC

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A3	BOHOL	-1

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Main Func = Thermal Sensor

Close to Thermal sensor

@CPU

Close to CPU chips

3D3V_AUX_KBC
R2611 16KR2F-GP
R2606 NTC-100K-11-GP-U 69.60013.201
C2610 SCD1U16V2KX-L-GP
C2611 SC100P50V2JN-3GP
VD_IN1 24
VD_IN1_C
R2608 0R0402-PAD

@GPU

Close to KBC chips

3D3V_AUX_KBC
R2612 16KR2F-GP
R2615 NTC-100K-11-GP-U 69.60013.201
C2612 SCD1U16V2KX-L-GP
C2613 SC100P50V2JN-3GP
VD_IN2 24
VD_IN2_C
R2616 0R0402-PAD

@On Board DIMM

Close to KBC chips

3D3V_AUX_KBC
TV
R2618 16KR2F-GP
R2621 NTC-100K-11-GP-U 69.60013.201
C2617 SCD1U16V2KX-L-GP
C2618 SC100P50V2JN-3GP
VD_IN3 24
VD_IN3_C
R2617 0R0402-PAD

2017/03/05
SIT U2602 and related circuit.

2017/03/05
SIT R2608, R2616, R2617,
R2602, R2613
R2623 change to short pad

20161219
Need check resistor value

3D3V_S0
R2605 2KR2F-3-GP
R2614 DY Do Not Stuff
R2613 0R0402-PAD
VD_OUT1# 24
VD_OUT2# 24
D2603 Do Not Stuff
Q2602 2N7002K-2-GP 84.2N702.J31
THERM_SYS_SHDN#
24,40 PURE_HW_SHUTDOWN#
R2604 Do Not Stuff DY
C2606 Do Not Stuff DY
R2602 0R0402-PAD

3D3V_S0
R2610 10KR2J-L-GP
24 FAN_TACH1
D2602 RB551V30-GP 83.R5003.H8H
FAN_TACH1_C
24,89 FAN1_PWM1
24,89 FAN1_PWM2
5V_FAN_S0
FAN1
ACES-CON8-13-GP-U2 20.F1295.008

3D3V_S0
R2628 10KR2J-L-GP
24 FAN_TACH2
D2605 RB551V30-GP 83.R5003.H8H
FAN_TACH2_C

AFTP2607
5V_S0
R2623 0R0603-PAD
D2601 RB551V30-GP 83.R5003.H8H
5V_FAN_S0
C2603 C2604 SCD1U16V2KX-L-GP

AFTP2601
AFTP2602
AFTP2603
AFTP2604
AFTP2605
AFTP2606
FAN1_PWM1
FAN_TACH1_C
5V_FAN_S0
FAN1_PWM2
FAN_TACH2_C
FAN_TACH1_C 89
FAN_TACH2_C 89

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL/FAN
Size: Custom
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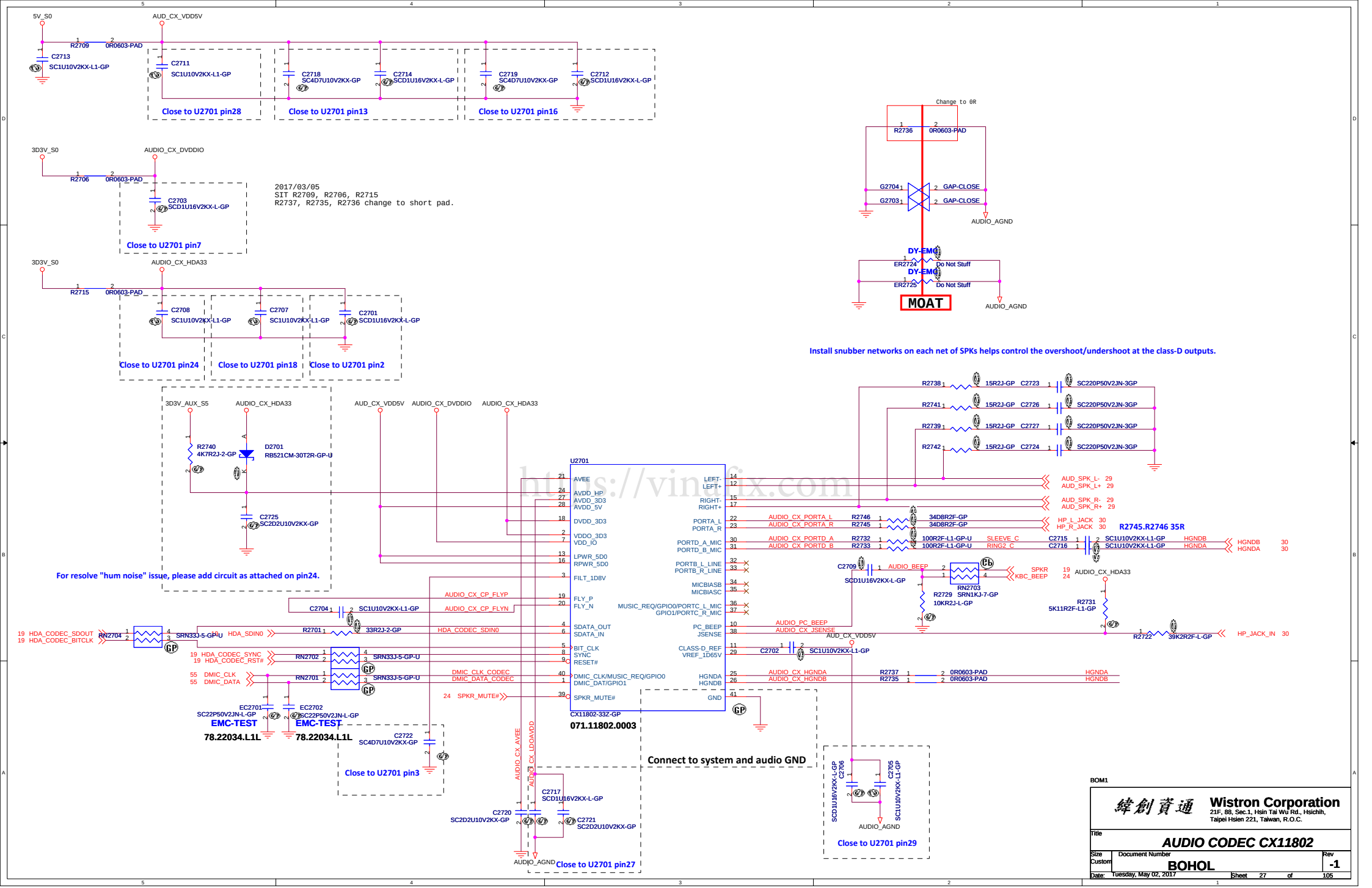
5V_S0
AUD_CX_VDD5V
R2709 0R0603-PAD
C2713 SC1U10V2KX-L1-GP
C2711 SC1U10V2KX-L1-GP
C2718 SC4D7U10V2KX-GP
C2714 SCD1U16V2KX-L-GP
C2719 SC4D7U10V2KX-GP
C2712 SCD1U16V2KX-L-GP
Close to U2701 pin28
Close to U2701 pin13
Close to U2701 pin16
3D3V_S0
AUDIO_CX_DVDDIO
R2706 0R0603-PAD
C2703 SCD1U16V2KX-L-GP
Close to U2701 pin7
2017/03/05
SIT R2709, R2706, R2715
R2737, R2735, R2736 change to short pad.
3D3V_S0
AUDIO_CX_HDA33
R2715 0R0603-PAD
C2708 SC1U10V2KX-L1-GP
C2707 SC1U10V2KX-L1-GP
C2701 SCD1U16V2KX-L-GP
Close to U2701 pin24
Close to U2701 pin18
Close to U2701 pin2
Change to 0R
R2736 0R0603-PAD
G2704 GAP-CLOSE
G2703 GAP-CLOSE
AUDIO_AGND
DY-EMC
ER2724 Do Not Stuff
DY-EMC
ER2725 Do Not Stuff
MOAT
AUDIO_AGND
Install snubber networks on each net of SPKs helps control the overshoot/undershoot at the class-D outputs.
3D3V_AUX_S5
AUDIO_CX_HDA33
R2740 4K7R2J-2-GP
D2701 RB521CM-30T2R-GP-U
C2725 SC2D2U10V2KX-GP
For resolve "hum noise" issue, please add circuit as attached on pin24.
AUD_CX_VDD5V
AUDIO_CX_DVDDIO
AUDIO_CX_HDA33
U2701
CX11802-33Z-GP
071.11802.0003
R2738 15R2J-GP C2723 SC220P50V2JN-3GP
R2741 15R2J-GP C2726 SC220P50V2JN-3GP
R2739 15R2J-GP C2727 SC220P50V2JN-3GP
R2742 15R2J-GP C2724 SC220P50V2JN-3GP
AUD_SPK_L- 29
AUD_SPK_L+ 29
AUD_SPK_R- 29
AUD_SPK_R+ 29
AUDIO_CX_PORTA_L R2746 34D8R2F-GP HP_L_JACK 30
AUDIO_CX_PORTA_R R2745 34D8R2F-GP HP_R_JACK 30
R2745.R2746 35R
AUDIO_CX_PORTD_A R2732 100R2F-L1-GP-U SLEEVE_C C2715 SC1U10V2KX-L1-GP HGNDB
AUDIO_CX_PORTD_B R2733 100R2F-L1-GP-U RING2_C C2716 SC1U10V2KX-L1-GP HGNDA
HGNDB 30
HGNDA 30
C2709 SCD1U16V2KX-L-GP
AUDIO_BEEP
RN2703 R2729 SRN1KJ-7-GP 10KR2J-L-GP
SPKR 19
KBC_BEEP 24
AUDIO_CX_HDA33
R2731 5K11R2F-L1-GP
R2722 39K2R2F-L-GP
HP_JACK_IN 30
AUDIO_PC_BEEP
AUDIO_CX_JSENSE
AUD_CX_VDD5V
C2702 SC1U10V2KX-L1-GP
AUDIO_CX_HGNDA R2737 0R0603-PAD HGNDA
AUDIO_CX_HGNDB R2735 0R0603-PAD HGNDB
C2704 SC1U10V2KX-L1-GP
AUDIO_CX_CP_FLYP
AUDIO_CX_CP_FLYN
19 HDA_CODEC_SDOUT
19 HDA_CODEC_BITCLK
RN2704 SRN33J-5-GP-U
HDA_SDIN0
R2701 33R2J-2-GP
HDA_CODEC_SDIN0
19 HDA_CODEC_SYNC
19 HDA_CODEC_RST#
RN2702 SRN33J-5-GP-U
55 DMIC_CLK
55 DMIC_DATA
RN2701 SRN33J-5-GP-U
DMIC_CLK_CODEC
DMIC_DATA_CODEC
24 SPKR_MUTE#
EC2701 SC22P50V2JN-L-GP
EC2702 SC22P50V2JN-L-GP
EMC-TEST
78.22034.L1L
EMC-TEST
78.22034.L1L
C2722 SC4D7U10V2KX-GP
Close to U2701 pin3
Connect to system and audio GND
AUDIO_CX_AVEE
AUDIO_CX_LDOAVDD
C2717 SCD1U16V2KX-L-GP
C2720 SC2D2U10V2KX-GP
C2721 SC2D2U10V2KX-GP
AUDIO_AGND
Close to U2701 pin27
C2706 SCD1U16V2KX-L-GP
C2705 SC1U10V2KX-L1-GP
AUDIO_AGND
Close to U2701 pin29
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC CX11802
Size Custom
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Rev -1
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
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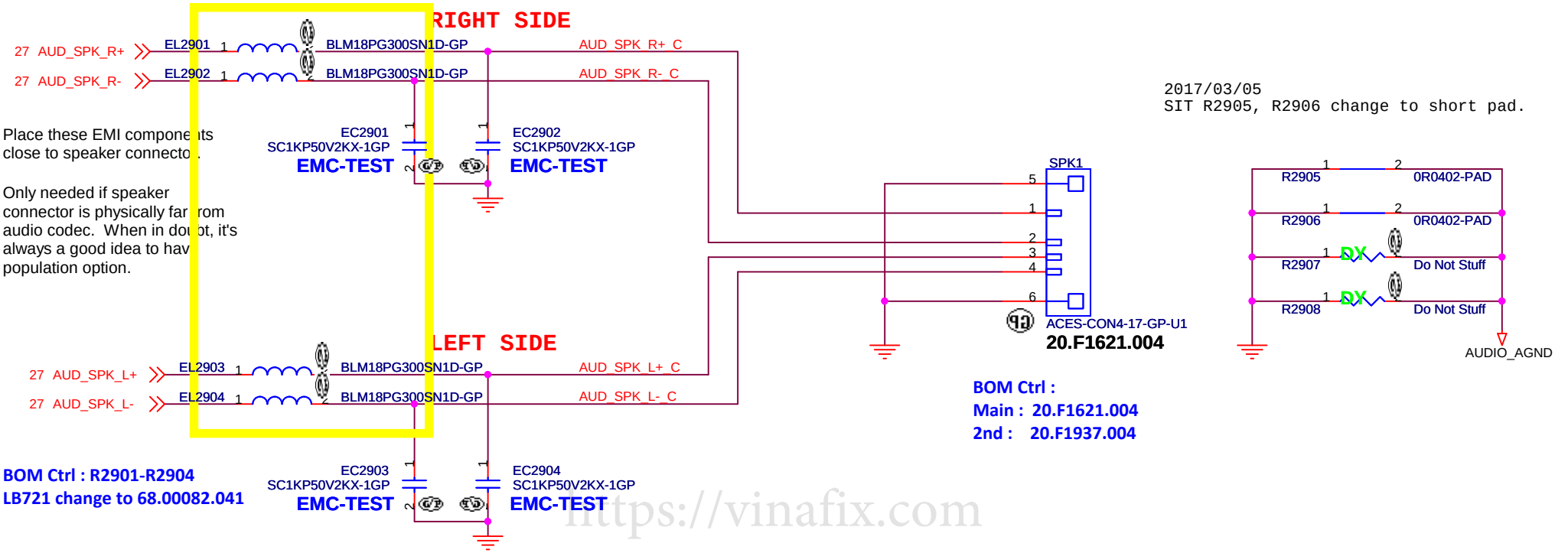
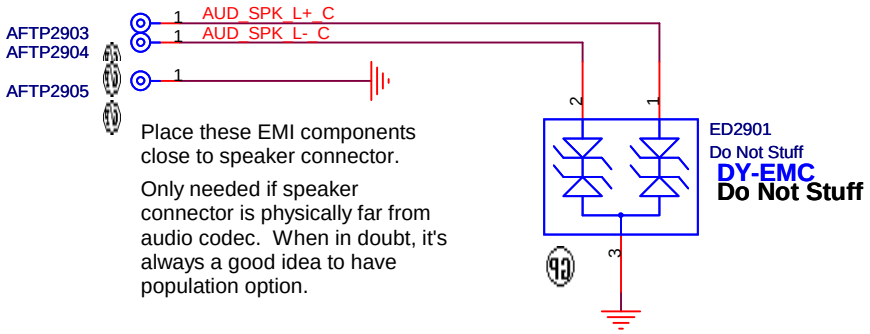
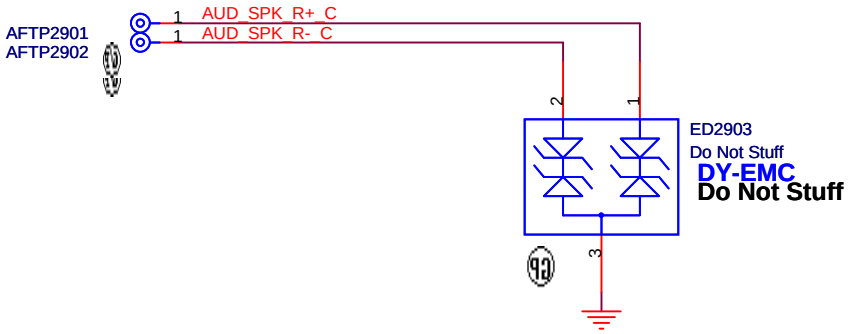
INTERNAL STEREO SPEAKERS







BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO SPEAKER***	
Size A4	Document Number **BOHOL**	Rev **-1**
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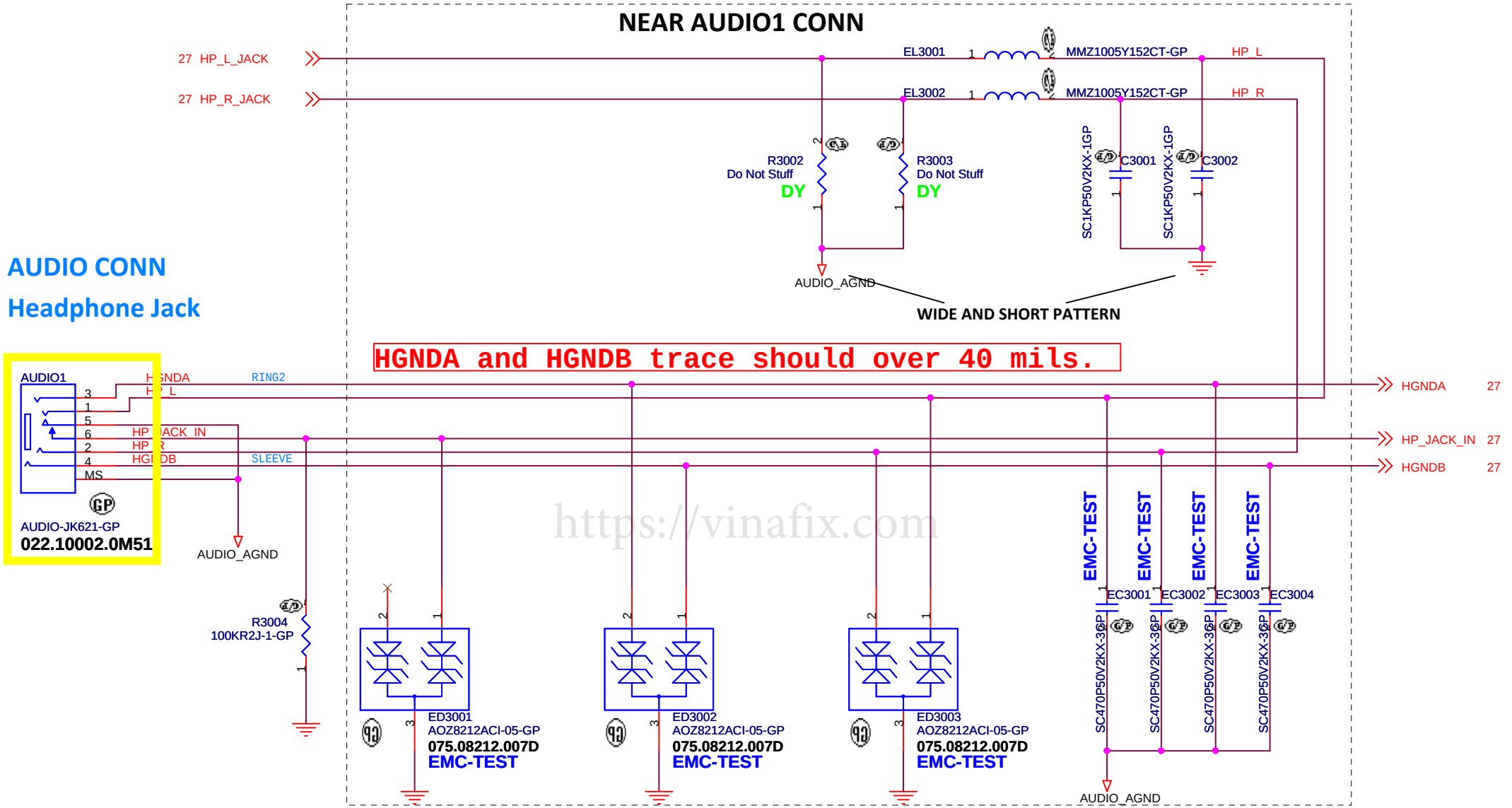

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO COMBO JACK***	
Size A4	Document Number **BOHOL**	Rev -1
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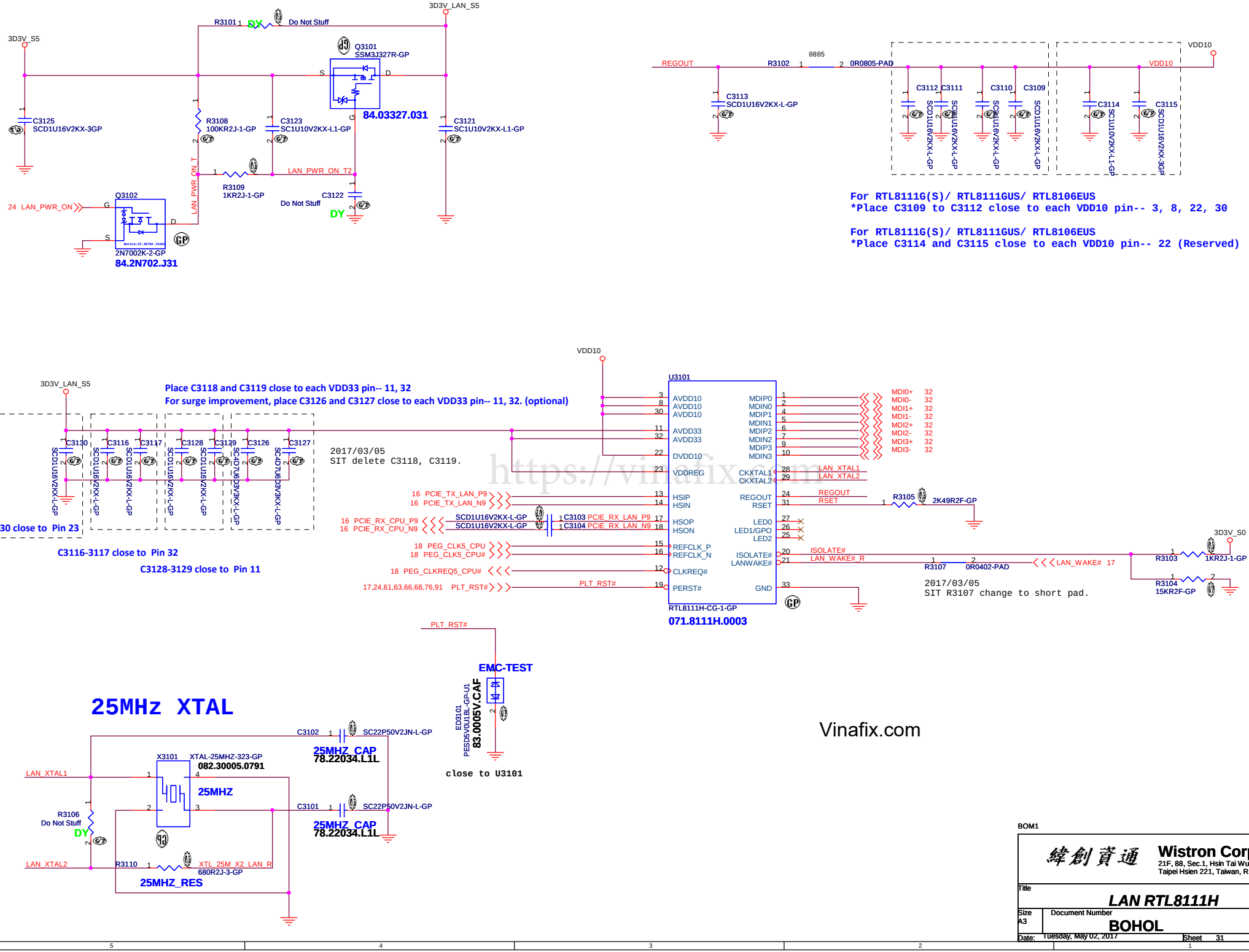
3D3V_S5
3D3V_LAN_S5
R3101 DY Do Not Stuff
Q3101 SSM3J327R-GP
84.03327.031
C3125 SCD1U16V2KX-3GP
R3108 100KR2J-1-GP
C3123 SC1U10V2KX-L1-GP
C3121 SC1U10V2KX-L1-GP
LAN_PWR_ON_T
LAN_PWR_ON_T2
R3109 1KR2J-1-GP
C3122 Do Not Stuff DY
24 LAN_PWR_ON
Q3102 2N7002K-2-GP
84.2N702.J31
REGOUT
R3102 0805 0R0805-PAD
C3113 SCD1U16V2KX-L-GP
VDD10
C3112 C3111 C3110 C3109 SCD1U16V2KX-L-GP
C3114 SC1U10V2KX-L1-GP
C3115 SCD1U16V2KX-3GP
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30
For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
*Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)
Place C3118 and C3119 close to each VDD33 pin-- 11, 32
For surge improvement, place C3126 and C3127 close to each VDD33 pin-- 11, 32. (optional)
C3130 C3116 C3117 C3128 C3129 C3126 C3127
C3130 close to Pin 23
C3116-3117 close to Pin 32
C3128-3129 close to Pin 11
2017/03/05
SIT delete C3118, C3119.
U3101
AVDD10 AVDD10 AVDD10 AVDD33 AVDD33 DVDD10 VDDREG
MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
CKXTAL1 CKXTAL2 LAN_XTAL1 LAN_XTAL2
REGOUT RSET R3105 2K49R2F-GP
HSIP HSIN HSOP HSON
16 PCIE_TX_LAN_P9 16 PCIE_TX_LAN_N9
16 PCIE_RX_CPU_P9 16 PCIE_RX_CPU_N9
SCD1U16V2KX-L-GP C3103 PCIE_RX_LAN_P9 C3104 PCIE_RX_LAN_N9
LED0 LED1/GPO LED2
REFCLK_P REFCLK_N
18 PEG_CLK5_CPU 18 PEG_CLK5_CPU#
ISOLATE# LANWAKE#
ISOLATE# LAN_WAKE#_R
R3107 0R0402-PAD
LAN_WAKE# 17
CLKREQ#
18 PEG_CLKREQ5_CPU#
PERST#
17,24,61,63,66,68,76,91 PLT_RST#
PLT_RST#
GND
RTL8111H-CG-1-GP
071.8111H.0003
2017/03/05
SIT R3107 change to short pad.
3D3V_S0
R3103 1KR2J-1-GP
R3104 15KR2F-GP
EMC-TEST
ED3101 PESD5V0U1BL-GP-U1
83.0005V.CAF
close to U3101
25MHz XTAL
X3101 XTAL-25MHZ-323-GP
082.30005.0791
25MHZ
C3102 SC22P50V2JN-L-GP
25MHZ_CAP
78.22034.L1L
C3101 SC22P50V2JN-L-GP
25MHZ_CAP
78.22034.L1L
LAN_XTAL1
LAN_XTAL2
R3106 Do Not Stuff DY
R3110 XTL_25M_X2_LAN_R 680R2J-3-GP
25MHZ_RES
Vinafix.com
BOM1
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN RTL8111H
Size A3
Document Number BOHOL
Rev -1
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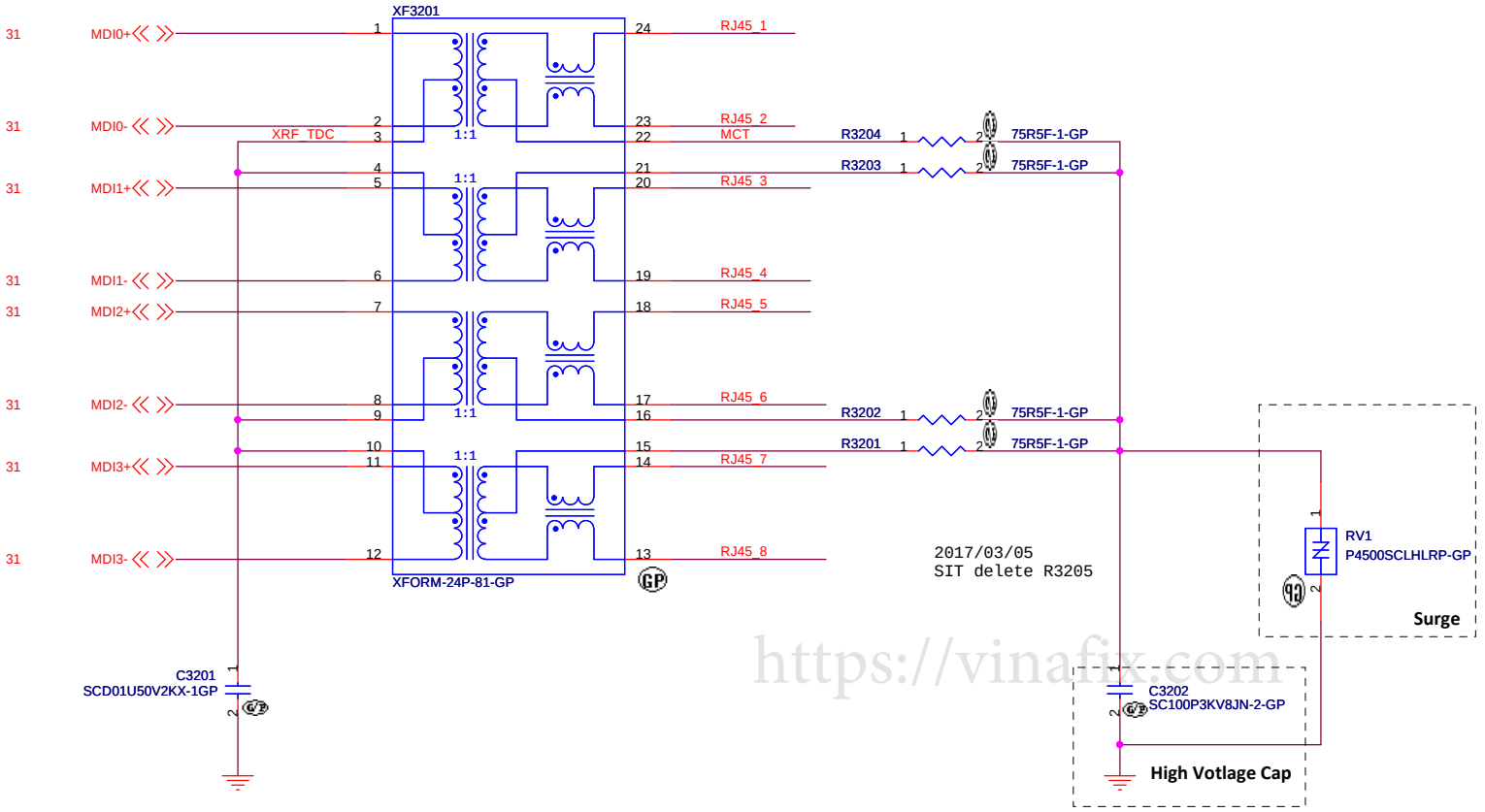
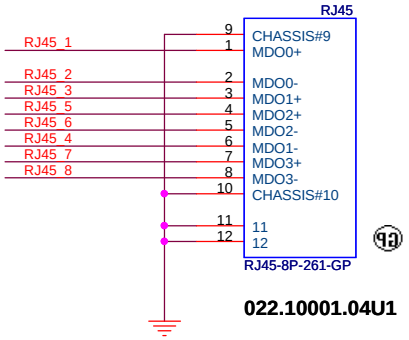
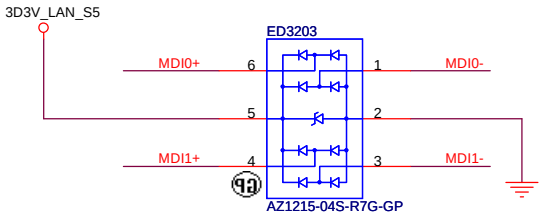
10/100M/1000M Lan Transformer



LAN Connector

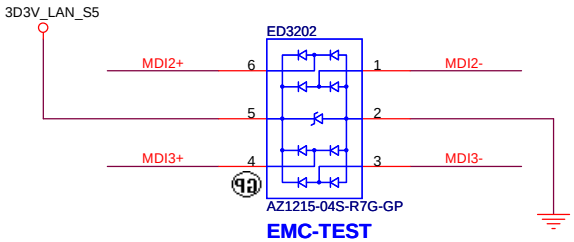


022.10001.04U1



EMC-TEST

75.01215.07C



EMC-TEST

75.01215.07C

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
	RJ45		
Size: Custom	Document Number: **BOHOL**		Rev: **-1**
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***RESERVED***	
Size A4	Document Number **BOHOL**	Rev -1
Date: Tuesday, May 02, 2017	Sheet 33 of 105	

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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***RESERVED***	
Size A4	Document Number **BOHOL**	Rev **-1**
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BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***RESERVED***	
Size: A4	Document Number: **BOHOL** Rev: **-1**
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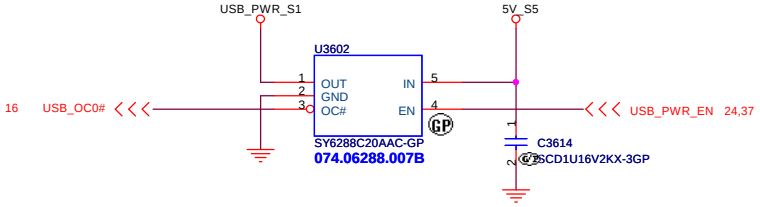
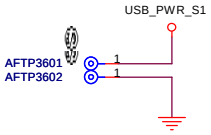


FOR ON BOARD SINGLE USB 3.0 CONNECTOR

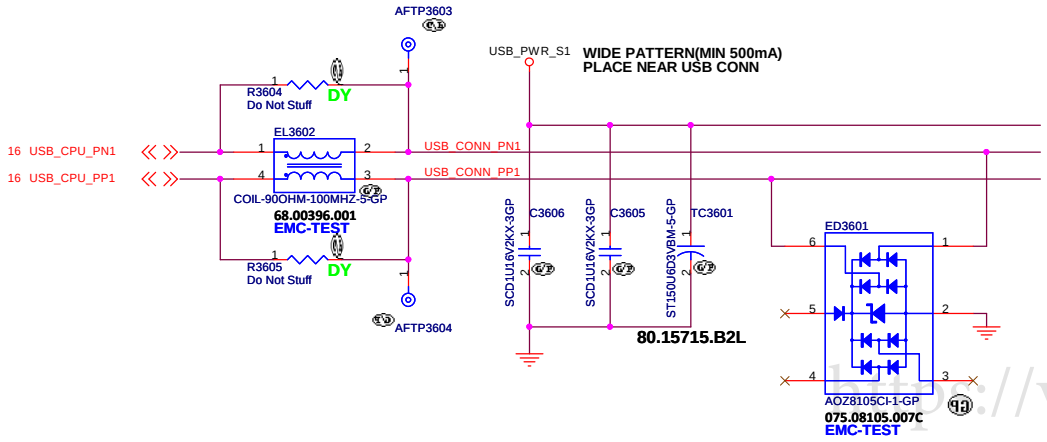
Continous Current Limit 1.5A

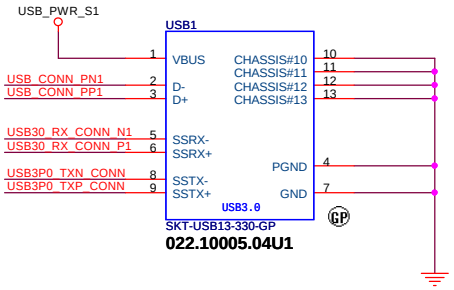
TABLE of USB 3.0 port: U3302

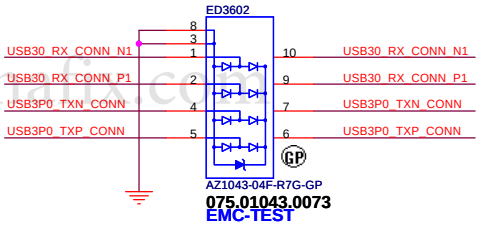
	Vendor	Vendor P/N	Wistron P/N
1st	TI	TPS2069CDGNR	74.02069.A79
2nd	ROHM	BD82032FVJ-GE2	74.82032.07G

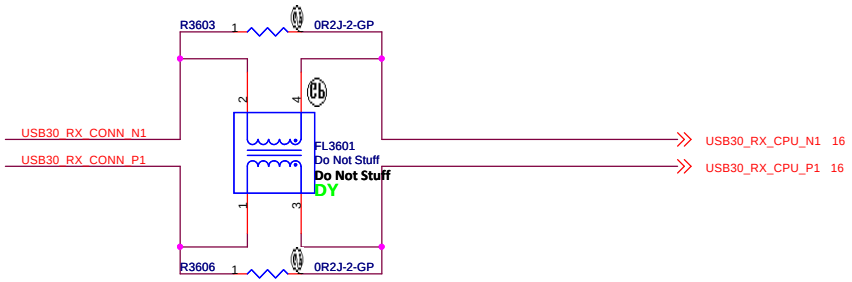


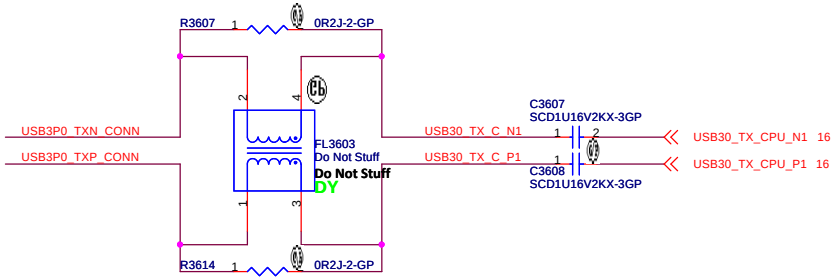
Vinafix.com











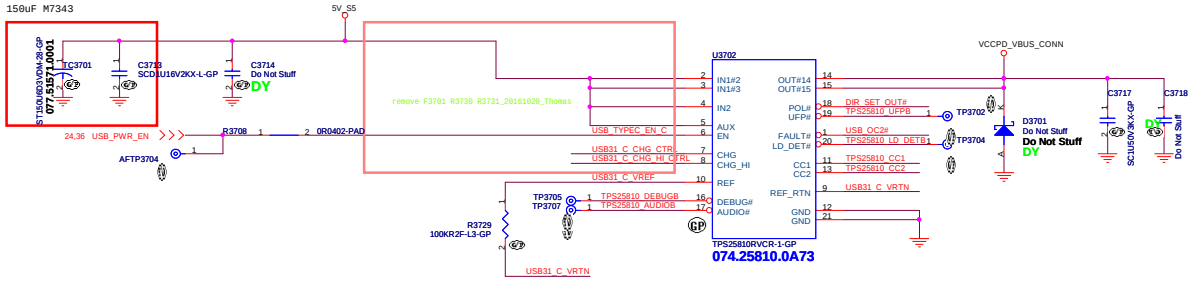
BOM1

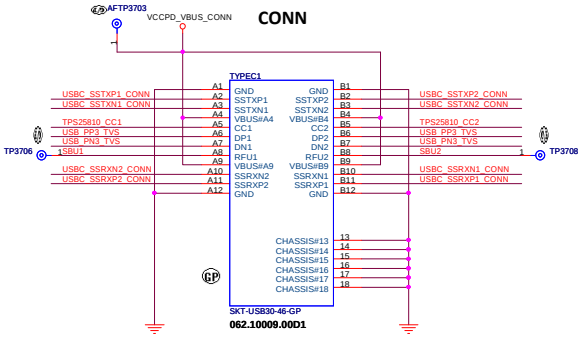
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

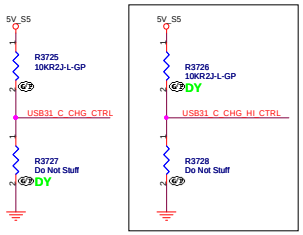
Title: ***USB30 CONN***

Size	Document Number	Rev
A3	BOHOL	-1

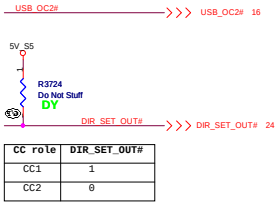
Date: Tuesday, May 02, 2017 Sheet 36 of 105



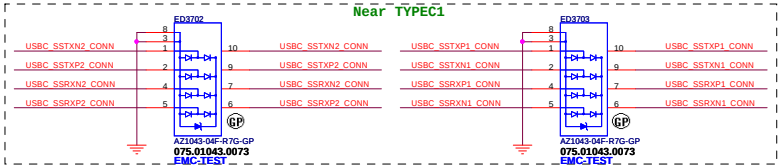


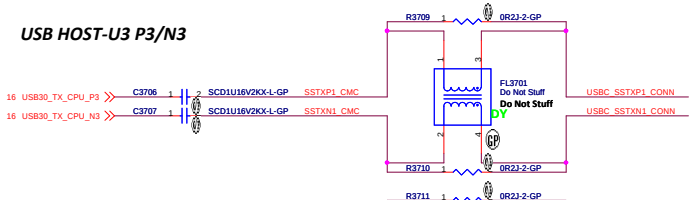


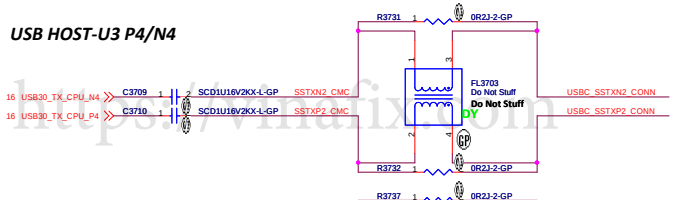
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

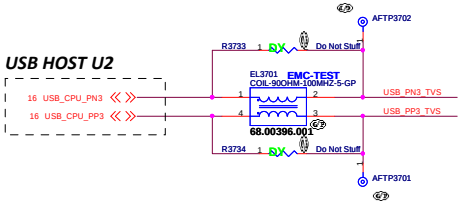


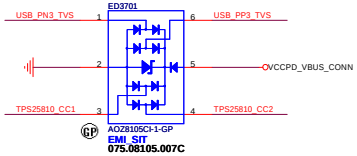
CC role	DIR_SET_OUT#
CC1	1
CC2	0











BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TYPEC USB3.1***

Size: A2 | Document Number: **BOHOL** | Rev: **-1**

Date: Tuesday, May 02, 2017 | Sheet 37 of 105

Main Func = USB3.0 Re-driver

(Blank)

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB30 RE-DRIVER*

Size	Document Number	Rev
A4	BOHOL	-1

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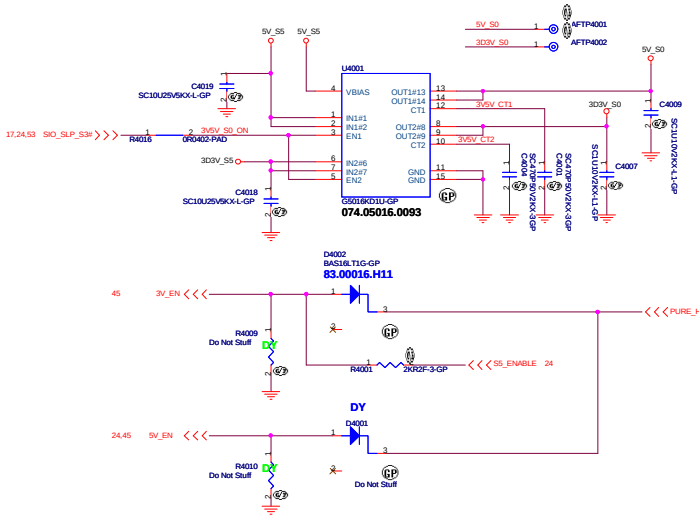
BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***RESERVED***		
Size A4	Document Number **BOHOL**	Rev **-1**
Date: Tuesday, May 02, 2017	Sheet 39 of 105	

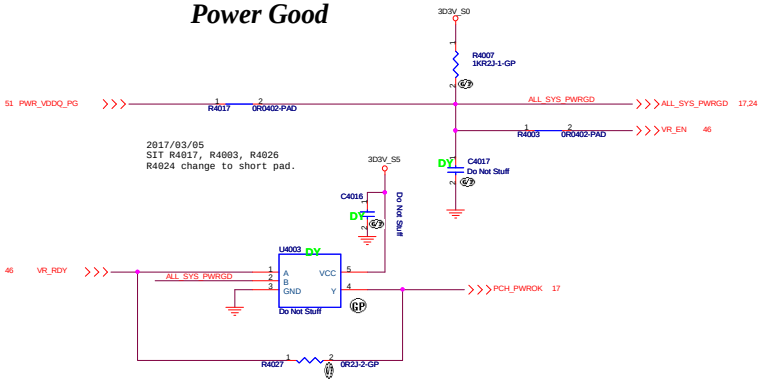
Main Func = Power Plane & Sequence



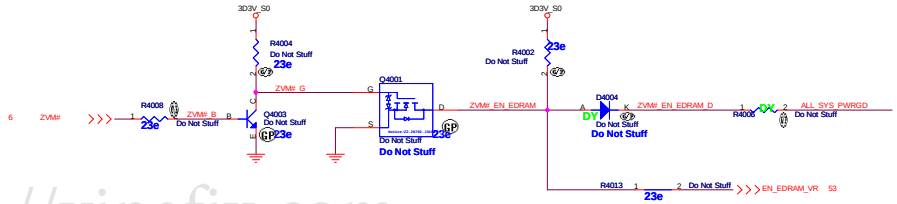
5V_S0

3D3V_S0

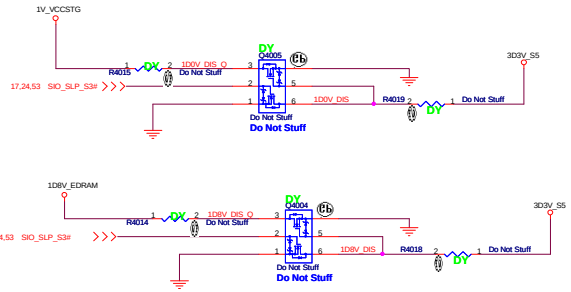
Power Good



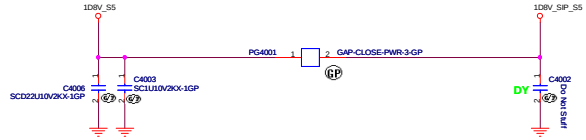
GT3 Low Power Circuit (ZVM)



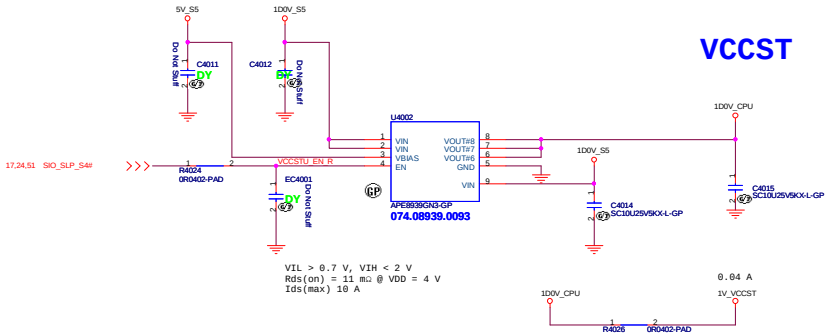
Discharge circuit



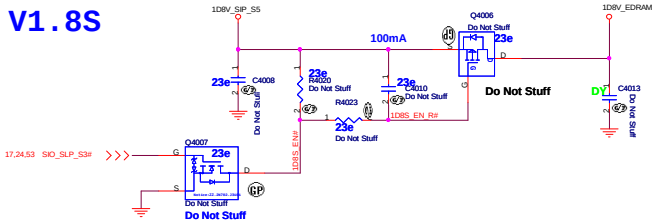
V1.8A



VCCST



V1.8S



561280 KBL UY PDG Rev2.0 Notes:
On power up sequence, VCCOPC_1p8 must never ramp up after VCCOPC/VCCEOPIO under any circumstance.
There are no ramp down requirements between VCCOPC_1p8 and VCCOPC/VCCEOPIO.
Platform must guarantee VCCOPC/VCCEOPIO rails do not start ramping back up for any reason while VCCOPC_1p8 is ramping down or OFF.

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER PLAN EN&SEQUENCE

Size	Document Number	Rev
Custom	BOHOL	-1

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	**BOHOL**	**-1**

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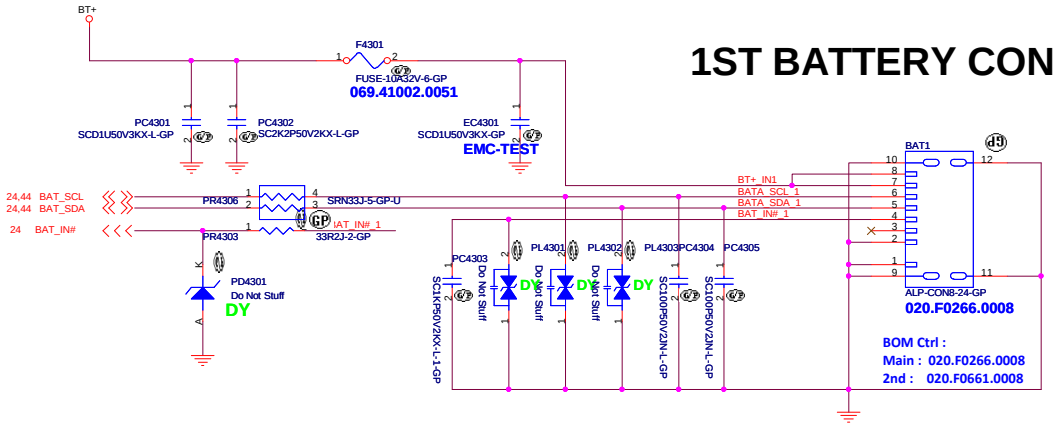
BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 42 of 105	

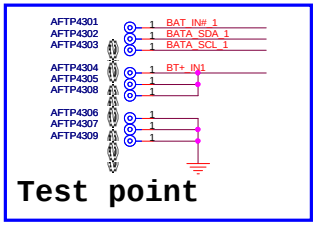
1ST BATTERY CONNECTOR

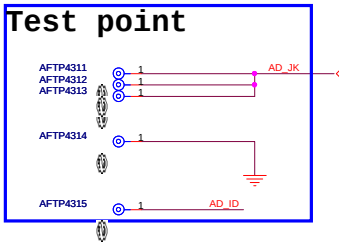


Connector Pin Alignment(Vendor: Suyin,Aces)

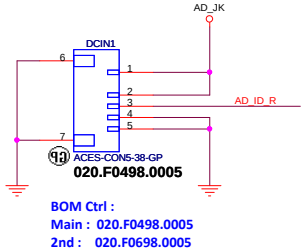
Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

It is required to follow Lenovo common connector requirement for both battery side and system side.
Common connector drawing:

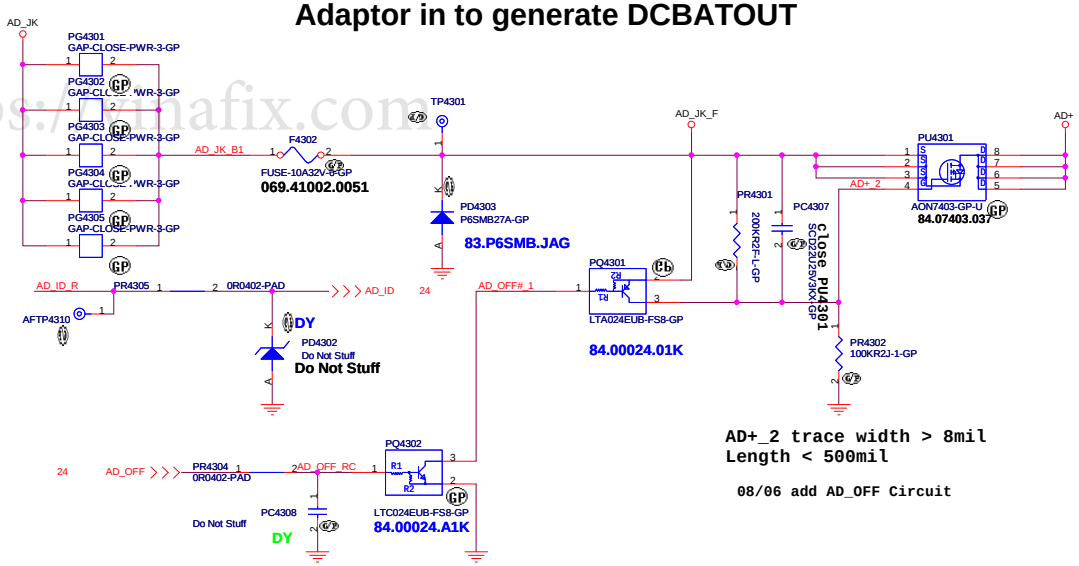




DC Jack



Adaptor in to generate DCBATOUT



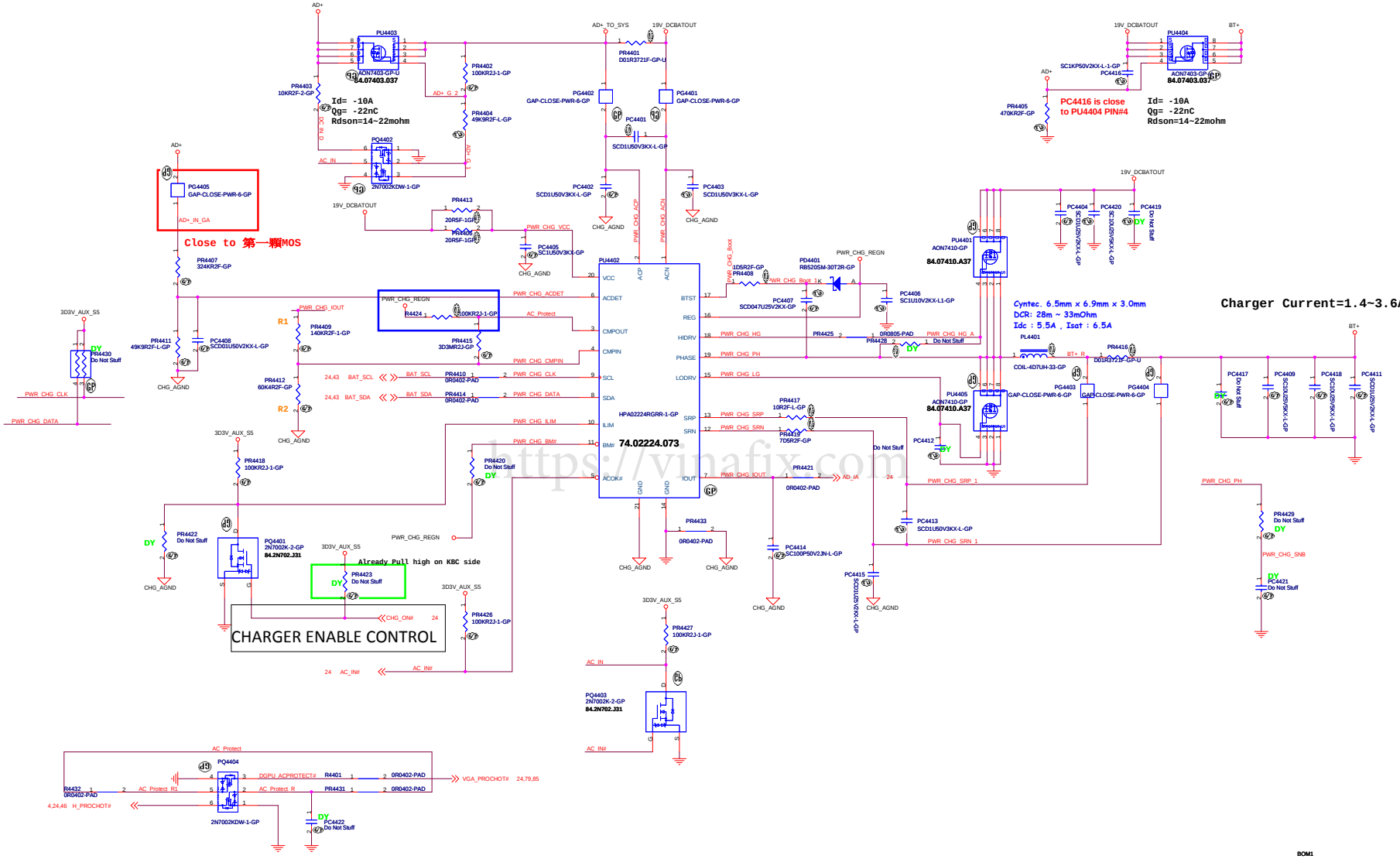
AD+_2 trace width > 8mil
Length < 500mil

08/06 add AD_OFF Circuit

BOM1

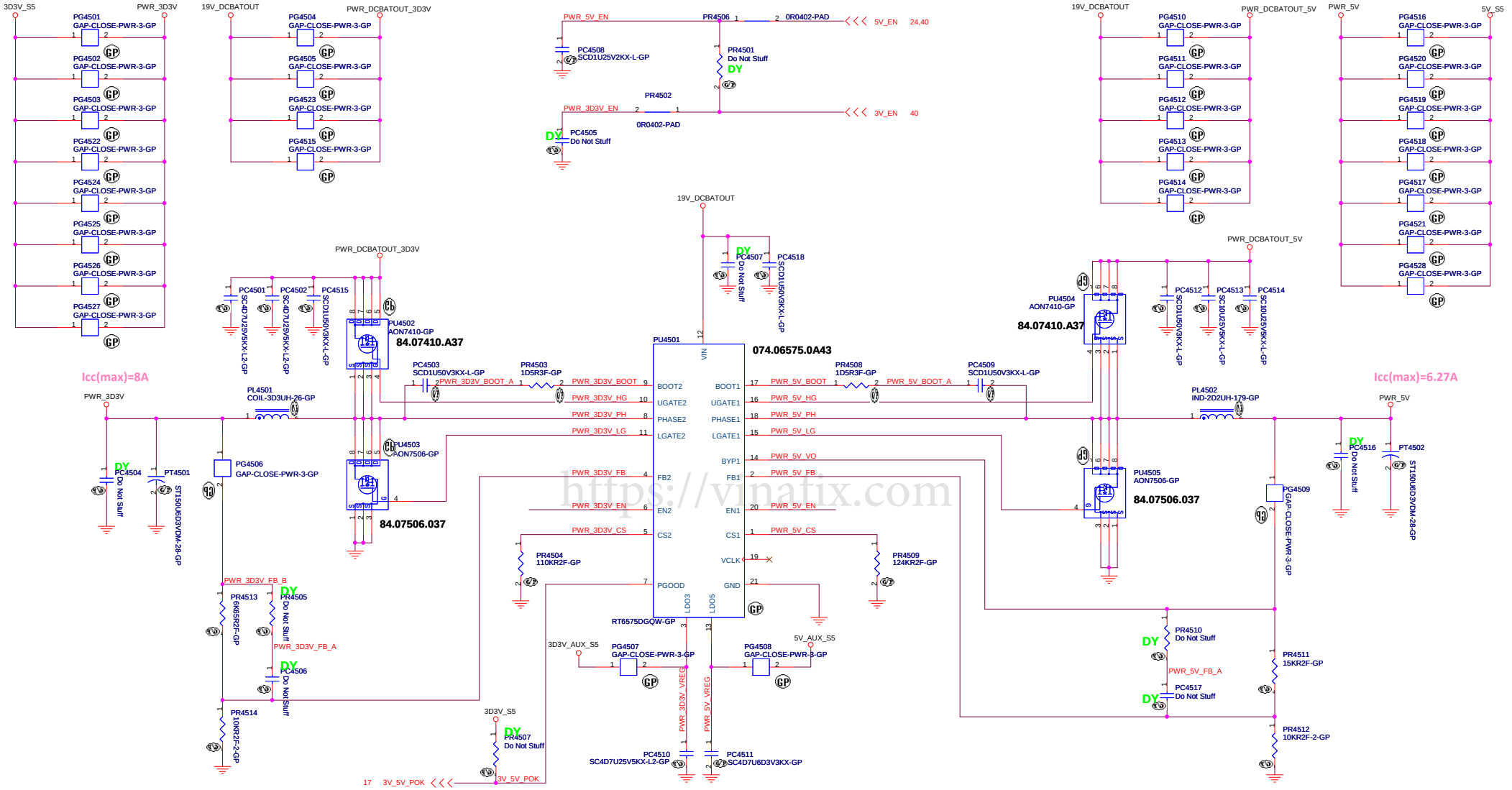
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN & BATT CONN		
Size: Custom	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 43 of 105	

SSID = Charger



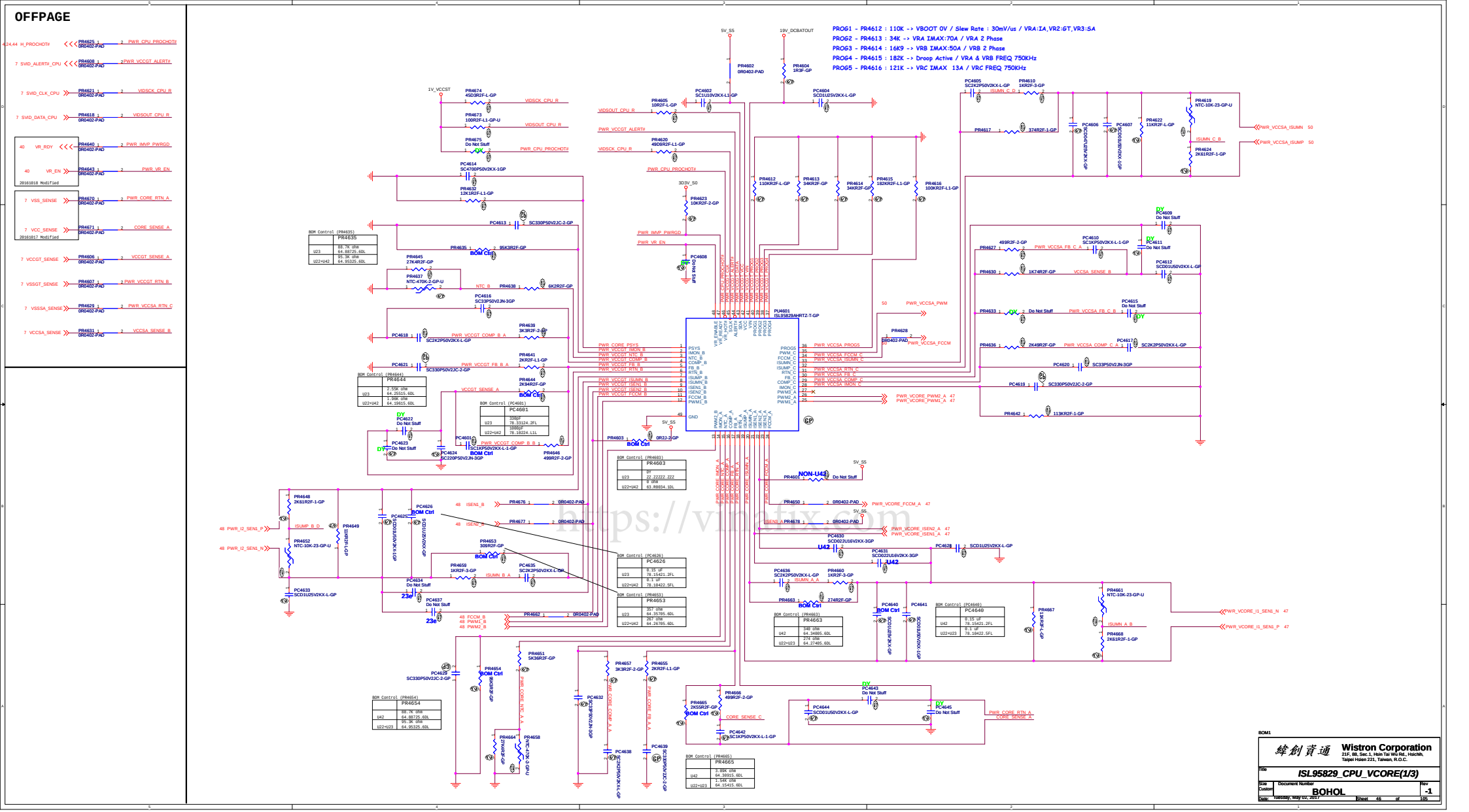
BOM1	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER HPA02224RGRR
Size: Custom	Document Number: BOHOL
Rev	-1
Date: Tuesday, May 02, 2017	Sheet 44 of 105

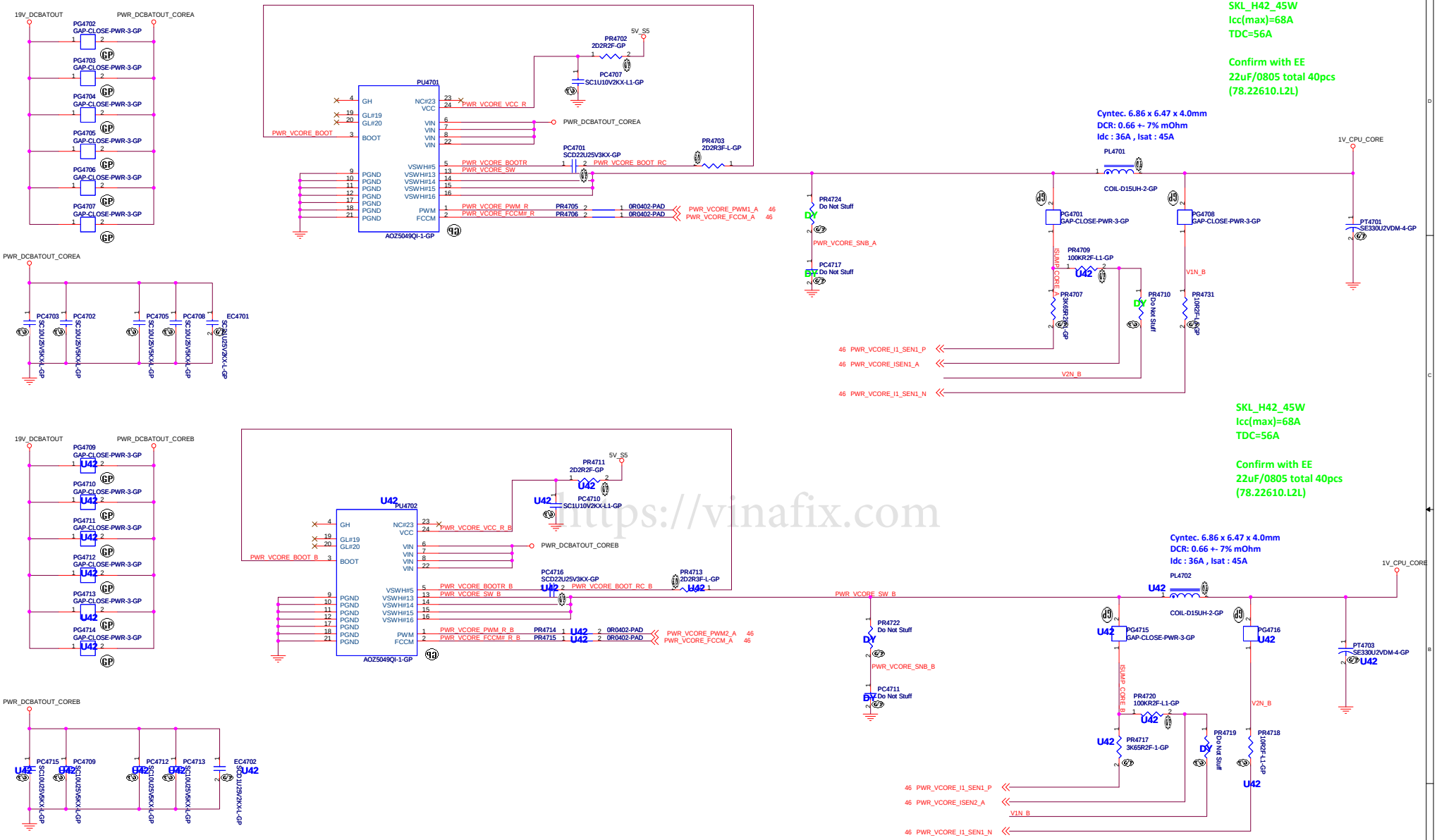
2017/03/06
SIT ASM PR4506, DY PR4501 for AOU DC Mode charge issue.



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT6575DGQW_5V/3D3V		
Size: Custom	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 45 of 105	


OFFPAGE
PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz
ISL95829_CPU_VCORE(1/3)
Wistron Corporation
BOHOL
https://vinafix.com


SKL_H42_45W
Icc(max)=68A
TDC=56A
Confirm with EE
22uF/0805 total 40pcs
(78.22610.L2L)
Cyntec. 6.86 x 6.47 x 4.0mm
DCR: 0.66 +- 7% mOhm
Idc : 36A , Isat : 45A
19V_DCBATOUT
PWR_DCBATOUT_COREA
PWR_DCBATOUT_COREB
PU4701
PU4702
AOZ5049QI-1-GP
1V_CPU_CORE
PL4701
PL4702
COIL-D15UH-2-GP
https://vinafix.com
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL95829_CPU_VCORE(2/3)
BOHOL
Tuesday, May 02, 2017
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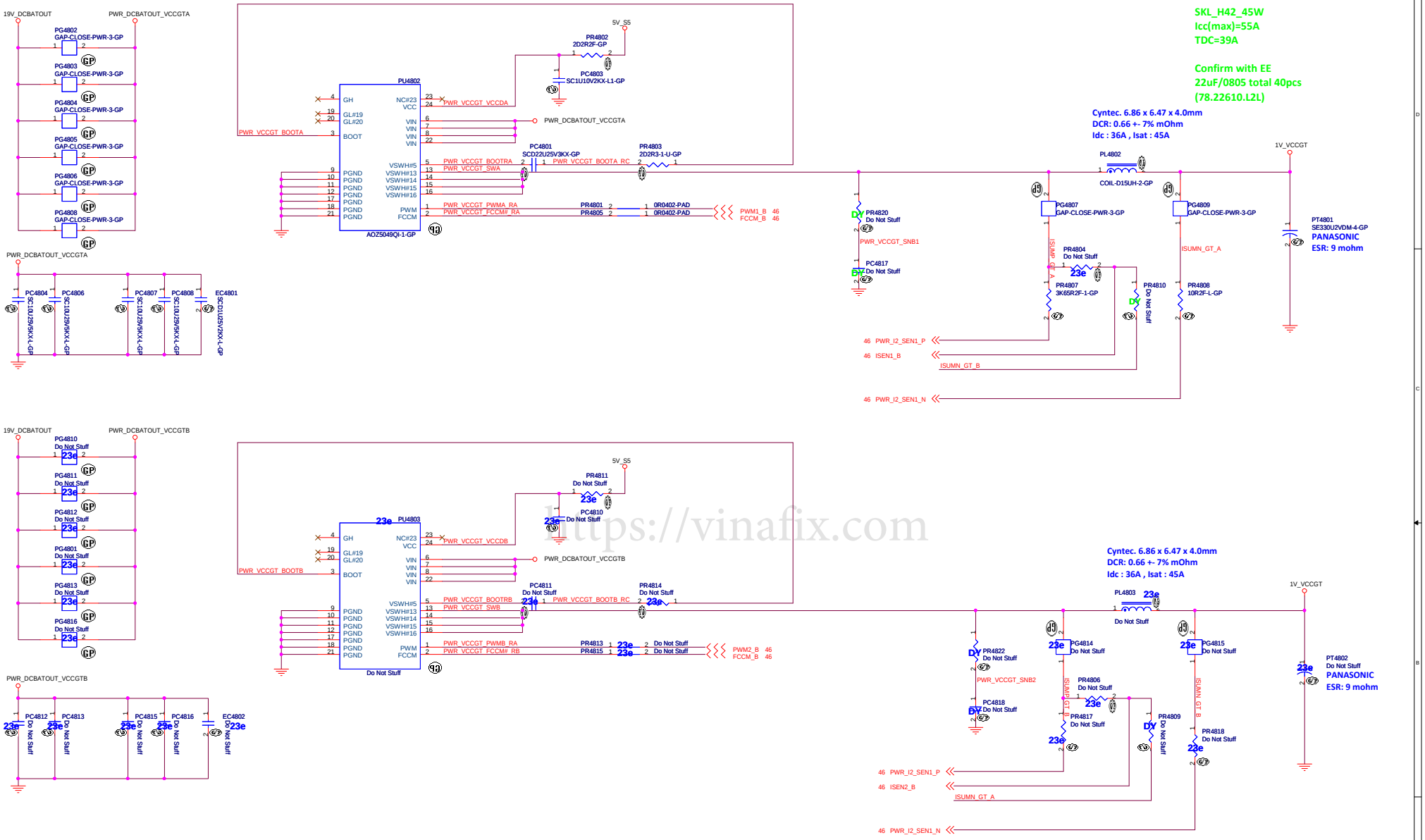

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95829_CPU_VCORE(3/3)

Size	Document Number	Rev
C	BOHOL	-1

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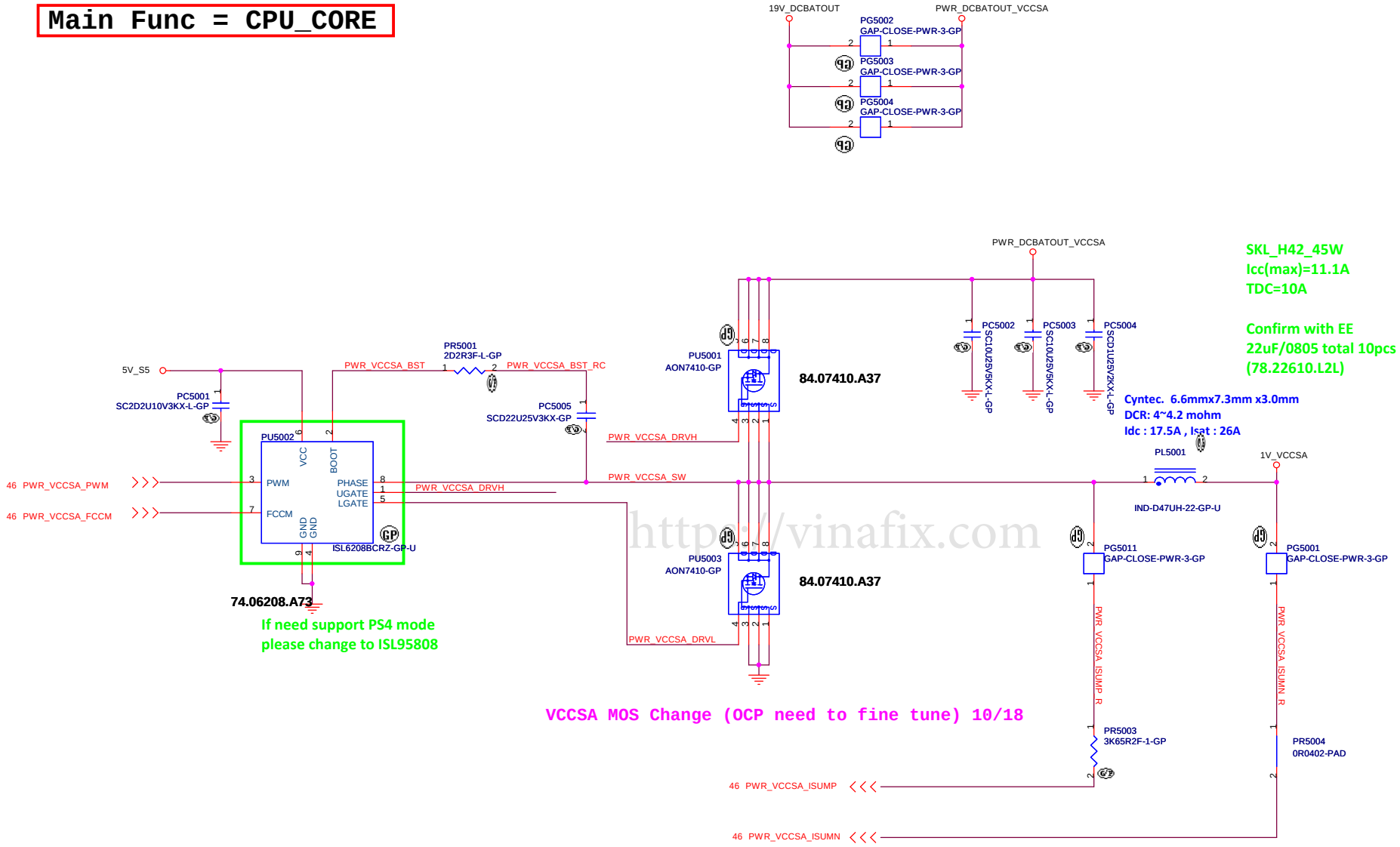
BOM1

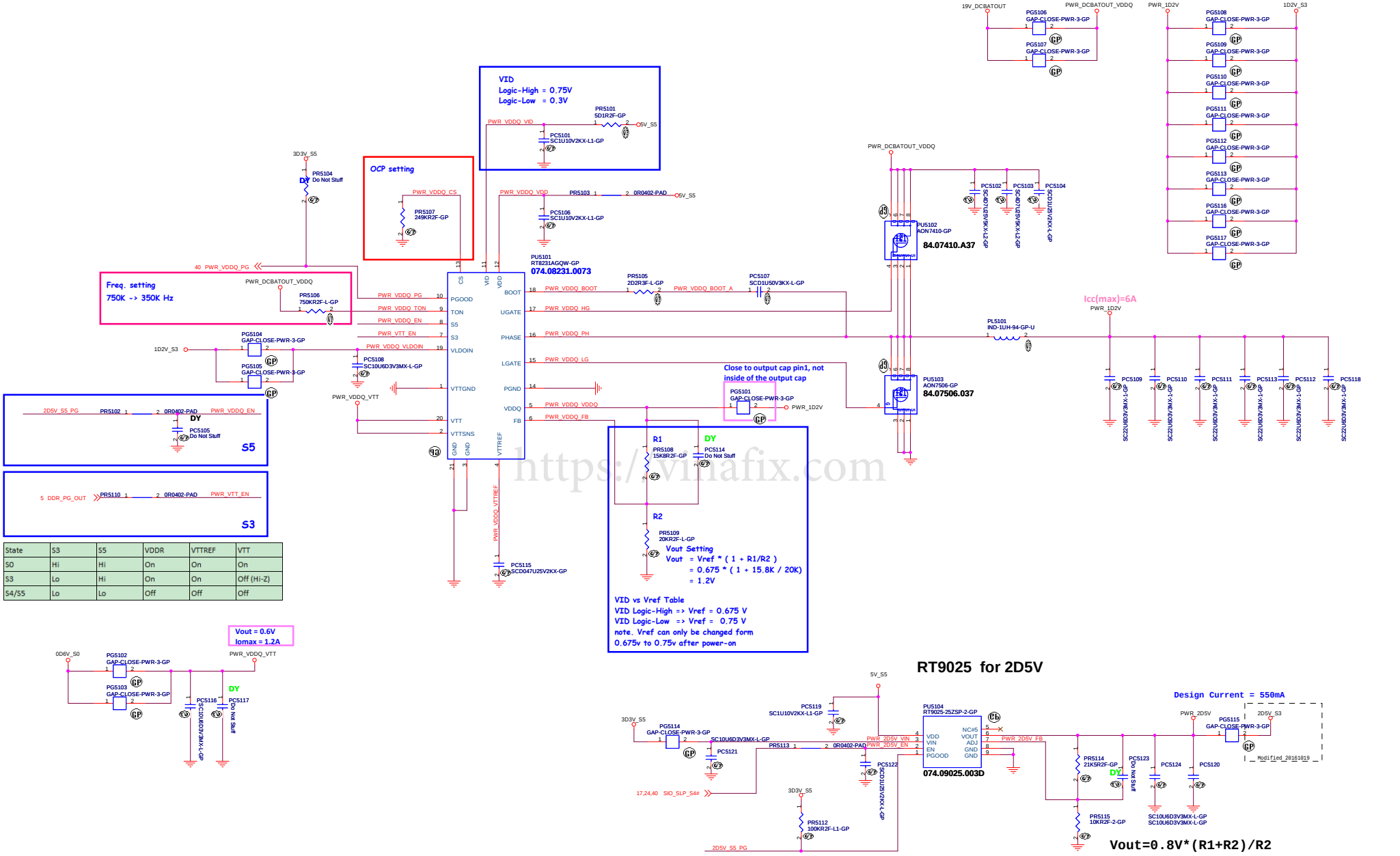
緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***CPU_VCCGTUS***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 49 of 105	

Main Func = CPU_CORE



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL6208_CPU_VCCSA		
Size: A3	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 50 of 105	



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Vinafix.com

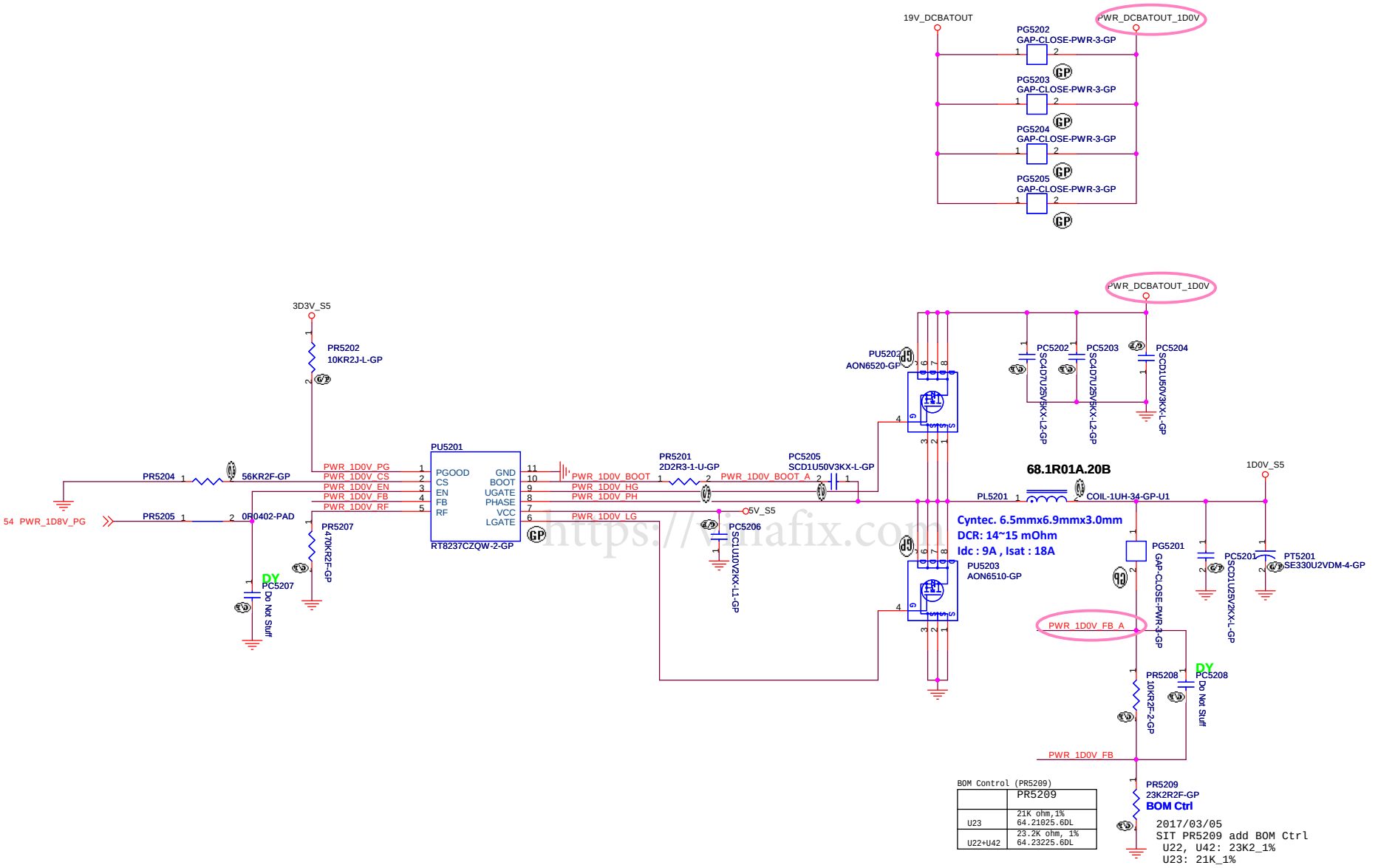
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_VDDQ/VTT

Size: A2 | Document Number: BOHOL | Rev: -1

Date: Tuesday, May 02, 2017 | Sheet 51 of 105



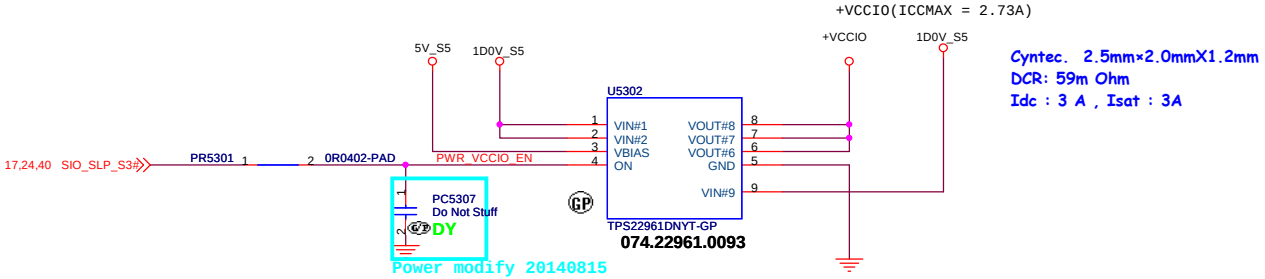
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

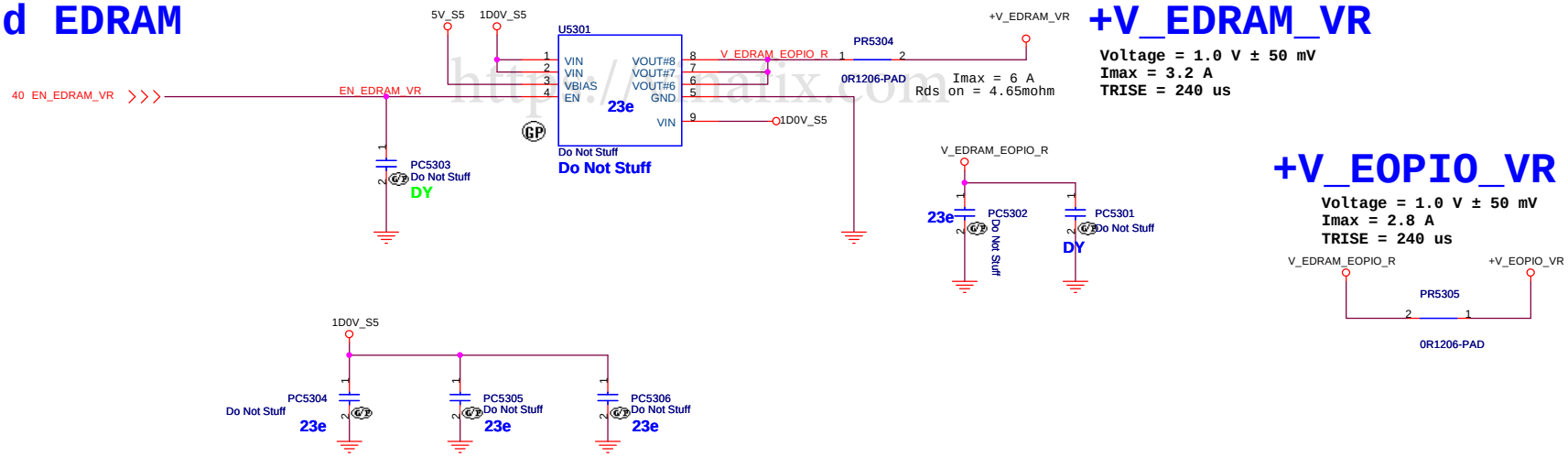
Title	RT8237_1D0V	
Size A3	Document Number BOHOL	Rev -1
Date: Tuesday, May 02, 2017	Sheet 52 of 105	

Main Func = 1D0V

VCCIO



EOPIO and EDRAM



+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS2296_VCCIO&VCCPRIM

Size: A3 | Document Number: BOHOL | Rev: -1

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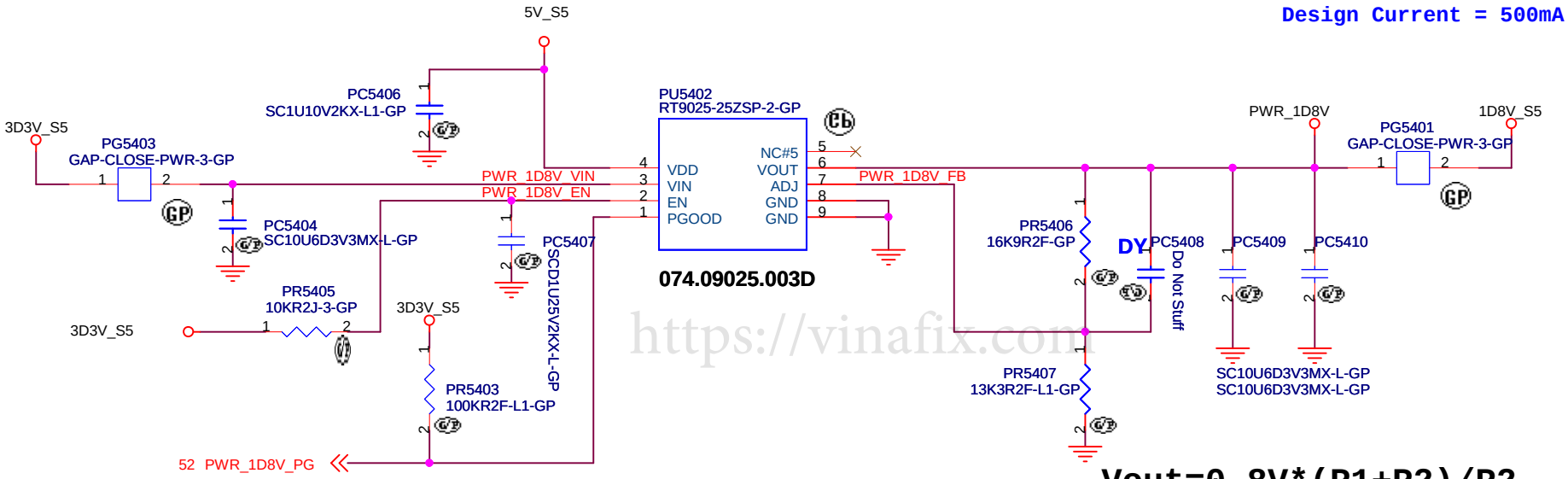
Main Func = 1D8V



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RT9025_1D8V*		
Size: A4	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 54 of 105	

SSID = VIDEO

eDP connector

INVERTER POWER

DCBATOUT_LCD → F5501 POLYSW-1D1A24V-4-GP 69.42402.001 → 19V_DCBATOUT

C5503 DY Do Not Stuff, C5501 SC1K5P50V2KX-1GP, C5502 SCD1U50V3KX-GP, C5508 DY Do Not Stuff

Layout 40 mil

3D3V_S0 → U5501 SY6288C20AAC-GP 074.06288.007B → LCDVDD

8 EDP_VDD_EN → R5503 0R0402-PAD → LCDVDD_EN

R5509 100KR2J-1-GP, C5506 Do Not Stuff, C5512 DY, C5504 SC4D7U6D3V3KX-GP, C5505 SC4D7U6D3V3KX-GP

2017/03/05
SIT R5518, R5514, R5503
R5504 change to short pad.

LCD1 ACES-CON40-18-GP 20.K0678.040

DCBATOUT_LCD

R5510 L_BKLT_CTRL_1 33R2J-2-GP

LCD_BRIGHTNESS
BLON_OUT_C

eDP_AUXP_CPU_C C5515 SCD1U16V2KX-L-GP → eDP_AUX_CPU_P 8
eDP_AUXN_CPU_C C5517 SCD1U16V2KX-L-GP → eDP_AUX_CPU_N 8

eDP_TXP0_CPU_C C5521 SCD1U16V2KX-L-GP → eDP_TX_CPU_P0 8
eDP_TXN0_CPU_C C5518 SCD1U16V2KX-L-GP → eDP_TX_CPU_N0 8

eDP_TXP1_CPU_C C5510 SCD1U16V2KX-L-GP → eDP_TX_CPU_P1 8
eDP_TXN1_CPU_C C5509 SCD1U16V2KX-L-GP → eDP_TX_CPU_N1 8

EMB_HPD_R → R5518 0R0402-PAD → LCDVDD → EDP_HPD 8

LCDVDD_R → R5514 0R0603-PAD

LID_CLOSE#_C → R5502 100R2J-2-GP → LID_CLOSE# 24
DMIC_DATA_R → ER5501 0R0402-PAD EMC-TEST → DMIC_DATA 27
DMIC_CLK_R → ER5502 0R0402-PAD EMC-TEST → DMIC_CLK 27

USB_CON_PP5
USB_CON_PN5

3D3V_AUX_KBC
3D3V_CAMERA_S0

R5511 100KR2F-L1-GP

C5511 SCD1U16V2KX-L-GP, C5513 SC1U10V2KX-L-GP

EC5502 DY Do Not Stuff, EC5503 DY Do Not Stuff

Close to eDP connector
LCD_BRIGHTNESS → EC5501 DY Do Not Stuff

Panel BL brightness/Power En/BL En

8 L_BKLT_EN → R5506 0R0402-PAD → PANEL_BLEN 24

24 BLON_OUT → R5501 1KR2J-1-GP → BLON_OUT_C

8 L_BKLT_CTRL → R5504 0R0402-PAD → L_BKLT_CTRL_1

C5516 SC100P50V2JN-3GP, R5515 100KR2J-1-GP, C5507 SC100P50V2JN-3GP, R5517 100KR2J-1-GP

Test point

LCDVDD_R → AFTP5501

DCBATOUT_LCD → AFTP5503
BLON_OUT_C → AFTP5507
LCD_BRIGHTNESS → AFTP5506

EMB_HPD_R → AFTP5508
AFTP5505

3D3V_AUX_KBC → AFTP5510
3D3V_CAMERA_S0 → AFTP5511

LID_CLOSE#_C → AFTP5509
DMIC_CLK_R → AFTP5512
DMIC_DATA_R → AFTP5513
USB_CON_PP5 → AFTP5514
USB_CON_PN5 → AFTP5515
AFTP5516

CAMERA POWER

Layout 40 mil

3D3V_CAMERA_S0 → R5512 0R2J-2-GP → 3D3V_S0

DY R5513 Do Not Stuff → 3D3V_S0_CAMERA

U5502 OUT GND OC# IN EN → CAMERA_EN 20

C5520 SC10U6D3V3MX-L-GP

Do Not Stuff

C5519 Do Not Stuff DY

Camera

DY-EMC

ED5501

USB_CON_PP5 ↔ USB_CON_PN5
DMIC_DATA_R ↔ DMIC_CLK_R

3D3V_S0

Do Not Stuff

Do Not Stuff

USB_CON_PN5 → R5507 0R0402-PAD → USB_CPU_PN5 16

USB_CON_PP5 → R5508 0R0402-PAD → USB_CPU_PP5 16

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/CAM/DMIC/TOUCH

Size: A3 | Document Number: BOHOL | Rev: -1

Date: Tuesday, May 02, 2017 | Sheet 55 of 105

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BOM1

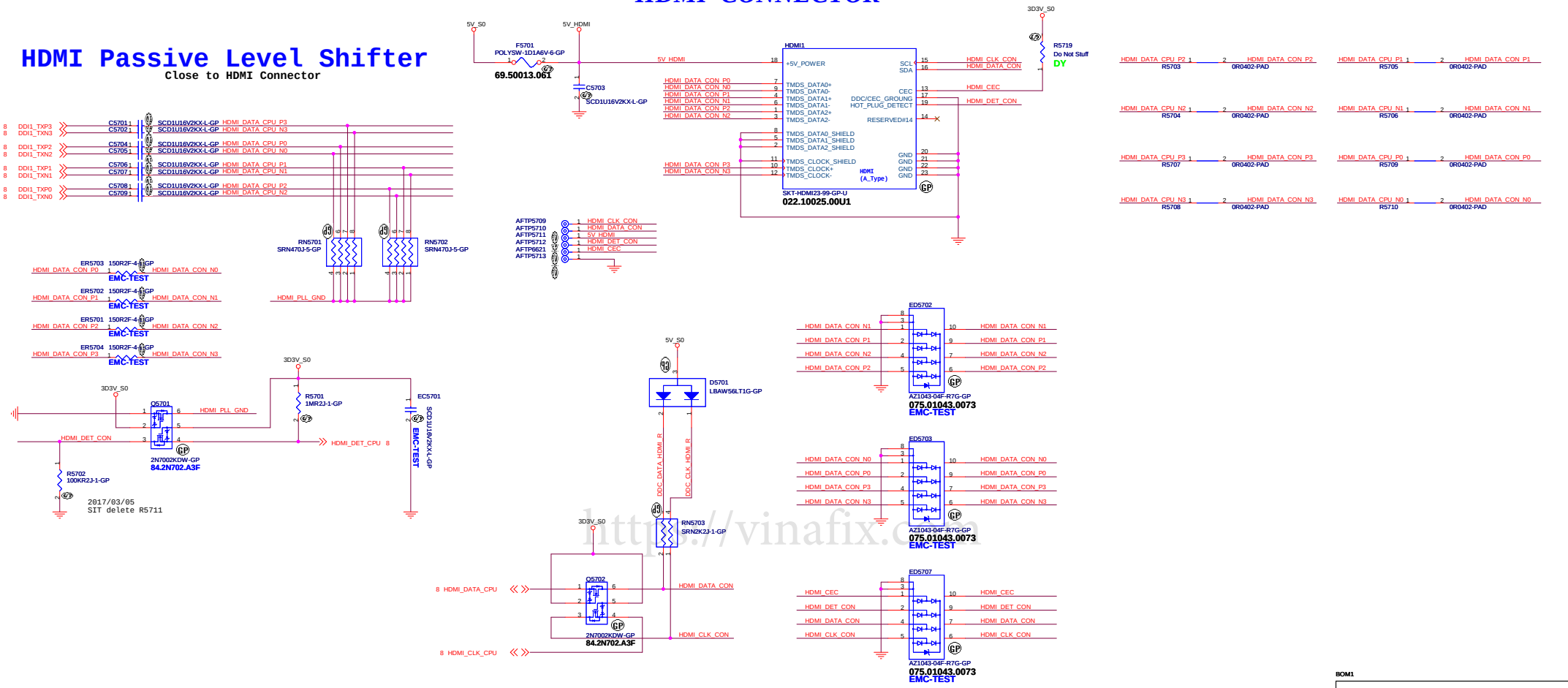
緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 56 of 105	

SSID = HDMI

HDMI CONNECTOR

HDMI Passive Level Shifter

Close to HDMI Connector



20170421- BOM Ctrl- ED5707- Main: 075.PUSB3.0073

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI CONN		
Size: Custom	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 57 of 105	

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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 58 of 105	

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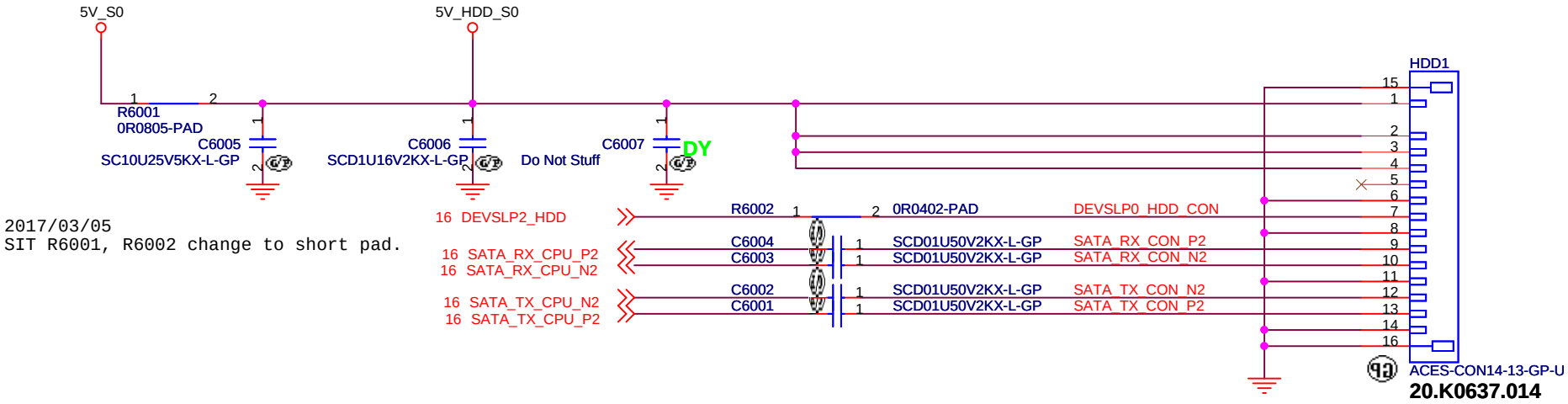
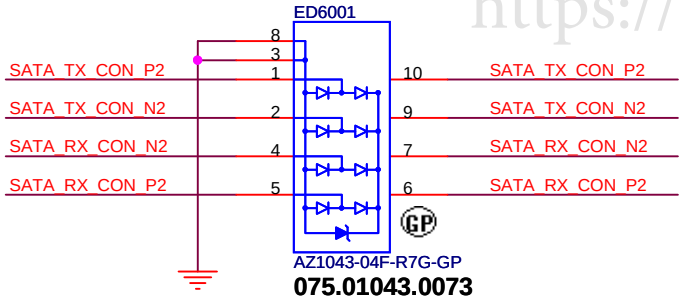
BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***RESERVED***		
Size A4	Document Number **BOHOL**	Rev **-1**
Date: Tuesday, May 02, 2017	Sheet 59 of 105	

SSID = SATA



2017/03/05
SIT R6001, R6002 change to short pad.



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD***

Size	Document Number	Rev
A4	**BOHOL**	**-1**

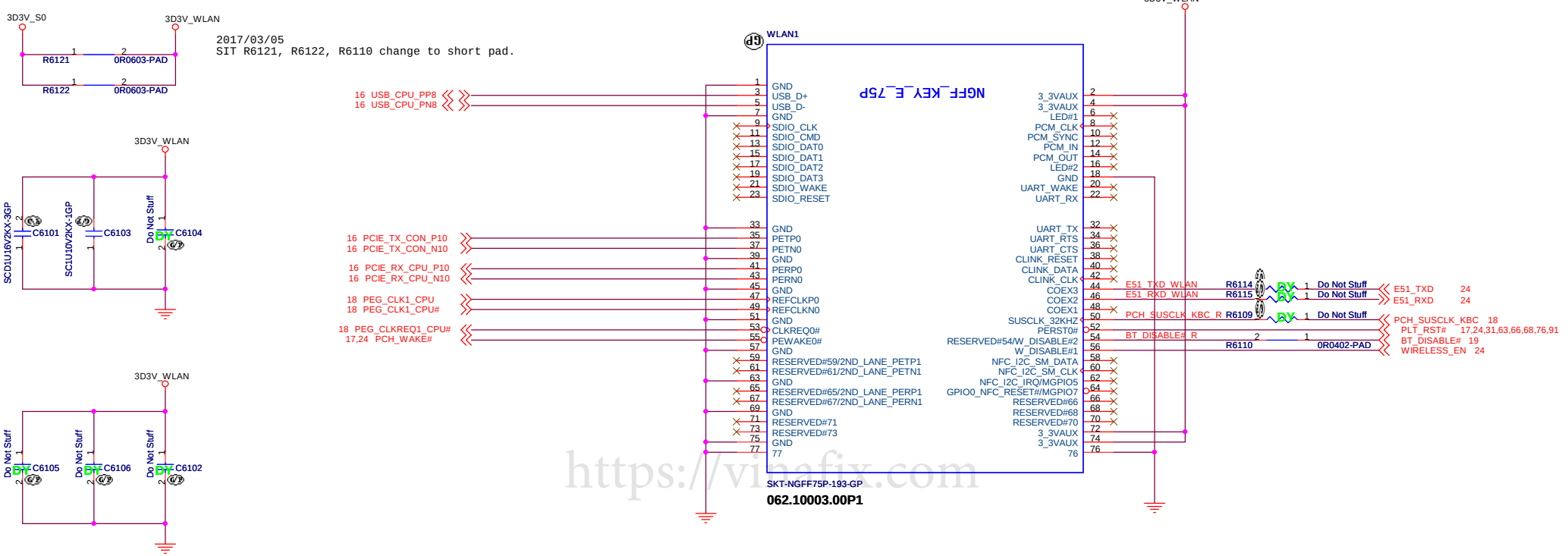
Date: Tuesday, May 02, 2017 Sheet 60 of 105

Main Func = WLAN

M.2 Key-E FOR WLAN / BT

2.5A peak
1.1A Cont

2017/03/05
SIT R6121, R6122, R6110 change to short pad.



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M.2 WLAN CONN***

Size	Document Number	Rev
A3	BOHOL	-1

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BOM1

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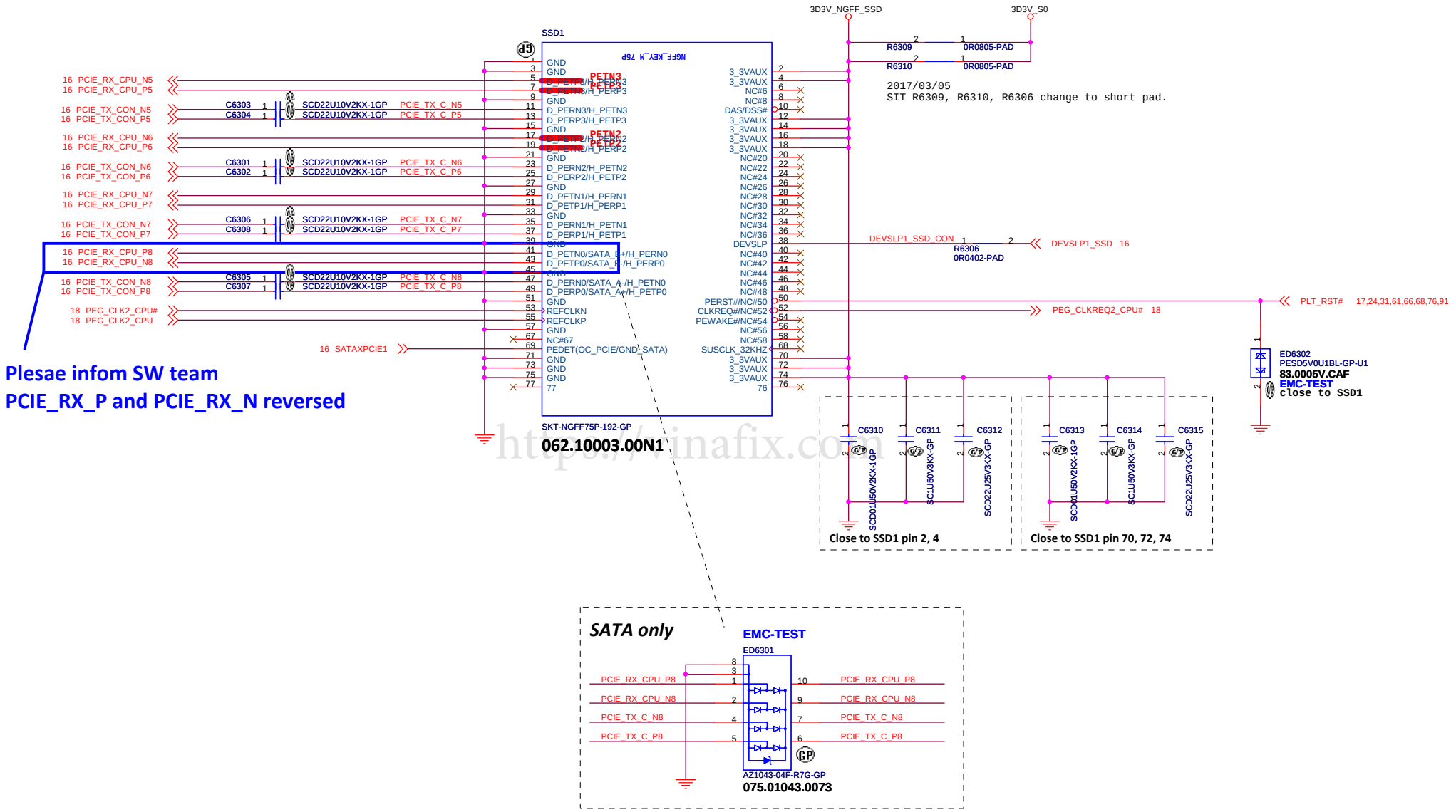
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A4	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 62 of 105

Main Func = SSD TYPE-M NGFF CARD FOR PCIE SSD/Optane



Vinafix.com

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M.2 SSD SLOT

Size	Document Number	Rev
A3	BOHOL	-1

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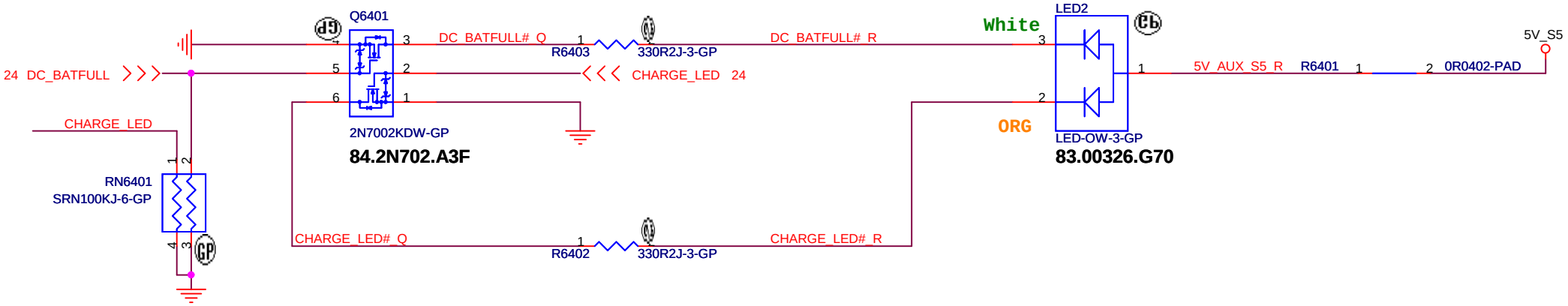
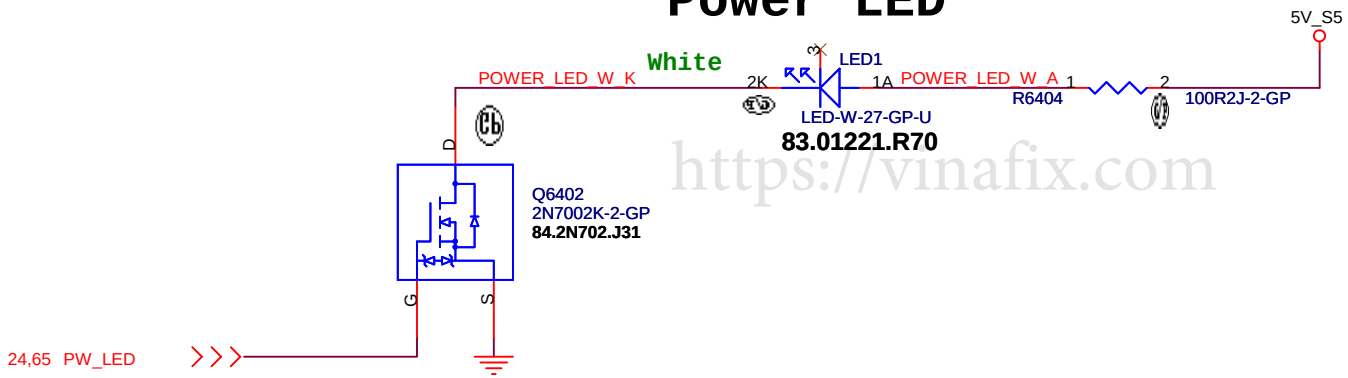
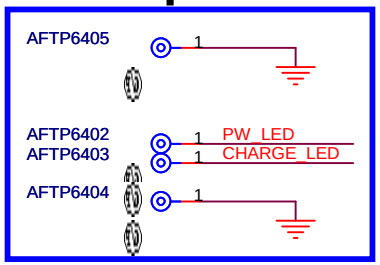
CHARGER LED



Power LED



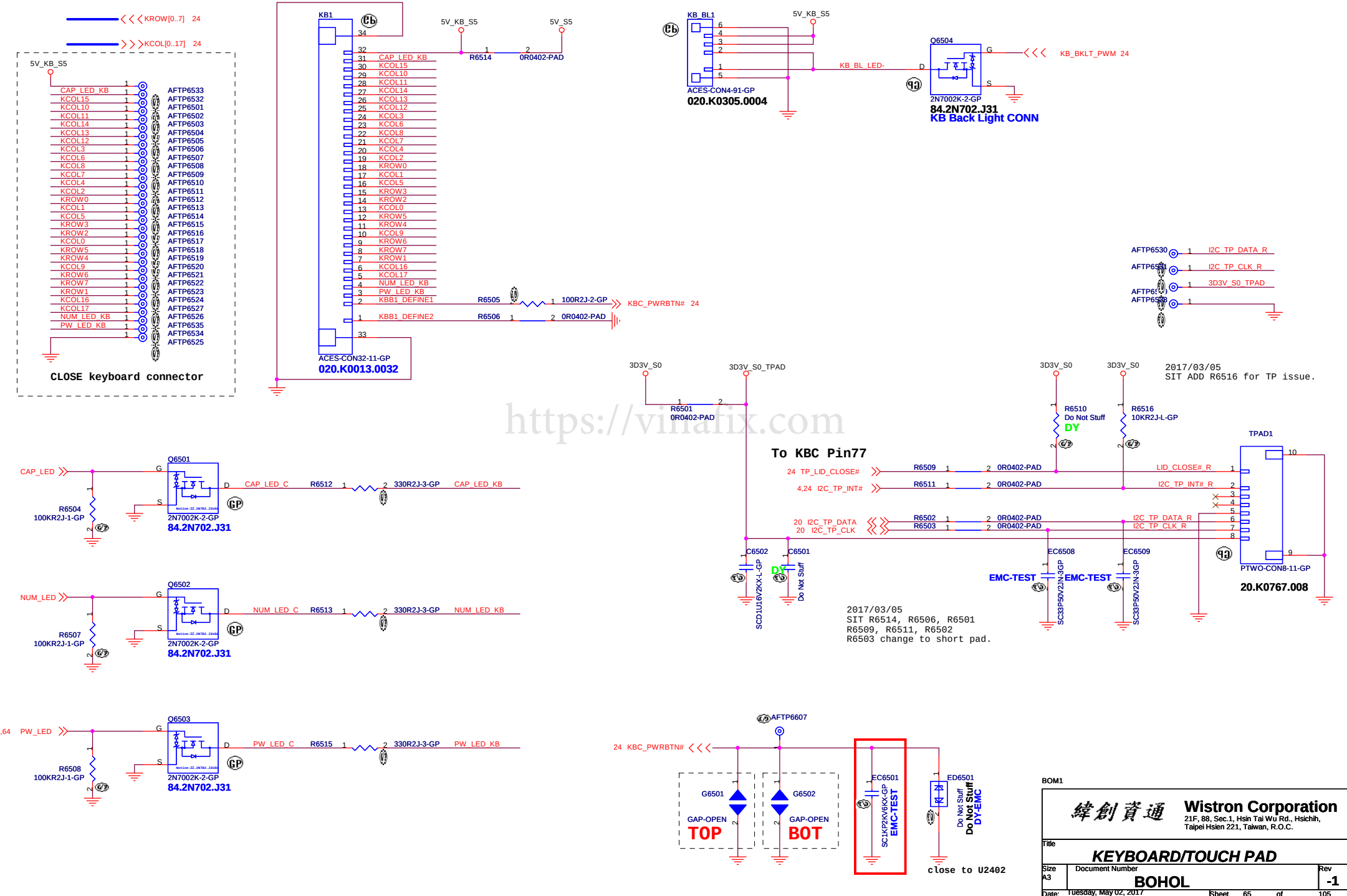
Test point



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LED BOARD/POWER BUTTON*		
Size: A4	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 64 of 105	

SSID = Touch.Pad



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCH PAD

Size	Document Number	Rev
A3	BOHOL	-1

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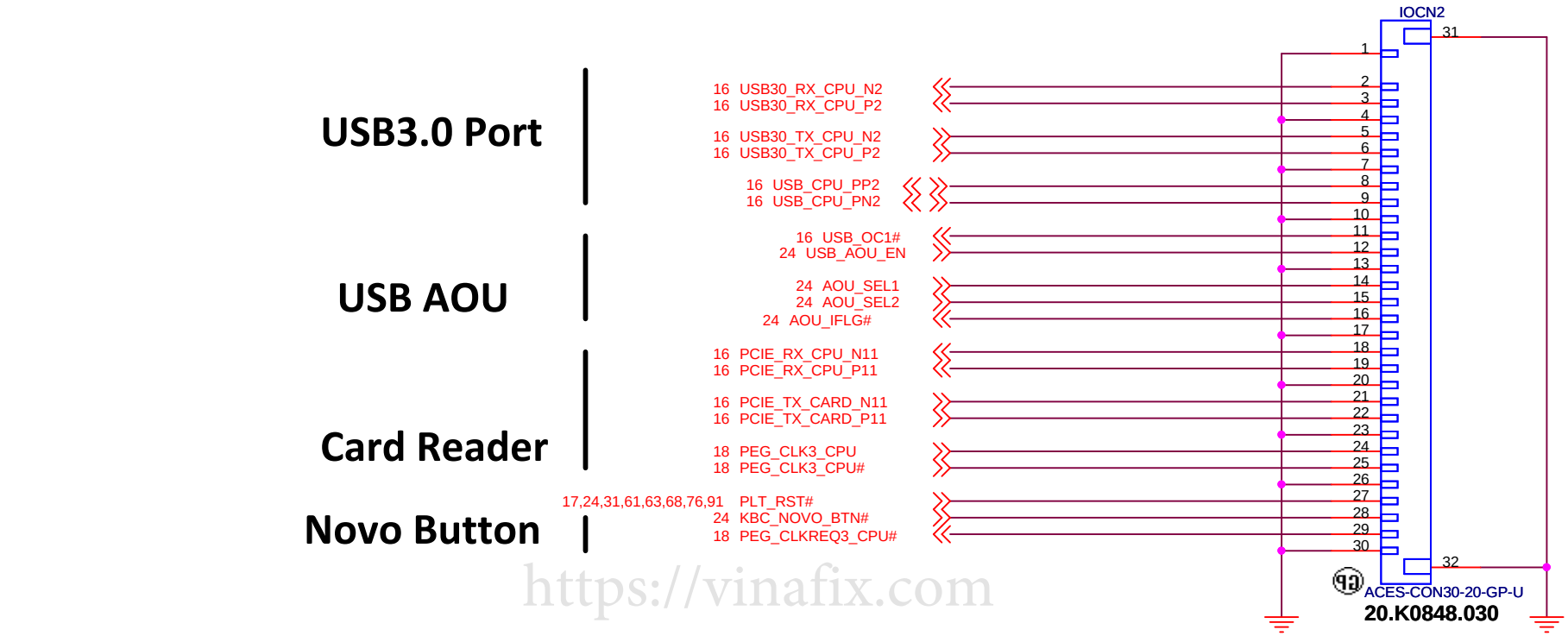

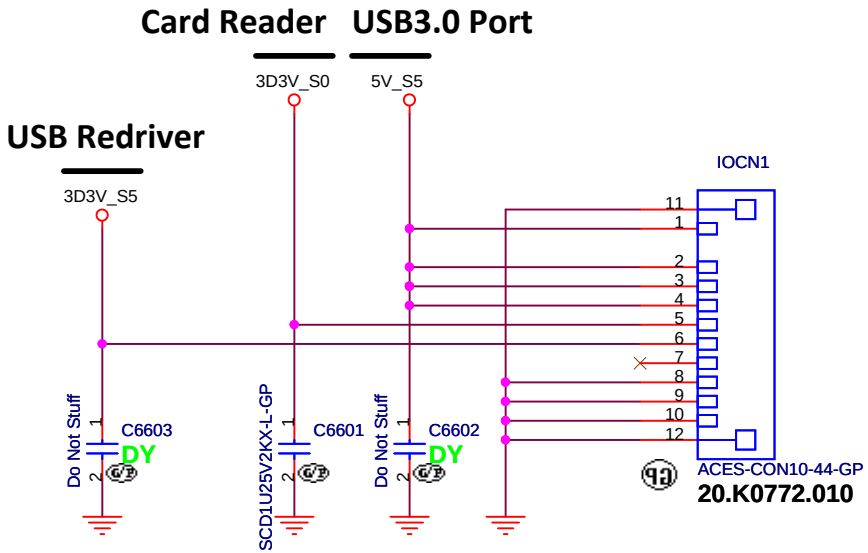

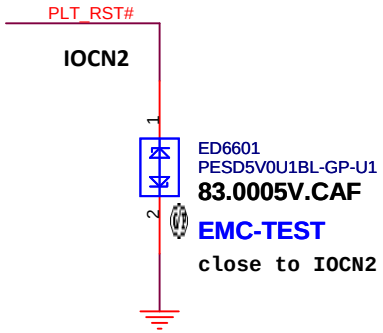

BOM Ctrl :
Main : 20.K0848.030
2nd : 20.K0809.030
3rd : 020.K0160.0030

2017/03/05
SIT chagne IO pin define, add 3d3v_s5 for usb redriver.

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***IO BOARD CONN***	
Size A4	Document Number **BOHOL**	Rev **-1**
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
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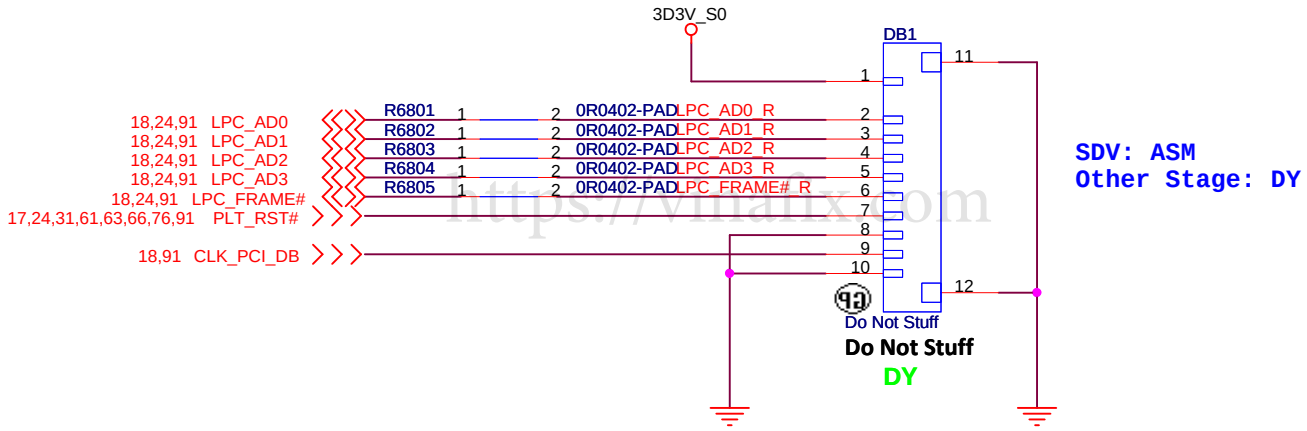
Main Func = Debug

Debug Connector



SDV: ASM
Other Stage: DY

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DEBUG CONN		
Size: A4	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 68 of 105	

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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***RESERVED***		
Size A4	Document Number **BOHOL**	Rev **-1**
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 73 of 105	

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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***RESERVED***		
Size A4	Document Number **BOHOL**	Rev **-1**
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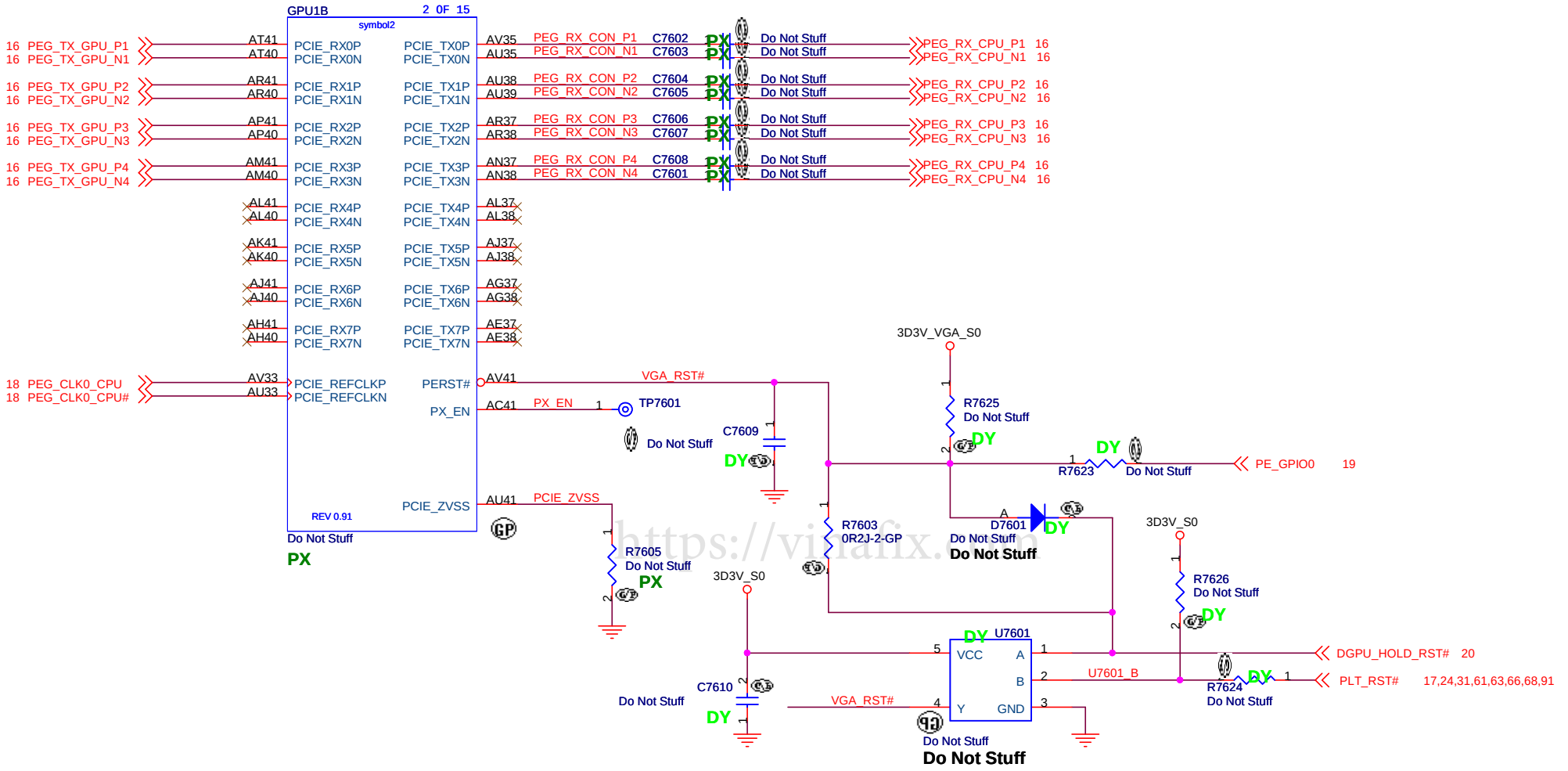
BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ***RESERVED***		
Size A4	Document Number **BOHOL**	Rev **-1**
Date: Tuesday, May 02, 2017	Sheet 75 of 105	



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (1/5) PEG

Size	Document Number	Rev
Custom	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 76 of 105

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (2/5) DIGITALOUT**

Size	Document Number	Rev
Custom	BOHOL	-1

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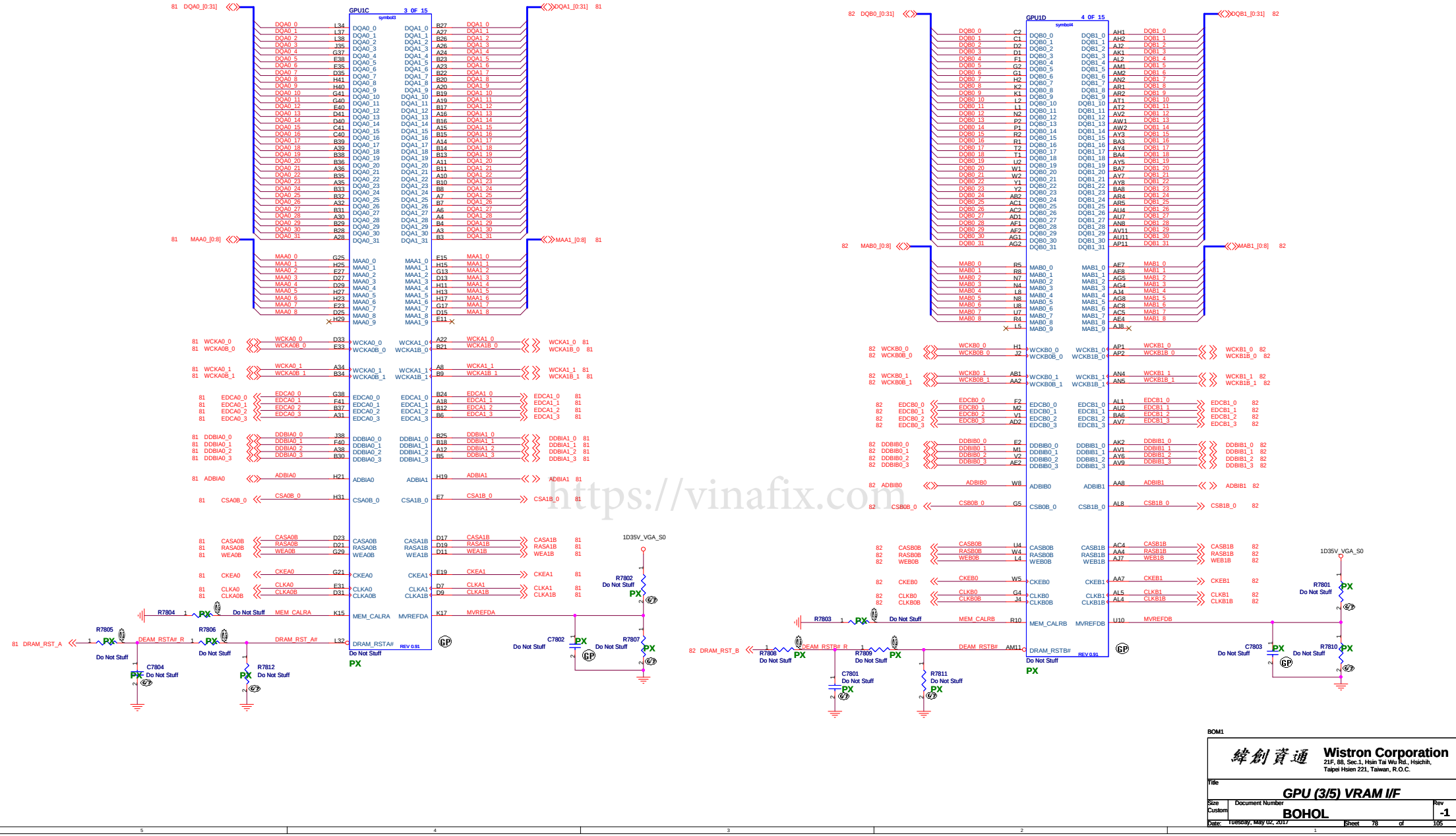
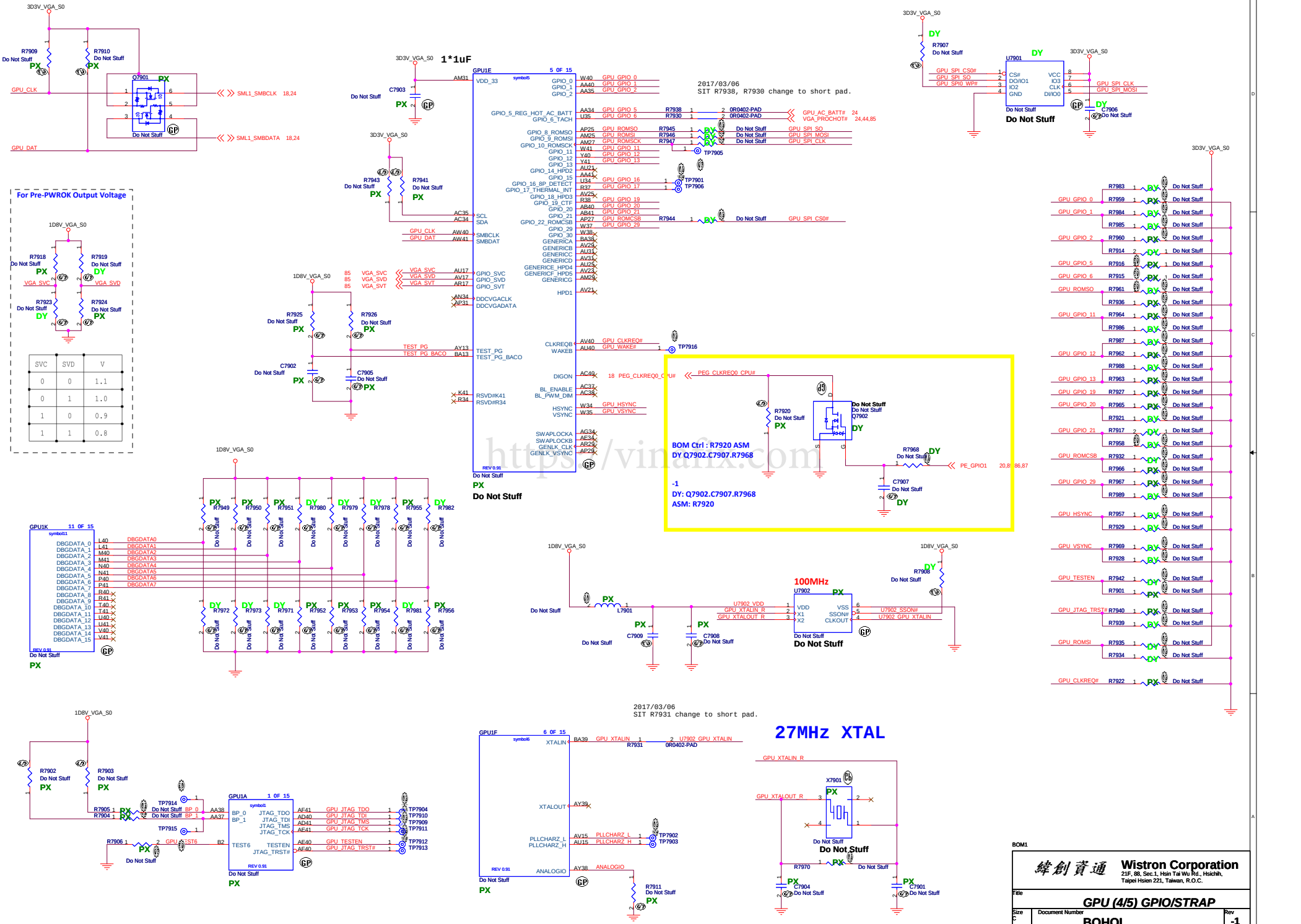
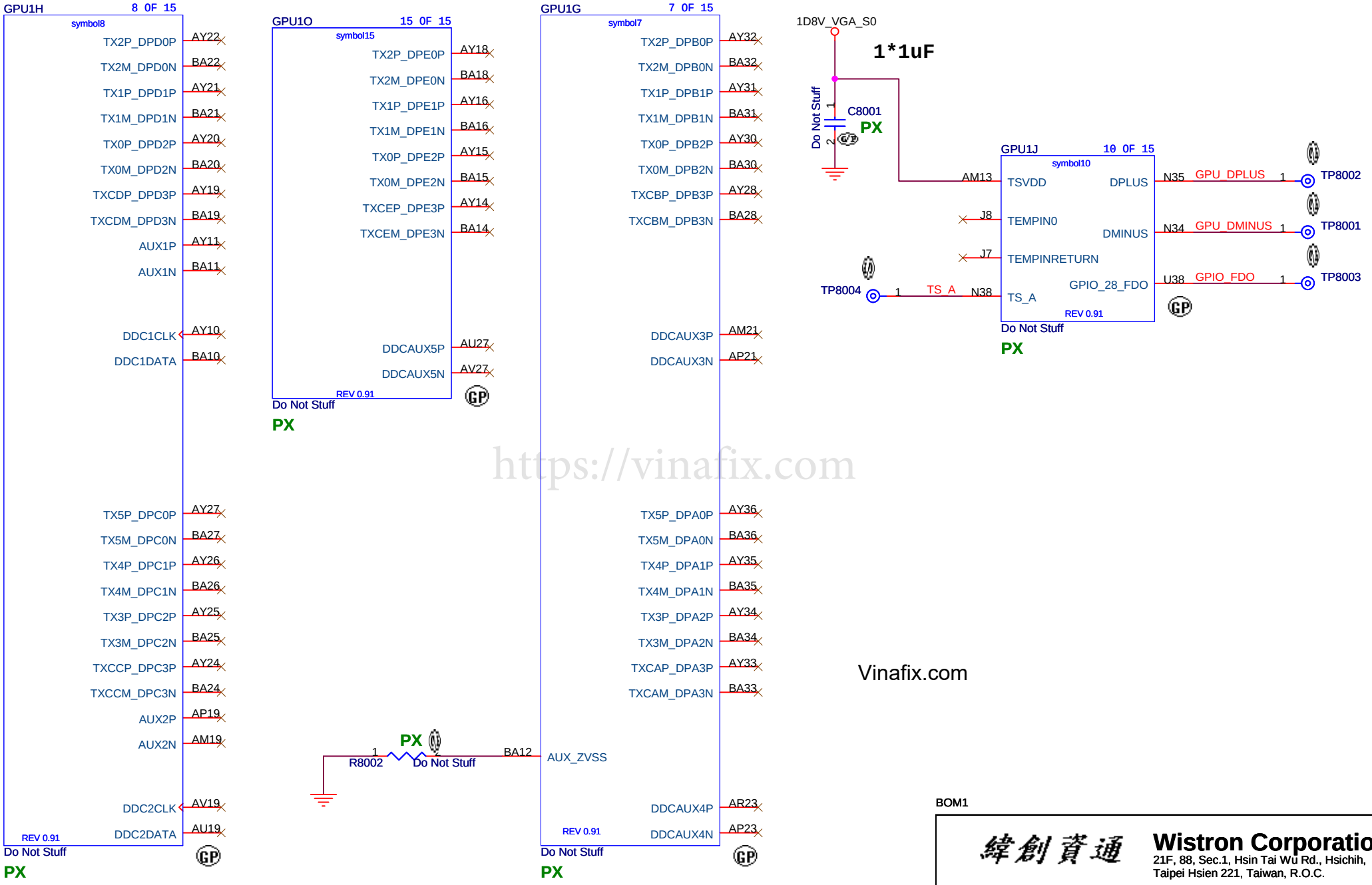
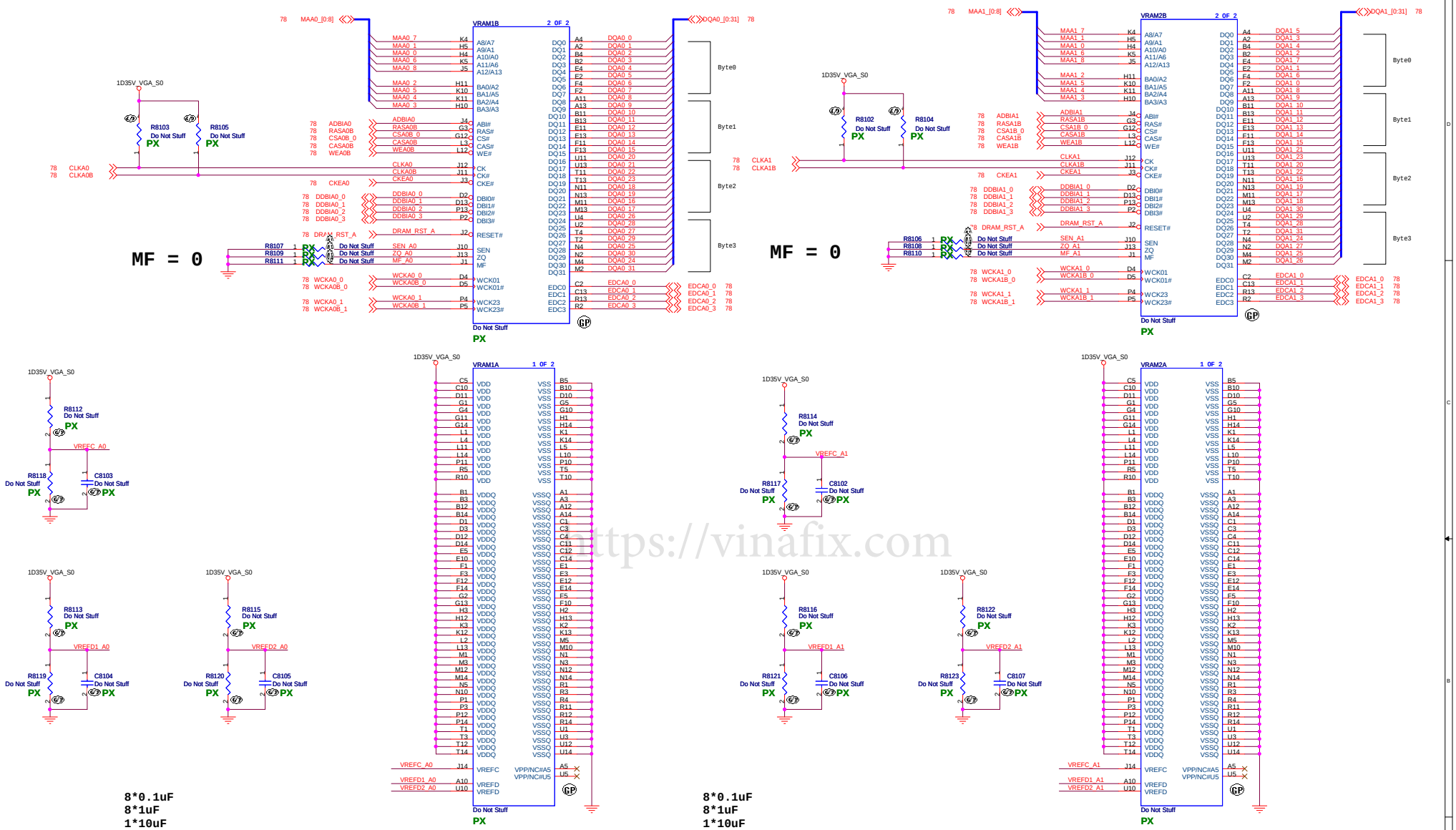






BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU (5/5) PWR/GND*		
Size: A4	Document Number: BOHOL	Rev: -1
Date: Tuesday, May 02, 2017	Sheet 80 of 105	



3/9 RF request

3/9 RF request

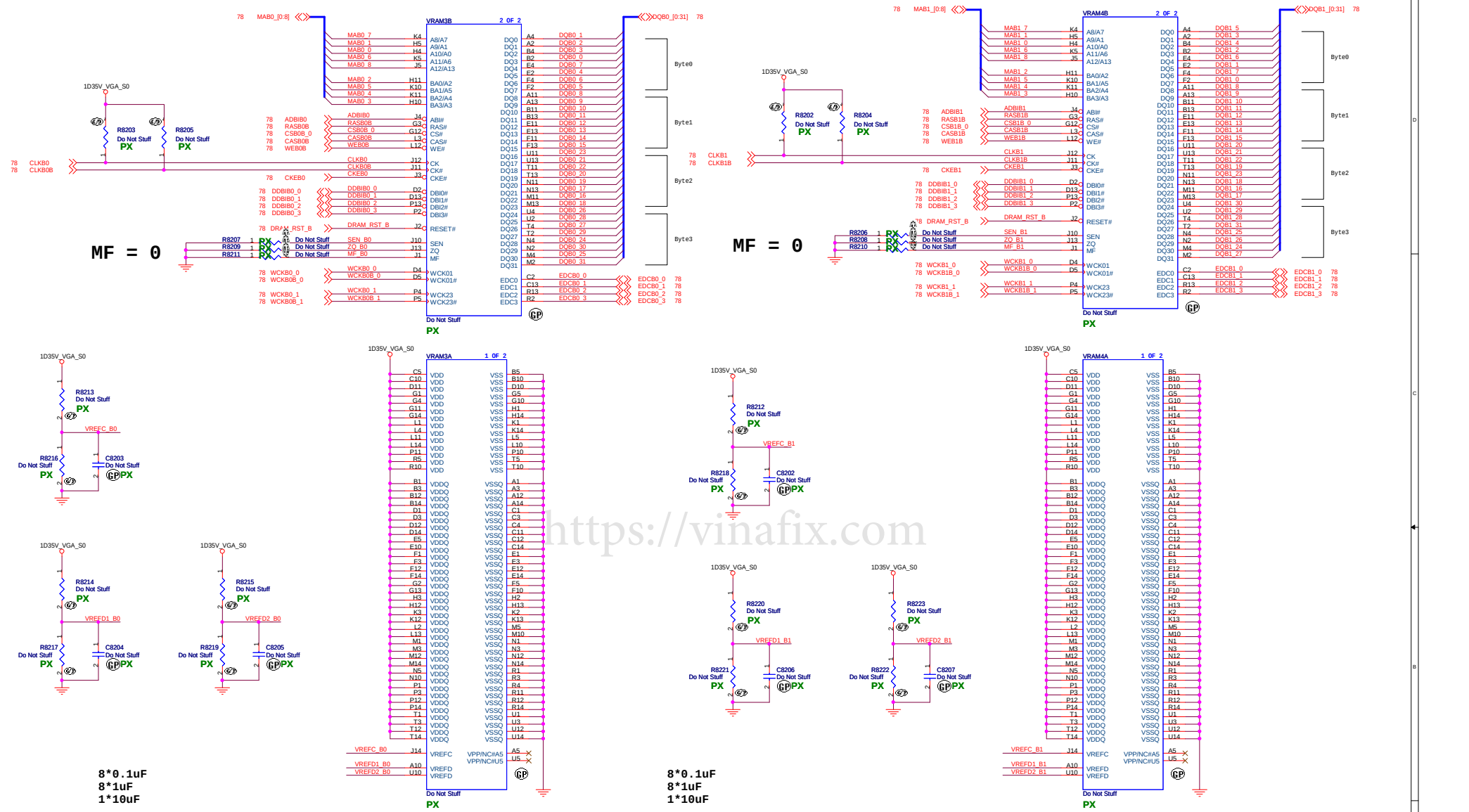
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU VRAM1,2 (1/4)

Size	Document Number	Rev
C	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 81 of 105



3/9 RF request

3/9 RF request

BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU VRAM3,4 (2/4)

Size	Document Number	Rev
C	BOHOL	-1

Date: Tuesday, May 02, 2017 Sheet 82 of 105

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BOM1

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
A	**BOHOL**	**-1**

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BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU VRAM7,8 (4/4)*

Size	Document Number	Rev
A	BOHOL	-1

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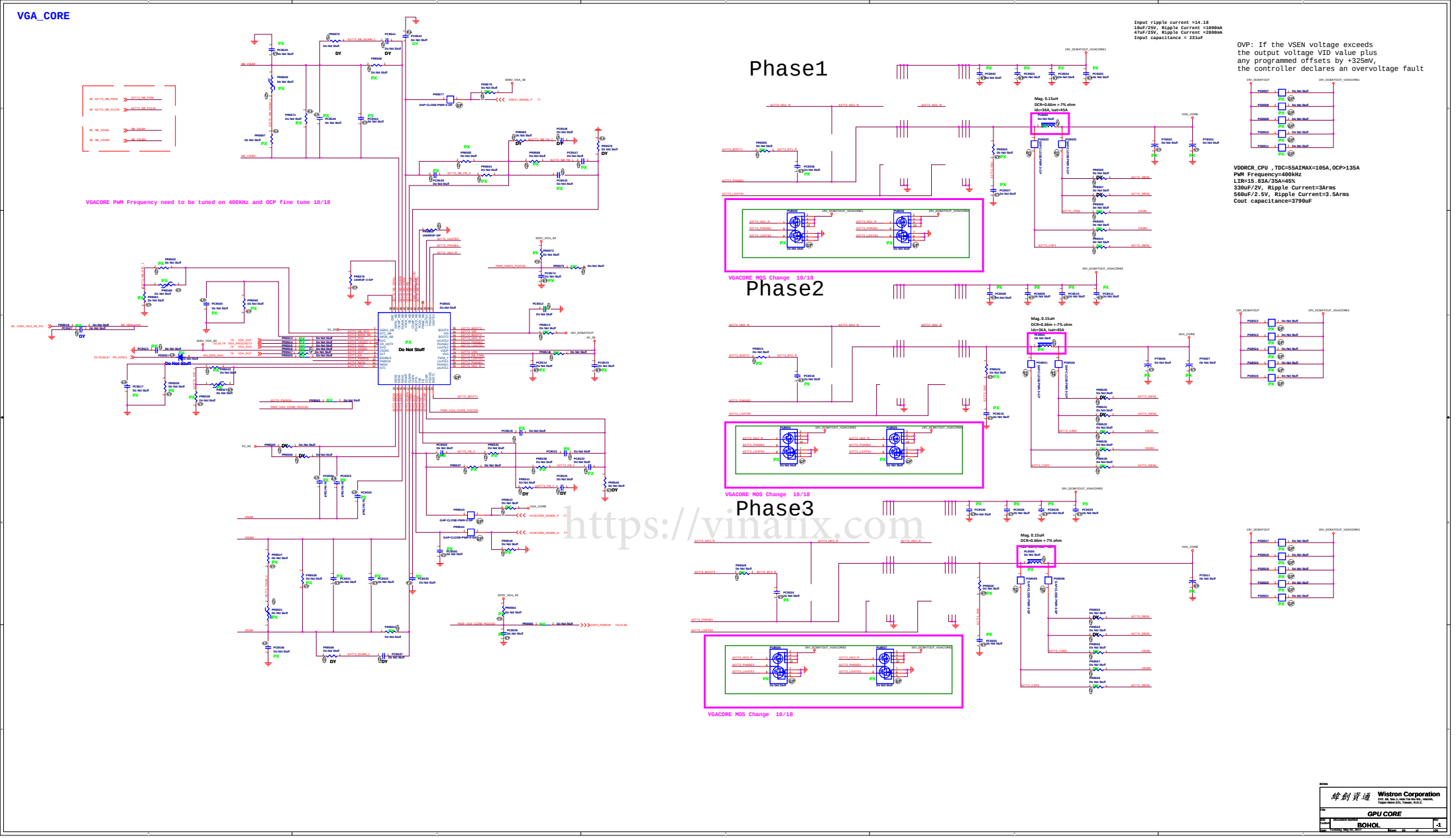
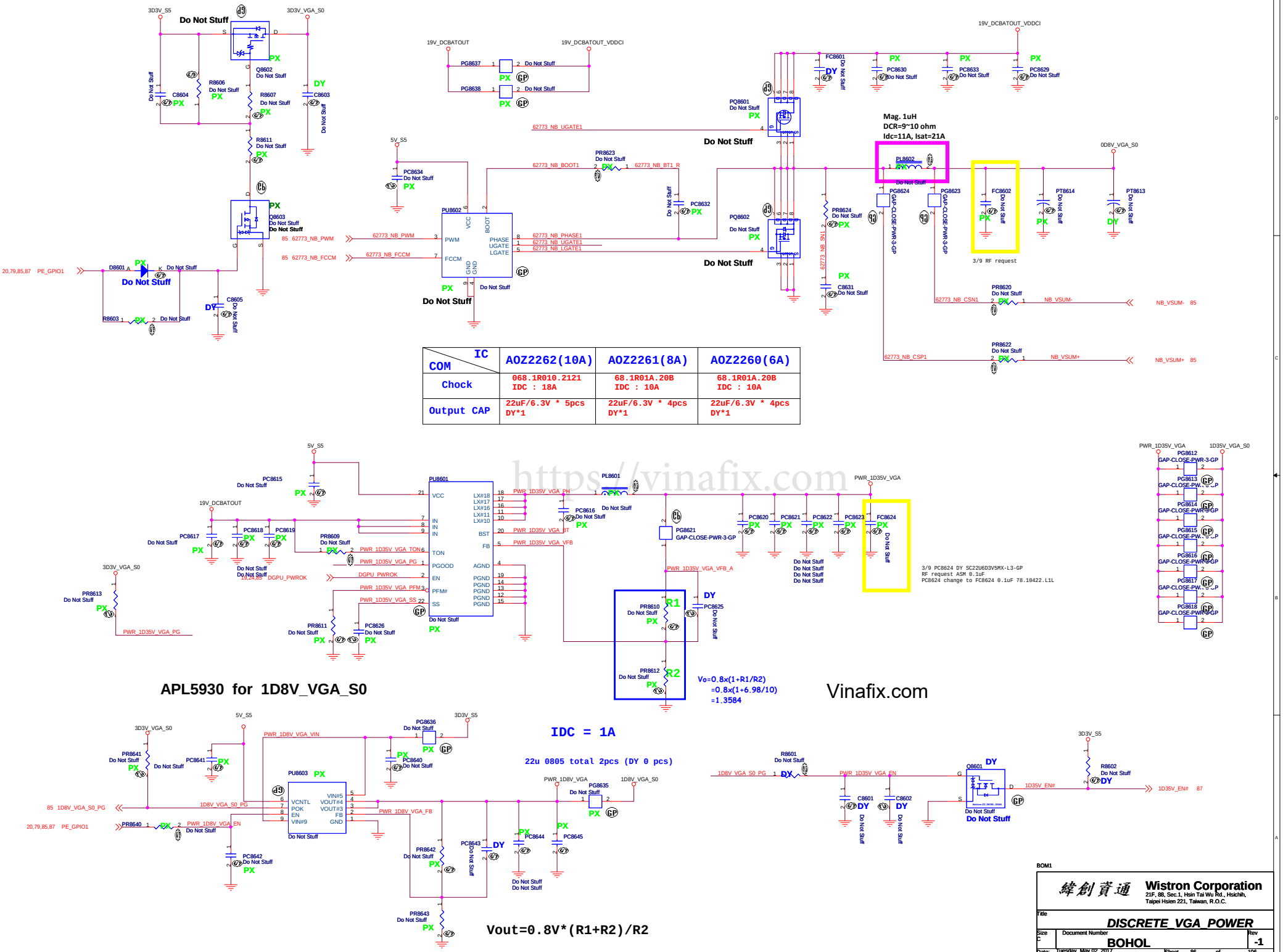
VGA_CORE





IC / COM	AOZ2262(10A)	AOZ2261(8A)	AOZ2260(6A)
Chock	068.1R010.2121 IDC : 18A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE_VGA_POWER

Size: C | Document Number: BOHOL | Rev: -1

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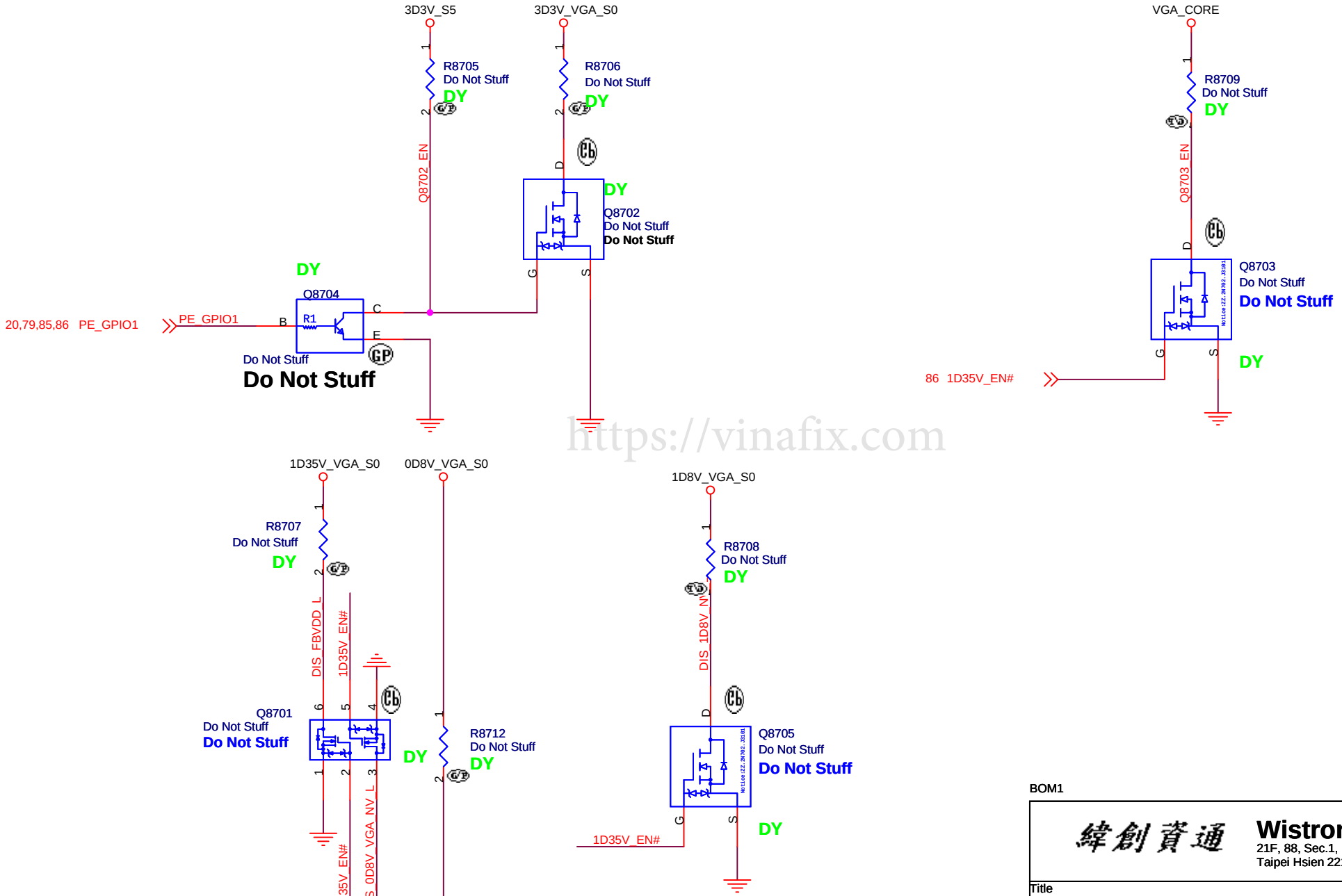
Discharge Circuit



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *GPU DISCHARGE*		
Size: A4	Document Number: BOHOL	Rev: -1
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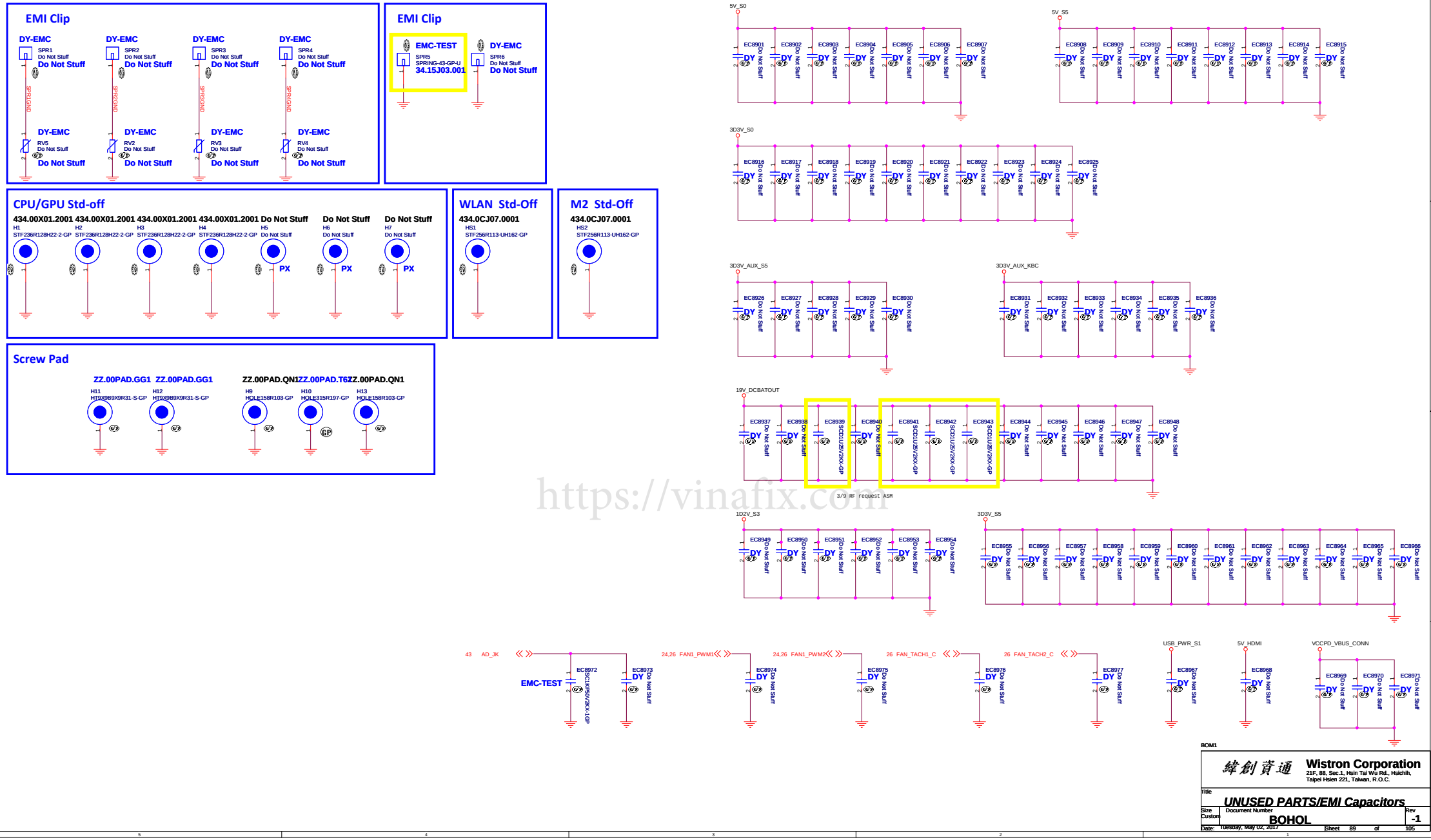
BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
Date: Tuesday, May 02, 2017	Sheet 88 of 105	



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BOM1

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **BOHOL**	Rev: **-1**
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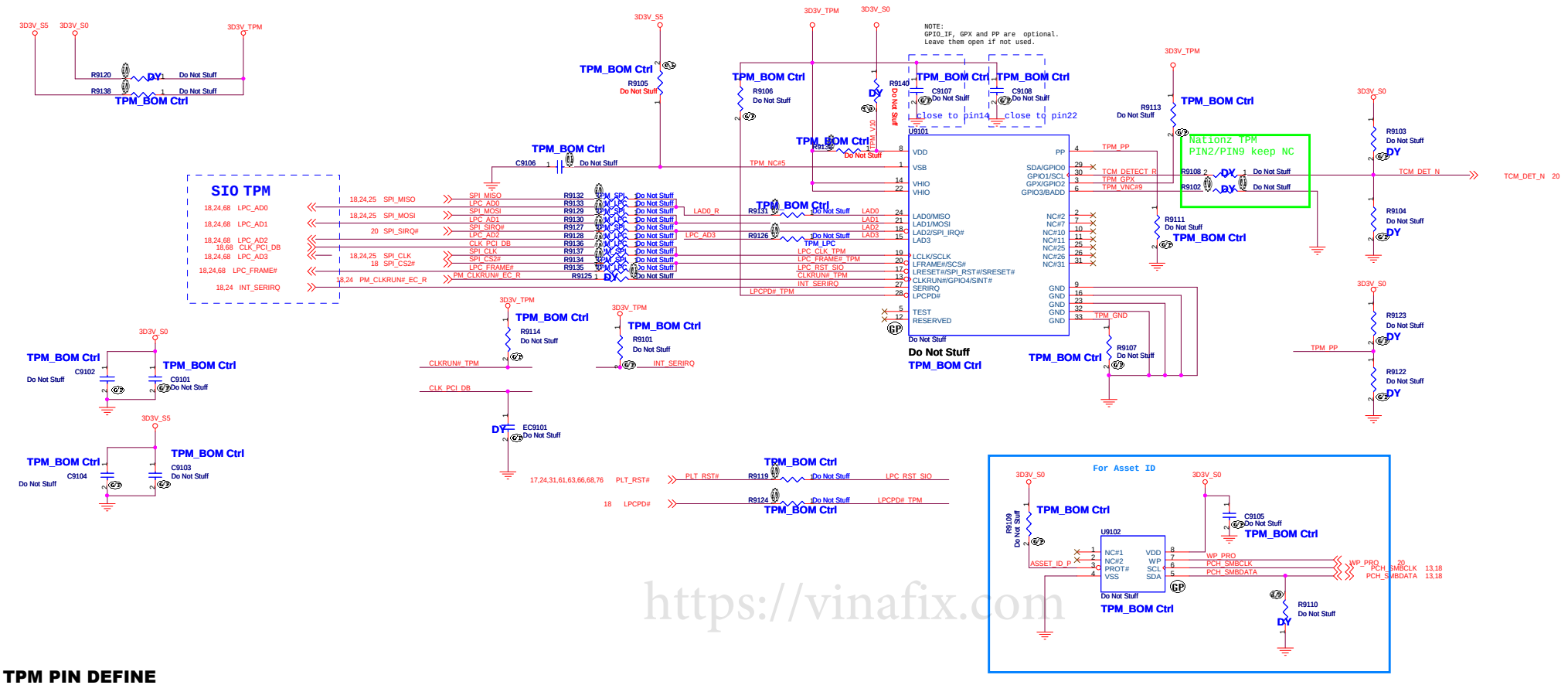

TPM PIN DEFINE

Vendor	ST	Nuvoton	Nationz Tech	Infineon	Lenovo design
PN	ST33ZP24	NPCT650LAAWX	ZH320TC-LPC-T28-401	SLB9665	Colay 4 vendors
Package	TSSOP28, LPC interface				
pin1	NC	GPIO/SDA	NC	NC	Floating
pin2	NC	GPIO/SCL	NC	NC	Floating
pin3	NC	NC	NC	NC	Floating
pin4	GND	GND	GND	GND	Pull down to GND without resistor
pin5	NC	VSB	NC	VCC	Connect to 3VSB and 3VSYS through serial resistor Connect 0.1uf cap to GND,cap near to pin5
pin6	NC	GPIO	NC	GPIO	Floating
pin7	PP	PP	PP	PP	Reserve pull down resistor to GND and pull high resister to VCC
pin8	NC	TEST	NC	NC	Connect to test point
pin9	NC	GPIO	NC	NC	Floating
pin10	VCC	VCC	VCC	VCC	Connect to 3VSYS Connect 10uf and 0.1uf cap to GND,cap near to pin10
pin11	GND	GND	GND	GND	Connect to GND
pin12	NC	NC	NC	NC	Floating
pin13	NC	NC	NC	NC	Floating
pin14	NC	NC	NC	NC	Floating
pin15	NC	CLKRUN#/GPIO	CLKRUN#	NC	Reserve serial resistor to chipset CLKRUN#
pin16	LRESET#	LRESET#	LRESET#	LRESET#	Connect to reset signal through serial resistor
pin17	LAD3	LAD3	LAD3	LAD3	Connect to LAD3 of chipset
pin18	GND	GND	GND	GND	Connect to GND directly
pin19	NC	VCC	VCC	VCC	Connect to 3VSYS through serial resistor Connect 0.1uf cap to GND,cap near to pin19
pin20	LAD2	LAD2	LAD2	LAD2	Connect to LAD2 of chipset
pin21	LCLK	LCLK	LCLK	LCLK	Connect to 33M clock through serial resistor
pin22	LFRAME#	LFRAME#	LFRAME#	LFRAME#	Connect to LFRAME# of chipset
pin23	LAD1	LAD1	LAD1	LAD1	Connect to LAD1 of chipset
pin24	VCC	VCC	VCC	VCC	Connect to 3VSYS
pin25	NC	GND	GND	GND	Connect to GND through serial resistor
pin26	LAD0	LAD0	LAD0	LAD0	Connect to LAD0 of chipset
pin27	SERIRQ	SERIRQ	SERIRQ	SERIRQ	Connect to SERIRQ of chipset or SIO, need pull high resistor
pin28	LPCPD#	LPCPD#	LPCPD#	NC	Connect to GPIO pin through serial resistor

BOM Control	TPM_ST_SPI	TPM_Nuvoton	TPM_NationZ	TPM_Infineon	TCM_NationZ	TPM_ST_LPC
U9101	071.33228.000W	071.00650.0C0W	071.32320.000W	071.09660.000W	071.32320.0A0W	71.03324.F0W
R9105	Un-Stuff	Stuff	Un-Stuff	Un-Stuff	Un-Stuff	Un-Stuff
R9121	Un-Stuff	Un-Stuff	Un-Stuff	Stuff	Un-Stuff	Un-Stuff
R9106	Un-Stuff	Un-Stuff	Stuff	Un-Stuff	Stuff	Un-Stuff
C9107	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
C9108	Stuff	Un-Stuff	Un-Stuff	Un-Stuff	Un-Stuff	Stuff
R9113	Un-Stuff	Un-Stuff	Un-Stuff	Stuff	Un-Stuff	Un-Stuff
R9125	Un-Stuff	Stuff	Un-Stuff	Un-Stuff	Un-Stuff	Un-Stuff
R9112	Un-Stuff	Un-Stuff	Stuff	Un-Stuff	Stuff	Un-Stuff
R9111	Un-Stuff	Un-Stuff	Stuff	Stuff	Stuff	Un-Stuff
R9107	Un-Stuff	Stuff	Stuff	Stuff	Stuff	Un-Stuff
C9106	Un-Stuff	Stuff	Un-Stuff	Stuff	Un-Stuff	Un-Stuff
R9124	Un-Stuff	Stuff	Stuff	Un-Stuff	Stuff	Un-Stuff

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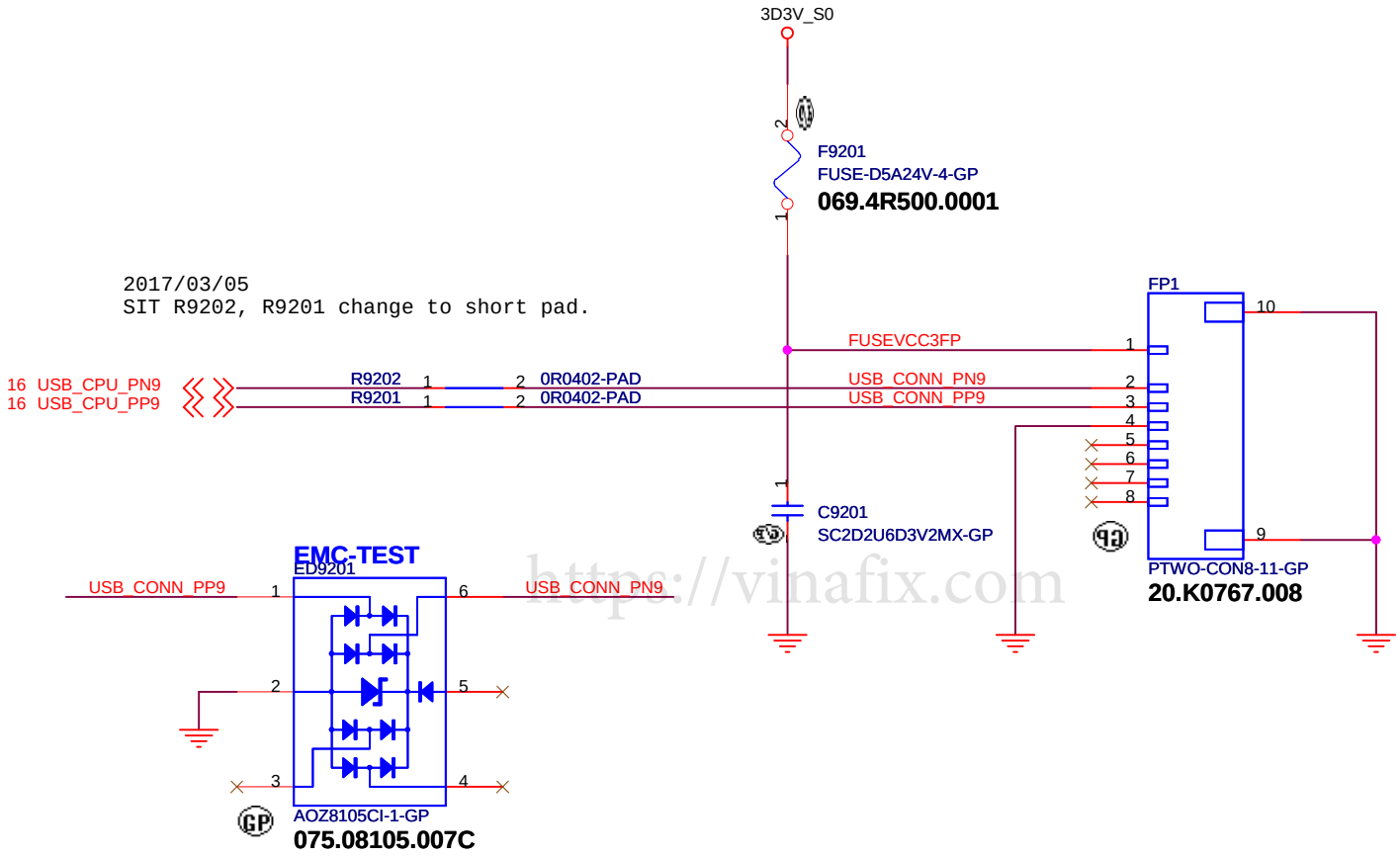

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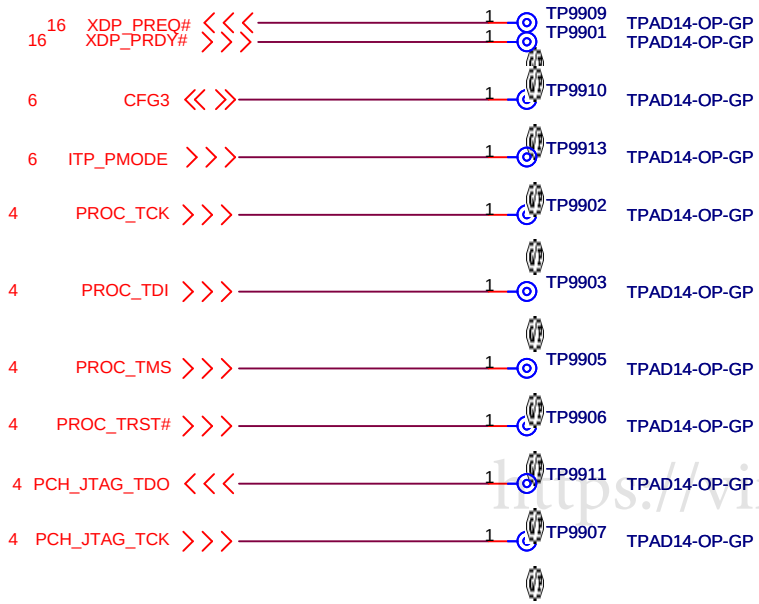

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