Compal Confidential

ELMV2

DIS M/B Schematics Document

Intel Kabylake RU Processor with DDR4

AMD R17M

2017-11-06

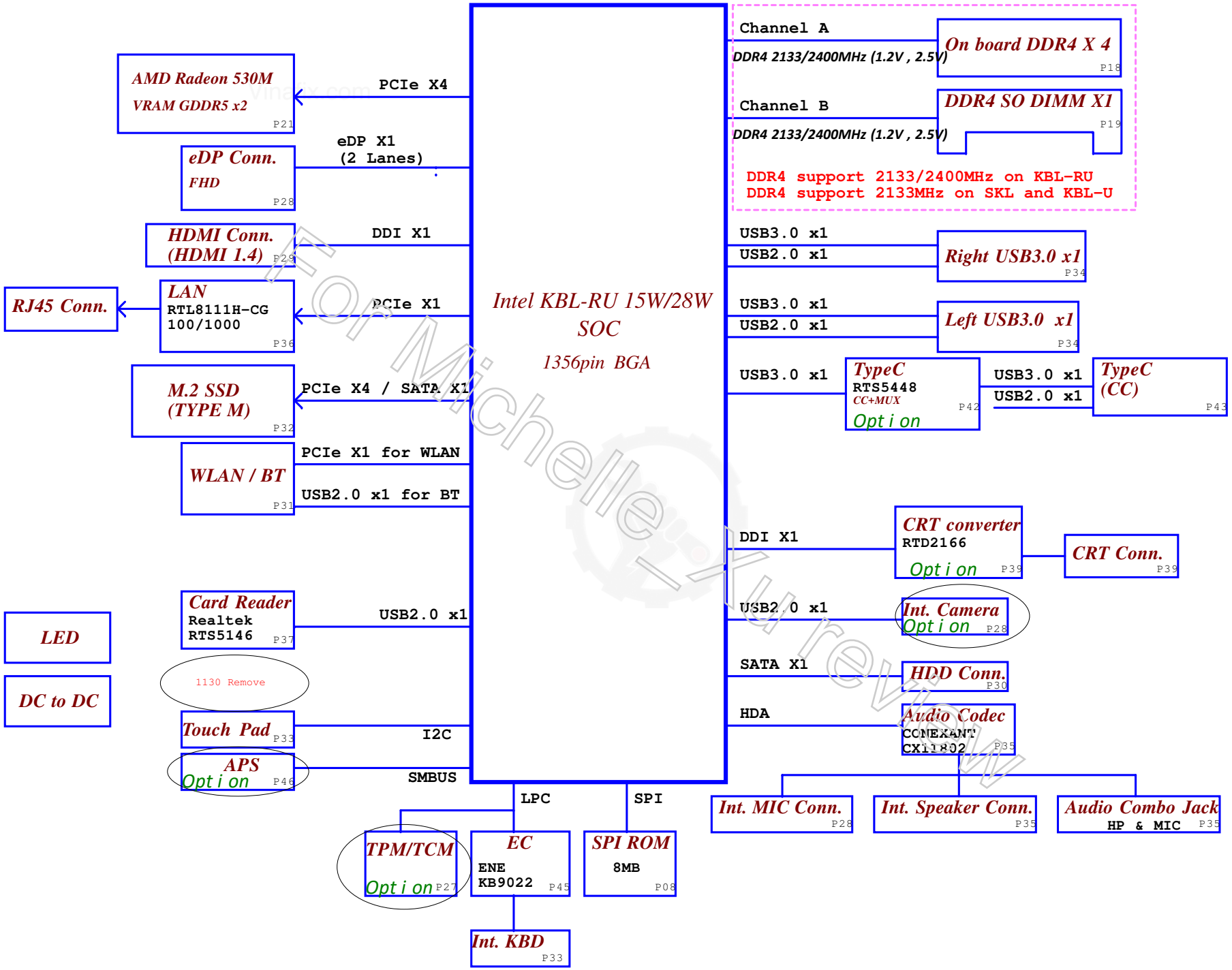
LA-F486P

REV :0.1

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Cover Page

Size	Document Number	Rev
C	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 1 of 66



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Block Diagram
Size: C	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 2 of 66		

Voltage Rails

State \ power plane	+RTCBATT	+B +5VL +3VL	+5VALW +3VALW +1.8VALW +1VALW	+1.0V_VCCST +2.5V +1.2V	+5VS +3VS +3VGS +1.8VGS +1.0VS_VCCIO +PCIE_VGS +VGA_CORE +1.35VS_VRAM +0.6VS +VCCCORE +VCCGT +VCCSA
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 and S4/AC	O	O	O	X	X
S5 and S4/Battery only	O	O	X	X	X
S5 and S4/AC&Battery don't exist(Only RTC)	O	X	X	X	X

USB 2.0 Port Table

Port	3 External USB Port
1	USB 3.0 Port
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	
5	Camera
6	M.2 BT
7	Card Reader
8	
9	
10	

USB 3.0 Port Table

Port	
1	USB 3.0 Port
2	USB 3.0 Port
3	TYPE-C USB 3.0 Port
4	
5	
6	

SATA Port Table

Port	
0	HDD
1	
2	M.2 SATA SSD

PCIE Port Table

Port	Lane	
1	1	GPU
2	2	
3	3	
4	4	
5		LAN
6		M.2 WLAN+BT
7		
8		
9		
10		M.2 PCIE*4 SSD
11		
12		

BOM Structure Table

Item	BOM Structure
SKL only	SKL@
For 2+2	U22@
For 4+2	U42@
For DIS	DIS@
For UMA	UMA@
EMI pop	EMI@
EMI Un-pop	@EMI@
ESD pop	ESD@
ESD Un-pop	@ESD@
RF pop	RF@
RF unpop	@RF@
For SPI 8M	8M@
NONAOU	NONAOU@
NO 2nd Battery	NOBATT2@
Camera	CMOS@
TPM	TPM@
TCM	TCM@
NO TPM/TCM	NOTPM@
TYPEC 5448	TYPEC@
NONTYPEC	NONTYPEC@
APS	APS@
NOAPS	NOAPS@
CRT@	CRT@
SPEAKER STEREO	STE@
SPEAKER MONO	MONO@
Onboard RAM HYNIX	X76DDRH@
Onboard RAM MICRON	X76DDRM@
Onboard RAM SAMSUNG	X76DDRS@
VRAM HYNIX	X76H2G@
VRAM MICRON	X76M4G@
VRAM SAMSUNG	X76S2G@
Connector	ME@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

PCH SM Bus address

Device	Address
DDR_JDIMM1 RTD2166	1010 000x A0h 1100 100 A0h

SMBUS Control Table

	SOURCE	GPU	BATT	NECP388	SODIMM	SOC
SMB_EC_CK1 SMB_EC_DA1	EC KB9022 +3VALW	X	V +3VALW	X	X	X
SMB_EC_CK2 SMB_EC_DA2	EC KB9022 +3VS	V +3VGS	X	X	X	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V(RAM)	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

CPU

2+2

2+3

SKL-U

UC1 CPU1@ i7-6500U SA000092P80
UC1 CPU2@ i5-6300U SA000092T60
UC1 CPU3@ i5-6200U SA000092OA0
UC1 CPU4@ i3-6006U SA0000ACN10
1003 CPU3@ change to 920A0
UC1 CPU5@ i7-6567U SA00009E620
UC1 CPU6@ i5-6267U SA00009E510

KBL-U

UC1 CPU7@ i5-7100U SA0000B2Y20
UC1 CPU8@ i5-7200U SA0000A3730
UC1 CPU9@ i7-7500U SA0000A34A0
UC1 CPU10@ i5-7300U SA0000ADO60
UC1 CPU11@ 3865U SA0000ADL61
UC1 CPU12@ 4415U SA0000ADV20
UC1 CPU13@ i7-7567U SA0000AW630
UC1 CPU14@ i5-7267U SA0000AKR30

KBL-RU 4+2

UC1 CPU15@ KBL-R QN5D SA0000AR010
UC1 CPU16@ KBL-R QN5C SA0000AQZ10
UC1 CPU17@ KBL-R QNEF SA0000AWB00
UC1 CPU18@ KBL-R QNBF SA0000AWC00
UC1 CPU19@ KBL-R QNEF SA0000AWB50
UC1 CPU20@ KBL-R QNBF SA0000AWC50

X4E	TYPEC_5448	CRT
X4EACE38L01	Y	Y
X4EACE38L02	N	Y

ZZZ X4E1@ X4E X4EACE38L01
ZZZ X4E2@ X4E X4EACE38L02

1215 update

On Board RAM

ZZZ X76DDR4H@ 2G HYNIX X7675138L01
ZZZ X76DDR4M@ 2G MICRON X7675138L02
ZZZ X76DDR4S@ 2G SAMSUNG X7675138L03

GPU

UV1 GPU1@ VGA SA000098VB0
UV1 GPU2@ VGA SA000098VC0

ZZZ PCB DA6001Z7000

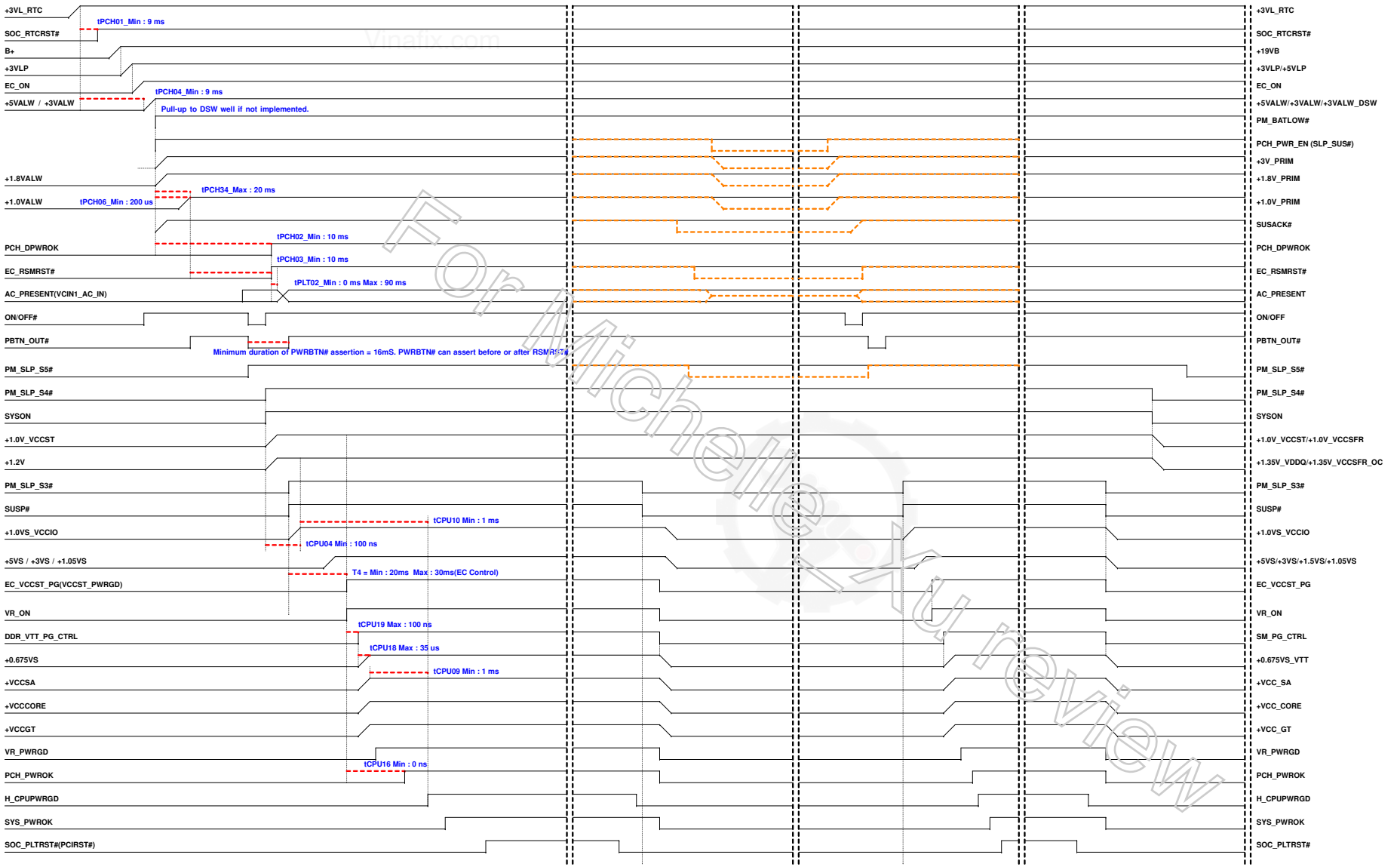
Security Classification	Compal Secret Data
Issued Date	Deciphered Date

Compal Electronics, Inc.

Title: Notes List

Size: C | Document Number: LA-F486P | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 3 of 66



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Power Sequence
			Size: Document Number: LA-F486P Rev: 0.3
			Date: Tuesday, December 19, 2017 Sheet: 4 of 66

M1-30 VRAM STRAP

	X76@ Vendor UV3, UV4, UV5, UV6	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV22	X76@ R_pd RV27
X76S2G@ X7675138L06	SAMSUNG 4096Mbits 2GBytes SA000092D30 256M32 K4G80325FB-HC28	0	0	0	0	NC	4.75K
X76H2G@ X7675138L04	HYNIX 4096Mbits 2GBytes SA00009U130 256M32 H5GC8H24MJR-R0C	1	0	0	1	8.45K	2K
X76M2G@ X7675138L05	MICRON 4096Mbits 2GBytes SA00009TV20 256M32 MT51J256M32HF-70:A	2	0	1	0	4.53K	2K
		4	1	0	0	4.53K	4.99K
		5	1	0	1	3.24K	5.62K
		6	1	1	0	3.4K	10K

zzz zzz zzz

X76H2G@ 2G HYNIX X7675138L04

X76M2G@ 2G MICRON X7675138L05

X76S2G@ 2G SAMSUNG X7675138L06

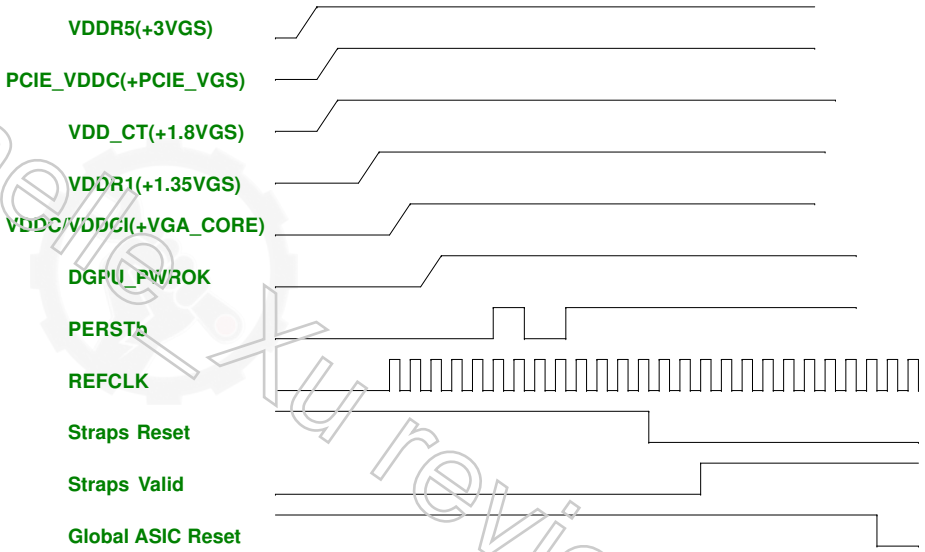
R_pu (Ω)	R_pd (Ω)	Bits [2:0]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

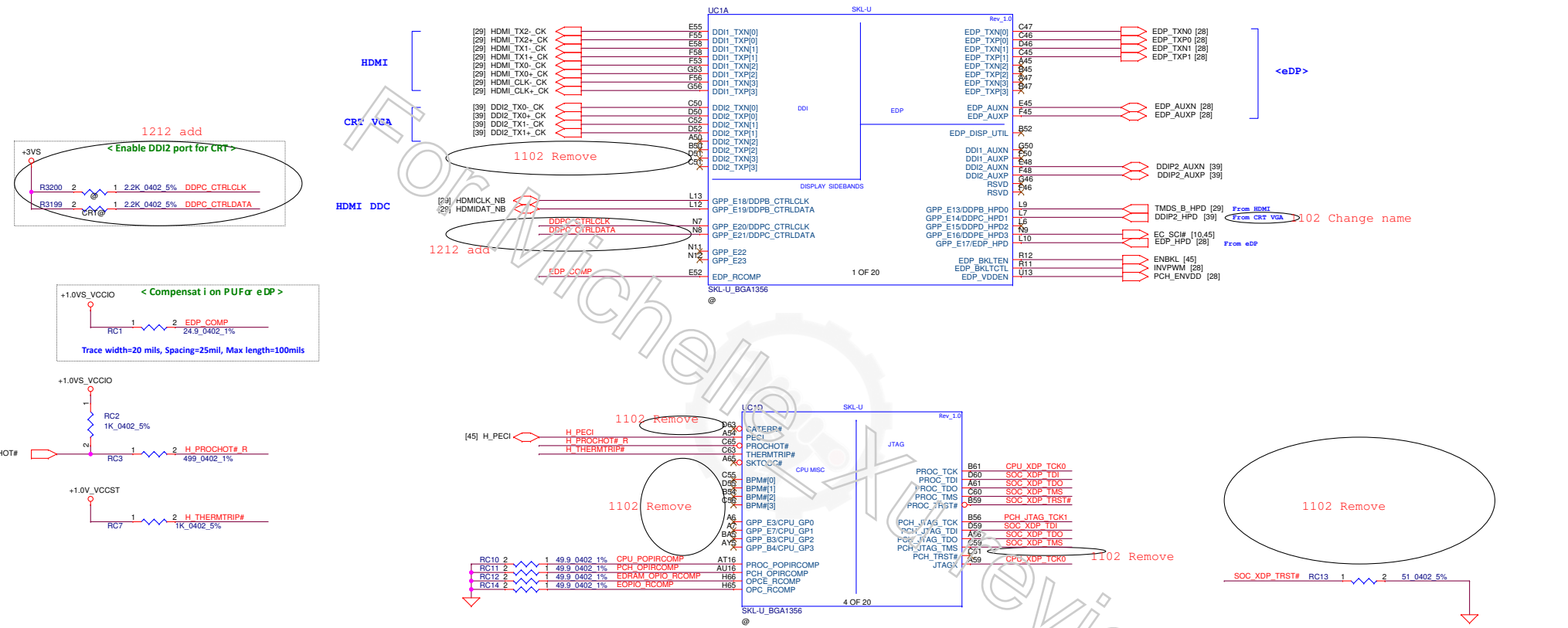
Power-Up/Down Sequence

"M1" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.
- It is recommended that the 3.3-V rail ramp up frist.
- It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2ms from the start of VDDC ramping up.
- The power rails that are shared with other components on the system should be gated for the dGPU so that when dGPU is powered down (for example AMD PowerXpressTM idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≦ 50mV/us)
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/02	Deciphered Date	2018/08/02
Title	VGA Notes List		
Size C	Document Number LA-F486P		Rev 0.3
Date: Tuesday, December 19, 2017	Sheet 5 of 66		



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

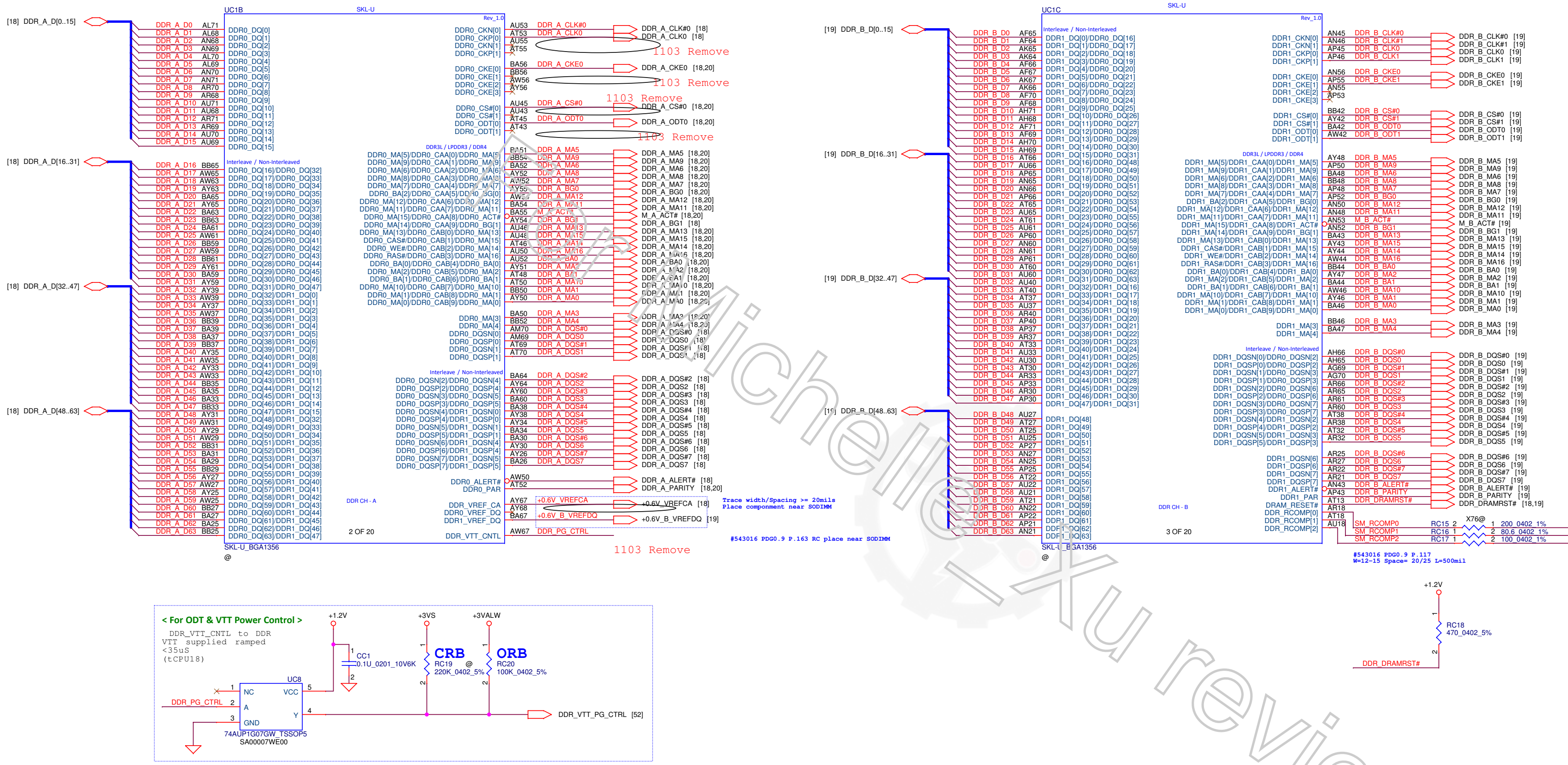
Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,EDP,MISC,CMC

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 6 of 66

Interleaved Memory



	SDP	DDP
RC15	200 1%	121 1%

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: SKL-U(2/12)DDR4

Size: Custom | Document Number: LA-F486P | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 7 of 66

SMBALERT# (Internal Pull Down):

0 = Disable Intel ME TLS function ==> Default

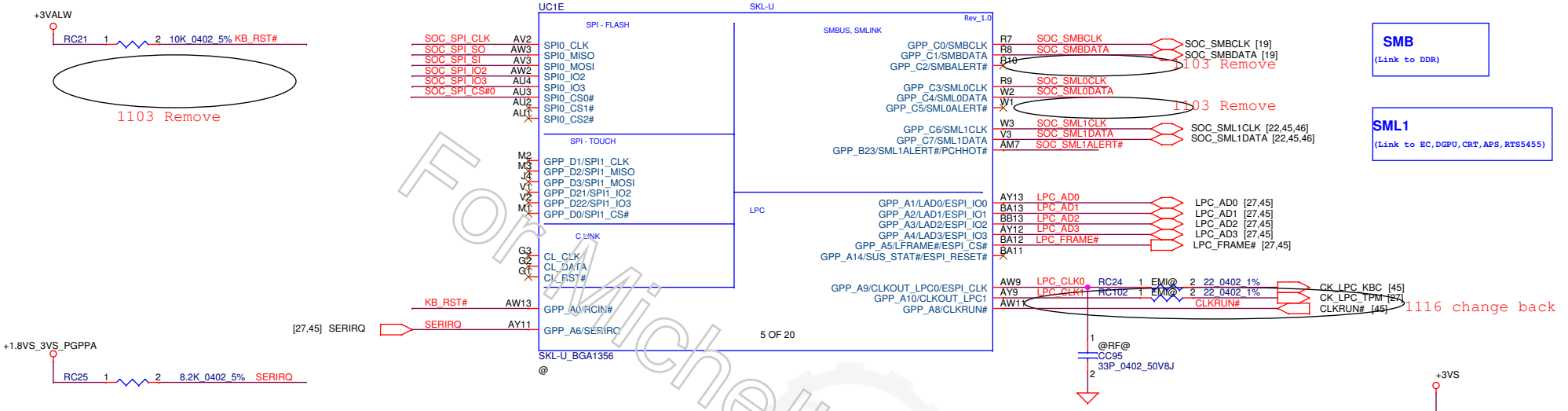
1 = Enable Intel ME TLS function

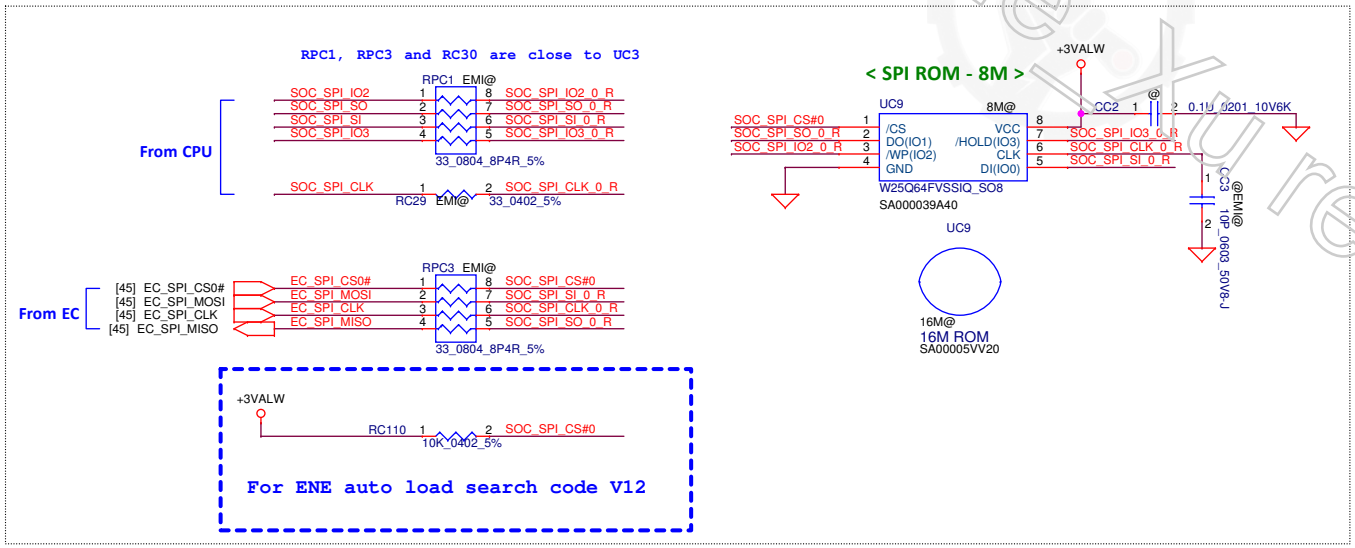
SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC





Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 8 of 66

< HD AUDIO >

RPC4_EMI@

[35] HDA_BITCLK_AUDIO — 1 — 8 — HDA_BIT_CLK
[35] HDA_SYNC_AUDIO — 2 — 7 — HDA_SYNC
[35] HDA_SDOUT_AUDIO — 3 — 6 — ME_EN
[35] HDA_RST_AUDIO# — 4 — 5 — HDA_RST#

33_0804_8P4R_5%

< To Enable ME Override >

UC1G — SKL-U — Rev_1.0

AUDIO

[44] HDA_SYNC — HDA_SYNC — BA22 — HDA_SYNC/I2S0_SFRM
[44] HDA_BIT_CLK — HDA_BIT_CLK — AY22 — HDA_BLK/I2S0_SCLK
[44,45] ME_EN — ME_EN — BB22 — HDA_SDO/I2S0_TXD
[35] HDA_SDIN0 — BA21 — HDA_SDI0/I2S0_RXD
AY21 — HDA_SDI1/I2S1_RXD
[44] HDA_RST# — HDA_RST# — AW22 — HDA_RST#/I2S1_SCLK
J5 — GPP_D23/I2S_MCLK
AY20 — I2S1_SFRM
AW20 — I2S1_TXD

AK7 — GPP_F1/I2S2_SFRM
AK8 — GPP_F0/I2S2_SCLK
AK9 — GPP_F2/I2S2_TXD
AK10 — GPP_F3/I2S2_RXD

H5 — GPP_D19/DMIC_CLK0
D7 — GPP_D20/DMIC_DATA0

1103 Remove
D8 — GPP_D17/DMIC_CLK1
C8 — GPP_D18/DMIC_DATA1

[35] HDA_SPKR — HDA_SPKR — AW5 — GPP_B14/SPKR

7 OF 20

SDIO / SDXC

AB11 — GPP_G0/SD_CMD
AB13 — GPP_G1/SD_DATA0
AB12 — GPP_G2/SD_DATA1
W12 — GPP_G3/SD_DATA2
W11 — GPP_G4/SD_DATA3
W10 — GPP_G5/SD_CD#
W8 — GPP_G6/SD_CLK
W7 — GPP_G7/SD_WP

BA9 — GPP_A17/SD_PWR_EN#/ISH_GP7
BB9 — GPP_A16/SD_1P8_SEL

AB7 — SD_RCOMP

AF13 — GPP_F23

1103 Remove

SKL-U_BGA1356
@

1103 Remove

UC1I — SKL-U — Rev_1.0

CSI-2

A36 — CSI2_DN0
B35 — CSI2_DP0
C38 — CSI2_DN1
D38 — CSI2_DP1
C36 — CSI2_DN2
D36 — CSI2_DP2
A38 — CSI2_DN3
B38 — CSI2_DP3

C31 — CSI2_DN4
D31 — CSI2_DP4
C33 — CSI2_DN5
D33 — CSI2_DP5
A31 — CSI2_DN6
B31 — CSI2_DP6
A33 — CSI2_DN7
B33 — CSI2_DP7

A29 — CSI2_DN8
B29 — CSI2_DP8
C28 — CSI2_DN9
D28 — CSI2_DP9
A27 — CSI2_DN10
B27 — CSI2_DP10
C27 — CSI2_DN11
D27 — CSI2_DP11

CSI2_CLKN0 — C37
CSI2_CLKP0 — D37
CSI2_CLKN1 — C32
CSI2_CLKP1 — D32
CSI2_CLKN2 — C29
CSI2_CLKP2 — D29
CSI2_CLKN3 — B26
CSI2_CLKP3 — A26

CSI2_COMP — E13
GPP_D4/FLASHTRIG — B7

EMMC

GPP_F13/EMMC_DATA0 — AP2
GPP_F14/EMMC_DATA1 — AP1
GPP_F15/EMMC_DATA2 — AP3
GPP_F16/EMMC_DATA3 — AN2
GPP_F17/EMMC_DATA4 — AN1
GPP_F18/EMMC_DATA5 — AN3
GPP_F19/EMMC_DATA6 — AM4
GPP_F20/EMMC_DATA7 — AM1

GPP_F21/EMMC_RCLK — AM2
GPP_F22/EMMC_CLK — AM3
GPP_F12/EMMC_CMD — AP4

EMMC_RCOMP — AT1

9 OF 20

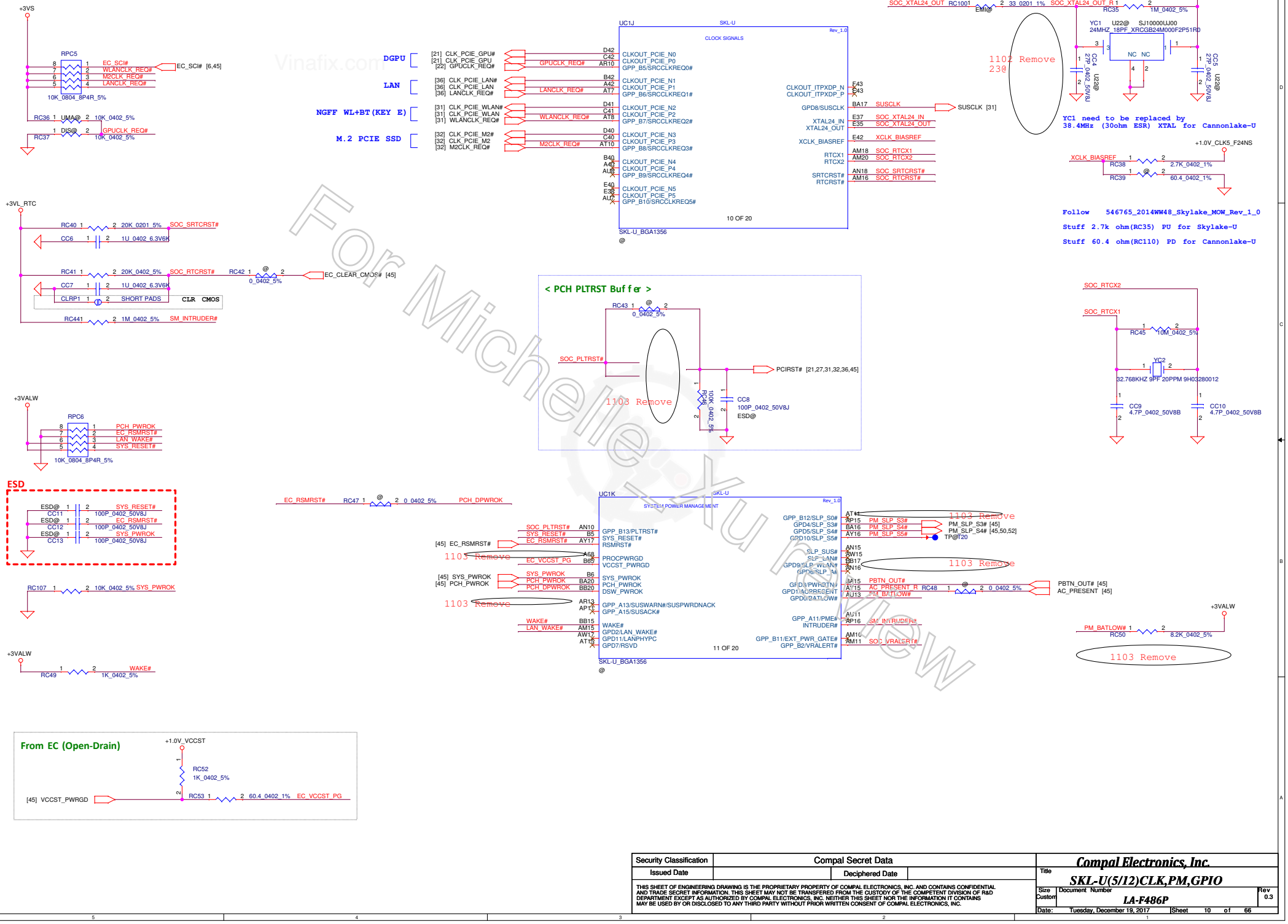
1103 Remove

1103 Remove

SKL-U_BGA1356
@

1103 Remove

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2
Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 9 of 66		



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: **SKL-U(5/12)CLK,PM,GPIO**

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 | Sheet 10 of 66

RAM vender	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0
Hynix	1	1	1
Micron	1	1	0
Samsung	1	0	1
Reserve	1	0	0

Reserve

RC105 10K_0402_5% X76@ — OBRAM_ID2 — RC104 10K_0402_5% X76@

RC55 10K_0402_5% X76@ — OBRAM_ID1 — RC57 10K_0402_5% X76@

RC54 10K_0402_5% X76@ — OBRAM_ID0 — RC56 10K_0402_5% X76@

1103 Remove

RC1031 2 10K_0402_5% WLBT_OFF#

RC1061 2 10K_0402_5% DMIC_DET#

1130 Remove

If UART interface is used, 50 KΩ pull-up resistors to 3.3V are required on all UART signals.
If the interface is not used, the signals can be used as GPIO. If GPIO functionality is also not used, the signals can be left as no-connect.

R469 1 2 2.2K_0201_5% I2C1_SDA_TP

R470 1 2 2.2K_0201_5% I2C1_SCL_TP

1102 Remove

[33] TP_INT#
[28] DMIC_DET#
[31] WLBT_OFF#
T255 TP@
T256 TP@

1103 Remove intersheet
1130 add test point

[33] I2C1_SDA_TP
[33] I2C1_SCL_TP

UC1F — SKL-U — LPSS — ISH — Rev_1.0

OBRAM_ID2	AN8	GPP_B15/GSPI0_CS#
OBRAM_ID0	AP7	GPP_B16/GSPI0_CLK
OBRAM_ID1	AP8	GPP_B17/GSPI0_MISO
GSPI0_MOSI	AR7	GPP_B18/GSPI0_MOSI
	AM5	GPP_B19/GSPI1_CS#
	AN7	GPP_B20/GSPI1_CLK
	AP6	GPP_B21/GSPI1_MISO
GSPI1_MOSI	AN5	GPP_B22/GSPI1_MOSI
	AB1	
	AB2	GPP_C8/UART0_RXD
	AB4	GPP_C9/UART0_TXD
	AB3	GPP_C10/UART0_RTS#
WLBT_OFF#	AB5	GPP_C11/UART0_CTS#
UART_2_CRXD_DTXD	AD1	GPP_C20/UART2_RXD
UART_2_CTXD_DRXD	AD2	GPP_C21/UART2_TXD
	AD3	GPP_C22/UART2_RTS#
	AD4	GPP_C23/UART2_CTS#
	U7	
I2C1_SDA_TP	U8	GPP_C16/I2C0_SDA
I2C1_SCL_TP	U9	GPP_C17/I2C0_SCL
		GPP_C18/I2C1_SDA
		GPP_C19/I2C1_SCL
	AH9	
	AH10	GPP_F4/I2C2_SDA
		GPP_F5/I2C2_SCL
	AH11	
	AH12	GPP_F6/I2C3_SDA
		GPP_F7/I2C3_SCL
	AF11	
	AF12	GPP_F8/I2C4_SDA
		GPP_F9/I2C4_SCL

	P2	GPP_D9
	P3	GPP_D10
	P4	GPP_D11
	P1	GPP_D12
	M4	GPP_D5/ISH_I2C0_SDA
	N3	GPP_D6/ISH_I2C0_SCL
	N1	GPP_D7/ISH_I2C1_SDA
	N2	GPP_D8/ISH_I2C1_SCL
	AD11	GPP_F10/I2C5_SDA/ISH_I2C2_SDA
	AD12	GPP_F11/I2C5_SCL/ISH_I2C2_SCL
	U1	GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
	U2	GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
	U3	GPP_D15/ISH_UART0_RTS#
	U4	GPP_D16/ISH_UART0_CTS#/SML0BALERT#
	AC1	GPP_C12/UART1_RXD/ISH_UART1_RXD
	AC2	GPP_C13/UART1_TXD/ISH_UART1_TXD
	AC3	GPP_C14/UART1_RTS#/ISH_UART1_RTS#
	AB4	GPP_C15/UART1_CTS#/ISH_UART1_CTS#
	AY8	GPP_A18/ISH_GP0
	BA8	GPP_A19/ISH_GP1
	BB7	GPP_A20/ISH_GP2
	BA7	GPP_A21/ISH_GP3
	AY7	GPP_A22/ISH_GP4
	AW7	GPP_A23/ISH_GP5
	AP13	Sx_EXIT_HOLDOFF# / GPP_A12 / BM_BUSY# / ISH_GP6

SKL-U_BGA1356
@

R3198 1 @ 2 0_0201_5% — SPEAKER_STRAP — DIR_SET [42]
S_BATT_STRAP
V130_STRAP

1103 add back

RC121 10K_0402_5%

1213 add strap pin for V130_strap
1214 change resist to 10K

DGPU_PWR_EN
DGPU_HOLD_RST#
DGPU_PWROK
DGPU_PRSNT#

DGPU_PWR_EN [23,45,57,58]
DGPU_HOLD_RST# [21]
DGPU_PWROK [57,58]

1103 add back

RPC7 DIS@
DGPU_HOLD_RST# 1 8
DGPU_PWR_EN 2 7
DGPU_PWROK 3 6
DGPU_PRSNT# 4 5
10K_0804_8P4R_5%

DGPU_PRSNT# PD for DIS SKU

Function	GPP_C15
UMA	1
DIS	0

RC62 1 UMA@ 2 10K_0402_5% DGPU_PRSNT#

Function	GPP_D10
STEREO	1
MONO	0

SPEAKER_STRAP — STE@ RC118 — MONO@ RC117

Function	GPP_A18
AOU	1
NONAOU	0

AOU_STRAP — AOU@ RC112 — NONAOU@ RC111

Function	GPP_A20
APS	1
NO APS	0

APS_STRAP — APS@ RC108 — NOAPS@ RC109

Function	GPP_D11
W/O SECOND BATT	1
W/ SECOND BATT	0

S_BATT_STRAP — NOBATT2@ RC120 — BATT2@ RC119

Function	GPP_A23
CRT	1
NO CRT	0

ULTBY_STRAP — CRT@ RC114 — @ RC113

1215 update
next phase change net name

Function	GPP_A22
TYPEC_5448	1
NO TYPEC_5448	0

PD_STRAP — TYPEC@ RC116 — NONTYPEC@RC115

1215 update
next phase change net name

R3163 TCM@ 10K_0402_5% SD028100280

TPM_STRAP — NOTPM@ R3163 — TPM@ R3164

Function	PCH_[GPPA20,GPPA19]	
	TPM_STRAP2	TPM_STRAP
NOTPM	0	1
TCM	1	1
TPM	1	0

TPM_STRAP2 — TCM@ R3165 — NOTPM@ R3166

R3165 TPM@ 10K_0402_5% SD028100280

1103 add back

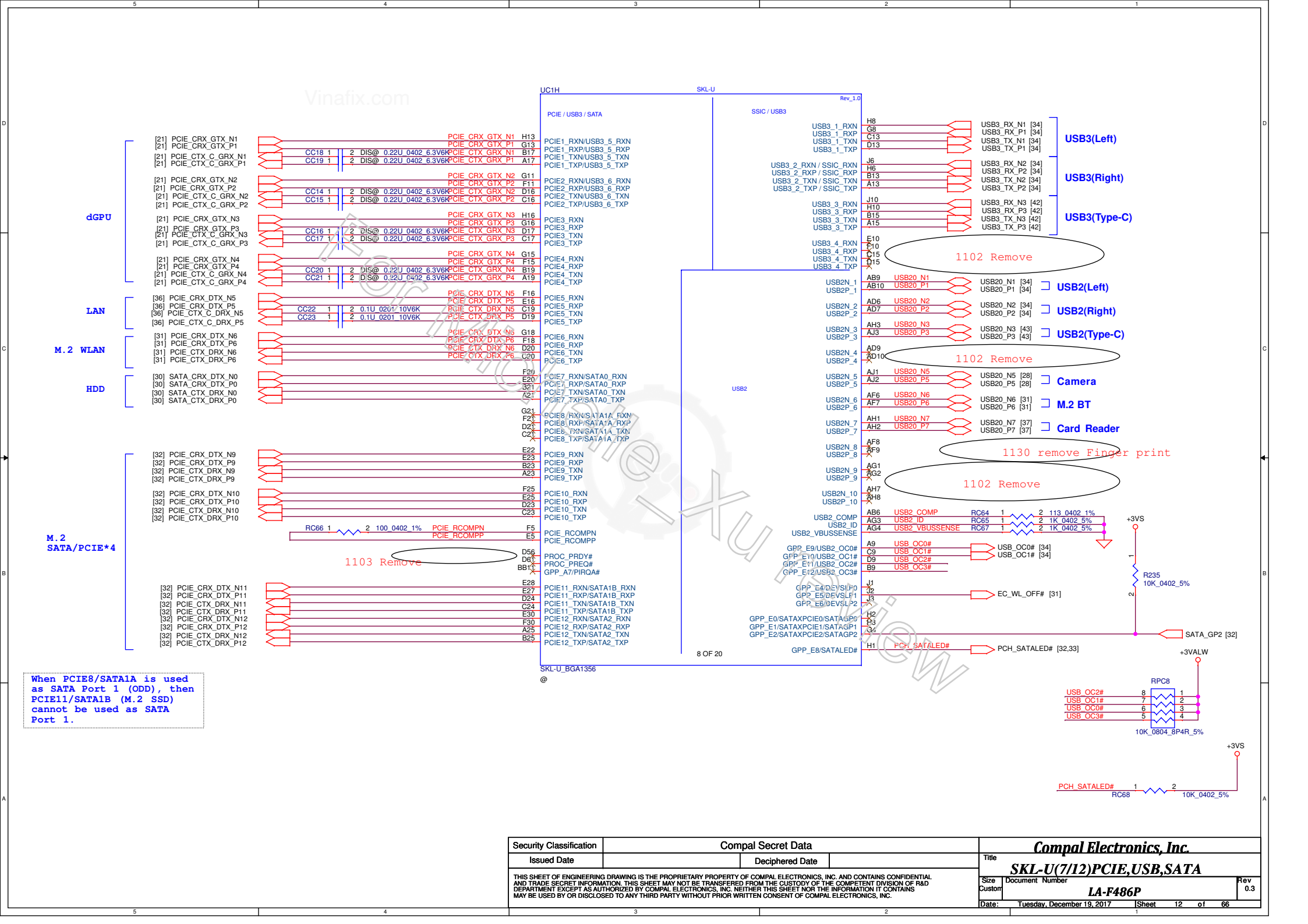
Security Classification	Compal Secret Data	
Issued Date		Deciphered Date

Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size: Custom | Document Number: LA-F486P | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 11 of 66



Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **SKL-U(7/12)PCIE,USB,SATA**

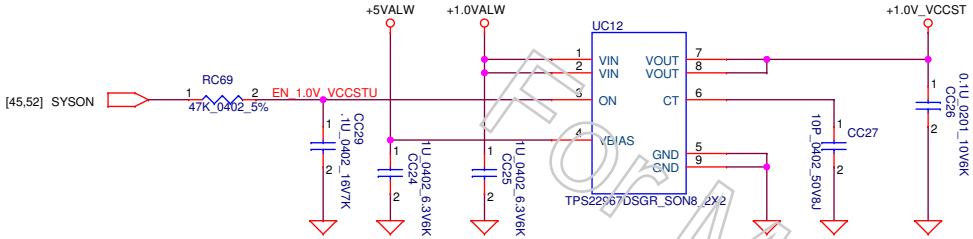
Size	Document Number	Rev
Custom	LA-F486P	0.3

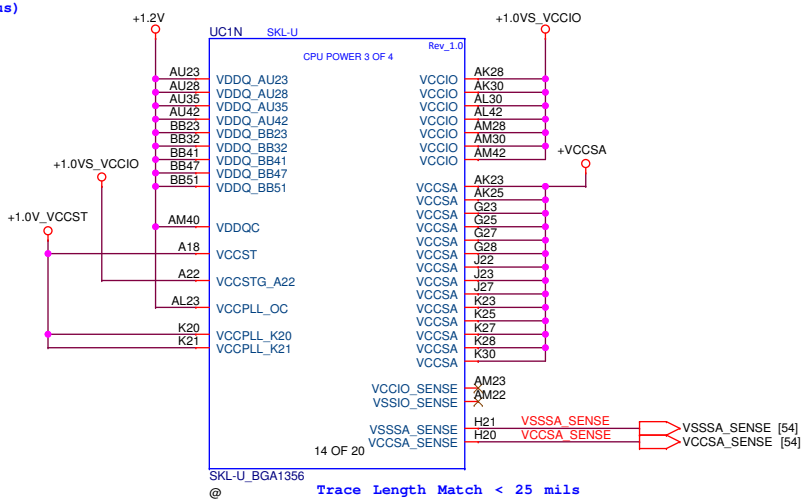
Date: Tuesday, December 19, 2017 | Sheet 12 of 66

Follow 543977_SKL_PDDG_Rev0_91
CC24 10PF ->22us(Spec:<= 65us)

+1.0VALW TO +1.0V_VCCST

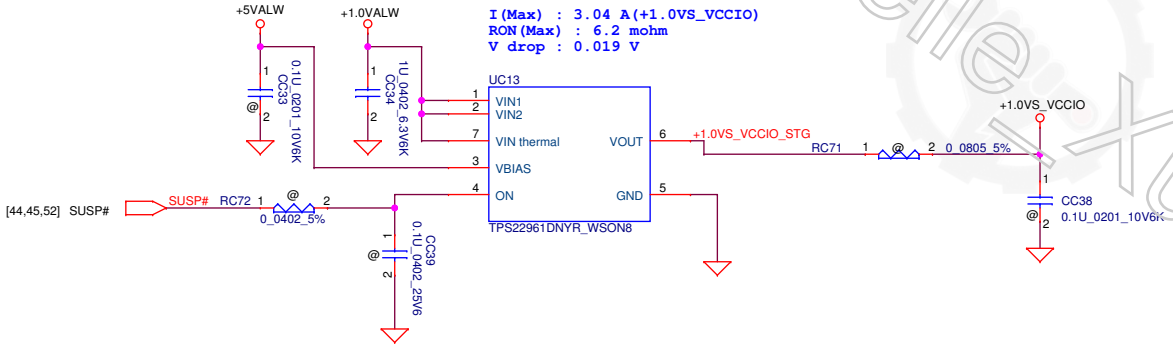
I(Max) : 0.16 A(+1.0V_VCCST)
RON(Max) : 25 mohm
V drop : 0.004 V

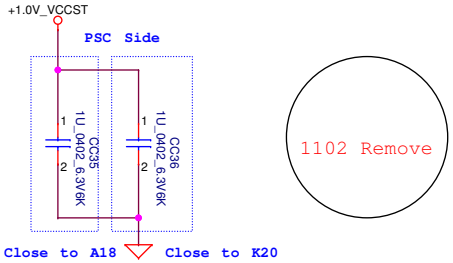




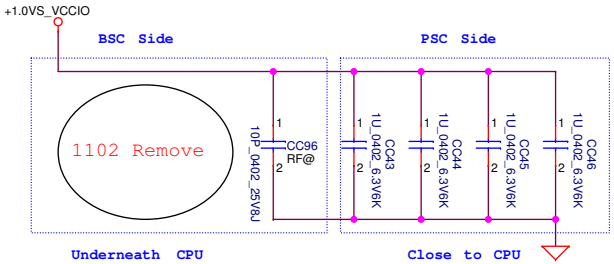
+1.0VALW TO +1.0VS_VCCIO

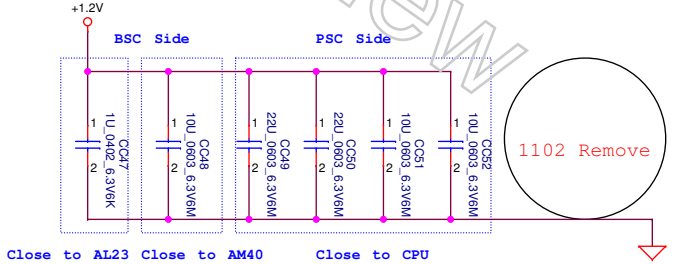
I(Max) : 3.04 A(+1.0VS_VCCIO)
RON(Max) : 6.2 mohm
V drop : 0.019 V





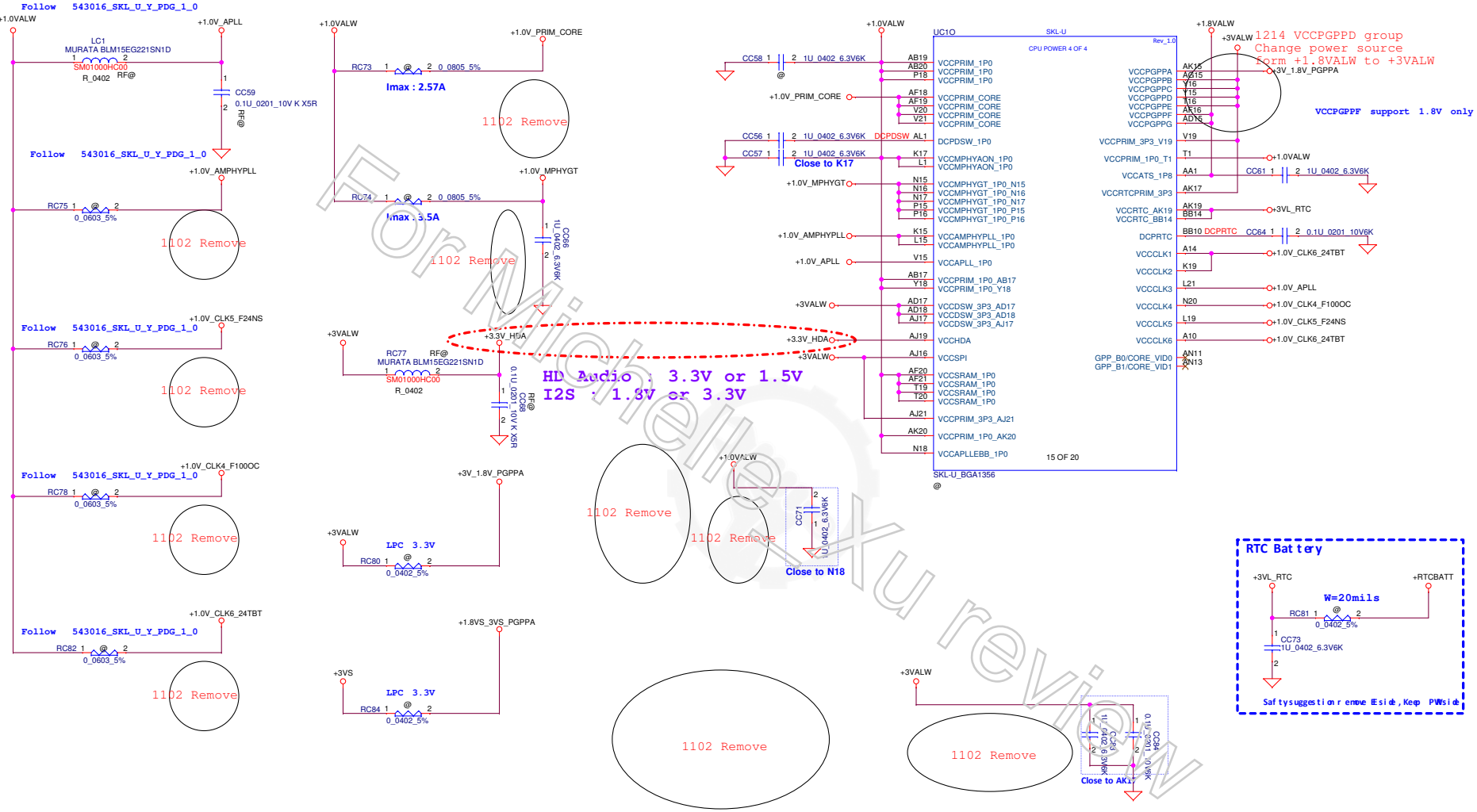
1102 Remove





Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.		
Title: SKL-U(8/12)Power		
Size: Custom	Document Number: LA-F486P	Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 13 of 66	



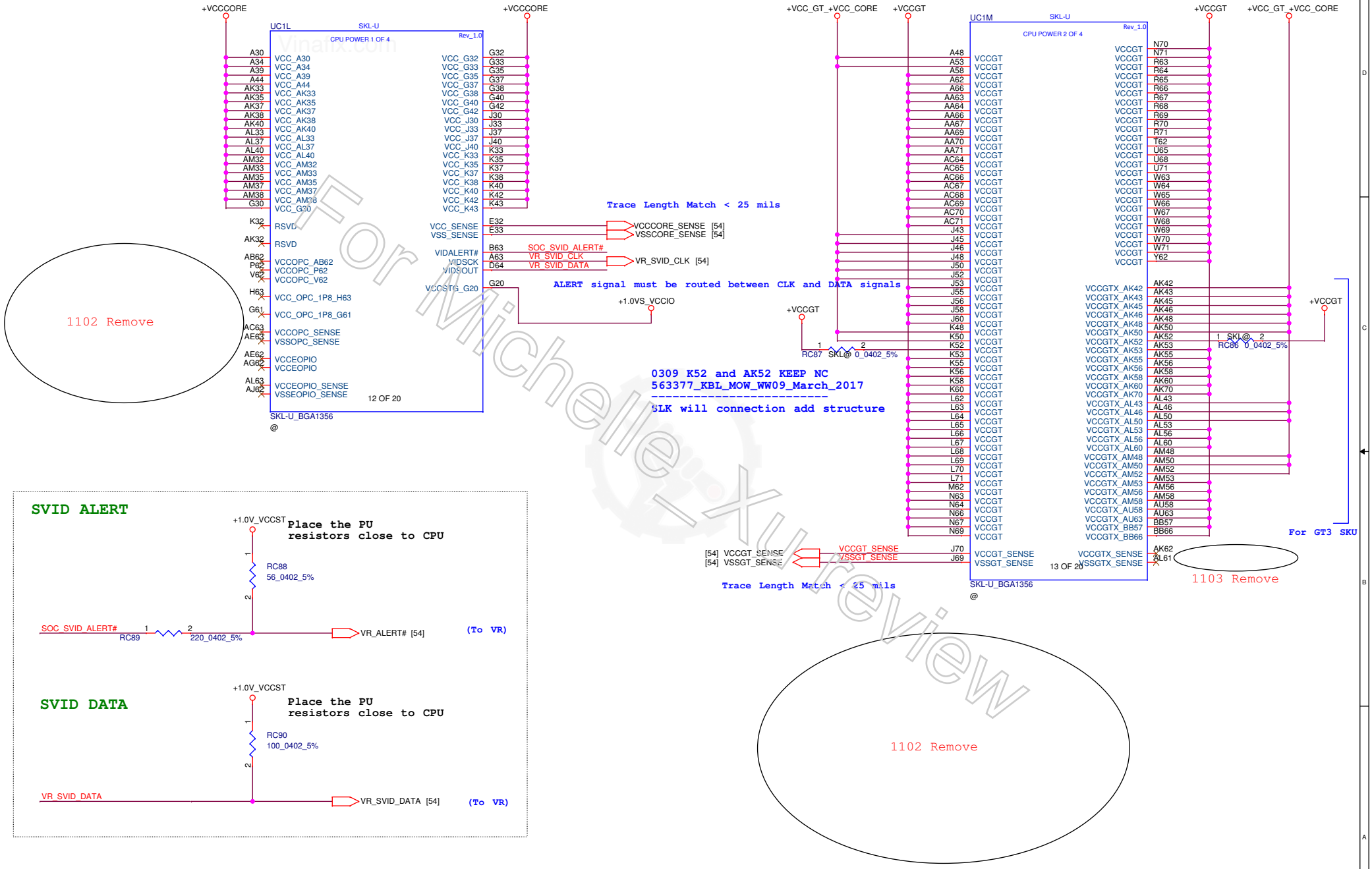
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: **SKL-U(9/12)Power**

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 | Sheet 14 of 66



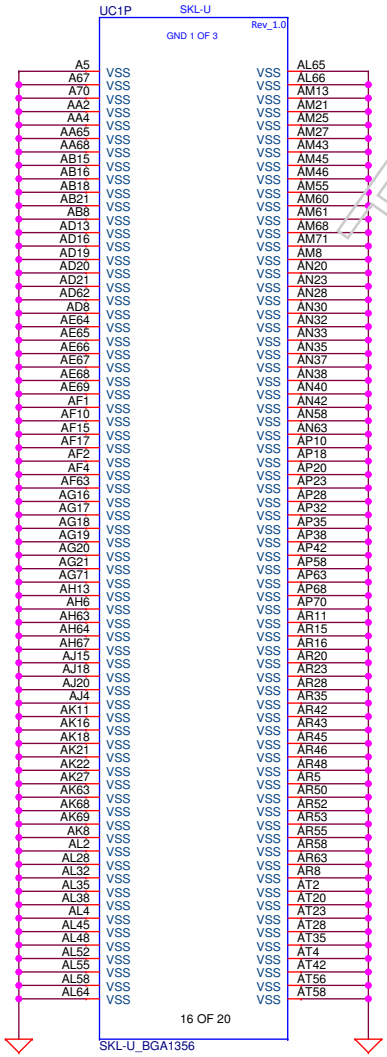
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

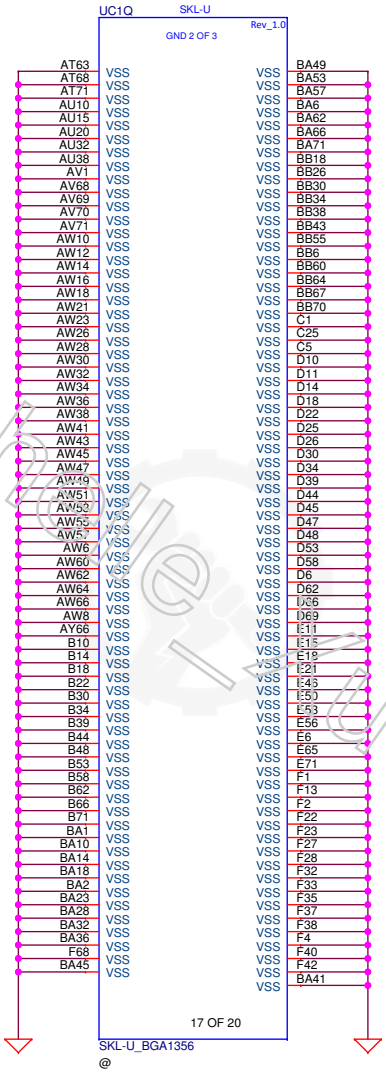
Compal Electronics, Inc.

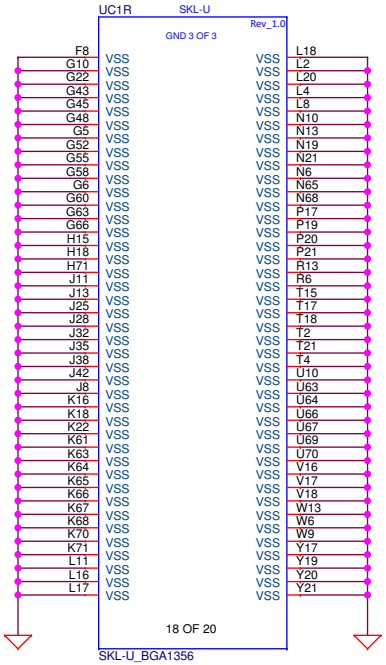
Title: **SKL-U(10/12)Power,SVID**

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 15 of 66

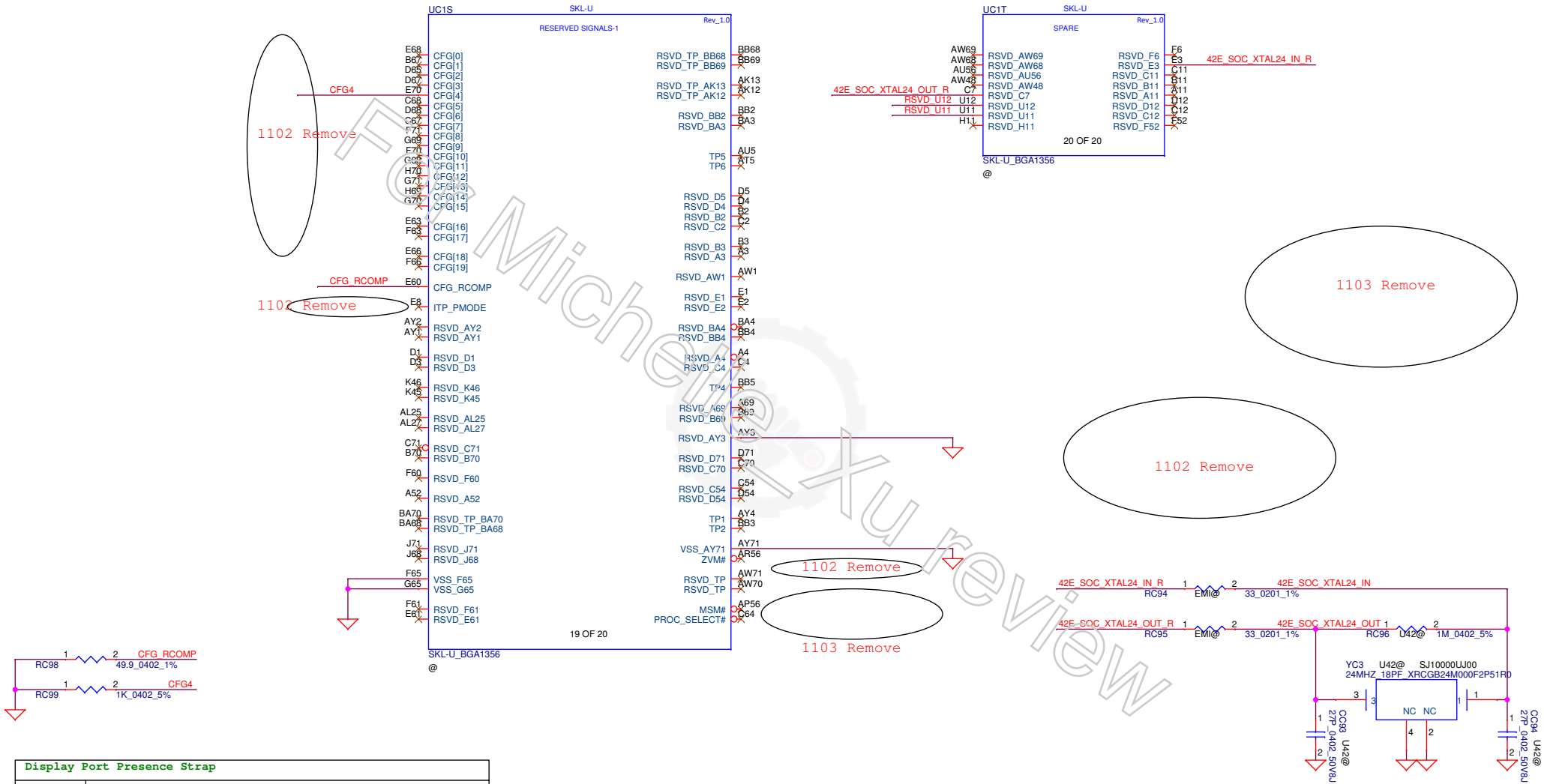






Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

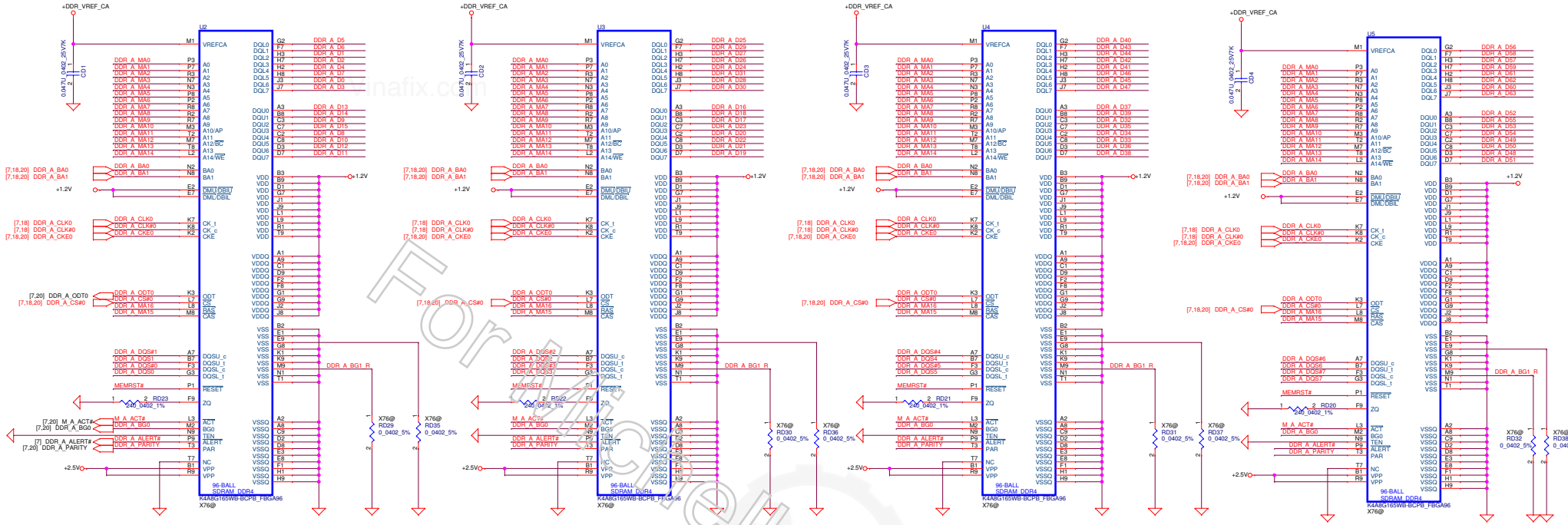
Compal Electronics, Inc.		
Title: SKL-U(11/12)GND		
Size: Custom	Document Number: LA-F486P	Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 16 of 66	



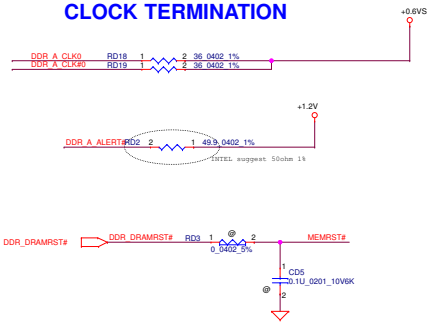
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.			
Title: SKL-U(12/12)CFG,RSVD			
Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 17 of 66		



CLOCK TERMINATION

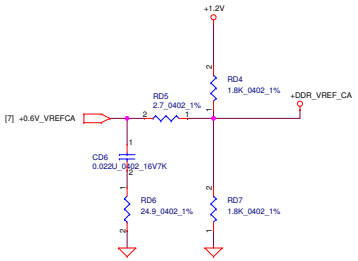


0606 add

TABLE

	SDP	DDP
RD29 RD30 RD31 RD32	ASM ASM ASM ASM	NA NA NA NA
RD33	NA	ASM
RD34	NA	ASM
RD35 RD36 RD37 RD38	0_5% 0_5% 0_5% 0_5%	243_1% 243_1% 243_1% 243_1%

LOGIC

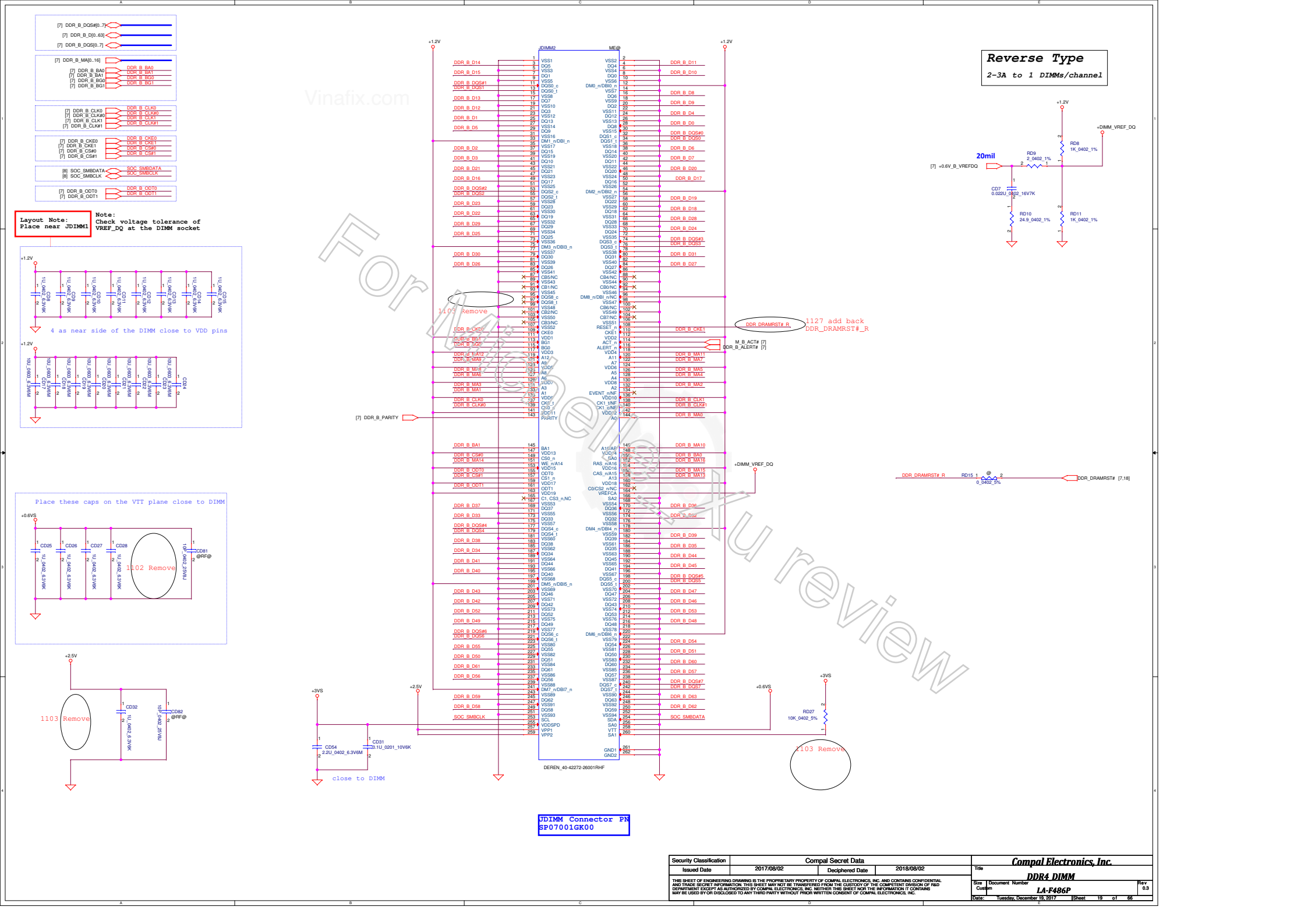


Data mapping

U2	DQ	U3	DQ	U4	DQ	U5	DQ
DQL0	D3	DQL0	D19	DQL0	D35	DQL0	D51
DQL1	D1	DQL1	D17	DQL1	D33	DQL1	D49
DQL2	D2	DQL2	D18	DQL2	D34	DQL2	D50
DQL3	D0	DQL3	D16	DQL3	D32	DQL3	D48
DQL4	D7	DQL4	D23	DQL4	D39	DQL4	D55
DQL5	D5	DQL5	D21	DQL5	D37	DQL5	D53
DQL6	D6	DQL6	D22	DQL6	D38	DQL6	D54
DQL7	D4	DQL7	D20	DQL7	D36	DQL7	D52
DQU0	D10	DQU0	D26	DQU0	D42	DQU0	D58
DQU1	D8	DQU1	D24	DQU1	D40	DQU1	D56
DQU2	D11	DQU2	D27	DQU2	D43	DQU2	D59
DQU3	D9	DQU3	D25	DQU3	D41	DQU3	D57
DQU4	D14	DQU4	D30	DQU4	D46	DQU4	D62
DQU5	D13	DQU5	D29	DQU5	D45	DQU5	D61
DQU6	D15	DQU6	D31	DQU6	D47	DQU6	D63
DQU7	D12	DQU7	D28	DQU7	D44	DQU7	D60

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.			
Title: DDR4 ON BOARD CHIPS			
Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 18 of 66		


Reverse Type
2-3A to 1 DIMMs/channel
Layout Note:
Place near JDIMM1
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket
4 as near side of the DIMM close to VDD pins
Place these caps on the VTT plane close to DIMM
1103 Remove
1102 Remove
1127 add back
DDR_DRAMRST#_R
20mil
close to DIMM
JDIMM Connector PN
SP07001GK00
DEREN_40-42272-26001RHF
For Wistron Xu review

[7,18] DDR_A_MA[0..16]

+1.2V

4 as near each on board RAM device as possible

+2.5V

2 as near each on board RAM device as possible

1102 Remove

+0.6VS

2 as near each on board RAM device as possible

+0.6VS

RP1 DDR_A_MA1 DDR_A_MA5 DDR_A_MA7 DDR_A_MA9 36_0804_8P4R_5%

RP2 DDR_A_MA13 DDR_A_MA8 DDR_A_PARITY DDR_A_MA11 [7,18] DDR_A_PARITY 36_0804_8P4R_5%

RP3 DDR_A_CKE0 DDR_A_MA16 DDR_A_ODT0 M_A_ACT# [7,18] DDR_A_CKE0 [7,18] DDR_A_ODT0 [7,18] M_A_ACT# 36_0804_8P4R_5%

DDR_A_MA2 RD28 36_0201_1%

[18] DDR_A_BG1_R RD34 X7@ 36_0201_1%

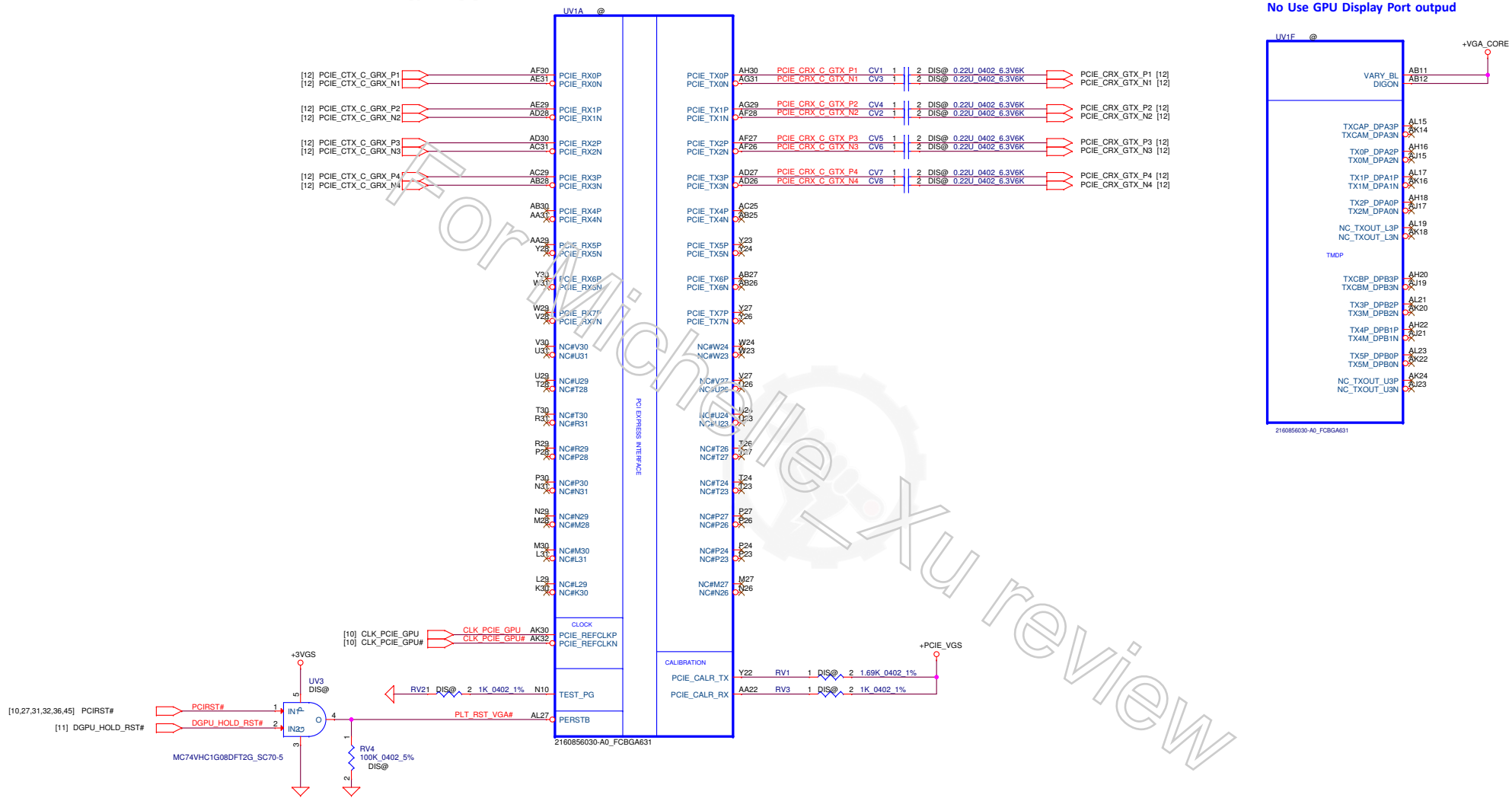
RP5 DDR_A_BG0 DDR_A_MA10 DDR_A_MA3 DDR_A_BA1 [7,18] DDR_A_BG0 [7,18] DDR_A_BA1 36_0804_8P4R_5%

RP6 DDR_A_MA14 DDR_A_CS#0 DDR_A_MA15 DDR_A_MA12 [7,18] DDR_A_CS#0 36_0804_8P4R_5%

RP7 DDR_A_MA4 DDR_A_BA0 DDR_A_MA0 DDR_A_MA6 [7,18] DDR_A_BA0 36_0804_8P4R_5%

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: DDR4 ON BOARD CHIPS

Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 20 of 66		



No Use GPU Display Port outpud

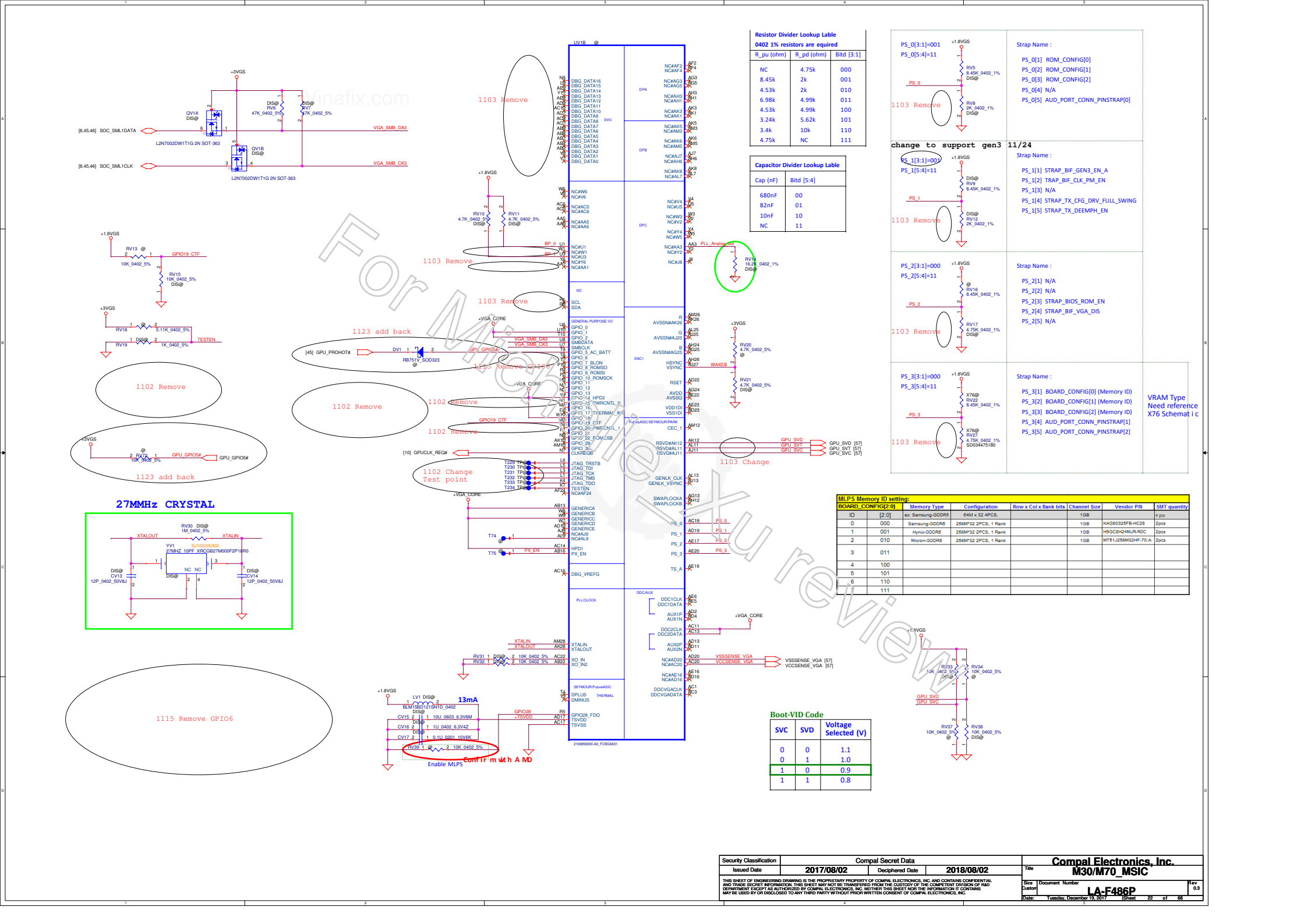
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: **M30/M70_PCIE/DP**

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 21 of 66



Resistor Divider Lookup Lable
0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

VRAM Type
Need reference X76 Schematic

MLPS Memory ID setting:

BOARD_CONFIG[2:0]		Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor P/N	SMT quantity
ID	[2:0]	ex: Samsung-GDDR5	64M x 32 4PCS,		1GB		4 pcs
0	000	Samsung-GDDR5	256M*32 2PCS, 1 Rank		1GB	K4G80325FB-HC28	2pcs
1	001	Hynix-GDDR5	256M*32 2PCS, 1 Rank		1GB	H5GC8H24MJR-R0C	2pcs
2	010	Micron-GDDR5	256M*32 2PCS, 1 Rank		1GB	MT51J256M32HF-70:A	2pcs
3	011						
4	100						
5	101						
6	110						
7	111						

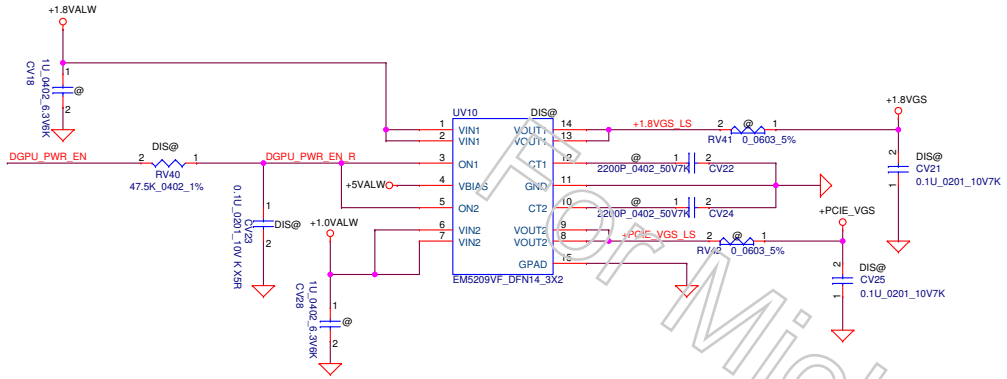
Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

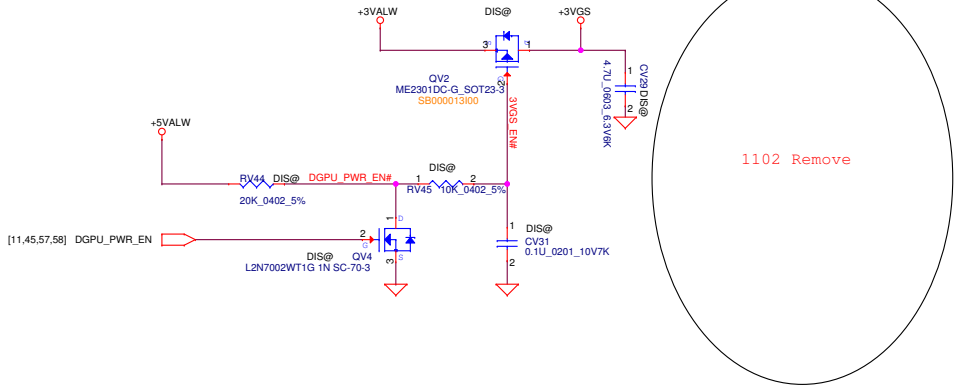
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

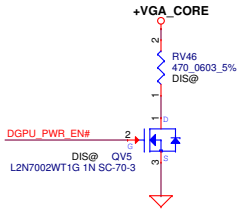
Compal Electronics, Inc.			
Title: M30/M70_MSIC			
Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 22 of 66		

+1.8VALW TO +1.8VGS
+1.0VALW TO +PCIE_VGS
Load switch

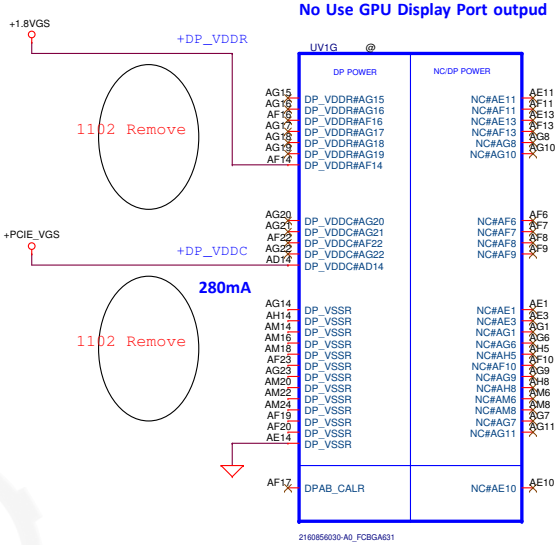


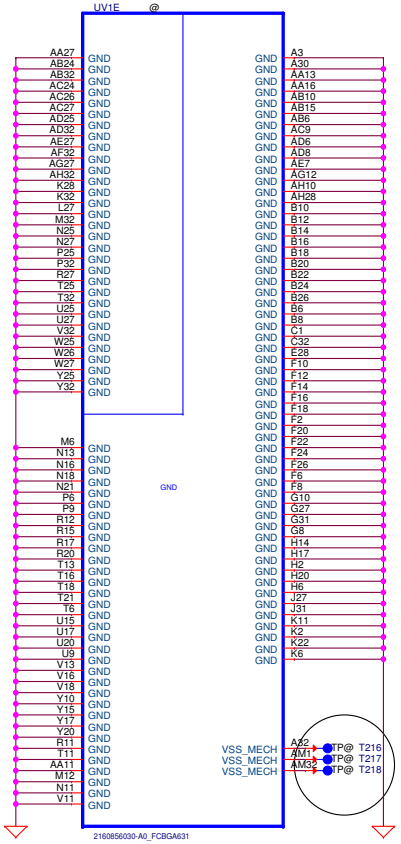
+3VALW to +3VGS





1102 Remove





1127 change back

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: **M30/M70_PWR**

Size: Custom | Document Number: **LA-F486P** | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 23 of 66

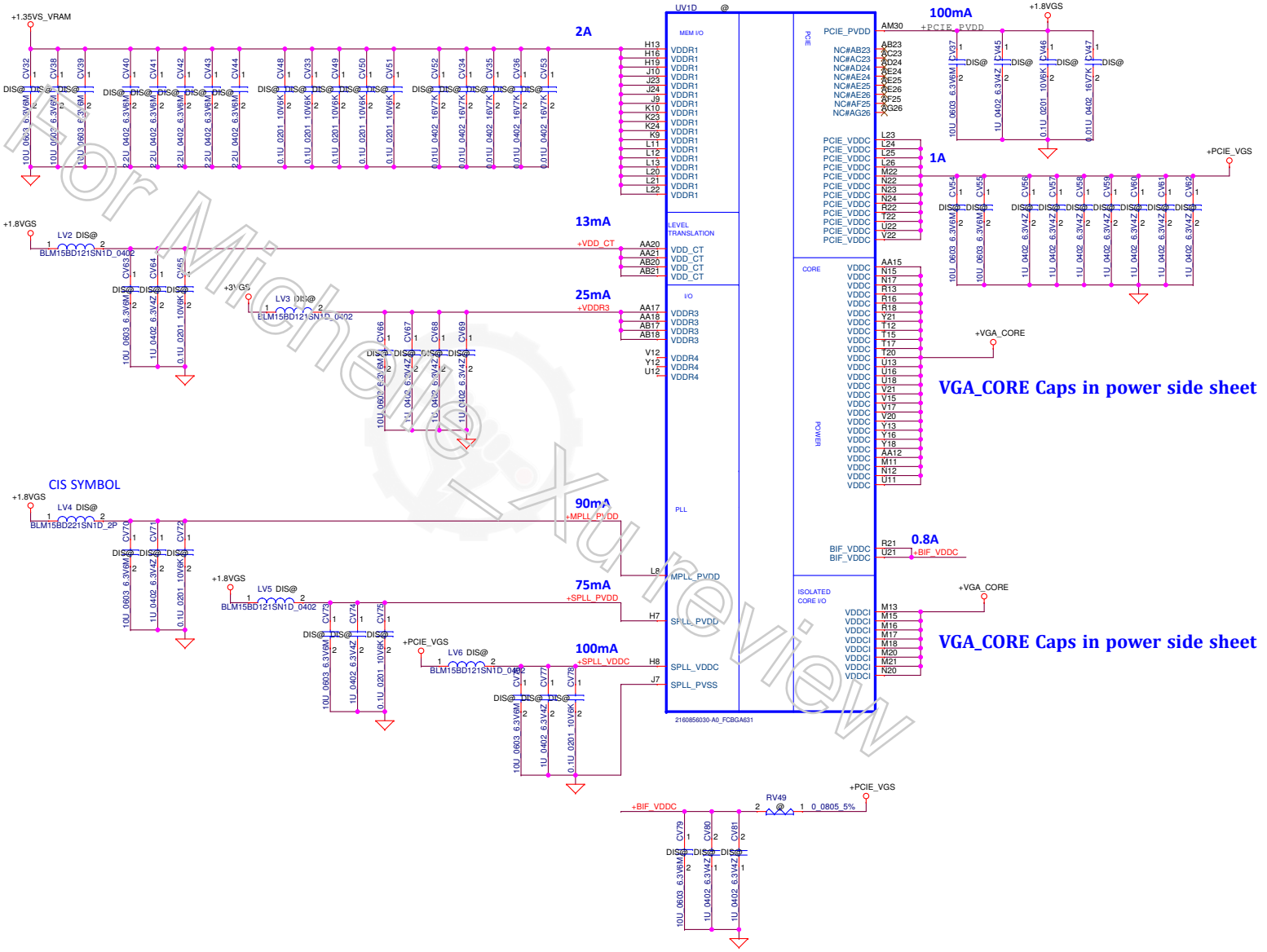
+VGA_CORE	10uF	1uF	0.1uF
VDDC VDDC and VDDCI TDC 28A	4	30	0
VDDCI	1	3	3

+PCIE_VGS		10uF	1uF	0.1uF
PCIE_VDDC	2A	2	7	0
BIF_VDDC	0.8A	1	2	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 2A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF	0.01uF
PCIE_PVDD	100mA	1	1	1	1
MPLL_PVDD	90mA	1	1	1	0
SPLL_PVDD	75mA	1	1	1	0
VDD_CT	13mA	1	1	1	0
+DP_VDDR	40mA	1(@)	1(@)	1(@)	0
+DP_VDDC		1(@)	1(@)	1(@)	0

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



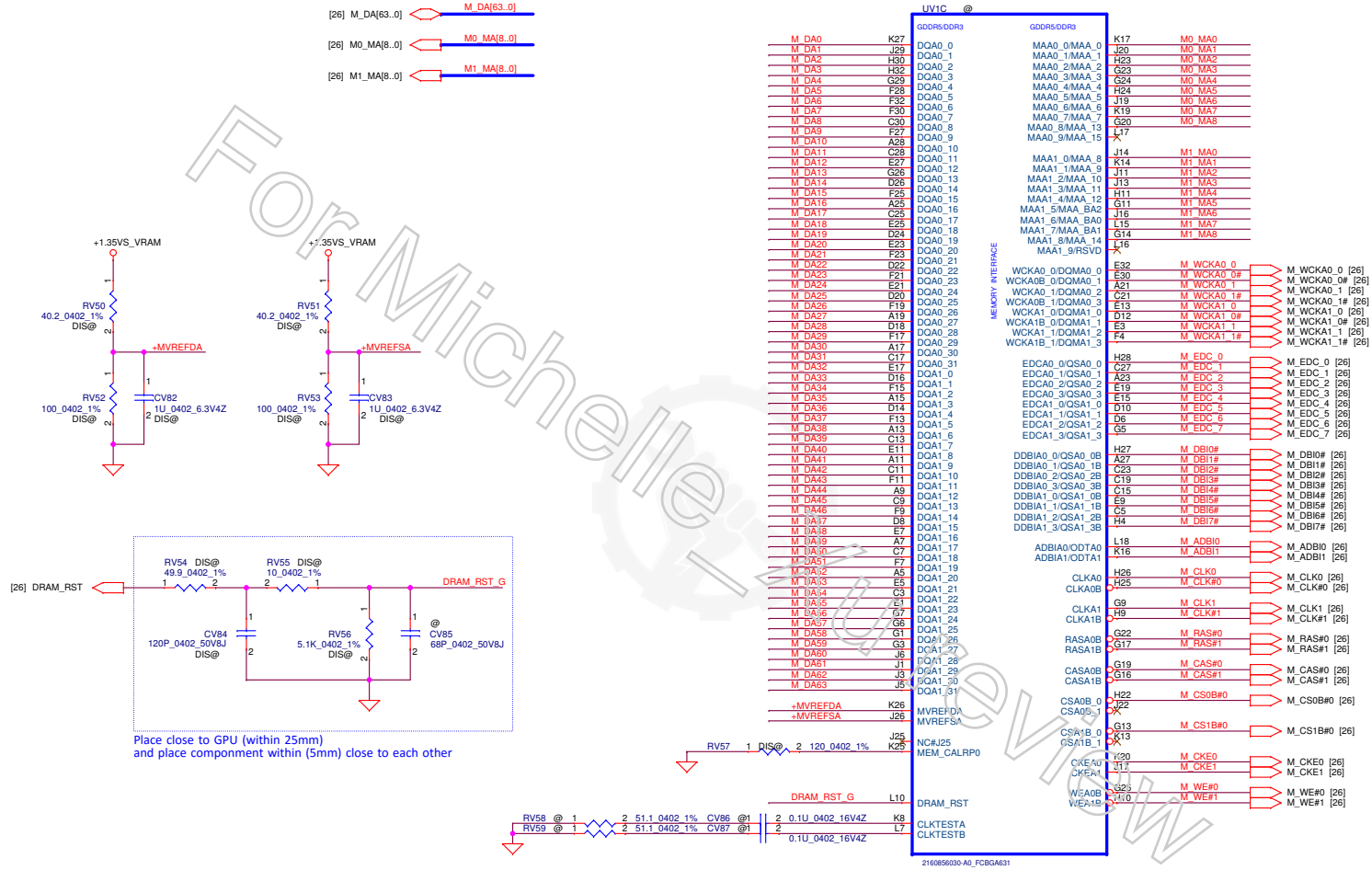
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: M30/M70_PWR

Size: Custom | Document Number: LA-F486P | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 24 of 66



Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

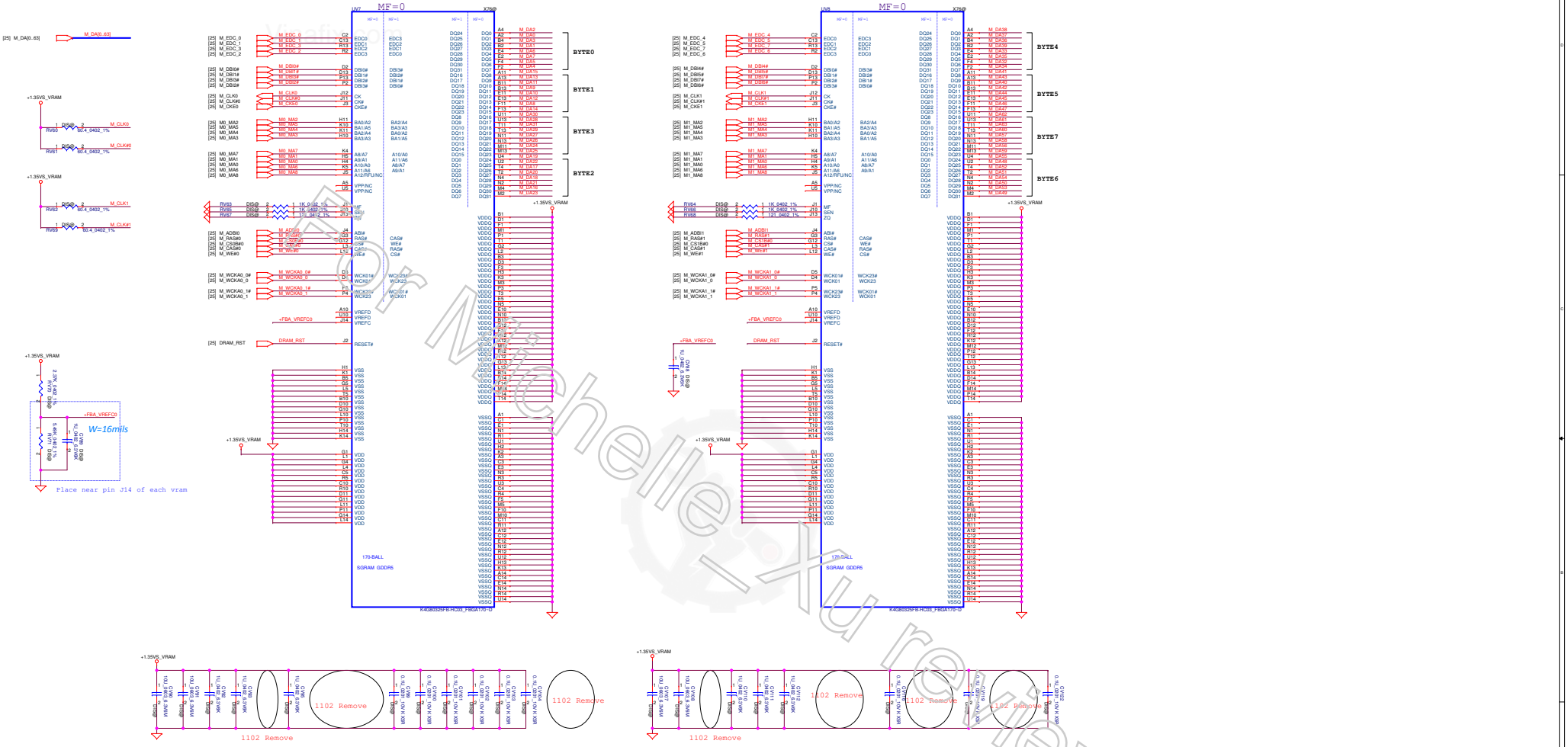
Compal Electronics, Inc.

Title: **M30/M70_MEM**

Size: Custom | Document Number: **LA-F486P** | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 25 of 66

Memory Partition A

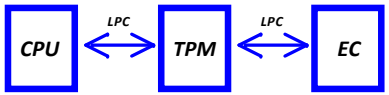


Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.			
Title	GDDR5_A0		
Size	Document Number		Rev
	LA-F486P		0.3
Date: Tuesday, December 19, 2017	Sheet 25 of 55		

TPM 2.0

Layout Routing

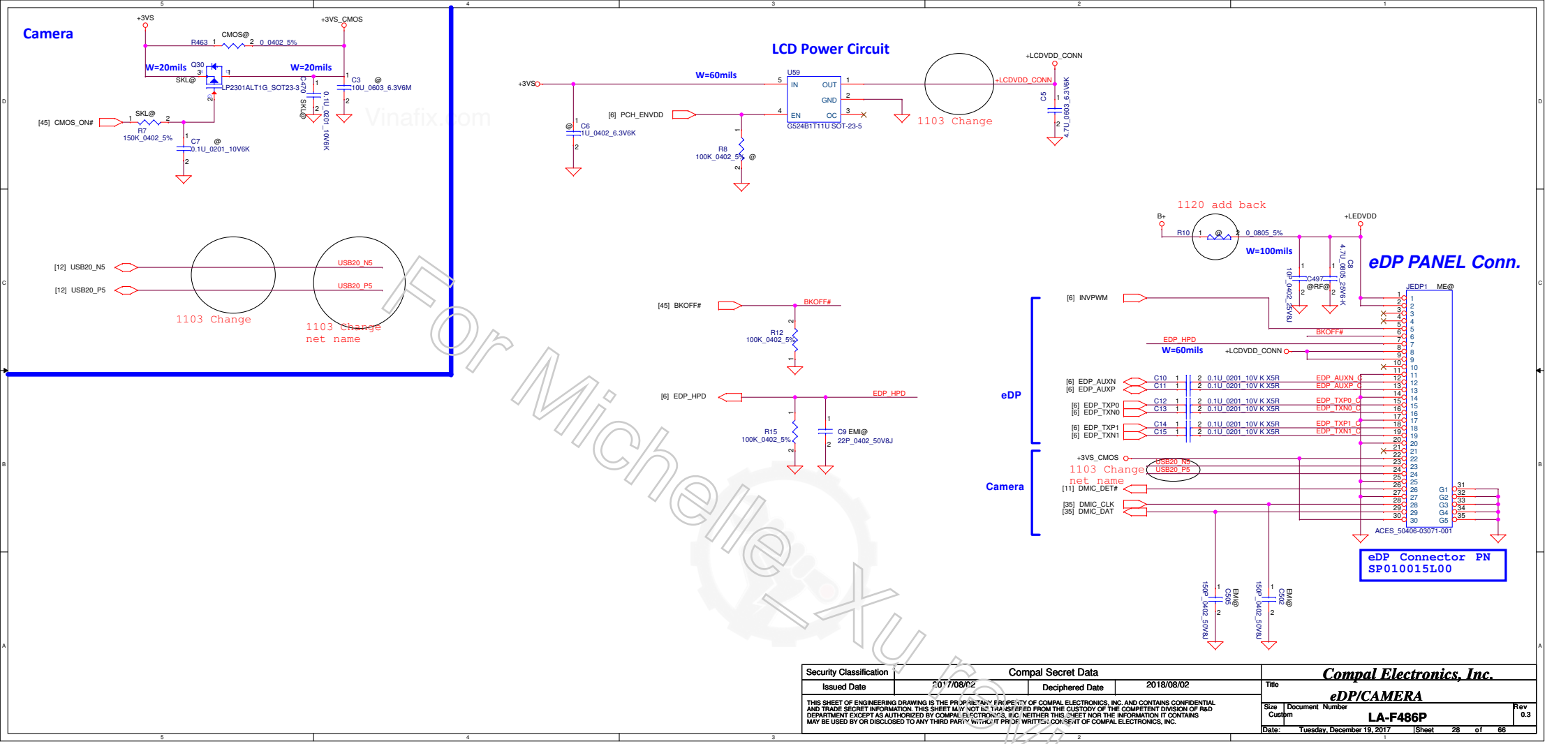


TPM/TCP Colay

	Nationz Infineon TCM	TPM		Nationz Infineon TCM	TPM
Pin1	NC	VDD	Pin17	NC	NC
Pin2	NC	GPIO	Pin18	LRESET#	LRESET#
Pin3	NC	NC	Pin19	LAD3	LAD3
Pin4	NC	NC	Pin20	VDD	VDD
Pin5	NC	NC	Pin21	LAD2	LAD2
Pin6	NC	NC	Pin22	LCLK	LCLK
Pin7	NC	NC	Pin23	LFRAME#	LFRAME#
Pin8	NC	NC	Pin24	LAD1	LAD1
Pin9	VDD	VDD	Pin25	VDD	VDD
Pin10	NC	VDD	Pin26	GND	GND
Pin11	GND	NC	Pin27	LAD0	LAD0
Pin12	NC	NC	Pin28	NC	SERIRQ
Pin13	NC	NC	Pin29	NC	NC
Pin14	NC	NC	Pin30	NC	NC
Pin15	NC	GND	Pin31	NC	PP
Pin16	GND	GND	Pin32	GND	GND

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.		
Title: TPM/TCM		
Size	Document Number: LA-F486P	Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 27 of 66	



Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.			
Title	eDP/CAMERA		
Size Custom	Document Number LA-F486P		Rev 0.3
Date: Tuesday, December 19, 2017	Sheet 28 of 66		

EMI

Near JHDMI1

Base on EMI HDMI test

Near JHDMI1

[6] HDMI_CLK-_CK — C17 1 2 0.1U_0201_10V6K — HDMI_CLK-_CK_C
[6] HDMI_CLK+_CK — C20 1 2 0.1U_0201_10V6K — HDMI_CLK+_CK_C
[6] HDMI_TX0-_CK — C21 1 2 0.1U_0201_10V6K — HDMI_TX0-_CK_C
[6] HDMI_TX0+_CK — C22 1 2 0.1U_0201_10V6K — HDMI_TX0+_CK_C
[6] HDMI_TX1-_CK — C23 1 2 0.1U_0201_10V6K — HDMI_TX1-_CK_C
[6] HDMI_TX1+_CK — C24 1 2 0.1U_0201_10V6K — HDMI_TX1+_CK_C
[6] HDMI_TX2-_CK — C25 1 2 0.1U_0201_10V6K — HDMI_TX2-_CK_C
[6] HDMI_TX2+_CK — C26 1 2 0.1U_0201_10V6K — HDMI_TX2+_CK_C

EMI@ R16 1 2 1 0402 5% — HDMI_CLK-_CONN
EMI@ R18 1 2 1 0402 5% — HDMI_CLK+_CONN
R17 @EMI@ 150_0402_5%

EMI@ R19 1 2 1 0402 5% — HDMI_TX0-_CONN
EMI@ R21 1 2 1 0402 5% — HDMI_TX0+_CONN
R20 @EMI@ 150_0402_5%

EMI@ R22 1 2 1 0402 5% — HDMI_TX1-_CONN
EMI@ R25 1 2 1 0402 5% — HDMI_TX1+_CONN
R24 @EMI@ 150_0402_5%

EMI@ R27 1 2 1 0402 5% — HDMI_TX2-_CONN
EMI@ R29 1 2 1 0402 5% — HDMI_TX2+_CONN
R28 @EMI@ 150_0402_5%

For HDMI

U9 G5250Q1T73U SOT-23
+5VS — @ C19 0.1U_0201_10V6K — IN
OUT — W=40mils — +5V_DSP
GND — C18 0.1U_0201_10V6K

+3VS — R23 1M_0402_5% — Q2 2N7002K_SOT23-3
[6] TMDS_B_HPD — R26 20K_0402_5%

HDMI_DET
HDMIDAT_R
HDMICLK_R
HDMI_CLK-_CONN
HDMI_CLK+_CONN
HDMI_TX0-_CONN
HDMI_TX0+_CONN
HDMI_TX1-_CONN
HDMI_TX1+_CONN
HDMI_TX2-_CONN
HDMI_TX2+_CONN

JHDMI1 ME@
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK- CK_shield CK+
D0- D0_shield D0+
D1- D1_shield D1+
D2- D2_shield D2+
GND GND GND GND
ACON_HMRA3-AK120C

HDMI Connector PN DC232003A00

ZZZ15 45@
HDMI Logo
RO0000003HM

+3VS — R30 1 2 2.2K_0402_5% — HDMIDAT_NB
R31 1 2 2.2K_0402_5% — HDMICLK_NB

HDMIDAT_NB(Internal Pull Down):
Display Port C Detected
0 = Port C is not detected.
1 = Port C is detected.

+3VS — Q3A L2N7002DW1T1G 2N SC88-6
[6] HDMICLK_NB — HDMICLK_R
[6] HDMIDAT_NB — HDMIDAT_R
Q3B L2N7002DW1T1G 2N SC88-6

+5V_DSP — R32 1 2 2.2K_0402_5% — HDMIDAT_R
R33 1 2 2.2K_0402_5% — HDMICLK_R

HDMI_TX1-_CK_C
HDMI_TX1+_CK_C
HDMI_TX2-_CK_C
HDMI_TX2+_CK_C
RP8 470 +-5% 8P4R

HDMI_CLK-_CK_C
HDMI_CLK+_CK_C
HDMI_TX0-_CK_C
HDMI_TX0+_CK_C
RP9 470 +-5% 8P4R

+3VS — Q4 2N7002K_SOT23-3

ESD

D1 @ESD@
HDMIDAT_R — HDMIDAT_R
HDMICLK_R — HDMICLK_R
HDMI_DET — HDMI_DET
L05ESDL5V0NA-4_SLP2510P8-10-9
SC300003Z00

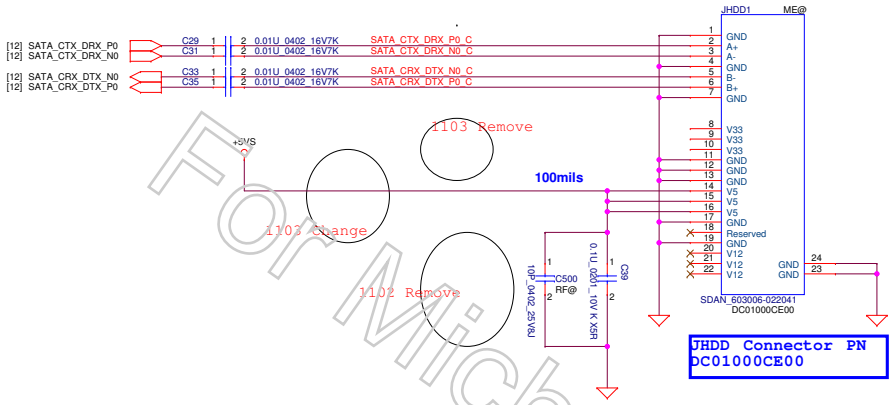
D2 @ESD@
HDMI_CLK-_CONN — HDMI_CLK-_CONN
HDMI_CLK+_CONN — HDMI_CLK+_CONN
HDMI_TX0-_CONN — HDMI_TX0-_CONN
HDMI_TX0+_CONN — HDMI_TX0+_CONN
L05ESDL5V0NA-4_SLP2510P8-10-9
SC300003Z00

D3 @ESD@
HDMI_TX1-_CONN — HDMI_TX1-_CONN
HDMI_TX1+_CONN — HDMI_TX1+_CONN
HDMI_TX2-_CONN — HDMI_TX2-_CONN
HDMI_TX2+_CONN — HDMI_TX2+_CONN
L05ESDL5V0NA-4_SLP2510P8-10-9
SC300003Z00

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/02	Deciphered Date	2018/08/02
Title	HDMI CONN		
Size C	Document Number LA-F486P		Rev 0.3
Date: Tuesday, December 19, 2017	Sheet 29 of 66		

HDD

SATA HDD Conn.



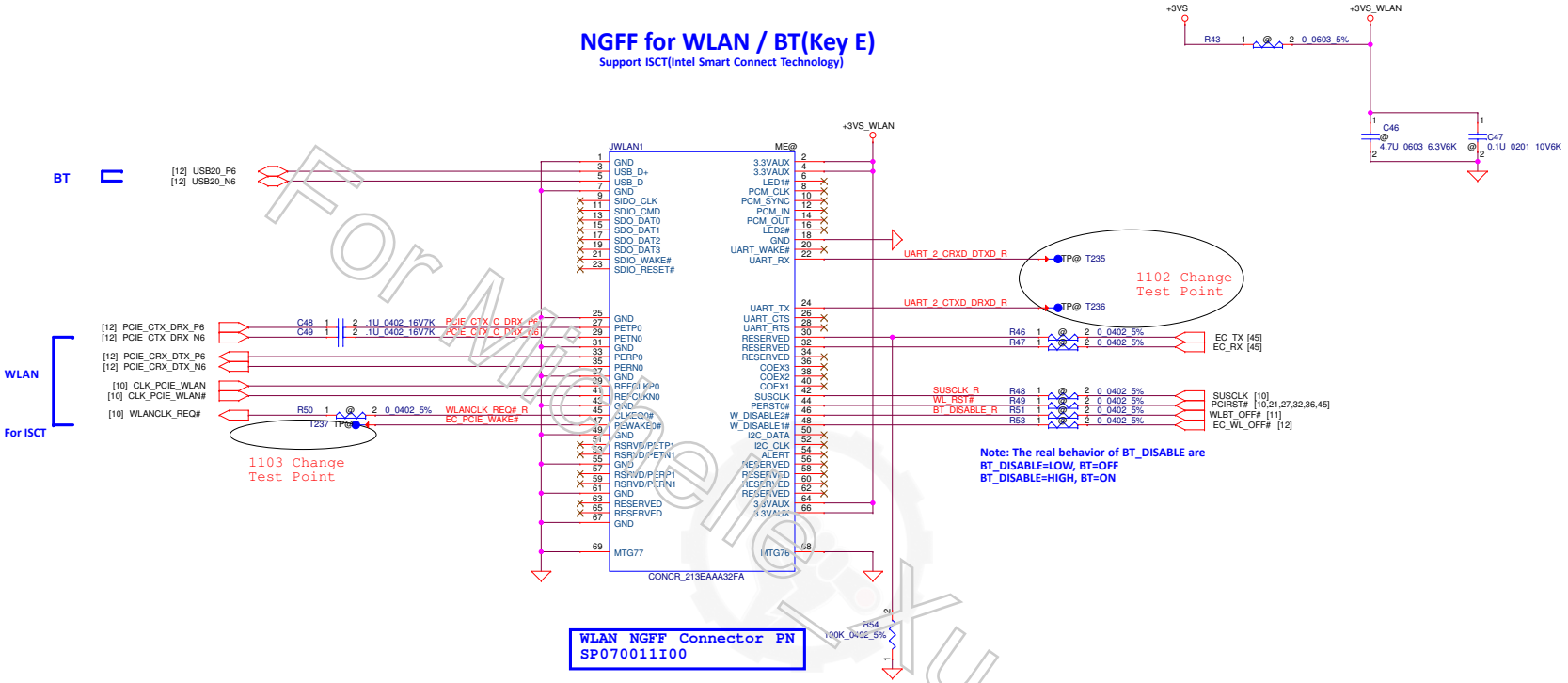
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: **HDD Connector**

Size	Document Number	Rev
C	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 30 of 66



6.2. NGFF Module Pin outs

The following section incorporates a series of NGFF module side pin outs covering the different Slots. Because some signals have directionality associated with them, their names and locations may be different between the Platform side and the Module side.

Please note the main differences between Platform side pin outs and Module side pin outs as seen in the diagram below:

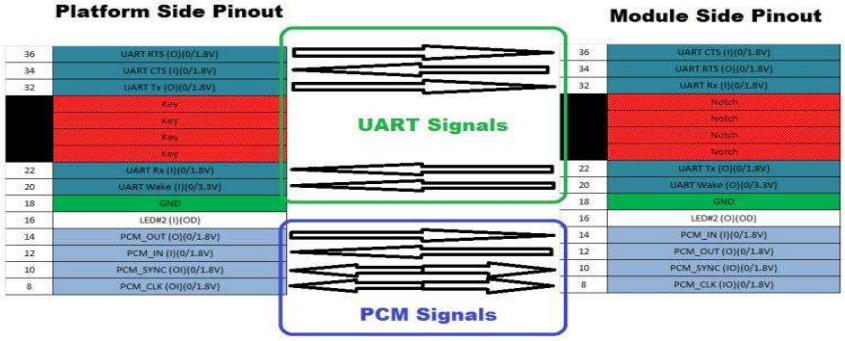
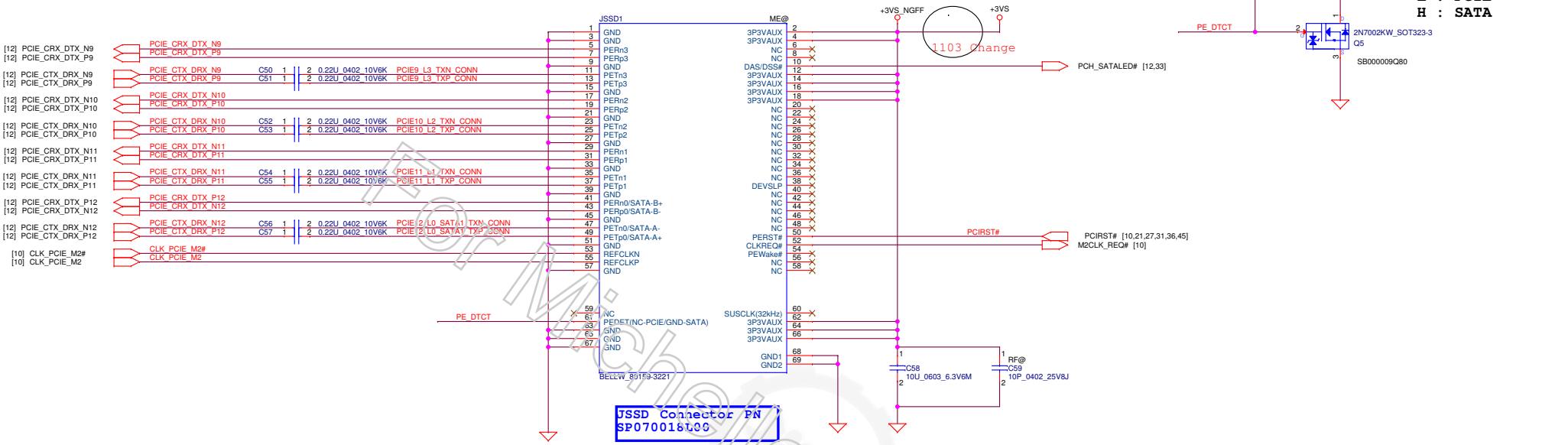


Figure 6-1: UART & PCM Signal Direction & Signal Name Changes

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.			
Title	Mini-Card/NEW Card		
Size	Document Number	LA-F486P	Rev 0.3
Date: Tuesday, December 19, 2017	Sheet 31 of 66		

M.2 mSATA Conn



Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

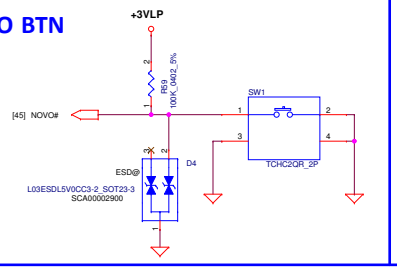
Compal Electronics, Inc.

Title: **M.2 SSD**

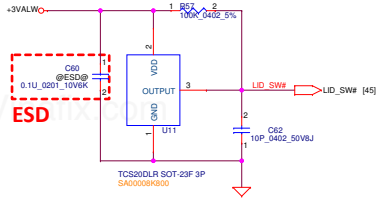
Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 32 of 66

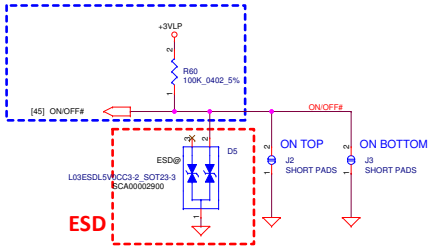
NOVO BTN



LID

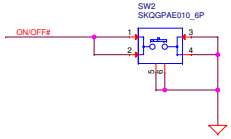


Power BTN



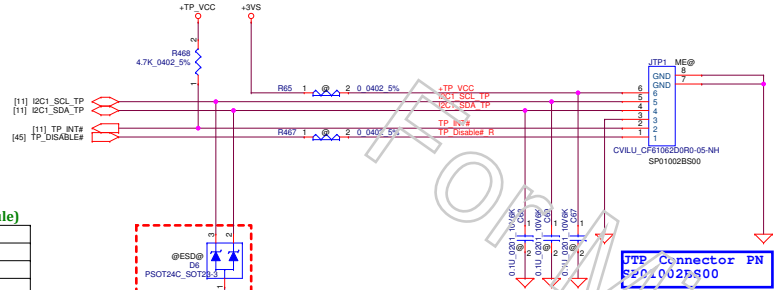
Power BTN

SN100004Y00



1130 remove

ClickPad

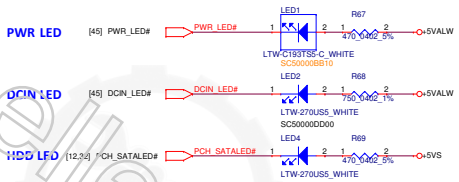


Click Pad Pin define(Module)

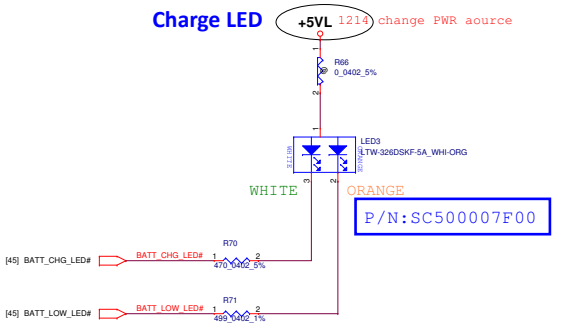
Pin1	VDD_3.3V
Pin2	SCL
Pin3	SDA
Pin4	GND
Pin5	INT
Pin6	LID CLOSE

JTP Connector PN SP01002SS00

LED



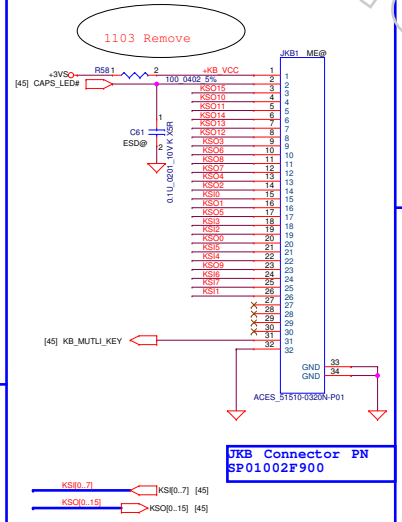
Charge LED



1130 remove Finger print

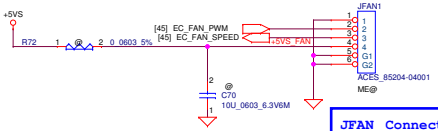
KB

1103 Remove



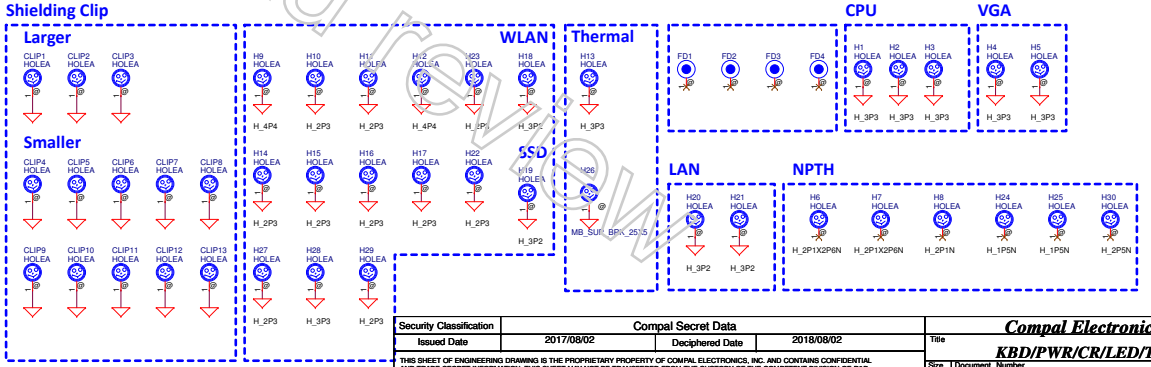
JKB Connector PN SP01002F900

FAN Conn



JFAN Connector PN SP02000CW00

Shielding Clip



Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: KBD/PWR/CR/LED/TP Conn.

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 33 of 66

USB 3.0 (Lef t)

1102 Remove

W=80mils +5VALW

W=80mils +5V_CHGUSB

NONAOU@ C71 0.1U_0201_10V K XSR

U55_NONAOU@ OUT IN GND OCB E57

[45] USB_EN#

SY6288D20AAC_SOT23-5

R73 0_0402_5%

USB_OC0# [12]

1102 Remove

1102 Remove

USB3.0_Port

+5V_CHGUSB

JUSB1 ME@ VBUS D- D+ GND SSRX- SSRX+ GND SSTX- SSTX+ GND

[12] USB3_RX_N1 [12] USB3_RX_P1 [12] USB3_TX_N1 [12] USB3_TX_P1

C75 0.1U_0201_10V K XSR C74 0.1U_0201_10V K XSR

USB3_RX_N1 USB3_RX_P1 USB3_TX_N1_C USB3_TX_P1_C

USB20_N1_C USB20_P1_L

ACON_TARAC-3UTU91

+5V_CHGUSB

C498 RF@

C246 470P_0402_50V7K

USB3.0 Connector PN DC23300AGB0

ESD

D43 ESD@

USB3_RX_N1 USB3_RX_P1 USB3_TX_N1_C USB3_TX_P1_C

L3SE5DL5V0NA-4_SLP2510P8-10-9

SC300005Z00

D8 ESD@

+5V_CHGUSB

USB20_N1_L USB20_P1_L

L3SE3DL5V0DK4_SOT23-6

SC300004W00

[12] USB20_P1 [12] USB20_N1

L13 EMI@

USB20_P1_L USB20_N1_L

EXC24CG900U_4P

1103 remove Net Name add inter sheet

USB 3.0 (Right)

W=80mils +5VALW

W=80mils +5V_USB

U56 OUT IN GND OCB E57

USB_EN#

SY6288D20AAC_SOT23-5

R228 0_0402_5%

USB_OC1# [12]

C248 0.1U_0201_10V K XSR

+5V_USB

1103 Remove

1103 Change

1103 Remove

1103 Change

1103 Remove

[12] USB3_RX_N2 [12] USB3_RX_P2 [12] USB3_TX_N2 [12] USB3_TX_P2

USB3_RX_N2 USB3_RX_P2 USB3_TX_N2_C USB3_TX_P2_C

C481 0.1U_0201_10V K XSR C480 0.1U_0201_10V K XSR

C499 RF@ C471 470P_0402_50V7K

JUSB2 ME@ VBUS D- D+ GND SSRX- SSRX+ GND SSTX- SSTX+ GND

ACON_TARAC-3UTU91

1103 Change net name

USB3.0 Connector PN DC23300AGB0

[12] USB20_N2 [12] USB20_P2

L11 EMI@

USB20_N2_L USB20_P2_L

EXC24CG900U_4P

ESD

D39 ESD@

USB3_RX_N2 USB3_RX_P2 USB3_TX_N2_C USB3_TX_P2_C

L0SE5DL5V0NA-4_SLP2510P8-10-9

SC300003Z00

D38 ESD@

+5V_USB

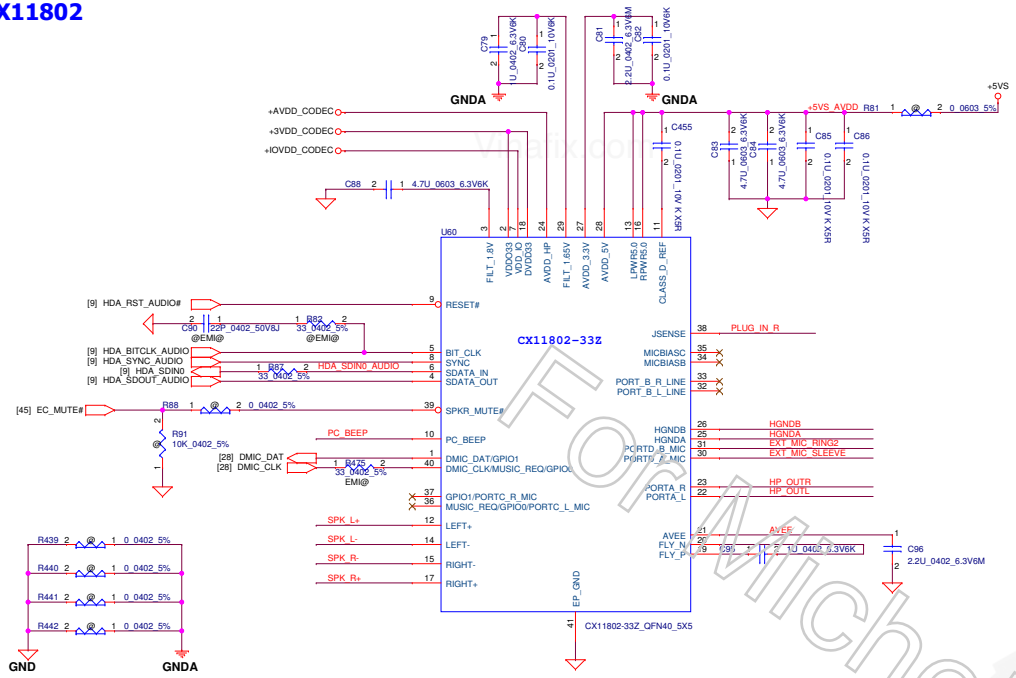
USB20_N2_L USB20_P2_L

L3SE3DL5V0DK4_SOT23-6

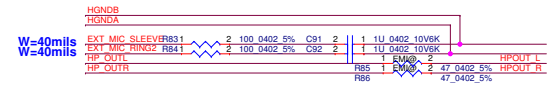
SC300004W00

Title	<Title>		
Size	Document Number		Rev
Custom	LA-F486P		<RevCode>
Date:	Tuesday, December 19, 2017	Sheet 34 of 66	

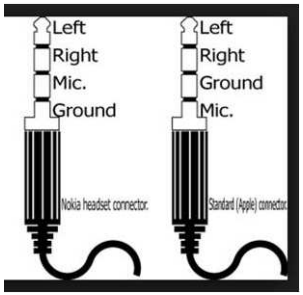
CX11802

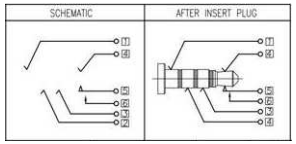


Combo Jack



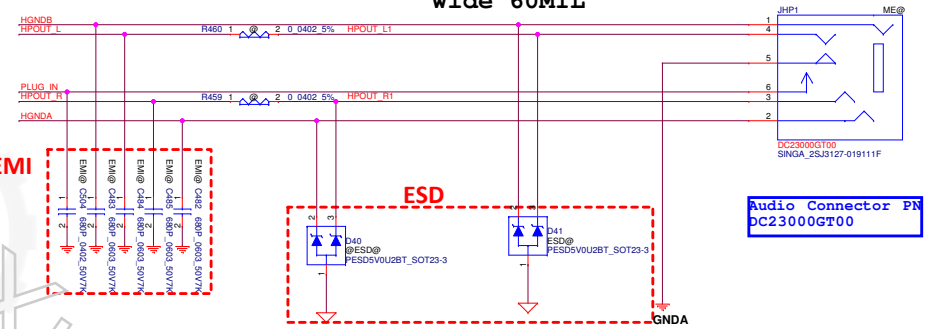
place close audio codec





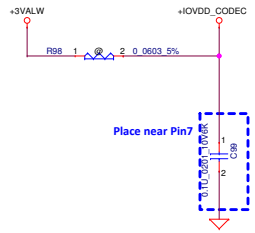
wide 60MIL

Combo Jack (Normal Open)



Audio Connector PN
DC23000GT00

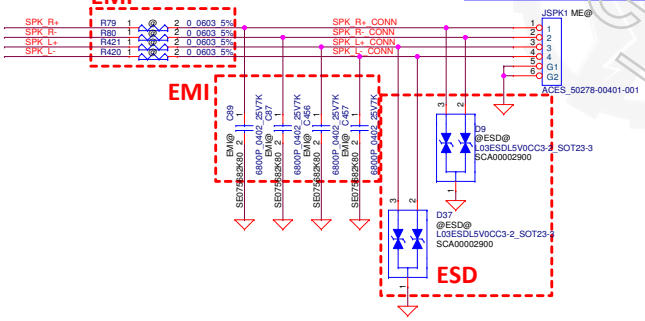
+3VS → +IOVDD_CODEC



Speaker

wide 40MIL

Speaker Connector PN
SP02000RR00

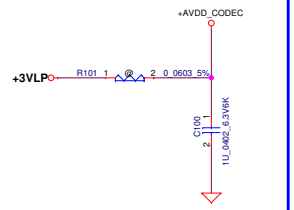


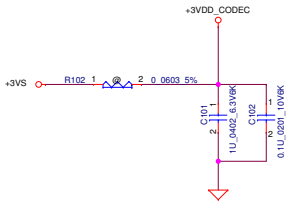
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V		V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

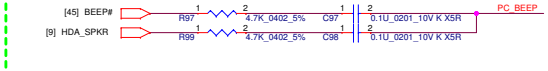
Each Platform HDA Link Voltage Support (Pin 7):

	3.3V	1.5V/1.8V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V



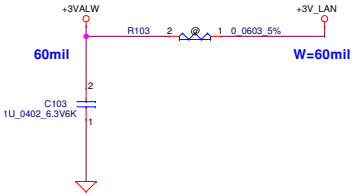


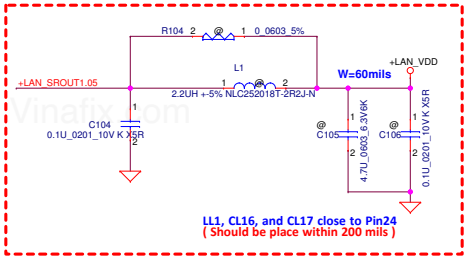
PC Beep



Security Classification	Compal Secret Data		
Issued Date	2014/09/01	Deciphered Date	2015/09/01

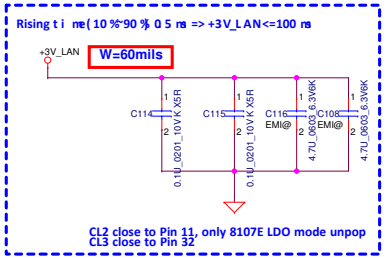
Compal Electronics, Inc.	
Title	HD Audio Codec_ALC3240
Size / Document Number / Rev	Custom / LA-F486P / 0.1
Date: Tuesday, December 19, 2017	Sheet 35 of 66

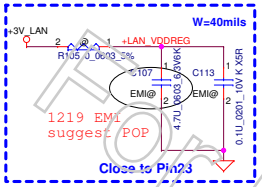


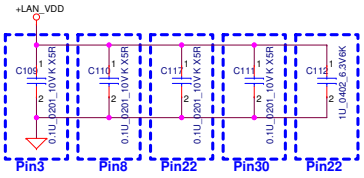


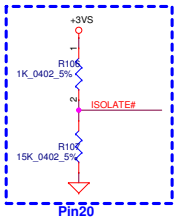
	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O

Please refer to the table above when using different 1.0V supply source.

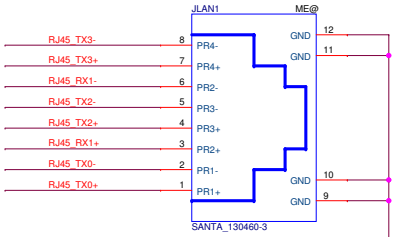




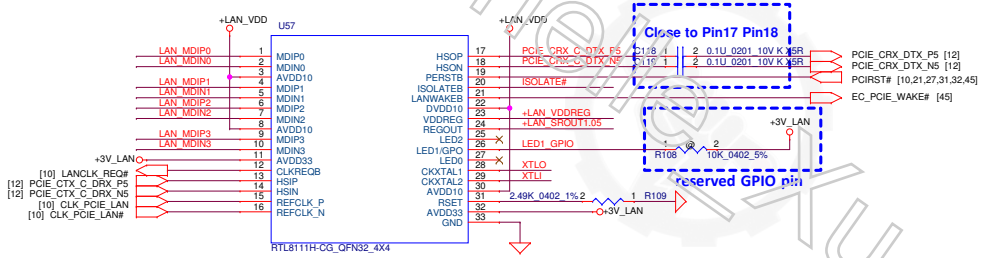


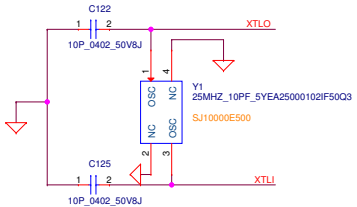


RJ-45 CONN.

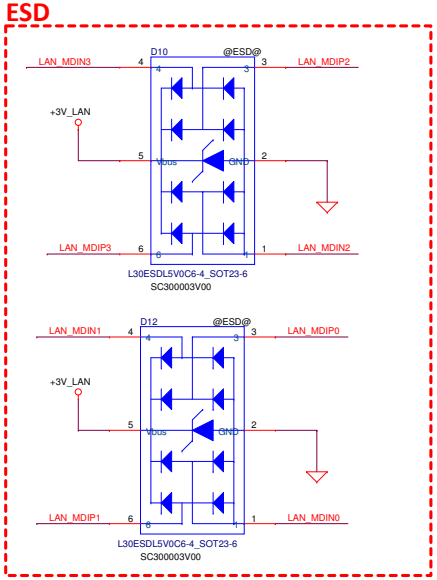


LAN Connector PN
DC23400DP00

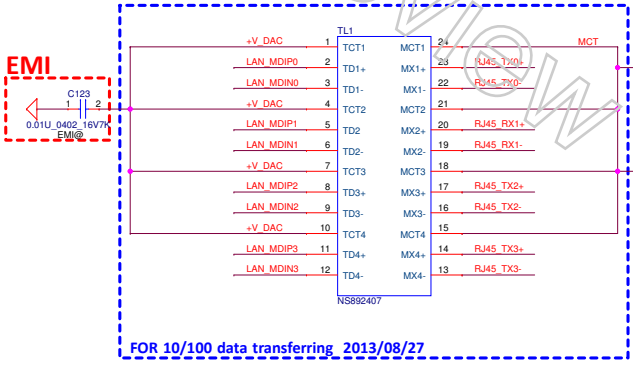




ESD

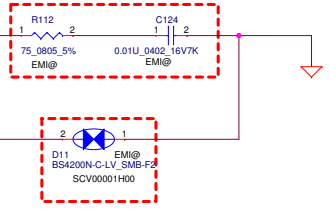


EMI



EMI

0726 change partnumber



EMI

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

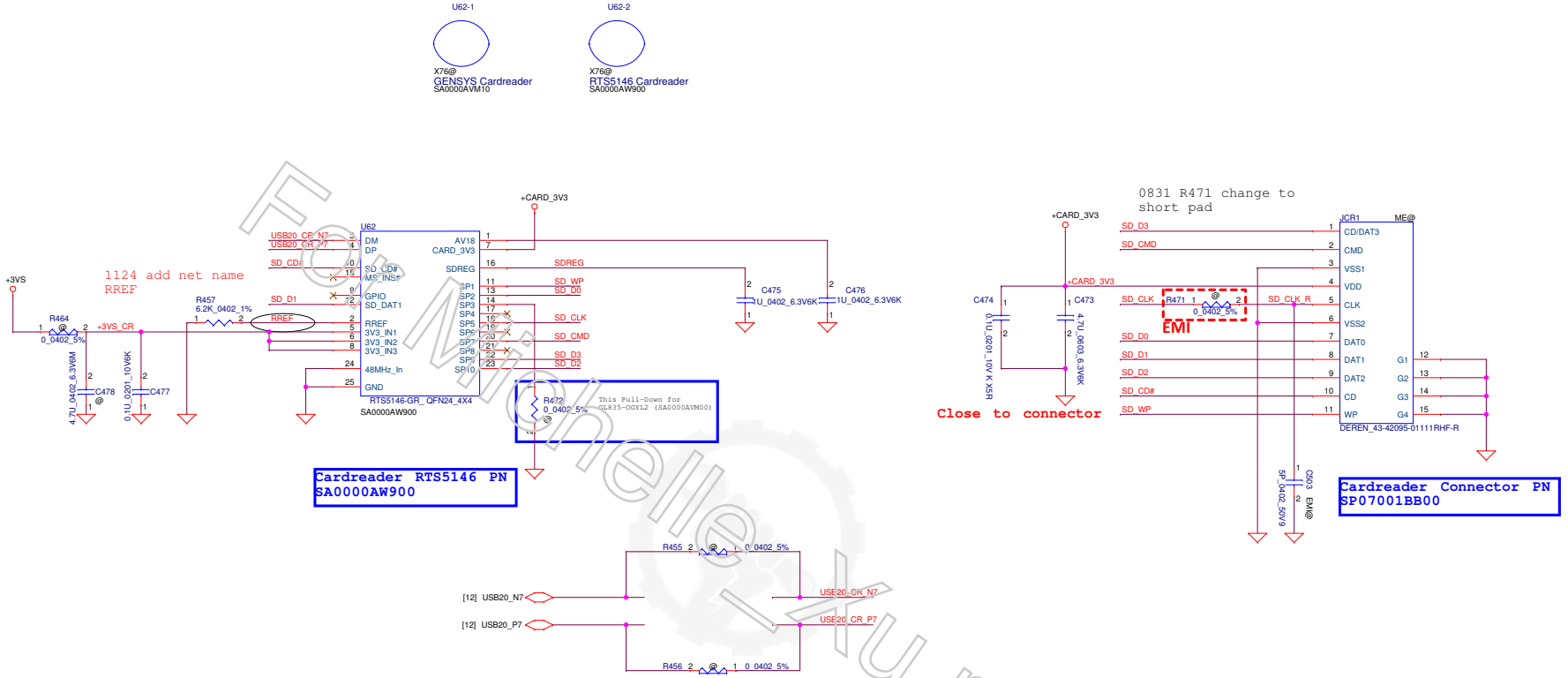
Compal Electronics, Inc.

Title: LAN_RTL8111H

Size	Document Number	Rev
C	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 36 of 66

Card Reader



Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: **CARDREADER**

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 37 of 66

1102 Remove

BLANK

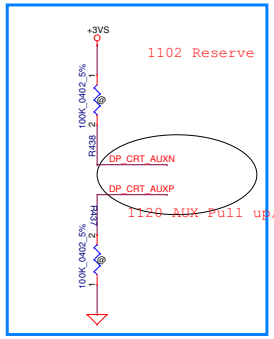
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: BLANK

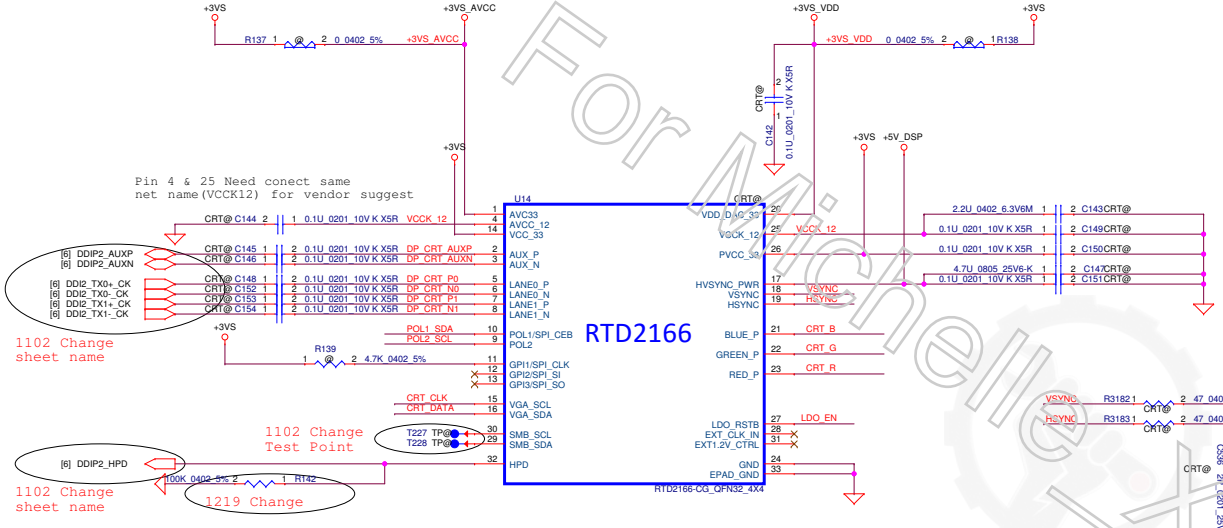
Size	Document Number	Rev
Custom	LA-F486P	0.3

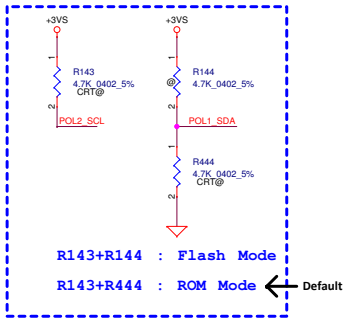
Date: Tuesday, December 19, 2017 | Sheet 38 of 66

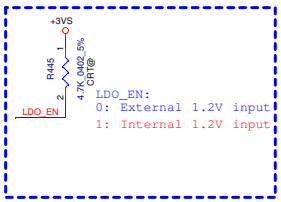


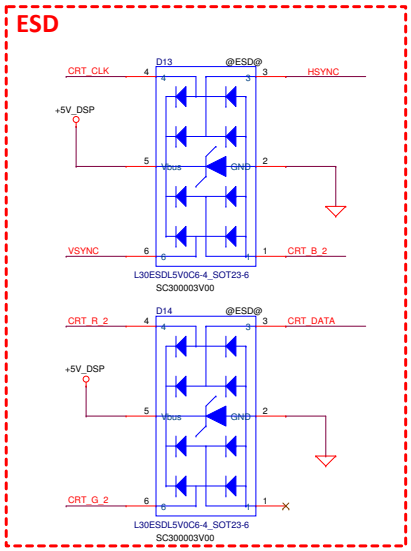
DDPB_AUXP DDPB_AUXN	Use a 75~200 nF AC coupling capacitor between the PCH and the connector. Intel recommends having a pull-up resistor of 100 KΩ on AUXN and 100 KΩ Pull-down on AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

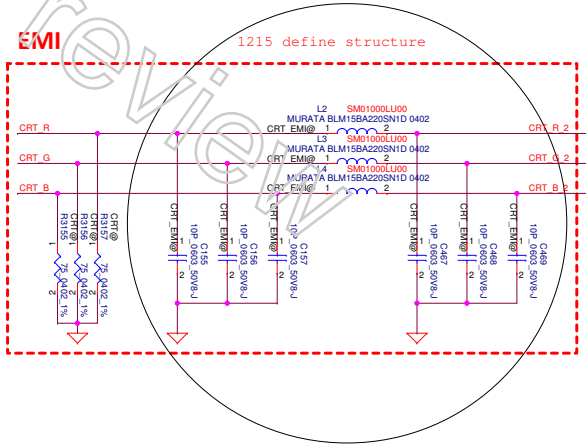
1120 AUX Pull up/down reserve modify after cap

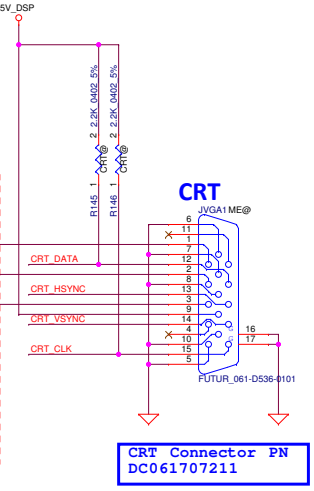












CRT Connector PN DC061707211

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.			
Title	DP to VGA - RTD2168		
Size: Custom	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 39 of 66		

1102 Remove

BLANK

Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: BLANK

Size	Document Number	Rev
Custom	LA-F486P	0.3

Date: Tuesday, December 19, 2017 | Sheet 40 of 63

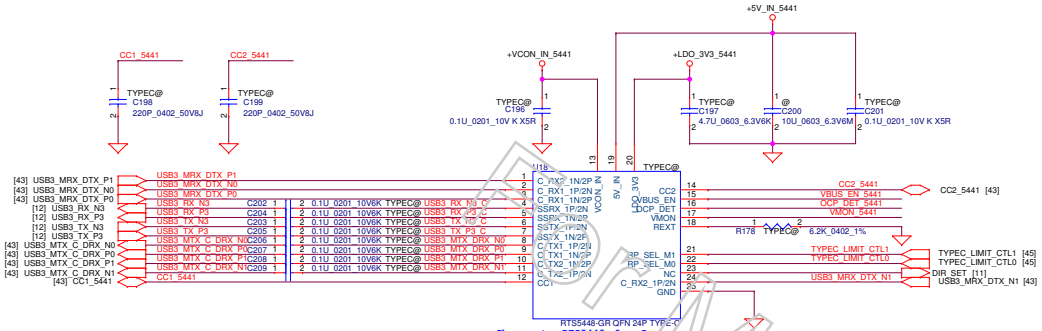
1102 Remove

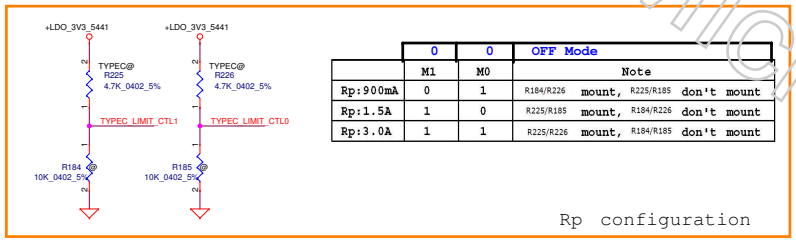
BLANK

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: BLANK

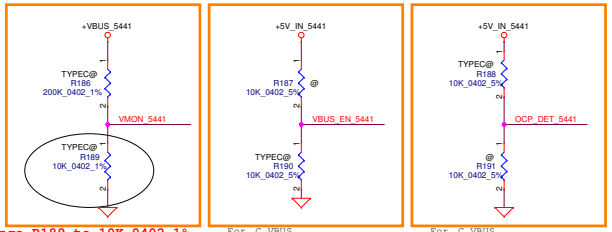
Size	Document Number	Rev
C	LA-F486P	0.3

Date: Tuesday, December 19, 2017 Sheet 41 of 66





0	0	OFF Mode	
	M1	M0	Note
Rp:900mA	0	1	R184/R226 mount, R225/R185 don't mount
Rp:1.5A	1	0	R225/R185 mount, R184/R226 don't mount
Rp:3.0A	1	1	R225/R226 mount, R184/R185 don't mount



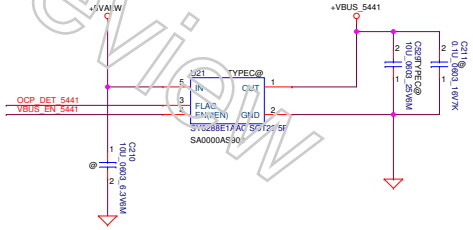
1127 Change R189 to 10K_0402_1%
follow reference schematic

Power switch enable pin	Note
Low Active	R190/R187 mount
High Active	R190 mount, R187 don't mount

Pull Up & Down
Pull Down

Power switch OCP pin	Note
Low Active	R191/R188 mount
High Active	R191 mount, R188 don't mount

Pull Up & Down
Pull Down



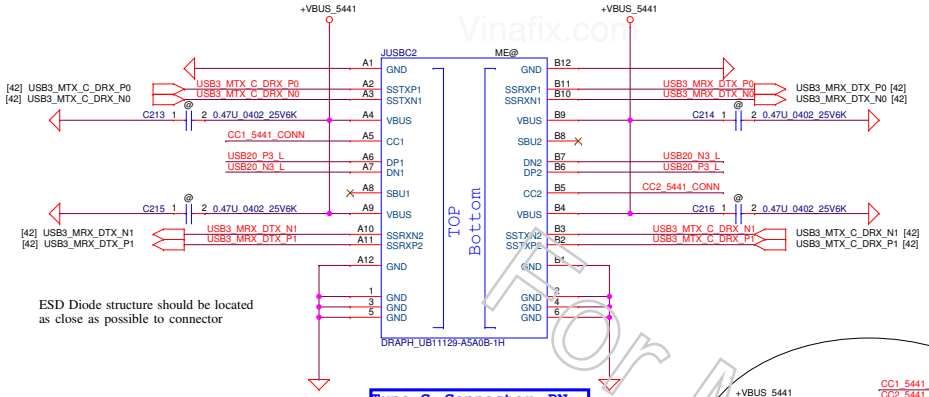
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: Type-C RTS5441

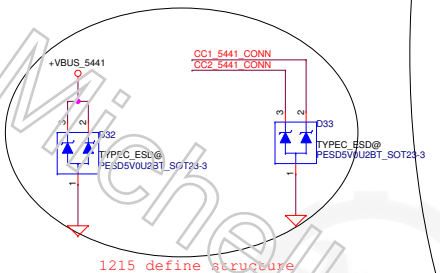
Size: Custom | Document Number: LA-F486P | Rev: 0.3

Date: Tuesday, December 19, 2017 | Sheet 42 of 63

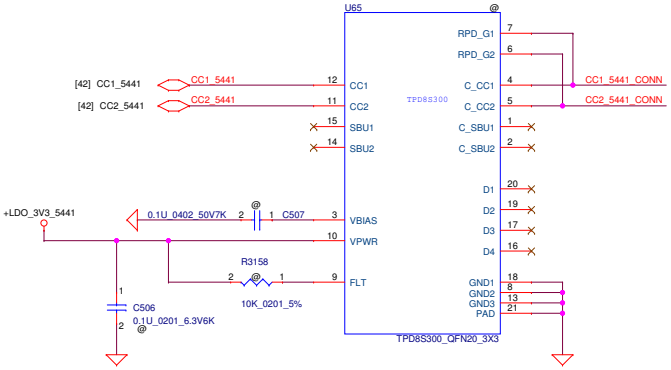


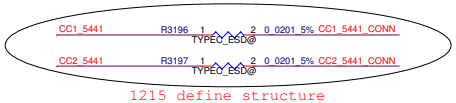
ESD Diode structure should be located as close as possible to connector

Type-C Connector PN TMP DC231707201



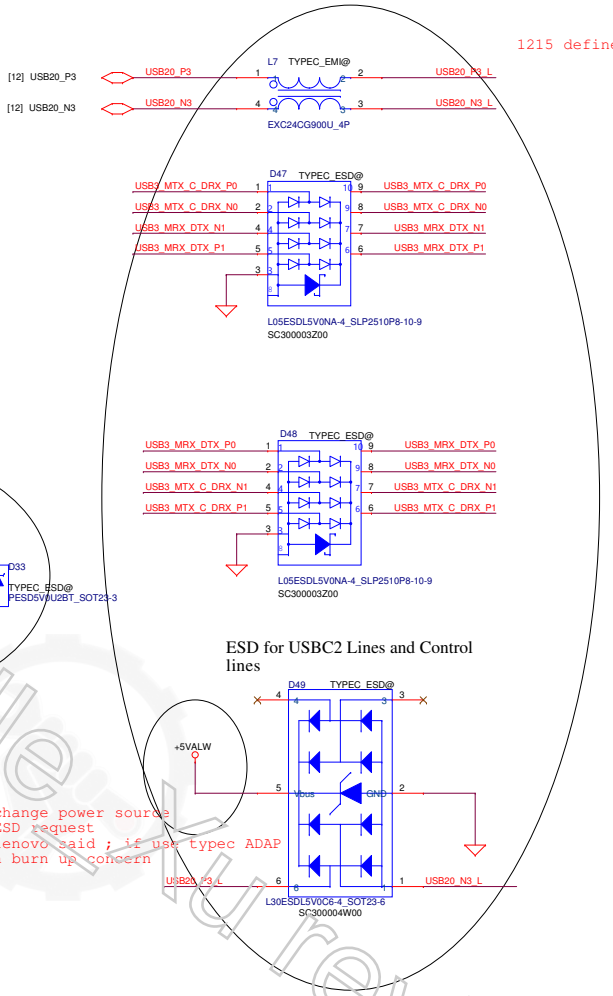
1215 define structure





1215 define structure

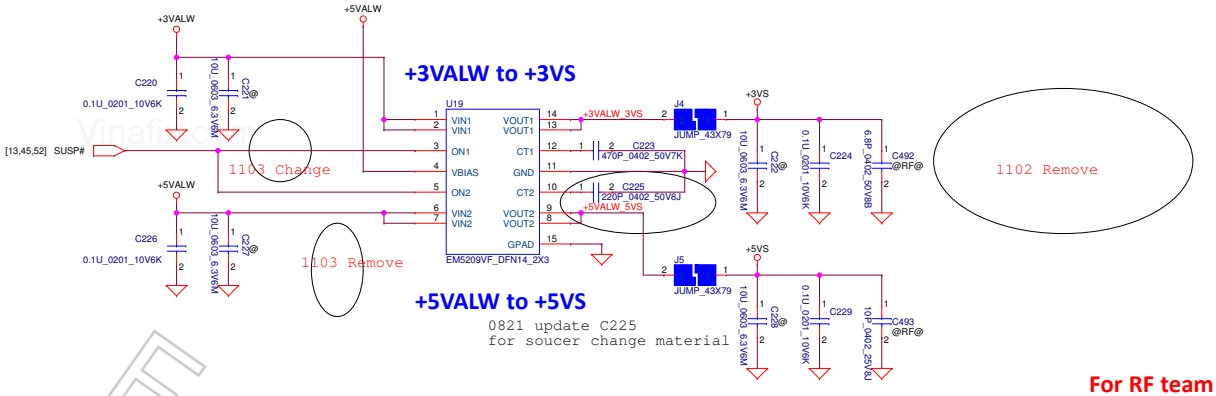
1214 change power source form ESD request that lenovo said ; if use typec ADAP have a burn up concern

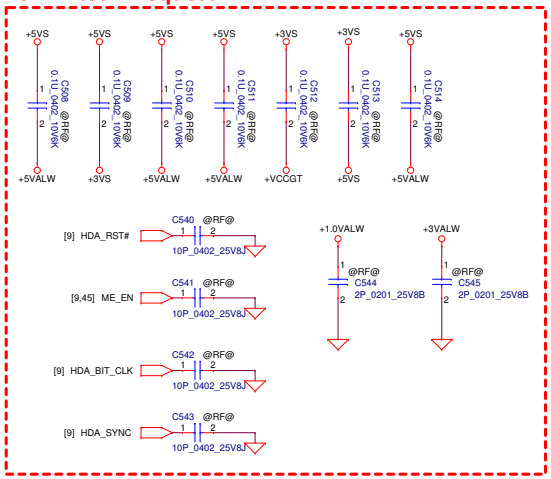


ESD for USBC2 Lines and Control lines

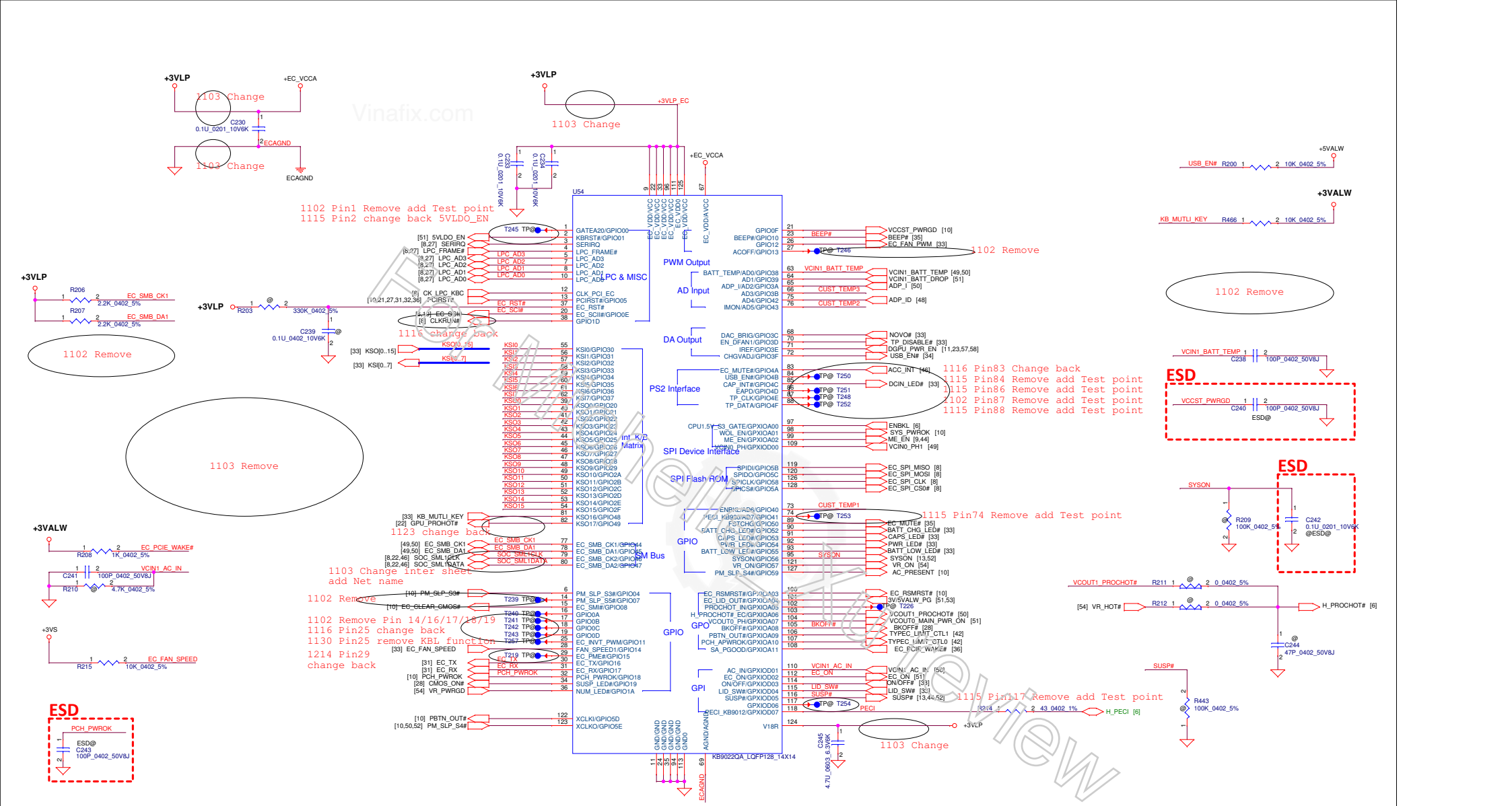
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.			
Title: Type-C RTS5441 CONN			
Size: C	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 43 of 63		





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/02	Deciphered Date	2018/08/02
Title	DC Interface		
Size C	Document Number LA-F486P		Rev 0.3
Date: Tuesday, December 19, 2017	Sheet 44 of 66		



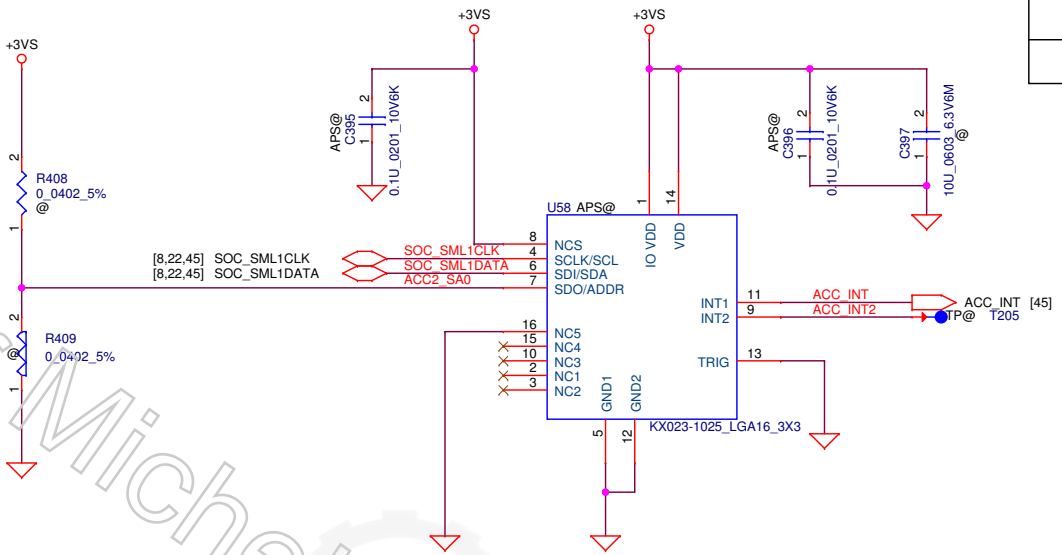
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.	
Title	EC_NPCE388N
Size	C
Document Number	LA-F486P
Rev	0.3
Date:	Tuesday, December 19, 2017
Sheet	45 of 66

APS G-Sensor

Kionix KX023-1025

SDO/ADDR	Address R/W
VDD	3Fh/3Eh
VSS	3Dh/3Ch



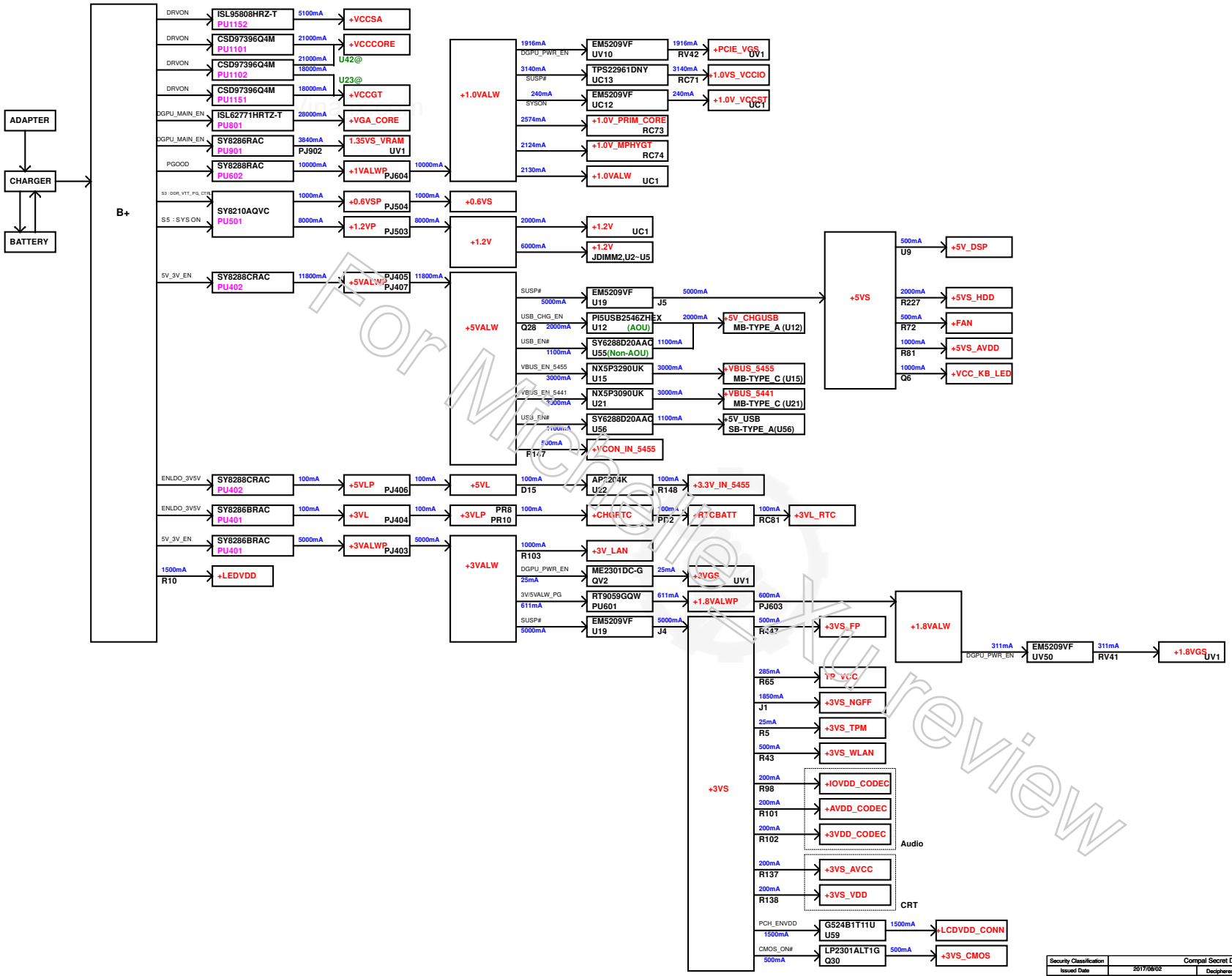
Security Classification	Compal Secret Data		
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Compal Electronics, Inc.

Title: **APS , ULTRABAY**

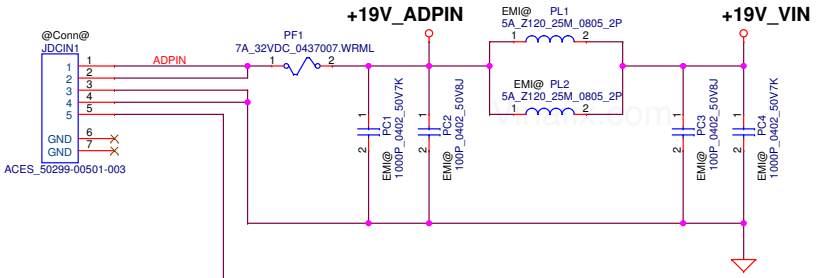
Size	Document Number	Rev
B	LA-F486P	0.3

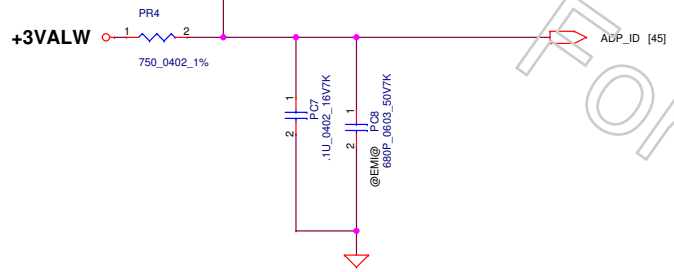
Date: Tuesday, December 19, 2017 Sheet 46 of 66

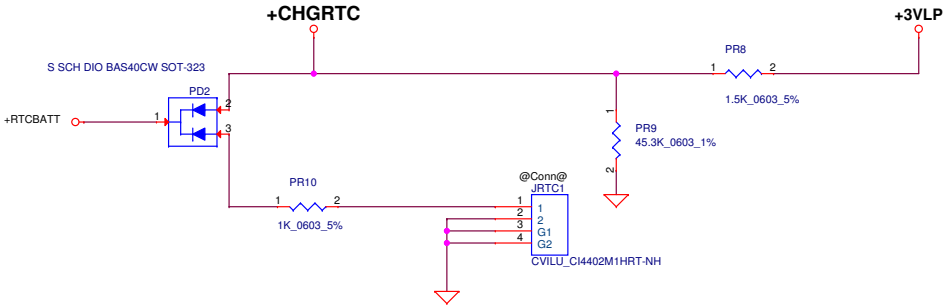


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/08/02	Deciphered Date	2018/08/02

Title	Power Rail		
Size: D	Document Number: LA-F486P		Rev: 0.3
Date: Tuesday, December 19, 2017	Sheet 47 of 85		







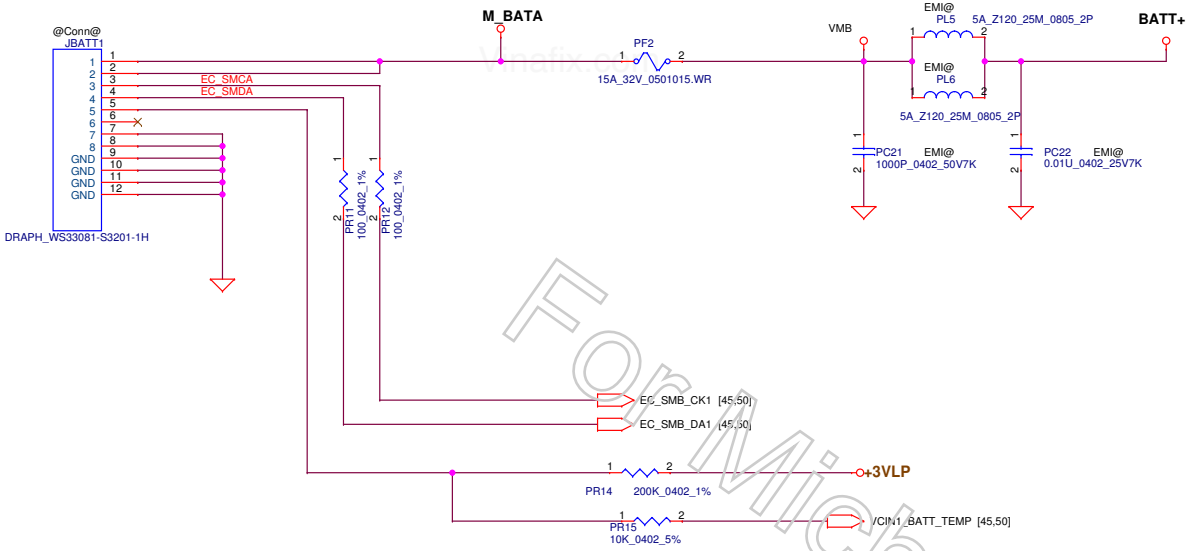
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

Compal Electronics, Inc.

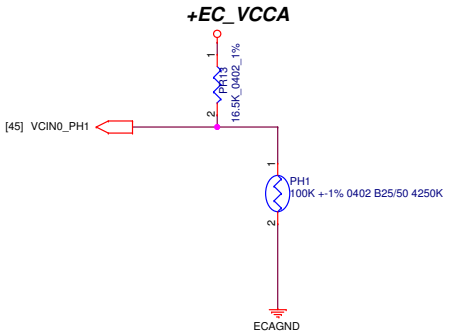
Title: **PWR-DCIN / Vin Detector**

Size	Document Number	Rev
Custom	VE	0.1

Date: Tuesday, December 19, 2017 | Sheet 48 of 59



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



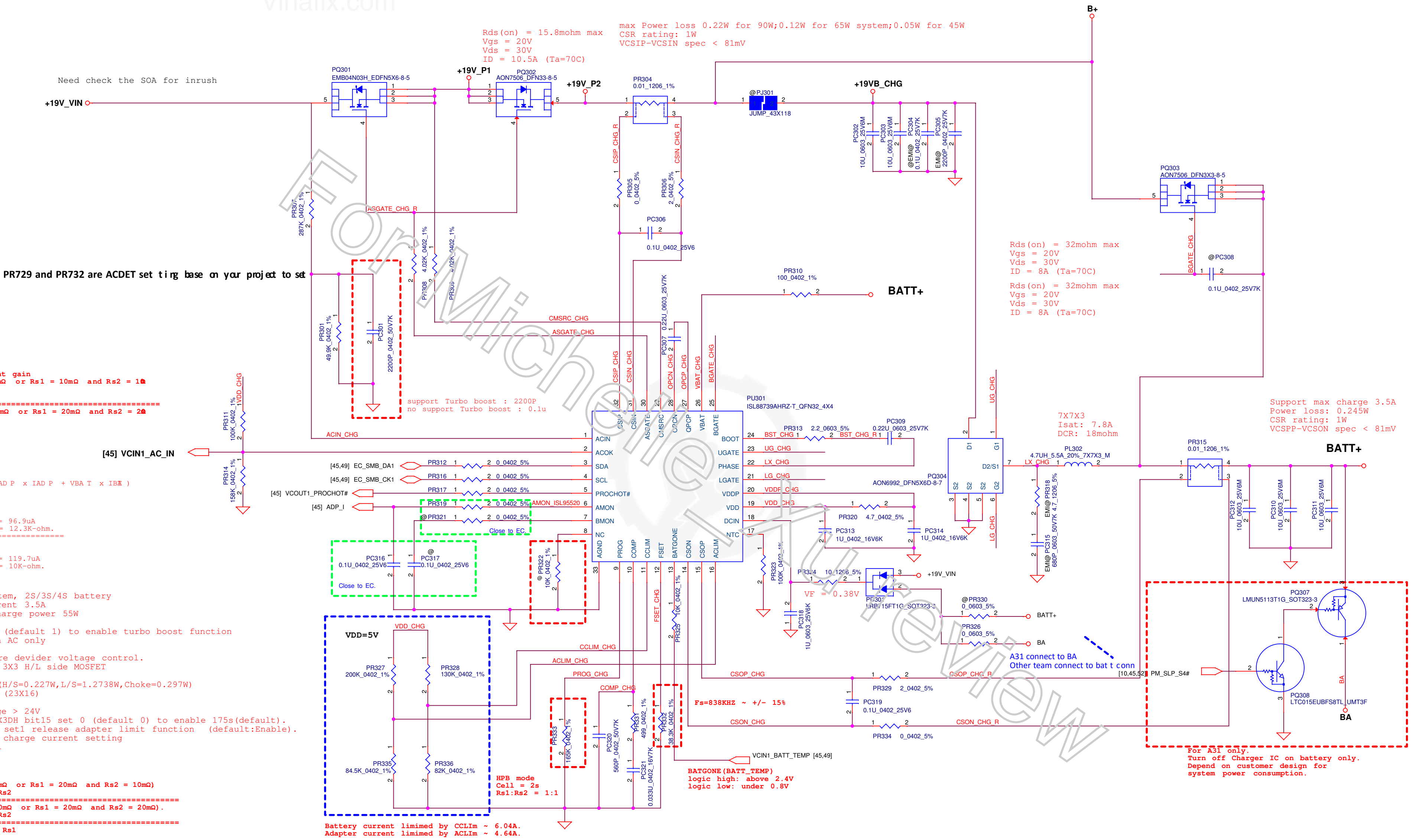
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	VE	0.1

Date: Tuesday, December 19, 2017 | Sheet 49 of 59



0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

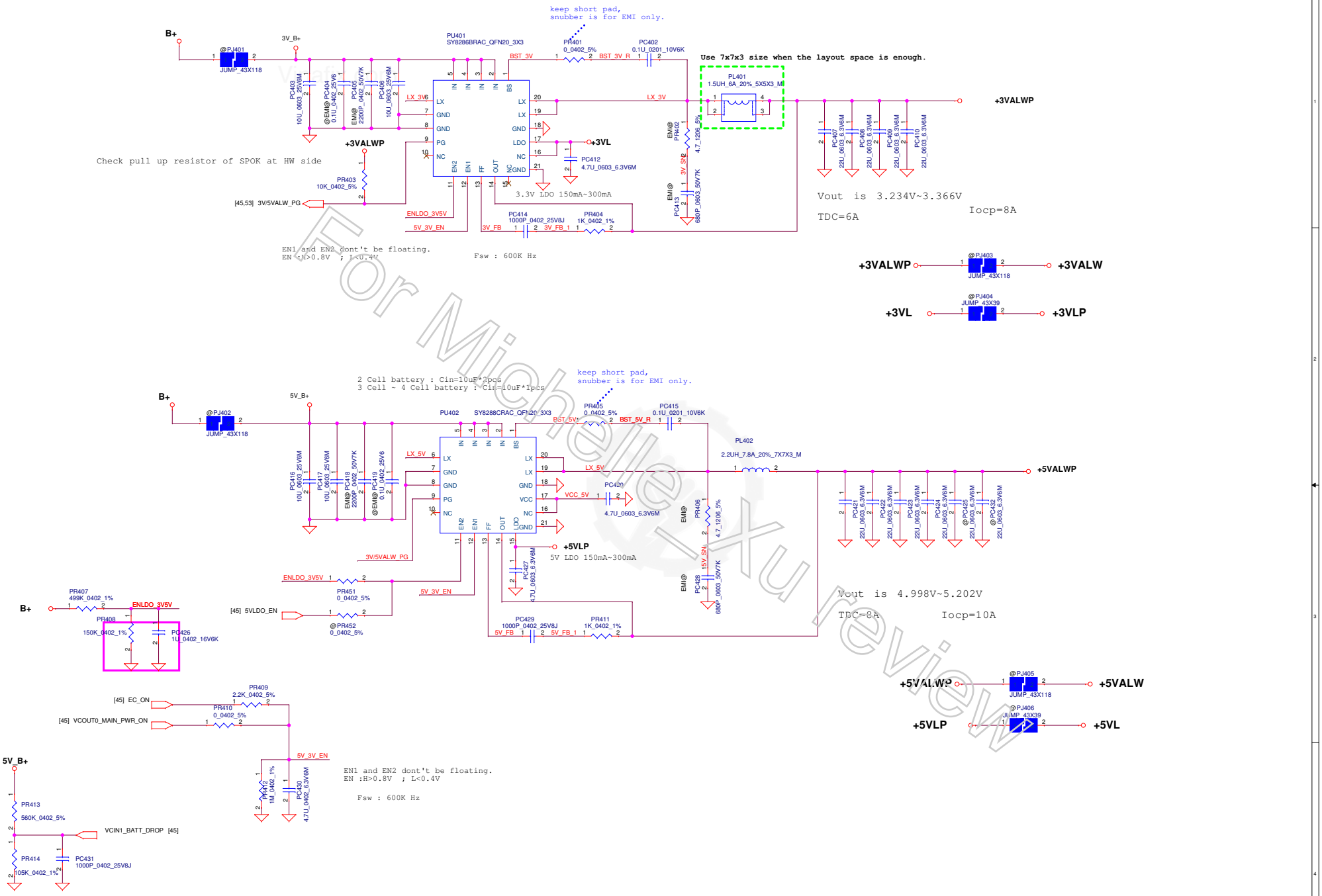
Ipsys = KPSYS x (VAD P x IAD P + VBA T x IBAT)
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
==============================
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : 0X3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ)
CC_LIM = VccLIM / 64 x Rs2
==
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ).
CC_LIM = VccLIM / 32 x Rs2
==
AC_LIM = Vac_LIM / 32 x Rs1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2017/11/15	Deciphered Date	2018/12/31	Title: PWR_CHARGER

Size | Document Number: VE | Rev 0.1
Date: Tuesday, December 19, 2017 | Sheet 50 of 59



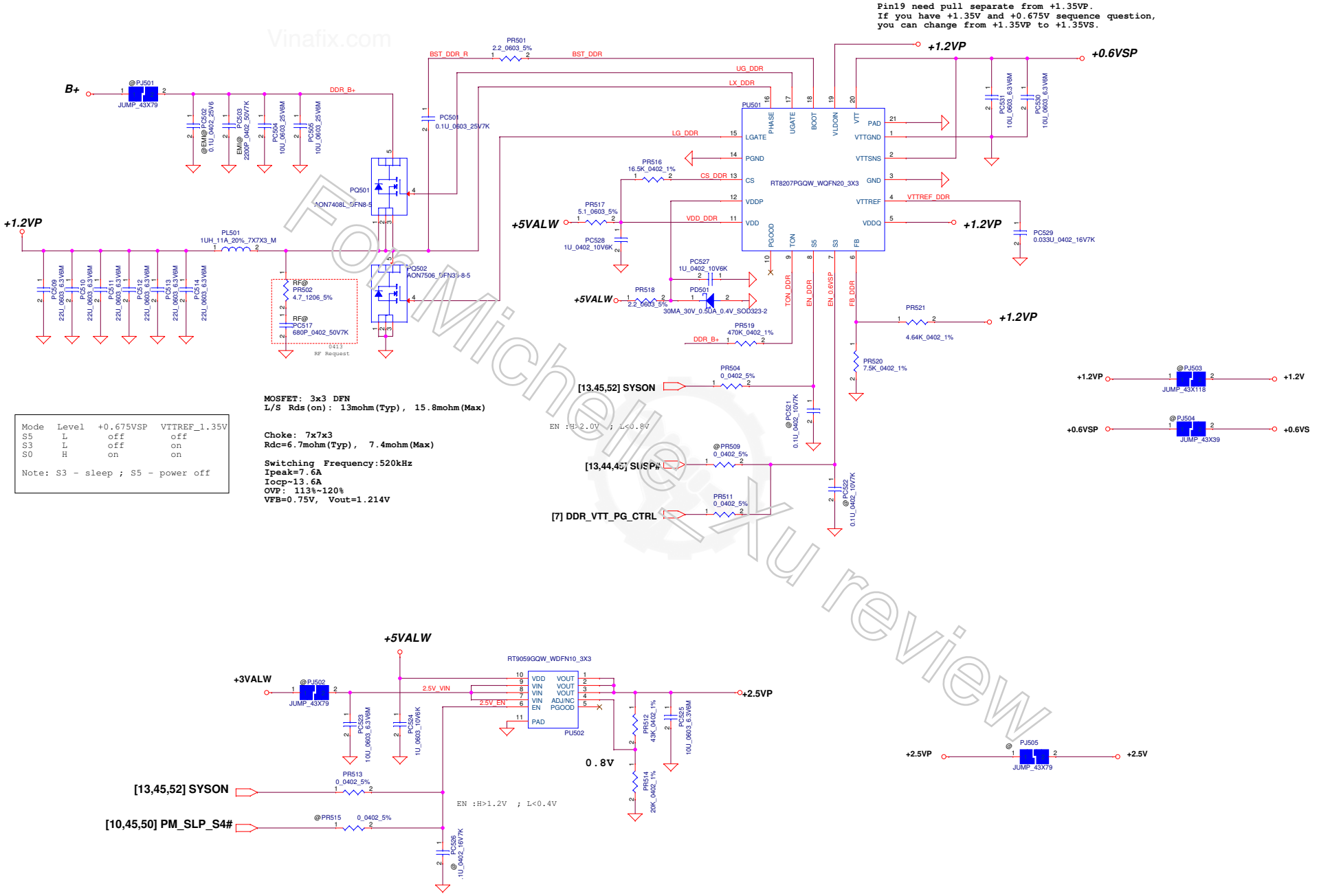
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

Compal Electronics, Inc.

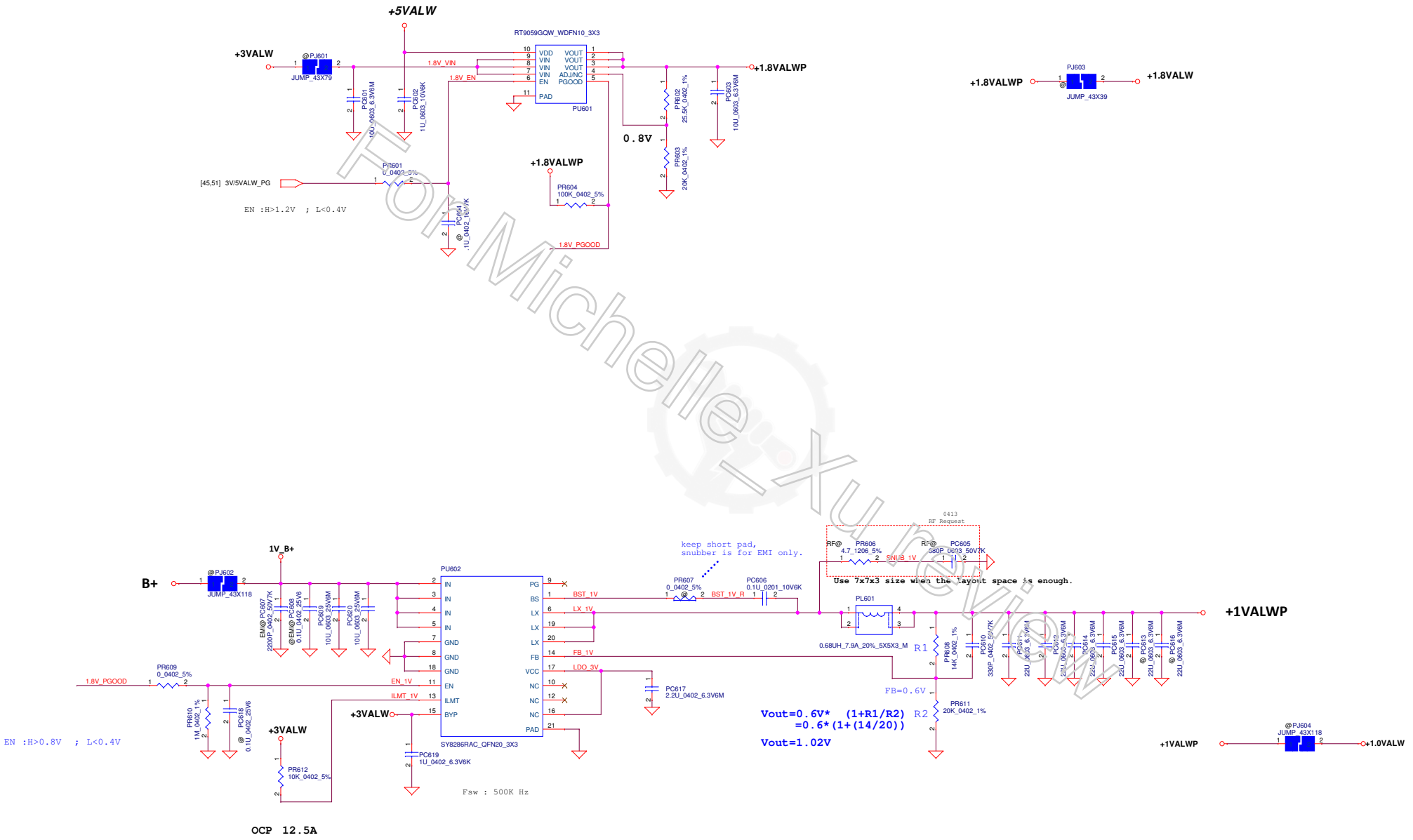
Title: PWR- +3VALW/+5VALW

Size	Document Number	Rev
C	VE	0.1

Date: Tuesday, December 19, 2017 Sheet 51 of 59

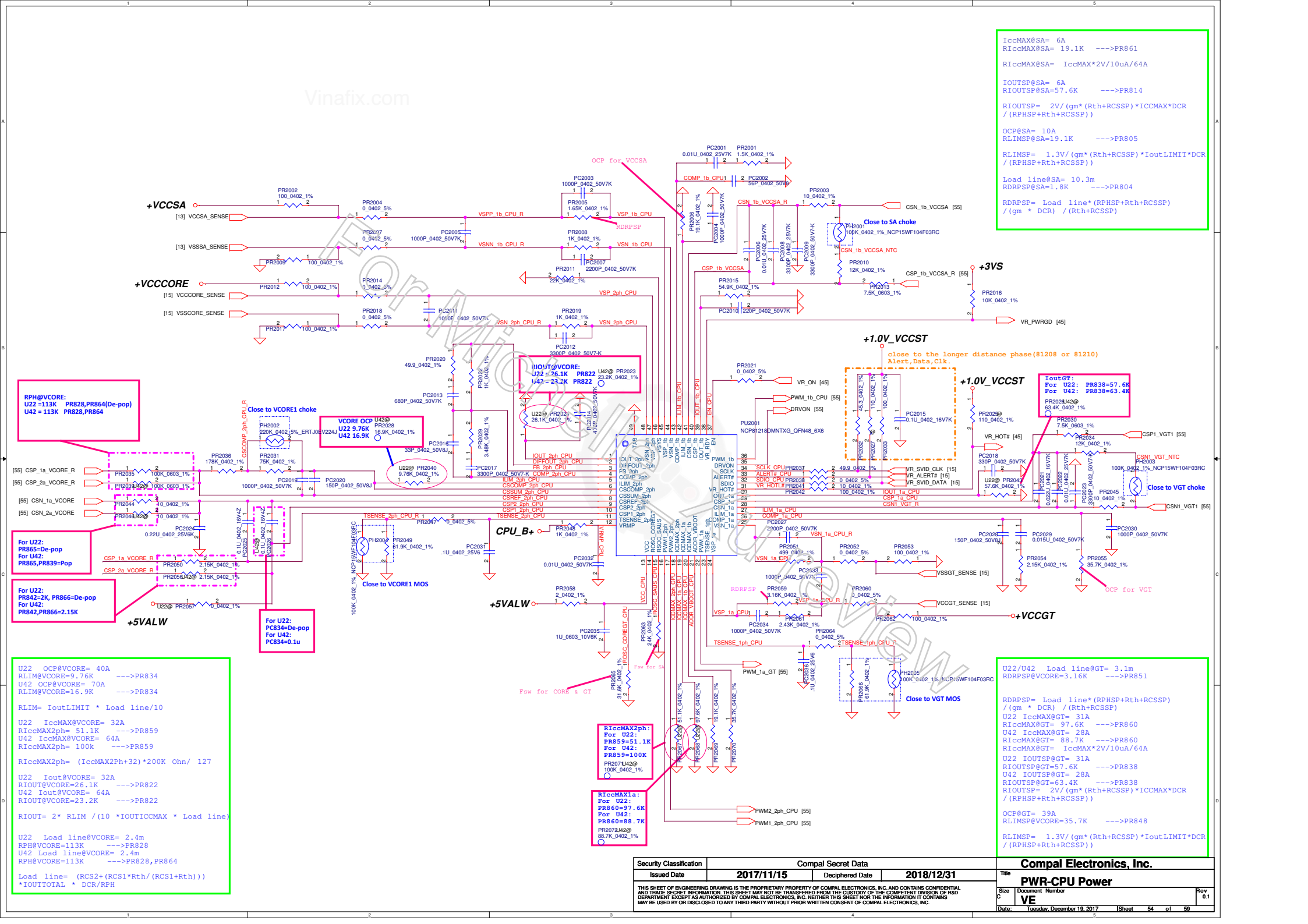


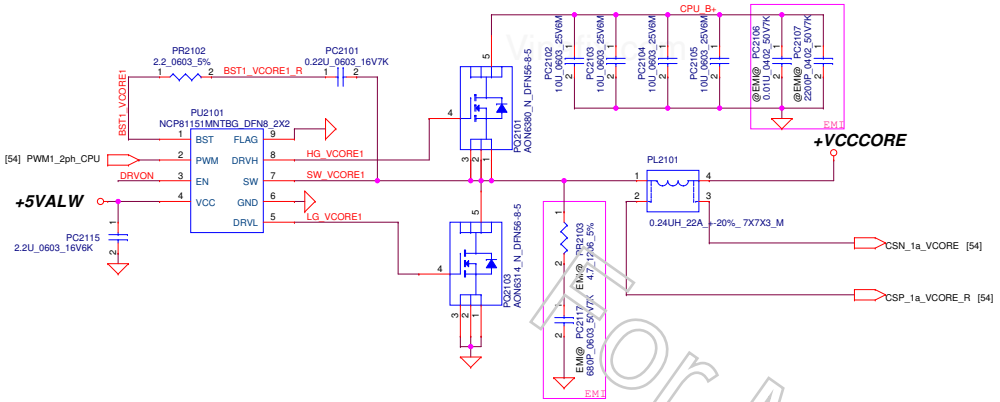
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/11/15	Deciphered Date	2018/12/31
Title	PWR- 1.2VP/0.6VSP/2.5VP		
Size C	Document Number VE		Rev 0.1
Date: Tuesday, December 19, 2017	Sheet 52 of 59		

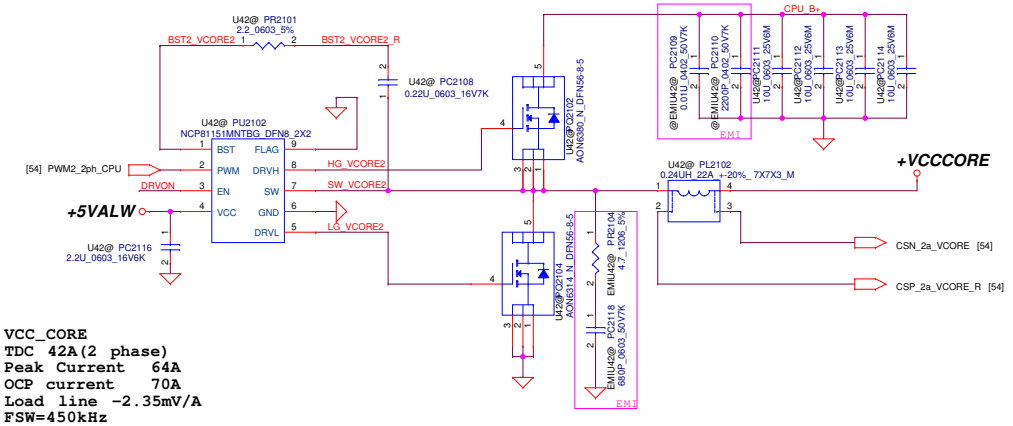


Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

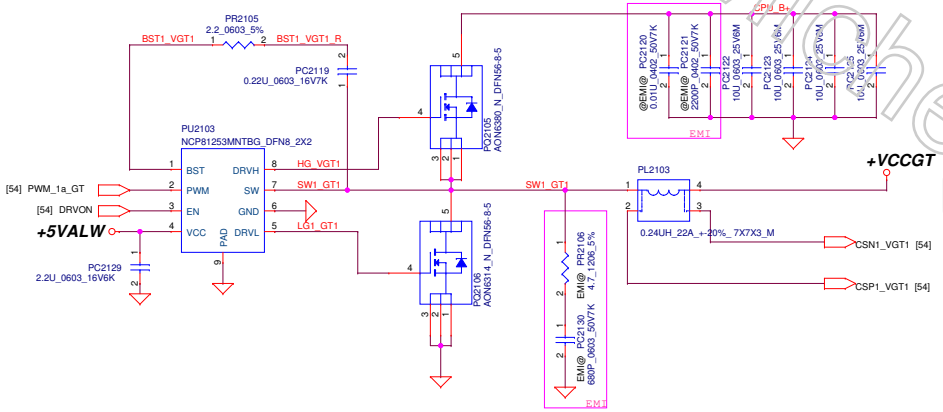
Compal Electronics, Inc.			
Title	PWR- 1.8VALWP/1VALWP		
Size C	Document Number VE		Rev 0.1
Date: Tuesday, December 19, 2017	Sheet 53 of 59		


IccMAX@SA= 6A
RIccMAX@SA= 19.1K ---->PR861
RIccMAX@SA= IccMAX*2V/10uA/64A
IOUTSP@SA= 6A
RIOUTSP@SA=57.6K ---->PR814
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))
OCP@SA= 10A
RLIMSP@SA=19.1K ---->PR805
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))
Load line@SA= 10.3m
RDRPSP@SA=1.8K ---->PR804
RDRPSP= Load line*(RPHSP+Rth+RCSSP) /(gm * DCR) /(Rth+RCSSP)
+VCCSA
+VCCCORE
+3VS
+1.0V_VCCST
close to the longer distance phase(81208 or 81210)
Alert,Data,Clk.
IoutGT:
For U22: PR838=57.6K
For U42: PR838=63.4K
RPH@VCORE:
U22 =113K PR828,PR864(De-pop)
U42 = 113K PR828,PR864
Close to VCORE1 choke
VCORE OCP U42@
U22 9.76K PR2028
U42 16.9K
IOUT@VCORE:
U22 = 26.1K PR822
U42 = 23.2K PR822
Close to SA choke
Close to VGT choke
Close to VCORE1 MOS
Close to VGT MOS
OCP for VCCSA
OCP for VGT
CPU_B+
+5VALW
+VCCGT
RDRPSP
Fsw for CORE & GT
For U22:
PR865=De-pop
For U42:
PR865,PR839=Pop
For U22:
PR842=2K, PR866=De-pop
For U42:
PR842,PR866=2.15K
For U22:
PC834=De-pop
For U42:
PC834=0.1u
RIccMAX2ph:
For U22:
PR859=51.1K
For U42:
PR859=100K
RIccMAX1a:
For U22:
PR860=97.6K
For U42:
PR860=88.7K
U22 OCP@VCORE= 40A
RLIM@VCORE=9.76K ---->PR834
U42 OCP@VCORE= 70A
RLIM@VCORE=16.9K ---->PR834
RLIM= IoutLIMIT * Load line/10
U22 IccMAX@VCORE= 32A
RIccMAX2ph= 51.1K ---->PR859
U42 IccMAX@VCORE= 64A
RIccMAX2ph= 100k ---->PR859
RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127
U22 Iout@VCORE= 32A
RIOUT@VCORE=26.1K ---->PR822
U42 Iout@VCORE= 64A
RIOUT@VCORE=23.2K ---->PR822
RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)
U22 Load line@VCORE= 2.4m
RPH@VCORE=113K ---->PR828
U42 Load line@VCORE= 2.4m
RPH@VCORE=113K ---->PR828,PR864
Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH
U22/U42 Load line@GT= 3.1m
RDRPSP@VCORE=3.16K ---->PR851
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)
U22 IccMAX@GT= 31A
RIccMAX@GT= 97.6K ---->PR860
U42 IccMAX@GT= 28A
RIccMAX@GT= 88.7K ---->PR860
RIccMAX@GT= IccMAX*2V/10uA/64A
U22 IOUTSP@GT= 31A
RIOUTSP@GT=57.6K ---->PR838
U42 IOUTSP@GT= 28A
RIOUTSP@GT=63.4K ---->PR838
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))
OCP@GT= 39A
RLIMSP@VCORE=35.7K ---->PR848
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))
Security Classification
Compal Secret Data
Issued Date
2017/11/15
Deciphered Date
2018/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
PWR-CPU Power
Size
C
Document Number
VE
Rev
0.1
Date: Tuesday, December 19, 2017
Sheet 54 of 59

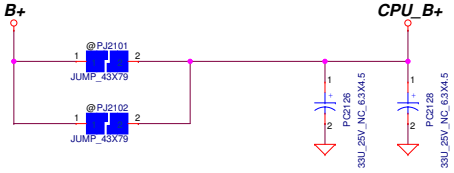


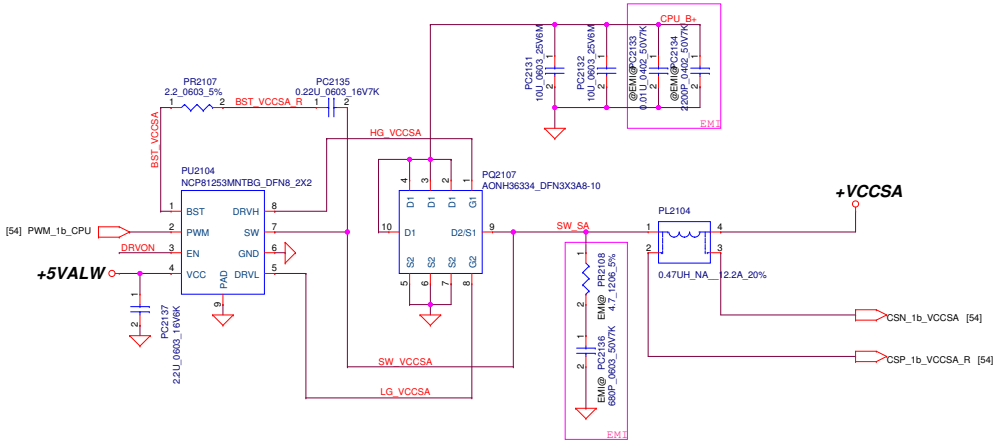


VCC_CORE
TDC 42A(2 phase)
Peak Current 64A
OCP current 70A
Load line -2.35mV/A
FSW=450kHz
DCR 0.97mohm +/-5%
H/S Rds(on) :5~15 mohm
L/S Rds(on) :3.2~5 mohm



VCCGT(1 phase)
TDC 12A(1H1L)
Peak Current 31A
OCP current 39A
Load line -3.1mV/A (KBL U-22)
FSW=450kHz
DCR 0.97mohm +/-5%
H/S Rds(on) :5~15 mohm
L/S Rds(on) :3.2~5 mohm





VCCSA
TDC 4A(1H1L)
Peak Current 6A
OCP current 10A
Load line -10.3mV/A
FSW=450kHz
DCR 6.2 mohm +/-5%
H/S Rds(on) :10.2~19.2 mohm
L/S Rds(on) :7.7~14 mohm

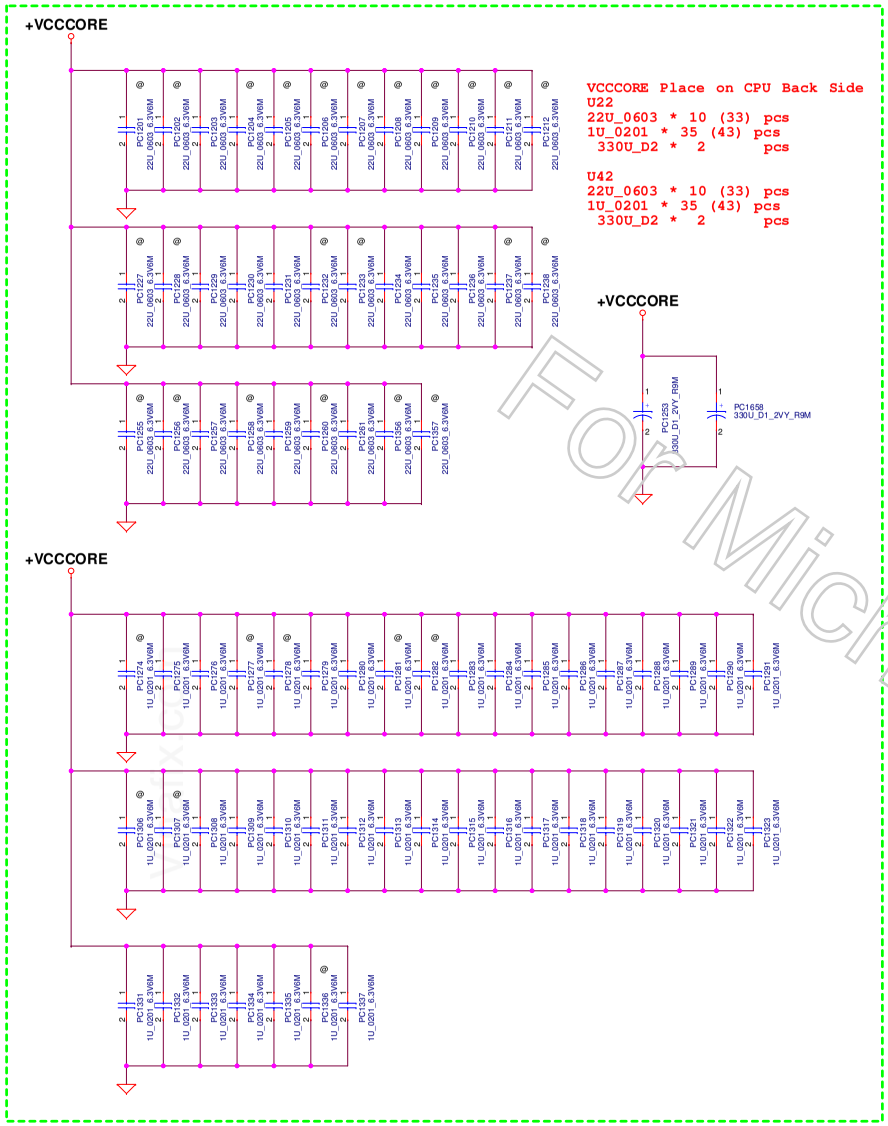
Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

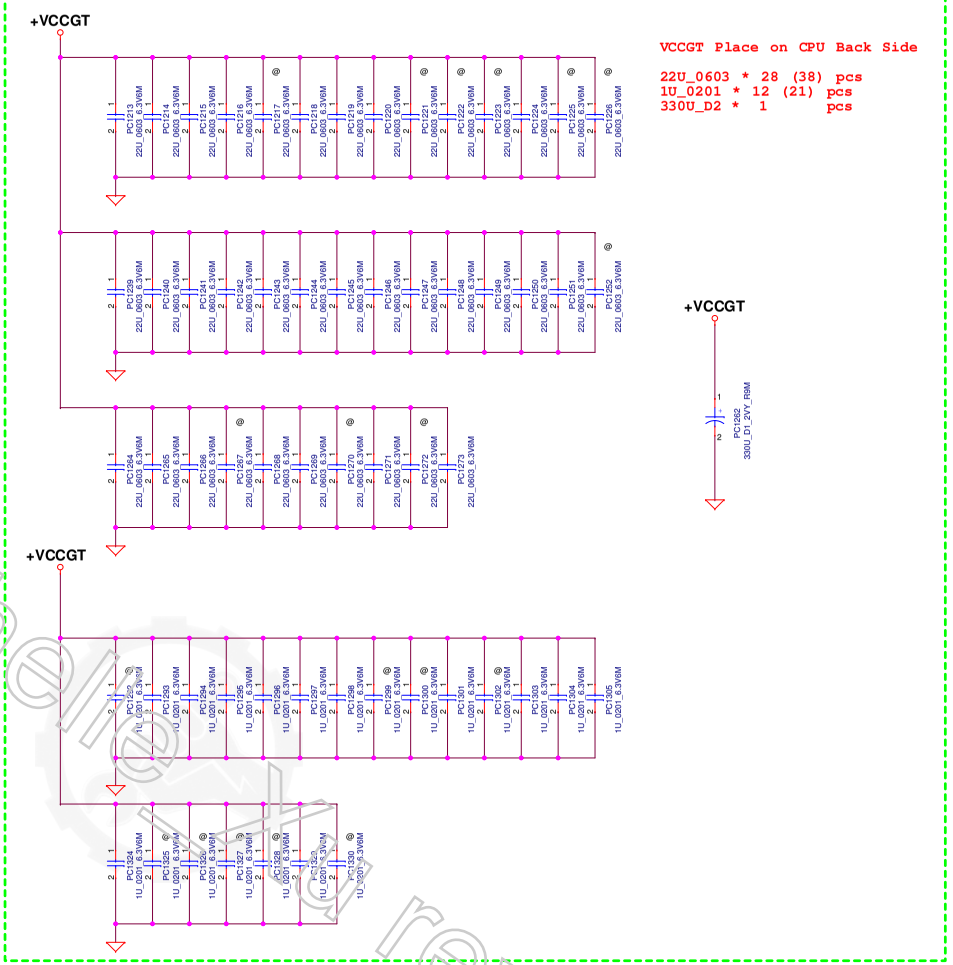
Compal Electronics, Inc.

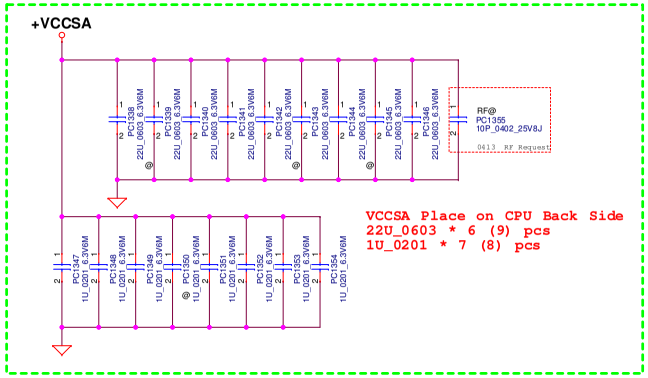
Title: PWR-CPU Power Stages

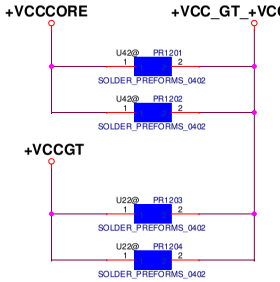
Size	Document Number	Rev
C	VE	0.1

Date: Tuesday, December 19, 2017 Sheet 55 of 59





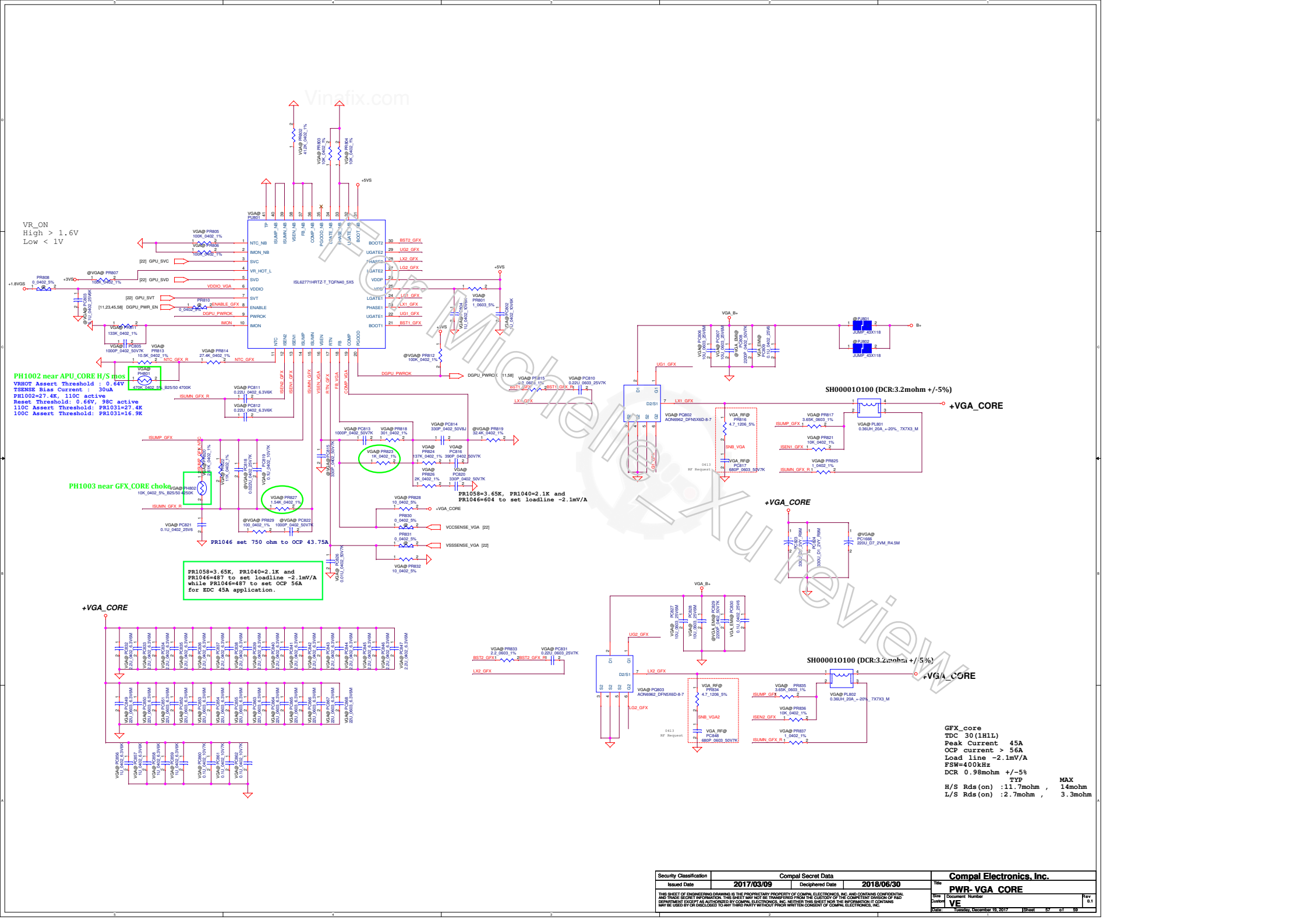




VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6), VCC_IAGT out cap(36.7)

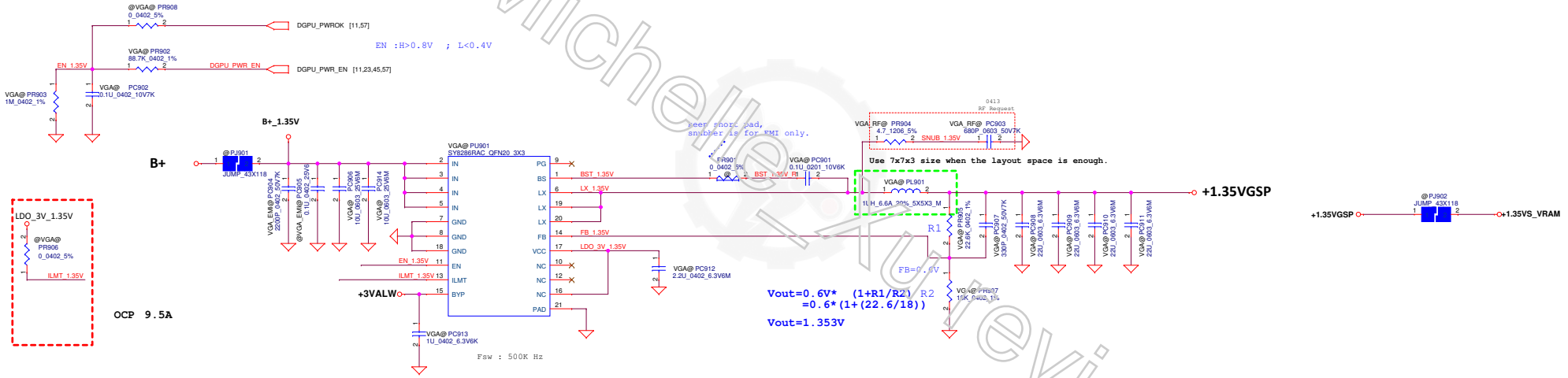
Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.			
Title	PWR- CPU BACK SIDE MLCC		
Size: Custom	Document Number: VE		Rev: 0.1
Date: Tuesday, December 19, 2017	Sheet 56 of 59		



Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.			
Title	PWR- VGA_CORE		
Size	Document Number		Rev
Custom	VE		0.1
Date:	Tuesday, December 19, 2017	Sheet	57 of 59



Security Classification	Compal Secret Data		
Issued Date	2017/03/09	Deciphered Date	2018/06/30

Compal Electronics, Inc.

Title: **PWR- 1.35VRAM**

Size	Document Number	Rev
Custom	VE	0.1

Date: Tuesday, December 19, 2017 | Sheet 58 of 59

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					

Security Classification	Compal Secret Data		
Issued Date	2017/11/15	Deciphered Date	2018/12/31

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size	Document Number	Rev
C	LA-E981P	0.1

Date: Tuesday, December 19, 2017 Sheet 59 of 59